Design and Performance of a 200 kHz All-SiC JFET Current Source Converter

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***Abstract*—Silicon carbide (SiC) switching devices have been widely discussed in power electronics due to their desirable properties and are believed to set new standards in efficiency, switching behavior, and power density for state-of-the-art converter systems. In this paper the design, construction, and performance of a 3 kVA All-SiC Current Source Converter (CSC) also known as Current DC-Link Back-to-Back Converter (CLBBC), is presented. CSC topologies have been successfully used for many years for high power applications. However, for low power range converter systems they could not compete with Voltage Source Converter (VSC) topologies with capacitors in the DC-link, since the link inductor has always been a physically large and heavy component due to the comparatively low switching frequencies of conventional high blocking voltage silicon devices. New SiC switches such as the JFET, which are providing simultaneously high voltage blocking, low switching losses, and low on-state resistance, offer new possibilities and allow for implementing a high switching frequency CLBBC and thus reducing size and weight of the DC-link inductor. The prototype CLBBC has been designed specifically for latest generation 1200 V, 6 A SiC JFETs for a target switching frequency of 200 kHz.**

I. Introduction

Bidirectional AC-AC power converters with active front-end are capable of providing simultaneous amplitude and frequency transformation of three-phase voltages, sinusoidal input currents, and unity power factor at the converter input. They are typically applied in electrical drives and frequency changers. These power converters can be divided into two basic categories; those that have an energy storage element in the interconnecting DC-link and those which have no energy storage elements, such as the Matrix Converter (MC) [1], [2]. For the converters with DC energy storage the component can be either a capacitor, as is in the case of the commonly used Voltage DC-Link Back-to-Back Converter (VLBBC), or an inductor, as in the case of a Current DC-Link Back-to-Back Converter (CLBBC) shown in Fig. 1. The CLBBC is a three-phase AC-AC, bidirectional power flow converter with a current DC-link, interconnecting the converter input and output stage with an inductor [3]–[5]. Traditionally, the VLBBC is the preferred converter type since the per volume energy storage density is much higher in a capacitor than in an equivalent inductor. In the CLBBC the inductive storage element typically has had a high inductance value and consequently has been physically large, mainly due to comparatively low switching frequency of conventional high blocking voltage silicon devices (e.g. 1200 V RB-IGBTs). Furthermore, the VLBBC has a higher efficiency compared to the CLBBC, as it has no additional series diodes in the individual bridge-legs. However, a significant advantage of the CLBBC, inherently given by its topology, is that the output voltage is sinusoidal, rather than pulsed as for a VLBBC without additional output filter. Furthermore, thermal aging of a DC-link inductor is significantly lower compared with a DC-link capacitor.

New wide band-gap power devices, such as SiC JFETs, are offering the possibility of high blocking voltage, low on-state resistance, and high switching frequency capability. Because of the normally-on characteristic of the SiC JFET, the device conducts the current when zero voltage or a slightly positive voltage is applied to the gate. In order to turn-off the devices, a negative gate-source voltage is required. The question that arises out of the SiC JFETs' properties is on whether and how they can be best applied for bidirectional AC-AC converter

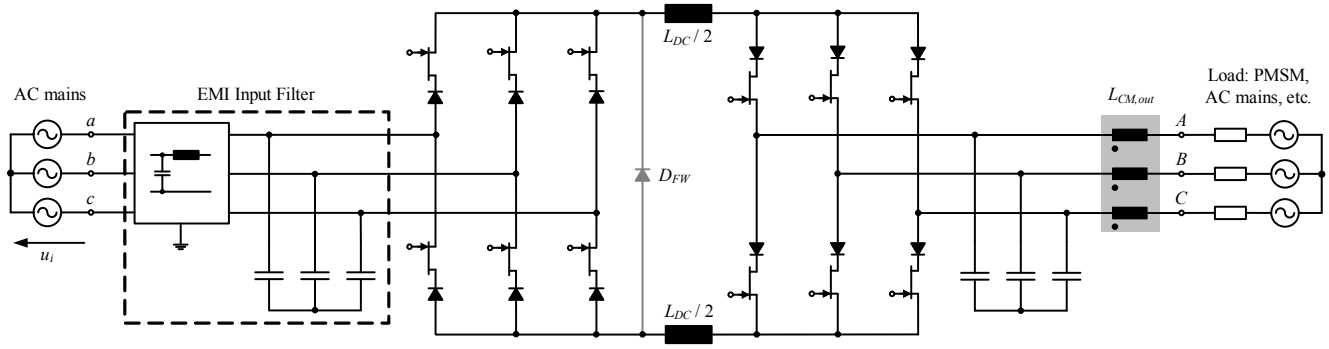

Fig. 1. Schematic of the All-SiC JFET Current DC-Link Back-to-Back Converter (CLBBC). If only unidirectional power flow operation is required the additional free-wheeling diode D_{FW} can be implemented in order to reduce conduction losses.

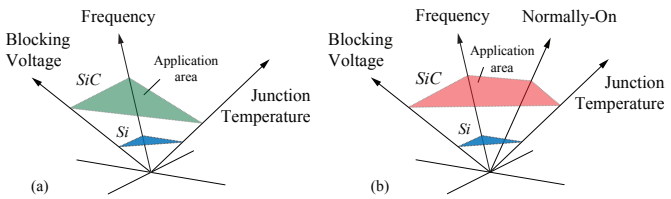

Fig. 2. Benefits of utilizing SiC instead of Si power devices: (a) in general and (b) specifically for the All-SiC JFET CLBBC.

system, or even better to find a topology which favors the SiC JFET properties. The motivation for this work is not to simply replace conventional Si devices by SiC but to advantageously match the device properties with the converter topology. Therefore, different converter topologies have been investigated in terms of power semiconductor requirements and suitability for utilizing SiC JFETs.

This paper firstly presents in Section II the available SiC semiconductor devices that determine the power specifications of the CLBBC, followed by the design and the physical construction of the overall converter system. In Section III the performance of the SiC JFET CLBBC, operating at a switching frequency of 200 kHz, is demonstrated including characteristic input and output waveforms, THD, achievable efficiency, and EMI. A brief performance comparison between the All-SiC JFET CLBBC and an All-SiC JFET Indirect Matrix Converter (IMC), operating both at 200 kHz, is described in Section IV. Finally, the conclusions and an outlook for future research are given in Section V.

II. Design and Construction of the CLBBC

A. Suitability of CLBBC Topology for SiC JFETs

The topology evaluation and analysis has shown that the best match between power semiconductor and converter topology can be achieved with a current source type converter, in this case a CLBBC, as it naturally favors the normally-on characteristic of the SiC JFETs. These devices are particularly advantageous for the CLBBC in terms of simplicity of implementation, fault tolerance, and general ruggedness. Under fault conditions, such as for example gate driver supply power loss, a natural free-wheeling path is provided for the DC-link inductor current as the JFETs become conducting. An additional advantage is that a phase-leg short circuit can not occur such as in the case of a MC or a VSC. An equivalent 3 kVA SiC JFET VLBBC, optimized for low DC-link capacitance of e.g. 20 μF and a nominal DC-link voltage of 700 V, has a stored link energy of 4.9 J, which is sufficient to thermally destroy the SiC JFETs in case of a phase-leg shoot-through.

Similar to the MC and VLBBC, a proper start-up procedure for the CLBBC must be followed in order to avoid an excessively high DC-link current, when the power circuit is connected to the mains before the JFETs are blocking. When input power is first applied, relays in line with the input EMI filter prevent the voltage from being instantaneously applied to the power switches. Once the auxiliary power supply is running and the controller verifies correct gate driver operation, then the relays can be energized and the CLBBC operated.

TABLE I
SiC Power Device Parameters

Quantity	***Value***
SiC JFET voltage rating	1200 V
SiC JFET DC current rating	6 A
SiC JFET on-resistance $r_{DS,on}$ at $I_{DS} = 6\,\text{A}$, $T_J = 125\,^\circ\text{C}$	0.55 Ω
Voltage drop across body diode, JFET off $I_{DS} = -6\,\text{A}$, $T_J = 125\,^\circ\text{C}$	4.6 V
Voltage drop across body diode, JFET on $I_{DS} = -6\,\text{A}$, $T_J = 125\,^\circ\text{C}$	2.8 V
Gate-source capacitance C_{GS} at $V_{DS} = 40\,\text{V}$, $V_{GS} = V_{\text{pinchoff}}$	≈ 0.5 nF
Input capacitance C_{GS} parallel C_{GD} at $V_{DS} = 0\,\text{V}$, $V_{GS} = V_{\text{pinchoff}}$	≈ 1.0 nF
SiC Schottky diode voltage rating	1200 V
SiC Schottky diode DC current rating	10 A
SiC Schottky diode forward voltage drop at $I_F = 6\,\text{A}$, $T_J = 125\,^\circ\text{C}$	1.6 V
SiC Schottky diode total capacitive charge	61 nC

Voltage drop, resistance, and capacitance values are based on sample measurement data.

The application of SiC power semiconductor devices generally broadens the overall converter system application area in terms of switching frequency, blocking voltage, and junction temperature, as shown in Fig. 2. For the CLBBC the normally-on characteristic of the SiC JFET provides an additional benefit in terms of system failure behavior and pinpoints the importance of matching semiconductor properties to the converter topology.

B. Power Semiconductors Selection

In order to analyze the in-system performance of SiC semiconductors the aim was to develop a CLBBC entirely of SiC power semiconductors, including both the power switches and the blocking diodes, despite their increased forward voltage drop compared with Si diodes. The possible power devices are limited by their availability. The switching device selected for this design is the SiC JFET produced, in sample quantities, by SiCED and packed in a standard TO-220 package. The JFET is rated for 1200 V with a breakdown voltage typically exceeding the 1300 V level. The DC current handling capability is limited to 6 A mainly by the die size of 2.4 mm × 2.4 mm and the thermal properties of the package. The essential SiC power semiconductor parameters are summarized in Table I.

In the CLBBC topology the series diodes significantly contribute to the overall converter conduction losses, as always 4 diodes are conducting the DC-link current. The device

Fig. 3. Replacement of the bridge-leg series diode (a) with a SiC JFET (b).

TABLE II
ALL-SIC JFET CLBBC SPECIFICATION SUMMARY

Quantity	*Value*
3∼AC Input	
Nominal RMS line-to-line voltages	$3 \times 400\,\mathrm{V}$, $50\,\mathrm{Hz}$
Current displacement angle	$\Phi_1 = 0°, 180°$
3∼AC Output	
Nominal RMS line-to-line voltages	$3 \times 400\,\mathrm{V}$, $0 \ldots 300\,\mathrm{Hz}$
Current displacement angle	$\Phi_2 = 0 \ldots 360°$
Nominal output power	$2.9\,\mathrm{kVA}$
Switching frequency	$200\,\mathrm{kHz}$
Power switches	SiCED SiC VJFET $1200\,\mathrm{V}$, $6\,\mathrm{A}$
Power diodes	CREE SiC Schottky diode C2D10120, $1200\,\mathrm{V}$, $10\,\mathrm{A}$
Overall outer dimensions	$230\,\mathrm{mm} \times 80\,\mathrm{mm} \times 65\,\mathrm{mm}$
Boxed volume	$1200\,\mathrm{cm}^3 = 1.2\,\mathrm{litre} = 73\,\mathrm{in}^3$
Power density	$2.4\,\mathrm{kVA/litre} = 40\,\mathrm{W/in}^3$
Weigth	$1.1\,\mathrm{kg}$

of choice is a $1200\,\mathrm{V}$, $10\,\mathrm{A}$ SiC Schottky barrier diode C2D10120 from CREE. As the SiC Schottky diode is a majority carrier device there is virtually no reverse recovery charge, which is desirable for high switching frequency operation. Basically, there are two diodes available from CREE with similar current rating and the same package as the SiC JFET: a $5\,\mathrm{A}$ and a $10\,\mathrm{A}$ device. In order to minimize the overall converter losses the diode was selected loss-optimal and not optimal in terms of semiconductor die usage. By selecting the $10\,\mathrm{A}$ SiC diode with a forward voltage drop of $U_F = 1.6\,\mathrm{V}$ (at $I_F = 6\,\mathrm{A}$, $T_J = 125°\mathrm{C}$) instead of the $5\,\mathrm{A}$ device with $U_F = 2.4\,\mathrm{V}$, the forward voltage drop is lowered by $0.8\,\mathrm{V}$, which leads to a reduction of the total conduction losses of 33%.

Optionally, the series diode could be replaced by a SiC JFET, as depicted in Fig. 3, leading to a common-drain configuration of two discrete JFETs. Depending on the SiC power device parameters, replacing the series diode by a JFET allows for further reduction of the conduction losses. The disadvantage of this approach is that instead of 12 gate driver circuits 24 are required and that the minimal number of isolated gate driver supplies is increased from 8 to 10. The conduction losses evaluated for a DC current of $6\,\mathrm{A}$ and a junction temperature of $125°\mathrm{C}$ for both, the series connection of JFET and diode (1) and the common-drain configuration of two JFETs (2), shows that for the given semiconductor parameters (Table I) the series diode configuration produces less losses and therefore was selected for implementation.

$$P_{L,JFET,Diode} = 0.55\,\Omega \cdot 6^2\,\mathrm{A}^2 + 1.6\,\mathrm{V} \cdot 6\,\mathrm{A} = 29.4\,\mathrm{W} \quad (1)$$

$$P_{L,JFET,JFET} = 0.55\,\Omega \cdot 6^2\,\mathrm{A}^2 + 2.8\,\mathrm{V} \cdot 6\,\mathrm{A} = 36.6\,\mathrm{W} \quad (2)$$

C. CLBBC Specifications

The CLBBC power specifications are determined by the rating of the available SiC JFETs. In order to provide a wide switching frequency range for optimization purposes and to be able to investigate EMI performance of AC-AC converters, operating at a switching frequency above the start of the CISPR 11 EMI norm at $150\,\mathrm{kHz}$, the nominal switching frequency was selected to be $200\,\mathrm{kHz}$. The overall design requirements can be summarized as follows:

- Exclusively SiC power semiconductors must be implemented.
- The electro-mechanical construction aims for a compact design to enable converter motor embedding. The input EMI filter, an additional CM output filter, and an auxiliary power supply should be integrated into the converter system.
- Only ceramic capacitors are allowed to be used in the power circuit in order to investigate their suitability and performance in AC-AC converter applications and to enable a compact design.

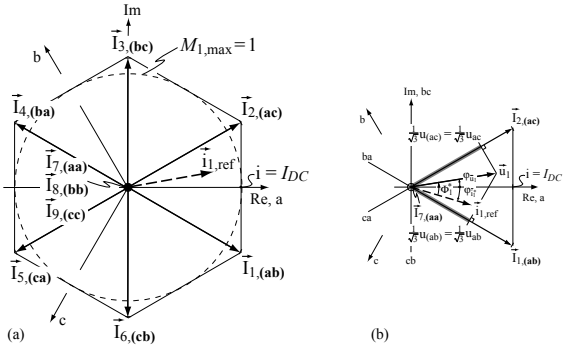

Fig. 4. (a) Space vectors for CSCs, shown for input stage on mains (a, b, c) and (b) weighting of the vectors for a given reference vector $\vec{i}_{1,ref}$.

D. Modulation Scheme

When considering space vectors, there are 6 active current vectors and 3 different zero vectors available for CSC topologies. Thus, there is one more zero vector compared to standard two-level VSCs.

In the literature, a wide variety of different modulation schemes for current source type converters can be found [6], [7]. Basically, in all these modulation strategies, typically two active current vectors and one or two zero vectors are used per modulation cycle. The main differences between the modulation methods are the number of switches involved in one modulation cycle, the different dependencies between losses and voltage to current displacement angle, and on where the vector sequence starts and ends.

As previously stated, the intended load for the prototype CLBBC is either a permanent magnet synchronous machine or an R-L-type load if it is used as a utility interface between two three-phase mains systems. Both of these applications have in common that the stationary output stage current displacement angle Φ_2 is close to $0°$. Due to the unity power factor requirement at the converter input the phase displacement angle Φ_1 is also close to $0°$ or $180°$ apart from a small offset for stationary input EMI filter current to voltage displacement compensation. This means that the CLBBC modulation scheme has to result in low losses exactly for this operating condition and should naturally also be advantageous in terms of EMI.

A space vector modulation scheme, which fulfils the above requirements, has been selected for implementation. It uses the two neighboring active vectors i.e. $\vec{I}_1$ and $\vec{I}_2$, with $t_{1,on} > t_{2,on}$ of the actual current reference vector $\vec{i}_{1,ref}$ and the corresponding switching loss-optimal zero vector $\vec{I}_7$, as depicted in Fig. 4. The applied current vector sequence of one modulation cycle for this case is then: $\vec{I}_7$-$\vec{I}_1$-$\vec{I}_2$-$\vec{I}_2$-$\vec{I}_1$-$\vec{I}_7$. For EMI purposes the vector, leading to the smaller line-to-line voltage switched to the DC-link of the two neighboring vectors, is switched first. Consequently, this minimizes the voltage change per switching action in the DC-link.

E. Control

Due to the integration of the input and output filter into the CLBBC the current measurement sensors can be placed beneficially in terms of converter control. Two current sensors are used to measure the output phase currents (after the common mode filter) and one sensor for the DC-link current. At the same time, through observing the actual output stage switching state, the currents flowing into the output stage capacitors can also be derived based on the DC-link current measurement. That means that with only three current sensors all relevant output currents can either be measured or calculated. The following signals are measured and used for modulation and control: 3 input and 3 output voltages, the DC-link current, and 2 output phase currents.

The basic idea for designing an appropriate control scheme is considering the apparent system dynamics:

- The switching frequency of 200 kHz provides theoretically a maximum control bandwidth of approximately 15 kHz to 20 kHz.
- The determined DC-link inductance allows a minimum magnetization time from 0 A to nominal DC-link current of 6 A within a switching period of 5 μs.
- The load time constants (inductance of PMSM or coupling inductors for mains application) are by contrary in the ms range.

This allows the application of the same decoupling principle of individual control loops as is used for cascaded control

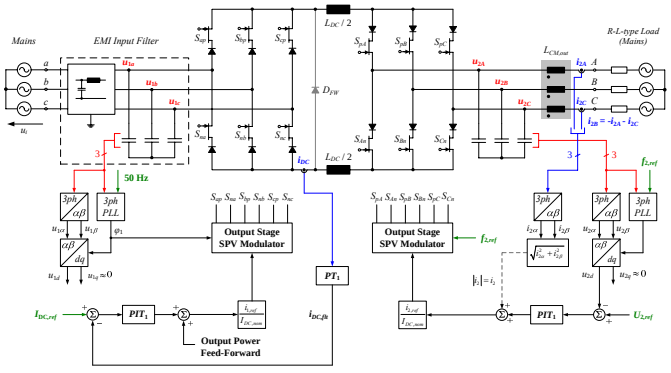

Fig. 5. Simplified dynamic feed-back control system, shown for R-L load. Red: voltage measurement, blue: current measurement, and green: input/feed-forward quantities. (Saturation and anti wind-up elements are not shown).

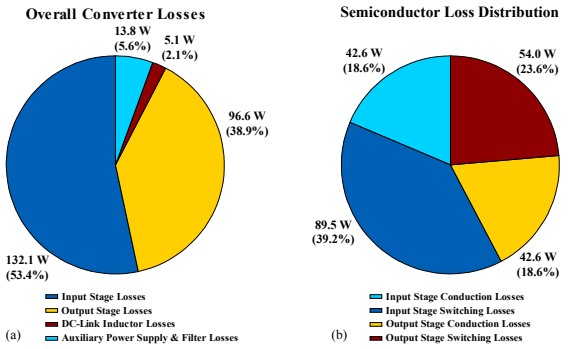

Fig. 6. (a) Overall converter losses and (b) semiconductor loss distribution.

systems, where the inner (fast) control loops can be designed independent of the outer (slow) control loops. Compared to the decoupling approach for cascaded control loops, for the CLBBC system, decoupling does not only occur on control level but even on system level, due to the difference in time constants.

For simplicity Fig. 5 depicts the implemented control scheme for operation on a R-L-type load. The quantities to be controlled are the DC-link current and the converter output voltage. The above described concept enables decoupling the DC-link current control from the output voltage control. The DC-link current control loop is the fast loop, while the output voltage is the slow loop. For best possible load current response time, the DC-link current is always controlled to be at its nominal level of 6 A, taking into account that the losses are increased. From a control point of view the CLBBC is a series connection of a buck-type Current Source Rectifier (CSR) and boost-type Current Source Inverter (CSI). For the present control scheme the CLBBC is restricted to buck-type operation.

The selected strategy is to control the desired CLBBC output voltage and frequency by the output stage and the DC-link current by the input stage. The output stage control consists of an outer voltage control loop and an inner current control loop that generates the required output current reference vector. The input current reference is then calculated by feed-forward (pre-control) of the estimated output power and the difference of the measured link current and its reference value.

For operation with a permanent magnet synchronous machine the control scheme needs simply being extended with the dq reference frame machine model and the output stage filtering capacitors as suggested in [3]. The switching frequency related decoupling principle is still valid.

The overall control scheme is digitally implemented in a DSP and optimized for processing speed. The achieved control cycle speed is 100 kHz, leading to an average system death time of 10 μs.

F. Losses

With the modulation and control scheme defined, the semiconductor switching losses and consequently the overall converter losses can be analytically modeled and calculated

[8], [9]. The conduction losses can easily be determined by calculating the average currents I_{avg} and rms currents I_{rms} through the individual devices and applying them to (3) where U_F is the diode forward voltage drop and $r_{DS,on}$ the on resistance of the JFET.

$$P_{Cond} = U_F \cdot I_{avg} + r_{DS,on} \cdot I_{rms}^2 \tag{3}$$

Based on the implemented modulation scheme the equations for calculating the switching losses can be derived and parameterized with measured switching loss data. For that purpose the switching loss energy is represented with a voltage and current dependent loss energy polynomial $w(u,i)$ according to (4).

$$w(u,i) = k_1 \cdot u \cdot i + k_2 \cdot u \cdot i^2 + k_3 \cdot u^2 + k_4 \cdot u \cdot i^2 + k_5 \cdot u^2 \cdot i^2 \tag{4}$$

The loss polynomial is then evaluated in dependency of the applied voltage and current during the switching action, averaged over all sectors for the input and output stage (Fig. 4), and then multiplied by the apparent switching frequency of 200 kHz. A more detailed description of the procedure is given for MC in [10].
The outcomes of the overall converter loss calculations, evaluated for nominal operation as specified in Table II, are summarized in Fig. 6. The resulting calculated overall converter efficiency for the nominal operating point is 92%.

G. Construction Concept

The physical construction of the CLBBC consists of a planar arrangement in which a stack is assembled from individual printed circuit boards (PCBs). The stack is designed such that the power flows in through the EMI input filter and then directly through the input stage, DC-link and output stage of the power board. The PCBs in the stack, starting at the bottom, are the power board, gate driver board, DSP control and measurement board, and EMI board (Fig. 7). A base plate is used as a thermal interface to a variety of cooling systems for testing purposes and has the same volume as a high-performance water-cooled heat sink. The resulting outer dimensions of the CLBBC are $230\,\mathrm{mm} \times 80\,\mathrm{mm} \times 65\,\mathrm{mm}$, corresponding to a boxed volume of $1.2\,\mathrm{litres}$ ($73\,\mathrm{in}^3$). This results in a power density of $2.4\,\mathrm{kVA/litre}$ ($40\,\mathrm{W/in}^3$). The actual power density for the given CLBBC is mainly limited by the current rating of the SiC JFETs and could easily be double by paralleling two JFET dies.

H. Power Circuit

The power board, shown in Fig. 7 contains the interconnections for the three-phase input from the EMI filter and the three-phase output to the load, the input and output capacitors, the DC-link connection to the inductor, and three low-profile magneto-resistive current sensors (Sensitec CDS4006). These sensors have a typical bandwidth of $150\,\mathrm{kHz}$.
The 4-layer PCB separates the input rectifier stage and the output inverter stage with the high frequency link inductor. The AC filter capacitors are soldered directly on the power board above the JFET switches in order to provide a degree of over-voltage protection, a low impedance connection, and improved filtering.

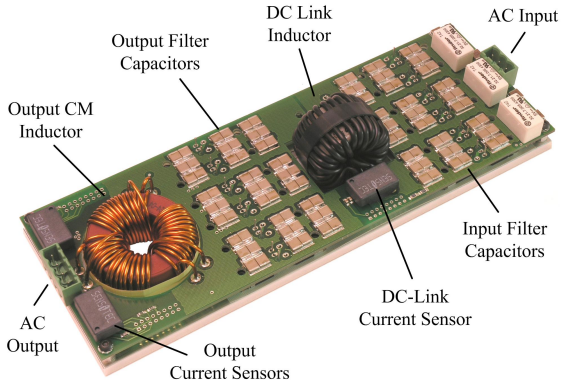

Fig. 7. Power board, showing the essential components.

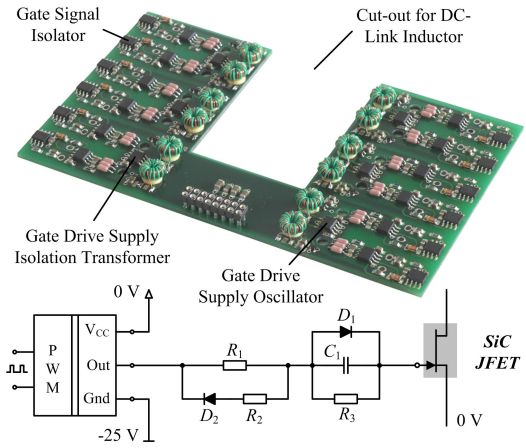

Fig. 8. Gate driver board with schematic of the gate drive circuit.

I. Gate Drives

To turn off the SiC JFET a negative bias voltage less than the pinch-off voltage is required. Due to the present processing variations in the SiC JFET's pinch-off voltage ($-15\,\mathrm{V}$ to $-23\,\mathrm{V}$) and gate-source breakdown voltage, a gate driver concept has been developed that includes a DC blocking capacitor C_1 as shown in Fig. 8. This capacitor blocks and protects the gate junction from any DC current caused by the applied turn-off voltage ($-25\,\mathrm{V}$) exceeding the gate-source breakdown voltage. The capacitor is sized to be $47\,\mathrm{nF}$ to ensure a correct time constant for operation at $200\,\mathrm{kHz}$. To ensure a low delay time in the switching signals, which is required for high frequency operation, a magnetic isolator (ADuM1100) is used followed by a $4\,\mathrm{A}$ gate drive IC (IXDN404). The total signal propagation time is only $30\,\mathrm{ns}$. An isolated $-25\,\mathrm{V}$ supply is generated for each gate driver by a full-bridge IC (MAX256) and a small toroidal transformer followed by a rectifier circuit.

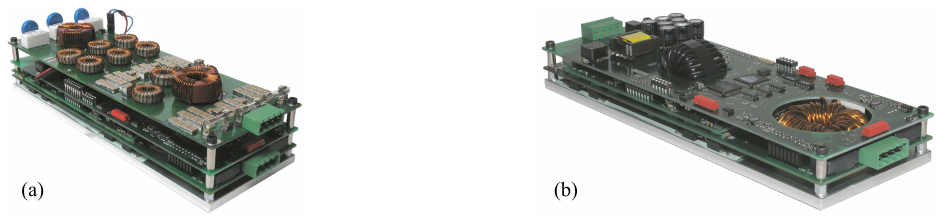

Fig. 9. Hardware prototype of the All-SiC JFET CLBBC. (a) Complete CLBBC, dimensions 230 mm × 80 mm × 65 mm. (b) CLBBC without EMI input filter board, showing the DSP/FPGA control and measurement board with wide input voltage range auxiliary power supply.

J. DC-Link Inductor

The main advantage of increasing the switching frequency is to reduce size and weight of the passive components. The DC-link inductor is the most significant passive component of the All-SiC JFET CLBBC. Volume, weight, and losses are the key criteria for its design.

In a first step the required inductance value has to be calculated. The approach is to limit the DC-link current ripple $\Delta I_{L,DC}$ to 15% of the nominal DC-link current of 6 A which leads to $\Delta I_{L,DC} \approx 1\,\mathrm{A}$. This is a reasonable value in terms of dynamic performance [11] and typical AC core losses. The apparent DC-link ripple can be derived based on the equations for the modulation scheme as a function of the DC-link inductance L_{DC}, the input and output stage modulation indices M_1, M_2, the switching frequency f_S, the input and output voltages $\hat{U}_1$, $\hat{U}_2$, and the input and output stage current reference angles $\varphi_{I1,ref}$, $\varphi_{I2,ref}$ according to equation (5).

$$\Delta I_{L,DC}\big(M_1, \hat{U}_1, \varphi_{I1,ref}, M_2, \hat{U}_2, \varphi_{I2,ref}, f_S\big)\Big|_{max} \tag{5}$$

Equation (5) evaluated for L_{DC} leads to

$$L_{DC} = \frac{3 \cdot (2-\sqrt{3}) \cdot \hat{U}_1}{4 \cdot \Delta I_{L,DC} \cdot f_S} = 327\,\mu\mathrm{H}\,. \tag{6}$$

Different magnetic materials and inductor construction principles such as planar E and SMD ferrite cores, toroidal and E powder cores, and tape wound C-cores have been analyzed regarding losses, size, fringing flux, and cooling performance. Toroidal powder core materials (distributed air gap) provide the best compromise between losses, cooling, and size due to the DC bias.

The power board layout allows for splitting the DC-link inductance into two equal inductors for common mode EMI purposes (one for the positive link one for the negative link, Fig. 1) or using just a single link inductor. Fig. 10 shows the implemented single link inductor.

Core	2 stacked Magnetics MPP 55071-A2
Winding	57 turns
Wire	Multi-stranded copper wire (0.8 mm^2)
Inductance	400 µH at 0 A, 200 kHz
	320 µH at 6 A, 200 kHz
Losses	5.1 W
Weight	120 g
Volume	40 cm^3 = 2.4 in^3

Fig. 10. Implemented DC-link inductor with construction data.

K. Integrated EMI Input and Output Filter

An EMI input and an output filter are required to meet CISPR Class A conducted emission levels. The filter design procedure is a combination of a time and frequency domain analysis using analytical calculations and simulations. It is based on differential mode (DM) and common mode (CM) equivalent circuits of the CLBBC system depicted in Fig. 11. Several simplifications are assumed in order to reduce the calculation effort: the switching waveforms do not account for the influence of inner converter non-idealities, the circuits are considered to be symmetric with respect to the three-phases, and the parasitics of the passive components are not considered.

A volume minimized design procedure is used, which minimizes the value of the DM inductive components. This can be achieved by increasing the amount of DM capacitance, as the capacitance per volume ratio is much higher than the inductance per volume ratio if ceramic capacitors are used (Fig. 25–27, [12]). The maximum amount of capacitance per phase is selected such that at nominal output power the voltage to current lag at the filter input is equal or less than 5°, leading to approximately 6 µF per phase.

The key point of the filter design is the determination of the frequency spectrum of the converter DM input current and the resulting CM voltage, representing the expected DM and CM noise sources. These noise sources are then injected into equivalent circuits to calculate the required filter attenuation by determining the LISN voltage u_{LSIN}. For the DM source

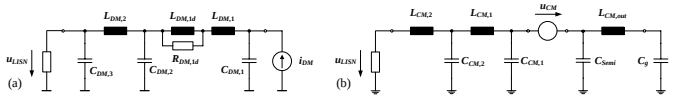

Fig. 11. (a) DM equivalent circuit and (b) CM equivalent circuit.

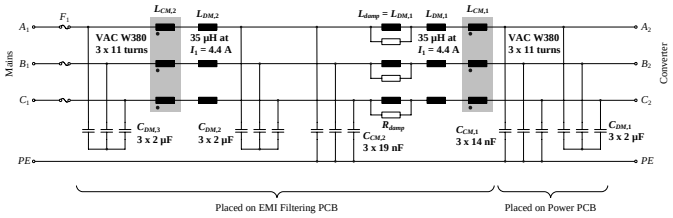

Fig. 12. Schematic of the implemented input EMI filter.

of the CLBBC the input current i_{DM} needs to be considered as it is impressed by the DC-link inductor. The CM equivalent circuit uses the CM voltage u_{CM} as noise source and tries to account for the dominant components in the CM path. C_{Semi} models the output stage power semiconductor capacitance to protective earth (PE). The measured parasitic capacitance of a TO-220 package to the heat sink (PE potential) is approximately 20 pF. The parasitic capacitance of the input stage semiconductors is included in the capacitance C_{CM1}. C_g represents the resulting capacitance to PE of the load machine. The capacitance of C_g has been determined through measurements of the target permanent magnet synchronous load machine (Lust LST-127) and is set to 5 nF. The requirement for the CM output inductor is to provide enough impedance to keep the resulting CM rms voltage for the switching frequency and its harmonics across C_g lower than 15 V. This allows limiting the motor bearing currents to a harmless level [12].
For both equivalent models the LISN voltage u_{LISN} is processed similar as in an EMC test receiver to find the worst case noise peak value. The filtering components are then designed such that the DM and CM spectrum fulfils CISPR class A norm. For the DM filter, a margin of 5 dB to 6 dB is used for the CM filter a margin of approximately 10 dB. Fig. 12 shows the resulting EMI filter with its parameters.

III. Experimental Performance at 200 kHz

A. Characteristic Waveforms and THD

The following measurements demonstrate the in-system switching behavior of the SiC JFETs for a gate resistance of $R_1 = 10\,\Omega$ and a DC blocking capacitance of $C_1 = 47$ nF. Fig. 13 presents the drain-source voltage switching waveforms of a low-side output stage switch. A turn-on and turn-off time of approximately 20 ns to 30 ns is achieved.
The input and output voltage and current waveforms at nominal output power for a R-L load are shown in Fig. 14. The input frequency is 50 Hz the output frequency is 40 Hz. As can be seen the input and output phase currents are of sinusoidal shape, which proves proper operation of the implemented modulation scheme. The semi triangular voltage waveform shape is caused by the voltage (E-field) dependent variation of the selected ceramic AC filtering capacitors. The input current is slightly leading the input voltage in consequence of the capacitive behavior of the CLBBC input filter, as the stationary active filter current to voltage lead compensator was deactivated.
The measured total harmonic distortion (THD) for nominal operation is 5%. The comparatively high THD value can be explained with the above mentioned nonlinear behavior of the filtering capacitors and the resulting distortion of the capacitor voltage waveform. By replacing the implemented X7R ceramic capacitors by COG ceramic capacitors the THD can be improved considerably, as COG dielectric material is virtually insensitive to voltage, frequency, and temperature variation. Unfortunately, the capacitance per volume ratio of COG ceramic capacitors typically is lower by a factor of 5 compared with X7R.

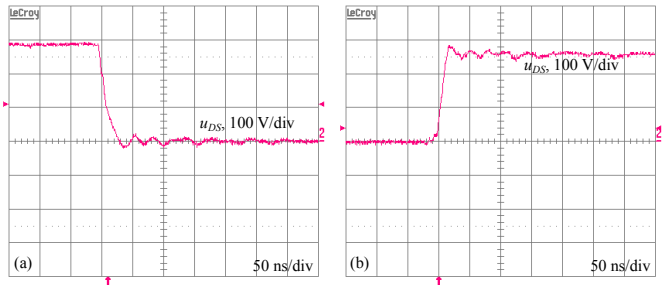

Fig. 13. (a) SiC JFET turn-on and (b) turn-off switching waveforms.

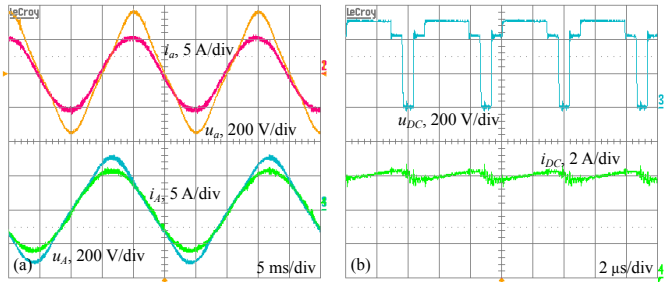

Fig. 14. (a) CLBBC input and output voltage and current waveforms. (b) DC-link voltage and current waveforms.

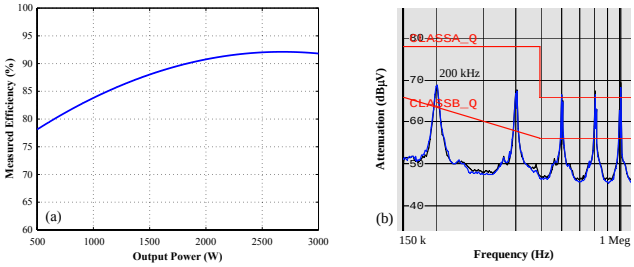

Fig. 15. (a) Measured efficiency vs. output power. (b) Quasi-peak CE EMI measurement result up to 1 MHz: blue DM, black CM.

B. Efficiency

The overall converter efficiency was measured for different output power levels and plotted in 15(a). The maximum efficiency is in the range of 92% and matches very well with the analytically predicted efficiency.

C. Conducted Emission EMI Measurements

The prototype All-SiC CLBBC (Fig. 1) has not yet been constructed with an appropriate enclosure. Therefore, CISPR 11 Class A conducted emission (CE) levels obviously cannot be fulfilled over the relevant frequency range from 150 kHz to 30 MHz, as the PE (protective earth) interconnection of the individual PCBs is too high impedance. For that reason Fig. 15(b) presents CE measurement results only in the frequency range of 150 kHz to 1 MHz, which seems to be representative for the given electro-mechanical construction. As can be clearly seen, the low frequency performance below 1 MHz meets the CE Class A requirements and at 200 kHz (switching frequency) there are 6 dB margin as calculated in the design. Above 1 MHz the CLBBC falls outside the specified levels.

IV. Comparison to SiC Indirect Matrix Converter

Prior to the CLBBC, a 200 kHz All-SiC JFET Indirect Matrix Converter (IMC) had been developed [13]. The IMC utilizes 18 SiC JFETs as power semiconductors and has an output power of 2.5 kVA. Compared to the CLBBC the IMC input current waveform quality is similar, since the input stages of both converters are current impressed. In the case of the IMC the current is impressed by the load inductance and in the case of the CLBBC from the DC-link inductor. This accounts for their topology based relationship and why they are appropriate for comparison.

On the load side the IMC has a switched voltage output compared to the sinusoidal voltage of the CLBBC. This is an advantage for the CLBBC since an additional, voluminous output filter is not required. A three-phase, sine-type output filter for the IMC would basically need 3 times the DC-link inductor of the CLBBC with a similar amount of output filtering capacitance. From this perspective the CLBBC allows for a more compact, higher power density implementation compared to the IMC if a sine-type output is required. The disadvantage of the CLBBC compared to the IMC is the lower efficiency: 92% for the CLBBC and approximately 94% for the IMC, both operating at a switching frequency of 200 kHz. In terms of conduction losses this is mainly due to the absence of the series diode in the IMC output stage. Furthermore, the input stage of the IMC can be switched at zero current, enabling almost lossless switching apart from parasitic effects.

V. Conclusions and Outlook

In this paper the design, construction, and operation of a fully digitally controlled All-SiC JFET Current DC-Link Back-to-Back Converter has been presented. The CLBBC can be operated at the desired switching frequency of 200 kHz and at nominal output power of 2.9 kVA. Given inherently by its topology, the CLBBC features an integrated sine-type output filter, which has been further enhanced by adding a CM stage to the converter output. The EMI requirements could only be achieved in the low frequency range due to the lack of a converter enclosure.

Design and construction of a proper enclosure, providing low impedance connection to PE, is subject to ongoing research and will hopefully provide a better understanding about the high-frequency suitability of the described filter design procedure. Further work will also focus on the boost-operation of the CLBBC.

It is unlikely that the CLBBC will replace the well known and well established VLBBC. Nevertheless, for applications where e.g. mains-bridging capability or ultimate control performance, which evidentially requires sufficiently high converter internal energy storage, is of secondary importance the SiC JFET CLBBC is a serious alternative. A further point in favor of the CLBBC is that due the absence of a link capacitor with thermally sensitive aging, the CLBBC could also be operated at elevated temperatures compared with a VLBBC. This would also match well with the advantageous temperature properties of SiC devices.

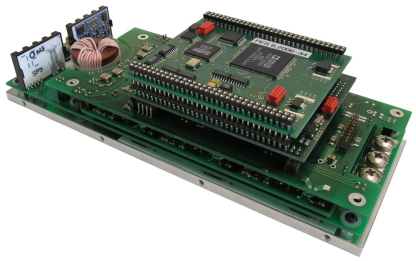

Fig. 16. 200 kHz, 2.5 kVA All-SiC JFET Indirect Matrix Converter, shown without EMI input filter. Base area: 220 mm × 80 mm.

To conclude with, ostensibly unwanted features such as the normally-on characteristic of the SiC JFET can be beneficially used in a appropriate topology such as the CLBBC and pinpoints the importance of matching semiconductor properties to the converter topology requirements.

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