Diss. ETH No. 29141

Synergetically Controlled Three-Phase Boost-Buck Ultra-Wide Output Voltage Range Isolated EV Battery Charger

A thesis submitted to attain the degree of

DOCTOR OF SCIENCES of ETH ZURICH
(Dr. sc. ETH Zurich)

presented by

YUNNI LI

MSc ETH
born on 19.09.1994
citizen of Wuhan, China

accepted on the recommendation of

Prof. Dr. Johann W. Kolar, examiner
Prof. Dr. Marcelo Lobo Heldwein, co-examiner

2023

ETH Zurich
Power Electronic Systems Laboratory
Physikstrasse 3 | ETL H13
8092 Zurich | Switzerland

http://www.pes.ee.ethz.ch

For my parents,
and my husband.

Acknowledgments

First and foremost, I would like to thank Prof. Dr. Johann W. Kolar, for offering me the amazing opportunity to pursue a Ph.D. at Power Electronic Systems Laboratory (PES). Starting from the very beginning of your inspirational lectures, I was deeply fascinated by how you unraveled the myth and puzzles in the world of power electronics like a detective, ultimately shaping my career path. More importantly, getting the chance to do a Ph.D. in your magnificent group has changed my life completely. This remarkable journey has been nothing short of an exhilarating adventure filled with challenges, and I could not have made it without your guidance, for which I can never be more grateful.

I would also like to thank Prof. Dr. Marcelo Lobo Heldwein for being my co-examiner. Thank you for taking the time to read my thesis and for joining my Ph.D. defense in person here in Zurich. Additionally, I extend my gratitude to Prof. Dr. Christian Franck for chairing my doctoral examination. Furthermore, many thanks go to my industrial partners, especially Dr. Jordi Everts from Prodrive Technologies and Dr. Gerald Deboy from Infineon Technologies Austria AG, for your trust and support.

The most special thanks go to my supervisor, Dr. Jannik Schäfer, who I had the pleasure to work with not only during my doctoral studies, but also during the course of my semester and master thesis project. I will forever be grateful for the things you taught me, for the countless discussions we had, for the support and inspiration you showed not only technically, but also personally. You are such a happy and creative person, a role model with a forever optimistic and energetic attitude towards not only work, but also life, which has inspired me so much. Most importantly, it has been so much fun working with you, for which I always feel so lucky.

In particular, I would like to thank Dr. Jon Azurza Anderson, who supervised me and helped me a lot, especially during the beginning of my Ph.D., which was not an easy time. I still recall all those discussions in the evenings and weekends, for which I am truly grateful. Your technical and social skills always set a good example for me. Afterwards, having you as the contact person in Infineon and on the other side of the presentation during the lab tour has made all the communications so smooth and easy.

Specifically, I would like to thank the girls, my dearest Neha Nein and Gwendolin Rohner. It's such a pleasure to meet and get to know you. We are so different, yet at the same time I feel we are so strongly connected and I never feel alone in your presence, which is the kind of friendship I will forever cherish. Our trips together, our countless conversations, and all the joy we

had at PES and off work have bonded us incredibly, and I hope it will never break.

This journey would never have been possible without the glorious PES team. I would like to thank my office mate Rosario Giuffrida, for all the technical and non-technical discussions in H13, and the fun time during the sports and coffee breaks. Particularly, to the people with whom I spent countless hours in the lab, coffee room, mensa, superkondi, and drinking (fake) cocktails, Dr. Pascal Niklaus, Dr. Menzi David, Dr. Michael Haider, Dr. Daifei Zhang, Reto Bonetti, Ivana Bagarić, Emanuel Hubmann, it has been such a fun, enchanting, meaningful journey, thank you! Furthermore, I would like to thank our senior researchers, Dr. Jonas Huber, Dr. Florian Krismer, and Dr. Dominik Bortis, who I had the pleasure to work with and learn from. When I was still doing my studies at PES as a student, it was motivating to see the old generations of PES, namely Dr. Thomas Guillod, Dr. Pedro Bezerra, Dr. Dominik Neumayr, Dr. Mattia Guacci, Dr. Michalis Antivachis, Dr. Julian Böhler, Dr. Piotr Czyz, Dr. Pantelis Papamanolis, DDr. Spasoje Miric, Dr. Gustavo Knabben, who completed their research projects exceptionally.

Thanks to the PES administrative team, Monica Kohn, Prisca Maurantonio, Roswitha Coccia and Yvonne Schnyder, and Peter Seitz, our lab technician, who helped me to assemble my hardware prototypes. In addition, I would like to express my appreciation to the D-ITET workshop around Silvio Scherr and formerly, Stefan Brassel, Stephan Siegrist and Daniel Wegmann under Martin Vogt for manufacturing various mechanical parts.

I would like to thank my parents Ailan Zheng and Xiaohui Li, who gave me life and strength. Last but certainly not least, to my husband Jiawei Liao, who always understands me, supports me, encourages me, who completes my soul and shares my dream, I am so lucky to have you in my life. Thank you for always being there for me, and with you, I will always have the courage to face the unknown fearlessly.

Danke! Thank you! 谢谢!

Yunni Li

Zurich, March 2023

Abstract

In the recent years, electric vehicles (EVs) have become increasingly popular owing to people's efforts to protect the environment and to cut off fossil fuel usage. To support the development of EVs, a charging infrastructure must be built, which many governments and companies around the world are working on. Power electronics plays a crucial role in providing power-dense and highly efficient EV chargers, which is not easy due to the wide output voltage range required to meet the battery voltage specifications of cars from different manufacturers, i.e. output voltage ranges as wide as 200 V...1000 V need to be covered by state-of-the-art EV chargers. Additionally, EV chargers need to provide galvanic isolation between the three-phase grid and the EV battery for safety reasons, which is why multiple converter stages are usually used, each fulfilling different aspects of the electrical requirements. In state-of-the-art EV chargers, there are usually two series-connected converter stages employed, comprising a non-isolated PFC rectifier front-end, which ensures the required sinusoidal input currents, followed by an isolated DC/DC converter stage, which on the one hand provides the required galvanic isolation and, on the other hand, controls the charging process of the EV battery by generating the required output voltage. In this work, the two-stage approach is investigated in detail in terms of topological solutions as well as optimal control, with a special focus on how the two converter stages can collaborate, i.e., synergetic control, such that the overall performance with regard to efficiency and power density of the EV charger is optimal.

First, the synergetic control of the three-phase six-switch PFC rectifier front-end is analyzed, where the 1/3-PWM is recapitulated, which allows for switching only one bridge-leg at a time, while still keeping sinusoidal currents at the input. This modulation reduces the switching losses significantly compared to the conventional 3/3-PWM, where all three bridge-legs of the PFC rectifier are actively switched. In the next step, the focus is placed on the feasibility of the 1/3-PWM under irregular grid conditions, and it is found that with a few simple protection devices, converters using 1/3-PWM can survive even in harsh environments. The proven applicability of the modulation for real charging applications paves the path for the subsequent discussions of using this modulation in the two-stage EV charger under investigation. Both the two-level six-switch three-phase PFC rectifier and the three-level three-phase PFC rectifier, i.e., the Vienna Rectifier, are considered in the investigations, where the components stress comparison between the conventional modulation (3/3-PWM) and the 1/3-PWM reveal significant switching loss savings, indicating a huge potential of this type of modulation

in the future. At this point, the second converter stage is not yet discussed in detail, with the only assumption that it can handle the necessary dynamics required by the PFC rectifier stage.

Therefore, in the second step, the isolated DC/DC stage is investigated in detail. To begin with, the widely used LLC converter and the DAB converter are analyzed, which are found to have serious limitations in the application at hand, i.e., for a wide output voltage variation. For LLC converters, the wide range of step-up and step-down ratios leads to a widely varying switching frequency, which on the one hand, results in the fact that a complex modulation has to be used for partial power operation. On the other hand, it is difficult to design compact EMI filters for converter systems with widely varying switching frequencies. Furthermore, due to the large deviation of the switching frequency from the resonant frequency, the simple frequency domain analysis is no longer suitable, which is why complicated time-domain methods have to be adopted. The second option, the DAB converter, can be operated with a constant switching frequency or at least a limited switching frequency range, but suffers from severe RMS current increases in deep buck or boost regions and also from a limited output voltage range where soft switching can be achieved. The large number of degrees of freedom of DAB converters makes it possible to mitigate these drawbacks to a certain extent, but at the expense of a significantly more complicated design and control of the converter. To speed up the time-consuming optimization, a simple modulation is proposed, which results in RMS currents close to optimal and soft switching can be achieved over a wide operating range. Nevertheless, since the soft-switching currents cannot be increased arbitrarily, and react sensitively towards all the non-idealities in the system, such as e.g., parasitic components, deadtime, delays in the controller etc., a calibration needs to be done in the modulation during the implementation of the converter, which is not trivial. Therefore, a new type of resonant converter is investigated to solve the aforementioned problems, and is referred to as the Quantum Series Resonant Converter (QSRC). It is characterized by the discretized length of the voltage intervals applied to the resonant tank and is always operated at the resonant frequency. By applying zero voltage intervals on either the primary side or secondary side, buck or boost functionality can be achieved. By selecting appropriate voltage patterns, full soft switching can be achieved under all operating conditions. Based on the optimal control patterns, design guidelines are developed for the QSRC to attain an efficient operation. To evaluate its performance objectively, the QSRC is compared with the LLC and the DAB converter, first by means of theoretical Pareto-optimizations,

where exemplary designs are chosen for each topology to demonstrate more details and insights. From the comprehensive comparison of different aspects, including RMS currents, semiconductor losses, and magnetic components losses, the QSRC shows similar performance compared to the LLC converter, but with the great advantage of having a constant switching frequency, and much better performance than the DAB converter due to lower RMS currents and soft switching over the entire operating range (at full load). Last but not least, to complete the comparison, there is one aspect where the DAB converter is significantly better than the resonant converters, which is the dynamic performance, which is an important criterion, especially considering the 1/3-PWM operation of the PFC rectifier front-end. The comparison is then validated with experimental measurements, using two hardware demonstrators of the QSRC and DAB converter, both rated for 2.5 kW, with the same switches, heatsinks, and volumes of the magnetic components, i.e., the same power density. The efficiency measurements show clear benefits for the QSRC, as expected according to the theoretical considerations. Finally, to further improve the performance of the QSRC, the Hybrid Quantum Series Resonant Converter (H-QSRC) is proposed, where one two-level half-bridge leg of the primary-side full-bridge is replaced with a T-type three-level half-bridge leg to increase the number of voltage levels which results in a decreased RMS current and an increased control accuracy.

After the two converter stages of the EV charger have been analyzed separately, the joint operation of the two stages is considered in the last step in order to identify possible benefits which can be achieved from a synergetic control. The combination of the two-level front-end PFC rectifier stage and the H-QSRC DC/DC converter output stage is considered first. Due to the capability of the isolated DC/DC stage to both step up and down the voltage, there exist different possibilities to combine 1/3-PWM and the conventional modulation in the two-stage EV charger, together with the buck, SRC, and boost-mode of the H-QSRC. Different synergetic control options are evaluated based on component stresses and the best one is identified, where none of the stages is over-stressed. The feasibility of the proposed synergetic control is finally successfully verified by means of simulations. In the next step, the two-stage EV charger is realized in hardware as a 10 kW module. Combining a three-level Vienna Rectifier (VR) with four isolated Dual Active Bridge DC/DC Converter (DABC) modules and latest-generation 600 V GaN technology enables very high switching frequencies of 560 kHz for the VR and up to 330 kHz for the DABCs. Hence, in this work an ultra-compact realization of a 10 kW EV charger module with a power density of 9 kW/dm^3

(about 150 W/in^3), not including the coldplate, is presented. In this context, the simplified DABC modulation method used for the single module is again employed, and straightforward yet accurate (confirmed by experiments) loss models for the DABCs and the VR are introduced, which facilitate a thorough investigation of the optimum synergetic operation of the two stages: For the considered converter, changing the VR operating mode from conventional 3/3-PWM (where the two stages operate rather independently and hence all three VR bridge-legs operate with PWM) to 1/3-PWM (where the DABCs shape the voltage of the shared intermediate DC-link such that always only one of the VR's three bridge-legs must operate with PWM) results in an advantageous efficiency improvement of up to about 2% over a large part of the output voltage and power range, and in a peak efficiency of more than 97%. Further, the synergetic operation of the two-stage system (VR and DABCs) is experimentally verified for the first time, confirming the modeling results and the efficiency advantage of 1/3-PWM (i.e., 95.4% vs. 95.1% at the rated load of 10 kW and with 500 V output voltage). Conducted EMI pre-compliance measurements indicate that the change of the operating strategy from 3/3-PWM to 1/3-PWM only requires minor changes of the EMI filter design.

Kurzfassung

In den letzten Jahren sind Elektrofahrzeuge (EVs) aufgrund der Bemühungen der Gesellschaft, die Umwelt zu schützen und den Verbrauch fossiler Brennstoffe einzuschränken, immer beliebter geworden. Um die Entwicklung von EVs zu unterstützen und voranzutreiben, muss jedoch auch die entsprechende Ladeinfrastruktur bereitgestellt werden, woran viele Regierungen und Unternehmen weltweit intensivst arbeiten. Leistungselektronik spielt dabei eine entscheidende Rolle, da sie es ermöglicht leistungsstarke und hocheffiziente EV-Ladegeräte zu entwickeln. Dies ist jedoch nicht trivial, da ein solches Ladegerät einen weiten Ausgangsspannungsbereich abdecken muss, welcher aufgrund der unterschiedlichen Batteriespannungsspezifikationen verschiedener Hersteller erforderlich ist. Der Ausgangsspannungsbereich, welcher von modernen Ladegeräten erwartet wird, reicht von üblicherweise 200 V bis zu 1000 V. Zudem müssen EV-Ladegeräte aus Sicherheitsgründen eine galvanische Trennung zwischen dem dreiphasigen Energieversorgungsnetz und der EV-Batterie aufweisen. Aus diesem Grund werden in der Regel mehrere Wandlerstufen verwendet, von denen jede Stufe unterschiedliche Aufgabenbereiche der elektrischen Anforderungen übernimmt.
Bei modernen EV-Ladegeräten werden in der Regel zwei in Serie geschaltete Konverterstufen eingesetzt. Bei der ersten Stufe handelt es sich um einen nicht-isolierten Gleichrichter mit Leistungsfaktorkorrektur, welcher die erforderlichen sinusförmigen Eingangsströme sicherstellt. Am Ausgang dieses Gleichrichters wird eine zweite Stufe, ein isolierter Gleichspannungswandler, angeschlossen, der einerseits die erforderliche galvanische Trennung bereitstellt und andererseits den Ladevorgang der EV-Batterie steuert, indem er die erforderliche Ausgangsspannung erzeugt.
In dieser Arbeit wird der zweistufige Ansatz hinsichtlich neuer topologischer Ansätze sowie deren optimaler Steuerungen im Detail untersucht. Ein besonderer Fokus liegt dabei auf der Zusammenarbeit der beiden Konverterstufen, d. h. auf einer synergetischen Steuerung, welche die jeweils auftretenden Strom- und Spannungsbeanspruchungen der Bauelemente so zwischen den Stufen verteilt, dass eine optimale Gesamtperformance hinsichtlich Effizienz und Leistungsdichte des EV-Ladegeräts erzielt wird.

Zu Beginn wird die Steuerung der ersten Stufe, des dreiphasigen Sechs-Schalter-PFC-Gleichrichters, analysiert, mit speziellem Fokus auf den sogenannten 1/3-PWM Betrieb. Dieser ermöglicht es, dass jeweils nur eine Halbbrücke mit einer hohen Frequenz geschaltet werden muss, und trotzdem sinusförmige Ströme am Eingang erreicht werden. Diese Art der Modulati-

on reduziert die Schaltverluste erheblich im Vergleich zur herkömmlichen sogenannten 3/3-PWM Steuerung, bei welcher alle drei Halbbrücken des PFC-Gleichrichters aktiv mit einer hohen Frequenz geschaltet werden.
In einem nächsten Schritt wird überprüft, ob die 1/3-PWM Steuerung auch unter irregulären Netzbedingungen funktioniert, was eine Voraussetzung für deren Anwendung in kommerziellen EV-Ladegeräten ist. Es wird gezeigt, dass mit einigen wenigen Schutzvorrichtungen ein sicherer Betrieb von PFC-Wandlern mit 1/3-PWM Steuerung möglich ist und diese mit allen gängigen Netzstörungen umgehen können.
Als Nächstes wird der Einfluss dieses Betriebs auf die Effizienz verschiedener PFC-Gleichrichter Topologien genauer untersucht, mit Hauptaugenmerk auf den konventionellen Sechs-Schalter-Dreiphasen-PFC-Gleichrichter, sowie den Dreiphasen-Vienna-Gleichrichter. Dabei zeigt der Vergleich der Strom- und Spannungsbeanspruchungen der leistungselektronischen Komponenten zwischen der herkömmlichen Modulation (3/3-PWM) und der 1/3-PWM Steuerung erhebliche Einsparungen bei den Schaltverlusten, womit diese Art der Steuerung großes Potenzial für den Einsatz in zukünftigen EV-Ladegeräten birgt.
In dieser ersten Betrachtung wird die zweite Wandlerstufe, der isolierte DC/DC-Wandler, noch nicht im Detail besprochen. Es wird lediglich davon ausgegangen, dass sie die erforderlichen Dynamiken, die vom PFC-Gleichrichter benötigt werden, bereitstellen kann.

Entsprechend wird im zweiten Teil ebendiese Wandlerstufe, die isolierte DC/DC-Stufe, detaillierter untersucht. Zunächst werden die weit verbreiteten LLC-Wandler und DAB-Wandler Topologien analysiert, welche sich jedoch nur bedingt für Anwendungen mit einem weiten Ausgangsspannungsbereich eignen. Beispielsweise führt bei LLC-Wandlern der weite Bereich der Verhältnisse zwischen Ein- und Ausgangsspannung zu einer stark variierenden Schaltfrequenz, welche das Design eines kompakten EMI-Filters erheblich erschwert. Des Weiteren wird für den Teillastbetrieb eine sehr komplexe Modulation benötigt, da aufgrund der großen Abweichung der Schaltfrequenz von der Resonanzfrequenz die normalerweise verwendete Frequenzbereichsanalyse nicht mehr genügend genau ist, und zeitdiskrete Methoden für die Implementierung einer geeigneten Regelung verwendet werden müssen. Dies macht diese Topologie für den Einsatz in einer solchen industriellen Anwendung unattraktiv.
Die zweite Topologie, der DAB-Wandler, kann im Gegensatz zum LLC-Wandler mit einer konstanten Schaltfrequenz oder zumindest einem begrenzten Schaltfrequenzbereich betrieben werden. Allerdings zirkulieren in dieser

Topologie für hohe Spannungsübersetzungsverhältnisse sehr hohe Ströme, welche nicht zur übertragenen Wirkleistung beitragen, weshalb Wandler mit dieser Topologie für hohe Übersetzungsverhältnisse oftmals eine geringe Effizient aufweisen. Die hohe Anzahl an Freiheitsgraden der Regelung von DAB-Wandlern ermöglicht es zwar, diese Nachteile in gewissem Maße zu mildern, jedoch sind diese Nachteile prinzipbedingt und können auch mit der komplexesten Regelung des Konverters nicht vollständig ausgeglichen werden.
Dennoch ist es natürlich möglich, über weite Betriebsbereiche effiziente DAB-Wandler zu bauen, weshalb in dieser Arbeit eine einfache Modulation entwickelt wird, die zu einem nahezu optimalen RMS-Strom führt und ein weiches Schalten der Vollbrücken über einen weiten Betriebsbereich sicherstellt. Da die Ströme für das weiche Schalten der Vollbrücken jedoch nicht beliebig erhöht werden können und empfindlich auf alle Nichtidealitäten im System reagieren, wie z. B. parasitäre Elemente, Totzeiten, Verzögerungen im Regler usw., ist eine Kalibrierung der Modulation während der Implementierung des Konverters erforderlich. Auch dies ist ein erheblicher Nachteil hinsichtlich des Einsatzes dieser Topologie in einer industrielle Anwendung.
Aus diesem Grund wird eine neue Art von Resonanzkonverter vorgestellt, welche die Nachteile der zwei obengenannten Topologien bis zu einem gewissen Grad vermeidet. Diese neue Topologie wird als Quantum Series Resonant Converter (QSRC) bezeichnet. Der QSRC wird mit einer konstanten Schaltfrequenz betrieben, welche geringfügig höher als die Resonanzfrequenz liegt, und wird mit sich wiederholenden Sequenzen von positiven und negativen Spannungszeitflächen, die jeweils eine Dauer einer halben Schaltperiode aufweisen, gesteuert. Durch das Einfügen von Null-Spannungsintervallen in diese Sequenzen (entweder auf der Primär- oder der Sekundärseite) kann eine Tiefsetzsteller- oder Hochsetzsteller-Funktionalität erreicht werden. Des Weiteren kann durch die Auswahl geeigneter Spannungssequenzen weiches Schalten über den gesamten Betriebsbereich garantiert werden. Mithilfe dieser Regelung werden anschliessend einfache Design-Richtlinien für den QSRC-Wandler abgeleitet, welche eine effiziente und kompakte Realisierung eines solchen Wandlers ermöglichen.
In einem letzten Schritt wird die neue QSRC Topologie mit den bekannten LLC- und DAB-Wandler Topologien anhand von Mehrzieloptimierungen verglichen. Aus dem Vergleich verschiedener Aspekte, wie z.B. der auftretenden RMS-Ströme, Halbleiterverluste und Verluste in den magnetischen Komponenten, geht hervor, dass der QSRC ähnliche Effizienzen und Leistungsdichten wie der LLC-Wandler erzielt, jedoch mit dem großen Vorteil

einer konstanten Schaltfrequenz und einer einfacheren Regelung. Im Vergleich zum DAB-Wandler schneidet der QSRC-Wandler deutlich besser ab, insbesondere aufgrund geringerer RMS-Ströme sowie dem weichen Schalten über den gesamten Betriebsbereich (im Betrieb unter Volllast). Abschließend wird noch eine potenzielle topologische Verbesserung des QSRC gezeigt, welche als Hybrid Quantum Series Resonant Converter (H-QSRC) bezeichnet wird. Dabei wird eine Zwei-Level-Halbbrücke auf der Primärseite durch einen zusätzlichen Schalter zu einer sogenannten T-Typ-Drei-Level-Halbbrücke erweitert, welche die Anzahl der zur Verfügung stehenden Spannungsniveaus erhöht, was zu einer Verringerung der RMS-Ströme im Wandler, sowie einer präziseren Regelung führt.

Nachdem die beiden Wandlerstufen des EV-Ladegeräts separat analysiert wurden, wird im letzten Teil der Arbeit der simultane Betrieb der beiden Stufen betrachtet, um mögliche Vorteile einer synergetischen Steuerung zu finden. Als Erstes wird die Kombination aus einem Sechs-Schalter-Dreiphasen-PFC-Gleichrichter und einem H-QSRC-DC/DC-Wandler betrachtet. Aufgrund der Fähigkeit der isolierten DC/DC-Stufe, die Ausgangsspannung sowohl zu erhöhen als auch zu senken, ergeben sich verschiedene Möglichkeiten, die 1/3-PWM Steuerung und die 3/3-PWM Steuerung des PFC-Gleichrichters mit den verschiedenen Betriebsmodi des H-QSRC zu kombinieren. Entsprechend werden verschiedene synergetische Regelungsvarianten anhand der auftretenden Strom- und Spannungsbeanspruchungen der leistungselektronischen Komponenten bewertet, um das beste Regelverfahren zu finden.
Die so gefundene optimale synergetischen Regelung wird schließlich erfolgreich mittels numerischen Simulationen verifiziert. Im nächsten Schritt wird das zweistufige EV-Ladegerät als Hardwaremodul mit einer Ausgangsleistung von 10 kW realisiert. Durch die Kombination eines Vienna-PFC-Gleichrichters (VR) mit vier isolierten Dual-Active-Bridge-DC/DC-Wandler (DABC) Modulen und neuester 600-V-GaN-Halbleiter-Technologie können sehr hohe Schaltfrequenzen von 560 kHz für den VR und bis zu 330 kHz für die DABCs erreicht werden. Die hohen Schaltfrequenzen ermöglichen eine ultrakompakte Realisierung des 10 kW EV-Ladegerätmoduls mit einer Leistungsdichte von 9 kW/dm^3 (ca. 150 W/in^3), ohne Berücksichtigung des Kühlkörpervolumens.
Anhand experimenteller Messungen am Hardwaremodul werden die Verlustmodelle für die DABCs und den VR präzisiert, und anschliessend dazu verwendet eine optimale synergetische Regelung für die beiden Stufen zu entwickeln. Im betrachteten Hardwaremodul führt die neue synergetische Regelung, in der anstelle der konventionellen 3/3-PWM (bei der die beiden Stufen unabhängig voneinander arbeiten und daher alle drei VR-Halbbrücken

schnell geschaltet werden müssen) die 1/3-PWM (bei der die DABCs den Verlauf der gemeinsamen Zwischenkreisspannung so formen, dass immer nur eine der drei VR-Halbbrücken schnell geschaltet werden muss) verwendet wird, zu einer Effizienzverbesserung von bis zu 2% über einen weiten Ausgangsspannungs- und Leistungsbereich, sowie einem Spitzenwirkungsgrad von mehr als 97%. Damit werden die Vorteile einer synergetischen Regelung eines zweistufigen Systems (VR und DABCs) erstmals experimentell nachgewiesen, wodurch die Simulationsergebnisse der Effizienzverbesserung unter Verwendung der 1/3-PWM (95.4% gegenüber 95.1% bei der Nennlast von 10 kW und einer Ausgangsspannung von 500 V) bestätigt werden. Abschliessend zeigen die durchgeführten EMI-Konformitätsmessungen, dass die Änderung der Regelung von 3/3-PWM auf 1/3-PWM nur geringfügige Anpassungen des EMI-Filterdesigns erfordert.

Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
BEV	Battery Electric Vehicle
CCM	Continuous Conduction Mode
CM	Common-Mode
CWG	Combination Wave Generator
DAB	Dual Active Bridge
DC	Direct Current
DCM	Discontinuous Conduction Mode
DM	Differential Mode
DPWM	Discontinuous PWM
EMI	Electromagnetic Interference
EUT	Equipment Under Test
EV	Electric Vehicle
FHA	Fundamental Harmonic Approximation
HEMT	High Electron Mobility Transistor
HF	High Frequency
H-QSRC	Hybrid Quantum Series Resonant Converter
ICE	Internal Combustion Engine
IPOP	Input-Parallel Output-Parallel
IPOS	Input-Parallel Output-Series
ISOP	Input-Series Output-Parallel
ISOS	Input-Series Output-Series
LISN	Line Impedance Stabilization Network
LLC	LLC Resonant Converter
LUT	Lookup Table
LV	Low Voltage
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MV	Medium Voltage
NPC	Neutral Point Clamped Converter
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PE	Protective Earth
PFC	Power Factor Correction
PI	PI Controller
PLL	Phase-Locked Loop
PSM	Phase Shift Modulation

PWM	Pulse-Width Modulation
QSRC	Quantum Series Resonant Converter
RMS	Root-Mean-Square
SPD	Surge Protection Devices
SRC	Series Resonant Converter
SSC	Six-Switch Converter
THD	Total Harmonic Distortion
TIM	Thermal Interface Material
TVS	Transient-Voltage-Suppression
V2G	Vehicle-to-Grid
VR	Vienna Rectifier
Bb-VSR	Boost-buck Voltage Source Rectifier
ZVS	Zero-Voltage-Switching

Contents

1 Introduction

1.1 Motivation

On December 12th, 2015, the Paris Agreement was signed by the major economies in the world to fight against climate change [1]. Specifically, the goal was to keep the global temperature rise within 2℃, or even more ideally, below 1.5℃. The temperature increase is closely related to the cumulative carbon emissions [2], whereby the latest studies [2, 3] show that we are already on the edge of exceeding it. To achieve these ambitious goals, joint efforts from humankind are vital in all different aspects, e.g. customer behavior, intensive research in energy technology, environmentally friendly political decisions, and so on [4]. Amongst others, the energy sector is one of the largest contributors to global greenhouse gas emissions, particularly CO_2, primarily due to the combustion of fossil coal, oil, and gas [3]. Within the energy sector, the transportation and mobility business significantly contribute to these emissions. For example, 15% of the total CO_2 emissions in Europe are emitted by cars and vans [5]. Therefore, new innovative technology in this area is particularly in demand to advance the decarbonization process.

Over the past decade, electric vehicle (EV) sales have grown significantly [6]. For example, since 2019, the share of EVs among global car sales has risen by a factor of four to almost 10% in 2021 [7]. By reducing the number of cars utilizing internal combustion engines (ICE), carbon emissions can be decreased significantly in the mobility sector. For example, the shift from ICEs to battery-powered electric vehicles (BEVs) could reduce the CO_2 emissions of road-based traffic by 65% with the current average energy mix in Europe [4]. To push this transformation forward, many countries have already set out policies and regulations. The EU has announced its "Fit for 55" program,

which promises to reduce the emissions by 55% by 2035 [4]. The proposed regulation stipulates the phase-out task for ICEs by 2035, particularly for cars and vans. As further examples, the U.S. Biden government is aiming at a target of having 50% electric vehicles (EVs) by the end of 2030 [4, 8], and the Chinese government has imposed a mandate on the car manufacturers to increase the percentage of total sales of EVs to 40% by 2030 [4]. Beyond all these regulations, EVs are also often heavily subsidized.

To ensure the successful electrification of transportation, the whole electric energy distribution network needs to be advanced, whereby the charging infrastructure is particularly important for obvious reasons. With more than 70 million EVs on the road by 2030 [4], a large number of public and private charging stations need to be installed to avoid a potential bottleneck in EV charging [9]. Recent studies show that the number of charging stations is expected to grow significantly, with 1.2 million in the U.S., 1.15 million in China, and 2.9 million in Europe by 2030 [10, 11]. The sheer number of future charging stations is the clear motivation for this work, where a highly efficient and compact EV charging system is developed, which could be part of a reliable and efficient charging infrastructure for future mobility.

1.2 State-of-the-Art EV Chargers

For mainstream EVs, the nominal voltage of the battery is typically around 400 V [12], and might decrease to 200 V…300 V [12, 13] during operation depending on the state of charge of the battery. To decrease the charging time, the latest and next-generation cars are targeting 800 V batteries [14–16], of which the voltage can decrease to around 600 V [17].

Depending on where they are installed, EV battery chargers can be classified as either on-board or off-board chargers [18]. On-board chargers feature an AC input, and standards such as IEC 62196 or SAE J1772 define charging power levels in the range of 3 kW to 22 kW, depending also on whether a single- or three-phase mains is available [13, 18–20]. The single-phase input is usually used for on-board chargers with a power rating of 3.6 kW or 7.4 kW [18]. However, to speed up the charging process, some OEMs (original equipment manufacturers) have started to equip their EVs with on-board chargers that are powered from the three-phase power supply network to increase the power to 11 kW or even 22 kW [12, 19–21]. These chargers are usually more expensive, but at the same time more convenient for the customer, since short charging times can be achieved even without a well-developed charging infrastructure. Off-board chargers, on the other hand, typically are

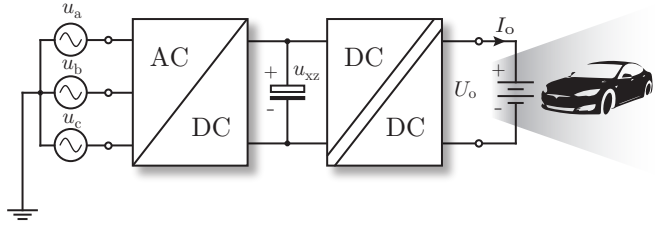


Fig. 1.1: Typical charging system structure, with the three-phase AC/DC front-end and the isolated DC/DC stage.

capable of transferring comparably high power and are therefore supplied from the three-phase grid, realized with stationary charging stations and a DC interface to the EV, ranging from 11 kW to 400 kW [12], e.g., the CHAdeMo standard allows power levels of up to 400 kW at 1000 V DC [12, 22] (note that even higher voltage and current ratings of up to 1250 V DC and 3000 A are envisioned for the future [23], e.g., targeting electric trucks). To ensure compatibility with a wide range of EV batteries, such stationary fast-charging stations should feature a wide output voltage range of typically 200 V to 1000 V.

Fig. 1.1 further shows the typical block diagram of an EV charger: there is a power-factor-correcting (PFC) AC/DC rectifier stage, an intermediate DC bus, and an isolated DC/DC converter [12, 22, 24] that provides galvanic separation to ensure user safety and contributes to covering the wide output voltage range [25] (this is necessary as, e.g., a typical boost-type PFC rectifier operating from a 400 V line-to-line mains cannot generate a DC voltage below about 650 V if some control margin is taken into account [26]). Even though non-isolated EV chargers are being considered as an alternative that could possibly facilitate higher efficiency and compactness [27], the two-stage approach with galvanic separation still is the most widely employed solution, not least because of electrical safety considerations. For simplicity reasons, the two stages are usually connected through an intermediate DC-link comprising large electrolytic capacitors, which keep the DC-link voltage constant under all operating conditions.

Furthermore, conventional silicon (Si) switches are typically utilized in such systems for cost reasons, although silicon-carbide (SiC) switches have recently become increasingly popular because of their more efficient switching behavior, and the fact that their manufacturing costs have fallen drastically in recent years [28].

Literature discusses a wide variety of converter topologies for the realization of the AC/DC PFC rectifier and the isolated DC/DC converter stages of EV chargers [12, 22, 24]. The common choice of topology for the PFC rectifier front-end in state-of-the-art EV chargers depends on the power supply connected to the input. For single-phase inputs, one or two interleaved conventional boost converter stages, or totem pole converters are commonly used [13, 28]. For three-phase inputs, on the other hand, either simple two-level six-switch converters (SSC) are employed, or the Vienna Rectifier is used, which has several advantages over the SSC, such as e.g., improved power conversion performance, reduced required breakdown voltages of the switches, as well as lower overall costs. In some cases, other topologies, e.g., the Neutral Point Clamped (NPC) converter, the flying capacitor multilevel AC/DC converter, etc., are used [12, 22].

For the second stage, the isolated DC/DC converter between the DC-link capacitor and the EV battery, the commonly used converter systems can be classified into two categories: phase-shifted converter systems, as, e.g., the phase-shifted full-bridge converter or the Dual Active Bridge (DAB) converter, and resonant converter systems, such as e.g., LLC or CLLC resonant converters [12, 13, 22, 28].

Even though today's single-phase chargers for electric vehicles are very efficient and, above all, compact, three-phase on-board chargers are becoming more and more popular, due to the higher rated power and the ability to be operated with single-phase supply with minor rearrangements. For this reason, increasing the power density of such systems is particularly important when it comes to developing competitive three-phase EV charger on-board products. Furthermore, due to the economies of scale, it would be desirable to develop a modular three-phase EV charger that is compact enough such that one module can be used as an on-board charger, but at the same time is also efficient enough such that multiple parallel-connected modules can be used as a high-power off-board charger.

The development of such an EV charging module is the core of this work, taking into account various challenges of real applications, such as, e.g., irregular grid conditions or electromagnetic interference (EMI) limitations.

In the following, the most important electrical specifications of state-of-the-art three-phase on-board and off-board EV charging systems are summarized, which are also used as references for the investigations in the course of this work.

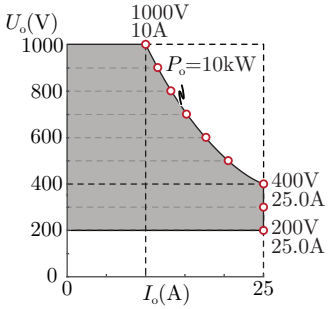


Fig. 1.2: Output voltage U_o and output current I_o range for a 10 kW EV charging module, where the red circles represent the nominal operating points.

1.3 Specifications of the Investigated EV Charging Systems

The main electrical specifications considered in this work are shown in **Fig. 1.2**, with a maximum output power of 10 kW and the nominal output voltage from 200 V to 1000 V, such that the applicability for all types of car batteries is given. The output current is limited to 25 A, which means the maximum power is only available from 400 V upwards. The unit could be employed as an on-board charger, where the achieved high compactness is beneficial, or several units could be operated in parallel to realize a high-power fast-charging station.

The input voltage of the charger differs by country, for example, 380 V in China, 400 V in Europe, while 480 V in the U.S. (line-to-line RMS voltage). On top of the nominal voltage, usually ±10% variation is considered [12]. In this work, 400 V is chosen as the nominal input voltage.

In order to compare newly developed EV charging systems with state-of-the-art solutions, efficiency is often used as a performance indicator. However, due to the widely varying output voltage of the EV charger, it is not sensible to use the efficiency at just one operating point for comparing different EV chargers, which is why a fair comparison is only possible using the average efficiency of the charger over the entire operating range. However, since the operating time of the EV charger is not evenly distributed over the operating range, the individual operating points are weighted as follows [29, 30]:

$$\bar{\eta} = \frac{1}{N} \sum_{i=1}^{N} \eta_i, \tag{1.1}$$

where $N = 9$, i.e., nine operating points are selected, with three points at $U_o = 200\,\text{V}, 300\,\text{V}, 400\,\text{V}$ in the constant current operating range, i.e., with the maximum output current of 25 A, and six points at $U_o = 500\,\text{V}, 600\,\text{V}...1000\,\text{V}$ in the constant power range, i.e., with the maximum output power of 10 kW, as marked by the red circles in **Fig. 1.2**. The average efficiency, in combination with the achieved overall power density of the system, is finally used as the main performance factor in the evaluation of the developed solution for the application at hand.

1.4 Aims and Contributions

The objective of this work is to develop and evaluate various ideas for increasing the efficiency and/or the power density of state-of-the-art three-phase high-power EV chargers, such that a three-phase EV charging module can be built at the end, which can be used both as a three-phase on-board charger at 10 kW, or with the help of a parallel connection of multiple modules, as a three-phase off-board EV charger with higher output power. The challenges of the wide output voltage range and the required high power density of the system can be addressed in a variety of ways, which are described in the following.

1.4.1 Synergetic Control Scheme of the PFC Rectifier Stage

In state-of-the-art two-stage EV chargers, the two stages are usually controlled independently, with the PFC rectifier stage ensuring sinusoidal input currents and at the same time regulating the voltage of the intermediate DC-link capacitor to a fixed level, which is usually well above the maximum line-to-line voltage amplitude. In particular, this implies that all three bridge-legs of the three-phase AC/DC front-end must operate with PWM (3/3-PWM). The DC/DC converter stage then draws power from the intermediate DC-link capacitor and delivers it to the output port of the converter, while ensuring a certain desired output voltage value, which follows approximately the charge-level dependent battery voltage. Although this approach is simple, it

is not optimal, since due to the wide output voltage range and the constant intermediate DC-link voltage, the DC/DC stage has to be operated with very wide voltage transfer ratios, which means that its operation is characterized by high voltage and current stresses on the components.

In order to reduce the required voltage transfer ratio of the DC/DC stage, the constant intermediate DC-link voltage can be varied within certain limits depending on the required output voltage [31]. The permissible upper limit of the intermediate DC-link voltage is thereby given by the permissible blocking voltage of the switches, whereby the lower limit is set by the peak value of the momentary line-to-line voltage of the power grid (for boost-type PFC rectifier front-ends), considering a certain margin. This means a low intermediate DC-link voltage is set for low output voltages, while the highest possible intermediate DC-link voltage is selected for the maximum output voltage. Due to this combined control of the two converter stages, the required voltage transfer ratios of the DC/DC stage are greatly reduced, which means that this stage can be operated more efficiently [31].

However, this approach can be extended, by further reducing the intermediate DC-link voltage for low output voltages such that it follows the six-pulse shape of the maximum line-to-line voltage, using the novel synergetic control of the two converter stages [32, 33], also referred to as 1/3-PWM, where the intermediate DC-link voltage is actively controlled by the DC/DC stage. At the same time, two bridge-legs in the PFC rectifier can be clamped, with only one bridge-leg being pulse width modulated, such that the switching losses can be reduced by more than 2/3, since it is always the bridge-leg with the absolute minimum voltage and current that is continuously switched. With this control strategy, the power factor correction and the resulting sinusoidal currents are therefore not only ensured by the PFC rectifier stage itself, but also by the subsequent DC/DC stage.

Due to the time-varying intermediate DC-link voltage, a small capacitor has to be employed, which on the one hand reduces the volume, but also makes the system susceptible to over-voltages when there is a fault in the grid, since now the voltage in the intermediate DC-link might rise much faster. Therefore, in order to exploit this new modulation in reality, it is critical to investigate whether it can survive common grid faults. In this work, the most critical grid conditions for three-phase rectifiers are discussed based on relevant standards, and it is shown that with minor changes, the proposed synergetic control can be used in a practical application in real environments, if appropriate protective devices and protective circuits are employed.

1.4.2 Optimal DC/DC Converter Topology

Since the only requirements for the DC/DC stage are providing galvanic isolation and a wide output voltage range to be covered, there are quite a number of possible topologies that can be used for this converter stage. The most popular topologies in charging applications are LLC resonant converters and Dual Active Bridge (DAB) converters. Both topologies are easy to control and highly efficient as long as they are operated close to unity gain, but have considerable disadvantages if a wide output voltage range has to be covered, which means that the topologies are operated in deep buck or boost-mode.

Since the voltage transfer ratio in LLC resonant converters is typically controlled by changing the switching frequency, a wide output voltage range inherently results in a wide switching frequency range, which entails several technical implementation challenges. For example, a wide switching frequency range usually results in a large EMI filter, since its volume is always defined by the first frequency component above 150 kHz, which for LLC resonant converters is in the boost-mode with the highest port voltages and a rather low switching frequency. Furthermore, alternative modulations might have to be used to reduce the switching frequency in light load conditions in order not to exceed the physical limit of the converters. Last but not least, such a wide frequency range makes the simple first harmonic analysis no longer accurate, and the more complicated time-domain analysis has to be adopted, in combination with the alternative modulation for partial power, making the whole system more complex.

In contrast to LLC resonant converters, DAB converters can be controlled with a narrower frequency range or operated at a constant frequency, since the voltage transfer ratio is primarily controlled via the phase shift between the primary-side and secondary-side voltages. However, due to the phase shift between the two port voltages, there is inevitably a considerable proportion of reactive power, which increases the RMS currents and thus the resulting conduction losses in the system. Furthermore, the trapezoidal shape of the currents in the magnetic components leads to a high harmonic content, which further increases the high-frequency conduction losses in the windings. Moreover, unlike in resonant converters, where the soft-switching capability is inherently given by the topology, a DAB converter modulation scheme ensuring ZVS for all switches over a wide operating range can be complicated, if at the same time the RMS current needs to be low. In this work, a simple yet still close-to-optimal modulation of the DAB converter is proposed and analyzed, to facilitate a performance baseline for the following research.

Given all the aforementioned disadvantages of the existing topological solutions, a new type of resonant converter is investigated in this work, referred to as the Quantum Series Resonant Converter (QSRC). It is always operated at the resonant frequency of the resonant tank, whereby the currents are perfectly sinusoidal, eliminating all harmonic losses and greatly simplifying the design of the EMI filter. The voltage transfer ratio in this converter is controlled by introducing zero-voltage intervals with a length of an integer multiple of half a resonant period, on either the primary side (buck-mode), or the secondary side (boost-mode). A straightforward control structure is proposed, utilizing a hysteresis controller to guarantee a good balance between dynamic performance and control accuracy, which is extremely simple, compared to the LLC or the DAB converter. Furthermore, by employing proper voltage patterns, the magnetizing current in the transformer can be utilized to achieve soft switching of the semiconductors over a wide operating range. Moreover, low RMS current can be ensured by keeping the QSRC in continuous conduction mode.

The only disadvantage of the QSRC is the limited control resolution, since in contrast to phase-shift- or frequency-controlled converter topologies, in which the control parameters can theoretically be resolved with any resolution, the length of the zero-voltage intervals of the QSRC can only be an integer multiple of half a resonance period. Therefore, the control parameter and thus the voltage transfer ratio are discretized in a QSRC. To mitigate this problem, one two-level bridge-leg could be replaced by a three-level T-type bridge-leg, referred to as the Hybrid Quantum Series Resonant Converter (H-QSRC), whereby more voltage levels can be utilized and the resolution of the control parameter is improved at the cost of higher complexity.

The aforementioned theoretical analysis and findings are first verified in a Pareto optimization, where virtual designs for all three topologies are selected and compared. Secondly, to experimentally verify them, two 2.5 kW isolated DC/DC converter modules with identical volumes are designed and tested, whereby the first module is implemented as a DAB converter while the second module is implemented as a QSRC. The QSRC shows clear efficiency benefits compared to the DAB converter, mainly due to the sinusoidal currents in the system and the resulting lower HF winding losses, as well as the low switching losses over a wide operating range. Furthermore, the control of the QSRC is much easier to implement since there is only one control parameter available, whereas a DAB converter is controlled via four control parameters (two duty cycles, phase shift, and switching frequency), resulting in a comparably complex control.

1.4.3 Optimal Synergetic Control of the Two-Stage System

Since the considered DC/DC stage topologies are capable of both stepping up and down the voltage, the intermediate DC-link voltage then becomes a degree of freedom, which can be chosen to optimize the stresses of both stages. For example, the rectifier stage can be operated with 1/3-PWM for the whole operating range, since this is the most efficient region for the PFC rectifier front-end, even though it might lead to high stresses in the DC/DC stage at some operation points. As the optimal operating mode (i.e., 3/3-PWM or 1/3-PWM) is determined by the loss contributions of the specific system, a 10kW EV charger module is built and analyzed, and experimentally verified and easy-to-use loss models for the VR and DAB converter are developed, which provide the basis for a comprehensive evaluation. Different synergetic operation options are compared, and the optimal overall system performance is achieved when none of the stages are over-stressed. Furthermore, it turns out that utilizing the 1/3-PWM mode improves the efficiency up to around 2% for a majority of operating points (power, output voltage), which is confirmed through measurements. Such an analysis with accurate loss models is vital for the considered two-stage system, e.g., to determine the boundary between 1/3-PWM and 3/3-PWM operation, which depends on the specific converter design and the occurring losses in the system, and also varies with the output voltage level and power.

1.4.4 Experimental Verification Utilizing New Power Semiconductor Technologies (GaN)

In contrast to the state-of-the-art EV chargers, where usually silicon (Si) or silicon-carbide (SiC) semiconductors are employed, the latest-generation 600 V GaN transistors with low switching losses are used in the hardware demonstrators (including the two 2.5 kW modules mentioned in **Sec. 1.4.2** and the 10 kW two-stage system in **Sec. 1.4.3**), to push the switching frequency to even higher values, i.e., 560 kHz, whereby the size of the magnetic components can be significantly reduced compared to state-of-the-art EV chargers. The 10 kW two-stage hardware demonstrator is realized with a power density of 9 kW/dm^3 (about 150 W/in^3), not including the coldplate-type heatsink, and a power density of 6 kW/dm^3 for the overall system, including the water-cooling heatsink, which is three times higher than the power density of state-of-the-art EV chargers [31, 34–36]. The challenges associated with using GaN switches, e.g., noise problems brought by the high switching speed, can

be tackled with proper design practices, such that the system can be operated stably.

1.5 Thesis Outline

According to the goals and contributions mentioned above, the content of the thesis is divided into three main chapters and conclusions. All the chapters can be read independently since the interdependencies have been reduced to the strict minimum.

- **Chapter 2** investigates different possible control schemes for the PFC rectifier front-end. It is divided into two parts, where the first part deals with the control of two-level six-switch converters and the second part covers the control of the three-level Vienna Rectifier, respectively. In each part, the conventional modulation, meaning switching two or three bridge-legs at the same time, by injecting different common-mode voltages, is summarized first. Subsequently, the synergetic control, meaning switching only one bridge-leg at a time by controlling the intermediate DC-link voltage with the DC/DC stage, is recapitulated and compared to the conventional ones. In the next step, to explore the applicability of the synergetic control for converters in real environments, different irregular mains conditions are considered, based on the required standards which the converters need to pass. The required protection concepts are therefore discussed and simulated in detail using the two-level converter as an example, whereby the feasibility of the proposed synergetic control in real environments can be proven.

- **Chapter 3** analyzes different DC/DC converter typologies which feature galvanic isolation. The most promising topologies are classified into two categories: phase-shifted converters, such as the DAB converters, and resonant converters, e.g., LLC converters. The feasibility of both topologies is analyzed with regard to the given specifications. Furthermore, a new type of resonant converter is investigated, referred to as the Quantum Series Resonant Converter (QSRC). The converter is always operated at the resonant frequency, whereby sinusoidal currents are guaranteed. The voltage transfer ratio is controlled by applying zero-voltage intervals to the resonant tank, but in a discretized way, i.e., the length of the zero-voltage interval can only be the integer multiple of half a resonance period. The operating principles, control scheme,

and design guidelines are discussed. To evaluate the performance of the QSRC more objectively, it is compared to the LLC and the DAB converter, first in terms of theoretical analyses, followed by experimental verifications using various hardware demonstrators. Specifically, a 2.5 kW DAB converter module and a 2.5 kW QSRC module are designed and optimized with respect to minimal circuit complexity. To be able to use the measurement results for a fair comparison of the two topologies, both systems are designed using the same switches and the same total volume of the magnetic components, whereby an identical overall power density is guaranteed. The measurements clearly show that the QSRC has a better performance in terms of efficiency for the same power density. Furthermore, the QSRC convinces with a significantly more straightforward design process and a reliable operation, which makes this topology a promising concept for industrial applications. Furthermore, to reduce the effect of discretization in the QSRC, one two-level bridge-leg is replaced by a three-level T-type bridge-leg such that more voltage levels can be utilized, referred to as the Hybrid Quantum Series Resonant Converter (H-QSRC).

- **Chapter 4** explores different ways of operating the two-stage system. The isolated DC/DC stage, capable of both stepping up and down the voltage, provides an extra degree of freedom regarding system operation. First of all, using the two-level front-end and the H-QSRC DC/DC stage, different synergetic control options are evaluated, based on the component stresses. In the next step, the GaN-based 10 kW hardware demonstrator of the complete two-stage EV charger is built, but uses different topologies. The AC/DC stage employs the Vienna Rectifier for its better performance compared to a two-level approach, while the DC/DC stage employs four DAB converters for the better dynamic performance required by the synergetic control. The system is finally operated with full power, where both the conventional control strategy and the proposed synergetic control concept are tested. Furthermore, different synergetic control options are compared with the accurate loss models, and the most efficient one occurs when none of the two stages are over-stressed, which is also verified in measurements.

- **Chapter 5** concludes the thesis and briefly summarizes the main contributions and key findings. In addition, an outlook on possible future research is provided.

1.6 List of Publications

Key insights presented in this thesis have already been published or will be published in international scientific journals, conference proceedings, or presented at workshops. The publications created as part of this thesis, or also in the scope of other related projects, are listed below.

1.6.1 Journal Papers

- Y. Li, J. A. Anderson, M. Haider, J. Schäfer, J. Miniböck, J. Huber, G. Deboy, J. W. Kolar, "Optimal Synergetic Operation and Experimental Evaluation of an Ultra-Compact GaN-Based Three-Phase 10 kW EV Charger," in *IEEE Transactions on Transportation Electrification (Early Access)*, DOI: 10.1109/TTE.2023.3297502.

- Y. Li, J. Schäfer, G. Deboy, J. W. Kolar, "Comparative Evaluation of Ultra-Wide Output Voltage Range Isolated EV Battery Chargers: Novel Quantum Series Resonant Converter vs. Dual Active Bridge Converter," under review, July 2023.

1.6.2 Conference Papers

- Y. Li, J. A. Anderson, J. Schäfer, D. Bortis, J. W. Kolar and J. Everts, "Control and Protection of a Synergetically Controlled Two-Stage Boost-Buck PFC Rectifier System Under Irregular Grid Conditions," *Proc. of the IEEE International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Nanjing, China, November 2020, DOI: 10.1109/IPEMC-ECCEAsia48364.2020.9367872

- Y. Li, J. Schäfer, D. Bortis, J. W. Kolar and G. Deboy, "Optimal Synergetic Control of a Three-Phase Two-Stage Ultra-Wide Output Voltage Range EV Battery Charger Employing a Novel Hybrid Quantum Series Resonant DC/DC Converter," in *Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Aalborg, Denmark, November 2020, pp. 1-11, DOI: 10.1109/COMPEL49091.2020.9265732

- M. Kasper, J. Azurza, G. Deboy, Y. Li, M. Haider, J. W. Kolar, "Next Generation GaN-based Architectures: From 240W USB-C Adapters to 11kW EV On-Board Chargers with Ultra-high Power Density and Wide Output Voltage Range," in *Proceedings of the Conference on Power*

Electronics and Intelligent Motion (PCIM Europe), Nuremberg, Germany, May 2022, pp. 1-10, DOI: 10.30420/565822004

Best Paper Award

1.6.3 Patents

- Y. Li, J. Schäfer, J. W. Kolar, "Power Conversion Method using a Synergetic Control of Two Power Converters," Patent Application, 2020

1.6.4 Workshops and Seminars

- Y. Li and J. W. Kolar, "Synergetically Controlled Three-Phase Boost-Buck Ultra-Wide Output Voltage Range Isolated EV Battery Charger," *Presentation at Technology Talks of Infineon Technologies Austria AG*, Villach, Austria, 2021.
- J. Azurza, M. Kasper, G. Deboy, Y. Li, J. W. Kolar, "The Path Towards 10kW 3-Phase On-Board Chargers Featuring 600V CoolGaNTM GIT HEMT Technology," *Industry Session on Chargers, Traction Inverters & DC-DC Converters for EV, 37th Applied Power Electronics Conference and Exposition (APEC)*, Houston, TX, USA, March 20-24, 2022.
- J. Azurza Anderson, Y. Li and J. W. Kolar, "Record Breaking Concepts in Power Electronics: Multi-Level Power Conversion and Synergetic Control," *Presentation at Technology Talks of Infineon Technologies Austria AG*, Villach, Austria, 2020.

2 Synergetic Control of the PFC Rectifier Input Stage

Chapter Abstract

In this chapter, different control strategies for the PFC rectifier front-end are analyzed. Starting with the simple two-level six-switch boost-type rectifier, both the conventional control and the novel synergetic control are recapitulated, followed by a comparative evaluation in terms of component stresses. To figure out the feasibility of using this novel control method in real environments, different irregular mains conditions are considered and simulated. Based on the simulation results, necessary protection schemes are discussed. Furthermore, reactive power control is also discussed. In the next step, the same is applied to the three-level PFC rectifier front-end, the Vienna Rectifier (VR), i.e., the conventional and synergetic control are discussed, followed by the comparative evaluation.

2.1 Introduction

The proliferation of Electric Vehicles (EVs) results in a growing demand for EV chargers that can handle a wide output voltage range, due to widely varying battery voltages used by different EV manufacturers. As discussed in the introduction, the state-of-the-art chargers usually consist of two stages, including an AC/DC front-end, and a DC/DC stage. For simplicity reasons, the rectifier and the DC/DC converter stage are often operated rather independently, as typically the intermediate DC-link is realized with large electrolytic capacitors that serve to decouple the control of both stages. Thus the voltage u_{xz} (see **Fig. 2.14**) is usually constant for a given operating point. The PFC

rectifier stage ensures sinusoidal input currents and at the same time regulates u_{xz} to a fixed voltage $u_{xz} = U_{xz}$ (cf. **Fig. 2.14**). The DC/DC converter stage then draws power from the intermediate DC-link capacitor and delivers the power to the output port of the converter, while regulating the output voltage, U_o, to the desired value. In order to reduce the required range of the DC/DC stage's voltage transfer ratios (which typically leads to more favorable design trade-offs), it is advantageous to adapt U_{xz} depending on the output voltage. The upper limit for U_{xz} is given by the permissible blocking voltage of the power semiconductors and the selected DC-link capacitors, and the lower limit follows from the grid voltage (i.e., the peak line-to-line voltage plus a certain margin; for a 400 V grid, $U_{xz} \geq 640$ V follows [26]).

It seems now sensible to think of ways in which the operation of the two converter stages could be further integrated, such that ultimately minimum overall losses could be achieved. A first such option [37–40] (based on [41]) reduces the functionality of the AC/DC front-end to that of a three-phase unfolder; there is no high-frequency (HF) switching of the unfolder power semiconductors and consequently near-zero switching losses. The DC/DC converters then experience time-varying intermediate DC-link voltages and ultimately ensure sinusoidal grid currents *and* regulate the output voltage. Whereas these solutions advantageously completely avoid HF switching of the three-phase unfolder (showing the same topology as the switching stage of a Vienna Rectifier) and do not require AC-side boost inductors, the intermediate DC bus voltages are varying widely, and, in particular, reach 0 V three times per grid period—and thus so does the power processed by each of the two DC/DC converters, i.e., their utilization is relatively low. Furthermore, the blocking voltage stress on the power transistors increases and a blocking capability of 600 V would no longer provide sufficient margin (assuming a 400 V grid).

For three-phase boost-type PFC rectifier front-ends (not only for VRs), it is well known that Discontinuous PWM (DPWM) methods [42,43] require HF switching of each bridge-leg only during 2/3 of the mains period, lowering switching losses accordingly. Furthermore, the intermediate DC voltage U_{xz} theoretically could be lowered to the minimum possible but still constant value, i.e., the peak value of the line-to-line voltages [26].

Instead, by using the DC/DC converter to shape u_{xz} into the six-pulse envelope of the line-to-line voltage absolute values, the currents in the two phases with the highest and the lowest instantaneous voltage, respectively, can be controlled. Accordingly, only the third phase current needs to be shaped by PWM of the corresponding AC/DC-stage bridge-leg. Advanta-

geously, this phase (for PFC operation with near unity power factor) always carries the current with the lowest absolute value. Thus, each front-end bridge-leg only operates with PWM during 1/3 of the mains period (1/3-PWM) where also the switched currents are low [44, 45]. Therefore, 1/3-PWM significantly reduces the switching losses of the AC/DC rectifier stage. Originally proposed in 2005, [44, 45], the concept has been further analyzed in [46, 47], and [33] has pointed out the close relationship to the integrated active filter (IAF) [48] topology. Furthermore, [26] provides a detailed comparison with 2/3-PWM (DPWM), and [49, 50] analyze the behavior under irregular grid conditions, [51] employs a delta-switch front-end converter, and [52] details a generalized carrier-based modulation implementation. Whereas the former references all discuss non-isolated systems, i.e., with non-isolated DC/DC converter stages, the same advantageous reduction of the front-end stage's switching losses can be achieved with isolated DC/DC stages shaping the intermediate DC-link voltage accordingly [53–55].

In this chapter, the synergetic control, i.e., 1/3-PWM is analyzed in detail, with a focus on the PFC rectifier front-end of the two-stage system, starting from the two-level six-switch boost converter in **Sec. 2.2**. The conventional modulation methods, i.e., 3/3-PWM and 2/3-PWM, are summarized in **Sec. 2.2.1**. Then the synergetic control that allows to switch only one half-bridge at a time, referred to as 1/3-PWM, is introduced in **Sec. 2.2.2**, followed by the comparative evaluation of component stresses in **Sec. 2.2.3**. Although this concept has been proven to work correctly for ideal three-phase mains conditions, it is unclear whether it can safely operate under irregular three-phase grid conditions such as heavy harmonic distortions, unbalances, phase failures, and grid overvoltages caused by, e.g., lightning. Hence, **Sec. 2.2.4** focuses on the operation of the proposed boost-buck converter for an application subject to a wide variety of three-phase grid disturbances. Comprehensive analysis with respect to irregular grid conditions is performed, resulting in a slight modification of the converter' s front-end and its control structure in order to be able to handle faulty mains conditions. The proposed hardware and control modifications enabling the proper converter functionality under regular and irregular grid conditions are verified by circuit simulations. Finally, design guidelines are given for the hardware implementation of a resilient three-phase grid-interfaced EV charger that fulfills all required grid standards. Furthermore, reactive power control is also discussed in **Sec. 2.2.5** based on the slightly modified control structure, which can provide ±180° phase-shifted currents. As the second part of this chapter, **Sec. 2.3** recapitulates the conventional and synergetic control of the VR, followed again by the

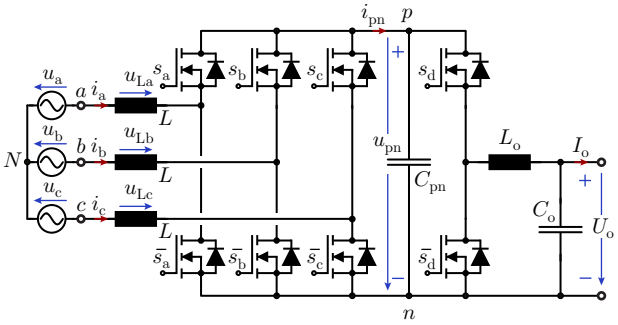


Fig. 2.1: Topology of the Boost-buck-(Bb)-VSR, consisting of a boost-type three-phase PFC rectifier front-end, followed by a subsequent DC/DC buck converter.

comparative evaluation of component stresses. The DC/DC stage is treated as general blocks, assuming that it can handle the required dynamics, since its detailed implementation is irrelevant to the operation of the VR. Finally, conclusions are drawn in **Sec. 2.4**.

2.2 Two-Level Converter Topology

In the case of an EV charging park, the galvanic isolation of the individual charging ports can be provided by a medium voltage (MV) transformer where non-isolated AC/DC converters are directly connected to individual sets of three-phase secondary-side windings [56]. Considering a transformer secondary line-to-line RMS voltage of 400 V and a widely varying battery voltage of 200 V...1000 V (as shown in **Fig. 1.2**), the non-isolated AC/DC converter has to feature boost and buck capability, in order to allow an adaption of the rectified transformer output voltage to the EV battery voltage level. In **Fig. 2.1**, the conventional two-stage solution of such a non-isolated AC/DC converter system is shown. It consists of a boost-type three-phase PFC rectifier front-end, followed by a subsequent DC/DC buck converter that regulates the output voltage, hereafter referred as the Boost-buck Voltage Source Rectifier (Bb-VSR).

2.2.1 Conventional Control

As discussed in the introduction, the PFC rectifier front-end generates a constant intermediate DC-link voltage u_{pn} in between $u_{\mathrm{ll,max}}$ and $U_{\mathrm{o,max}}$, according to the required momentary output voltage U_{o}, where $u_{\mathrm{ll,max}}$ and $U_{\mathrm{o,max}}$ denote the maximum grid line-to-line voltage and the maximum required output voltage, respectively. The subsequent DC/DC buck converter then controls the output voltage in case of $U_{\mathrm{o}} < u_{\mathrm{ll,max}}$. Consequently, a wide output voltage range can be covered. For the two-level six-switch boost converter, different modulation methods have been proposed to improve the performance, mainly by injecting different common-mode (CM) mode voltages. Starting from the basic modulation, where all three half-bridges are switched simultaneously, i.e., 3/3-PWM, adding CM mode voltages increases the linear modulation range, and the minimum required u_{pn} can be decreased from $2\hat{u}_{\mathrm{n}}$ to as low as $\sqrt{3}\hat{u}_{\mathrm{n}}$ (where u_{n} denotes the phase voltages $u_{\mathrm{a,b,c}}$). To reduce the switching losses, different clamping strategies have been proposed as Discontinuous PWM (DPWM) [42, 43, 57–59], where only two half-brides are switching at a time, giving at least 33% reduction of the switching losses. In the meantime, the sinusoidal currents at the input are still maintained. However, especially during *buck − mode* operation, i.e., when the output voltage U_{o} is below the instantaneous maximum line-to-line voltage $u_{\mathrm{ll,max}}$, the maximum achievable efficiency is clearly limited by the two-stage energy conversion of such EV charger systems. This is particularly the case because both converter systems are controlled separately without exploiting the potential advantages that would result from a so-called synergetic control, i.e. a joint control of the two converter stages that might be advantageous in terms of the overall system efficiency. For this reason, it is investigated in the following, what kind of advantages can be achieved by such a synergetic control strategy.

2.2.2 Synergetic Control

In order to reduce the converter losses, a so-called *synergetic* control strategy was presented in [33] for the converter topology shown in **Fig. 2.1**, that allows to only switch one of the three rectifier stage bridge-legs. This is achieved by generating a six-pulse voltage shape u_{pn} in the intermediate DC-link, which follows the instantaneous maximum line-to-line voltage $u_{\mathrm{ll,max}}$. The pulsating voltage is enforced by controlling the input power of the step-down converter, which is why a smaller DC-link capacitor C_{pn} has to be used for the synergetic control compared to the one in conventional solutions, in order to limit the required power fluctuation (the power drawn from the mains is still constant)

in the DC/DC output stage. Besides the smaller DC-link capacitor, no further adaption of the converter topology is required, which is why the conventional topology of **Fig. 2.1** can be used even for the synergetic control strategy (cf. **Fig. 2.2**). Consequently, the high-side switch of the PFC rectifier stage half-bridge with the most positive phase voltage and the low-side switch of the half-bridge with the most negative phase voltage can be continuously turned on within a 60°-wide interval (cf. 1/3-PWM in **Fig. 2.3**). The input currents of the phases with the most positive and negative voltages are then controlled by u_{pn}, which in turn is controlled by the subsequent DC/DC buck converter. Hence, only the input half-bridge corresponding to the medium input phase voltage has to be pulse-width modulated in order to control the corresponding input current, which means that only one out of the three PFC rectifier bridge-legs, and/or the bridge-leg carrying the lowest current is switching at any point in time (1/3-PWM operation).

However, when the output battery voltage is higher than the instantaneous maximum line-to-line voltage ($U_{\mathrm{o}} > u_{\mathrm{ll,max}}$), i.e., for $boost - mode$, the three-phase PFC rectifier steps up the input voltage by switching either two or three of its bridge-legs (2/3 or 3/3-PWM, and/or Discontinuous or Continuous PWM [57]), such that the constant DC-link voltage equals the battery voltage ($u_{\mathrm{pn}} = U_{\mathrm{o}}$), and the buck-stage is clamped by turning its high-side switch on (cf. **Fig. 2.3**).

A cascaded control scheme for the Bb-VSR, similar to the one in **Fig. 2.2**, was initially presented in [33] focusing mainly on buck-mode operation, i.e., $U_{\mathrm{o}} < u_{\mathrm{ll,max}}$, and proved to work correctly for ideal mains conditions. A demonstration of the operation of the Bb-VSR under ideal mains conditions is shown in **Fig. 2.3**, where in extension of [33] also a smooth transition of the output voltage U_{o} between buck and boost-mode operation is obtained. All presented simulations are considering a system of 10 kW rated power, according to the specifications of **Fig. 1.2**.

In the following, the main advantages of the proposed synergetic control over the conventional approach are summarized, but also the challenges that come along with the 1/3-PWM operation are discussed.

2.2.3 Comparative Evaluation

In order to demonstrate the potential of the novel synergetic control, i.e., 1/3-PWM, the occurring losses can be compared with those of the conventional modulation. In [33], the losses and the efficiencies of the 3/3-PWM, 2/3-PWM, and 1/3-PWM are calculated based on a virtual system rated at 10 kW, which

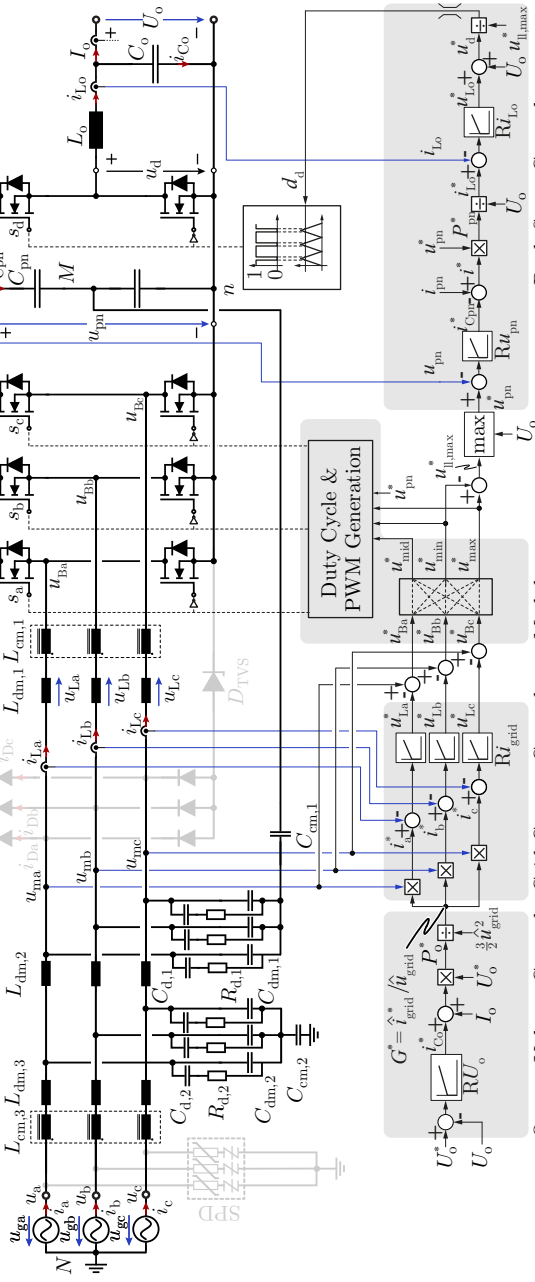


Fig. 2.2: Cascaded output voltage control structure for the Bb-VSR, where the required measurements are indicated in blue. The voltages across the capacitors C_{dm1} are measured ($u_{\mathrm{ma,mb,mc}}$) and used as phase voltages in the control.

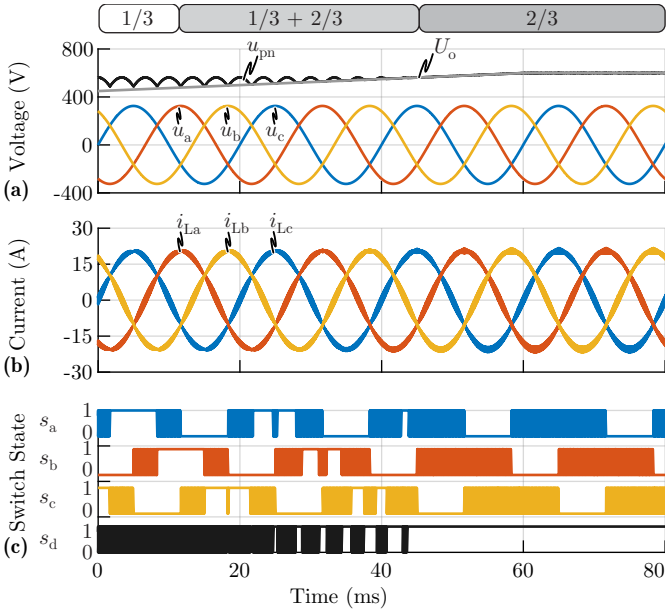


Fig. 2.3: Simulation of the characteristic waveforms of the Bb-VSR: **(a)** the input grid voltages $u_{a,b,c}$ (measured at the converter input, between line to ground), intermediate DC-link voltage u_{pn}, output battery voltage U_o and **(b)** boost inductor currents $i_{La,Lb,Lc}$, **(c)** gate signals of the three-phase PFC rectifier stage and the buck-stage. The main simulation parameters are: switching frequency f_{sw} = 140 kHz (for both converter stages), C_{pn}=10 µF, L_o=100 µH and C_o= 5 mF (to emulate the behaviour of batteries), for other components refer to **Tab. 2.3**. When $U_o < u_{ll,max}$, only one of the PFC rectifier bridge-legs is operating at any point in time (1/3-PWM operation) together with the buck-stage bridge-leg. When $U_o > u_{ll,max}$, the high-side switch of the buck-stage is clamped, and two out of three rectifier stage bridge-legs are switching (2/3-PWM, also known as Discontinuous PWM [57]).

was initially designed for operation with 3/3-PWM. Compared to 3/3-PWM, the switching losses are reduced by a factor of 2 for 2/3-PWM and a factor of 12 for 1/3-PWM. The enormous reduction in switching losses in 1/3-PWM is due to the actively switched bridge-leg having the minimum phase current and voltage. Furthermore, since the switching transitions happen only in the near vicinity of the zero crossings of the phase currents, soft switching can be achieved to a large extent due to the current ripples in the input inductors. Reference [26] presents a more comprehensive analysis of the component

stresses by means of analytical solutions, where the switching losses are assumed to be independent of current ripples, and is summarized in **Tab. 2.1** for 2/3-PWM and 1/3-PWM.

In **Tab. 2.1**, f_{sw} is the switching frequency, while I_{avg} and $\hat{I}$ are the average and the peak value of the sinusoidal input currents, respectively ($I_{avg} = \frac{2}{\pi}\hat{I}$). Furthermore, M is the modulation index, and $\hat{U}$ is the peak value of the grid (input) phase voltages $u_{a,b,c}$. It needs to be noted that here the modulation index M is not defined as in most three-phase converters, but rather as the ratio between the amplitude of the phase voltage $\hat{U}$ and half of the output voltage U_o, in order to characterize the component stresses of the DC/DC stage. Additionally, the intermediate DC-link voltage is chosen to be at its minimum value, i.e., $\sqrt{3}\hat{U}$ for 2/3-PWM as shown in **Tab. 2.1**. The switching losses of the PFC rectifier stage consist of two parts, $P_{sw} = P_{sw,0} + P_{sw,1}$, with $P_{sw,0}$ representing the current-independent capacitive switching loss contributions, while $P_{sw,1}$ denotes the current-dependent switching losses, which are assumed to scale linearly with respect to the switched currents. It can be seen that the switching losses of the 1/3-PWM are reduced by more than 50% compared to 2/3-PWM, as only the phase with the lowest voltage and current is actively switched. Furthermore, the switching losses are reduced for 1/3-PWM by more than 66% compared to 3/3-PWM, though not shown here. $I_{TDC1,RMS}$ and $I_{TDC2,RMS}$ represent the RMS currents in the upper and lower switch of buck-stage respectively, while $I_{TAC1,RMS}$ and $I_{TAC2,RMS}$ represent the RMS currents in the upper and lower switch of one half-bridge leg of the PFC rectifier stage respectively. From the RMS currents of the switches in both stages, it can be seen that the conduction losses in the two types of modulation only change marginally, which is why they can be assumed to be constant. Consequently, using 1/3-PWM results in significant loss reduction by only changing the control of a three-phase converter system, which is why it seems to be a promising solution for practical applications. Therefore, it is worthwhile to investigate whether it can be applied in real environments under all kinds of irregular mains conditions, a prerequisite for commercial products, and discussed in the next section.

2.2.4 Irregular Mains Conditions

Given that the Bb-VSR operates at the modulation index limit, there is no DC-link voltage margin that would allow to control the input current in case of a grid overvoltage. Moreover, a small DC-link capacitance is required by the synergetic control (unlike conventional boost converters, where typically

Tab. 2.1: Comparison of the Semiconductor Stresses of 2/3 and 1/3-PWM, Where the Switching Losses are Given for the PFC Rectifier Stage.

Parameter		Equation		Difference	Condition
		2/3	1/3		
Switching	$P_{\mathrm{sw},0}$	$\frac{2}{3} \cdot k_{\mathrm{sw},0} \cdot f_{\mathrm{sw}}$	$\frac{1}{3} \cdot k_{\mathrm{sw},0} \cdot f_{\mathrm{sw}}$	−50%	/
Losses P_{sw}	$P_{\mathrm{sw},1}$	$\left(1 - \frac{\sqrt{3}}{4}\right) k_{\mathrm{sw},1} \cdot I_{\mathrm{avg}} \cdot f_{\mathrm{sw}}$	$\left(1 - \frac{\sqrt{3}}{2}\right) k_{\mathrm{sw},1} \cdot I_{\mathrm{avg}} \cdot f_{\mathrm{sw}}$	−76%	/
DC/DC Stage	$I_{\mathrm{TDC1,RMS}}$	$I_{\mathrm{o}} \sqrt{\frac{2}{\sqrt{3}M}}$	$I_{\mathrm{o}} \sqrt{\frac{6 \ln 3}{\sqrt{3}\pi M}}$	+2.37%	$U_{\mathrm{o}} = 400\,\mathrm{V}$, $\hat{U} = 325\,\mathrm{V}$, $M = \frac{\hat{U}}{(U_{\mathrm{o}}/2)} = 1.625$
Switch Current	$I_{\mathrm{TDC2,RMS}}$	$I_{\mathrm{o}} \sqrt{1 - \frac{2}{\sqrt{3}M}}$	$I_{\mathrm{o}} \sqrt{1 - \frac{6 \ln 3}{\sqrt{3}\pi M}}$	−6.63%	
AC/DC Stage	$I_{\mathrm{TAC1,RMS}}$	$\frac{\hat{I}}{\sqrt{2}} \sqrt{\frac{3}{2\pi}}$	$\frac{\hat{I}}{\sqrt{2}} \frac{1}{\sqrt{2}}$	+2.28%	$u_{\mathrm{pn},2/3} = \sqrt{3}\hat{U}$,
Switch Current	$I_{\mathrm{TAC2,RMS}}$	$\frac{\hat{I}}{\sqrt{2}} \sqrt{1 - \frac{3}{2\pi}}$	$\frac{\hat{I}}{\sqrt{2}} \frac{1}{\sqrt{2}}$	−2.23%	$\hat{U} = 325\,\mathrm{V}$

a relatively large capacitance is present in the DC-link [60]), whose voltage reacts sharply to inrush currents. Hence, the question arises if this is a feasible solution when operated in a grid with unbalanced three-phase voltages, harmonic distortions, and voltage surges caused by, e.g., lightning, which could cause permanent damage to the hardware.

Hence, in this section, a comprehensive approach is taken for both the topology and the control structure, to analyze its robustness under irregular three-phase mains conditions, as this is essential to the applicability of the proposed system as an EV charger. The most important critical grid conditions for three-phase rectifiers are summarised in **Sec. 2.2.4.1** and are discussed based on related standards. Subsequently, the Bb-VSR and its control structure are tested by means of simulations for a selection of the most critical grid irregularities: harmonics in **Sec. 2.2.4.2**, voltage dips and phase voltage interruptions in **Sec. 2.2.4.3**, and overvoltages in **Sec. 2.2.4.4**, verifying that the proposed approach with the corresponding modifications is indeed suitable for ensuring reliable operation. Finally, **Sec. 2.2.4.4** provides design guidelines for the resilient design of an overvoltage clamping circuit, which are also useful for conventional boost-type grid-connected three-phase PFC rectifiers.

2.2.4.1 Overview of the Immunity Requirements in Standards for Power Supplies Under Irregular Grid Conditions

The standards of immunity requirements [61–64] specify different irregular grid conditions that power supplies need to withstand, among which the IEC standards are mainly used in European countries, while similar IEEE standards are widely applied in North America. In this section, the IEC standards will be used to evaluate different critical conditions. As the Bb-VSR is mainly designed for charging applications, the standards dedicated for this purpose will be considered here [61, 62].

The grid faults mentioned in [61, 62] can be classified into two main categories: voltage dips and interruptions, and overvoltages. In addition, there are also standards specifying immunity requirements for harmonic distortions of the three-phase grid voltages [65, 66], which, however, are not mandatory for EV chargers. Nevertheless, they are widely applied for equipment in medical and semiconductor industry applications, and must be considered for equipment containing phase-controls or other zero-crossing detection techniques [63], which is the case for 1/3-PWM operation of the rectifier stage. Therefore, they are considered in this section as well. **Tab. 2.2** summarizes the classification of all considered irregular grid conditions. In order to

Tab. 2.2: Classification of Irregular Grid Conditions and Immunity Requirements for EV Chargers.

Phenomenon		**Standards (IEC 61000-)**	**On-Board Charger**	**Off-Board Charger**	**Performance Criteria**
Harmonics		2-4, 4-13	×	×	/
Voltage Dips & Interruptions	Voltage Dips	4-11 (phase current < 16 A) 4-34 (phase current > 16 A)	×	✓	B
	Interruptions		×	✓	C
	Voltage Variations		×	×	/
Overvoltages	Voltage Surge	4-5	✓	✓	B
	Fast Transients or Bursts	4-4	✓	✓	B
	Oscillatory Overvoltages	4-12, 4-18	×	×	/

Tab. 2.3: Component Values for the Considered EMI Filter.

Component	Parameter	Component	Parameter
$L_{\mathrm{dm},1}$	163.5 µH	$C_{\mathrm{dm},1}$	850 nF
$L_{\mathrm{cm},1}$	2.9 mH	$C_{\mathrm{cm},1}$	87 nF
$C_{\mathrm{d},1}$	212 nF	$R_{\mathrm{d},1}$	66.1 Ω
$L_{\mathrm{dm},2}$	29 µH	$C_{\mathrm{dm},2}$	2.1 µF
$C_{\mathrm{d},2}$	517 nF	$R_{\mathrm{d},2}$	17.8 Ω
$C_{\mathrm{cd},2}$	5 nF	$R_{\mathrm{cd},2}$	199 Ω
$L_{\mathrm{dm},3}$	11.7 µH	$L_{\mathrm{cm},3}$	2 mH

evaluate the immunity capability of the equipment under test (EUT), three performance criteria are defined: A (normal performance), B (degradation of performance during the test is allowed, automatic recovery required), and C (loss of function is allowed, restored by simple operations). These criteria are specified in **Tab. 2.2** for each aforementioned grid irregularity. Depending on the location of the charger (on-board or off-board), the requirement is different, which is indicated with "✓" (obligatory) or "×" (not obligatory) for each test. The detailed test procedures are specified in the IEC61000-4 series, which will be discussed and simulated in the following sections for all three main categories of grid irregularities (harmonics, voltage dips and interruptions, and overvoltages).

However, in order to get conclusive results from the simulations of the irregular grid conditions, not only should the aforementioned two converter stages be taken into account, but also the upstream EMI filter needs to be considered. This is especially important for abrupt changes in the grid voltages, as the EMI filter defines the transient behavior of the total converter system to a large extent. Thus, an EMI filter is placed in front of the converter, using the same structure and component values as in [67], which are repeated in **Tab. 2.3**. The noise level is verified to comply with CISPR 11, Class A, EMI requirements. To take into account the effects of inrush currents, the inductors in the EMI filter, except for $L_{\mathrm{dm},1}$ and $L_{\mathrm{cm},1}$ which are protected by the bypass diodes ($D_{\mathrm{a,b,c}}$), are simulated with the reluctance models using saturable cores [68–71], with saturation characteristics extracted from measurements. As a reference, $L_{\mathrm{dm},2}$ and $L_{\mathrm{dm},3}$ drop to 50% of the nominal value

at 45 A and 30 A respectively, while $L_{\mathrm{cm},3}$ drop to 50% of the nominal value at 110 A differential mode current or 150 mA common-mode current.

2.2.4.2 Mains Voltage Harmonics

There are two relevant standards concerning grid voltage harmonics: one specifies the compatibility levels [65], and the other one specifies the immunity levels [66]. The given test voltage levels of both standards are summarized in **Tab. 2.4** for the first five odd non-multiple-of-three harmonics. The test levels for compatibility are lower than the respective test levels for immunity, but in contrast to the immunity test levels, where the standard specifies two particular ways to combine the harmonics, the compatibility test levels can be combined arbitrarily (regarding mutual phase shifts) in order to test the worst-case scenario. As for 1/3-PWM operation, it is crucial to ensure the automatic clamping of the required phases with the respective highest and lowest voltage values in all operating conditions. Thus, a worst-case grid voltage waveform is created, where the phase voltages $u_{\mathrm{a,b,c}}$ intersect three times every 60° (cf. **Fig. 2.4**). Hence, the clamped phase changes three times instead of only once every 60°, as in nominal operation. This waveform was created by superimposing the 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} voltage harmonics to the 50 Hz fundamental voltage component, with the maximum amplitudes specified in [65] and phases specifically chosen to create a repeating cross-over between the phase voltages. Accordingly, in order to still achieve a resistive input behavior of the EV charger, the intermediate DC-link voltage u_{pn} has to be able to follow the maximum instantaneous (distorted) line-to-line voltage. **Fig. 2.4** shows the simulated waveforms of u_{pn} and the resulting input phase currents $i_{\mathrm{a,b,c}}$. It can be seen that the DC-link voltage controller dynamics is high enough and ensures an ohmic mains behavior of the EV charger.

2.2.4.3 Mains Voltage Dips and Interruptions

Voltage dips and short interruptions originate primarily from short circuits or sudden large load steps in the network [72, 73]. This kind of fault is classified into three sub-categories [72, 73]: voltage dips, interruptions, and voltage variations. Voltage dips refer to one-phase voltage dips, including line-to-line dips and line-to-neutral dips, whereby the latter is obviously not required for power supplies without a neutral connection. Interruptions stand for the dropout of all three phases at the same time, lasting for 250 (50 Hz) or 300 (60 Hz) cycles. During this time interval, the converter does not have to continue working. As it is similar to the start-up process, this test will not be

Tab. 2.4: Test Levels for Harmonics.

Order	**Compatibility** Test levels% U_n	**Immunity** Test levels% U_n
5	8	12
7	7	10
11	5	7
13	4.5	7
17	4	6
...	...	...

further discussed here. The third phenomenon, voltage variations, represents a voltage sag of all three phases happening simultaneously by the same amplitude, usually caused by continuously varying loads connected to the network [72, 73]. The preferred test level is 70% of the nominal voltage, with a voltage fall time of 1 µs to 5 µs, staying at the reduced voltage for one cycle and then gradually going back to normal during 25 cycles. It needs to be noted that this test is not obligatory. Moreover, it does not entail extra challenges for the proposed synergetic Bb-VSR, i.e., the converter which survives the voltage dip tests can also pass the voltage variation tests. Therefore, this grid irregularity will not be further discussed here.

For the following simulations of the voltage dips, the test generator is directly connected to the EUT, and maintains low output impedance over the fault. Therefore, to consider the worst-case scenario, the grid impedance is not included (which would further limit the inrush currents in a real installation), and the inrush currents are only limited by the EMI filter. Furthermore, it is assumed that the fault occurs at the peak of the line-to-line (phase-to-phase) voltage (*phase* and *line* are synonymously used in the following).

The voltage dip tests should be performed for each phase-to-neutral voltage (when a neutral conductor is present) and phase-to-phase voltage. The preferred test levels and durations of class 3 (highest level, harshest environment, for 50 Hz mains frequency) are: 0% during 1/2 cycle, 0% during 1 cycle, 40% during 10 cycles, 70% during 25 cycles and 80% during 250 cycles. The rise and fall times are between 1 µs to 5 µs. As for 1/3-PWM operation, it is especially important to see how the controller reacts for a phase-to-phase voltage dip to 0%, when two phases have the same voltage and there is no phase with a voltage in between (which would be high-frequency modulated

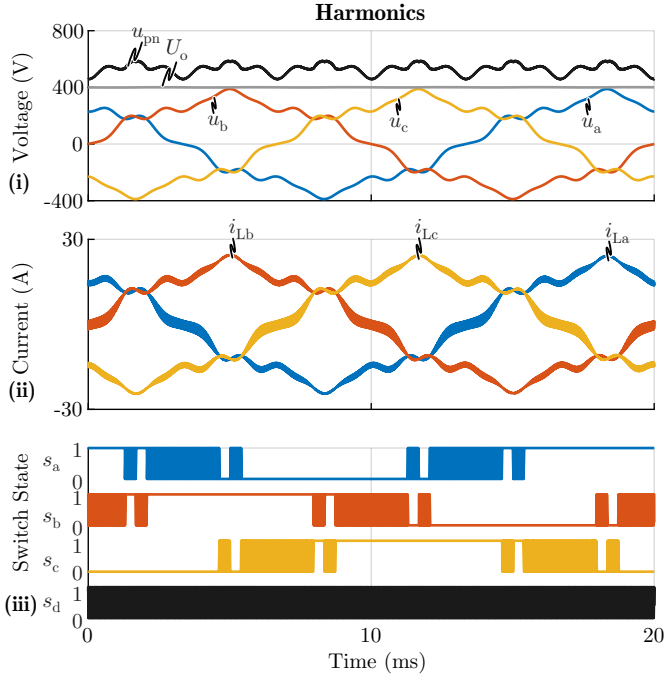


Fig. 2.4: Simulation waveforms for voltage harmonics occurring in the three phases: **(i)** grid phase voltages $u_{a,b,c}$ (measured at the input of converter, from line to ground), intermediate DC-link voltage u_{pn}, and output voltage U_o (controlled to 400 V), **(ii)** currents $i_{La,Lb,Lc}$ in the boost inductors of the PFC rectifier stage and **(iii)** gate signals of the three-phase PFC rectifier and the buck-stage.

in normal operation). Thus, the 0% line-to-line voltage dip between phase a and b is simulated and shown in **Fig. 2.5**. There are two acceptable methods presented in [72, 73] to perform the voltage dip tests as shown in **Fig. 2.6**, and the more realistic one [72, 73] (method 2) is chosen for the simulation in **Fig. 2.5**. It can be noted that, using this method for the 0% line-to-line voltage dip test, both the amplitude and the phase of the affected two voltages (u_a and u_b) change when the fault happens, ending up in the same resulting vector, which is 180° phase-shifted with respect to the remaining phase voltage (u_c), as can be seen in **Fig. 2.5(i)**.

According to the control structure of **Fig. 2.2**, the reference voltage u^*_{pn} is defined as the maximum of the output voltage U_o and the maximum line-to-

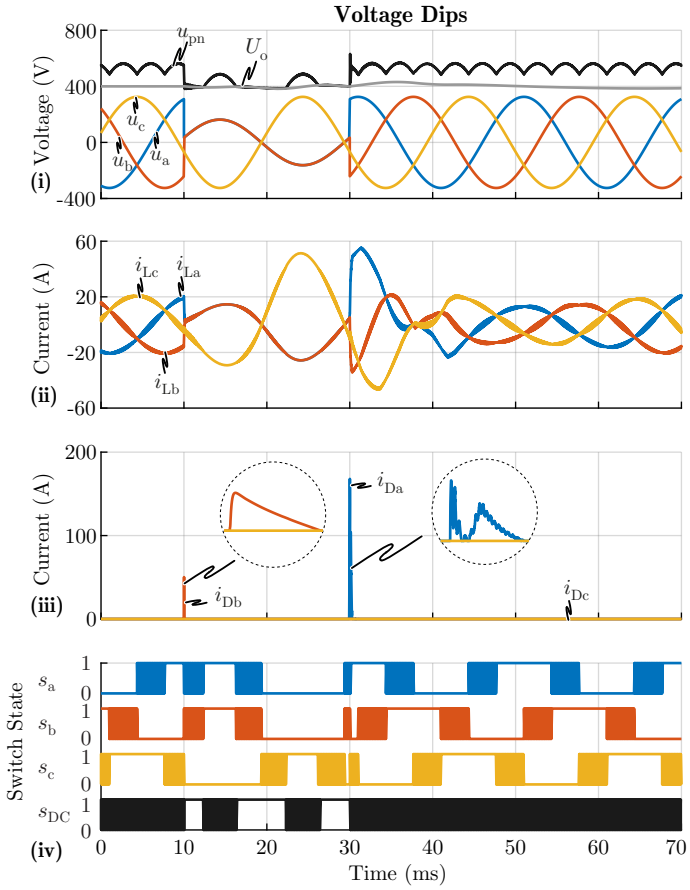


Fig. 2.5: Simulation waveforms for phase-to-phase voltage dip occurring from phase a and b: **(i)** grid phase voltages $u_{a,b,c}$ (measured at the input of converter, from line to ground), intermediate DC-link voltage u_{pn}, and output voltage U_o (controlled to 400 V), **(ii)** currents $i_{La,Lb,Lc}$ in the boost inductors of the PFC rectifier stage, **(iii)** currents in the upper bypass diodes of $D_{a,b,c}$ (cf. **Fig. 2.2**), and **(iv)** gate signals of the three-phase PFC rectifier and the buck-stage.

line input voltage (reference) $u^*_{ll,max} = u^*_{max} - u^*_{min}$, which in turn is generated from the rectifier voltage references (u^*_{Ba}, u^*_{Bb} and u^*_{Bc}). Thus, due to the loss of u_{ab}, the maximum line-to-line voltage ($u_{ac} = u_{bc} = -3/2\, u_c$) no longer

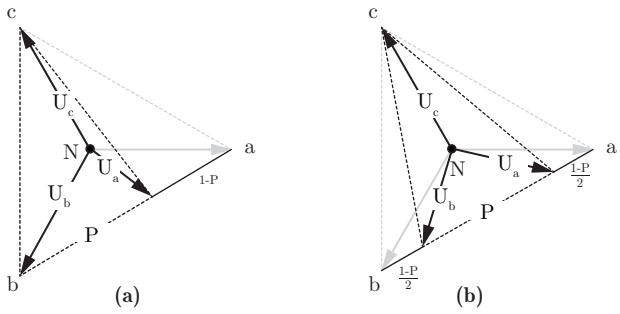


Fig. 2.6: Phasor diagrams for phase-to-phase voltage dip between phase a and b, where P is the relative amount of the remaining u_{ab}: **(a)** method 1 (easier to realize in test labs [73]), and **(b)** method 2 (more realistic [73], simulated in **Fig. 2.5** for P = 0).

features a six-pulse shape, but instead varies with twice the mains frequency. Since it reaches zero every half mains cycle, it inherently intersects with U_o, whereby the converter always alternates between buck and boost-mode operation. Since the controller is designed to ensure the emulation of an ohmic load, the currents in three phases are changing in the same way as the voltages. However, the converter still manages to draw sinusoidal currents from the mains, as shown in **Fig. 2.5(ii)**. It needs to be noted that, as there is no voltage in between u_{max} and u_{min}, when u^*_{pn} is set to follow $u^*_{ll,max}$, all three half-bridges in the rectifier stage are clamped. This proves the proper operation of the clamping function even under fault conditions.

Furthermore, due to the pulsating input power with twice the mains frequency, the output voltage starts to fluctuate. With the high bandwidth of the output voltage control, the controller would try to correct this low-frequency ripple in the output voltage, leading to distortions in the input phase currents. Accordingly, there is a trade-off between keeping currents sinusoidal and the fast control of the output voltage [74] and/or the amount of installed output capacitance C_o.

During the fault, u^*_{pn} is set by the controller to U_o when $u^*_{ll,max} < U_o$. Hence, when the voltage steps back to its nominal value, there will be a large voltage difference between the instantaneous maximum line-to-line voltage $u_{ll,max}$ and u_{pn}, especially when U_o is low and $u_{ll,max}$ is high. Since u_{pn} inherently follows $u_{ll,max}$, the controllability of the input currents is temporarily lost, generating a large inrush current, which is only limited by the EMI filter. To prevent these large inrush currents from flowing through the semiconductors

and therefore, potentially damaging them, bypass diodes $D_{\mathrm{a,b,c}}$, which can handle such surge currents have to be placed between the grid interface and the input of the converter, as shown in **Fig. 2.2**. Similar measures are used for the protection of single-phase PFC rectifiers at the end of a hold-up period [60]. It can be seen in **Fig. 2.5(iii)**, that when the voltage comes back, the inrush current up to 170 A (i_{Da}) flows through the bypass diodes instead of the less robust MOSFETs. With an appropriate selection of the bypass diodes, as e.g. $P600M$ [75] with a surge current capability of 600 A for 8.3 ms, the Bb-VSR can survive the voltage dip test.

In buck-mode, u_{pn} closely follows the line-to-line voltage. For the considered power rating and a realization using SiC MOSFETs, the voltage drop across the first stage of the EMI filter (L_{dm1} and L_{cm1}) and the MOSFETs can easily reach 2 V~3 V (during clamping), which is higher than the forward voltage drop of most diodes. Therefore, it is likely for the bypass diodes $D_{\mathrm{a,b,c}}$ to conduct at normal operation, making it difficult to control the grid currents. Therefore, in order to ensure that these diodes are blocking in nominal operation, transient-voltage-suppression (TVS) diodes (D_{TVS}) with a higher breakdown voltage of 5 V are placed in the bypass path, which can easily withstand surge currents of hundreds of amperes (e.g., $SMCJ5.0A\text{-}TR$ from STMicroelectronics [76]).

2.2.4.4 Overvoltages

There are mainly two kinds of overvoltages that can occur in a grid [77]: oscillatory and impulsive overvoltages. The oscillatory overvoltages result from, e.g., capacitor bank energization, whereby the impulsive overvoltages are usually caused by lightning strikes. As shown in **Tab. 2.2**, it is obligatory for power supplies to withstand two different kinds of impulsive overvoltages, as defined in [78] and [79, 80]. The first one, referred to as *surge*, features voltage pulses in the microsecond range, while the second one, referred to as *fast transients* or *bursts*, is in the nanosecond range. Due to the short duration and low energy of the latter one, a converter that survives the voltage surge, should also survive fast transients or bursts at the same voltage level. Therefore, in the following sections, only the surge voltage pulse tests will be analyzed. The test levels are shown in **Tab. 2.5** for both line-to-line tests (L-L) and line-to-ground tests (L-G), depending on the environment and the charger type.

Test Setup The required test setup is shown in **Fig. 2.7(a)** [78]. The combination wave generator (CWG) [81], which is used for generating the voltage

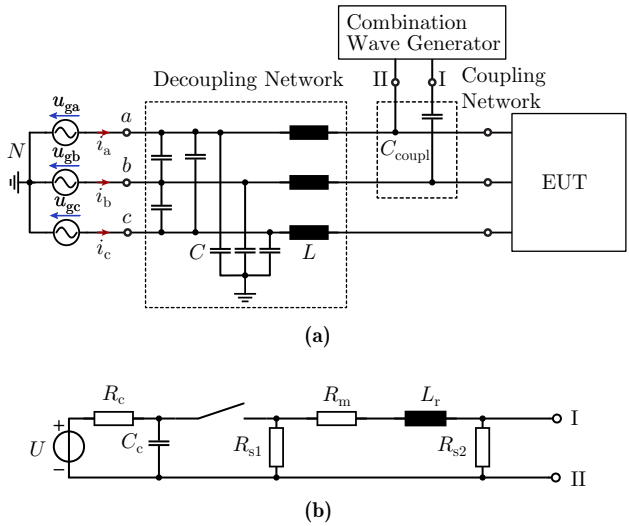


Fig. 2.7: Test setup for surge immunity tests with **(a)** connections of the three-phase voltage source, decoupling network ($C = 30\,\mu F$, $L = 1.5\,mH$), combination wave generator (CWG), coupling network (a $18\,\mu F$ capacitor C_{coupl} for line-to-line tests, or a $9\,\mu F$ capacitor C_{coupl} in series with a $10\,\Omega$ resistor for line-to-ground tests), and the EUT, **(b)** the schematic of the CWG ($R_c = 1000\,\Omega$, $C_c = 9.98\,\mu F$, $R_{s1} = 9.39\,\Omega$, $R_m = 0.83\,\Omega$, $L_r = 10.7\,\mu H$, $R_{s2} = 25.5\,\Omega$).

pulses, is connected to the EUT through the coupling network. The line-to-line surge tests require a coupling capacitor C_{coupl} of $18\,\mu F$, while the line-to-ground surge test requires a $9\,\mu F$ coupling capacitor in series with a $10\,\Omega$ resistor. The decoupling network [82], comprising inductors and capacitors, is placed in front of the CWG to prevent its high current and voltage from damaging the three-phase voltage source. The schematic of the CWG is shown in **Fig. 2.7(b)**. The voltage surge is generated by releasing the energy in the precharged capacitor C_c. Hence, after the electronic switch is turned on, the output voltage of the CWG rises to the required peak value (test level) in $1.2\,\mu s$, before decaying to half of its peak value within the following $50\,\mu s$. Due to different configurations of the coupling network, the current sourcing capability of the CWG is different in line-to-line and line-to-ground tests. Even though the line-to-ground tests specify higher voltage, their short-circuit currents are much lower than for the line-to-line tests.

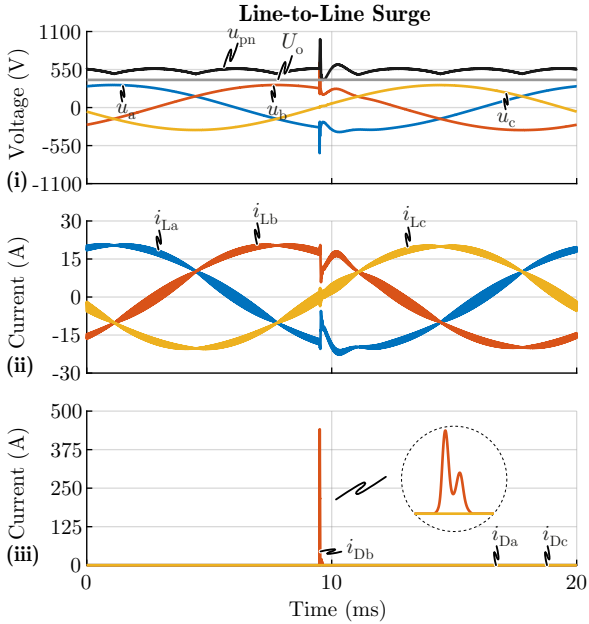


Fig. 2.8: Simulation waveforms for line-to-line surge test at 1 kV, applied between phase a and b: **(i)** grid phase voltages $u_{a,b,c}$ (measured at the input of the converter, from line to ground), intermediate DC-link voltage u_{pn}, and output voltage U_o (controlled to 400 V), **(ii)** currents $i_{La,Lb,Lc}$ in the boost inductors of the PFC rectifier stage, **(iii)** currents in the upper bypass diodes of $D_{a,b,c}$ (cf. **Fig. 2.2**). No Surge Protection Devices (SPDs) are considered.

Simulation Results for On-Board Chargers and Residential Off-Board Chargers Without Surge Protection Devices (SPDs) The simulations are first carried out for voltage impulses at lower test levels, i.e., a line-to-line voltage surge of 1 kV between phases a and b, and a line-to-ground voltage surge of 2 kV between phase b and ground. In this first simulation, no surge protection devices (SPDs) are employed and the EUT is simulated as it is. The simulation results of both tests are shown in **Fig. 2.8**, where the phase voltages $u_{a,b,c}$ are measured at the input of the converter (EUT) between each phase and ground. As shown in **Fig. 2.8(i)**, the maximum u_{pn} in the line-to-line surge test reaches 1000 V. As the rectifier stage of the Bb-VSR is based on 1200 V SiC MOSFETs, this stage can survive the overvoltage due to the voltage surge without being damaged.

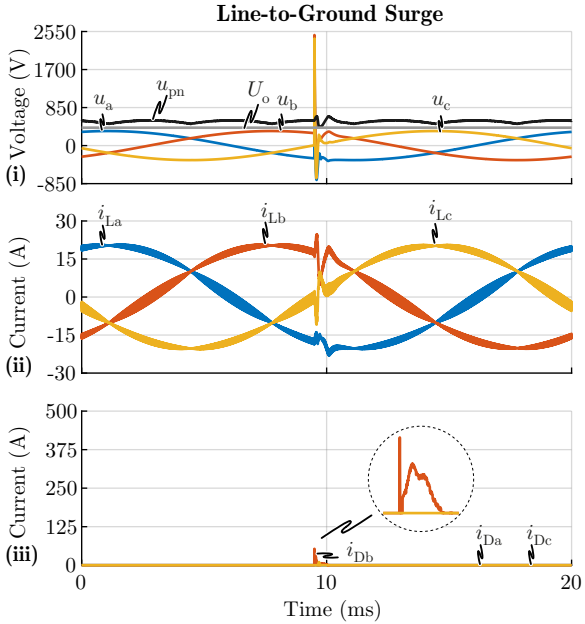


Fig. 2.9: Simulation waveforms for line-to-ground surge test at 2 kV, applied to phase b: **(i)** grid phase voltages $u_{a,b,c}$ (measured at the input of the converter, from line to ground), intermediate DC-link voltage u_{pn}, and output voltage U_o (controlled to 400 V), **(ii)** currents $i_{La,Lb,Lc}$ in the boost inductors of the PFC rectifier stage, **(iii)** currents in the upper bypass diodes of $D_{a,b,c}$ (cf. **Fig. 2.2**). No Surge Protection Devices (SPDs) are considered.

For a line-to-ground fault, u_{pn} reaches only 600 V, as the surge current provided by the CWG is much smaller compared to the line-to-line test setup. Though, the three phase voltages $u_{a,b,c}$ with respect to the ground are relatively high, owing to the small capacitance between line and ground (e.g. C_{cm2} and parasitic capacitance). In **Fig. 2.8** and **Fig. 2.9**, it can be seen during both tests, that most of the surge currents flow through the bypass diodes and not through the switches, whereby the diodes effectively protect the switches from being destroyed. Even though the maximum surge current reaches 450 A, it is still within the ratings of the chosen diodes, which is why it can be concluded that even though the intermediate DC-link capacitor C_{pn} is comparably small, the Bb-VSR can still survive overvoltages as specified in the standards for low surge levels. However, it can also be inferred that, if

Tab. 2.5: Overvoltage Test Levels.

Charger Type	Location	Test Level L-L	Test Level L-G
On-Board	/	1 kV	2 kV
Off-Board	Residential		
	Other Than Residential	2 kV	4 kV

the higher test level would be applied, as required for non-residential off-board chargers, u_{pn} would easily go beyond 1200 V. Consequently, under this circumstance, surge protection devices are inevitable, which will be discussed in the following sections.

Recommended Applications of the SPDs **Star Connection** of SPDs in three-phase power supplies is highly recommended in [83], as shown in **Fig. 2.2.** Whether it is necessary to connect an extra SPD between the neutral and ground point depends on the configuration of the supplying low voltage (LV) network. It is recommended to install this SPD, if the distance between the converter and the PE-N bonding point on the grid side is above 10 m [83]. As the extra SPD connecting the neutral and the ground mainly affects the line-to-ground voltage instead of the line-to-line voltage, it has no effect on u_{pn} in case of a fault, and therefore has no impact whether the converter will be damaged or not. Therefore, for simplicity reasons, the TN-C network, where a combined PE and N conductors is applied [84, 85], is used here as an example.

Voltage Ratings of SPDs are selected based on the breakdown voltage of the equipment and the maximum continuous operating voltage (U_{c}) of the grid. It is recommended to have a protection level 20% lower than the breakdown voltage of the employed power semiconductors. Hence, for the considered Bb-VSR with 1200 V devices, the clamping voltage should be lower than 960 V. Another important parameter is the maximum continuous operating voltage of the SPDs, denoted as $U_{\mathrm{c,SPD}}$. To prevent the SPDs from being triggered under normal operating conditions, $U_{\mathrm{c,SPD}}$ has to be higher than the maximum continuous operating voltage U_{c} of the grid. It is specified that the temporary overvoltages U_{TOV} in the grid, which last longer than 5 s, should be considered as the continuous operating voltage [83], which is around 30% to 50% higher than the nominal voltage for the considered LV grid. Therefore,

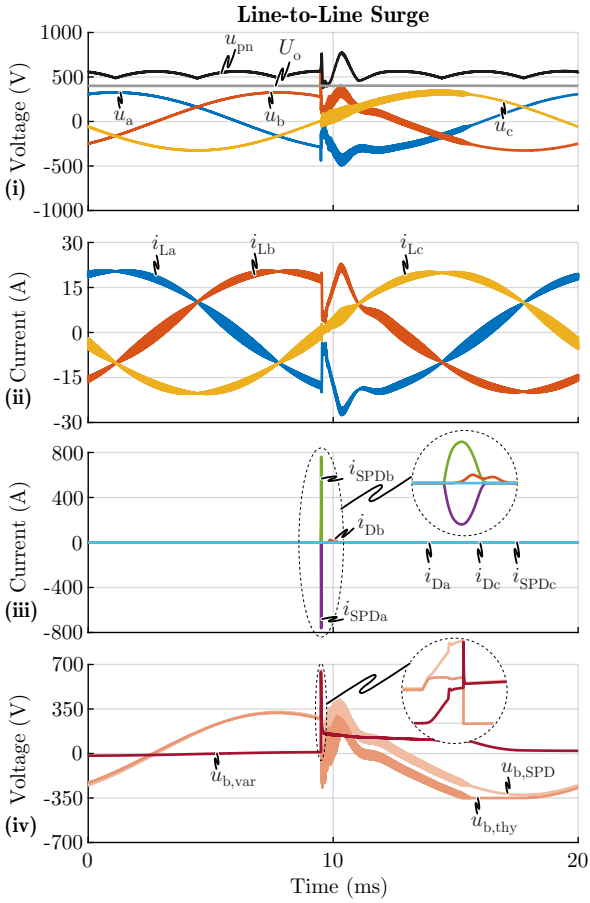


Fig. 2.10: Simulation waveforms for line-to-line surge test at 2 kV, applied between phase a and b: **(i)** grid phase voltages $u_{a,b,c}$ (measured at the input of the converter, from line to ground), intermediate DC-link voltage u_{pn}, and output voltage U_o (controlled to 400 V), **(ii)** currents $i_{La,Lb,Lc}$ in the boost inductors of the PFC rectifier stage, **(iii)** currents in the upper bypass diodes of $D_{a,b,c}$, and **(iv)** varistor voltage $u_{b,var}$, thyristor voltage $u_{b,thy}$, and the total SPD voltage $u_{b,SPD}$ of phase b (cf. **Fig. 2.2**).

it is recommended to select $U_{c,SPD}$ to be 50% higher than the nominal system voltage (RMS). For the considered LV network with a RMS line-to-neutral voltage of 230 V, $U_{c,SPD}$ should be selected to be around 345 V.

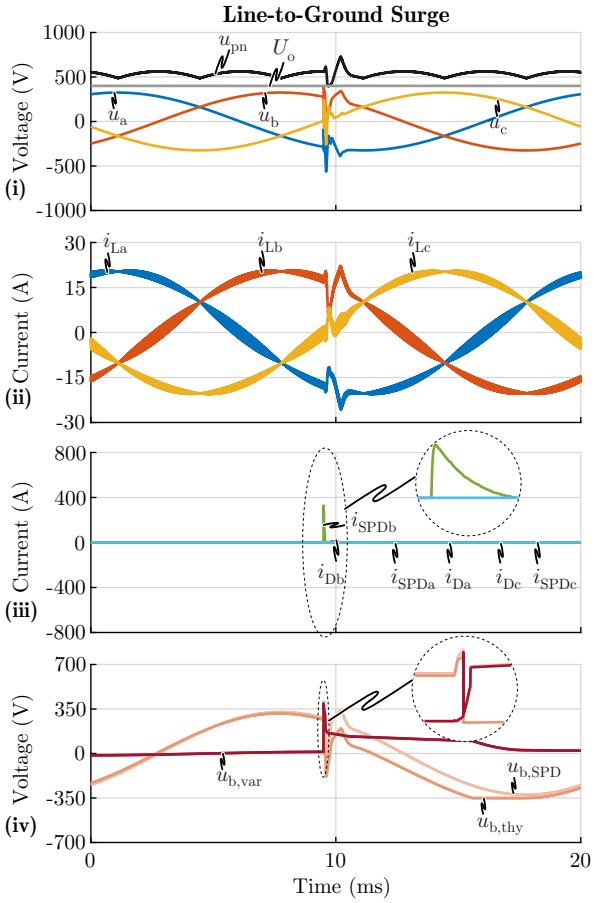


Fig. 2.11: Simulation waveforms for line-to-ground surge test at 4 kV, applied to phase b: **(i)** grid phase voltages $u_{a,b,c}$ (measured at the input of the converter, from line to ground), intermediate DC-link voltage u_{pn}, and output voltage U_o (controlled to 400 V), **(ii)** currents $i_{La,Lb,Lc}$ in the boost inductors of the PFC rectifier stage, **(iii)** currents in the upper bypass diodes of $D_{a,b,c}$, and **(iv)** varistor voltage $u_{b,var}$, thyristor voltage $u_{b,thy}$, and the total SPD voltage $u_{b,SPD}$ of phase b (cf. **Fig. 2.2**).

Selection of the Surge Protection Devices **Varistors** are widely used for overvoltage protection due to their low price and simplicity in terms of application. However, their use comes with the disadvantage of a relatively

high clamping voltage, as e.g., for a varistor with a U_c of 350 V, the final clamping voltage is usually around 900 V. Considering the star connection of the three phase voltages, the maximum line-to-line voltage, which would be applied on u_{pn}, could go beyond 1200 V and, therefore, destroy the switches. Thus, it is not safe to use varistors with high U_c. One option would be to choose varistors with lower U_c, if the connected LV network is not subject to high U_{TOV}. However, alternative solutions need to be considered in a harsher environment.

Transient-Voltage-Suppression (TVS) Diodes would be such an alternative choice, as they react much faster on overvoltages than varistors and are behaving like Zener diodes, clamping to their breakdown voltage in case of overvoltages. However, high-voltage and high-current TVS diodes are usually very expensive.

Two-Stage Protection is a second possibility which is also considered in literature [83]. The first stage is usually a varistor with a high U_c, followed by a second stage consisting of a TVS diode with a lower current handling capability and a lower clamping voltage as well. As an inductor is used to connect the first and the second stage of this SPD design, it is clear that this solution is usually quite bulky compared to the previous approaches.

Varistors Combined with Surge Protection Thyristors are considered in [86], and achieve a low clamping voltage and a high U_c, with reasonable cost and are therefore considered as the most promising solution for the application at hand. The surge protection thyristor is a switching type SPD, i.e., its impedance is very high when no surge is present, but can drop to a low value relatively fast in case of a voltage surge. The internal structure can be found in [87]. As a switching type SPD, it can be modeled using a normal thyristor with a Zener diode controlling its gate [88]. Thus, when there is a voltage surge, the Zener diode exceeds its breakdown voltage and/or allows a current flow and a gate current results, providing a firing pulse for the thyristor. When the voltage surge is gone and the current in the thyristor decreases below the threshold, it will turn off automatically. Based on the voltage ratings discussed in the last section, an appropriate varistor ($V20E130P$, U_c at 130 V [89]) and surge protection thyristor ($P3500SDLRP$, U_c at 320 V [90]) can be selected, both from $Littelfuse$. LT SPICE models of the chosen devices can be found in [91] and were used to extract the parameters of the SPDs, such that they can be modeled properly in a system-level simulation. According to the datasheet values, the parasitic capacitance of the varistor (1900 pF) is much higher than the one of the thyristor (65 pF), whereby during regular operation and the rising edge of the voltage surge, most of the voltage

is directly applied to the surge protection thyristor, which is crucial for the combined varistor/thyristor circuit to function as intended. Moreover, the leakage current at the nominal voltage (10 µA for the varistor and 5 µA for the thyristor) implies a slightly larger off-state resistance of the surge protection thyristor, whereby in steady-state, most of the voltage is applied across the thyristor, preventing the low-voltage varistor from being triggered in normal operation. In case of a voltage surge, the thyristor is therefore triggered first, whereby all the surge voltage is then applied across the varistor, which finally clamps at a rather low voltage level. However, as the parasitic values of the devices may vary in reality, extra resistors and capacitors should be used in parallel to the SPDs, in order to ensure the aforementioned coordination between the varistor and the surge protection thyristor.

Simulation Results with SPDs The simulation results for a line-to-line surge voltage of 2 kV and a line-to-ground surge voltage of 4 kV are shown in **Fig. 2.10** and **Fig. 2.11**, respectively. With the SPDs diverting the surge energy, the peak value of u_{pn} is much smaller compared to **Fig. 2.8**, reaching 800 V in the line-to-line surge test and 730 V in the line-to-ground test (cf. **Fig. 2.9**), even though the test level is higher. The clamping process is shown in detail in **Fig. 2.10(iv)** and **Fig. 2.11(iv)** based on the voltages across the varistor $u_{\mathrm{b,var}}$, the thyristor $u_{\mathrm{b,thy}}$, and the total SPD $u_{\mathrm{b,SPD}}$ for phase b, where the positive terminal of the CWG is connected to. It can be noted that, most of the surge voltage is applied to the thyristor first, and when it breaks down at around 350 V, the total voltage drops as well since there is not enough current charging the parasitic capacitance of the varistor. Then as the current increases, the voltage $u_{\mathrm{b,var}}$ across the varistor increases as well and finally is clamped at 370 V. When the surge voltage is gone, $u_{\mathrm{b,var}}$ will not drop to zero immediately due to the lack of negative current discharging its parasitic capacitance. Owing to $u_{\mathrm{b,var}}$, the thyristor will reach its breakdown voltage in another direction afterwards. At this point, the negative current will increase slightly and the varistor parasitic capacitance will be discharged to nearly zero. It needs to be noted that the thyristor will not break down as the discharging current is not large enough for the firing pulse, which is in the range of a few hundred milliamperes [90].

The maximum current through the SPDs is lower than 800 A and lasts less than 20 µs, which is within the ratings of the selected SPDs. The maximum current through the bypass diodes is 160 A, which is also within its surge current rating. For the line-to-line surge voltage, the current flows into one phase, then coming back through another phase, so there are two branches

of SPDs in the surge current path, leading to higher total clamping voltage than in the line-to-ground test, where only one SPD branch is activated.

Therefore, it can be concluded that the SPD network works for both types of voltage surges. With the previous discussions, the Bb-VSR is proven to be capable of withstanding the required grid irregularities, including harmonics, voltage dips and interruptions, and overvoltages, and hence can be utilized in real-world applications.

2.2.5 Reactive Power Control

Though not required for the mainstream chargers, the bidirectional power flow or reactive power control capability has been getting increasing attention in recent years, e.g., in V2G applications [92] where the batteries of EVs are used to stabilize the grid. Therefore, it is of interest to investigate whether 1/3-PWM can be used for such applications. **Fig. 2.12** shows the control diagram of the Bb-VSR required for introducing a phase shift between the grid voltages and currents. Hence, the extra block, highlighted in blue, generates the new voltage references. The vector diagram shows the principle of calculation, where u_{a}^{*} is calculated with the phase voltage u_{a} and the line-to-line voltage u_{bc} which is 90° phase shifted, i.e., vertical to u_{a}. In this control structure, no PLL is required and thus minimum implementation effort can be maintained. **Fig. 2.13** shows the simulated waveforms with 45° phase shift between the voltages and currents, which can be extended to ±180°.

2.3 Three-Level Converter Topology

In this section, the Vienna Rectifier (VR) is analyzed as another option for realizing the PFC rectifier front-end of the two-stage system. The VR is a boost-type PFC rectifier topology that is widely used in industry [93]. For the sake of clarity and to estimate the potential improvement achievable by synergetic control in a three-level VR, the DC/DC stage is not discussed here concerning implementation details, but is treated as two generic blocks as shown in **Fig. 2.14**, with the assumption that it can handle the necessary dynamics.

2.3.1 Conventional Control

As discussed in the introduction, there are two interesting options for how to operate a boost-type AC/DC PFC rectifier, specifically a VR, in a two-stage

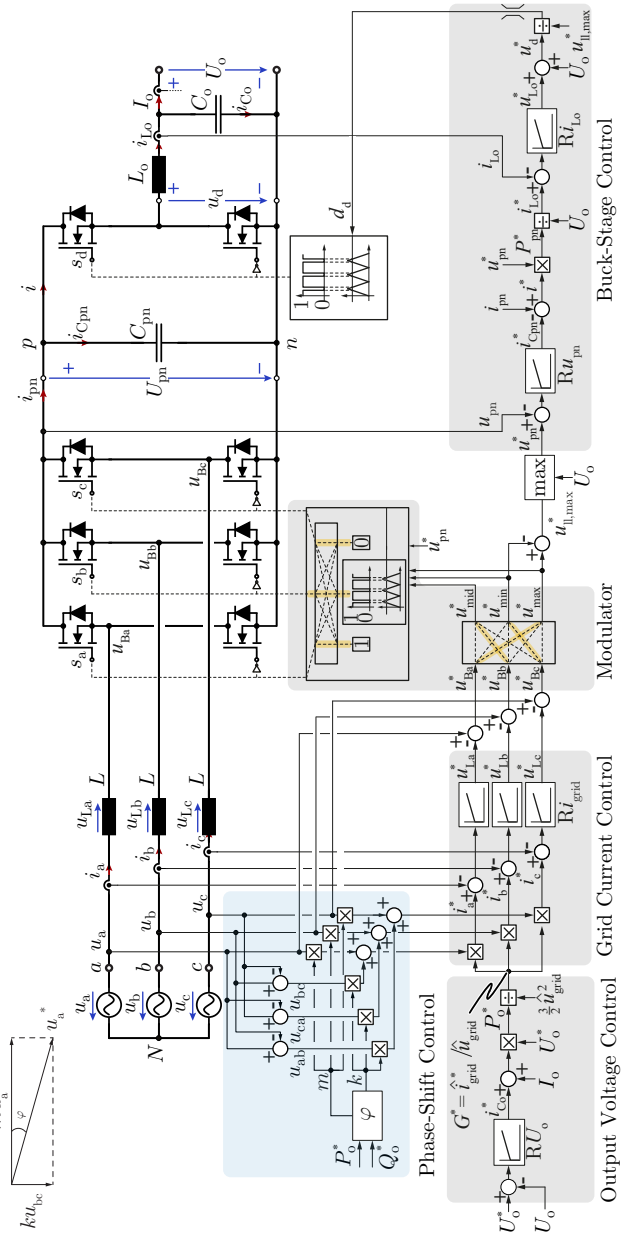


Fig. 2.12: Cascaded output voltage control structure for the Bb-VSR, where an extra block is added, highlighted in blue, to generate the required voltage references with the phase shift, finally determining the phase-shifted phase current references.

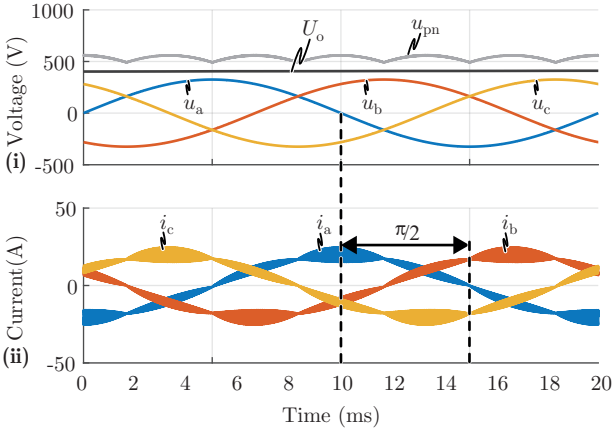


Fig. 2.13: Simulation waveforms for 90° phase shift between the voltages and currents.

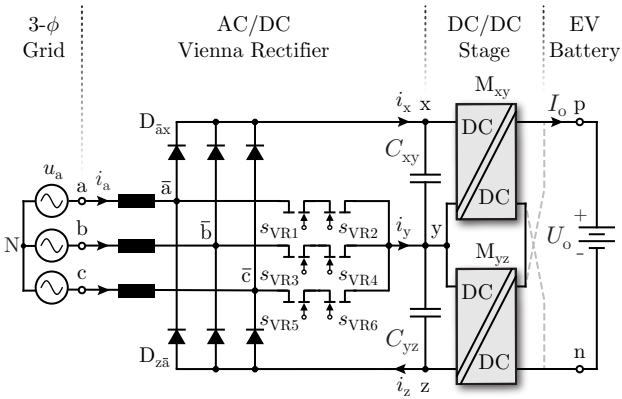


Fig. 2.14: Conceptual power circuit of the considered EV charger with generic DC-DC stages, where the AC/DC PFC rectifier is realized as a Vienna Rectifier (VR). The dashed lines symbolize the possibility of reconfiguring the output connection of the isolated DC/DC converter modules from series to parallel arrangement.

system. First, if standard 3/3-PWM is used, the intermediate DC-link voltage U_{xz} is kept at a constant value (for a given output voltage and power; different constant values may be favorable for different operating points). Furthermore, unlike the two-level converters discussed in the last section, for the sake of

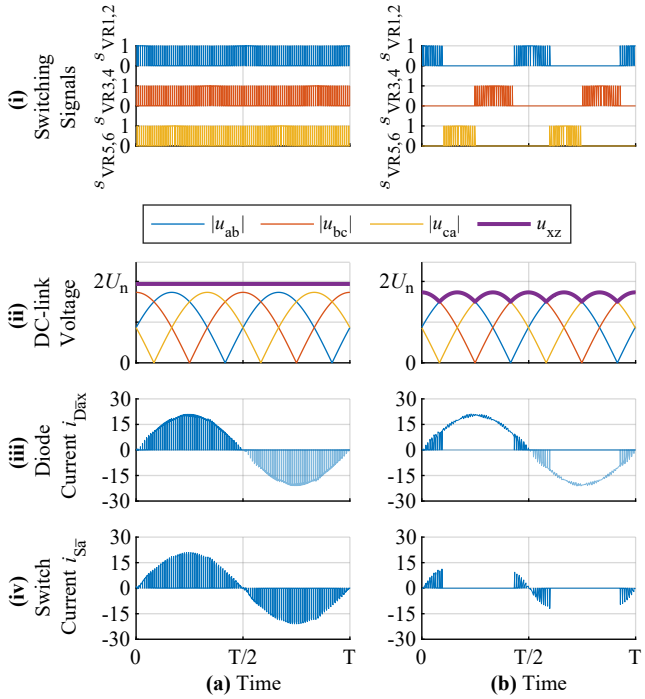


Fig. 2.15: Simulated waveforms of the VR operating with **(a)** 3/3-PWM and **(b)** 1/3-PWM (note the six-pulse shape of the intermediate DC-link voltage u_{xz}, which is controlled by the DC/DC converters to impress currents in two of the three mains phases). **(i)** Switch gate signals, **(ii)** DC-link voltage u_{xz}, **(iii)** diode current of phase a, **(iv)** switch current of phase a.

clarity, Discontinuous PWM (DPWM) methods [94] are not considered here, as these result in a relatively large midpoint current, i_y [95]. As a result, either bulky electrolytic capacitors have to be used, or the two DC/DC converters would need to compensate a relatively large power mismatch. Therefore, only 3/3-PWM is used, as indicated in **Fig. 2.15(a)**.

2.3.2 Synergetic Control

Finally, 1/3-PWM can also be implemented in the VR, whose split intermediate DC-link is connected to two stacked isolated DC/DC converters, as

initially mentioned in [53], using a three-level NPC front-end and three-phase PWM-operated DC/DC converters. However, as mentioned previously, the downstream DC/DC converters can contribute to the rectifier's task of shaping the grid currents by controlling the intermediate DC-link voltage u_{xz} along a six-pulse reference defined by $u_{xz} = \max(|u_a b|, |u_b c|, |u_c a|)$ (1/3-PWM) as indicated in **Fig. 2.15(b)**[1], which then implies that, advantageously, at all times only one of the rectifier's bridge-legs is operating with PWM. Note that to do so (i.e., to achieve sufficiently high control dynamics), the intermediate DC-link capacitors, C_{xy} and C_{yz} must be relatively small.

2.3.3 Comparative Evaluation

A detailed comparative analysis of the VR semiconductor stresses and losses occurring with 3/3-PWM and 1/3-PWM is given in [32]. For the sake of brevity, we summarize the key results in **Tab. 2.6**, where $f_{sw,VR}$ is the switching frequency, I_{avg} and $\hat{I}$ are the average and peak value of the sinusoidal input currents, respectively ($I_{avg} = 2/\pi \cdot \hat{I}$), M is the modulation index, and $\hat{U}$ is the peak value of the grid (input) phase voltages. Note that for 3/3-PWM, space-vector PWM (SVPWM), i.e., a common-mode (CM) third-harmonic voltage injection of $u_{CM} = (u_{max} + u_{min})/2$ is assumed, whereby u_{max} and u_{min} are the maximum and minimum instantaneous phase voltages, respectively. The same CM voltage also appears for 1/3-PWM as a consequence of always two phases being clamped. The switching losses are considered with a linear model, $P_{sw} = P_{sw,0} + P_{sw,1}$, where $P_{sw,0}$ represents the current-independent capacitive switching loss contributions and $P_{sw,1}$ the dependency on the switched current. Compared to 3/3-PWM, 1/3-PWM reduces the switching losses by more than 66%, as at all times only the bride-leg corresponding to the phase with the lowest (absolute value) current operates with PWM. For the same reason, also the conduction losses of the transistors decrease significantly while the diode currents only increase slightly.

2.4 Summary

In this chapter, the synergetic control structures, for both the two-level PFC rectifier front-end, i.e., the six-switch boost converter, and the three-level PFC rectifier front-end, i.e., Vienna Rectifier (VR), are analyzed, which feature a

[1] Note that this is essentially an approximation that neglects the (mains-frequency) voltage drop across the boost inductors, which, however, is very low especially if high VR switching frequencies and hence small boost inductors with a low inductance value are used.

Tab. 2.6: Comparison of the VR Semiconductor Stresses Resulting with 3/3-PWM and 1/3-PWM, for Unity Power Factor Operation.

Parameter		Equation		Difference	Condition
		3/3-PWM	1/3-PWM		
Switching Losses P_{sw}	$P_{sw,0}$	$k_{sw,0} \cdot f_{sw,VR}$	$\frac{k_{sw,0}}{3} \cdot f_{sw,VR}$	-66%	/
	$P_{sw,1}$	$k_{sw,1} \cdot I_{avg} \cdot f_{sw,VR}$	$\left(1-\frac{\sqrt{3}}{2}\right) k_{sw,1} \cdot I_{avg} \cdot f_{sw,VR}$	-86%	/
Switch RMS Current $I_{S,RMS}$		$\frac{\hat{I}}{\sqrt{\pi}}\sqrt{\frac{\pi}{2}+\frac{5\sqrt{3}-16M-8}{12}}$	$\frac{\hat{I}}{\sqrt{\pi}}\sqrt{\frac{\pi}{6}+2\sqrt{3}\ln\left(\frac{\sqrt{3}}{2}\right)}$	-69.4%	$U_{xz} = 640\,\mathrm{V}$, $\hat{U} = 325\,\mathrm{V}$ $M = \frac{\hat{U}}{(U_{xz}/2)} = 1.015$
Diode RMS Current $I_{D,RMS}$		$\frac{\hat{I}}{\sqrt{\pi}}\sqrt{\left(\frac{1}{3}-\frac{3\sqrt{3}}{16}\right)(2M+1)+\frac{18M-1}{16\sqrt{3}}}$	$\frac{\hat{I}}{\sqrt{\pi}}\sqrt{\frac{\pi}{6}+\frac{\sqrt{3}}{8}\ln\left(\frac{256}{81}\right)}$	$+9\%$	
Diode Average Current $I_{D,avg}$		$\hat{I}\frac{M}{4}$	$\hat{I}\frac{\sqrt{3}\ln(3)}{2\pi}$	$+19.1\%$	

wide DC output voltage range. The investigation of the occurring component stresses in the PFC rectifier stage using 1/3-PWM shows that this control strategy results in significant loss savings compared to conventional 2/3-PWM and 3/3-PWM. Furthermore, the exemplary analysis in the two-level Bb-VSR reveals that the proposed control structure guarantees the continuation of converter operation for a wide variety of grid disturbances and irregularities, which need to be considered in EV charger applications. A review and summary of the low-voltage (LV) grid standards is provided, and the test methods for irregular grid conditions are described. The critical grid conditions are identified, and it is shown that a safe operation is ensured for all critical grid conditions, by means of either appropriate control of the converter, or additional protection circuitry. Moreover, current spikes following grid voltage steps or grid voltage surges are analyzed in detail, including the behavior of the EMI filter components under such conditions. Based on this analysis, a comprehensive guideline for the selection of overvoltage protection circuits and elements is derived.

3 Advanced Output Stage DC/DC Converter Topologies

Chapter Abstract

In this chapter, different solutions for the isolated DC/DC converter stage in EV chargers are analyzed. In the first step, the most popular solution in industry - the LLC converter, is investigated and the topology-related challenges are identified and explained. Subsequently, the second prominent DC/DC converter topology - the Dual Active Bridge (DAB) converter, is introduced and analyzed in detail. To overcome the drawbacks of the two aforementioned topologies, a new type of resonant converter is investigated, referred to as Quantum Series Resonant Converter (QSRC), which features buck and boost functionality. Subsequently, the operating principle, control scheme, soft-switching strategy, and main design guidelines are illustrated. To fairly assess the performance of the QSRC, the three topologies are compared first in terms of theoretical analyses, i.e., Pareto optimization results. In the next step, the QSRC and the DAB converter are compared experimentally using suitable hardware demonstrators. Finally, in order to further increase the performance of the QSRC, the Hybrid Quantum Series Resonant Converter (H-QSRC) is introduced and analyzed.

3.1 Introduction

In order to facilitate a fair comparison of different isolated DC/DC converter topologies, the output power and the output voltage levels specified in **Fig. 3.1(c)** are considered. As discussed in **Sec. 1.3**, nine nominal operating points (cf. in **Fig. 3.1(c)**) are selected for the evaluation of the overall efficiency and are weighted as follows [29, 30]:

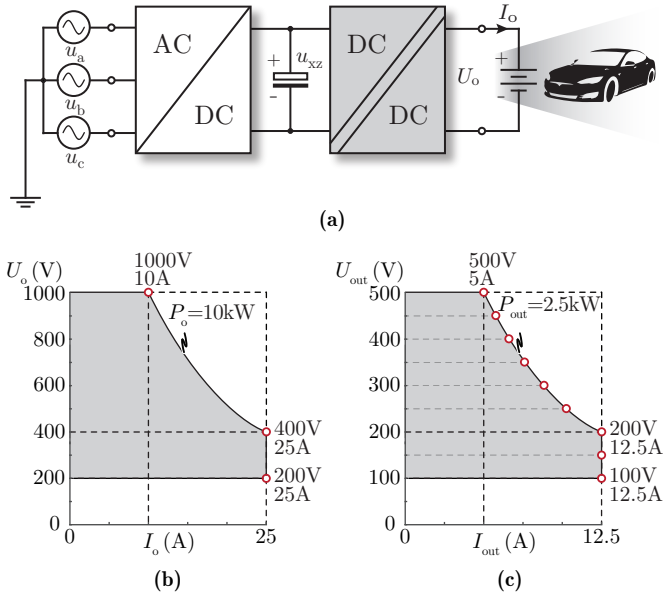


Fig. 3.1: (a) Block diagram of a typical two-stage EV charger with a three-phase AC/DC PFC rectifier front-end and a downstream isolated DC/DC converter, and **(b)** the corresponding output voltage U_o, and output current I_o range of the 10 kW system. **(c)** Output voltage U_{out} and output current I_{out} of the considered DC/DC converter; the operating parameters are determined considering a realization of the 10 kW system in form of a series/parallel connection of 4 individual converters, each with a maximum output power of 2.5 kW. The 9 nominal operating points are marked in red.

$$\bar{\eta} = \frac{1}{N} \sum_{i=1}^{N} \eta_i. \tag{3.1}$$

The required output voltage of the DC/DC converter is given by the charge-level dependent momentary battery voltage, whereas the input voltage is considered as a degree of freedom that can be used to maximize the efficiency. Wherever possible, it is selected such that the converter can be operated with unity gain, where most typologies have the highest efficiency. However, considering the operation of the PFC rectifier front-end, the scaled input voltage range is limited to 280 V...400 V, as shown in **Tab. 3.1**, which is why

Tab. 3.1: Single DC/DC Module Specifications.

Parameter	Value
Input Voltage U_{in}	280 V... 400 V
Output Voltage U_{out}	100 V... 500 V
Maximum Output Power $P_{\text{out,max}}$	2.5 kW
Maximum Output Current $I_{\text{out,max}}$	12.5 A

the unity-gain operation of the DC/DC converter cannot be used for all output voltages. In such cases, the input voltage is then selected to minimize the step-up or step-down ratio.

In this chapter, the design and optimization of the LLC converter are presented in **Sec. 3.2**, where the topology-specific challenges are identified. In the next step, **Sec. 3.3** introduces the DAB converter, including the design of the modulation, optimization, and the experimental results of a 2.5 kW module. To overcome the disadvantages of the LLC and DAB converter, the Quantum Series Resonant Converter (QSRC) is investigated in **Sec. 3.4**, followed by the control schemes and design principles. To experimentally demonstrate the performance of the QSRC, a 2.5 kW module is built, with the same volume of magnetics and switches as the DAB converter. Subsequently, a comprehensive comparison is given in **Sec. 3.5**, providing insight into the three topologies. Finally, to improve the performance of the QSRC, the Hybrid Quantum Series Resonant Converter (H-QSRC) is discussed in **Sec. 3.6**.

3.2 LLC Converter

3.2.1 Operating Principle of the LLC Converter

The LLC converter is one of the most popular topologies for applications where galvanic isolation is required, due to its relatively high efficiency and simple operating principle. The topology is shown in **Fig. 3.2**, where the resonant inductor L_{r} can either be implemented as a discrete component or integrated into the transformer as the leakage inductance. For the sake of simplicity, in this chapter, only frequency modulation is considered [96], i.e. the conventional LLC converter control strategy. Hence, the frequency-dependent total impedance of the LLC converter resonant tank is used to control the voltage transfer ratio of the converter. For switching frequencies above the resonant frequency of the series-connected L_{r} and C_{r}, the total

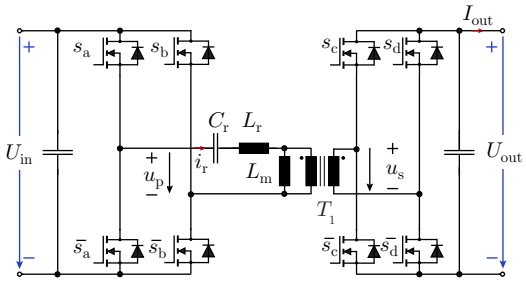


Fig. 3.2: Topology of the isolated DC/DC LLC converter, where the resonant inductor L_r can either be implemented as a discrete component or integrated into the transformer as the leakage inductance.

impedance increases with increasing frequency, which is why a step-down converter functionality is achieved in this frequency range. Below this resonance frequency, the series connection of C_r and L_m dominates, and since the output is in parallel with L_m, whose voltage can be higher than the input voltage, a step-up converter functionality is achieved.

There are different analysis methods for the LLC converter to calculate the frequency- and load-dependent gain characteristics and dynamics. The most common and simple method is the frequency domain analysis / fundamental harmonic approximation (FHA), which works very well when the switching frequency is close to the resonant frequency of the L_r-C_r resonant tank. However, in the application at hand, where a wide output voltage range needs to be covered, an extremely wide switching frequency range will inevitably result. **Fig. 3.3** shows the calculated gain characteristics using both, frequency domain and time domain analysis methods [97] for one design ($f_r = 350\,\text{kHz}$, $L_r = 13\,\mu\text{H}$, $L_m = 78\,\mu\text{H}$, $m = 7$; for the definition of m see **Tab. 3.2**). It can be seen that there are significant differences between the two methods when deviating from unity gain operation, whereby the time domain analysis gives much more accurate results [98]. Therefore, even though more complicated in terms of calculation, it is vital to perform the time domain analysis to calculate accurately the required switching frequency and the voltage and current waveforms when setting up an LLC converter optimization.

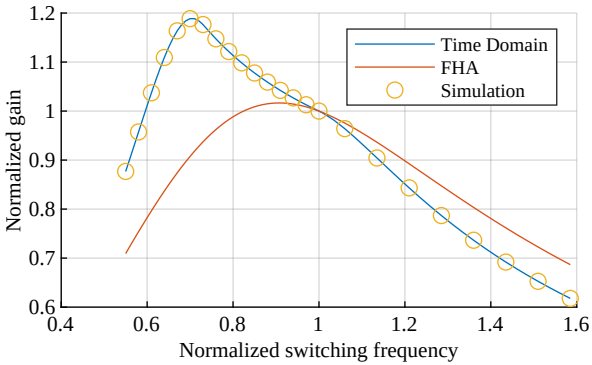


Fig. 3.3: Comparison of the calculation of the LLC converter gain characteristics using the time domain analysis and the fundamental harmonic approximation (FHA), for a resonant frequency of $f_r = 350\,\text{kHz}$, a series resonant inductance of $L_r = 13\,\mu\text{H}$, a magnetizing inductance of $L_m = 78\,\mu\text{H}$, and an inductance ratio of $m = 7$.

3.2.2 Design and Optimization of the LLC Converter

In order to accurately predict the component stresses and the operating parameters of the different components in the LLC converter, a waveform generator based on time-domain analysis was implemented in MATLAB. Based on these calculated component stresses and suitable loss models for the magnetic components and the switches (for the considered transistors, accurate calorimetric switching loss data for both, soft-switched and hard-switched operation has been published earlier [99]), an optimization can be carried out, where possible converter designs for a specific set of design space variables are evaluated. The design space variables and their respective limits are listed in **Tab. 3.2.** Hence, the optimization aims to find the optimal combination of transformer turns ratio n, resonant frequency f_r, inductance ratio m as well as resonant inductance L_r. For power density reasons, the resonant inductor L_r is implemented as the leakage inductance of the transformer.

The Pareto optimization results are shown in **Fig. 3.4**, where the different designs are represented as dots colored according to the turns ratios of the transformer. As mentioned previously, the same switches will be used for all three topologies, which means in terms of volume, it is the magnetic components that will make a difference. Hence for the sake of clarity, the x-axis in the Pareto optimization results is the box volume of the magnetic components, rather than the converter, even though the efficiency is for the

Tab. 3.2: Design Space Variables for the LLC Converter Optimization.

Parameter	Range
Transformer Turns Ratio n	1.0…2.0
Resonant Frequency f_r	100 kHz…600 kHz
Inductance Ratio $m = \frac{L_r+L_m}{L_r}$	4…16
Resonant Inductance L_r	3 µH…18 µH

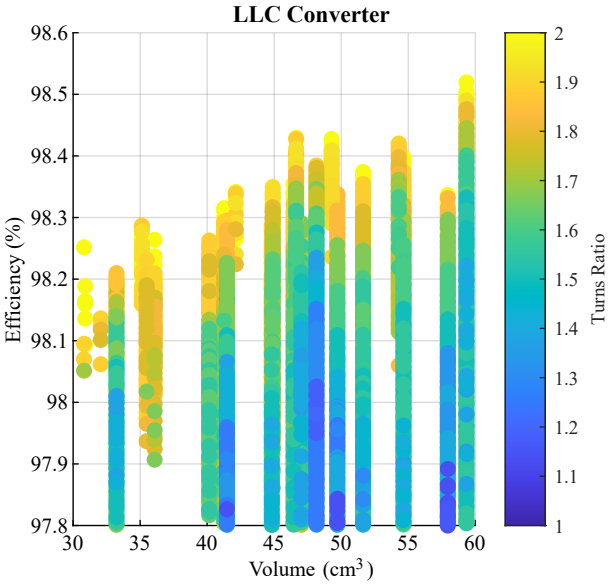


Fig. 3.4: Pareto optimization results of a 2.5 kW LLC converter module, where the volume on the x-axis corresponds to the total magnetics volume and the color-coding of the different converter designs indicates the turns ratio of the respective transformers.

whole system. The same will be applied to the Pareto fronts in the following sections for the other topologies. For the considered volumes, it can be seen that efficiencies of up to 98.5 % can be achieved with the LLC converter resonant converter topology. Furthermore, the efficiency increases with the turns ratio of the transformer up to a certain point (1.6…2), which means that the LLC converter is in general less efficient in buck-mode than in boost-mode. This is due to the lower output voltage and thus higher output current and

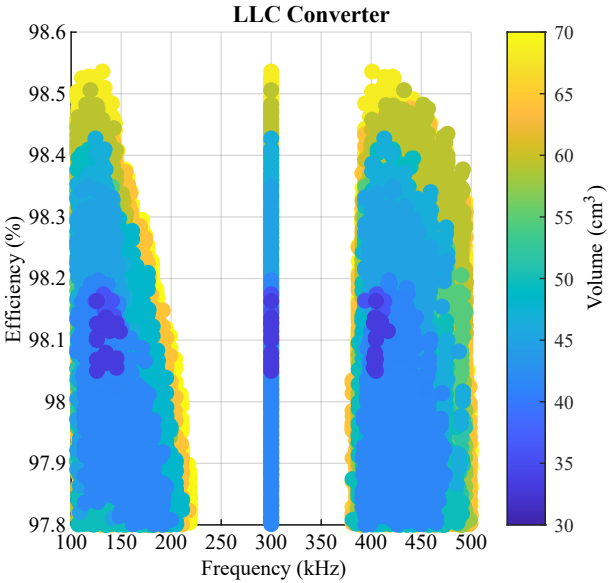


Fig. 3.5: The maximum and minimum switching frequency required to cover the entire voltage operating range for full-load operation for the designs from the Pareto optimization (cf. **Fig. 3.4**) with a resonant frequency of 300 kHz. The color-coding of the dots indicates the total magnetics volume of the considered LLC converter designs.

also higher switching frequency in buck-mode. Consequently, the worst-case operating point occurs at 100 V, 12.5 A in buck-mode at full-load operation. Since a higher turns ratio of the transformer reduces the step-down ratio and therefore the switching frequency at this operating point without sacrificing too much the other operating points, a generally higher average efficiency of the converter can be achieved.

Despite the relatively high efficiency, the disadvantage of the LLC converter is the extremely wide frequency range. To demonstrate the required frequency range for the considered application, the maximum and the minimum switching frequency of the converter designs in **Fig. 3.4** with an exemplary resonant frequency of 300 kHz have been selected and are shown in **Fig. 3.5**. Each design is represented by three dots (the minimum frequency on the left side, the maximum frequency on the right side, and the resonant frequency in the middle of the figure), whereby the colors indicate the magnetic component

volume of the converter. It is clear from **Fig. 3.5** that a frequency range of at least 200 kHz to 400 kHz is required just for output voltage regulation at full power. In part-load operation, the maximum required switching frequency would be much higher due to the required large impedance of the resonant tank, if the frequency modulation is used. To limit the switching frequency range, alternative modulation methods can be employed, which makes the overall analysis more complicated. Furthermore, such wide switching frequency ranges make it difficult to design suitable EMI filters. Moreover, it is also not easy to find suitable litz wires that can conduct high currents efficiently, i.e., with low AC losses at such high frequencies (e.g., 40 µm strand diameter or even smaller with a large number of strands, > 1000 [100, 101], which usually requires long delivery lead time and are very expensive).

Even though these problems can be mitigated to a certain extent by more complicated control methods [102], most of them remain to a large extent, which is why this topology is not considered suitable for the application at hand, and more promising topologies are investigated in the following.

3.3 Dual Active Bridge Converter

3.3.1 Operating Principle of the DAB Converter

The Dual Active Bridge (DAB) converter consists of two full-bridges as shown in **Fig. 3.6**, where both can actively generate voltage pulses (u_p and u_s) with adjustable duty cycles. These two voltages are then applied across the inductor L_σ, which can either be the leakage inductance of the transformer or an external inductor. The transferred power can be adjusted by controlling the phase shift between these rectangular voltages, i.e., u_p and u_s. Furthermore, the DAB converter is capable of stepping up and down the output voltage, as well as providing bidirectional power flow. The high degrees of freedom in terms of control (primary-side and secondary-side duty cycles D_1 and D_2, phase shift ϕ and switching frequency f_sw), can be leveraged to achieve certain optimality criteria, resulting in different modulation schemes [25, 103, 104], which differ primarily in their complexity and the achievable efficiency of the energy transmission. The simplest modulation is referred to as phase shift modulation (PSM), where the duty cycles of both full-bridges are kept at 0.5, and the phase shift is then used to control the output power. In the analyses and calculations of this work, a duty cycle of 0.5 corresponds to the maximum duty cycle, i.e., a square-wave voltage that follows the positive DC-link voltage during the first half of the switching period and the negative

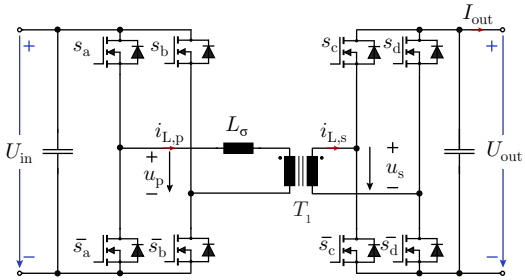


Fig. 3.6: Topology of the DAB converter, where the series inductance L_σ can either be implemented as a discrete component or integrated into the transformer as the leakage inductance.

DC-link voltage during the second half of the switching period. The PSM is the most suitable modulation for high-power operation or at unity gain [103]. For lower power levels at buck or boost-mode, the circulating current can be significantly reduced if the duty cycle of one of the two active full-bridges is reduced. For even lower power levels, it is often optimal to keep the duty cycles of both sides below 50%. However, analytical equations only exist for modulations that minimize the RMS current in the system, where the switching losses are not considered [103, 105]. But, the switching losses cannot be neglected in a real system when finding its optimal state, which is why it is inevitable to sweep through all possible combinations of duty cycles, phase shifts, and switching frequencies with accurate loss models of the magnetic components and switches, and only then the most efficient combination for a certain operating point (input voltage, output voltage, and output power) and for a certain design can be determined. This needs to be done for all possible operating points of a certain application, whereby the optimal control parameter combinations are finally summarized in a 3-D or even 4-D lookup table (LUT). Unfortunately, this is relatively complicated and time-consuming, and the discontinuous transitions in the LUT lead to problems when implementing the control in a real converter system.

3.3.2 Design and Optimization of the DAB Converter

To speed up the design process and to reduce implementation effort for the control, a simplified modulation is used here, which offers a continuous, hence easy-to-implement, and close-to-optimal solution that makes use of 3 degrees

of freedom: the duty cycles D_1 and D_2 as well as the switching frequency f_{sw} (the phase shift ϕ is used as a control parameter in an underlying closed-loop PI controller), where one duty cycle is always set to 0.5, and the other is adapted according to the momentary port voltages. In buck-mode, where the input voltage is higher than the primary-side referred output voltage, the primary-side duty cycle is $D_1 < 0.5$ and the secondary-side duty cycle $D_2 = 0.5$, while in boost-mode, $D_1 = 0.5$, and $D_2 < 0.5$ is selected.

In a DAB converter, there are in total twelve possible basic voltage patterns, which can be distinguished based on the voltage sequences applied, i.e., the sequence of rising and falling edges of the primary-side and secondary-side rectangular voltages. However, only six of the twelve voltage patterns make sense from an efficiency point of view, since the remaining six patterns lead to higher RMS currents for the same power transferred [103]. Out of the six remaining patterns, four patterns result in a positive power transfer, i.e. power flow from the input to the output. Taking into account the above-mentioned selection of the duty cycles (the one with the lower voltage is set to 0.5), two of the four patterns can be assigned to buck-mode and two to boost-mode. **Figs. 3.7(a)(b)** shows the two possible waveforms in boost-mode. Using the voltage pattern of **Fig. 3.7(b)** in boost-mode leads to either extremely high circulating currents, due to the large fraction of reactive power flow in the system for the considered switching frequency (200 kHz...300 kHz), or extremely high switching frequency (400 kHz...500 kHz) for lower reactive power, resulting in substantial high-frequency winding losses. Therefore, this pattern is not utilized. Consequently, in boost-mode, the voltage pattern according to **Fig. 3.7(a)** is used, whereas in buck-mode, **Fig. 3.7(d)** is used, as the waveforms/voltage sequences are symmetrical to **Fig. 3.7(a)**, and only the primary-side and secondary-side voltages are swapped. Therefore, the calculations of the RMS currents and the transmitted power are identical, reducing the implementation effort.

In addition to minimum RMS currents for a certain specific power to be transmitted, there is another goal in terms of modulation, namely the soft switching for all semiconductors in order to minimize the switching losses. This means that the currents in the switches must have the correct sign during the switching transitions and must be large enough to charge/discharge the parasitic output capacitances C_{oss} of the switches. In both buck and boost-mode, there are two switching transitions where it is inherently more difficult to achieve zero-voltage-switching (ZVS) conditions for the switches, i.e., t_1 and t_3 in buck-mode and t_2 and t_3 in boost-mode (cf. **Figs. 3.7(a)(d)**). The crucial switching currents in boost-mode can be calculated according to:

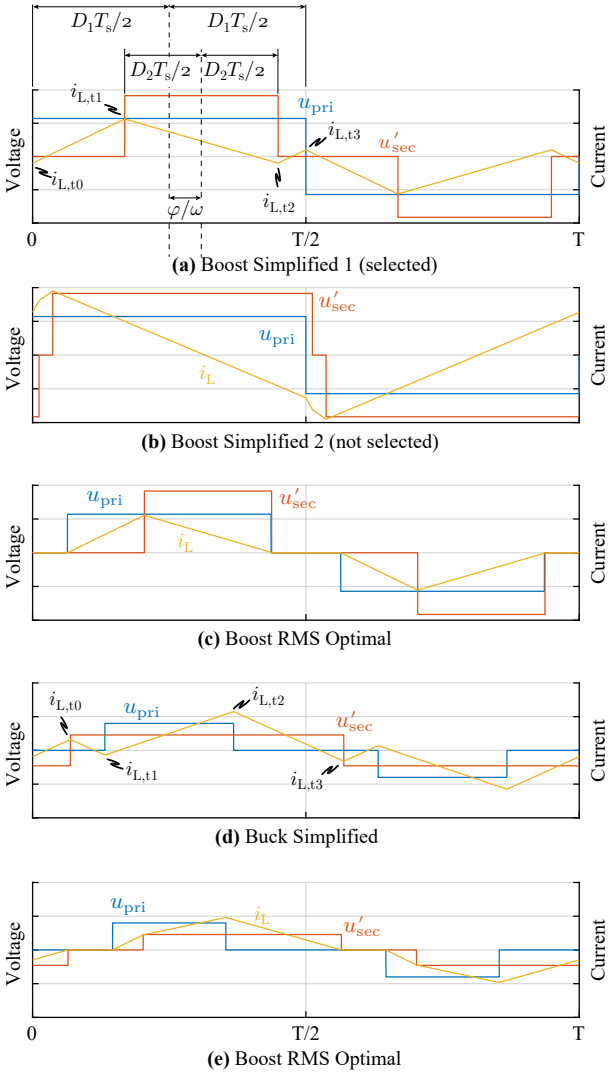


Fig. 3.7: Calculated DAB converter voltage and current waveforms for different possible voltage sequences in boost-mode, i.e., **(a)** and **(b)**, and in buck-mode **(d)**, using the selected simplified modulation. For comparison, also the waveforms of the conduction-loss-optimal modulation are shown in **(c)** and **(e)**, which result in minimal RMS transformer currents for a certain required output power.

$$i_{\mathrm{L,t2,boost}} = \frac{-\frac{1}{f_{\mathrm{sw}}} n U_{\mathrm{out}} \left(U_{\mathrm{out}} n - U_{\mathrm{in}}\right) D_2^2 + P L_{\mathrm{s}}}{2 U_{\mathrm{out}} D_2 n L_{\mathrm{s}}}, \tag{3.2}$$

$$i_{\mathrm{L,t3,boost}} = \frac{1}{2 L_{\mathrm{s}} f_{\mathrm{sw}}} \left(\frac{1}{2} U_{\mathrm{in}} - n D_2 U_{\mathrm{out}}\right), \tag{3.3}$$

where U_{in} and U_{out} denote the input and output voltages of the DAB converter, and no magnetization current is considered.

Note that all current values are referred to the primary side, even though the first of these transitions actually happens in the secondary-side bridge with a correspondingly scaled (by the turns ratio n) current of the opposite sign (if the positive current direction is in all cases defined as out of the bride-leg's switch node).

Assuming a minimum required absolute ZVS current $I_{\mathrm{ZVS}} > 0$ in the switches results in the ZVS conditions $i_{\mathrm{L,t2,boost}} = -I_{\mathrm{ZVS}}$, $i_{\mathrm{L,t3,boost}} = I_{\mathrm{ZVS}}$, whereby the required switching frequency f_{sw} and the duty cycle D_2 on the secondary side can be calculated as:

$$f_{\mathrm{sw}} = \frac{U_{\mathrm{in}}^2 \left(U_{\mathrm{in}} - n U_{\mathrm{out}}\right)}{2 \left(2 I_{\mathrm{ZVS}} U_{\mathrm{in}}^2 - 3 I_{\mathrm{ZVS}} U_{\mathrm{in}} n U_{\mathrm{out}} - P_{\mathrm{o}} n U_{\mathrm{out}} - a\right) L_{\mathrm{s}}}, \tag{3.4}$$

with

$$a = \sqrt{I_{\mathrm{ZVS}}^2 U_{\mathrm{in}}^2 n U_{\mathrm{out}}^2 - 4 I_{\mathrm{ZVS}} P_{\mathrm{o}} U_{\mathrm{in}}^2 n U_{\mathrm{out}} + 6 I_{\mathrm{ZVS}} P_{\mathrm{o}} U_{\mathrm{in}} n^2 U_{\mathrm{out}}^2 + P_{\mathrm{o}}^2 n U_{\mathrm{out}}^2}, \tag{3.5}$$

and

$$D_2 = \frac{-4 f_{\mathrm{sw}} I_{\mathrm{ZVS}} L + U_{\mathrm{in}}}{2 U_{\mathrm{out}} n}. \tag{3.6}$$

In buck-mode, $i_{\mathrm{L,t1,buck}} = -I_{\mathrm{ZVS}}$, and $i_{\mathrm{L,t3,buck}} = -I_{\mathrm{ZVS}}$ have to be fulfilled for ZVS conditions, which due to the symmetry of the DAB converter, results in the same equations for f_{sw} and D_1 as (3.4), (3.5), and (3.6), where only nU_{out} and U_{in} need to be exchanged in the two equations. By doing so (3.6) is valid for D_1, while D_2 is kept at 0.5. This results in the characteristic waveforms shown in **Fig. 3.7(d)**.

Considering three exemplary input voltages, **Fig. 3.8(a)** gives an overview of the resulting modulation parameters' dependency on the output voltage, for

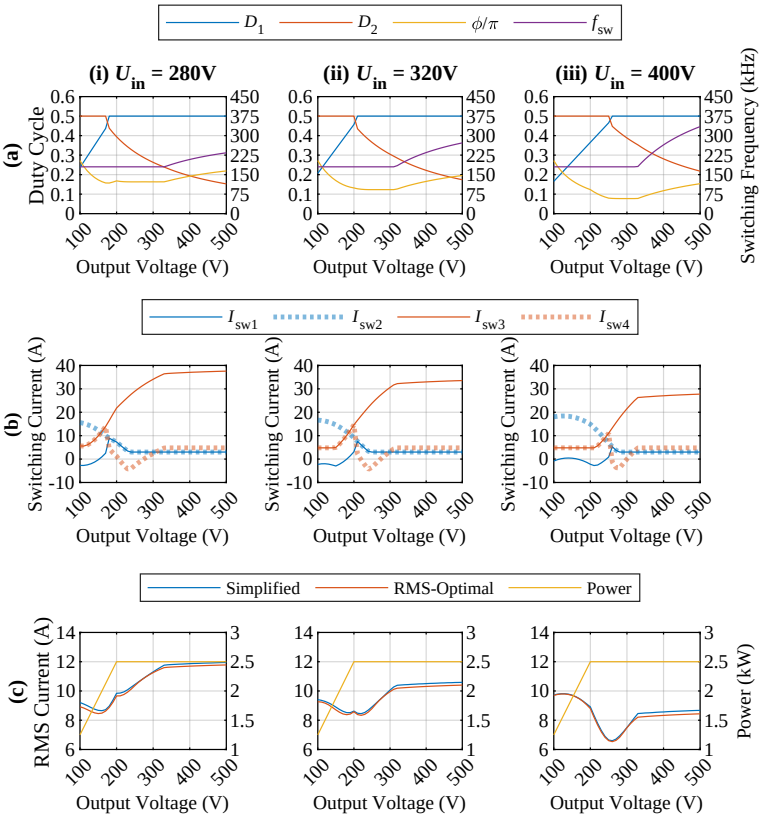


Fig. 3.8: (a) DAB converter control parameters (duty cycles D_1, D_2, normalized phase shift ϕ/π, and switching frequency $f_{sw,DABC}$) obtained with the proposed simplified modulation scheme; note that one duty cycle is always clamped to 0.5. Nominal power (or, for low output voltages, the maximum power compatible with the output current limit of 12.5 A, see (c)), and three different input voltages are considered in (i), (ii), and (iii), respectively. **(b)** Switched currents (I_{sw1} and I_{sw2} are in the primary-side bridge, I_{sw3} and I_{sw4} in the secondary-side bridge) within one half period; positive values indicate ZVS transitions. **(c)** RMS transformer currents of the proposed simplified and the RMS-optimal modulation scheme from [103, 105]. All parameters are calculated for an exemplary transformer with an ELP43 core, operated with a minimum switching frequency of 180 kHz due to saturation reasons. The transformer has a turns ratio of 1.6 and a leakage inductance of 13 µH.

the nominal output power of 2.5 kW (note that at low output voltages, the maximum output current of 12.5 A limits the power as indicated in **Fig. 3.8(c)**).[1] The modulation parameters and the corresponding switching currents are calculated for an exemplary transformer with an ELP43 core, which can be operated with a minimum switching frequency of 180 kHz due to saturation reasons. Furthermore, the transformer has a turns ratio of 1.6 and a leakage inductance of 13 µH.

Furthermore, **Fig. 3.8(b)** shows the four (per half period) switched current values (I_{sw1} and I_{sw2} are for the primary-side bridge, I_{sw3} and I_{sw4} are for the secondary-side bridge), where a negative value indicates hard switching. In the DAB converter, the power and the RMS currents increase with the port voltages and decrease with the switching frequency. To keep the same soft-switching current and output power, the frequency increases with the port voltages as a natural result of (3.4). However, for low port voltages, the required switching frequency for guaranteeing soft-switching conditions would be below the minimum permissible switching frequency of the transformer, which is why for these operating points, the soft switching for all half-bridges cannot be guaranteed anymore. This cannot be remedied by varying the duty cycles either, since a change in the duty cycle has a positive effect on the switching current of one half-bridge, but at the same time hurts the switching current of the second half-bridge, as shown in **Fig. 3.9** for the switching currents I_{sw1} and I_{sw4} of the corresponding half-bridges at the exemplary operating conditions ($U_{in} = 400\,\mathrm{V}$, $U_{out} = 300\,\mathrm{V}$, $n = 1.6$, $L_\sigma = 13\,\mu\mathrm{H}$). When both currents are large enough, the switching frequency is either too small (180 kHz minimum permissible switching frequency of the transformer) or too large (too high winding losses). However, even in the worst case, only one half-bridge is being hard-switched with a relatively low current, which only happens with low voltage and low frequencies, as can be seen in **Fig. 3.8(b)**, whereby the switching losses remain rather small.

Finally, **Fig. 3.8(c)** indicates the transformer RMS current and compares it against that achieved by the RMS-optimal modulation method from [103, 105] (see **Figs. 3.7(c)(e)** for the conceptual waveforms obtained with that modulation method). Clearly, the employed simplified modulation scheme results in only slightly higher RMS current stress, but ensures ZVS for most switching transitions.

[1] Note that for now each operating point's phase shift ϕ is calculated numerically such that the desired power transfer results; in the final realization, ϕ is calculated by the DAB converter voltage controller (see **Sec. 4.3.5.1**).

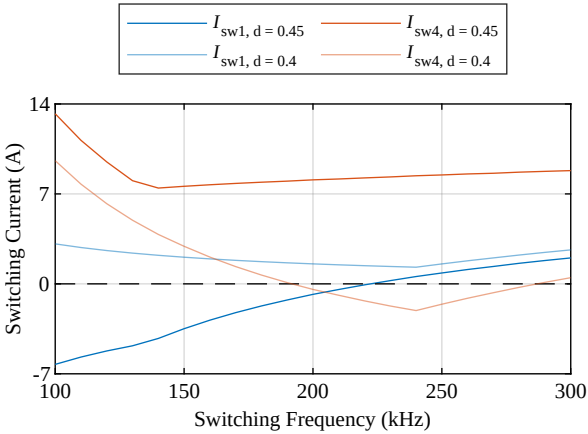


Fig. 3.9: Switching currents I_{sw1} and I_{sw4} of the corresponding half-bridges with different duty cycles D_2 of 0.45 and 0.4 (D_1 = 0.5 for both cases) and different frequencies f_{sw}, where negative switching currents indicate hard-switching conditions of the respective switch. It can be seen that when both currents are large enough, the switching frequency is either too small (180 kHz minimum permissible switching frequency of the transformer) or too large (too high winding losses). The currents are calculated for an exemplary transformer with an ELP43 core, operated with a minimum switching frequency of 180 kHz due to saturation reasons. The transformer has a turns ratio of 1.6 and a leakage inductance of 13 µH.

In order to accurately predict the stresses of different components in the DAB converter, a waveform generator was implemented in MATLAB, considering only ideal waveforms, i.e., no parasitic resistances, capacitances, deadtimes, delays, etc. Based on these calculated component stresses and suitable loss models for the switches (for the considered transistors shown in **Tab. 3.5,** accurate calorimetric switching loss data for both, soft-switched and hard-switched operation has been published earlier [99]) and the magnetic components, an optimization can be carried out similarly to the LLC converter, where possible converter designs for a specific set of design space variables are calculated. The design space variables and their respective limits are listed in **Tab. 3.3**. Hence, the goal of the optimization is to find the optimal combination of transformer turns ratio n and series inductance L_σ. For power density reasons, the series inductance L_σ is implemented as the leakage inductance of the transformer.

Tab. 3.3: Design Space Variables for the Optimization of the DAB Converter Topology.

Parameter	Range
Transformer Turns Ratio n	1.0...2.0
Resonant Inductance L_σ	3 µH...45 µH

The optimization results are shown in **Fig. 3.10**, where the different designs are represented as dots colored according to the turns ratios of the transformer. Similar to the LLC converter, the x-axis in the Pareto optimization is the box volume of the magnetic components. The lowest switching frequency is determined by the selected transformer core, where the peak flux density is limited to 340 mT due to core saturation. Furthermore, the efficiency increases with the turns ratio of the transformer up to a certain point (1.2...1.5), which means that the DAB converter is in general less efficient in buck-mode than in boost-mode, the same characteristic as given for the LLC converter due to the large current in buck-mode. The selected design is marked with a red star in **Fig. 3.10**, where a slightly higher turns ratio (1.6) is selected, to have more circulating currents such that ZVS can be achieved in a larger range (as can be seen later in **Sec. 3.3.3** and **Sec. 3.5.2**, the DAB converter can easily have higher switching losses in reality than in calculations due to the extremely sensitive switching currents towards non-idealities in the circuit). The transformer is built with an N97 ELP_{43} core and litz wires with comparably thin single strand diameter of 40 µm with 1200 strands, since the magnetic fields due to the large leakage inductance of 13 µH within the winding window are extremely high and would lead to significant HF conduction losses, if litz wires with thicker strands would be employed. The details of the transformer design and the employed semiconductors of the selected hardware demonstrator design are summarized in **Tab. 3.5**.

3.3.3 Measurements of the DAB Converter

In order to experimentally verify the loss models of the DAB converter optimization, the aforementioned design is realized in a 2.5 kW hardware demonstrator. In **Fig. 3.11** and **Fig. 3.12**, the experimentally measured voltage and current waveforms of the DAB converter for 100 V, 200 V, 300 V and 400 V output voltage at full load are shown, where the input voltage is selected in such a way, that the converter is operated at unity gain if possible, or at least with minimum step-up or step-down ratio.

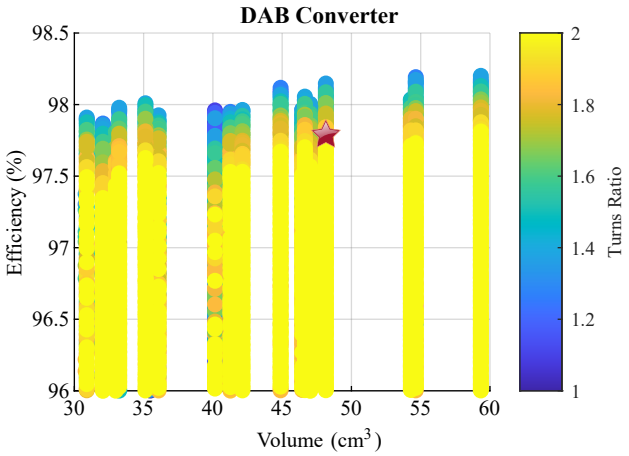


Fig. 3.10: Pareto optimization results of a 2.5 kW DAB converter module, where the volume on the x-axis corresponds to the total magnetics volume and the color-coding of the different converter designs (dots) indicates the turns ratio of the transformer. The converter design, which has finally been implemented in hardware is marked with a red star.

During commissioning, it was found that the actually measured waveforms sometimes slightly deviate from the calculated waveforms, since the parasitic components, the deadtime, digital delays, and so on are not considered in the waveform generator of the optimization. Although in most topologies this does not have a major impact on the efficiency, it is the case for the DAB converter, since the switching currents in a DAB converter react very sensitively to minor changes in the modulation and the voltage waveforms. Consequently, the non-idealities can easily increase or decrease the switching currents by a few amperes, which causes the switching losses to increase substantially [106]. For this reason, the waveform generator must take all the non-idealities into account so that the occurring switching losses can be accurately predicted.

In the first step, the effects of all resistances in the current path and of the magnetizing inductance on the primary-side and secondary-side current, are considered according to [107]. Subsequently, the voltage-time areas applied across the transformer windings during the deadtime of 50 ns are also considered, which can be estimated based on the output capacitances C_{oss} of the semiconductors and the direction and the magnitude of the switching

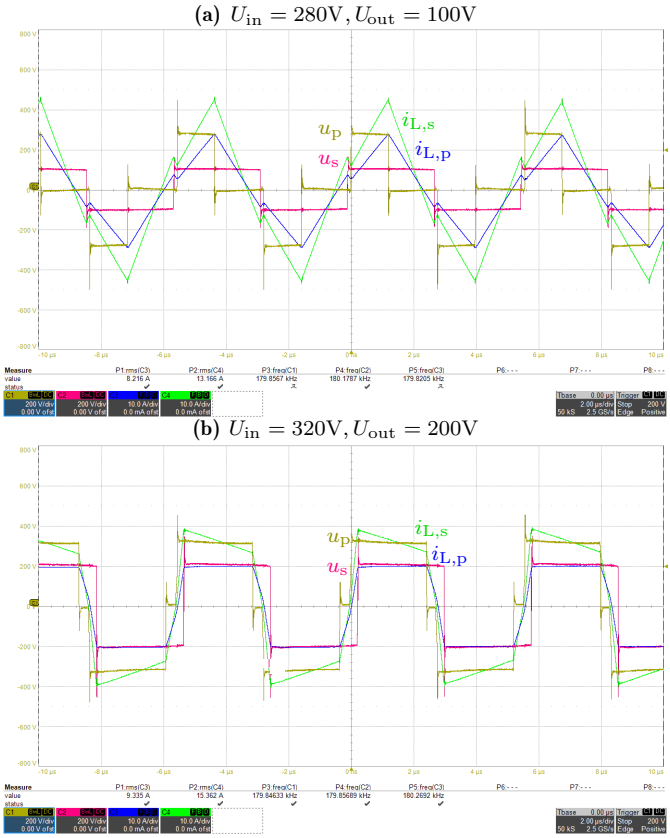


Fig. 3.11: Experimentally measured waveforms of the 2.5 kW DAB converter hardware demonstrator for an output voltage U_{out} of **(a)** 100 V and **(b)** 200 V at full load, with the input voltage U_{in} selected in such a way that the converter is operated with unity gain or at least with minimum step-up or step-down ratio, where u_{p}, u_{s}, i_{p} and i_{s} are the primary-side and secondary-side winding voltages and the primary-side and secondary-side transformer currents, respectively.

current. A few iterations in the waveform generator are sufficient to let the current waveform converge to a final shape, by means of which the switching losses (soft-switching, partial hard-switching and hard-switching losses) can be predicted according to [106].

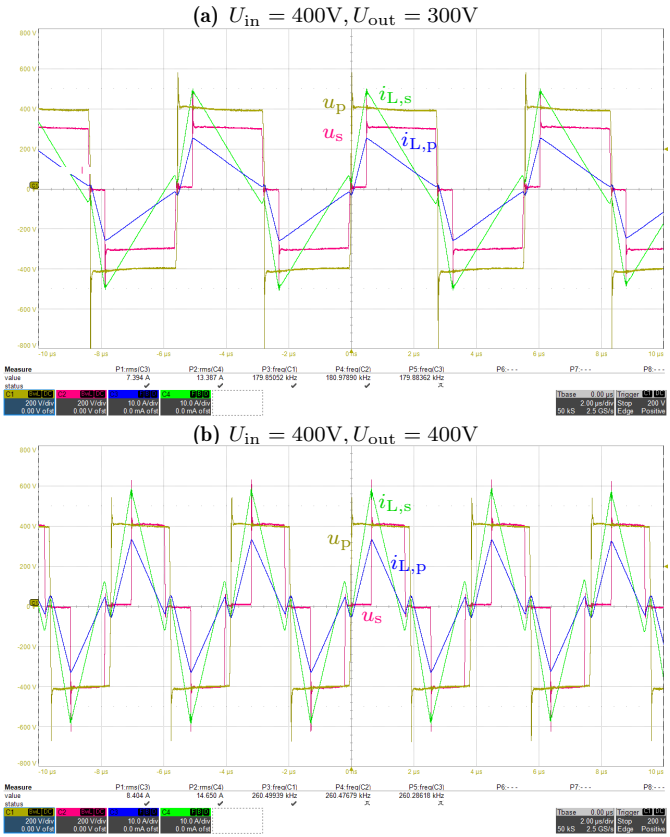


Fig. 3.12: Experimentally measured waveforms of the 2.5 kW DAB converter hardware demonstrator for an output voltage U_{out} of **(a)** 300 V and **(b)** 400 V at full load, with the input voltage U_{in} selected in such a way that the converter is operated with unity gain or at least with minimum step-up or step-down ratio, where u_{p}, u_{s}, i_{p} and i_{s} are the primary-side and secondary-side winding voltages and the primary-side and secondary-side transformer currents, respectively.

The accurately calculated and measured efficiencies of the overall system are shown in **Fig. 3.13** with the loss breakdowns for different operating points, where it can be seen that, depending on the operating point, completely different loss components dominate, which makes the efficient design of such systems for wide voltage ranges so difficult. For low output voltages, the

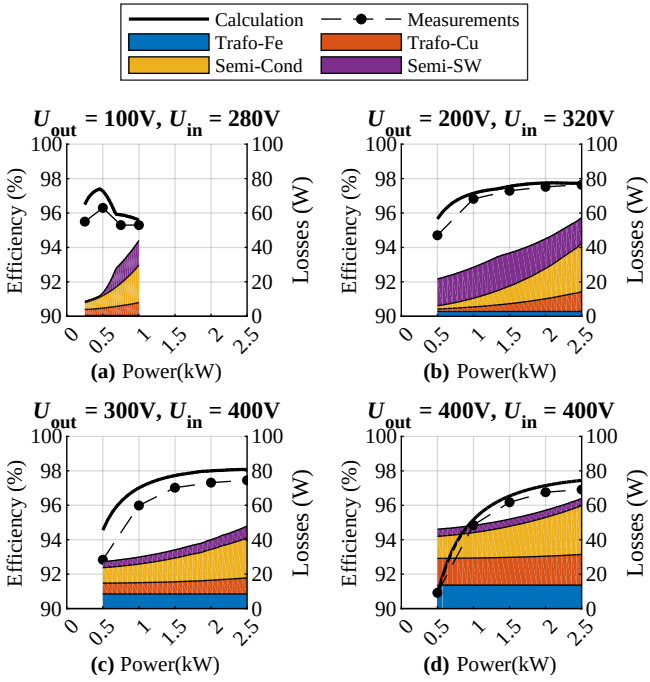


Fig. 3.13: The calculated and the measured efficiencies of the 2.5 kW DAB converter hardware demonstrator for output voltages of **(a)** 100 V, **(b)** 200 V, **(c)** 300 V, and **(d)** 400 V, including the respective loss breakdowns.

switching losses are comparably large, as the required switching frequency to achieve soft switching is not reached and therefore hard switching occurs. The conduction losses (yellow and orange region) decrease with power, since the step-down ratio is not too high (with a turns ratio at 1.6, which helps buck-mode at low output voltages) and the circulating current is moderate. For higher output voltages, e.g., in **Fig. 3.13(d)**, the step-up ratio is relatively high due to the turns ratio, leading to a rather large circulating current/reactive power. The conduction losses of the switches (yellow region) decrease much less with power, and the winding losses (orange region) barely decrease due to the harmonic components.

Furthermore, the loss components shown in **Fig. 3.13** and the sensitivity of the switching currents towards non-idealities indicate that the selection of the input voltage U_{in} might not be optimal, since a few volts of difference

in U_{in} might result in different switching conditions and therefore totally different switching losses. Therefore, for the DAB converter in the application at hand, the input voltage is theoretically another dimension to be included in the optimization, which, however, is difficult to implement in reality due to discontinuous transitions, further complicating the design and operation of the system, which is why it is not considered here.

Although the two topologies analyzed so far had their advantages, they also had severe disadvantages, since the LLC converter, for example, is easy to control but requires a very wide switching frequency range, while the DAB converter, on the other hand, manages to operate with a narrower switching frequency range, but is more difficult to control and to design. For this reason, a third, rather unknown topology is analyzed in the following, which is very easy to control and is operated with a constant switching frequency.

3.4 Quantum Series Resonant Converter

3.4.1 Operating Principle of the QSRC

Even though the QSRC topology [108, 109] can hardly be distinguished from the LLC converter topology, there is one important difference to the LLC converter, namely the secondary-side full-bridge must be implemented with active switches if the QSRC also needs to be used in boost-mode. If only buck-mode is required, the secondary-side full-bridge can also be implemented with passive diodes, as in a conventional LLC converter. Furthermore, the resonant tank can be placed either on the primary side or secondary side of the transformer, depending on the specifications and design requirements, as will be explained later in this section. In terms of control, the operating modes can be classified into three categories depending on the voltage transfer ratio: the buck-mode, the boost-mode, and the SRC-mode. Whichever mode it is in, the switching frequency f_{sw} is constant and chosen to be equal to or slightly higher than the resonant frequency of the resonant tank. The term "quantum" in the name of the topology comes from the fact that the control variable can only be adjusted at the beginning of each switching half period and is therefore "discretized", as will be explained in the following for the three operating modes.

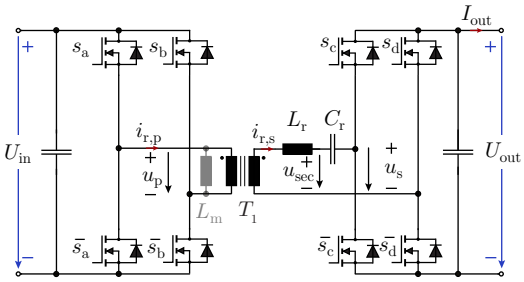


Fig. 3.14: Topology of the Quantum Series Resonant Converter (QSRC) with the resonant tank placed on the secondary side of the transformer. The magnetizing inductance is only used for soft switching and not for voltage regulation, therefore greyed out to differentiate the topology from LLC converter.

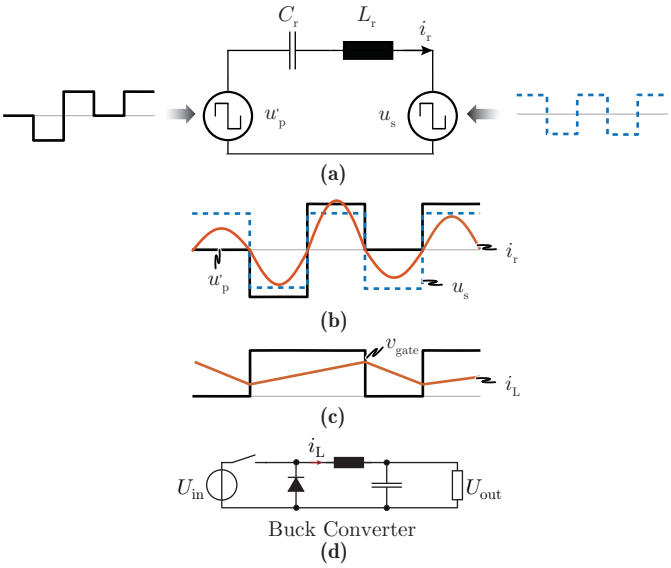


Fig. 3.15: Operating principle of the QSRC in buck-mode, with the equivalent circuit in **(a)**, characteristic waveforms in **(b)**, and the analogy to a conventional non-isolated buck converter with the corresponding characteristic waveforms in **(c)**, topology in **(d)**.

3.4.1.1 Buck-Mode

In buck-mode, the input voltage is higher than the primary-side referred output voltage. The full-bridge on the secondary side is operated as a synchronous rectifier and therefore has no active influence on the transmitted power. The primary side, on the other hand, is actively controlled and generates a voltage u_p on the primary side of the transformer of $+U_\mathrm{in}$, 0 V, or $-U_\mathrm{in}$ (cf. **Fig. 3.15**). If a voltage u_p of $+U_\mathrm{in}$ or $-U_\mathrm{in}$ is applied, this is referred to as full-voltage interval or full-voltage period in the following. If, on the other hand, 0 V is applied, this is referred to as a zero-voltage interval or zero-voltage period. Hence, applying a full-voltage interval on the primary side of the transformer, which is larger than the primary-side referred output voltage, increases the amplitude of the resonant current i_r, whereas a zero-voltage interval decreases i_r. Thus, by controlling the average resonant current, the desired output voltage can be achieved. If the output voltage is too small, then the number of full-voltage intervals needs to be increased, and vice versa if the output voltage is too high. The general operating principle is therefore similar to a conventional buck converter, where the inductor current increases if there is a positive voltage applied at the switch node, and the current decreases when no voltage is applied, i.e., the free-wheeling diode is conducting.

In order to facilitate the mathematical characterization of the QSRC, a macroscopic period t_p and macroscopic duty cycle $d_\mathrm{m,buck}$ can be defined as in a conventional buck converter. The macroscopic period consists of n_p half resonant periods, and is repeated like the switching period for pulse-width-modulated converters. In buck-mode, during one macroscopic period, the macroscopic duty cycle $d_\mathrm{m,buck}$ is defined as the ratio of the number of full-voltage periods n_full and the number of half resonant periods n_p over a macroscopic period t_p, according to:

$$d_\mathrm{m,buck} = \frac{t_\mathrm{full}}{t_\mathrm{p}} = \frac{n_\mathrm{full}}{n_\mathrm{p}}. \tag{3.7}$$

The voltage transfer ratio of the QSRC can be determined using the same equation as for a buck converter:

$$\frac{U_\mathrm{out}}{U_\mathrm{in}} = d_\mathrm{m,buck}. \tag{3.8}$$

3.4.1.2 Boost-Mode

In boost-mode, the primary-side full-bridge is constantly applying full-voltage intervals to the primary transformer winding, whereas the secondary-side full-bridge is now actively controlled and either applies full-voltage or zero-voltage intervals to the resonant tank and the transformer (cf. **Fig. 3.16**). In the case of zero-voltage intervals, the current in the resonant tank increases, whereby this additional energy is transferred to the output during the full-voltage intervals. This is similar to a conventional boost converter, where the inductor current and, therefore, the magnetic energy in the inductor is increasing while the switch is turned on. Subsequently, when the switch is turned off, the stored energy is transferred to the output with a higher voltage. Thus, similar to the buck-mode, the output voltage of the QSRC in boost-mode is controlled by the ratio between zero-voltage and full-voltage periods, and $d_{\mathrm{m,boost}}$ can be defined as

$$d_{\mathrm{m,boost}} = \frac{t_{\mathrm{zero}}}{t_{\mathrm{p}}} = \frac{n_{\mathrm{zero}}}{n_{\mathrm{p}}}. \tag{3.9}$$

For the voltage transfer ratio, the same equation as for a conventional boost converter is used:

$$\frac{U_{\mathrm{out}}}{U_{\mathrm{in}}} = \frac{1}{1 - d_{\mathrm{m,boost}}}. \tag{3.10}$$

3.4.1.3 SRC-Mode

In the SRC-mode, where the QSRC features unity gain and the input voltage is equal to the primary-side referred output voltage, the converter is operated like a conventional series resonant converter, whereby the secondary-side full-bridge is again operated as a synchronous rectifier and the primary-side full-bridge generates full-voltage intervals only.

3.4.2 Control Principle of the QSRC

Despite all the similarities between the QSRC and conventional buck/boost converters, the QSRC cannot be directly controlled like the pulse-width-modulated converters, since the discretization of the control parameter (zero-voltage intervals and full-voltage intervals) leads to a tradeoff between control accuracy and control bandwidth. For example, if a resolution of the duty cycle $d_{\mathrm{m,buck}}$ of 1 % is required, at least 100 half resonant periods must be

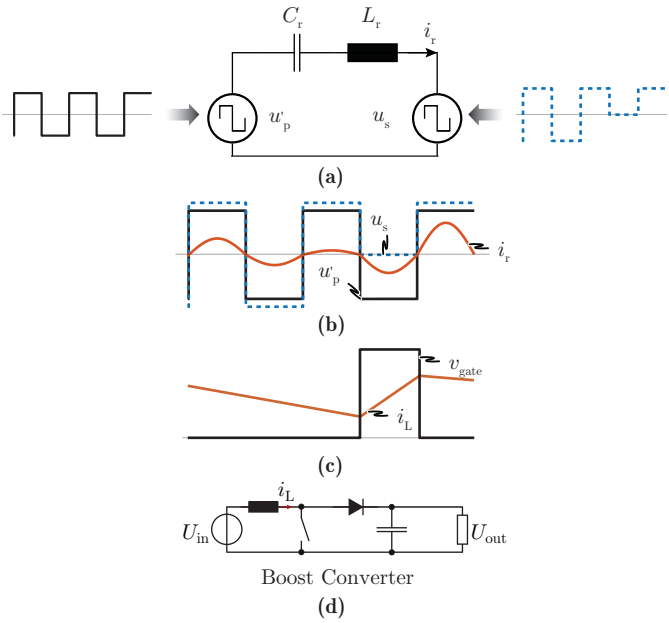


Fig. 3.16: Operating principle of the QSRC in boost-mode, with the equivalent circuit in **(a)**, characteristic waveforms in **(b)**, and the analogy to a conventional non-isolated boost converter with the corresponding characteristic waveforms in **(c)**, topology in **(d)**.

used for n_p, which for a resonant frequency of e.g., 300 kHz would lead to a controller update frequency of only 3 kHz. Unfortunately, this is way too slow for the application at hand, as a high controller bandwidth of the DC/DC stage is required if the PFC rectifier front-end should be operated using the proposed synergetic control. Furthermore, for the same voltage transfer ratio, different from conventional buck/boost converters, the voltage sequence, i.e., the arrangement of the positions of the full-voltage intervals and zero-voltage intervals influences the RMS current stress significantly [110], which cannot be taken into account in conventional duty cycle control or modulation.

For this reason, no direct pulse-width modulation is used for the QSRC, but a cascaded hysteresis control [111, 112] is employed as shown in **Fig. 3.17**, where the output voltage U_{out} is measured and compared to the reference, and the error is sent to an outer voltage PI control loop to produce the current reference $i^*_{r,s}$. The inner hysteresis current control loop compares the current

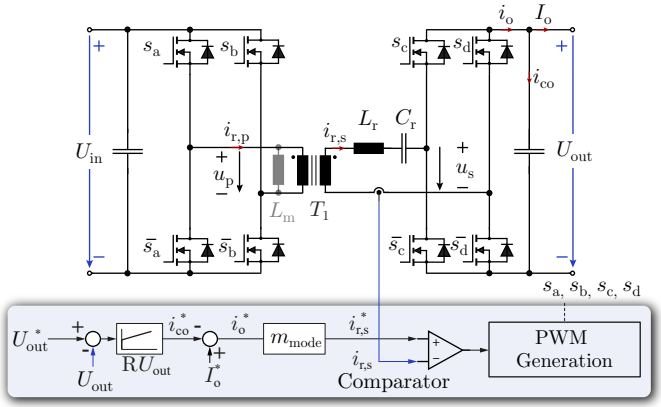


Fig. 3.17: Control structure of the QSRC with the $L_r - C_r$ resonant tank placed on the secondary side of the transformer.

reference $i^*_{r,s}$ with the measured resonant current $i_{r,s}$, which can either be a peak current measurement or an average current measurement over half a resonant period. Depending on the current deviation, the controller tries to decrease the error by adding or removing zero-voltage intervals to either the primary-side full-bridge in buck-mode, or the secondary-side full-bridge in boost-mode. This control method can achieve a relatively high controller bandwidth, while the resulting voltage patterns lead to almost the minimum possible RMS current stresses in the system.

However, even though minimal conduction losses can be achieved with this control, the switching currents must also be analyzed more precisely so that soft switching can be guaranteed for all semiconductors, which is done in the following.

3.4.3 Soft-Switching Schemes of the QSRC

3.4.3.1 Discrete Series Inductor

In the conventional SRC, the soft switching for the primary-side full-bridge is usually achieved by using the magnetizing current of the transformer, whereas the secondary-side full-bridge is operated as a synchronous rectifier and is therefore inherently performing ZVS. Using the magnetizing current for achieving ZVS of the primary-side switches is feasible, as long as the current directions are correct during the switching transitions. This is, however, not

the case for some operating modes of the QSRC, as will be explained in the following. In the first step, it is assumed that the resonant inductor L_r is implemented as a discrete component for simplicity reasons. If the resonant tank is placed on the secondary side of the transformer, the magnetizing current is mostly determined by the primary-side applied voltage, if the leakage inductance of the transformer is much smaller than the inductance of the discrete inductor. Consequently, in boost-mode, the magnetizing current is symmetrical due to the symmetrical voltage-time areas applied to the transformer. However, in buck-mode, the primary-side full-bridge generates an arbitrary sequence of full-voltage and zero-voltage intervals due to the hysteresis control, which results in inappropriate voltage patterns applied to the transformer, and, therefore, wrong directions of the magnetizing currents during switching transitions as well, as shown in **Fig. 3.18(b)**, leading to hard-switching transitions, as marked by the red circles.

The same happens in boost-mode, if the resonant tank is placed on the primary side of the transformer. Hence if both step-up and step-down functionalities are required, only those voltage sequences that guarantee the correct direction of the magnetizing currents during switching transitions should be used, where ZVS conditions can be achieved. This is easiest to fulfill by using only zero-voltage intervals with a length of one complete resonant period, while the full-voltage intervals can still have a length of any integer multiple of half a resonant period (cf. **Figs. 3.18(c)(d)**). Two different voltage sequences are shown here, where one ensures the same positive and negative amplitude of the magnetizing current (cf. **Fig. 3.18(d)**) and the other doesn't (cf. **Fig. 3.18(c)**), but both can facilitate ZVS conditions due to correction directions of the magnetizing currents during switching transitions. The pattern in **Fig. 3.18(c)** requires a higher magnetizing current to achieve full soft switching for all transitions, which leads to higher core losses due to the higher peak flux density, but also results in lower RMS current due to the more uniformly distributed zero and full-voltage intervals, compared to **Fig. 3.18(d)**. It then depends on the specific design to choose the best pattern which yields the lowest losses.

Even though the restriction of the length of the zero-voltage intervals leads to slightly higher RMS current stresses in the power components, this restriction pays off, since the savings in switching losses by far exceed the increase in conduction losses. It needs to be noted that only one mode is required to use such voltage sequences, as the buck-mode when placing the resonant tank on the primary side, and boost-mode when placing the resonant tank on the secondary side always have symmetrical magnetizing currents.

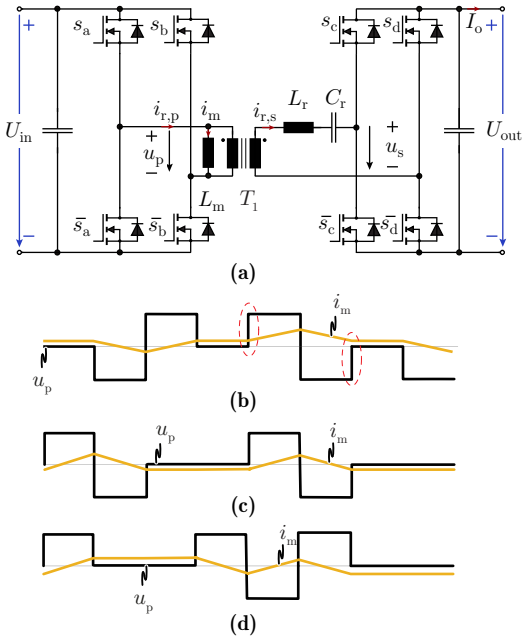


Fig. 3.18: The topology of the QSRC with the resonant tank on the secondary side and the magnetizing inductance explicitly shown in **(a)**, and three different voltage sequences of the primary-side applied voltage in buck-mode with identical numbers of full-voltage and zero-voltage intervals (hence, a similar output power), but different resulting magnetizing currents as well as different switching conditions for the semiconductors, with voltage sequence **(b)** leading to asymmetrical magnetizing current, where positive magnetizing currents during rising voltage edges result in hard-switching conditions; **(c)** voltage sequence leading to asymmetrical magnetizing current (different positive and negative amplitudes) but with correct directions, where ZVS can be achieved, **(d)** voltage sequence leading to symmetrical magnetizing current (same positive and negative amplitude) and ZVS switching conditions.

Therefore, the position of the resonant tank (primary or secondary) will affect the RMS current in the system due to the required voltage sequences, and is then a dimension to be optimized, which will be further discussed in **Sec. 3.4.4.2**.

If not a discrete inductor is used for the resonance tank, but rather the leakage inductance of the transformer, the calculation of the magnetizing current is no longer straightforward, since different voltages are induced

in the two transformer windings. Consequently, ZVS conditions cannot be guaranteed so easily, which is why this special case is examined in detail in the following.

3.4.3.2 Integrated Series Inductor

If the leakage inductance of the transformer is used as the resonant inductor, the realization of soft-switching conditions is more complicated, as the magnetizing current now depends on both the primary-side and the secondary-side applied voltages, as well as on the structure of the transformer. Since the secondary-side transformer terminal voltage u_{sec} (not the switch node voltage u_{s}, cf. **Fig. 3.14**) depends on the asymmetric capacitor voltage u_{r}, which cannot be balanced in every switching period even using the voltage patterns introduced in the last section, this inevitably leads to an inappropriate magnetizing current, which is repeated only in a macroscopic cycle. This results in a wide variety of switching currents during this macroscopic cycle, some of which even have the wrong signs and thus lead to hard-switching conditions for the semiconductors.

For this reason, when using the leakage inductance as the resonant inductance, the magnetizing current would have to be calculated for a wide variety of voltage patterns and output power values, whereby the permitted voltage patterns would need to be stored in a comprehensive lookup table which then needs to be implemented in the control hardware. However, this is very complex and usually obsolete anyway, since the resonant inductances required for the QSRC are often too large to be reasonably integrated as leakage inductance in the transformer (as will be explained in the next section, due to the continuous conduction mode of the QSRC). Therefore, only discrete resonant inductors are considered in the optimization of the QSRC in the following sections. As a simple solution to decrease the total box volume, one can also choose to use the same type of core as for the transformer also for the inductor, as well as the same litz wire and the same number of turns of the secondary side (or primary side depending on the location of the resonant tank), such that the secondary winding of the transformer is shared with the inductor.

3.4.4 Design and Optimization of the QSRC

There are several degrees of freedom in the optimization of the QSRC, for example, the resonant tank's inductance/impedance, the location of the resonant tank, the transformer turns ratio, as well as the resonant frequency. Due

to the large number of sweep parameters, a multitude of different designs would have to be calculated in a brute force optimization, which is why it is worth developing rough design guidelines in a first step, with the help of which the limits of the sweep parameters can be narrowed down. One of the most important criteria for determining if a certain QSRC design is sensible or not is whether the converter is operated in continuous conduction mode (CCM) over the entire operating range (full load). The CCM is characterized by a continuous sinusoidal current flowing through the transformer, which results in minimum RMS current stresses in the power components for certain required output power. However, this is only the case if the resonant inductance is above a certain level, which is why this criterion can directly be used to calculate the minimum required resonant inductance for a given resonant frequency. For power density reasons, this minimum inductance is, at the same time, the optimal resonant inductance, which is why this parameter can be analytically calculated and is therefore not anymore part of the optimization. Furthermore, the position of the resonant tank can be selected to reduce the value of the inductance. Consequently, the only remaining sweep parameters are the turns ratio of the transformer and the resonant frequency, as will be explained in detail in the following.

3.4.4.1 Continuous Conduction Mode

In order to be able to estimate the effect of the quantum operation on the RMS current stresses of the power components, the transformer winding currents during a macroscopic period can be approximated in a simplified manner as a series of half-sine waves with linearly increasing amplitudes. Thus, assuming a macroscopic period with an exemplary length of five half resonant periods (cf. **Fig. 3.19(a)**), the amplitudes of the five half periods can be expressed as:

$$\hat{I}_1 = (1-k)\cdot\hat{I}, \quad \hat{I}_2 = \left(1-\frac{k}{2}\right)\cdot\hat{I}, \quad \hat{I}_3 = \hat{I}, \quad \hat{I}_4 = \left(1+\frac{k}{2}\right)\cdot\hat{I}, \quad \hat{I}_5 = (1+k)\cdot\hat{I}, \tag{3.11}$$

with $k \in (0,1)$ and $\hat{I}$ being the average amplitude of the resonant current. This sequence of half-sine waves is repeated periodically during operation, which is why this sequence is referred to as the macroscopic period, as previously mentioned. Even though the amplitudes $\hat{I}_x$ change within the macroscopic period, they are always greater than zero, and therefore power is continuously transmitted. This operating mode is then referred to as CCM.

The average current I_{CCM} during a macroscopic period is independent of k and is given as $I_{\mathrm{CCM}} = \frac{\hat{I}}{\pi/2}$, whereas the RMS current in CCM does depend on k and can be derived as:

$$\begin{aligned} I_{\mathrm{r,rms}} &= \sqrt{\frac{1}{5}\left(\left((1+k)\,I_{\mathrm{rms}}\right)^2 + \ldots \left((1-k)\,I_{\mathrm{rms}}\right)^2\right)} \\ &= \sqrt{1+0.5k^2}\cdot I_{\mathrm{rms}}, \end{aligned} \tag{3.12}$$

with I_{rms} being the RMS current of the ideal current waveform where each half resonant period has the same amplitude. This equation shows that the variation of the current amplitudes $\hat{I}_{\mathrm{x}}$ due to the quantum control of the resonance converter does not have a particularly negative impact on the resulting conduction losses, since, for example, an amplitude variation of +/- 50 % results in a conduction loss increase of only approximately 12 % (cf. **Fig. 3.19(b)**).

However, this only applies to the operation of the converter in continuous conduction mode. If a too-small resonant inductance is selected, the resonant capacitor voltage u_{c} in, e.g., buck-mode, might not be high enough during the zero-voltage intervals on the primary side to continue driving a positive current through the secondary-side synchronous rectifier. This is the case if u_{c} at the beginning of a zero-voltage half resonant period is lower than the output voltage U_{out}. Hence, during this half resonant period, there is no current flow in the system and, therefore, no power flow to the output. This lack of power needs to be compensated for in the following full-voltage intervals. Assuming that the macroscopic period again consists of five half resonant intervals, the first being a zero-voltage interval followed by four full-voltage intervals, and at the same time a resonant inductance chosen so small that no power is transmitted during the zero-voltage interval, then the entire power must be transmitted during four instead of five half resonant intervals, which is referred to as discontinuous conduction mode (DCM). Consequently, the average current I_{DCM}, and therefore also the average peak current $\hat{I}_{\mathrm{DCM}}$ in DCM during the full-voltage intervals need to be 25 % higher than in CCM, resulting in a significant increase of the RMS current in the transformer according to:

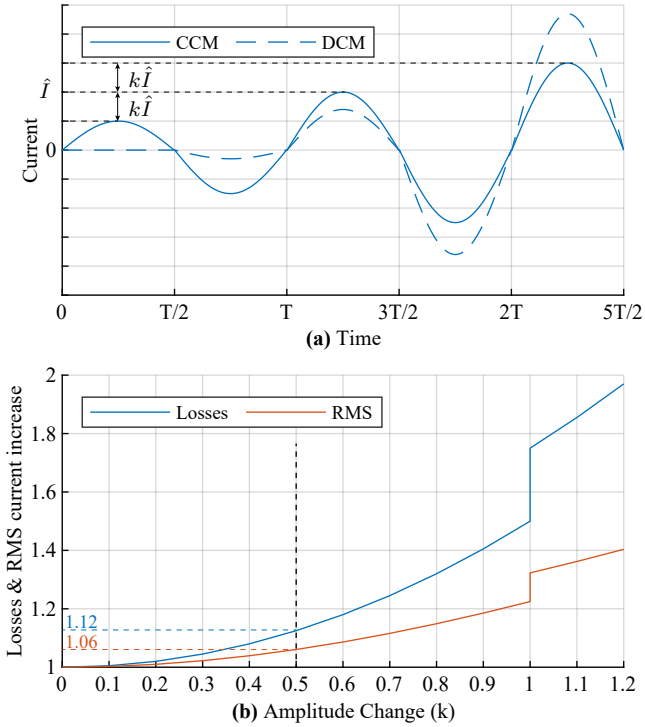


Fig. 3.19: Typical QSRC CCM and DCM current waveforms in **(a)**, RMS current and losses increase versus amplitude change in **(b)**.

$$I_{\mathrm{r,rms}} = \sqrt{\frac{\hat{I}_{\mathrm{rms}}^2}{5} \cdot \left((1.25-k)^2 + \left(1.25 - \frac{k}{2}\right)^2 + \left(1.25 + \frac{k}{2}\right)^2 + (1.25+k)^2 \right)}$$
$$= \sqrt{1.25 + 0.5k^2} \cdot I_{\mathrm{rms}}, \tag{3.13}$$

with $k \in (1, 1.25)$, as shown in **Fig. 3.19(b)**.

Thus, in CCM, even an amplitude change of up to 50 % only marginally increases the occurring conduction losses (< 12 %), but at the boundary between CCM and DCM ($k = 1$), there is a step in terms of conduction losses of almost 30 %, even though the exact same power is transferred. This clearly shows

why it is so important to remain in the CCM over the entire operating range, as otherwise high conduction losses would occur, which could have been relatively easily prevented with a suitable dimensioning of the resonant tank. Hence, when designing a QSRC, the resonant inductor should be chosen to be large enough to keep the converter in CCM under all operating conditions to take full advantage of the QSRC topology.

In order to ensure that the QSRC operates in CCM, the current and voltage waveforms in the resonant tank must be calculated in both buck-mode and boost-mode for different inductance values. Based on these waveforms, the minimum required inductance can be found, which is just large enough to ensure CCM over the entire operating range.

The resonant inductor current $i_{\mathrm{r,k}}$ and resonant capacitor voltage $u_{\mathrm{c,k}}$ for k^{th} half resonant period can be calculated according to:

$$i_{\mathrm{r,k}}(t) = \frac{u_{\mathrm{d,k}} - u_{\mathrm{c0,k}}}{Z_0} \sin\left(\omega_0 t - (k-1)\,\pi\right) \tag{3.14}$$

and

$$u_{\mathrm{c,k}}(t) = u_{\mathrm{d,k}} - \left(u_{\mathrm{d,k}} - u_{\mathrm{c0,k}}\right) \cos\left(\omega_0 t - (k-1)\pi\right), \tag{3.15}$$

where the magnetizing current and parasitic resistances of the components are neglected for simplicity reasons. The voltage $u_{\mathrm{d,k}}$ in the expressions is the DC voltage applied to the resonant tank in the respective half resonant period, i.e., the difference between the primary-side switch-node voltage $u_{\mathrm{p,k}}$ and secondary-side switch-node voltage $u_{\mathrm{s,k}}$, and is considered to be known for a certain voltage sequence, according to:

$$u_{\mathrm{d,k}} = u_{\mathrm{p,k}} - u_{\mathrm{s,k}}. \tag{3.16}$$

Furthermore, the characteristic impedance Z_0 and the resonant frequency ω_0 are given as:

$$Z_0 = \sqrt{\frac{L_{\mathrm{r}}}{C_{\mathrm{r}}}}, \tag{3.17}$$

and

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_{\mathrm{r}} C_{\mathrm{r}}}}, \tag{3.18}$$

respectively. $u_{c0,k}$ is the initial capacitor voltage at the beginning of the kth half resonant period, and therefore $u_{c0,k} = u_{c,k}\left(t = \frac{(k-1)\pi}{\omega_0}\right)$, which can be derived according to:

$$\begin{aligned} u_{c0,k} &= u_{c,k-1}\left(t = \frac{(k-1)\,\pi}{\omega_0}\right) \\ &= u_{d,k-1} - \left(u_{d,k-1} - u_{c0,k-1}\right) cos\,(\pi) \\ &= 2u_{d,k-1} - u_{c0,k-1} \\ &= 2u_{d,k-1} - 2u_{d,k-2} + u_{c0,k-2} \\ &\dots \\ &= 2\left(u_{d,k-1} + (-1)^1 u_{d,k-2} + (-1)^2 u_{d,k-3} \dots + (-1)^{k-2} u_{d,1}\right) + (-1)^{k-1} u_{c0,1}, \end{aligned} \tag{3.19}$$

whereby the initial capacitor voltage $u_{c0,1}$ at the beginning of the overall voltage sequence is the only unknown in this equation. Based on (3.14), the resonant current $i_{r,k}$ in each half resonant period can be calculated. In order to guarantee the required output power, the average value of $i_{r,k}$ over the macroscopic period should be equal to the average output current $I_{out} = P_{out}/U_{out}$ in buck-mode or the average input current $I_{in} = P_{in}/U_{in}$ in boost-mode, respectively. This condition can now be used to numerically calculate the still unknown initial capacitor voltage $u_{c0,1}$. Consequently, following this sequence of calculations allows the determination of the inductor currents and the capacitor voltages for arbitrary voltage sequences, resonant tanks and operating conditions.

The condition that the QSRC stays in CCM is then for each zero-voltage period in buck-mode and full-voltage period in boost-mode:

$$|u_{c0,k}| > |u_{d,k}|. \tag{3.20}$$

Hence, for each macroscopic period containing n_{full} full-voltage intervals and a total of n_p half resonant periods, the possible number of voltage sequences, i.e., permutations, is given as $P_k^n = \frac{n!}{(n-k)!} = \frac{n_p!}{n_{full}!}$, which inherently lead to the same transferred power. Consequently, for each permutation the resulting capacitor voltages need to be calculated and the condition of (3.20) needs to be checked, until at least one permutation is found that fulfills (3.20) and can therefore be used as feasible voltage sequence which both ensures the required output power and guarantees CCM. However, if for a certain Z_0

none of the permutations satisfies (3.20), then this is a clear indicator that the inductor is below the minimum required inductance value for CCM, which is why the calculation must be repeated with a larger Z_0 until the smallest Z_0 is found that results in CCM over the entire operating range.

In order to reduce the number of calculations required, it makes sense to consider the worst-case conditions under which CCM is most difficult to achieve. In buck-mode, it is obvious that it is most difficult to guarantee CCM when the output voltage is at its maximum, because on the one hand the current in the resonant tank is relatively low and thus the capacitor voltage is only slightly deflected (small $|u_{c0,k}|$ in (3.20)), and at the same time the output voltage and thus the $|u_{d,k}|$ becomes maximum. Consequently, the CCM criterion needs to be fulfilled especially for the operation close to the unity gain in buck-mode. In boost-mode, the relationships are no longer so obvious, since on the one hand, the voltage $|u_{d,k}|$ increases with the output voltage, but on the other hand the capacitor voltage $|u_{c0,k}|$ does increase too, due to the increasing current ripple and the resulting large currents during the full-voltage intervals. For this reason, it is essential to find the worst-case conditions using a sweep over the entire boost range, whereby it turns out for the application at hand that the operation close to unity gain also describes the worst-case operating conditions in boost-mode. Hence, assuming a transformer with a 1 : 1 turns ratio and the specifications given in **Fig. 1.2**, the QSRC will operate at unity gain for output voltages between 280 V and 400 V, where the input voltage is controlled to follow approximately the output voltage. Thus, the worst-case operating point for buck-mode is the operation slightly below 280 V, whereas for boost-mode it is slightly above 400 V. When the turns ratio changes, the worst-case scenario then changes accordingly.

3.4.4.2 Resonant Tank Position

As already mentioned at the beginning of the previous section, the placement of the resonant tank plays a major role in controlling the QSRC, since depending on the placement, the available voltage sequences are limited either in buck-mode or in boost-mode, since only those which lead to the required magnetizing current may be used. Thus, due to these limitations, not all permutations of voltage sequences are available to achieve CCM (cf. (3.20)), which is why the selection of the placement of the resonance tank also has an influence on the minimum required inductance L_r.

The calculated minimum required resonant inductance values are shown in **Fig. 3.20** for placement of the resonant tank on the primary side and sec-

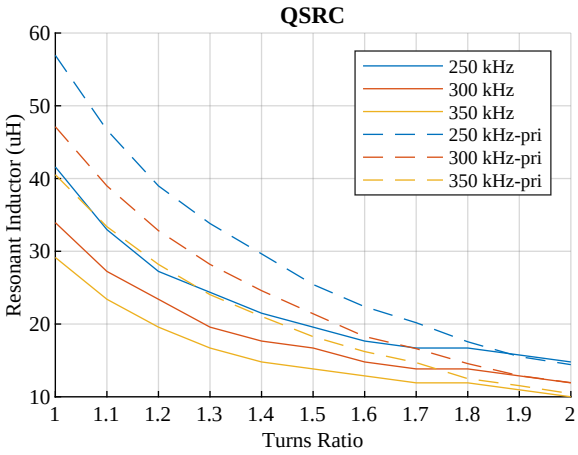


Fig. 3.20: Minimum required resonant inductance values for different turns ratios of the transformer and different resonant frequencies, where the solid lines correspond to the QSRC topology with the resonant tank on the secondary side, where the available switching patterns are limited by the magnetizing current constraint in buck-mode, and the dashed lines correspond to the QSRC topology with the resonant tank on the primary side, where the available switching patterns are limited by the magnetizing current constraint in boost-mode. All values are referred to the secondary side of the transformer in order to allow for a direct comparison.

ondary side of the transformer, for different resonant frequencies and different turns ratios (all values referred to the secondary side of the transformer). It can be seen that the placement of the resonant tank on the secondary side is more beneficial when it comes to the minimum required resonant inductance values. In general, the resonant tank should be placed on the side of the transformer with the higher effective port voltage and consequently lower current, i.e. in boost-mode, where the low currents make it more difficult to guarantee CCM, which is why the number of possibly usable permutations in boost-mode must not be limited by the magnetizing current. In contrast, the restrictions imposed by this condition on the number of permutations in buck-mode are not particularly important, since the currents are generally larger and the CCM condition and (3.20) can therefore also be fulfilled more easily.

In addition to the conclusion that it is best to place the resonant tank on the secondary side of the transformer, **Fig. 3.20** also indicates that the

required minimum inductance decreases as the turns ratio increases, since a larger turns ratio places the unity gain at lower port voltages and therefore higher currents. As a result, CCM is easier to maintain. This might lead to the assumption that as high a turns ratio as possible should be used, which is not the case, since the choice of turns ratio has a large influence on the RMS current stresses of the components, as will be shown in the following section.

3.4.4.3 Selection of the Turns Ratio

In order to be able to estimate the influence of the turns ratio on the resulting conduction losses in the power components, a simplified analysis can be carried out based on the RMS current stresses in the transformer windings. Neglecting the RMS current increase due to the quantum operation, the average RMS current in the transformer can be defined as:

$$I_{\mathrm{rms}} = \sqrt{\frac{1}{2}\left(I_{\mathrm{r,p,rms}}^2 + I_{\mathrm{r,s,rms}}^2\right)}, \tag{3.21}$$

while the RMS current in buck-mode is mainly defined by the average output current I_{out}, according to

$$I_{\mathrm{r,s,rms}} = I_{\mathrm{out}} \cdot \frac{\pi}{2} \cdot \frac{1}{\sqrt{2}} = \frac{P_{\mathrm{out}}}{U_{\mathrm{out}}} \cdot \frac{\pi}{2} \cdot \frac{1}{\sqrt{2}}, \tag{3.22}$$

with the primary-side winding current calculated as:

$$I_{\mathrm{r,p,rms}} = \frac{I_{\mathrm{s,rms}}}{n}, \tag{3.23}$$

whereas in boost-mode, the RMS current is defined by the average input current I_{in}, according to

$$I_{\mathrm{r,p,rms}} = I_{\mathrm{in}} \cdot \frac{\pi}{2} \cdot \frac{1}{\sqrt{2}} = \frac{P_{\mathrm{in}}}{U_{\mathrm{in}}} \cdot \frac{\pi}{2} \cdot \frac{1}{\sqrt{2}}, \tag{3.24}$$

with

$$I_{\mathrm{r,s,rms}} = nI_{\mathrm{p,rms}}. \tag{3.25}$$

Due to the wide operating range of the converter, the different operating points can be weighted according to (3.1), whereby the average RMS current in the transformer can be found.

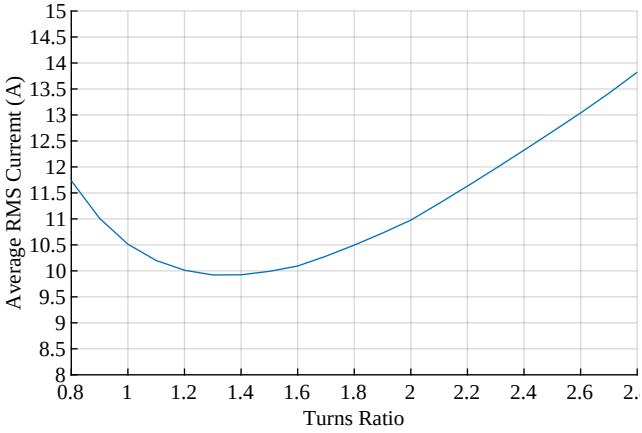


Fig. 3.21: The RMS current stress in the transformer of the QSRC for different turns ratios, whereby the RMS current is averaged over the entire operating range.

The results are plotted in **Fig. 3.21** for different turns ratios n. Two main insights can be gained from the two figures **Fig. 3.20** and **Fig. 3.21**. On the one hand, it is not sensible to select a turns ratio n below approximately 1.3, since both the average RMS current stresses in the transformer as well as the minimum required resonant inductance increase for $n < 1.3$. On the other hand, the optimal n will most probably be slightly higher than 1.3, e.g., in the range of 1.3...1.6, since although the RMS currents increase slightly, the minimum required resonant inductance continues to decrease. However, it is only possible to determine the optimal n if a complete optimization of the QSRC is performed. This is done in the next section and the corresponding results are analyzed.

3.4.4.4 Pareto Front

Similar to the DAB converter topology, an optimization was also carried out for the QSRC by using suitable loss models for a converter module according to the specifications of **Fig. 3.1**. As sweep parameters, the resonant frequency f_r of the resonant tank and the turns ratio n of the transformer are used with sweep limits as listed in **Tab. 3.4.** For the reasons mentioned previously, only discrete resonant inductors are considered in the optimization, which is why the sum of the box volume of the transformer and the inductor is used as

Tab. 3.4: Design Space Variables for the Optimization of the QSRC Converter Topology.

Parameter	Range
Transformer Turns Ratio n	1.0...2.0
Resonant Frequency f_r	200 kHz...450 kHz

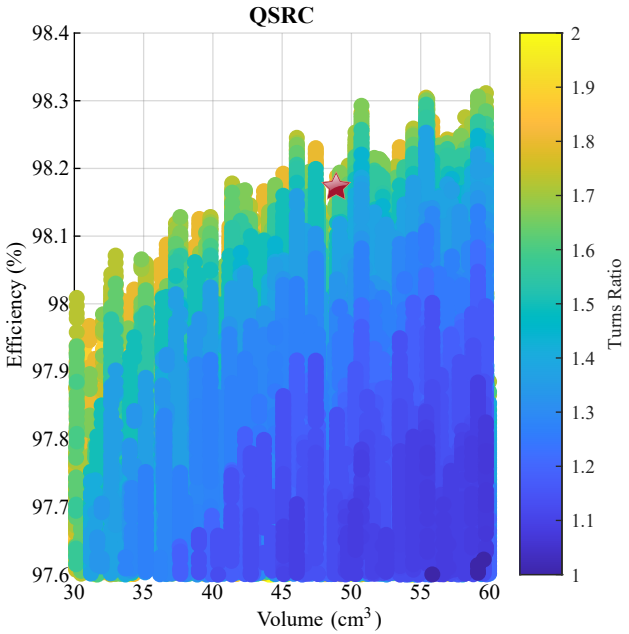


Fig. 3.22: Pareto optimization results of a 2.5 kW QSRC converter module, where the volume on the x-axis corresponds to the total magnetics volume and the color-coding of the different converter designs (dots) indicates the turns ratio of the transformer. The converter design, which has finally been implemented in hardware is marked with a red star.

an estimation of the overall size of the converter. The results are shown in **Fig. 3.22**, where each dot corresponds to a specific QSRC design and the color-coding is used for indicating the turns ratios of the transformers of the

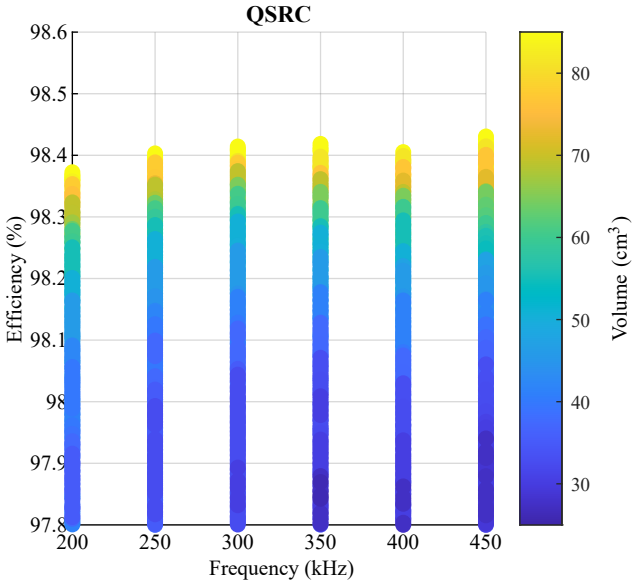


Fig. 3.23: Pareto front of the QSRC converter for different resonant frequencies, with the volume as the color code.

specific designs. Similar to the LLC and DAB converter, the x-axis in the Pareto optimization is the box volume of the magnetic components.

As expected, it turns out that the optimal turns ratio n is slightly higher than 1.3, approximately around 1.6. The finally selected converter design, which is used for hardware implementation, is marked with a red star. The respective parameters of the design are listed in **Tab. 3.5.** In order to see not only the influence of the turns ratio but also the influence of the resonance frequency on the Pareto-optimal designs, **Fig. 3.23** shows various designs with identical volumes but different resonance frequencies of the resonant tanks. It is evident, that it does not really matter which resonance frequency is used between 200 kHz and 450 kHz, since the efficiency changes only marginally. Accordingly, the resonance frequency can be selected based on other criteria, such as the required bandwidth of the measurement circuits, the size of possibly required EMI filters, and so on.

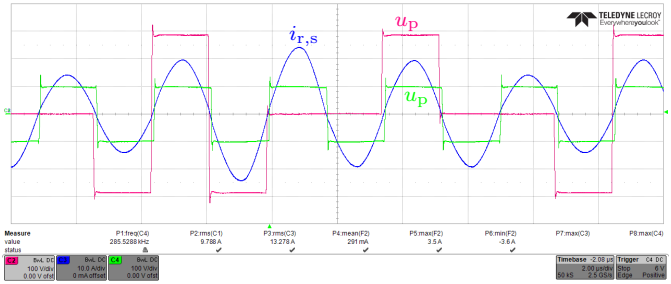
3.4.4.5 Bidirectionality of the QSRC

Since it is becoming increasingly important in today's EV chargers to be able to feed power back into the grid, it is a great advantage if the charger has a bidirectional power flow capability. This is the case with the QSRC because the topology, apart from the placement of the resonance tank, is symmetrical. In other words, the control remains the same, regardless of whether power is supplied to the output or drawn from it. This is also true for the DAB converter topology, but not for the LLC converter, which, however, is also capable of bidirectional power flow, even though the operation is not symmetrical [113].

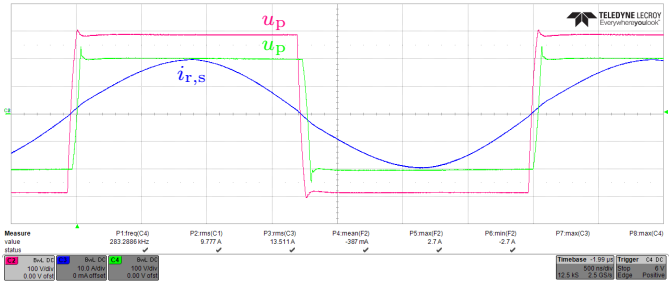
3.4.5 Experimental Measurements of the QSRC

The experimentally measured voltage and current waveforms under full-load operation are shown in **Fig. 3.24** and **Fig. 3.25** for an output voltage of 100 V (buck-mode), 200 V (SRC-mode, unity gain), 300 V (SRC-mode, unity gain) and 400 V (boost-mode). The voltage and current waveforms show that soft switching can be ensured at full power for all output voltages in all operating modes. Furthermore, the currents are almost perfectly sinusoidal, which is why conduction losses due to current harmonics can be avoided to a large extent.

In **Figs. 3.26(a)(b)**, the magnetizing currents (calculated based on the experimentally measured primary-side and secondary-side currents) for two different switching patterns in buck-mode, resulting in the same output power, are shown. Switching pattern 1 in **Fig. 3.26(a)** (cf.**Fig. 3.18(d)**) features the same peak value of the positive and the negative magnetizing current, as explained in **Sec. 3.4.3**, which leads to lower core losses compared to switching pattern 2 in **Fig. 3.26(b)** (cf.**Fig. 3.18(c)**), where the positive and negative magnetizing current values do not have the same amplitudes (the average value of the magnetizing current is forced to be zero by adding DC blocking capacitors in series with the transformer windings in the real system). However, the switching pattern 2 uses a voltage sequence with more uniformly distributed full-voltage and zero-voltage intervals, resulting in lower RMS currents and therefore lower conduction losses. Thus, switching pattern 1 has higher conduction losses but lower core losses than switching pattern 2. In the realized system, the differences between the two different switching patterns are very small (difference in efficiency$<$ 0.1%). In boost-mode, the magnetizing current is inherently triangular, since the resonant tank is placed on the secondary side of the transformer and the primary-side full-bridge is



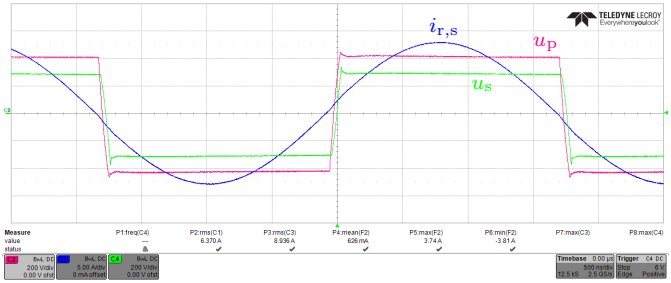
(a)



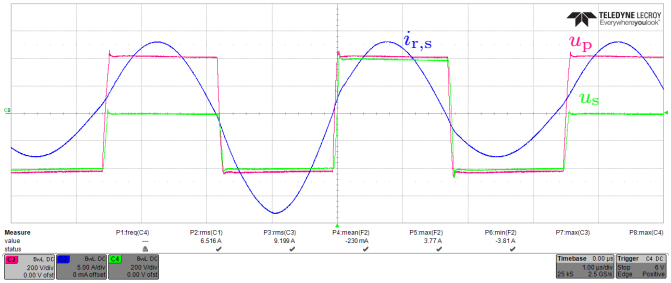
(b)

Fig. 3.24: Measured waveforms of the 2.5 kW QSRC hardware demonstrator for **(a)** $U_{out} = 100\,V$, $U_{in} = 280\,V$ and **(b)** $U_{out} = 200\,V$, $U_{in} = 280\,V$. The input voltage is selected to maximize the unity gain operating region and/or to decrease the step-up or step-down ratio.

operated with full-voltage intervals only (cf. **Fig. 3.26(c)**). Consequently, in this mode the switching pattern can be optimized for minimum RMS currents in the system without considering the magnetizing current. Compared to the magnetizing current shown in boost-mode, the ones in buck-mode have more fluctuations, which is due to the effect of the leakage inductance of the transformer. Even though it is very small (2 µH compared to the discrete resonant inductor of 18.4 µH), it still leads to a secondary-side voltage u_s not equal to u_p/n for the same reasons discussed in **Sec. 3.4.3** for the integrated leakage series inductor, which is affected by the capacitor voltage. The larger the current (e.g., in buck-mode, the current is larger than in boost-mode), the larger the capacitor voltage, the more effect on u_s, and the larger the fluctuations.



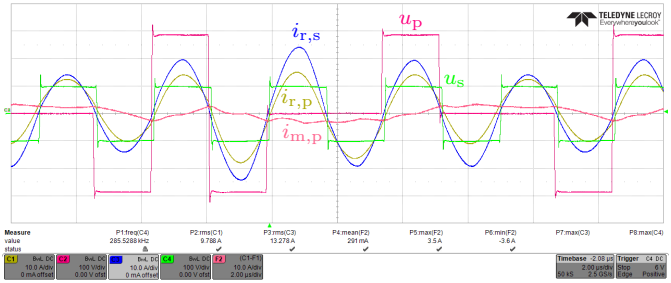
(a)



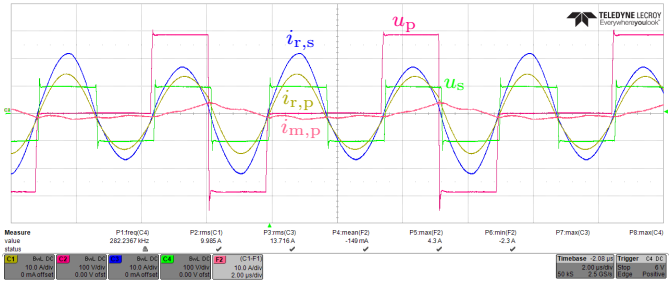
(b)

Fig. 3.25: Measured waveforms of the 2.5 kW QSRC hardware demonstrator for **(a)** $U_{out} = 300\,V$, $U_{in} = 400\,V$ and **(b)** $U_{out} = 400\,V$, $U_{in} = 400\,V$. The input voltage is selected to maximize the unity gain operating region and/or to decrease the step-up or step-down ratio.

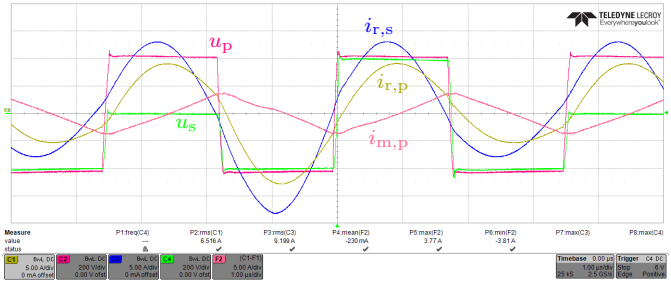
The measured efficiencies of the hardware demonstrator are shown in **Fig. 3.27** for output voltages from 100 V...400 V and for different power values, with the dots representing measurements and the solid lines representing calculations. It turned out that the measured conduction losses were much higher than the originally calculated conduction losses, primarily due to the much higher AC resistances of the windings of the magnetics. A 50 % higher AC resistance was measured in the transformer, while that of the inductor was 20 % higher. After careful investigation, it turned out that the employed litz wires had relatively poor twisting patterns, with the smallest bundle comprising 50 strands of 40 µm wire, whereby the primary-side winding comprises a total number of strands of 600 and the secondary-side winding of 800 strands. Consequently, 12 and 15 bundles are twisted together, which are comparably large numbers, and therefore it is difficult to ensure that identical flux linkages



(a)



(b)



(c)

Fig. 3.26: Calculated magnetizing currents $i_{m,p}$ by subtracting the measured primary-side and secondary-side winding currents $i_{r,p}$ and $i_{r,s}$ of the QSRC hardware demonstrator for two different switching patterns in buck-mode in **(a)** and **(b)**, and a third switching pattern in boost-mode in **(c)**.

are resulting for the individual bundles [114]. Compared to the litz wire of the transformer, the one of the inductor uses one more layer of twisting, i.e., in the first layer each bundle comprises 50 strands and in the second

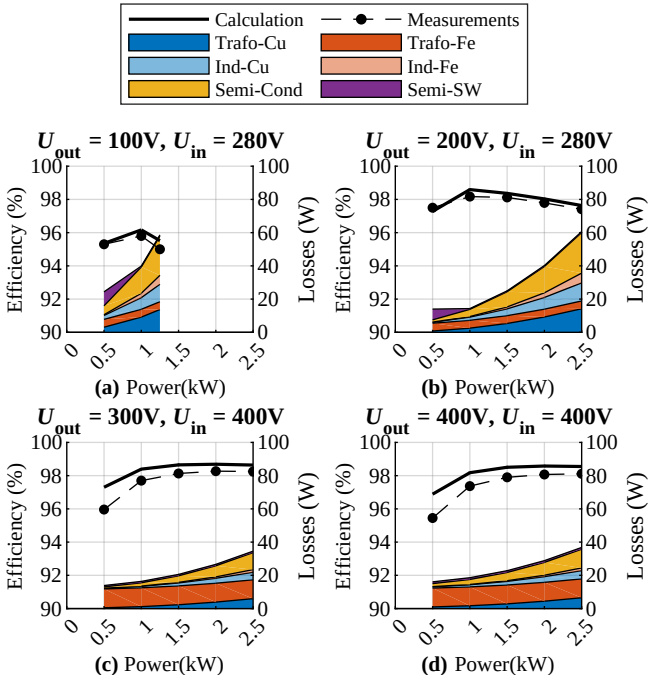


Fig. 3.27: Efficiency calculations and measurements of the QSRC hardware demonstrator for **(a)** $U_{\text{out}} = 100\,\text{V}$, $U_{\text{in}} = 280\,\text{V}$, **(b)** $U_{\text{out}} = 200\,\text{V}$, $U_{\text{in}} = 280\,\text{V}$, **(c)** $U_{\text{out}} = 300\,\text{V}$, $U_{\text{in}} = 400\,\text{V}$ and **(d)** $U_{\text{out}} = 400\,\text{V}$, $U_{\text{in}} = 400\,\text{V}$. The input voltages are again selected in such a way, that the converter is operated with unity gain if possible, or at least such that the step-up or step-down ratio is minimized. The black dots represent the measured efficiencies, while the solids lines correspond to the calculated efficiencies. Furthermore, the calculated loss breakdowns are shown for the different operating points.

layer each of the 6 bundles comprises 4 sub-bundles. This greatly reduces the proximity effect at the bundle level, which is why the conduction losses in the inductance are significantly lower than in the transformer. Nevertheless, the efficiency of the QSRC is already very high, although the efficiency could be increased even further with a better litz wire (which for the required strand diameter and the number of strands usually has long delivery times and high costs).

3.5 Comparative Evaluation: QSRC vs. DAB Converter vs. LLC Converter

After individually investigating the three isolated DC/DC converter topologies (LLC converter, DAB converter, QSRC) in detail, they are now directly compared to each other in this section based on various performance criteria. Starting with the theoretical properties of the topologies, such as the occurring RMS currents, the switching conditions of the semiconductors, and the complexity of the control, in a second step the topologies are compared using real hardware demonstrators such that the most suitable topology for the application can finally be identified.

3.5.1 Comparison of the Pareto Fronts and the Optimal Converter Designs

The Pareto fronts of the three topologies are summarized in **Fig. 3.28**, where it can clearly be seen that the theoretically achievable average efficiencies are very close together (differences of 0.2 % to 0.3 %).

Accordingly, with regard to the selection of optimal topology, the *theoretical* efficiency per power density is not the only important aspect. Other important factors that play a role in real converter implementations must also be taken into account, such as, e.g., the component stresses over the entire operating range, the required switching frequency range (since it has a significant impact on the EMI filter volume), the ease of guaranteeing ZVS condition for the semiconductors over the entire operating range (since it might influence the final achieved efficiencies), and so on. For this reason, four exemplary converter designs with equal total magnetics volumes of 47 cm^3 were selected (see converter designs marked in **Fig. 3.28**), which are compared in detail in the following. A design close to the Pareto front was chosen for the LLC converter and the QSRC, while two different systems were chosen for the DAB converter topology, with one of the designs close to the Pareto front being chosen with a turns ratio of 1.23 ($DABC_{option2}$, marked by a red circle in **Fig. 3.28**) and a second, less efficient one with a turns ratio of 1.6 ($DABC_{selected}$, marked by a red star in **Fig. 3.28**). The reasons for choosing these two different designs for the DAB converter will be explained later in more detail, but is related to providing ZVS conditions for the semiconductors. The detailed circuit parameters and efficiencies are listed in **Tab. 3.5,** whereby the resulting calculated component losses and efficiencies for different output voltages are shown in **Fig. 3.29** (η_{meas} are the efficiency calculations

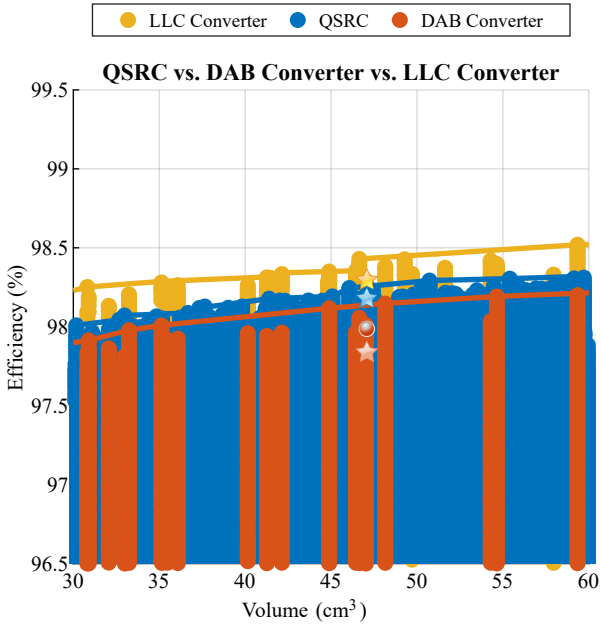


Fig. 3.28: Comparison of the Pareto fronts of QSRC, the DAB converter, and the LLC converter, where the designs marked by stars are finally considered for practical implementations in the application at hand.

using the adapted accurate loss models as already shown in **Fig. 3.27** and **Fig. 3.13**, while η_{cal} are the efficiency calculations using the initial/unadapted loss models, which are also employed in the Pareto optimizations). It needs to be mentioned, in **Fig. 3.28** and **Fig. 3.29**, only the initial/unadapted loss models are used for the three topologies, whereby, for example, the increased measured HF winding losses in the non-ideally manufactured litz wires, or the occurring residual switching losses in the DAB converter are not yet taken into account. This is mainly for the simple reason that it is only fair to compare the three topologies based on their ideally achievable efficiencies in a first step, without taking into account the degree of difficulty of the practical implementations.

The course of the RMS current stress over the output voltage (cf. **Fig. 3.29(a)**) mainly depends on how deep the converter operates in the

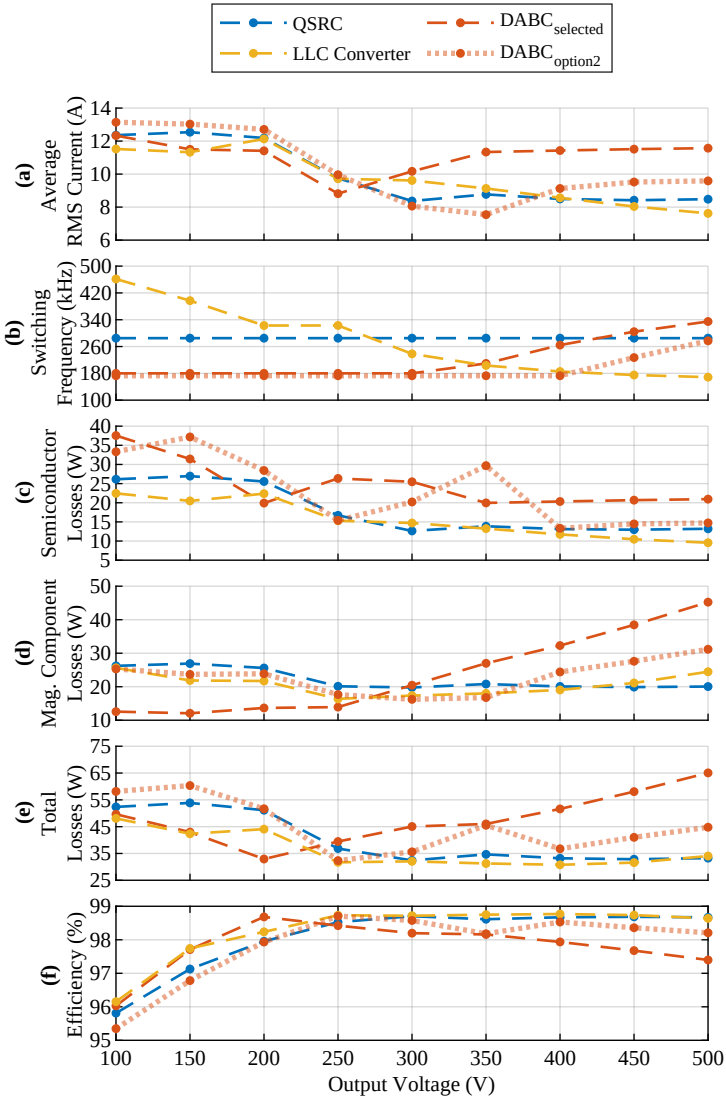


Fig. 3.29: Comparison of the selected 2.5 kW isolated DC/DC converter designs of **Fig. 3.28**, with regard to **(a)** average RMS current, **(b)** switching frequency, **(c)** semiconductor losses, **(d)** magnetic component losses, **(e)** total losses and **(f)** efficiencies for different output voltages at full load, using the calculated loss models.

Tab. 3.5: Circuit Parameters and Performances of the Selected 2.5 kW Isolated DC/DC Converter Designs of **Fig. 3.28**.

Parameter	**QSRC**	**DABC$_{\text{option2}}$**	**DABC$_{\text{selected}}$**	**LLC Converter**
Switches	IGOT60R042D1 (37 mΩ GaN)			
V_{mag}	47 cm^3			
Turns Ratio	15/11	16/13	16/10	20/12
Inductance	18.4 µH (sec)	11.5 µH (pri)	13 µH (pri)	17.5 µH (pri)
Core	E25/13/7 x3 (trafo) E32/16/9 x2 (inductor)	ELP43/10/28	ELP43/10/28	ELP43/10/28
Material	N87 (trafo) N49 (ind)	N97	N97	N97
Litz Wire	40 µm x 600 (Pri) 40 µm x 800 (Sec)	40 µm x 500 (Pri) 40 µm x 1000 (Sec)	40 µm x 1200 (Both)	40 µm x 600 (Pri) 40 µm x 1200 (Sec)
Air Gap	0.25 mm	none	none	0.6 mm
L_{m}	100 µH	300 µH	300 µH	110 µH
f_{sw}	285 kHz	170…270 kHz	180… 330 kHz	150…450 kHz
f_{r}	285 kHz	\	\	350 kHz
$\bar{\eta}_{\text{cal}}$	98.22%	97.85%	97.71%	98.31%
$\bar{\eta}_{\text{meas}}$	97.78%	\	97.17%	\
$\hat{\eta}_{\text{cal}}$	98.79%	98.71%	98.55%	98.79%
$\hat{\eta}_{\text{meas}}$	98.25%	\	97.6%	\

buck or boost region for all three topologies, which in turn is directly related to the choice of the turns ratio of the transformer. For the considered application, since in boost-mode there is higher voltage and less current, which usually means fewer losses, it is beneficial to operate more in boost

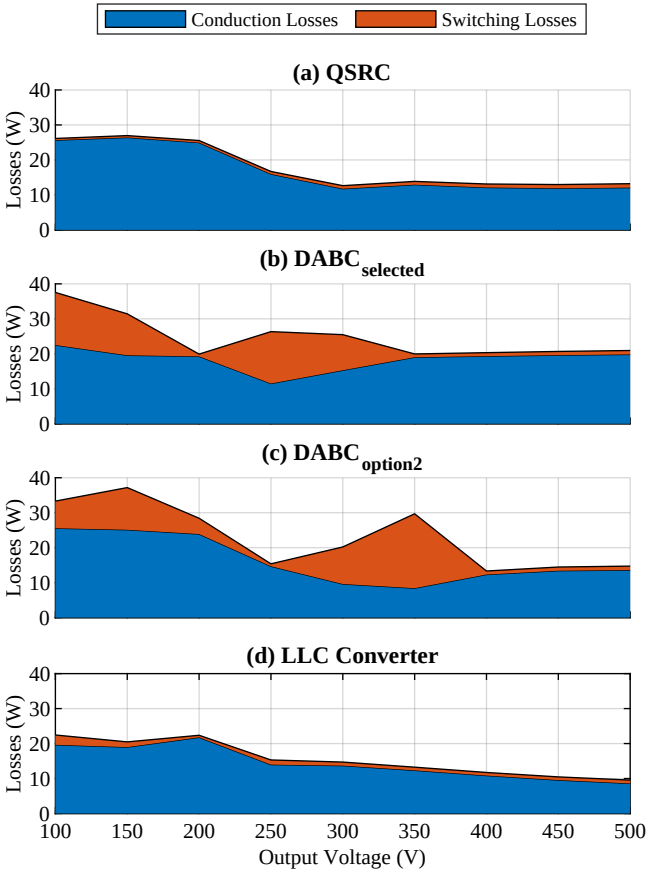


Fig. 3.30: Comparison with regard to semiconductor loss breakdown for the selected 2.5 kW isolated DC/DC converter designs of **Fig. 3.28**, **(a)** QSRC, **(b)** realized DAB converter, **(c)** second option of the DAB converter and **(c)** LLC converter for different output voltages at full load, using the calculated loss models.

region, i.e., to have a turns ratio larger than 1, which can be seen from the selected optimal designs for all three typologies (cf. **Tab. 3.5**). Accordingly, the characteristics of the RMS current stresses of the two DAB converter designs are very different and reach their minimum values at different output voltages. Even though the proportion of reactive power, and thus the RMS

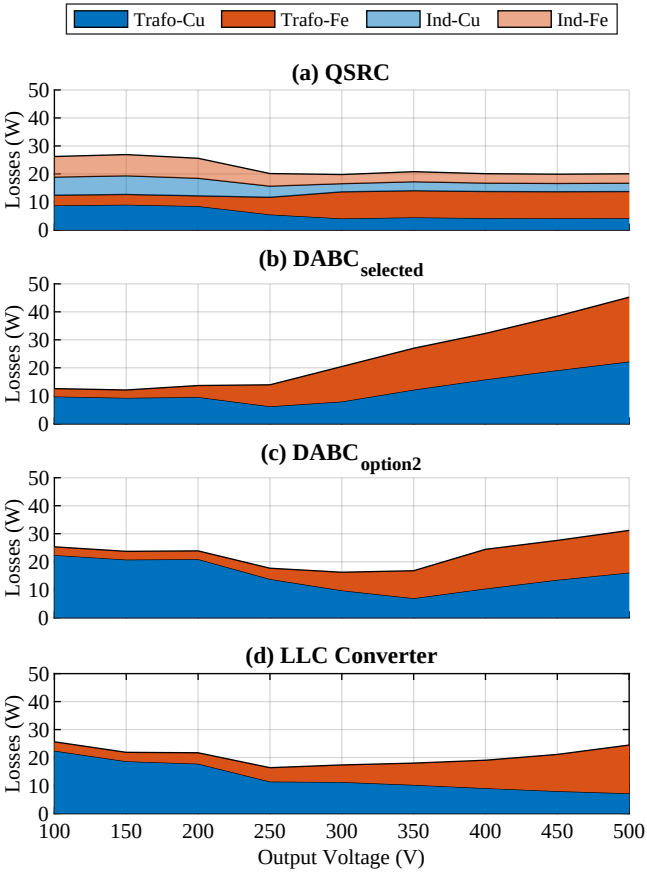


Fig. 3.31: Comparison with regard to magnetic component loss breakdown of the selected 2.5 kW isolated DC/DC converter designs of **Fig. 3.28**, **(a)** QSRC, **(b)** realized DAB converter, **(c)** second option of the DAB converter and **(c)** LLC converter for different output voltages at full load, using the calculated loss models.

current stresses, are lower in $\mathrm{DABC}_{\mathrm{option2}}$ than in $\mathrm{DABC}_{\mathrm{selected}}$, the higher proportion of reactive power has a positive effect on the switching losses in the converter, as will be explained in more detail later. Although the reactive power share also increases in the case of the resonant converter topologies, the further away they are operated from the unity gain voltage transfer, this

power share is, however, significantly smaller than in the DAB converter topology, which is why the conduction losses in these topologies are lower as well. For the LLC converter, due to high current and high switching frequency in buck-mode, the maximum losses occur for this mode of operation. While it is the same for the QSRC, the effect of the switching frequency is not present. Furthermore, the boost-mode of the LLC converter is also more efficient than for the QSRC, as its secondary side is not conducting current during part of the period. Therefore, the optimal turns raio of LLC converter (1.6...1.8, cf. **Fig. 3.4**) is higher than for the QSRC (1.4...1.6, cf. **Fig. 3.22**).

In terms of switching frequency, as shown in **Fig. 3.29(b)**, the QSRC topology is by far the best topology, since it can be operated with a constant switching frequency regardless of the port voltages and the output power. The DAB converter could theoretically also be operated with a constant switching frequency, but only at the expense of a more complex modulation and/or lower efficiency. The LLC converter inherently requires the widest switching frequency range, which makes it particularly difficult to design power-dense EMI filters for this topology.

Due to the ability of the resonant converter topologies to achieve soft switching for all semiconductors for all operating points at full load, there are almost no switching losses with these topologies, which is why only conduction losses occur in the semiconductors (cf. **Fig. 3.29(c)** and **Fig. 3.30**). Even though the switching losses are very small in both topologies, the residual soft-switching losses are slightly higher in the LLC converter than in the QSRC, since the switching currents in the LLC converter, especially in buck-mode, are significantly higher than in the QSRC. The switching losses are highest in the DAB converter, since with this topology ZVS cannot be guaranteed over the entire operating range with the proposed simplified modulation. Although more complex modulation schemes could possibly guarantee ZVS over the entire operating range, the ZVS switching losses can never be lower than in the QSRC, since the soft-switching currents are at least as high as those of the QSRC. Because of this and the generally higher RMS currents in the DAB converter, the semiconductor losses in the DAB converter are typically higher than for QSRC.

The total losses in the magnetic components are very similar in the two resonant converter topologies, as can be seen in **Fig. 3.29(d)** and **Fig. 3.31** where the detailed loss breakdown of the magnetic components for the three topologies is shown. Due to the wide output voltage range, it is not so easy to design the magnetic components according to the well-known design rules, e.g., for a single worst-case operating point, since the conduction losses dom-

inate for low voltages and high currents, while the core losses dominate for high voltages and low currents. Consequently, it is hardly possible to avoid a numerical optimization of the magnetic components, where the losses of various transformer designs for the nine operating points shown in **Fig. 3.29** are calculated and their average is used to calculate the respective Pareto front. Based on the loss distributions of the three converter designs that are on the Pareto front (cf. QSRC, $\text{DABC}_{\text{option2}}$ and LLC converter in **Fig. 3.31**), it can be seen that those optimal transformers have similar values for the maximum core losses and the maximum winding losses, at the highest and the lowest output voltage, respectively. One aspect to be noted here is that the optimization is based on perfectly twisted litz wire, which is why the HF conduction losses in the LLC converter are surprisingly low despite the operation with the highest switching frequency for the highest currents. Hence, higher HF conduction losses are likely to be present in real windings, depending on the quality of the litz wire, as seen from the measurements previously carried out for the QSRC transformer. The fourth design, $\text{DABC}_{\text{selected}}$, which is not exactly on the Pareto front, has an asymmetric loss curve, with the losses of the magnetic components increasing sharply towards higher output voltages, which is due to the increased RMS currents and the comparably high switching frequency. On the other hand, the design has by far the lowest losses for low output voltages.

Based on the total converter losses and the efficiencies over the entire operating range, it can finally be concluded that the QSRC topology has clear advantages over the LLC converter topology and the DAB converter topology. Compared to the LLC converter topology, the QSRC achieves similar performance in terms of efficiency but with a constant switching frequency, which makes it easier to design the magnetic components and the respective EMI filter. In reality, the LLC converter is likely to have higher conduction losses due to the high switching frequency for low output voltages. Compared to the DAB converter topology, the QSRC has a significantly higher efficiency, although the design and the control are significantly simpler. It is of course possible to increase the DAB converter efficiency by means of a more elaborate modulation, but it cannot reach the efficiency of the QSRC, due to the still slightly higher RMS current, the higher soft-switching currents (although ZVS can be guaranteed over the entire operating range), and the harmonic components in the currents. In the real implementations of the two DAB converter designs, higher switching losses than calculated in **Fig. 3.30** must also be expected, since the switching currents react very sensitively to all non-idealities such as parasitic resistances, parasitic capacitances, dead

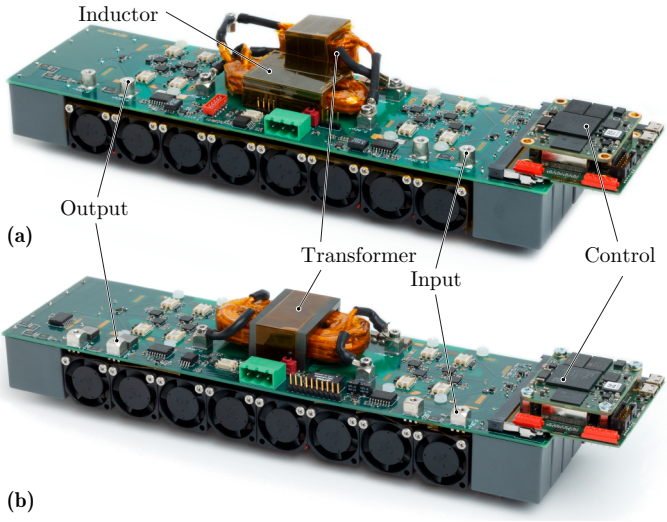


Fig. 3.32: Photos of the two 2.5 kW hardware demonstrators **(a)** using the QSRC approach, with a small transformer and an external series inductance and **(b)** implementing the DAB converter topology where the series inductance is integrated in the transformer as leakage inductance.

times, delays in the controller, measurement inaccuracies, and so on, as can be seen in **Sec. 3.3.3**. In order to minimize the switching losses, a complex control system would have to be implemented, which takes all these non-idealities into account and adapts the modulation accordingly, which is not really feasible in a practical converter system.

In the previous considerations, the maximum achievable efficiencies of the three converter topologies were calculated based on relatively ideal loss models of the components, which is why the conclusions drawn from these considerations are verified in the following for real systems using two hardware demonstrators based on the QSRC and the DAB converter topology.

3.5.2 Comparison of the Realized Hardware Systems

In order to allow for a direct, fair comparison between the three topologies, the hardware demonstrators were built with identical heat sinks, identical input and output capacitors, and identical switches. Accordingly, the converters are only differing concerning the magnetic components, which in turn have

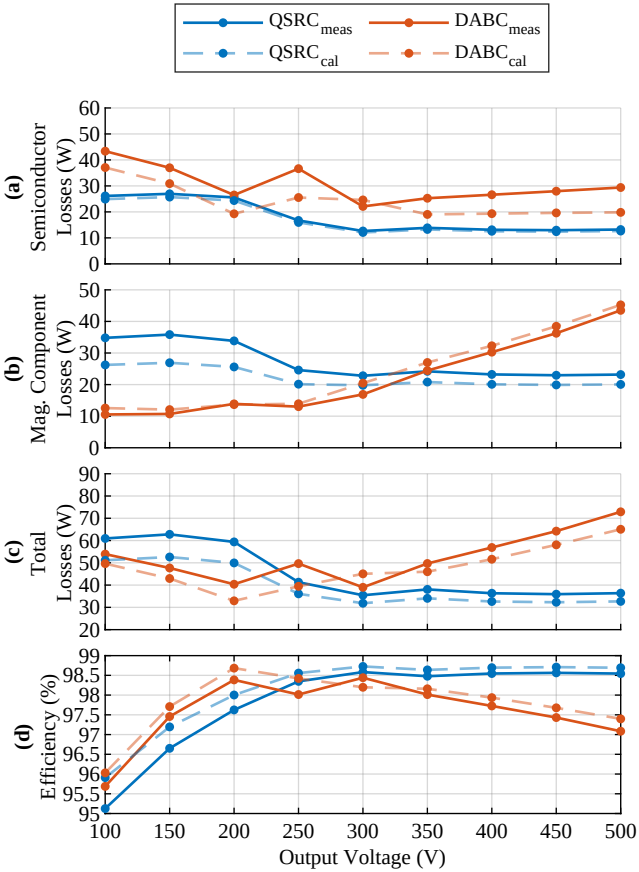


Fig. 3.33: Performance comparison of the realized systems of QSRC and the DAB converter, with regard to **(a)** semiconductor losses, **(b)** magnetic component losses, **(c)** total losses **(d)** efficiencies for different output voltages at full load, using the initial ideal loss models and the adapted accurate loss models.

identical total volumes, such that identical power densities are achieved. Since the LLC converter topology achieves similar performance as the QSRC, but has serious disadvantages compared to the QSRC, only the QSRC and the DAB converter topology were implemented as 2.5 kW isolated DC/DC hardware demonstrators, as shown in **Fig. 3.32**. The converters are designed according

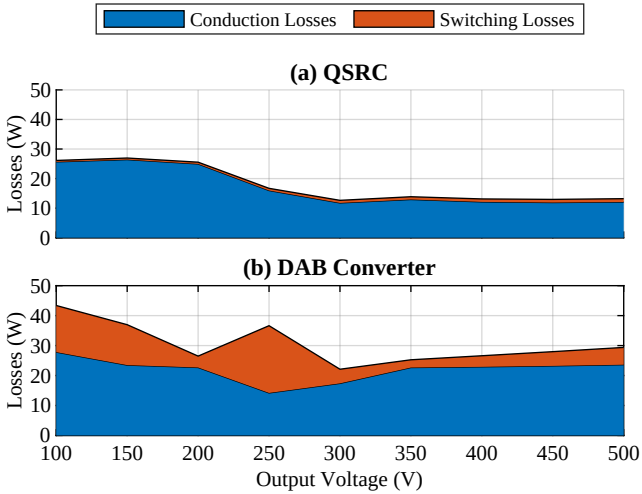


Fig. 3.34: Comparison with regard to semiconductor loss breakdown of the realized systems of the **(a)** QSRC and **(b)** the DAB converter for different output voltages at full-load operation, using the adapted accurate loss models.

to the parameters listed in **Tab. 3.5,** whereby it needs to be mentioned, that the DAB converter is implemented with a transformer with a turns ratio of 1.6, since the additional reactive power, especially in boost-mode, is required to reduce the occurring switching losses.

The measured efficiencies are in relatively good agreement with the calculated efficiencies, particularly under full-load operating conditions, as already shown in **Fig. 3.27** and **Fig. 3.13** for the QSRC and the DAB converter, respectively. Consequently, it can be concluded that the loss models are accurate enough to predict the main losses in the systems. **Fig. 3.33** shows the loss distributions calculated according to the initial ideal loss models (indicated by dashed lines) and the corrected loss models according to the measurements of the real components (indicated by solid lines), where, e.g., the increased HF resistance of the litz wire is considered, or a more detailed waveform generator is implemented.

In terms of semiconductor losses, the QSRC measurements are almost the same as the calculations, while for the DAB converter, the losses are higher due to higher switching losses, which can be seen from the loss breakdown shown

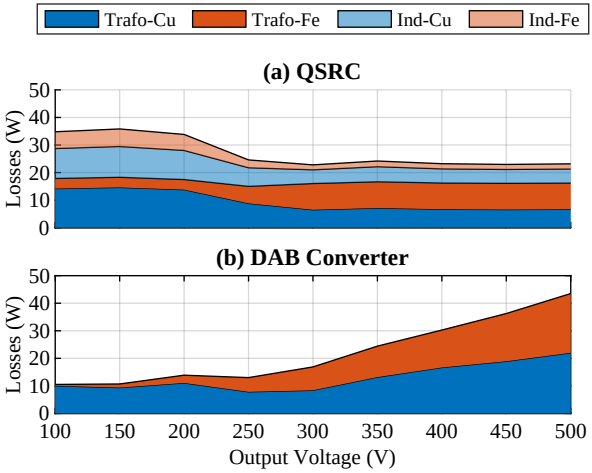


Fig. 3.35: Comparison with regard to magnetic component loss breakdown of the realized systems of **(a)** the QSRC and **(b)** the DAB converter for different output voltages at full-load operation, using the adapted accurate loss models.

in **Fig. 3.33(a)**. The increased switching losses are due to the non-idealities in the system, i.e., parasitics, deadtime, etc., as discussed in **Sec. 3.3.3**. The ratios between switching losses and conduction losses are shown in **Fig. 3.34**.

The losses of the magnetic components of the QSRC are slightly higher than expected, mainly due to the low quality of the employed 40 µm litz wire and the resulting increased HF resistance (cf. **Fig. 3.35**). In contrast, the total losses of the magnetics of the DAB converter are almost exactly as calculated, which is due to the fact that the employed litz wire (40 µm x 1200) by accident has better twisting patterns. Furthermore, core losses are also slightly reduced, since in the real system cores are made of more efficient N97 ferrite material and not N87 material as considered in the optimization.

Despite the changes made in the adapted loss models, the corresponding (more accurately) predicted efficiencies deviate only slightly from the ones with initial ideal loss models, which validates the conclusions drawn from the theoretical analyses.

Fig. 3.36 shows the comparison of the measured efficiencies of QSRC and DAB converter for different voltages and output power values. It can be seen

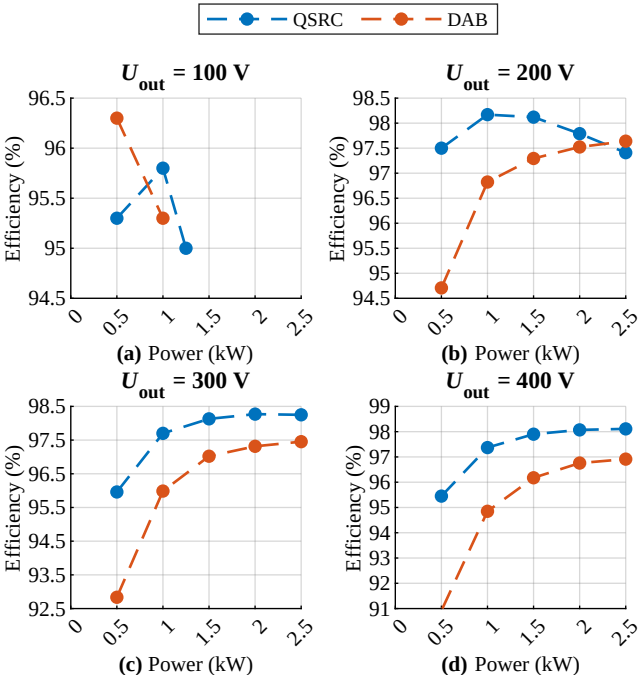


Fig. 3.36: Comparison of the measured efficiencies for the DAB converter and QSRC at **(a)** $U_{\text{out}} = 100\,\text{V}$, **(b)** $U_{\text{out}} = 200\,\text{V}$, **(c)** $U_{\text{out}} = 300\,\text{V}$, **(d)** $U_{\text{out}} = 400\,\text{V}$. The input voltage is selected to maximize the unity gain region and to decrease the step-up/down ratio.

that the QSRC shows better performance for most operating points, not only in full load, but also for partial power operation, due to the low circulating current/reactive power in the system, and also due to the lower switching losses. It needs to be mentioned, that the efficiencies of the DAB converter could be further improved using a significantly more complex modulation, but it will still not reach the efficiency of the QSRC. The efficiencies shown in **Fig. 3.36** can also be seen as achievable efficiencies with similar control efforts for both topologies.

Despite all the aforementioned advantages of QSRC, it does not mean that it is the better topology in all aspects. In terms of dynamics, for example, the DAB converter is much faster than QSRC and LLC converter due to its single energy storage component. For the QSRC, due to the concept of a

Tab. 3.6: Summary of the Comparison of QSRC vs. DAB vs. LLC Converter.

Dimension	QSRC	DAB	LLC
RMS Current	Moderate	High	Low
Switching Frequency Range	Constant	Moderate/Constant	Wide
Soft Switching	Easy	Difficult	Easy
Design and Operation Complexity	Low	High	Moderate
Efficiency Performance	Good	Moderate	Good
Bidirectionality	Yes	Yes	Yes
Dynamics	Moderate	High	Moderate

'macroscopic' duty cycle, it essentially needs more time (multiple resonant periods) to control the current and the voltage, which is why it cannot achieve the same control bandwidth as the DAB converter.

Table 3.6 summarizes the above comparison of the three typologies qualitatively based on different important performance criteria.

Although the QSRC is already significantly more efficient and easier to control than the DAB converter, the QSRC topology can be further improved by refining the discretized control variable using an additional bidirectional switch, which leads to a reduction in the RMS currents and thus the conduction losses. This adaptation of the QSRC topology and the resulting advantages are analyzed in more detail in the following.

3.6 Hybrid Quantum Series Resonant Converter

The only disadvantage of the conventional QSRC topology is that there are only two possible states for the controller to regulate the transferred power, as either full-voltage intervals or zero-voltage intervals can be applied to the transformer. As discussed in **Sec. 3.4**, this on the one hand inevitably leads to an increase in the RMS currents in the system due to the fluctuation in the amplitudes of the currents. On the other hand, it results in limited control resolution as discussed in **Sec. 3.4.2**. Hence, it would be advantageous to increase the number of possible states of the controller output so that the current ripple, i.e., the fluctuation of the current amplitudes during the half resonant intervals, can be reduced. This can be achieved by replacing one two-level bridge-leg on the primary with a three-level T-type bridge-leg, such

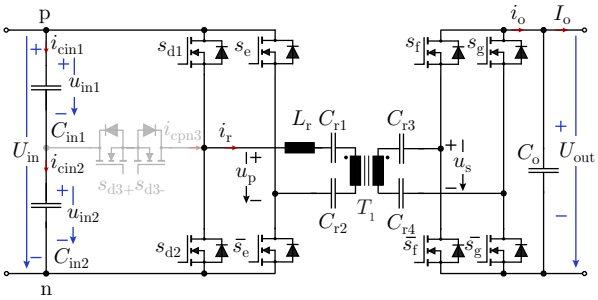


Fig. 3.37: Topology of a full-bridge series resonant DC/DC converter (SRC). A primary-side two-level bridge-leg is extended into a three-level T-type bridge-leg for improving the voltage control capability and lowering the stresses on the components. Accordingly, the DC/DC converter is denominated as H-QSRC.

that a hybrid (H) combination of a two-level and a three-level bridge-leg is employed, resulting in the topology of **Fig. 3.37**, which is referred to as the Hybrid Quantum Series Resonant Converter (H-QSRC). Compared with a traditional QSRC, two more voltage levels, $\pm\frac{1}{2}U_{in}$, can be utilized [115]. The resonant capacitor C_r is split among the primary side and secondary side of the transformer to prevent the magnetic core from saturation. It is also split among both terminals of the windings in order to reduce the common-mode voltage applied across the transformer. The detailed operating principle of the proposed H-QSRC topology is introduced in the following, where the different operating modes are explained.

3.6.1 Operating Principle of the H-QSRC

As already discussed for the three previously analyzed isolated DC/DC converter topologies, a series resonant converter (SRC) is operated at its resonant frequency, with an input-to-output voltage transfer ratio corresponding to the turns ratio of the transformer. However, due to the wide output voltage range required for EV chargers, it is not always possible to keep its input voltage U_{in} equal to the primary-side referred output voltage $n \cdot U_{out}$, which is why the H-QSRC considered in the case at hand needs to be operated in different modes for different output voltage levels. These modes will be introduced in the following, whereby for simplicity reasons, the turns ratio is assumed to be $n = 1 : 1$.

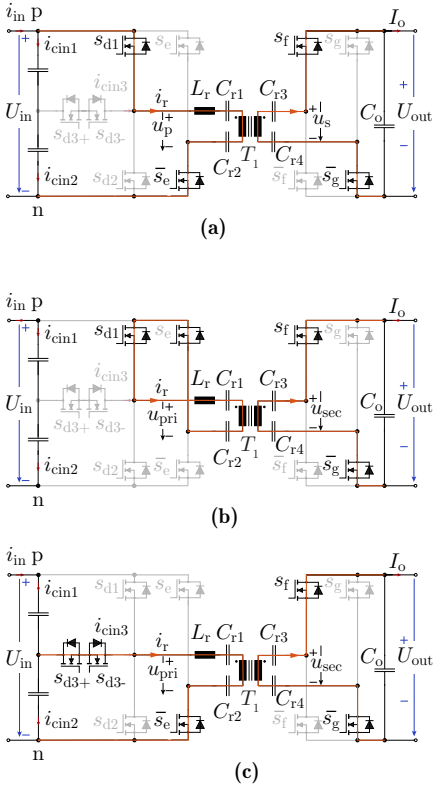


Fig. 3.38: Conduction states ($i_r > 0$) of the H-QSRC topology in buck-mode for **(a)** a full-voltage interval, **(b)** a zero-voltage interval, and **(c)** a half-voltage interval.

3.6.2 Buck-Mode

In buck-mode, the primary-side referred output voltage $n \cdot U_{out}$ is lower than the input voltage U_{in}, which is why there is a continuous power flow to the output and the secondary-side full-bridge is operated as a synchronous rectifier as in the case of the conventional QSRC. Consequently, the power flow is controlled by means of either applying full-voltage intervals (U_{in}) on the primary side of the transformer to increase the output power (cf. **Fig. 3.38(a)**), or zero-voltage intervals are applied by shorting the primary-side switch nodes (cf. **Fig. 3.38(b)**), whereby the output power is reduced. In contrast to the conventional QSRC, however, a third voltage level is available

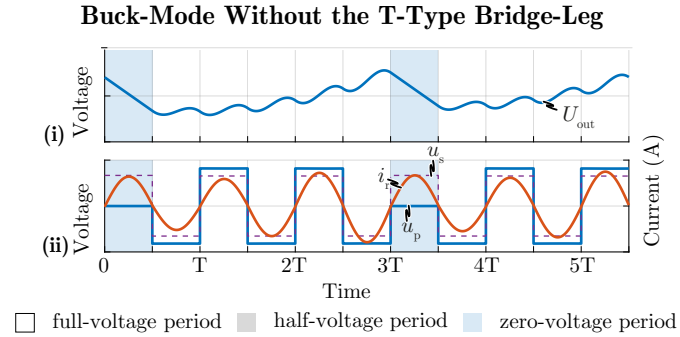


Fig. 3.39: Simulation waveforms of the H-QSRC topology without the T-type bridge-leg for: **(i)** Output voltage U_{out}, **(ii)** primary-side switch-node voltage u_p, secondary-side switch-node voltage u_s and resonant current i_r.

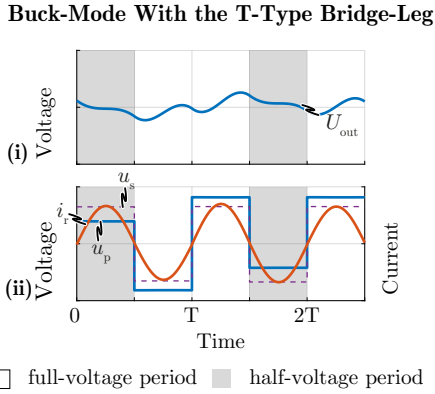


Fig. 3.40: Simulation waveforms of the H-QSRC topology with the T-type bridge-leg for: **(i)** Output voltage U_{out}, **(ii)** primary-side switch-node voltage u_p, secondary-side switch-node voltage u_s and resonant current i_r.

in the H-QSRC, as by means of the bidirectional switch, also only half of the input voltage can be applied to the primary side of the transformer, which is referred to as half-voltage interval or half-voltage period in the following (cf. **Fig. 3.38(c)**). The additional voltage level has the great advantage that both the output voltage can be controlled more precisely and the RMS currents

can be reduced, since the number of half periods in a macroscopic period can be reduced, as is explained in more detail below based on an example. In order to compare the H-QSRC with the conventional QSRC, the characteristic voltage and current waveforms in the two converter topologies are plotted in **Fig. 3.39** and **Fig. 3.40** for the same exemplary operating point, where the input voltage is only slightly higher than the primary-side referred output voltage. In **Fig. 3.39**, the waveforms for the conventional QSRC in buck-mode are shown for a macroscopic period of six half resonant intervals, where only full-voltage intervals and zero-voltage intervals are used for controlling the output voltage, resulting in low-frequency ripples of the output voltage and higher RMS current. The relatively long duration of the macroscopic period is due to the fact that during the full-voltage intervals, there is only a small voltage difference between the primary-side voltage u_p and the primary-side referred secondary-side voltage $n \cdot u_\mathrm{s}$, which means that the amplitude of the resonant current increases only slowly, but during the zero-voltage intervals there is a very large voltage difference, and in consequence the amplitude of the resonant current drops sharply. In order to prevent this, it would be necessary to apply a voltage to the primary side during the zero-voltage intervals which is smaller than $n \cdot U_\mathrm{out}$ but does not deviate too much from this value, so that the current amplitude does not drop as sharply. This can be achieved in the H-QSRC by means of the T-type bridge-leg, since for this operating point, instead of zero-voltage intervals, half-voltage intervals are used (cf. **Fig. 3.40**). Consequently, the amplitudes of the net voltage applied across the resonant tank no longer differ so much during the full-voltage and half-voltage intervals, which is why the length of the macroscopic period can be reduced to three half resonant intervals. Thus, a more accurate output voltage control can be achieved and the RMS value of the transformer current can be reduced. Nevertheless, the control bandwidth is not improved by the additional voltage level, as this only depends on the maximum possible applicable voltage across the resonant tank, which is not influenced by the T-type bridge-leg. It therefore highly depends on the application whether it is worth installing the additional components of the T-type bridge-leg of the H-QSRC, or whether the cheaper option, the conventional QSRC, with its coarser controller resolution is sufficient.

3.6.3 Boost-Mode and SRC-Mode

In boost-mode, the primary-side referred output voltage is higher than the input voltage, and therefore the primary side must be driven with full-voltage

intervals, whereas the secondary side takes over the control of the output voltage by sequentially applying full-voltage and zero-voltage intervals. Since in this mode only full-voltage intervals are generated with the primary-side semiconductors, the bidirectional switch of the T-type bridge-leg is not required, which is why the boost-mode of the H-QSRC does not differ from that of the conventional QSRC. The same applies to the SRC-mode.

3.6.4 Buck-Boost-Mode

As discussed previously, for small differences between the input and output voltage, the macroscopic cycle becomes relatively long, and sometimes even comprises tens of half periods, leading to a poor dynamic performance in these operating points. Adding another voltage level as introduced in **Sec. 3.6.2** mitigates this issue but does not solve the problem completely. It can be tackled by using an alternative buck-boost-mode – where the current is increased by short-circuiting the secondary side instead of using full-voltage periods ($u_\mathrm{p} = \pm U_\mathrm{in} \,\&\, u_\mathrm{s} = 0$ to increase the current, $u_\mathrm{p} = 0 \,\&\, u_\mathrm{s} = U_\mathrm{out}$ to decrease the current). However, just like in a non-isolated buck-boost converter, this leads to relatively high component stresses, e.g., nearly 100% resonant RMS current increase is expected if a voltage transfer ratio close to $1:1$ is required, since the power is only transferred during half of the time. By using the extra voltage level of the T-type bridge-leg, this value can be reduced to 50%, if the half-voltage periods are used to decrease the current ($u_\mathrm{p} = \pm U_\mathrm{in} \,\&\, u_\mathrm{s} = 0$ to increase the current, $u_\mathrm{p} = \pm\frac{1}{2}U_\mathrm{in} \,\&\, u_\mathrm{s} = \pm U_\mathrm{out}$ to decrease the current), and can be further reduced if more voltage levels are available. Even though 50% higher RMS currents might seem significant, it does not necessarily mean the thermal limit of the converter has to be increased. For example, since the operating range where the buck-boost-mode is needed is rather small (near unity gain), this operating mode can be shifted towards regions with generally low RMS currents by suitably selecting the turns ratio of the transformer. For a turns ratio equal to 1, since $U_\mathrm{in,min}$ =280 V, the buck-boost-mode utilized here leads to an RMS current of 14.8 A (50% higher than the RMS current of 9.7 A in pure buck-mode), which is only around 6% higher than the overall maximum RMS current, e.g., at 200 V, which is similar to the increase brought by the quantum operation.

For the specifications of the intended application as an EV charger, it turned out that the RMS currents in the conventional QSRC are already relatively low, which is why the potential small efficiency gains that can be

achieved by using the H-QSRC topology are not justifying the additional hardware effort.

3.7 Summary

In this chapter, different isolated DC/DC converter topology candidates are discussed for the realization of the second stage in the considered EV charger system with a wide output voltage range. First of all, the widely used LLC and DAB converter topologies are investigated, and are found to have significant disadvantages, making them not really suitable for the application at hand. For the LLC converter, despite being very efficient, the required frequency change is extremely wide, which makes the design of an EMI filter very challenging. To narrow the frequency range, frequency modulation has to be combined with other modulation techniques, making the analysis more complex. Additionally, the design of the LLC converter requires complex time-domain analyses to accurately predict component stresses and gain characteristics due to the large deviation of the switching frequency from the resonant frequency. For the DAB converter, the modulation to achieve full soft switching of all the semiconductors and low RMS currents in the system is complicated and has to be coupled with accurate loss modeling of the components, making it difficult to design an efficient converter with a reasonable effort. Furthermore, the switching currents/losses usually react very sensitively to non-idealities in the circuit, which either has to be considered in the modeling process, or compensation has to be made during the commissioning such that the system is behaving as expected. The advantage is that it has very high dynamics and can react extremely fast if required, which on the other hand, is also a double-edged sword, as the DAB converter is susceptible to over-currents and the corresponding protection circuitry has to be faster than in other topologies. In order to overcome the aforementioned disadvantages, the novel Quantum Series Resonant Converter (QSRC) is investigated, which is straightforward to understand, design, and operate. Using the cascaded hysteresis control structure, a good trade-off between the control resolution and dynamics can be achieved. With the appropriate voltage patterns, soft switching can be achieved for all semiconductors. Last but not least, by keeping the system in continuous conduction mode, the RMS current can be maintained at a rather low level. Following these design guidelines, a very efficient operation can be guaranteed. The comparison of the different topologies is validated by means of detailed Pareto optimizations and subsequent experimental measurements using 2.5 kW hardware demon-

strators, where the aforementioned arguments drawn from the theoretical analyses are validated. Finally, to further improve the performance of the QSRC, the H-QSRC is proposed as an extended version of the QSRC topology, which is characterized by two additional available voltage levels, resulting in a reduction of the occurring RMS currents and improved control accuracy.

4

Optimal Synergetic Operation and Performance Evaluation of the Two-Stage EV Charger System

Chapter Abstract

Having analyzed the PFC rectifier stage and the subsequent DC/DC stage separately in the previous two chapters, different combinations of the operating modes of the PFC rectifier stage and the DC/DC stage and their corresponding performances are evaluated in this chapter, starting with the theoretical analysis of the simultaneous operation of the two-level front-end and the H-QSRC DC/DC converter. The best synergetic combination of the operating modes of both stages is identified for the different output voltage regions. The corresponding control structure, which achieves smooth transitions between all operating regimes is presented, and it is shown, that the extremely wide output voltage range can be covered without having to overdimension any of the two converter stages. In the second step, to experimentally verify the 1/3-PWM operation, the 10 kW hardware demonstrator is realized with a Vienna Rectifier front-end, due to its superior performance compared to two-level PFC rectifier topologies, followed by four DAB DC/DC converter modules due to their fast control dynamics. First of all, simple but accurate loss models are presented for both stages separately, which are used in the next step to determine the optimal operating modes for both stages over the entire operating range, resulting in the most efficient operation of the overall converter system. It is found that the wide output voltage range can be covered efficiently without over-stressing any of the two stages in any operating point. This is then finally verified by means of experimental measurements of the complete system, where latest-technology GaN HEMTs are employed and operated at 560 kHz, such that a power density at 9 kW/dm^3 (about 150 W/in^3), not including the coldplate-type heatsink, is reached.

4.1 Introduction

After investigating the two stages of the EV charger separately, in the final step, it is vital to analyze how they can be operated together and how much we can benefit from the synergetic control of the two stages. First of all, the simultaneous operation of the boost-type two-level PFC rectifier front-end and the subsequent novel Hybrid Quantum Series Resonant DC/DC Converter (H-QSRC) output stage is discussed. The PFC rectifier stage is either operated in conventional boost-mode with two out of three phases switching (2/3-PWM), or in 1/3-PWM, while the H-QSRC is operated in either buck-mode, SRC-mode, or boost-mode. **Sec. 4.2** investigates the suitability and performance of possible combinations of the different operating modes of the H-QSRC and the PFC rectifier stage. The resulting control options are then compared concerning component stresses. The optimal combination of the operating modes for both stages is determined for various output voltage ranges, and it is shown, that by using the identified optimal control scheme the extremely wide operating range of an EV charger can be covered without having to overdimension any of the two stages. Finally, the complete control structure of the optimal scheme is presented in **Sec. 4.2.5**, and the implementation of the synergetic control of the two stages is explained in detail.

Subsequently, a 10 kW two-stage EV charger demonstrator system is realized, utilizing the most suitable topologies for both stages, i.e., the Vienna Rectifier (VR) is used as the PFC rectifier front-end due to its much better efficiency performance and low breakdown voltage requirements for the switches compared to the two-level PFC rectifier, and the subsequent DC/DC stage is realized with four identical DAB converter modules, due to their fast dynamic response, which is important for 1/3-PWM operation. As a detailed overview of the considered system is needed for the discussions in later parts of the work (whose focus, after all, is not on the hardware design but on the different operating modes of a given hardware), we choose the somewhat unorthodox approach of first introducing some details of the realized 10 kW two-stage hardware demonstrator in **Sec. 4.3.1**. Then, based on straightforward but sufficiently accurate loss models (confirmed by experiments) for the GaN-based VR introduced in **Sec. 4.3.2** and for the DAB DC/DC converter modules in **Sec. 4.3.3**, we provide a comprehensive performance evaluation of the two-stage system in **Sec. 4.3.4**. For each operating point, the analysis quantifies the achievable system-level efficiency improvement (if any) for a change of the operating strategy from the baseline 3/3-PWM to 1/3-PWM.

Then, **Sec. 4.3.5** discusses control implementation details of the two-stage system and provides experimental verification for typical operating points, including also a brief discussion of the EMI performance, which confirms that a change of the operating strategy from 3/3-PWM to 1/3-PWM has no significant impact on the EMI filter design.

In the end, the findings of this chapter are summarized in **Sec.. 4.4**.

4.2 Optimal Synergetic Operation of a Two-Stage EV Charging System Employing a Two-Level PFC Rectifier Front-End and H-QSRC DC/DC Stage

As mentioned in the beginning of this chapter, the three modes of operation (buck, SRC, boost) of the H-QSRC offer various possibilities for a synergetic control of the PFC rectifier stage and the subsequent H-QSRC. In this section, different two-stage control strategies are investigated in detail and their benefits and drawbacks are discussed. By modifying the turns ratio n of the transformer, the maximum primary-side referred output voltage $U_{\mathrm{o}}^{'}$ can be adjusted. Consequently, depending on n, the required operating modes are different. In this section, four possible synergetic control options are investigated and comprehensively evaluated, such that the most appropriate one can finally be selected for a certain application.

4.2.1 Pure Buck Operation

The most simple solution would be to operate the PFC rectifier stage with 1/3-PWM only and the DC/DC stage in buck-mode across the whole operating range. This could be achieved by limiting the maximum $U_{\mathrm{o}}^{'}$ to be smaller than the minimum value of the positive envelope of the grid line-to-line voltages. Hence, considering a certain margin, the turns ratio would have to be selected as $n = 4 : 9 = 0.44$, such that $U_{\mathrm{o,max}}^{'} = 440\,\mathrm{V}$ (considering $U_{\mathrm{o}} = 1000\,\mathrm{V}$). In this mode, the large voltage and current stresses are shifted to the components of the DC/DC stage while only one bridge-leg of the PFC rectifier stage is switching at a time, resulting in a very efficient operation of the rectifier front-end. The resulting main component stresses for the H-QSRC are plotted in **Fig. 4.2**, whereby the dashed line refers to a constant power of 10 kW. For output power values P_{out} lower than 3 kW, the rectifier

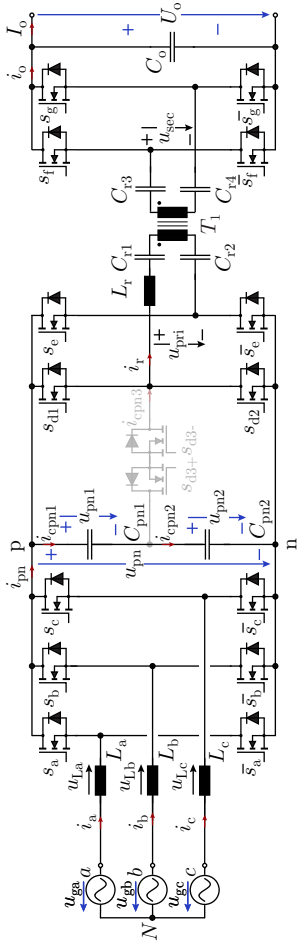


Fig. 4.1: Topology of the two-stage power circuit of the EV charger module comprising a PFC rectifier front-end and a full-bridge series resonant DC/DC converter (SRC) output stage. The SRC is always working at the resonant frequency and left uncontrolled or operating in buck or boost quantum (Q) mode. Furthermore, an extension of a primary-side two-level bridge-leg into a three-level T-type bridge-leg is considered for improving the voltage control capability and lowering the stresses on the components. Accordingly, the DC/DC stage is denominated as H-QSRC. Finally considered component values and operating parameters according to **Fig. 4.4**.

Fig. 4.2: Stresses of the H-QSRC for **(i)** Pure Buck Operation, **(ii)** Synergetic Operation 1, **(iii)** Synergetic Operation 2, **(iv)** finally selected Synergetic Operation 3: **(a)** peak resonant current, **(b)** RMS resonant current, **(c)** peak resonant voltage (total).

stage is not anymore operated with 1/3-PWM and u_{pn} is increased to 600 V, as a certain minimum reactive power is required to maintain the six-pulse course of u_{pn}, which is not available for $P_{\mathrm{out}} < 3\,\mathrm{kW}$. It should be noted that the component stresses are very high for this control strategy [$i_{\mathrm{r,peak,max}} = 110\,\mathrm{A}$, $i_{\mathrm{r,rms,max}} = 60\,\mathrm{A}$, $U_{\mathrm{Cr,peak}} = 4.9\,\mathrm{kV}$ (total voltage across all the resonant capacitors $C_{\mathrm{r1,2,3,4}}$)], especially for low $U_{\mathrm{o}}^{'}$. Due to the small turns ratio, the transformer is stepping up the voltage for all operating points, which is why the step-down ratio of the DC/DC converter system is further increased and the efficiency is therefore reduced.

4.2.2 Synergetic Operation 1

To decrease the current and voltage stresses of the resonant tank, the turns ratio can be increased whereby the 2/3-PWM of the PFC rectifier stage needs to be included, such that the DC-link voltage can be boosted. If the breakdown voltage of the switches in the rectifier stage and the primary side of the H-QSRC is 1200 V, which is a standard voltage level for commercially available SiC power MOSFETs, the maximum allowed DC-link voltage u_{pn} is limited to 850 V. Similarly, for the H-QSRC to work in buck-mode, a certain margin between u_{pn} and $U_{\mathrm{o}}^{'}$ needs to be kept (for example $u_{\mathrm{diff}} = 50\,\mathrm{V}$), such that the voltage applied to the resonant tank is large enough to regulate i_{r} with comparably high dynamics. Therefore, the maximum primary-side referred output voltage $U_{\mathrm{o,max}}^{'}$ is limited to around 800 V. Consequently, the turns ratio can be increased to $n = 0.75$. Thus, as long as $U_{\mathrm{o,max}}^{'}$ is lower than $u_{\mathrm{ll,max}} - u_{\mathrm{diff}}$, the rectifier stage is again operated with 1/3-PWM (cf. **Sec. 4.2.1**). However, once $U_{\mathrm{o,max}}^{'}$ exceeds $u_{\mathrm{ll,max}} - u_{\mathrm{diff}}$, the PFC rectifier has to start boost-mode with 2/3-PWM to keep u_{pn} above $U_{\mathrm{o,max}}^{'}$. The H-QSRC still operates in buck-mode across the whole operating range and SRC-mode is not yet employed. Compared to pure buck operation, the peak value of the resonant current is decreased by 32% ($i_{\mathrm{r,peak,max}} = 75\,\mathrm{A}$), the RMS current decreased by 38% ($i_{\mathrm{r,rms,max}} = 37\,\mathrm{A}$), and the peak resonant capacitor voltage decreased by 33% ($U_{\mathrm{Cr,peak}} = 3.3\,\mathrm{kV}$).

4.2.3 Synergetic Operation 2

An improvement of Synergetic Operation 1 can be achieved by adding SRC-mode of the H-QSRC. To use conventional 1200 V SiC devices in the PFC rectifier front-end, u_{pn} is again limited to 850 V. Since SRC-mode is added, $U_{\mathrm{o,max}}^{'}$ can be increased to the same level as u_{pn}, and therefore the turns ratio

can be chosen as 0.83. The transition between buck-mode and SRC-mode will be discussed in detail in **Sec. 4.2.5**. Similarly, depending on $U_{\mathrm{o,max}}^{'}$ and $u_{\mathrm{ll,max}}$, the PFC rectifier changes between 1/3 and 2/3-PWM, while the H-QSRC stage switches between buck-mode and SRC-mode in the same way, i.e., 1/3-PWM of the rectifier stage is combined with buck-mode of the H-QSRC, and 2/3-PWM of the PFC rectifier is used with SRC-mode of the H-QSRC. Compared to Synergetic Operation 1 (cf. **Sec. 4.2.2**), the resonant inductor peak current is further decreased by 9% ($i_{\mathrm{r,peak,max}} = 68\,\mathrm{A}$), the RMS current is decreased by 8% ($i_{\mathrm{r,rms,max}} = 34\,\mathrm{A}$), and the peak resonant capacitor voltage is decreased by 9% ($U_{\mathrm{Cr,peak}} = 3\,\mathrm{kV}$).

4.2.4 Synergetic Operation 3

Finally, by also utilizing boost-mode of the H-QSRC, the turns ratio can be set as $1:1$. The upper limit of the PFC rectifier output voltage is again set to 850 V, which is why for output voltages above 850 V the H-QSRC stage switches from SRC-mode to boost-mode, and starts to step up the voltage. The choice of the optimal boundary between SRC-mode and boost-mode (850 V for now) may be changed in a practical application and is subject to a system optimization. Compared to Synergetic Operation 2 (cf. **Sec. 4.2.3**), the resonant inductor peak current is decreased by 16% ($i_{\mathrm{r,peak,max}} = 57\,\mathrm{A}$), the RMS current is decreased by 18% ($i_{\mathrm{r,rms,max}} = 28\,\mathrm{A}$), and the peak resonant capacitor voltage is decreased by 17% ($U_{\mathrm{Cr,peak}} = 2.5\,\mathrm{kV}$). It can be noted that the stresses in the boost-mode region are slightly higher than for Synergetic Operation 2 (for example, at $U_{\mathrm{o}} = 1000\,\mathrm{V}$, $P_{\mathrm{out}} = 10\,\mathrm{kW}$, $i_{\mathrm{r,rms}}$ is increased from 13.3 A to 14.3 A). However, the stresses in the other regions are lower and the average efficiency over the whole operating range is still higher.

An output voltage sweep from 200 V to 1000 V was simulated for the above described control concept (Synergetic Operation 3) and the key transition waveforms are shown in **Fig. 4.4**. It should be noted that it is possible to design a suitable control structure which guarantees smooth transitions between the different modes of operation. Such a control structure is introduced and discussed in detail in the next section.

4.2.5 Control Structure of Synergetic Operation 3

A multi-cascaded control structure implementing the aforementioned Synergetic Operation 3 is shown in **Fig. 4.3**. For the PFC rectifier stage, the output voltage U_{o} is measured and used to calculate the output power reference P_{o}^{*}, which is then translated to the references $i_{\mathrm{a,b,c}}^{*}$ of the phase currents. The grid

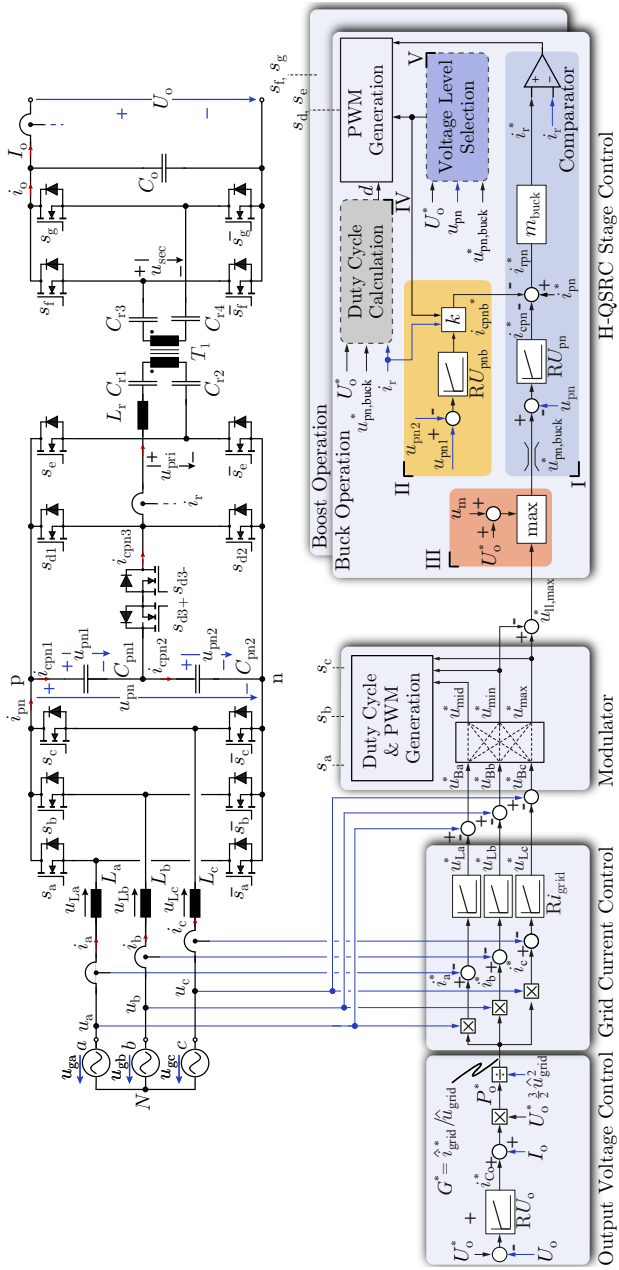


Fig. 4.3: Cascaded output voltage control structure of the two-stage EV charger power module comprising a three-phase PFC rectifier front-end and a DC/DC Hybrid Quantum Series Resonant Converter (H-QSRC) output stage, where measurement values are displayed in blue.

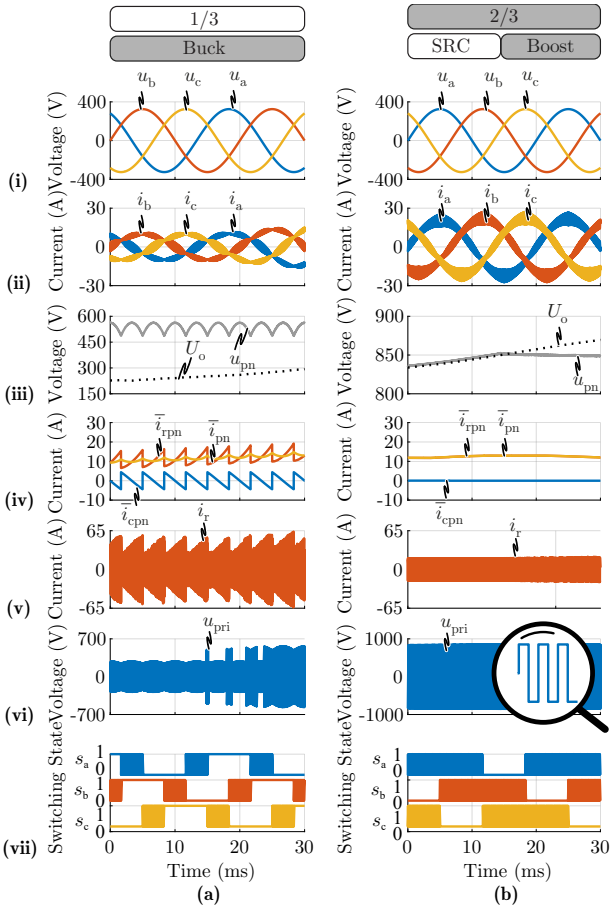


Fig. 4.4: Simulation waveforms of the two-stage EV charger power module (cf. **Fig. 4.1(b)**) employing Synergetic Operation 3 (cf. **Sec. 4.2.5**) for **(a)** U_o = 210 V - 300 V, **(b)** U_o = 830 V - 870 V: **(i)** grid voltages $u_{a,b,c}$, **(ii)** PFC rectifier inductor currents $i_{a,b,c}$, **(iii)** DC-link voltage u_{pn}, output voltage U_o, **(iv)** average PFC rectifier stage output current $\bar{i}_{pn}$, average DC-link current $\bar{i}_{cpn}$, and average input current $\bar{i}_{rpn}$ of the resonant converter over a switching period ($\bar{i}_{rpn} = \bar{i}_{pn} - \bar{i}_{cpn}$), **(v)** resonant current i_r, **(vi)** primary-side switch-node voltage u_{pri}, **(vii)** gate signals of the three bridge-legs $S_{a,b,c}$ of the PFC rectifier stage. The main simulation parameters are: switching frequency of the PFC rectifier stage and the H-QSRC: 140 kHz, $L_{a,b,c}$ = 100 µH, $C_{pn1} = C_{pn2} = 100\,\mu F = 2C_{pn}$, L_r = 50 µH, $C_{r1} = C_{r2} = C_{r3} = C_{r4} = 4C_r$ = 104 nF (with C_r representing the total capacitance) and C_o= 3 mF (to emulate the behaviour of batteries).

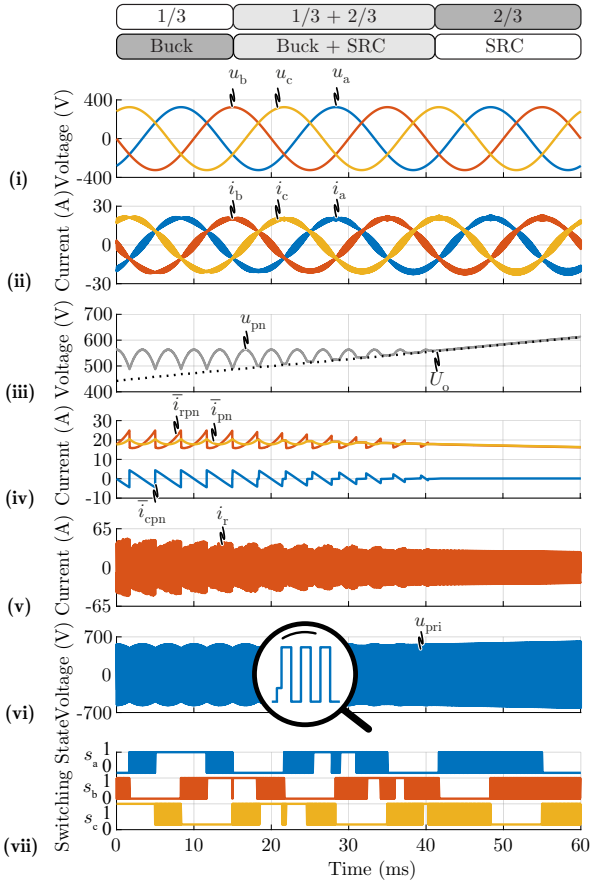


Fig. 4.5: Simulation waveforms of the two-stage EV charger power module (cf. **Fig. 4.1(b)**) employing Synergetic Operation 3 (cf. **Sec. 4.2.5**) for U_o = 440 V - 610 V: **(i)** grid voltages $u_{a,b,c}$, **(ii)** PFC rectifier inductor currents $i_{a,b,c}$, **(iii)** DC-link voltage u_{pn}, output voltage U_o, **(iv)** average PFC rectifier stage output current $\bar{i}_{pn}$, average DC-link current $\bar{i}_{cpn}$, and average input current $\bar{i}_{rpn}$ of the resonant converter over a switching period ($\bar{i}_{rpn} = \bar{i}_{pn} - \bar{i}_{cpn}$), **(v)** resonant current i_r, **(vi)** primary-side switch-node voltage u_{pri}, **(vii)** gate signals of the three bridge-legs $S_{a,b,c}$ of the PFC rectifier stage. The main simulation parameters are: switching frequency of the PFC rectifier stage and the H-QSRC: 140 kHz, $L_{a,b,c}$ = 100 µH, $C_{pn1} = C_{pn2}$ = 100 µF = $2C_{pn}$, L_r = 50 µH, $C_{r1} = C_{r2} = C_{r3} = C_{r4} = 4C_r$ = 104 nF (with C_r representing the total capacitance) and C_o= 3 mF (to emulate the behaviour of batteries).

current controllers Ri_{grid} then set the reference values of the voltages across the inductors $L_{\mathrm{a,b,c}}$, which are added to the measured mains phase voltages to create the references of the PFC rectifier switching stage input voltages (u^*_{Ba}, u^*_{Bb} and u^*_{Bc}). Based on these references, the gate signals of the half-bridges of the PFC rectifier are generated, and the required clamping of phases is performed [26, 33].

For the H-QSRC stage, two controllers are working in parallel: the buck controller generating the gate signals for the primary side ($s_{\mathrm{d,e}}$), and the boost controller generating the gate signals for the secondary side ($s_{\mathrm{f,g}}$). These two controllers have very similar structures, which is why in a first step only the buck controller is investigated in detail in the following sections.

4.2.5.1 Hysteresis Controller (Block I in Fig. 4.3)

The DC-link voltage u_{pn} of the two-stage system is always controlled by the H-QSRC stage, whose reference $u^*_{\mathrm{pn,buck}}$ is calculated using the output voltage U_{o} and $u^*_{\mathrm{ll,max}}$, where the latter is the instantaneous maximum line-to-line input voltage reference, defined as $u^*_{\mathrm{ll,max}} = u^*_{\mathrm{max}} - u^*_{\mathrm{min}}$. Furthermore, an additional term u_{m} is added to the output voltage reference U^*_{o}, whose purpose and magnitude will be discussed in **Sec. 4.2.5.3**. In the next step, $u^*_{\mathrm{pn,buck}}$ is compared with the measured value u_{pn} to calculate the current reference i^*_{cpn}, which is then subtracted from i^*_{pn}, a feed-forward term representing the output current of the PFC rectifier, and can be calculated from the PFC rectifier inductor currents and the corresponding duty cycles ($i^*_{\mathrm{pn}} = i^*_{\mathrm{a}} d_{\mathrm{a}} + i^*_{\mathrm{b}} d_{\mathrm{b}} + i^*_{\mathrm{c}} d_{\mathrm{c}}$). Furthermore, a second term i^*_{cpnb} is subtracted from i^*_{pn}, which is used to ensure balanced voltages across the two DC-link capacitors $C_{\mathrm{pn1}}, C_{\mathrm{pn2}}$, which will be explained in detail in **Sec. 4.2.5.2**. Finally, with $i^*_{\mathrm{rpn}} = i^*_{\mathrm{pn}} - i^*_{\mathrm{cpnb}} - i^*_{\mathrm{cpn}}$, the input current reference i^*_{rpn} of the H-QSRC stage is found. To calculate the resonant current reference i^*_{r} in buck-mode, i^*_{rpn} is multiplied by $m_{\mathrm{buck}} = u^*_{\mathrm{pn,buck}}/U^*_{\mathrm{o}}$, which is the same as the relationship between the input current and the inductor current in a conventional buck converter. Subsequently, i^*_{r} is compared to the measured resonant current $|i_{\mathrm{r}}|$ [111, 112], which is sampled once every half period (peak current is sampled and multiplied by $2/\pi$ to calculate the average current). Based on this comparison, it can then be determined whether the resonant current should be decreased or increased, which, in combination with the results of the voltage level selection block and the duty cycle calculation block, is used to generate the PWM signals.

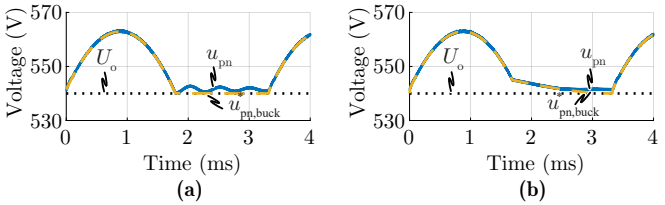


Fig. 4.6: Simulation waveforms of the DC-link voltage u_{pn}, its reference $u^*_{\mathrm{pn,buck}}$ and the output voltage U_{o} when the H-QSRC transitions between buck-mode and SRC-mode for $U_{\mathrm{o}} = 540\,\mathrm{V}$ **(a)** without the transition voltage u_{m} and **(b)** with the transition voltage u_{m}.

4.2.5.2 Control of the Midpoint Voltage (Block II in Fig. 4.3)

As mentioned previously, the balance between the voltages across C_{pn1} and C_{pn2} needs to be maintained for the proper operation of the converter. Therefore, a PI controller $\mathrm{R}U_{\mathrm{pnb}}$ is added, where the difference of u_{pn1} and u_{pn2} is used as the error signal. The output of this PI controller is then multiplied with an index k ($k = 1$ or -1) to obtain i^*_{cpnb}, whose sign depends on the selected voltage levels and the sign of the resonant current. For example, if $u_{\mathrm{pn1}} > u_{\mathrm{pn2}}$, the half-voltage intervals should be used more often for $i_{\mathrm{r}} < 0$ and less often for $i_{\mathrm{r}} > 0$ in order to discharge C_{pn1} (during half resonant periods, C_{pn1} is only discharged for $i_{\mathrm{r}} < 0$, and C_{pn2} is only discharged for $i_{\mathrm{r}} > 0$). Therefore, if full-voltage intervals and half-voltage intervals are used, i^*_{cpnb} should be positive ($k = 1$) for $i_{\mathrm{r}} < 0$ and negative ($k = -1$) for $i_{\mathrm{r}} > 0$, such that i^*_{r} is decreased for $i_{\mathrm{r}} < 0$ and increased for $i_{\mathrm{r}} > 0$, leading to more half resonant periods used for $i_{\mathrm{r}} < 0$ and less used for $i_{\mathrm{r}} > 0$ to discharge C_{pn1}. The situation is exactly the opposite if half-voltage intervals and zero-voltage intervals are used and is therefore not explained further.

4.2.5.3 Intermediate DC-Link Voltage Reference (Block III in Fig. 4.3)

Ideally, the voltage reference $u^*_{\mathrm{pn,buck}}$ should be selected from the maximum of two values, the output voltage U_{o} and $u^*_{\mathrm{ll,max}}$, as it is done in [26, 33]. However, due to the limited dynamic response of the resonant converter, the transition from buck-mode to SRC-mode cannot be achieved instantaneously. When the rectifier is operated with 1/3-PWM, the average input current $\bar{i}_{\mathrm{rpn}}$ of the H-QSRC is different from the average rectifier output current $\bar{i}_{\mathrm{pn}}$, due to the average capacitor current $\bar{i}_{\mathrm{cpn}}$. However, as soon as the H-QSRC enters

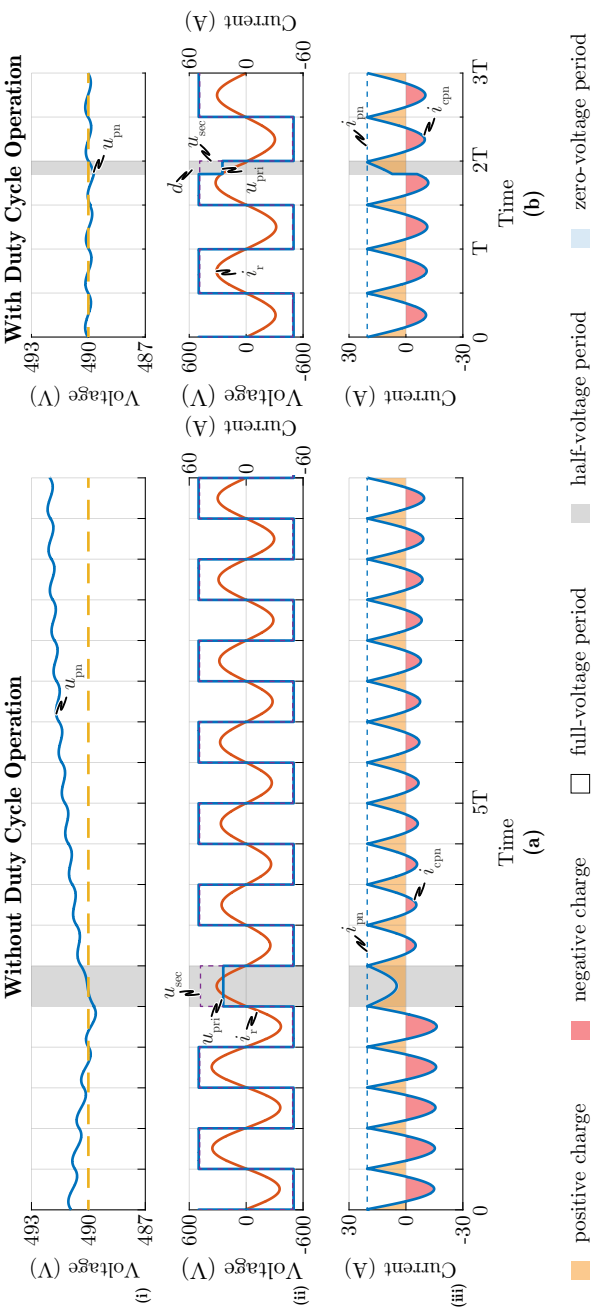


Fig. 4.7: Simulation waveforms of the H-QSRC in buck-mode for $u^*_{\mathrm{pn,buck}} = 490$ V and $U_\mathrm{o} = 480$ V **(a)** without duty cycle operation and **(b)** with duty cycle operation: **(i)** DC-link voltage u_pn, its reference $u^*_{\mathrm{pn,buck}}$, **(ii)** primary-side switch-node voltage u_pri, secondary-side switch-node voltage u_sec, resonant current i_r, **(iii)** rectifier output current i_pn, net current flowing into the DC-link i_cpn.

SRC-mode, its input current $\bar{i}_{\mathrm{rpn}}$ should be adapted to the rectifier output current $\bar{i}_{\mathrm{pn}}$, as in SRC-mode the H-QSRC is operated in open-loop and does not control $\bar{i}_{\mathrm{pn}}$ anymore. However, in H-QSRCs, it is difficult to adjust the resonant current fast and accurately during a short time interval, especially if a relatively large resonant inductor is employed. This is relevant, as even a small deviation from the steady-state can cause oscillations as shown in **Fig. 4.6(a)**. Therefore, to achieve a smooth transition as shown in **Fig. 4.6(b)**, a voltage u_{m} is added to U_{o}^{*}, which gradually decreases to zero with a much lower rate, e.g., a quarter of a sinusoidal wave, with a small amplitude, e.g., 5 V, and a low frequency, e.g., 150 Hz, such that the resonant current is adjusted step by step until $\bar{i}_{\mathrm{rpn}} = \bar{i}_{\mathrm{pn}}$.

4.2.5.4 Duty Cycle Operation (Block IV in Fig. 4.3)

For a conventional QSRC, large voltage ripples would appear in u_{pn}, especially when the input and output voltages are close, as the differences between the absolute voltage-time areas applied to the resonant tank during half-voltage intervals and full-voltage intervals are very large. In this condition, the 'net' voltage applied to the resonant tank during full-voltage intervals is nearly zero, while in half-voltage intervals, it is close to half of the DC-link voltage, as shown in **Fig. 4.7(a)**. Consequently, the decrease rate of i_{r} during the half-voltage periods is much larger than the increase rate during the following full-voltage intervals. As a result, it takes a comparably long time (tens of half periods) to bring the current back to its reference value. Consequently, a low-frequency ripple appears across u_{pn} with a large amplitude, leading to distortions in the three-phase PFC rectifier input currents. This problem can be mitigated by introducing duty cycle operation, as shown in **Fig. 4.7(b)**, where only a fraction of a full half-voltage interval is used. By introducing duty cycle operation, the effective voltage-time area applied to the resonant tank during one half-voltage interval is much smaller, enabling a much smoother regulation of u_{pn}.

To ensure soft switching for every switching transition in duty cycle operation, the appropriate voltage level sequence has to be selected. For example, if power and half-voltage intervals are used, the higher voltage level always needs to be applied first, such that the direction of i_{r} during the intermediate transition from u_{pn} to $\frac{1}{2}u_{\mathrm{pn}}$ inherently results in soft switching (cf. **Fig. 4.7(b)**). Nevertheless, for a certain duty cycle, i_{r} is not anymore precisely in phase with u_{pri}, which means it may reach zero before the end of the half period, leading to hard-switching transitions. There are two solutions to achieve soft switching under this circumstance: 1. increasing the switching

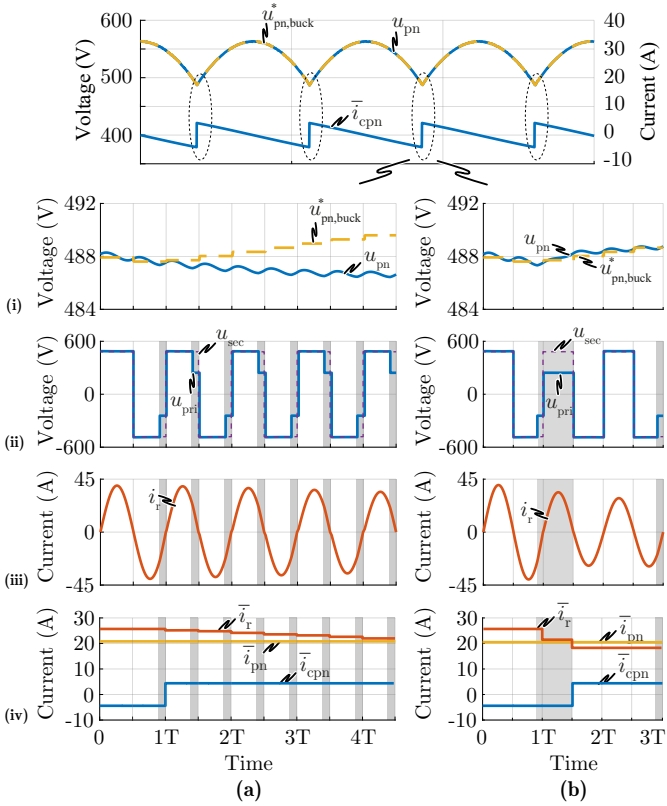


Fig. 4.8: Simulation waveforms of the H-QSRC in buck-mode when $u^*_{pn,buck}$ reaches the lowest point of its six-pulse course and $U_o = 480$ V **(a)** without d_{ic} and **(b)** with d_{ic}: **(i)** DC-link voltage u_{pn}, its reference $u^*_{pn,buck}$, **(ii)** primary-side switch-node voltage u_{pri}, secondary-side switch-node voltage u_{sec}, **(iii)** resonant current i_r, **(iv)** average rectifier output current $\bar{i}_{pn}$, average DC-link current $\bar{i}_{cpn}$, and average resonant current $\bar{i}_r$ over a switching period ($\bar{i}_r = \frac{u_{pn}}{U_o}\bar{i}_{rpn} = \frac{u_{pn}}{U_o}(\bar{i}_{pn} - \bar{i}_{cpn})$).

frequency (slightly increasing the switching frequency does not affect the output voltage), 2. using the magnetizing current of the transformer, which, however, is not considered further here. Having ensured soft switching in duty cycle operation, the calculation of the appropriate duty cycle needs to be investigated. Ideally, it can be derived considering the voltage-time area balance, i.e., zero net voltage applied to the resonant tank during a control

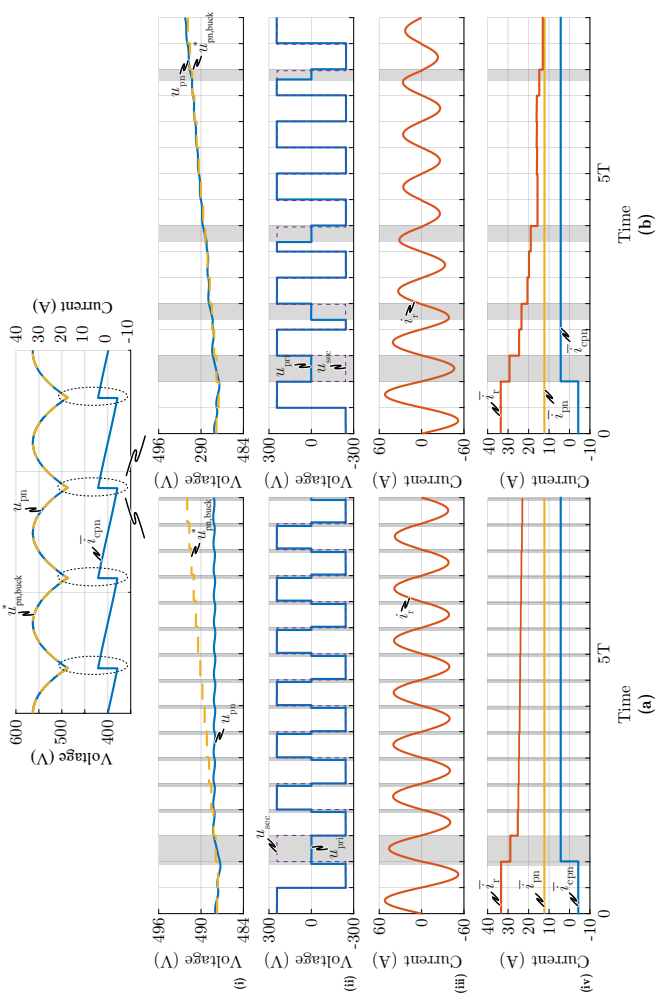


Fig. 4.9: Simulation waveforms of the H-QSRC in buck-mode when $u^*_{\mathrm{pn,buck}}$ reaches the lowest point of its six-pulse course and $U_\mathrm{o} = 240\,\mathrm{V}$, with larger requirement of $\Delta|\bar{i}_\mathrm{r}|_\mathrm{max}$ **(a)** without adjusted d_ic and **(b)** with adjusted d_ic: **(i)** DC-link voltage u_pn and its reference $u^*_{\mathrm{pn,buck}}$; **(ii)** primary-side switch-node voltage u_pri, secondary-side switch-node voltage u_sec, **(iii)** resonant current i_r, **(iv)** average rectifier output current $\bar{i}_\mathrm{pn}$, average DC-link current $\bar{i}_\mathrm{cpn}$, and average resonant current $\bar{i}_\mathrm{r}$ over a switching period ($\bar{i}_\mathrm{r} = \frac{u_\mathrm{pn}}{U_\mathrm{o}}\bar{i}_\mathrm{rpn} = \frac{u_\mathrm{pn}}{U_\mathrm{o}}(\bar{i}_\mathrm{pn} - \bar{i}_\mathrm{cpn})$.

period. A control period is defined as the time interval where the average of u_{pn} is equal to the reference. Considering again the case depicted in **Fig. 4.7(a)** with the same u_{pn} and U_{o}, and assuming a control period containing n half periods, the duration d of the half-voltage interval can be derived as

$$d = d_{\mathrm{vb}} = 2(n+1) \cdot \frac{u_{\mathrm{pn}} - U_{\mathrm{o}}}{u_{\mathrm{pn}}}. \tag{4.1}$$

However, as the current is not in phase with the voltage due to the applied duty cycle, the secondary-side applied voltage u_{sec} is not anymore in phase with u_{pri}, leading to different voltage-time areas which are applied to the resonant tank. For the considered component values of the resonant tank, the H-QSRC operates in continuous conduction mode, as the voltage across the resonant capacitor C_{r} is larger than U_{o} when i_{r} reaches zero. Thus, even if all four switches of the secondary-side full-bridge are turned off, the large capacitor voltage forces a continuation of i_{r} through the anti-parallel diodes of the switches. To compensate for this voltage-time area discrepancy, another term is added to d_{vb}, where d_{off} represents the time interval where the current is flowing into the opposite direction:

$$d = d_{\mathrm{vb}}^{'} = d_{\mathrm{vb}} + 4 \cdot \frac{d_{\mathrm{off}} U_{\mathrm{o}}}{u_{\mathrm{pn}}}; \tag{4.2}$$

d_{off} is a function of d_{vb} and can be calculated with the differential equations of the inductor current and the capacitor voltage. As (4.2) does not have an explicit solution, the duty cycle $d_{\mathrm{vb}}^{'}$ needs to be calculated numerically. Furthermore, it should be noted that (4.2) needs to be modified accordingly if the impedance of the resonant tank is decreased to a certain extent, when the system enters discontinuous conduction mode.

It can be noted from (4.1) that, the closer u_{pn} and U_{o} get, the smaller the duty cycle is, which, however, leads to limited dynamic performance of the system. In buck-mode, u_{pn} follows the six-pulse course, where between each pulse, the capacitor current needs to be changed instantaneously (cf. **Fig. 4.4(a.iv),(b.iv)**), requiring the H-QSRC to react accordingly. Therefore, another term d_{ic} is added to the duty cycle calculation, which varies depending on the required capacitor current:

$$d = d_{\mathrm{vb}}^{'} + d_{\mathrm{ic}}. \tag{4.3}$$

Fig. 4.8 shows the comparison of different duty cycles applied, without and with d_{ic} in the calculations respectively, when $U_{\mathrm{o}} = 480\,\mathrm{V}$ ($u^{*}_{\mathrm{pn,buck,min}} =$

488 V). It can be noted that when U_o is close to u_{pn}, d'_{vb} is comparably small (grey areas in **Fig. 4.8(a)**), and the system is not capable of decreasing the resonant current i_r fast enough, leading to insufficient current feeding into C_{pn}, whereby the capacitor voltage u_{pn} cannot be increased as required. Hence, the duty cycle d has to be adjusted if a certain dynamic response is required, as in **Fig. 4.8(b)**, which is realized by means of d_{ic}. To calculate d_{ic}, first of all, the required change of the resonant current has to be identified. According to the power balance, the output current i_o can be calculated as

$$i_o = \frac{u_{pn}}{U_o} \cdot i_{rpn}. \tag{4.4}$$

With $i_{rpn} = i_{pn} - i_{cpn}$ and $i_o = |i_r|$, (4.4) can be re-written as

$$|i_r| = \frac{u_{pn}}{U_o} \cdot (i_{pn} - i_{cpn}). \tag{4.5}$$

The same applies to the average values:

$$|\bar{i}_r| = \frac{u_{pn}}{U_o} \cdot (\bar{i}_{pn} - \bar{i}_{cpn}). \tag{4.6}$$

Thus the change of the resonant current due to the required change of the capacitor current is

$$\Delta|\bar{i}_r|_{max} = \frac{u_{pn}}{U_o} \cdot \Delta\bar{i}_{cpn,max} = \frac{u_{pn}}{U_o} \cdot 2\bar{i}_{cpn,max}, \tag{4.7}$$

where $i_{cpn} = C_{pn}\frac{du_{pn}}{dt}$ and its average value over one switching period $\bar{i}_{cpn}$ is shown in **Fig. 4.4(a.iv),(b.iv)**.

Similarly, the relationship between d_{ic} and the required change of the resonant current $\Delta|\bar{i}_r|$ needs to be determined numerically. For the sake of simplicity, it can be assumed that before each half period with a certain duty cycle, the steady-state is reached, i.e., $\bar{i}_r = I_o$ and i_r reaches zero at the end of the half period, whereby the resonant current can be calculated and the change of its average value with respect to the previous period can be derived. One solution to avoid complicated calculations of d_{ic} is to keep always a certain margin ($u_{diff} = 50$ V) between u_{pn} and U'_o, as long as U'_o is smaller than the absolute maximum line-to-line voltage (around 563 V), and only changing to SRC-mode when no additional i_{cpn} is present ($\bar{i}_{rpn} \approx \bar{i}_{pn}$).

Ideally, the sharp reduction of $\bar{i}_r$ should be accomplished within a short time interval, e.g., in one or two resonant half cycles as shown in **Fig. 4.8(b)**, which however, cannot be achieved for all operating points. It can be noted

from (4.7) that the lower the U_o, the higher the $\Delta|\bar{i}_r|_{max}$. Therefore, for a small U_o the required change of the resonant current may not be achieved even by applying a complete zero-voltage period ($d = 1$), especially for resonant tanks with comparably large inductors, as shown in **Fig. 4.9(a)** with $U_o = 240\,V$. After one cycle where $d = 1$, i_r has not yet been reduced to the desired value and the d'_{vb} in the next few periods is not sufficient to decrease i_r fast enough (due to a small difference between u_{pn} and U_o), resulting in low-frequency ripples across u_{pn}. Thus, once $\Delta|\bar{i}_r|_{max}$ is above $\Delta|\bar{i}_r|_{d=1}$, d_{ic} needs to be adjusted according to i_r as well until it reaches the required value. Another solution would be to use a resonant tank with smaller impedance, e.g., reducing L_r to 25 µH or to decrease the value of C_{pn}, e.g., to 25 µF. However, this would lead to larger RMS currents or larger fluctuations across u_{pn}, which would deteriorate the performance of the system.

4.2.5.5 Voltage Level Selection (Block V in Fig. 4.3)

Depending on the output voltage, different voltage levels on the primary side are applied to the resonant tank. In general, if U_o is lower than $\frac{1}{2}u^*_{pn,buck}$, zero-voltage intervals (0) and half-voltage intervals ($\pm\frac{1}{2}u_{pn}$) should be used, whereas full-voltage intervals ($\pm u_{pn}$) and half-voltage intervals ($\pm\frac{1}{2}u_{pn}$) should be used when $U_o > \frac{1}{2}u^*_{pn,buck}$. However, when U_o is in the near vicinity of $\frac{1}{2}u_{pn}$, due to the voltage drop across all the components, the voltages applied to the resonant tank (u_{pri} and u_{sec}) may be slightly different from u_{pn} and U_o. As a result, if the measured U_o is smaller than $\frac{1}{2}u_{pn}$ and the T-type bridge-leg is used to increase i_r, u_{pri} may be smaller than u_{sec}, leading to a decreased i_r instead. Such inappropriate selections of voltage levels are causing distortions across u_{pn}, as shown in **Fig. 4.11(a)**, which will affect the inductor currents $i_{a,b,c}$ of the PFC rectifier stage. Hence, in order to facilitate a smooth transition from one pair of voltage levels to another, the system is allowed to switch back and forth between the voltage pairs. A flowchart is shown in **Fig. 4.10**, exhibiting the procedure of the voltage level selection. First of all, u_{pn} is compared to $u^*_{pn,buck}$ to check if the system is in the transient state due to disturbances or due to a load step, etc. If u_{pn} deviates from $u^*_{pn,buck}$ by more than u_{n2} (in the range of 5...10V), then only full-voltage intervals and zero-voltage intervals are used, such that the system is brought back to the steady state fast enough. In this situation, the use of duty cycle operation is disabled. Next, if U_o falls in the range of $\frac{1}{2}u_{pn} \pm u_n$ (u_n is again around 3 V...5 V), all voltage levels are used. When u_{pn} is lower than its reference $u^*_{pn,buck}$, zero-voltage intervals (0) and half-voltage intervals ($\pm\frac{1}{2}u_{pn}$) are employed, while full-

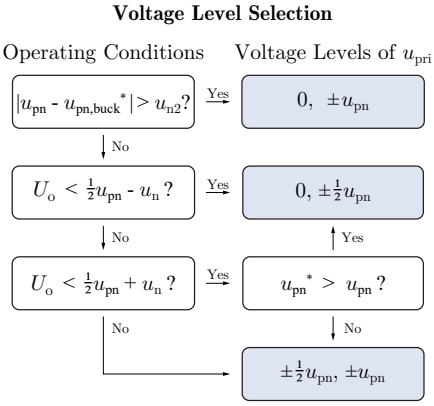


Fig. 4.10: Flowchart for selecting the appropriate voltage levels of the primary-side switch-node voltage u_{pri} used for the generation of PWM signals.

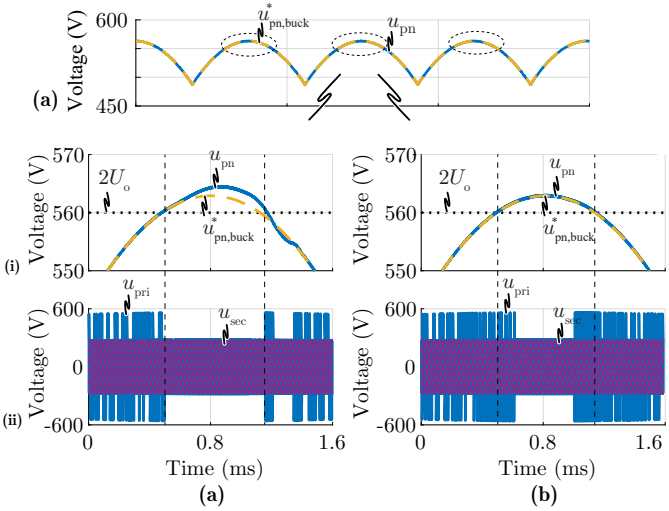


Fig. 4.11: Simulation waveforms of the H-QSRC in buck-mode for $U_o = 280\,V$ **(a)** selecting the voltage levels simply based on the relationship between U_o and $u^*_{pn,buck}$ and **(b)** with the modified strategy depicted in **Fig. 4.10**: **(i)** DC-link voltage u_{pn} and its reference $u^*_{pn,buck}$, **(ii)** primary-side applied voltage u_{pri}, and secondary-side applied voltage u_{sec}.

voltage intervals ($\pm u_{\mathrm{pn}}$) and half-voltage intervals ($\pm\frac{1}{2}u_{\mathrm{pn}}$) are utilized if u_{pn} is larger than its reference $u^*_{\mathrm{pn,buck}}$, whereby the controllability of i_{r} is guaranteed. **Fig. 4.11** shows the comparison between using the aforementioned selection strategy (**Fig. 4.11(b)**) and simply selecting the voltage level according to the relationship between U_{o} and $u^*_{\mathrm{pn,buck}}$ (**Fig. 4.11(a)**). It can be noted that the transitions become much smoother with the proposed strategy.

It needs to be mentioned that due to the requirement of $\Delta|\bar{i}_{\mathrm{r}}|$ in the valley of the six-pulse course of u_{pn}, as discussed in the last section, for a U_{o} which is only slightly above $\frac{1}{2}u^*_{\mathrm{pn,buck}} + u_{\mathrm{n}}$, applying half-voltage intervals cannot reduce i_{r} fast enough as well, and zero-voltage intervals need to be used. Again similar strategies are implemented here, i.e., as long as the resonant current is not decreased to the required value, switching back and forth between voltage levels is allowed.

4.2.5.6 Boost-Mode

In boost-mode, the control of the H-QSRC is much simpler than in buck-mode, as $u^*_{\mathrm{pn,boost}}$ is fixed at 850 V, which is the highest voltage level the primary-side switches can withstand safely. Furthermore, i^*_{cpnb} is set to zero as the T-type bridge-leg is not used. The voltage selection block is also disabled since there is no T-type bridge-leg on the secondary side. Moreover, $m_{\mathrm{boost}} = 1$, which is the same as in a conventional boost converter, where the inductor current is equal to the input current. Moreover, the calculation of the duty cycle is easier as $d_{\mathrm{ic}} = 0$ and $d = d^{'}_{\mathrm{vb}}$. The PWM signals are therefore calculated based on i_{r}, i^*_{r} and the calculated duty cycle.

To sum up, with the all aforementioned control blocks, Synergetic Operation 3 can be implemented successfully; the resulting simulation waveforms are shown in **Fig. 4.4**.

4.3 Optimal Synergetic Operation and Experimental Evaluation of a Two-Stage EV Charging System Employing the Vienna Rectifier Front-End and Four DAB Converters

Aiming for a very compact realization, we select a Vienna Rectifier (VR) [116] front-end (see **Fig. 2.14**), which advantageously can be realized using latest-generation 600 V GaN transistors and 1200 V SiC diodes. The thus enabled

high switching frequency and the three-level characteristic of the VR facilitate a very compact realization of the boost inductors and the EMI filter stages. Note that bidirectional power flow could be achieved by replacing the diodes with transistors. The split intermediate DC-link of the VR is then used as input for the subsequent stage realizing the galvanic separation with two stacked DC/DC converter modules, which then also can be realized with 600 V GaN technology. The direct precursor to the analysis presented in the following is [32], which details the 1/3-PWM concept for an EV charger module consisting of a VR and two generic DC/DC converter stages. As an aside, note that also non-isolated DC/DC converters could be employed. In that case, only the ratio of the required output voltage to the grid line-to-line voltage amplitude decides whether the DC/DC stage must operate; if it does, it is always advantageous to operate it in a way that allows 1/3-PWM for the rectifier stage, i.e., for each operating point there is a clearly defined optimum operating mode of the two converter stages [117, 118]. This is different in the cases considered in [32] and here, where the isolated DC/DC converter stage necessarily *always* operates and hence a system-level efficiency analysis must be employed to identify the optimum operating mode for a given operating point. However, [32] did not include a quantitative analysis of the optimum operating mode selection (3/3-PWM, 1/3-PWM) considering the VR front-end *and* the DC/DC converters, nor an experimental analysis. Therefore, the optimal operation and experimental verification of a 1/3-PWM VR in combination with isolated DC/DC converter stages is analyzed in this work, considering an exemplary three-phase 10 kW ultra-compact EV charger module with a wide output voltage range of 200 V to 1000 V.

4.3.1 Demonstrator System Overview

Whereas a theoretical analysis of the VR loss reduction achieved by 1/3-PWM compared to 3/3-PWM can be carried out by assuming arbitrary (ideal) DC/DC converters (see [32] and a brief summary in **Sec. 4.3.2**), this perspective is incomplete as the losses of actual DC/DC converters depend on the operating point and in particular on u_{xz} (cf. **Fig. 4.12**). Therefore, specific realizations of the VR front-end *and* the DC/DC converter stages must be considered to analyze the system-level optimum operating modes over the output voltage and power ranges.

Fig. 4.12 shows the power circuit schematic, including an EMI filter for compliance with CISPR 11 Class A, of the thus considered 10 kW two-stage EV charger system, an early prototype version of which has been mentioned

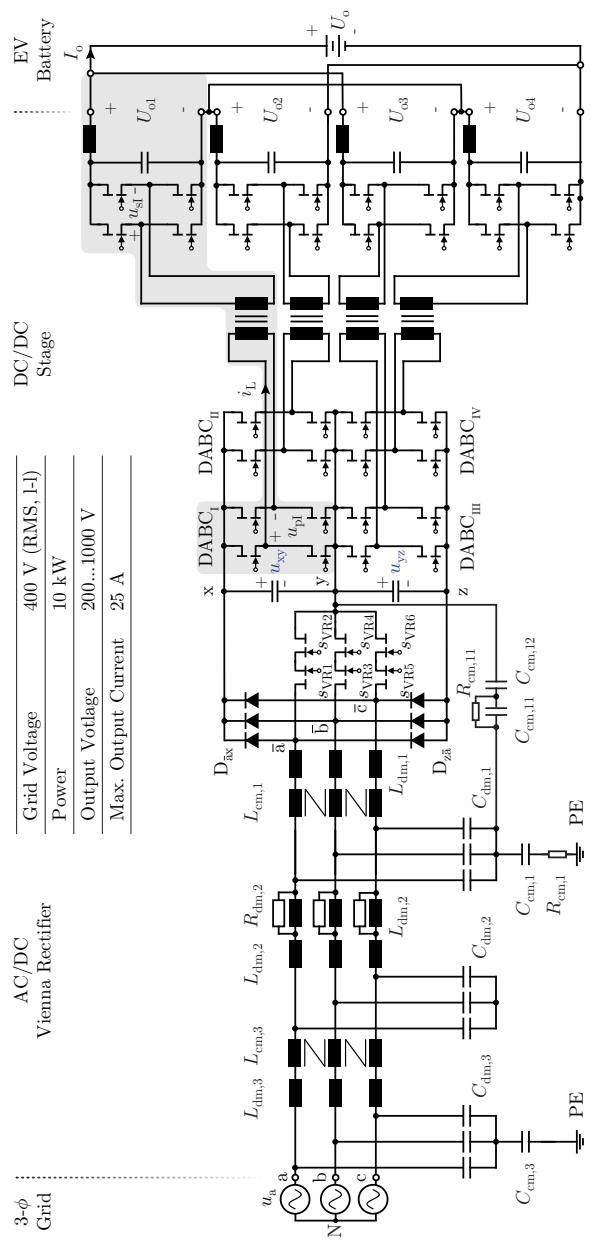


Fig. 4.12: Full schematics of the considered two-stage EV charger hardware prototype, including an EMI filter, the VR front-end, and four DABC modules.

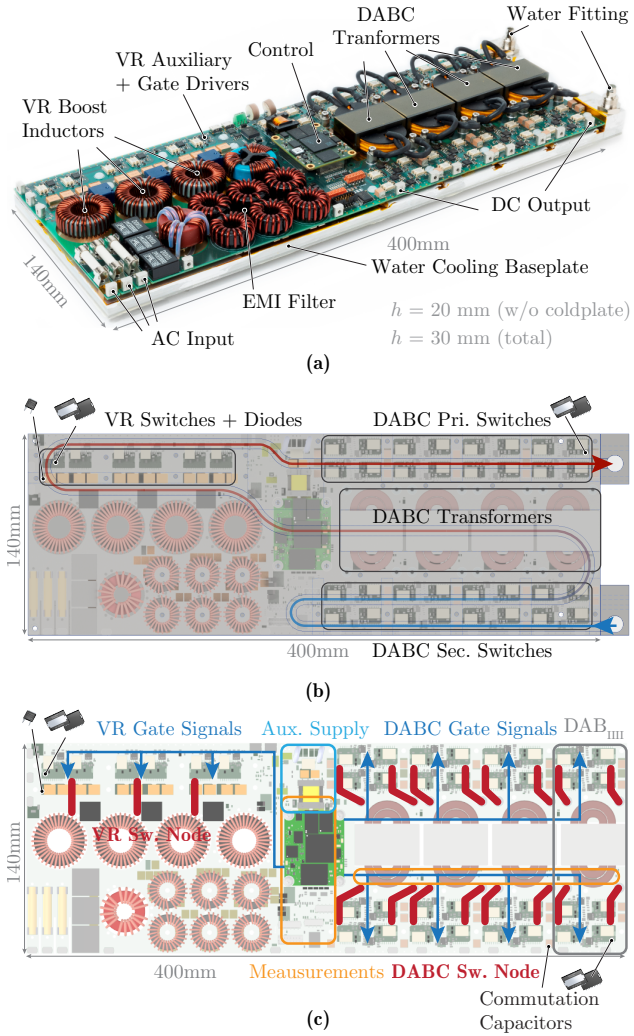


Fig. 4.13: **(a)** Photograph of the considered realized 10 kW three-phase two-stage VR and DABC hardware prototype. The overall dimensions of 400 mm × 140 mm × 20 mm (not including the non-optimized coldplate) yield a power density of around 9 kW/dm^3 or about 150 W/in^3. **(b)** Coldplate with the 7 mm × 4.3 mm water channel passing underneath the 38 GaN switches, the 12 SiC Schottky diodes, and the 4 DABC transformers. **(c)** Overview of key aspects of the PCB layout; the whole converter is realized on a single PCB.

in [119]. Note that each of the two DC/DC converters is realized with *two* DABCs, each rated at 2.5 kW. This, first, facilitates an ultra-flat realization and increases the DABC transformer surface area that can be attached to the coldplate, and, second, would enable improved part-load efficiency by only operating two instead of all four DABCs. Note further that the DABC modules are configured in a cross-wise input-parallel, output-series (IPOS, e.g., $\mathrm{DABC_I}$ and $\mathrm{DABC_{II}}$) and input-series, output-parallel (ISOP; e.g., $\mathrm{DABC_I}$ and $\mathrm{DABC_{III}}$) structure, thus utilizing the known natural balancing properties of IPOS and ISOP arrangements [120] to ensure balanced intermediate DC-link voltages.

Fig. 4.13 shows a photo of the realized system, and **Tab. 4.1** summarizes its main components. The high switching frequency ($f_{\mathrm{sw,VR}} = 560\,\mathrm{kHz}$) of the VR and the ultra-flat realization (overall dimensions of 400 mm × 140 mm × 20 mm, not including the coldplate) result in a comparably high power density of around $9\,\mathrm{kW/dm^3}$ (or about $150\,\mathrm{W/in^3}$). The system is liquid-cooled and the non-optimized and thus 10 mm thick coldplate[1] increases the volume by about 30%, corresponding to a power density reduction to about $6\,\mathrm{kW/dm^3}$ (or $98\,\mathrm{W/in^3}$). As shown in **Fig. 4.13(b)**, the water channel is shaped to cool all the 38 GaN switches, the 12 SiC Schottky diodes, and the 4 DABC transformers.

Further, **Fig. 4.13(c)** gives an overview on some key aspects of the PCB layout, which otherwise follows state-of-the-art best practices, e.g., regarding the design of GaN transistors' commutation loops, etc. Note that, except for a small credit-card-sized control board carrying a Xilinx Zynq-7000 SoC, the converter is realized on a single 8-layer PCB. Therefore, care has to be taken to prevent noise emissions from the power stages from disturbing measurements and logic circuitry. Placing the controller in the center of the converter facilitates routing the gate signals (blue arrows) without any overlap with noisy switch-node planes (red). Furthermore, common-mode chokes are placed between the controller and all the gate drivers to further suppress the noise coupled along the comparably long digital lines. This is necessary even though the employed gate drivers have a comparably high common-mode rejection capability [122]. The analog circuitry of the VR measurements (orange) is also placed in the relatively quiet center of the PCB, whereas the DABC measurements (orange) are beneath the transformer winding; a shielding layer in the PCB (top layer connected to logic ground) prevents noise issues. Furthermore, the PCB features cutouts for the boost inductors and the transformers, which facilitates the ultra-flat realization.

[1] As shown in [121], the thickness of the coldplate could be cut in half, i.e., reduced to about 5 mm without impairing the cooling properties.

Tab. 4.1: Main Components of the 10 kW EV Charger Module (see **Fig. 4.12**).

Parameter	Value
	EMI Filter
Boost Ind. $L_{\mathrm{dm,1}}$	36 µH, Magnetics Molypermalloy Powder (MPP), 55550 core, 36 turns, 1.4 mm wire
CM Ind. $L_{\mathrm{cm,1}}$	320 µH, TDK N87, R34 (B64290L0058X087), 12 turns per winding, 1.4 mm wire
DM Cap. $C_{\mathrm{dm,1}}$	560 nF (10x56 nF X2 rated)
CM Cap. $C_{\mathrm{cm,1}}$	18.8 nF (4x4.7 nF Y2 rated)
CM Resistor $R_{\mathrm{cm,1}}$	22 Ω
CM Cap. $C_{\mathrm{cm,11}}$	220 nF
CM Resistor. $R_{\mathrm{cm,11}}$	47 Ω
CM Cap. $C_{\mathrm{cm,12}}$	220 nF
DM Ind. $L_{\mathrm{dm,2}}$	16.5 µH, Kool Mµ MAX Toroids (79351), 18 turns, 1.8 mm wire
DM Resistor. $R_{\mathrm{dm,2}}$	47 Ω
DM Cap. $C_{\mathrm{dm,2}}$	336 nF (6x56 nF X2 rated)
CM Ind. $L_{\mathrm{cm,2}}$	560 µH, VAC Nanocrystalline VITROPERM cores T60006-L2025-W380, 6 turns per winding, 1.8 mm wire
DM Ind. $L_{\mathrm{dm,3}}$	6.8 µH, shielded wirewound inductor (Würth 7443556680)
DM Cap. $C_{\mathrm{dm,3}}$	224 nF (4x56 nF X2 rated)
CM Cap. $C_{\mathrm{cm,3}}$	9.4 nF (2x4.7 nF Y2 rated)
	Vienna Rectifier Stage
Boost Ind. L	36 µH, Magnetics Molypermalloy Powder (MPP), 55550 core, 36 turns, 1.4 mm wire
Switches	600 V, 70 $\mathrm{m\Omega_{max}}$ / 55 $\mathrm{m\Omega_{typ}}$ CoolGaN™ IGOT60R070D1
Diodes	1200 V SiC Schottky CoolSiC™ IDM10G120C5 (2 in parallel)
Gate Drivers	EiceDRIVER™ 1EDF5673K
Sw. Freq. $f_{\mathrm{sw,VR}}$	560 kHz
DC Cap. $C_{\mathrm{xy}}, C_{\mathrm{xy}}$	28 µF
	Dual Active Bridge Converter Stage
Switches (Pri. & Sec.)	600 V, 42 $\mathrm{m\Omega_{max}}$ / 37 $\mathrm{m\Omega_{typ}}$ CoolGaN™ IGOT60R042D1
Gate Drivers	EiceDRIVER™ 1EDF5673K
Transformer	ELP43/10/28 core, N97 ferrite, no air-gap, 16 turns prim., 1200x40 µm litz, 10 turns sec., 1200x40 µm litz, L_{σ} = 13 µH, L_{m} = 300 µH
Sw. Freq. $f_{\mathrm{sw,DABC}}$	180-330 kHz

In the following, the operating modes and especially the loss models for the VR (**Sec. 4.3.2**) and the DABC (**Sec. 4.3.3**) stages will be introduced, which

then allow a quantitative comparison of the efficiency that the two-stage system achieves when it operates with 3/3-PWM or 1/3-PWM (**Sec. 4.3.4**).

4.3.2 Vienna Rectifier Stage

4.3.2.1 VR Loss Model

This work's goal of providing a system-level comparative analysis of the EV charger operation with 3/3-PWM and 1/3-PWM requires a straightforward yet accurate loss model of the VR, which considers the main loss components (i.e., conduction and switching losses of the 600 V, 70 m Ω GaN transistors and the 1200 V SiC diodes, and the EMI filter losses; please refer to **Tab. 4.1** for a detailed component list).

The conduction losses of all semiconductors follow directly from the per-device average and RMS currents given in **Tab. 2.6** and the respective on-state characteristics from the datasheets. An electro-thermal model is used to account for the temperature-dependency of the conduction losses using a linear approximation of the on-state resistance's dependency on the junction temperature as $R_{\mathrm{on}}(T_{\mathrm{j}}) \approx 70\,\mathrm{m\Omega} + 0.36\,\mathrm{m\Omega/K} \cdot (T_{\mathrm{j}}[^{\circ}\mathrm{C}] - 25\,^{\circ}\mathrm{C})$ (note that the maximum specified nominal on-state resistance at room temperature, i.e., 70 m Ω, is used to ensure a conservative design). Furthermore, a (measured) thermal resistance from transistor junction to the cooling liquid of $R_{\mathrm{th,j-w}} = 2.5\,\mathrm{K/W}$ and an average liquid temperature of 35 °C are considered (note that the temperature difference between liquid inlet and outlet is less than 6 K and hence neglected).

Similarly, the switching losses can again be calculated with the equations from **Tab. 2.6**, but it is interesting to briefly consider how the switching loss model parameters $k_{\mathrm{sw,0}}$ and $k_{\mathrm{sw,1}}$ are obtained. Even though full (calorimetrically) measured loss maps for the employed GaN transistors are available [123], these pertain to symmetric half-bridges and not to the (relevant hard switching) commutations against a 1200 V SiC Schottky diode as occurring in the considered VR. To account for this, and especially also for the second diode that is not actively involved in a commutation but, being connected to the switch node, contributes to the capacitive switching losses, we calculate $k_{\mathrm{sw,0}}$ from the involved voltage-dependent device capacitances (and the parasitic switch-node capacitance resulting from the PCB layout) as described in [124]. Note that $k_{\mathrm{sw,0}}$ thus depends on the voltage u_{xy} (with 1/3-PWM, this value would be even time-variant, but, for simplicity, we use a constant value of $\overline{u}_{\mathrm{xz}} = 537\,\mathrm{V}$, i.e., the time average of u_{xz}, to calculate $k_{\mathrm{sw,0}}$). On the other hand, the current-dependency of the switching losses is assumed to be dominated

by the transistor's characteristic and hence $k_{sw,1}$ from the mentioned loss maps [123] is used.

Finally, the main loss contributions of the compact EMI filter (given the 560 kHz switching frequency) are the conduction losses of all inductive components, which can be modeled by a 70 mΩ series resistance for each phase; core losses of the magnetic components are neglected.[2]

4.3.2.2 Experimental Verification

To verify the aforementioned loss models, the VR stage is commissioned and operated with 3/3-PWM and with a (for testing purposes) reduced switching frequency of 400 kHz. **Fig. 4.14(a)** compares the calculated (using the model from above) and measured efficiencies of the VR stage and provides a (calculated) loss breakdown. Even though the loss model is quite straightforward, it achieves a reasonably good accuracy. **Fig. 4.14(b)** shows the calculated efficiency curve and loss breakdown of the VR stage operating with 1/3-PWM.[3] The significant reduction of switching losses improves the efficiency by almost one percentage point at nominal and even more at lower output power; this effect will be even more pronounced at the final switching frequency of 560 kHz.

4.3.3 DAB Converter Modules with Wide Output Voltage Range

From a VR perspective alone, operation with 1/3-PWM seems clearly favorable. However, the question to be answered later in **Sec. 4.3.4** is at what cost in terms of possibly increased DABC losses the VR's efficiency gain comes. Therefore, this section discusses, similarly, the operating modes and loss model of the DABC modules.

The DABC modules employ the same modulation and are built identically as the DAB converter introduced in **Sec. 3.3**. **Fig. 4.15** shows measured voltage and current waveforms of a DABC module for six different operating points (remember that each DABC module connects to only one half of the

[2] For the operating conditions of **Fig. 4.14(a)**, calculations based on manufacturer data indicate less than 0.6 W of core losses per boost inductor; the other magnetic components of the EMI filter are expected to show lower core losses as they carry already much lower high-frequency ripple currents. At rated output power, core losses thus account for less than 1% of the total losses.

[3] Note that it is not possible to measure the efficiency of the VR operating with 1/3-PWM without also running the DC/DC converters to shape u_{xz}. The corresponding measurements of the two-stage system are presented later in **Sec. 4.3.5**.

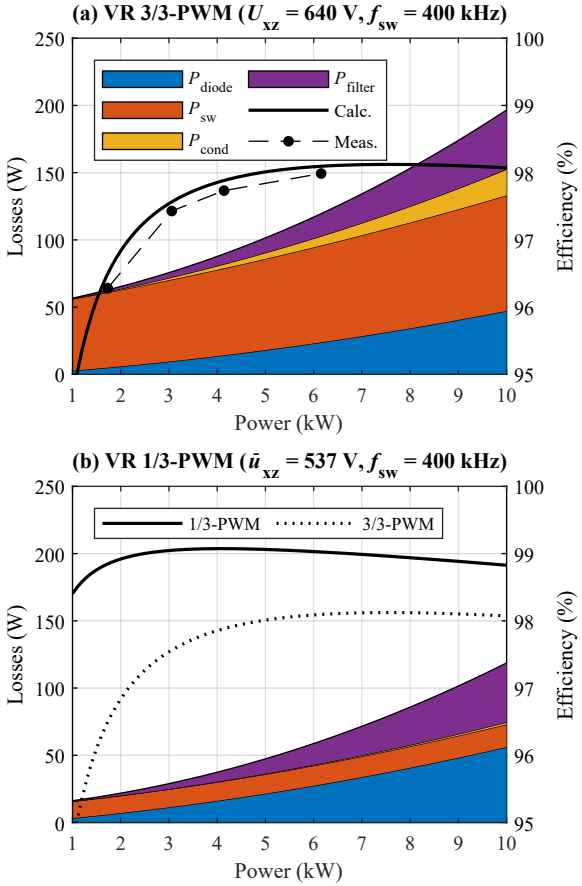


Fig. 4.14: Calculated efficiencies and loss breakdowns of the VR operated **(a)** with 3/3-PWM (U_{xz} = 640 V), including measured (Yokogawa WT-1804E) efficiencies for verification, and **(b)** with 1/3-PWM, which achieves a significant reduction of the switching losses. Note that this comparison considers a switching frequency of 400 kHz, i.e., lower than the 560 kHz used in the final prototype.

split VR DC-link, see **Fig. 4.12**, hence the maximum input voltage is 400 V for the maximum U_{xz} = 800 V and, similarly, the output voltage is, e.g., 400 V for a system output voltage of U_o = 800 V). **Fig. 4.16** shows the measured (Yokogawa WT-3000) efficiencies of the DABC module, again for six different

operating points. The comparison with the calculated efficiency curves shows good accuracy.

Subsequently, the remaining three modules of the DAB converter stage were commissioned and tested individually, and showed similar performance to the first module. In the last step, the four modules were operated simultaneously. The measured current waveforms of all four modules are shown in **Fig. 4.17** for a total output voltage U_o of 500 V and a total input voltage u_{xz} of 640 V, at 4.1 kW output power. For simplicity reasons, interleaving on a switching frequency level is not implemented in this system.

4.3.4 Optimum Operation of the Two-Stage System

In the previous two sections, the detailed loss modeling of the VR stage and the DABC modules have been discussed, and the accuracy of the relatively straightforward models has been demonstrated by close agreement of calculated and measured efficiencies. In a next step, the introduced loss models can thus be used to assess the different options of how to operate the full, two-stage EV charger demonstrator comprising a VR stage and four DABC modules (see **Fig. 4.13**). This is done by calculating efficiency maps, i.e., efficiencies for a grid of operating points defined by the tuples (U_o, P_o) in the ranges given in **Fig. 4.12**, and considering different operating regimes. **Fig. 4.18** provides an overview of this process, which is detailed in the following together with the results.

4.3.4.1 Operation with 3/3-PWM

A first basic option is to select a single, *constant* value for U_{xz} that is kept regardless of the operating point. The VR then operates with 3/3-PWM, regulates U_{xz} to a constant value, and the DABCs provide isolation and scale the voltage as required by the load. **Fig. 4.19(a)** and **Fig. 4.19(b)** show the resulting efficiency maps for the considered output power and output voltage ranges for $U_{xz} = 640$ V and $U_{xz} = 800$ V, respectively. Clearly, the region of maximum efficiency shifts between the two cases. Therefore, it is beneficial to consider adapting the intermediate DC-link voltage U_{xz} depending on the operating point, such that minimum overall losses (i.e., the sum of VR and DABC losses) result.

Fig. 4.19(c) shows the corresponding optimal selection of U_{xz} in the range of 640 V to 840 V (the lower limit ensures sufficient control margin for a 400 V grid, and the upper ensures compatibility with the employed 1200 V diodes and 600 V GaN transistors, the latter being exposed to $U_{xz}/2$ only).

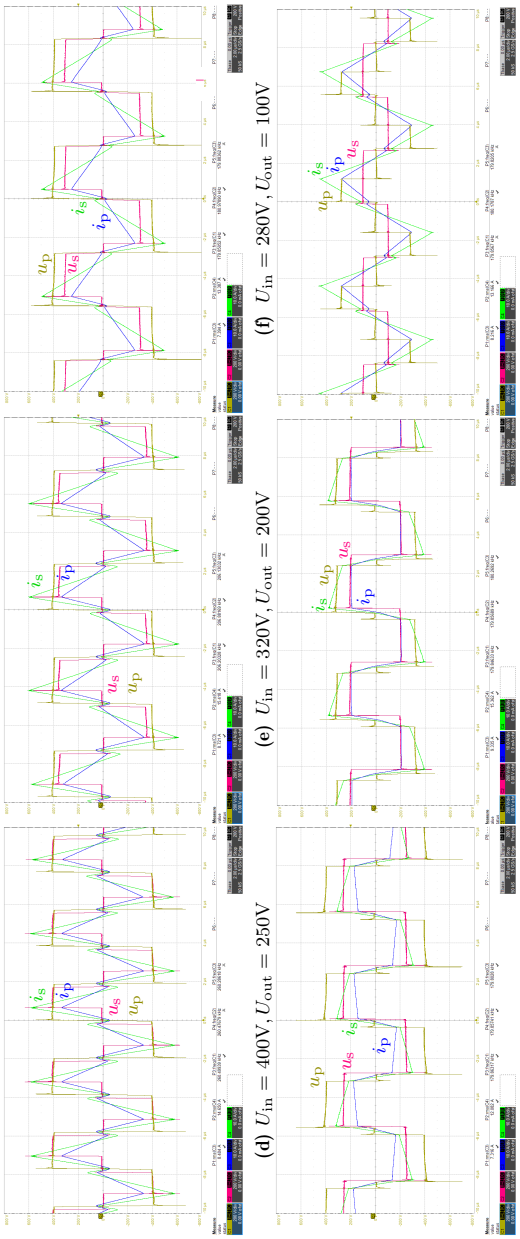


Fig. 4.15: Measured waveforms of a DABC module operating at rated load of 2.5 kW (except for the case with an output voltage of 100 V, where the 12.5 A maximum output current limits the power to 1.25 kW, see also **Fig. 4.16**) and with various input/output voltage combinations. u_{p}, u_{s}, i_{p} and i_{s} are the primary-side and secondary-side transformer voltages and the primary-side and secondary-side transformer currents, respectively.

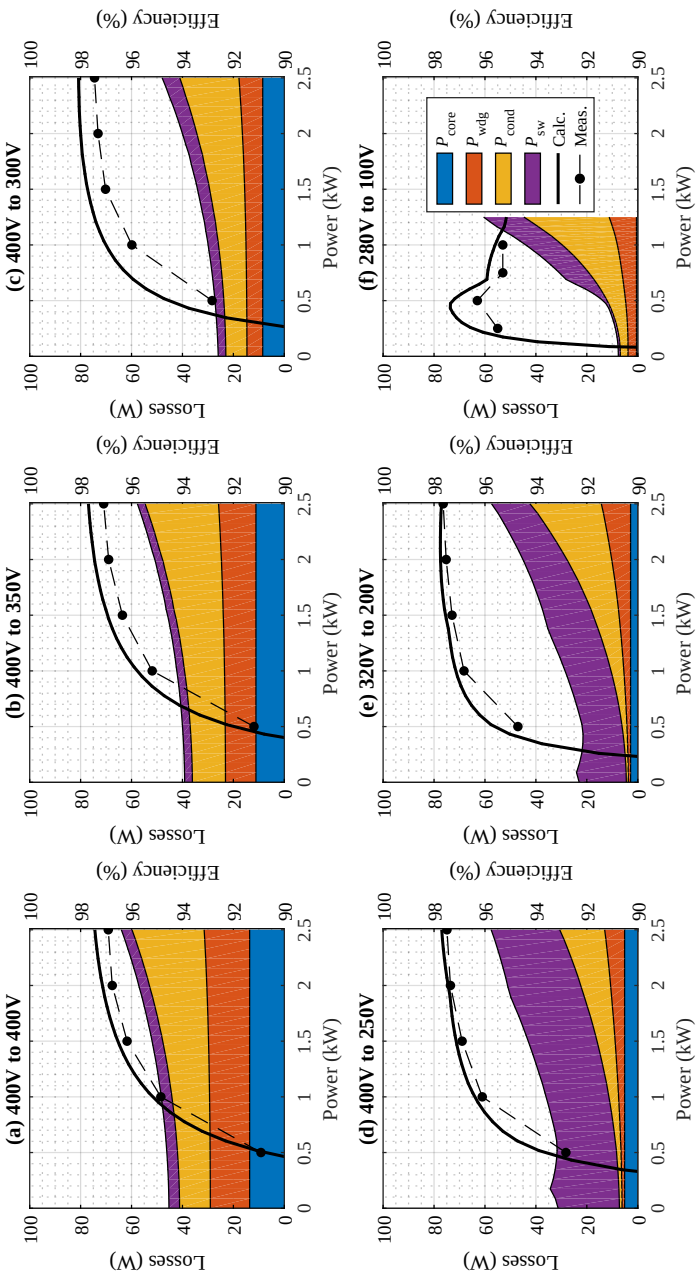


Fig. 4.16: Measured and calculated DABC module efficiencies for various operating points, and calculated loss breakdowns. Note that the output current limit (12.5 A, single module) limits the power to 1.25 kW when operating with an output voltage of 100 V only.

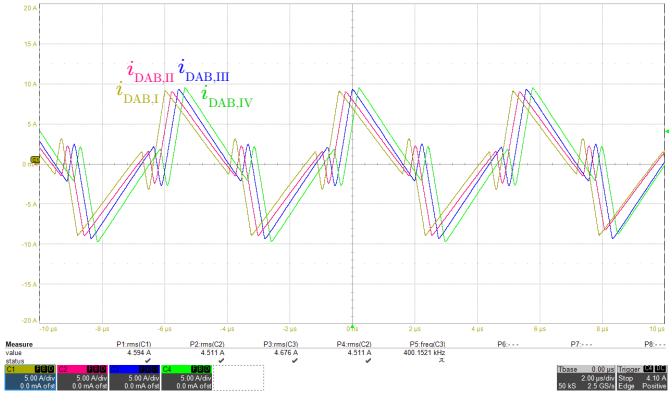


Fig. 4.17: Experimentally measured waveforms of four DAB converter modules for a total output voltage U_{out} of 500 V and a total input voltage of 640 V, at 4.1 kW output power. Interleaving is not implemented.

Fig. 4.19(d) shows the corresponding efficiency map for optimally selected U_{xz} values and **Fig. 4.19(e)** illustrates the improvement (in percentage points, p.p.) over the case with an operation-point-independent $U_{xz} = 800$ V shown in **Fig. 4.19(a)**. Especially at lower output voltage, it pays to select a low U_{xz} value, too, which enables the DABCs to operate closer to their natural voltage transfer ratio ($n = 16/10$). Correspondingly, U_{xz} should increase with the output voltage, but only up to a point ($U_o \approx 600$ V). For even higher output voltages, a slight reduction of U_{xz} lowers the VR switching losses more than it increases the DABC losses. The changing VR loss share shown in **Fig. 4.20(a)** illustrates this point.

4.3.4.2 Operation with 1/3-PWM

So far, adaptive but, for a given operating point, still *constant* intermediate DC-link voltages U_{xz} and hence 3/3-PWM of the VR have been considered. However, as discussed earlier, the DABC modules can be utilized to shape the intermediate DC-link voltage into a time-varying six-pulse shape to facilitate 1/3-PWM operation of the VR with the associated significant reduction of switching losses (note the lower VR loss share in **Fig. 4.20(b)**). **Fig. 4.19(f)** shows the corresponding efficiency map, whereby the losses have been calculated approximating the time-varying voltage u_{xz} by its average value $\overline{u}_{xz} = 537$ V. **Fig. 4.19(g)** then shows the efficiency change (in percentage

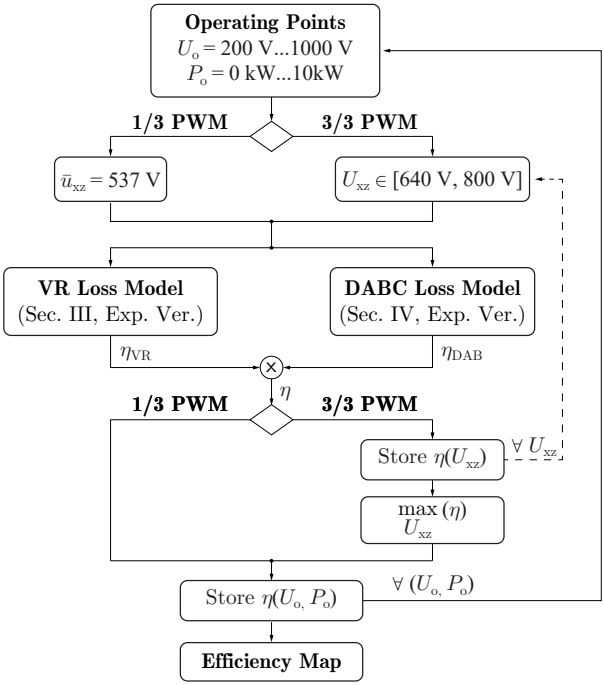


Fig. 4.18: Flowchart illustrating the procedure used for obtaining the efficiency maps shown in **Fig. 4.19**. For 3/3-PWM, either a fixed U_{xz} for all operating points can be used, or, alternatively and as indicated by the dashed line, for each operating point an optimized U_{xz} that results in the highest overall efficiency can be used. In contrast, for 1/3-PWM, u_{xz} shows a time-varying six-pulse shape regardless of the operating point, and the corresponding average value $\bar{u}_{xz}$ is used for the calculations. Note further that the loss models of the VR and of the DABC have been introduced and experimentally verified individually in **Sec. 4.3.2** and **Sec. 4.3.3**, respectively.

points, p.p.) between 1/3-PWM and 3/3-PWM (with adaptive U_{xz}). Especially for lower output voltages and lower power levels, a significant efficiency increase of up to 2% results; this is not only because of the switching loss saving of the VR stage, but also because the lower u_{xz} in 1/3-PWM allows the DABC modules to operate closer to the natural voltage transfer ratio. At high output voltages and higher power levels, switching to 1/3-PWM is not always beneficial, as on the system level the VR loss reduction might be overcompensated by increasing DABC losses.

Fig. 4.19: Efficiency of the two-stage system operated with 3/3-PWM and **(a)** constant U_{xz} = 640 V or **(b)** U_{xz} = 800 V. Advantageously, however, U_{xz} is adapted with the operating points as shown in **(c)** to achieve the best possible (with 3/3-PWM) overall efficiency shown in **(d)**; **(e)** shows the improvement compared to (b) in percentage points (p.p.). **(f)** shows the efficiency when operating with 1/3-PWM and **(g)** gives the improvement compared to (d), i.e., 3/3-PWM with adaptive U_{xz}. Finally, **(h)** shows the best overall efficiency obtained when both, 3/3-PWM and 1/3-PWM are considered; the area where 1/3-PWM should be selected is highlighted. Note that the maximum output current of 25 A limits the power for low output voltages.

4.3.4.3 Combined 1/3-PWM and 3/3-PWM

Finally, **Fig. 4.19(h)** shows the efficiency map that can be achieved by the optimal combination of 1/3-PWM and 3/3-PWM. The thick dashed line delineates the region where 1/3-PWM should be used (i.e., where 1/3-PWM gives higher system-level efficiency than 3/3-PWM). **Fig. 4.20(c)** shows the corresponding VR loss share. The sharp step change at the boundary exists because even though the efficiency of the total system does change only very slightly (see **Fig. 4.19(h)**), the loss contributions of the VR and the DABCs change significantly when switching from 1/3-PWM to 3/3-PWM.

Note that in terms of efficiency (gains), see **Fig. 4.19(g)**, for the given system it might as well be a good engineering decision to *always* operate with 1/3-PWM, i.e., to forego certain minor loss savings in a rather small part of the operating range in favor of a simpler implementation. It is also essential to highlight that the results shown here are valid for our specific realization of the two converter stages. It should be noted that the system has been initially designed for 3/3-PWM operation; by changing the operating regime, a significant efficiency improvement can be achieved. In general, note that the boundary between 1/3-PWM and 3/3-PWM, and the overall efficiency map, depend (amongst other parameters), on the DABC modules' natural voltage transfer ratio and hence on the selected transformer turns ratio. Such degrees of freedom, and the possibility to employ 3/3-PWM and 1/3-PWM, should be considered for a new converter design, whereby a mission profile (weighted efficiency) could be used to identify, e.g., the optimum natural voltage transfer ratios of the DABC modules (i.e., the transformer turns ratio).

4.3.4.4 Output Series/Parallel Reconfiguration

In the standard prototype configuration (see **Fig. 4.12**), the total output voltage is shared by a series connection of two DABC modules. However, at lower output voltages it would be beneficial to reconfigure the DABC modules such that all four would be connected in parallel. Clearly, the maximum output voltage is then limited to 500 V. However, advantageously, the maximum output current increases to $4 \cdot 12.5\,\mathrm{A} = 50\,\mathrm{A}$, which implies that nominal power can be supplied even at only 200 V output voltage. Thus, **Fig. 4.21** shows the efficiency map considering all degrees of freedom (i.e., 3/3-PWM, 1/3-PWM, parallel reconfiguration of DABC outputs) to optimize the efficiency for each operating point. As an aside, note that this reconfiguration of the DABC outputs essentially has a similar effect as changing the transformer turns ratio: it shifts the area of maximum efficiency. Finally, note further

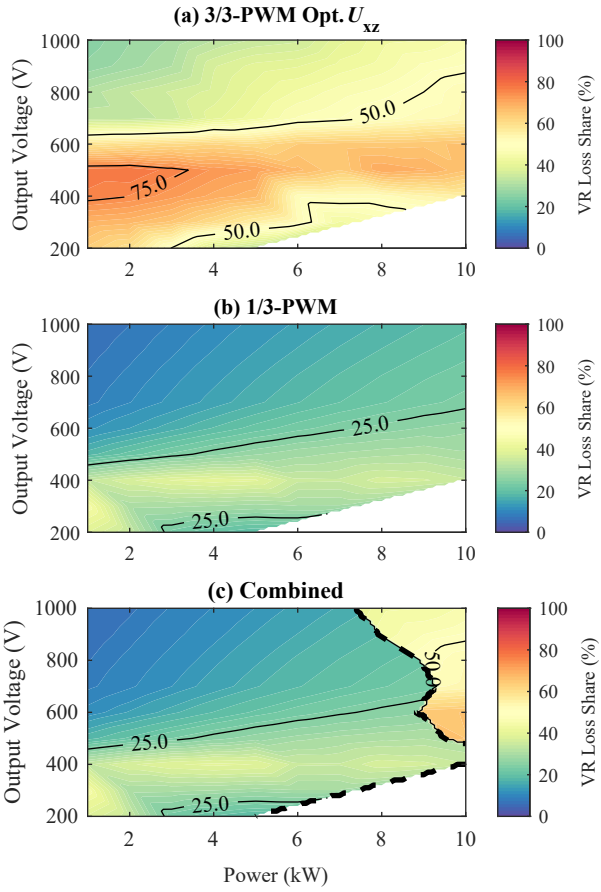


Fig. 4.20: Distribution of losses between the VR and the DABCs for operation with **(a)** 3/3-PWM (with optimum DC-link voltage), **(b)** 1/3-PWM, and **(c)** optimum combination of the two modes. Note that the maximum output current of 25 A limits the power for low output voltages.

that the availability of four DABC modules could also be utilized to improve the part-load efficiency by only operating two instead of four modules. This, however, is not investigated further here.

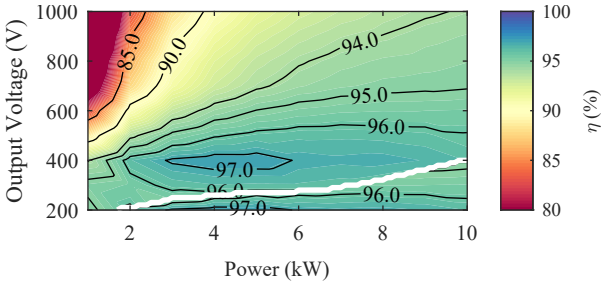


Fig. 4.21: Extension of the operating range by reconfiguring the four DABC modules (all four in parallel for output voltages lower than the white line indicates). The efficiency map considers the best combination of modulation (3/3-PWM and 1/3-PWM) and DABC module configuration for each operating point.

4.3.4.5 Influence of the Synergetic Control on the Optimal Turns Ratio of the DAB Converter Transformers

As already shown in **Sec. 3.3.2**, the optimal turns ratio of the DAB converter transformers for the given specifications is between 1.2...1.5, mainly because it is more efficient to operate the DAB converter in boost-mode rather than buck-mode. Consequently, its optimal input voltage, i.e., u_{xz}, tends to be higher, following nU_{out}, as shown in **Fig. 4.22(a)** with the x-axis indicating the output voltages U_o and the corresponding optimal u_{xz} for full load operation. It can be seen that the efficiencies of VR do not change significantly with the output voltages, compared to the DAB converter stage. Therefore, the whole system efficiency (indicated with the black line) follows the trend of the DAB converter stage, and it is still the case that the boost-mode is more efficient than the buck-mode for the two-stage system.

However, if the 1/3-PWM operation of the VR for low output voltages is also taken into account, it can be seen that the VR efficiency and the overall efficiency of the system in these operating regions are significantly increased (cf. **Fig. 4.22(b)**, where the u_{xz} equal to 537 V, the average voltage of the six-pulse curve, means the system is operated with 1/3-PWM). Consequently, the system is now more efficient in buck-mode than in boost-mode, and the range where the VR can be operated with the 1/3-PWM should be maximized, which can be achieved with a reduced turns ratio in the DAB converters. For this reason, the overall efficiency of the system must be considered when optimizing the turns ratio of the DAB converter transformers if both 1/3-PWM and 3/3-PWM are to be used in the VR. **Fig. 4.23** shows the comparison of the

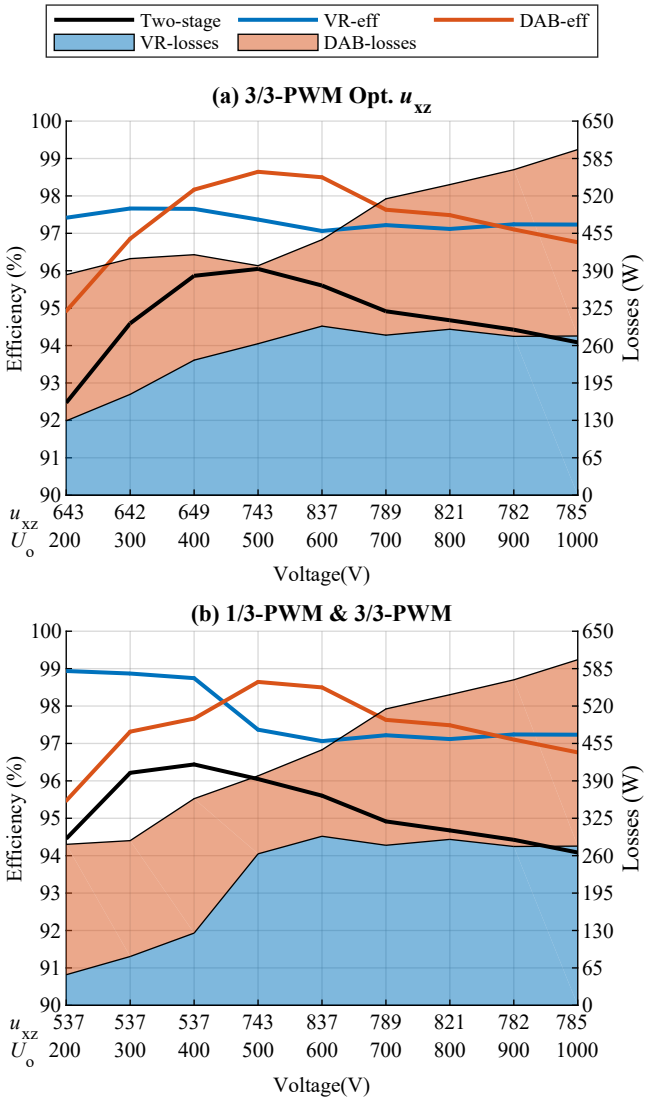


Fig. 4.22: System efficiencies and losses at full load for **(a)** 3/3-PWM (with optimum DC-link voltage) **(b)** optimum combination of the two modes.

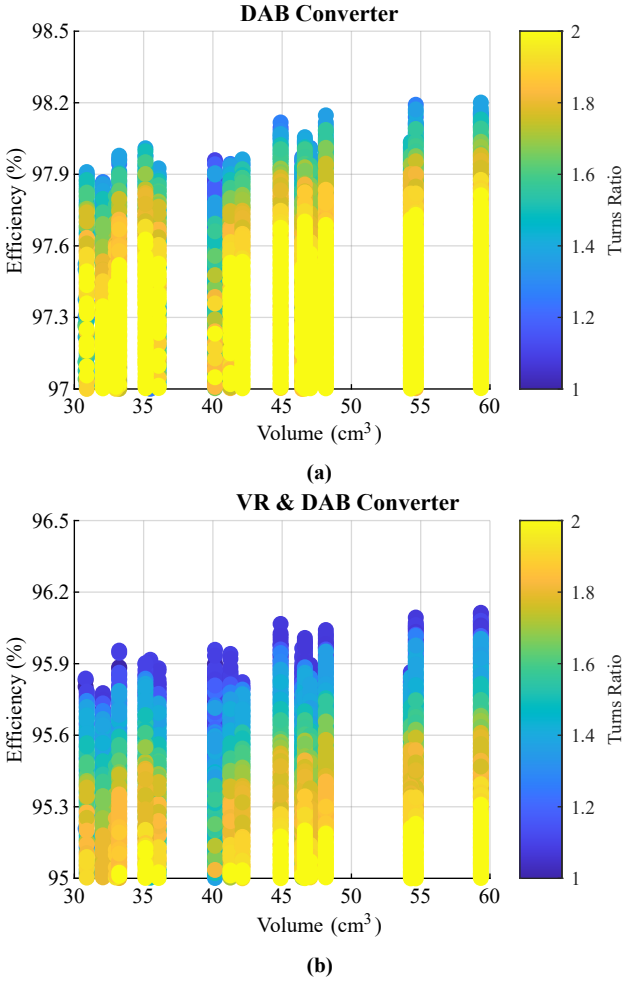


Fig. 4.23: Pareto optimization results for **(a)** only considering the DAB converter stage **(b)** considering the efficicies of the two-stage system using 1/3 and 3/3-PWM.

optimization results without and with considering the VR stage efficiencies (1/3-PWM included), and it can be seen that the optimal turns ratio has shifted to approximately 1 (can be even lower since n lower than 1 is not considered in the calculations) compared to the 1.2...1.5 from before, indicating that the

advantages of the DAB converter in boost-mode are offset by the VR operation in 1/3-PWM.

4.3.5 Hardware Verification

The two-stage demonstrator introduced in **Sec. 4.3.1** and analyzed throughout the work has originally been designed for operation with 3/3-PWM. After briefly discussing some control implementation aspects, we then provide a comparison of grid current total harmonic distortion (THD), system efficiency, and EMI performance for operation with 3/3-PWM and with 1/3-PWM, which is the main subject of this work.

4.3.5.1 Control System and Implementation

The control of the two-stage system is implemented on a Zynq-7000 SoC, which features a dual-core ARM central processing unit (CPU) and an integrated FPGA fabric. Advantageously, this allows to implement certain time-critical functions in the FPGA and more advanced algorithms in the CPU, as indicated in the overview control diagram shown in **Fig. 4.24**.

The SoC provides enough PWM outputs for the 38 switches, which require individual gate signals due to the employed single-channel gate drivers [122], capable of ensuring negative gate voltages under all operating conditions while being powered from a single supply voltage. This is crucial to prevent parasitic turn-on in fast-switching systems with a high number of WBG (GaN) power semiconductors. There are 16 measurement channels in the demonstrator system, including 5 voltage measurements (mains voltages u_{ab}, u_{bc} and intermediate DC-link voltages u_{xy}, u_{yz}) and 3 current measurements (i_a, i_b, i_c) for the VR, as well as 4 output voltage measurements and 4 output current measurements for the DAB converter modules. Since the DAB converter is a topology with very high dynamics, it is also very sensitive towards the applied voltage-time areas to the transformer windings, where in the case of a fault due to, e.g., noise coupled to gate signals, the transformer current can increase drastically within a very short time, leading to potential damage to the switches. Therefore, an over-current detection needs to be employed for each DAB converter, which reacts fast enough to protect the system, if the possibility of incorrect control of the DAB converters exists, e.g. during commissioning. In order to help safely commission the system, 8 over-current detection channels for the DAB converter stages are implemented in a separate PCB, which can be attached to the main PCB during commissioning (not shown in **Fig. 4.13** since they are not absolutely necessary during the

final operation of the system). It also needs to be noted that the DC blocking caps are also placed on this separate PCB, to prevent the DAB converter transformers from saturation, in case of slightly asymmetric voltage-time areas applied to the windings. Unlike the other measurements of the system, where the analog signals are fed into ADCs, and the protection logic in the FPGA then reacts based on the outputs of the ADCs, both the primary-side and secondary-side winding currents of the DAB converter transformer of each module are measured using analog high-bandwidth current sensors, where the outputs are directly compared to tunable voltage references using high-speed digital comparators (hence, no analog-to-digital conversion in between). The generated binary signals are then sent to the FPGA, where the internal logic is implemented in such a way that it immediately forces all the gate drivers to output negative gate voltages once a fault is detected. Consequently, due to the missing A/D conversion these over-current sensors have a much faster response time than conventional ADC measurements.

Even though a smooth transition from 1/3-PWM to 3/3-PWM is possible [32], it is not strictly needed: as discussed in the previous **Sec. 4.3.4**, due to the DAB's capability to step down or step up u_{xz} to the desired output voltage U_o, the selection of 1/3-PWM or 3/3-PWM is purely determined by efficiency considerations.[4] Therefore, the control implementation can be (externally) reconfigured between 3/3-PWM and 1/3-PWM operation; this is indicated by the two signal selectors in **Fig. 4.24**.

We will now briefly explain the main functional blocks of that control diagram, proceeding from left to right. First, the outer VR control loop regulates the intermediate DC-link voltage U_{xz} if 3/3-PWM is used; the DABCs then regulate, fully decoupled, the output voltage U_o. In contrast, if 1/3-PWM is used, the outer VR control loop regulates the output voltage. In both cases, a mains power reference (P^*_{33} or P^*_{13}) results. Together with the three measured (via two line-to-line voltage sensors, u_{ab} and u_{bc}) grid phase voltages, u_{abc}, the phase current references, i^*_{abc}, are then calculated. For 1/3-PWM, a common-mode voltage injection of $u_{CM} = 1/2 \cdot (u_{max} + u_{min})$ must be used, where u_{max} and u_{min} are the maximum and the minimum of the measured instantaneous phase voltages, respectively. As the duty cycles are calculated (in the FPGA, see below) by essentially dividing the phase voltage references by the actual intermediate DC-link voltage, u_{xz}, which,

[4] This is in contrast to non-isolated two-stage systems such as analyzed in [26, 33, 117, 118], where the non-isolated DC/DC stage provides only buck *or* boost functionality, i.e., for certain output voltages, the front-end can not operate with 1/3-PWM (e.g., if a boost-type rectifier is combined with a buck-type DC/DC converter, $u_{xz} \geq U_o$ must hold at all times and hence 1/3-PWM is not possible for high output voltages.)

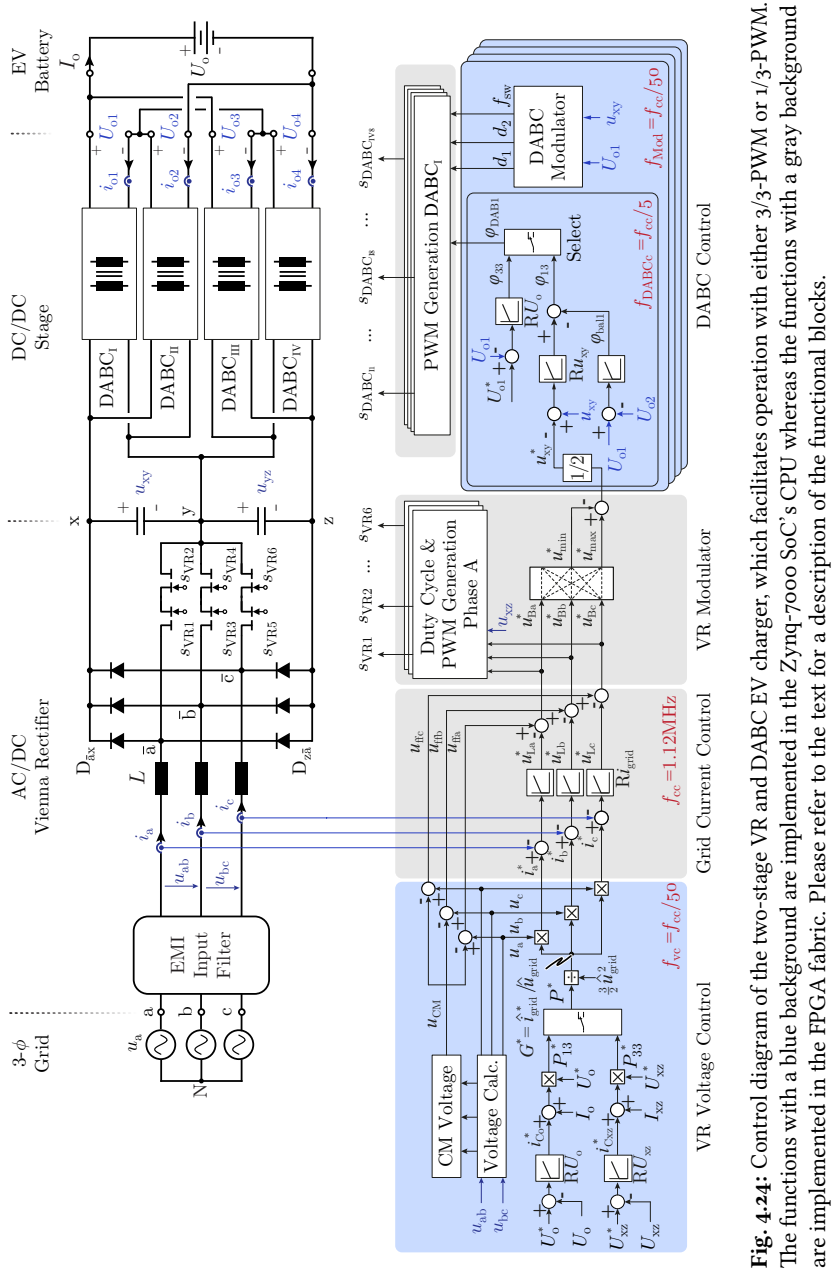


Fig. 4.24: Control diagram of the two-stage VR and DABC EV charger, which facilitates operation with either 3/3-PWM or 1/3-PWM. The functions with a blue background are implemented in the Zynq-7000 SoC's CPU whereas the functions with a gray background are implemented in the FPGA fabric. Please refer to the text for a description of the functional blocks.

for 1/3-PWM, follows $u_{xz} = \max(u_{max}, |u_{min}|)$, this ensures automatically that the two respective phases are clamped (the duty cycles become 1 and 0, respectively). For 3/3-PWM, the common-mode voltage injection, u_{CM}, is a degree of freedom and various options do exist [125]; advantageously, the method from [95] could ensure zero midpoint current. However, in the following, the same CM voltage injection as for 1/3-PWM is employed, which is equivalent to employing standard space-vector PWM (SVPWM). As the required bandwidth is relatively low, these calculations are implemented in the CPU and executed with an update rate of $f_{vc} = f_{cc}/50 = 22\,\text{kHz}$, where f_{cc} will be explained immediately.

On the other hand, given the VR's rather high switching frequency of $f_{sw,VR} = 560\,\text{kHz}$ and the thus small inductance of the boost inductors ($L = 30\,\mu\text{H}$) the grid current controllers are implemented in the FPGA to realize dual-update mode, i.e., a control loop execution frequency of $f_{cc} = 2f_{sw,VR} = 1.12\,\text{MHz}$. The controller outputs plus the feed-forward terms (i.e., the phase voltages including the CM injection) are then used to generate the VR reference voltages, u^*_{Babc}. Finally, using the measured DC-link voltage u_{xz}, the duty cycles are calculated[5] and ultimately the modulator generates the VR gate signals. Note that the FPGA clock frequency of 100 MHz results in limited yet sufficient quantization resolution (between 7 bit and 8 bit).

Further, the reference value for the intermediate DC-link voltage, u^*_{xz}, follows from the VR phase reference voltages and is fed to the DABC controllers, where, if 1/3-PWM operation is enabled, it is used as a control reference. Actually, two and two DABC modules regulate $u^*_{xy} = u^*_{xz}/2$ and $u^*_{yz} = u^*_{xz}/2$, respectively, and thereby ensure balanced intermediate DC-link halves (in addition to the shaping of u_{xz} as required by 1/3-PWM). Furthermore, since the VR can only control the total output voltage, an additional balancing controller is needed to ensure $U_{o1} = U_{o2} = U_{o3} = U_{o4}$. These controllers define the required power transfers of the DABC modules and hence the phase shifts $\phi_{DAB1,2,3,4}$. Because the required control bandwidth to shape u_{xz} is rather high (roughly 3 kHz in the current implementation), these controllers are executed in a CPU task with an update rate of $f_{DABCc} = f_{cc}/5 = 220\,\text{kHz}$. On the other hand, the modulation parameters, i.e., the duty cycles D_1 and D_2 and the switching frequency $f_{sw,DABC}$, are calculated based on measured voltage val-

[5] To avoid the costly division in the FPGA, the actual implementation correspondingly uses an approximation and scales the feed-forward terms u_{ffa}, u_{ffb}, and u_{ffc} with $1/u_{xz}$ in the CPU before passing them to the FPGA; a corresponding re-scaling of $u^*_{max} - u^*_{min}$ after being passed from the FPGA to the DABC control in the CPU is thus needed. This approach is feasible because of the small low-frequency voltage drops across the boost inductors (which are small given the high switching frequency) mentioned earlier, i.e., small values of u^*_{Labc}.

ues (see **Sec. 4.3.3**) in a slower task updating at again $f_{\mathrm{Mod}} = f_{\mathrm{cc}}/50 = 22\,\mathrm{kHz}$. Finally, the DABC PWM modulators are implemented in the FPGA.

4.3.5.2 Waveforms and THD Measurements

Using the control structure discussed in the last subsection, the EV charger is operated with both 3/3-PWM and 1/3-PWM at the rated power of 10 kW and with an output voltage of $U_{\mathrm{o}} = 500\,\mathrm{V}$. For 3/3-PWM, the total intermediate DC-link voltage is selected as $U_{\mathrm{xz}} = 640\,\mathrm{V}$, i.e., the lowest possible value for 3/3-PWM which is hence closest ot $\bar{u}_{\mathrm{xz}} = 537\,\mathrm{V}$ resulting for 1/3-PWM. **Fig. 4.25** shows the measured waveforms of the three-phase mains currents, the intermediate DC-link voltages u_{xy} and u_{yz} (with $u_{\mathrm{xy}} + u_{\mathrm{yz}} = u_{\mathrm{xz}}$), and the split output DC voltages $U_{\mathrm{o1}} = U_{\mathrm{o3}}$ and $U_{\mathrm{o2}} = U_{\mathrm{o4}}$ (remember that $U_{\mathrm{o1}} + U_{\mathrm{o2}} = U_{\mathrm{o}}$). The split DC voltages on either side of the DABC modules are balanced well.

In 1/3-PWM mode, the three-phase mains currents show some low-frequency distortions around the peak values. This is a consequence of the limited control bandwidth of the DABCs, which thus cannot exactly reproduce the six-pulse waveform of u^*_{xz} around the polarity change of the du^*_{xz}/dt in the valleys. Nevertheless, with a DABC control execution frequency of 220 kHz, operation with 1/3-PWM (where two of the three phase currents follow from the u_{xz} impressed by the DABCs and the VR directly controls only the remaining one) still achieves a total harmonic distortion (THD) of the mains currents of about 3% at rated power, see **Fig. 4.26**. This is higher compared to the about 1% resulting for 3/3-PWM (where the VR directly controls all three phase currents) but, given the efficiency improvement achieved with 1/3-PWM, seems a reasonable price to pay. Note that due to the high VR switching frequency, a turn-off delay compensation must be implemented to achieve these THD values; this is detailed in the **Appendix**.

4.3.5.3 Efficiency Measurements

Fig. 4.27(a) shows the calculated and measured (Yokogawa WT-1804E) efficiency characteristics of the two-stage system operating with 3/3-PWM ($U_{\mathrm{xz}} = 640\,\mathrm{V}$) and with 1/3-PWM, respectively, and an output voltage of $U_{\mathrm{o}} = 500\,\mathrm{V}$. The calculation results contain an additional offset of 16 W to account for the control hardware (Zynq-7000 SoC, gate drives, etc.). Similarly, **Figs. 4.27(b)(c)** show the calculated loss distributions between the stages as well as the measured total losses, demonstrating again a good accuracy of the relatively straightforward loss models for the VR and the DABCs intro-

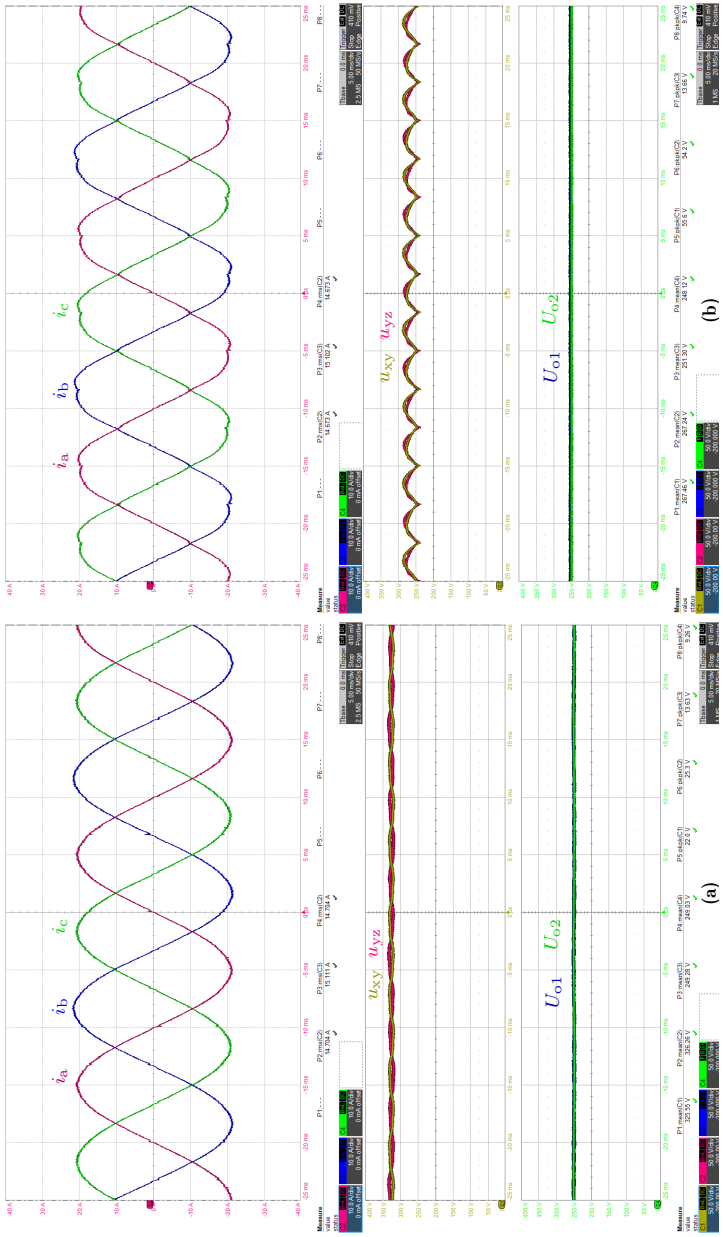


Fig. 4.25: Measured grid currents (i_a, i_b, i_c), intermediate DC-link voltages (u_{xy}, u_{yz} with $u_{xz} = u_{xy} + u_{yz}$), and output voltages (U_{o1}, U_{o2}) for $U_o = U_{o1} + U_{o2} = 500$ V and 10 kW rated output power; in **(a)** with 3/3-PWM ($U_{xz} = 640$ V) and in **(b)** with 1/3-PWM.

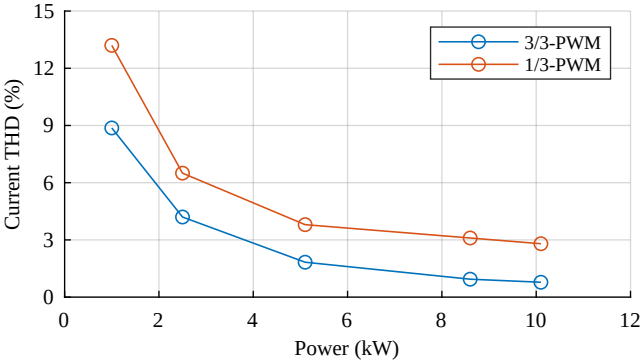


Fig. 4.26: Measured mains current THD (Yokogawa WT-1804E) for 3/3-PWM (with $U_{xz} = 640\,\text{V}$) and 1/3-PWM, respectively, in dependence of the output power and with an output voltage of $U_o = 500\,\text{V}$.

duced in **Sec. 4.3.2** and **Sec. 4.3.3**, respectively. Clearly, at the considered exemplary operating points, operating with 1/3-PWM significantly reduces the VR losses at the expense of a moderate increase of the DABC losses only, as also visible in the full efficiency maps shown earlier in **Fig. 4.19**, which have been obtained using the individually verified loss models of the VR and the DABCs.

4.3.5.4 Comparative Conducted EMI Pre-Compliance Tests

Finally, it is an interesting question whether changing the operating mode of the two-stage system from 3/3-PWM (for which the system has been designed) to 1/3-PWM (which, advantageously, gives higher efficiency) affects the EMI noise emissions to an extent that would require modifications of the EMI filter design. Therefore, *comparative* pre-compliance EMI measurements have been carried out. To emulate worst-case grounding conditions, the DC output midpoint is connected to earth. The coldplate, on the other hand, is tied to the intermediate DC-link midpoint; deionized water is used as a coolant.

Figs. 4.28(a)(b) show the measured conducted EMI emissions for 2.5 kW and 5 kW output power, and with 500 V output voltage. For all measurements, an external CM choke has been placed at the mains input (3×5 turns on a VAC W517-51 core resulting in 140 µH CM inductance at 500 kHz; this CM impedance could be realized in a much smaller form factor for integration into the converter). On the other hand, no housing has been placed, which would

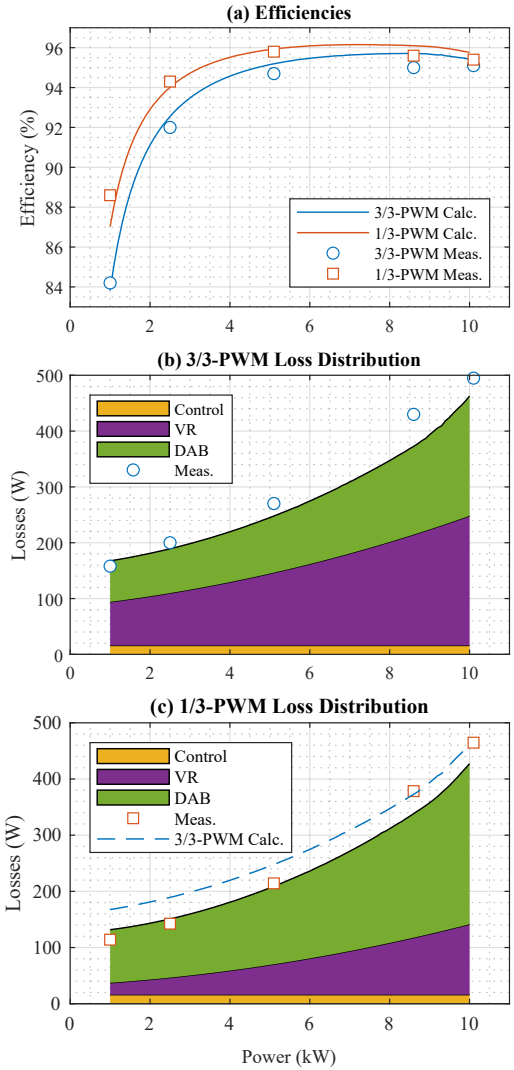


Fig. 4.27: **(a)** Calculated and measured (Yokogawa WT-1804E) efficiencies of the two-stage system with $U_o = 500\,\mathrm{V}$ and operation with 3/3-PWM ($U_{xz} = 640\,\mathrm{V}$) and 1/3-PWM, respectively. **(b)** and **(c)** show the measured total losses and the (calculated) loss distributions between the VR and the DABCs for operation with 3/3-PWM and 1/3-PWM, respectively.

help to reduce the noise emissions in the high-frequency range. Note that for both, operations with 3/3-PWM and with 1/3-PWM, the DABCs are expected to show at least some switching transitions without ZVS (see **Fig. 3.8**) and thus the selected operating point constitutes a worst-case for dv/dt-imposed emissions in the upper frequency range. The observed difference between 3/3-PWM and 1/3-PWM for frequencies above 5 MHz could well be explained by the circuit's non-idealities and component tolerances, which might allow for partial ZVS in case of 3/3-PWM.

Even though around 180 kHz, there is a minor violation of the CISPR 11 Class A limit[6], the main point of these results is *comparative* in nature: the noise emissions resulting for 3/3-PWM and 1/3-PWM operation are very similar. Hence, a system designed for 3/3-PWM can operate with 1/3-PWM without a redesign of the EMI filter.

4.4 Summary

In this chapter, different synergetic control options are evaluated, first for a two-stage EV charger module employing a three-phase boost-type PFC rectifier front-end and a novel Hybrid Quantum Series Resonant DC/DC Converter (H-QSRC) output stage, with a special focus on how to cope with the three-phase PFC rectifier stage to cover an extremely wide output voltage range. Different operating modes are demonstrated and analyzed for both stages. Subsequently, four different synergetic combinations of the PFC rectifier and the DC/DC converter control are developed. All combinations are evaluated considering the stresses on the main power components, and it can be concluded that by utilizing all degrees of freedom of the control of the individual stages and a synergetic partitioning of the overall control tasks between the stages, the required wide operating range can be covered without overdesign of any of the stages. Finally, a detailed explanation of the optimal control scheme is provided, which ensures smooth transitions between the different operating modes. Furthermore, the necessary analytical solutions, which are required for the control implementation are provided, in order to support hardware implementation of the system.

In the second part, the realization of a 10 kW two-stage EV charger module with a wide output voltage range of 200 V to 1000 V is presented, which

[6]This is because the DABC operating frequency has been lowered slightly compared to the switching frequency targeted in the original design; this could be addressed in a next design iteration by selecting a slightly lower EMI filter cutoff frequency and likely be implemented without a significant impact on the EMI filter volume.

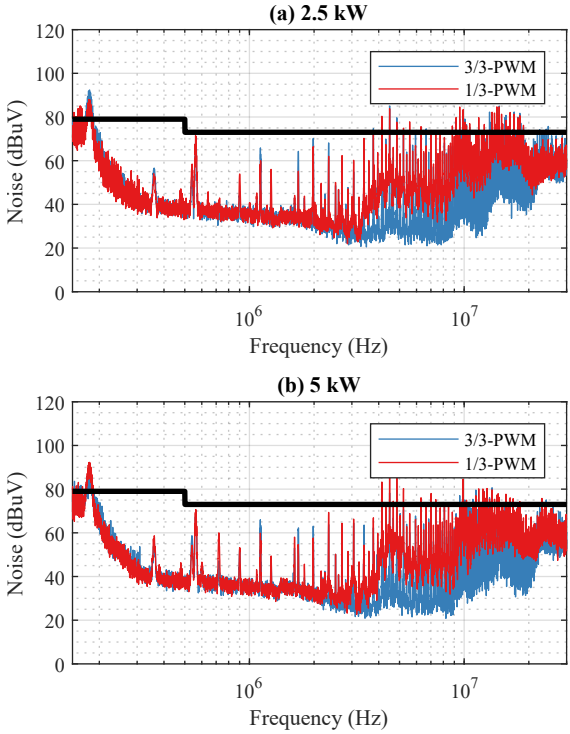


Fig. 4.28: Conducted EMI noise emission spectra of the two-stage demonstrator system for operation with 3/3-PWM (U_{xz} = 640 V) and 1/3-PWM, an output voltage of U_o = 500 V, and with **(a)** 2.5 kW output power and **(b)** 5 kW output power. A Rhode & Schwarz ESH2-Z5 three-phase LISN and a Rhode & Schwarz ESPI3 test receiver (settings: PK detector with 9 kHz resolution bandwidth (RBW), 1 ms measurement time, 0.1 % step size) have been used. The solid black line indicates the CISPR 11 Class A limit.

combines a three-level Vienna Rectifier (VR) AC/DC stage and four Dual Active Bridge Converter (DABC) modules. This, advantageously, enables a realization with latest-generation 600 V GaN power transistor technology and enables very high switching frequencies of 560 kHz for the VR and of up to 330 kHz for the DABCs, resulting thus in a flat, ultra-compact design with a power density of around 9 kW/dm^3 (about 150 W/in^3), not including the coldplate. Although, conventionally, the two stages would operate largely independently and hence the VR would switch all three bridge-legs with

high-frequency PWM (3/3-PWM), alternative synergetic operation concepts can be employed. Specifically, the DABCs can be used to shape the shared intermediate DC-link voltage such that always only *one* of the VR's three bridge-legs must operate with PWM (1/3-PWM). Whereas it is directly possible (and has been done before) to evaluate the according loss savings of the VR *alone*, a system-level analysis including *both* converter stages has been missing so far. As the optimum operating mode selection (i.e., 3/3-PWM or 1/3-PWM) depends on the operating-point-dependent loss contributions of both stages, such an analysis can only be carried out for a specific system realization. Therefore, in this work a built 10 kW charger is considered and straightforward but accurate and experimentally verified loss models are introduced for the VR and the DABCs (for which, in addition, a simplified modulation scheme is proposed). These then enable a comprehensive analysis of the optimum synergetic operation. Changing the operating mode from 3/3-PWM to 1/3-PWM gives efficiency improvements of up to about 2% for a large share of the operating points (power, output voltage). This is confirmed by running the two-stage system with 3/3-PWM and with 1/3-PWM for an output voltage of 500 V, whereby the full-load efficiency improves from 95.1% to 95.4%, respectively. Whereas a minor degradation of the mains current total harmonic distortion for 1/3-PWM must be accepted, conducted EMI pre-compliance tests confirm that changing from 3/3-PWM to 1/3-PWM operation does not necessitate significant changes of the EMI filter design. All in all, three-level VR front-ends and (cascaded) DABC isolation stages that are both realized with latest-generation 600 V GaN power transistors, and the advantageous synergetic operation of the two stages, are both very promising concepts for future highly efficient and ultra-compact EV charging solutions.

5 Conclusions and Outlook

To keep up with the rapid growth of the EV market, which will be a key contributor to reducing the carbon footprint of modern society, compact and efficient battery charging systems are of vital importance. In order to be compatible with cars from different manufacturers, a wide output voltage range is required, which poses new technical challenges on the power electronic systems. In this work, various novel approaches are investigated, where the main contributions are summarized below, followed by an outlook on future research areas.

5.1 Results and Conclusions

To cope with the wide output voltage range requirement, which spans from 200 V to 1000 V, the typical architecture of state-of-the-art EV chargers consists of two stages, including a PFC rectifier front-end, and a subsequent isolated DC/DC stage. The two stages are electrically connected through a DC-link, which typically is kept at a constant voltage for simplicity reasons even though this clearly limits the achievable performance of the system. In the recently proposed 1/3-PWM, a periodically fluctuating intermediate DC-link voltage is used, which is controlled by the DC/DC stage, whereby the PFC rectifier front-end needs to switch only one out of three bridge-legs, while still guaranteeing sinusoidal grid currents. This approach results in a significant switching loss reduction ($> 66\%$). In this work, the 1/3-PWM is evaluated under various irregular grid conditions, in order to find out whether this promising modulation can also be used in real applications. It is found that a two-stage three-phase EV charger using the 1/3-PWM can survive in

harsh environments with minor changes to the 1/3-PWM control structure and a few simple protection devices.

Furthermore, for the isolated DC/DC stage, different topological solutions are considered and compared. A novel Quantum Series Resonant Converter (QSRC) is proposed, which operates at a constant (its resonance) frequency, but is still able to step up and step down the output voltage, by applying zero-voltage intervals for integer multiples of resonant half periods on either the primary side or secondary side. In terms of operating and control principles, it is found that the combination of an outer voltage PI control and an inner hysteresis current control loop gives the best balance between control accuracy and bandwidth. A few straightforward design guidelines are developed to ensure an efficient operation with minimum effort, where the optimization procedures for the main circuit parameters are decoupled to the largest extent from the design/modeling of the components. Specifically, using certain voltage patterns, soft switching for all half-bridges can be achieved, while keeping the converter in CCM, which is required for low RMS currents, and can be ensured by properly selecting the inductance value of the resonant inductor. To assess its performance objectively, the QSRC is compared to the widely used LLC converter and the DAB converter. Both the theoretical Pareto optimization and experimental analysis show that the QSRC has clear advantages. Compared to the LLC converter, it gives similar performance while being able to maintain a constant switching frequency, independent of the voltage transfer ratio or the output power. Compared to a DAB converter, it shows efficiency advantages resulting from the low RMS currents and the ability to achieve full soft switching over the entire operating range. Two 2.5 kW hardware demonstrators, for the QSRC and the DAB converter are built, which utilize the same control board, the same switches (GaN HEMTs), and have the same volume of the magnetic components. The aforementioned theoretical findings are verified by means of these two hardware demonstrators based on various experimental measurements. To further improve the performance of the QSRC, a Hybrid Quantum Series Resonant Converter (H-QSRC) is proposed, where one two-level bridge-leg is replaced with a three-level T-type bridge-leg to increase the number of available voltage levels, such that the RMS currents are decreased and the control accuracy can be increased.

Due to the ability of the DC/DC stage to both step up and step down the input voltage, there exist different synergetic control options to employ the 1/3-PWM and the conventional modulations for the PFC rectifier stage, and the corresponding buck/boost mode of the DC/DC stage. Starting from

the combination of the two-level six-switch boost PFC rectifier and the H-QSRC, different synergetic control options are evaluated based on component stresses, while the optimal control turns out to avoid over-stressing of any of the two stages. In order to experimentally verify the theoretical findings, a 10 kW two-stage EV charger demonstrator system is built, where the PFC stage is implemented as a Vienna Rectifier, due to its better performance and lower breakdown voltage requirements for the switches compared to the two-level rectifier, such that 600 V GaN devices can be used. The DC/DC stage is implemented with four DAB converter modules, due to the faster dynamic performance of DAB converters compared to the QSRCs, which is required by the 1/3-PWM. To improve the power density of the system, GaN HEMTs are utilized for both stages, allowing to reach a power density of 9 kW/dm^3 (about 150 W/in^3), not including the coldplate-type heatsink, by increasing the switching frequency, e.g., in the VR to 560 kHz. The corresponding requirement for the high bandwidth of the control system is accomplished by an FPGA-based digital platform (Zynq-7000). The individual measurement results of the two stages validate the accuracy of the employed loss models, which are then used to derive the efficiency maps of different synergetic control options. The comparison between the efficiency maps reveals, on the one hand, that a significant efficiency improvement of the complete converter system of up to 2% can be achieved, if the 1/3-PWM is used. This is then finally verified with experimental results where the two stages are operated together. On the other hand, the boundary between 1/3-PWM and 3/3-PWM in the optimal synergetic control depends on the design of the converter stages, which also depends on the output voltage and power operating range, indicating that a detailed analysis, utilizing accurate loss models, is crucial for the considered two-stage system. For the specific design considered in this work, it may be a reasonable engineering decision to always utilize 1/3-PWM, even if it means giving up some minor loss savings, in exchange for a more straightforward implementation.

5.2 Outlook and Future Research Areas

This work focuses on the conventional charging operation of the system, where a power transfer from the three-phase mains to a load with a power factor close to 1 is considered most of the time for 1/3-PWM. With the growing adoption of EVs, future-generation chargers could potentially be used to support the grid by means of delivering power from the EV batteries to the grid (bidirectional power flow capability). The bidirectional power control has

been discussed briefly for the two-level PFC rectifier operated at 1/3-PWM, but not yet for the Vienna Rectifier topology. Hence, it is also critical to investigate the feasibility of bidirectional power flow in the Vienna Rectifier, including the necessary replacement of the diodes with power transistors. Furthermore, since three-phase voltages are not always accessible, e.g., in residential areas, the three-phase on-board chargers are also required to operate with a single-phase supply, where it might be necessary to add additional circuitry to handle the corresponding pulsating power.

The main focus of this work was on developing and testing new ideas for converter topologies. However, future research should concentrate more on the practical implementation of these proposed topologies and design concepts in hardware. For example, the realized hardware demonstrator system doesn't fully comply with the EMI standards, and a detailed EMI analysis of the combined system is missing for the two-stage charger, especially concerning the influence of the isolated DC/DC converter on the system noise spectrum and also the EMI filter design, which is important, since the DC/DC stage can be operated with a different switching frequency compared to the Vienna Rectifier. Furthermore, since the work mainly focuses on how the 1/3-PWM can improve the efficiency of a 3/3-PWM system, which proves to be significant, it is worth investigating how the 1/3-PWM influences the design of the whole system, which is shortly discussed for the selection of the turns ratio of the DAB converter, but can be extended to other aspects, i.e., on the selection of the components, or operation parameters like switching frequency, to fully exploit its potential.

Appendix

A

Turn-Off Delay Compensation in the Vienna Rectifier for High Switching Frequency Operation

Two of the main challenges of operating the VR with a high switching frequency of 560 kHz are the practical implementation of the current control and the modulation. The need for a fast current control loop requires an FPGA-based implementation as discussed in **Sec. 4.3.5**. However, the turn-off delay caused by the GaN transistor's parasitic capacitances, C_{oss}, has to be compensated for, particularly for duty cycles close to unity, to limit low-frequency current distortions.

As discussed in [126] for silicon superjunction (Si-SJ) MOSFETs, the challenge at higher switching frequencies (e.g., 560 kHz as opposed to 100 kHz) is that the *effective* duty cycle (i.e., the voltage-time area that is actually applied at the VR bridge-leg switch node) is distorted by the turn-on, and, particularly, the turn-off delays of the power semiconductors (in addition to the propagation delays of the gate drive and control signal isolation stages). This ultimately leads to an increase of the mains current THD. The turn-on of wide-bandgap (WBG) devices, assuming that the gate is driven by a strong gate driver and the gate loop PCB layout is adequate, can, in a first step, be assumed to have a much smaller effect than the device's turn-off process (considering also the missing turn-on of a complementary transistor in case of current commutation to a diode path). This is because the turn-off delay depends on the charge stored in the parasitic output capacitance, and, in particular, also on the switched current, i.e., it varies over the grid period as the phase current does.

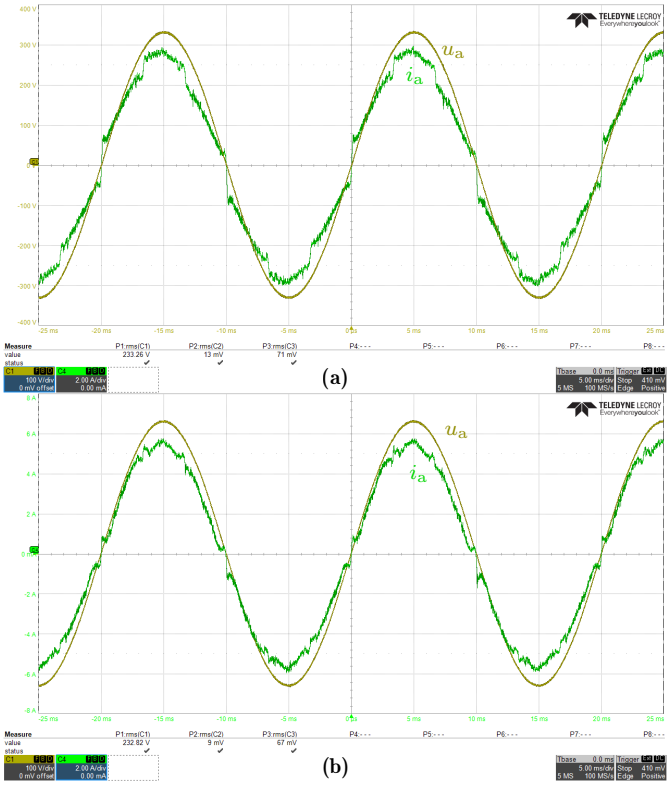


Fig. A.1: Measured mains phase currents with 3/3-PWM and 2.5 kW output power, in **(a)** without and in **(b)** with the turn-off delay compensation activated.

Although for the same $R_{\mathrm{ds,on}}$, GaN devices feature a much more linear output capacitance and smaller output charge than their Si-SJ counterparts [127, 128], it is still necessary to adjust the duty cycles of the VR to compensate for the above-mentioned current-dependency of the turn-off delay and the thus introduced voltage-time area error. In the case at hand this is achieved by shortening the on-time of the switches by

$$t_{\mathrm{comp},i} = \min\left(50\,\mathrm{ns}, 50\,\mathrm{nsA}^2 \cdot i_i^{-2}\right), \tag{A.1}$$

where t_{comp} is the on-time compensation in nanoseconds, and i_i is the (measured) input current of phase i. As in [126], the equation parameters are obtained empirically.

Tab. A.1: Improvement of Mains Current THD by Turn-Off Delay Compensation.

Power	Modulation	Uncompensated	Compensated
2.5 kW	3/3-PWM	7.3 %	4.2 % (-3.1 %)
	1/3-PWM	9.0 %	6.5 % (-2.5 %)
5 kW	3/3-PWM	4.2 %	3.8 % (-0.4 %)
	1/3-PWM	2.9 %	1.8 % (-1.1 %)

Fig. A.1 depicts measured mains current waveforms without and with turn-off delay compensation, which clearly show the reduction of the low-frequency distortions. This is reflected by a corresponding improvement in the mains current THD, as listed in **Tab. A.1**. Note that the compensation is advantageous for both operations with 3/3-PWM and with 1/3-PWM.

Bibliography

[1] UNFCCC, "The Paris Agreement," 2015. [Online]. Available: https://unfccc.int/process-and-meetings/the-paris-agreement/the-paris-agreement

[2] IPCC, "Summary for policymakers," in *Global Warming of 1.5℃. An IPCC Special Report on the impacts of global warming of 1.5℃ above pre-industrial levels and related global greenhouse gas emission pathways, in the context of strengthening the global response to the threat of climate change, sustainable development, and efforts to eradicate poverty.* Cambridge, UK, and New York, NY, USA: Cambridge University Press, 2018, pp. 3–24.

[3] H. Desing and R. Widmer, "Reducing climate risks with fast and complete energy transitions: Applying the precautionary principle to the Paris agreement," *Environ. Res. Lett.*, vol. 16, no. 12, 2021.

[4] A. Cornet, J. Conzade, P. Schaufuss, S. Schenk, A. Tschiesner, R. Hensley, P. Hertzke, R. Heuss, K. von Laufenberg, and T. Möller, "Why the automotive future is electric," 2021. [Online]. Available: https://www.mckinsey.com/industries/automotive-and-assembly/our-insights/why-the-automotive-future-is-electric

[5] Council of the European Union, "Fit for 55: Why the EU is toughening CO2 emission standards for cars and vans - Consilium," 2021. [Online]. Available: https://www.consilium.europa.eu/en/infographics/fit-for-55-emissions-cars-and-vans/

[6] P. Hertzke, N. Müller, S. Schenk, and T. Wu, "The global electric-vehicle market is amped up and on the rise," 2018. [Online]. Available: https://www.mckinsey.com/industries/automotive-and-assembly/our-insights/the-global-electric-vehicle-market-is-amped-up-and-on-the-rise

[7] IEA, "Global electric vehicle outlook 2022," 2022. [Online]. Available: https://www.iea.org/reports/global-ev-outlook-2022

[8] U.S. Exec. Order No. 14037, "Strengthening American leadership in clean cars and trucks," Aug. 2021.

[9] S. Heldmann, F. Nägele, and F. Richter, "Shaping the future of fast-charging EV infrastructure," 2021. [Online]. Available:

https://www.mckinsey.com/capabilities/operations/our-insights/shaping-the-future-of-fast-charging-ev-infrastructure

[10] R. Hensley, K. Laczkowski, T. Möller, and D. Schwedhelm, "Can the automotive industry scale fast enough?," 2022. [Online]. Available: https://www.mckinsey.com/industries/automotive-and-assembly/our-insights/can-the-automotive-industry-scale-fast-enough

[11] P. Kampshoff, A. Kumar, and S. Sahdev, "America's electric-vehicle charging infrastructure," Apr. 2022. [Online]. Available: https://www.mckinsey.com/industries/public-and-social-sector/our-insights/building-the-electric-vehicle-charging-infrastructure-america-needs

[12] M. Safayatullah, M. T. Elrais, S. Ghosh, R. Rezaii, and I. Batarseh, "A comprehensive review of power converter topologies and control methods for electric vehicle fast charging applications," *IEEE Access*, vol. 10, pp. 40 753–40 793, 2022.

[13] H. Karneddi, D. Ronanki, and R. L. Fuentes, "Technological overview of onboard chargers for electrified automotive transportation," in *Proc. IEEE Ann. Conf. Ind. Electron. Soc. (IECON)*, 2021.

[14] I. Aghabali, J. Bauman, P. J. Kollmeyer, Y. Wang, B. Bilgin, and A. Emadi, "800-V electric vehicle powertrains: Review and analysis of benefits, challenges, and future trends," *IEEE Trans. Transp. Electrific.*, vol. 7, no. 3, pp. 927–948, Sep. 2021.

[15] Hyundai, "Ioniq 5 technology | ECO - Hyundai Worldwide," 2021. [Online]. Available: https://www.hyundai.com/worldwide/en/eco/ioniq5/technology

[16] Kia Global, "The Kia EV6," 2021. [Online]. Available: https://worldwide.kia.com/int/ev6

[17] Porsche, "Taycan, Taycan 4S, Turbo and Turbo S – The battery - Porsche Taycan," 2022. [Online]. Available: https://media.porsche.com/mediakit/taycan/en/porsche-taycan/die-batterie

[18] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2151–2169, 2013.

[19] Tesla, "Onboard charger," 2021. [Online]. Available: https://www.tesla.com/support/home-charging-installation/onboard-charger

[20] Porsche, "The charging process - Taycan Cross Turismo," 2022. [Online]. Available: https://media.porsche.com/mediakit/taycan-cross-turismo/en/taycan-cross-turismo/the-charging-process

[21] A. Khaligh and M. Dantonio, "Global trends in high-power on-board chargers for electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 68, no. 4, pp. 3306–3324, 2019.

[22] H. Tu, H. Feng, S. Srdic, and S. Lukic, "Extreme fast charging of electric vehicles: A technology overview," *IEEE Trans. Transp. Electrific.*, vol. 5, no. 4, pp. 861–878, Dec. 2019.

[23] CharIN, "Whitepaper: Megawatt charging system (MCS)," Nov. 2022. [Online]. Available: https://www.charin.global/technology/knowledge-base/

[24] X. Wang, C. Jiang, B. Lei, H. Teng, H. K. Bai, and J. L. Kirtley, "Power-loss analysis and efficiency maximization of a silicon-carbide MOSFET-based three-phase 10-kW bidirectional EV charger using variable-DC-bus control," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 880–892, 2016.

[25] O. Zayed, A. Elezab, A. Abuelnaga, and M. Narimani, "A dual-active bridge converter with a wide output voltage range (200-1000 V) for ultra-fast DC-connected EV charging stations," *IEEE Transactions on Transportation Electrification (Early Access)*, 2022.

[26] M. Antivachis, J. Azurza Anderson, D. Bortis, and J. W. Kolar, "Analysis of a synergetically controlled two-stage three-phase DC/AC buck-boost converter," *CPSS Trans. Power Electron. Appl.*, vol. 5, no. 1, pp. 34–53, 2020.

[27] J. Wang, Y. Zhang, M. Elshaer, W. Perdikakis, C. Yao, K. Zou, Z. Xu, and C. Chen, "Nonisolated electric vehicle chargers: Their current status and future challenges," *IEEE Electrific. Mag.*, vol. 9, no. 2, pp. 23–33, Jun. 2021.

[28] J. Yuan, L. Dorn-Gomba, A. D. Callegaro, J. Reimers, and A. Emadi, "A review of bidirectional on-board chargers for electric vehicles," *IEEE Access*, vol. 9, pp. 51 501–51 518, 2021.

[29] A. M. Haidar and K. M. Muttaqi, "Behavioral characterization of electric vehicle charging loads in a distribution power grid through modeling of battery chargers," *IEEE Trans. Ind. Appl.*, vol. 52, no. 1, pp. 483–492, 2016.

[30] D. Zhang, M. Guacci, M. Haider, D. Bortis, J. W. Kolar, and J. Everts, "Three-phase bidirectional buck-boost current DC-link EV battery charger featuring a wide output voltage range of 200 to 1000V," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE USA)*, Detroit, MI, USA, 2020, pp. 4555–4562.

[31] R. Gadelrab, Y. Yang, B. Li, F. Lee, and Q. Li, "High-frequency high-density bidirectional EV charger," in *Proc. IEEE Transp. Electrification Conf. Expo. (ITEC)*, 2018, pp. 687–694.

[32] J. Azurza Anderson, M. Haider, D. Bortis, J. W. Kolar, M. Kasper, and G. Deboy, "New synergetic control of a 20kW isolated VIENNA rectifier front-end EV battery charger," in *Proc. 20th IEEE Workshop Control Modeling Power Electron. (COMPEL)*, Toronto, Canada, Jun. 2019.

[33] D. Menzi, D. Bortis, and J. W. Kolar, "Three-phase two-phase-clamped boost-buck unity power factor rectifier employing novel variable DC link voltage input current control," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo. (PEAC)*, Shenzhen, China, Nov. 2018.

[34] Texas Instruments, "Design guide: TIDM-02013 7.4-kW EV/HEV bidirectional on-board charger reference design with GaN," 2022. [Online]. Available: www.ti.com

[35] Wolfspeed, "6.6kW high power density bi-directional EV on-board charger," 2021. [Online]. Available: https://www.wolfspeed.com/knowledge-center/article/6-6kw-high-power-density-bi-directional-ev-on-board-charger/

[36] UUGreenPower, "UR100020-SW: 20kW wide range constant power charging module," 2023. [Online]. Available: https://www.uugreenpower.com/20kW-Wide-Range-Constant-Power-Charging-Module.html#pro3

[37] B. S. Jacobson and E. N. Holmansky, "Methods and apparatus for three-phase inverter with reduced energy storage," U.S. Patent 7,839,023, Nov., 2010.

[38] W. W. Chen, R. Zane, and L. Corradini, "Isolated bidirectional grid-tied three-phase AC – DC power conversion using series-resonant converter modules and a three-phase unfolder," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9001–9012, Dec. 2017.

[39] W. W. Chen, B. Riar, and R. Zane, "Battery integrated modular multi-function converter for grid energy storage," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE USA)*, Portland, OR, Sep. 2018, pp. 2157–2163.

[40] A. Blinov, D. Zinchenko, J. Rabkowski, G. Wrona, and D. Vinnikov, "Quasi single-stage three-phase filterless converter for EV charging applications," *IEEE Open J. Power Electron.*, vol. 3, pp. 51–60, 2022.

[41] K. Oguchi, E. Ikawa, and Y. Tsukiori, "A three-phase sine wave inverter system using multiple phase-shifted single-phase resonant inverters," in *Proc. IEEE Ind. Appl. Soc. Annu. Meet.*, Seattle, WA, Oct. 1990, pp. 1125–1131.

[42] K. Taniguchi, Y. Ogino, and H. Irie, "PWM technique for power MOSFET inverter," *IEEE Trans. Power Electron.*, vol. 3, no. 3, pp. 328–334, Jul. 1988.

[43] A. Hava, R. Kerkman, and T. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan. 1999.

[44] P. Lürkens, M. Wendt, T. Duerbaum, and H. van der Broeck, "3-phase solar converter circuit and method," U.S. Patent 7,539,029B2, May, 2009.

[45] K. Rigbers, S. Schroder, R. DeDoncker, P. Lurkens, M. Wendt, and U. Boke, "High-efficient soft-switching converter for three-phase grid connections of renewable energy systems," in *Proc. Int. Conf. Power Electon. Drive Syst.*, Kuala Lumpur, Malaysia, Nov. 2005, pp. 246–250.

[46] H. Fujita, "A three-phase voltage-source solar power conditioner using a single-phase PWM control method," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE USA)*, San Jose, CA, USA, Sep. 2009, pp. 3748–3754.

[47] Q. Lei and F. Z. Peng, "Space vector pulsewidth amplitude modulation for a buck–boost voltage/current source inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 266–274, 2014.

[48] M. Jantsch and C. W. G. Verhoeve, "Inverters with three phase output and without electrolyte capacitor for improved lifetime, efficiency and

costs of grid connected systems," in *Proc. 14th Europ. Photovoltaic Solar Energy Conf.*, Barcelona, Spain, June 1997, pp. 2198–2200.

[49] Y. Li, J. Azurza Anderson, J. Schafer, D. Bortis, J. W. Kolar, and J. Everts, "Control and protection of a synergetically controlled two-stage boost-buck PFC rectifier system under irregular grid conditions," in *Proc. 9th IEEE Int. Power Electron. Motion Control Conf. (IPEMC/ECCE Asia)*, Nanjing, China, Nov. 2020, pp. 422–429.

[50] H. Qamar, H. Qamar, N. Korada, and R. Ayyanar, "Control and performance of 240°-clamped space vector PWM in three-phase grid-connected photovoltaic converters under adverse grid conditions," *IEEE Trans. Ind. Appl.*, vol. 58, no. 6, pp. 7408–7420, 2022.

[51] T. B. Soeiro and P. Bauer, "Three-phase unidirectional quasi-single-stage delta-switch rectifier + DC-DC buck converter," in *Proc. 45th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Lisbon, Portugal, Oct. 2019, pp. 3479–3484.

[52] J. Xu, T. B. Soeiro, Y. Wu, F. Gao, Y. Wang, H. Tang, and P. Bauer, "A carrier-based two-phase-clamped DPWM strategy with zero-sequence voltage injection for three-phase quasi-two-stage buck-type rectifiers," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5196–5211, May 2022.

[53] S. K. Mazumder and R. Huang, "A high-power high-frequency and scalable multi-megawatt fuel-cell inverter for power quality and distributed generation," in *Proc. Int. Conf. Power Electron., Drives, Energy Syst.*, New Delhi, India, Dec. 2006.

[54] V. K. Kanakesh, D. B. Yelaverthi, A. Ghoshal, A. K. Rathore, and R. Mahanty, "Analysis and implementation of closed-loop control of electrolytic capacitor-less six-pulse DC-link bidirectional three-phase grid-tied inverter," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 539–550, Jan. 2018.

[55] Y. Li, J. Schäfer, D. Bortis, J. W. Kolar, and G. Deboy, "Optimal synergetic control of a three-phase two-stage ultra-wide output voltage range EV battery charger employing a novel hybrid quantum series resonant DC/DC converter," in *Proc. 21st IEEE Workshop Control Model. Power Electron. (COMPEL)*, Aalborg, Denmark, Nov. 2020.

[56] Infineon Technologies AG, *Chargers from 50 kW to 350 kW*, [Online]. Available: www.infineon.com.

[57] J. W. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system," *IEEE Transactions on Industry Applications*, vol. 27, no. 6, pp. 1063–1075, 1991.

[58] C. Charumit and V. Kinnares, "Discontinuous SVPWM techniques of three-leg VSI-fed balanced two-phase loads for reduced switching losses and current ripple," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2191–2204, 2015.

[59] F. Liu, K. Xin, and Y. Liu, "An adaptive discontinuous pulse width modulation (DPWM) method for three phase inverter," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 1467–1472.

[60] K. Mino, H. Matsumoto, S. Fujita, Y. Nemoto, D. Kawasaki, R. Yamada, and N. Tawada, "Novel bridgeless PFC converters with low inrush current stress and high efficiency," in *Proc. of the International Power Electronics Conference (IPEC)*, vol. 131, no. 5, 2011, pp. 700–707.

[61] *Electric vehicle conductive charging system - Part 21-1 Electric vehicle on-board charger EMC requirements for conductive connection to AC/DC supply*, IEC 61851-21-1, 2017.

[62] *Electric vehicle conductive charging system - Part 21-2: Electric vehicle requirements for conductive connection to an AC/DC supply - EMC requirements for off-board electric vehicle charging systems*, IEC 61851-21-2, 2018.

[63] *Electromagnetic compatibility (EMC) - Part 6-1: Generic standards - Immunity standard for residential, commercial and light-industrial environments*, IEC 61000-6-1, 2016.

[64] *IEEE Recommended practice and requirements for harmonic control in electric power systems*, IEEE Std 519, 2014.

[65] *Electromagnetic compatibility (EMC) - Part 2-4: Environment - Compatibility levels in industrial plants for low-frequency conducted disturbances*, IEC 61000-2-4, 2002.

[66] *Electromagnetic compatibility (EMC) - Part 4-13: Testing and measurement techniques - Harmonics and interharmonics includingmains signalling at a.c. power port, low frequency immunity tests*, IEC 61000-4-13, 2015.

[67] D. O. Boillat, F. Krismer, and J. W. Kolar, "EMI filter volume minimization of a three-phase, three-level T-type PWM converter system," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2473–2480, 2017.

[68] R. West, "Common mode inductors for EMI filters require careful attention to core material selection," in *Proc. of the Intern. Conf. on Power Conversion and Intelligent Motion (PCIM Europe)*, 1996.

[69] D. O. Boillat, F. Krismer, and J. W. Kolar, "Ground current control scheme for back-to-back three-phase T-type rectifier and inverter systems," *IEEJ Transactions on Industry Applications*, vol. 138, no. 11, pp. 1–5, 2018.

[70] M. L. Heldwein, L. Dalessandro, and J. W. Kolar, "The three-phase common-mode inductor: Modeling and design issues," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 8, pp. 3264–3274, 2011.

[71] M. J. Nave, "On modeling the common mode inductor," in *Proc. of the IEEE International Symposium on Electromagnetic Compatibility*, 1991, pp. 452–457.

[72] *Electromagnetic compatibility (EMC) - Part 4-11: Testing and measurement techniques - Voltage dips, short interruptions and voltage variations immunity tests for equipment with input current up to 16 A per phase*, IEC 61000-4-11, 2020.

[73] *Electromagnetic compatibility (EMC) - Part 4-34: Testing and measurement techniques - Voltage dips, short interruptions and voltage variations immunity tests for equipment with input current more than 16 A per phase*, IEC 61000-4-34, 2005.

[74] R. Erickson, M. Madigan, and S. Singer, "Design of a simple high-power-factor rectifier based on the flyback converter," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 1990, pp. 792–801.

[75] Vishay General Semiconductor, *General Purpose Plastic Rectifier*, [Online]. Available: www.vishay.com.

[76] STMicroelectronics, *SMCJxxA, SMCJxxCA 1500 W TVS in SMC*, [Online]. Available: www.st.com.

[77] S. Santoso, M. F. McGranaghan, R. C. Dugan, and H. W. Beaty, *Electrical power systems quality*, 2nd ed. McGraw-Hill Education, 1996.

[78] *Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test*, IEC 61000-4-5, 2017.

[79] *Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test*, IEC 61000-4-4, 2012.

[80] Analog Devices, Inc, *AN-1161 Application note: EMC-Compliant RS-485 Communication Networks*, [Online]. Available: www.analog.com.

[81] C. F. M. Carobbi and A. Bonci, "Elementary and ideal equivalent circuit model of the 1, 2/50-8/20 μs combination wave generator," *IEEE Electromagnetic Compatibility Magazine*, vol. 2, no. 4, pp. 51–57, 2013.

[82] Z. Mi, W. Jianguo, L. Yang, X. Nianwen, S. Zhen, C. Junjie, and F. Chunhua, "Development of coupling and decoupling network for surge immunity test," in *Proc. of the Intern. Conf. on High Voltage Engineering and Application*, 2008, pp. 190–193.

[83] *Low-voltage surge protective devices - Part 12: Surge protective devices connected to low-voltage power systems - Selection and application principles*, IEC 61643-12, 2020.

[84] *Low-voltage electrical installations - Part 1: Fundamental principles, assessment of general characteristics, definitions*, IEC 60364-1, 2005.

[85] Wikipedia contributors, *Earthing system — Wikipedia, The Free Encyclopedia*, [Online]. Available: en.wikipedia.org/wiki/Earthing_system.

[86] Littelfuse, Inc., *Application Note: High power semiconductor crowbar protector for AC power line applications*, 2019. [Online]. Available: www.littelfuse.com.

[87] Littelfuse, Inc., *Protection thyristor semiconductor product catalog*, 2017. [Online]. Available: www.littelfuse.com.

[88] Littelfuse, Inc., *Transient suppression devices and principles*, 1998. [Online]. Available: www.littelfuse.com.

[89] Littelfuse, Inc., *Metal-oxide varistors (MOVs): Radial lead varistors ultra-MOV varistor series*, 2019. [Online]. Available: www.littelfuse.com.

[90] Littelfuse, Inc., *SIDACtor protection thyristors: High surge current series - DO-214*, 2016. [Online]. Available: www.littelfuse.com.

[91] Littelfuse, Inc., *SIDACtor SPICE models*, 2020. [Online]. Available: www.littelfuse.com.

[92] M. Falahi, H.-M. Chou, M. Ehsani, L. Xie, and K. L. Butler-Purry, "Potential power quality benefits of electric vehicles," *IEEE Transactions on Sustainable Energy*, vol. 4, no. 4, pp. 1016–1023, 2013.

[93] S. Kampl, Infineon Technologies AG, *Topologies in on-board charging*, White Paper, May 2020.

[94] J. W. Kolar, H. Ertl, and F. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system," in *Proc. IEEE Ind. Appl. Soc. Ann. Meeting (IAS)*, Seattle, WA, USA, 1990, pp. 502–512 vol.1.

[95] M. Leibl, "Three-phase PFC rectifier and high-voltage generator," Ph.D. dissertation, ETH Zurich, 2017.

[96] B. Yang, F. Lee, A. Zhang, and G. Huang, "LLC resonant converter for front-end DC/DC conversion," in *Proc. Appl. Power Electron. Conf. (APEC)*, vol. 2, 2002, pp. 1108–1112 vol.2.

[97] X. Fang, H. Hu, Z. J. Shen, and I. Batarseh, "Operation mode analysis and peak gain approximation of the LLC resonant converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1985–1995, 2012.

[98] E. S. Glitz and M. Ordonez, "MOSFET power loss estimation in LLC resonant converters: Time interval analysis," *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 11 964–11 980, 2019.

[99] D. Menzi, Z. Yu, J. Huber, and J. W. Kolar, "Comparative evaluation of ultra-lightweight buck-coost DC-DC converter topologies for future eVTOL aircraft," in *Proc. 23rd Workshop Control Modeling Power Electron. (COMPEL)*, Tel Aviv, Israel, Jun. 2022.

[100] ELEKTRISOLA, "Selection of litz wire parameters," 2022. [Online]. Available: https://www.elektrisola.com/en/Litz-Wire/Info#single-wire-diameter-versus-range-of-frequency

[101] C. R. Sullivan and R. Y. Zhang, "Simplified design method for litz wire," in *Proc. Appl. Power Electron. Conf. (APEC)*, 2014, pp. 2667–2674.

[102] G. C. Knabben, G. Zulauf, J. Schäfer, J. W. Kolar, M. J. Kasper, J. A. Anderson, and G. Deboy, "Conceptualization and analysis of a next-generation ultra-compact 1.5-kW PCB-integrated wide-input-voltage-range 12v-output industrial DC/DC converter module," *Electronics*, vol. 10, no. 17, pp. 1–30, 2021.

[103] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, 2012.

[104] R. W. A. A. DeDoncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan. 1991.

[105] F. Krismer, "Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies," Doctoral Thesis, ETH Zurich, Switzerland, 2010.

[106] M. Kasper, R. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.

[107] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, July 2012.

[108] G. B. Joung, C. T. Rim, and G. H. Cho, "Integral cycle mode control of the series resonant converter," *IEEE Transactions on Power Electronics*, vol. 4, no. 1, pp. 83–91, Jan. 1989.

[109] G. B. Joung, C. T. Rim and G. H. Cho, "Modeling of quantum series resonant converters-controlled by integral cycle mode," in *Conf. Record of the IEEE Industry Applications Society Annual Meeting*, Oct. 1988, pp. 821–826.

[110] W. Kwon and G. Cho, "Optimum quantum sequence control of quantum series resonant converter for minimum output voltage ripple," *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 74–84, 1994.

[111] M. Castilla, L. Garcia de Vicuna, J. Matas, J. Miret, and J. C. Vasquez, "A comparative study of sliding-mode control schemes for quantum

series resonant inverters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 9, pp. 3487–3495, 2009.

[112] P. Bidan, M. Valentin, and L. Martinez, "Modeling and current-mode control of a zero-current switching resonant converter used for AC sine voltage generation," in *Proc. of IEEE Power Electronics Specialist Conference (PESC)*, 1993, pp. 636–640.

[113] A. Hillers, D. Christen, and J. Biela, "Design of a highly efficient bidirectional isolated LLC resonant converter," in *Proc. 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, Novi Sad, Serbia, 2012, pp. DS2b.13–1–DS2b.13–8.

[114] T. Guillod, J. Huber, F. Krismer, and J. W. Kolar, "Computation and analysis of dielectric losses in MV power electronic converter insulation," in *Proc. 18th IEEE Workshop Control Modeling Power Electron. (COMPEL)*, Stanford, CA, USA, 2017, pp. 1–8.

[115] R. M. Burkart and J. W. Kolar, "Comparative $\eta - \rho - \sigma$ pareto optimization of Si and SiC multilevel dual-active-bridge topologies with wide input voltage range," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5258–5270, July 2017.

[116] J. W. Kolar and F. C. Zach, "A novel three-phase utility interface minimizing line current harmonics of high-power telecommunications rectifier modules," *IEEE Trans. Ind. Electron.*, vol. 44, no. 4, pp. 456–467, Aug. 1997.

[117] D. Zhang, C. Leontaris, J. Huber, and J. W. Kolar, "Optimal synergetic control of high-efficiency three-phase/level boost-buck voltage DC-link very wide output voltage range EV charger," TechRxiv preprint, Mar. 13, 2023, doi: 10.36227/techrxiv.22227889.v1.

[118] D. Zhang, D. Cao, J. Huber, and J. W. Kolar, "Three-phase synergetically controlled current DC-link AC/DC buck-boost converter with two independently regulated DC outputs," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4195–4202, Apr. 2023.

[119] M. J. Kasper, J. Azurza Anderson, G. Deboy, Y. Li, M. Haider, and J. W. Kolar, "Next generation GaN-based architectures: From 240W USB-C adapters to 11kW EV on-board chargers with ultra-high power density and wide output voltage range," in *Proc. Power Conv. Intell. Motion Conf. (PCIM Europe)*, Nuremberg, Germany, May 2022.

[120] M. Kasper, D. Bortis, and J. W. Kolar, "Scaling and balancing of multi-cell converters," in *Proc. Int. Power Electron. Conf. (IPEC/ECCE Asia)*, Hiroshima, Japan, May 2014, pp. 2079–2086.

[121] P. S. Niklaus, J. W. Kolar, and D. Bortis, "100 kHz large-signal bandwidth GaN-based 10 kVA Class-D power amplifier with 4.8 MHz switching frequency," *IEEE Transactions on Power Electronics*, vol. 38, no. 2, pp. 2307–2326, 2023.

[122] Infineon Technologies AG, "GaN EiceDRIVER ™ product family single-channel functional and reinforced isolated gate-drive ICs for high-voltage enhancement-mode GaN HEMTs," 2021. [Online]. Available: www.infineon.com

[123] P. S. Niklaus, J. Azurza Anderson, D. Bortis, and J. W. Kolar, "Ultra-high bandwidth GaN-based Class-D power amplifier for testing of three-phase mains interfaces of renewable energy systems," in *Proc. Int. Renewable Energy Res. Appl. Conf. (ICRERA)*, Brasov, Romania, Nov. 2019, pp. 615–622.

[124] D. Cittanti, C. Gammeter, J. Huber, R. Bojoi, and J. W. Kolar, "A simplified hard-switching loss model for fast-switching three-level T-type SiC bridge-legs," *Electronics*, vol. 11, no. 11, p. 1686, 2022.

[125] K. Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis," *IEEE Trans. Ind. Electron.*, vol. 49, no. 1, pp. 186–196, Feb. 2002.

[126] M. Hartmann, H. Ertl, and J. W. Kolar, "On the tradeoff between input current quality and efficiency of high switching frequency PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3137–3149, 2011.

[127] G. Deboy, O. Haeberlen, and M. Treu, "Perspective of loss mechanisms for silicon and wide band-gap power devices," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 2, pp. 89–100, June 2017.

[128] M. Escudero, M.-A. Kutschak, N. Fontana, N. Rodriguez, and D. P. Morales, "Non-linear capacitance of Si SJ MOSFETs in resonant zero voltage switching application," *IEEE Access*, vol. 8, pp. 116 117–116 131, 2020.

Curriculum Vitae

Personal Information

Name	Yunni Li
Date of birth	September 19, 1994
Nationality	Chinese
Citizen of	Wuhan, China
Contact	li@lem.ee.ethz.ch

Education

2019 – 2023	Doctorate, ETH Zurich Power Electronic Systems Laboratory (PES)
2016 – 2019	MSc ETH , ETH Zurich Information Technology and Electrical Engineering
2015 – 2016	BEng, University of Birmingham, United Kingdom Electronic and Electrical Engineering (Double-Degree Program)
2012 – 2015	BEng, Huazhong University of Science and Technology (HUST), China Electrical Engineering and Automation (Double-Degree Program)