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Highly Integrated Ultra-Compact Three-Port Converter Systems for Automotive Applications

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Wisdom is not a product of schooling but of the lifelong attempt to acquire it.
– Albert Einstein

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Abstract

In recent years, the demand for electric vehicles (EVs) has virtually exploded worldwide, as the ever increasing environmental pollution and the finiteness of fossil fuels persuaded most people to switch to more environmental-friendly means of transportation. Consequently, the share of EVs in the automotive market significantly increased, whereby many companies, which were previously focusing on conventional vehicles with combustion engines, now start to enter this interesting market segment. Hence, the increasing number of competing suppliers, in combination with the large demand for affordable EVs, led to an enormous cost pressure on the product development of all different kinds of components in EVs, as e.g. the various power electronic systems. Hence, the whole system and each of its components need to be optimized with respect to manufacturing costs and power density in order to develop competitive products.
In today's EVs, a high level of integration is therefore a key criterion for electrical systems, as one single device should cover as many functionalities as possible, whereby the device utilization is maximized and the fixed costs can be reduced. Unfortunately, the overall device utilization in state-of-the-art EVs is comparably poor, as there are many devices which are only used if the car is inactive (as e.g. on-board chargers) or if the car is driving (as e.g. the DC/AC inverter motor drive), but there are hardly any devices which are operated in both situations.
From a cost and power density point of view, it would therefore be beneficial to combine two systems which are operated in different situations, such that the new integrated solution is operated almost all the time. Thereby, the total component count and, therefore, the overall cost and the power density of the energy distribution in EVs could be significantly improved.

In this work, a combined EV charger is proposed, where two individual converter systems of today's EVs are combined, namely: the 3.6 kW single-phase AC/DC auxiliary charger and the 3 kW DC/DC step-down converter, which is used to feed power from the high-voltage (HV) battery to the low-voltage (LV) DC-bus during drive mode. Hence, the combined converter system is operated in charge mode and in drive mode, whereby a much higher integration level is achieved and the manufacturing costs of the two individual converter systems can be drastically reduced.
However, the challenging specifications of the combined EV charger, as e.g. a wide output voltage range due to the HV battery (250 V…500 V) or the huge output currents in the 15 V LV bus (up to 200 A), restrict the application of

conventional converter topologies, as is exemplarily shown based on the well-known triple-active-bridge (TAB) topology. The TAB is also used to identify the main practical challenges of the proposed combined EV charger, which are finally verified by means of a 1 kW triple-active-bridge (TAB) hardware demonstrator. Subsequently, based on the findings of the TAB, two new converter topologies are developed, which are tailored to the requirements of the application at hand.

The first proposed three-port DC/DC converter topology is based on multiple interconnected series-resonant converters (SRC) and is built around a special five-winding transformer structure. In this transformer, additive and subtractive superposition of magnetic flux linkages is used to completely decouple the two power flows to the HV battery and to the LV bus, whereby these two power values can be controlled independently, which is a big advantage compared to the TAB. The control of the converter is based on simple analytical formulas, whereby the computational effort for the control hardware is minimized and a high controller bandwidth can be achieved. Furthermore, soft-switching of all power semiconductors can be ensured, whereby the converter can be operated efficiently up to high switching frequencies. In the converter port which is connected to the LV bus, a winding-integrated synchronous rectifier is used, as this circuit has been found to be particularly efficient for applications with low port voltages and large port currents. The suitability of this rectifier circuit has been experimentally verified by means of a conventional 3 kW 500 V/15 V series-resonant DC/DC step-down converter, which achieves a peak efficiency of 94.9 % and a power density of 17.9 kW/L. The capabilities of the proposed three-port topology are finally tested by means of a simple 1 kW hardware prototype with a peak efficiency of 95.8 % in charge mode operation, whereby the targeted full-load efficiency of 95 % is easily met. However, the target efficiency in drive mode has been missed by 1 %, mainly due to the inefficient PCB-winding transformer design and the resulting large currents in the HV port. For this reason, the initial transformer structure is extended by means of a sixth winding, such that operating mode dependent turns ratios are achieved and the converter efficiency in drive mode can be increased significantly. Hence, using this improved transformer structure, the efficiency target of 95 % could easily be met. The only drawback of this topology is a comparably high component count, which is why a second topology is derived, where this issue is mitigated.

The second three-port DC/DC converter topology was developed with a special focus on minimizing the number of active power components, as

well as simplifying the control of the converter system as far as possible. The topology comprises a SRC between the DC-link capacitor of an upstream PFC rectifier and the HV battery, as well as a phase-shifted full-bridge circuit equivalent in the LV port, which is magnetically connected to the same transformer core as the aforementioned SRC. The control of this three-port converter system is extremely simple and is comparable to the control complexity of a conventional buck converter, but in return, the topology relies on a variable output voltage of the upstream PFC rectifier, as the SRC is operated as a simple DC-transformer with a fixed voltage gain given by the numbers of turns of the transformer. Nevertheless, this is not really a drawback, as the power-density of the overall system could still be increased. The suitability of the topology is finally verified by means of a 3.6 kW 500 V/500 V/15 V DC/DC hardware demonstrator with a power density of 16.4 kW/L, which is only slightly lower than the 17.9 kW/L of the equivalent two-port DC/DC converter system. The hardware demonstrator easily meets the targeted efficiency requirements of 95 % in full-load operation in charge mode, where it achieves a peak efficiency of 96.6 %, as well as in partial-load operation in drive mode, where a peak efficiency of 95.5 % is achieved.

In order to further reduce the costs of the combined EV charger, not only the topology, but also the individual components of the converter system need to be optimized with respect to manufacturing costs. Consequently, a new design concept for PCB-winding inductors is proposed, where the fringing field around one or multiple (distributed) air gaps is used to partially compensate the parasitic magnetic skin and proximity fields, whereby the high-frequency conduction losses in PCB-winding inductors can be significantly reduced. Hence, the efficiency and the power density of such inductors can be increased and, more importantly, extremely cost-effective inductors can be built.
Finally, a zero-voltage-switching (ZVS) auxiliary circuit is introduced, which ensures ZVS for arbitrary switching frequencies, arbitrary port voltages, works independent of the output power, and only processes the absolute minimum of the power necessary to achieve ZVS, without increasing the control complexity of the main converter. Hence, using this simple auxiliary circuit, silicon (Si) superjunction MOSFETs can be used up to comparably high switching frequencies, whereby the more expensive GaN semiconductors could be avoided in many applications.

The conclusions of the thesis are summarizing the main findings and contributions of this work and provide an outlook on future research topics, which go hand in hand with advances in PCB manufacturing and technological improvements of wide band-gap semiconductor devices.

Kurzfassung

Im Verlauf des vergangenen Jahrzehnts ist die weltweite Nachfrage nach Elektrofahrzeugen förmlich explodiert, da die zunehmende Umweltbelastung durch den CO_2-Ausstoss konventioneller Fahrzeuge, sowie die Endlichkeit fossiler Ressourcen, immer mehr Menschen dazu bewogen haben auf umweltfreundlichere Transportmittel umzusteigen. Folglich hat der Anteil elektrifizierter Fahrzeuge am Automobilmarkt deutlich zugenommen, wodurch viele Unternehmen, welche sich zuvor auf konventionelle Fahrzeuge mit Verbrennungsmotoren fokussierten, nun auch in dieses vielversprechende Marktsegment eingestiegen sind. Die dadurch stark gestiegene Anzahl an konkurrierenden Herstellern, sowie die steigende Nachfrage nach günstigen Elektrofahrzeugen, führten zu einem immensen Kostendruck auf die Produktentwickler der verschiedenen Baugruppen in Elektrofahrzeugen, wie z. B. der verschiedenen leistungselektronischen Systeme. Aus diesem Grund muss das gesamte System und jede seiner Komponenten bezüglich Herstellungskosten und Leistungsdichte optimiert werden, damit wettbewerbsfähige Produkte entstehen können.
In heutigen Elektrofahrzeugen ist demnach ein hohes Mass an System-Integration unabdingbar, um kosteneffiziente Lösungen anzubieten. Sprich, ein einzelnes Gerät sollte so viele Funktionen wie möglich abdecken, um die Geräteausnutzung zu maximieren und die Fixkosten dadurch zu minimieren. Leider ist die Geräteauslastung in heutigen Elektrofahrzeugen relativ gering, da viele Geräte entweder nur im Ruhezustand (z. B. On-Board Ladegeräte) oder nur im Fahrbetrieb (z. B. der Motorantrieb) verwendet werden, und es kaum Systeme gibt, welche in beiden Situationen betrieben werden.
In Anbetracht einer Kostenreduzierung wäre es demnach vorteilhaft zwei bestehende Systeme, welche in unterschiedlichen Situationen betrieben werden, zu kombinieren, sodass die neue integrierte Lösung in beiden Fällen betrieben werden kann. Durch die Kombination der zwei Systeme würde die Auslastung der einzelnen Systemkomponenten erhöht, wobei die Gesamtkosten reduziert würden und die Leistungsdichte des Energieverteilsystems in Elektrofahrzeugen erheblich verbessert werden könnte.

In dieser Arbeit wird ein kombiniertes Ladegerät für künftige Elektrofahrzeuge vorgestellt, in welchem die Funktionen zweier individueller Konvertersysteme heutiger Elektrofahrzeuge kombiniert werden, nämlich die eines 3.6 kW AC/DC Hilfsladegeräts sowie die eines 3 kW DC/DC Abwärtswandlers, welcher im Fahrbetrieb den 15 V Niederspannungs-Bus (LV) mit Energie aus der Hochvolt-Batterie (HV) versorgt. Das kombinierte System wird daher

im Ladebetrieb und im Fahrbetrieb verwendet, wodurch ein bedeutend höherer Nutzungs- und Integrationsgrad erreicht wird und die Herstellkosten gegenüber den zwei ursprünglichen Systeme reduziert werden können.
Leider limitieren die herausfordernden Spezifikationen des kombinierten Ladegeräts, wie z.B. der weite Ausgangsspannungsbereich aufgrund der variablen Spannung der HV Batterie (250 V ... 500 V) oder die enormen Ausgangsströme im Niederspannungs-Bus (bis zu 200 A), die Anwendbarkeit herkömmlicher Konverter-Topologien. Dies wird beispielhaft anhand der bekannten Triple-Active-Bridge (TAB) Topologie gezeigt, welche dazu verwendet wird, die wichtigsten Herausforderungen in einer möglichen praktischen Implementierung des kombinierten Ladegeräts zu identifizieren. Die dadurch gewonnenen Einsichten werden anschliessend anhand eines experimentellen 1 kW Hardware-Demonstrators verifiziert, und werden des Weiteren dazu verwendet zwei neue Konverter-Topologien zu entwickeln, welche auf die Anforderungen des kombinierten Ladegeräts zugeschnitten sind.

Die erste vorgestellte Drei-Port DC/DC Konverter-Topologie basiert auf mehreren miteinander verbundenen Serienresonanzwandlern (SRC), welche um einen speziellen Transformator mit fünf Wicklungen angeordnet werden. In diesem Transformator werden mittels additiver und subtraktiver Überlagerung magnetischer Flussverkettungen die zwei Leistungsflüsse zur HV Batterie sowie zum LV Bus komplett voneinander entkoppelt, wodurch die Leistungsflüsse unabhängig voneinander geregelt werden können. Die Regelung des Konverters basiert auf einfachen analytischen Formeln, wodurch der Rechenaufwand in der Steuerungshardware minimiert wird und somit auch eine hohe Regelbandbreite erzielt werden kann. Des Weiteren werden alle Halbleiter weich geschaltet, wodurch ein effizienter Betrieb bis zu relativ hohen Schaltfrequenzen ermöglicht wird. Im Konverter-Port, welcher an den LV Bus angeschlossen wird, wird ein hoch-integrierter Synchrongleichrichter verwendet, da sich diese Schaltung in Anwendungen mit niedrigen Portspannungen and grossen Portströmen als besonders effizient herausgestellt hat. Dies wurde mittels eines konventionellen 3 kW 500 V/15 V Serienresonanz-DC/DC-Abwärtswandlers experimentell verifiziert, wobei der Hardware-Demonstrator eine maximale Effizienz von 94.9 % und eine Leistungsdichte von 17.9 kW/L erreicht.
Die Leistungsfähigkeit der vorgestellten Drei-Port Topologie wird schliesslich mittels eines einfachen 1 kW Hardware-Demonstrators getestet, welcher einen Volllastwirkungsgrad von 95.8 % im Ladebetrieb zeigt und dadurch die angestrebte Effizienz von 95 % unter Volllast sicher erreicht. Im Fahrbetrieb

liegt der Wirkungsgrad jedoch 1 % unter dem angestrebten Wirkungsgrad von 95 % unter Teillast, was hauptsächlich vom ineffizienten Transformatordesign und den hohen Strömen im HV Port verursacht wird. Aus diesem Grund wird eine verbesserte Transformatorstruktur vorgestellt, welche um eine sechste Wicklung erweitert wurde und damit betriebsartabhängige Windungsverhältnisse aufweist. Dadurch wird die Effizienz im Fahrbetrieb signifikant erhöht, wobei das Effizienzziel sicher erreicht werden kann.
Der einzige Nachteil dieser Topologie ist die vergleichsweise hohe Anzahl an Komponenten, welche sich negativ auf die Ausfallsicherheit des Systems auswirkt. Aus diesem Grund wird eine zweite Konverter-Topologie vorgestellt, welche mit bedeutend weniger Leistungskomponenten auskommt.

Die zweite vorgestellte Drei-Port DC/DC Konverter-Topologie wurde mit besonderem Augenmerk auf die Minimierung der Anzahl Leistungskomponenten entwickelt, ohne dabei auf eine komplexe Regelung des Konverters angewiesen zu sein. Der Konverter besteht aus einem SRC zwischen dem Zwischenkreis-Kondensator des vorgeschalteten PFC-Gleichrichters und der HV Batterie, sowie zwei phasenversetzt arbeitenden Tiefsetzstellern im LV Port, welche mittels einer separaten Wicklung an den gemeinsamen Transformatorkern angeschlossen werden. Die Regelung dieses Konverters ist sehr einfach und ist in etwa vergleichbar mit der Steuerungskomplexität eines gewöhnlichen Tiefsetzstellers, was jedoch eine variable Ausgangsspannung des vorgeschalteten PFC-Gleichrichters bedingt, da der SRC als einfacher Gleichspannungstransformator mit fester Spannungsverstärkung (entsprechend dem Windungsverhältnis des Transformators) betrieben wird. Dies ist jedoch nicht per se ein Nachteil, da das gesamte System dadurch noch leistungsdichter gebaut werden kann.
Die Eignung der vorgestellten Topologie für die Anwendung als kombiniertes Ladegerät wird schliesslich mittels eines 3.6 kW 500 V/500 V/15 V DC/DC Hardware-Demonstrators verifiziert, welcher eine Leistungsdichte von 16.4 kW/L erzielt, was nur leicht unterhalb der Leistungsdichte von 17.9 kW/L des äquivalenten Zwei-Port DC/DC Konverters liegt. Der Hardware-Demonstrator erfüllt problemlos die Effizienzanforderungen von 95 % unter Volllast im Ladebetrieb (mit einer maximalen gemessenen Effizienz von 96.6 %), sowie unter Teillast im Fahrbetrieb (mit einer maximalen gemessenen Effizienz von 95.5 %).

Um die Produktionskosten des kombinierten Ladegeräts noch weiter zu senken, werden die verschiedenen Komponenten des Konverters nochmals ge-

sondert hinsichtlich einer möglichen Kostenreduktion betrachtet. Dabei wird beispielsweise ein neuartiges Designkonzept für Induktivitäten mit leiterplattenintegrierten Wicklungen vorgestellt, welches das magnetische Streufeld um einen oder mehrere Luftspalte verwendet, um die parasitären magnetischen Skin- und Proximity-Felder innerhalb der Wicklung partiell zu kompensieren. Durch diese Kompensation werden die Hochfrequenz-Leitverluste stark reduziert, wodurch die Leistungsdichte und die Effizienz dieser äusserst kostengünstigen Induktivitäten signifikant erhöht werden kann, und sie für industrielle Anwendungen äusserst attraktiv werden.
Zum Schluss wird eine Hilfsschaltung vorgestellt, welche das weiche Schalten von Halbleitern in Resonanzwandlern garantiert, unabhängig von der Schaltfrequenz, der angelegten Spannung und der momentanen Ausgangsleistung. Die Hilfsschaltung arbeitet dabei nur mit der absolut minimal notwendigen Leistung um das weiche Schalten zu garantieren, wodurch der Betrieb der Schaltung extrem effizient wird. All dies wird erreicht, ohne die Regelung des Hauptkonverters zu beeinflussen oder zu erschweren, da die Hilfsschaltung selbstregulierend operiert. Unter Verwendung dieser einfachen Hilfsschaltung können Superjunction-Silizium-MOSFETs bis zu vergleichsweise hohen Schaltfrequenzen eingesetzt werden, wodurch der Einsatz von teuren Gallium-Nitrid-Halbleitern erst für sehr hohe Schaltfrequenzen notwendig wird.

Abschliessend werden die wesentlichen Resultate und Beiträge der Arbeit zusammengefasst, sowie weitere Forschungsthemen diskutiert, welche primär von der Weiterentwicklung der Leiterplattenherstellung- und -technologie, sowie dem Fortschritt in der Wide-Bandgap Halbleiter-Technologie abhängen.

Abbreviations

AC	Alternating Current
BCM	Boundary Conduction Mode
CC	Constant Current
CCM	Continuous Conduction Mode
CFFC	Compensating Fringing Field Concept
CM	Charge Mode
CNC	Computerized Numerical Control
CP	Constant Power
CV	Constant Voltage
DAB	Dual Active Bridge
DC	Direct Current
DCM	Discontinuous Conduction Mode
DM	Drive Mode
EV	Electric Vehicle
FEM	Finite Element Method
FET	Field-Effect Transistor
GaN	Gallium Nitride
HB	Half-Bridge
HEMT	High-Electron-Mobility Transistor
HF	High Frequency
HV	High Voltage
iGSE	Improved General Steinmetz Equation
ISOP	Input-Series Output-Parallel
LLC	LLC Resonant Converter
LV	Low Voltage
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MPMC	Multi-Port Multi-Cell
OBC	On-Board Charger
PCB	Printed Circuit Board
PFC	Power Factor Correction
PPB	Power Pulsation Buffer
PSFB	Phase-Shifted Full-Bridge
RMS	Root Mean Square
Si	Silicon
SRC	Series-Resonant Converter
SSW	Soft Switching
TAB	Triple Active Bridge

TCM	Triangular Current Mode
TIM	Thermal Interface Material
ZCC	Zero-Current-Crossing
ZCD	Zero-Current-Detection
ZCS	Zero-Current-Switching
ZVS	Zero-Voltage-Switching

Contents

1 Introduction

The awareness of continuously increasing emissions of carbon dioxide, combined with the finite fuel resources, has intensified the search for alternative energy sources in the past decades. Hence, in order to obtain a sustainable energy utilization, a reduction of today's global fossil fuel combustion is inevitable [1]. As the amount of environmental pollution caused by road transport substantially contributes to the global carbon emissions, a general trend towards greater electrification in transportation has emerged in the recent years [2]. Hence, driven by the increasing environmental awareness of the end customers and the resulting steadily growing demand for electric vehicles (EVs), an exceedingly competitive market evolved, especially in the automotive sector with its enormous commercial potential. The low achievable profit margins in this area demand for more and more cost-effective solutions, while at the same time better performances need to be achieved. Consequently, each component of the vehicle needs to be optimized in terms of cost, efficiency and power density in order to develop competitive products. Besides the mechanical drive train, the most important components in state-of-the-art EVs are the various power electronic converter systems of the energy distribution grid, as e.g. battery chargers, DC/AC inverters and DC/DC step-down converters, as illustrated in Fig. 1.1, based on a typical power system architecture in an EV. This energy distribution grid is discussed in the following in more detail and possible improvements are investigated.

In order to compete with the short refueling times of conventional vehicles with combustion engines, the limited storage capacity of today's EVs built-in Li-ion batteries requires high-power high-performance chargers, which are either placed on-board the EV, which is quite expensive, or are stationary installed as so-called fast-charging stations. Nowadays, these fast-charging

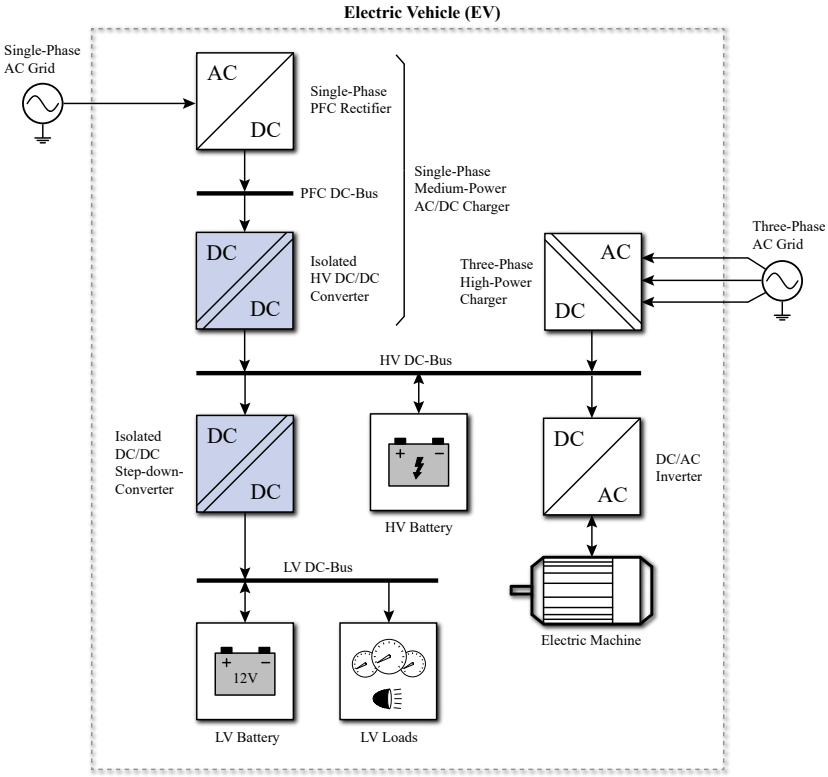


Fig. 1.1: Typical electric power system architecture in an electric vehicle, with the single-phase AC/DC-charger and the isolated DC/DC step-down converter (both blue-shaded), which are the main topics of this work.

stations achieve a peak power of up to 350 kW [3, 4], or in other words, a charge rate of up to 130 km in 5 min [5], whereby the disadvantage of long charging times of EVs is practically gone. Unfortunately, the fast-charging infrastructure is still being developed in most countries, which is why an alternative on-board charging system is required, which allows to charge the EV either at home or on the go, without special charging stations. For this reason, a small 3.6 kW on-board charger (OBC) is usually employed in today's EVs, which can be used to charge the vehicle-internal high-voltage (HV) battery, directly from the widely accessible single-phase AC mains (cf. Fig. 1.1) [6]. The HV battery, for its part, is the main energy storage of the vehicle and supplies both, the HV load (electric machine) as well as the low-voltage (LV) loads through additional converter systems. The aforementioned OBC comprises two independent converter stages, namely a single-phase PFC rectifier supplying the PFC DC-bus, followed by a galvanically isolated DC/DC converter, which adapts the output voltage of the PFC rectifier to the HV DC-bus voltage, which depends on the momentary charge-level of the HV battery. However, due to its low power rating, this charger is mainly used in emergency situations, where the remaining charge of the HV battery is not sufficient to reach the next fast-charging station. Hence, as this charger is on-board, it is carried around all the time, even though it is hardly ever operated and is therefore considered as "dead" volume with an extremely low component utilization. From an economical point of view, the rare use of this auxiliary charging unit and the limited available space in an EV, demand for extremely low cost and high power density, while the efficiency of this system plays only a subordinate role.

The various LV loads in an EV, as e.g. the board-computer, lights and the sound system, are connected to the LV DC-bus, which is buffered by its own small LV battery. However, as previously mentioned, during normal (drive) operation, the required power of the LV loads is provided by a galvanically isolated DC/DC step-down converter, which feeds the LV bus directly from the aforementioned HV battery (cf. Fig. 1.1) [7]. Thus, considering the operating states of the two blue-shaded converter systems, it can be noted that only one of them is operating at a time. Hence, either the charger feeds power from the AC grid to the HV battery and the LV bus is only marginally loaded, or while driving the car, the DC/DC step-down converter is operating and the AC/DC charger is idle mode. This inevitably yields suboptimal use of space and a poor power density of the car-internal power system. For this reason, a combined charger/step-down converter would be optimal, which covers both

functionalities, can be used in both operating modes and therefore reduces the total cost and volume of the energy distribution network.

In this thesis, the possibility and feasibility of such a combined charger/step-down converter is investigated, which allows for using the scarce space in an EV more efficiently. At the same time, the integration of both systems into a single converter promises reduced manufacturing costs due to the shared use of its components.
In the following, the most important specifications of the investigated converter systems are summarized, which are nowadays used in industrial applications.

1.1 Specifications of the Investigated Converter Systems

The main specifications for a combined OBC and isolated DC/DC step-down converter are listed in Tab. 1.1 and Tab. 1.2. Especially the wide voltage variation of the HV DC-bus (which is originating from the charge-level dependent battery voltage) and the large output currents in the LV DC-bus, yield challenging design constraints, whereby special attention needs to payed on the latter, as it is in general extremely difficult to handle large currents in standard PCBs. Furthermore, if large currents and low voltages are combined in one converter port, a very low characteristic output impedance of this port results, whereby even the smallest parasitic components in the converter usually have a huge impact on the converter performance. However, this will be explained in more detail in the course of this thesis.
Based on the given power ratings in Tab. 1.1, there are two different converter

	AC Grid	HV Bus	LV Bus
Voltage Range	80…275 V_{rms}	250…500 V	10.5…15 V
Maximum Current	16 A_{rms}	12 A	200 A
Frequency	45…65 Hz	-	-
Power Factor	>98 %	-	-
Maximum Power	3.6 kW	3.6 kW	3 kW

Tab. 1.1: Specifications of the electrical parameters of the combined charger/step-down converter.

	V_{AC}	I_{AC}	V_{HV}	V_{LV}	I_{LV}	η
Charge Mode	230 V_{rms}	16 A_{rms}	500 V	14.5 V	<20 A	>95 %
Drive Mode	-	-	500 V	14.5 V	60...100 A	>95 %

Tab. 1.2: Efficiency requirements for the system in the different operating modes.

systems in the energy distribution network of conventional EVs (cf. Fig. 1.2a), with a total power capability of 3.6 kW (OBC) + 3 kW (step-down converter) = 6.6 kW. However, as already mentioned, the total power flow in the two systems never exceeds the limit of a single converter system, due to their alternating operation. To simplify somewhat, a 6.6 kW system has to be built, even though the total power flow never exceeds half of its power rating. This inevitably yields a low power density of the total energy distribution network, which is why these two systems should ideally be merged into a single 3.6 kW device.
In the next section, different possible topological solutions for such a combined charger/step-down converter are investigated, based on existing literature, state-of-the-art solutions and simple calculations.

1.2 Topology Analysis

Starting with the conventional solution of today's EVs, the main specifications and requirements for each of the two converter systems are derived, which are then used to investigate and compare the different topological solutions for a combined charger/step-down converter system, as shown in Fig. 1.2b-g.

The converter structure, which is usually employed in state-of-the-art EVs, is shown in Fig. 1.2a, as the node of the flow chart. Based on this structure, the different requirements for both converter stages (OBC and step-down converter) are analyzed, which will finally lead to the benchmark system of this application.
The AC/DC charger (OBC) has to provide galvanic isolation between the single-phase AC grid and the HV DC-bus, requiring at least one isolation element, as. e.g. a transformer, between the two reference potentials. In addition, a power factor correction (PFC) rectifier must be used to comply with the required power factor specification. At last, the charger needs to be able to operate with different charging methods as for example constant-

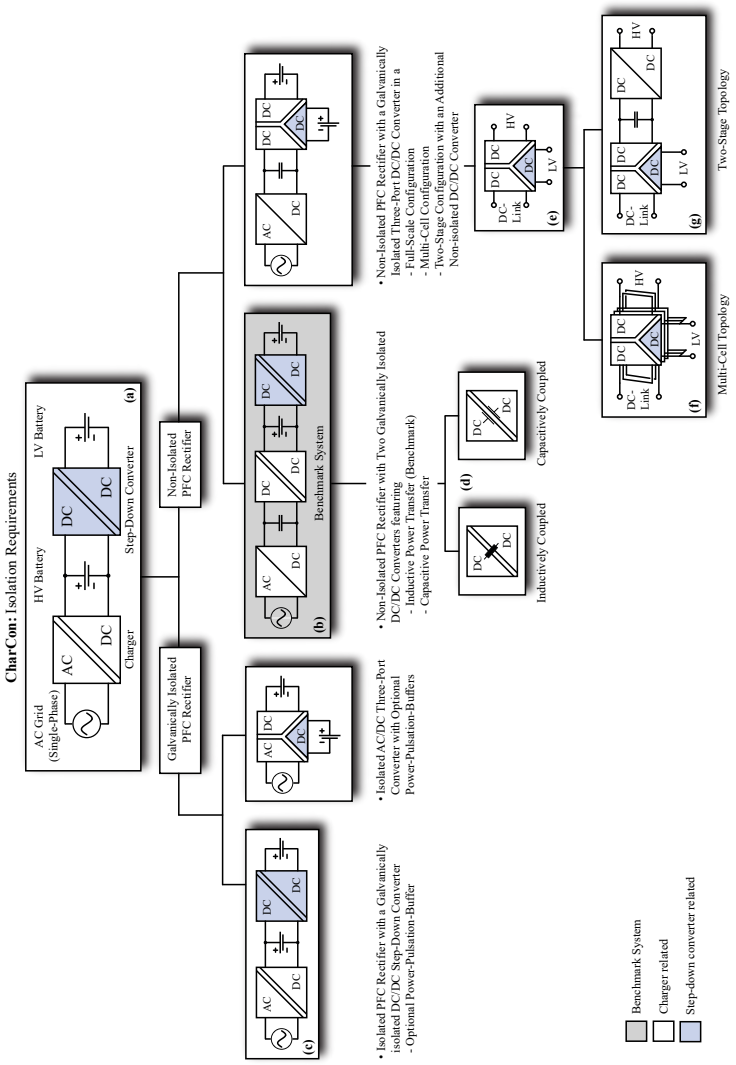


Fig. 1.2: Topological overview of the different possible converter topologies, which can be used for the combined charger/step-down converter.

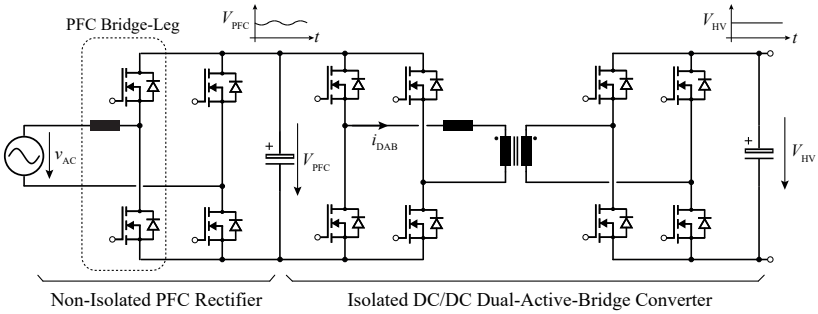


Fig. 1.3: Benchmark system of the single-phase on-board charger consisting of a non-isolated PFC rectifier (single bridge-leg) followed by a galvanically isolated dual-active bridge (DAB) converter (cf. Fig. 1.2b).

current (CC), constant-voltage (CV) or constant-power (CP).
Similarly to the OBC, the step-down DC/DC converter, between the HV and the LV DC-bus, needs to provide galvanic isolation between the two reference potentials for safety reasons. In this converter, especially the high step-down ratio and the large LV output currents yield challenging design constraints. However, the required isolation is the only restriction on the selected topology in this stage.

1.2.1 Benchmark System

In today's state-of-the-art EV electric distribution systems, the AC/DC charger usually consists of two different stages as shown in Fig. 1.2b (grey-shaded): A non-isolated PFC rectifier followed by a galvanically isolated DC/DC converter, which generates the required charging voltages and currents according to the selected charging method (CC, CV, CP). Fig. 1.3 shows a common topology of such a single-phase charger. The PFC rectifier consists of one or multiple interleaved boost converter bridge-legs, which can be controlled to triangular current mode (TCM) operation [8] to keep soft-switching (SSW) of the power switches over a wide input voltage and power range. This allows for high switching frequencies and therefore small passive components. However, due to the relatively high ripple os the DC-link capacitor voltage V_{PFC} and the missing galvanic isolation, an additional isolated DC/DC converter is used, which converts the PFC rectifier output voltage to a smooth desired output voltage V_{HV}. This stage is usually built as dual-active-bridge [9] (DAB) or LLC resonant converter [10]. Both topologies feature a high conversion

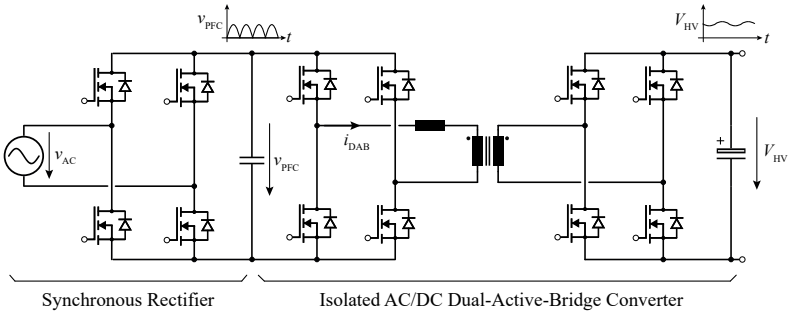


Fig. 1.4: Galvanically isolated PFC rectifier as a single-stage charger solution (cf. Fig. 1.2c).

efficiency and a high power density due to their SSW capabilities.

Instead of two independent converter stages, one might expect an increase in power density by integrating both stages into a single galvanically isolated PFC rectifier stage. The missing additional boost inductors promise a reduced total converter volume, as the transformer, with its leakage inductance, is the only left and required inductive component. The feasibility of this single-stage approach is investigated in the next section.

1.3 Isolated vs. Non-Isolated PFC Rectifier

The integration of the galvanic isolation into the PFC rectifier supersedes the use of an additional boost inductor, as the leakage inductance of the transformer can be used instead. This reduces the total amount of passive components, what might increase the power density of the system. The investigated galvanically isolated PFC rectifier consists of a synchronous rectifier stage followed by an isolated DAB converter according to Fig. 1.4. The rectified AC mains voltage is converted to the required HV DC-bus voltage V_{HV}, while keeping the input power factor as close to one as possible.
However, even though the boost inductor can be eliminated, the complete system is getting larger, mainly due to the following two reasons [11]:
On the one hand, the transformer of the single-stage solution is getting larger due to the varying AC input voltage of the converter. Hence, the transformer has to be designed for both, the maximum AC input current of 16 $\mathrm{A_{rms}}$ as well as the maximum AC input voltage of 275 $\mathrm{V_{rms}}$, yielding a total power of

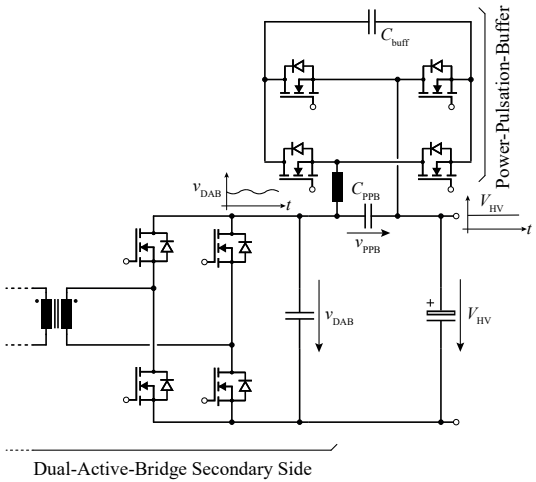


Fig. 1.5: Power-pulsation-buffer topology, used to reduce the output voltage ripple as well as the output capacitor volume.

4.4 kW instead of 3.6 kW.
On the other hand, the output capacitor of the single-stage solution needs to be much larger compared to the one of the benchmark topology, as the output power of the PFC rectifier inherently pulsating with double line frequency needs to be smoothed to achieve all three charging modes (CC, CV, CP) with a reasonable voltage and/or current ripple.
The issue of the pulsating output power could be eliminated using a power-pulsation-buffer (PPB) stage [12] in front of the output capacitor, according to Fig. 1.5. This PPB compensates the fluctuation in v_{DAB} by generating the voltage difference between v_{DAB} and V_{HV} across C_{PPB}, whereby the size of the required output capacitor substantially decreases. However, the additional circuit complexity and the still larger isolation transformer yield a worse total power density compared to the benchmark system. For this reason, topologies with galvanically isolated or integrated PFC rectifiers are considered not to be suitable for the application at hand, whereby only topologies with separate non-isolated PFC rectifier stages are considered in the course of this thesis.

So far, the galvanic isolation between the different voltage levels was always considered to be given by an appropriate transformer. However, galvanic isolation can also be achieved by using two parallel Y2 capacitors

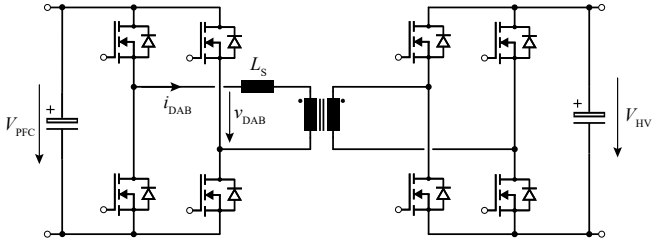


Fig. 1.6: Galvanically isolated dual-active-bridge topology with a transformer as coupling component.

instead of the transformer, which seems to be a promising solution due to the much higher energy density of capacitors compared to the one of inductive components. The feasibility of this isolation method for the application at hand, is discussed in more detail in the following section.

1.4 Inductive vs. Capacitive Power Transfer

The previously discussed DAB couples the two different voltages V_{PFC} and V_{HV} by means of a transformer, as shown in Fig. 1.6. This yields the desired galvanic isolation between the two potentials and at the same time a controllable voltage adaption according to the turns ratio of the transformer. However, if both port voltages are approximately equal ($V_{PFC} \approx V_{HV}$), the transformer has a turns ratio of 1:1 and its only purpose is to provide the galvanic isolation. This galvanic isolation can, however, also be achieved by much smaller Y2 capacitors according to Fig. 1.7 [13]. For large values of C_S and high switching frequencies, the coupling capacitors do not influence the power flow through the converter, whereby the equivalent circuits of inductively and capacitively coupled DABs are the same and the control of an inductively coupled DAB does not differ from the one of a capacitively coupled DAB. To further reduce the size of this converter stage, the capacitor values can be reduced, yielding a series-resonant converter (SRC) topology, instead of the previous DAB. However, even in the SRC, for a certain maximum required converter power, the capacitors C_S need a minimum capacitance, which depends on the port voltages, the maximum power and the switching frequency of the system. Unfortunately, there is also an upper limit for the coupling capacitance C_S, which is given by safety regulations. This limits the allowable capacitance between two different reference potentials in the system. In the application

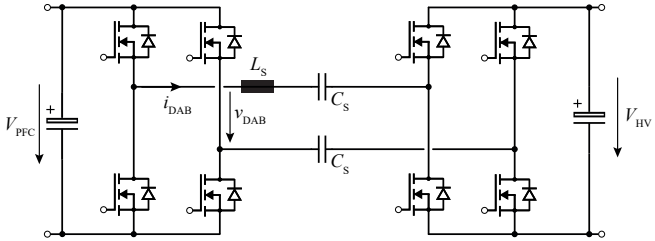


Fig. 1.7: Galvanically isolated dual-active-bridge topology with two Y2 capacitors as coupling components (cf. Fig. 1.2d).

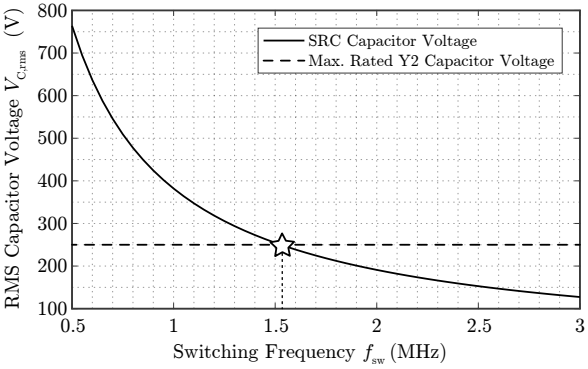


Fig. 1.8: Minimum switching frequency required for using a series-resonant converter between the DC-link and the HV DC-bus.

at hand, this value is given with 10 nF. Considering the RMS voltage limitation of Y2 capacitors (250 V_{rms}) and the required maximum converter power of 3.6 kW, a minimum required switching frequency of 1.53 MHz results (cf. Fig. 1.8).
Even for SSW operation, a switching frequency of 1.5 MHz with 650 V semiconductors is not reasonable due to the residual switching losses. In addition, compared to LLC converters with a galvanically isolating transformer, the missing magnetizing inductance in the given SRC converter restricts the converter operation to step-down operation, whereby a wide switching frequency variation would be required (cf. Fig. 1.9).
In summary, the limited allowed capacitance between the two voltage po-

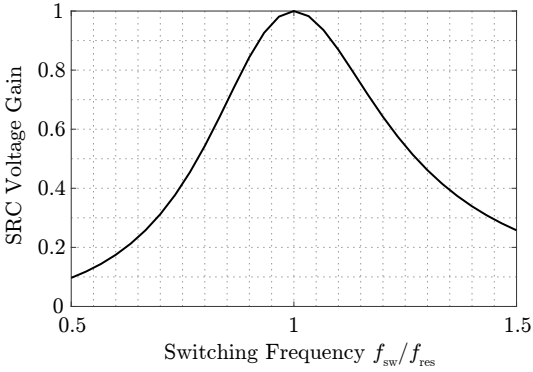


Fig. 1.9: Voltage gain of the proposed SRC for different switching frequencies.

tentials would result in a too high switching frequency in a capacitively coupled DC/DC converter for the application at hand, which is why the galvanic isolation between the different voltage levels in this thesis will rely on transformers.

1.5 Combined Use of Transformer Core

So far, neither the integration of the PFC rectifier into the galvanically isolated DC/DC converter, nor the replacement of the isolating transformer by two capacitors yielded a performance improvement compared to the initial benchmark system. Consequently, the AC/DC stage is realized with an inevitable non-isolated PFC rectifier followed by two inductively coupled DC/DC converters. The only improvement, which has not yet been investigated, is the combination of both galvanically isolated DC/DC converters into a single system.

To find a possible approach for an integration, both DC/DC converters are assumed to be DABs in the following (without loss of generality). As the power processed by one of the two converters never exceeds a certain power level, the two transformers can be combined to a single three-winding transformer with only a fraction of the initial total core cross-section area. This yields a component saving of one transformer core, one full-bridge and one HV winding compared to the initial two converter solution. Hence, a

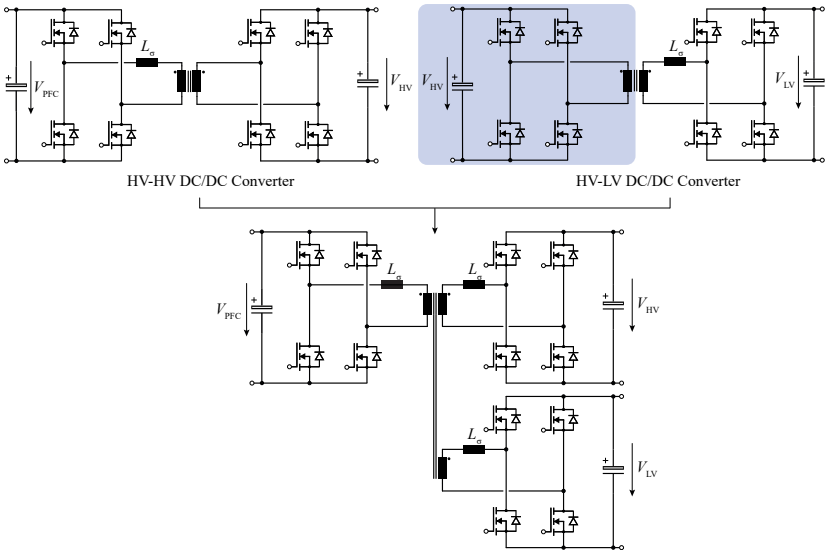


Fig. 1.10: Example derivation of a topology featuring a combined use of a transformer core, where the saved components are marked in blue (cf. Fig. 1.2e).

reduction of both, volume and costs of the converter (cf. Fig. 1.10) results.

In a second step, the control of the three winding transformer has to be investigated, as the DAB topology was only used for illustrative reasons. To do so, one has to consider the different operating modes of the converter.
In charge mode (CM), the major part of the power has to flow from the PFC rectifier port to the HV DC-bus, while a small amount of power flows from the PFC rectifier to the LV port.
In drive mode (DM), there is only power flowing between the HV and the LV port, whereas the PFC rectifier port would not be required.
The respective power flow direction requirements are summarized in Fig. 1.11.

The crucial operating mode in this application is clearly the charge mode, as both, the HV port as well as the LV port need to be able to draw an arbitrary amount of power out of the corresponding transformer winding, independent of the voltages and the power flow in the remaining system. This fact substantially reduces the number of possible converter port topologies, which are connected to the respective transformer windings.

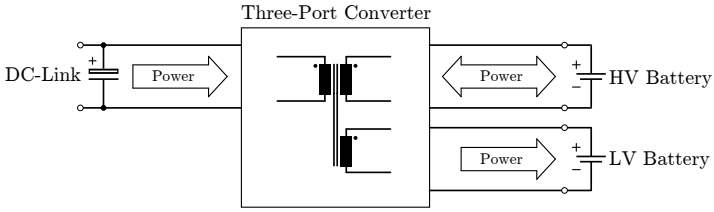


Fig. 1.11: Power flow requirements for the different converter ports.

For instance, a phase-shifted full-bridge (PSFB) converter with a current doubler rectifier on the secondary side [14] (a common and efficient converter topology for galvanically isolated power transfer and high step-down ratios) is not suitable in this application, as the passive rectification characteristic of the PSFB output makes the extraction of an arbitrary power for a given primary side voltage impossible. Hence, for a certain phase-shift φ_{PFC} at the PFC rectifier side, the rectangular voltages induced in the HV and the LV windings are directly given as $v_{\mathrm{HV}} = {}^{n_{\mathrm{HV}}}/_{n_{\mathrm{PFC}}} \cdot v_{\mathrm{PFC}}$ and $v_{\mathrm{LV}} = {}^{n_{\mathrm{LV}}}/_{n_{\mathrm{PFC}}} \cdot v_{\mathrm{PFC}}$, respectively. The resulting output voltages V_{HV} and V_{LV} can therefore be calculated as

$$V_{\mathrm{HV}} = \frac{\varphi_{\mathrm{PFC}}}{180^\circ} \cdot \frac{n_{\mathrm{HV}}}{n_{\mathrm{PFC}}} \cdot V_{\mathrm{PFC}} \qquad \text{and} \qquad V_{\mathrm{LV}} = \frac{\varphi_{\mathrm{PFC}}}{180^\circ} \cdot \frac{n_{\mathrm{LV}}}{n_{\mathrm{PFC}}} \cdot V_{\mathrm{PFC}}, \tag{1.1}$$

whereby the output voltage ratio is given by

$$\frac{V_{\mathrm{HV}}}{V_{\mathrm{LV}}} = \frac{n_{\mathrm{HV}}}{n_{\mathrm{LV}}} \tag{1.2}$$

and is independent of the control variable φ_{PFC}. Hence, as the ratio between the two port voltages V_{HV} and V_{LV} needs to adjustable according to the momentary charge-level dependent battery voltages in this application, the PSFB, or more generally, all topologies with two converter ports with a passive rectification characteristic cannot be used with this three-winding transformer approach.

The most promising and versatile conventional topology, which allows for omnidirectional and arbitrary power flow within the three-winding transformer, was found to be a triple-active-bridge (TAB) topology [15] (cf. Fig. 1.10). Hence, with only three full-bridges, three output capacitors and one three-winding transformer, it is possible to provide a galvanically isolated three-port DC/DC converter for arbitrary port voltages and power levels.

However, as will be shown in Chapter 2 of this thesis, the TAB topology is not really ideal for the specifications of the application at hand, which is why in the course of this thesis, different alternative topological solution for this three-port DC/DC converter stage are developed and are finally verified by means of hardware demonstrators. These three-port DC/DC converter systems, in combination with an upstream non-isolated PFC rectifier, could finally be used in industrial EV charging applications. However, as the design of non-isolated PFC rectifiers has already been discussed extensively in literature [16, 17], it is not part of this thesis as there is hardly any additional scientific contribution expected from analyzing this converter stage.
Furthermore, in addition to the optimization of the converter topology, the different required power components, such as e.g. transformers, inductors and semiconductors, are investigated in detail with regard to performance and manufacturing costs. Based on these considerations, new design concepts for the PCB-integrated magnetic components are derived, which achieve significantly reduced manufacturing costs, while still being power-dense and efficient.

1.6 Aims and Contributions

The objective of this work is to optimize the electric power distribution grid in today's EVs in terms of both, power density and cost. Nowadays, usually two independent converter systems are employed, namely an isolated 3.6 kW single-phase AC/DC charger and an isolated 3 kW 500 V/15 V DC/DC step-down converter, where especially the former is rarely ever used and, therefore, suffers from an extremely low component utilization. For this reason, a possible combination of these two converter systems is investigated in this work and appropriate solutions for a combined three-port charger/step-down converter are presented. Hence, after investigating the suitability of conventional three-port converter topologies for the application at hand, alternative new topologies are proposed, which aim to mitigate the arising challenges in the aforementioned conventional topologies. One of these topologies employs a newly developed transformer structure, which employs additive and subtractive superposition of magnetic flux linkages, yielding a significant simplification in terms of converter control. Furthermore, a new design concept for inductors is introduced, which allows to use PCB-integrated windings with a comparably high efficiency, whereby especially the manufacturing costs of these components are minimized.

1.6.1 Three-Port DC/DC Resonant Converter with Magnetic Flux Cancellation

The main challenge in isolated three-port DC/DC converter systems is the control of the individual output power values of the different converter ports, as a variation of one control parameter usually affects all ports at the same time, whereby the control can be extremely complex. Unfortunately, this is often the case in conventional three-port converter topologies, whereby their application in industrial products, where a simple control and high reliability are key, is usually problematic. Consequently, a decoupled power flow control should be targeted, where a change of the momentary power supplied to/drawn from a certain converter port, by no means affects the remaining output ports.
This behavior can be achieved with the proposed three-port DC/DC resonant converter topology, where a special transformer structure allows to use additive and subtractive superposition of magnetic flux linkages, whereby a perfectly decoupled power flow control is achieved. Furthermore, the initially proposed transformer structure is extended by means of an additional sub-winding, whereby operating mode dependent turns ratios are obtained. Hence, the transformer windings can be optimized independently for charge mode and drive mode operation, which is not a common feature in state-of-the-art converter topologies.
In terms of hardware design, the extremely large output currents at the LV side (up to 200 A) at comparably low voltages (10.5 V…15 V) cause serious issues, as it is hardly possible to actively switch such currents with low-voltage (LV) semiconductors in an efficient way (neither hard-switching nor soft-switching). Consequently, the only reasonable solution for this port is a synchronous rectification, as this allows the switches to be always operated under perfect soft-switching (ZVS and ZCS) conditions. However, this means that the LV port cannot take any influence on the amount of power, which is transferred to the LV DC-bus, whereby the control of the overall power distribution needs to be taken over by the remaining two converter ports. For this reason, the topologies of these two ports have been ”tailored” to the specifications of the application at hand, such that they are able to accomplish the aforementioned control task in both operating modes (charge mode and drive mode), and the targeted synchronous rectification in the LV port can be used.
The main scientific contribution to the combined EV charger/step-down converter is of course the invention of the topology and its particular control strategy, as the required upstream 3.6 kW PFC rectifier has already been

discussed extensively in literature, which is also the reason, why it is not discussed in this work any further.
The feasibility and the achievable performance of the proposed topology have been verified by means of a 1 kW 166 V/166 V/15 V DC/DC converter hardware demonstrator.

1.6.2 Three-Port DC/DC Resonant Converter with Phase-Shifted Full-Bridge Equivalent

In industrial applications the reliability of a system is key for a successful product implementation. Consequently, the circuit complexity should be reduced to a minimum, which can e.g. be achieved by minimizing the number of actively switched components (power semiconductors). For the converter topology proposed in Section 1.6.1, a comparably large number of semiconductor devices is required, in order to achieve the targeted converter operation. For this reason, a second, more industry-friendly three-port DC/DC converter topology has been developed in the course of this work, with the main goal of minimizing the total number of power switches. Furthermore, the volume of the required magnetic components could be minimized, whereby the achievable power density of the overall system is further increased.
The proposed second converter topology comprises an unregulated, isolated series-resonant converter (SRC) between the DC-link of an upstream PFC rectifier and the HV battery (also known as DC-transformer), and a phase-shifted full-bridge (PSFB) circuit equivalent in the LV port, which is connected to the transformer core of the SRC by means of a third winding. The SRC and the PSFB converter are controlled synergetically, such that they mutually benefit from each others operation, as e.g. the PSFB ensures soft-switching of the power switches of the SRC, and vice versa.
Again, in contrast to many conventional three-port topologies, a perfectly decoupled power flow control is achieved and the control of the converter is as simple as the one of a conventional non-isolated buck converter. Furthermore, the circuit complexity is reduced to a minimum, which facilitates its implementation in a potential industrial product.
Even though the unregulated SRC requires a PFC rectifier with a variable output voltage, whereby usually larger inductors in the PFC rectifier result, the overall volume of the magnetic components in the converter system is not increased significantly if the proposed PCB-winding integrated inductors are employed. Hence, the proposed topology allows to build cost-effective, power-dense converter systems which are extremely simple to control.

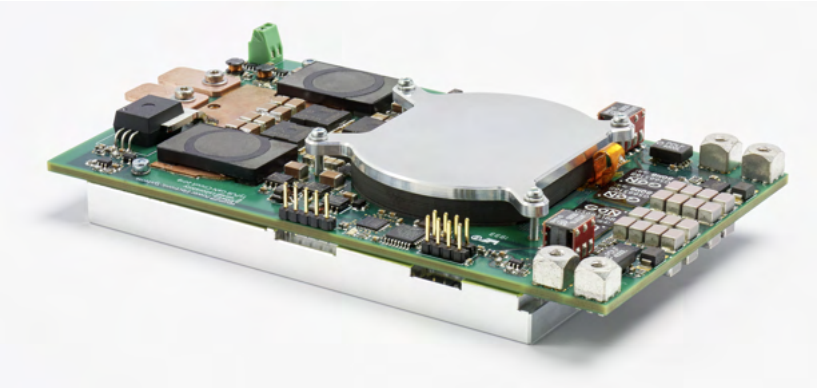


Fig. 1.12: Hardware demonstrator of the 3.6 kW 500 V/500 V/15 V three-port DC/DC resonant converter with a phase-shifted full-bridge equivalent circuit in the LV port.

The feasibility and the achievable performance of the proposed topology have been verified by means of a 3.6 kW 500 V/500 V/15 V DC/DC hardware demonstrator (cf. Fig. 1.12).

1.6.3 Compensating Fringing-Field Concept for PCB-Winding Inductors

Besides the selection of an optimal topology for a certain application, an optimal implementation of the individual power components is equally important for reducing the manufacturing costs and for increasing the power density of a converter system. The most voluminous components in conventional power electronic systems are usually the magnetic components, such as e.g. the transformers and the inductors, which are also quite expensive, due to the required wire-wrapping process of conventional wire-wound magnetics. In order to avoid the wire-wrapping process, the windings of these components are ideally integrated into the converter printed-circuit-board (PCB), whereby the overall manufacturing costs are significantly reduced. However, especially a PCB integration of inductor windings usually leads to very high high-frequency (HF) conduction losses, due to the pronounced proximity effect between vertically aligned PCB copper tracks. For this reason, a design concept for PCB-winding inductors has been developed in the course of this thesis, where the fringing field around the air gap of an inductor core is used to compensate the adverse magnetic skin and proximity fields within the

PCB-winding, yielding significantly reduced HF losses.
This compensating fringing field concept (CFFC) cannot only be used in inductors, but can be employed in all applications, where the AC resistance of a copper track with a large HF current should be minimized. Furthermore, the horizontal current distribution in a foil conductor can be shaped arbitrarily by utilizing an appropriate multi-air-gap arrangement, according to the aforementioned CFFC. This might be of particular advantage, if the current should be forced to flow on a predefined path in a large copper plane.
However, in this work, the CFFC is mainly used for inductor applications, and the effectiveness of the concept has been verified by means of multiple hardware prototypes.

1.7 List of Publications

Key insights presented in this thesis have already been published or will be published in international scientific journals, conference proceedings, or presented at workshops. The publications created as part of this thesis, or also in the scope of other related projects, are listed below.

1.7.1 Journal Papers

- J. Schäfer, D. Bortis and J. W. Kolar, "Novel Highly Efficient/Compact Automotive PCB-Winding Inductors Based on the Compensating Air-Gap Fringing Field Concept," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9619-9633, September 2020. DOI: 10.1109/TPEL.2020.2969295.
- J. Schäfer and J. W. Kolar, "Zero-Voltage-Switching Auxiliary Circuit for Minimized Inductance Requirement in Series-Resonant DC/DC Converter Systems," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6469-6479, November 2020. DOI: 10.1109/TPEL.2020.3038996.
- J. Schäfer, D. Bortis and J. W. Kolar, "Three-Port DC/DC Converter Topology with a Transformer Structure Employing Additive and Subtractive Superposition of Flux Linkages," *IEEE Transactions on Power Electronics*, in preparation for publication, March 2021. DOI: n/a.
- J. Schäfer and J. W. Kolar, "Three-Port DC/DC Converter Topology Comprising a Series-Resonant Converter and a Phase-Shifted Full-Bridge Equivalent," *IEEE Transactions on Power Electronics*, under revision, November 2020. DOI: n/a.

1.7.2 Conference Papers

- J. Schäfer, D. Bortis, and J. W. Kolar, "Multi-Port Multi-Cell DC/DC Converter Topology for Electric Vehicle's Power Distribution Networks," in *Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, USA, July 2017. DOI: 10.1109/COMPEL.2017.8013326.

- J. Schäfer, D. Bortis, and J. W. Kolar, "Optimal Design of Highly Efficient and Highly Compact PCB-Winding Inductors," in *Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Padova, Italy, June 2018. DOI: 10.1109/COMPEL.2018.8460166.

1.7.3 Workshops and Seminars

- J. Schäfer, D. Bortis, and J. W. Kolar, "Design of Highly Efficient and Compact PCB-Winding Inductors for Automotive Applications," presented at the *ECPE Magnetic Components in Power Electronics Workshop*, Grenoble, France, February 2020.

- J. Schäfer, D. Bortis, and J. W. Kolar, "Introduction of the CFFC-Compensating Fringing Field Concept and its Application in PCB Inductors," presented at the *PSMA Power Magnetics @ High Frequency Workshop*, New Orleans, USA, May 2020.

1.7.4 Patents

- J. Schäfer, D. Bortis, and J. W. Kolar, "Isolated DC/DC Converter for Controlling Power Flows Between Three DC Terminals," European, US, and Chinese Patent Application No. WO002018192754A1, US020200076311A1, CN000110506383A, filed Mar. 27, 2018, published Oct. 25, 2018.

- J. Schäfer, D. Bortis, and J. W. Kolar, "Transformer for a Three-Port Voltage Converter, Three-Port Voltage Converter and Method for Transmitting Electrical Power," European Patent Application No. WO002019110314A1, filed Nov. 22, 2018, published Jun. 13, 2019.

- J. Schäfer, D. Bortis, and J. W. Kolar, "Inductive Component and High-Frequency Filter Device," European Patent Application No. WO002019179749A1, filed Mar. 1, 2019, published Sep. 26, 2019.

- J. Schäfer, D. Bortis, and J. W. Kolar, "Transformer, Voltage Converter and Method for Transmitting Electric Power," European Patent Application No. WO002019174916A1, filed Feb. 27, 2019, published Sep. 19, 2019.

1.7.5 Further Scientific Contributions

- G. Knabben, J. Schäfer, L. Peluso, J. W. Kolar, M. Kasper, and G. Deboy, "New PCB-Winding "Snake-Core" Matrix Transformer for Ultra-Compact Wide DC Input Voltage Range Hybrid B+DCM Resonant Converter Server Power Supply," in *Proc. of the 2nd IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Shenzhen, China, November 2018.

- G. Knabben, G, Zulauf, J. Schäfer, and J. W. Kolar, "Wide-Input-Voltage, Multi-kW DC-DC Converters with Hybrid Boundary/Discontinuous Mode Control," in *Proc. of the 35th IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, USA, March 2020.

- Y. Li, J. Schäfer, D. Bortis, J. W. Kolar, "Optimal Synergetic Control of a Three-Phase Two-Stage Ultra-Wide Output Voltage Range EV Battery Charger Employing a Novel Hybrid Quantum Series Resonant DC/DC Converter," in *Proc. of the 21st IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Denmark, June 2020.

1.8 Thesis Outline

According to the goals and contributions mentioned above, the content of the thesis is divided into six main chapters and conclusions. All the chapters can be read independently since the interdependencies have been reduced to the strict minimum.

- **Chapter 2** first investigates the advantages and drawbacks of a well-known conventional three-port DC/DC converter topology for application as combined EV charger, namely, the triple-active-bridge (TAB) converter. Based on the findings of these investigations, different alternative TAB-based solutions are proposed, as e.g. a multi-cell converter system or the use of a matrix transformer, whereby all these solutions have significant drawbacks, if a possible implementation in an industrial product is considered. The challenges arising in real hardware

implementations of the TAB converter topology for the given specifications, are finally verified by means of a 1 kW hardware demonstrator. This chapter is partially based on [18].

- **Chapter 3** proposes a PCB-winding inductor design concept, which utilizes the fringing field around a single or multiple air gaps to partially compensate the parasitic magnetic skin and proximity fields in an inductor winding, whereby extremely low HF conduction losses can be achieved. The proposed compensating fringing field concept (hereinafter referred to as CFFC) allows for designing cost-effective and power-dense PCB-winding inductors, which is extremely important in industrial applications with high production quantities. The suitability and effectiveness of the CFFC is finally verified by means of multiple hardware demonstrators. This chapter is adapted from [19] and [20].

- **Chapter 4** analyzes the suitability of a series-resonant converter topology for the application at hand, and especially the winding-integration of the synchronous rectifier of the low-voltage (LV) port, whereby minimized termination losses of the LV winding can be achieved. This is done by means of a 3 kW 500 V/15 V two-port series-resonant DC/DC converter, as usually employed in today's EVs between the HV battery and the LV bus (cf. Fig. 1.2a). At the same time, the in-system performance of a CFFC-based PCB-winding inductor is investigated, as the series-resonant inductor is designed according to the guidelines which are introduced in Chapter 3. The theoretical findings of this chapter are finally experimentally verified by means of the aforementioned 3 kW 500 V/15 V hardware demonstrator.

- **Chapter 5** proposes a new three-port DC/DC resonant converter topology, which is based on a five-winding transformer structure, where additive and subtractive superposition of magnetic flux linkages is used, such that a perfectly decoupled power flow control can be achieved. Furthermore, a concept featuring operating mode dependent turns ratios is introduced, whereby the efficiency of the transformer in both operating modes (charge mode and drive mode) can be optimized independently. Besides the comparably large number of power switches, the topology is perfectly suitable for the application as combined EV charger, as its operation is based on simple analytical formulas, which can easily be implemented in a DSP. The suitability of the proposed converter topology is experimentally verified by means of a simple 1 kW hardware demonstrator, where the main design targets are a high flexibility with

respect to interchangeability of the inductive components, as well as an easy access to the most important waveform measurements.

- **Chapter 6** presents another three-port DC/DC resonant converter topology, which was developed with special focus on reducing the number of power semiconductors, in order to maximize the reliability of the converter system and, at the same time, reduce the auxiliary costs due to the various gate drivers and their required auxiliary supplies. The converter comprises a conventional series-resonant converter stage in the main power path between the PFC rectifier and the HV port, whereby in the third LV converter port a phase-shifted full-bridge circuit equivalent is used, which allows to arbitrarily connect/disconnect the output inductors of the LV port to/from the LV winding. Consequently, the two converter parts supplying the HV and the LV port can be operated individually, whereby the two output ports are perfectly decoupled. Furthermore, a synergetic control is proposed, whereby the LV converter port is used to guarantee ZVS of the PFC rectifier and the HV port power semiconductors to further increase the efficiency of the converter. The suitability of the proposed topology is finally verified by means of a 3.6 kW 500 V/500 V/15 V hardware demonstrator, which easily meets the targeted efficiency requirements of the application at hand.

- **Chapter 7** investigates the suitability of a zero-voltage-switching (ZVS) auxiliary circuit, which allows for using cost-effective superjunction silicon MOSFETs up to comparably high switching frequencies. The proposed circuit ensures ZVS for arbitrary switching frequencies, arbitrary port voltages, works independent of the output power, only processes the absolutely necessary power to achieve ZVS, and ensures perfectly synchronized primary- and secondary-side switch-node voltages in series-resonant converters. Furthermore, the proposed auxiliary circuit does not at all increase the control complexity of the overall converter system, as it is inherently controlled by means of the circuit design. Hence, only the dead time of the power semiconductors needs to be slightly adapted, which, however, has no impact on the actual converter operation. The performance and the effectiveness of the ZVS auxiliary circuit is finally experimentally verified by means of two hardware demonstrators with different power semiconductors (Si and GaN).

- **Chapter 8** concludes the thesis and briefly summarizes the main contributions and key findings. In addition, an outlook on possible future research is provided.

2

Conventional Three-Port DC/DC Converter Topologies

Chapter Abstract

In this chapter, different solutions for the three-port DC/DC converter stage are analyzed, which are all based on the conventional triple-active-bridge (TAB) converter topology. Starting with a short derivation of the characteristics of the TAB, the arising challenges in the design of a TAB for the specifications of the application at hand are discussed, and different possible adaptions of the topology are investigated. Amongst others, a two-stage converter solution is investigated, where a conventional non-isolated step-down converter is connected in between the HV port of the TAB and the HV battery, in order to reduce the voltage range, which needs to be covered by the TAB itself. Furthermore, a multi-cell approach is investigated, where multiple smaller TAB-cells are connected in a beneficial way. Finally, a 1 kW hardware demonstrator is built, in order to experimentally verify the derived findings.

2.1 Triple-Active-Bridge Converter

The triple-active-bridge (TAB) converter has been considered as the most versatile and most promising conventional topology for a three-port DC/DC converter, with a requirement for bidirectional power flow in the high-voltage (HV) port, as well as widely varying port voltages. The topology consists of a three-winding transformer, which is directly connected to three independent full-bridges, each consisting of four power switches $S_{X,y}$, where $X \in \{\text{A,B,C}\}$ and $y \in \{\text{a,b,c,d}\}$ (cf. Fig. 2.1). These full-bridges are used to generate rectangular voltage waveforms v_X, with arbitrary duty cycles D_X and mutual

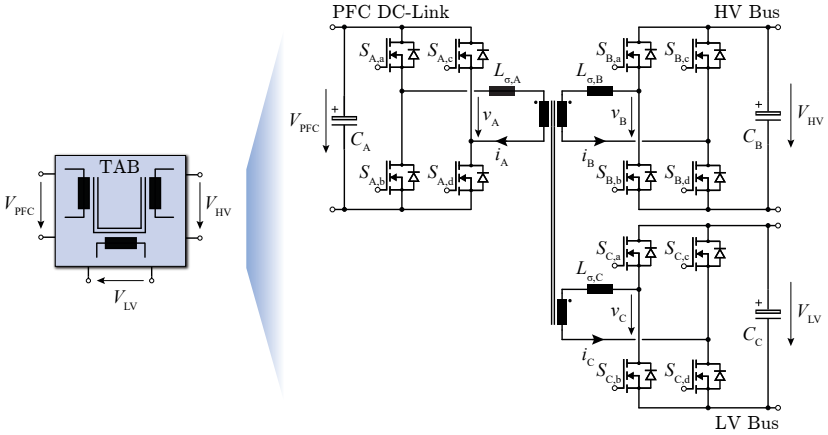


Fig. 2.1: Triple-active-bridge topology consisting of a three-winding transformer, three full-bridges and three output capacitors, where letter A is related to the PFC rectifier port, letter B to the HV port and letter C to the LV port, respectively (cf. Fig. 1.2e).

phase shifts φ_X, out of the three DC port voltages V_{PFC}, V_{HV} and V_{LV}. For the sake of clarity, the PFC rectifier port (in the following referred to as *PFC port* for short), the HV port and the LV port are related to the indices A, B and C, hereinafter. Hence, as an example, the voltage waveform v_{A} of the PFC port, including its gate drive signals, is shown in Fig. 2.2, with an exemplary duty cycle D_{A} of 50 % and a phase shift φ_{A} of 0°.
The three rectangular voltages v_X are then directly applied to the respective transformer windings, whereby the winding currents i_X inherently depend on the voltage differences between the applied winding voltages v_X and the respective leakage inductances $L_{\sigma,X}$ of the transformer.

According to [21], the complete TAB converter can be represented by the simplified equivalent circuit diagram of Fig. 2.3a. However, in most applications, the magnetizing inductance L_{m} of the transformer is much larger than its leakage inductances, which is why it can be neglected for high switching frequencies. Consequently, the circulating power in the converter only depends on v_X and $L_{\sigma,X}$, and can be controlled by means of the three duty cycles D_X, the two phase shifts φ_{AB} and φ_{AC} between the converter ports and the switching frequency f_{s}, according to Fig. 2.3b. Using these six control variables, and assuming unity turns ratios of $n_{\mathrm{AB}} = n_{\mathrm{AC}} = 1$, the

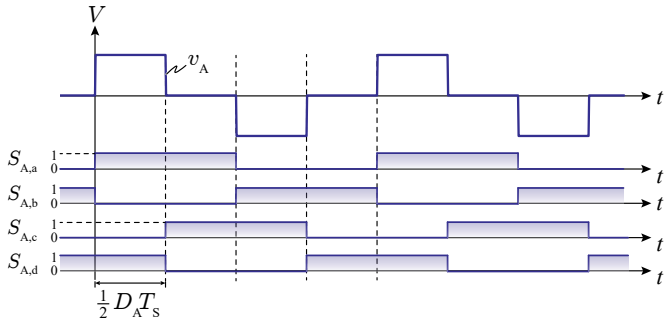


Fig. 2.2: Exemplary voltage waveform generated by the PFC port full-bridge with the corresponding gate drive signals $S_{A,y}$, $y \in \{a,b,c,d\}$.

port powers P_X, $X \in \{A,B,C\}$ can be calculated based on a first harmonic approximation [15] according to

$$
\begin{aligned}
I_A &= \frac{4V_A}{\pi^3 f_s L} \sin\left(\frac{D_A \pi}{2}\right) \\
I_B &= \frac{4V_B}{\pi^3 f_s L} \sin\left(\frac{D_B \pi}{2}\right) \\
I_C &= \frac{4V_C}{\pi^3 f_s L} \sin\left(\frac{D_C \pi}{2}\right) \\
P_A &= I_A \left[V_B \sin\left(\frac{D_B \pi}{2}\right) \sin(\varphi_{AB}) + V_C \sin\left(\frac{D_C \pi}{2}\right) \sin(\varphi_{AC}) \right] \\
P_B &= I_B \left[V_A \sin\left(\frac{D_A \pi}{2}\right) \sin(-\varphi_{AB}) + V_C \sin\left(\frac{D_C \pi}{2}\right) \sin(\varphi_{AC} - \varphi_{AB}) \right] \\
P_C &= I_C \left[V_A \sin\left(\frac{D_A \pi}{2}\right) \sin(-\varphi_{AC}) + V_B \sin\left(\frac{D_B \pi}{2}\right) \sin(\varphi_{AB} - \varphi_{AC}) \right],
\end{aligned}
\tag{2.1}
$$

whereby the equivalent leakage inductances $L'_{\sigma,X}$ have been assumed to be identical with a value of L for simplicity reasons. If the TAB is assumed to be lossless, only two of the port powers can be chosen independently, due to $P_A + P_B + P_C = 0$. Hence, these two port power values are controlled by means of six different control parameters D_A, D_B, D_C, φ_{AB}, φ_{AC} and f_s. Consequently, multiple parameter combinations yield exactly the same power distribution, whereby only one of these combinations guarantees the required power transfer with a minimum power loss. The optimal parameters can be

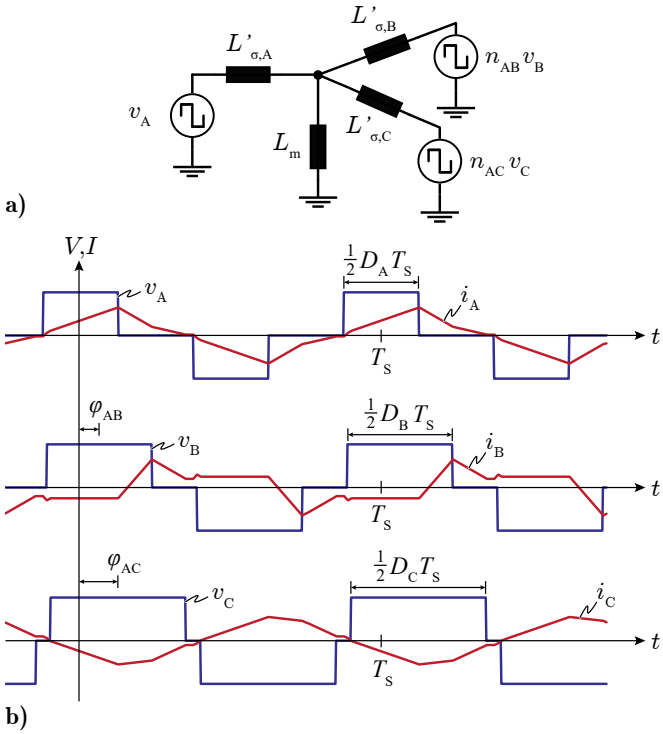


Fig. 2.3: a) Equivalent circuit of a TAB with the equivalent leakage inductances $L'_{\sigma,X}$ and the winding turns ratios n_{XZ}, $X, Z \in \{\text{A,B,C}\}$. **b)** Exemplary current and voltage waveforms in the TAB.

found numerically in consideration of soft-switching operation (switching losses) and the occurring RMS currents (conduction losses).
Based on a numerical optimization for minimal conduction losses, a comparably easy, close to optimal solution for the three duty cycles can be found, according to

$$D_\mathrm{A} = \frac{\min\{V_\mathrm{A}, V_\mathrm{B}, V_\mathrm{C}\}}{V_\mathrm{A}} \qquad D_\mathrm{B} = \frac{\min\{V_\mathrm{A}, V_\mathrm{B}, V_\mathrm{C}\}}{V_\mathrm{B}} \qquad D_\mathrm{C} = \frac{\min\{V_\mathrm{A}, V_\mathrm{B}, V_\mathrm{C}\}}{V_\mathrm{C}}. \tag{2.2}$$

Based on these duty cycles, and using the following auxiliary functions

$$\alpha = V_\mathrm{A} \sin\left(\frac{\pi}{2} D_\mathrm{A}\right) \quad \beta = V_\mathrm{B} \sin\left(\frac{\pi}{2} D_\mathrm{B}\right) \quad \gamma = V_\mathrm{C} \sin\left(\frac{\pi}{2} D_\mathrm{C}\right) \quad \mu = \frac{4}{3\pi^3 f_\mathrm{s} L}, \tag{2.3}$$

the two phase-shifts φ_AB and φ_AC, which yield the targeted port powers P_A and P_B, can be found according to

$$\varphi_\mathrm{AB} = \sin^{-1}\left(\frac{P_\mathrm{A}}{\alpha\beta\mu} - \frac{\gamma}{\beta}\sin(\varphi_\mathrm{AC})\right) \tag{2.4}$$

and

$$P_\mathrm{B} = -P_\mathrm{A}\left(1 + \frac{\gamma}{\alpha}\cos(\varphi_\mathrm{AC})\right) + \alpha\gamma\mu\sin(\varphi_\mathrm{AC}) + \gamma^2\mu\sin(\varphi_\mathrm{AC})\cos(\varphi_\mathrm{AC}) + \beta\gamma\mu\sin(\varphi_\mathrm{AC})\sqrt{1 - \left(\frac{P_\mathrm{A}}{\alpha\beta\mu} - \frac{\gamma}{\beta}\sin(\varphi_\mathrm{AC})\right)^2}. \tag{2.5}$$

However, equation (2.5) cannot be solved explicitly for φ_AC, which is why either a lookup table, or a numeric solver needs do be implemented in the controller.
Nevertheless, using these control parameters, the required power flow within the TAB can be achieved in a highly efficient manner, as long as the port voltage ratios more or less correspond to the turns ratios of the transformer. For these operating conditions, the ratios between the RMS port currents and the average output currents are close to one and therefore optimal.

In contrast, if the port voltage ratios deviate from their respective winding ratios, the share of reactive power flow in the converter significantly increases, as the duty cycles D_X, during which active power is transferred, have to be reduced (cf. (2.2)). Hence, an increase in conduction losses cannot be avoided. This fact is illustrated in Fig. 2.4a based on simulated current waveforms in

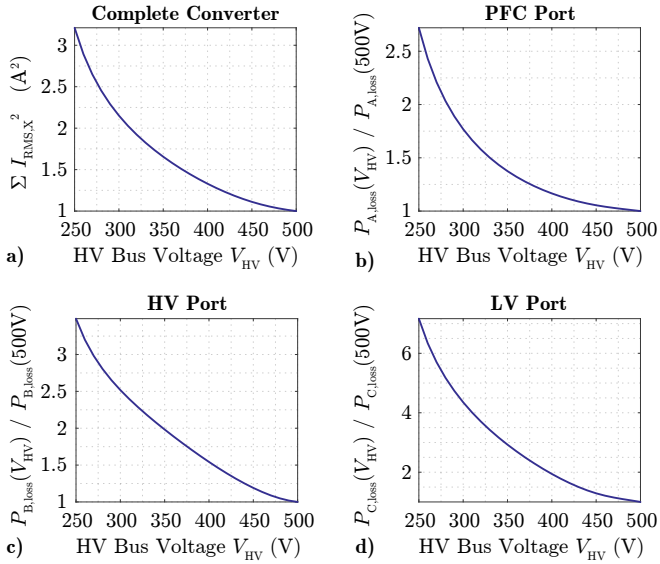


Fig. 2.4: a) Normalized change of the conduction losses for a voltage variation of the HV bus for the exemplary port powers $P_{\mathrm{A}} = 3.6\,\mathrm{kW}$, $P_{\mathrm{B}} = -2.6\,\mathrm{kW}$, $P_{\mathrm{C}} = -1\,\mathrm{kW}$, port voltages $V_{\mathrm{A}} = 500\,\mathrm{V}$, $V_{\mathrm{B}} = 250...500\,\mathrm{V}$, $V_{\mathrm{C}} = 14.5\,\mathrm{V}$ and winding turns ratios $n_{\mathrm{AB}} = 1$ and $n_{\mathrm{AC}} = \frac{500}{14.5}$. **b)-d)** Normalized ratios of the individual port conduction losses with reference to their respective port powers.

an example TAB for the specifications of Tab. 1.1, whereby the sum of the squares of the occurring port RMS currents is used as an indicator for the total occurring conduction losses.

As shown in the aforementioned figure, the conduction losses in the complete converter system are increasing by a factor of more than 3, if the HV port voltage is reduced from the nominal 500 V to its minimum value of 250 V. However, the theoretically expected minimal increase in conduction losses would be much smaller, as can be calculated according to

$$\frac{P_{\mathrm{tot,250V}}}{P_{\mathrm{tot,500V}}} \propto \frac{\left(\frac{3600}{500}\right)^2 + \left(\frac{2600}{250}\right)^2 + \left(\frac{1000}{500}\right)^2}{\left(\frac{3600}{500}\right)^2 + \left(\frac{2600}{500}\right)^2 + \left(\frac{1000}{500}\right)^2} = 1.97 \rightarrow +97\,\%. \tag{2.6}$$

The significant increase of losses results from the aforementioned decreased power factor, if the port voltages deviate from their nominal values, as shown in Fig. 2.4b-d based on the normalized conduction losses for each individual

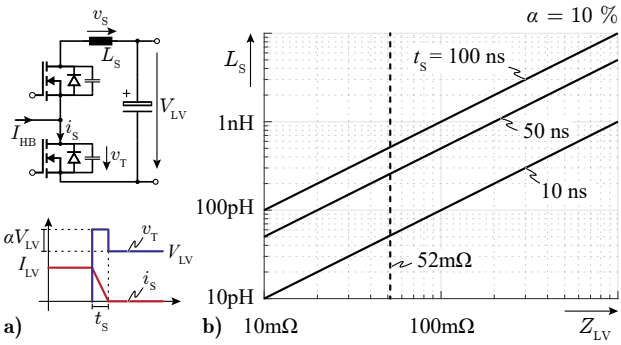


Fig. 2.5: a) Schematic of a half-bridge transistor circuit with the considered parasitic power loop inductance L_S, and the corresponding voltage v_T and current waveform i_S during a switching transition. **b)** Maximum allowed parasitic power loop inductance L_S for a certain output impedance Z_{LV}, switching time t_S and a maximum allowed voltage overshoot α of 10 % [22].

converter port and different V_{HV}.
Hence, even though the port voltages and the port powers of the PFC port and the LV port are kept constant, a significant increase in conduction losses in both ports can be observed. This yields (especially in the LV port) considerable issues, as will be shown in the following.

Besides the obvious issue of significantly increased conduction losses due to the additional reactive power flow for widely varying port voltages, especially the large currents during the switching transitions in the LV port, together with the relatively small output capacitance of the switching devices, result in very short commutation intervals t_S (cf. Fig. 2.5). Consequently, this leads to extremely high $^{di}/_{dt}$ values and, accordingly to large switching overvoltages v_S

$$v_S = \frac{L_S I_{sw}}{t_S}, \tag{2.7}$$

due to the parasitic inductance L_S of the commutation loop (cf. Fig. 2.5a). In practical applications, v_S should be limited to a certain fraction α of the port voltage V_{LV}, to allow for using semiconductors with relatively low breakdown voltage and therefore beneficial $R_{DS,on}$ properties. The maximum allowed overvoltage αV_{LV} and the characteristic impedance Z_{LV} of the converter port, directly define the maximum allowable parasitic inductance of the

commutation loop according to

$$L_S \leq t_S \alpha Z_{LV} \qquad Z_{LV} = \frac{V_{LV}}{I_{LV,max}}. \tag{2.8}$$

This limitation of L_S is illustrated in Fig. 2.5b for different commutation intervals t_S and a maximum allowed voltage overshoot of $\alpha = 10\,\%$.
In the application at hand, the characteristic impedance of the LV port shows a value of only $Z_{LV} = 52\,\text{m}\Omega$, i.e. is extremely small. Hence, based on Fig. 2.5b, this definitely demands a power loop inductance below 1 nH, which is hardly achievable in a real circuit design, due to the inevitable parasitic inductances of the semiconductor packages, the DC-link capacitor and the PCB tracks. For this reason, a significant switching overvoltage has to be expected. As a consequence, the employment of MOSFETs with high breakdown voltage and therefore relatively high $R_{DS,on}$ per chip area is unavoidable, resulting in either substantial conduction losses or a large total required silicon area A_{Si}.

In contrast to the characteristic impedance Z_{LV} of the LV port, the characteristic impedances of the two remaining ports (HV and PFC) are relatively high, as both ports are connected to high voltages and carry a comparably low current. Even though a high characteristic impedance is beneficial regarding overvoltage issues, during the switching transients in soft-switching applications, a large current is required in order to charge and discharge the MOSFETs parasitic output capacitances C_{oss} within a reasonably short time interval t_S:

$$Q_{oss} = C_{oss} \cdot V_{DS} \rightarrow t_S = \frac{C_{oss} \cdot V_{DS}}{I_X} = C_{oss} \cdot Z_X, \quad X \in \{\text{PFC}, \text{HV}\}. \tag{2.9}$$

As can be noticed, the duration of the soft-switching transition t_S is proportional to Z_X, which means that for high-voltage ports with high characteristic impedances, and a high switching frequency, a large amount of the port current is only needed to achieve soft-switching, resulting in a substantial amount of reactive power flow in the converter. Consequently, soft-switching operation in a converter port with a high characteristic impedance can only be achieved at the expense of significantly increased conduction losses.

Besides these disadvantages, also the combination of low and high characteristic output impedances Z_X implies an additional converter performance limitation, as the huge difference between the port voltages demands for a high turns-ratio of the transformer, and therefore limits the HV windings to

a large minimum number of turns, even if the LV-winding is realized with a single turn. This limitation yields sub-optimal transformer designs with either high winding losses or low power density, especially if PCB-windings should be employed.

For these reasons, a single TAB is not suitable for the specifications of the application at hand with its wide port voltage variations, high LV port currents an their large port voltage ratios. Consequently, the conventional TAB needs to be extended by additional converter stages and/or circuit designs, as will be discussed in the following.

2.2 Triple-Active-Bridge Extensions

The previous section showed the importance of winding ratio proportional port voltages in a TAB. However, the port voltages in the application at hand are varying within a wide range, which is why the topology has to be extended by an additional stage, which helps keeping the port voltages on a constant level. This can be done by adding a non-isolated DC/DC converter between the HV DC-bus and the HV port of the TAB converter, according to Fig. 2.6a. The additional stage compensates the difference between the nominal port voltage of 500 V and the actual HV battery voltage, whereby this approach ensures optimal operating conditions for the TAB and, therefore, limits the occurring RMS currents in its ports.
Even though the additional converter stage allows for minimizing the RMS currents in the TAB, the remaining issues related to the characteristic impedances of the converter ports and the adverse turns ratio of the transformer are still existent. Hence, instead of trying to keep the TAB port currents as low as possible, one could try to change the converter topology in a way, that it is capable of handling the occurring currents even for varying port voltages. Thus, the winding ratio of the transformer has to be reduced and at the same time, the characteristic impedance of the LV converter port has to be increased. This can be achieved by using multiple identical TAB converter cells and a smart connection of the different converter ports as shown in Fig. 2.6b. Hence, the series-connected HV ports and the parallel-connected LV ports provide the desired reduced cell-internal turns ratios as well as the reduced LV port currents due to their equal current/power sharing.
In the following two sections, these two topologies are discussed in more detail.

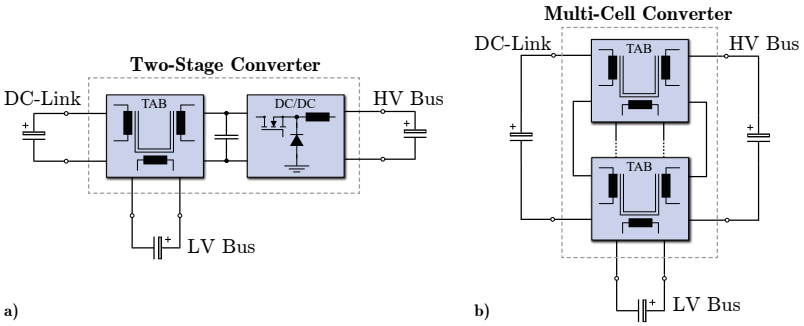


Fig. 2.6: a) Two-stage converter topology consisting of a TAB followed by a non-isolated DC/DC converter and **b)** multi-cell TAB converter topology used to reduce the cell-internal turns ratios and to increase the cell-internal characteristic impedances of the LV ports.

2.2.1 Multi-Port Multi-Cell Topology

The previously introduced challenges in a single TAB converter can effectively be mitigated by means of the proposed multi-port multi-cell (MPMC) converter structure, which is shown in Fig. 2.7. It comprises n identical TAB cells (blue-shaded), whose ports are all connected either in series or in parallel, depending on the level of the applied bus voltage. Hence, the ports connected to the HV buses V_{PFC} and V_{HV} are connected in series, while the LV ports are connected in parallel. The series connection of multiple TAB-cells equally distributes the bus voltage between the cell-internal HV ports, which means that the characteristic impedances of the cell-internal HV ports are reduced. Accordingly, soft-switching operation can be achieved with a much lower commutation current, providing reduced conduction losses in the converter. In addition, the required breakdown voltage of the switching devices can be reduced, which offers the possibility of using alternative semiconductor technologies with beneficial properties regarding conduction and switching losses (figure-of-merit) [23].
Furthermore, the series connection of multiple TAB-cells at the HV ports reduces the cell-internal port voltage ratios by a factor of n, which means that with the number of cells n a further degree of freedom is introduced. For this reason, the design space of the transformer is considerably enlarged, which typically results in transformer designs with higher efficiency and/or power density.

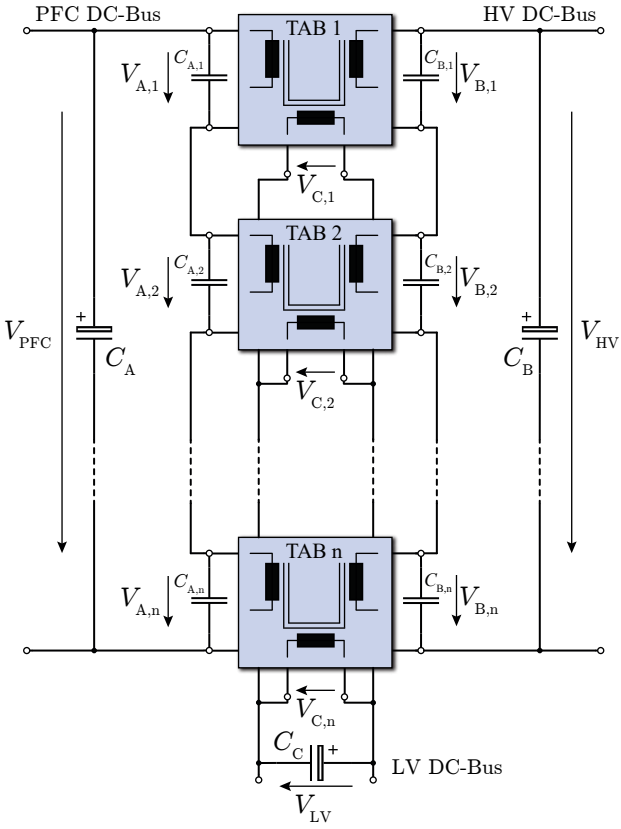


Fig. 2.7: Structure of the proposed multi-port multi-cell (MPMC) converter system with n identical TAB cells.

Similarly, the parallel connection of multiple converter ports enables an equal distribution of the LV output current among the cell-internal LV ports, whereby their characteristic impedance is increased, and the commutation loop related overvoltage can be substantially reduced. Accordingly, semiconductors with low breakdown voltages and therefore beneficial $R_{\mathrm{DS,on}}$ values can be used again.
Furthermore, in order to reduce the current ripple in the DC-link capacitors $C_{\mathrm{A,B,C}}$, the TAB-cells can be operated in an interleaved fashion by phase shifting the switching cycles of the individual TAB-cells by $\varphi_{\mathrm{cell}} = \frac{2\pi}{n}$, which results in an effective switching frequency of $n \cdot f_{\mathrm{s}}$. This also reduces the required DC-link capacitance for a certain allowed voltage ripple and lowers the volume of these components.

The proposed multi-cell approach for multi-port converter systems has already been investigated for two-port converter systems in telecom applications, where, due to the aforementioned benefits, a significant improvement in terms of efficiency and power density was achieved [24]. However, while for two-port converter systems, e.g. in input-series output-parallel (ISOP) configuration, natural voltage and current balancing is guaranteed, for three-port converter systems, the voltage and current sharing needs to be actively controlled. Therefore, in the following subsection, a new control strategy is presented, which guarantees equal power distribution in multi-cell multi-port converter systems.

MPMC Converter Control

In two-port converter systems, e.g. with ISOP structure, a simple modulation scheme with common duty cycles and phase shifts for all individual converter cells can be applied [23], due to their inherent natural voltage and current balancing behavior. The advantage of this control strategy is the minimization of the complexity and computation effort of the control, as a single controller can be used to calculate the common control parameter set (D_{A}, D_{B} and φ_{AB} in case of DABs) for all converter cells. Hence, each cell is controlled with the same gate drive signals, whereby a cell-internal control can be omitted and the controller hardware and software effort is reduced to the same amount, as required in a single-cell converter. Unfortunately, this natural balancing is lost in multi-port ($n_{\mathrm{port}} > 2$) systems, as it is exemplarily shown in Fig. 2.8 for a three-port two-cell converter system.
Initially, it is assumed that the port voltages $V_{\mathrm{B},1}$ and $V_{\mathrm{B},2}$ are not balanced and that a certain power P_{B} is supplied from the PFC rectifier DC-bus to the

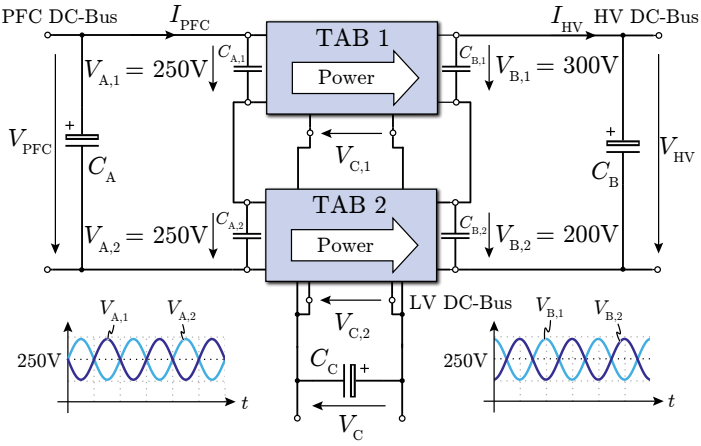


Fig. 2.8: Example of an asymmetric port voltage distribution in a three-port two-cell converter with the port voltage oscillations induced by a common duty cycle control.

HV DC-bus. Such an asymmetric voltage distribution is a likely scenario after e.g. a load step, as due to component tolerances and aging effects in a real system, the capacitance values of the cell-internal capacitors $C_{A,k}$ and $C_{B,k}$ are slightly different and therefore result in a series connection of dissimilar capacitances in the PFC and HV converter ports. Consequently, during a load step at e.g. the HV DC-bus, the cell-internal capacitors $C_{B,1}$, $C_{B,2}$ to $C_{B,n}$ are discharged by the same load current, which in case of unequal capacitance values leads to different voltage changes of the cell-internal capacitors and, therefore, to an asymmetric voltage distribution.
Thus, applying the aforementioned common duty cycle/phase shift control modulation scheme to the example of the three-port two-cell converter system shown in Fig. 2.8, results in a further destabilization of the port voltages, as the cell-internal port power values $P_{B,1}$ and $P_{B,2}$ are directly proportional to the momentary port voltages $V_{B,1}$ and $V_{B,2}$ according to (2.1). Consequently, the higher port voltage $V_{B,1}$ leads to a larger cell-internal power $P_{B,1}$, whereas the lower port voltage $V_{B,2}$ yields a smaller cell-internal power $P_{B,2}$. This difference between the cell-internal port power values $P_{B,1}$ and $P_{B,2}$ in turn also causes an asymmetry in the port voltages $V_{A,1}$ and $V_{A,2}$ due to the unequal power demand from the two converter cells TAB 1 and TAB 2, which finally result in a hardly damped port voltage oscillation between port A and port B, as shown in Fig. 2.8, which in turn increases the required breakdown voltages

of the employed cell-internal power semiconductors.
Consequently, in order to avoid unbalanced voltage distributions and unequal power sharing among the converter cells, an individual control of each cell is inevitable in MPMC converter systems. Ideally, due to the occurring conduction losses, the total converter power should be equally distributed among the converter cells. However, as will be shown later, an equal distribution of the aforementioned converter power among the individual converter cells cannot balance out asymmetries in the voltage distribution and, therefore, yields an unstable converter operation. For this reason, a more sophisticated controller needs to be employed.

In the following, the structure of a suitable MPMC controller is presented, which guarantees the appropriate power distribution P_{A}, P_{B} and P_{C} between the three DC-buses, while at the same time the port voltages can be balanced for all operating points. Thereby, the set-points $P_{\mathrm{A,set}}$, $P_{\mathrm{B,set}}$ and $P_{\mathrm{C,set}}$ of the aforementioned power distribution P_{A}, P_{B} and P_{C} are calculated by a superordinate battery charge controller and are then forwarded as reference values to the central MPMC master controller, which is the main focus of this subsection.
Based on the actual cell-internal port voltages $V_{\mathrm{A,k}}$ and $V_{\mathrm{B,k}}$, $k \in \{1, .., n\}$, and the given power set-points $P_{\mathrm{A,set}}$, $P_{\mathrm{B,set}}$ and $P_{\mathrm{C,set}}$, the central MPMC master controller then calculates the cell-dependent power set-points $P_{\mathrm{A,k,set}}$, $P_{\mathrm{B,k,set}}$ and $P_{\mathrm{C,k,set}}$, $k \in \{1, .., n\}$ in such a way that a symmetric voltage distribution among the individual converter cells is achieved (cf. Fig. 2.9).
Afterwards, these cell-dependent power set-points $P_{\mathrm{A,k,set}}$, $P_{\mathrm{B,k,set}}$ and $P_{\mathrm{C,k,set}}$ are forwarded to the cell-internal controllers of the individual TAB cells, which then calculate the appropriate duty cycles $D_{\mathrm{A,k}}$, $D_{\mathrm{B,k}}$, $D_{\mathrm{C,k}}$ and phase shifts $\varphi_{\mathrm{AB,k}}$ and $\varphi_{\mathrm{AC,k}}$, according to Section 2.1, in order to process the targeted power values $P_{\mathrm{A,k}}$, $P_{\mathrm{B,k}}$ and $P_{\mathrm{C,k}}$. Hence, each converter cell operates as an individual TAB converter, whose reference values $P_{\mathrm{A,k,set}}$, $P_{\mathrm{B,k,set}}$ and $P_{\mathrm{C,k,set}}$ are given by the central MPMC master controller.
Thereby, actually only two of the three set-point values $P_{\mathrm{A,k,set}}$, $P_{\mathrm{B,k,set}}$ and $P_{\mathrm{C,k,set}}$ have to be provided by the central MPMC master controller, since the third power set-point can be calculated based on $P_{\mathrm{A,k,set}} + P_{\mathrm{B,k,set}} + P_{\mathrm{C,k,set}} = 0$.
Furthermore, in the proposed MPMC topology only the series connected ports $\mathrm{A_k}$ and $\mathrm{B_k}$ can lead to unbalanced voltage distributions among the cell converter ports, hence, only the power values of these two ports need to be actively controlled. However, in order to be able to redistribute power between series connected ports, in the proposed MPMC topology at least one

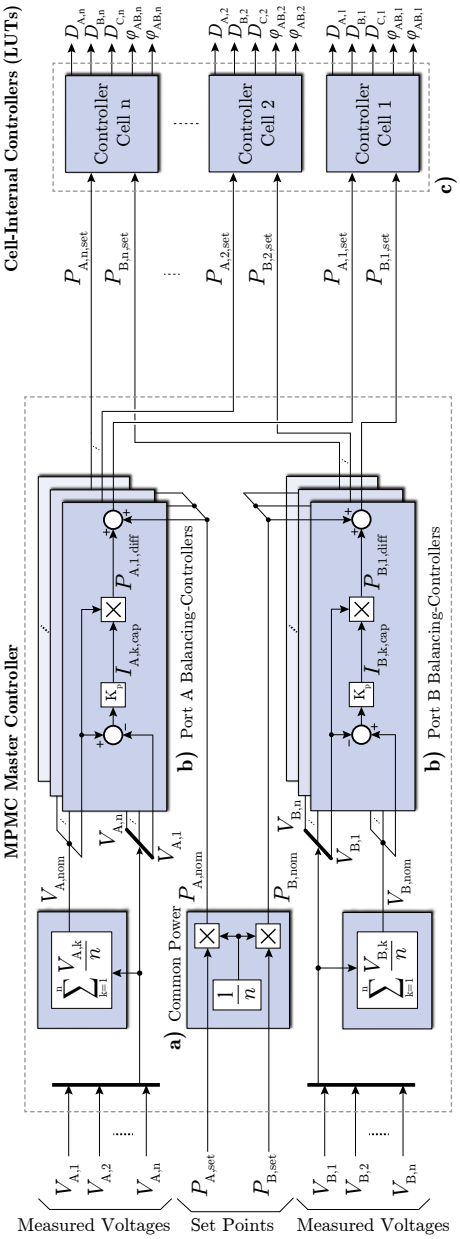


Fig. 2.9: Complete control scheme of the MPMC converter, comprising the different sub-controllers and the cell-internal look-up-tables (LUTs).

parallel port is needed, as a direct power transfer between series connected ports, e.g. from port B_1 to B_2, as would be required in the example of Fig. 2.8, is not possible. In this case, for example, TAB 1 would have to transfer the excess energy stored in $C_{B,1}$ to the parallel port C, while TAB 2 retrieves the needed amount of energy from port C to recharge the capacitor $C_{B,2}$. Hence, in addition to providing the required port power P_C, the parallel connected port is also used to compensate for possible voltage asymmetries in the power distributions of the series connected converter ports A_k and B_k.
For the calculation of the cell-dependent power set-points $P_{A,k,set}$ and $P_{B,k,set}$, the proposed MPMC master controller uses a two-step approach, where in a first step, the required power levels $P_{A,B,C}$ are equally distributed among the individual converter cells, and in a second step, parts of these cell-internal powers are redistributed between the different cells to achieve the required voltage balancing, without affecting the total converter output power values $P_{A,B,C}$. In the following, both calculation steps are explained in more detail. For the sake of clarity, since the set-points $P_{A,k,set}$ and $P_{B,k,set}$ of both series connected ports A and B are calculated in the same manner, only the nomenclature for port A is used in the following description.

Common Power Share In a first step, the central MPMC master controller equally distributes the received power set-point $P_{A,set}$ among the converter cells by dividing the total power $P_{A,set}$ by the number of converter cells n according to Fig. 2.9a. Thus, the MPMC controller assigns the same nominal port power $P_{A,nom} = \frac{P_{A,set}}{n}$ to each cell-port A_k. This common power distribution strategy guarantees that the power requirement $P_{A,set}$ is met, as

$$\sum_{k=1}^{n} P_{A,k,set} = \sum_{k=1}^{n} P_{A,nom} = P_{A,set}. \tag{2.10}$$

As already mentioned, in order to balance the individual port voltages $V_{A,k}$ of the converter cells, a part of the common power share $P_{A,nom}$ has to be redistributed among the different cells, which means that each individual port power $P_{A,k,set}$ is modified by a certain voltage balancing power share $P_{A,k,diff}$:

$$\sum_{k=1}^{n} P_{A,k,set} = \sum_{k=1}^{n} P_{A,nom} + P_{A,k,diff} = \underbrace{\sum_{k=1}^{n} P_{A,nom}}_{=!P_{A,set}} + \underbrace{\sum_{k=1}^{n} P_{A,k,diff}}_{=!0} \tag{2.11}$$

Consequently, based on (2.10) and (2.11), the sum of the power shares $P_{A,k,diff}$, used for the voltage balancing, has to be zero such that the total converter

power value $P_{\mathrm{A,set}}$ is not affected. The detailed calculation method of the individual power shares $P_{\mathrm{A,k,diff}}$ is explained in the following.

Voltage Balancing Power Share The objective of the voltage balancing power share $P_{\mathrm{A,k,diff}}$ is to control all port voltages $V_{\mathrm{A,k}}$ to the same voltage level. Therefore, the reference voltage $V_{\mathrm{A,nom}}$ corresponds to the average of the port voltages $V_{\mathrm{A,k}}$ and can be calculated based on the sum of the port voltages divided by the number of individual converter cells n according to

$$V_{\mathrm{A,nom}} = \sum_{\mathrm{k}=1}^{n} \frac{V_{\mathrm{A,k}}}{n}, \tag{2.12}$$

as shown in Fig. 2.9. For the balancing of the port voltages this basically means that for a too high port voltage $V_{\mathrm{A,k}}$ the corresponding DC-link capacitor $C_{\mathrm{A,k}}$ has to be discharged by a certain current $I_{\mathrm{A,k,cap}}$, or in other words, that a certain power $P_{\mathrm{A,k,diff}} = I_{\mathrm{A,k,cap}} \cdot V_{\mathrm{A,nom}}$ has to be extracted from this capacitor. On the other hand, for a too low port voltage $V_{\mathrm{A,k}}$, the DC-link capacitor needs to be charged by a certain current $I_{\mathrm{A,k,cap}}$, or again by analogy, a certain power $P_{\mathrm{A,k,diff}} = I_{\mathrm{A,k,cap}} \cdot V_{\mathrm{A,nom}}$ has to be delivered to this capacitor. Hence, according to a conventional voltage controller, the charging/discharging current $I_{\mathrm{A,k,cap}}$ can be determined by means of a proportional controller, which scales the difference between the reference voltage $V_{\mathrm{A,nom}}$ and the actual port voltage $V_{\mathrm{A,k}}$ by a proportional gain $\mathrm{K_P}$ (cf. Fig. 2.9). Finally, the power share $P_{\mathrm{A,k,diff}}$, which basically corresponds to the momentary power flowing into or out of the capacitor, can be calculated by multiplying the charging/discharging current $I_{\mathrm{A,k,cap}}$ with the reference voltage $V_{\mathrm{A,nom}}$ (cf. Fig. 2.9b) according to

$$P_{\mathrm{A,k,diff}} = \frac{V_{\mathrm{A}}}{n} \cdot I_{\mathrm{A,k,cap}} = \frac{V_{\mathrm{A}}}{n} \cdot K_{\mathrm{P}} \cdot \left(\frac{V_{\mathrm{A}}}{n} - V_{\mathrm{A,k}} \right). \tag{2.13}$$

It is important to note, that based on (2.13) the sum of all voltage balancing power shares $P_{\mathrm{A,k,diff}}$ equals zero

$$\sum_{\mathrm{k}=1}^{n} P_{\mathrm{A,k,diff}} = \frac{V_{\mathrm{A}} K_{\mathrm{P}}}{n} \left(\underbrace{\sum_{\mathrm{k}=1}^{n} \frac{V_{\mathrm{A}}}{n}}_{=\mathrm{V_A}} - \underbrace{\sum_{\mathrm{k}=1}^{n} V_{\mathrm{A,k}}}_{=\mathrm{V_A}} \right) = 0 \tag{2.14}$$

and therefore the condition of (2.11) is always fulfilled. Consequently, the redistribution of the power shares $P_{\mathrm{A,k,diff}}$ does not affect the total power P_{A}.

For the sake of completeness, instead of a P-controller with a proportional gain K_P, a PI-controller could be used for the voltage controller. However, in this case, (2.11) would not be fulfilled anymore at any point in time, which means that e.g. during load transients, the momentary total power P_A does not coincide with the power set-point $P_{A,set}$ given from e.g. the superordinate battery charge controller.

In a last step, the different power shares $P_{A,nom}$ and $P_{A,k,diff}$ are added up, resulting in the cell-dependent power set-points $P_{A,k,set}$ as shown in Fig. 2.9b. As mentioned in the beginning, exactly the same calculation method is applied to the cell ports B_k in order to calculate their respective power set-points $P_{B,k,set}$. Finally, the set-points $P_{A,k,set}$ and $P_{B,k,set}$ are forwarded to the cell-internal TAB controllers, which for their part calculate the optimal duty-cycles $D_{A,B,C}$ and phase shifts φ_{AB} and φ_{AC} according to Fig. 2.9c and Section 2.1.
In the following, the operating principle of the proposed MPMC controller is verified by means of simulations, and the necessity of a voltage balancing controller in this type of converter is pointed out.

MPMC Control Simulation

In order to prove the proposed control concept and to show the performance of the MPMC master controller in balancing the port voltages, the example of Fig. 2.8 with initially unbalanced port voltages $V_{B,1}$ and $V_{B,2}$, and initial power levels according to Tab. 2.1 is used. Hence, constant power values P_A, P_B and P_C are drawn from/delivered to the converter ports in this simulation, while the MPMC master controller solely balances out the asymmetry between $V_{B,1}$ and $V_{B,2}$ by using the aforementioned redistribution of the power shares $P_{B,k,diff}$. As already mentioned, since a direct power transfer between series connected ports B_1 and B_2 is not possible, TAB 1 transfers the excess energy stored in $C_{B,1}$ to the parallel port C ($P_{B,1,diff} > 0$ and $P_{C,1,diff} < 0$), while TAB 2 retrieves the needed amount of energy from port C to recharge the capacitor $C_{B,2}$ ($P_{B,2,diff} < 0$ and $P_{C,2,diff} > 0$). Hence, during the step response, not only the port power levels $P_{B,k,set}$, but also the port power levels $P_{C,k,set}$, differ from the nominal power levels $P_{B,nom}$ and $P_{C,nom}$, respectively. The power levels $P_{A,k,set}$, however, stay constant ($P_{A,k,diff} = 0$), since there it is assumed that the voltages $V_{A,1}$ and $V_{A,2}$ are perfectly balanced. The resulting port voltages $V_{B,1}$ and $V_{B,2}$, the power set-points $P_{A,k,set}$, $P_{B,k,set} = P_{B,k,diff} + P_{B,nom}$ and $P_{C,k,set} = P_{C,k,diff} + P_{C,nom}$, as well as the actual port power values $P_{A,k}$, $P_{B,k}$ and $P_{C,k}$ are shown in Fig. 2.10.
As expected from the P-controller of Fig. 2.9b, the two port voltages $V_{B,1}$ and

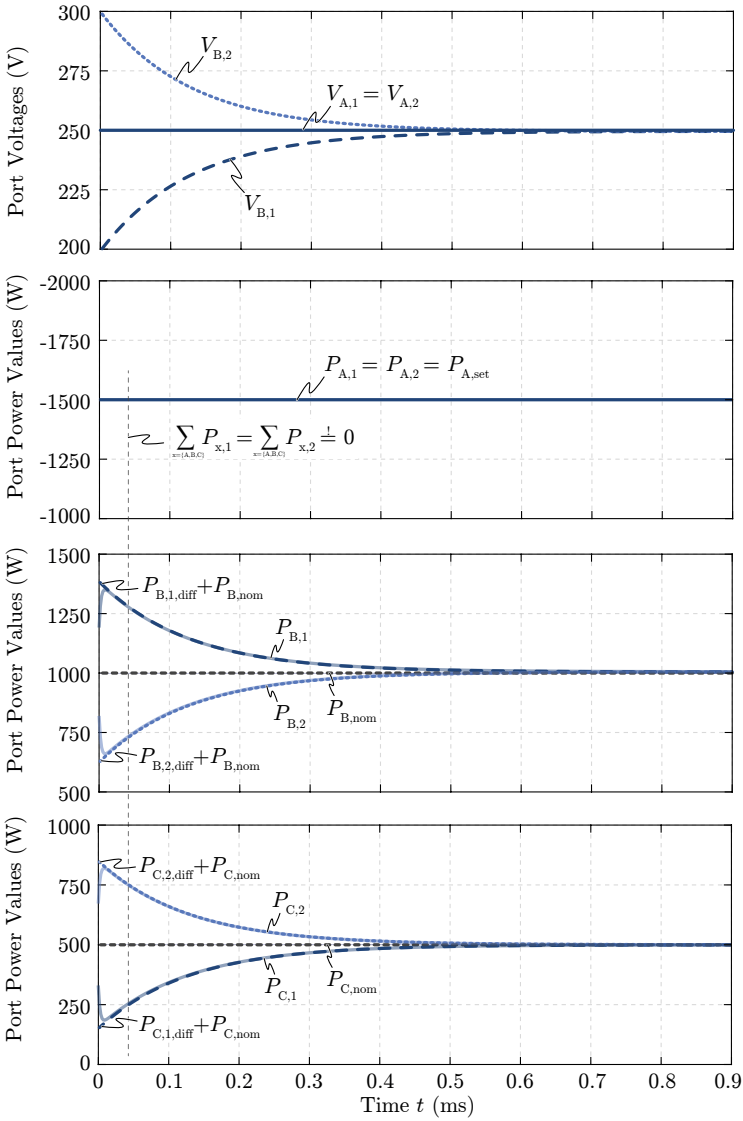


Fig. 2.10: Simulation results of the cell-dependent power set-points $P_{A,k,set} = P_{A,k,diff} + P_{A,nom}$, $P_{B,k,set} = P_{B,k,diff} + P_{B,nom}$ and $P_{C,k,set} = P_{C,k,diff} + P_{C,nom}$ as well as the actual power values $P_{A,k}$, $P_{B,k}$ and $P_{C,k}$ for the application of the MPMC master controller in the example of Fig. 2.8.

Tab. 2.1: Initial conditions of the simulation of Fig. 2.8 and the corresponding waveforms of Fig. 2.10.

P_A	P_B	P_C	$V_{A,1}$	$V_{A,2}$	$V_{B,1}$	$V_{B,2}$	V_C
−3 kW	2 kW	1 kW	250 V	250 V	200 V	300 V	15 V

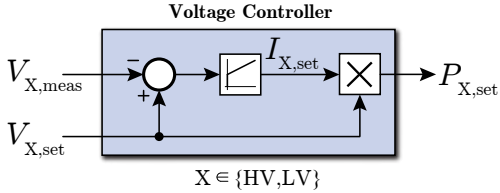


Fig. 2.11: Voltage PI-controller used to control the power set-point values of the MPMC converter.

$V_{B,2}$ exponentially converge to their nominal value $V_{B,nom}$. The same behavior can be found for $P_{B,1,diff}$ and $P_{B,2,diff}$, as they are directly proportional to the voltage error $V_{B,nom} - V_{B,k}$ according to (2.13). It can be seen, that the simulated output power values $P_{B,k}$ smoothly follow their reference values $P_{B,k,set} = P_{B,k,diff} + P_{B,nom}$, yielding the desired voltage balancing of $V_{B,1}$ and $V_{B,2}$.
Furthermore, as the power transfer between $P_{B,1}$ and $P_{B,2}$ can only be performed through the parallel port C, and the sum of the cell-internal port power values always has to be zero (cf. Fig. 2.10), the power levels $P_{C,k,diff}$ have to be equal to $-P_{B,k,diff}$ during the complete simulation time.

In order to analyze the system behavior of a complete EV distribution network, a PI voltage controller, emulating the superordinate battery charge controller, is added to the simulation according to Fig. 2.11, which in reality calculates the required total converter power set-points $P_{HV,set}$ and $P_{LV,set}$ based on the momentary port voltages V_{HV} and V_{LV}.
This voltage controller, in combination with the proposed MPMC master controller, is applied to the same two-cell three-port converter as depicted in Fig. 2.8. However, in this simulation example, it is assumed that, due to component tolerances, the capacitor connected to the HV port of TAB 1 has a lower capacitance than the one connected to TAB 2 (cf. Fig. 2.12). Hence, the employment of the proposed MPMC master controller becomes essential,

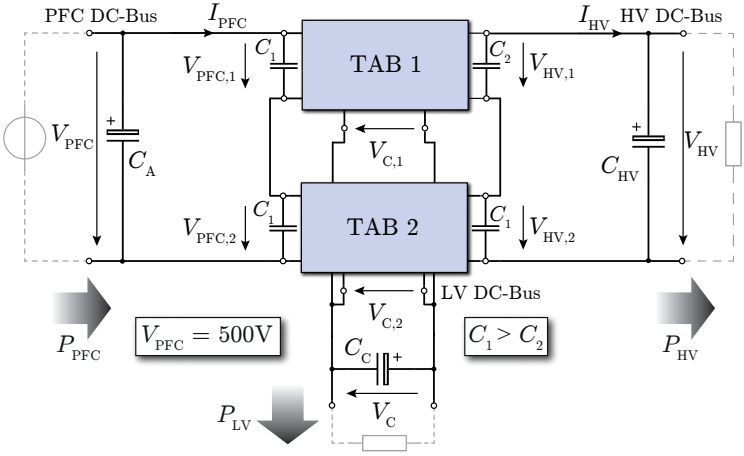


Fig. 2.12: Exemplary two-cell three-port converter system with different capacitor values in the series-connected HV ports during charge mode operation (power flow from the PFC to the HV and the LV port).

as will be shown in the following by means of the simulated, primary-side referred port voltages and power waveforms.
Initially, the converter is in steady-state with a HV output power P_{HV} of 3 kW, a LV output power P_{LV} of 600 W and a symmetric port voltage distribution between the series-connected converter ports, as shown in Fig. 2.13a. This is the most common situation during charging operation, as the major part of the system power is used to recharge the large HV battery and only a small share of the power is used to recharge the small LV battery.
At the time t_{st}, a load step occurs in both, the HV as well as the LV port, which is caused when a high power LV load, e.g. turning-on the air conditioning, is activated during charge operation. The load step in the HV port results from the input power limitation in the PFC port of 3.6 kW, since now more power has to be delivered to the LV port, and therefore only $P_{PFC} - P_{LV}$ can be used to recharge the HV battery. These load steps activate the superordinate battery charge controller as well as the central MPMC master controller, which try to regulate the output voltages of the converter.
The general shapes and magnitudes of the individual port power values $P_{HV,1}$, $P_{HV,2}$, $P_{LV,1}$ and $P_{LV,2}$, shown in Fig. 2.13a, are dominated by the step response of the battery voltage controller (cf. Fig. 2.11), since its time constant is much higher than the one of the central MPMC master controller. However, a

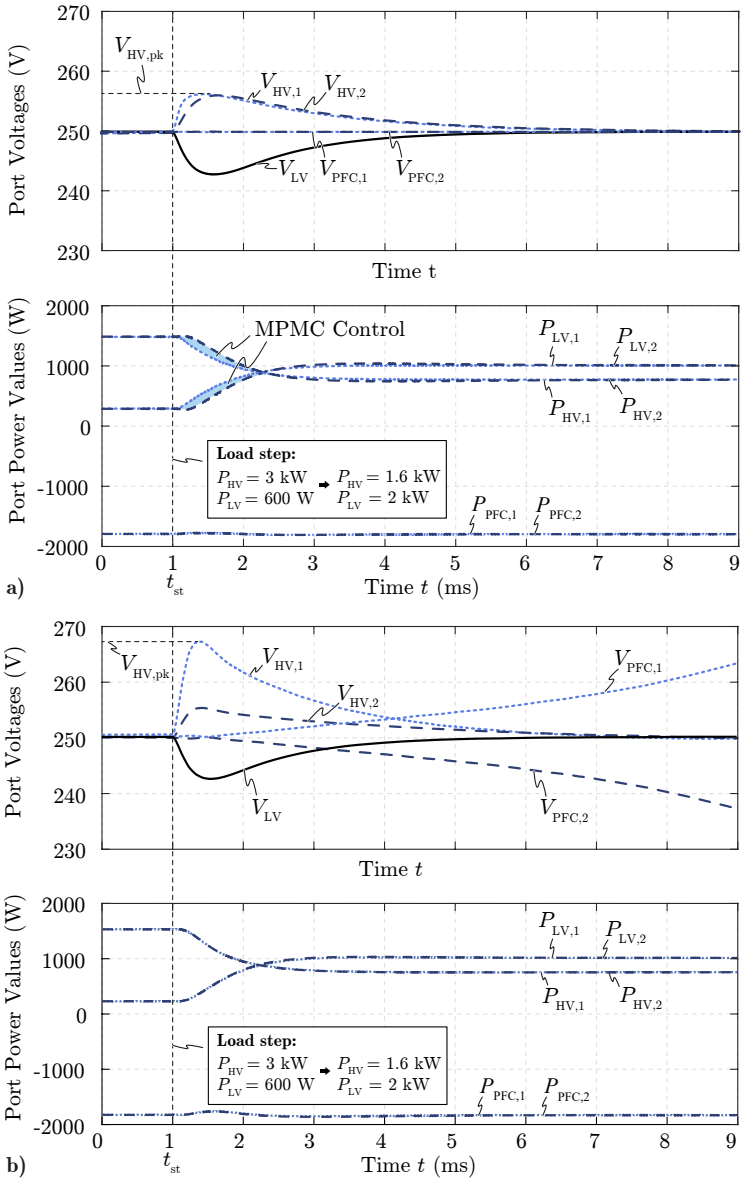


Fig. 2.13: Simulation results of a two-cell three-port converter system with different capacitor values in the series-connected HV ports and a load step at the time t_{st} **a)** with and **b)** without activated voltage balancing controller.

certain difference between the two port power values $P_{\mathrm{HV},1}$ and $P_{\mathrm{HV},2}$ can be observed (blue-shaded), which is induced by the MPMC master controller by generating a certain voltage balancing power share $P_{\mathrm{HV,k,diff}}$, based on the voltage difference $V_{\mathrm{HV},1} - V_{\mathrm{HV},2}$ in order to keep the port voltages at the HV DC-Bus $V_{\mathrm{HV},1}$ and $V_{\mathrm{HV},2}$ balanced. Accordingly, the same power difference between $P_{\mathrm{LV},1}$ and $P_{\mathrm{LV},2}$ is visible, due to the indirect power transfer between series-connected cells via port C. As a result of the MPMC master controller, which features a much higher control bandwidth than the battery charge controller, these voltage differences remain small, hence excessive overvoltages across the series-connected converter ports can be avoided, even though the DC-link capacitor values are different.
Finally, due to the aforementioned active port voltage balancing control, the voltages $V_{\mathrm{PFC},1}$ and $V_{\mathrm{PFC},2}$ of the PFC port are perfectly balanced and are therefore not affected by the asymmetric voltages in the HV port.

In order to show the importance and the benefits of the proposed controller, the same simulation was conducted for a system without the MPMC master controller, which means without the voltage balancing power share $P_{\mathrm{HV,k,diff}}$. In this case, the port power is equally distributed among the different converter cells, irrespective of the particular port voltages. It is important to note that in contrast to the previously mentioned common duty cycle control, this common power control does not lead to equal duty cycles in all individual cells, since in this case the individual cell-internal duty cycles also depend on the individual cell voltages. The resulting waveforms are shown in Fig. 2.13b, where two key differences with respect to Fig. 2.13a immediately become apparent: On the one hand, a large voltage overshoot in the HV port of TAB 1 can be observed, arising from the asymmetry of the capacitance values of the series-connected capacitors. However, at least after a certain time the voltages at the HV port are balanced again.
On the other hand, the far greater issue is that the system is unstable in the PFC port, as the cell voltages end up in a runaway situation.
These simulation results clearly show the importance of the proposed MPMC master control strategy in order to ensure a stable converter operation with balanced voltages and power distributions among the individual converter cells.

Hence, by utilizing the proposed MPMC control structure, it is possible to operate multiple TABs in the proposed multi-cell structure, whereby significantly improved design specifications for each individual TAB-cell are

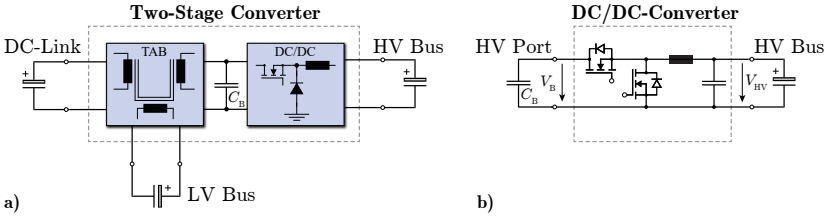


Fig. 2.14: Two-stage topology for the given application consisting of a TAB with an additional non-isolated DC/DC converter between its HV port and the HV bus (cf. Fig. 1.2g).

obtained. However, in order to really benefit from the advantages of the multi-cell structure, at least three TAB cells have to be used. Thus, the complete three-port DC/DC converter system would comprise at least three individual transformers and 36 power semiconductors, which is usually problematic for an industrial application, where the overall circuit complexity should be minimized to achieve reasonable reliability and manufacturing costs.
For this reason, the two-stage converter topology is investigated in more detail in the following, as it promises a significantly reduced number of components and therefore a reduced complexity compared to the MPMC approach.

2.2.2 Two-Stage Converter Topology

The two-stage converter approach is based on the same TAB topology as the MPMC converter. However, instead of using multiple TAB cells, a single TAB is extended by an additional non-isolated DC/DC converter at its HV port (cf. Fig. 2.14a), which converts the constant HV port voltage of 500 V to the respective momentary HV battery voltage. This new converter stage has to be able to feed power in both directions, as in charge mode, the TAB keeps the HV port voltage at a constant level of 500 V, while the DC/DC converter controls the power flow from the TAB to the HV battery, and in drive mode, the power flow is reversed, whereby the DC/DC converter controls the HV port voltage to its optimal level, while the TAB provides the required power flow from the HV port to the LV port.

One possible topology for this DC/DC converter is a conventional bidirectional buck/boost converter stage as shown in Fig. 2.14b. It is easy to build, cost-effective and already well documented in literature [25]. The soft-switching capability of this topology in triangular-current-mode (TCM) [8]

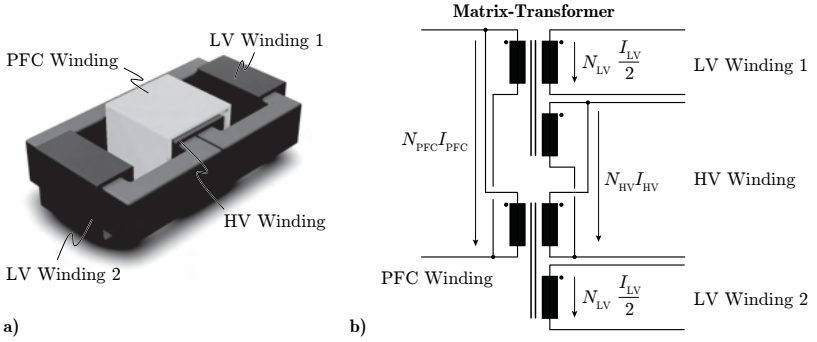


Fig. 2.15: a) Simplified 3D model of a matrix-transformer with two LV windings and two sub-cores and **b)** the corresponding equivalent circuit.

allows for very high switching frequencies and therefore small volumes of the passive components.
Depending on the required efficiency and power density of this non-isolated DC/DC converter, alternative topologies and/or control schemes, like interleaved operation of two bridge-legs for reduced current-ripple, could be employed as well.
However, even though the additional converter stage allows the TAB to operate with its optimal operating conditions, the high RMS output currents in the LV port and the large turns ratio still cause the aforementioned overvoltage issues across the LV-side semiconductors and the high winding losses. For this reason, an alternative TAB transformer structure could be used, which is based on the MPMC approach and uses multiple windings in the LV port to reduce both, winding ratio as well as overvoltages across their power switches. This so-called matrix-transformer is investigated in more detail in the following.

TAB Employing Matrix-Transformer

In a matrix-transformer, the original core is split into multiple identical sub-cores, where the PFC and the HV windings are still wound around all cores, but each sub-core now carries its own LV winding (cf. Fig. 2.15a). The equivalent circuit of this winding arrangement is shown in Fig. 2.15b by means of a two-core matrix-transformer, whereby the magnetic flux linkage seen by each LV-side winding is only half compared to the one of the conventional transformer. For this reason, the winding ratio within the transformer is

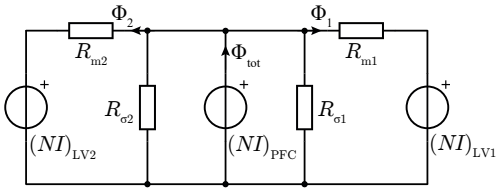


Fig. 2.16: Simplified equivalent reluctance model of the matrix-transformer of Fig. 2.15 with an open circuit in the HV winding.

halved as well and the design space for the transformer is enlarged. In addition, the output current in the LV port is evenly distributed among the two LV windings, whereby the characteristic impedances of the individual LV ports are increased, as will be shown in the following.

On the basis of the reluctance model for a two-core matrix-transformer, as shown in Fig. 2.16, fundamental laws for the relationships between the winding currents and the winding voltages can be derived, according to

$$N_{\mathrm{PFC}} \cdot I_{\mathrm{PFC}} = N_{\mathrm{LV1}} \cdot I_{\mathrm{LV1}} = N_{\mathrm{LV2}} \cdot I_{\mathrm{LV2}} \tag{2.15}$$

and

$$\Phi_{\mathrm{tot}} = \Phi_1 + \Phi_2 \rightarrow \frac{\Psi_{\mathrm{PFC}}}{N_{\mathrm{PFC}}} = \frac{\Psi_{\mathrm{LV1}}}{N_{\mathrm{LV1}}} + \frac{\Psi_{\mathrm{LV2}}}{N_{\mathrm{LV2}}}, \tag{2.16}$$

where for the sake of simplicity, it is assumed that $R_{\mathrm{m1}} = R_{\mathrm{m2}}$ and $R_{\sigma 1} = R_{\sigma 2} = 0$. The assumption of equal magnetizing reluctances and vanishing leakage reluctances is feasible, as long as a symmetric sub-core arrangement is chosen and $R_{\sigma \mathrm{x}} \ll R_{\mathrm{mx}}, x \in \{1, 2\}$. Based on (2.16), the transformer-internal relationships between the winding voltages can be calculated, according to

$$\frac{1}{N_{\mathrm{PFC}}} \frac{\mathrm{d}(\Psi_{\mathrm{PFC}})}{\mathrm{d}t} = \frac{1}{N_{\mathrm{LV}}} \frac{\mathrm{d}(\Psi_{\mathrm{LV1}} + \Psi_{\mathrm{LV2}})}{\mathrm{d}t} \rightarrow \frac{V_{\mathrm{PFC}}}{N_{\mathrm{PFC}}} = \frac{1}{N_{\mathrm{LV}}} \left(V_{\mathrm{LV1}} + V_{\mathrm{LV2}} \right), \tag{2.17}$$

where $N_{\mathrm{LV}} = N_{\mathrm{LV1}} = N_{\mathrm{LV2}}$. Thus, in magnetically parallel-connected sub-transformer structures, as e.g. shown in Fig. 2.15a, different voltages V_{LV1} and V_{LV2} can be induced in the LV windings, whereas the currents I_{LV1} and I_{LV2} are forced to be the same. This is possible, as the ratio between V_{LV1} and V_{LV2} is automatically adapted to potential unequal resistances of the LV current paths of LV winding 1 and LV winding 2, such that $I_{\mathrm{LV1}} = I_{\mathrm{LV2}}$ holds at all times.
This natural balancing of the LV-side output currents in matrix-transformers

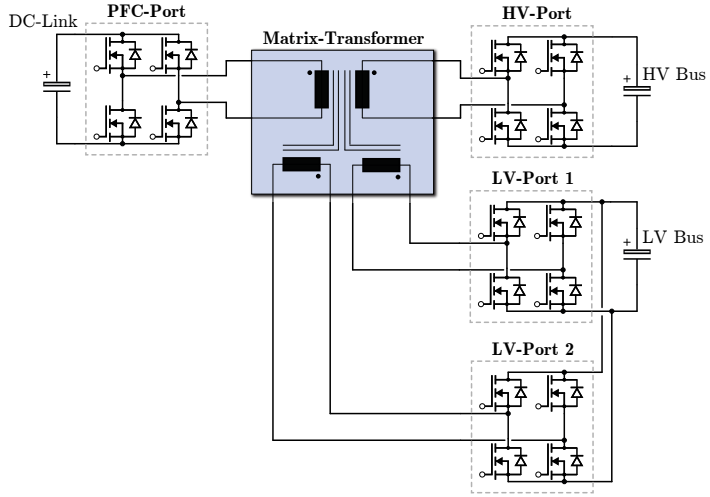


Fig. 2.17: Simplified circuit of a triple-active-bridge using a matrix-transformer with two parallel-connected LV converter ports.

therefore allows for a parallel connection of multiple LV ports, without an additional active current balancing control.

The complete circuit diagram of a TAB with matrix-transformer is shown in Fig. 2.17, where the two LV full-bridges are connected in parallel and are driven synchronously, as previously mentioned. For this reason, the control of this topology does not differ from the one of a conventional TAB and the control strategy of Section 2.1 can be adopted.
In comparison to the MPMC converter, this topology relies again on high-voltage semiconductors, due to the missing physical splitting of the high-voltage (PFC and HV) ports. However, the total number of full-bridges in the converter can be reduced, yielding a lower overall circuit complexity, while still profiting from the MPMC benefits on the LV side.

However, all these conventional topological solutions cannot avoid the main issues of the TAB topology (and of many other conventional three-port DC/DC converter topologies) as on the one hand, the control is comparably complex, as a variation of one of the six control parameters $D_{\mathrm{A,B,C}}$, φ_{AB}, φ_{AC} or f_{s} always affects all three converter ports, whereby they are mutually coupled.

On the other hand, an active switching of comparably large currents on the LV side cannot be avoided, even if multiple LV-side converter ports are used. Hence, even theoretically soft-switched semiconductors induce substantial switching losses, if the zero-voltage-switching (ZVS) current is too large.
In addition, the wide port voltage variations demand for very large leakage inductance values $L_{\sigma,X}$ in order to guarantee an efficient power transfer for all possible port voltage combinations. This is a particular disadvantage, keeping in mind the targeted cost-effective PCB integration of the transformer windings, as it is extremely difficult to achieve large leakage inductances in PCB-winding transformers (cf. Appendix C).
Unfortunately, the last two drawbacks are counteracting, as a reduction of the inductance values demands for a high switching frequency, which for its part leads to increased switching losses in the LV port. Hence, there is no possibility of mitigating both disadvantages at the same time.

In order to estimate the severity of these issues in a real converter system, a 1.2 kW TAB hardware demonstrator has been built according to the specifications for a single converter cell of a MPMC converter with overall three converter cells (cf. Tab. 2.2). This hardware prototype has mainly been used to investigate the influence of the parasitic elements on the occurring switching losses in a real hardware design, as well as for testing different PCB-integrated transformer designs, as will be discussed in the following.

2.3 Triple-Active-Bridge Hardware Demonstrator

The TAB hardware demonstrator has been built according to the project specifications, as one converter cell of a three-port three-cell TAB converter. Hence, each cell needs to deliver only one third of the LV output current and the semiconductors in the PFC and the HV ports need only one third of the initial breakdown voltage rating (cf. Tab. 2.2). For this reason, 200 V GaN switches can be employed, which can be used for both, hard as well as soft switched converter operation. This is especially important as, depending on the performance of the switches on the LV side, the top priority should be changed from minimal conduction losses and ZVS of all power semiconductors, to minimized switching currents in the LV port. Consequently, in order to achieve reasonable conduction losses, the PFC and the HV ports might need to be operated under hard switching conditions, such that the overall

Tab. 2.2: Specifications of the TAB converter cell hardware demonstrator.

	PFC Port	HV Port	LV Port
Port Voltage	166 V	83...166 V	10.5...15 V
RMS Port Current	7.2 A_{RMS}	12 A_{RMS}	66.6 A_{RMS}
Port Power	1.2 kW	1.2 kW	1 kW

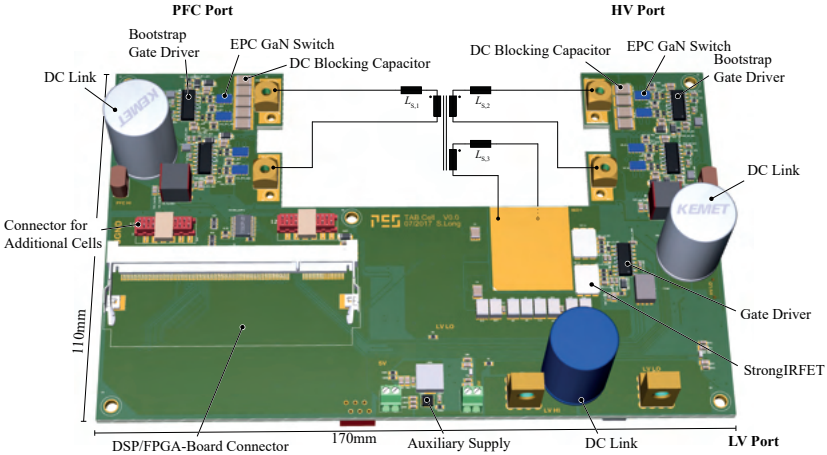


Fig. 2.18: 3D model of the TAB development board, comprising the three full-bridges with their gate drive circuits, multiple auxiliary supplies and a connector for the DSP/FPGA controller board. Different transformer designs can be connected to the development board via screwed fittings.

converter losses can be kept as small as possible.

In Fig. 2.18, the 3D drawing of the TAB development board is shown. It can easily be seen, that the PCB is not designed for high power density, as on the one hand, the large PCB increases the cooling surface of the converter, whereby additional heat sinks can be avoided such that all the power components can easily be accessed and the debugging in general is facilitated. On the other hand, the PCB tracks in the LV port are over-dimensioned in order to provide a large copper cross-section for the LV-side currents.
Tab. 2.3 lists the most important components used in the TAB prototype, where the two current sensors ACS780 (LV) and ACS724 (HV) are used for

Tab. 2.3: Main components used in the TAB hardware prototype.

Part No.	Description
EPC2034	200V eGaN Enhancement Mode Power Transistor 10 mΩ
Si8274	Bootstrap Gate Driver
IRL7472L	40V StrongIRFET 375A, 0.52 mΩ
ACS780	Allegro Hall-Effect Current Sensor 100A, 120kHz
ACS724	Allegro Hall-Effect Current Sensor +/-30A, 120kHz
ACS730	Allegro Hall-Effect Current Sensor +/-50A, 1MHz

the control, as during charge operation, either a constant output voltage or a constant output current is required. In addition, the high bandwidth current sensor ACS730 is used as overcurrent detector, which is placed in the current path of the HV winding and prevents damaging of the system in case of saturation of the transformer core.
Besides the power semiconductors, the most important component in the TAB is the three-winding transformer, whose design is discussed in detail in the following.

2.3.1 TAB Transformer Design

The difficulty in the transformer design for this topology lies in the large required series inductance values $L_{\sigma,X}$ of the system, as for the sake of high power density, these series inductances should be integrated in the three-winding transformer by increasing the leakage inductance values of the different windings. However, due to the close coupling between the windings in a PCB transformer, this is not an easy task and some sophisticated approaches need to be used. Two possible approaches are investigated and discussed in the following sections, where either a single ferrite core, or multiple separated ferrite cores are used.

Single Core PCB Transformer Design

The main goal of each PCB-winding transformer design should be to guarantee vertically aligned current flow in the different windings, in order to achieve a homogeneous current distribution within the windings and, therefore, minimum overall conduction losses. The vertical alignment of the windings is key for a high efficiency, as it results in a mutual compensation of the vertical

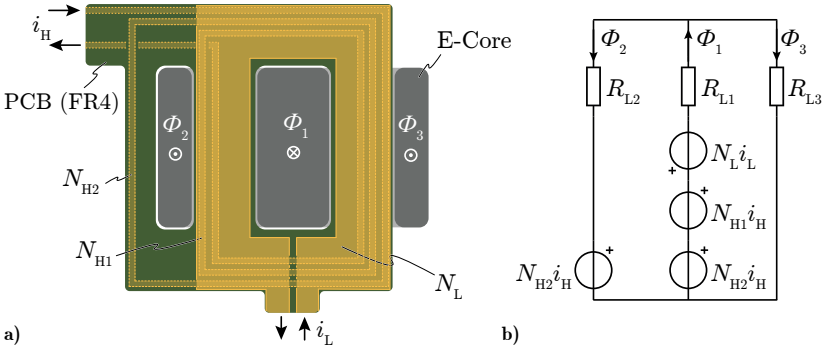


Fig. 2.19: a) Two-winding transformer design with a partially redistributed high-voltage winding, in order to increase the overall leakage inductance. **b)** The corresponding reluctance model of the transformer arrangement of **a)**.

parasitic magnetic proximity fields around the windings, whereby an AC to DC resistance ratio of almost one can be achieved, as will be explained in a later chapter.
Consequently, a complete separation of the different windings is disadvantageous, as the skin and the proximity effects force the current to flow only at the outer edges of a winding track, resulting in an extremely low copper utilization. This is especially problematic for very high currents in a single-turn winding (as given in this application), where a large effective copper cross-section is usually required.

With this in mind, a winding approach was investigated, where a certain fraction of the total number of turns is wound around two instead of just one leg of a conventional E-core. This arrangement is shown in Fig. 2.19a based on a two winding transformer example, with a total number of turns of $N_{H1} + N_{H2}$ and N_{LV} on the HV and the LV side, respectively. Hence, the main parts of the windings are vertically aligned, and only a small fraction of the number of turns of the HV winding is separated. However, due to the much thinner track widths of the HV winding, the skin and proximity effects in these turns are less pronounced, whereby the increase in conduction losses is almost negligible.
The equivalent reluctance model of Fig. 2.19b for this winding arrangement

allows for deriving the following expressions:

$$\frac{i_\mathrm{L}}{i_\mathrm{H}} = \frac{(N_\mathrm{H1}+N_\mathrm{H2})R_\mathrm{L2}+N_\mathrm{H1}R_\mathrm{L3}}{(R_\mathrm{L2}+R_\mathrm{L3})N_\mathrm{L}} \xrightarrow{R_\mathrm{L2}=R_\mathrm{L3}} \frac{i_\mathrm{L}}{i_\mathrm{H}} = \frac{2N_\mathrm{H1}+N_\mathrm{H2}}{2N_\mathrm{L}} \tag{2.18}$$

$$L_{\sigma\mathrm{H}} = \frac{N_\mathrm{H2}^2}{R_\mathrm{L2}+R_\mathrm{L3}} \qquad L_\mathrm{mH} = \frac{1}{4}\frac{(2N_\mathrm{H1}+N_\mathrm{H2})^2}{R_\mathrm{L1}+\frac{R_\mathrm{L2}R_\mathrm{L3}}{R_\mathrm{L2}+R_\mathrm{L3}}} \tag{2.19}$$

$$R_\mathrm{Lx} = \frac{l_\mathrm{agx}}{\mu_0 A_\mathrm{Ex}} \quad \text{with} \quad x \in \{1,2,3\}. \tag{2.20}$$

These equations show some interesting characteristics for this type of transformer. On the one hand, assuming a constant total air gap of $l_\mathrm{ag,tot} = l_\mathrm{ag2}+l_\mathrm{ag3}$, the current transfer ratio can be changed linearly by changing the distribution of $l_\mathrm{ag,tot}$ among l_ag2 and l_ag3, without affecting the leakage inductance $L_{\sigma\mathrm{H}}$ of the HV winding. On the other hand, the leakage inductance of the HV winding can be varied by changing the total air gap $l_\mathrm{ag,tot}$ without influencing the current transfer ratio (at least for a constant air gap ratio $l_\mathrm{ag2}/l_\mathrm{ag3}$). The aforementioned dependencies are illustrated in Fig. 2.20 for a three-winding transformer example.

Even though this winding arrangement allows for arbitrary leakage inductance values and current transfer ratios, it usually requires a very precisely manufactured custom transformer core, as the leakage flux is flowing in the outer legs of the E-core, whereby larger core areas A_E2 and A_E3 need to be provided. Furthermore, a precise implementation of different air gap lengths in the three transformer core legs is extremely challenging, if the required air gaps are small and a homogeneous flux density in the ferrite core should be achieved. Unfortunately, the manufacturing of such a custom transformer core takes a long time and is very expensive, which is why the transformer structure has slightly been adapted, such that commercially available ferrite cores can be used, while the advantages of the aforementioned transformer structure remain.
The design of this adapted multi-core transformer is discussed in the following section.

Multi-Core PCB Transformer Design

In comparison to the single-core transformer of the previous section, the multi-core transformer provides separate ferrite cores for both leakage flux paths (HV and PFC) as well as the magnetizing flux (LV, HV and PFC). Hence,

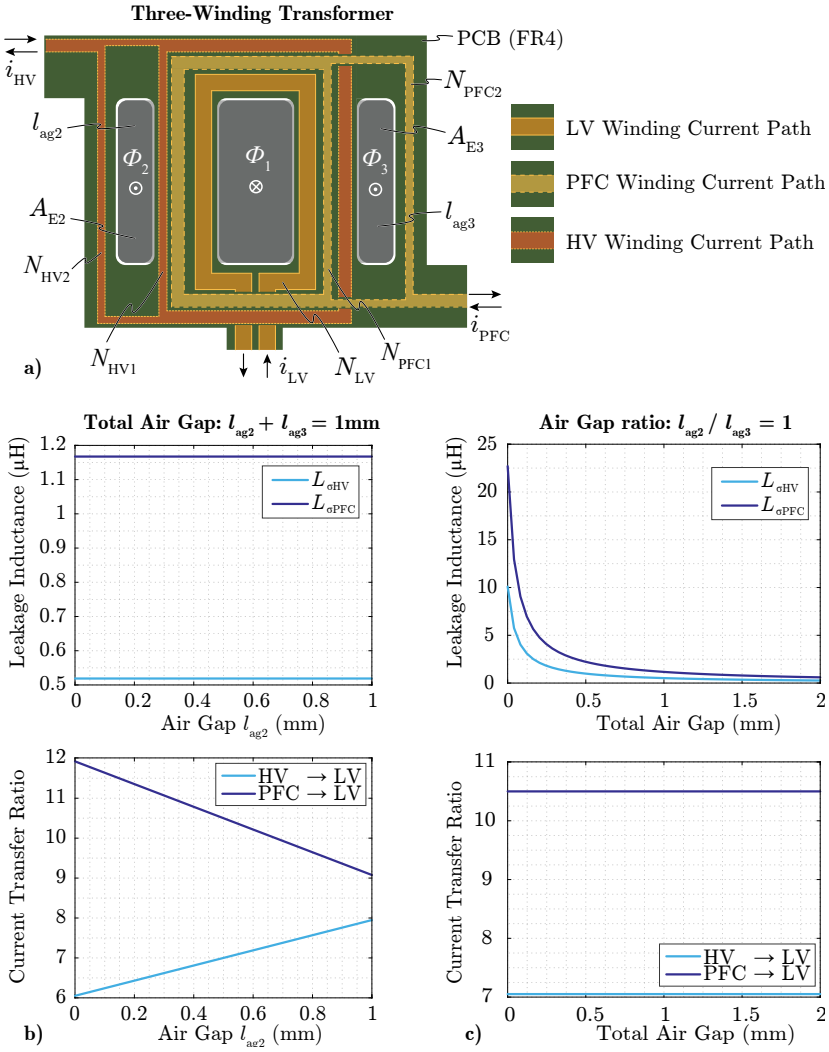


Fig. 2.20: a) Three-winding transformer example with partially redistributed PFC and HV windings, in order to increase their leakage inductance values. For the sake of clarity, the windings are drawn side by side instead of vertically aligned. **b)** Leakage inductance values and current transfer ratios for a constant total air gap and a varying ratio between l_{ag2} and l_{ag3}. **c)** Leakage inductance values and current transfer ratios for a varying total air gap and a constant air gap ratio l_{ag2}/l_{ag3}.

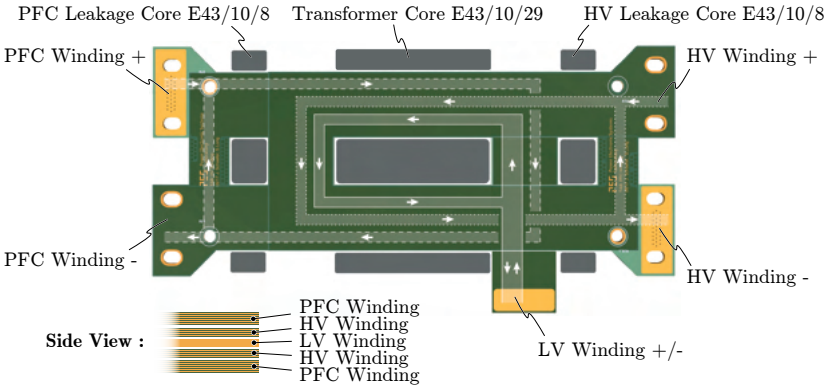


Fig. 2.21: Three-winding PCB transformer arrangement for large leakage inductance values, which are required for efficient power transfer in TAB converter systems. The transformer comprises four stacked PCBs (PFC winding 1 and 2 as well as HV winding 1 and 2) with a copper foil in between, where each PCB contains either half of the PFC turns n_{PFC} or half of the HV turns n_{HV}, respectively. The copper foil is used to form the single turn of the LV winding. On top of the windings, the accumulated current paths of the three winding currents are shown, in order simplify the identification of winding sections where the sum of the three currents cancels out and, therefore, very low HF winding losses can be expected.

Tab. 2.4: Specifications of the Transformer Prototype of Fig. 2.21.

Description	N_{PFC}	N_{HV}	N_{LV}	$L_{\sigma\mathrm{PFC}}$	$L_{\sigma\mathrm{HV}}$
Value	12	8	1	18 µH	7 µH

this approach allows for designing each core separately, as the magnetic fluxes are decoupled. Consequently, the different cores can be made of conventional ferrite core shapes, and their individual air gaps can easily be adapted afterwards. The structure of the multi-core transformer, which was finally used in the TAB prototype, is shown in Fig. 2.21. It comprises five PCBs and three ferrite cores as illustrated in the aforementioned figure. The main benefit of this design is its modularity, as the air gaps of the different cores can easily be adjusted and, in addition, the winding PCBs can be exchanged if necessary, as the whole setup is screwed together instead of being soldered.

The specifications of the transformer prototype are listed in Tab. 2.4 and the corresponding measurements of the leakage inductance values of the hardware prototype are shown in Fig. 2.22. The negative inductance of the LV winding originates from the simplified transformer model of the TAB, hence the star connection of the three leakage inductances $L_{\sigma,\mathrm{PFC}}$, $L_{\sigma,\mathrm{HV}}$ and $L_{\sigma,\mathrm{LV}}$, as shown in Fig. 2.3a.
Besides the three leakage inductance values, the measured total inductance $L_{\mathrm{PFC}\rightarrow\mathrm{HV}}$ and resistance $R_{\mathrm{PFC}\rightarrow\mathrm{HV}}$ from the PFC to the HV winding are shown. It can easily be seen, that the resistance of the two windings rapidly increases with the switching frequency, which is one of the biggest issues in PCB transformers with large required leakage inductances, as will be discussed in the following.

In order to generate a certain leakage flux in a winding, it is inevitable to leave the vertically aligned current flow at some point, such that the leakage flux can flow between the different windings. Unfortunately, in this part of the winding, where the coplanar complementary current is missing, the current distribution is very inhomogeneous, as (due to the skin and proximity effects) most of the current is flowing at the two edges of the copper track, regardless of the track-width (cf. Fig. 2.23a). This drawback cannot be avoided, but it can be reduced to a certain extent by providing a floating copper layer on top or at the bottom of the winding. This floating layer allows an eddy current to flow in the opposite direction to the actual winding current,

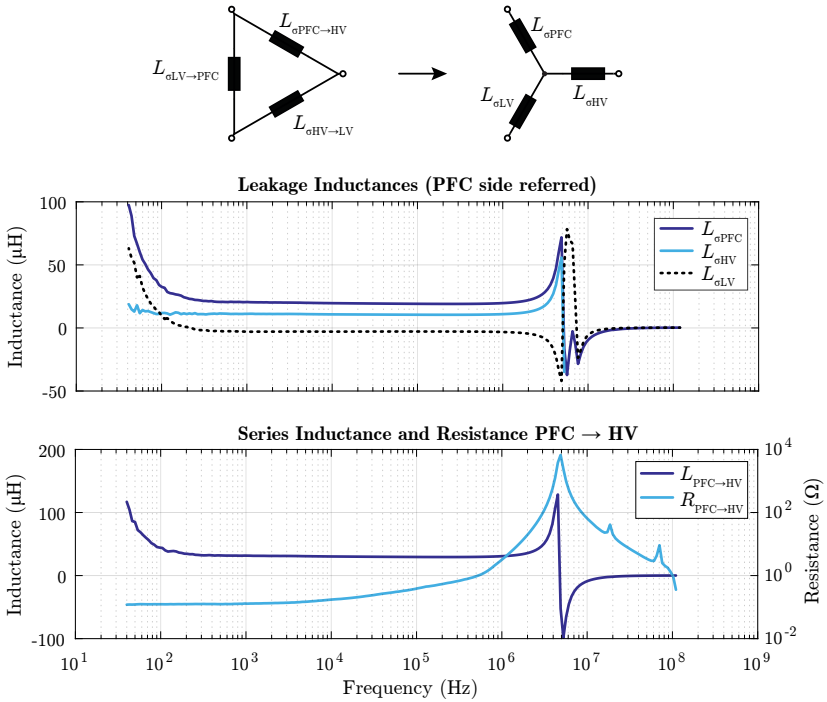


Fig. 2.22: Leakage inductance values of the three transformer windings, which were derived by applying the delta-star transformation on the actually measured inductance values $L_{X \to Y}$, $X, Y \in \{\text{PFC, HV, LV}\}$. Thereby, $L_{X \to Y}$ denotes the measured inductance at the winding X for a shorted winding Y (and an open third winding). In addition, the total inductance and the total resistance of the power path from the PFC to the HV port are shown, where the total impedance of the transformer has been measured on the PFC side for a shorted HV winding and an open LV winding.

whereby an almost homogeneous current distribution in the winding can be achieved (cf. Fig. 2.23b-c). Even though the additional eddy currents induce conduction losses in the floating copper layer, the overall conduction losses can considerably be reduced, if the track-width of the winding is much wider than two times the skin depth.

The complete setup of the TAB hardware prototype is shown in Fig. 2.24a, including the assembled aforementioned PCB-winding transformer. As shown in Fig. 2.24b, the PCB temperature of the leakage paths, even during partial-load operation, is extremely high compared to the rest of the circuit, no matter if the aforementioned floating copper layers are employed or not. Consequently, besides the aforementioned skin and proximity effect, there needs to be another loss mechanism effective in the leakage paths of the winding, in order to explain the high temperature and, therefore, the occurring losses in these PCB sections. This loss mechanism is investigated in the following in more detail.

Even though the negative effects due to the skin and proximity fields can effectively be mitigated by means of vertically aligned floating copper layers, the negative effect of the third magnetic field component, namely the fringing field around the air gap of the leakage cores, cannot be avoided. Hence, as in the TAB hardware demonstrator, two small E-cores are used as leakage cores, which are separated by a certain air gap l_{ag}, the air gap is inherently located in the same physical layer as the PCB-windings (cf. Fig. 2.25a). Consequently, a large part of the fringing field around the air gap directly penetrates the PCB-windings, whereby significant eddy currents and, therefore, additional conduction losses are induced. This is the main reason, why in Fig. 2.24b the PCB temperature of the leakage paths is significantly higher than the temperature of the rest of the converter.
Consequently, a different approach is in demand, where the negative impact of the fringing field around the air gap on the overall conduction losses can be minimized. For this reason, the location of the air gap needs to be changed, such that the amount of penetrating fringing field can be reduced. Surprisingly, it has been found, that a relocation of the air gap to the top and to the bottom of the winding not only reduces the negative effect of the fringing field on the occurring conduction losses, but it can be noticed, that the fringing field even has a beneficial impact on the AC-resistance of the PCB tracks, as with an appropriate positioning, the fringing field acts like a vertically aligned complementary current (cf. Fig. 2.25b). Thus, the

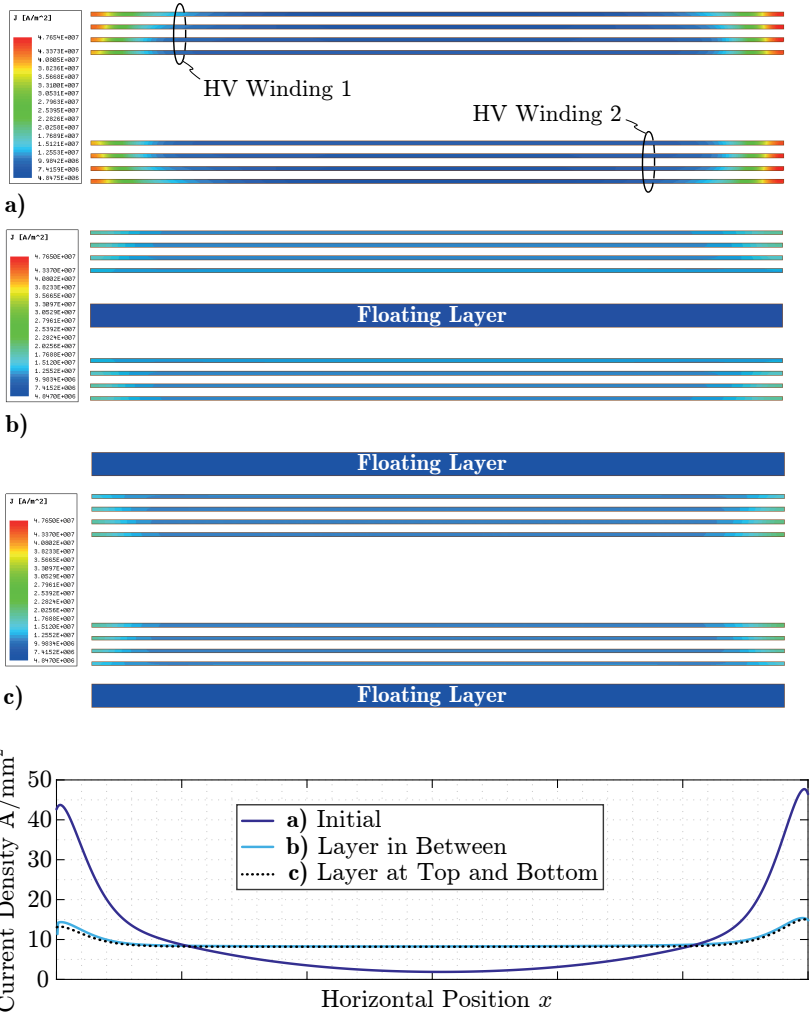


Fig. 2.23: Current distribution in the HV winding in the leakage path for **a)** the standard arrangement, **b)** a floating copper layer in between the PCB and **c)** with two floating copper layers on top and on the bottom of the PCB-windings for a winding width of 5 mm, a frequency of 100 kHz and a total HV current of 28 A.

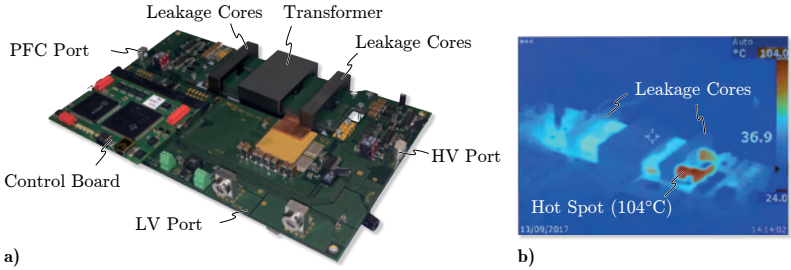


Fig. 2.24: a) The fully assembled TAB hardware prototype, including the assembled PCB-winding transformer of Fig. 2.21 and the DSP control board. **b)** Thermal image of the converter for partial-load operation with $V_{\mathrm{PFC}} = 166\,\mathrm{V}$, $V_{\mathrm{HV}} = 166\,\mathrm{V}$, $V_{\mathrm{LV}} = 15\,\mathrm{V}$, $P_{\mathrm{HV}} = 400\,\mathrm{W}$ and $P_{\mathrm{LV}} = 100\,\mathrm{W}$.

fringing field effectively compensates the skin and proximity fields, whereby the aforementioned floating copper layers are redundant and can be removed. This concept of using the fringing field around an air gap to actively compensate adverse skin and proximity fields in a conductor is investigated in detail in Chapter 3 (cf. compensating fringing field concept, CFFC) and is therefore not explained any further here.

However, the effectiveness of the concept can easily be seen based on the efficiency measurements of the TAB hardware demonstrator with and without the relocation of the air gaps during charge mode operation, hence, with a main power flow from the PFC to the HV port and only a small power flow from the PFC to the LV port ($P_{\mathrm{LV}} = 100\,\mathrm{W}$) (cf. Fig. 2.26). The utilization of the adapted leakage core design yields a full-load efficiency increase of 1.71 %, which corresponds to a loss-reduction of 18 W. Especially regarding the comparably short length of the leakage winding, this loss-saving is significant, which is why the compensating fringing field concept (CFFC) is considered to be very promising, not only for the application in the proposed integrated planar magnetics, but also considering a potential PCB-integration of the windings of discrete inductors.

Unfortunately, even though the efficiency could be improved by means of the CFFC, the target efficiency of 95 % at full load was just missed, mainly due to the occurring soft-switching losses in the LV port, which have been strongly underestimated in the theoretical calculations. Hence, the LV semiconductors

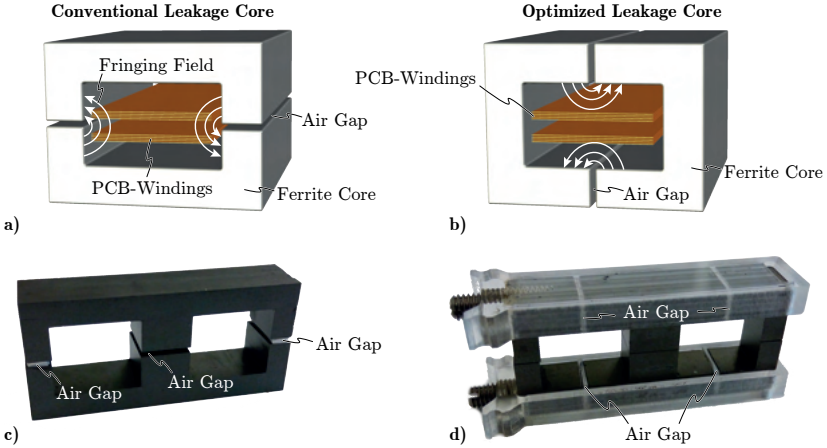


Fig. 2.25: Simplified 3D model of the leakage core arrangement with **a)** the air gaps in the same physical layer as the windings and **b)** the air gaps positioned perpendicularly to the windings. The respective hardware implementations are shown in **c)** and **d)**.

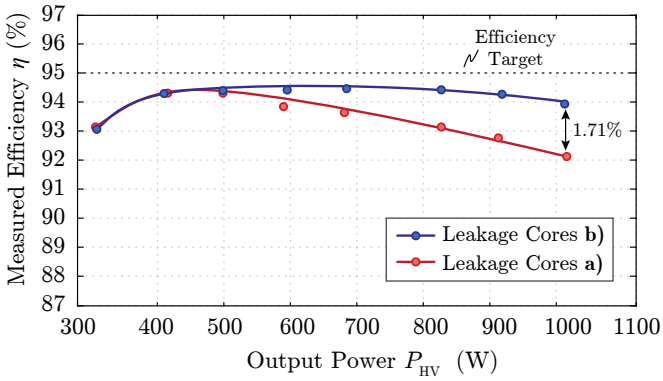


Fig. 2.26: Measured efficiencies of the TAB hardware prototype for charge mode operation with $V_{PFC} = 166\,V$, $V_{HV} = 166\,V$, $V_{LV} = 15\,V$, $P_{LV} = 100\,W$ and a variable HV output power P_{HV} for **a)** the leakage cores shown in Fig. 2.25c and **b)** the leakage cores shown in Fig. 2.25d.

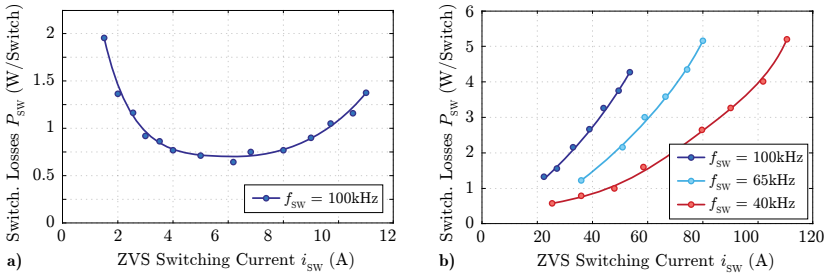


Fig. 2.27: a) Experimentally measured switching losses of the PFC and the HV-side semiconductors (EPC2034) for a switching frequency of 100 kHz and a drain-source voltage V_{DS} of 166 V and **b)** the same measurement results for the LV-side semiconductors (IRL7472L) with a V_{DS} of 15 V and different switching frequencies.

cause substantial soft-switching losses if the switch-node currents exceed a certain value. This is a severe issue in the application at hand, as for many operating points, it is impossible to avoid large LV-side switch-node currents during the switching transitions on the LV side. In order to quantify the ZVS losses of the semiconductors, the occurring losses have been measured for both switches (HV and LV) and different switch-node currents (cf. Fig. 2.27). The ZVS performance of the 200 V EPC GaN semiconductors is extremely good, up to the maximum ZVS currents ($\approx$ 12 A) which will ever occur in the system. However, the ZVS losses of the LV silicon MOSFETs are increasing extremely fast with increasing switch-node currents, whereby the allowable switching frequency in a TAB, with at least one low characteristic impedance port, is strongly limited. Hence, for e.g. the switching frequency of the hardware demonstrator (100 kHz) and an average ZVS current of 50 A, more than 4 W of switching losses are generated per switch. Consequently, the efficiency could only be increased, if a lower switching frequency would be used, whereby the volume of the inductive components would be significantly increased.

However, due to a targeted high power density and low manufacturing costs, this is not feasible, which is why different, new topologies need to be developed. These topologies are ”tailored” to the application, such that the arising challenges of the TAB topology can be circumvented. Hence, the new topologies should be developed in consideration of the following aspects:

- The magnitudes of the currents in the LV semiconductors during the switching operations should be minimized, in order to avoid the ZVS losses of these semiconductors (cf. Fig. 2.27b). Consequently, the ideal topology for the LV converter port is a synchronous rectifier, as ZVS and ZCS are ensured, whereby the LV-side switching transitions can assumed to be loss-less. However, if a synchronous rectifier cannot be used, the ZVS currents should at least be limited to values below $\approx 20\,\mathrm{A}$, in order to avoid unnecessary switching losses, whereby high switching frequencies can be used.

- In the final application, a switching frequency much higher than the 100 kHz of the TAB should be targeted, as the wide port voltage variations inherently result in large voltage differences between the converter ports. These voltage differences are usually directly applied across a certain inductive component (as e.g. in a DAB, TAB or a resonant converter), whereby the effective voltage time areas across these inductors are inversely proportional to the switching frequency. Hence, in order to keep a certain controllability of the inductor current (and therefore limited current gradients) even for large voltage differences between the converter ports, either a high switching frequency or a comparably large inductance is required, which, however, is directly related to the volume of the magnetic components in the converter system.
  As an example, in the TAB hardware prototype, the required series-inductance between the PFC and the HV port for $f_{\mathrm{sw}} = 100\,\mathrm{kHz}$ is $L_{\sigma,\mathrm{PFC}\rightarrow\mathrm{HV}} = 32\,\mu\mathrm{H}$, even though the port voltages are reduced by a factor of 3, as 3 cells are employed. Thus, in a single-cell converter, the required inductance would be significantly higher, which would result in huge magnetic components. Consequently, a high switching frequency is always preferred, if reasonable from an efficiency perspective (switching losses).

- The large number of control variables in a TAB, which all have an influence on all port power values, makes it extremely difficult to develop a simple and stable control, which guarantees a reliable and efficient converter operation under all operating conditions. Consequently, the new topology should be controllable by means of an as simple as possible controller, whereby ideally, a completely decoupled power flow between the different converter ports should be achieved. Hence, a load step or a voltage step in one port should by no means affect the

power flow in the respective other port, and vice versa. This would increase the probability for the topology of being applied in an industrial application.

- In order to minimize the harmonic content of the port currents and, therefore, the HF winding losses in the magnetic components, sinusoidal transformer currents should be targeted, as this is the most efficient way of transmitting power at a high frequency.
- Lastly, the derived compensating fringing field concept (CFFC) should be employed, wherever discrete inductors are required. By using this concept, the inductor windings can be integrated into the PCB very efficiently, whereby their volume and their manufacturing costs can be minimized.

2.4 Summary of the Chapter

In this chapter, the conventional triple-active-bridge (TAB) topology has been investigated and its suitability for the application at hand has been discussed. It was found, that a single TAB converter cannot be used in an efficient way due to multiple reasons, as e.g. ZVS losses in the LV power switches, a large reactive power flow (for port voltage ratios which deviate from the turns ratio of the transformer), a high harmonic content in the transformer currents and large required inductance values of the series inductors. Consequently, two alternative topological solutions have been investigated, namely a two-stage converter comprising a TAB and a subsequent non-isolated DC/DC converter between the HV port of the TAB and the HV battery, as well as a multi-cell approach, where multiple TAB converters are interconnected in a beneficial way. However, both topological solutions cannot resolve all the issues of the TAB topology, which has finally been verified by means of a 1 kW hardware prototype.
Based on the findings of the investigations of the TAB, the most important aspects of a theoretically ideal topology for the application at hand have been summarized, which are used in the course of this work as a basis for the derivation of novel converter topologies, "tailored" to the specifications of the combined charger/step-down converter. The new topologies, which try to implement the aforementioned aspects, are subject of Chapter 4, Chapter 5 and Chapter 6.
Furthermore, it has been found, that in the design process of PCB-integrated inductive components the fringing field around air gaps can be actively used

to achieve extremely low HF conduction losses in the respective windings. Hence, cost-effective and power-dense inductive components can be built, which widens the design space of possible converter topologies for this application significantly. This concept is called compensating fringing field concept (CFFC) and is investigated in more detail in Chapter 3.

3

Design of Cost-Effective and Power-Dense PCB-Winding Inductors

Chapter Abstract

Especially in the automotive sector, the design of power electronic converters is subject to extreme cost pressure. Consequently, each component needs to be optimized regarding material and manufacturing cost, whereby the latter is especially important for magnetic components, as the expensive wire-wrapping process has a significant impact on the overall production costs. In this chapter, a new inductor design concept is proposed, where the winding is directly integrated into the printed-circuit-board (PCB), while at the same time the usually large high-frequency conduction losses are mitigated. This is achieved by using the fringing field around a single air gap or around several (distributed) air gaps for compensating the adverse magnetic skin and proximity fields within the winding. Consequently, low AC to DC resistance ratios are achieved and the required copper cross-section of the winding can effectively be reduced. Furthermore, a thermal model for the PCB-winding is derived, which allows for designing PCB-windings close to the thermal limit, whereby inductors with very high power densities are obtained. Finally, the findings of this chapter are verified by means of various experimental measurements and simplified design guidelines are provided.

3.1 Design Challenges in Conventional Inductor Arrangements

Inductors are used in a variety of electronic applications and especially in the area of power electronic converter systems, where they are usually employed as filter components in order to attenuate the switching frequency output voltage ripple, e.g. of buck converter topologies [26] [27]. Hence, the inductive components need to be designed in such a way that they can handle a certain required maximum output current, whereby an appropriate copper cross-section of the winding needs to be provided in order to limit the occurring ohmic losses in the inductor winding. However, especially in high-power low-voltage (LV) applications, these inductor currents can be huge and, therefore, large copper cross-sections A_{cu}, as e.g. achieved using wide copper bars or solid conductor windings, are required. However, to achieve a high power density, it is important to obtain a homogeneous current density throughout A_{cu}, in order to optimally use the employed copper material and, therefore, maximize the effective copper cross-sectional area $A_{\mathrm{cu,eff}}$ of the winding. Unfortunately, a homogeneous current density is difficult to achieve, since due to the high-frequency (HF) current components resulting from the switching frequency, different parasitic effects come into play, which deflect the current towards the surface or edges of the conductor and, thereby, reduce the effective $A_{\mathrm{cu,eff}}$. These parasitic HF effects can be divided into three main components: First, the skin effect, which characterizes the impact of the magnetic field H_{skin} of a HF current in a conductor on its own conductivity, second, the proximity effect, which describes the mutual influence of the magnetic fields H_{prox} of multiple current carrying conductors on their individual current distributions and lastly the third component, which originates from the impact of the fringing field H_{ag} around an air gap of the magnetic circuit on conductors in its near vicinity [28]. Hence, if H_{ag} penetrates a conductive material, it induces eddy currents according to the well-known law of induction and, therefore, acts similar to the aforementioned proximity effect (cf. Fig. 3.1).

These effects can be minimized in wire-wound inductors using litz wire, where multiple insulated thin copper strands are twisted in prescribed patterns, such that the flux linkages of all strands are equalized. As a result, the current splits equally among the individual wire strands and, due to their much smaller wire diameter, the skin effect caused by H_{skin} and the induced currents due to H_{prox} and H_{ag} in each strand can strongly be reduced [29–31]. Unfortunately, litz wire has some significant drawbacks compared to solid

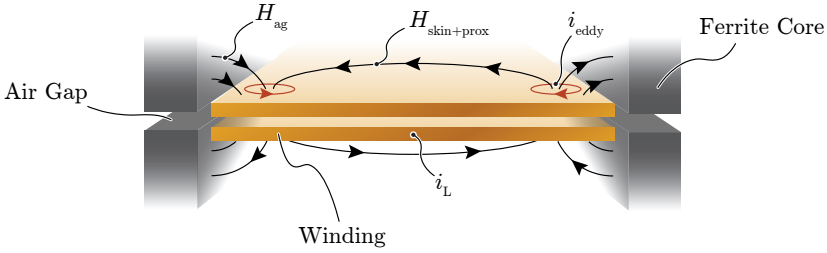


Fig. 3.1: Parasitic magnetic fields $H_{skin+prox}$ and H_{ag} in a conventional arrangement of a PCB-winding inductor, which are inducing eddy currents i_{eddy} in the conductor and, therefore, increase the total conduction losses.

copper conductors: The copper fill factor is comparably poor, as a significant amount of the available wire cross-sectional area is wasted due to the spaces between the strands and the required insulation of each individual strand. Furthermore, the allowable current density in litz wire is strongly limited due to its large thermal resistance orthogonal to the wire surface [32]. In cost driven applications, however, the most significant downside of litz wire windings is their price, since the costs per unit weight of litz wire are much higher than the ones of solid conductors [33]. Moreover, the wire-wrapping process and the termination of litz wire windings are challenging and also increase the manufacturing costs.

In industrial applications, solid conductor windings, and especially PCB-integrated windings, are therefore preferred, as they allow for much higher current densities (improved power density) and a cheap and simple manufacturing of inductors. However, as already mentioned, large conductive surfaces are prone to induced eddy currents due to external magnetic fields. For this reason, different approaches have been presented in literature, which all try to minimize the external magnetic fields penetrating the conductor. The most efficient approaches use two different concepts: The first option is to reduce the fringing field of the air gap by means of either using multiple smaller air gaps (quasidistributed air gap, cf. Fig. 3.2a) or by using a low permeability material (true distributed air gap, cf. Fig. 3.2b) [34]. Another possibility is to place the distributed air gaps perpendicular (z-direction) to the conductor, such that the main component of the resulting fringing field is heading into x-direction and therefore does not penetrate the conductor

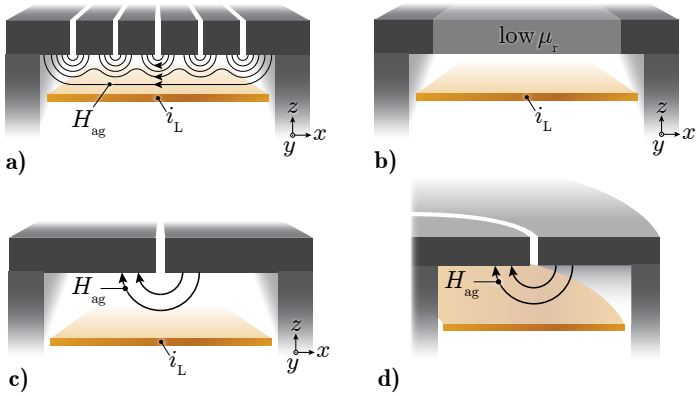


Fig. 3.2: Different air gap arrangements to reduce the ohmic losses in PCB-windings; e.g. **a)** multiple air gaps placed in parallel, i.e. in x-direction, along a straight conductor; **b)** distributed air gap using low permeability material. In **c)** and **d)**, single air gap arrangements along a straight and a circular conductor are shown.

perpendicular to its surface, i.e. in z-direction. Consequently, the HF losses due to the fringing field of the air gap can be minimized, as long as the distance between the air gap and the conductor is larger than a certain value [34].

However, the manufacturing of inductor cores with multiple air gaps and/or low permeability material is difficult and expensive, which is why a design with a single air gap is usually preferred in industrial applications. Furthermore, in the aforementioned considerations, the influence of the existing perpendicular skin and proximity fields are usually neglected, even though they lead to significant HF losses in a real conductor. For this reason, these fields are taken into account as well in this work, in order to end up with an optimized inductor geometry that ensures an almost frequency-independent current distribution and, therefore, optimal utilization of the cross section of the conductor. Thus, minimal HF losses in the windings and a high suitability for real implementations in efficient, power-dense and cost-driven applications are obtained.

In the next section, all aforementioned magnetic field components are derived by means of analytical and numerical calculations and, based on these derivations, a simple field compensation concept is introduced, which allows for partial active compensation of the skin and proximity fields in a straight

conductor using the fringing field of a single air gap placed perpendicularly to the conductor (cf. Fig. 3.2c). Hence, the AC resistance can be kept almost at the level of the DC resistance even for very high frequencies. Based on the findings of the investigation of a straight conductor, the concept is then applied to a more practice-oriented circular conductor arrangement (cf. Fig. 3.2d) and simple design guidelines are provided.

3.2 Field Compensation in Straight Conductors

The main challenge in the design of a highly efficient HF inductor winding is the minimization of its AC resistance R_{AC}, which is the same as striving for an AC to DC resistance factor F_{R} close to one:

$$F_{\mathrm{R}} = \frac{R_{\mathrm{AC}}}{R_{\mathrm{DC}}} \xrightarrow{\text{minimize}} F_{\mathrm{R,opt}} = 1. \tag{3.1}$$

Hence, assuming $F_{\mathrm{R}} = 1$ and according to

$$P_{\mathrm{cond}} = R_{\mathrm{DC}} F_{\mathrm{R}} I_{\mathrm{rms}}^2 = \int_{\mathrm{V}} \frac{J(x,y,z)^2}{\sigma} \mathrm{d}V, \tag{3.2}$$

the conduction losses in the winding do not change with frequency, what inherently implies that the current distribution $J(x, y, z)$ in a conductor should be frequency-independent as well. Thus, independent of the actual inductor geometry, the AC current density J_{AC} should be equal to its DC equivalent J_{DC} in order to minimize the AC-resistance R_{AC} and, therefore, also the conduction losses.

However, this is usually difficult to achieve, as various magnetic field components, summarized in $\vec{H}_{\mathrm{eddy}}$, penetrate the conductor and induce eddy currents according to

$$\nabla \times \vec{E} = -\mu_0 \frac{\partial \vec{H}_{\mathrm{eddy}}}{\partial t}, \tag{3.3}$$

wherefore a current displacement and an increased F_{R} value result.

In the following, the different field components contained in $\vec{H}_{\mathrm{eddy}}$ are analyzed based on the example arrangement of Fig. 3.3a, and their effects on the current distribution $J(x, y, z)$ are discussed.

The considered geometrical arrangement comprises an infinitesimally long straight conductor, surrounded by a ferrite core with a single air gap perpendicularly arranged to the top surface of the conductor, as illustrated in

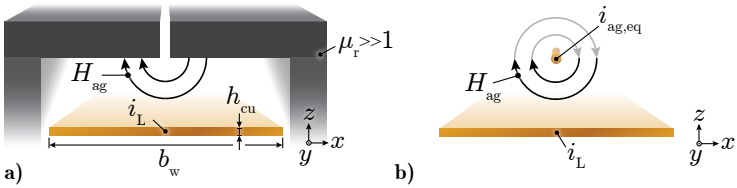


Fig. 3.3: a) Single air gap arrangement with the fringing field H_{ag} and **b)** its equivalent circuit where the fringing field H_{ag} is assumed to be induced by an equivalent current $i_{ag,eq}$.

Fig. 3.3a. Hence, the corresponding DC current density can be calculated according to

$$J_{DC}(x,z) = \frac{i_L}{h_{cu} \cdot b_w} \cdot \vec{e}_y, \tag{3.4}$$

where h_{cu} denotes the thickness and b_w the width of the copper track. However, in order to simplify the calculation of the various field components of $\vec{H}_{eddy}$, it is assumed that the thickness h_{cu} of the conductor is smaller than the skin depth of the considered frequency f_{sw}, whereby even for high-frequency currents an almost homogeneous current density in z-direction results. This assumption is usually valid for PCB-integrated inductor windings, where the copper layer thickness of the PCB with 35 µm...70 µm is smaller than the skin depth. Thus, an equivalent line current density J_{line} can be defined according to

$$J_{line}(x) = h_{cu} \cdot J_{DC}(x) = \frac{i_L}{b_w} \cdot \vec{e}_y, \tag{3.5}$$

emulating a current sheet with $h_{cu} \to 0$.
In order to achieve the desired $F_R = 1$, the same constant line current density obtained with DC currents should also be achieved for HF currents, requiring zero time-varying magnetic field inside the conductor, as otherwise a current displacement would result (cf. (3.3)).
However, in the inductor arrangement at hand, there are always two main magnetic field components penetrating the conductor in z-direction. On the one hand, the magnetic skin field $H_{z,skin}$ (cf. Fig. 3.4a), which originates from the current in the conductor and can be calculated according to Ampere's

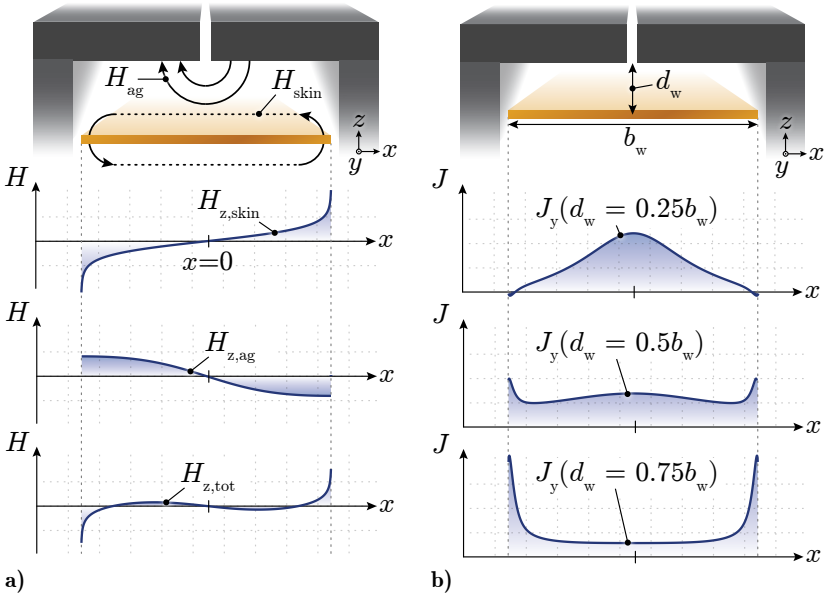


Fig. 3.4: a) Magnetic fields $H_{z,skin}$, $H_{z,ag}$ and $H_{z,tot}$, where only their components perpendicular to the conductor surface, i.e. in z-direction, are considered. Additionally, $H_{z,skin}$ corresponds to a homogeneous current distribution in the conductor and $H_{z,tot} = H_{z,skin} + H_{z,ag}$. **b)** shows the resulting HF current densities J_y for different distances d_w between the air gap and the conductor.

Law

$$H_{\mathrm{z,skin}}(x) = \int_{\frac{-b_\mathrm{w}}{2}}^{\frac{b_\mathrm{w}}{2}} \frac{J_\mathrm{line}}{2\pi(\alpha - x)} \mathrm{d}\alpha \tag{3.6}$$
$$= \frac{i_\mathrm{L}}{2\pi b_\mathrm{w}} \left(\ln\left(x + \frac{b_\mathrm{w}}{2} \right) - \ln\left(\frac{b_\mathrm{w}}{2} - x \right) \right) \cdot \vec{e}_\mathrm{z}.$$

On the other hand, the fringing field H_ag around the air gap, which can be derived according to [35], or for small air gaps even easier based on Fig. 3.4b, where the fringing field is assumed to be generated by an equivalent current $i_\mathrm{ag,eq} \approx 2i_\mathrm{L}$ [36]. The z-component of this magnetic field can therefore be calculated according to

$$H_\mathrm{z,ag}(x) = \frac{i_\mathrm{L}}{\pi} \cdot \frac{x}{d_\mathrm{w}^2 + x^2} \cdot \vec{e}_\mathrm{z}, \tag{3.7}$$

as shown in Fig. 3.4a. As can be noticed, both field components $H_\mathrm{z,skin}$ and $H_\mathrm{z,ag}$ are heading into opposite directions, whereby a partial mutual compensation of these fields can be observed. Consequently, the fringing field H_ag of the air gap counteracts the field of the skin effect H_skin, as the total magnetic field perpendicular to the conductor can be reduced according to

$$H_\mathrm{z,tot}(x) = H_\mathrm{z,skin}(x) + H_\mathrm{z,ag}(x). \tag{3.8}$$

However, as illustrated in Fig. 3.4b, the quality of the compensation, i.e. the distribution of the current density J_y, highly depends on the distance d_w between the conductor and the air gap, as for very small values of d_w, $H_\mathrm{z,ag}$ overcompensates $H_\mathrm{z,skin}$, whereby most of the current is attracted towards the middle of the conductor (dominating proximity effect), and for large values of d_w an undercompensation results and the current is pushed towards the edges of the conductor (dominating skin effect). Hence, there is an optimum distance $d_\mathrm{w,opt}$, where an almost homogeneous current distribution can be achieved and therefore a very low F_R value of close to one results.

There are different approaches to find this optimum value of d_w, as e.g. the finite element method (FEM), where the geometric arrangement of Fig. 3.3a is simulated for different values of d_w and different frequencies f_sw. The resulting AC to DC resistance factors F_R are shown in Fig. 3.5a, where two different regions can be defined: First, the proximity effect region for $d_\mathrm{w,norm} < 0.5$, where the fringing field of the air gap pulls the current towards the center of the conductor and second, the skin effect region for $d_\mathrm{w,norm} > 0.5$, where the

fringing field of the air gap cannot compensate the skin field anymore and the current flows at the edges of the conductor only. In Fig. 3.5b, these two regions are depicted in more detail for different frequencies f_{sw} and different discrete distances d_w at ①...⑥.
On the left side, the F_R-values for three different $d_{w,norm}$ at ①...③ in the proximity region are shown. For low frequencies f_{sw}, the proximity losses are strongly increasing with f_{sw}, as the current distribution is getting more and more triangularly shaped. However, the current is pulled towards a region with a very low perpendicular magnetic field $H_{z,tot}$ (cf. Fig. 3.4a), which is why the losses do no longer significantly increase with frequency, once all the current is in this "low-field-region".
On the right-hand side, the F_R-values for the three different $d_{w,norm}$ at ④...⑥ in the skin region are shown. As the current is pushed towards the edges of the conductor, where the highest magnetic fields occur, the conduction losses are constantly increasing with frequency with the well-known $\sqrt{f_{sw}}$ dependency.
However, between the two regions, where the optimal air gap position can be found, the F_R value is less than 1.1 even for very high frequencies. Consequently, an almost homogeneous current density can be achieved, where $H_{z,tot}$ hardly affects the current distribution. As a result, a loss factor F_{H2} can be introduced

$$P_{loss} \propto \int_V H_{z,tot}^2 \mathrm{d}V \rightarrow F_{H2} = \int_V H_{z,tot}^2 \mathrm{d}V, \tag{3.9}$$

as the HF losses are directly proportional to the penetrating magnetic field, as long as the current distribution in the winding does not change significantly [37]. This simple H^2-loss factor can be used to accurately predict the optimal air gap position, without carrying out a time-consuming FEM optimization. In addition, for very simple geometries, the optimum air gap position can even be found analytically. For the arrangement at hand, the H^2-loss factor and the optimal air gap position $d_{w,opt}$ can be calculated based on (3.6)-(3.8) according to

$$F_{H2} = \int_V H_{z,tot}^2 \mathrm{d}V \xrightarrow{\text{minimize}} \frac{\partial}{\partial d_w} F_{H2} \stackrel{!}{=} 0 \tag{3.10}$$

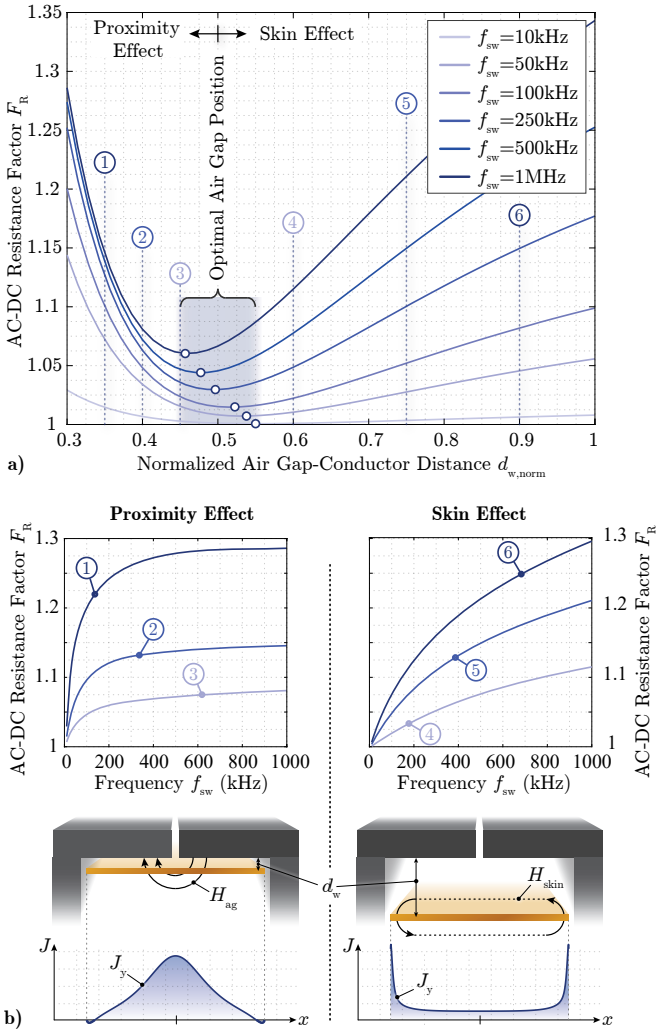


Fig. 3.5: a) AC to DC resistance factor F_R of a straight conductor for different values $d_{w,norm} = \frac{d_w}{b_w}$ and different frequencies f_{sw}. The optimal air gap placement for all frequencies lies around $d_{w,norm} = 0.5$, where below this value the proximity effect increases F_R and above the optimum the skin effect becomes dominant. Both effects are illustrated in **b)** for three different $d_{w,norm}$ values ①, ②, ③ and ④, ⑤, ⑥ , respectively.

and

$$\begin{aligned}\frac{\partial}{\partial d_\mathrm{w}} F_\mathrm{H2} &= \frac{\partial}{\partial d_\mathrm{w}} \int_\mathrm{V} H_\mathrm{z,tot}^2 \mathrm{d}V \\ &= \int_\mathrm{V} 2H_\mathrm{z,tot} \frac{\partial}{\partial d_\mathrm{w}} H_\mathrm{z,tot} \mathrm{d}V \\ &\rightarrow d_\mathrm{w,opt} = \frac{b_\mathrm{w}}{2}.\end{aligned} \tag{3.11}$$

Hence, the analytically derived optimal air gap position $d_\mathrm{w,opt}$ coincides with the optimal position found based on FEM simulations (cf. Fig. 3.5a).
Unfortunately, (3.11) yields a comparably poor filling factor of the available winding window, as a large distance $d_\mathrm{w,opt}$ between the air gap and the conductor is required, if a large winding width b_w is used. Consequently, a more power-dense design is in demand, which can be achieved by utilizing multiple air gaps instead of a single one.

3.2.1 Impact of Multiple Air Gaps on the Field Compensation

Similar to the optimal distance for a single air gap arrangement (cf. Fig. 3.5b), the optimal distance for a multi air gap arrangement can be calculated (cf. Fig. 3.6). Hence, based on the H^2-loss factor of the multi air gap arrangement, the following simplified optimal distances can be found:

$$d_\mathrm{w,opt}(N_\mathrm{ag}) = \frac{b_\mathrm{w}}{2 \cdot N_\mathrm{ag}}, \tag{3.12}$$

$$d_\mathrm{ag,opt}(N_\mathrm{ag}) = \frac{b_\mathrm{w}}{N_\mathrm{ag}}, \tag{3.13}$$

where b_w and $d_\mathrm{ag,opt}$ denote the width of the conductor and the optimal distance between multiple air gaps, respectively. Hence, with more air gaps, the core can be placed closer to the winding, leading to a more power-dense inductor design. Thus, for a true distributed air gap with a low permeability material instead of air gaps, $d_\mathrm{w,opt}(\infty) = 0$ results, whereby the ferrite core can be glued directly to the PCB, resulting in an extremely power-dense arrangement. However, today's low permeability materials are often lossy and show irreversible damages after a core saturation, whereby their application in industrial products is problematic. Furthermore, the complexity of the core manufacturing increases significantly with the number of air gaps, which is

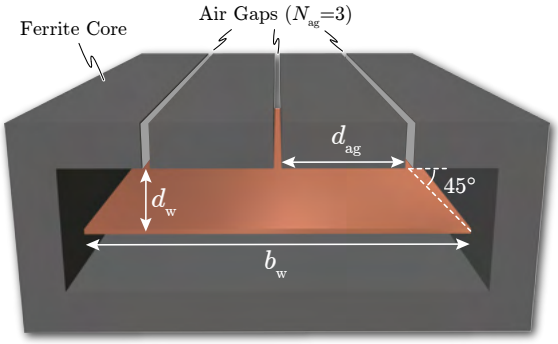


Fig. 3.6: Optimal arrangement of a PCB-winding inductor with three air gaps. The cutting surfaces of the core are colored in light gray in order to ensure good visibility of the air gap placement.

why N_{ag} should be chosen to be as small as possible, while still complying with the required power density of the component.
Fortunately, in most practical applications it is sufficient to use a single air gap, as will be shown in the following.

3.2.2 Practical Implementation of the CFFC

A possible practical implementation of a PCB-winding inductor, using the proposed field compensation concept on straight winding sections, is shown in Fig. 3.7a. However, this design has significant drawbacks, as the end-winding sections are not covered by the air gap. Hence, the skin and proximity fields are not compensated anymore and the conduction losses in these sections significantly increase. In addition, the ratio between the winding length l_{ws} and the core area A_C is very large compared to the circular arrangement shown in Fig. 3.7b, whereby the conduction losses are unnecessarily high, as will be explained in the following.
Assuming the same total core cross-section A_C in both designs, the ratio between the winding lengths can be calculated according to

$$L_w(k) = \frac{l_{ws}}{l_{wc}} = \frac{1+k}{\sqrt{\pi k}}, \tag{3.14}$$

where k denotes the ratio between the length and the width of the core cross section A_C of Fig. 3.7a. Hence, the minimum ratio between the winding

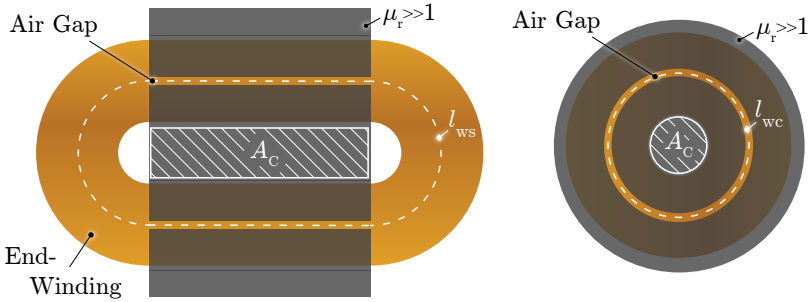


Fig. 3.7: a) Practical implementation of a PCB-winding inductor with a partially straight winding, resulting in large end-winding losses and **b)** improved pot core arrangement with a circular winding with a minimum winding length.

lengths can be found to be

$$\frac{\partial}{\partial k} L_w(k) \stackrel{!}{=} 0 \xrightarrow{k=1} L_w(1) = \frac{2}{\sqrt{\pi}} > 1. \tag{3.15}$$

Thus, even for the optimal value $k = 1$ (square cross-section), the winding length of the rectangular core l_{ws} is larger than l_{wc}. Consequently, the circular arrangement of Fig. 3.7b should be used in practical applications, as in addition to the reduced winding length, the circularly shaped winding and air gap allow to compensate the skin and proximity fields along the whole winding, whereby the aforementioned end-winding losses can be avoided. However, the circular shape of the conductor might influence the optimal air gap position, which will be investigated in the following section.

3.3 Field Compensation in Circular Conductors

Unlike in a straight conductor, the DC current density J_{DC} in circular conductors is not homogeneous anymore and can be calculated according to

$$J_{DC}(r) = \frac{i_L}{r \cdot h_{cu} \cdot \ln\left(\frac{r_{in}}{r_{out}}\right)}, \tag{3.16}$$

as shown in Fig. 3.8a. Hence, as already mentioned in the previous section,

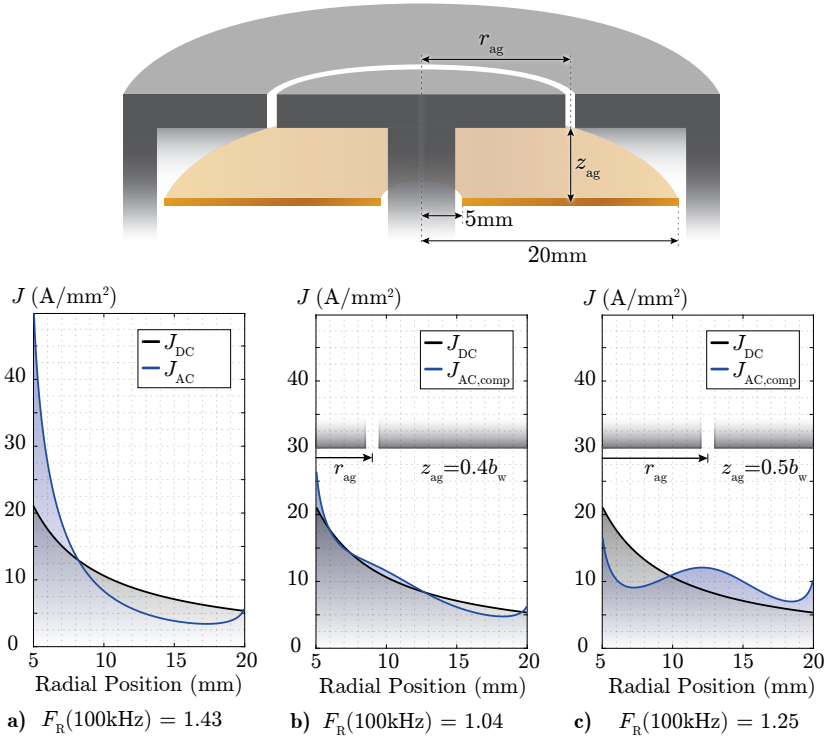


Fig. 3.8: Qualitative sketch of a circular PCB-winding inductor arrangement (in reality, the width of the outer shell would be much smaller) and three different current distributions: **a)** DC current density J_{DC} in a circular conductor and its HF equivalent J_{AC} without an air gap in its near vicinity. **b)** DC current density and its HF counterpart $J_{AC,comp}$ with the air gap ideally positioned. **c)** DC current density and its HF counterpart $J_{AC,comp}$ with the air gap positioned in the optimal spot for a straight conductor (cf. (3.11)).

the HF current density J_{AC} should match J_{DC} as closely as possible in order to achieve a low F_R value. In the same figure, the current distribution J_{AC} due to the skin effect only, thus without an air gap in the near vicinity of the conductor, is illustrated. Thus, the magnetic skin field $H_{z,skin}$ pushes the current towards the center of the inductor, whereby an increased F_R value results, even for comparably low frequencies (F_R = 1.43 at 100 kHz). Therefore, the fringing field $H_{z,ag}$ of the air gap is again required to compensate $H_{z,skin}$ and to pull the current away from the center of the winding to match J_{DC} as accurately as possible. The compensating effect of $H_{z,ag}$ is shown for two different air gap locations in Fig. 3.8b and Fig. 3.8c, respectively.
In Fig. 3.8b, the air gap is located in the optimal position for this circular geometry, whereby a very low value for $F_R (= 1.04)$ results and $J_{AC,comp}$ hardly deviates from J_{DC}.
In Fig. 3.8c, the air gap is placed at the position which would be optimal for a straight conductor, hence, in the middle of the track with a distance z_{ag} of $\frac{b_w}{2}$ (3.11). However, this location is far from optimal, as an almost homogeneous current distribution is achieved, which does not correspond to $J_{DC}(r)$. Consequently, the optimal air gap positions in straight and circular conductors are different and need to be calculated individually.

Once again, there are two different options to find the optimal air gap position in a circular conductor.
Either the time-consuming FEM simulation, whose results are shown in Fig. 3.9 for varying z_{ag} and r_{ag} values, where z_{ag} denotes the distance between the conductor and the air gap and r_{ag} the radial position of the air gap, or by using the previously introduced H^2-loss factor F_{H2}, which is calculated based on the magnetic skin field $H_{z,skin}$ of the DC current distribution $J_{DC}(r)$ and the fringing field $H_{z,ag}$ around the air gap according to

$$J_{line}(r) = J_{DC}(r) \cdot h_{cu} = \frac{i_L}{r \cdot \ln\left(\frac{r_{in}}{r_{out}}\right)}, \tag{3.17}$$

$$H_{z,skin}(r) = \int_{r_{in}}^{r_{out}} \frac{J_{line}}{2\pi(r+\alpha)} \left(\frac{\alpha^2 - r^2}{(\alpha - r)^2} E(k^2) + K(k^2) \right) \mathrm{d}\alpha,$$
$$k^2 = \frac{4\alpha r}{(\alpha + r)^2} \tag{3.18}$$

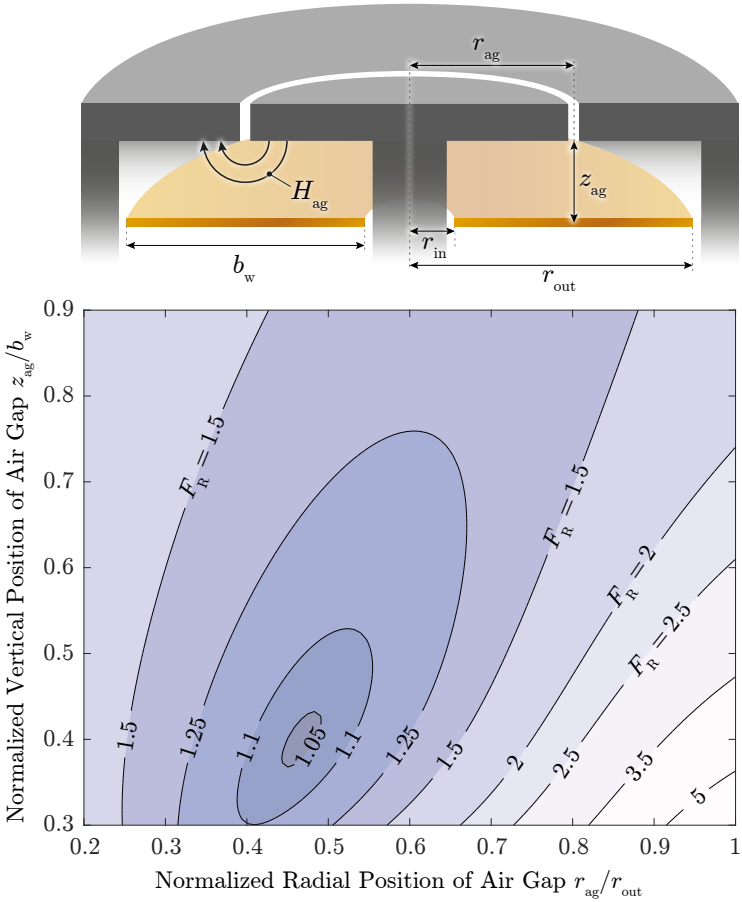


Fig. 3.9: AC to DC resistance factor F_R for different normalized air gap positions ($\frac{r_{ag}}{r_{out}}$, $\frac{z_{ag}}{b_w}$), a frequency of 500 kHz and a ratio of radii $\frac{r_{in}}{r_{out}}$ of 0.2.

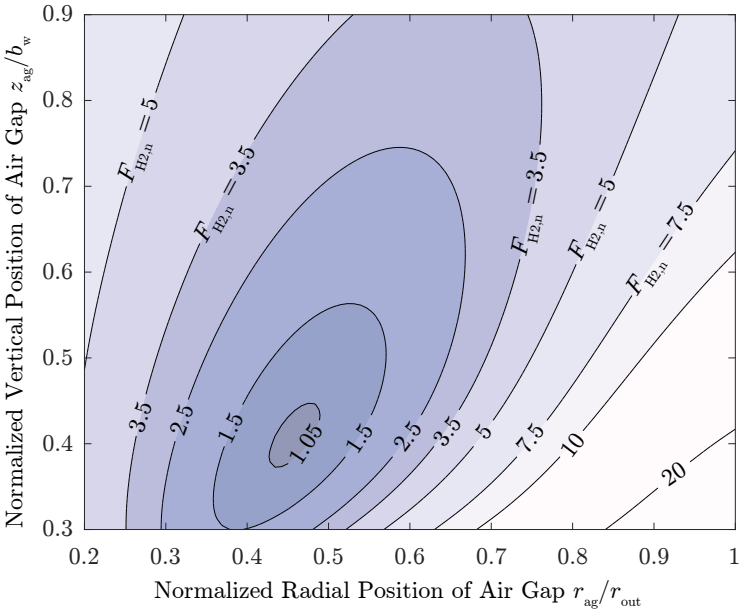


Fig. 3.10: Calculated normalized H^2-loss factor for the same arrangement as shown in Fig. 3.9, in order to estimate the optimal air gap position (r_{ag}, z_{ag}).

and

$$H_{\mathrm{z,ag}}(r) = \frac{i_{\mathrm{L}}}{\pi\sqrt{(r+r_{\mathrm{ag}})^2+z_{\mathrm{ag}}^2}} \cdot \left(\frac{r_{\mathrm{ag}}^2 - r^2 - z_{\mathrm{ag}}^2}{(r_{\mathrm{ag}}-r)^2+z_{\mathrm{ag}}^2} E(k^2) + K(k^2) \right),$$
$$k^2 = \frac{4 r_{\mathrm{ag}} r}{(r_{\mathrm{ag}}+r)^2+z_{\mathrm{ag}}^2}, \tag{3.19}$$

where $E(k^2)$ and $K(k^2)$ denote the complete elliptic integrals of the first and second kind. The results are shown in Fig. 3.10, whereby a very close match between the results of the actual F_{R} values of Fig. 3.9 and the H^2-loss factors F_{H2} can be observed. Especially for locations $(r_{\mathrm{ag}}, z_{\mathrm{ag}})$ with the lowest F_{R} values, the curves are almost identical, which allows for accurately predicting the optimal position $(r_{\mathrm{ag,opt}}, z_{\mathrm{ag,opt}})$ within a fraction of the time it would take to simulate the geometry in a FEM software.
The benefit of the significantly reduced calculation time of the H^2-loss factors cannot only be used for the previously shown straight and circular conductor arrangements, as the principle of calculating the optimal air gap position using the H^2-loss factor is very general and can be applied to all kinds of winding geometries, once the DC current distribution is known.

However, in order to simplify the usage of this concept in practice, a general design guideline would be advantageous, which reduces the computational effort for the inductor designer.
Fortunately, in the circular arrangement of Fig. 3.9, the optimal air gap positions change with the ratio of radii only and do not depend on their absolute dimensions, which is why the desired general design guideline for circular conductors can be calculated for all ratios of radii $r_{\mathrm{in}}/r_{\mathrm{out}}$. The resulting optimal air gap positions $(r_{\mathrm{ag,opt}}, z_{\mathrm{ag,opt}})$ are depicted in Fig. 3.11.
In order to illustrate the difference between the actual optimal air gap position for a circular conductor and the simplified calculation based on a straight conductor (3.11), the results of both calculation methods are shown. For $r_{\mathrm{in}}/r_{\mathrm{out}} > 0.5$, the simplified calculation based on $z_{\mathrm{ag,est}} = \frac{b_{\mathrm{w}}}{2}$ and $r_{\mathrm{ag,est}} = \frac{r_{\mathrm{in}}+r_{\mathrm{out}}}{2}$ yields very good results, closely following the optimum $z_{\mathrm{ag,opt}}$ and $r_{\mathrm{ag,opt}}$ obtained from (3.18) and (3.19), as the DC current density $J_{\mathrm{DC}}(r)$ in the circular conductor is almost homogeneous. However, for lower ratios of radii, the optimal air gap position should be chosen according to the solid lines depicted in Fig. 3.11, due to the inhomogeneity of $J_{\mathrm{DC}}(r)$.
So far, only a single layer conductor has been considered. However, in practice, inductor windings usually comprise multiple turns and multiple layers

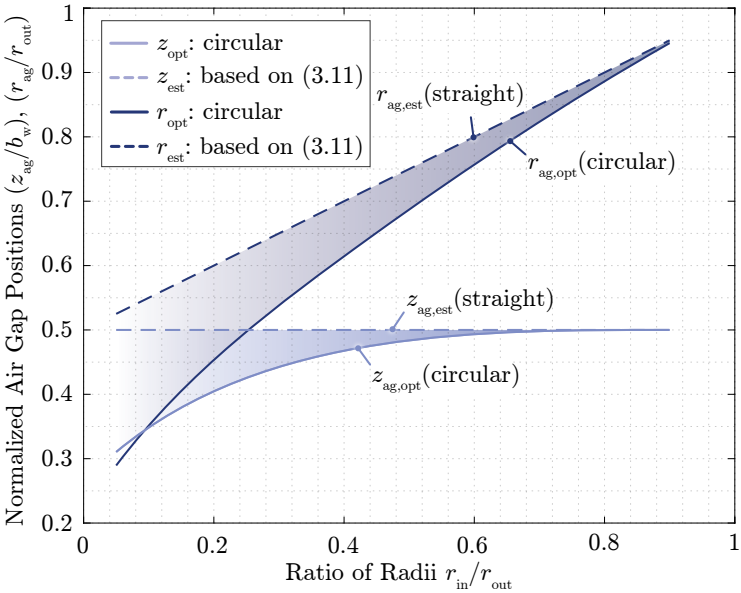


Fig. 3.11: Comparison between the estimated optimal air gap position based on the calculations for a straight conductor ($r_{ag,est}$, $z_{ag,est}$) and the actual optimal position based on the calculations for a circular conductor ($r_{ag,opt}$, $z_{ag,opt}$), for different ratios of radii $\frac{r_{in}}{r_{out}}$.

in order to achieve a certain required inductance. Therefore, it is crucial to investigate the applicability of the proposed concept to multilayer windings, to prove its suitability for practical applications. This will be done in the following section.

3.4 Field Compensation in Multi-Layer Arrangements

In a practical application, the number of turns of an inductor is usually larger than one, whereby either multiple tracks on one PCB layer, multiple PCB layers with one track each, or a combination of both needs to be used. Ideally, only a single PCB layer with a spiral winding should be employed, as this layer can be placed in the ideal distance $d_{\mathrm{w,opt}}$ to the air gap, whereby AC to DC resistance ratios of close to one can again be achieved. Additionally, there is no need for layer transitions within the winding and vias can therefore be completely omitted. However, in high power applications, the limited height of a PCB copper layer (35 µm...105 µm) demands for large track widths, in order to carry the currents through the winding with a reasonable current density ($\leq$ 100 A/mm^2). For a single layer winding this inherently would result in a large total winding width $b_{\mathrm{w,SL}}$ and therefore huge overall inductor dimensions.

The only possibility to reduce the winding width, while at the same time keeping a certain maximum current density, is therefore the utilization of multiple helical PCB layers, where the individual turns are placed on top of each other. Hence, compared to a single-layer spiral winding, in a multi-layer helical winding there is only a single turn per layer, where the individual turns are interconnected through vias in vertical direction. Consequently, each layer of the PCB can be used for the winding, whereby the ratio between the width of a multi-layer winding $b_{\mathrm{w,ML}}$ and the width of the equivalent single-layer winding $b_{\mathrm{w,SL}}$ is inversely proportional to the number of PCB layers N_{layer} used, according to $b_{\mathrm{w,ML}}/b_{\mathrm{w,SL}} = 1/N_{\mathrm{layer}}$.

However, this inherently results in non-homogeneous magnetic field distributions within the winding, as each layer is located at a different distance d_{w} from the air gap(s). Consequently, the proximity effect between the layers starts to play an important role, as it amplifies the inhomogeneities of the current densities within the PCB tracks. This is illustrated in Fig. 3.12a based on a four-layer PCB example, where the first layer is located in a distance $d_{\mathrm{w,opt}}$ from the air gap. In the first graph, the simulated current densities of

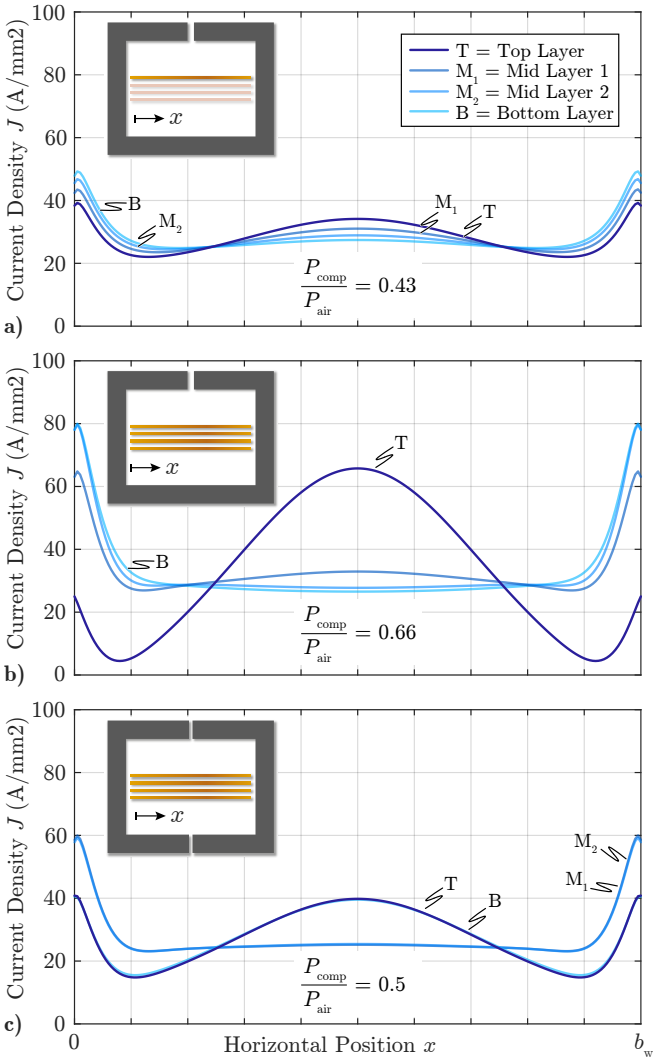


Fig. 3.12: Simulated current densities in a four-layer PCB for **a)** a single air gap and all layers simulated independently from each other, one at a time (neglecting the proximity effect), **b)** a single air gap and all layers simulated simultaneously (real situation) and **c)** a dual air gap arrangement with simultaneously simulated PCB layers. Additionally, the occurring conduction losses are always compared to the one occurring in the PCB without a magnetic core (air coil).

the four PCB tracks are shown, without taking into account the proximity effect among the tracks, i.e. the current distribution of each track is simulated independent from the others. Hence, they were simulated one after the other, whereby only the skin field and fringing field were considered. Thus, almost homogeneous current densities are achieved, as predicted by the analysis of the previous section. The effectiveness of the field compensation can also be quantified by the ratio between the total conduction losses in the four PCB tracks in the field-compensated arrangement (P_{comp}), thus, the arrangement shown in the figure, and the conduction losses occurring in the same PCB tracks operated as an air coil (P_{air}) without an air gap in the near vicinity of the conductors. Hence, in the arrangement without considering the proximity effect, a $P_{\mathrm{comp}}/P_{\mathrm{air}}$ ratio of 0.43 can be achieved, which is equivalent to a reduction of the conduction losses by 57 %.
However, if the proximity effect is considered, thus, the complete system is simulated simultaneously, the current densities of Fig. 3.12b are found. There is still a certain compensating effect visible, but due to the proximity effect, most of the fringing field of the air gap is "shielded" by the top layer, whereby its compensating effect on the mid layers is reduced. Still, the conduction losses of this arrangement are 34 % lower than the one of the same PCB-winding without a core (operated as air coil), proofing the benefits of the proposed compensating fringing field concept (CFFC). Nevertheless, the effectiveness of the field compensation can further be enhanced by using two air gaps, one above and one below the PCB, as shown in Fig. 3.12c. Splitting the air gap reduces the magnetically effective number of PCB layers by half, due to the symmetry of the arrangement around the horizontal axis. Thus, the proximity effect can significantly be reduced, which means in terms of conduction losses, a reduction by almost 50 % compared to the air coil. It should be noted, that the optimal distance $d_{\mathrm{w,opt}}$ between the air gap and the top/bottom layer of the PCB-winding does not change if the air gap is split into two air gaps above and below the PCB-winding. This follows from the symmetry of the arrangement, as in a first approximation, the upper air gap can be considered to be responsible for the compensation of the upper half of the PCB layers and the lower air gap for the lower half of the PCB layers, respectively. Consequently, for PCB-windings with more than one layer, the dual air gap arrangement should be used, where the optimal distance between the PCB and the air gaps can still be calculated according to (3.11). Hence, the top and the bottom layers should always be placed in the optimal distance $d_{\mathrm{w,opt}}$ to the respective air gap, as can be proven by means of FEM simulations.

So far, it has been shown, that the CFFC can also be used in multi-layer PCB-windings, where it effectively mitigates the parasitic HF effects in the conductors. However, when it comes to the practical implementation of a multi-layer helical winding, there are a couple of things which need to be considered, as will be discussed in the following.

3.5 Practical Implementation of a Multi-Layer Helical PCB-Winding

As already mentioned in the previous section, in practical applications, the number of turns of an inductor is usually larger than one, whereby ideally a helical multi-layer winding is employed, where each turn of the winding is placed on a different PCB layer, and all layers are interconnected by means of vias (cf. Fig. 3.13). Even though the transition between the layers should ideally be done with blind and buried vias within the winding, this is usually not possible due to cost reasons. Thus, through-hole vias need to be used, which can either be placed at the inner or outer edge of the winding. However, the inner location should be preferred, as it is more efficient due to the shorter total winding length.
The layer transition with through-hole vias, however, requires a certain overlap between two consecutive turns, such that multiple vias can be used for the layer transition and the maximum current per via is not exceeded. Consequently, the effective winding length per layer $l_{\mathrm{w,eff}}$ is reduced (cf. Fig. 3.13), whereby the number of turns per layer N_{pL} is always smaller than one. Thus, if a vertically aligned termination is required, which means that the beginning of the winding needs to be exactly at the same position as its respective end, the total number of turns N_{L} will always be lower than the number of PCB layers N_{layer}, as for $N_{\mathrm{L}} = N_{\mathrm{layer}}$, an N_{pL} value of exactly one would be required. This, however, would only be possible with vias at the inner and outer radius of the winding, yielding a significantly reduced available copper cross-section of the winding for a certain given b_{w}. The optimal number of turns of such a PCB-winding inductor, which results in the best copper utilization, is therefore given as

$$N_{\mathrm{L}} = N_{\mathrm{layer}} - 1. \tag{3.20}$$

For large required inductance values, it is of course also possible to use multiple turns per layer, however, this inherently demands for vias at the inner and outer radius of the winding, as the positions of the layer transitions are alter-

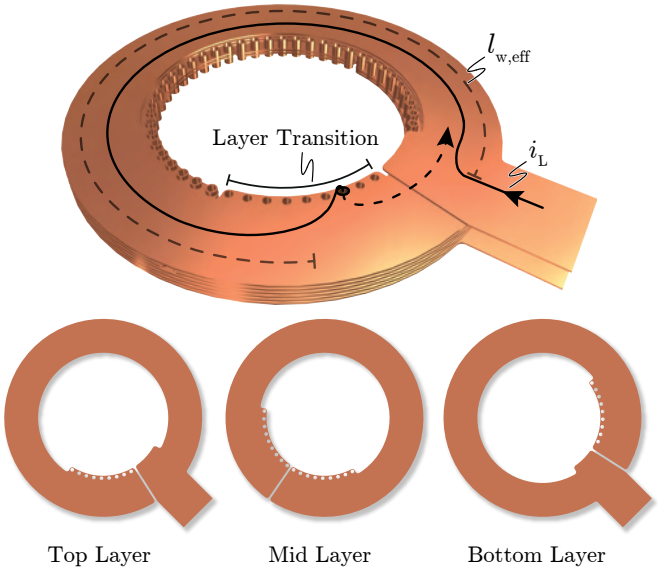


Fig. 3.13: Design of a multi-layer PCB-winding with single turns on each layer and through-hole vias for the transitions between the layers and/or interconnections of the turns. Additionally, the shapes of the different copper layers are shown, where it needs to be mentioned, that all the inner layers (Mid Layer) look the same just rotated by a certain rotation angle, which is why only a simple example is depicted.

nating between inner radius and outer radius of the winding. Thus, the total width of the PCB-winding is further increased, as at least 1 mm is required for the vias and their necessary clearance to the adjacent turns. Especially for small winding widths b_w, this has a large influence on the overall power density of the inductor, which is why the multi-layer helical winding with single turns per layer should be preferred whenever possible.

Finally, it is important to pay attention to the termination of the PCB-winding, as otherwise, significant conduction losses might occur. As known from PCB-winding transformers, a vertically aligned arrangement, with two conductors on top of each other, is the most efficient way of carrying anti-parallel currents in PCBs. Consequently, the same arrangement should be used in the winding termination too, as the two currents in an inductor termination are heading into opposite directions as well (cf. Fig. 3.14). Hence, assuming a track width of e.g. 5 mm and a frequency of 500 kHz, a vertically aligned termination Ⓥ saves 65 % of conduction losses compared to a lateral parallel termination Ⓗ. This reduction of losses originates from the fact, that two currents flowing into opposite directions physically attract each other, whereby in arrangement Ⓗ, most of the current is flowing at the inner edges of the terminals only and the respective effective copper cross-section is significantly reduced. In contrast, in arrangement Ⓥ, the mutual attracting force between the two terminal currents yields a slight current displacement in vertical direction only, whereby still an almost homogeneous current density in horizontal direction can be found, and the effective copper cross-section is not significantly reduced. For this reason, a vertically aligned termination should always be used if in any way possible (cf. Fig. 3.13).

In order to experimentally verify the effectiveness and the suitability of the CFFC in practical applications, an exemplary PCB-winding inductor is designed and measured in the following section, which will later also be used as series-resonant inductor in a 3 kW DC/DC step-down converter to test the ”in-system” performance of the concept.

3.6 Experimental Verification of the CFFC

The proposed compensating fringing field concept (CFFC) is verified by means of an exemplary inductor designed according to the specifications of Tab. 3.1, which were derived for a series-resonant inductor of a 3 kW 500 V/15 V isolated DC/DC converter. This converter could finally be used in automotive

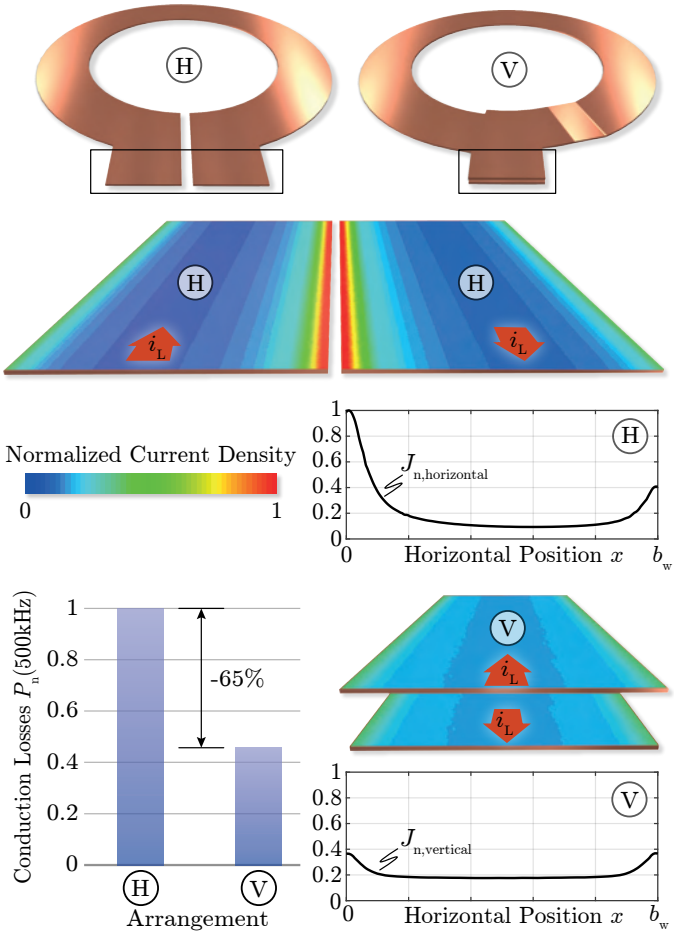


Fig. 3.14: FEM-simulated current densities in a horizontal (H) and a vertical (V) parallel termination for a frequency of 500 kHz and a track width of 5 mm. The normalized conduction losses P_n of the two possible terminations are shown as well.

Inductance	L	6.8 µH
Max. RMS Current	$I_{\mathrm{L,RMS}}$	17.9 $\mathrm{A_{RMS}}$
Peak Current	$I_{\mathrm{L,pk}}$	25.2 $\mathrm{A_{pk}}$
Switching Frequency	f_{sw}	300 kHz...720 kHz

Tab. 3.1: Specifications of the PCB-winding inductor hardware prototype, which employs the proposed CFFC.

applications as e.g. the step-down converter of Fig. 1.2a and is discussed in detail in Chapter 4.

For cost reasons, an 8-layer PCB is used for the aforementioned DC/DC converter, which is why the inductor is ideally designed with $N_{\mathrm{L}} = N_{\mathrm{layer}} - 1 = 7$ turns, such that through-hole vias for the layer transitions and a coplanar termination can be used (cf. (3.20)). However, the optimal number of turns depends on the required specifications and does not always match $N_{\mathrm{layer}} - 1$, which would result in the best copper-utilization. For this reason, N_{L} should be chosen according to an η-ρ-Pareto-optimization, which in this case indeed yields $N_{\mathrm{L}} = 7$ as the best choice for the given application. The dimensions such as winding width b_{w}, air gap length l_{ag} and core cross-section A_{C} result from the same η-ρ-optimization considering both, the winding losses as well as the core losses of the inductor. The final values are then chosen based on a trade-off between efficiency and power density of the inductor. This optimization is based on well-known equations for calculating the different loss components [38] and is briefly explained in a later section, which is why only the dimensions of the finally selected inductor design are given here (cf. Fig. 3.15a).

Due to the circular winding arrangement and, therefore, the required circular air gaps above and below the PCB-winding, conventional ferrite cores cannot be used in this application, whereby customized core shapes are in demand. Hence, the core is designed in a similar way as conventional pot cores, but with the difference, that there are air gaps cut into the upper and the lower halves of the pot core (cf. Fig. 3.15b). This is done using a CNC-milling machine with diamond drill bits, which allows to accurately manufacture arbitrary core shapes in a comparably short time. Finally, the different parts of the core of this hardware demonstrator are hold together by means of a 3D-printed core holder, such that a homogeneous air gap width is guaranteed and a certain mechanical stability is provided.

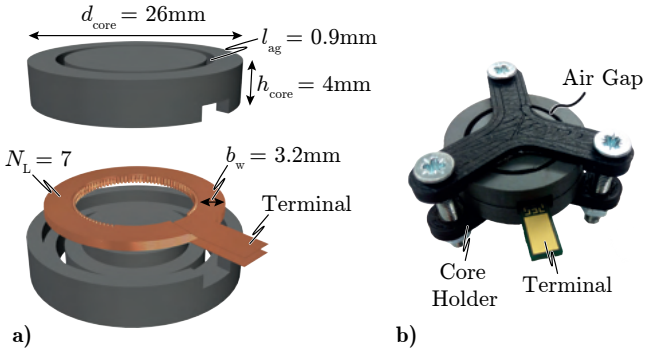


Fig. 3.15: a) 3D model of the practical implementation of a 6.8 µH multi-layer PCB-winding inductor using the proposed fringing field compensation concept, by means of a ferrite core with two air gaps and **b)** picture of the assembled inductor with a 3D-printed core holder.

In order to verify the findings of the previous sections, the impedance of both, the PCB-winding without a core (air coil), as well as the PCB-winding with the proposed core arrangement were measured. The measurement results of the total winding resistance are shown in Fig. 3.16, whereby a good agreement between the FEM simulations and the measurements can be found. Two observations have to be noted: On the one hand, in the frequency range of interest (300 kHz...720 kHz), the effectiveness of the CFFC is clearly visible, as the winding resistance of the assembled PCB inductor is reduced by almost 50 % compared to the air coil. The reduction of the winding resistance originates from the fact, that in contrast to the air coil, in the assembled inductor the fringing field around the air gap effectively counteracts the skin and proximity fields within the PCB-winding. On the other hand, the influence of the core material on the overall inductor losses, especially for high frequencies, becomes noticable, i.e. already constitutes half of the total inductor loss at around 1 MHz for N95. Hence, the eddy-current losses (the hysteresis losses are negligible when measuring the impedance with an impedance analyzer) in the core made of N95 ferrite material are significantly higher then the ones occurring in exactly the same core but made of N49 ferrite material. Consequently, the effect of an improperly chosen core material is directly visible in the AC-resistance measurement of an inductor, whereby a careful selection of an appropriate core material is key for high

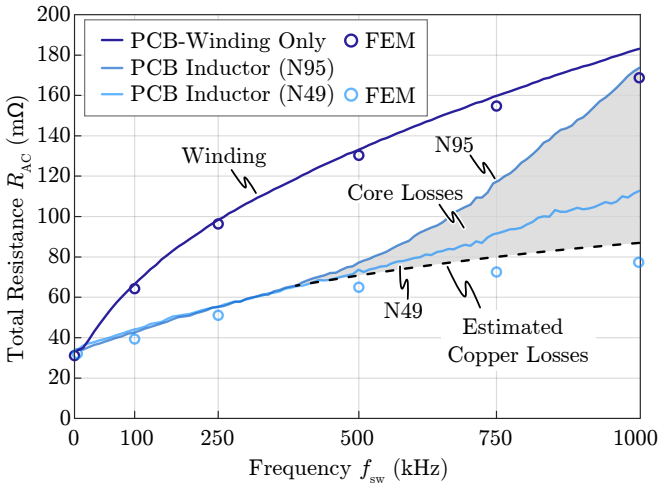


Fig. 3.16: Total winding resistance of the PCB-winding only (air coil), the fully assembled inductor with a core made of N95, and the same inductor but with a core made of N49 ferrite material. All three measurements were taken using an impedance analyzer.

efficiency applications.

In order to consider the hysteresis losses in the ferrite core as well, the same components have been excited in a calorimeter with a sinusoidal current of 5 A_{pk} at a frequency of 500 kHz. In order to compare the proposed design concept to state-of-the-art solutions, an additional core arrangement has been measured, with exactly the same dimensions as shown in Fig. 3.15a, but instead of two perpendicular air gaps, i.e. one air gap on top and another air gap at the bottom of the winding, the air gaps are located in the same physical layer as the PCB-winding, as usually the case in conventional pot cores (cf. Fig. 3.17 Ⓒ). The results are shown in Fig. 3.17, where the ratios between winding and core losses are estimated based on the impedance measurements of Fig. 3.16, as in a calorimetric setup only the total losses of a device can be measured. The benefits of the proposed CFFC are obvious: even though the inductance of the field compensated inductor Ⓑ is 10 times larger then the one of the air coil Ⓐ, the overall losses can be reduced by 25 %. Of course this ratio changes with current, as the winding losses scale quadratically with the current, while the core losses show an i_L^{β} dependency, where β denotes the

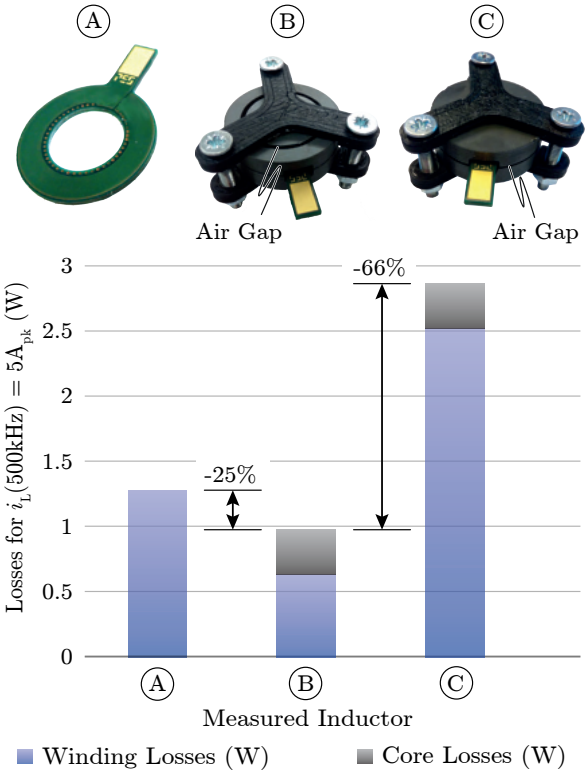


Fig. 3.17: Calorimetric loss measurements of Ⓐ the PCB-winding only, with an inductance of 700 nH, Ⓑ the proposed PCB-winding inductor design (N49) with an inductance of 6.7 µH and Ⓒ the conventional design approach with the air gap in the same physical layer as the PCB (6.8 µH).

according Steinmetz parameter [39] of the core material. Nevertheless, the ratio between the conventional inductor Ⓒ and the field compensated inductor Ⓑ does not change significantly with the current amplitude, whereby for the same inductance L, 66 % of the total losses can be saved by the proposed field compensation concept.
However, there is one major drawback of this concept compared to conventional inductor core arrangements: The air gap is directly given by the manufactured core and can hardly be changed afterwards (cf. Fig. 3.15b). Thus, the only possible adjustment of the inductance in the given arrangement is the increase of the total air gap by separating the two core halves, whereby an additional small air gap in the same physical layer as the winding results. However, as previously mentioned, the fringing field around this air gap would increase the conduction losses of the winding, whereby it should be avoided at all costs. Fortunately, the air gaps in inductors employing the CFFC are usually large, whereby possible inaccuracies during the manufacturing of the cores do not affect the inductance significantly and the resulting inductance values are quite consistent.

Unfortunately, in the proposed PCB-winding inductor of Fig. 3.15b, the allowable RMS current is strongly limited due to the poor thermal conductivity of the PCB, in combination with the terminal of the winding as the only possible thermal interface between the winding and the heat sink. Consequently, a thermally enhanced PCB-winding inductor design is required, which will be introduced in the next section.

3.7 Thermally Enhanced PCB-Winding Inductor Design

Even though the CFFC can significantly reduce the occurring conduction losses in a PCB-winding inductor, these losses can hardly be dissipated in the initially proposed PCB-winding design. Hence, in order to improve the thermal interface between the winding and the heat sink, the thermal model of the existing PCB-winding needs to be derived first. For this reason, an equivalent thermal conductivity λ_{eff} of a PCB in horizontal direction is defined [40] according to

$$\lambda_{\mathrm{eff}} = r_{\mathrm{PCB}}\lambda_{\mathrm{Cu}} + (1 - r_{\mathrm{PCB}})\lambda_{\mathrm{FR4}}, \tag{3.21}$$

with

$$r_{\mathrm{PCB}} = \frac{A_{\mathrm{Cu}}}{A_{\mathrm{FR4}} + A_{\mathrm{Cu}}} = \frac{N_{\mathrm{layer}} \cdot h_{\mathrm{Cu}}}{h_{\mathrm{PCB}}}, \tag{3.22}$$

where λ_{Cu}, λ_{FR4}, h_{Cu} and h_{PCB} denote the thermal conductivity of copper, the thermal conductivity of FR4, the height of a copper layer and the total height of the PCB, respectively (cf. Fig. 3.18a). Using this effective thermal conductivity, the thermal resistance R_{th} of a piece of PCB can be calculated according to

$$R_{\mathrm{th}} = \frac{l_{\mathrm{w}}}{\lambda_{\mathrm{eff}} \cdot b_{\mathrm{w}} \cdot h_{\mathrm{PCB}}}, \tag{3.23}$$

where l_{w} denotes the length and b_{w} the width of the considered PCB part, as shown in Fig. 3.18b for an exemplary piece of PCB with a variable length l_{w}.

The same calculation method can now be used to estimate the temperature distribution in the PCB-winding, based on the thermal model shown in Fig. 3.19a. In order to simplify the calculations, a homogeneous loss density q_{W} within the winding is assumed, which is calculated according to

$$q_{\mathrm{W}} = \frac{P_{\mathrm{W}}}{2\pi}, \tag{3.24}$$

where P_{W} denotes the total occurring conduction losses in the winding. It should be noted, that for simplicity reasons q_{W} and all further parameters are normalized with respect to 2π instead of $2\pi r_{\mathrm{W}}$, as only the angular dependency of the temperature is of interest and a constant temperature in radial direction is assumed. Besides q_{W}, a constant thermal "per-length" resistance $r_{\mathrm{th,W}}$ of the winding is defined, which is calculated according to

$$r_{\mathrm{th,W}} = \frac{1}{2\pi} \left(\frac{2 r_{\mathrm{W}} \pi}{\lambda_{\mathrm{eff}} \cdot b_{\mathrm{W}} \cdot h_{\mathrm{PCB}}} \right). \tag{3.25}$$

Furthermore, as indicated in Fig. 3.19a, an infinite number of heat sources and thermal resistances along the winding are assumed, which are finally connected to the ambient temperature T_{A} through a single additional thermal resistance $R_{\mathrm{th,T}}$, which represents three individual components: The thermal resistance of the terminal of the winding, the thermal resistance of the thermal interface material between the winding terminals and the heat sink, and finally, the thermal resistance from the heat sink to the ambient. The employed thermal interface material (TIM) between the winding terminals and the heat sink provides a tight thermal connection and at the same time

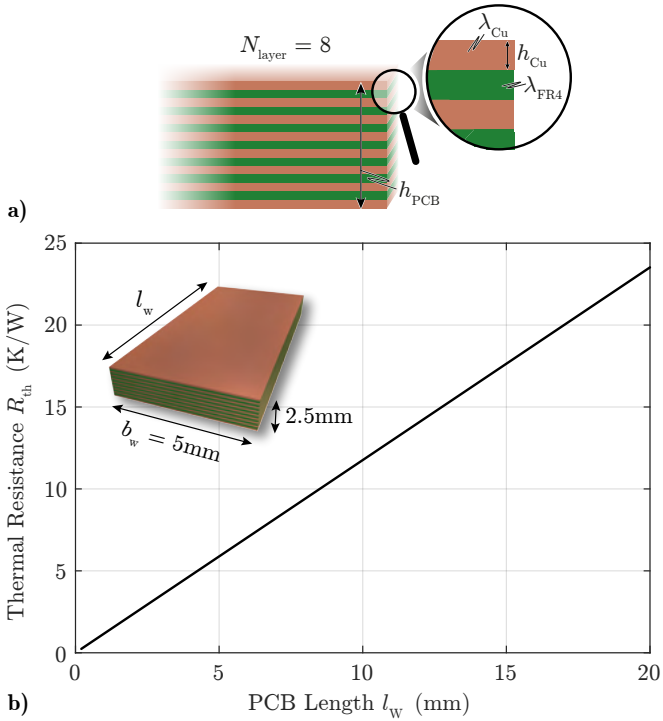


Fig. 3.18: a) Sketch of an eight-layer PCB with all the definitions used to introduce an effective thermal conductivity λ_{eff} of a PCB (cf. Eqs. (3.21-3.23)) and **b)** the lateral thermal resistance of a piece of an eight-layer 70 µm PCB with a width of 5 mm, a height of 2.5 mm and a variable length l_{w}.

ensures the required isolation between them, as otherwise the heat sink would short-circuit the winding.
As the total generated power loss has to flow through $R_{\mathrm{th,T}}$, this thermal resistance needs to be particularly small, as otherwise a significant temperature drop across $R_{\mathrm{th,T}}$ would be induced.
Based on the aforementioned quantities and the thermal model of Fig. 3.19a, the angle-dependent PCB temperature T_{W} can be calculated, according to

$$T_{\mathrm{W}}(\varphi) = T_{\mathrm{A}} + R_{\mathrm{th,T}} \cdot P_{\mathrm{W}} + \int_0^{\varphi} q_{\mathrm{W}} r_{\mathrm{th,W}}(\pi - \varphi)\mathrm{d}\varphi. \tag{3.26}$$

Hence, the following temperature profile can be found

$$T_{\mathrm{W}}(\varphi) = T_{\mathrm{A}} + R_{\mathrm{th,T}} \cdot P_{\mathrm{W}} + q_{\mathrm{W}} r_{\mathrm{th,W}} \cdot \varphi \left(\pi - \frac{\varphi}{2}\right). \tag{3.27}$$

As an example, Fig. 3.19b shows the temperature profile within the PCB-winding of Fig. 3.15b and Fig. 3.19a for 6 W of conduction losses and an ideal heat sink with a temperature of 25 °C connected to the winding terminal. As shown in the figure, the calculated temperatures are in good agreement with the FEM-simulated temperatures, even though the calculation is based on various simplifications.

The thermal bottlenecks of the initial PCB-winding design can now easily be identified with (3.27) and Fig. 3.19b. One the one hand, there is a large temperature drop across the winding terminals (55 °C), as the total losses have to flow through a narrow piece of PCB with a comparably large thermal resistance, according to

$$T_{\mathrm{W}}(\varphi = 0) = T_{\mathrm{A}} + R_{\mathrm{th,T}} \cdot P_{\mathrm{W}} \tag{3.28}$$

(cf. $l_{\mathrm{w}} = 8$ mm in Fig. 3.18b). On the other hand, the temperature gradient is increasing for smaller φ, as there is more and more heat flux accumulated along the winding, which needs to flow through $r_{\mathrm{th,W}}$ towards the terminals. Therefore, in order to thermally improve the design, more thermal interfaces should be used, whereby the total heat flux is distributed among multiple thermal terminals and at the same time the mean length of the thermal path for the heat flux from its origin to the heat sink is reduced. Such a thermally enhanced design is shown in Fig. 3.20a, where three additional thermal interfaces are used. These additional thermal interfaces do not carry any current, as they are fully isolated from the aluminum heat sink by means of a thermal interface material, but they provide a thermally conductive path

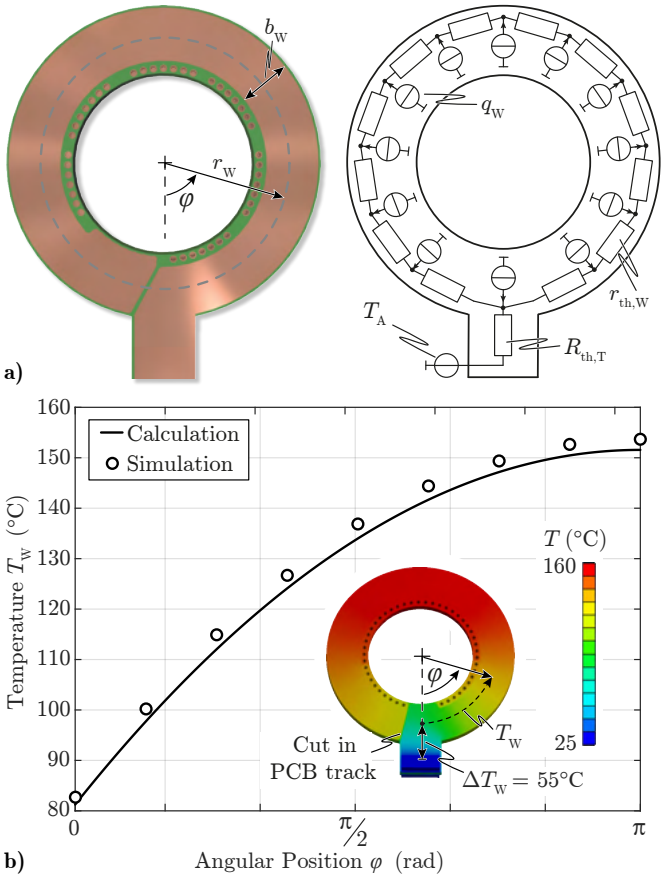


Fig. 3.19: a) Thermal model of the initially proposed multi-layer PCB-winding design and **b)** the respective temperature profile for the PCB-winding shown in Fig. 3.15b and Fig. 3.19a for 6 W of total losses. Additionally, the solutions of the corresponding FEM simulation are shown.

from the actual PCB-winding to the aluminum heat sink. Consequently, only one quarter of the total heat flux flows through each terminal and the mean length of the thermal path is reduced by a factor of four as well.

Similar to (3.27), the following angle-dependent PCB temperature T_W can be derived for the thermally enhanced winding design:

$$T_W(\varphi) = T_A + R_{th,T} \cdot \frac{P_W}{4} + \frac{q_W r_{th,W}}{4} \cdot \varphi \, (\pi - 2\varphi) \,, \tag{3.29}$$

which is valid for $\varphi \in (0, \frac{\pi}{2})$ and is periodically repeating (cf. Fig. 3.20b). The calculated temperature profile is again in good agreement with the FEM simulations. However, due to the necessary cuts in the copper layers, there are always some hot spots in the winding, which need to be considered when designing a PCB-winding close to the thermal limit. For most applications, however, it is sufficient to add a safety margin of $\approx 10\,°C$ to the maximum calculated PCB temperature.

The comparison of the temperature profiles (3.27) and (3.29) reveals the benefits of additional thermal interfaces on the temperature distribution within the winding, as the temperature drop across $R_{th,T}$ is reduced to approximately one fourth, or more generally, to $1/N_T$ of the initial value, where N_T denotes the number of thermal terminals. Furthermore, the maximum temperature difference within the winding is even reduced to $1/N_T^2$ of the initial value (which can be explained considering the lower thermal resistance besides the lower heat flux), allowing for much higher loss densities and therefore much higher RMS currents in the winding. Consequently, the number of required thermal interfaces for a certain given maximum PCB temperature can be calculated as

$$T_{W,max} = T_A + R_{th,T} \cdot \frac{P_W}{N_T} + \frac{q_W r_{th,W} \pi^2}{2 N_T^2}. \tag{3.30}$$

In addition to the enhanced thermal properties of the winding, multiple thermal interfaces improve the mechanical stability of the inductor as well, whereby a high vibration resistance is achieved, which is especially important in automotive applications.

In order to experimentally verify the derived thermal model, PCB-windings with the same dimensions as given in Fig. 3.15b, but with either one or four thermal interfaces were designed and tested. The corresponding test setups are shown in Fig. 3.21, where the winding arrangement without enhanced

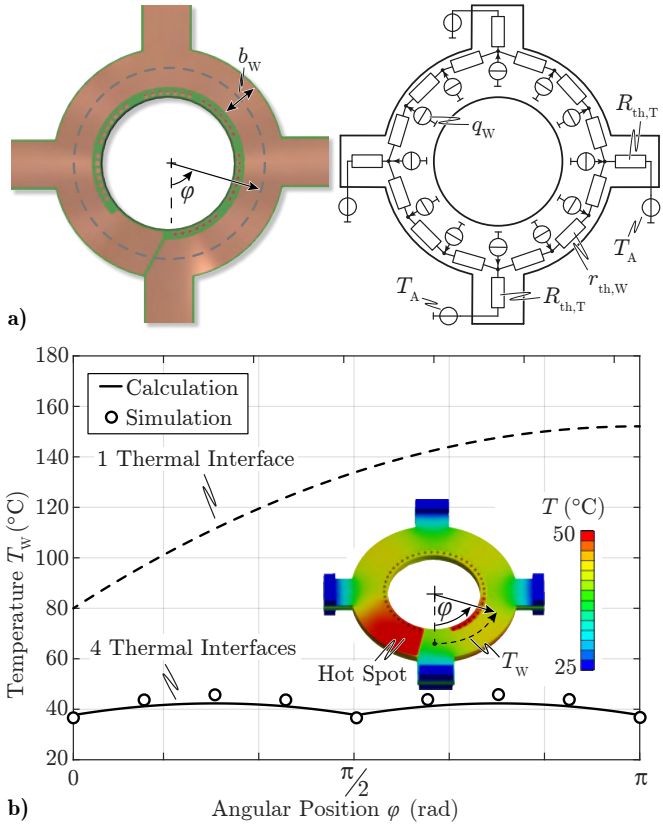


Fig. 3.20: a) Thermal model of a thermally enhanced multi-layer PCB-winding with four thermal interfaces and **b)** the respective temperature profile of the thermally enhanced PCB-winding (4 thermal interfaces) for 6 W of total losses. Additionally, the corresponding FEM simulation is shown.

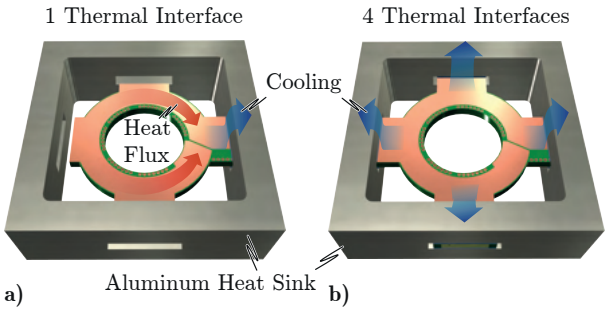


Fig. 3.21: Experimental test setups of **a)** a PCB-winding with only one thermal interface at the electric winding terminals, and **b)** the same winding but with four thermal interfaces connected to the aluminum heat sink.

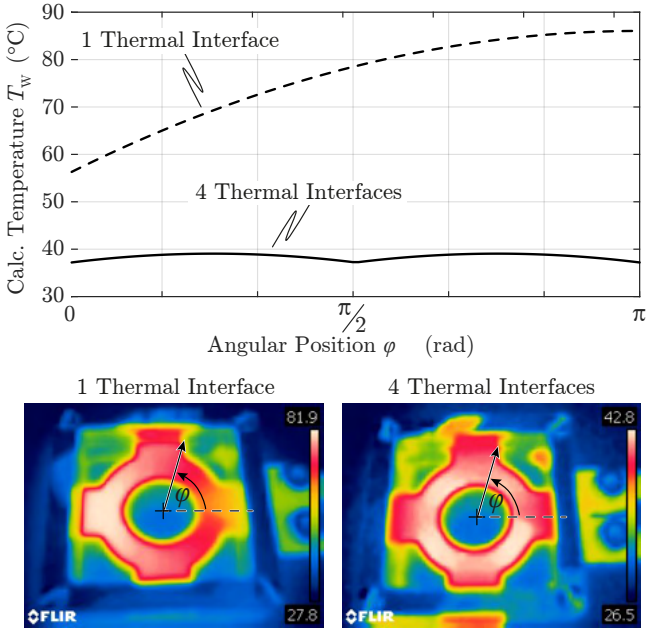


Fig. 3.22: Calculated thermal profiles of the inductors shown in Fig. 3.21, for total winding losses of 3.5 W. Additionally, the corresponding thermal images of the measured inductor temperatures are shown for the same amount of losses.

cooling is thermally connected to the quadratic aluminum heat sink only at the electric winding terminals (cf. Fig. 3.21a), while the thermally improved winding configuration is connected to the heat sink via four thermal interfaces (cf. Fig. 3.21b), as indicated by the blue arrows. In Fig. 3.22, the calculated and the measured PCB temperatures are shown for 3.5 W of conduction losses induced by a sinusoidal current of 500 kHz from a power amplifier. Based on the thermal images (aquired using a FLIR infrared camera), a high accuracy of both, the predicted peak temperatures (based on (3.29), peak temperatures of 86 °C and 39 °C are expected) as well as the measured temperature profiles can be observed. The slightly lower measured temperatures originate from the additional natural convection of the PCB-windings, which is neglected in the proposed thermal model. However, as soon as the ferrite core is placed around the PCB-winding, the contribution to the cooling due to natural convection will almost vanish. Consequently, the proposed simple thermal model can efficiently be used to optimize the thermal design of PCB-winding inductors.

However, due to the additional lateral thermal interfaces of the winding, the shape of the ferrite core needs to be adapted as well. In order to compensate for the reduced core cross-section of the outer limb (due to the cut-outs around the thermal interfaces), the total core dimensions need to be slightly increased, such that the saturation flux density of the ferrite material is not exceeded. For power density reasons, this is ideally done by changing the outer shape of the core to a square, according to Fig. 3.23. In this way, the boxed volume of the inductor is not significantly increased, but rather more efficiently used. Hence, almost homogeneous magnetic flux densities within the inner and outer limbs are again achieved. Even though the return path for the magnetic flux in the outer limbs is not concentric anymore, the fringing field around the air gap does not change, as the uniform circular air gap inherently yields a radially symmetric field distribution. Consequently, the field compensation within the winding is not affected by the shape of the outer limbs.

So far, only the winding has been considered for the thermal model of the inductor. However, there are of course also core losses generated during operation, which need to be dissipated as well. In contrast to conventional inductors, the cores of the proposed inductor design concept cannot be directly attached to an aluminum heat sink, as the fringing field around the air gap would induce substantial eddy current losses in the aluminum of the heat sink. For this reason, a free space between the top and/or the bottom

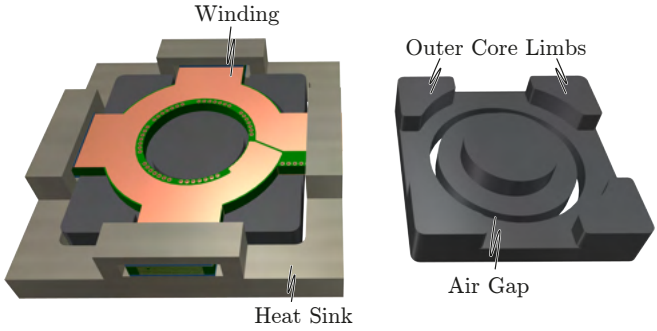


Fig. 3.23: 3D model of the adapted ferrite core shape for a winding with four thermal interfaces, connected to an exemplary aluminum heat sink.

surface of the inductor cores and any conductive material around the inductor should be left. Consequently, there are only two possible ways to dissipate the occurring core losses: On the one hand, natural or forced convection can be used, which, however, limits the allowable core losses due to a comparably low power dissipation capability. On other hand, thermally conductive epoxy resin can be used for potting the complete inductor, whereby the core pieces are thermally attached to the PCB-winding and the core losses can therefore be dissipated through the thermal interfaces of the winding as well. Consequently, the thermal interfaces would need to be enlarged in order to dissipate both, the winding losses as well as the core losses of the inductor. However, due to the complexity of this arrangement, the thermal model would be far more complicated and is therefore usually directly solved by means of FEM simulations. For this reason, it is not discussed any further in this thesis.

In the following section, the electromagnetic and thermal design process of the inductor is shortly summarized and explained considering the series-resonant inductor for the application mentioned at the beginning of this section.

3.8 Design Guidelines for PCB-Winding Inductors

In this section, the simplified design process of a PCB-winding inductor is explained, based on the specifications given in Tab. 3.1. As mentioned earlier,

the PCB of the application has eight copper layers with a thickness of 70 µm each. Consequently, from a copper utilization point of view, the ideal number of turns would be $N_L = 7$, as explained in Section 3.5. However, depending on the application, it might be better to increase or decrease the number of turns N_L, in order to find the most appropriate inductor design, even though the copper utilization would be slightly worse. For this reason, N_L is varied during the optimization of the inductor, in order to explore the widest possible design space and to find the best suited inductor design. Nevertheless, in the following, a number of turns of $N_L = 7$ is assumed (which in this specific case is also the optimum) in order to give a certain impression of the geometrical dimensions, which can be expected for inductors employing the CFFC.

Thus, based on the inductor specifications and N_L, the minimum core cross-section $A_{C,min}$ can be calculated, which is used in order to avoid saturation of the ferrite core:

$$A_{C,min} = \frac{L \cdot I_{pk}}{N_L \cdot B_{sat}} = \frac{6.8\,\mu H \cdot 25.2\,A}{7 \cdot 0.35\,T} = 70\,mm^2. \tag{3.31}$$

Hence, the minimum radius of the inner core limb is

$$r_{C,min} = \sqrt{\frac{A_{C,min}}{\pi}} = 4.7\,mm. \tag{3.32}$$

This value is of course only a lower limit and in most cases not the optimal choice regarding losses. Thus, this value is iteratively increased during the design process in order to find the optimal dimension.
Based on the core radius r_C, the mean winding length l_W for a certain winding width b_W can be calculated according to

$$l_W = N_L \cdot 2\pi \cdot \left(r_C + d_{via} + \frac{b_W}{2} \right), \tag{3.33}$$

where d_{via} denotes the additional required radius due to the clearance between the core and the PCB-winding as well as the vias of the layer transitions. As a first guess, a value of $d_{via} = 1\,mm$ can be used for applications with voltages $\leq 500\,V$ within the winding. For higher voltages, the creepage/clearance standards given in the IPC2221B standards should be followed [41]. Consequently, the simplified DC-resistance R_{DC} of the winding is calculated according to

$$R_{DC} = \frac{l_W}{\sigma_{Cu} \cdot b_W \cdot h_{Cu}}, \tag{3.34}$$

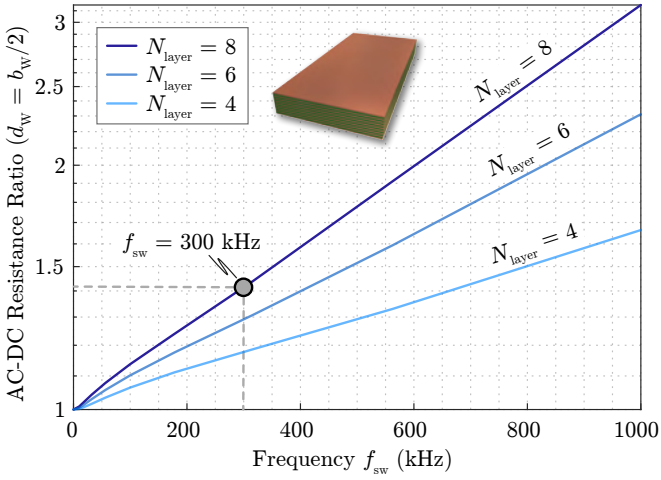


Fig. 3.24: AC to DC resistance ratios of inductor windings implemented in 4, 6 and 8 layer 70 µm PCBs for an air gap placement according to (3.11).

where σ_{Cu} denotes the electrical conductivity of copper.
In order to estimate the effectively occurring conduction losses in the winding, the AC to DC resistance ratio needs to be known. Even though this is ideally calculated by means of FEM simulations of the total inductor, a very good estimate can be found in Fig. 3.24, where the FEM-simulated AC to DC resistance ratios for 4, 6 and 8 layer 70 µm PCB pieces are shown. These ratios are independent of the actual winding width b_W, and are valid if the air gaps are placed above and beneath the winding according to (3.11).

The core losses of the inductor, however, are derived based on the inductor current waveforms and the core dimensions, which are calculated such that the same flux density in the inner and outer core limbs is achieved (cf. Fig. 3.25). Hence, based on the estimated conduction losses in the PCB-winding and a certain number of thermal interfaces N_T, the minimum width of the thermal interfaces b_{th} can be calculated, which keeps the peak temperature within the winding below the maximum allowed PCB temperature (cf. (3.30)). Using this value, the side length of the core l_C can be calculated according to the

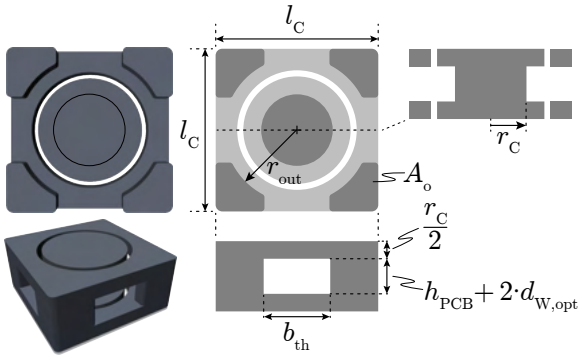


Fig. 3.25: Minimum core dimensions which are required to avoid saturation of the core material along the complete magnetic path.

simplified equation

$$l_C = b_{th} + \sqrt{\pi r_C^2 + 2r_{out}^2 - b_{th}\sqrt{4r_{out}^2 - b_{th}^2}}, \tag{3.35}$$

or using the exact solution given in Appendix A.1, which results in the same peak flux density in the inner and outer core limbs. Based on these core dimensions, the iGSE is finally applied to estimate the occurring core losses according to [38].
Hence, in order to find the most appropriate solution for a certain application, the two parameters r_C and b_W are varied and the corresponding core losses and conduction losses are calculated. This results in a performance Pareto plot, where the total losses and the characteristic length l_C of the core of the different designs are illustrated (cf. Fig. 3.26).

For the application at hand, the most power dense inductor should be chosen, which does not exceed the maximum allowable losses of $P_L = 23$ W for a maximum inductor current of $I_{L,RMS} = 17.9\ A_{RMS}$. The value for P_L originates from an overall optimization of the initially mentioned 3 kW DC/DC converter system, which was conducted with respect to power density and a targeted partial-load efficiency of $\eta = 95\,\%$ @ $50\,\%\ P_{max}$. The corresponding optimal inductor dimensions and the assembled component are shown in Fig. 3.27. It should be noted, that even though the two connectors of the inductor prototype are horizontally aligned, the terminals of the inductor are still vertically aligned along most of the current path (the transition between the

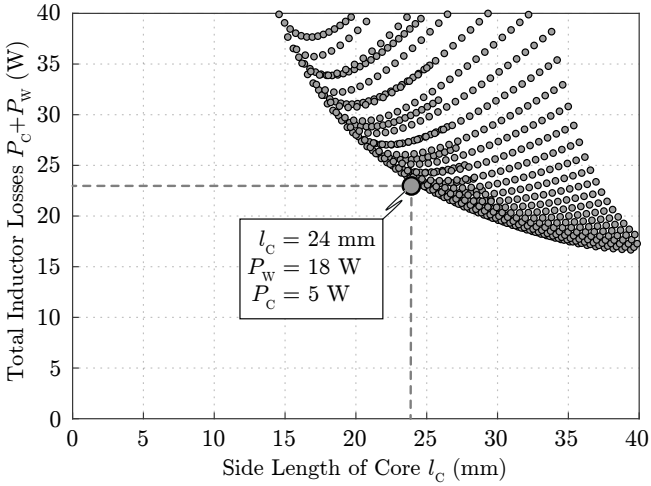


Fig. 3.26: Pareto optimization of a PCB-winding inductor according to the specifications given in Tab. 3.1. Additionally, the selected design is shown with its loss composition and the side length of the ferrite core.

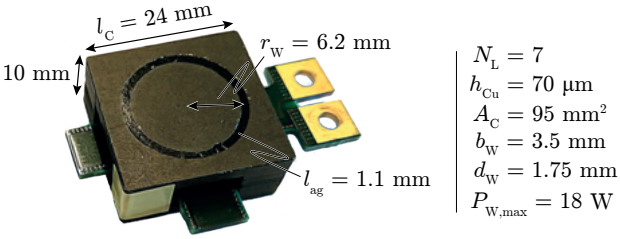


Fig. 3.27: Practically implemented 6.8 µH PCB-winding inductor with a CNC-milled ferrite core made out of N49 material.

Water Cooling	T_A	80 °C
Thermal Interface Resistance	$R_{th,T}$	9.5 K/W
Thermal Resistance of Winding	$r_{th,W}$	10.6 K/W
Max. PCB Temperature	$T_{W,max}$	150 °C

Tab. 3.2: Thermal Specifications and Parameters of the PCB-Winding Inductor shown in Fig. 3.27.

vertically and the horizontally aligned termination was only necessary to facilitate the connection of the inductor to the impedance analyzer and would not be required in a real application).
Based on these inductor dimensions, a 3D model of the inductor has been created and the frequency-dependent resistance of the winding has been simulated by means of Ansys Maxwell (cf. Fig. 3.28). The current density distribution of the first PCB layer clearly reveals the impact of the air gap on the inductor current, as the attracting force of the fringing field on the current yields a current crowding along the air gap, which counteracts the natural tendency of the current to flow at the outer edges of the PCB-winding. Hence, based on the simulation results, an AC to DC resistance ratio of ≈1.42 at $f_{sw} = 300\,\text{kHz}$ can be expected.

In order to quantify the cooling performances of different numbers of thermal interfaces, the peak temperatures $T_{W,max}$ for $N_T = 2, ..., 4$ in the core design of Fig. 3.27 have been calculated. Hence for total conduction losses of $P_{W,max} = 18\,\text{W}$ and the specifications and parameters of Tab. 3.2, the following peak temperatures can be found according to (3.30):

$$T_{W,max}(N_T = 2) = 202\,°\text{C}$$
$$T_{W,max}(N_T = 3) = 154\,°\text{C}$$
$$T_{W,max}(N_T = 4) = 132\,°\text{C}.$$

Hence, all four thermal interfaces are required in order to be able to keep the worst case inductor temperature below the thermal limit of 150 °C.
In order to verify the calculated peak temperature of the winding, the inductor has been mounted on an aluminum base plate with a temperature of $T_A = 25\,°\text{C}$. The winding was then excited by an equivalent DC current of 22.5 A, which resulted in the highest expected conduction losses of 18 W in the winding. The maximum measured temperature of the winding was $T_{W,max}(18\,\text{W}) = 80.1\,°\text{C}$, which yields a temperature difference from the hot

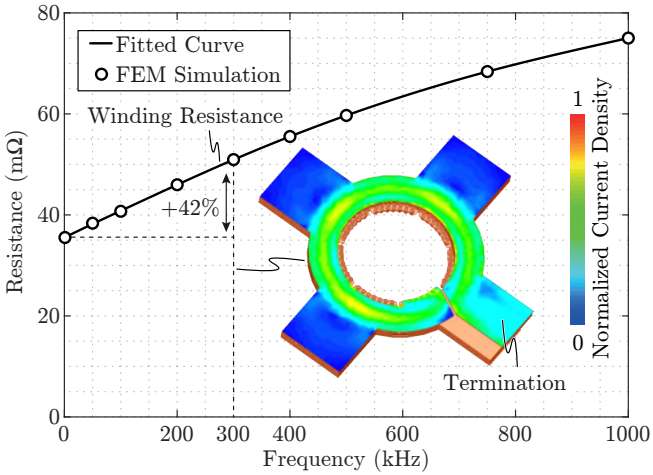


Fig. 3.28: FEM-simulated winding resistance of the PCB-winding inductor shown in Fig. 3.27 and the corresponding normalized current density distribution at 300 kHz.

spot to the heat sink of $\Delta T(18\,\mathrm{W}) = 55.1\,^{\circ}\mathrm{C}$. Hence, assuming a maximum heat sink temperature of $T_\mathrm{A} = 80\,^{\circ}\mathrm{C}$ (cf. Tab. 3.2), the hot spot temperature within the winding would be $T_\mathrm{W,max} = 135.1\,^{\circ}\mathrm{C}$ in the final converter system, which is in good agreement with the estimated maximum temperature of 132 °C.

Based on this measurement, the maximum allowable AC to DC resistance ratio at 300 kHz can be calculated according to

$$\frac{R_\mathrm{AC}(300\,\mathrm{kHz})}{R_\mathrm{DC}} \propto \frac{I^2_\mathrm{RMS,DC}(P_\mathrm{W} = 18W)}{I^2_\mathrm{RMS,AC}(P_\mathrm{W} = 18W)} = \frac{22.5^2}{17.9^2} = 1.58. \tag{3.36}$$

Hence, at 300 kHz where the maximum RMS currents of 17.9 A_RMS will occur, an AC to DC resistance ratio below 1.58 should be achieved, such that the peak temperature of the winding stays below the targeted 132 °C.
The actual AC to DC resistance ratio of the PCB-winding can be measured using an impedance analyzer, whereby an AC to DC resistance ratio of 1.49 @ 300 kHz has been found, which yields a safety margin of 6 % before the maximum calculated PCB temperature is reached. As the inductor currents for higher switching frequencies are significantly lower, only the AC to DC resistance ratio at 300 kHz needs to be considered here. However, in other

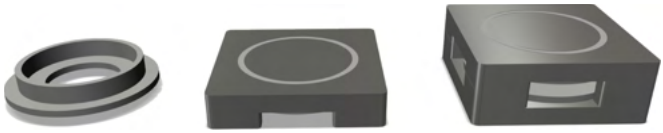


Fig. 3.29: Plastic core holder which is used to fix the individual core pieces.

applications, this might be different, which is why the losses over the full switching frequency range should be calculated, in order to find the absolute worst case inductor losses. If the measured AC to DC resistance ratio should be higher than the one found in (3.36), a larger number of air gaps could be used in order to improve the magnetic field compensation and therefore reducing the AC to DC resistance ratio of the winding. Alternatively, more and/or wider thermal interfaces could be used in order to decrease the thermal resistance of the PCB-winding.
Consequently, these measurements show the applicability and feasibility of the proposed PCB-winding inductor design concept in practical applications, which is why it will also be used in the three-port DC/DC converter systems, which are developed in the further course of this work.

However, in practical implementations of this concept, some mechanical challenges are arising, especially if the inductors are employed in a harsh operating environment, as e.g. in automotive applications, where sensitivity to vibration is a serious issue. Thus, even though the manufacturing of large quantities of the different core parts is not very difficult, as the same forming and sintering processes as for conventional ferrite cores can be applied, it is essential to end up with a stable assembly of the total inductor by fixing the individual parts of the core sturdily. This can be achieved by potting the core using a thermally conductive epoxy resin, which then guarantees a stable mechanical connection among the individual core parts, as well as between the core and the PCB-winding. Alternatively, a plastic core holder as shown in Fig. 3.29 can be used, which is glued to the individual ferrite pieces and ensures both, a homogeneous air gap length along the circular air gaps, as well as the optimal distance between the winding and the air gap. The two resulting core halves can then be treated as conventional E or EQ cores and can be attached to the PCB by means of clamps.
Another issue, which needs to be addressed in a practical application, is the isolation between the winding and the inductor core. Even though the re-

quired clearance between the edges of the PCB and the most outer PCB track (which is given by the PCB manufacturer ($\approx 200\,\mu m$)) is usually sufficient to guarantee full galvanic isolation between the core and the winding, a more elaborate isolation method might be required in high-voltage applications. In order to ensure a certain required isolation, Kapton tape can be wrapped around the inner and the outer core limbs to separate the PCB from the ferrite core, or, more production-friendly, the complete core could simply be coated. Thus, the proposed inductor design concept can even be used in high-voltage applications.

In the following chapter, the in-system performance of the proposed CFFC, and in particular the PCB-winding inductor of Fig. 3.27 will be tested in the aforementioned 3 kW 500 V/15 V DC/DC step-down converter hardware prototype, which has been built according to the specifications of the blue-shaded converter stage in Fig. 1.2a.

3.9 Summary of the Chapter

In this chapter, the concept of actively utilizing the fringing field around a single air gap or multiple (distributed) air gaps for compensating the parasitic magnetic fields (as e.g. skin and proximity fields) in planar conductors has been investigated, based on analytical and numerical calculations. Hence, as initially observed in the TAB hardware demonstrator, an appropriately positioned air gap has a highly beneficial effect on the HF conduction losses in planar conductors, as it effectively counteracts the adverse magnetic skin and proximity fields. Based on different FEM simulations, a remarkable effectiveness of the proposed concept has been found, independent of the number of air gaps, or the shape of the winding. Consequently, compared to state-of-the-art PCB-winding inductors, significantly lower HF conduction losses can be achieved, as has been shown by means of various experimental measurements.
The proposed loss model of the PCB-winding allows for an accurate prediction of the occurring conduction losses and, therefore, can directly be used in simple design optimization algorithms. Furthermore, an accurate thermal model of the PCB-winding has been introduced, which allows to estimate the temperatures within the PCB-winding for a given amount of conduction losses. It has been shown, that a utilization of multiple thermal interfaces allows for operating the inductor with very high current densities, whereby highly power-dense inductor designs are obtained. However, even though

the proposed field compensation concept results in low AC to DC resistance ratios and, therefore, a good copper utilization even for very high frequencies, the limited available copper in a PCB impedes the design of PCB-winding inductors which are highly efficient and power-dense at the same time. Hence, compared to solid wire inductors, the winding fill factor of inductors with a PCB-winding will always be lower and thus the efficiency often as well. Nevertheless, as proven in this chapter by multiple experimental hardware prototypes, the extremely high allowable current densities in PCB-windings outweigh the lower winding fill factor, whereby highly power-dense and cost-effective inductors can be built, where especially the latter is of particular importance in automotive applications.

4

Two-Port Series-Resonant DC/DC Converter

Chapter Abstract

In the chapter about the triple-active-bridge (TAB) converter, it has been found, that a resonant converter topology and especially a synchronous rectifier in the LV port are the most suitable solutions for the application at hand, as high harmonics of the transformer currents can be avoided and at the same time, the low-voltage (LV) semiconductors are operated under zero-voltage-switching (ZVS) and zero-current-switching (ZCS) conditions. However, before starting to develop novel three-port DC/DC converter topologies, it should first be verified, that the above assumptions are correct, which is why in this chapter a conventional 3 kW 500 V/15 V series-resonant step-down converter is designed and built. Hence, this hardware prototype is finally used to test the LV synchronous rectification, an appropriate PCB-winding transformer design, which is capable of handling the very high currents of the LV port, as well as the feasibility of employing PCB-winding inductors, which use the previously introduced compensating fringing field concept (CFFC).

4.1 Two-Port Series-Resonant Converter Topology

The most simple isolated DC/DC resonant converter topology is a series-resonant converter, which comprises a full-bridge on the primary side, a *L*-*C* series-resonant tank between the full-bridge and the transformer, as well as some sort of synchronous rectifier on the secondary side (cf. Fig. 4.1). Even though for power density reasons, the leakage inductance of the PCB-winding

V_{in}	250…500 V
V_{out}	10.5…15 V
P_{max}	3 kW (max. $I_{\text{out}} = 200$ A)
Efficiency (@V_{nom})	$\eta > 95\,\% \text{ for } 30\,\% \cdot P_{\text{max}} < P_{\text{out}} < 50\,\% \cdot P_{\text{max}}$
Target Power Density	As high as possible

Tab. 4.1: Specifications of the two-port series-resonant DC/DC converter.

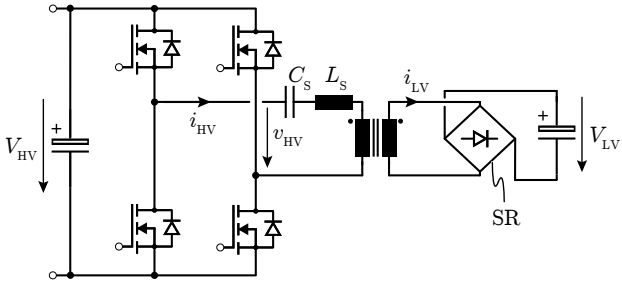


Fig. 4.1: Simplified two-port series-resonant DC/DC converter with an arbitrary synchronous rectifier (SR).

transformer is usually used as series-resonant inductance, this is often not possible in applications with widely varying port voltages, as the required inductance value for an efficient converter operation is very large. Thereby, it is often more efficient to use discrete external inductors. In the application at hand, the two-port converter is designed according to the specifications of the second converter stage shown in Fig. 1.2a, which are repeated in Tab. 4.1. Hence, due to the wide port voltage ranges of the primary and secondary side of the converter in this application, the use of the transformer's leakage inductance as resonant inductor would result in an extremely inefficient transformer design, which is why an external discrete inductor needs to be employed. However, this inductor can be designed according to Chapter 3, whereby a power-dense and cost-effective implementation can be expected.

The control of this topology relies on two different parameters: the variable switching frequency f_{sw} and the duty cycle D of the primary-side rectangular voltage v_{HV}, which is generated by means of the primary side full-bridge (cf. Fig. 4.2). Hence, depending on the output load and the switching frequency, two different conduction modes can be distinguished. On the one

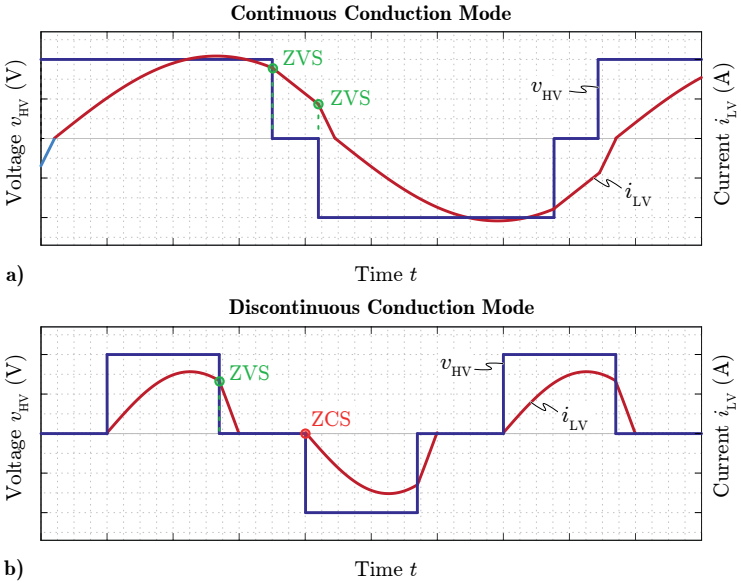


Fig. 4.2: Voltage waveform generated by the high-voltage (HV) full-bridge v_{HV} and the transformer current i_{LV} for **a)** continuous conduction mode and **b)** discontinuous conduction mode.

hand, the continuous conduction mode (CCM), where the current is almost sinusoidal and both HV-side half-bridges are soft-switched (cf. Fig. 4.2a) and, on the other hand, the discontinuous conduction mode (DCM), where certain zero-current intervals are introduced and only one half-bridge is operated under ZVS conditions (cf. Fig. 4.2b). The remaining half-bridge is operated under ZCS conditions only, whereby the Q_{oss}-related energy of these switches is dissipated.
Consequently, the converter should be operated in CCM for as long as possible, but below a certain output power P_{lim}, the required switching frequency for CCM would be too high, accordingly the switching frequency is limited to $f_{sw,max}$ and DCM is used.

In order to optimize the design of this simple two-port converter system, the loss models for all power components need to be derived, which can then also be used later in the design algorithms of the three-port DC/DC converter systems. Hence, in the application at hand, appropriate loss models for the HV

semiconductors, the PCB-winding transformer, the series-resonant inductor as well as the LV synchronous rectifier switches need to be derived, which will finally be used to conduct a multi-objective optimization with respect to power density and efficiency. These loss models are discussed in detail in the next section.

4.2 Loss Models

In this section the different loss models of the most important components are introduced in detail and, where required, simple design guidelines are provided. First, the electrical requirements for the semiconductors are discussed and the considered loss mechanisms are explained. Subsequently, the design of the PCB-winding transformer with winding-integrated synchronous rectifier switches and output capacitors is presented. Finally, the new CFFC design approach for PCB-winding inductors is shortly revisited, as this is by far the most difficult component to design and to integrate into the PCB in an efficient way.

4.2.1 Semiconductor Loss Model

In the application at hand, all semiconductors are either switched with zero current (ZCS) and/or zero voltage (ZVS) in all operating conditions. Thus the total semiconductor losses can be calculated comparably easy by adding up the well-known conduction losses $P_{\mathrm{MOS,c}}$, given by

$$P_{\mathrm{MOS,c}} = R_{\mathrm{DS,on}}(T_{\mathrm{j}}) I_{\mathrm{RMS}}^2, \tag{4.1}$$

where T_{j} denotes the junction temperature of the switch, and the total occurring switching losses $P_{\mathrm{MOS,sw}}$. Thereby, $P_{\mathrm{MOS,sw}}$ comprises three different components, namely, the gate drive losses $P_{\mathrm{MOS,gate}}$, the worst case C_{oss} losses $P_{\mathrm{MOS,Coss}}$ and the conduction losses $P_{\mathrm{MOS,diode}}$ due to the current in the anti-parallel diode during the commutation intervals. The switching losses can therefore be expressed as

$$P_{\mathrm{MOS,sw}} = P_{\mathrm{MOS,gate}} + P_{\mathrm{MOS,Coss}} + P_{\mathrm{MOS,diode}}, \tag{4.2}$$

with

$$P_{\mathrm{MOS,gate}} = Q_{\mathrm{gate}} V_{\mathrm{gate}} f_{\mathrm{sw}}, \tag{4.3}$$

$$P_{\mathrm{MOS,Coss}} = Q_{\mathrm{oss}} V_{\mathrm{DS}} f_{\mathrm{sw}} \tag{4.4}$$

$$P_{\mathrm{MOS,diode}} = V_{\mathrm{f}} I_{\mathrm{D}} t_{\mathrm{d}} f_{\mathrm{sw}}, \tag{4.5}$$

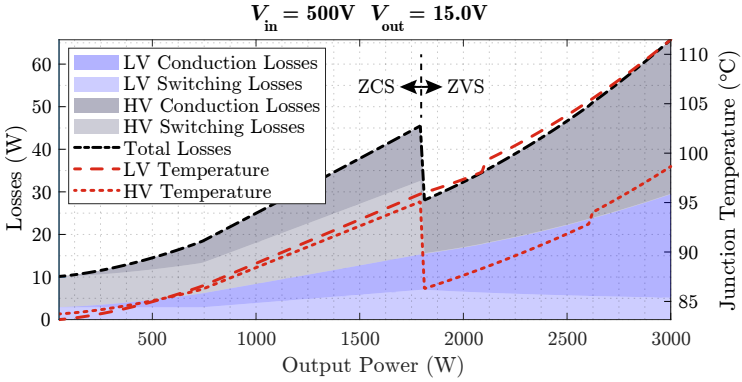


Fig. 4.3: Semiconductor losses and junction temperatures for different output power levels and exemplary HV and LV semiconductors.

where V_f, I_D and t_d denote the forward voltage of the anti-parallel diode, the current in the diode during the commutation interval and the dead time, respectively. The C_{oss} losses are only accounted for, if the drain current during the switching transient is zero. Hence, only in the discontinuous conduction mode (DCM) of the converter.

Due to the temperature dependent $R_{DS,on}$ of the switches, it is important to consider the junction temperature T_j in the optimization as well. For this reason, the junction temperature is calculated iteratively based on a thermal model including the package of the switch, a thermal interface material (TIM) as well as a heat sink.
The results of such an optimization are shown in Fig. 4.3, for an input voltage of 500 V and an output voltage of 15 V with increasing output power. The transition from DCM to CCM operation can easily be seen, as in DCM, the leading leg of the primary (HV) side full-bridge is switched with zero current only, whereby the output charge Q_{oss} of the switches is dissipated and, therefore, significant switching losses occur. Consequently, a switch with a superior figure-of-merit and a well-suited trade-off between low $R_{DS,on}$ and low C_{oss} is required. Hence, wide band-gap semiconductors are most suitable in this application (at least on the primary side).
On the secondary side, soft-switching is achieved in all operating modes, whereby a low $R_{DS,on}$ is the most important criteria for these switches. Consequently, silicon switches are a promising solution for the rectifier switches,

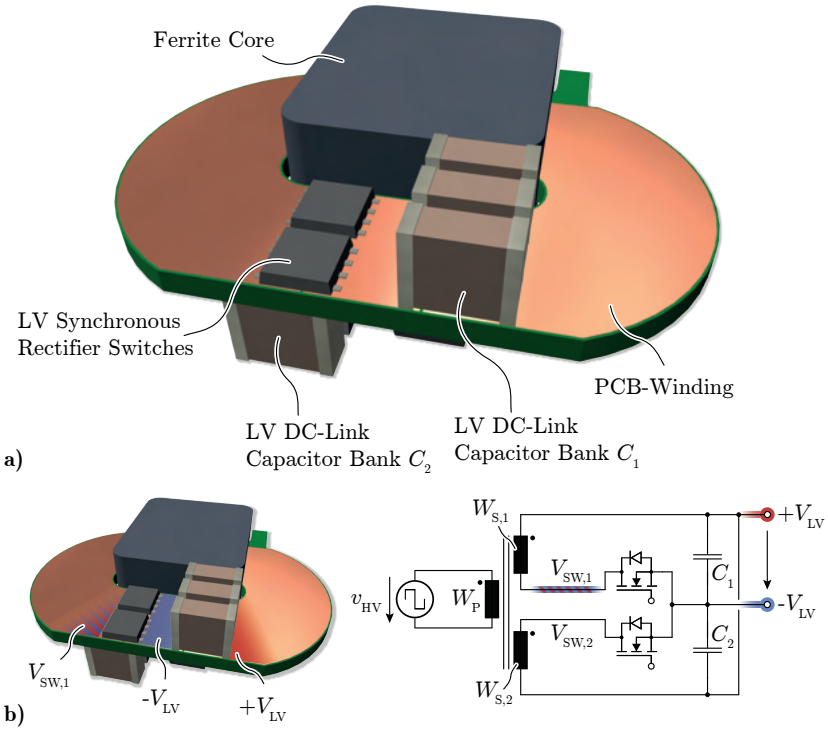


Fig. 4.4: a) PCB-winding transformer design with winding-integrated rectifier switches and DC-link capacitors and **b)** circuit of the employed center-tapped rectifier.

especially due to their low material costs.
In the optimization script, the losses for a large number of different HV and LV switches are calculated, in order to find the best solution for the given application. However, as will be explained in the following, the selection of the switches not only affects the semiconductor losses in the converter, but also the design and therefore the losses of the PCB-winding transformer, as the package of the LV switches has a strong impact on the width of the LV winding of the transformer, as will be shown in the following.

4.2.2 PCB-Winding Transformer Design

In the application at hand, the main design challenge of the PCB-winding transformer are the large winding currents of up to 250 A_{RMS} in the secondary low-voltage (LV) winding. Hence, it is very difficult to keep the conduction losses at a reasonable level and at the same time achieve a high power density, as a PCB is not very suitable to carry large high-frequency currents, due to the small available copper cross-section A_W in PCBs. The effective copper cross-sectional area $A_{W,eff}$ is even further reduced, as the time varying magnetic fields perpendicular to the PCB result in a current displacement in lateral direction and, therefore, only a fraction of A_W is effectively utilized.

Fortunately, these perpendicular magnetic fields can be minimized by using a vertically aligned arrangement of the primary and the secondary windings, as the opposite flow directions of the winding currents result in a destructive interference of the perpendicular magnetic field components (skin and proximity fields). However, this is only applicable within the winding area itself, where the primary and secondary currents flow anti-parallel. The terminations of the windings still suffer from the aforementioned HF effects, which is why a termination of the secondary winding should be avoided at all costs.
The only way to avoid the termination of a winding is an integration of both, the rectifier switches as well as the output capacitors right into the winding, which is e.g. possible if a center-tapped rectifier is used. This rectifier topology is in particular suitable in applications with large output currents, as the total output current is split among two sub-windings ($W_{S,1}$ and $W_{S,2}$), whereby the current stresses of each sub-winding can be reduced (cf. Fig. 4.4b). This approach is used in the proposed transformer design, as shown in Fig. 4.4a. Thus, the rectifier switches as well as the output capacitors of the first branch of the center tapped rectifier are located on the top side of the PCB, whilst the switches and the capacitors of the second branch are soldered to the bottom side of the PCB. Consequently, the DC load current can directly be extracted from the two DC-link capacitor banks, whereby the PCB track length of the HF currents of the secondary side are minimized.
In order to optimize the overall copper usage, the different layers of the PCB could be distributed among the windings as shown in Fig. 4.5. Hence, four layers are allocated to the primary winding W_P, while the remaining four layers are used for the secondary side windings W_{S1} and W_{S2}. This distribution yields a homogeneous current density throughout the windings and minimizes the proximity effects in vertical direction, which is important due to

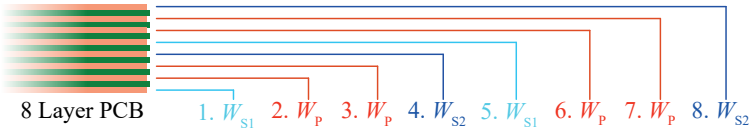


Fig. 4.5: Distribution of the eight available PCB layers among the three windings W_P, W_{S1} and W_{S2}.

the parallel connection of the secondary side winding layers 1 and 5 as well as 4 and 8, respectively.
However, the available copper cross-section in the PCB is in general extremely small, which is why it is usually beneficial to solder additional copper foils to the top and the bottom of the PCB, whereby these two copper foils are used for the large LV currents, and at the same time, the six remaining inner layers can be used for the HV winding. In addition to the significantly increased copper cross-section of the windings, the thermal design of the transformer is also improved, as the additional copper layers are excellent thermal conductors and help to dissipate the occurring conduction losses in the transformer.

PCB-Winding Transformer Optimization

The final design of the aforementioned PCB-winding transformer depends on two main limitations: On the one hand, the minimum required core area in order to limit the core losses and to prevent saturation of the transformer, and on the other hand, the winding width, which is mainly defined by the maximum allowable copper losses of the winding and the package of the secondary side switches. The latter limitation is explained in the following in more detail.
Even though, in theory, the width of the PCB-winding can arbitrarily be chosen, in a practical implementation the winding width is restricted to a limited range of values. This comes due to the fact, that the current at some point needs to enter the source of the rectifier switch and leave the drain before flowing into the low voltage output capacitor bank. Hence, no matter how wide the winding is, within the LV switches, the width of the current path is limited to the size of the MOSFET package. If this package is small compared to the winding width, the vertically aligned current distribution between primary and secondary winding is lost, and the proximity effect is significantly exacerbated (cf. Fig. 4.6a). Thus, increased conduction losses

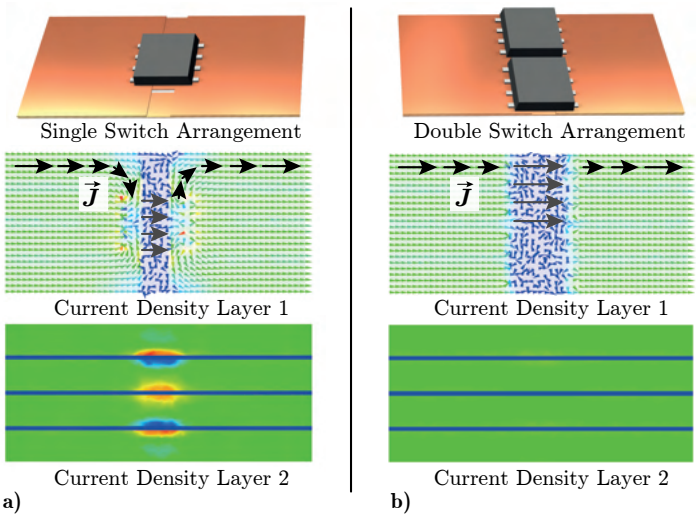


Fig. 4.6: Current densities in the two windings for four turns of the HV winding and a single turn of the LV winding with **a)** a winding width larger than the package width of the switch and **b)** a winding width equal to the package width of the switches.

result, even though they could easily be avoided by correlating the dimensions of the PCB-winding and the one of the LV switch packages. Consequently, the width of the winding should match the width of the semiconductor package (switches with small packages can be placed in parallel), whereby a homogeneous current density results, even in the subjacent primary winding (cf. Fig. 4.6b).
The transformer optimization routine is therefore closely linked to the selection of the synchronous rectifier switches, which is why for every possible LV switch, the suitable transformer design is calculated (winding width equal to the width of the package(s) of the switch) and the corresponding losses for two different operating points are calculated ($P_{\text{out}} = P_{\text{max}}$ and $P_{\text{out}} = 50\,\% \cdot P_{\text{max}}$). The results are shown in Fig. 4.7, where each number corresponds to a certain converter design comprising HV switches, LV switches, transformer and inductor. Based on the numbers of the different converter designs, it can be seen that there is always a trade-off between the efficiency for maximum output power and for partial power. However, there are designs which provide a comparably high efficiency and a small PCB area, i.e. high power density, over the whole important output power range ($P_{\text{out}} > 30\,\% \cdot P_{\text{max}}$), as e.g.

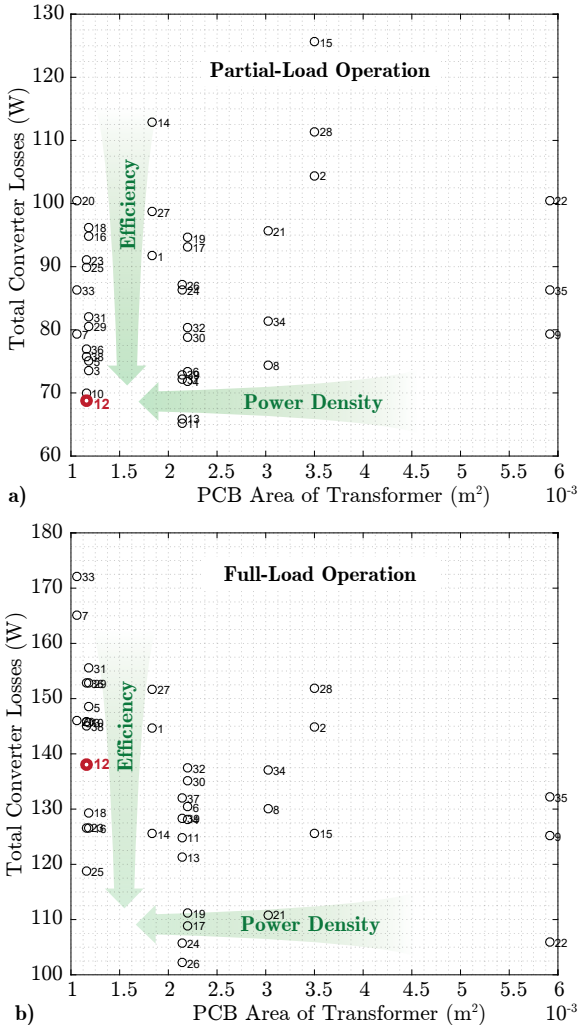


Fig. 4.7: a) Total converter losses for 50 % (1.5 kW) output power for all suitable designs and **b)** the converter losses for full power (3 kW) of the same designs.

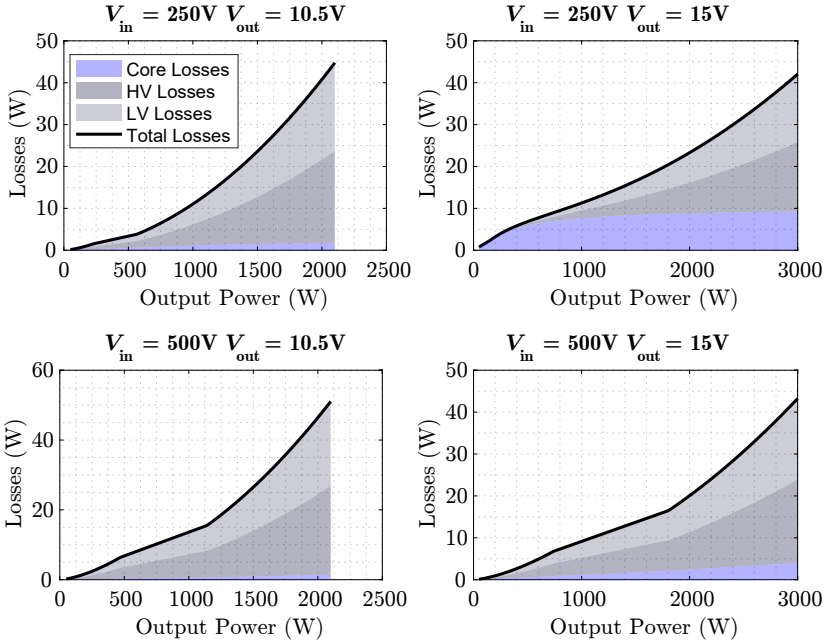


Fig. 4.8: Transformer loss distribution for different input and output voltages. Due to the allocation of the different PCB layers and the additional copper foils (h_{cu} = 0.3 mm), the LV and the HV winding losses are almost the same in all operating conditions.

design number ○**12**.
The detailed loss distribution within the transformer for this design can be found in Fig. 4.8b and its dimensions and properties are listed in Tab. 4.2.

The significant amount of occurring losses within a comparably small PCB area, together with the winding-integrated LV switches on both sides of the PCB, requires a sophisticated cooling concept in order to limit the PCB temperature and the junction temperature of the switches to acceptable levels. Such a cooling concept is shown in the following, where only one larger water-cooled heat-sink is required, where all heat generating components are thermally connected to.

Number of Turns	LV Winding Width	Core Area	Core Material
16:1	11 mm	87 mm^2	N49

Tab. 4.2: Specifications of the PCB-winding transformer.

PCB-Winding Transformer Cooling Concept

In most applications, the system is designed in such a way, that only one heat sink (e.g. on the bottom side of the PCB) is required. Hence, all lossy components are placed on the bottom side of the PCB, such that they can easily be connected to the heat sink. Unfortunately, this is not possible for the transformer design at hand, as the rectifier switches are placed on both sides of the PCB. Hence, at least one of the switches cannot directly be connected to the main heat sink.
For this reason, a thermal path with a low resistance is required in order to extract the heat from the top side switches and to dissipate it to the main heat sink on the bottom side of the PCB. Using the approach shown in Fig. 4.9, where additional heat sink extensions are screwed to the main heat sink and, therefore, clasp the transformer from both sides, both, the top side switches as well as the top side copper foil of the winding can thermally be connected to the main heat sink. Consequently, a higher loss density is allowed and, therefore, a higher power density is achieved.

In the final hardware, there is only one PCB for all components. Hence, the PCB-winding transformer will be embedded in this PCB and suitable cutouts for the top-side heat sink extensions need to be provided, as exemplarily shown in Fig. 4.10.
In the same PCB, the resonant inductor will be embedded as well. However, the design of this component has already been discussed in detail in Chapter 3, which is why only the results are given here.

4.2.3 PCB-Winding Inductor Design

In order to find the optimal PCB-winding inductor for the given application, a large number of different inductor designs are calculated based on the design rules which were introduced in Chapter 3 and the given specifications as e.g. the peak current $I_{\mathrm{L,pk}}$, the maximum rms current $I_{\mathrm{L,rms}}$ as well as the required total inductance L. All inductor designs differ either in their number of turns N, the core area A_{C} or the winding width b_{W}. However, these values are

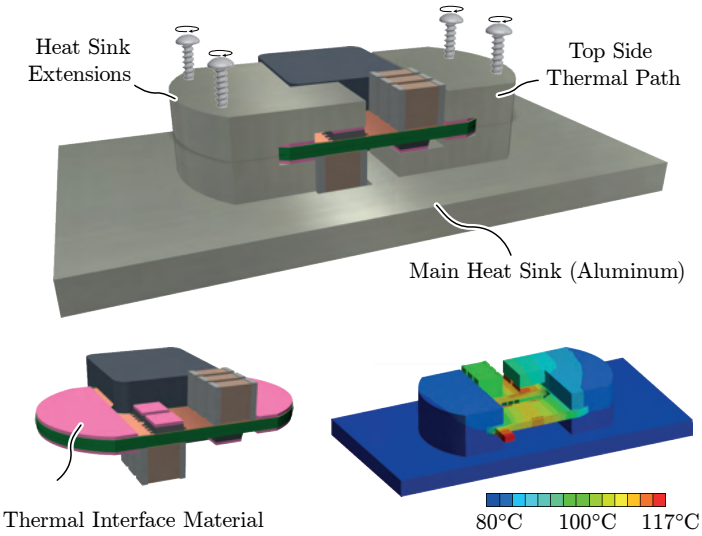


Fig. 4.9: Thermal connection of the PCB-winding transformer and the rectifier switches to the main heat sink.

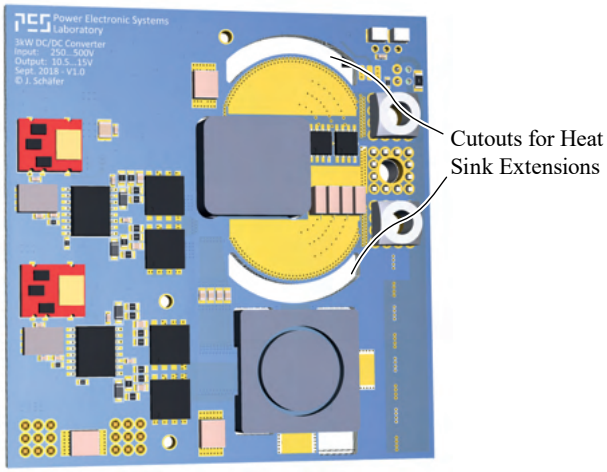


Fig. 4.10: Cutouts for the heat sink extensions in an exemplary PCB design of the complete converter.

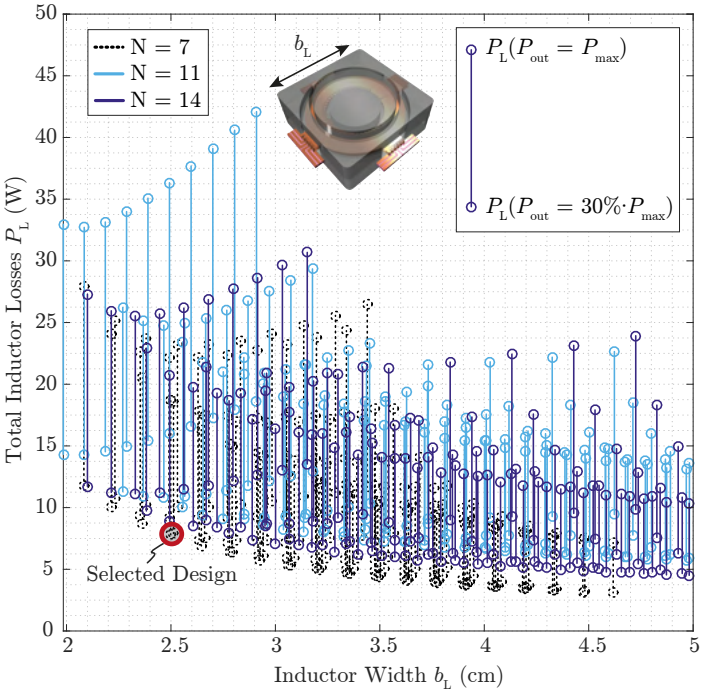


Fig. 4.11: Inductor optimization results where all different kinds of inductor designs are calculated and their total losses for both $P_{out} = P_{max}$ and $P_{out} = 30\,\% \cdot P_{max}$ are shown.

subject to specific limits, as the minimum core area is given by the minimum required saturation current $I_{L,pk}$, the minimum winding width is limited by the maximum allowable current density in the winding (thermal limit) and finally, the number of turns N, which can be either one turn per layer (7 turns in an 8 layer PCB), two turns per layer ($N = 14$), or alternating with one and two turns per layer ($N = 11$). The results of such an optimization are shown in Fig. 4.11, where the losses for each inductor design are calculated twice: First for full output power (lowest switching frequency), where the highest conduction losses are induced, and second for the output power where the highest switching frequencies occur, as in this operating point the core losses are significantly increased.

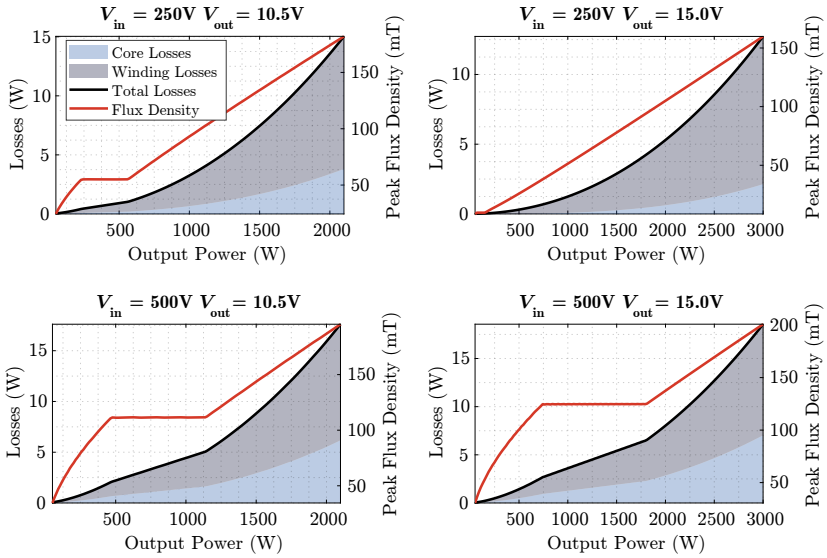


Fig. 4.12: Detailed loss distribution of the selected inductor design for different input and output voltage levels.

After selecting the most suitable inductor design (in this application: b_L = 2.5 cm, N = 7) which features both, low losses as well as high compactness, the detailed loss distributions are calculated for all crucial input and output voltage levels (min, max values) and the whole power range. Such a loss distribution graph is shown in Fig. 4.12, where the flux densities inside the inductor can be found as well.
In the following section, the loss models of all the components are merged together, in order to find the overall efficiency of the selected converter system.

4.3 Converter Optimization

In this section, the basic framework of the optimization for the series-resonant converter is introduced and the corresponding results are discussed. First of all, the optimization framework needs the main specifications of the final converter system, in order to be able to optimize and select all different kinds of power components. These specifications are given by the customer and

HV Switches	LV Switches	Transformer
Breakdown Voltage	Breakdown Voltage	Turns Ratio
$V_{\mathrm{DS,max}} > 500\,\mathrm{V}$	$V_{\mathrm{DS,max}} > 30\,\mathrm{V}$	$n = \frac{N_{\mathrm{HV}}}{N_{\mathrm{LV}}} = \frac{16}{1}$

Tab. 4.3: Specifications and limits of the power components.

they are listed in Tab. 4.1.

Based on these values, together with the known topology of the converter (cf. Fig. 4.1), the first physical limits and specifications of certain components are calculated. These values are summarized in Tab. 4.3, where it needs to be noted, that the LV MOSFETs should be avalanche rated, in order to survive possible overvoltages during the commutation intervals (center-tapped rectifier specific behavior).
The breakdown voltages mainly affect the pre-selection of possible power switches, which should be chosen in such a way, that a certain safety margin between the calculated $V_{\mathrm{DS,max}}$ and the corresponding datasheet value is guaranteed. However, in order to calculate the voltage and current stresses of the other components as well, the actual voltage and current waveforms need to be known, as they directly affect the occurring losses in the power components. Hence, for different sets of resonant frequencies f_{res} and $L_{\mathrm{S}}/C_{\mathrm{S}}$ ratios, the current and voltage waveforms can be calculated analytically and are then used to run the optimization scripts of the individual components. The simplified sequence of the overall optimization is shown in Fig. 4.13, where the main steps are illustrated by means of a flow chart.

Hence, starting with the converter specifications, the component stresses are calculated for a parameter sweep of f_{res} and $L_{\mathrm{S}}/C_{\mathrm{S}}$, whereby for each set ($f_{\mathrm{res}}$,$L_{\mathrm{S}}/C_{\mathrm{S}}$) a complete converter optimization is conducted. Thus, the capacitor volume and losses are calculated in parallel to the series-resonant inductor optimization, followed by the appropriate selection of the primary side semiconductors. Subsequently, the LV semiconductors are selected and the PCB-winding transformer is designed. This then yields a large number of possible converter designs, which, however, are very difficult to evaluate, as there are hardly any converter designs which perform well for both, partial-load as well as full-load operation. Consequently, out of all possible solutions, the most power-dense converter design is selected, which fits best to the

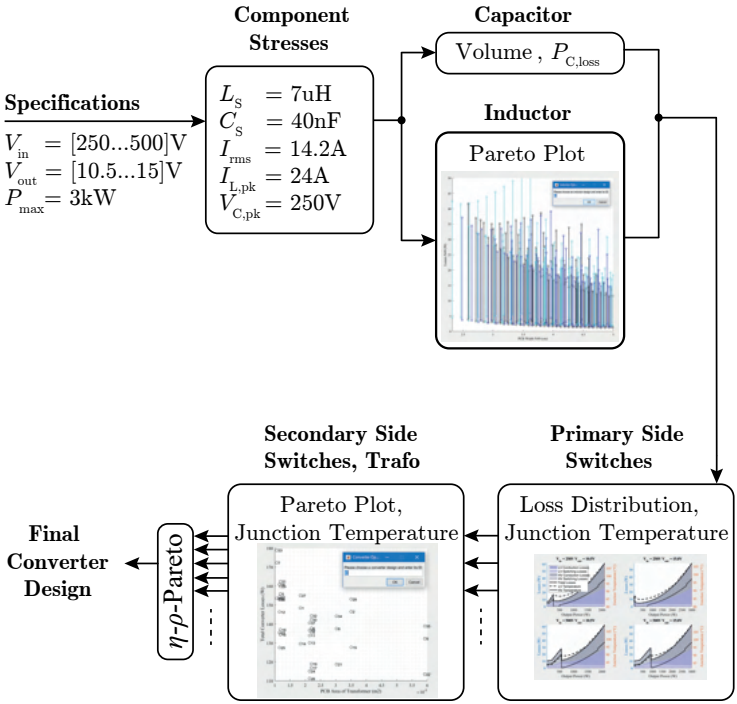


Fig. 4.13: Simplified sequence of the overall optimization routine for a series-resonant converter.

targeted partial-load efficiency of 95 %.
For this final converter design, the overall efficiency for different input and output voltages and variable output power values are then calculated, as shown in Fig. 4.14.

The step in the efficiency characteristic originates from the transition between the continuous and the discontinuous conduction mode (DCM), as in continuous conduction mode (CCM), all switches are soft-switched and the switching losses are almost negligible, whereas in DCM, one half-bridge of the primary side is zero-current-switched only, whereby significant C_{oss} losses occur. These C_{oss} losses could be reduced in the final hardware by operating the converter with a lower switching frequency in DCM, however this requires a sophisticated control strategy, which is out of the scope of this work, as this hardware is only used for reference purposes.

In order to verify the loss models and the operation of the converter, the two-port series-resonant converter has been implemented in hardware and the achievable performance has been experimentally measured. The final design of the hardware demonstrator and the corresponding measurement results are discussed in the following section.

4.4 Experimental Results

The most suitable two-port resonant converter design, found in the last section, has finally been built in hardware, according to the preceding considerations. Thus, the HV full-bridge is built around four IGLD60R070D1 600 V GaN switches from Infineon, as they feature a comparably low $R_{\mathrm{ds,on}}$ and E_{oss}, which is especially important due to the partial ZCS operation during DCM. In contrast to the initial PCB design of Fig. 4.10, the inductor has been separated from the main PCB, in order to test different inductor designs, which can then be connected to the circuit via connectors (cf. Fig. 4.15). In the first commissioning phase, a wire-wound inductor with a litz wire winding has been used for simplicity reasons, however, the final efficiency measurements have then been conducted using the PCB-winding inductor shown in Fig. 3.27, which employs the previously introduced CFFC. Consequently, a compact and efficient PCB-winding inductor design was achieved, which could directly be integrated into the PCB of a final converter product.

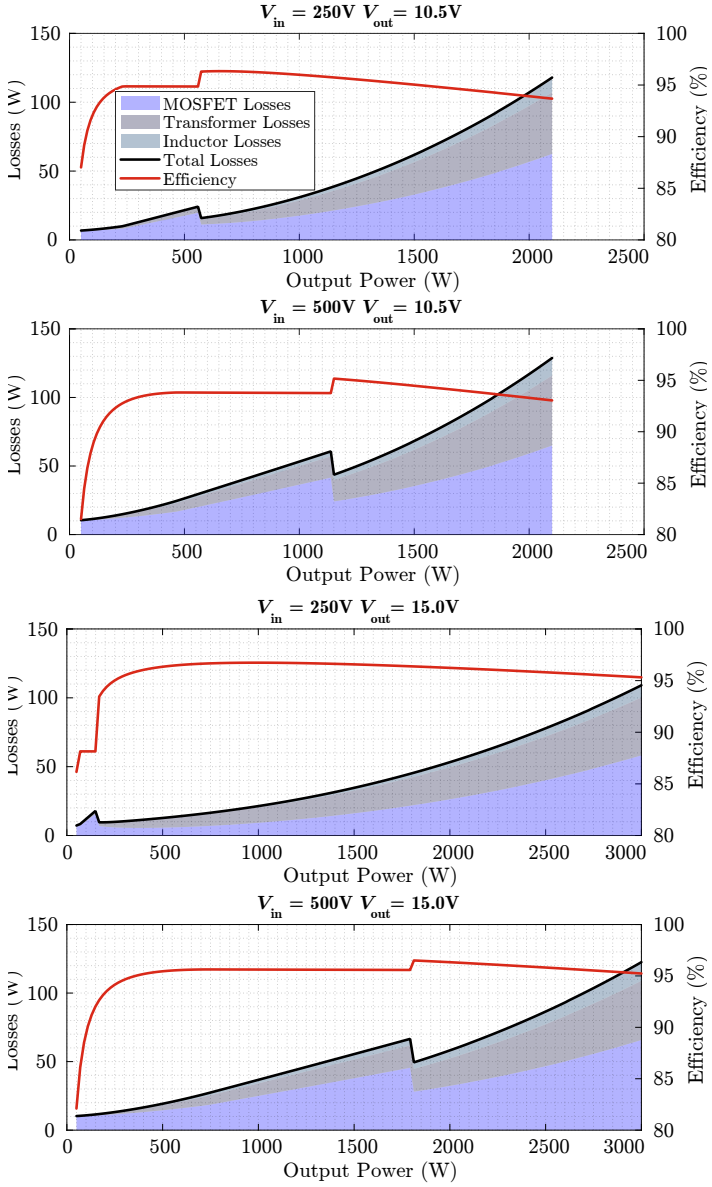


Fig. 4.14: Calculated efficiency of the overall two-port series-resonant converter system for different input and output voltages.

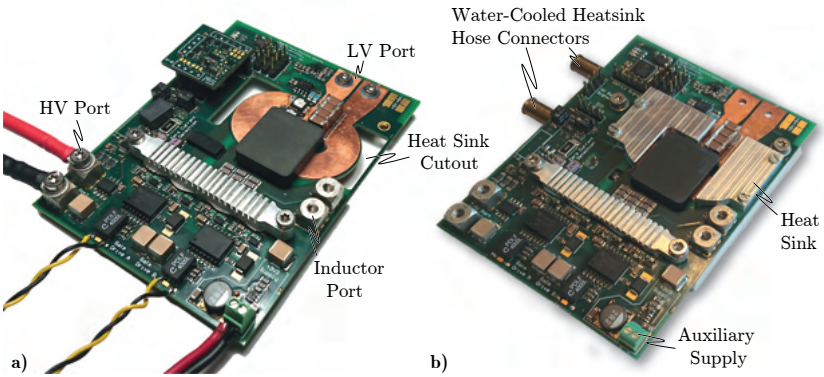


Fig. 4.15: a) Hardware demonstrator of the 3 kW two-port series-resonant converter without the heat sink and without the PCB-winding inductor and **b)** the same converter with the assembled water-cooled aluminum heat sink.

4.4.1 Experimentally Measured Waveforms

The hardware demonstrator has been tested under all different kinds of operating conditions, as, e.g. DCM operation for high input voltages V_{HV} and low output power values P_{LV} and boundary conduction mode (BCM) operation for large output power values, where the converter is operated at the boundary between DCM and CCM. In Fig. 4.16, the experimentally measured transformer current $i_{\mathrm{T,HV}}$, as well as the gate voltages $v_{\mathrm{g,SR1}}$ and $v_{\mathrm{g,SR2}}$ of the synchronous rectifier switches are shown for both operating modes and an output power P_{LV} of 500 W. Thus, in the first graph, a high input voltage V_{HV} results in DCM operation of the converter, as a comparably small output current is required and at the same time the large voltage difference between the input voltage V_{HV} and the primary side referred output voltage V'_{LV} yields steep current gradients within the inductor. In contrast, in Fig. 4.16b, a low input voltage was used, in order to transfer the required output power with BCM operation, hence, with a continuous transformer current $i_{\mathrm{T,HV}}$.
It can be seen, that the synchronous rectification works quite well, but only due to a change of the initially planned resistive measurement circuit, using a shunt resistor in the current path of the HV side, to an inductive measurement technique, using a zero-current-detection (ZCD) transformer [42]. This change in strategy was necessary, as the measured voltage signal across the shunt resistor was prone to disturbances due to both, ground currents originating form the capacitive coupling within the PCB-winding transformer,

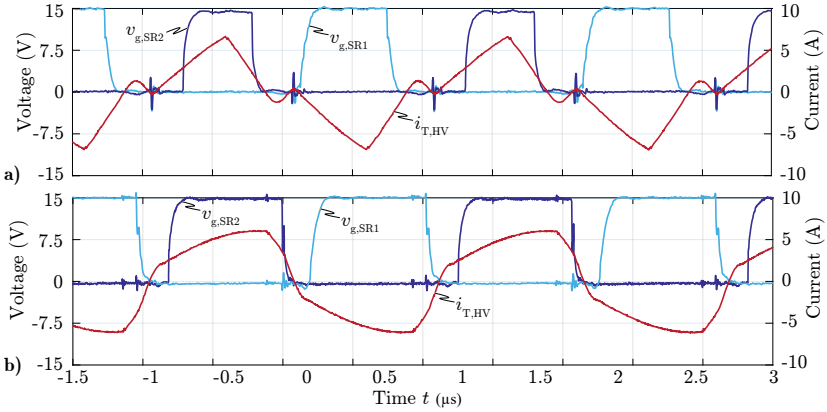


Fig. 4.16: HV-side transformer current $i_{T,HV}$ and the corresponding gate signals of the synchronous rectifiers SR1 and SR2 for **a)** DCM and **b)** CCM operation, an output voltage V_{LV} of 15 V, and an output power P_{LV} of 500 W.

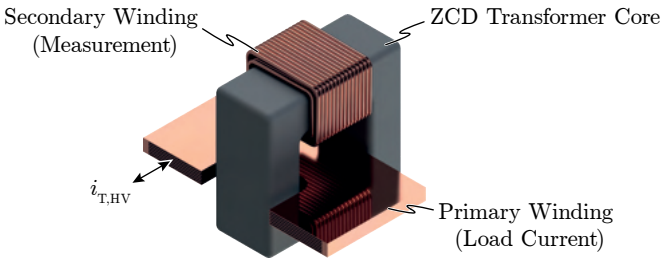


Fig. 4.17: 3D model of the employed zero-current-detection transformer, which allows for a galvanically isolated measurement of the transformer current.

as well as the large $\mathrm{d}v/\mathrm{d}t$ of the switch-node voltages on the HV side of the converter. The use of a ZCD transformer mitigated this issue, as its galvanic isolation yields a much better signal-to-noise (SNR) ratio. Thus, the current in the transformer $i_{\mathrm{T,HV}}$ is fed through a square-shaped ferrite core without air gap, around which a second winding with around 50 turns is wound as well. This second winding is directly connected to a shunt resistor, which can now have a much higher resistance compared to the initial solution, as the current flowing through the shunt is 50 times lower than before. Accordingly, for the same amount of losses (assuming an ideal transformer), the ratio between the shunt voltage v_{m} and the transformer current $i_{\mathrm{T,HV}}$ is 50 times larger than without a ZCD transformer, whereby a beneficial SNR results. Furthermore, the inherent isolation between the measurement circuit and the transformer current $i_{\mathrm{T,HV}}$ minimizes the impact of the large $\mathrm{d}v/\mathrm{d}t$ of the switch-node voltages on the measurement signal v_{m}. This measurement signal v_{m} is then compared to reference voltages v_{ref}, which can be adapted in order to choose the current value, which is considered as "zero current", arbitrarily. As the two reference voltages for the two half cycles are set independently by means of two potentiometers, these values can be slightly different (as can be seen in Fig. 4.16a). However, in practice, they should be as close as possible in order to avoid unbalanced operating conditions.

4.4.2 Experimentally Measured Efficiency

Using the aforementioned ZCD measurement circuitry, the efficiency of the hardware demonstrator has finally been measured for various operating points and three different input voltages V_{HV} (cf. Fig. 4.18). Thus, as required, the converter achieves an efficiency of $\approx 95\,\%$ for $P_{\mathrm{LV}} = 30\,\%...50\,\%$ of P_{max} at $V_{\mathrm{HV}} = 500\,\mathrm{V}$, but also over almost the complete input voltage range. However, as soon as the converter cannot be operated in BCM anymore, the efficiency drops significantly. Nevertheless, as the converter was designed in such a way, that BCM is guaranteed in the output power range, where a high efficiency is required, this is not an issue and was expected beforehand.

The main challenge in the converter design at hand was the thermal attachment of the LV-side semiconductors, as their tight thermal connection to the top part of the aluminum heat sink could hardly be achieved, mainly due to the unevenness of the top surfaces of the two power switches in combination with a lack of mechanical pressure between the heat sink and

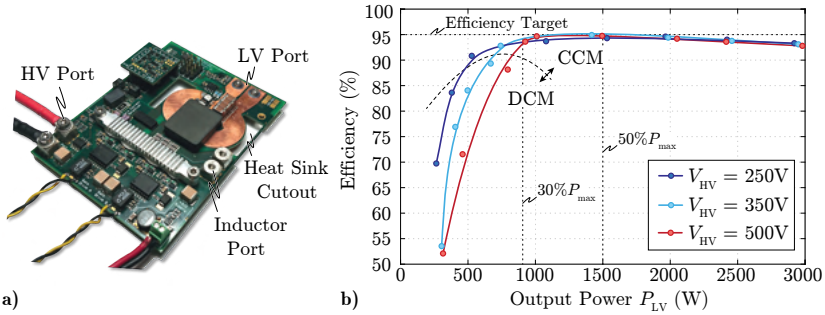


Fig. 4.18: a) 3 kW hardware demonstrator and **b)** corresponding efficiency measurements for different input voltages V_{HV} and an output voltage V_{LV} of 15 V.

the switches. Consequently, these switches have been replaced multiple times during the efficiency measurements, as for large output currents, the switches got too hot and failed. Thus, in a redesign, an improved cooling concept of the top side LV semiconductors would be required.
The gained experiences due to the main difficulties in the design of this converter, namely, the efficient design of the current track of the LV port, as well as a proper thermal attachment of the switches to the heat sink, have been used for the design of the more complex three-port resonant converter, which will be introduced in the following chapter.

4.5 Summary of the Chapter

In this chapter, the suitability of the series-resonant converter topology for applications with extremely large output currents and widely varying port voltages has been investigated. Especially the performance of the LV-side synchronous rectifier has been of interest, as it has been considered to be the most efficient and most reasonable converter port topology for such specifications.
In order to be able to find the most suitable converter design, various loss models of the different power components have been derived and were used in a multi-objective optimization, which was conducted with respect to power density and efficiency of the converter.
Based on the results of the aforementioned optimization, the most power-dense converter, which still meets the given efficiency requirements, has finally been implemented in hardware. To keep a certain flexibility regarding

the design of the series-resonant inductor, a modular approach has been chosen, such that different implementations of this inductor can be tested (PCB-winding inductors and conventional wire-wound inductors).

It has been found, that the loss models of the switches and the inductor can be used to accurately predict the occurring losses in these components, which is why these loss models will also be used for the three-port DC/DC converters of Chapter 5 and Chapter 6. However, the very high currents in the LV port yield higher losses than expected, as the conduction losses in the PCB-winding and the LV semiconductors react extremely sensitive to non-idealities in the manufacturing of the hardware. Hence, an imperfect solder joint or slightly increased thermal resistances of the thermal paths significantly increase the occurring losses, which, accordingly, are extremely difficult to simulate accurately beforehand. The major challenge in the hardware design of a high-current low-voltage application is therefore an accurate prediction of the losses in consideration of the non-idealities in a real system. Hence, for the design of the three-port converter systems, it should be kept in mind, that the LV-side conduction losses are most probably higher than the calculated ideal values.

Nevertheless, the efficiency target was just reached and a very high power density of 17.9 kW/L was achieved. Thus, the suitability of the winding-integrated center-tapped synchronous rectifier has been proven, which is why it will also be used in the three-port converter system, if possible. In addition, it has also been found, that a wide port voltage range demands for a large series-resonant inductance, such that a sufficiently high efficiency for a wide output power range and wide port voltage variations can be achieved. However, this inherently reduces the power density of the converter, which is why concepts should be developed, which somehow can mitigate this issue and allow for utilizing smaller inductors.
This will be done in the following chapter by means of a new three-port DC/DC converter topology.

5

Three-Port Series-Resonant DC/DC Converter Employing Additive and Subtractive Superposition of Flux Linkages

Chapter Abstract

In previous chapters of this thesis, it has been found, that a resonant power transfer, and especially a synchronous rectification of the large currents in the LV port, are the most promising and efficient topological solutions for the application at hand. Furthermore, an as simple as possible control of the three-port converter is desirable, which means that the output ports of the three-port converter should be perfectly decoupled, such that the converter can be controlled as two independent sub-converter systems. In this chapter, such a topology is developed, which is based on a special transformer structure where additive and subtractive superposition of magnetic flux linkages is used to achieve the aforementioned decoupling of the converter ports. Furthermore, a new concept of operating mode dependent turns ratios is proposed, which allows to optimize the turns ratio of the transformer for both operating modes (drive mode and charge mode) individually. After deriving a suitable control strategy based on simplified equivalent circuits, a 1 kW 166 V/166 V/15 V hardware demonstrator is built in order to verify the suitability and the achievable performance of the proposed converter topology.

In the previous chapters, it has been shown, that the power transfer to the low-voltage (LV) battery is most efficient, if a synchronous rectifier in the LV port is used, which simply rectifies the sinusoidally shaped LV winding currents. Thus, the LV semiconductors are inherently operated under zero-

voltage-switching (ZVS) and zero-current-switching (ZCS) conditions, which is the most efficient operation for power semiconductors (from a switching loss perspective). Consequently, it makes sense to try to use the same efficient and simple circuit in the high-voltage (HV) port as well, such that both, the HV and the LV port are operated as synchronous rectifiers.
However, as a synchronous rectifier has no impact on the amount of power which is transferred to its respective converter port, the control of the power flow from the PFC to the HV and the LV port in charge mode (CM) needs to be taken over by the PFC port alone, which cannot be achieved by means of just a single PFC winding. Consequently, a more sophisticated transformer structure is in demand, which allows to generate arbitrary HV- and LV winding currents, which are controlled by the PFC winding currents alone. Hence, at least two independent PFC-side currents are necessary to control the aforementioned output currents, which in turn requires at least two independent PFC-side windings.
In the following, the general idea of the converter operation is introduced and an appropriate transformer structure is derived, which complies with the aforementioned requirements and can finally be used in a three-port DC/DC converter topology.

5.1 General Idea of the Converter Operation

The fundamental idea of the power flow control in this converter topology is, to generate two sinusoidal currents i_1 and i_2 with equal amplitudes $\hat{i}$, but phase-shifted by a certain angle $\varphi \in \{0°...180°\}$ (cf. Fig. 5.1a). By additive and subtractive superposition of these two currents, two new currents i_+ and i_- are generated (cf. Fig. 5.1b), with the same frequency as the original currents, but with an amplitude ratio, which can be controlled by means of φ, according to

$$\begin{aligned} i_+ = i_1 + i_2 &= \hat{i}\sin(\omega t) + \hat{i}\sin(\omega t + \varphi) \\ &= 2\hat{i}\cos\left(\frac{\varphi}{2}\right) \cdot \sin\left(\omega t + \frac{\varphi}{2}\right) \end{aligned} \tag{5.1}$$

and

$$\begin{aligned} i_- = i_1 - i_2 &= \hat{i}\sin(\omega t) - \hat{i}\sin(\omega t + \varphi) \\ &= 2\hat{i}\sin\left(-\frac{\varphi}{2}\right) \cdot \cos\left(\omega t + \frac{\varphi}{2}\right). \end{aligned} \tag{5.2}$$

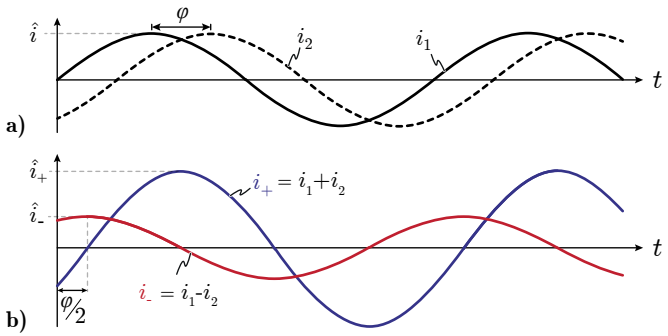


Fig. 5.1: a) Ideally sinusoidal currents i_1 and i_2 with the same amplitude $\hat{i}$, but phase-shifted by a certain angle φ. **b)** Resulting currents for additive (i_+) and subtractive (i_-) superposition of the two currents i_1 and i_2.

Hence, the ratio $\hat{i}_+/\hat{i}_-$ between the two output currents is given as

$$\frac{\hat{i}_+}{\hat{i}_-} = \cot\left(\frac{\varphi}{2}\right). \tag{5.3}$$

Consequently, the amplitudes of the two output currents i_+ and i_- can be controlled independently by varying $\hat{i}$ and φ.
In the application at hand, i_1 and i_2 correspond to two PFC-side winding currents i_{PFC1} and i_{PFC2}, whereas i_+ and i_- correspond to the winding currents in the HV and the LV ports, respectively. The mathematical addition and subtraction of i_1 and i_2 can be achieved by means of an appropriate transformer structure, where i_1 and i_2 are impressed in two individual windings, which are arranged around the outer legs of a conventional E-core (cf. PFC1 and PFC2 in Fig. 5.2a). Consequently, these currents induce the corresponding flux linkages $\psi_1 = n_{\mathrm{PFC}} i_{\mathrm{PFC1}}$ and $\psi_2 = n_{\mathrm{PFC}} i_{\mathrm{PFC2}}$ in the two outer core legs. In order to extract the sum of the two currents for the HV port, an additional winding is required, which encircles the sum of both aforementioned flux linkages. For this reason, the HV winding is split into two identical series-connected windings, where each sub-winding encircles one of the flux linkages (cf. HV1 and HV2 in Fig. 5.2a). Finally, the LV winding is wrapped around the center leg of the transformer, as in this section of the core, only the difference between the two flux linkages appears (cf. LV in Fig. 5.2a).
The simplified reluctance model of this transformer structure is shown in Fig. 5.2b, where an infinite permeability μ_{r} of the core material is assumed.

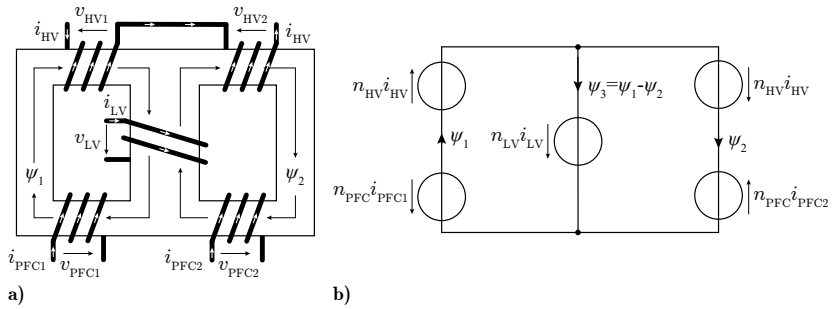


Fig. 5.2: a) Transformer structure of the proposed converter topology and **b)** the corresponding simplified reluctance model, where an infinite permeability μ_r of the core material is assumed.

Based on this reluctance model, the following set of equations can be derived:

$$i_{PFC1} + i_{PFC2} = 2\left(\frac{n_{HV}}{n_{PFC}}\right) i_{HV}, \tag{5.4}$$

$$i_{PFC1} - i_{PFC2} = 2\left(\frac{n_{LV}}{n_{PFC}}\right) i_{LV}, \tag{5.5}$$

$$v_{PFC1} + v_{PFC2} = \left(\frac{n_{PFC}}{n_{HV}}\right)(v_{HV1} + v_{HV2}), \tag{5.6}$$

$$v_{PFC1} - v_{PFC2} = \left(\frac{n_{PFC}}{n_{LV}}\right) v_{LV}. \tag{5.7}$$

As desired, the HV-side winding current is proportional to the sum of the two PFC-side currents, whereas the LV-side winding current depends on the difference of the two aforementioned currents only. However, considering the generation of the sinusoidal currents i_{PFC1} and i_{PFC2}, the two equations (5.6) and (5.7) introduce a challenging behavior of this transformer structure, as will be discussed in the following.

As the HV- and LV-side winding currents are synchronously rectified through respective semiconductors devices, the port voltages V_{HV} and V_{LV} are directly applied to the respective transformer windings and, therefore, inherently define the PFC-side winding voltages v_{PFC1} and v_{PFC2}, according to the aforementioned equations. Hence, depending on the sign of the currents $i_X, X \in \{HV, LV\}$, either the positive or the negative port voltage V_X is applied

to the respective transformer winding. However, due to the phase shift φ between i_{PFC1} and i_{PFC2}, there is a constant phase shift of $\pi/2$ between i_{HV} and i_{LV} and, therefore, between v_{HV} and v_{LV} as well.
Consequently, based on (5.6) and (5.7), the PFC-side voltages can be calculated according to

$$v_{\mathrm{PFC1}} = \frac{n_{\mathrm{PFC}}}{2n_{\mathrm{HV}}n_{\mathrm{LV}}} \left(n_{\mathrm{LV}}V_{\mathrm{HV}} + n_{\mathrm{HV}}V_{\mathrm{LV}}\right) \tag{5.8}$$

and

$$v_{\mathrm{PFC2}} = \frac{n_{\mathrm{PFC}}}{2n_{\mathrm{HV}}n_{\mathrm{LV}}} \left(n_{\mathrm{LV}}V_{\mathrm{HV}} - n_{\mathrm{HV}}V_{\mathrm{LV}}\right). \tag{5.9}$$

These voltages are shown in Fig. 5.3 for an exemplary phase shift φ of $\pi/3$ and operating conditions as listed in the caption of the figure. During the first half-period ($0 \leq t \leq \pi$) of i_{PFC1}, the corresponding winding voltage v_{PFC1} changes its level twice (from 865 V $\rightarrow$ −78 V and from −78 V $\rightarrow$ −865 V), according to

$$v_{\mathrm{PFC1}}(i_{\mathrm{HV}} > 0, i_{\mathrm{LV}} < 0) = \frac{n_{\mathrm{PFC}}}{2n_{\mathrm{HV}}n_{\mathrm{LV}}} \left(n_{\mathrm{LV}} \cdot 400\,\mathrm{V} + n_{\mathrm{HV}} \cdot 14.5\,\mathrm{V}\right) = 865\,\mathrm{V} \tag{5.10}$$

and

$$v_{\mathrm{PFC1}}(i_{\mathrm{HV}} > 0, i_{\mathrm{LV}} > 0) = \frac{n_{\mathrm{PFC}}}{2n_{\mathrm{HV}}n_{\mathrm{LV}}} \left(n_{\mathrm{LV}} \cdot 400\,\mathrm{V} + n_{\mathrm{HV}} \cdot (-14.5\,\mathrm{V})\right) = -78\,\mathrm{V}, \tag{5.11}$$

which makes it extremely difficult to generate the required sinusoidal current i_{PFC1} with a reasonable hardware effort, as will be shown in the following.

The easiest way to generate a sinusoidal current is a series-resonant tank, comprising a series-connected inductor L_{r} and capacitor C_{r}, which is excited by means of a perfectly rectangular voltage v_{LC}. However, due to the various voltage steps in the winding voltages $v_{\mathrm{X}}, \mathrm{X} \in \{\mathrm{PFC1}, \mathrm{PFC2}\}$ during one resonant period, the required perfectly rectangular exciting voltage v_{LC} can hardly be generated. The simplest method to still be able to generate the sinusoidal currents i_{X}, despite the aforementioned voltage steps, is to minimize the impact of the winding voltage v_{X} on the resonant tank. Hence, the larger the $L_{\mathrm{r}}/C_{\mathrm{r}}$-ratio is, the higher the resonant capacitor voltage gets, whereby the winding voltage v_{X} has less impact on the resonant current in L_{r}. However, a large $L_{\mathrm{r}}/C_{\mathrm{r}}$-ratio results in a large volume of the required inductor L_{r} and, moreover, the resonant capacitor voltage is huge, as the voltage step in v_{X} of almost 1 kV should only have a minor impact on the current change in L_{r}. For this reason, an alternative operation of this transformer structure should

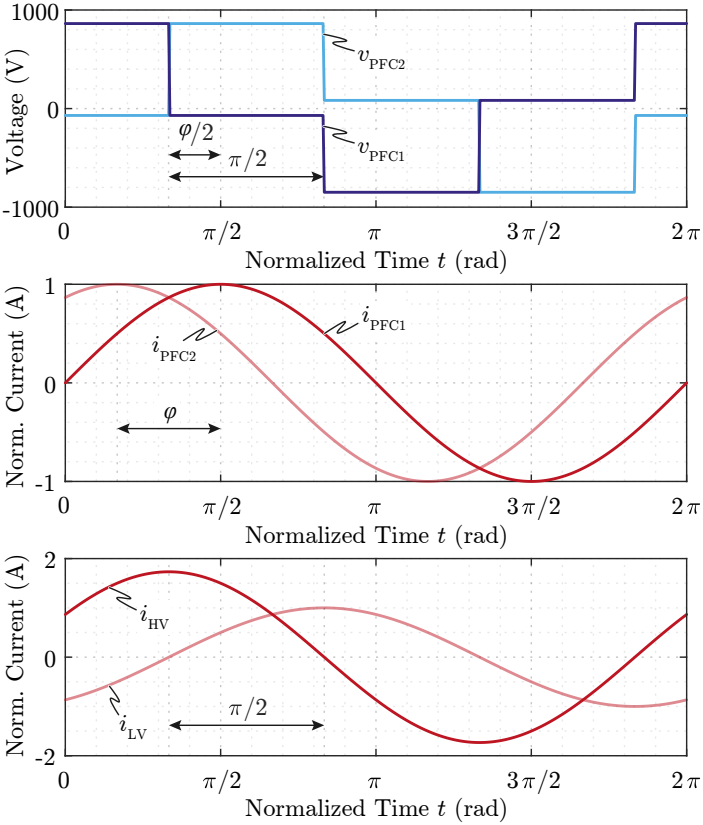


Fig. 5.3: Voltage and current waveforms in the proposed transformer structure for two phase-shifted impressed sinusoidal currents i_{PFC1} and i_{PFC2}, port voltages of $V_{HV} = 400\,V$ and $V_{LV} = 14.5\,V$ and numbers of turns of $n_{PFC} = 65, n_{HV} = 33$ and $n_{LV} = 1$.

be targeted, where the benefits of the proposed transformer structure can be kept and at the same time the voltage steps can be used in a beneficial way. This is achieved by loosening the constraint of purely sinusoidal currents i_X and by investigating the discontinuous conduction mode (DCM) operation of the transformer currents, which will be done in the following sections for both, CM and DM operation.

5.2 Converter Topology in Charge Mode Operation

In the previous section, the required currents in the transformer in CM have been discussed. However, the actual generation of these currents has not yet been investigated in detail, which is why this is done in the following.
As already mentioned, the simplest way to generate partially sinusoidally shaped currents is a *LC* series-resonant tank, which is excited by rectangular voltages. Consequently, for each PFC-side winding, a separate resonant tank is required, in order to be able to generate different currents in the respective windings (cf. Fig. 5.4). Furthermore, both resonant-tank/PFC winding combinations need to be excited with different rectangular voltages, which can either be generated by means of a full-bridge for each sub-circuit, or, for the sake of cost reduction, with three half-bridges as shown in Fig. 5.4a, where one half-bridge (HB_B) is shared by the two resonant tanks. Theoretically, the number of switches could be further reduced to a total of four switches, if the resonant capacitors would be split into capacitive voltage dividers, as shown in Fig. 5.4b. However, by doing so, there would be no possibility to use zero-voltage time-intervals in v_{A1} and v_{A2}, which is essential, if DCM of i_{PFC1} and i_{PFC2} should be used (which is inevitable for low output power values). Consequently, the circuit of Fig. 5.4a is chosen as most appropriate solution for this application. It needs to be mentioned, that for the sake of clarity, the synchronous rectifiers of the HV and the LV port are not shown in this figure, but are of course required for the converter operation.
In the following, the control of the PFC-side resonant circuits is discussed in detail, such that the achievable performance of this topology in a possible hardware implementation can be explored.

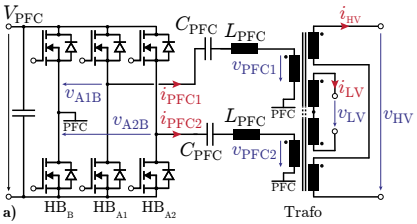


Fig. 5.4: a) Simplified circuit of the proposed topology during CM operation, where the HV- and the LV-side synchronous rectifiers are not shown. Furthermore, the LV winding is drawn as two individual sub-windings in order to illustrate the subtraction of the flux linkages, even though in reality there is only a single LV winding, as shown in Fig. 5.2a.

5.2.1 Converter Control in Charge Mode Operation

In charge mode (CM) operation, most of the power flows from the PFC to the HV port and only a small fraction of the total power flows from the PFC to the LV port. Hence, equivalent circuits for both power paths (PFC→HV and PFC→LV) should be derived, in order to simplify the analysis of the converter operation. Starting with the main power path from the PFC to the HV port, the rather complex circuit of Fig. 5.4a can be simplified in a four-step approach, as shown in Fig. 5.5a-e. Thus, the three half-bridges of the PFC port can be replaced by the two ideal rectangular voltage sources v_{A1B} and v_{A2B}, while the two PFC-side transformer windings are replaced by equivalent voltage sources v_{PFC1} and v_{PFC2}. In a second step, the lower sub-circuit can be rotated by 180° and the reference potentials ($\overline{PFC}$) can be electrically connected. According to (5.4), only the common mode component of i_{PFC1} and i_{PFC2} is mapped to the HV port, which is why the dashed connections in Fig. 5.5b can be neglected, if only PFC→HV power flow is considered. Consequently, the common mode equivalent circuit of Fig. 5.5c can be derived, which is then further simplified based on (5.6) to the well-known equivalent circuit of a

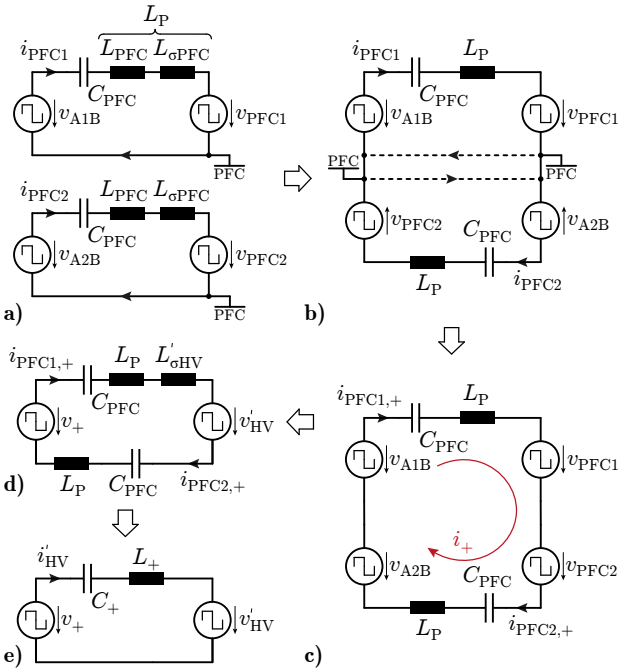


Fig. 5.5: Derivation of the simplified equivalent circuit for the power flow from the PFC to the HV port during charge mode (CM) operation.

series-resonant converter as shown in Fig. 5.5e, with

$$v_+ = v_{A1B} + v_{A2B} \tag{5.12}$$

$$C_+ = \frac{C_{PFC}}{2} \tag{5.13}$$

$$L_+ = 2L_{PFC} + 2L_{\sigma PFC} + 2L_{\sigma HV}\left(\frac{n_{PFC}}{n_{HV}}\right)^2 \tag{5.14}$$

$$v'_{HV} = \frac{n_{PFC}}{n_{HV}} v_{HV}, \tag{5.15}$$

where $L_{\sigma X}$ denote the leakage inductance values of the respective transformer windings.

The equivalent circuit for the power flow from the PFC to the LV port can now be derived in a similar way, as shown in Fig. 5.6a-e. Hence, in

contrast to the derivation of the equivalent circuit for the PFC→HV power flow, where the lower sub-circuit was rotated by 180°, the lower sub-circuit is now vertically flipped, such that only the differential mode component of the two currents i_{PFC1} and i_{PFC2} is circulating through the resonant tanks. Thus, the dashed lines can again be neglected and the equivalent circuit can be simplified by means of (5.7). The different components of the series-resonant converter equivalent circuit of Fig. 5.6e are then given by

$$v_{-} = v_{\mathrm{A1B}} - v_{\mathrm{A2B}} \tag{5.16}$$

$$C_{-} = \frac{C_{\mathrm{PFC}}}{2} \tag{5.17}$$

$$L_{-} = 2L_{\mathrm{PFC}} + 2L_{\sigma\mathrm{PFC}} + 2L_{\sigma\mathrm{LV}} \left(\frac{n_{\mathrm{PFC}}}{n_{\mathrm{LV}}} \right)^2 \tag{5.18}$$

$$v'_{\mathrm{LV}} = \frac{n_{\mathrm{PFC}}}{n_{\mathrm{LV}}} v_{\mathrm{LV}}. \tag{5.19}$$

As the PFC→HV and the PFC→LV series-resonant circuits are both excited by means of either v_{+} or v_{-}, the shapes of these two voltages needs to be known in order to develop a reasonable control strategy for this converter topology. According to the previously derived equations (5.12) and (5.16), the two voltages depend on v_{A1B} and v_{A2B} and, therefore, the switch-node voltages of the three half-bridges $\mathrm{HB_B}$, $\mathrm{HB_{A1}}$ and $\mathrm{HB_{A2}}$ as well. Due to symmetry reasons, these half-bridges should all be operated with the same switching frequency f_{sw} and a duty cycle of 50 %. However, the phase shifts t_{+} and t_{-} between them can be selected arbitrarily, resulting in the three degrees of freedom (DOF): switching frequency f_{sw}, duty cycle D_{+} and duty cycle D_{-} (cf. Fig. 5.7). As illustrated in the figure, the exciting voltage for the PFC→HV power flow is a five-level voltage according to $v_{+} \in \{-2V_{\mathrm{PFC}}, -V_{\mathrm{PFC}}, 0, V_{\mathrm{PFC}}, 2V_{\mathrm{PFC}}\}$, whereas the exciting voltage for the PFC→LV power flow is given by $v_{-} \in \{-V_{\mathrm{PFC}}, 0, V_{\mathrm{PFC}}\}$. Hence, while D_{-} specifies the length of the time intervals with $v(t) = \pm V_{\mathrm{PFC}}$ for both voltages, D_{+} defines the length of the time interval with $v_{+}(t) = \pm 2V_{\mathrm{PFC}}$ only, and has therefore no effect on v_{-}.

Based on these voltage waveforms and the derived equivalent circuits, the currents in the HV and the LV winding can be derived. However, for each power path, different conduction modes need to be distinguished, depending on whether a continuous (CCM) or discontinuous (DCM) winding current is achieved. Furthermore, for the PFC→HV power path, the discontinuous

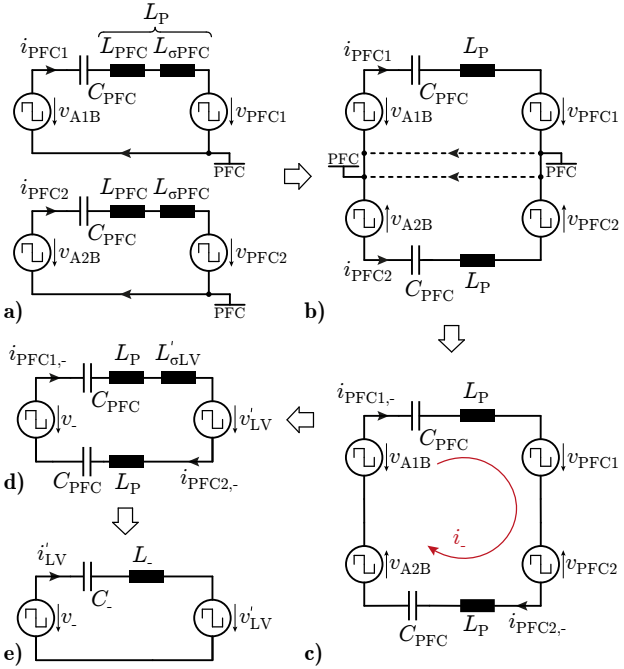


Fig. 5.6: Derivation of the simplified equivalent circuit for the power flow from the PFC to the LV port during charge mode (CM) operation.

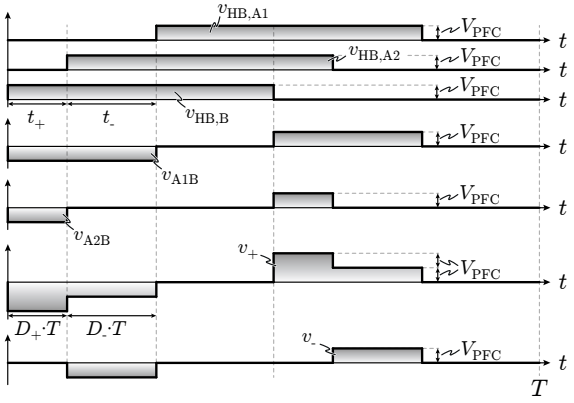


Fig. 5.7: Voltage waveforms in the PFC port and the respective control parameters during charge mode (CM) operation.

conduction mode is again divided into two different conduction modes (DCM1 and DCM2), which are differentiated by the momentary value of v_+ at the time where the HV winding current drops to zero. All these possible modes are summarized in Fig. 5.8 and will be discussed in the following in detail.

In the first plot, the DCM for the PFC→LV power flow is illustrated. In this mode, the applied voltage across the resonant tank v_{LC} of $v_- - V'_{\mathrm{LV}}$ yields a current rise during the active period ($0 \leq t \leq D_- \cdot T$), before the current drops back to zero during the inactive period ($D_- \cdot T \leq t \leq T/2$), where $v_{\mathrm{LC}} = -V'_{\mathrm{LV}}$. Consequently, the transferred power from the PFC to the LV port can be calculated according to

$$P_{\mathrm{LV}} = \frac{4C_- V'_{\mathrm{LV}} V_{\mathrm{PFC}} (V_{\mathrm{PFC}} - V'_{\mathrm{LV}}) \cdot \left(1 - \cos\left(\frac{D_- T}{\sqrt{L_- C_-}}\right)\right)}{T \cdot \left(\cos\left(\frac{D_- T}{\sqrt{L_- C_-}}\right) V_{\mathrm{PFC}} - V_{\mathrm{PFC}} + 2V'_{\mathrm{LV}}\right)}. \tag{5.20}$$

As neither the HV port voltage V_{HV}, nor the respective HV output power P_{HV} appears in (5.20), a perfectly decoupled power flow control is achieved, whereby the LV port is controlled by means of D_-, independent of the momentary V_{HV} and P_{HV}.
In Fig. 5.8b, the waveforms of the CCM for the PFC→LV power flow is illustrated. Thus, in contrast to the DCM, the inactive period is too short for the current i_{LV} to drop to zero, which is why the zero-current-crossing (ZCC) is

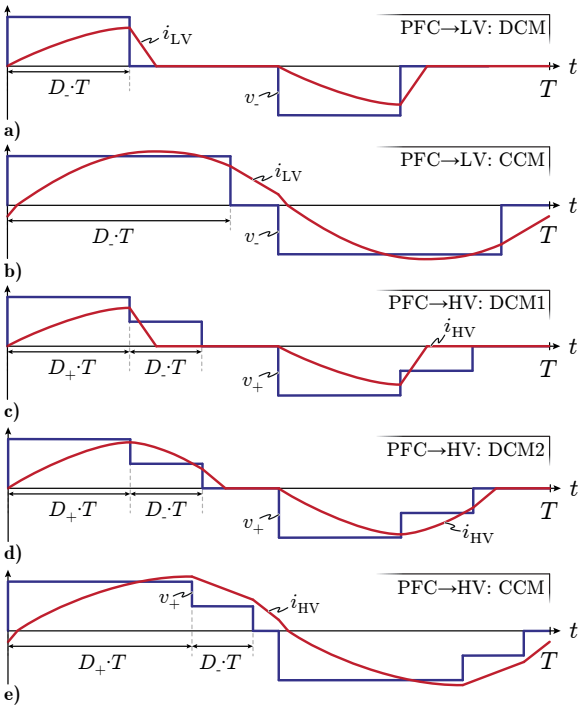


Fig. 5.8: Voltage and current waveforms for all different kinds of operating modes and for both power paths PFC→HV and PFC→LV.

shifted into the subsequent active period ($T/2 \leq t$). For this operating mode, a closed form solution of the output power in dependence of the duty cycle D_- can hardly be found, which is however not of importance, as this mode is never used during operation. Even though in DCM, the peak-to-average ratio of i_{LV} is higher compared to CCM, this is not really a drawback, as the LV output power in CM operation is comparably small. For larger P_{LV}, the active period is inherently extended, whereby the converter is operated close to the boundary between DCM and CCM, and the peak-to-average current ratio approaches the ideal ratio as in CCM operation.

In Fig. 5.8c, the first DCM for a power flow from the PFC to the HV port is shown. The waveforms look very similar to the ones discussed for the DCM in the LV port, but with the difference that the voltage across the resonant tank v_{LC} during the first active period ($0 \leq t \leq D_+ \cdot T$) is $2V_{\mathrm{PFC}} - V'_{\mathrm{HV}}$ and during the second active period ($D_- \cdot T \leq t \leq (D_+ + D_-) \cdot T$), where the current drops to zero, is $V_{\mathrm{PFC}} - V'_{\mathrm{HV}}$. The power flow can therefore be calculated according to

$$P_{\mathrm{HV}} = \frac{4C_+ V_{\mathrm{PFC}} V'_{\mathrm{HV}} (2V_{\mathrm{PFC}} - V'_{\mathrm{HV}}) \left(1 - \cos\left(\frac{D_+ T}{\sqrt{L_+ C_+}}\right)\right)}{T \left(\cos\left(\frac{D_+ T}{\sqrt{L_+ C_+}}\right) V_{\mathrm{PFC}} - 3V_{\mathrm{PFC}} + 2V'_{\mathrm{HV}}\right)}. \tag{5.21}$$

Again, neither V_{LV} nor D_- appear in (5.21), whereby a perfectly decoupled control of the two output power values P_{HV} and P_{LV} is achieved.
However, for low LV output power values and, therefore, small D_-, the time interval $D_- \cdot T$ might not be long enough for the current i_{HV} to drop to zero, whereby the ZCC is shifted into the subsequent zero-voltage time interval (DCM2), as shown in Fig. 5.8d. Consequently, the length of $D_- \cdot T$ now also has an impact on the HV power flow according to

$$P_{\mathrm{HV}} = \frac{4C_+ V_{\mathrm{i}} V_{\mathrm{o}}}{T} \cdot \beta, \tag{5.22}$$

where

$$\beta = \frac{2V_{\mathrm{o}} - 3V_{\mathrm{i}} + (2V_{\mathrm{i}} - V_{\mathrm{o}})(\alpha_{\mathrm{D}+} + \alpha_{\mathrm{D}\pm}) - V_{\mathrm{i}} \alpha_{\mathrm{D}-}}{2V_{\mathrm{i}} - 2V_{\mathrm{o}} - V_{\mathrm{i}}(\alpha_{\mathrm{D}+} + \alpha_{\mathrm{D}\pm})}, \tag{5.23}$$

with $V_\mathrm{i} = V_\mathrm{PFC}$, $V_\mathrm{o} = V'_\mathrm{HV}$ and

$$\begin{aligned} \alpha_{\mathrm{D}+} &= \cos\left(\frac{D_+ T}{\sqrt{L_+ C_+}}\right) \\ \alpha_{\mathrm{D}-} &= \cos\left(\frac{D_- T}{\sqrt{L_+ C_+}}\right) \\ \alpha_{\mathrm{D}\pm} &= \cos\left(\frac{(D_+ + D_-)T}{\sqrt{L_+ C_+}}\right). \end{aligned} \tag{5.24}$$

Thus, in DCM2, the controller needs to calculate in a first step D_-, based on the momentary port voltage V_LV and the output power requirement for P_LV, before this duty cycle is used to calculate the second duty cycle D_+ according to the previously derived equations. The benefit of the decoupled power flow of the LV port now becomes obvious, as it would otherwise not be possible to control the two output ports independently, by means of the two control parameters (D_+ and D_-).
Similar to the CCM of the LV port, the CCM of the HV port is not used in this application, as a closed form solution of the power flow in dependency of the control variables can hardly be found. Furthermore, this mode is not really required, as for large HV output power values, where the HV-side transformer current would enter CCM, the switching frequency can be lowered such that the HV port is operated at the boundary between DCM and CCM. Consequently, (5.21) and (5.22) are still valid and, in addition, a continuous current in the HV port is achieved, whereby the peak-to-average current ratio of i_HV is reduced and the conduction losses are minimized. However, varying the switching frequency affects the power flow in both output ports of the converter, which is why this parameter should not be used as a primary control parameter for the output power. Nevertheless, as both, the HV and the LV port are connected to batteries, their port voltages are changing only slowly, which is why the switching frequency can be adapted according to the momentary port voltages in order to optimize the operating conditions for the converter in terms of conduction and switching losses.

Based on the aforementioned five conduction modes, the switching conditions for each employed power semiconductor can be derived. Obviously, due to the synchronous rectification of the winding currents in the HV and the LV port, these semiconductors are inherently operated under ZVS conditions. However, the three half-bridges in the PFC port are actively switched, whereby the currents in the switch-nodes of these half-bridges during the

switching transitions need to be investigated. Based on (5.4) and (5.5), the currents in the three switch-nodes can be calculated according to

$$i_{\mathrm{PFC,A1}} = i'_{\mathrm{HV}} + i'_{\mathrm{LV}} \tag{5.25}$$

$$i_{\mathrm{PFC,A2}} = i'_{\mathrm{HV}} - i'_{\mathrm{LV}} \tag{5.26}$$

$$i_{\mathrm{PFC,B}} = 2 \cdot i'_{\mathrm{HV}}. \tag{5.27}$$

These three currents and the corresponding switch-node voltages $v_{\mathrm{HB,A1}}$, $v_{\mathrm{HB,A2}}$ and $v_{\mathrm{HB,B}}$ are shown in Fig. 5.9 for an exemplary power flow from the PFC to the HV and from the PFC to the LV port. As shown in the figure, the half-bridge $\mathrm{HB_{A1}}$ is always switched at the peak of the LV winding current i'_{LV}, whereas the half-bridge $\mathrm{HB_{A2}}$ is switched at the peak of the HV winding current i'_{HV}. Thus, both half-bridges are inherently operated under ZVS conditions, as long as the output power in both ports is larger than zero. The third half-bridge, however, is operated under ZCS conditions only, whereby the Q_{oss} of this half-bridge is dissipated during every switching transition. Consequently, semiconductors with minimal C_{oss} should be employed in this half-bridge. Nevertheless, at the boundary between DCM and CCM of i'_{HV}, thus, for large output power values, even this half-bridge can be operated under ZVS conditions. Alternatively, if an operating mode independent ZVS of this half-bridge is required, the magnetizing inductance of the transformer could be decreased in order to increase the magnetizing current in the PFC winding, which assists ZVS of $\mathrm{HB_B}$. However, the utilization of the magnetizing current is a tradeoff between switching losses and additional conduction losses and might not always be beneficial for the converter operation.

In summary, the proposed topology can be operated in CM with a decoupled power flow control of the HV and the LV port by means of the two duty cycles D_+ and D_-, whereby almost all semiconductors are inherently operated under ZVS conditions. Furthermore, the switching frequency can be adapted to the momentary port voltages, in order to optimize the operating conditions of the converter. In the following section, the drive mode (DM) operation of the converter is investigated in a similar way.

5.3 Converter Topology in Drive Mode Operation

In drive mode (DM) operation, the PFC-side half-bridges and the two resonant tanks are not operated actively, as there is no power flow from/to the PFC port

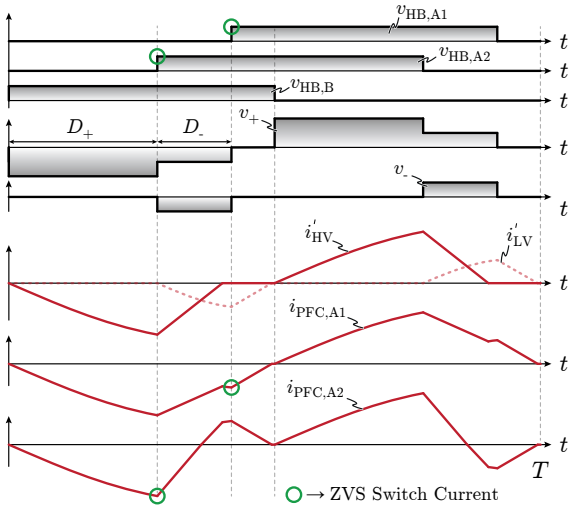


Fig. 5.9: Exemplary voltage and current waveforms in charge mode (CM) operation in order to illustrate the ZVS transitions of the PFC-side half-bridges.

anymore. Instead, power is flowing from the HV to the LV port, whereby the synchronous rectifier circuit of the HV port needs to be extended, such that again a series-resonant tank is in the current path. However, this resonant tank should not affect the CM operation, whereby one of its terminals is connected to the center tap of the HV windings and the second terminal is connected to an additional bridge-leg HB_3 (cf. Fig. 5.10a). Consequently, as HB_3 is only operated in DM, it does not affect the CM operation at all.
The main reason why the third bridge-leg is required is, that the two HV-side half-bridges HB_1 and HB_2 (which were used as synchronous rectifiers in CM) and the two series connected HV windings are not able to generate a magnetic flux $\psi_1 - \psi_2$ through the LV winding in the center leg of the transformer core (cf. Fig. 5.2a), as the symmetry of the arrangement forces the magnitudes of ψ_1 and ψ_2 to be the same. Consequently, either ψ_1 or ψ_2 needs to change its polarity, such that a voltage v_{LV} in the LV winding is induced. This is achieved by operating the two aforementioned half-bridges HB_1 and HB_2 synchronously and in phase, and the third half-bridge HB_3 with the same frequency but with a variable phase shift with respect to the other two half-bridges. Thus, the mid-point voltage of the series-connected HV windings can now actively be controlled, whereby the polarity of v_{HV2} is inverted and,

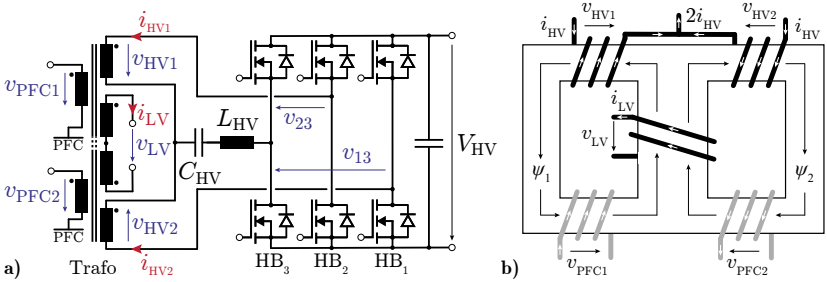


Fig. 5.10: a) Simplified circuit of the proposed topology during drive mode (DM) operation, where the PFC-side half-bridges and resonant tanks are neglected, as they are not used in DM. **b)** Equivalent transformer structure of the proposed topology during DM operation.

therefore, the polarity of ψ_2 as well (cf. Fig. 5.10b).

5.3.1 Converter Control in Drive Mode Operation

Based on the previous considerations, the DM equivalent circuit can now be derived in a similar way, as was previously done for the CM operation. Thus, as shown in Fig. 5.11a, the simplified topology of Fig. 5.10a can be replaced by the *LC* resonant tank and the four voltage sources, which represent the three half-bridges as well as the two HV winding voltages. Due to symmetry reasons, i_{HV1} is equal to i_{HV2} and the two sub-circuits can be separated as shown in Fig. 5.11b. Finally, v_{HVx} can be replaced by the equivalent LV winding voltage v'_{LV} and the respective leakage inductance $L'_{\sigma LV}$, yielding the well-known equivalent circuit for the series-resonant converter as shown in Fig. 5.11d,

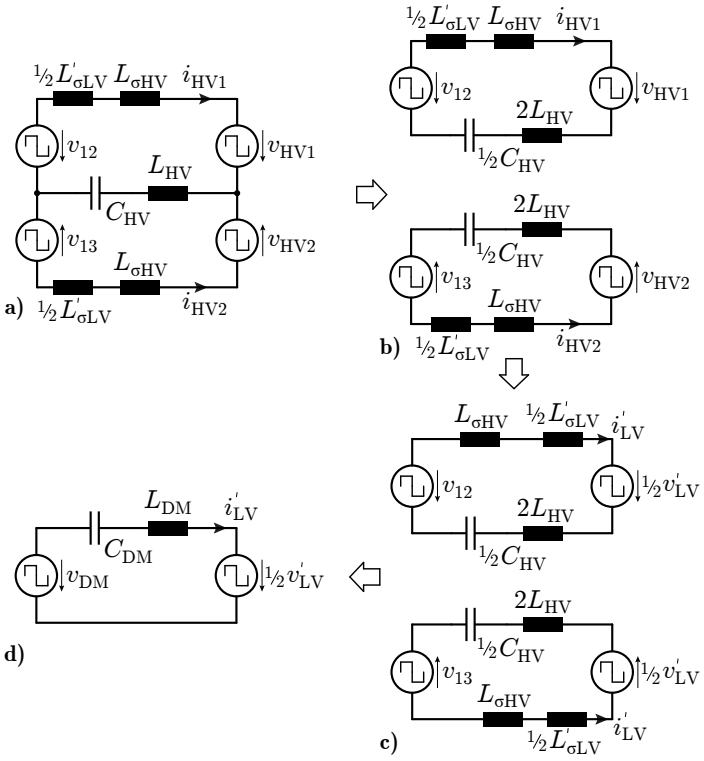


Fig. 5.11: Derivation of the simplified equivalent circuit for the power flow from the HV to the LV port during drive mode (DM) operation.

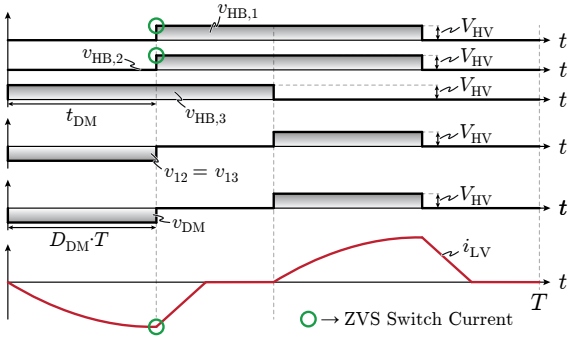


Fig. 5.12: Voltage waveforms in the HV and current waveform in the LV port and the respective control parameter D_{DM} during drive mode (DM) operation.

where

$$v_{DM} = v_{13} = v_{23} \tag{5.28}$$

$$C_{DM} = \frac{C_{HV}}{2} \tag{5.29}$$

$$L_{DM} = 2L_{HV} + L_{\sigma HV} + \left(\frac{n_{HV}}{n_{LV}}\right)^2 \cdot \frac{L_{\sigma LV}}{2} \tag{5.30}$$

$$v'_{LV} = \left(\frac{n_{HV}}{n_{LV}}\right) \cdot v_{LV} \tag{5.31}$$

$$i'_{LV} = \left(\frac{n_{LV}}{n_{HV}}\right) \cdot i_{LV}. \tag{5.32}$$

Thus, similar to the PFC→LV power flow, the resonant tank L_{DM}-C_{DM} is excited by a three-level voltage v_{DM} according to $v_{DM} \in \{-V_{HV}, 0, V_{HV}\}$. The corresponding voltage and current waveforms are illustrated in Fig. 5.12 for DCM of the LV winding current i_{LV}. Even though the converter could also be operated in CCM, this mode of operation is not used in this application for the same reasons as already mentioned in the previous section. Hence, either DCM or boundary conduction mode (BCM) is used in DM operation, where the switching frequency is adapted such that i_{LV} is kept at the boundary between DCM and CCM. Similarly to the PFC→LV power flow in CM, the power flow from the HV to the LV port is controlled by means of the duty cycle D_{DM} of v_{DM}. Consequently, the equation for the output power P_{LV} in

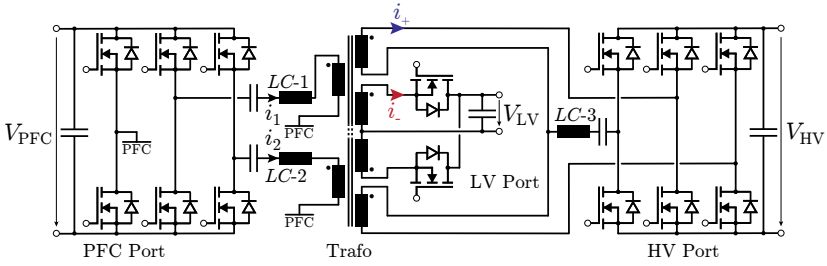


Fig. 5.13: Topology of the proposed three-port series-resonant DC/DC converter system.

dependency of D_{DM} is given by

$$P_{\mathrm{LV}} = \frac{4C_{\mathrm{DM}}V_{\mathrm{LV}}^{*}V_{\mathrm{HV}}(V_{\mathrm{HV}} - V_{\mathrm{LV}}^{*}) \cdot \left(1 - \cos\left(\frac{D_{\mathrm{DM}}T}{\sqrt{L_{\mathrm{DM}}C_{\mathrm{DM}}}}\right)\right)}{T \cdot \left(\cos\left(\frac{D_{\mathrm{DM}}T}{\sqrt{L_{\mathrm{DM}}C_{\mathrm{DM}}}}\right) V_{\mathrm{HV}} - V_{\mathrm{HV}} + 2V_{\mathrm{LV}}^{*}\right)}, \tag{5.33}$$

with $V_{\mathrm{LV}}^{*} = {}^{1}\!/_{2}V_{\mathrm{LV}}'$. As shown in Fig. 5.12, two out of the three half-bridges are inherently operated under ZVS conditions, whereby the remaining half-bridge is operated under ZCS conditions only. However, as mentioned in the previous section, even this half-bridge can be soft-switched, if the magnetizing inductance of the transformer is reduced and the resulting magnetizing current is used for this purpose.

In summary, the proposed topology can be controlled in DM by means of the duty cycle D_{DM} and the switching frequency f_{sw}, as a conventional series-resonant converter [43]. Furthermore, depending on the transformer design, thus, if the magnetizing current is used or not, either two or all three half-bridges are operated under ZVS conditions, resulting in a very efficient power transfer.

Finally, the complete converter topology is shown in Fig. 5.13, where the different port topologies can be seen. In the next section, the design of the five-winding transformer is discussed in detail and a new concept of operating mode dependent turns ratios is introduced, which significantly improves the achievable converter efficiency in DM operation.

Tab. 5.1: Specifications of the three-port DC/DC converter hardware demonstrator.

	PFC Port	HV Port	LV Port
Port Voltage	166 V	83…166 V	10.5…15 V
RMS Port Current	7.2 A_{RMS}	12 A_{RMS}	66.6 A_{RMS}
Port Power	1 kW	1 kW	1 kW

5.4 Transformer Design

In order to transfer power through the equivalent series-resonant circuits (cf. Fig. 5.5e, Fig. 5.6e and Fig. 5.11d), a positive voltage across the resonant tanks needs to be applied. Hence, the voltage at the input side of the resonant tank needs to be higher than the voltage at the output side. Taking into account possible voltage variations in the two output ports of the converter, the following three inequalities can be found:

$$2V_{\mathrm{PFC}} > \frac{n_{\mathrm{PFC}}}{n_{\mathrm{HV}}} \max(V_{\mathrm{HV}}) \tag{5.34}$$

$$V_{\mathrm{PFC}} > \frac{n_{\mathrm{PFC}}}{n_{\mathrm{LV}}} \max(V_{\mathrm{LV}}) \tag{5.35}$$

$$2\min(V_{\mathrm{HV}}) > \frac{n_{\mathrm{HV}}}{n_{\mathrm{LV}}} \max(V_{\mathrm{LV}}). \tag{5.36}$$

Hereafter, these inequalities are evaluated according to the previously introduced specifications of the TAB hardware prototype (cf. Tab. 2.2), which will be used later on for a hardware implementation of the proposed converter topology and which are repeated here for convenience reasons (cf. Tab. 5.1).

Due to the large currents in the LV port, only a single turn should be used for this winding, in order to minimize the occurring conduction losses ($n_{\mathrm{LV}} = 1$). Consequently, according to the aforementioned specifications, the following inequalities can be derived

$$n_{\mathrm{PFC}} < 2n_{\mathrm{HV}} \tag{5.37}$$

$$n_{\mathrm{PFC}} < 11 \tag{5.38}$$

$$n_{\mathrm{HV}} < 11. \tag{5.39}$$

In general, the number of turns in the PFC windings should be chosen to be as large as possible, such that the winding currents are minimized and, therefore, the currents in the PFC-side semiconductors as well. Considering the

additional voltage drop across the anti-parallel diodes of the LV synchronous rectifiers and the limitation for the sum of the duty cycles ($D_+ + D_- < 0.5$, cf. Section 5.5.1), $n_{\mathrm{PFC}} = 9$ has been found to be the best solution, which guarantees a certain safety margin with respect to the aforementioned limitations, such that for all possible port voltage combinations the maximum output power can be supplied.
The selection of n_{HV} is somewhat more difficult, as there is a trade-off between the conduction losses in the CM and the DM operation. Hence, in CM operation, a large n_{HV} increases the current in the PFC port according to (5.4) and, therefore, the conduction losses as well. Consequently, an as small as possible n_{HV} should be targeted. In DM operation, however, a small number of n_{HV} increases the currents in the HV port for a certain i_{LV} according to (5.32), which is why n_{HV} should be maximized in order to minimize the occurring conduction losses in the HV port. In the application at hand, the full-load efficiency in CM is much more important than the one in DM, as in CM the converter is operated with the maximum output power almost all the time, whereas in DM, the converter is mostly operated with a partial power of 30 %-50 % of P_{max}. Thus, a n_{HV} of 5 turns is selected, whereby the full-load efficiency of the converter in CM is maximized and the occurring conduction losses are "shifted" to the DM operation.

Alternatively, a more complex transformer structure can be used, where operating mode dependent turns ratios are achieved, and the number of turns for each mode can be optimized independently. This concept is introduced in the following section.

5.4.1 Operating Mode Dependent Turns Ratios

Nowadays, the windings of the magnetic components are more and more integrated into the PCB, as the expensive wire-wrapping process is omitted and comparably complex magnetic structures can easily be built. Especially the latter facilitates the design of transformers with many different windings, where still a certain symmetry in the arrangement is desired. Furthermore, the high-frequency (HF) conduction losses in vertically aligned PCB-windings are extremely low, as the vertical parasitic magnetic field components in the transformer windings compensate each other [44, 45] and, therefore, the skin and proximity effects are effectively mitigated. Thus, all PCB-windings should be exactly aligned and arranged on top of each other, whereby the minimum AC resistance in all windings is achieved. In the application at hand, this

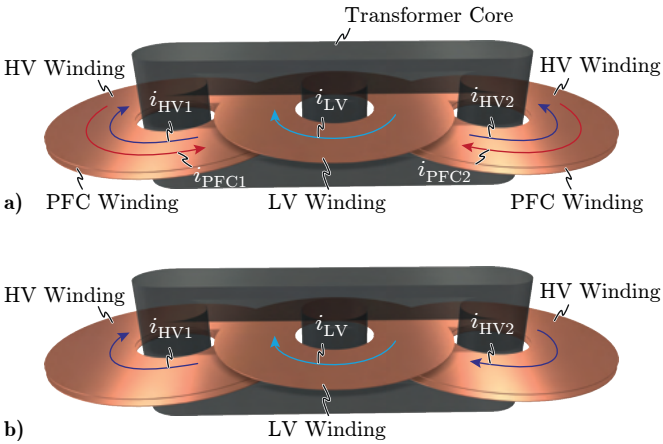


Fig. 5.14: Simplified 3D model of the proposed transformer structure implemented as a PCB-winding transformer for **a)** charge mode (CM) and **b)** drive mode (DM) operation.

means that all five windings should be vertically aligned, which is of course not possible due to the transformer structure, as shown in Fig. 5.14.

Hence, in CM operation, the PFC and the HV windings are perfectly vertically aligned and therefore ideally arranged from an efficiency perspective. However, the area where all three windings overlap is only small, whereby the AC resistance of the LV winding is significantly higher compared to a perfectly aligned arrangement. Nevertheless, as the major part of the power in CM is flowing from the PFC to the HV port and the current in the LV winding is therefore comparably small, the increased LV winding resistance does not reduce the overall efficiency too much.

However, in DM operation, all the power flows from the HV to the LV port, which is why there is hardly any winding area where the winding currents are vertically aligned. Consequently, both windings suffer from the aforementioned HF effects, resulting in a significantly increased AC resistance of the complete current path. The only possibility to mitigate the HF effects and, therefore, to reduce the AC resistance of the current path, is a third HV sub-winding, which is wrapped around the center leg of the transformer core, such that this sub-winding and the LV winding are vertically aligned.

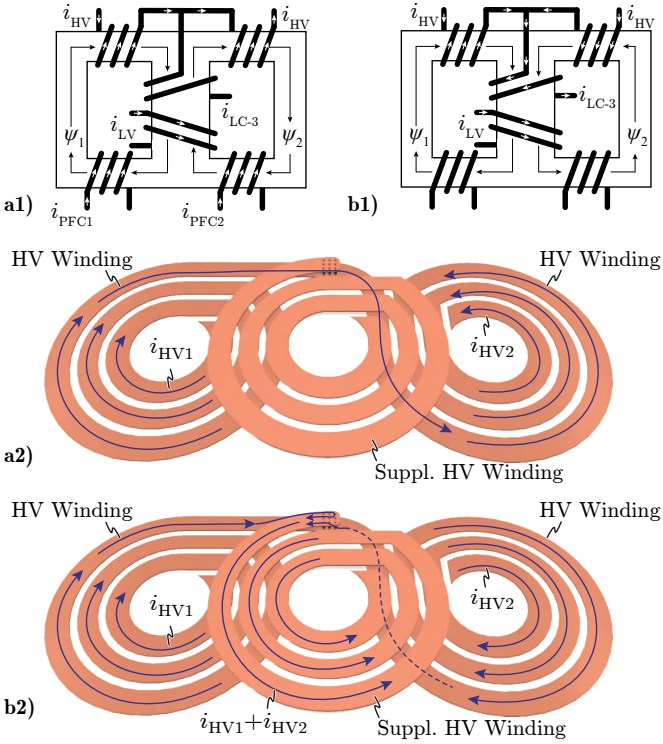
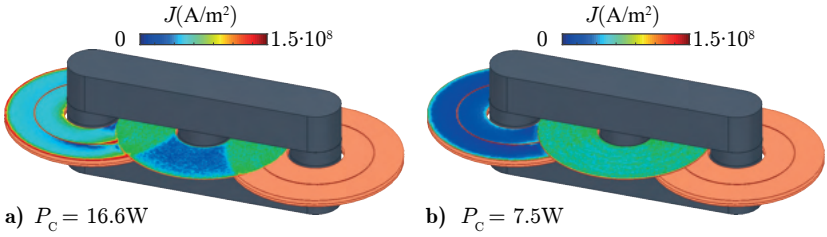


Fig. 5.15: Simplified 3D model of the proposed transformer structure with an operating mode dependent turns ratio, which is achieved by means of the supplementary HV sub-winding as illustrated, for **a)** charge mode (CM) and **b)** drive mode (DM) operation.

However, the additional sub-winding should have no impact on the CM operation, as in this mode the proposed transformer structure has been found to be already very efficient. Hence, the transformer needs to provide an operating mode dependent turns ratio, where the previously mentioned third sub-winding is only effective in DM operation.

This behavior can be achieved by a winding arrangement as illustrated in Fig. 5.15, where in CM operation, the additional sub-winding is inactive and the current flows in the two "old" series-connected HV windings only (cf. Fig. 5.15a), and in DM operation, the HV currents i_{HV1} and i_{HV2} first flow in the two "old" windings, before they merge and continue to flow through the third



a) $P_C = 16.6\text{W}$ **b)** $P_C = 7.5\text{W}$

Fig. 5.16: FEM-simulated current densities and conduction losses in **a)** a conventional transformer arrangement with only two HV sub-windings, and **b)** the same simulation results for a transformer design which employs the concept of operating mode dependent turns ratios, whereby for simplicity reasons, only the current densities in the left HV windings are shown, even though both windings see the same currents.

sub-winding towards the HV-side resonant tank (cf. Fig. 5.15b). Thus, by using the supplementary sub-winding, both aforementioned issues can be solved, as the effective number of turns of the HV winding in DM operation can be increased by an arbitrary number of turns, without affecting the turns ratios during CM operation. Furthermore, the additional sub-winding effectively mitigates the HF effects in the LV winding, whereby again a very efficient transformer structure is achieved.

In order to find the optimal number of turns for the supplementary winding, (5.36), (5.39) and the previously derived number of turns $n_{\text{HV}} = 5$ of the two HV windings around the outer legs of the transformer need to be considered. Thus, as the total number of effective turns of the HV winding needs to be lower than 11, the number of turns of the supplementary winding is directly given as $n_{\text{HV,sup}} < 1/2 \cdot (11 - n_{\text{HV}}) = 3$. Consequently, according to (5.32), the utilization of the supplementary winding in DM operation yields a reduction of the currents in the HV port by more than 50 %, whereby the conduction losses in the HV-side semiconductors during DM operation are even reduced to less than 25 % of their initial values.

Furthermore, the reduction of the HV winding current i_{HV}, in combination with the vertically aligned current flow in the LV winding and the third HV winding, yields significantly reduced conduction losses in the PCB-windings. This is shown based on two simplified PCB-winding transformer designs, as depicted in Fig. 5.16a for a design with only two HV sub-windings and Fig. 5.16b for a design with three HV sub-windings, whereby in both figures the simulated current densities J and the simulated conduction losses P_C for $i_{\text{LV,pk}} = 95$ A are shown. Hence, with the proposed concept of operating mode

dependent turns ratios, the conduction losses in the windings can be reduced by almost 55 %, without changing the size of the transformer.

Having optimized the design of the PFC- and the HV-side windings, the only winding which has not yet been considered is the LV winding. However, the optimization of the LV winding is crucial for an efficient converter operation, which is why it is discussed in detail in the next section.

5.4.2 Winding-Integration of the Low-Voltage Synchronous Rectifier

The large currents in the LV port require a large copper cross-section of the LV winding, in order to minimize the occurring conduction losses. Unfortunately, the copper layer thickness in conventional PCBs is somewhere between 35 µm...105 µm only, which is why the available copper cross-section for current conduction in PCBs is fairly limited. Thus, a large winding width would be required in order to end up with a reasonable cross-section of the LV winding, which would reduce the power density of the transformer significantly. Fortunately, there are two possibilities on how to circumvent this issue, as previously introduced in Section 4.2.2: On the one hand, the LV port can be implemented as a center-tapped rectifier, where the positive and the negative half-wave are rectified by means of two separate circuits and the current in each sub-winding is therefore halved (cf. Fig. 5.17a), or on the other hand, the copper cross-section of the PCB can be enlarged by means of additional copper foils, which are solder to the top and the bottom layer of the PCB and are then used as LV windings. In addition, the same design strategy as in the two-port converter can be applied, where the LV rectifier switches as well as the LV output capacitors are directly integrated into the the transformer winding, if the top and the bottom layer of the PCB are used for the two sub-windings of the center-tapped rectifier [44] (cf. Fig. 5.17b). Consequently, the lossy terminations of the windings are avoided and the length of the current path for the HF current in the LV port is minimized.

By utilizing the derived design guidelines and the proposed design concepts for the main transformer, very efficient and power-dense transformer designs can be achieved. However, besides the main transformer, there are also the three resonant tanks and the various semiconductors, which have a large impact on the efficiency and the power density of the overall converter system. The selection of these components is part of an overall system optimization, which is briefly discussed in the next section.

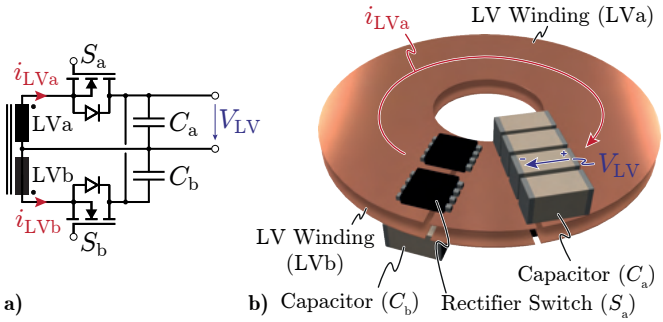


Fig. 5.17: a) Schematic of a center-tapped synchronous rectifier with a split winding (LVa and LVb) and **b)** its practical implementation in a PCB-winding transformer, where the two sub-circuits are identical, but flipped with respect to the PCB plane.

5.5 System Optimization

So far, only the design of the main transformer of the proposed converter topology has been discussed in detail. However, an appropriate selection of the power semiconductors and the three resonant tanks is equally important to achieve a reasonable efficiency and power density of the overall converter system. Consequently, some general guidelines for the selection of these components will be given in the following sections.

5.5.1 Optimal Selection of the Resonant Tanks

The total impedance of a L-C series-resonant circuit is defined by

$$|Z_{LC}| = \frac{\omega^2 LC - 1}{\omega C}. \tag{5.40}$$

Thus, assuming a certain given resonant frequency $f_{res} = 1/(2\pi\sqrt{LC})$, the only remaining degree of freedom (DOF) is the ratio between L and C. The selection of this ratio, however, is extremely important for the overall converter operation and efficiency, as it has a direct impact on the occurring conduction losses in all power components.
Hence, assuming a certain input voltage V_{in}, a certain output voltage V_{out} and a desired output power P_{out}, the required periodic voltage-time area ψ_{LC} at the input of the resonant tank depends on the resonant tank impedance $Z_{LC}(f_{sw})$ only, which for its part is inherently defined by the L/C ratio (cf. Fig. 5.18).

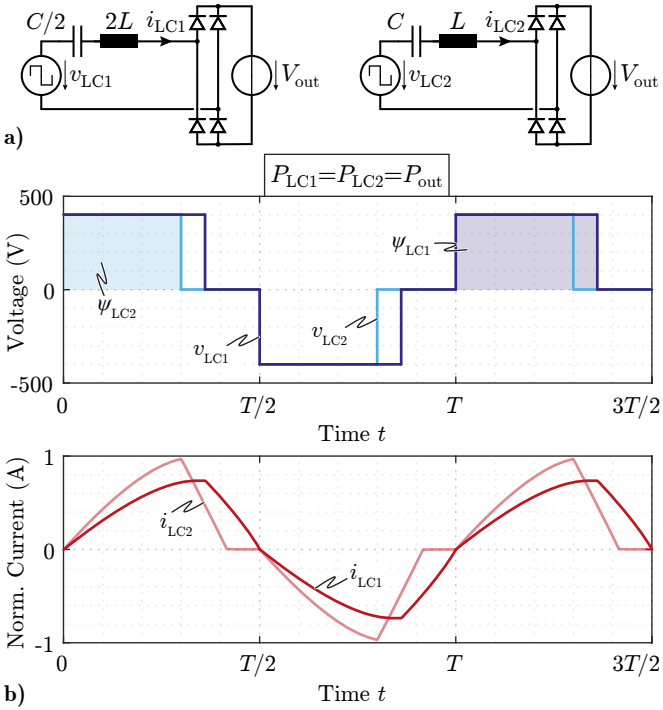


Fig. 5.18: a) Series-resonant circuits with the same resonant frequency f_{res}, but different L/C ratios. **b)** Corresponding voltage and current waveforms, which lead to the same output power ($P_{LC1} = P_{LC2} = P_{out}$).

Thus, the larger L/C is, the more ψ_{LC} is required, whereby the current waveform i_{LCx} is approaching the CCM, where the minimum peak-to-average current ratio is achieved (cf. Fig. 5.18b). Consequently, for a certain required output power P_{out} and a given switching frequency f_{sw}, a maximized L/C ratio always results in minimal rms currents, whereby minimal overall conduction losses are expected.

However, the duty-cycle constraint ($D_+ + D_- < 0.5$) inherently limits the maximum ψ_{LC}, which can be generated at the lowest switching frequency $f_{sw,min} = f_{res}$ and, therefore, the maximum transferable output power P_{max} (L/C) as well. This constraint yields an upper limit for the L/C ratio, as for all possible port voltage combinations (V_{PFC}, V_{HV}, V_{LV}) the supply of the maximum required output power P_{max} needs to be ensured.

In CM operation, it can be shown, that the sum of D_+ and D_- is maximum if the total output power P_{max} is split equally among the HV and the LV port. Thus, the maximum allowable L/C ratio is found for $f_{sw} = f_{res}$, $P_{HV} = P_{LV} = P_{max}/2$, $V_{HV} = \max(V_{HV})$ and $V_{LV} = \max(V_{LV})$, where $D_+ + D_- < 0.5$ needs to be ensured. However, for the sake of clarity, the detailed calculation of this ratio is explained in Appendix B.1, which is why only the results are given here.
For the specifications of the application at hand (cf. Tab. 5.1) and an exemplary resonant frequency of $f_{res} = 300\,\text{kHz}$, the loss-optimal resonant tank is given as $L_{PFC} = 4\,\mu\text{H}$ and $C_{PFC} = 70\,\text{nH}$. However, depending on the application, a higher power density might be desired, whereby a lower L/C ratio could be chosen to minimize the volume of the resonant inductor. Unfortunately, this would come at the expense of increased conduction losses in the complete converter system, which is why L/C should not be lowered too much.

The same analysis can also be done for the DM operation, where the optimal L_{HV}/C_{HV} ratio for a constant switching frequency operation is found the same way. However, assuming a standard transformer design, without operating mode dependent turns ratios, the comparably small HV side referred output voltage of $V'_{LV} = n_{HV}/2 \cdot V_{LV}$ results in large voltages across the resonant tank during the active phase of a half-period ($t \in D_{DM} \cdot T$). Consequently, a large inductance L_{DM} is required in order to limit the current rise during that period and, therefore, the peak-to-average ratio of the resonant current as well. Thus, for a certain resonant frequency $f_{res,DM}$, only a small resonant capacitor C_{DM} can be used, which inherently results in large capacitor voltages for large

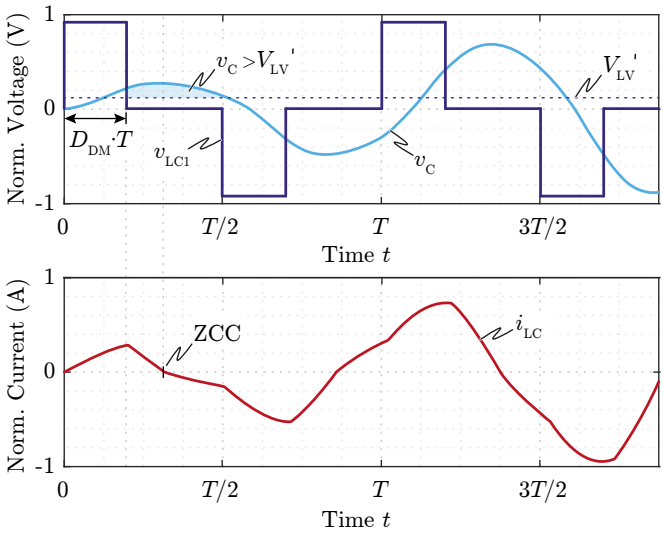


Fig. 5.19: Voltage and current waveforms of an unstable converter operation due to a too small resonant capacitor, resulting in a runaway situation.

output power values. The peak voltage $v_{C,max}$ across the capacitor should, however, not exceed the HV side referred output voltage V_{LV}' of the converter, as otherwise, the synchronous rectifier in the output port is positively biased during the inactive phase of a half-period, where $v_{LCx} = 0\,V$ (cf. Fig. 5.19). Hence, the subsequent resonant half-cycle does not start synchronously with the respective subsequent active phase, but rather starts already right after the ZCC of the resonant current during the inactive phase. Consequently, the resonant operation is destabilized and the resonant current keeps increasing until the first component in the power path is destroyed.

The minimum allowable resonant capacitance for $P_{LV} = P_{max}$ and $f_{sw} = f_{res,DM}$, for which the peak voltage across the capacitor stays below the HV side referred output voltage, can be calculated according to

$$C_{DM,min} = \frac{P_{max}}{4 f_{res,DM} \cdot \left(\frac{n_{HV}}{2} \min(V_{LV})\right)^2}, \tag{5.41}$$

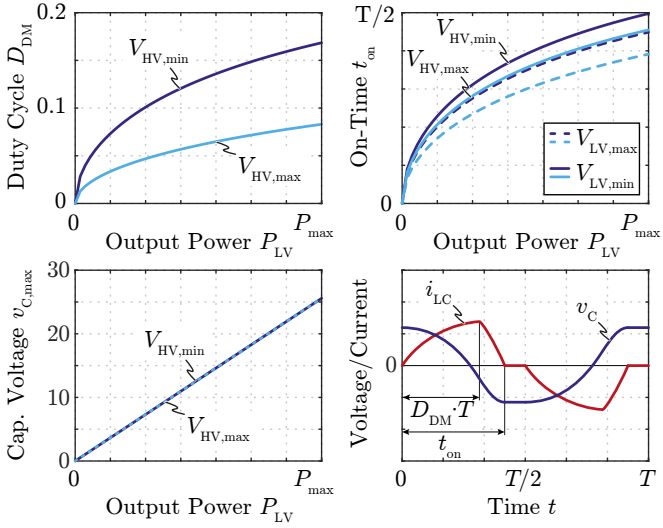


Fig. 5.20: Required duty cycle D_{DM}, resulting on-times t_{on} and peak capacitor voltages $v_{C,max}$ for the minimum and the maximum HV and LV port voltages V_{HV} and V_{LV}, where a constant switching frequency f_{sw} is assumed. Simulation parameters are: $f_{sw} = f_{sw,CM} = 300\,\text{kHz}$, $f_{sw,DM} = 180\,\text{kHz}$, $L_{HV} = 450\,\text{nH}$ and $C_{HV} = 1.73\,\mu\text{F}$.

whereby the maximum resonant inductance is given by

$$L_{DM,max} = \frac{\left(\frac{n_{HV}}{2} \min(V_{LV})\right)^2}{P_{max} f_{res,DM} \pi^2}. \tag{5.42}$$

Unfortunately, $L_{DM,max}$ is usually small, which inherently results in an extremely large peak-to-average ratio of the resonant current i_{LC}, whereby the efficiency of the converter operation is reduced.
Nevertheless, there are three possibilities to circumvent this issue: First, the proposed concept of the operating mode dependent turns ratios can be used, whereby n_{HV} and $L_{DM,max}$ are increased, and the applied voltage time areas across the resonant tank during the active phase are therefore significantly decreased.
Second, the converter could be operated with a constant switching frequency f_{sw}, which is far above the resonant frequency of the HV-side resonant tank $f_{res,DM}$, in order to minimize the amount of charge, which is transferred through the resonant tank per switching cycle, and therefore, the peak cur-

rents and the capacitor voltage as well. A higher switching frequency, however, would further increase the switching losses of the converter, which is why not the switching frequency f_{sw} is increased, but rather $f_{res,DM}$ is decreased. Thus, in order to optimally use the transformer core, the switching frequency $f_{sw,DM}$ in DM is chosen to be equal to the resonant frequency of the PFC-side resonant tanks $f_{res,CM}$, whereby the efficiency of the converter in DM operation needs to be maximized by lowering $f_{res,DM}$.
The optimal value for $f_{res,DM}$ is found in such a way, that for the maximum output power P_{max} and $f_{sw,DM} = f_{res,CM}$, an almost continuous resonant current i_{LC} is achieved, according to $t_{on,max} \approx T/2$ (cf. Fig. 5.20). Hence, in contrast to the optimization of the PFC-side resonant tanks, where the switching frequency and the resonant frequency were assumed to be equal, in the optimization of the HV-side resonant tank, both the optimal L/C ratio as well as the optimal $f_{res,DM}$ need to be found. Fortunately, this is not much more difficult than the optimization of the PFC-side resonant tanks, as explained in Appendix B.2. In the application at hand, and for the same exemplary $f_{res,CM}$ of 300 kHz, the optimal $f_{res,DM}$, L_{HV} and C_{HV} are given as 180 kHz, 450 nH and 1.73 µF, respectively.

However, in order to further increase the partial-load efficiency of the converter in DM, the third option can be used, where the switching frequency can be dynamically adapted to the momentary output power P_{out}, such that BCM is maintained over a large output power range and the conduction losses are therefore minimized (cf. Fig. 5.21). Furthermore, the operation of the converter in BCM mitigates the issue of a destabilized resonant operation, as there is no zero-current interval, where the synchronous rectifier could be mistakenly positive biased (cf. Fig. 5.19). Thus, the limitation due to (5.41) does not hold anymore and the L_{DM}/C_{DM} ratio can be selected similarly to the L_{CM}/C_{CM} ratio for the same resonant frequency $f_{res,DM} = f_{res,CM}$. However, the optimal switching frequency $f_{sw}(P_{LV})$ is a tradeoff between switching losses and conduction losses and depends on the final converter design. Hence, below a certain minimum output power $P_{LV,min}$, a constant switching frequency and DCM is used to limit the occurring switching losses (cf. Fig. 5.21a).

Finally, in the optimization of the overall converter system, the resonant frequency $f_{res,CM}$ is an optimization parameter, where for each $f_{res,CM}$ the optimal values for L_{PFC}, C_{PFC}, L_{HV} and C_{HV} are calculated and, therefore, the waveforms in all power components under all operating conditions are known. These waveforms are then used to optimize the designs of the main

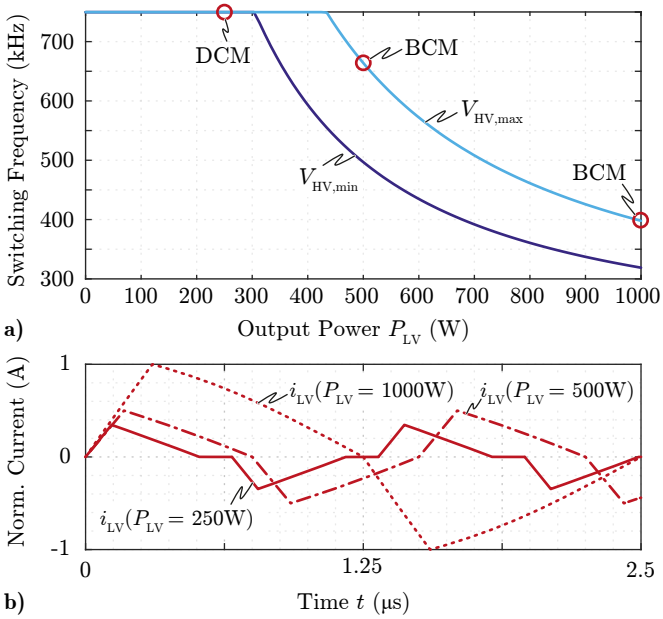
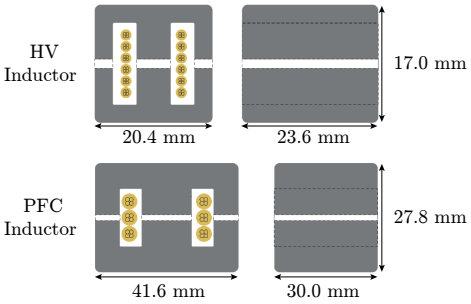


Fig. 5.21: a) Switching frequency variation $f_{sw}(P_{LV})$ in DM with an exemplary $f_{res,CM}$ of 300 kHz, $f_{res,DM}$ of 180 kHz and an arbitrary $f_{sw,max}$ of 750 kHz. **b)** Resonant currents, which correspond to the red circles indicated in **a)**, where the boundary (BCM) and the discontinuous (DCM) conduction mode are illustrated.



Specifications	
Type of Wire:	Litz (900/40 µm)
Number of Turns:	6
Air Gap Length:	1.6 mm
Core Losses:	2.83 W
Winding Losses:	1.12 W

Specifications	
Type of Wire:	Litz (5000/40 µm)
Number of Turns:	3
Air Gap Length:	1.7 mm
Core Losses:	6.13 W
Winding Losses:	1.73 W

Fig. 5.22: Exemplary design specifications for of the PFC- and HV-side litz wire winding inductors, together with their respective worst case losses (max. current), which were derived by a MATLAB-based design optimization script.

power components, as e.g. the transformer, the power semiconductors and the resonant inductors, as will be discussed in the following.

5.5.2 Optimal Design of the Resonant Inductors

The design of the resonant inductor is a standard optimization problem for a given set of specifications (L, i_{pk}, i_{rms}), which has already been discussed extensively in literature for both, conventional wire-wound [46–49] as well as PCB-integrated inductors (cf. Chapter 3). Consequently, there is no need to further elaborate on the design of this component, which is why it is not explained any further here and only the exemplary optimization results are shown in Fig. 5.22.

5.5.3 Optimal Design of the Transformer

The design of the transformer, however, is unique to this application and its structure has already been explained in Section 5.4. As the number of turns is inherently given according to (5.37)-(5.39), there are mainly two optimization parameters left: On the one hand, the core cross-section A_{C}, which allows to increase/decrease the occurring core losses and at the same time to decrease/increase the volume of the transformer core, and on the other hand, the total winding width b_{W} of the circular transformer windings, whereby the expected conduction losses in the windings can be influenced. Especially

this parameter has a large impact on the overall transformer volume, as it inherently defines the total PCB area A_{tot}, which is occupied by the transformer in the final application. Thus, there is a trade-off between power density and efficiency, as in every power electronic system.
The results of such an exemplary Pareto-optimization for the five winding transformer is shown in Fig. 5.23a, for the specifications given in Tab. 5.1 and an exemplary resonant frequency of $f_{\text{res}} = 300\,\text{kHz}$. The main parameters of the highlighted transformer design are summarized in Fig. 5.23b, which has finally also been selected for hardware implementation. The corresponding 3D model is shown in Fig. 5.23c, where the terminations of the windings are drawn comparably long and wide, as they are adapted in the final PCB design in order to optimize the connection between the power semiconductors and the respective winding terminals.

One of the main benefits of PCB-winding transformers are the large allowable current densities in the PCB-windings (up to $100\,\text{A/mm}^2$), which is why they can be built extremely power-dense. However, such large current densities can only be used, if the occurring conduction losses can be dissipated by means of an appropriate cooling system, in order to keep the maximum PCB temperature below a certain limit (usually 130°…150°). In the application at hand, the complete transformer is enclosed by means of a CNC-milled aluminum heat sink, which is attached to the winding and the core by means of a thermal interface material (TIM), such that galvanic isolation is ensured (cf. Fig. 5.23d). The same heat sink is also used to dissipate the losses of the LV-side synchronous rectifiers, as the employed packages are designed for top-side cooling and, therefore, allow for an easy attachment to the common aluminum heat sink through a TIM.
The thermal performance of the aluminum heat sink is shown in Fig. 5.24 for the worst case scenarios in charge and drive mode, respectively.

5.5.4 Optimal Selection of the Power Semiconductors

Finally, compared to the design of the magnetic components, the selection of the power semiconductors is quite straight-forward, as a preselection of appropriate power semiconductors can be made based on the required minimum breakdown voltages of the switches, in combination with their figures-of-merit ($R_{\text{ds,on}} \cdot C_{\text{oss}}$). The most promising candidates are then used in the overall system optimization, where the conduction losses in each semiconductor are estimated based on a simple thermal model of the switches

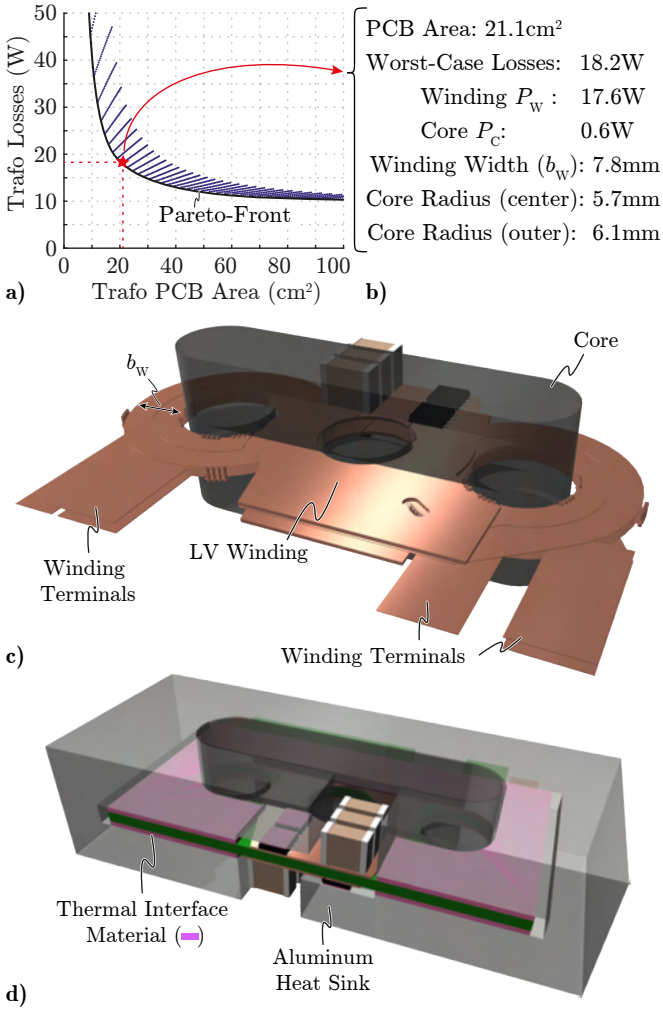


Fig. 5.23: a) Results of an exemplary Pareto optimization for the five winding transformer and **b)** the specifications of the highlighted design. **c)** and **d)** 3D models of the selected transformer design with and without the aluminum heat sink.

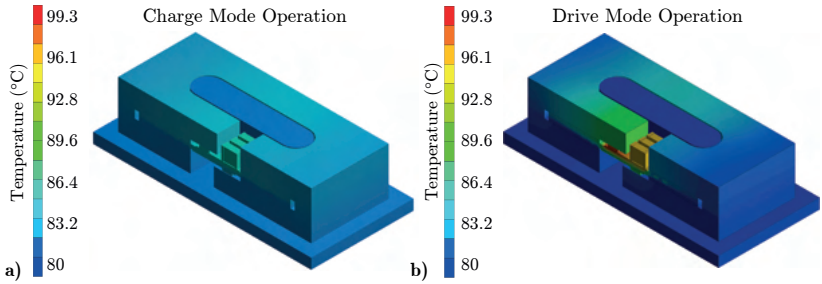


Fig. 5.24: Thermal simulations for the worst case scenarios of both, **a)** charge mode (CM) and **b)** drive mode (DM) operation.

and the temperature dependent datasheet values of the $R_{\mathrm{ds,on}}$, according to

$$P_{\mathrm{cond}}(T_{\mathrm{jc}}) = R_{\mathrm{ds,on}}(T_{\mathrm{jc}}) \cdot I_{\mathrm{rms}}^2. \tag{5.43}$$

The switching losses of the zero-current-switched half-bridges can then be estimated based on the given C_{oss} values, according to [50]

$$P_{\mathrm{oss}}(f_{\mathrm{sw}}) = 2 f_{\mathrm{sw}} V_{\mathrm{dc}} \cdot \int_0^{V_{\mathrm{dc}}} C_{\mathrm{oss}}(v)\mathrm{d}v. \tag{5.44}$$

Hence, for each $f_{\mathrm{res,CM}}$, the most efficient semiconductors are selected for all three converter ports and the resulting efficiency of the overall converter system is calculated. Finally, the converter design is selected, which fits best the targeted power density and efficiency.

However, it should be mentioned that it is extremely important to use a realistic thermal model for the semiconductors, as otherwise, the optimization results might lead to a wrong selection of the semiconductors, whereby thermal issues in the final hardware prototype could hardly be avoided. This is shown in the following based on two exemplary 200 V semiconductors.

Thermal Constraints for the Semiconductor Selection For the PFC and the HV port, there are two different possible 200 V GaN switches, which are worth being considered: The EPC2034 and the EPC2010C eGaN FETs. The first one has a much lower $R_{\mathrm{DS,on}}$ but a comparably high C_{oss}, whereby the latter has a very low C_{oss} at the expense of a higher $R_{\mathrm{ds,on}}$. Calculating the losses for both switch types for different HV port voltages V_{HV} and maximum

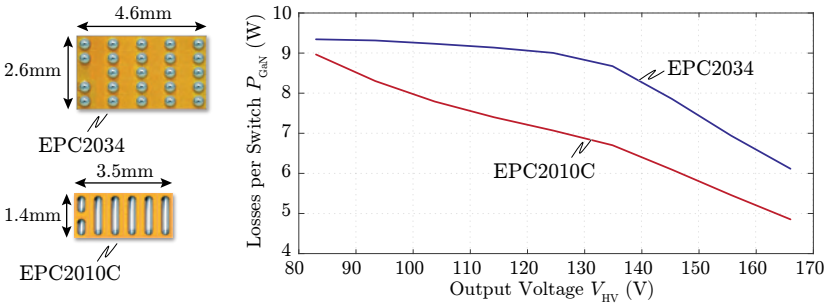


Fig. 5.25: Calculated losses occurring in the PFC-side GaN switches in half-bridge HB_B for two different devices (cf. Fig. 5.4a).

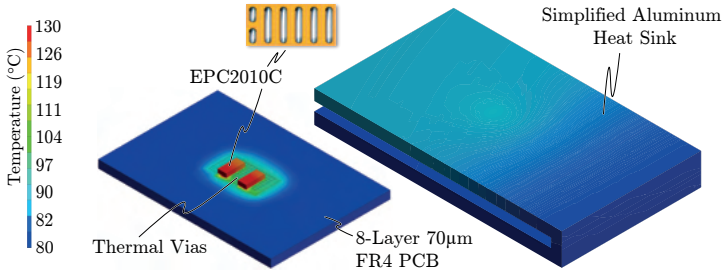


Fig. 5.26: Thermal simulation of a half-bridge comprising two EPC2010C devices for 9 W of losses per switch. The switches are soldered to an 8-layer PCB using the recommended footprint of the datasheet and additional thermal vias, whereby the PCB and the switches are thermally connected to a U-shaped aluminum profile (which emulates the heat sink) through thermal interface material (TIM) with a thermal conductivity of 6 W/(m K).

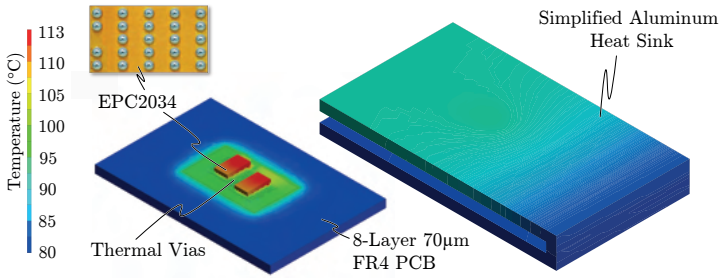


Fig. 5.27: Thermal simulation of a half-bridge comprising two EPC2034 devices for 9.3 W of losses per switch. The switches are soldered to an 8-layer PCB using the recommended footprint of the datasheet and additional thermal vias, whereby the PCB and the switches are thermally connected to a U-shaped aluminum profile (which emulates the heat sink) through thermal interface material (TIM) with a thermal conductivity of 6 W/(m K).

output power P_{HV}, yields the loss curve shown in Fig. 5.25. Thus, one might think that the EPC2010C is clearly the better option in this case, which is true from an electrical point of view, but the extremely small package of those switches limits the amount of losses which can be extracted from the switches, as can be proven by means of thermal simulations. Hence, even though the switch is cooled through the PCB by means of thermal vias and at the same time is directly attached to the top side heat sink through a thermal interface material, the case temperature is still above 130 °C, which is far beyond the safe operating area in a practical application, especially in consideration of potential non-idealities in the thermal paths of a real setup (cf. Fig. 5.26). Consequently, the more lossy EPC2034 have to be used, as their larger package allows for dissipating more losses, as shown in Fig. 5.27 (for the same cooling system as used in the simulation for the EPC2010C). The simulated peak case temperature of 113 °C lies within the limits, whereby these switches are used in the final hardware prototype, even though they generate higher losses than the EPC2010C.

Furthermore, the EPC2034 switches are also used in all the other half-bridges in the PFC and the HV port, as on the one hand, they have a very low $R_{\mathrm{ds,on}}$ compared to the size of the switch, and on the other hand, using the same package for all the switches simplifies their thermal connection to a common heat sink, as their top surfaces are on the same level.

In order to explore the achievable performance of the proposed topology and to experimentally verify the functionality of the converter operation, a simple hardware demonstrator has been built, which was optimized with respect to flexibility in terms of interchangeability of the power components and at the same time accessibility of the most important voltage and current measurements. The specifications of the hardware demonstrator and the corresponding experimental measurements are discussed in the next section.

5.6 Experimental Measurements

The aforementioned optimization has been conducted for the specifications of Tab. 5.1, where it has been found, that due to the different operating modes and the wide port voltage variations, it is hardly possible to find a converter design, which is optimal under all operating conditions. However, it has been found, that a resonant frequency $f_{\mathrm{res,CM}}$ of 300 kHz yields a good compromise between power density, partial-load efficiency and full-load efficiency in both operating modes, which is why the results of the calculations in the previous sections have all been shown for this specific frequency. Even though a higher resonant/switching frequency would result in a higher power density of the converter, the resulting increase of the switching losses would lower the partial-load efficiency significantly, which is an important factor, especially in DM operation. The specifications of the selected converter design are summarized in Tab. 5.2 and the respective PCB design of the hardware demonstrator is depicted in Fig. 5.28. As can be seen based on the number of turns of the transformer, the concept of operating mode dependent turn ratios has not been employed in the hardware demonstrator, as in this application, the supplementary HV winding would require a comparably expensive 10-layer PCB. Instead, a conventional transformer arrangement is employed, where an inexpensive 8-layer PCB can be used. The application of the conventional transformer comes at the expense of a significantly reduced efficiency in DM and a slightly reduced power density of the converter, as the reduced $n_{\mathrm{HV}}/n_{\mathrm{LV}}$ ratio results in significantly higher conduction losses in the windings and the HV semiconductors in DM operation. Furthermore, the necessary reduction of $f_{\mathrm{res,DM}}$ yields a larger volume of the resonant inductor L_{HV}, as already mentioned in the previous section. Nevertheless, even with the conventional transformer, a decent performance of the converter is expected, especially in CM (cf. Fig. 5.29), as will be shown in the following.

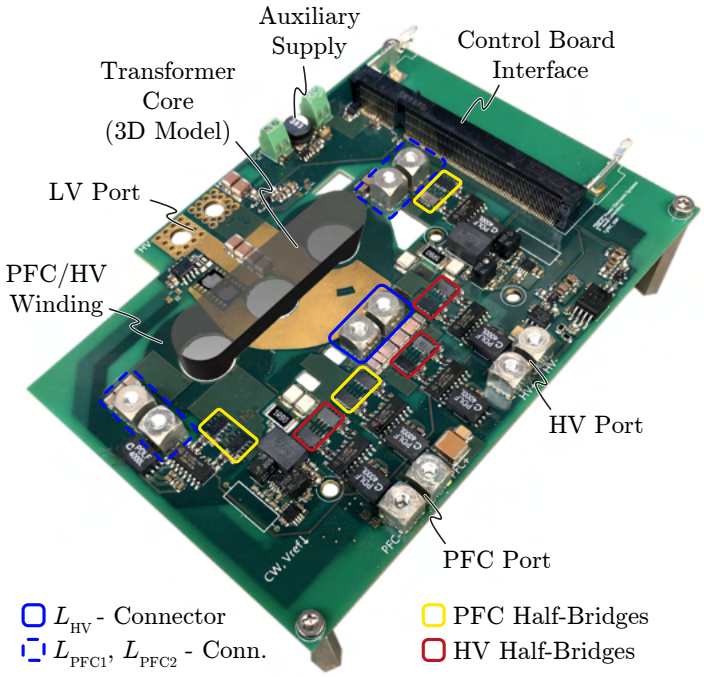


Fig. 5.28: 1 kW hardware demonstrator, which is optimized with respect to accessibility of all important voltage and current measurements, as well as flexibility in terms of interchangeability of the resonant inductors, which can be attached by means of screw connectors (Dimensions: 14 cm x 10 cm x 2.5 cm).

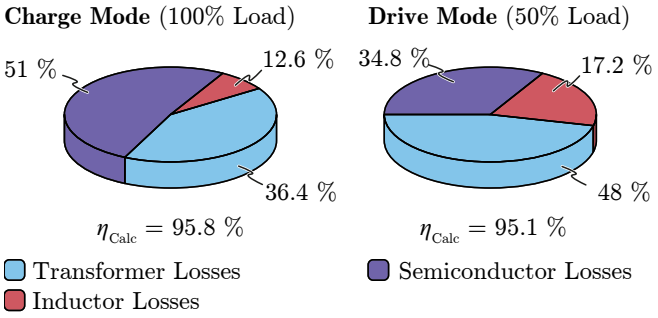


Fig. 5.29: Loss distribution for two exemplary operating conditions in charge mode (CM) and drive mode (DM) operation.

Tab. 5.2: Specifications of the 1 kW three-port DC/DC converter hardware prototype.

Semiconductors		
PFC Port	HV Port	LV Port
EPC2034 (GaN)	EPC2034 (GaN)	TPWR7904 (Si)
Resonant Tanks		
PFC Port	HV Port	LV Port
$L_{\mathrm{PFC}} = 4\,\mu\mathrm{H}$	$L_{\mathrm{HV}} = 2.17\,\mu\mathrm{H}$	
$C_{\mathrm{PFC}} = 70\,\mathrm{nF}$	$C_{\mathrm{HV}} = 130\,\mathrm{nF}$	
Transformer		
PFC Port	HV Port	LV Port
$n_{\mathrm{PFC}} = 9$	$n_{\mathrm{HV}} = 5$	$n_{\mathrm{LV}} = 1$
$b_{\mathrm{W,PFC}} = 2.5\,\mathrm{mm}$	$b_{\mathrm{W,HV}} = 3.8\,\mathrm{mm}$	$b_{\mathrm{W,LV}} = 7.8\,\mathrm{mm}$
$h_{\mathrm{Cu,PFC}} = 70\,\mu\mathrm{m}$	$h_{\mathrm{Cu,HV}} = 70\,\mu\mathrm{m}$	$h_{\mathrm{Cu,LV}} = 500\,\mu\mathrm{m}$
$A_{\mathrm{C}} = 117\,\mathrm{mm}^2$ (N87)		

5.6.1 Charge Mode Operation

The first and most important topology-specific behavior of the converter, which needs to be experimentally verified, is the perfectly decoupled power flow control in CM. Hence, a load step in either the HV or the LV port should by no means affect the power flow to the other port. This behavior is shown in Fig. 5.30a for a load step in the HV port, and in Fig. 5.30b for a load step in the LV port by means of the experimentally measured current waveforms i_{HV} and i_{LV}.

In both cases, a perfect decoupling can be observed, as the two output ports are controlled by two completely independent control variables (D_+ and D_-). This perfect decoupling is achieved for DCM1 only, where the HV current drops to zero within the active period of the LV current (cf. Fig. 5.31). As can be seen based on the measured current waveforms, the C_{oss} of especially the LV-side semiconductors, yield significant oscillations during the zero-current intervals. These oscillations can unfortunately not be avoided, due to the undefined LV-side winding voltage during the aforementioned zero-current intervals, as the C_{oss} of the LV switches can be charged to arbitrary voltages v_{Coss}. However, these oscillations do not harm the converter efficiency too

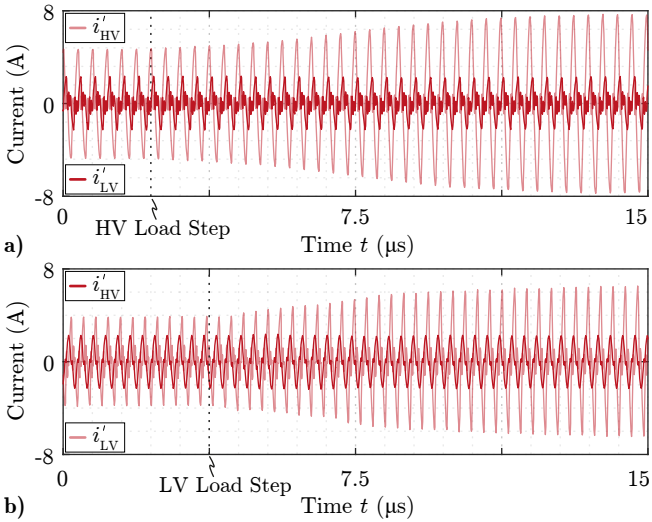


Fig. 5.30: Experimentally measured PFC side referred output currents i'_{HV} and i'_{LV} for **a)** a load step in the HV port and **b)** a load step in the LV port. As expected, the two ports do not affect each other at all.

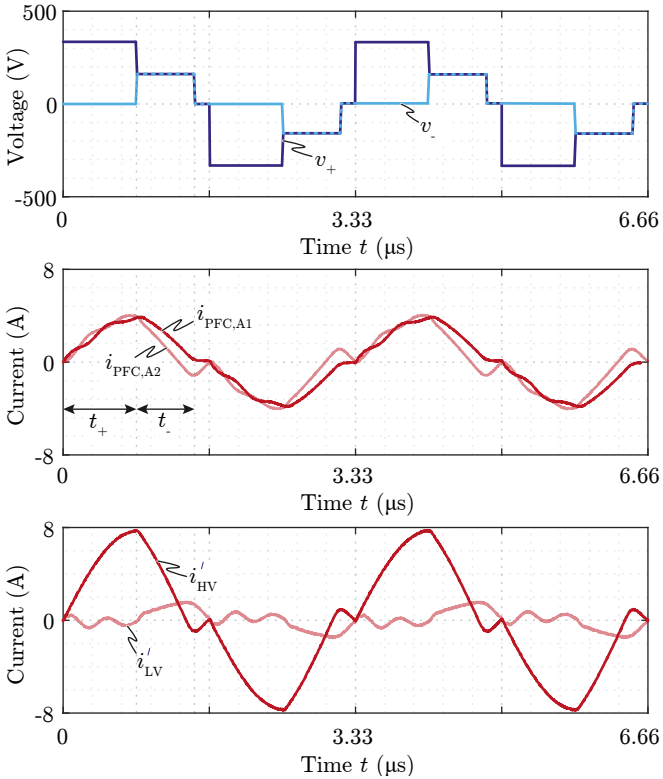


Fig. 5.31: Experimentally measured currents $i_{PFC,A1}$, $i_{PFC,A2}$, i'_{HV} and i'_{LV}, all referred to the PFC side, for charge mode (CM) operation in DCM1.

much, as long as they do not result in partial hard-switching of the power semiconductors.
For very low LV output power values or low HV port voltages V_{HV}, the HV port current i_{HV} enters DCM2, as shown in Fig. 5.32. Consequently, the LV port is still decoupled from the HV port, but a change in D_- needs to be compensated by D_+, such that a load step in the LV-side still does not affect the HV port by any means (cf. Section 5.2.1). Fortunately, this can easily be achieved by means of an appropriate control, as discussed in Section 5.2.1.

In order to evaluate the achievable performance of the converter in nominal CM operation ($V_{LV} = 15\,V$, $P_{LV} = 100\,W$), the efficiency has been measured

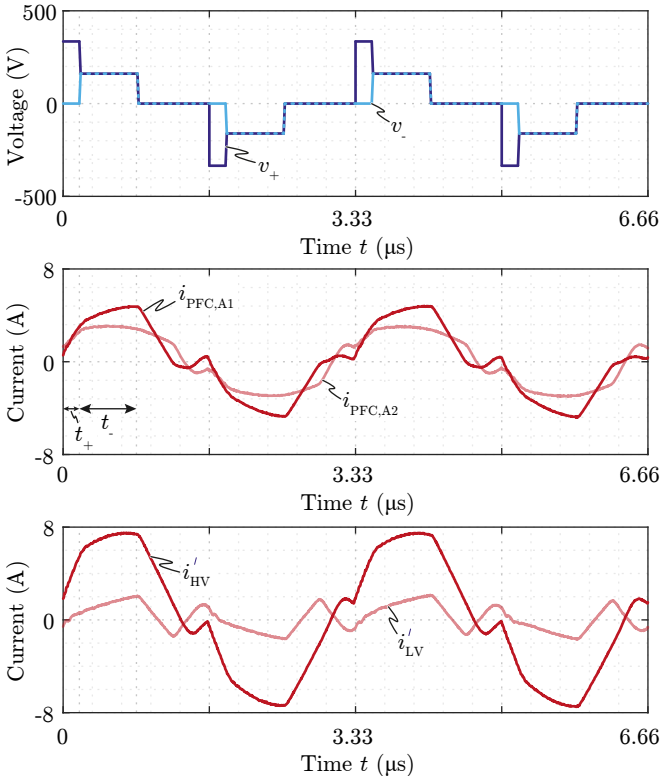


Fig. 5.32: Experimentally measured currents $i_{PFC,A1}$, $i_{PFC,A2}$, i'_{HV} and i'_{LV}, all referred to the PFC side, for charge mode (CM) operation in DCM2.

with different HV output power values P_{HV} for the maximum and the minimum HV port voltage. The results are summarized in Fig. 5.33, where it can easily be seen, that for the nominal HV output voltage (166 V), where the PFC/HV semiconductors are optimally utilized by means of a high voltage and a low current, the targeted full-load efficiency of 95 % is easily met. In contrast, the comparably poor PFC/HV semiconductor utilization for worst-case conditions ($V_{\mathrm{HV}} = 83\,\mathrm{V}$), where large currents in both ports are required, results in significant conduction losses and, therefore, only limited efficiency. However, the efficiency for this operating condition is not of importance, as it hardly ever occurs and the converter just needs to withstand the thermal stresses during operation with low HV-side voltages and/or low LV-side voltages.
It should be noted, that especially for low output power values, the measured efficiencies show certain fluctuations, which mainly originate due to the aforementioned oscillatory currents during the zero-current intervals of i_{LV}. Hence, if the subsequent switching cycle starts during a valley of i_{LV}, the oscillatory current assists ZVS of the semiconductors, whereby the switching losses are reduced and the efficiency is increased. In contrast, starting the subsequent switching cycle during a peak of i_{LV} impedes ZVS of the semiconductors, whereby only partial soft-switching is achieved. Nevertheless, this issue could be mitigated by increasing the magnetizing current, which, however, would further increase the conduction losses in return.

In the next section, the converter performance in the second operating mode, the DM, is investigated in a similar way.

5.6.2 Drive Mode Operation

In DM, the converter topology is operated as a conventional SRC by means of duty cycle and switching frequency variation. Hence, for a large output power P_{LV}, the control keeps BCM by adapting the switching frequency, such that the occurring conduction losses are minimized and ZVS of all power semiconductors is achieved (cf. Fig. 5.34a). However, below a certain P_{LV}, the required switching frequency for BCM would be too high, whereby the AC conduction losses would be significantly increased and at the same time, the timing of the LV-side synchronous rectifier would be difficult. Furthermore, the gate drive losses of the LV Si switches would start to affect the converter efficiency significantly, which is why the switching frequency is kept constant and the duty cycle is further decreased. Consequently, the converter

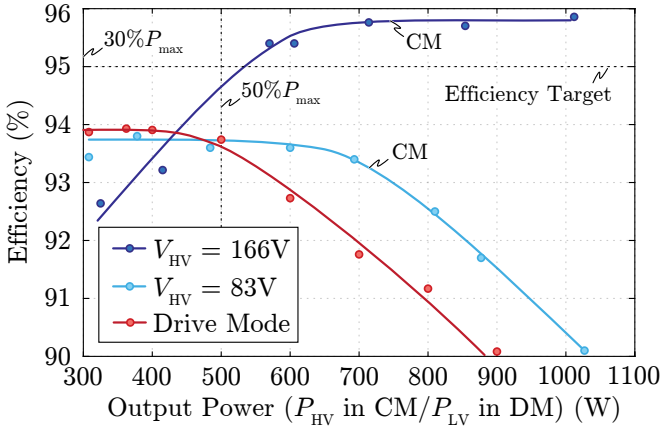


Fig. 5.33: Experimentally measured efficiency of the 1 kW hardware demonstrator for both, charge mode (CM) and drive mode (DM) operation with a LV output voltage of 15 V and a LV output power in CM of 100 W.

enters DCM, whereby the magnetizing current ensures ZVS of the HV-side semiconductors (cf. Fig. 5.34b).

Similar to the CM, the efficiency was measured in DM for different output power values P_{LV}, a nominal LV output voltage of 15 V and a HV port voltage V_{HV} of 166 V. The measured performance is summarized in Fig. 5.33, where it can be seen, that the targeted partial-load efficiency of 95 % for 30 %-50 % of $P_{LV,max}$ was missed by 1.2 % with the current hardware demonstrator.
However, this is not really surprising, as the HF conduction losses in the transformer in DM are extremely high, as there is no vertically aligned current flow in the cost-optimized transformer design, where the concept of operating mode dependent turns ratios is not applied. These losses have been underestimated in the optimization, as they highly depend on the actual transformer and overall PCB design.
Furthermore, as discussed in Section 5.4.1, not only the HF conduction losses in the transformer are significant, but also the HV-side currents are extremely large, due to the low effective turns ratio in DM, whereby the ratio between the current in the LV winding and the current in the leading bridge-leg of the HV side (HB_3) is 2.5 only. Hence, there is a huge current flowing in the HV-side semiconductors, whereby a poor semiconductor utilization results.

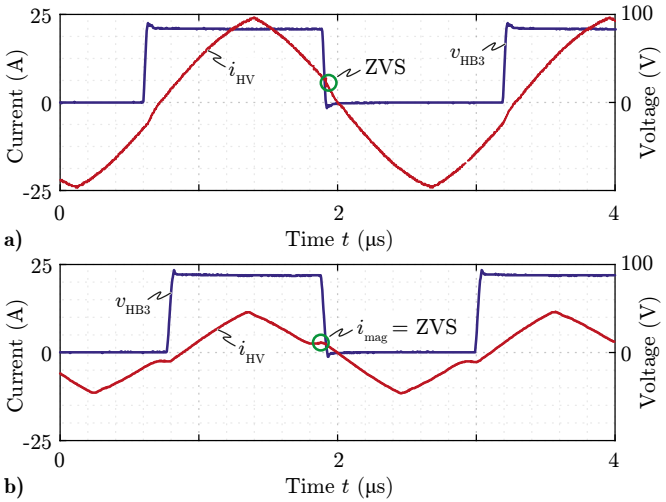


Fig. 5.34: Experimentally measured HV winding currents i_{HV} and switch-node voltages v_{HB3} of the leading HV bridge-leg for **a)** boundary conduction mode (BCM) which is used for large output power values and **b)** discontinuous conduction mode (DCM), where the magnetizing current ensures ZVS of HB_3.

Consequently, even though the converter can easily withstand the thermal stresses due to the low efficiency in DM, the proposed concept of operating mode dependent turns ratios should always be applied in converter systems, where the proposed three-port topology is employed. Hence, even though the PCB costs might be higher due to the additionally required PCB layers, the third HV sub-winding is necessary, as otherwise, it is hardly possible to meet the efficiency requirements in DM.

Nevertheless, with the simple hardware demonstrator of Fig. 5.28 it is shown, that the topology can easily be used for the target application in electric vehicles, especially as there is still quite some room for improvements in terms of power density and efficiency of the hardware implementation.

5.7 Summary of the Chapter

In this chapter, a new three-port DC/DC converter topology for automotive applications has been proposed and analyzed, which can be used to interconnect the DC-link capacitor of an upstream single-phase PFC rectifier with a HV battery and a LV DC-bus. The topology comprises multiple individual series-resonant converters (SRCs), which are coupled by means of one common transformer core. Furthermore, the SRCs are arranged in such a way, that additive and subtractive superposition of magnetic flux linkages can be used, in order to achieve a decoupled power flow control between the different converter ports. For each power path, a simplified equivalent circuit has been derived, based on which an appropriate control of the converter has been developed. It is shown, that ZVS of all power semiconductors can be achieved and that the application of a new concept of operating mode dependent turns ratios of the PCB-winding transformer yields a significant improvement in terms of converter performance. In order to facilitate a possible hardware implementation of the proposed topology, simple design guidelines are given, which can be used to optimize the design for certain given specifications. Finally, the feasibility of the proposed topology has been verified by means of a 1 kW 166 V/166 V/15 V hardware demonstrator, which meets the targeted efficiency of 95 % in CM operation for full-load conditions, but missed the efficiency target in DM operation for partial-load conditions by $\approx 1\,\%$. However, this is not really an issue, as by utilizing the concept of operating mode dependent turns ratios, the efficiency in DM can be significantly improved, whereby the efficiency target could easily be met.

Even though the proposed converter topology has lots of advantages and is perfectly suitable for the target application, the large number of semiconductors might be a reliability issue and could be considered to be too complex for an industrial application. For this reason, a second topology is developed in the next chapter, which minimizes the number of switches of the converter system.

6

Three-Port Series-Resonant DC/DC Converter with a Phase-Shifted Full-Bridge Equivalent Converter Port

Chapter Abstract

In this chapter, a three-port DC/DC converter topology is introduced, which was developed with a special focus on minimizing the number of active power components, as well as simplifying the control of the converter system as far as possible. The converter comprises three individual converter ports, which are all arranged around one common transformer core. In charge mode (CM) operation, two of these converter ports are operated as a conventional series-resonant converter (SRC), whereas the third port behaves like a current source, which can be actively connected/disconnected to/from the third transformer winding. Consequently, an arbitrary amount of power can be extracted from this converter port, without interfering the previously mentioned resonant power transfer. In drive mode (DM) operation, only two converter ports are actively operated and together form a phase-shifted full-bridge equivalent two-port converter. In a first step, the topology is analyzed in detail and a suitable control strategy is proposed. Subsequently, general design guidelines are given and the achievable converter performance is experimentally verified by means of a 3.6 kW 500 V/500 V/15 V hardware demonstrator.

In the previous chapter, a comparably complex converter topology has been introduced, which has lots of advantages in terms of converter operation and is also simple to control, but at the same time also requires a large number of components, which is an issue when it comes to reliability of a converter

system. Thus, from an industry perspective, a converter topology would be desirable, where the number of switches is minimized, such that the overall reliability is improved and the additional costs due to the numerous gate drive circuits and auxiliary supplies can be minimized.
Furthermore, it has been found in Chapter 3 that for PCB-winding inductors, it is extremely difficult to design reasonably power-dense components for small magnetic energies $E_{\mathrm{L}} = L \cdot i_{\mathrm{pk}}^2$ (thus, small inductances and/or low peak currents), as the through-hole via transitions, the clearance between PCB-winding and core, as well as the inter-winding clearance yield a large offset in terms of component volume. Consequently, it is often more reasonable to build one large inductor instead of two small inductors, which are connected in series from a power flow perspective. However, considering the main power flow from the AC mains to the HV port in charge mode (CM) operation, this is exactly the case, as there are usually three different voltage levels in the power path, namely, the AC mains voltage, the DC-link voltage in between the PFC rectifier and the three-port DC/DC converter, and last, the HV battery voltage, which is connected to the HV port of the aforementioned DC/DC converter. As all three voltages are different, there are at least two inductive components required: One between the AC mains and the DC-link capacitor, and a second one between the DC-link capacitor and the HV port, where the inductive components are used to bridge the voltage differences between the two respective voltage levels. Hence, for this power path, there are two inductive components connected in series, even though, according to the previous considerations, a single PCB-winding inductor would be preferable. This is, however, only possible, if two of the three voltage levels are equal, which in this case means that the DC-link voltage needs to follow the HV battery voltage, whereby the inductor between these two voltage levels can be omitted and only the inductor between the AC mains and the DC-link capacitor is required. Of course, this inductor needs to cope with higher peak currents, but at large, the total volume of the PCB-integrated magnetic components is expected to decrease, as will be explained in more detail in Section 6.1.

Besides the conventional approach of using an inductive component to bridge a certain voltage difference within a converter system [51–53], also a capacitor can be used for this purpose, as e.g. in so-called switched capacitor converters (SCCs) [54, 55], or hybrid SCCs, if a voltage regulation is required [56–58]. However, even though capacitors achieve a higher energy density compared to inductors, which makes them the more promising energy storage elements in power-dense applications, the usually large number of

switches needed in SCC topologies in combination with a comparably poor reliability of such systems make them less attractive for automotive applications, where reliability is key for all system components. Consequently, inductors are still widely used in industrial applications in order to ensure the required simplicity and reliability, which is why they were also considered as the more promising energy storage element for the proposed three-port converter topology of this chapter.

The proposed topology uses the above-mentioned concept that discrete inductors are employed only in the PFC stage of the converter, which is why the DC-link voltage needs to be controlled by means of the PFC rectifier, such that it corresponds to the PFC side referred HV battery voltage. Thus, the three-port DC/DC converter solely provides the required galvanic isolation between the PFC rectifier and the HV battery, without the necessity of any further voltage control between the PFC port and the HV port. The corresponding converter topology is introduced and explained in detail in the following section.

6.1 General Converter Operation

The proposed three-port DC/DC converter topology was developed for the specific requirements of a combined EV charger (cf. Chapter 1), thus, it provides galvanic isolation between the HV battery, the LV bus and the DC-link capacitor of an upstream single-phase PFC rectifier, whose output voltage is now actively controlled to follow the PFC side referred HV battery voltage. Furthermore, the main power path in charge mode (CM) operation from the PFC port to the HV port is designed for maximum efficiency, whereas the auxiliary power path in CM from the PFC port to the LV port has been designed in such a way, that the two output power flows are fully decoupled (cf. Chapter 5). The simplified topology is shown in Fig. 6.1 and comprises three individual ports arranged around one common transformer. In CM operation, the PFC-side half-bridge and capacitive voltage divider, together with the HV-side half-bridge and capacitive voltage divider, are operated as a series-resonant converter (SRC), whereby the leakage inductance of the transformer and the two capacitive voltage dividers form the required resonant tank. The third port, which is connected to the LV bus, comprises two inductors, which can actively be connected/disconnected to/from the third transformer winding by means of the four switches LV.xy, $xy \in \{1a, 1b, 2a, 2b\}$. Hence, for $v_{T,LV} > 0$, L_a, LV.1a and LV.1b form a conventional step-down converter with

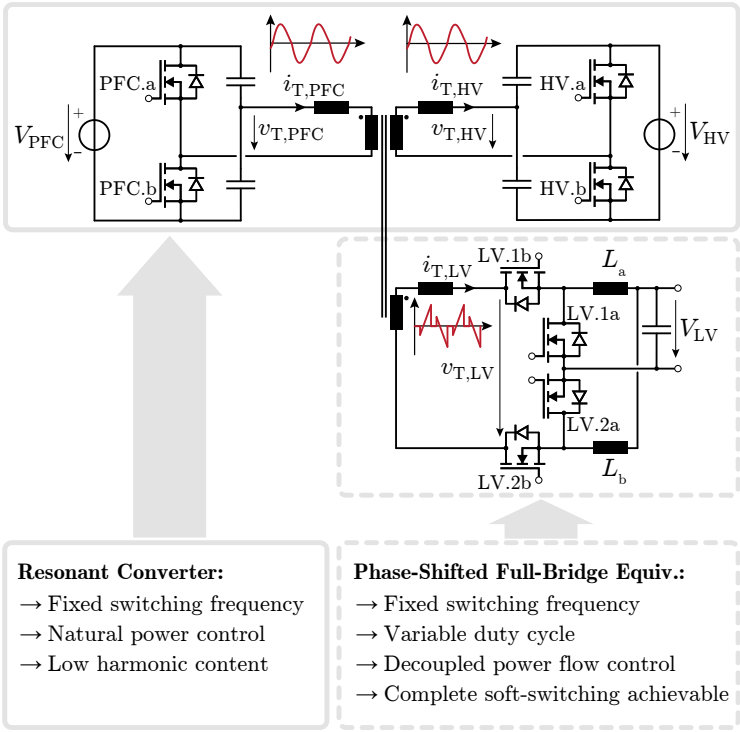


Fig. 6.1: Topology of the proposed three-port DC/DC converter comprising a resonant part for the power flow from the output of an upstream PFC rectifier to the high-voltage battery and a phase-shifted full-bridge equivalent, which controls the power flow to the low-voltage battery of the EV.

an input voltage of $v_{T,LV}$, whereas for $v_{T,LV} < 0$, L_b, LV.2a and LV.2b form a second step-down converter with an input voltage of $-v_{T,LV}$. Consequently, these two step-down converters are inherently interleaved with a phase shift of 180°, due to the 50 % duty cycle of the transformer voltage, which is given by the resonant operation of the SRC.

In the following, the general operation of this converter in the two different modes of operation (charge mode (CM) and drive mode (DM)) are discussed and analyzed.

6.1.1 Charge Mode Operation of the Converter

In a first step, only the SRC part of the converter is investigated, as it is only operated in CM and hardly any control is required. In a second step, the LV port is also taken into account and its control is analyzed in detail.

Operation of the Series-Resonant-Converter Subsystem

As already mentioned, the SRC is only operated in CM, where most of the power flows from the output of the PFC rectifier into the HV battery and only a fraction is flowing from the PFC output to the LV bus. Hence, in this mode, the converter is operated with full power for most of the time, which is why the converter should be designed in such a way, that the power transfer from the PFC to the HV side is as efficient as possible. One of the most efficient topologies for such applications is a so-called DC-transformer [59], hence, a SRC which is operated with a switching frequency close to the resonant frequency of its resonant tank, resulting in a fixed voltage transfer ratio given by the ratio of the numbers of turns of the transformer. Consequently, the currents are all perfectly sinusoidal, whereby both, the high-frequency (HF) conduction losses as well as the EMI filtering effort are minimized. The only drawback of this topology is the fixed voltage transfer ratio, which inevitably leads to the necessity of a variable input voltage of the converter, which has to be adapted according to the required output voltage. In the application at hand, this is not really a drawback, as the whole system anyway comprises two independent stages, where the upstream PFC rectifier is capable of boosting the intermediate DC-link voltage V_{PFC} to arbitrary voltage levels (possibly at the expense of higher required blocking voltages of the employed semiconductors in the PFC rectifier stage).
Furthermore, as previously mentioned, by utilizing the PFC rectifier to indirectly control the output voltage V_{HV} through V_{PFC}, the number of discrete inductive components of the complete converter system can be reduced, which is cost-wise a significant advantage. Hence, compared to conventional two-stage solutions with a fixed DC-link voltage V_{PFC}, where one inductive component is used to bridge the voltage difference between the AC mains voltage and V_{PFC} and another inductive component is used to bridge the difference between V_{PFC} and the output voltage V_{HV} [11], only one, slightly larger inductive component in the PFC rectifier is used, if a DC-transformer stage is employed.
Surprisingly, the inductor in the second stage can be saved with almost no size- or loss-penalty in the inductor of the PFC stage, as the component

stresses of this component solely depend on the input voltage v_{AC} and the input power P_{AC} of the PFC rectifier, if triangular current mode (TCM) operation is used [60]. Thus, the current ripple $i_{\mathrm{AC,pkpk}}$ in the input inductor is directly given by the input power of the converter ($i_{\mathrm{AC,pkpk}}(t) \approx 2\hat{i}_{\mathrm{AC}} \cdot |\sin \omega t|$, $\hat{i}_{\mathrm{AC}} = {}^{2P_{\mathrm{AC}}}/_{\hat{v}_{\mathrm{AC}}}$) and does not depend on the intermediate DC-link voltage V_{PFC}. In contrast to the current ripple, however, the variable switching frequency $f_{\mathrm{sw,PFC}}(t)$ in TCM is affected by the variable output voltage V_{PFC}, according to

$$f_{\mathrm{sw,PFC}}(t) = \frac{\hat{v}_{\mathrm{AC}}}{2L_{\mathrm{PFC}}\hat{i}_{\mathrm{AC}}} - \frac{\hat{v}_{\mathrm{AC}}^2 \cdot |\sin \omega t|}{2L_{\mathrm{PFC}}\hat{i}_{\mathrm{AC}}V_{\mathrm{PFC}}}, \tag{6.1}$$

where $\hat{v}_{\mathrm{AC}}$, $\hat{i}_{\mathrm{AC}}$ and L_{PFC} denote the single-phase input voltage amplitude, the amplitude of the fundamental component of the input current and the inductance of the inductor in the PFC stage, respectively. Thus, the minimum switching frequency $f_{\mathrm{sw,PFC,min}}$ is slightly increasing with the output voltage V_{PFC}, according to

$$f_{\mathrm{sw,PFC,min}}(V_{\mathrm{PFC}}) = \frac{\hat{v}_{\mathrm{AC}}V_{\mathrm{PFC}} - \hat{v}_{\mathrm{AC}}^2}{2L_{\mathrm{PFC}}\hat{i}_{\mathrm{AC}}V_{\mathrm{PFC}}}. \tag{6.2}$$

Nevertheless, as the residual switching losses in TCM are small, the slightly higher average switching frequency does not harm the converter efficiency too much. Consequently, the only significant disadvantage of this approach are higher required breakdown voltages of the semiconductors in the PFC stage due to the variable output voltage V_{PFC}. However, due to the availability of 900 V wide band-gap semiconductor devices with very low on-resistance [61, 62], the single-inductor approach can be used for comparably wide input and output voltage ranges.
Thus, depending on the mains voltage and the required output voltage range, the turns ratio $n = {}^{n_{\mathrm{PFC}}}/_{n_{\mathrm{HV}}}$ of the transformer can be chosen in such a way, that the minimum PFC side referred output voltage $n \cdot \min\{V_{\mathrm{HV}}\}$ is just larger than the peak of the maximum AC input voltage. In the application at hand, the given specifications would require a turns ratio of ≈ 1.5, whereby customized semiconductors on the PFC side of the converter would need to be employed, in order to optimize the performance of the overall converter system. Even though this is common practice in industry, the development and manufacturing of customized semiconductor devices takes relatively long time and is quite expensive, which is why it has been decided to test the performance of the topology with a transformer with a turns ratio of $n = 1$, such that conventional 650 V semiconductor devices can be employed. However, this does

PFC Port Voltage	V_{PFC}	250 V…500 V
HV Port Voltage	V_{HV}	250 V…500 V
LV Port Voltage	V_{LV}	10.5 V…15 V
Output Power (HV Port)	P_{out}	0 W…3.6 kW (max. 12 A)
Output Power (LV Port)	P_{out}	0 W…3 kW (max. 200 A)
CM Efficiency (full-load)	η_{DM}	95 %@V_{HV} = 500 V, V_{LV} = 15 V
DM Efficiency (part-load)	η_{DM}	95 %@V_{HV} = 500 V, V_{LV} = 15 V

Tab. 6.1: Specifications for a hardware demonstrator of the proposed 3.6 kW three-port DC/DC converter.

neither affect the operation of the converter, nor the achievable performance of the system, which is why it has been considered to be a reasonable adaption of the specifications for a hardware demonstrator, which will be introduced at the end of this chapter. Consequently, in the course of this chapter, and without loss of generality, the analysis of the converter topology will be done for the aforementioned turns ratio of $n_{\mathrm{PFC}}/n_{\mathrm{HV}} = 1$ and the specifications of Tab. 6.1.

Another advantage of the DC-transformer is its inherent voltage and power control, whereby only the input voltage V_{PFC} of the converter needs to be regulated to its specified value, independent of the actual output power. This natural power balancing is shown in Fig. 6.2 based on the simulated current and voltage waveforms. As illustrated in Fig. 6.2a, the transformer current $i_{\mathrm{T,PFC}}$ automatically reacts on a load step in the output current I_{HV} of the HV port, by reducing its amplitude within a couple of cycles, before reaching its new stationary value. Due to the equal port voltages V_{PFC} and $n \cdot V_{\mathrm{HV}}$ and the synchronous operation of the PFC and the HV-side half-bridges, the applied voltage-time areas across the leakage inductance of the transformer are extremely small. Consequently, only a small resonant inductance is required, which is a particular advantage in designs with PCB-winding transformers, as the achievable leakage inductance in such transformers is strongly limited [63, 64]. However, compared to conventional wire-wound transformers, PCB-winding transformers are much cheaper to manufacture and at the same time, the vertically aligned arrangement of the transformer windings mitigates the HF conduction losses to a large extent [65, 66]. Consequently, this sort of transformer should be used whenever possible and reasonable from a power density perspective.

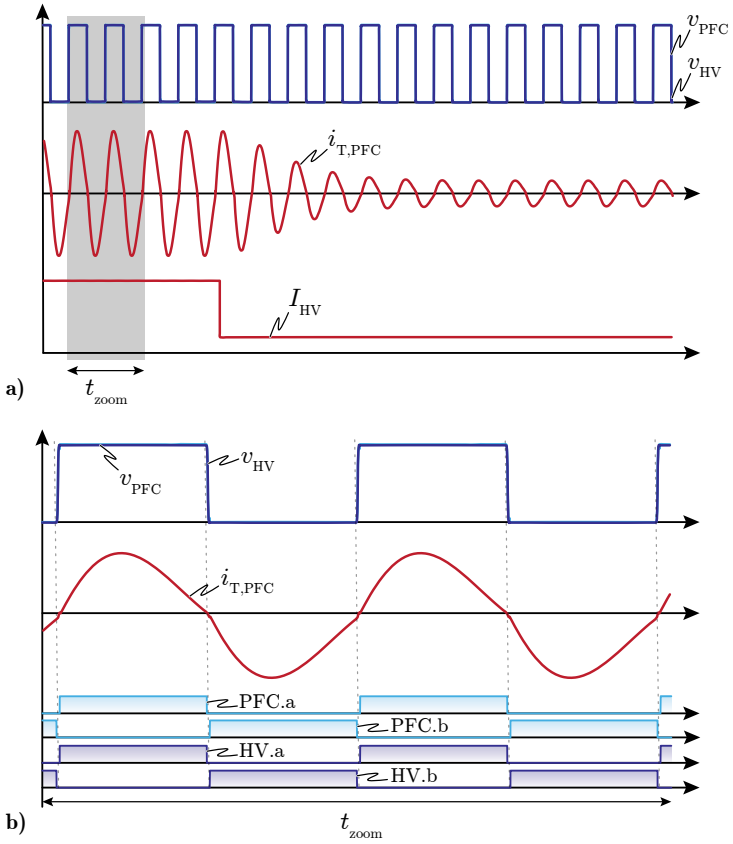


Fig. 6.2: a) Voltage and current waveforms in the SRC part of the converter for a disconnected LV port and a step in the output current I_{HV} of the HV port. **b)** Zoomed-in view of the aforementioned waveforms, including the gate signals of the power switches PFC.a, PFC.b, HV.a and HV.b.

So far, only the power flow from the PFC to the HV port has been considered and the advantages and disadvantages of the selected topology have been highlighted. However, there is also a small power flow from the PFC port to the LV bus required, which is why a third transformer winding is necessary to be able to extract the power for the LV bus directly from the common transformer core. Due to the extremely small leakage inductance in the PCB-winding transformer, the LV-side winding voltage $v_{\mathrm{T,LV}}$ is given by $v_{\mathrm{T,PFC}} \cdot n_{\mathrm{LV}}/n_{\mathrm{PFC}}$ and should not be forced to a different value, as otherwise, the resonant tank for the power flow from the PFC to the HV port would be affected too much and the SRC would not work properly. However, as the LV bus voltage V_{LV} varies between 10.5 V and 15 V, at least one inductive component needs to be employed, which can take the voltage difference between $v_{\mathrm{T,LV}}$ and V_{LV} (cf. Fig. 6.1). Consequently, the PFC and the HV port act as voltage sources, whereas the behavior of the LV port corresponds to a current source due to the aforementioned inductive component. In order to control the power, which is extracted from the LV winding, it is inevitable that the two output inductors L_{a} and L_{b} can be both, actively connected as well as actively disconnected to/from the LV winding. This can be achieved by means of the proposed LV-side circuit, whose simplified control is explained in the following.

Control of the LV Converter Port

The control of the LV port power switches can be divided into two identical time intervals: The first half-period ($0 < t < T/2$), where the LV winding voltage $v_{\mathrm{T,LV}}$ is positive and L_{a} can be applied to the LV winding, and the second half-period ($T/2 < t < T$), where $v_{\mathrm{T,LV}}$ is negative and L_{b} can be applied to the LV winding. Starting with the first half-period and the initial conditions shown in Fig. 6.3a+e, where the two currents in the output inductors L_{a} and L_{b} are circulating through the switches LV.1a and LV.2a, the switch LV.1b is blocking and prevents $v_{\mathrm{T,LV}}$ from being applied to L_{a}. After a certain time t_1, LV.1a is switched off and, due to the negative current i_{LVa} in L_{a}, the C_{oss} of LV.1a is charged until it reaches $v_{\mathrm{T,LV}}$. Subsequently, the body diode of LV.1b starts to conduct, whereby this switch can be turned on under ZVS conditions. From now on, $v_{\mathrm{T,LV}}$ is directly applied to L_{a} and the current in this inductor starts to increase again (cf. Fig. 6.3b). At $t = T/2$, the PFC-side and HV-side half-bridges are switched and $v_{\mathrm{T,LV}}$ becomes negative. Consequently, as $v_{\mathrm{T,LV}} < 0$, the current i_{LVa} commutates back to the body diode of LV.1a, whereby this switch can be turned on under ZVS conditions as well. During the second half-period, i_{La} continues to circulate through LV.1a, which is why

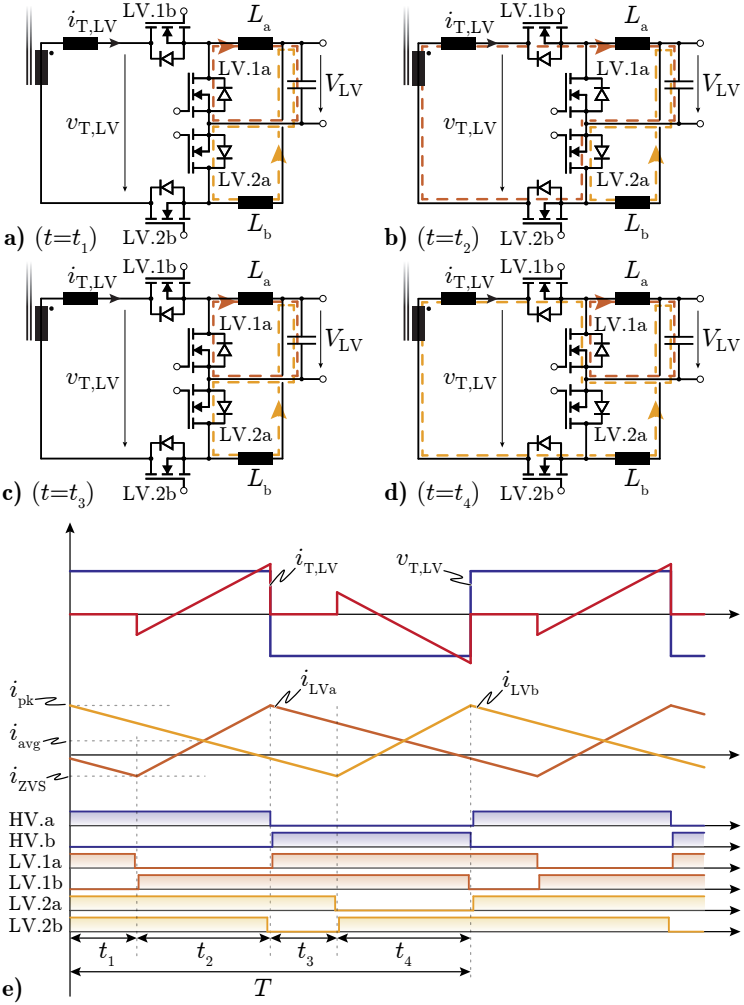


Fig. 6.3: a)-d) Current paths in the LV port during the time intervals $t = t_1, ..., t_4$, and **e)** the voltage and current waveforms in the LV port including the gate drive signals of all power switches.

the active period t_2, where the current in L_a is increasing, cannot exceed a value of $T/2$. If L_a, LV.1a and LV.1b are considered as a conventional step-down converter, this statement is equivalent to allowing a maximum duty cycle D_{LV} of 50 %. Hence, according to the well known formula for buck converters

$$\frac{V_{out}}{V_{in}} = \frac{V_{LV}}{|v_{T,LV}|} = D < 0.5, \tag{6.3}$$

the minimum winding voltage $|v_{T,LV}|$ needs to be larger than twice the maximum LV bus voltage V_{LV} in order to keep the required duty cycle below 50 %. This limit sets the following constraint for the numbers of turns of the transformer windings

$$\frac{2 \cdot n_{HV} \cdot \max\{V_{LV}\}}{n_{LV} \cdot \min\{V_{HV}\}} < 0.5. \tag{6.4}$$

During the second half-period, where $v_{T,LV}$ is negative, the second step-down converter (L_b, LV.2a and LV.2b) is controlled exactly the same way as previously explained for L_a, LV.1a and LV.1b. Hence, the only difference between the two sub-converter modules is, that their active periods are phase shifted by 180°.

Obviously, ZVS of LV.1b and LV.2b is only achieved, if the currents in the respective output inductors are negative before the switches are turned on. However, as the switching frequency f_{sw} in CM is given by the resonant frequency of the resonant tank between the PFC and the HV port, and the duty cycle D_{LV} is defined by (6.3), there is no degree of freedom left, which would allow to control the current ripple in L_a and L_b during operation. Consequently, the current ripple can only be influenced during the design phase of the converter by an appropriate selection of the inductance value of L_a and L_b. The inductance should be selected in such a way, that ZVS for at least the maximum LV output power during CM (300 W in this application) is guaranteed. However, a too small inductance results in a large current ripple and in unnecessary conduction losses in the LV port, as this ripple current flows even for zero LV output power. This behavior is illustrated in Fig. 6.3e, where the triangular currents i_{LVa} and i_{LVb} fluctuate around their average value i_{avg} with a constant ripple of $2 \cdot (i_{pk} - i_{avg})$, even if i_{avg} and therefore the LV output current I_{LV} are set to zero. Fortunately, this ripple current has a beneficial effect on the overall converter operation, as it assists the ZVS operation of the PFC and the HV-side power semiconductors, as will be explained later in this chapter.

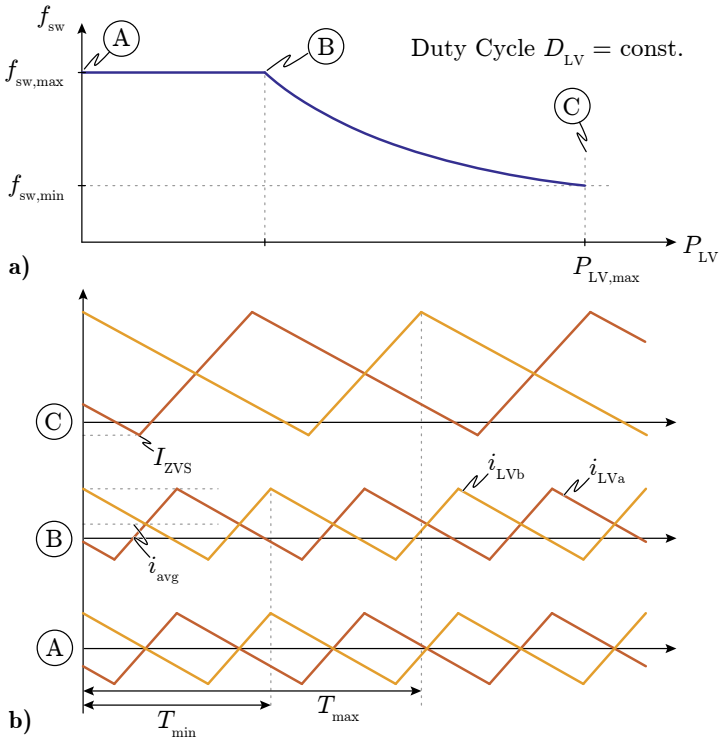


Fig. 6.4: a) Switching frequency variation in drive mode (DM) for a constant output voltage V_{LV} and a varying output power P_{LV} and **b)** the current waveforms for three exemplary output power levels Ⓐ, Ⓑ and Ⓒ.

6.1.2 Drive Mode Operation of the Converter

In contrast to the charge mode (CM), there is no power flow in the PFC port of the converter in drive mode (DM) operation, which is why the SRC is not operated anymore. Instead, the HV port now actively applies a rectangular voltage $v_{T,HV}$ to the transformer, as the power for the LV bus is now drawn from the HV battery. Consequently, the operating conditions for the LV port do not change compared to the previously introduced CM operation, as there is again a rectangular voltage $v_{T,LV}$ induced in the LV winding. However, there is one important difference between the CM and the DM, as in DM, there is no resonant power transfer required and the constraint of a fixed switching

frequency can therefore be loosened. Thus, the previously mentioned negative inductor currents $i_{\mathrm{LVx}} = -I_{\mathrm{ZVS}}, x \in \{\mathrm{a}, \mathrm{b}\}$ during the switching transitions can now also be ensured for LV output power values larger than 300 W, as the switching frequency f_{sw} can be reduced, whereby the current ripple is inherently increased. Hence, the converter is controlled by means of a variable switching frequency f_{sw} and a duty cycle D_{LV} according to (6.3), as usually referred to as triangular current mode (TCM) operation [60, 67] (cf. Fig. 6.4). The optimum switching frequency f_{sw} can be calculated based on the momentary output current I_{LV} and the required ZVS current I_{ZVS}, according to

$$f_{\mathrm{sw}} = \min \left\{ f_{\mathrm{sw,max}}, \frac{V_{\mathrm{LV}} \cdot \left(|v_{\mathrm{T,LV}}| - V_{\mathrm{LV}} \right)}{|v_{\mathrm{T,LV}}| \cdot L_{\mathrm{a}} \cdot \left(I_{\mathrm{LV}} + 2 I_{\mathrm{ZVS}} \right)} \right\}, \tag{6.5}$$

with

$$|v_{\mathrm{T,LV}}| = V_{\mathrm{HV}} \cdot \frac{n_{\mathrm{LV}}}{n_{\mathrm{HV}}}. \tag{6.6}$$

The upper limit for the switching frequency is selected as the resonant frequency f_{res} of the resonant tank between the PFC rectifier output and the HV port, in order to limit the remaining switching losses during the dead times of the power switches and to avoid possible timing issues due to a limited PWM resolution of the control hardware. Nevertheless, this limit could of course also be increased if reasonable from an efficiency perspective.

So far, most of the components in the converter have been assumed to be ideal. However, in a real application, all the non-idealities of the components, as e.g. the C_{oss} of the power switches, the parasitic inductances of all power tracks, etc. need to be considered as well. This is done in the following section and their impact on the converter operation is investigated in detail.

6.1.3 Impact of the Parasitic Components on the Converter Control

The current source behavior of the LV port, which can be connected/disconnected to/from the LV transformer winding, inevitably results in a problematic situation during the switching transitions, as the small, but still existing, leakage inductance of the LV transformer winding prevents current steps in $i_{\mathrm{T,LV}}$. Hence, if L_{b} is connected to the LV winding with a non-zero current i_{LVb}, $i_{\mathrm{T,LV}}$ would need to take over the momentary value of i_{LVb} instantaneously. However, this would require an infinite voltage $v_{\mathrm{T,LV}}$ across the LV transformer winding, which would result in a voltage breakdown of LV.2a. Consequently,

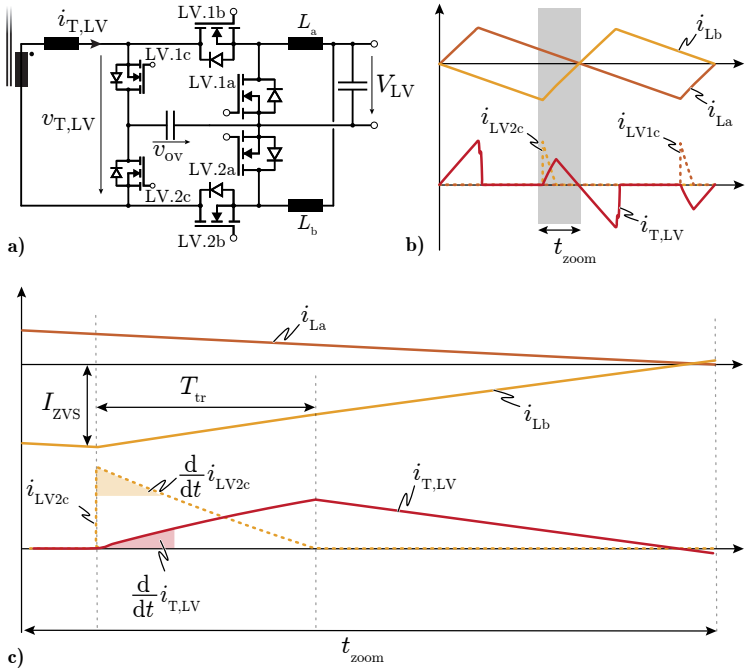


Fig. 6.5: a) Additional overvoltage protection circuit comprising the two small MOSFETs LV.1c and LV.2c, as well as the capacitor C_{ov} across which v_{ov} is applied. **b)** LV-side current waveforms during one switching period and **c)** zoomed-in view of the same waveforms during a switching transition, where i_{Lb} is assumed to be impressed for simplicity reasons.

an additional small overvoltage circuitry is required, which acts as an energy buffer for the time T_{tr} required to equalize the two currents i_{LVb} and $i_{\mathrm{T,LV}}$ (cf. Fig. 6.5).
As shown in Fig. 6.5c, the current in the LV winding $i_{\mathrm{T,LV}}$ starts at zero and should ideally immediately take over the current I_{ZVS} impressed in L_{b} at the beginning of the switching transient. However, the gradient of the current rise of $i_{\mathrm{T,LV}}$ is given by

$$\frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{T,LV}} = \frac{v_{\mathrm{ov}} - n_{\mathrm{LV}}/n_{\mathrm{HV}} \cdot v_{\mathrm{T,HV}}}{L_{\sigma,\mathrm{eff,LV}}}, \tag{6.7}$$

with

$$L_{\sigma,\mathrm{eff,LV}} = L_{\sigma,\mathrm{LV}} + \frac{L_{\sigma,\mathrm{PFC}} L_{\sigma,\mathrm{HV}}}{L_{\sigma,\mathrm{PFC}} + L_{\sigma,\mathrm{HV}}}, \tag{6.8}$$

where $L_{\sigma,\mathrm{X}}$ denote the leakage inductance values of the respective transformer windings. Consequently, $i_{\mathrm{T,LV}}$ cannot take over $i_{\mathrm{LV,b}}$ immediately, as the capacitor voltage v_{ov} cannot be higher than the breakdown voltage of the LV power semiconductors. As a result, a current $i_{\mathrm{LV,2c}}$ starts to flow in order to compensate for the difference between the two currents $i_{\mathrm{T,LV}}$ and i_{LVb}. As soon as $i_{\mathrm{T,LV}}$ is equal to i_{LVb}, $i_{\mathrm{LV,2c}}$ is zero and the transition is completed. The time T_{tr}, which is required for this transition, depends on the initial negative current I_{ZVS} and can be calculated according to

$$T_{\mathrm{tr}} = \frac{|I_{\mathrm{ZVS}}| L_{\sigma,\mathrm{eff,LV}} L_{\mathrm{b}}}{L_{\mathrm{b}} \left(v_{\mathrm{ov}} - n_{\mathrm{LV}}/n_{\mathrm{HV}} \cdot v_{\mathrm{T,HV}}\right) + L_{\sigma,\mathrm{eff,LV}} (v_{\mathrm{ov}} - V_{\mathrm{LV}})}. \tag{6.9}$$

Hence, the total charge Q_{ov} which is flowing into the capacitance C_{ov} within one switching period is given by

$$Q_{\mathrm{ov}} = 2 \cdot \left(\frac{1}{2} |I_{\mathrm{ZVS}}| T_{\mathrm{tr}} \right). \tag{6.10}$$

In order to achieve a stable v_{ov} and, therefore, a stable charge balance in C_{ov}, the auxiliary switches LV.1c and LV.2c need to be actively connected to the transformer at some point in time, such that the same amount of charge is extracted, as otherwise, v_{ov} would continuously be increasing. The obvious solution would be to turn on LV.1c and LV2.c, whenever there is current flowing through their body diode, as this results in ZVS and, therefore, the most efficient operation of these switches. By keeping them turned on for a certain amount of time, the charge, which was injected due to the aforementioned current difference $i_{\mathrm{T,LV}} - i_{\mathrm{LVb}}$, is then fed back to the PFC and

the HV port by means of a resonant transition between C_{ov}, $L_{\sigma,eff,LV}$ and the capacitive voltage dividers of the PFC and the HV port. However, due to the small leakage inductance within the transformer, this yields very high peak currents in the auxiliary switches and at the same time unnecessary conduction losses in various components, as there is no advantage which could be taken from this reactive power flow.
Fortunately, the E_{oss} of these auxiliary switches is comparably small, whereby zero-current-switching (ZCS) operation of these semiconductors does not harm the efficiency of the converter too much. Thus, the capacitor C_{ov} can be connected to the transformer winding whenever required and reasonable. Keeping in mind, that the charge in C_{ov} can only be transferred to the PFC and the HV port, as the leakage inductance values of the transformer are much smaller than the output inductors L_a and L_b, the only reasonable point in time to transfer this energy is during the switching transitions of the two aforementioned ports, as this additional energy supports the ZVS operation of the PFC and the HV-side power semiconductors (cf. Fig. 6.6).
For simplicity reasons, the ZVS transition is explained in the following for DM operation only, as in CM operation, the principle stays the same and the waveforms look similar.

Starting with the initial condition shown in Fig. 6.6c at $t = t_0$, the switching transition is initiated by turning off HV.a, whereby the inductor current i_{La} starts to discharge the parallel connected C_{oss} of HV.a, HV.b and LV.1a, as $i_{T,LV}$ approximately follows i_{La}. Consequently, $v_{T,HV}$ and $v_{T,LV}$ drop synchronously until $v_{T,LV}$ reaches 0 V. At this point ($t = t_1$), the body diode of LV.1a starts to conduct and the inductor current i_{La} commutates to LV.1a. Hence, due to $v_{T,HV} = v'_{T,LV}$, the HV-side switch-node voltage equals $V_{HV}/2$, which is why only partial ZVS would be achieved. However, there is still magnetic energy stored in the leakage inductance of the transformer, which now starts to further charge/discharge the C_{oss} of the HV-side half-bridge until $i_{T,LV} = 0$ A. Thus, the larger the initial current $i_{T,LV}(t_1)$ is, the more likely a full charge/discharge of the HV-side C_{oss} is achieved. Unfortunately, at $t = t_2$, the voltages across the HV and the LV transformer windings are different, as $v_{T,LV}$ is still zero, but $v_{T,HV}$ is somewhere in between 0 V and $-V_{HV}/2$. This voltage difference initiates a resonant current through the leakage inductance of the transformer between the C_{oss} of the HV port and the C_{oss} of LV.2b, which cannot be avoided and again increases $v_{T,HV}$ (for $t_2 < t < t_3$). Hence, it is impossible to ensure full ZVS with the magnetic energy only. At this point, the excess charge in C_{ov} comes into play, as LV.2c can be switched

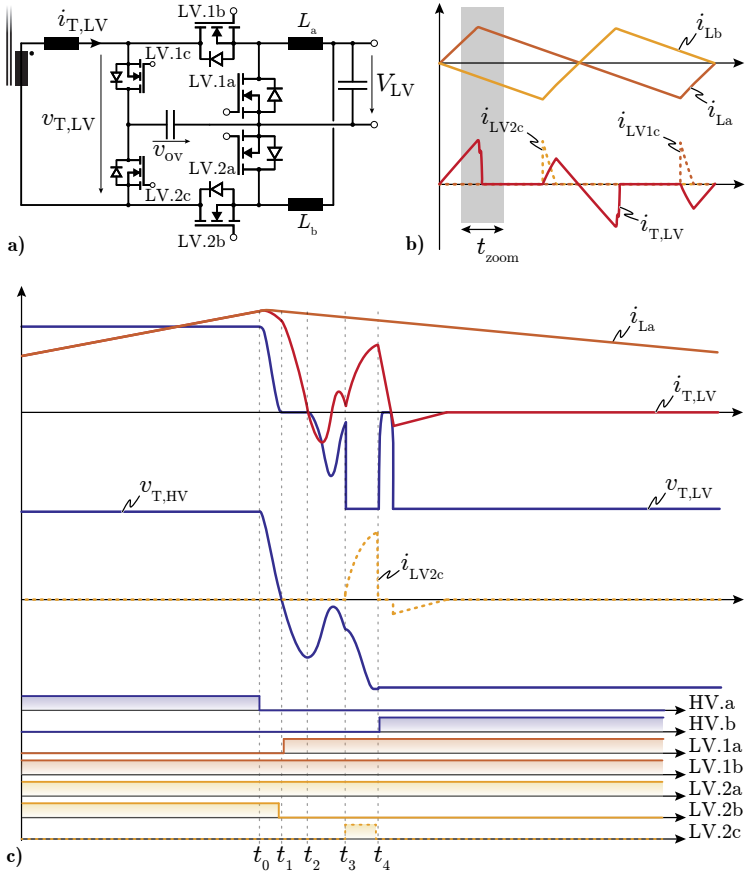


Fig. 6.6: Simplified drawing of the voltage and current waveforms during one ZVS transition including the currents in the overvoltage protection circuit (LV.1c, LV.2c and C_{ov}).

on in order to complete the HV-side ZVS transition by generating an additional positive current pulse in $i_{T,LV}$, which charges/discharges the C_{oss} of the HV-side half-bridge completely (cf. $t = t_3$). However, this comes at the expense of additional switching losses in the LV port, as the C_{oss} of LV.2b needs to be charged instantaneously from worst case 0 V to v_{ov} through LV.1c. Nevertheless, the additional losses due to the comparably small Q_{oss} of the LV power switches are still significantly lower than the switching losses, which would originate from incomplete ZVS of the HV power semiconductors.
After a certain on-time $t_{on} = t_4 - t_3$, the switch LV.2c is switched off again in order to minimize the RMS current stress in this component and to interrupt the discharging of C_{ov}. The actual length of the on-time t_{on} is controlled in such a way, that the voltage v_{ov} always stays below the breakdown voltage of the LV power semiconductors, including a certain safety margin.
Furthermore, from an efficiency point of view, the time interval from t_2 to t_3 should be as short as possible, as the resonant current during this time interval serves no purpose and solely increases the conduction losses and extends the total dead time. However, a certain delay $t_{delay} = t_3 - t_0$ is required, such that even for the maximum LV output currents, $i_{T,LV}$ drops to zero before switching on LV.2c. This is important, as otherwise the small auxiliary switches LV.1c and LV.2c might need to take over the huge transformer currents during the switching transitions, which can easily go up to 200 A. Consequently, the control effort can be minimized by keeping a constant t_{delay}, independent of the operating conditions, whereby ZVS of the PFC and HV semiconductors is guaranteed over the whole operating range. The optimal value of t_{delay} highly depends on the parasitics of the transformer design, the employed power semiconductors and the output inductors and is found easiest by means of simulation or experimental measurements.

Using this control strategy, the voltage and current waveforms in all the components can be calculated and/or simulated and the converter system can be designed accordingly. An exemplary design of such a converter is discussed in the following based on the specifications listed in Tab. 6.1.

6.2 Design of the Three-Port Converter System

The design of the converter can be divided into three main stages, which highly depend on each other: First, the selection of the power semiconductors, second, the design of the three-winding transformer and third, the LV output inductors. Especially the design of the magnetic components has a significant

impact on the current waveforms and, therefore, the occurring conduction losses of the complete converter system. Consequently, the optimization of the overall converter is an iterative process with multiple sweep variables, as e.g. resonant frequency f_{res}, the output inductance $L_x \in \{a, b\}$ and the ratio between the resonant inductance and the resonant capacitor.

6.2.1 Selection of the Power Semiconductors

Starting with the selection of the power semiconductors for the PFC and the HV port, switches are required which feature a low on-state resistance $R_{ds,on}$ for minimal conduction losses, as well as an as small as possible C_{oss} in order to reduce the ZVS effort.
Considering the maximum DC-link voltage of 500 V in both ports, a minimum required breakdown voltage of $V_{ds,max} = 600\,V$ is defined, in order to be able to make a pre-selection of appropriate power semiconductors. The most promising candidates are summarized in Fig. 6.7a, where the $R_{ds,on}$ vs. C_{oss} performances are shown. These switches were finally considered in the optimization to find the most suitable PFC/HV power semiconductors.

The selection of the power switches for the LV side depends not only on the output power, but also on the turns ratio n of the transformer, which directly defines the required minimum breakdown voltage of the switches LV.xy, $xy \in \{1a, 1b, 2a, 2b\}$. In order to minimize the required total semiconductor chip area, an as low as possible breakdown voltage should be targeted, as the $R_{ds,on}$ of conventional silicon MOSFETs usually scales with the breakdown voltage to the power of > 2.0 [68]. However, the previously mentioned limitation of $D_{LV} \leq 50\,\%$ yields a lower limit for the minimum $v_{T,LV,min}(V_{HV} = 250\,V) = 30\,V$ according to (6.3). Hence, the maximum PFC/HV port voltage of 500 V results in a $v_{T,LV,max}$ of 60 V, which is at the same time the minimum required breakdown voltage of the LV switches. Similar to the PFC/HV semiconductors, as small as possible $R_{ds,on}$ and C_{oss} values are in demand for minimizing the conduction and the switching losses in these components. Again, the most promising candidates are summarized in Fig. 6.7b, which were considered in the final converter optimization. In order to reasonably estimate the occurring conduction losses in the semiconductors in the aforementioned optimization, a thermal model needs to be used, which considers the thermal resistance of the package of the switch, the thermal vias in the PCB, as well as the isolating thermal interface material between the PCB and the heat sink (cf. Fig. 6.8). Based on this idealized model, the junction temperatures T_j of

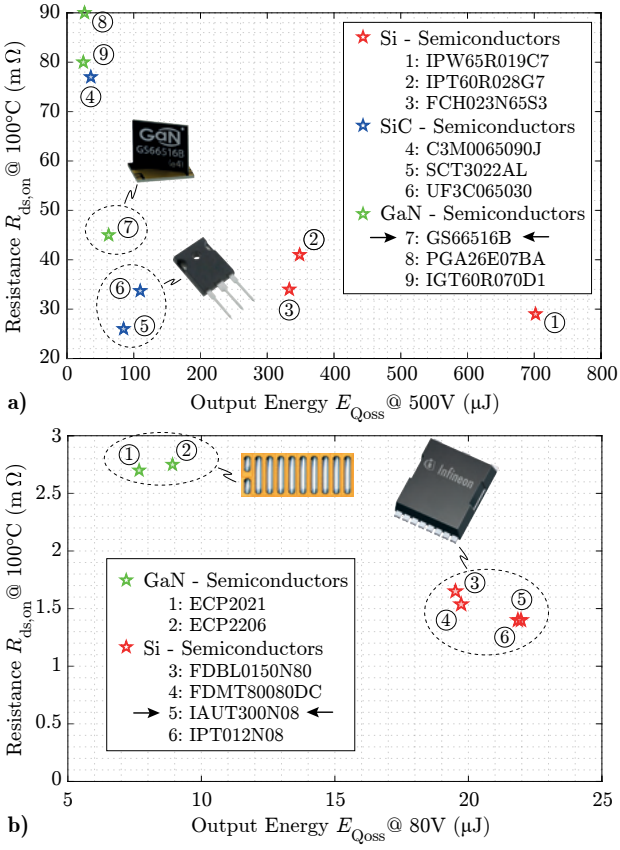


Fig. 6.7: a) Most promising candidates for the semiconductors of the PFC and the HV port and **b)** the same graph for the LV power semiconductors.

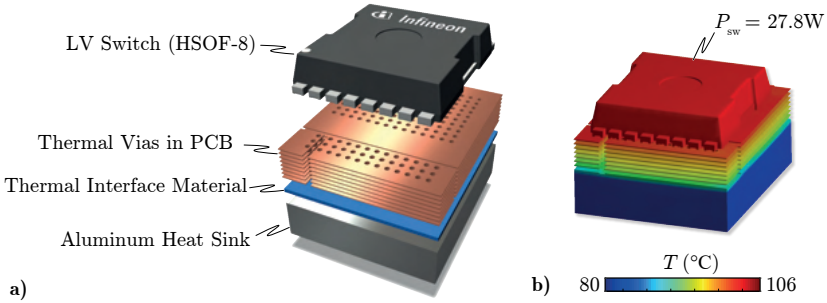


Fig. 6.8: a) Thermal path of the cooling system for exemplary LV-side semiconductors, comprising the thermal vias in the PCB, one layer of 0.5 mm thick thermal interface material with a thermal conductivity of 5 W/(m K) and the aluminum heat sink. **b)** Thermal FEM simulation of the cooling system for 27.8 W of losses and a coolant temperature of 80 °C.

the semiconductors can be estimated and the expected $R_{\mathrm{ds,on}}(T_{\mathrm{j}})$ can be used for a more accurate prediction of the converter efficiency.

6.2.2 Design of the Output Inductors

The design of the two output inductors depends on the resonant frequency f_{res} and the desired LV current ripple $\Delta i_{\mathrm{Lx,pp}}(f_{\mathrm{res}})$ in charge mode (CM) operation. The selection of $\Delta i_{\mathrm{Lx,pp}}$ inherently limits the maximum transferable power P_{lim} from the PFC to the LV port, for which ZVS operation of all power semiconductors can be maintained (cf. Section 6.1.1). Thus, P_{lim} should be at least 300 W in this application, as this power is defined in the specifications as maximum LV output power in CM. However, the smaller the selected current ripple $\Delta i_{\mathrm{Lx,pp}}(f_{\mathrm{res}})$ is, the wider the required switching frequency range in drive mode (DM) gets (cf. Fig. 6.4). A wide switching frequency range, in turn, makes it more difficult to design an efficient and power-dense transformer, as will be discussed in the next section about the optimal design of the transformer. For this reason, P_{lim}, or equivalently $L_{\mathrm{x}}, x \in \{\mathrm{a}, \mathrm{b}\}$, is considered as a degree of freedom in the overall converter optimization and for each L_{x} a separate inductor optimization is conducted.

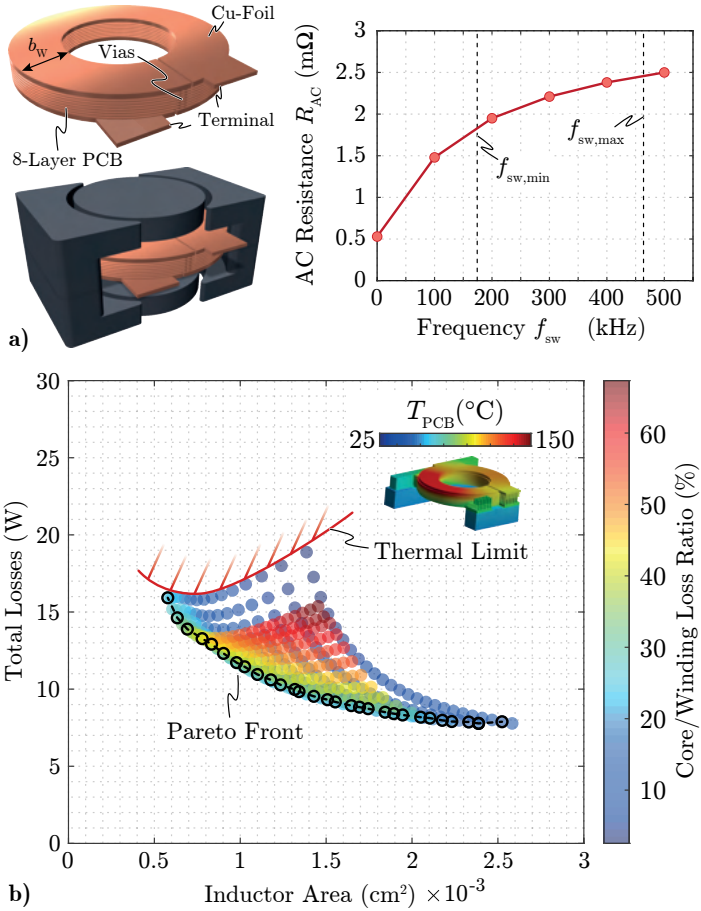


Fig. 6.9: a) PCB-winding inductor design with $L_x = 250\,\text{nH}$ and the FEM-simulated winding resistance. **b)** Pareto-optimization of a PCB-winding inductor with $L = 250\,\text{nH}$ and $f_{res} = 470\,\text{kHz}$, for varying winding widths b_W, core cross-sections A_C and numbers of turns N_L. The most suitable inductor design is finally selected from the Pareto front.

Based on f_{res} and L_x, the maximum current stresses for the inductor design can be calculated according to

$$\begin{aligned} I_{Lx,pk} &= I_{LV,max} + I_{ZVS}, \\ I_{Lx,DC} &= \frac{I_{LV,max}}{2} \\ I_{Lx,AC,rms} &= \frac{I_{LV,max}}{\sqrt{3}}, \end{aligned} \tag{6.11}$$

where $I_{Lx,DC}$ and $I_{Lx,AC,rms}$ denote the maximum DC current and the maximum total RMS current in the inductor, respectively. Hence, assuming a frequency independent resistance of the inductor winding, 75 % of the occurring conduction losses originate due to the DC component of the inductor current, according to

$$\frac{P_{DC}}{P_{total}} \propto \frac{I_{Lx,DC}^2}{I_{Lx,AC,rms}^2} = \frac{3}{4}. \tag{6.12}$$

Consequently, an as small as possible DC resistance of the winding is inevitable for an efficient converter operation. As previously mentioned, due to cost reasons, all the magnetic components should be designed with PCB-integrated windings, as by doing so, the expensive wire-wrapping process is omitted. However, the available copper in PCB-windings is strongly limited, which is why the easiest way to achieve a low DC resistance, and at the same time a reasonable power density, is to solder additional copper foils to the top and the bottom layer of the PCB (cf. Fig. 6.9a). Unfortunately, large copper planes in PCBs are prone to high-frequency (HF) effects, as e.g. skin and proximity losses, which is why the inductor is designed according to the optimization described in Chapter 3, where the HF effects are effectively mitigated by means of the fringing field around the air gap. Consequently, for each f_{res} and L_x, the performances of a large number of inductor designs with different winding widths b_W, core cross-sections A_C and numbers of turns N_L are calculated and compared to each other (cf. Fig. 6.9b). Finally, the most suitable inductor design is selected from the so-called Pareto front.

6.2.3 Three-Winding Transformer

To start the design of the transformer, the turns ratio needs to be known. Due to the large currents in the LV winding, only a single turn should be used in order to minimize the aoccurring conduction losses. Consequently, the

number of turns of the PFC and the HV winding can be calculated according to the specifications of Tab. 6.1 and the duty cycle limit given by (6.3) to be

$$n_{\mathrm{PFC}} = n_{\mathrm{HV}} = \left\lfloor n_{\mathrm{LV}} \cdot \frac{\min\{V_{\mathrm{HV}}\} \cdot D_{\mathrm{LV}}}{2 \cdot \max\{V_{\mathrm{LV}}\}} \right\rfloor = 4. \tag{6.13}$$

Based on the number of turns and a certain output inductance L_{x}, the minimum switching frequency $f_{\mathrm{sw,min}}$ in DM can be calculated according to

$$f_{\mathrm{sw,min}} = \frac{V_{\mathrm{LV,min}}(V_{\mathrm{HV,max}} - 2V_{\mathrm{LV,min}} n_{\mathrm{HV}})}{V_{\mathrm{HV,max}} L_{\mathrm{x}} (I_{\mathrm{LV,max}} + 2I_{\mathrm{ZVS}})}, \tag{6.14}$$

whereby the maximum flux linkage in the transformer core is inherently given by

$$\Psi_{\mathrm{max}} = \frac{V_{\mathrm{HV,max}}}{4 \cdot f_{\mathrm{sw,min}}}. \tag{6.15}$$

The maximum flux linkage Ψ_{max}, together with the saturation flux density B_{sat} of a certain ferrite material, then yields a lower limit for the required core cross-section A_{C}. However, due to the wide switching frequency variation in DM, it is essential to select an appropriate core material, which performs well for both, high switching frequencies and low flux densities in CM, as well as low frequencies and high flux densities in DM. Ferroxcubes 3C98 has been found to be the most suitable ferrite material for this application, as it shows a comparably flat loss density $p_{\mathrm{C}}(f_{\mathrm{sw}})$ throughout the whole switching frequency range, if the flux density varies inversely proportional to the frequency, according to $B_{\mathrm{C}} \cdot f_{\mathrm{sw}} = \text{const.}$ (cf. Fig. 6.10). This is equivalent to a Steinmetz parameter ratio of $\alpha/\beta \approx 1$.

Similarly to the LV output inductors, a Pareto optimization can now be conducted based on the derived turns ratio n and the selected core material 3C98 for variable winding widths b_{W}, core cross-sections A_{C} and different winding layer arrangements.
However, in order to maximize the achievable leakage inductance between the PFC and the HV winding, which is required for the resonant tank in CM, the turns of these two windings should be separated as far as possible [63] (cf. Appendix C). Furthermore, the large currents in the LV winding demand for an extremely low winding resistance, which is why the available copper of a single PCB layer is not sufficient. Consequently, the top layer of the PCB has to be used as LV winding, as it can be vertically extended by means of an additional copper foil which is soldered to it (cf. layer stack-up in Fig. 6.11a).

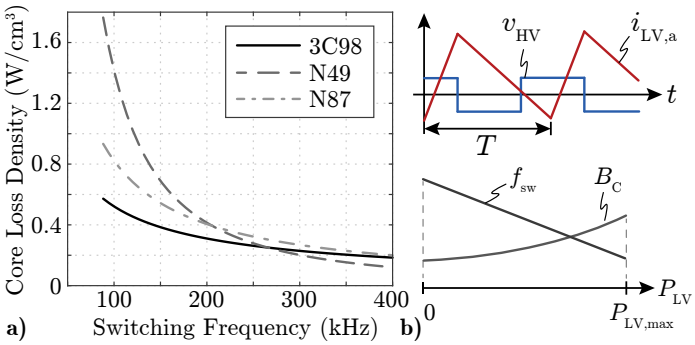


Fig. 6.10: a) Core loss densities of three different materials for a frequency dependent flux density B_C as shown in **b)**, where the switching frequency f_{sw} and the flux density B_C variation for different LV output power values is illustrated.

The remaining layers can therefore be used for the PFC and the HV winding as shown in Fig. 6.11a. The shielding layer between the PFC and the HV winding does not carry any current and is solely used to assist the cooling of the PCB-winding by extracting the heat out of the transformer. As shown in Fig. 6.11c, the proposed vertically aligned arrangement of the PCB-windings effectively mitigates the HF effects, whereby extremely low AC to DC resistance ratios result. Consequently, this arrangement was considered as the most promising solution and has been used in the overall optimization.

The leakage inductance values of a specific transformer design can be calculated as introduced in [64] and inherently define the required resonant capacitance C_{res} according to

$$C_{res} = \left(\frac{1}{2\pi f_{res}}\right)^2 \cdot \frac{1}{L_{\sigma,PFC\rightarrow HV}}, \tag{6.16}$$

where $L_{\sigma,PFC\rightarrow HV}$ denotes the total leakage inductance between the PFC and the HV winding.
Hence, the derived transformer model, the inductor optimization as well as the semiconductor pre-selection can now be used for the Pareto optimization of the overall converter system. Thus, for different P_{lim}, and therefore L_x, the occurring losses in the magnetic components, as well as the losses in the power semiconductors can be derived and are then set in relation to the total required PCB area of the transformer, which is by far the largest power

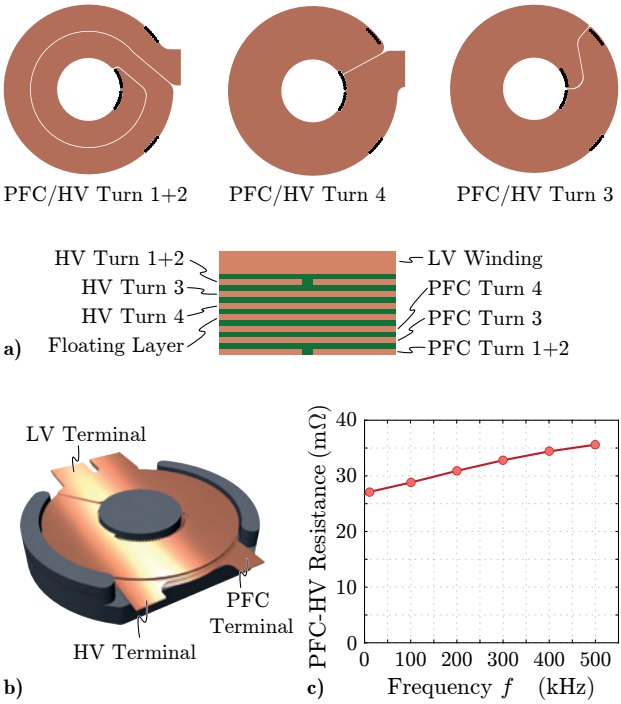


Fig. 6.11: a) Layer stack-up and the design of the eight layer PCB-winding and **b)** the corresponding 3D model. **c)** The FEM-simulated frequency dependent total winding resistance of the PFC and the HV winding (sum of the two).

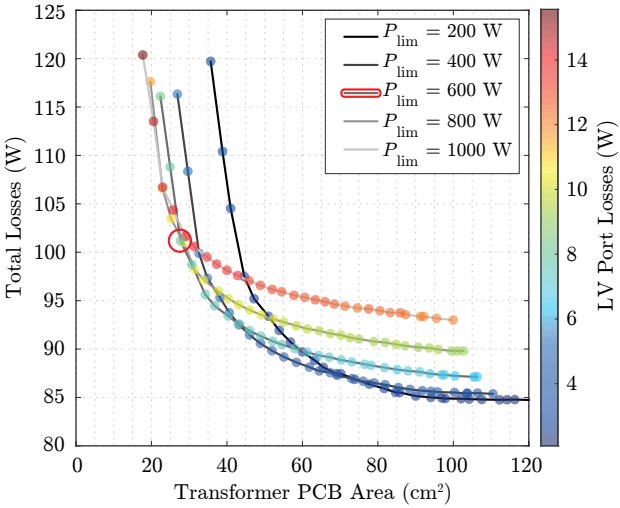


Fig. 6.12: Calculated Pareto fronts for different P_{lim}, a power flow of 3.6 kW from the PFC to the HV port and 0 W from the PFC to the LV port. Hence, only the ripple current is flowing in the LV port. The colors of the dots indicate the amount of losses, which are induced in the LV port due to these circulating currents.

component of the converter and therefore a good measure to estimate the power density of the overall converter system.

The results are shown in Fig. 6.12 for full power operation in CM, hence a power flow of 3.6 kW from the PFC to the HV port and zero power from the PFC to the LV port. Thus, only the current ripple $\Delta i_{\mathrm{Lx,pp}}$ with 0 A offset is circulating in the LV port, which ensures the necessary ZVS of the PFC and the HV-side power semiconductors. The additional conduction losses due to this circulating current in the LV port are indicated by means of the colors of the different converter designs, whereby these losses are an optimistic estimate, as for simplicity reasons, only the losses in the main power components, but not in the connecting PCB tracks in between these components are considered. In the same figure, the red circle specifies the converter design, which has finally been selected for hardware implementation, in order to experimentally verify the performance and the suitability of the proposed topology. The estimated efficiencies of the selected converter design are summarized in Fig. 6.13 and Fig. 6.14 for full-load operation in CM (cf. Fig. 6.13),

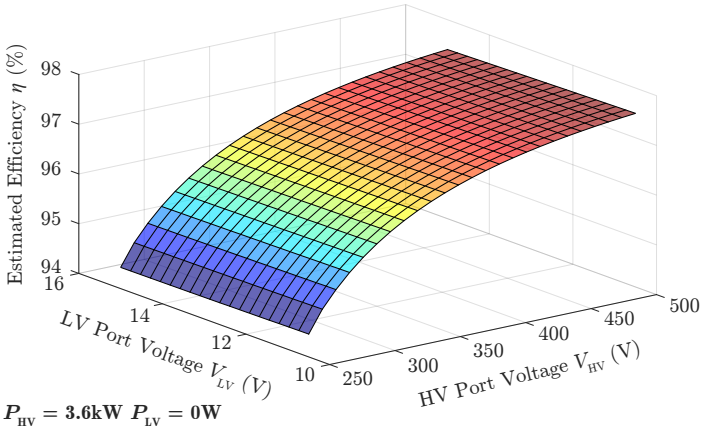


Fig. 6.13: Calculated efficiencies of the selected converter design for an output power of $P_{\mathrm{HV}} = 3.6\,\mathrm{kW}$ and $P_{\mathrm{LV}} = 0\,\mathrm{W}$ in charge mode (CM) operation.

partial-load operation in DM (cf. Fig. 6.14a) and full-load operation in DM (cf. Fig. 6.14b). In DM especially the partial-load efficiency is of importance, as the converter is operated most of the time with a partial load of 30 %-50 %. In contrast, an as high as possible full-load efficiency in CM is required, as during the charging process, the converter is operated at full load almost all the time. However, as already mentioned, these efficiencies are a very optimistic estimate, as in the real hardware prototype, the very high LV port currents do not only flow through the LV winding and the LV inductors, which are considered in the efficiency calculation, but also in the connecting PCB tracks and the necessary vias, where substantial additional conduction losses are induced. Unfortunately, these losses cannot reasonably be considered in the optimization, as they highly depend on the final PCB design. Consequently, as found for the TAB hardware prototype in Chapter 2, much higher LV-side conduction losses and therefore a lower overall efficiency are expected in the hardware prototype.

6.3 Experimental Verification

Based on the results of the aforementioned optimization, the most promising design has finally been implemented in hardware to test the suitability of the

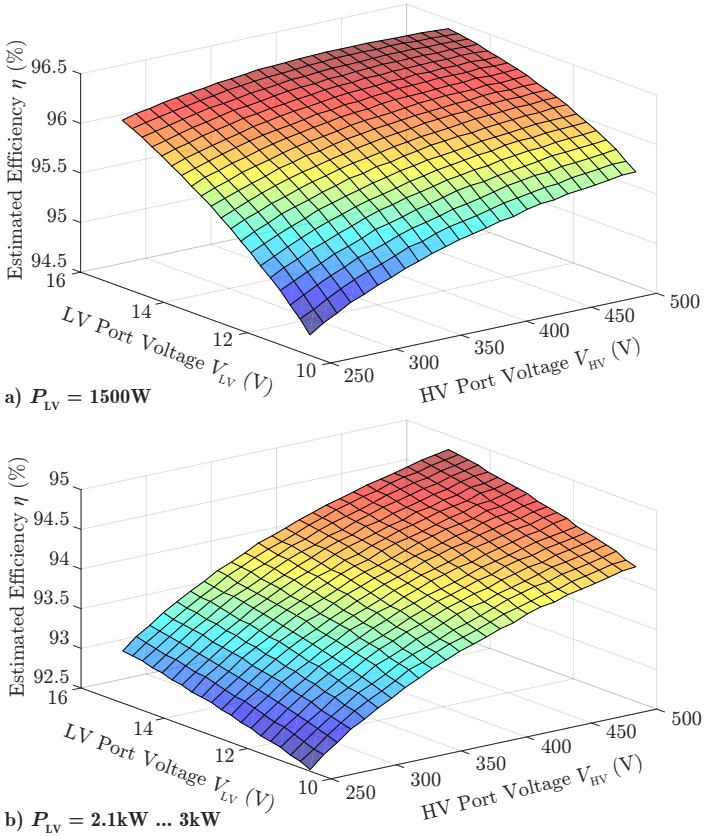


Fig. 6.14: Calculated efficiencies of the selected converter design for an output power of **a)** $P_{\mathrm{LV}} = 1.5\,\mathrm{kW}$ in drive mode operation and **b)** $P_{\mathrm{LV}} = 2.1\ldots3\,\mathrm{kW}$ in drive mode (DM) operation, which is limited by the maximum allowed output current I_{LV} of 200 A.

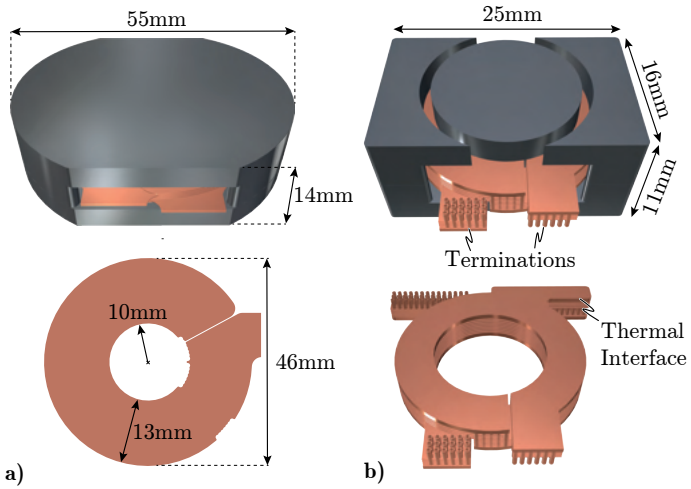


Fig. 6.15: a) Dimensions of the PCB-winding transformer of the hardware prototype and **b)** dimensions of the employed PCB-winding inductor.

proposed converter topology. The characteristic parameters of the selected converter design are summarized in Tab. 6.2 and the employed power components of the individual converter ports are listed in Tab. 6.3. Furthermore, the complete converter is controlled by means of a STM32F303 DSP in combination with a small MachXO2 FPGA, which generates the different gate signals and ensures the appropriate dead times.

The hardware design of the PCB-winding transformer corresponds to the one shown in Fig. 6.11b with a winding width b_W of 13 mm, whereby the PCB-winding is implemented in an 8-layer 70 µm PCB with an overall thickness of 2.4 mm (for isolation purposes). Furthermore, the thickness of the additional copper foil for the LV winding is 0.4 mm and the minimum core cross-section A_C is 290 mm^2 (cf. Fig. 6.15a).

The two capacitive voltage dividers of the PFC and the HV port comprise 16 individual 100 nF SMD capacitors (C4532NP02E104) each (8 on the top layer and 8 on the bottom layer of the PCB), in order to minimize the total ESR of the capacitor banks and, therefore, the occurring conduction losses as well. Hence, each capacitive voltage divider consists of two equivalent 800 nF capacitors, whereby the total effective resonant capacitance between the PFC and the HV port is 800 nF as well. This resonant capacitance, in combination with the expected total leakage inductance between the PFC and the HV port

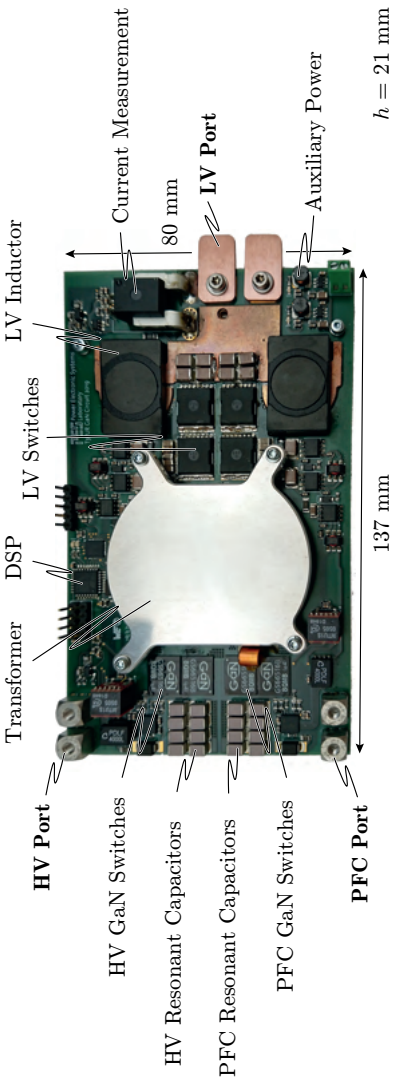


Fig. 6.16: Hardware prototype of the 3.6 kW three-port converter system with a total height of $h = 21\,\text{mm}$ (including heat sink volume).

Resonant Frequency	f_{res}	470 kHz
Minimum Frequency	f_{min}	155 kHz
Output Inductance	L_x	256 nH
Power Limit	P_{lim}	600 W

Tab. 6.2: Operating parameters of the 3.6 kW three-port DC/DC converter hardware prototype.

	PFC Port	HV Port	LV Port
Power Switches	GS66516B	GS66516B	IAUT300N08
Leakage Ind. $L_{\sigma,X}$	83 nH	59 nH	25 nH
Resonant Capacitors	800 nF	800 nF	-

Tab. 6.3: Component specifications of the 3.6 kW three-port DC/DC converter hardware prototype.

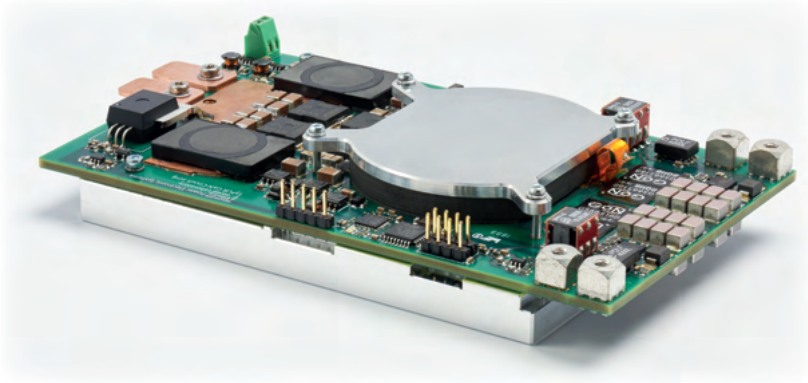


Fig. 6.17: Side-view of the hardware prototype of the 3.6 kW three-port converter system.

of 142 nH, results in the targeted resonant frequency f_{res} of 470 kHz.
The inductance of the output inductors is given by the design as $L_x = 256$ nH, which is why the minimum switching frequency $f_{sw,min}$ can be calculated according to (6.14) to be $f_{sw,min} = 155$ kHz.
The dimensions of the PCB-winding inductor are summarized in Fig. 6.15b, where the thickness of the additional copper foil on the top and on the bottom layer is again 0.4 mm. In order to improve the thermal coupling between the inductor winding and the heat sink, additional thermal interfaces are used, which are directly attached to the water-cooled heat sink through galvanically isolating thermal interface materials (TIM - Bergquist Gap Pad TGP HC5000). The additional copper foils for the LV inductor winding, on top and on the bottom of the PCB, are extended towards the output capacitors of the LV port, in order to minimize the overall resistance of the current paths, as shown in Fig. 6.16, where the fully assembled converter and the dimensions of the complete hardware prototype (including heat sink volume) are depicted. The water-cooled aluminum heat sink covers the complete bottom side of the converter and is screwed to the PCB in order to optimize the thermal interface between the PCB and the heat sink and to ensure short thermal paths from each component to the aforementioned common heat sink (cf. Fig. 6.17).

6.3.1 Experimentally Measured Performance in CM

The experimentally measured waveforms in charge mode (CM) operation are shown in Fig. 6.18 for exemplary full-load operating conditions with port voltages according to $V_{PFC} = 400$ V, $V_{HV} = 400$ V and $V_{LV} = 15$ V, and a power flow of 3.3 kW from the PFC to the HV port and 300 W from the PFC to the LV port. It should be mentioned, that the switching frequency in CM in the hardware demonstrator was set to 430 kHz instead of 470 kHz, as the measured total series-resonant inductance $L_{\sigma,PFC\rightarrow HV}$ was slightly higher than the calculated value, as the connection from the switch-nodes of the half-bridges to the transformer windings also contribute to the total series-resonant inductance. Consequently, the measured resonant frequency f_{res} is somewhat lower, which is why the converter was operated with a switching frequency of 430 kHz only. Furthermore, it can be noticed, that almost the full LV winding current i_{LV} is mapped to the HV winding, whereby the PFC winding current i_{PFC} is not really affected by the LV port. This asymmetry originates from the fact, that the coupling between the HV and the LV winding is much stronger than the coupling between the PFC and the LV winding, as the distance be-

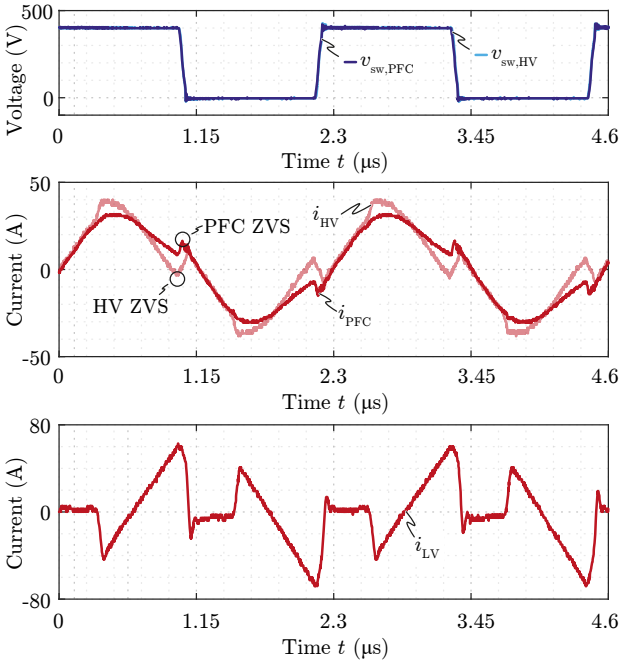


Fig. 6.18: Experimentally measured PFC-side switch-node voltage $v_{sw,PFC}$ and the three winding currents i_{PFC}, i_{HV} and i_{LV} of the PCB-winding transformer for nominal operation in CM with $V_{PFC} = V_{HV} = 400\,V$, $V_{LV} = 15\,V$, $P_{HV} = 3.3\,kW$ and $P_{LV} = 300\,W$.

tween the PFC and the LV winding is more than twice the distance between the HV and the LV winding. However, this asymmetry is intended, as due to this winding arrangement, during the switching transitions of the PFC and the HV port, the switch-node currents i_{PFC} and i_{HV} have different signs. Consequently, absolutely synchronous ZVS transitions of the two switch-node voltages $v_{sw,PFC}$ and $v_{sw,HV}$ are achieved, as the C_{oss} of the two half-bridges are synchronously charged/discharged. This is important, as otherwise, a comparably large voltage-time area $(v_{sw,PFC} - v_{sw,HV})$ across the small resonant inductance $L_{\sigma,PFC\rightarrow HV}$ would be applied, yielding a distortion of the resonant currents i_{PFC} and i_{HV} during the transitions, as will be explained in more detail in Chapter 7. Thus, the proposed layer stack-up of Fig. 6.11a should always be used for this topology, if a proper ZVS performance of the

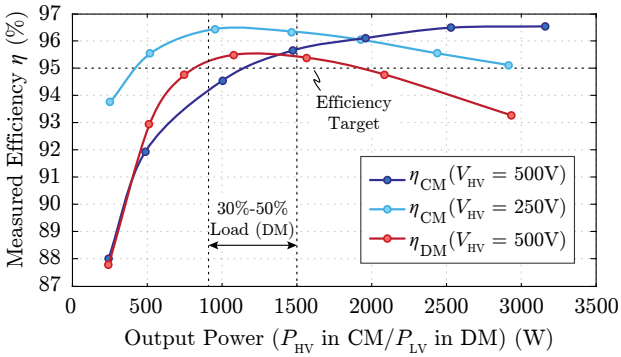


Fig. 6.19: Experimentally measured converter efficiencies in CM for the maximum and the minimum HV port voltage and a constant output power in the LV port of $P_{LV} = 300\,W$ at $V_{LV} = 15\,V$. Furthermore, the efficiency in DM for a V_{HV} of 500 V and a V_{LV} of 15 V is shown. The efficiency targets of 95 % at full load in CM, as well as partial load in DM are easily met.

converter should be guaranteed.
It needs to be mentioned, that due to the high level of system integration of the hardware demonstrator, only the PFC-side transformer current i_{PFC} can be measured accurately by means of a Rogowski current transducer (PEM CWT Ultra-mini, attached around the orange copper loop in Fig. 6.16). The HV- and the LV-side currents i_{HV} and i_{LV} were measured by means of a current sniffer probe (AimTTi I-Prober 520), which allows for contactless measurement of a current in a PCB track, based on its surrounding magnetic field. However, this method can only be used for a qualitative measurement, as a quantitative measurement, even with calibration, is extremely difficult in a densely packed converter. Fortunately, the magnitudes of the contactless measurements i_{HV} and i_{LV} can easily be estimated based on the accurate measurement of the PFC current i_{PFC}.

The experimentally measured efficiency curves in CM for nominal LV port operation ($V_{LV} = 15\,V$ and $P_{LV} = 300\,W$) and variable HV output power P_{HV}, for the maximum and the minimum HV port voltage are shown in Fig. 6.19. For the nominal HV port voltage ($V_{HV} = 500\,V$), a high full-load efficiency is achieved, as the 650 V semiconductors are optimally utilized, with a high voltage and a comparably low current. However, the efficiency drops significantly for partial-load operation, as the peak-to-peak value of

the circulating current in the LV port is proportional to V_{HV} and, therefore, results in a large constant loss-offset, which gains more and more impact on the efficiency, the lower the total output power is. Nevertheless, this was expected beforehand as it is a characteristic behavior of this topology. For the minimum HV port voltage (V_{HV} = 250 V), however, the picture changes completely. Hence, the full-load efficiency is comparably low, as the 650 V semiconductors are poorly utilized due to the low voltage and the resulting high currents, whereby the achievable efficiency is mainly limited by the conduction losses in these components. In contrast, the low V_{HV} reduces the circulating current in the LV port, whereby the partial-load efficiency is significantly increased. However, all the measured efficiencies are slightly lower than the calculated efficiencies for the ideal system, which has mainly two reasons: On the one hand, the conduction losses in the LV port are much higher than calculated, due to the previously mentioned additional current paths on the PCB, which are required to interconnect the various LV-side power components. On the other hand, the junction temperatures and the respective temperature dependent $R_{DS,on}$ values of the power semiconductors were calculated in the optimization based on the thermal model of the ideal thermal path from the semiconductor package to the heat sink (including thermal vias and TIMs). However, in reality, the idealized calculated thermal resistances can hardly be achieved, as the employed semiconductor packages are designed for bottom-side cooling, whereby all the semiconductor losses need to be dissipated through thermal vias in the 2.4 mm PCB and through the galvanically isolating TIM into the heat sink. Unfortunately, all these thermal vias in the footprints of the power switches make it more difficult to properly solder the switches to the PCB, as most of the solder paste is extracted though these vias during the reflow soldering process. Consequently the assumed ideal attachment of the switches to the PCB is hardly achieved, whereby the resistances of the thermal paths are increased. Consequently, the junction temperatures, as well as the $R_{ds,on}$ values, were slightly underestimated in the optimization, which has a significant impact on the occurring conduction losses, especially for GaN semiconductors. For this reason, it might be beneficial to use top-side cooled semiconductor packages, as both, the solder joints as well as the thermal coupling between the switches and the heat sink would be improved (at the expense of a more complex heat sink design).
Nevertheless, the efficiency target of 95 % at full load in charge mode is easily met, whereby the proposed topology has been proven to be a reasonable solution for three-port EV charging applications. In the following subsection, the converter performance is investigated in the second operating mode, the

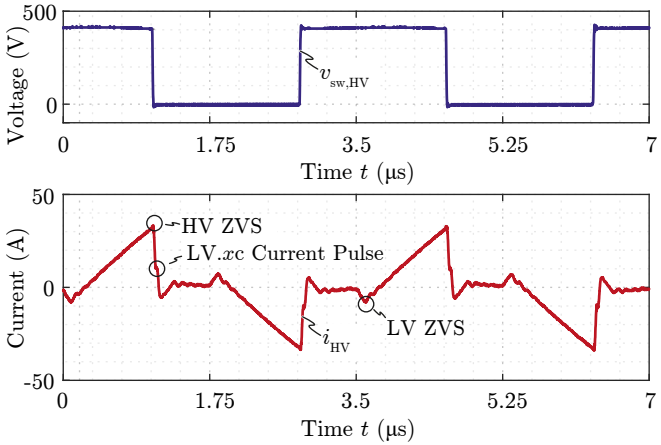


Fig. 6.20: Experimentally measured HV-side switch-node voltage $v_{sw,HV}$ and the HV winding current i_{HV} of the PCB-winding transformer for nominal operation in DM with $V_{HV} = 400\,V$, $V_{LV} = 15\,V$ and $P_{LV} = 1.5\,kW$.

drive mode (DM) operation.

6.3.2 Experimentally Measured Performance in DM

The experimentally measured waveforms in drive mode (DM) operation are shown in Fig. 6.20, for exemplary partial-load operating conditions according to $V_{HV} = 400\,V$, $V_{LV} = 15\,V$ and $P_{LV} = 1.5\,kW$. In order to ensure ZVS of the LV-side semiconductors, the switching frequency is set according to (6.5) to $f_{sw} \approx 285\,kHz$, whereby ZVS is guaranteed and at the same time the conduction losses are minimized. Furthermore, the additional short current pulses through the auxiliary switches LV.xc, $x \in \{1, 2\}$, during each HV-side switching transition can be observed. It needs to be mentioned, that the correct timing of the LV.xc switches is extremely important in a real system, as a slightly too early turn-on of these switches significantly increases their conduction losses. In contrast, a delayed turn-on in DM does not really have a negative effect on the operation of the converter, as there is no resonant current flow in the transformer, which could be distorted by an asynchronous switching transition of the PFC- and the HV-side half-bridges. However, in CM, a delayed switching transition indeed distorts the resonant current from

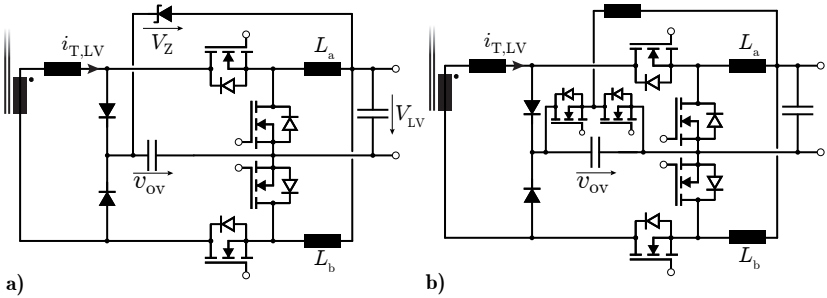


Fig. 6.21: Alternative over-voltage protection circuits using **a)** two passive diodes and a Zener diode and **b)** two passive diodes and an additional miniature step-down converter.

the PFC to the HV side, which in worst-case could lead to a destabilization of the resonant operation, as will be discussed in the next chapter. Hence, an extremely precise timing is especially important in CM, but unfortunately also very challenging to achieve.
In order to circumvent the timing issue, if e.g. a slow DSP or FPGA should be employed, passive diodes can be used instead of LV.*x*c, whereby the excess charge in C_{ov} needs to be transferred to the LV port by means of an additional circuitry. In case of only small Q_{ov} (6.10), a Zener diode (V_Z) can be connected between the positive C_{ov} potential and the positive V_{LV} potential, which keeps V_{ov} at $V_{LV} + V_Z$ (cf. Fig. 6.21a). This is the simplest and most reliable solution, but at the same time also quite inefficient, as a large fraction of $E_{ov} = f_{sw} \cdot Q_{ov} \cdot V_{ov}$ is dissipated in the Zener diode. Hence, for large E_{ov}, it might be better to employ a simple additional miniature step-down converter, which keeps V_{ov} at a specified level and feeds the excess energy to V_{LV} (cf. Fig. 6.21b). Even though these additional auxiliary circuits slightly increase the total number of components of the converter, the partial-load efficiency could be significantly increased, as the occurring switching losses during the switching actions of LV.*x*c (due to the Q_{oss} of LV.*x*c and LV.*x*b) could be circumvented.

However, with an appropriate control hardware, the two auxiliary switches can be controlled as described in Section 6.1.3, whereby the experimentally measured efficiency of Fig. 6.19 (red line) for the nominal port voltages $V_{HV} = 500\,V$ and $V_{LV} = 15\,V$ and a variable P_{LV} can be found. Similar to the efficiency curves in CM, two main loss mechanisms can be observed:

On the one hand, the inherently given circulating current in the LV port reduces the achievable low-load efficiency, whereas the huge currents in full-load operation induce substantial overall conduction losses in the converter, limiting the full-load efficiency of the converter. Nevertheless, the targeted partial-load efficiency of 95 % in nominal operation is easily met, whereby the proposed topology is proven to be a reasonable solution in drive mode operation.

Even though the proposed topology is perfectly suitable for the application at hand, there is still room for improvement in terms of hardware implementation, as especially the partial-load efficiency in nominal CM operation is limited by the large circulating currents in the LV port. Hence, in order to increase the partial-load efficiency in CM, somewhat larger output inductances should be used, whereby the peak-to-peak and the RMS value of the current ripple is reduced. However, this would require a larger transformer core cross-section, resulting in a reduction of the power density of the converter. Furthermore, a more sophisticated cooling concept might be beneficial, where either top-side cooled packages of the power semiconductors are used, which are then connected to the common heat sink by means of heat pipes, or cold welding instead of soldering of the switches could be used, in order to improve the joint between the switches and the PCB, whereby the thermal resistance from the semiconductor chip to the heat sink is significantly reduced. However, the application of these methods is always a trade-off between additional manufacturing costs and the achievable advantages in terms of system performance.

6.4 Summary of the Chapter

In this chapter, a novel three-port DC/DC converter topology for automotive applications has been introduced and analyzed. The topology comprises a combination of a series-resonant converter (SRC), which interconnects the DC-link capacitor of an upstream PFC rectifier with the high-voltage (HV) battery, and a modified phase-shifted full-bridge (MPSFB) converter, which connects the aforementioned HV battery with the auxiliary low-voltage (LV) battery. The two sub-systems are controlled synergetically, as they share a common transformer core, whereby the MPSFB can be used to ensure zero-voltage-switching (ZVS) and absolutely synchronous switching transitions of the PFC- and the HV-side half-bridges in the SRC. It is shown, that due to the aforementioned synchronous switching transitions, an extremely small

series-resonant inductance can be used, which is in particular beneficial, if the leakage inductance of conventional PCB-winding transformer structures should be used as series-resonant inductance. This is explained in more detail in Chapter 7.
In order to facilitate a possible hardware implementation of the proposed topology, simple design guidelines are given and the ideally achievable converter performance is found based on a multi-objective optimization. Finally, the suitability of the proposed converter topology has been proven by means of a 3.6 kW 500 V/500 V/15 V hardware demonstrator with a power density of 16.4 kW/L, which easily meets the targeted full-load efficiency of 95 % for nominal operating conditions (maximum port voltages) in charge mode (CM), and the partial-load efficiency of 95 % for nominal operating conditions in drive mode (DM).

7

Zero-Voltage-Switching Auxiliary Circuit for Minimized Inductance Requirement in Resonant Converter Systems

Chapter Abstract

In the previous chapter, the leakage inductance of a PCB-winding transformer has been used as series-resonant inductor, such that the number of discrete components and, therefore, the manufacturing costs of the complete converter system can be minimized. However, the achievable leakage inductance in power-dense and highly efficient PCB-winding transformer designs is extremely small, whereby the current through this leakage inductance reacts extremely sensitive to parasitic voltage-time areas, which e.g. occur during the switching transitions of the semiconductors on the primary and secondary side of the transformer. Consequently, perfectly synchronous switching transitions on both sides of the transformer are in demand, in order to guarantee a stable operation of the resonant converter. This can be achieved by means of an additional zero-voltage-switching (ZVS) auxiliary circuit, which is introduced and analyzed in this chapter. Furthermore, the proposed circuit allows for utilizing cost-effective superjunction silicon MOSFETs up to comparably high switching frequencies, whereby GaN power semiconductors can be avoided and the costs of the converter system can be reduced even further. The general operation of the proposed ZVS auxiliary circuit is explained by means of a simple DC-transformer example and is finally verified by means of experimental measurements .

Nowadays, PCB-integration of the windings of magnetic components is considered to be the most cost-effective solution, as the expensive wire-

Input Voltage	$V_{\mathrm{DC}-1}$	250 V…500 V
Output Voltage	$V_{\mathrm{DC}-2}$	250 V…500 V
Output Power	P_{out}	0 W…3.6 kW

Tab. 7.1: Specifications of a 3.6 kW DC-Transformer for Automotive Applications.

wrapping process is omitted and huge current densities can be allowed. Unfortunately, it is extremely challenging to achieve large inductance values with a reasonable efficiency in PCB-integrated magnetics [66, 69, 70], which is why the inductance requirements of converter systems in cost-driven applications should be minimized.
However, the actual size of the magnetic components mainly depends on two factors: The maximum output power of a considered converter system and the amount of magnetic energy, which needs to be stored temporarily. Especially the latter has a huge impact on the volume of the magnetic components and highly depends on the selected topology and the switching frequency, as a high switching frequency generally reduces the amount of magnetic energy which needs to be stored intermediately [71]. However, this unfortunately is not the only aspect, as in high-frequency (HF) applications zero-voltage-switching (ZVS) of the power switches is absolutely necessary for an efficient converter operation, which needs to be ensured by means of additional magnetic energy, stored in one of the main magnetic components [50]. In order to clarify this statement, the ZVS operation of power switches is explained based on the simple series-resonant converter (SRC) topology shown in Fig. 7.1, which corresponds to the SRC part of the three-port converter system of Chapter 6. For simplicity reasons, and without loss of generality, it is assumed that the converter is operated as a so-called DC-transformer, i.e. with unity voltage gain. Accordingly, a turns ratio of $n = 1 : 1$ and a switching frequency close to the resonant frequency f_{res} is selected, such that the primary side referred output voltage $n \cdot V_{\mathrm{DC}-2}$ follows the input voltage $V_{\mathrm{DC}-1}$. This converter could e.g. be used as an isolation stage between the high-voltage battery and a non-isolated single-stage charger in an EV [72], according to the exemplary specifications summarized in Tab. 7.1.

Consequently, there are two possibilities to achieve ZVS of the power switches HB-1.a and HB-1.b in this converter, if the ZVS auxiliary circuit (grey-shaded) is neglected: Either the magnetic energy stored in L_σ due to i_{load} is used to charge/discharge the C_{oss} of the power switches, or the magnetizing

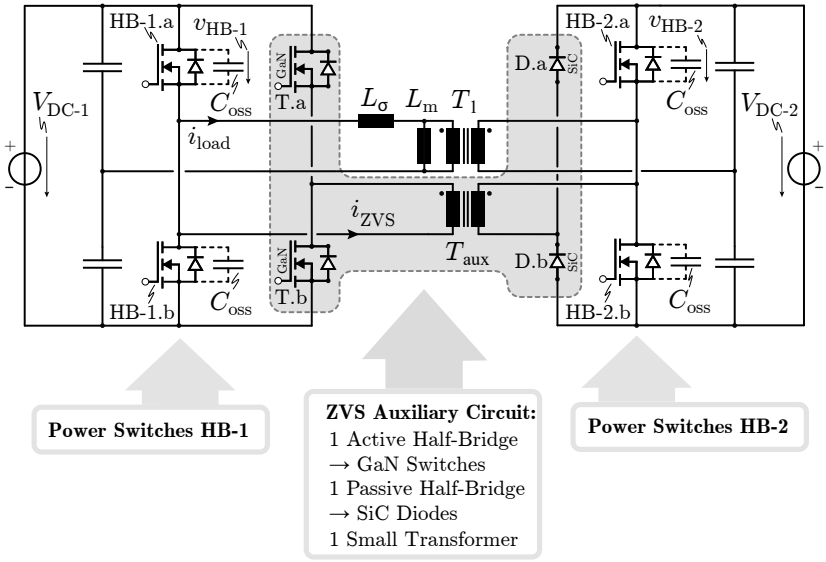


Fig. 7.1: Topology of a conventional series-resonant converter (SRC) with the main transformer T_1, the series-resonant inductance L_σ and two capacitive voltage dividers, which are used as resonant capacitors. Furthermore the grey-shaded components correspond to the proposed additional zero-voltage-switching (ZVS) auxiliary circuit, which comprises an active GaN half-bridge, a passive half-bridge with SiC diodes, as well as a small auxiliary transformer T_{aux}.

inductance is reduced and the resulting magnetizing current can be used to guarantee ZVS of the power switches. Hence, for both methods, the power switches can be turned on with discharged output capacitors, whereby the voltage across the switches is almost zero and the switching operation can be assumed to be lossless. Nevertheless, both of the aforementioned ZVS methods have their benefits and drawbacks, which will be discussed in the following.

In the first case, as the load current i_{load} is used for the ZVS transition, the Q_{oss} of the power switches is transferred to the secondary side as active power, which is why there are hardly any additional conduction losses induced for achieving ZVS. However, the required minimum peak current $i_{\sigma,\mathrm{pk}}$ at the beginning of the ZVS transition highly depends on the momentary DC-link voltage $V_{\mathrm{DC-1}}$, the employed series-resonant inductance L_σ and the nonlinear C_{oss} behavior and/or type of the employed power switches, as shown in Fig. 7.2a and Fig. 7.2b for an exemplary superjunction silicon MOSFET with an extremely non-linear $C_{\mathrm{oss}}(V_{\mathrm{ds}})$, and an exemplary GaN HEMT with a comparably flat $C_{\mathrm{oss}}(V_{\mathrm{ds}})$ curve. For this reason, either large inductance values L_σ have to be used, which are very difficult to achieve in PCB-integrated magnetics, or ZVS can only be achieved for the highest output power values, where sufficient i_{load} is available.

Alternatively, the magnetizing current can be used, which ensures ZVS independent of the output power. However, the magnetizing current is linearly increasing with the DC-link voltage, and for high switching frequencies, where short dead times t_{dead} need to be achieved, large magnetizing currents $i_{\mathrm{m,pk}}$ during the dead times are required (cf. Fig. 7.2c and Fig. 7.2d). Besides potential fringing losses around the additional air gap in the transformer core [73] (required for achieving a sufficient magnetizing current), the magnetizing current yields significant additional conduction losses, as this current results in reactive power, which circulates on the primary side of the converter and does not contribute to the power transfer to the output. Furthermore, this concept can only be used efficiently in applications with a fixed switching frequency, as otherwise, ZVS would only be achieved for the lowest switching frequencies, since the amplitude of the magnetizing current decreases inversely proportional to the switching frequency.

In order to overcome these limitations, different possible alternatives have already been proposed in literature [74, 75], where auxiliary circuits are

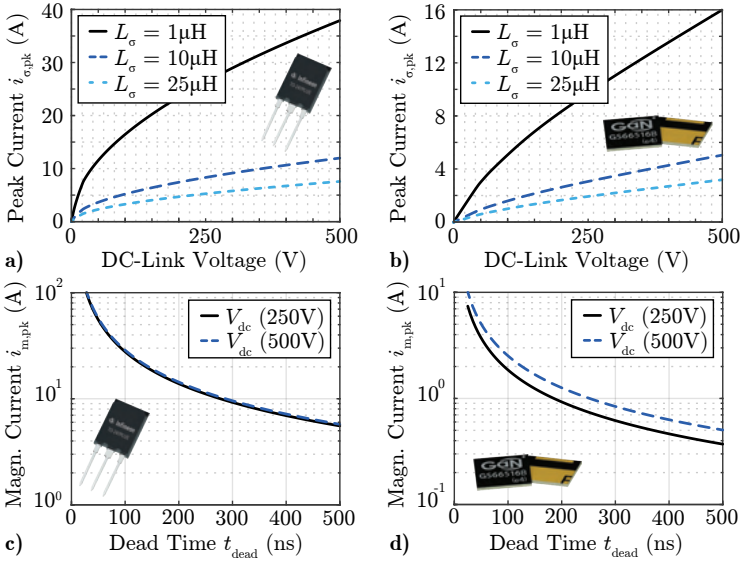


Fig. 7.2: a) Numerically calculated required peak currents to guarantee complete soft-switching of IPW60R018CFD7 silicon (Si) superjunction MOSFETs for three different series-resonant inductor values and **b)** the same currents for GS66516B gallium nitride (GaN) switches. **c)** Numerically calculated required magnetizing current to guarantee complete soft-switching within a certain dead time t_{dead} for the Si power transistor considered in **a)** and **d)** the same graphs for the GaN switch of **b)**.

used to guarantee ZVS of the power semiconductors. However, most of the solutions which are based on passive components suffer from exactly the same issues as the approach, where the magnetizing current is used for ZVS. Thus, the reactive power, which is circulating in the auxiliary circuit, depends on the switching frequency and the converter port voltage and can therefore not be controlled. Consequently, significant conduction losses usually arise in applications with widely varying port voltages and/or switching frequencies. In contrast, most active ZVS auxiliary circuits guarantee load independent ZVS conditions and some of them can even operate with varying switching frequencies. However, they struggle to efficiently ensure ZVS conditions for the power switches, if a wide port voltage range needs to be covered, as in principle, they are based on the same idea as using the circulating magnetizing current in the transformer. Thus, they generate a controllable triangular or trapezoidal reactive current, which is used for charging/discharging the C_{oss} of the power switches. Furthermore, the active ZVS auxiliary circuits are often bound to one specific converter topology, as they rely on a certain way the main converter is controlled.
Consequently, a ZVS concept would be desirable, which can be operated with an arbitrary switching frequency, an arbitrary port voltage, works independent of the output power, only processes the absolutely necessary power to ensure ZVS, and ensures perfectly synchronized primary- and secondary-side switch-node voltages. The synchronization is important, such that only minimal voltage-time areas across the series-resonant inductor L_σ are applied, whereby this inductance can be extremely small and, in addition, a fast dynamic response of the DC-transformer is ensured. Fortunately, all this can be achieved by introducing a small ZVS auxiliary circuit as shown in Fig. 7.1, which comprises two additional small active switches T.a and T.b, a small auxiliary transformer T_{aux}, as well as two passive diodes D.a and D.b. Even though in this work, the auxiliary circuit is explained based on the simple 1:1 DC transformer example, it can of course also be applied to converter systems with different topologies, different input to output voltage ratios and unequal primary and secondary-side switches.

In the following section, the operating principle of the proposed ZVS auxiliary circuit is explained based on an exemplary switching transition. Subsequently, the impact of different semiconductor materials of the power switches on the performance of the auxiliary circuit is investigated in detail.

7.1 ZVS Auxiliary Circuit Operation

In order to explain the general idea and the operation of the proposed ZVS auxiliary circuit, an exemplary switching transition of the converter, shown in Fig. 7.1, is investigated in detail in the following section.

7.1.1 Exemplary Zero-Voltage-Switching Transition

Assuming an initial condition according to t_1 in Fig. 7.3b, where the voltages $v_{\mathrm{HB-x}}, x \in \{1, 2\}$ across the switches are equal to V_{DC}, the Q_{oss} stored in the C_{oss} of HB-1.a needs to be transferred to the C_{oss} of HB-2.b, such that both, $v_{\mathrm{HB-1}}$ and $v_{\mathrm{HB-2}}$ drop to zero. Consequently, T.a needs to be turned on in order to apply $v_{\mathrm{HB-1}}$ to the auxiliary transformer, whereby the resulting voltage difference between the applied voltage on the primary side of the transformer ($v_{\mathrm{p}} = V_{\mathrm{DC}}$) and the voltage on the secondary side of the transformer ($v_{\mathrm{s}} = 0\,\mathrm{V}$) initiates a current i_{ZVS} through the leakage inductance L_{ZVS} of the auxiliary transformer. This current then starts to discharge the C_{oss} of HB-1.a and to charge the C_{oss} of HB-2.b, as desired.
It should be noticed, that the C_{oss} of the power switches of the primary and secondary side of the converter, together with the leakage inductance L_{ZVS} of the auxiliary transformer, form a resonant circuit, whereby no active control is required and the transfer of the Q_{oss} from the primary to the secondary-side switches is inherently regulated by means of the circuit design. Therefore, as soon as the complete Q_{oss} of HB.1a is transferred to the secondary side and thus, $v_{\mathrm{HB-1}}$ and i_{ZVS} drop to zero, the diode D.b would ideally start to block and $i_{\mathrm{ZVS}}(t > t_2)$ would remain zero. Unfortunately, like every semiconductor device, the diode has a certain parasitic capacitance C_{diode}, which needs to be charged in order to build up the blocking voltage across the device. As a result, a current $i_{\mathrm{C,diode}}$ is required for charging the C_{diode} of D.b from 0 V to V_{DC}. At $t = t_3$, the voltage across D.b reaches V_{DC} and i'_{ZVS} commutates from D.b to D.a. This current then circulates in L_{ZVS} and, as the voltage on both sides of the transformer is almost 0 V, its magnitude drops only slowly. As $i_{\mathrm{ZVS}}(t > t_2)$ is not used for the ZVS transition and does only contribute additional conduction losses to the auxiliary circuit, diodes with minimum C_{diode} should be employed in order to minimize the required $i_{\mathrm{C,diode}}$.
However, at $t = t_3$, the ZVS transition is theoretically completed and the next ZVS transition can be initiated after $T_{\mathrm{sw}}/2$ by switching off T.a and turning on T.b.

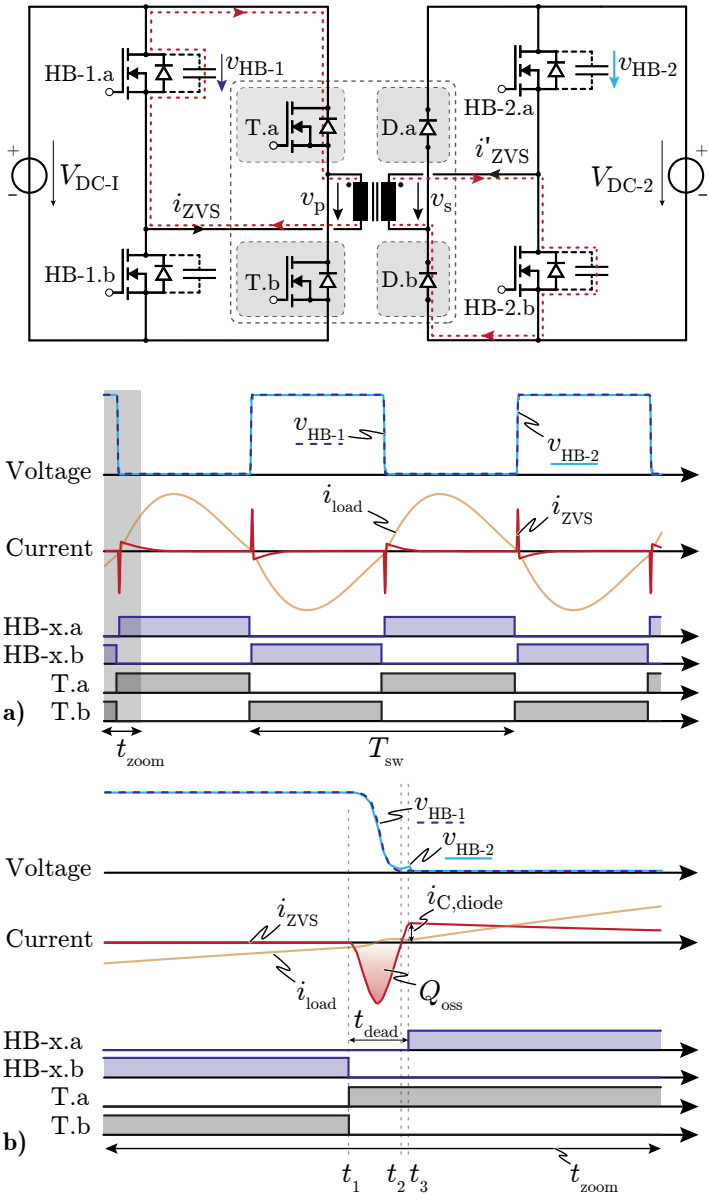


Fig. 7.3: a) Current and voltage waveforms as well as the gate signals of the SRC and the ZVS auxiliary circuit. **b)** Zoomed-in view of a single switching transition.

7.1.2 Effect of Different Types of the Power Switches

In a real application, the aforementioned $L_{ZVS} - C_{oss}$ resonant circuit is non-linear, as the output capacitance C_{oss} of semiconductors highly depends on the applied voltage and the employed type of switch (cf. Fig. 7.4a). Consequently, the voltage-dependent effective capacitance $C_{tot}(v_{sw})$ of a half-bridge configuration can be calculated according to

$$C_{tot}(v_{sw}) = C_{oss}(v_{sw}) + C_{oss}(V_{dc} - v_{sw}), \tag{7.1}$$

and is shown in Fig. 7.4a for two 650 V switches made of either silicon (Si) or gallium nitride (GaN). Due to the more linear behavior of the C_{oss} (and therefore C_{tot}) of GaN semiconductors, the voltage and current waveforms during a ZVS transition of these switches are of sinusoidal shape (cf. Fig. 7.4c1), whereas the waveforms for silicon switches look more like a voltage step resulting in a triangular current shape (cf. Fig. 7.4c2). This voltage step originates from the fact, that the C_{oss} of silicon switches for low voltages is orders of magnitude higher than for higher voltages. Hence, during the first half of the ZVS transition, almost all of i_{ZVS} flows into the C_{oss} of the upper MOSFET in order to charge this capacitance to a value of approximately 25 V. Thus, this C_{oss} forms the first resonant circuit with L_{ZVS} (cf. RC_1 in Fig. 7.4c2). As soon as v_{sw} reaches approximately $V_{DC} - 25\,V$, the C_{oss} of the upper switch drops significantly and, due to the large current and the small C_{tot}, the switch-node voltage drops to $v_{sw} \approx 25\,V$ almost immediately. As the C_{oss} of the lower MOSFET increases substantially for $v_{sw} < 25\,V$, this C_{oss} now forms a second resonant tank with L_{ZVS} (cf. RC_2), whereby v_{sw} drops to 0 V during the remaining $T_{tr}/2$.

The strong non-linearity of C_{tot} has the advantage, that the effective dead time T_{tr} of the circuit can hardly be seen based on the switch-node voltage, and that even during the dead time T_{tr}, the power flow through the main transformer continues. However, the load current i_{load} during the ZVS transition yields a charge imbalance in the auxiliary circuit, as i_{load} on the primary side of the converter assists the ZVS transition, whereas on the secondary side, i_{load} counteracts i_{ZVS} and therefore slightly delays the transition of the switch-node voltage of the secondary side (cf. t_{delay} in Fig. 7.5). Due to this delay, a large voltage time area $\psi_{L\sigma}$ is applied across the main inductor L_σ, which, depending on the inductance of L_σ, has a large impact on i_{load}. Consequently, T_{tr} should be chosen to be as short as possible for minimizing the L_σ inductance requirement. However, in order to be able to predict the impact of the length of the dead time T_{tr}, not only on L_σ, but also on the performance and the

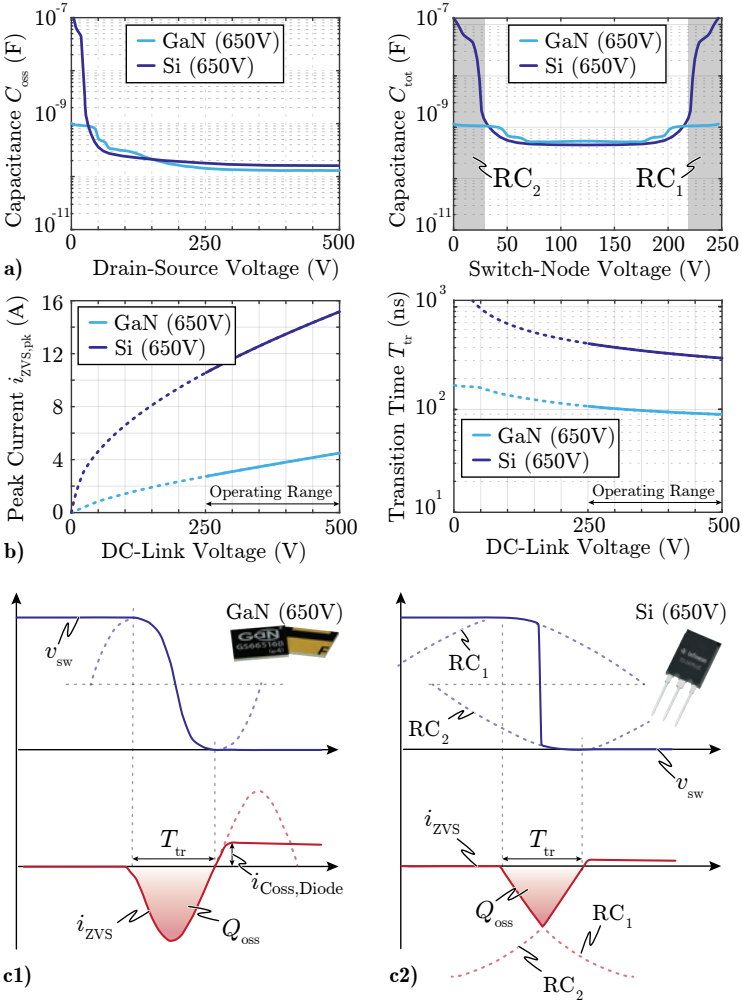


Fig. 7.4: a) C_{oss} and the total capacitance C_{tot} of a half-bridge for IPW60R018CFD7 Si superjunction MOSFETs [76] (cf. Fig. 7.2a and Fig. 7.2c) and GS66516B GaN switches [77] (cf. Fig. 7.2b and Fig. 7.2d). **b)** Peak values of i_{ZVS} and the transition times T_{tr} for a ZVS inductance L_{ZVS} of 3 µH for both aforementioned switches. **c)** Voltage and current waveforms during a switching transition for GaN (**c1**) and Si superjunction (**c2**) switches.

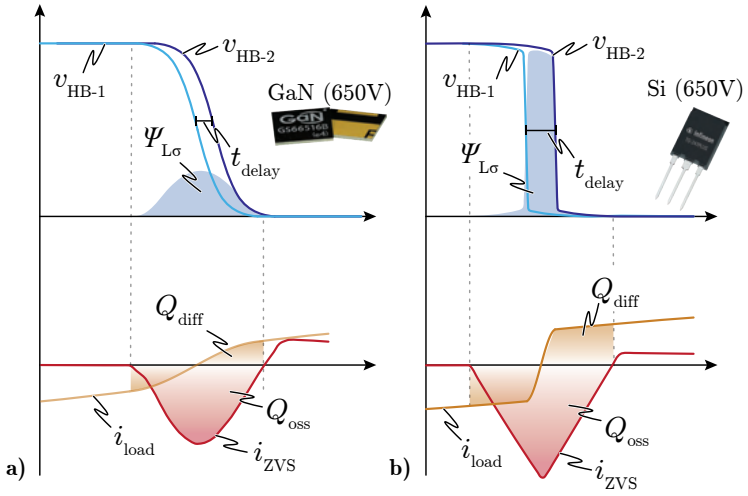


Fig. 7.5: Voltage and current waveforms of the delayed ZVS transition due to the load current i_{load} for **a)** GaN power switches and **b)** Si superjunction power MOSFETs.

efficiency of the ZVS auxiliary circuit, the RMS values of the ZVS current i_{ZVS} need to be known, which is why they are calculated in the following section.

7.1.3 Simplified Analytical Calculations

In order to simplify the analysis of the ZVS auxiliary circuit, a charge-equivalent effective capacitance of a half-bridge configuration can be defined according to

$$C_{eff}(V_{DC}) = \frac{1}{V_{DC}} \int_0^{V_{DC}} C_{oss}(v_{sw}) + C_{oss}(V_{DC} - v_{sw}) \mathrm{d}v_{sw}. \tag{7.2}$$

Using this equivalent capacitance, the peak currents and the transition times for both, sinusoidally shaped i_{ZVS} (as e.g. for GaN semiconductors) as well as triangular i_{ZVS} (as e.g. for Si superjunction MOSFETs), can easily be calculated according to

$$i_{ZVS,pk,GaN} = \sqrt{\frac{C_{eff}}{2 \cdot L_{ZVS}}} \cdot V_{DC} \tag{7.3}$$

$$i_{ZVS,pk,Si} = \sqrt{\frac{C_{eff}}{L_{ZVS}}} \cdot V_{DC} \tag{7.4}$$

and

$$T_{\mathrm{tr,GaN}} = \pi \cdot \sqrt{\frac{C_{\mathrm{eff}} \cdot L_{\mathrm{ZVS}}}{2}} \tag{7.5}$$

$$T_{\mathrm{tr,Si}} = 2\sqrt{C_{\mathrm{eff}} \cdot L_{\mathrm{ZVS}}}. \tag{7.6}$$

The voltage-dependent $i_{\mathrm{ZVS,pk}}$ and T_{tr} are shown in Fig. 7.4b for two exemplary 650 V switches. As indicated in the figure, the transition time varies only slightly for DC-link voltages above 250 V and shows an almost linear dependency on V_{DC}. Thus, for GaN switches, a constant dead time t_{dead} of the power switches can be used, as T_{tr} only marginally varies with V_{DC}, whereas for silicon superjunction switches, the dead time t_{dead} should be adapted to the momentary V_{DC} value according to the linear dependency of T_{tr} on V_{DC}. However, the transition times are completely independent of the load current i_{load} and the switching frequency f_{sw} of the power switches, which is why there is no need for any further control of the auxiliary circuit. Hence, no matter how large the C_{oss} of a certain semiconductor is, with an appropriately designed auxiliary circuit, the required ZVS can be ensured under all operating conditions. Nevertheless, the capacitance of the C_{oss} has a major impact on the occurring losses in the auxiliary circuit, as will be explained in the following.

In terms of system operation, an as small as possible T_{tr} and therefore L_{ZVS} would be desirable, in order to keep the ZVS transition as short as possible. However, from a loss perspective, a shorter transition time yields a higher harmonic content of i_{ZVS} and therefore significantly higher conduction losses in all components of the ZVS auxiliary circuit (cf. Fig. 7.6), according to

$$I_{\mathrm{RMS,Si}} = \sqrt{\frac{8}{3}} \cdot \frac{V_{\mathrm{DC}} \cdot C_{\mathrm{eff}}}{\sqrt{T_{\mathrm{tr,Si}} \cdot T_{\mathrm{sw}}}} \tag{7.7}$$

and

$$I_{\mathrm{RMS,GaN}} = \frac{\pi}{2} \cdot \frac{V_{\mathrm{DC}} \cdot C_{\mathrm{eff}}}{\sqrt{T_{\mathrm{tr,GaN}} \cdot T_{\mathrm{sw}}}}, \tag{7.8}$$

which have both been calculated based on the waveforms shown in Fig. 7.6a and the equations (7.5) and (7.6). Thus, the selection of T_{tr} yields a tradeoff between the overall system performance and the efficiency of the ZVS auxiliary circuit. In the following section, the individual loss components are investigated in detail, in order to simplify the design of the auxiliary circuit for a certain given set of power switches.

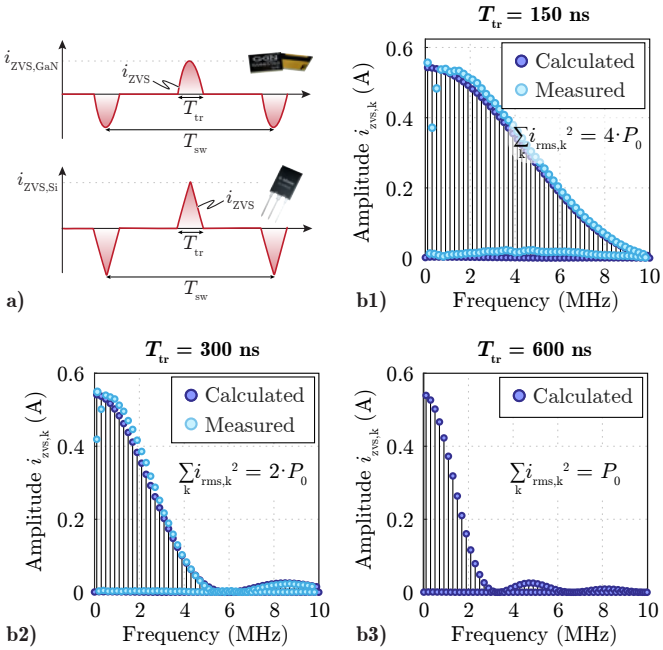


Fig. 7.6: a) Characteristic current waveforms for GaN and Si superjunction power switches and **b)** calculated (dark blue) and the experimentally measured (light blue) spectrum of the ZVS current i_{ZVS} for different transition times T_{tr}. Additionally, the calculated normalized conduction losses for a unity resistance are shown ($\sum_k i_{rms,k}^2$). Due to the neglected $i_{C,diode}$ in the calculation of the current spectrum, there is a slight deviation between calculation and measurement.

7.1.4 Losses in the Auxiliary Circuit

The total losses of the ZVS auxiliary circuit can be divided into three main components: First, the switching losses of T.a and T.b, as their Q_{oss} is dissipated in the beginning of each ZVS transition; Second, the conduction losses in T.a, T.b, the auxiliary transformer, D.a and D.b; and third, the hysteresis losses in the C_{oss} of the power switches, as not all of the energy stored in C_{oss} can be recycled [78, 79]. However, this loss component is given by the internal power transistor structure and can hardly be influenced by the design of the auxiliary circuit. Nevertheless, the two other loss components strongly depend on the design, which is why they are investigated in detail in the following.
The switching losses in T.a and T.b can be calculated based on the datasheet values of their C_{oss} according to [50]

$$P_{ZCS,sw} = 2 f_{sw} V_{DC} \cdot \int_0^{V_{DC}} C_{oss}(v) \mathrm{d}v. \tag{7.9}$$

Hence, in order to minimize the expected switching losses, an as small as possible C_{oss} should be targeted. For this reason, small GaN switches should be employed, as they feature an exceptional figure-of-merit ($C_{oss} \cdot R_{DS,on}$).
The second loss component is somewhat more difficult to calculate, as the conduction losses depend on the selection of T_{tr}. Thus, T_{tr} is considered as a degree of freedom for system optimization, which is why the conduction losses are calculated for each T_{tr} individually.
The estimation of the conduction losses in T.a, T.b, D.a and D.b is straightforward according to

$$P_{cond,sw} = R_{DS,on} \cdot I_{RMS,x}^2 \tag{7.10}$$

and

$$P_D = U_F \cdot I_{avg} + R_D \cdot I_{RMS,x}^2, \tag{7.11}$$

where the diode conduction losses can be approximated by $R_D \cdot I_{RMS,x}^2$, as this term is clearly dominating in this application. However, the limiting factor in the selection of appropriate diodes is usually not the conduction losses, but rather the allowable repetitive peak current of a certain device, which should correspond to the maximum peak current $i_{ZVS,pk}(V_{DC})$ in order to minimize the employed chip area and therefore the C_{diode} of D.a and D.b. For the application at hand, Schottky diodes made of silicon carbide (SiC) have been found to be the best solution due to their large ratio between the allowable repetitive peak current and their C_{diode} values.

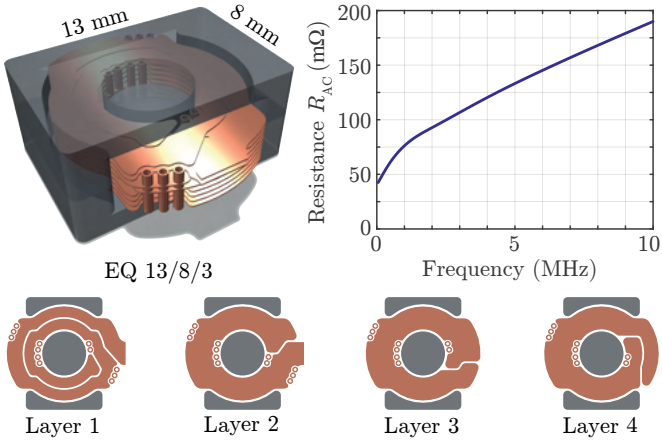


Fig. 7.7: ZVS auxiliary circuit transformer design with a turns ratio of 5:5, a leakage inductance L_{ZVS} of 256 nH and a total frequency-dependent winding resistance R_{AC} as illustrated.

However, in order to be able to calculate $i_{ZVS,pk}$ and $I_{RMS,x}$ (cf. (7.7) and (7.8)), the ZVS inductance L_{ZVS} needs to be known, which can be calculated for each T_{tr} based on (7.5) and (7.6) according to

$$L_{ZVS,GaN} = \left(\frac{T_{tr}}{\pi}\right)^2 \cdot \frac{2}{C_{eff}} \tag{7.12}$$

$$L_{ZVS,Si} = \left(\frac{T_{tr}}{2}\right)^2 \cdot \frac{1}{C_{eff}}. \tag{7.13}$$

In order to minimize the manufacturing cost and the AC resistance of this inductor, the inductance L_{ZVS} should be integrated as leakage inductance into the small auxiliary transformer, as the vertically aligned current flow in planar transformers reduces the proximity effect and therefore the high-frequency (HF) resistance of PCB-windings as well [65]. This is especially important in this application, as otherwise, the high harmonic content of i_{ZVS} would lead to significant HF conduction losses.
The leakage inductance between two PCB-windings can be influenced by the geometrical arrangement of their turns (cf. Fig. 7.7) and in particular by the distance between the primary and secondary-side windings. However, the calculation of the leakage inductance in planar transformers has already been discussed extensively in literature [63, 64], which is why it is not discussed

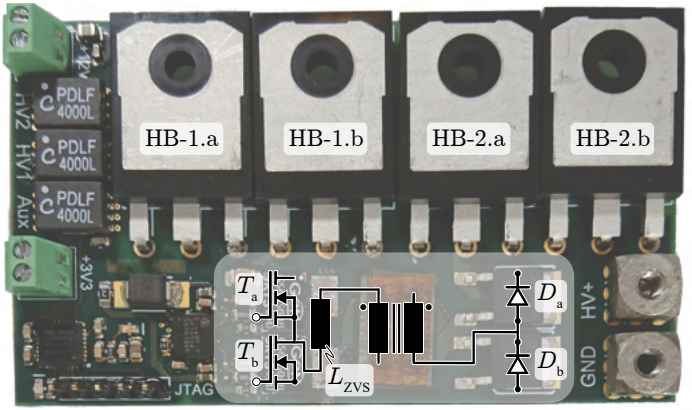
any further here.
The design of the transformer itself introduces again a large number of degrees of freedom (number of turns N, winding width b_w, core cross-section A_C, etc.) and is subject to an optimization with respect to efficiency and power density. This optimization is conducted based on the calculated winding current $i_{RMS,x}$ (cf. (7.7) and (7.8)) and the peak flux linkage $\psi_{ZVS,pk}$ given as

$$\psi_{ZVS,pk} = \frac{1}{2} \max\left(V_{DC}\right) T_{tr}. \tag{7.14}$$

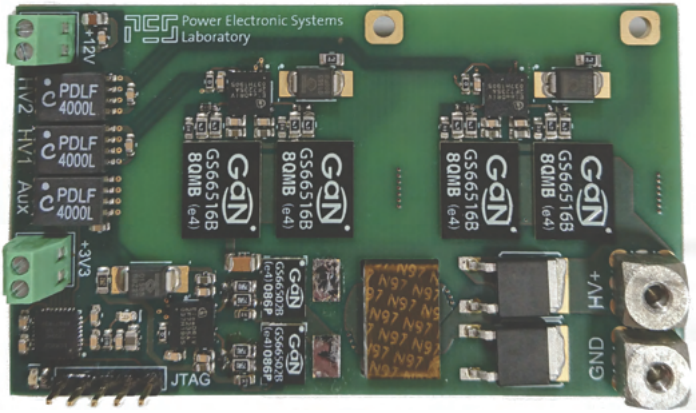
However, as this optimization is based on well-known formulas for calculating the winding [80] and the core losses [38], it is not explained in detail here.
In Fig. 7.7, an exemplary ZVS transformer with a turns ratio of 5:5 and a leakage inductance L_{ZVS} of 256 nH is shown. Furthermore, the corresponding layer arrangement of one winding is illustrated, whereby the second winding is identical and mirrored with respect to the center of the eight-layer PCB. This transformer is finally used in the two hardware demonstrators, which will be introduced in the following.

7.2 Experimental Verification

In order to verify the operating principle of the proposed ZVS auxiliary circuit, two hardware demonstrators have been built and measured (cf. Fig. 7.8). The ZVS auxiliary circuits are identical in both prototypes, but the power switches are either IPW60R018CFD7 Si superjunction MOSFETs from Infineon (Fig. 7.8a) or GS66516B GaN switches from GaN Systems (Fig. 7.8b). In order to be able to test the performance of the circuit for different L_{ZVS} and T_{tr} values, two SMD pads have been employed, to which different external inductors can be soldered (L_{ZVS}). The auxiliary switches T.a and T.b are GS66502, the diodes D.a and D.b are C3D03060A SiC diodes from Cree and the transformer is the one shown in Fig. 7.7 with an inherent leakage inductance of 256 nH. The whole circuit is controlled by means of a MachXO2 FPGA, which generates the required gate signals for the different switches.
Fig. 7.9 shows the experimentally measured waveforms during one switching transition for both hardware prototypes, a V_{DC} equal to 250 V and an external inductance of $L_{ZVS} = 3\,\mu H$. As expected, the shape of the measured waveforms as well as the T_{tr} and $i_{ZVS,pk}$ values are in good agreement with the calculated values shown in Fig. 7.4b. The ringing of the switch-node voltage v_{HB-2} in Fig. 7.9b originates from the parasitic inductance of the TO-247 package of the power switches and cannot be avoided, as the nonlinear C_{oss} of Si MOSFETs



a) Si - Hardware Demonstrator



b) GaN - Hardware Demonstrator

Fig. 7.8: a) Hardware demonstrator for Si superjunction power switches and the proposed ZVS auxiliary circuit (grey-shaded) and **b)** the same ZVS auxiliary circuit, but with GaN power switches. The dimensions of both PCBs are given by 113 mm x 73 mm (4.44 in x 2.87 in).

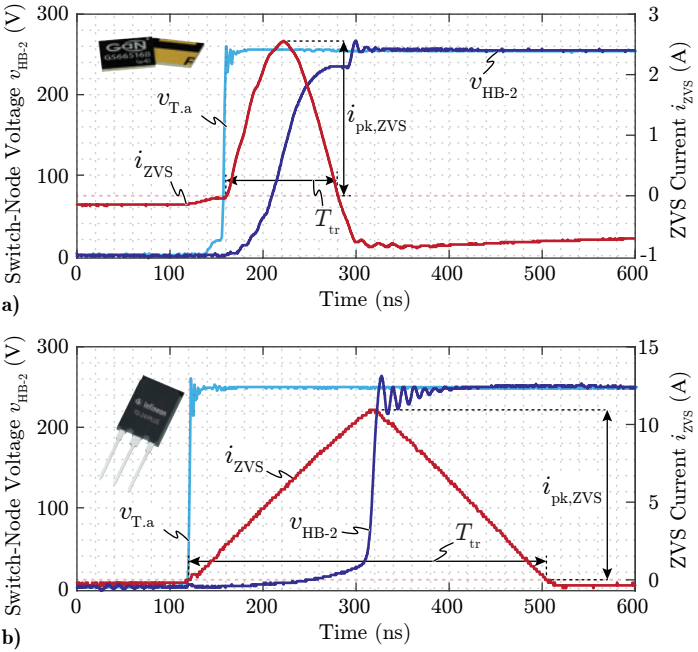


Fig. 7.9: Experimentally measured voltage and current waveforms during a switching transition for the hardware demonstrator with **a)** GaN power switches and **b)** Si superjunction MOSFETs.

yields huge $^{\text{d}i}/_{\text{d}t}$-values in the switches during a ZVS transition (cf. Fig. 7.10). Hence, almost all of the ZVS current flows in the switch with the larger momentary C_{oss} value and the commutation from one switch to the other happens extremely fast.

In order to estimate the achievable benefit by utilizing the proposed ZVS auxiliary circuit, the total losses of the hardware demonstrator have been measured for a switching frequency of 100 kHz with (P_{ZVS}) and without (P_{ZCS}) active ZVS auxiliary circuit. Hence, without the auxiliary circuit (P_{ZCS}), the total Q_{oss} of the four power switches is dissipated by means of switching losses. This operating mode is required, if perfectly synchronous transitions of the switch-node voltages on the primary and the secondary side of the converter are important. The simultaneous transitions are crucial in applications where only a small L_σ is employed, as otherwise, the resulting voltage-time area $\psi_{\text{L}\sigma}$

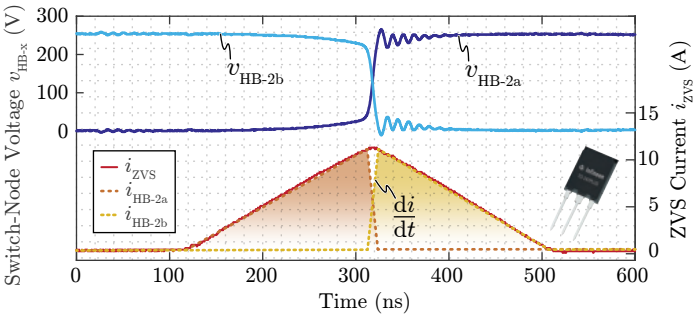


Fig. 7.10: Voltage and current waveforms of the Si hardware demonstrator with the indicated C_{oss} currents $i_{\text{HB-2a}}$ and $i_{\text{HB-2b}}$ in order to illustrate the large $\mathrm{d}i/\mathrm{d}t$-values during a ZVS transition.

results in a step in i_{load} (cf. Fig. 7.5). If a larger L_σ would be employed, only the half-bridge on the primary side would need to be switched, as the secondary-side half-bridge operates as a synchronous rectifier, thus is inherently operated under ZVS conditions. Consequently, only half of the aforementioned P_{ZCS} losses would be dissipated. However, as the ZVS auxiliary circuit targets applications with minimal L_σ requirements, the performance is compared to the first operating mode where all four switches are actively switched.

The results are shown in Fig. 7.11 for different ZVS inductance values, where the loss saving ξ (solid lines) indicates the amount of E_{oss} stored in the power switches which can be saved by operating the ZVS auxiliary circuit. Furthermore, the occurring losses P_{ZCS} and P_{ZVS} are shown for a $L_{\text{ZVS}} = 250\,\text{nH}$ in Fig. 7.11a and $L_{\text{ZVS}} = 720\,\text{nH}$ in Fig. 7.11b, respectively. As expected based on (7.7) and (7.8), the losses are increasing for smaller L_{ZVS} and therefore shorter T_{tr}. However, while the loss saving in percentage of silicon switches is more or less constant for different DC-link voltages, the one of GaN switches is dropping significantly. This behavior originates from the $^{dv}/_{dt}$-dependency of the ZVS losses in GaN switches [81, 82], as the hysteresis losses are increasing significantly with the applied DC-link voltage (cf. Fig. 7.12a). In contrast, the hysteresis loss-percentage of Si superjunction switches is almost constant and for this specific switch around 6 % (cf. Fig. 7.12b). However, the hysteresis losses strongly depend on the inner switch structure/design, i.e. manufacturer, device family, etc. [78, 79, 83], which is why they need to be measured for each device individually in order to estimate the expected hysteresis losses.

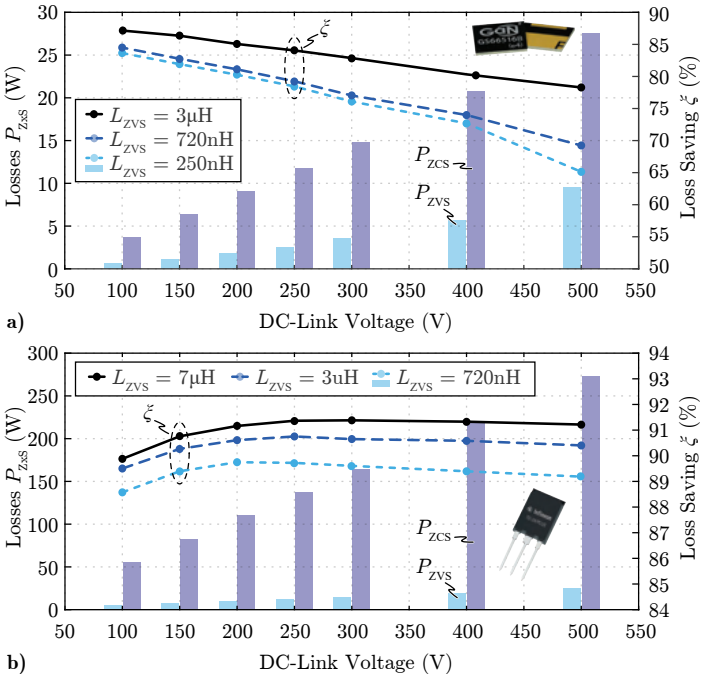


Fig. 7.11: Experimentally measured losses of the hardware prototypes with (P_{ZVS}) and without (P_{ZCS}) operating the ZVS auxiliary circuit in **a)** for GaN power switches and in **b)** for Si superjunction MOSFETs.

Nevertheless, as proven by means of the hardware demonstrators of Fig. 7.8, the utilization of the proposed ZVS auxiliary circuit allows for an efficient recycling of a large share of the E_{oss} of power semiconductors. Thus, for a DC-link voltage of e.g. 500 V and a switching frequency of 100 kHz, the utilization of the ZVS auxiliary circuit increases the full-load (3.6 kW) efficiency of the overall converter system for GaN power switches by more than 0.5 %, and for Si superjunction MOSFETs by more than 6 %. Therefore, even Si superjunction MOSFETs can now be used for comparably high switching frequencies, without an excessive amount of additional circuitry.

This is verified in Fig. 7.13, where the maximum achievable efficiencies of the DC-transformer example are shown for both, Si (IPW60R018CFD7) and GaN (GS66516T) power switches, a L_{ZVS} of 720 nH, and a switching frequency of 100 kHz, whereby only the losses in the power switches and the ZVS auxiliary

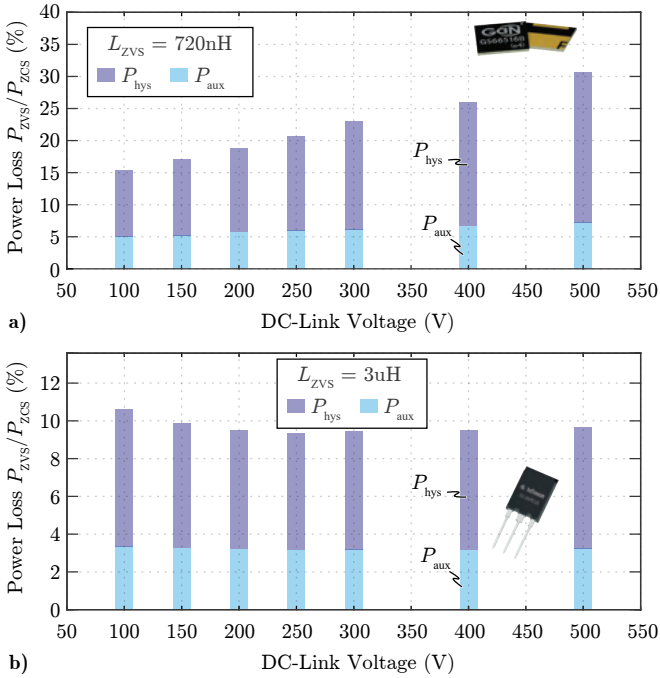


Fig. 7.12: Estimated distribution of the hysteresis losses P_{hys} and the total losses of the auxiliary circuit P_{aux} based on the total measured losses P_{ZVS}, the FFT of the measured i_{ZVS} and the measured AC resistances of the components for GaN switches (GS66516B) and an L_{ZVS} of 720 nH in **a)** and Si superjunction switches (IPW60R018CFD7) and an L_{ZVS} of 3 µH in **b)**.

switches are considered. Hence, the power transformer is assumed to be lossless, as its design highly depends on the targeted converter efficiency and has no impact on the occurring losses in the semiconductors. Thus, either an extremely power-dense transformer with high losses can be used, or a comparably large transformer with minimized conduction and core losses could be employed, whereby the efficiency of Fig. 7.13a can be approached. However, besides the additional transformer losses, all other loss components are considered, as will be discussed in the following.

The losses in the power semiconductors comprise two individual components: The switching losses, i.e. the hysteresis losses during the switching transitions (P_{hys}), and the conduction losses, which originate due to the sinu-

soidal transformer currents i_{load}. The switching losses are calculated based on experimental measurements (cf. Fig. 7.11), whereas the conduction losses are calculated based on the simulated i_{load} and the temperature dependent $R_{\mathrm{ds,on}}(T_{\mathrm{j}})$ of the power switches. The expected junction temperatures T_{j} are calculated iteratively based on the total losses in one semiconductor and a simple thermal model, which consists of the thermal resistance of the semiconductor package, the isolating thermal interface material ($\lambda = 6\,\mathrm{W\,K/m}$, thickness = 0.5 mm) and a water-cooled aluminum heat sink with a coolant temperature of 80 °C, which is a common specification in automotive applications. The resulting calculated junction temperatures are shown in Fig. 7.13b, where it should be noted, that for full-load operation and $V_{\mathrm{DC}} = 250\,\mathrm{V}$, the GaN switches would be operated very close to their thermal limit, whereas the hot spot temperature in the Si switches never exceeds 90 °C.
Furthermore, in Fig. 7.13a, the hatched areas for the two efficiency curves $\eta_{\mathrm{Si,250V}}$ and $\eta_{\mathrm{GaN,250V}}$ indicate the amount of losses, which originate from the hysteresis losses P_{hvs} and the auxiliary circuit P_{aux} alone, whereby the non-hatched area above the efficiency curves correspond to the conduction losses in the power semiconductors. It can be seen, that for the silicon MOSFETs, especially for partial-load operation, the switching losses $P_{\mathrm{hys}} + P_{\mathrm{aux}}$ have a huge impact on the achievable partial-load efficiency, whereby the conduction losses are almost negligible. In contrast, the switching losses of the GaN semiconductors are much lower and the conduction losses start to dominate the efficiency already at very low output power values. Hence, the GaN switches are very suitable for this application and the specified power level, whereby the Si MOSFETs are clearly under-utilized, as their junction temperatures are hardly increasing and they could be operated with much higher currents (at $P_{\mathrm{out}} = 6.6\,\mathrm{kW}$, $\eta_{\mathrm{Si,500V}}$ and $\eta_{\mathrm{Si,250V}}$ are still above 99 % and 97.5 %, respectively).
Nevertheless, the full-load efficiencies for both semiconductor materials are almost identical, even though the costs for Si superjunction MOSFETs are significantly lower compared to the GaN HEMTs. Hence, using the proposed ZVS auxiliary circuit, Si MOSFETs can be used with a similar full-load performance as GaN HEMTs up to comparably high switching frequencies.

In Fig. 7.14, the distribution of the occurring losses in the ZVS auxiliary circuit is shown for one specific operating point. Due to the much higher AC resistance of the external inductor L_{ZVS} compared to a PCB-integrated equivalent, it has not been considered in this loss distribution in order not to distort the results. Hence, in a fully PCB-integrated solution with an L_{ZVS} of

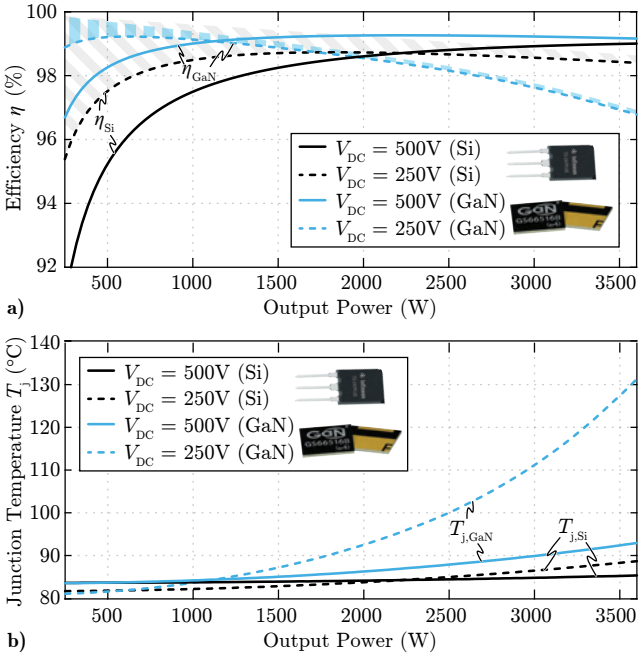


Fig. 7.13: a) Maximum achievable efficiency of the DC-transformer for two different power switches (Si = IPW60R018CFD7, GaN = GS66516T), a switching frequency of 100 kHz and DC-link voltages of 250 V and 500 V, where an ideal (lossless) transformer is assumed. Furthermore, the hatched areas for $V_{DC} = 250\,V$ indicate the share of switching losses (incl. ZVS auxiliary circuit). **b)** The corresponding junction temperatures of the power switches for a water-cooled aluminum heat sink with a coolant temperature of 80 °C.

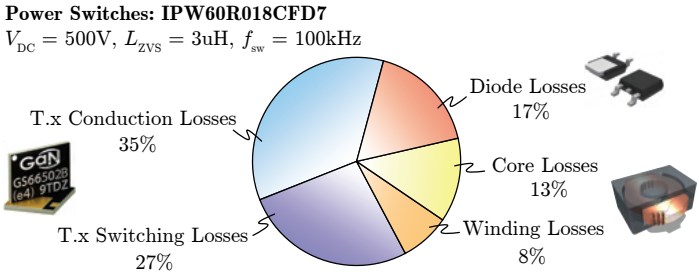


Fig. 7.14: Distribution of the losses occurring within the ZVS auxiliary circuit, shown in Fig. 7.8a, with Si superjunction MOSFETs as power switches, a DC-link voltage of 500 V, a switching frequency of 100 kHz and an external ZVS inductance of L_{ZVS} = 3 µH (whose losses are not considered in this graph, as they would be much lower if L_{ZVS} would be fully integrated in the auxiliary transformer).

3 µH, the share of the winding losses would be slightly larger, in the range of 25 %.

Despite ensuring ZVS conditions of the power switches, the ZVS auxiliary circuit can also be used to pre-charge the output capacitor of the secondary side, such that the power part of the circuit can start its operation with matching input and output voltages. Hence, L_σ does not need to be designed to withstand huge inrush currents, as it would be the case with a large initial voltage difference between the input and output voltage. As the auxiliary circuit is anyway designed in such a way, that the maximum energy which can be transferred within one switching cycle is the E_{oss} of the power switches, the initial voltage difference between the input and the output voltage does not matter and the peak value of i_{ZVS} is limited according to (7.3) and (7.4). Consequently, during each switching transition, the output capacitor C_{out} is charged due to i_{ZVS}, until it reaches the required output voltage $V_{out} = V_{DC}$. The corresponding simulated waveforms are shown in Fig. 7.15, where the (stepwise) charging of C_{out} can easily be observed. It should be noted, that the peak current $i_{ZVS,pk}$ is independent of V_{out}, which is why the usage of this functionality has no impact on the design of the auxiliary circuit and it can be utilized "for free".

So far, the application of the ZVS auxiliary circuit has only been discussed for equal primary- and secondary-side power switches. However, as previously mentioned, this concept can of course also be applied if different power switches are used, which is inevitable in converter systems with e.g. large

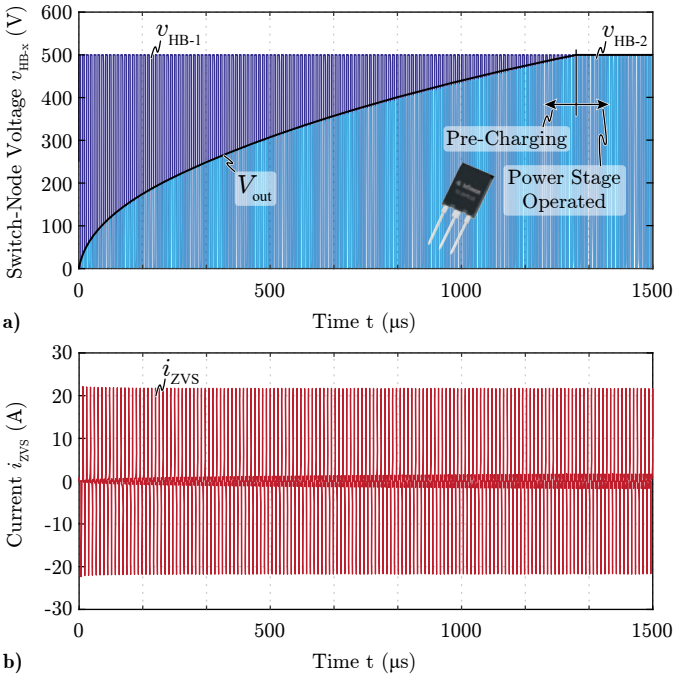


Fig. 7.15: a) Simulated switch-node voltages during a pre-charging sequence with initial input and output voltages of 500 V and 0 V, respectively. **b)** Corresponding simulated current i_{ZVS} during the pre-charging sequence.

input-to-output voltage ratios. In order to achieve the same ZVS behavior and synchronized switch-node voltages of the primary and secondary-side half-bridges, it just needs to be ensured, that the primary-side referred effective capacitance of the secondary-side power switches $C_{\text{eff,sec}}/n_{\text{ZVS}}^2$ equals the effective capacitance of the primary-side power semiconductors $C_{\text{eff,pri}}$. This can be achieved by increasing the smaller C_{eff} by means of additional ceramic capacitors, which are connected in parallel to the power switches. By doing so, the Q_{oss} of both half-bridges can be equalized and the ZVS auxiliary circuit can be operated in the same way as previously explained for equal power switches.

Until now, only the advantages of the proposed ZVS auxiliary circuit have been discussed. However, besides the topology-inherent benefits of unrestricted functionality with respect to the operating conditions, as e.g. DC-link voltage, switching frequency, and output power, there are of course also disadvantages of this topology. Thus, besides the increased system complexity due to the additional active circuitry and, therefore, lower reliability of the overall converter system, the suitability of the proposed concept for a certain application highly depends on the converter topology and the given specifications. Hence, if the output voltage range and/or the switching frequency range are not too wide, it could be more efficient to use an alternative, passive ZVS concept, as e.g. the magnetizing current of the main transformer, whereby there is no reason to use the more complex ZVS auxiliary circuit anymore. However, this can easily be estimated based on Fig. 12, where the distribution of the switching losses with the auxiliary circuit are shown.
Hence, assuming a certain given dead time t_{d}, the hysteresis losses P_{hys} are approximately the same for all ZVS concepts and cannot be avoided. Consequently, the additional losses due to the ZVS auxiliary circuit alone are given by P_{aux}, which therefore need to be compared to the losses of an alternative ZVS concept (hereafter referred to as P_{alt}). In the example of using the magnetizing current i_{m} for achieving ZVS, P_{alt} would correspond to the additional conduction losses in the power switches and the main transformer T_1 due to i_{m}. Hence, if P_{aux} should be larger than P_{alt}, the alternative ZVS concept is the more promising solution and should therefore be used, especially if it is more reliable and/or more cost-effective than the proposed circuit.
Nevertheless, if an extremely small series-resonant inductance should be employed and, therefore, synchronous switch-node voltages are required, even a certain efficiency penalty due to the employment of the proposed ZVS auxiliary circuit might be acceptable, if in turn the power density and the efficiency of the main transformer T_1 can be improved.

Furthermore, the application of the proposed ZVS auxiliary circuit is of course not limited to the simple DC-transformer topology of Fig. 7.1. Moreover, it can be applied to all different kinds of topologies, where two half-bridges are operated synchronously. Thereby, it does not matter, whether the two half-bridges are both located in the same converter port or in different ports of the converter, as long as the Q_{oss} of one half-bridge can be directly transferred to a second half-bridge, which therefore needs to be switching at the same time. However, if the two half-brides are in the same converter port, the auxiliary circuit processes reactive power only, whereby the advantage of the pre-charging of the output capacitor is lost. Consequently, the arrangement where the two half-bridges are in different converter ports should be preferred if possible.
Generally, it can be stated that the proposed ZVS auxiliary circuit is most suitable in applications, where ZVS for a wide output voltage range and/or a wide switching frequency range needs to be ensured, without increasing the control effort of the actual converter system. However, if in a certain application an alternative, passive ZVS concept is equally efficient as the proposed active ZVS circuit, the passive concept should be preferred, as it is usually the more reliable and more cost-effective solution. Nevertheless, as in all operating conditions, only the absolutely necessary ZVS energy is processed by the proposed auxiliary circuit, it allows for utilizing cost-effective Si superjunction MOSFETs up to comparably high switching frequencies. This is an important advantage over conventional, passive ZVS concepts, where the large Q_{oss} of Si superjunction MOSFETs demands for large circulating reactive currents, such that ZVS is guaranteed under all operating conditions. These currents, however, yield significant conduction losses, reducing the achievable converter efficiency significantly, especially for low output power values.

7.3 Summary of the Chapter

In this chapter, a simple auxiliary circuit has been proposed and analyzed, which ensures soft-switching of a series-resonant converter (SRC) by transferring the energy stored in the C_{oss} of the primary-side power switches to the C_{oss} of the secondary-side power transistors, by means of a resonant transition. Consequently, there is no need for storing magnetic energy in the main transformer, neither in the series-resonant inductance, nor in the magnetizing inductance, as ZVS is guaranteed by the proposed auxiliary circuit. Hence, an extremely small series-resonant inductance can be employed,

which facilitates the design of the power converter with a very efficient PCB-winding transformer, where the series-resonant inductor is integrated as leakage inductance. Furthermore, the structure of the ZVS auxiliary circuit inherently guarantees, that only the absolutely necessary amount of energy for ZVS is transferred from the primary to the secondary side, independent of the momentary output power and voltage level. This is a huge advantage compared to conventional approaches, where either the magnetizing current of the main transformer, or the load current in the series-resonant inductor is used to achieve ZVS of the power switches. Additionally, due to the resonant operating mode of the auxiliary circuit, there is hardly any additional control required, as the appropriate operation of the circuit is ensured by means of circuit design.

The suitability and performance of the proposed auxiliary circuit have been tested and measured based on two hardware demonstrators for both, GaN and Si superjunction power switches. For both types of switches, a significant improvement in terms of efficiency could be observed, whereby especially for Si switches, a remarkable amount of switching losses can be saved. Consequently, the proposed circuit allows for using cost-effective superjunction silicon MOSFETs up to comparably high switching frequencies.

Finally, it has been shown, that the auxiliary circuit can also be used for pre-charging the output capacitor of the power converter, in order to adapt the output voltage to the input voltage before starting the operation of the main power circuit.

8

Conclusion and Outlook

Nowadays the share of electric vehicles (EVs) in the automotive market is rapidly increasing, as people are more aware of the fact that the global carbon dioxide emissions need to be drastically reduced in order to get back to a sustainable energy utilization. Thus, the environmental awareness of the end customers, in combination with the affordability of modern EVs, yielded significantly growing sales figures in recent years, whereby this market segment became more and more attractive to companies, which were previously focusing on vehicles with conventional combustion engines only. However, this inevitably led to an increasingly competitive market, which is why the respective products underlie an extreme cost pressure, while they still need to perform at least equally well as the competitors. These two main aspects are targeted by the research presented in this work, where the total manufacturing costs of two separate power electronic converter systems of state-of-the-art EVs (cf. Fig. 1.1) should be minimized, without any performance penalty.

There are two different approaches pursued in the course of this work: On the one hand, an optimization on a system level is conducted, where the two independent converter systems are integrated into a single power electronic device, whereby the power density is significantly improved and the total component count is reduced. Hence, by merging the two aforementioned systems, many components as e.g. transformer, power semiconductors, heat sink, etc., which have previously been employed in both converter systems, are only required once in the combined device, whereby the overall manufacturing costs can be drastically reduced.

On the other hand, a more detailed optimization on a component level is conducted, whereby each power component is optimized with respect to cost and power density, e.g. by integrating the windings of the inductive

components in to the main PCB.

8.1 Results and Conclusions

The three-port DC/DC converter system, which is investigated within this work, has to provide a wide output voltage range on the high-voltage (HV) port (250 V…500 V), allowing for operating the converter with a HV battery at an arbitrary charge level, and it needs to cope with very high output currents in the low-voltage (LV) port (up to 200 A), in order to cover the LV power peaks during drive mode operation. Furthermore, galvanic isolation between all three converter ports needs to be ensured.

In a first step, the most promising and most versatile conventional three-port converter topology (TAB) has been investigated in detail, and the arising challenges due to the aforementioned specifications have been identified. It has been found that, even though the TAB could theoretically be used for the application at hand, various topology-inherent issues make it extremely difficult to design a power-dense and sufficiently efficient TAB for the given specifications. Consequently, instead of using the non-ideal TAB topology and trying to find an optimal design, which might just meet the targeted efficiency requirements, completely new topological approaches have been developed based on the previously identified issues of the TAB topology. These new topologies are ”tailored” to the specifications of the application at hand and are discussed in the following.

The first proposed three-port DC/DC converter topology utilizes a simple synchronous rectifier in the LV port, as this circuit has been found to be the only one, which can easily be operated with low port voltages and extremely large output currents. This has been experimentally verified by means of a 3 kW 500 V/15 V hardware demonstrator of a two-port series-resonant converter, where a winding-integrated synchronous rectifier in the LV port has been employed. The hardware demonstrator just met the targeted partial load efficiency of 95 % with a power density of 17.9 kW/L.
Besides the LV-side synchronous rectifier, a new five-winding transformer structure is used in the proposed three-port converter, which allows for utilizing additive and subtractive superposition of magnetic flux linkages in the different windings. The special structure of the transformer yields a perfect decoupling of the HV and the LV output power values during charge mode

(CM) operation, whereby the control of this converter is significantly easier than the one of the TAB. Finally, the transformer structure has been extended by means of a sixth winding, whereby operating mode dependent turns ratios are achieved and the drive mode (DM) efficiency of the complete converter system can be significantly increased.
The suitability of the proposed topology has finally been verified by means of a simple 1 kW hardware demonstrator, which easily meets the targeted full-load efficiency in CM of 95 % with a peak efficiency of 95.9 % for nominal port voltages. However, in DM the converter misses the targeted partial-load efficiency of 95 % by 1 %, as the concept of operating mode dependent turns ratios has not been used in this hardware demonstrator. Nevertheless, for the same power density, the partial-load efficiency would be way above 95 % if the aforementioned concept would be used, which is why this topology is perfectly suitable for the application as combined EV charger.
The only drawback of this topology is the large number of semiconductors, which is why a second topology has been developed, where this issue is mitigated.

The second three-port DC/DC topology has been developed with a special focus on reducing the number of power components. This has been achieved by a synergetically controlled series-resonant converter (SRC) between the PFC and the HV port, and an additional phase-shifted full-bridge equivalent circuit in the LV port. Hence, in this topology, the previously mentioned synchronous rectifier in the LV port cannot be used anymore, which is why the full-load efficiency in DM is much lower compared to the efficiency which can be achieved with an appropriately designed synchronous rectifier. However, in DM the full-load efficiency is of less importance than the realization costs, as long as the converter can withstand the thermal stressed due to the occurring losses. In contrast, the full-load efficiency in CM is comparably high, as the converter is mainly operated as DC-transformer, thus as a SRC with unity voltage gain.
The suitability of this topology has been verified by means of the final 3.6 kW 500 V/500 V/15 V hardware demonstrator with a power density of 16.4 kW/L (cf. Fig. 8.1), which is only slightly lower than the one of the 3 kW two-port series-resonant converter (17.9 kW/L). The converter easily meets the efficiency targets of 95 % in both, full-load operation in CM and partial-load operation in DM.

Besides the system level optimization, also the individual components of the converter have been investigated with regard to reducing their manufacturing costs. Of course, the costs of the different semiconductor materials

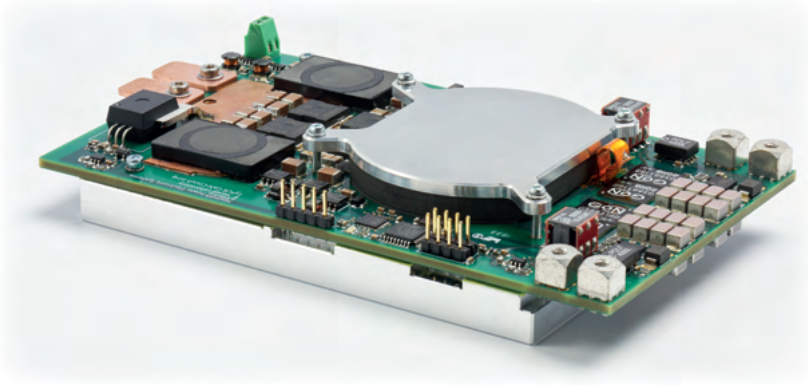


Fig. 8.1: Side-view of the hardware prototype of the final 3.6 kW three-port converter system.

cannot be influenced, but the topologies might be adapted in a way, such that more cost-effective semiconductors can be employed. Hence, as the proposed converter topologies are all based on comparably expensive GaN switches in the high-voltage ports, a simple zero-voltage-switching (ZVS) auxiliary circuit has been investigated, which allows for utilizing the cheaper silicon superjunction MOSFETs in SRCs up to comparably high switching frequencies. The proposed auxiliary circuit ensures ZVS for arbitrary switching frequencies, arbitrary port voltages, works independent of the output power, only processes the absolutely necessary power to achieve ZVS, and ensures perfectly synchronized primary- and secondary-side switch-node voltages in the SRC. Thus, not only cheaper Si MOSFETs can be used, but the synchronization of the switch-node voltages allows for utilizing extremely small series-resonant inductors, which is why the small leakage inductance of PCB-winding transformers can be used instead of bulky discrete external inductors.

However, in converter systems with widely varying port voltages, discrete inductors can hardly be avoided, which is why their design has been optimized as well by means of the proposed compensating fringing field concept. Hence, the fringing field around one or multiple air gaps is used to partially compensate the parasitic magnetic skin and proximity fields in the winding, whereby extremely low high-frequency conduction losses result and power-dense and cost-effective discrete inductors can be built. The effectiveness of the concept has been verified by means of multiple hardware prototypes

of inductors, and it has further been used in the hardware demonstrators of Chapter 4 and Chapter 6.

8.2 Future Research and Outlook

This work mainly focused on the development and the experimental verification of new ideas, both in terms of converter topology as well as in terms of component design. However, future investigations need to pay more attention to the actual hardware implementation of the proposed topologies and design concepts, as a reliable thermal management and a proper manufacturing of highly integrated converter systems is an extremely challenging task. Hence, in such converter systems, the PCB is no longer used to solely interconnect multiple components and to serve as a mechanical base plate, but it is an integral part of the converter system itself, as it is used for e.g. the windings of the magnetic components, for the EMI filter by means of shielding layers, for heat spreading and distribution, and much more. Consequently, all these tasks need to be considered in the design of the PCB of the converter, whereby in the application at hand, the very high currents in the LV port add another challenging task. Hence, in order to optimally use the proposed converter topologies in an industrial product, multiple hardware iterations and/or extensive detailed 3D FEM simulations of the PCBs would be required, whereby the achievable power densities and efficiencies could be significantly improved. In addition, recent advancements in the PCB technology, as e.g. cost-effective copper inlays or even the direct integration of semiconductor chips in the PCB, open up a whole new world of possibilities regarding PCB integration of converter systems, as large currents in the PCB and heat dissipation through the PCB suddenly become easy.

Furthermore, the ever-increasing performance of wide band-gap semiconductors allows for pushing the switching frequencies to even higher values, whereby at some point the parasitic components of the semiconductor packages and the PCB can be used as e.g. resonant components in resonant converter topologies. Thus, the manufacturing costs of these components will be practically gone and extremely cost-effective converter systems can be built. However, in today's GaN switches, the hysteresis losses for charging/discharging the output capacitance of the semiconductors are still extremely high (cf. Fig. 7.12a), which is why some C_{oss}-related technological improvements are required before going for the aforementioned high switching frequencies.

Appendices

A

Accurate Calculation of the PCB-Winding Inductor Core Dimensions

In the following, the calculation of the optimal core dimensions for the PCB-winding inductors of Chapter 3 is explained.

A.1 Derivation of the Design Equations for the Inductor Core

Based on the required magnetic core cross-section A_C of the inductor, the radius r_C of the center leg of the ferrite core can directly be calculated according to

$$r_C = \sqrt{\frac{A_C}{\pi}}. \tag{A.1}$$

If the flux density in the outer core limbs should be the same as in the center leg, the total core cross-section of the outer core limbs needs to be equal to A_C. Thus, each outer core limb needs a minimum cross-section A_o of

$$A_o = \frac{A_C}{4} = \frac{r_C^2 \pi}{4}. \tag{A.2}$$

However, the area A_o depends on various design parameters as e.g. the outer core radius r_{out}, the width of the thermal interfaces b_{th} as well as the total side length l_C of the core (cf. Fig. 3.25). The width b_{th} can easily be calculated based

on the thermal model of the winding and the maximum allowable thermal resistance of one thermal interface $R_{\mathrm{th,T}}$ (cf. (3.23)) according to

$$b_{\mathrm{th}} = \frac{l_{\mathrm{w}}}{\lambda_{\mathrm{eff}} \cdot h_{\mathrm{PCB}} \cdot R_{\mathrm{th,T}}}. \tag{A.3}$$

Furthermore, the outer radius r_{out} is given as

$$r_{\mathrm{out}} = r_{\mathrm{C}} + 2d_{\mathrm{clr}} + b_{\mathrm{w}}, \tag{A.4}$$

where $d_{\mathrm{clr}} \approx 1\,\mathrm{mm}$ denotes the required clearance between the ferrite core and the PCB-winding. As the area of one outer core limb A_{o} is defined as

$$A_{\mathrm{o}} = l_{\mathrm{C}}^2 - r_{\mathrm{out}}^2\pi + b_{\mathrm{th}}k - 2l_{\mathrm{C}}b_{\mathrm{th}} + 4r_{\mathrm{out}}^2 \tan^{-1}\left(\frac{b_{\mathrm{th}}}{k}\right), \tag{A.5}$$

with

$$k = \sqrt{4r_{\mathrm{out}}^2 - b_{\mathrm{th}}^2}, \tag{A.6}$$

the total width l_{C} of the inductor core can be calculated according to

$$l_{\mathrm{C}} = b_{\mathrm{th}} + \sqrt{b_{\mathrm{th}}^2 + A_{\mathrm{o}} + r_{\mathrm{out}}^2\pi - b_{\mathrm{th}}k - 4r_{\mathrm{out}}^2 \tan^{-1}\left(\frac{b_{\mathrm{th}}}{k}\right)}. \tag{A.7}$$

Hence, all required geometrical dimensions have been found and the core can be designed accordingly.

B

Calculations for the Optimization of the Resonant Tanks of the Three-Port DC/DC Converter

In the following, the calculations of the optimal resonant tanks in charge mode (CM) and drive mode (DM) for the three-port DC/DC converter topology of Chapter 5 are explained.

B.1 Derivation of the Optimal Component Values for the Resonant Tanks in CM

The duty cycle limit of $D_+ + D_- \leq 0.5$ inherently yields an upper limit for the allowable L_{CM}/C_{CM} ratio. Even though there is no closed form solution for calculating the optimal L_{CM}/C_{CM} ratio analytically, the solution can still be found numerically based on the following set of equations

$$x = \frac{C_{CM}}{L_{CM}} \tag{B.1}$$

$$a(x) = \frac{\pi\sqrt{x}P_{HV} \cdot (V_{PFC} - 2V'_{LV}) + 2xV_{PFC}V'_{LV} \cdot (V_{PFC} - V'_{LV})}{1/2\pi\sqrt{x}P_{HV} + xV'_{LV} \cdot (V_{PFC} - V'_{LV})} \tag{B.2}$$

$$b(x) = \frac{\pi\sqrt{x}P_{HV} \cdot (2V'_{HV} - 3V_{PFC}) + 2xV_{PFC}V'_{HV} \cdot (V'_{HV} - 2V_{PFC})}{1/2\pi\sqrt{x}P_{HV} + xV'_{HV} \cdot (2V_{PFC} - V'_{HV})} \tag{B.3}$$

$$f_0(x) = |a(x) - b(x)|, \tag{B.4}$$

which were all derived based on (5.20), (5.21) and $T = 1/f_{\mathrm{res,CM}}$.
Hence, the optimal $C_{\mathrm{CM}}/L_{\mathrm{CM}}$ ratio and, therefore, x_{opt} is found for $f_0(x_{\mathrm{opt}}) = 0$, where

$$P_{\mathrm{HV}} = \frac{P_{\max}}{2} \tag{B.5}$$

$$V_{\mathrm{PFC}} = \max\left(V_{\mathrm{PFC}}\right) \tag{B.6}$$

$$V'_{\mathrm{HV}} = \frac{n_{\mathrm{PFC}}}{n_{\mathrm{HV}}} \cdot \max\left(V_{\mathrm{HV}}\right) \tag{B.7}$$

$$V'_{\mathrm{LV}} = \frac{n_{\mathrm{PFC}}}{n_{\mathrm{LV}}} \cdot \max\left(V_{\mathrm{LV}}\right). \tag{B.8}$$

Consequently, based on $x_{\mathrm{opt}} = C_{\mathrm{CM}}/L_{\mathrm{CM}}$ and $f_{\mathrm{res,CM}} = 1/2\pi\sqrt{L_{\mathrm{CM}}C_{\mathrm{CM}}}$, the optimal component values can be calculated according to

$$L_{\mathrm{CM}} = \frac{1}{2\pi\sqrt{x}f_{\mathrm{res,CM}}} \qquad \text{and} \qquad C_{\mathrm{CM}} = \frac{\sqrt{x}}{2\pi f_{\mathrm{res,CM}}}. \tag{B.9}$$

B.2 Derivation of the Optimal Component Values for the Resonant Tank in DM

Compared to CM operation, in DM, not only the L/C ratio of the resonant tank components needs to be optimized, but also the optimal resonant frequency $f_{\mathrm{res,DM}}$ needs to be found. Furthermore, the additional constraint of the maximum allowable capacitor voltage $V_{\mathrm{C,max}}$ needs to be considered, whereby the resonant capacitance C_{DM} can be directly calculated according to

$$V_{\mathrm{C,max}} = \frac{1}{2} n_{\mathrm{HV}} V_{\mathrm{LV}} \tag{B.10}$$

$$Q_{\mathrm{C,max}} = \frac{P_{\mathrm{LV,max}} n_{\mathrm{HV}}}{4 f_{\mathrm{res,CM}} V_{\mathrm{LV}}} \tag{B.11}$$

$$C_{\mathrm{DM}} = \frac{Q_{\mathrm{C,max}}}{2 V_{\mathrm{C,max}}}. \tag{B.12}$$

Based on this C_{DM}, the optimal resonant frequency $f_{\mathrm{res,DM}}$ of the resonant tank can be calculated, such that for a switching frequency of $f_{\mathrm{res,CM}}$ and the maximum output power P_{LV}, the converter is operated at the boundary between DCM and CCM.

This can be ensured by numerically minimizing $f_{0,\mathrm{DM}}(f_{\mathrm{res,DM}})$ according to

$$L_{\mathrm{DM}}(f_{\mathrm{res,DM}}) = \frac{1}{(2\pi f_{\mathrm{res,DM}})^2 C_{\mathrm{DM}}} \tag{B.13}$$

$$\alpha = \frac{\sqrt{L_{\mathrm{DM}} C_{\mathrm{DM}}}}{T} \tag{B.14}$$

$$D_{\mathrm{DM}} = \alpha \cdot \cos^{-1}\left(\frac{4C_{\mathrm{DM}}V'_{\mathrm{LV}}V_{\mathrm{HV}}^2 - 4C_{\mathrm{DM}}V'^2_{\mathrm{LV}}V_{\mathrm{HV}} + P_{\mathrm{LV}}TV_{\mathrm{HV}} - 2P_{\mathrm{LV}}TV'_{\mathrm{LV}}}{V_{\mathrm{HV}} \cdot (4C_{\mathrm{DM}}V'_{\mathrm{LV}}V_{\mathrm{HV}} - 4C_{\mathrm{DM}}V'^2_{\mathrm{LV}} + P_{\mathrm{LV}}T)}\right) \tag{B.15}$$

$$X = 2\sin\left(\frac{D_{\mathrm{DM}}T}{\sqrt{L_{\mathrm{DM}}C_{\mathrm{DM}}}}\right) V'_{\mathrm{LV}} \cdot (V_{\mathrm{HV}} - V'_{\mathrm{LV}}) \tag{B.16}$$

$$\beta = \cos\left(\frac{D_{\mathrm{DM}}T}{\sqrt{L_{\mathrm{DM}}C_{\mathrm{DM}}}}\right) \tag{B.17}$$

$$Y = 2\beta V'^2_{\mathrm{LV}} + 2V_{\mathrm{HV}}V'_{\mathrm{LV}} - 2V_{\mathrm{HV}}V'_{\mathrm{LV}}\beta - V_{\mathrm{HV}}^2\beta \tag{B.18}$$

$$t_0 = -\tan^{-1}\left(\frac{X}{Y}\right)\sqrt{L_{\mathrm{DM}}C_{\mathrm{DM}}} + D_{\mathrm{DM}}T \tag{B.19}$$

$$f_{0,\mathrm{DM}}(f_{\mathrm{res,DM}}) = \left|t_0 - \frac{T}{2}\right|, \tag{B.20}$$

with $T = 1/f_{\mathrm{res,CM}}$. Hence, if $f_{0,\mathrm{DM}}(f_{\mathrm{res,DM}})$ equals zero, the optimal resonant frequency $f_{\mathrm{res,DM}}$ is found and L_{DM} can be calculated according to

$$L_{\mathrm{DM,opt}}(f_{\mathrm{res,DM}}) = \frac{1}{(2\pi f_{\mathrm{res,DM}})^2 C_{\mathrm{DM}}}. \tag{B.21}$$

Consequently, the optimal resonant tank is found, which guarantees minimal conduction losses and at the same time a stable converter operation for all operating conditions, if a constant switching frequency of $f_{\mathrm{res,CM}}$ is used.

C

PCB-Winding Integrated Transformer Design

The main advantage of PCB-winding transformers, compared to conventional wire-wound transformer structures, is the coplanar arrangement of the different windings. This coplanar arrangement yields an inherent mutual compensation of the parasitic magnetic skin and proximity fields among the windings, whereby very low AC to DC resistance ratios of the windings can be achieved. Consequently, PCB-winding transformers are especially suited for cost-sensitive high frequency applications in the low to medium power range. In high power applications, where large RMS currents are flowing in the transformer windings, the limited available copper cross-section in PCB-windings restrict the applicability of these transformers. However, at least on the top and the bottom layer of the PCB, additional copper foils can be soldered to the PCB layers, in order to extend the range of application for this kind of transformers.

Furthermore, the leakage inductance of PCB-winding transformers is extremely small, due to the inherent close coupling between the individual windings. Even though this might be beneficial in some applications, it is often more adverse than helping, as in many converter applications a certain leakage inductance is desirable, in order to omit the use of an additional external inductor. As the close coupling between the windings is inherently given, and can only be loosened by reducing the aforementioned mutual compensation of the magnetic fields, a large leakage inductance in a PCB-winding transformer always comes at the expense of additional conduction losses. Thus, instead of artificially increasing the leakage inductance of the PCB-winding transformer it is more efficient to develop a new topology, which can be operated with the small natural leakage inductance of a PCB-winding

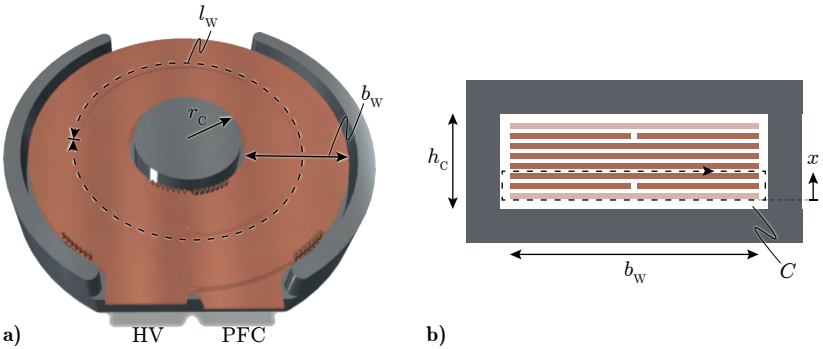


Fig. C.1: a) Design of a three winding PCB-winding transformer, where only the HV and the PFC winding are shown. The third (LV) winding comprises two parallel connected single turn windings on the top and the bottom layer. **b)** Cross-section view of the PCB-winding including the contour C, which is used for the calculation of the magnetic field strength $H(x)$.

Tab. C.1: Number of turns per layer within the 8-layer PCB for the three windings: PFC, HV and LV.

Top	Mid 1	Mid 2	Mid 3	Mid 4	Mid 5	Mid 6	Bottom
1x LV	2x HV	1x HV	1x HV	1x PFC	1x PFC	2x PFC	1x LV

transformer. Such a topology was derived and introduced in Chapter 6. Nevertheless, by proper placement and arrangement of the PCB-windings, even in a PCB-winding transformer a certain leakage inductance can be achieved. The calculation of the respective leakage inductance and the ideal placement of the windings are discussed in the following section.

C.1 Leakage Inductance Calculation in PCB-Winding Transformers

The leakage inductance of an arbitrary transformer structure can be calculated by integrating the product of the magnetic flux density B and the magnetic field strength H within the winding volume according to

$$L_\sigma \cdot I_T^2 = \int_V B \cdot H \, \mathrm{d}V. \tag{C.1}$$

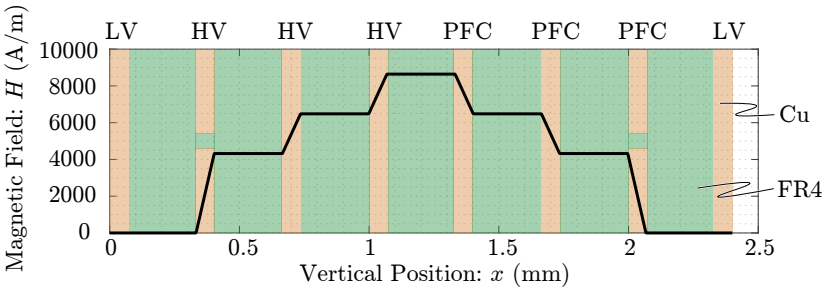


Fig. C.2: Magnetic field strength $H(x)$ in the proposed PCB-winding transformer for current flow in the PFC and the HV winding only (used for calculation of the leakage inductance between the PFC and the HV winding).

Thus, assuming a PCB-winding transformer structure as shown in Fig. C.1a, with three coplanar windings PFC, HV and LV (not shown), a winding width of b_w and a mean length of a turn of l_w, (C.1) can be simplified to

$$L_\sigma \cdot I_\mathrm{T}^2 = \int_\mathrm{V} B \cdot H \,\mathrm{d}V = \mu_0 l_\mathrm{w} b_\mathrm{w} \int_0^{h_\mathrm{PCB}} H(x)^2 \,\mathrm{d}x, \tag{C.2}$$

where a homogeneous magnetic field strength $H(x)$ along b_w and l_w is assumed. This approximation is valid, if the total winding area is covered by ferrite plates as illustrated in Fig. C.1a. The missing parts of the yoke at the terminations do not influence the magnetic field strength $H(x)$ too much, as the magnetically effective path in air (b_w, cf. (C.3)) is not significantly lengthened ($+\frac{h_\mathrm{c}}{2}$). Consequently, for the calculation of L_σ, only the magnetic field strength $H(x)$ needs to be known, which can easily be calculated by Ampères Law according to

$$\oint_\mathrm{l} \vec{H} \,\mathrm{d}\vec{l} = I \quad \rightarrow \quad H(x) = \frac{I_\mathrm{C}}{b_\mathrm{w}}, \tag{C.3}$$

where I_C denotes the enclosed current in the contour C, as shown in Fig. C.1b. Thus, for a turns distribution according to Tab. C.1 and a power flow from the PFC to the HV port, a magnetic field strength $H(x)$ as illustrated in Fig. C.2 can be found. For x in regions with FR4 material, $H(x)$ stays constant, as there is no current flow in FR4 regions, which would contribute to I_C. However, in each copper layer, $H(x)$ increases linearly as there is more and more current accumulated in C. The gradient of this increase depends on the number of

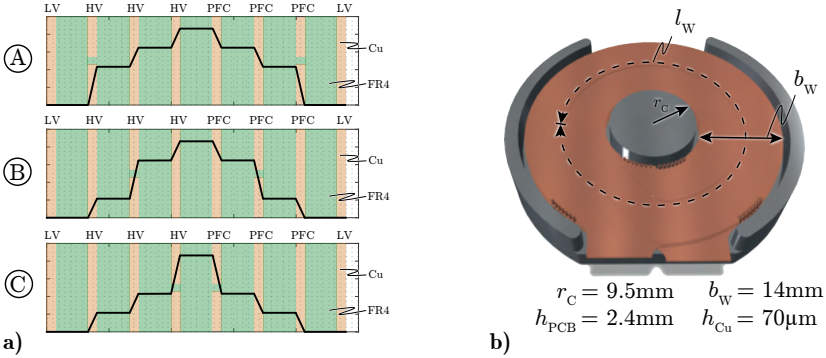


Fig. C.3: a) Magnetic field strength $H(x)$ for three different winding arrangements (number of turns: A = 12111121, B = 11211211 and C = 11122111), and **b)** dimensions of the transformer, which were used for the calculation of the leakage inductance $L_{\sigma,\text{PFC}\rightarrow\text{HV}}$.

turns in this specific layer and is calculated according to

$$\frac{\mathrm{d}H(x)}{\mathrm{d}x}(k) = \frac{N(k) \cdot I_\mathrm{T}}{b_\mathrm{w}}, \tag{C.4}$$

where $N(k)$ and I_T denote the number of turns on layer k and the transformer current, respectively.
Combining (C.2) with (C.3) yields

$$L_\sigma \propto h_\mathrm{PCB} \cdot \frac{l_\mathrm{w}}{b_\mathrm{w}} = h_\mathrm{PCB} \cdot \left(\frac{2\pi r_\mathrm{core}}{b_\mathrm{w}} + \pi \right), \tag{C.5}$$

where r_core denotes the radius of the center leg of the core. Consequently, two simple fundamental scaling laws can be derived: First, for a large leakage inductance, an as thick as possible PCB should be chosen, in order to maximize the area beneath the $H(x)$ curve. Second, by increasing the winding width b_w, the leakage inductance is reduced. Thus, surprisingly, it is much easier to achieve a large leakage inductance in a small PCB-winding transformer than in a larger one (for a certain required core area).
Finally, the third determining factor of the leakage inductance is the turns distribution withing the PCB (cf. Tab. C.1). In order to illustrate the impact of the number of turns per winding on the achievable leakage inductance of a transformer, the three different arrangements of Fig. C.3a have been

calculated for the transformer dimensions given in Fig. C.3b.
The corresponding calculated leakage inductance values are

$$L_{\sigma,\mathrm{A}} = 131.6\,\mathrm{nH}, \qquad L_{\sigma,\mathrm{B}} = 112.6\,\mathrm{nH} \quad \text{and} \quad L_{\sigma,\mathrm{C}} = 81.0\,\mathrm{nH}, \tag{C.6}$$

which were verified by means of FEM simulations (maximum deviation $< 4\,\%$).
The same winding arrangements can also be calculated for a PCB thickness of 1.55 mm, whereby the following leakage inductance values are found:

$$L_{\sigma,\mathrm{A}} = 83.1\,\mathrm{nH}, \qquad L_{\sigma,\mathrm{B}} = 71.0\,\mathrm{nH} \quad \text{and} \quad L_{\sigma,\mathrm{C}} = 50.9\,\mathrm{nH}. \tag{C.7}$$

Consequently, a reduction of the PCB thickness by 35 % yields approximately the same reduction in leakage inductance, as expected based on (C.5).
Based on these results, it can easily be seen, that in conventional PCB-winding transformers, without any further effort to increase the leakage inductance by loosening the coplanar current flow, only very small leakage inductance values are achieved. As a result, converter topologies with only minimal requirement for leakage inductance values should be sought, where the limitations of PCB-winding transformers can be accepted and their benefits can be fully utilized.

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