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The GOOGLE Little Box Challenge - Ultra-Compact GaN-Based Single-Phase DC/AC Power Conversion

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Technology is destructive only in the hands of people who do not realize that they are one and the same process as the universe.

– Alan Watts

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Abstract

With the ambition of achieving a cost reduction in solar power and microgrid technology, an increased efficiency of Uninterruptible Power Supplies (UPS) or the ability to use an electric vehicle's battery as backup power during a power outage, Google and IEEE initiated the Google Little Box Challenge (GLBC) back in July 2014 to build the worldwide smallest 2 kW / 450 V DC / 240 V AC single-phase PV inverter with $\eta > 95\,\%$ CEC weighted efficiency and an air-cooled case temperature of less than 60 °C by using latest power semiconductor technology and innovative converter concepts, advertising $1 million prize money. The challenging specifications and the attractive prize money created a remarkable interest in the power electronics community, which led to the participation of 2000+ teams – companies, research institutes and universities – in the GLBC. Finally, 100+ teams submitted technical descriptions of realized systems. Out of these applications, 18 finalists including ETH Zurich were invited to submit their hardware prototypes for final testing.

This dissertation reports all major findings and key lessons learned from the participation of the Power Electronic Systems Laboratory (PES) of ETH Zurich in the GLBC and during the research conducted afterwards to investigate encountered problems which could not be analyzed in detail because of the tight schedule of the competition. The power-density benchmark established by the realized inverter prototypes and considering the achievements of other GLBC finalists, indicates that a 20 times higher power-density compared to the current state-of-the-art in industry is principally possible. All necessary aspects to realize an extreme power-density converter in accordance with the GLBC specifications are discussed. First, a review of suitable converter topologies and advanced control concepts and component technologies to achieve a high power-density, adopted by the GLBC finalists and/or described in the scientific literature, is provided. Different bridge-leg control techniques (e.g. constant frequency PWM vs. Triangular Current Mode (TCM)), the selection of WBG power transistors, the implementation of compact High Frequency (HF) inductors and the selection of suitable capacitors, are discussed among other relevant topics.

Guided by the insights from a preceding multi-objective design optimization (virtual prototyping), two hardware implementations of the Little Box inverter concepts developed at ETH Zurich are presented and accompanied with experimental results to support the claimed performances with respect to efficiency, η, and power-density, ρ. The initial prototype implementation, a GaN based full-bridge inverter with TCM control and variable switching

frequency up to the MHz range, was ranked among the top ten contributions of the GLBC finalists. The continued research following the conclusion of the GLBC in October 2015, resulted in an improved understanding of key technologies and allowed to further improve component models for more accurate Pareto optimization results. Novel experimental methods to accurately determine the soft-switching losses in GaN and SiC semiconductors, to characterize the behavior of ceramic capacitors subject to a large-signal excitation at low-frequencies and to analyze unexpectedly high core losses in multi-airgap MnZn ferrite inductors, developed for the first version of the Little Box inverter, are reported. By means of the gained insights and the consideration of an alternative inverter concept, i.e. a DC/|AC|-buck converter operated with constant 140 kHz PWM and a subsequent low-frequency unfolding inverter, an improved version of the Little Box inverter, almost twice as compact as the initial version, is realized.

Because of the fluctuating power with twice the mains-frequency intrinsic to single-phase AC systems, active power buffer concepts with additional auxiliary converters are employed in the developed Little Box inverter systems in order to substitute bulky electrolytic capacitors and shrink the volume of the necessary energy storage element to compensate the fluctuating power. In particular, two promising concepts, a full-power processing buck-type and a partial-power processing Series Voltage Compensator (SVC)-type power buffer, are comparatively evaluated. The investigated partial-power auxiliary converter approach is subsequently also applied to a 380 V DC / 48 V DC series-resonant LLC converter, where a novel control concept achieves tight output voltage regulation for changing input voltage without varying the switching frequency or duty-cycle of the main DC/DC converter. Since the auxiliary converter only processes a small share of the rated power, only a marginal $\eta\rho$-impairment of the overall converter must be accepted compared to a system with constant voltage transfer ratio.

In conclusion, the main research findings and lessons learned over the course of the dissertation are summarized and an outlook on expected future power-density improvements is provided including a discussion of necessary advances of the involved component technologies. Finally, further insights on the origin of the observed excess cores losses in multi-airgap inductors and a comprehensive comparison of two promising ceramic capacitor technologies to implement ultra-compact power pulsation buffers are provided in the Appendices.

Kurzfassung

Mit dem Bestreben eine Kostensenkung von Solarsystemen und Inselnetzen zu erreichen, die Effizienz von unterbrechungsfreien Stromversorgungen zu steigern oder die Batterie von Elektrofahrzeugen zur Stromversorgung bei Netzausfällen verwenden zu können, haben Google und IEEE im Juli 2014 die Google Little Box Challenge (GLBC) mit dem Ziel lanciert mit Hilfe modernster Halbleitertechnologien und innovativer Konverterkonzepte den weltweit kleinsten 2 kW / 450 V DC / 240 V AC Wechselrichter zu realisieren. Dabei musste der Wechselrichter eine Mindesteffizienz grösser 95 % gemäss kalifornischer Gewichtung (CEC) aufweisen und die Gehäusetemperatur des luftgekühlten Systems durfte maximal 60 °C erreichen. Motiviert durch diese herausfordernden technischen Spezifikationen und das attraktive Preisgeld von 1 M$ haben weltweit 2000+ Teams, darunter Firmen, technische Berater und Universitäten, am Wettbewerb teilgenommen und über 100 Teams technische Beschreibungen ihres gebauten Systems eingereicht wovon 18 Finalisten ausgewählt wurden ihren Prototypen für finale Tests bereitzustellen. Die vorliegende Doktorarbeit beinhaltet alle wichtigen wissenschaftlichen Erkenntnisse und Erfahrungen aus der Teilnahme der Professur für Leistungselektronik der ETH Zürich an der Little Box Challenge an sich sowie an der finalen Ausscheidung und der weiterführenden Analysen von Problemen die während des Wettbewerbs aufgetreten waren aber, auf Grund des engen zeitlichen Rahmens des Wettbewerbs, nicht genauer analysiert werden konnten. Die unter Berücksichtigung der entwickelten Systeme und der Ergebnisse anderer GLBC Finalisten angegebenen Leistungsdichtekennwerte, deuten darauf hin dass, verglichen mit derzeitigen Systemen der Industrie, eine 20-fache Erhöhung der Leistungsdichte möglich ist.

Die Arbeit diskutiert alle notwendigen Aspekte und Schlüsseltechnologien zum Erreichen einer extrem hohen Leistungsdichte von Wechselrichtern mit Little Box Spezifikationen. Einleitend wird ein Überblick über geeignete Wechselrichter-Schaltungsstrukturen, fortschrittliche Steuerverfahren und Komponententechnologien gegeben welche entweder von den Finalisten der GLBC verwendet wurden und/oder in der wissenschaftlichen Fachliteratur beschrieben sind. Verschiede Verfahren zur Steuerung der Konverter-Halbbrücken (z.B.: PWM oder Triangular Current Mode – TCM), die Auswahl moderner Leistungshalbleiter mit breitem Bandabstand, die Implementierung kompakter Hochfrequenzdrosseln oder die Auswahl geeigneter Kondensatoren, sind Beispiele relevanter und näher diskutierter Themen. Den Erkenntnissen einer vorab durchgeführten Mehrkriterien-Designoptimierung (virtuelle Prototypenerstellung) folgend, werden zwei hochkompakte an der ETH Zü-

rich entwickelte „Little Box“ Wechselrichter vorgestellt und die berechnete Effizienz, η, und Leistungsdichte, ρ, mittels experimenteller Ergebnisse bestätigt. Der erste entwickelte Prototyp, ein auf GaN Halbleitertechnologie basierender Vollbrücken-Wechselrichter mit TCM Modulation und variabler Schaltfrequenz bis in den MHz-Bereich, erreichte eine Platzierung unter den 10 besten Systemen im Finale der GLBC.

Die fortgesetzte Forschung nach Abschluss der GLBC im Oktober 2015, führte auf ein vertieftes Verständnis der verwendeten Schlüsseltechnologien und ermöglichte eine Verbesserung der Komponentenmodelle was wiederum eine genauere Systemoptimierung ermöglichte. Entsprechend werden neue experimentelle Verfahren zur hochgenauen Bestimmung der Verluste bei weichem Schalten von GaN und SiC Leistungshalbleitern, zur Charakterisierung von Keramikkondensatoren bei niederfrequenter Grosssignalanregung und zur Analyse erhöhter Kernverluste in Induktivitäten mit verteiltem Luftspalt, welche für den ersten Little Box Prototypen entwickelt wurden, vorgestellt. Durch diese weiteren Erkenntnissen und durch Berücksichtigung eines alternativen Wechselrichterkonzeptes – eines Wechselrichters basierend auf einem DC/|AC|-Tiefsetzsteller betrieben mit 140 kHz konstanter Schaltfrequenz und einer nachgeschalteten niederfrequenten Umklappstufe – wurde schliesslich eine zweite Ausführung der Little Box mit nahezu zweifach höherer Leistungsdichte realisiert.

Aufgrund der bei Einphasennetzen prinzipbedingten Pulsation der Leistung mit doppelter Netzfrequenz, wurden im Rahmen der GLBC aktive Konzepte mit zusätzlichem Hilfskonverter verfolgt um sperrige Elektrolytkondensatoren zu vermeiden und somit das Volumen des, zur Kompensierung der Pendelleistung benötigten, Energiespeicherelementes zu reduzieren. Insbesondere werden in der vorliegenden Arbeit zwei eine Reihe von Vorteilen aufweisende Verfahren, ein auf einem Tiefsetzsteller basierendes Konzept welches die gesamte Pendelleistung verarbeitet und ein auf einem Serienspannungskompensator basierendes Konzept wo der Hilfskonverter nur einen kleinen Teil der gesamten Pendelleistung verarbeitet, im Detail analysiert und miteinander verglichen. Das untersuchte Hilfskonverterkonzept mit Serienspannungskompensator findet nachfolgend auch bei einem 380 V / 48 V LLC Serien-Resonanz Konverter Anwendung. Dort wird mittels eines neuartigen Regelkonzeptes und eines Hilfskonverters die 48 V Ausgangsspannung unabhängig von Änderungen der Eingangsspannung eng geregelt ohne dabei die Frequenz oder das Tastverhältnis des Hauptkonverters verändern zu müssen. Da der Hilfskonverter nur einen kleinen Teil der Nennleistung verarbeiten

muss, weist das Gesamtsystem eine sehr hohe Effizienz und Leistungsdichte auf.

Abschliessend werden die wichtigsten Erkenntnisse der einzelnen Forschungsarbeiten zusammengefasst und es wird die Möglichkeit einer zukünftigen weiteren Steigerung der Leistungsdichte behandelt bzw. werden die dafür notwendigen Fortschritte und zukünftigen Anforderungen an Komponententechnologien diskutiert. Anhänge mit weiteren Erkenntnissen bezüglich des Ursprungs der erhöhten Kernverluste in Induktivitäten mit verteiltem Luftspalt und ein fundierter Vergleich zwischen zwei vielversprechenden Keramikkondensatortechnologien zur Implementierung hochkompakter Hilfskonverter zur aktiven Pendelleistungskompensation schliessen die Arbeit ab.

Abbreviations

AC	Alternating Current
CEC	California Energy Commission
CM	Common Mode
CMV	Common Mode Voltage
CTE	Coefficient of Thermal Expansion
DM	Differential Mode
DMV	Differential Mode Voltage
DC	Direct Current
DCT	DC Transformer
DSC	Digital Signal Controller
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FCC	Flying Capacitor Converter
FP	Full-Power
FP-PCI	Full-Power Parallel Current Injector
FPGA	Field Programmable Gate Array
GLBC	Google Little Box Challenge
GIT	Gate Injection Transistor
HEMT	High Electron Mobility Transistor
HF	High Frequency
HV	High Voltage
LB	Little Box
LBC	Little Box Challenge
LF	Low Frequency
LISN	Line Impedance Stabilization Network
LV	Low Voltage
LUT	Look-Up Table
MAG	Multi Air Gap
MLCC	Multi-Layer Ceramic Capacitor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPC	Multi Point Clamped
OFM	Optimal Frequency Modulation
PCB	Printed Circuit Board
PCI	Parallel Current Injector
PF	Power Factor
PI	Proportional Integral

PWM	Pulse Width Modulation
PPB	Power Pulsation Buffer
PP	Partial-Power
PPC	Partial-Power Converter
PP-SVI	Partial-Power Series Voltage Injector
P^3DCT	Partial-Power Pre-Regulated DC Transformer
PV	Photovoltaic
SVI	Series Voltage Injector
TCM	Triangular Current Mode
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter
WBG	Wide Band-Gap
ZC	Zero Crossing
ZCD	Zero Crossing Detection
ZVS	Zero Voltage Switching

Contents

1

Introduction

It is without question that humanity is facing an unprecedented environmental crisis with potentially devastating outcome. With mankind's current resource consumption, the Earth generation capacity is exceeded already by a factor of 1.7 and this is expected to worsen significantly over the next decades because of the growing world population, the development of a middle-class in many developing countries and the anticipated loss of the Earths production capacity because of anthropogenic climate change. It is therefore inevitable that working towards sustainability will become the leading global Megatrend in the near future. Expedited by the falling cost of solar and lithium-ion battery technology, power electronics will therefore strengthen its position as a key enabling technology in the zero-carbon generation and conversion of electric energy. During the last decades, the advances in power semiconductors and microelectronics have been – besides innovative topology, modulation and control concepts – the driving force for the development of new power electronic converters towards higher compactness/power-density, efficiency and cost reduction [1]. In particular, wide-bandgap (WBG) power semiconductors are expected to bring a significant improvement of the performance of converter systems. Following this idea, Google and IEEE launched the Google Little Box Challenge (GLBC, [2]) in 2015 aiming for a massive enhancement of the power-density of a 2 kVA / 400 . . . 450 VDC / 230 VAC single-phase converter compared to state-of-the-art technology, advertising $1 million prize money.

1.1 Technical Specifications of the Google Little Box Challenge

In order to qualify for the competition, a minimum power-density of $\rho > 50\,\mathrm{W/in^3}$, a California Energy Commission (CEC) weighted efficiency,

$$\begin{aligned}\eta_{\mathrm{CEC}} =& 0.04 \times \eta_{10\,\%} + 0.05 \times \eta_{20\,\%} + 0.12 \times \eta_{30\,\%} + 0.21 \times \eta_{50\,\%} + \\ & 0.53 \times \eta_{75\,\%} + 0.05 \times \eta_{100\,\%},\end{aligned}$$

of greater than 95 %, an air-cooled case temperature of $T_\mathrm{c} < 60\,^\circ\mathrm{C}$, and a minimal system lifetime of $t_\mathrm{L} > 100\,\mathrm{h}$ were defined. The key inverter specifications of the LBC are listed in Tab. 1.1 and the specified converter test setup is depicted in Fig. 1.1. The DC input voltage of the Little Box was specified to be 450 V with a 10 Ω resistor inserted between the DC source and the converter input as illustrated in Fig. 1.1. The purpose of the 10 Ω resistor specified in the test setup is to emulate the $v - i$ relationship of a PV module and to decouple the DC source, V_s, from the inverter. Since the input voltage

Tab. 1.1: Key inverter specifications of the GOOGLE Little Box Challenge.

Parameter	Requirement
Input Voltage Source	$450\,\mathrm{V_{dc}}$ with $R_\mathrm{s} = 10\,\Omega$
Output Voltage & Frequency	$240\,\mathrm{V_{rms}}/60\,\mathrm{Hz}$
Maximum Apparent Output Power S	2 kVA
Power Factor	0.7 ... 1, lead & lag
Maximum Load Steps	500 W
Power Density	$> 3\,\mathrm{kW/dm^3}$ ($> 50\,\mathrm{W/in^3}$)
CEC Efficiency	≥95 %
Lifetime (Test Duration)	> 100 h
Max. Outer Enclosure Temperature	≤ 60 °C
DC Input Voltage Ripple (120 Hz)	≤ 2.5 % (i.e. ≤ 10 V pk-pk)
DC Input Current Ripple (120 Hz)	≤ 20 % (i.e. ≤ 1 A pk-pk)
Ground/Leakage Current	≤ 50 mA (initially ≤ 5 mA)
Electromagnetic Compliance	FCC Part 15B/CISPR 11 Class B
AC Output Voltage/Current THD	<5 %

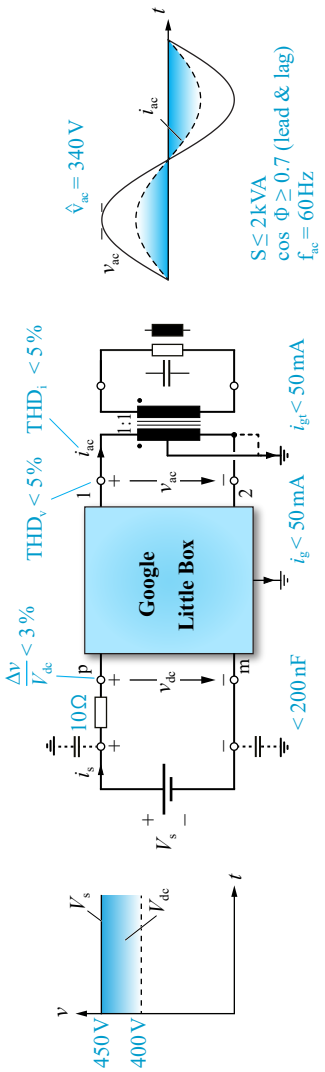


Fig. 1.1: Google Little Box Challenge test configuration with specified 10 Ω input resistor and 1 : 1 isolation transformer at the output.

ripple was strictly limited to 2.5 %[1], $\Delta v_{\mathrm{dc,pp}} \leq 2.5\,\% \, \overline{v}_{\mathrm{dc}} = 10\,\mathrm{V}$ pk-pk, it was necessary to include an energy storage element in the Little Box inverter in order to buffer the fluctuating power at the AC side intrinsic to single-phase power conversion systems. The specified maximum output power is 2 kVA with a Power Factor (PF) between 0.7 – 1, leading or lagging, and the inverter must be able to handle stepwise load variations as high as 500 VA. Due to the inserted 10 Ω resistor, v_{dc} reduces with increasing load from 450 V DC at idle operation to 400 V DC at nominal output power of 2 kVA for PF = 1.

Although the inverter was not required to feature galvanic isolation, for reasons of safety and protection of the test equipment, a 1 : 1 isolation transformer was specified to be inserted between the inverter AC output and the load. Depending on the preference of the contestants, a 240 V split-phase grounding configuration common in North America (indicated with solid lines in Fig. 1.1) or a phase-to-neutral configuration common in Europe (indicated with dashed lines in Fig. 1.1) was possible. The split-phase configuration allows to equally distribute the voltage stress between the Common Mode (CM) capacitors (Y-capacitors) of the EMI filter, which is advantageous when ceramic capacitors with non-linear capacitance-voltage dependency are employed. In order to limit initial inrush currents at the DC input (charging of a storage capacitor) and the magnetizing inrush currents at the AC side, 100 Ω resistors were temporarily inserted between the Little Box and the DC input and the isolation transformer, respectively, and bypassed during regular operation after startup.

Furthermore, electromagnetic compliance according to the rules for "unintentional radiators" as stated in the FCC Part 15 B standard (equivalent to EN 55022/32 Class B, residential equipment) was required. For the purpose of measuring conducted emissions with an EMI test receiver, a Line Impedance Stabilization Network (LISN) was specified to be inserted between the inverter and the isolation transformer. The emissions were measured at 400 W partial and 2 kW nominal load at unity PF. The ground or leakage current flowing in the wire connecting the converter chassis to ground, i_{g}, and the wire that connects either the split-phase of the isolation transformer or the neutral conductor to ground, i_{gt}, was limited to 50 mA and was not allowed to be exceeded at any time during the prototype testing. It is important to point out that this requirement was revised from the initially specified 5 mA leakage current since the parasitic capacitance (≈ 120 nF, certainly < 200 nF) from the

[1]The input voltage ripple specified in [2] was actually 3.0 %, however, the specified 20 % input current ripple requirement (cf. Tab. 1.1) and the stated $R_{\mathrm{s}} = 10\,\Omega$ input resistor resulted in a more stringent 2.5 % (10 V pk-pk) limit for the maximal permissible 120 Hz input voltage ripple.

positive terminal, p, and negative terminal, m, of the floating DC supply to ground was larger than anticipated. Interestingly, the parasitic capacitance formed between actual PV cells and the grounded metallic module case, in the range of 50 nF/kW – 150 nF/kW for crystalline-Silicon PV cells [3, 4], is in the same order of magnitude. The Total Harmonic Distortion (THD) levels including noise (i.e. including all spectral components besides the fundamental frequency) of the AC output voltage and current were required to be less than 5 % without scrutiny of individual harmonics as specified in grid connection standards such as the IEEE 1547 or IEC 61727.

Besides the technical aspects, the legal terms and requirements of the challenge had to be met, most importantly, the contestants were only allowed to use their own intellectual property (no 3rd party IP or patent infringement).

1.2 Little Box Inverter Research at ETH Zurich

The challenging specifications and the attractive prize money created a remarkable interest in the power electronics community, which led to the participation of 2000+ teams – companies, research institutes and universities – in the GLBC. The original technical requirements of the Google Little Box challenge were posted on the 22nd of July 2014 and revised several times throughout the competition. On the 25th of June 2015, just about one month before the deadline for the submission of the technical approach document – the basis for the selection of up to 18 finalists out of 100+ submitted technical descriptions of realized systems – the ground current limit was relaxed from initially 5 mA to 50 mA because the parasitic capacitance ($\approx$ 120 nF) of the specified laboratory voltage source was higher than originally anticipated. This decision was heavily criticized by many contestants because this suddenly promoted inverter concepts with a Low Frequency (LF) CM voltage at the output because the higher required CM attenuation of the EMI filter could be achieved fairly easy without significant increase in volume by an increase of the installed CM capacitance (Y-capacitors). Since this revision was posted just 4 weeks before the deadline for the submission of the final technical approach document, it was not possible to revise the converter design and competitors which did not select their inverter concept based on preventing the generation of a LF CM voltage at the inverter output perhaps had a strategic advantage.

The Power Electronic Systems Laboratory (PES) at the ETH Zurich, in collaboration with the Fraunhofer Institute for Reliability and Microintegration (FH-IZM) and the Fraza company, was selected as one of the 18 finalists [5],

who presented their final converter prototypes on the 21st of Oct. 2015, and handed over the prototype to the National Renewable Energy Laboratory (NREL), Golden (CO), USA, for final testing.

The achieved power-densities of the selected 18 finalists were mainly in the range of 120 W/in^3 – 220 W/in^3. With this, a distinctly higher performance compared to the minimum specification of 50 W/in^3 according to the state-of-the-art in industry was achieved. The winner of the grand prize of $ 1 Million, whose inverter also passed the 100 hours testing, was announced in Feb. 2016. The winning team from the Belgian company CE+T achieved a power-density of 8.72 kW/dm^3 (142.9 W/in^3) which is – not surprisingly – only slightly higher than the power-density of the converter system developed by ETH Zurich and described in Section 4.2 of this dissertation since (without prior discussions) the same technical approach was followed.

The basic reasoning and decision making which lead to the first implementation of the Google Little Box inverter, referred to as Little Box 1.0 in this work, is described in the following: To meet the specified stringent ground current requirement without the need for bulky CM inductors, ideally no CM voltage at all or at least no LF CM voltage should be generated by the inverter. Due to the superior switching characteristic, latest GaN semiconductor technology should be adopted for the implementation of the HF bridge-legs. Thanks to a close collaboration with Infineon Austria, a generous supply of GaN High Electron Mobility Transistors (HEMTs) with gate injection technique to achieve normally-off operation (Gate Injection Transistor – GIT) was provided throughout the competition. Besides the very low turn-on gate voltage threshold, the internal diode characteristic of the transistors rendered it necessary to develop a sophisticated and robust gate-drive circuit with negative turn-off voltage to prevent parasitic turn-on and provide the required quiescent current to keep the devices permanently in the on-state [6, 7]. Because of the high reverse conduction voltage drop of the GaN transistors, particularly with the applied negative gate voltage bias, anti-parallel 600 V SiC Schottky diodes should be employed in order to minimize conduction losses during dead times. In order to achieve a very high power-density, the switching frequency must be increased substantially compared to state-of-the-art systems in order to shrink all passive components. In order to support high switching frequencies up to the MHz range, Zero voltage Switching (ZVS) must apply throughout the AC period. Then, because of the ultra-fast switching characteristics of WBG and particularly of GaN power transistors, switching losses will be minuscule. Making use of the parasitic output capacitance of the power semiconductors, Triangular Current

Mode (TCM) control can be employed to achieve soft-switching without any additional circuit components. Because of the high resulting current ripple of TCM modulation, interleaving of bridge-legs and the resulting harmonic cancellation promotes a compact bridge-leg output and/or EMI filter. In order to reduce conduction losses and consequently cooling volume, paralleling of GaN transistors and the use of foil winding inductors with exceptionally low DC resistance values is preferable. Because of the high switching frequency, MnZn ferrite core materials with very low core loss densities up to the MHz range are preferred. Due to the fluctuating AC power with twice the mains-frequency intrinsic to single-phase power systems, an energy storage element must be incorporated in the converter. Since electrolytic capacitors occupy a large share of the total volume in conventional single-phase inverter systems, an active approach with auxiliary converter and dedicated buffer capacitor is advantageous. Because of their high energy density, excellent current ripple capability and low power loss, ceramic capacitor technology is favorable over electrolytic capacitors for the implementation of the power buffer and favorable over bulky film capacitors in the EMI filter. Ideally, because of the increased complexity of the control system and the given short time frame of the competition, the active buffer should be a stand-alone unit which can be easily replaced with an electrolytic capacitor bank to have a working back-up solution in case unexpected problems are encountered during the development. Ideally, to keep the engineering effort reasonable, the power stage of the auxiliary converter and the inverter should use the same power transistors.

In retrospect, certain decisions and choices which lead to the implementation of the first Little Box inverter would be clearly made differently now. Problems and difficulties which were encountered during the competition but could not be analyzed in detail because of the short competition time frame, were investigated carefully after the GLBC and are also documented in this dissertation. With the knowledge and insights gained over time in the aftermath of the GLBC, certain aspects of the initial design strategy are invalidated or can be questioned as it will become obvious throughout the chapters of this work. Based on the Pareto optimization with improved and more accurate component models and the consideration of a different inverter topology – the DC/|AC|- buck and LF unfolding inverter – a second version of the Google Little Box inverter was designed and implemented at ETH Zurich over the course of this dissertation. The so called Little Box 2.0 which will be presented in Section 4.3 features almost twice the power-density of the initial version and, interestingly, also achieves about 1 % higher conversion

efficiency with simple constant frequency PWM at a moderate switching frequency of 140 kHz. The achieved performance in terms of efficiency, η, and power-density, ρ, clearly outperforms the winning team of the GLBC.

1.3 Potential Real World Applications of the Google Little Box

In Photovoltaics, high compactness is desired for Module Level Power Electronics (MLPE) including DC/DC string optimizers, microinverters, and electronics for individual module monitoring and protection. The Little Box inverter was often referred to as a microinverter, however, a typical microinverter has an input voltage range of around 25 V – 45 V and is rated for only 250 W – 350 W to accommodate PV modules with 60 and 72 cells, and is not capable of providing reactive power. Recently, to reduce the system cost per watt, several manufacturers are offering microinverter units rated up to 1.2 kW where up to 4 PV modules can be connected to a single inverter (e.g. APSystems, Hoymiles). From this perspective, if a preceding DC/DC boost stage is employed, the findings from the GLBC can be used to realize an ultra-compact microinverter. With respect to the 400 V input voltage range, the Little Box specifications are more representative for a string inverter, although, typical single-phase string inverter ratings are in the range of 3 kW – 8 kW. In this application, ultra-high compactness might be of interest if the inverter is retrofitted in a switchboard with confined space. Other than that, it seems that in the case of string inverters high efficiency is preferred over high compactness.

A further very interesting and also important application of the Little Box inverter research is the off-grid solar generator market, particularly, the electrification of rural communities in sub-Saharan Africa and consequently the alleviation of energy poverty. A solar generator, also referred to as a Solar Homes System (SHS) in the off-grid market, is typically comprised of a PV module, a storage battery (Li-Ion), and a charge controller to effectively and safely charge/discharge the battery. By means of additional power electronics, regulated 12 V and 5 V are provided to the user. Depending on the size of the SHS, ranging from tens to hundreds of Wh, the 12 V outlet typically powers larger DC appliances such as LED lighting, TV, radio, fans, laptops, etc. and the 5 V outlets are commonly used to charge mobile gadgets (cell phone, tablets, flashlights, etc.). The outcome of the Little Box inverter research can be applied to premium SHSs with capacities up to 500 Wh – 2000 Wh, which

are particularly targeted towards local entrepreneurs and small businesses and are equipped with inverters rated at 500 W – 2000 W to supply larger household appliances and power tools. Since the solar generator should be portable and because of logistics, a high power-density of the inverter is desired.

1.4 Aims and Contributions

This dissertation aims to convey all major research findings and engineering experiences gained during and in the aftermath of the GLBC and is intended to provide a sound overview of concepts and method to implement very high power-density converter systems. The implemented hardware prototypes, described in detail in the respective chapters, allow to establish a power-density benchmark and indicate what is possible today in forced-air cooled, kW-scale converter applications by means of latest GaN semiconductor technology, Pareto design optimization (virtual prototyping) and sophisticated control concepts.

1.4.1 Scientific Contributions

In order to facilitate an optimal design of the high power-density converter systems analyzed in this dissertation, having accurate models of the individual components is crucial. For this reason, several research contributions are associated with the characterization of converter components. In particular, a novel calorimetric measurement technique based on accurate temperature rise monitoring was developed in order to characterize the ZVS losses of ultra-fast switching WBG power transistors. Based on the derived measurement setup, a switching loss map of the employed GaN transistor was used in the optimization routines to capture soft-switching losses. In continued research and close collaboration with Infineon Austria, the remaining ZVS losses could be attributed to the lossy charging and discharging of the GaN transistors parasitic output capacitance. Class II MLCCs and the novel CeraLink capacitor technology from TDK feature a high energy density but are challenging to dimension because of the non-linear relationship between capacitance and applied voltage. Particularly in case of the dedicated buffer capacitors installed in active power buffers of the developed Little Box inverter systems, the capacitor voltage typically features a DC bias and a superimposed large-amplitude AC voltage ripple at twice the mains-frequency. To accurately dimension the buffer capacitor and estimate the occurring loss

during operation, a capacitance and loss density map as a function of applied DC bias and superimposed AC ripple was established by means of experimental measurements. During the development of the multi-gap HF inductors employed in the first version of the Little Box inverter system, unexpected high losses in the MnZn ferrite core material were observed. In order to quantify and pinpoint the excess losses to shallow layers on the surfaces of the thin ferrite plates used to implement the multi-gap core structure, a novel measurement technique based on advanced thermography was derived and implemented. The developed method allows to distinguish between core loss densities associated with the bulk and surfaces of the investigated MnZn ferrite plates.

Besides the characterization of components and materials, scientific contributions were made in the area of power converter control. A novel efficiency-optimal bridge-leg frequency control scheme was proposed to combine the merits of Triangular Current Modulation (TCM) and conventional PWM for an increased efficiency in DC/AC power conversion. By means of a variation of the switching frequency and adoption of bridge-leg dead times in quasi-stationary DC/DC operating points, the switching frequency and dead time interval resulting in a minimum loss operation of the power stage was determined and stored in a Look-Up Table (LUT). Furthermore, advanced control schemes were proposed for the regulation of active power buffer circuits. By means of multi-loop cascaded control structures, several objectives such as compensation of the twice mains-frequency pulsating power, maintaining a defined buffer capacitor bias voltage and tight control of the DC-link voltage, were achieved through a single control variable. A novel, high performance output voltage control of a compact, high efficiency series-resonant LLC DC/DC converter was proposed based on an additional partial-power auxiliary converter which adjusts the input voltage applied to the resonant converter. Since the auxiliary converter only processes a small-share of the rated power and the resonant converter is kept in its optimal operating point, the overall efficiency and power-density is only marginally affected by the auxiliary converter. Throughout the course of this dissertation, a variety of ultra-compact power electronics prototype systems were realized to validate the proposed concepts and/or support the claimed $\eta\rho$-performances obtained from virtual prototyping (Pareto optimization). Most notably, two versions of the Google Little Box inverter systems described below in Subsection 1.4.2 were realized and rigorously tested in the laboratory. Based on the comparison with other Little Box inverter systems described in literature, a $\eta\rho$-performance benchmark is established. Moreover, based on the technical

approaches selected by other GLBC finalists and the scientific literature, this dissertation provides an overview of applicable topologies, technologies and concepts to realize ultra-compact single-phase DC/AC converter systems.

In summary, the following major research contributions were established over the course of this dissertation:

- Development of a novel calorimetric measurement technique based on accurate temperature rise monitoring to characterize the Zero Voltage Switching (ZVS) losses of ultra-fast switching WBG power transistors.
- Characterization and performance benchmark of ceramic capacitor technologies subject to a large-signal excitation at twice the mains-frequency typically present in active power buffers.
- Development of a measurement technique to quantify and distinguish between bulk and surface core losses in multi-gap inductors based on advanced thermography.
- Introduction of a novel concept to regulate a series-resonant LLC DC/DC converter (DC Transformer) by means of an additional partial-power auxiliary converter.
- Optimal design and hardware implementation of two selected DC/AC converter concepts in accordance with the GLBC requirements and comparative evaluation of the achieved $\eta\rho$-performance by means of experimental results.
- Optimal design and hardware implementation of two ultra-compact active power buffer concepts and comparative evaluation of the achieved performance by means of experimental results.
- Derivation and implementation of a novel efficiency-optimal modulation scheme for an inverter based on local loss minimization in quasi-stationary DC/DC operating points.

1.4.2 Implemented Hardware Demonstrators

During the course of this dissertation the following hardware demonstrators were realized:

- **Little Box 1.0**: The initial version of the Google Little Box developed at ETH Zurich in 2015 and submitted for testing in the final round of

the Google and IEEE Little Box competition. The prototype features a power-density of 8.18 kW/dm^3 (134 W/in^3) and a rated efficiency of 96.3 %. The converter is based on a full-bridge topology with interleaved bridge-legs and uses TCM modulation to achieve ZVS throughout the AC period. The bridge-legs are implemented with GaN HEMT/GIT technology from Infineon. The resulting variable switching frequency is in the range of 200 kHz – 1000 kHz and the system is compliant to all original LBC requirements (5 mA ground current limit).

- **Little Box 2.0**: The revised version of the Google Little Box developed at ETH Zurich. The prototype features a power-density of 14.8 kW/dm^3 (243 W/in^3) and a rated efficiency of 97.2 %. The converter is based on a DC/|AC|-buck and LF unfolding topology and uses 140 kHz constant frequency PWM. The HF bridge-legs are implemented with CoolGaN transistors and the LF unfolder is implemented with e-mode GaN transistors from GaNsystems. The system is compliant to the revised LBC specifications with 50 mA permitted ground current limit.

- **Active Power Buffer Prototypes**: Two variants of a buck-type auxiliary converter which are processing the entire pulsating power were implemented. The first version used in the Little Box 1.0 converter system employs TCM modulation and is equipped with CeraLink capacitors. The second version used in the Little Box 2.0 converter system relies on constant frequency 140 kHz PWM and employs class II MLCC technology. Both variants employ GaN HEMT/GIT technology (Infineon CoolGaN). A third hardware implementation is based on the investigated hybrid-power buffer concept where the size of the installed DC-link capacitance is substantially reduced and the twice mains-frequency voltage ripple, to large to meet the specifications, is eliminated by means of a Series Voltage Compensator (SVC) auxiliary converter which processes only a small share of the entire fluctuating power. The bridge-legs of the SVC are implemented with Low-Voltage (LV) e-mode GaN technology from EPC.

- **P^{3}DCT**: A prototype of a 380 V DC/48 V DC series-resonant converter (DC Transformer, DCT) rated at 1.5 kW was implemented. The output voltage of the converter is tightly regulated by means of an additional auxiliary converter processing only a small share (100 W) of the rated power. The prototype features a power-density of 8.6 kW/dm^3 (141 W/in^3 and a conversion efficiency of 97.7 %. The primary side full-bridge of the resonant converter is implemented with CoolGaN

transistors and the LV side with 60 V OptiMOS transistors. The auxiliary converter is implemented with LV e-mode GaN transistors from EPC.

- **Other Converter Systems**: In order to investigate the effectiveness of passive capacitor balancing schemes particularly during critical operating conditions such as converter start-up, mains outages or short-circuit faults etc., a 5-level Flying Capacitor Converter (FCC) rated at 2 kW was realized in a MSc thesis project. In order to explore the effectiveness of DC/AC power conversion with extreme switching frequencies up to 20 MHz, a Multi-MHz testbed was designed and implemented in a further MSc thesis project.

1.5 List of Publications

Key insights presented in this dissertation have already been published or will be published in international scientific journals and conference proceedings, or have been presented at workshops and professional educational seminars. The publications created as part of this dissertation, or within the scope of closely related projects, are listed below.

1.5.1 Journal Papers

- D. Neumayr, D. Bortis and J. W. Kolar, "The Essence of the Google Little Box Challenge - Part B: Hardware Demonstrators & Comparative Evaluations," *CPSS Transactions on Power Electronics and Applications*, 2020, accepted for publication. [PDF]
- D. Neumayr, D. Bortis and J. W. Kolar, "The Essence of the Google Little Box Challenge - Part A: Key Design Challenges and Solutions," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 2, 2020. [PDF]
- D. Neumayr, D. Bortis and J. W. Kolar, "Comparative Evaluation of a Full- and Partial-Power Processing Active Power Buffer for Ultra-Compact Single-Phase DC/AC Converter Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019, early access. DOI: 10.1109/JESTPE.2020.2987937.
- D. Neumayr, D. Bortis, J. W. Kolar, S. Hoffmann, and E. Hoene, "Origin and Quantification of Increased Core Loss in MnZn Ferrite Plates

of a Multi-Gap Inductor," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 1, pp. 72–93, 2019. DOI: 10.24295/CPSST-PEA.2019.00008.

- D. Neumayr, M. Vöhringer, N. Chrysogelos, G. Deboy, J. W. Kolar, "P3DCT - Partial-Power Pre-Regulated DC Transformer," in *IEEE Transactions on Power Electronics*, Vol. 34, No. 7, pp. 6036-6047, 2019. DOI: 10.1109/TPEL.2018.2879064.

1.5.2 Conference Papers

- D. Neumayr, D. Bortis, E. Hatipoglu, J. W. Kolar, and G. Deboy, "Novel Efficiency-Optimal Frequency Modulation for High Power Density DC/AC Converter Systems," in *Proc. of the 3rd IEEE Intern. Future Energy Electronics Conf. and ECCE Asia (IFEEC - ECCE Asia)*, June 2017. DOI: 10.1109/IFEEC.2017.7992148.

- D. Neumayr, M. Guacci, D. Bortis, and J. W. Kolar, "New Calorimetric Power Transistor Soft-Switching Loss Measurement Based on Accurate Temperature Rise Monitoring," in *Proc. of the 29th Intern. Symposium on Power Semiconductor Devices and IC's (ISPSD)*, June 2017. DOI: 10.23919/ISPSD.2017.7988914.

- D. Neumayr, D. Bortis, J. W. Kolar, and J. Konrad, "Comprehensive Large-Signal Performance Analysis of Ceramic Capacitors for Power Pulsation Buffers," in *Proc. of the 17th IEEE Workshop on Control and Model. of Power Electron. (COMPEL)*, Sept. 2016. DOI: 10.1109/COMPEL.2016.7556762.

- D. Neumayr, D. Bortis, and J. W. Kolar, "Ultra-Compact Power Pulsation Buffer for Single-Phase DC/AC Converter Systems," in *Proc. of the 8th Intern. Power Electronics and Motion Control Conference - (ECCE Asia / IPEMC)*, May 2016. DOI: 10.1109/IPEMC.2016.7512730.

1.5.3 Workshops and Seminars

- D. Neumayr, D. Bortis, J. W. Kolar, M. Guacci, J. Azurza, "Google Little Box Reloaded," presented at the *Intern. Wide-Bandgap Power Electronics Applications Workshop (SCAPE)*, Stockholm, Sweden, May 2019. [PDF]

- D. Neumayr, D. Bortis, M. Guacci, J. Azurza, J. W. Kolar, "Advances in Ultra-Compact GaN Based Single-Phase DC/AC Power Conversion,"

presented at the *STS (Spezial Transformatoren Stockach) Annual Seminar*, Ludwigshafen, Germany, Nov. 2018. [PDF]

- D. Neumayr, D. Bortis, J. W. Kolar , "Mystery Losses in Multi Air Gap (MAG) Inductor and Quantification by means of Advanced Thermometry," presented at the *PSMA Workshop - Power Magnetics @ High Frequency*, San Antonio, TX, USA, Mar. 2018. [PDF]

- J. W. Kolar, D. Neumayr, D. Bortis, "The Google Little Box Challenge - Ultra-Compact GaN- or SiC-Based Single-Phase DC/AC Power Conversion," presented at the *19th European Conference on Power Electronics and Applications (EPE - ECCE Europe)*, Warsaw, Poland, Sept. 2017. [PDF]

- J. W. Kolar, D. Neumayr, D. Bortis, "The Google Little Box Challenge - Ultra-Compact GaN- or SiC-Based Single-Phase DC/AC Power Conversion," presented at the *Intern. Future Energy Electronics Conference (IFEEC 2017-ECCE Asia)*, Kaohsiung, Taiwan, June 2017. [PDF]

- J. W. Kolar, D. Neumayr, D. Bortis, "How to Achieve 200 $\mathrm{W/in^3}$ & Beyond? Concepts - Evaluation - Barriers - Future," presented at the *32nd Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, USA, Mar. 2017. [PDF]

1.5.4 Further Scientific Contributions

- M. Guacci, M. Heller, D. Neumayr, D. Bortis, J. W. Kolar, G. Deboy, C. Ostermaier, and O. Häberlen, "On the Origin of the Coss-Losses in Soft-Switching GaN-on-Si Power HEMTs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 679–694, June 2018. DOI: 10.1109/JESTPE.2018.2885442.

- G. Knabben, D. Neumayr, J. W. Kolar, "Constant Duty Cycle Sinusoidal Output Inverter with Sine Amplitude Modulated High Frequency Link," in *Proc. of the 33rd Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, USA, March 2018. DOI: 10.1109/APEC.2018.8341372.

- P. Papamanolis, D. Neumayr, and J. W. Kolar, "Behavior of the Flying Capacitor Converter Under Critical Operating Conditions," in *Proc. of the 26th IEEE Intern. Symposium on Industrial Electronics (ISIE)*, June 2017. DOI: 10.1109/ISIE.2017.8001319.

- G. Deboy, M. Treu, O. Haeberlen, D. Neumayr, "Si, SiC and GaN Power Devices: An Unbiased View on Key Performance Indicators," in *Proc. of the 62nd IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2016. DOI: 10.1109/IEDM.2016.7838458.

- M. Guacci, D. Neumayr, D. Bortis, J. W. Kolar, G. Deboy, "Analysis and Design of a Multi-Tapped High-Frequency Auto-Transformer Based Inverter System," in *Proc. of the 17th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Trondheim, Norway, June 2016. DOI: 10.1109/COMPEL.2016.7556724.

- D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta\rho$ -Pareto Optimization and Comparative Evaluation of Inverter Concepts considered for the Google Little Box Challenge," in *Proc. of the 17th IEEE Workshop on Control Model. Power Electron. (COMPEL)*, June 2016. DOI: 10.1109/COMPEL.2016.7556767.

- J. W. Kolar, D. Bortis, and D. Neumayr, " The Ideal Switch is Not Enough," in *Proc. of the 28th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, June 2016. DOI: 10.1109/ISPSD.2016.7520767.

- D. Bortis, O. Knecht, D. Neumayr, and J. W. Kolar, "Comprehensive Evaluation of GaN GIT in Low- and High-Frequency Bridge Leg Applications," in *Proc. of the 8th IEEE Intern. Power Electron. and Motion Control Conf. (ECCE Asia)*, May 2016. DOI: 10.1109/IPEMC.2016.7512256.

1.5.5 Patents

- D. Neumayr, J. W. Kolar, G. Deboy, "Power Converter Circuit with a Main Converter and an Auxiliary Converter," United States Patent US2018278167(A1), 2018. [PDF]

- D. Neumayr, D. Bortis, J. W. Kolar, G. Deboy, M. Fahlenkamp, M. Krüger, "Power Converter Circuit with a Switched Mode Power Converter," United States Patent US2018337600(A1), 2018. [PDF]

- D. Neumayr, D. Bortis, M. Guacci, J. W. Kolar, M. Leibl, G. Deboy, "Power Converter Including an Autotransformer and Power Conversion Method," United States Patent US2017373608(A1), 2017. [PDF]

- J. W. Kolar, D. Bortis, M. Kaufmann, A. Tüysüz, D. Neumayr, "Steuerverfahren zur Minimierung der EM-Störaussendung und Verluste mehrphasiger AC/DC-Konverter mit TCM-Betrieb der Brückenzweige (in German)," Swiss Patent CH711454(A2), 2017. [PDF]
- J. W. Kolar, D. Bortis, O. Knecht, F. Krismer, and D. Neumayr, "Inverter zum Austausch elektrischer Energie zwischen einem DC-System und einem AC-System (in German)," Swiss Patent CH711566A2, 2015. [PDF]
- D. Bortis, J. Kolar, F. Krismer, Y. Lobsiger, and D. Neumayr, "Verfahren und Vorrichtung zur Steuerung eines Einphasen DC/AC-Konverters," Swiss Patent CH711423A2, 2015. [PDF]

1.6 Dissertation Outline

According to the goals and contributions mentioned above, the content of the dissertation is divided into five main chapters and conclusions. All the chapters can be read independently since the interdependencies and cross-references have been reduced to the strict minimum.

- **Chapter 2** provides a comprehensive review of applicable topologies, technologies and design considerations to overcome the key challenges of the GLBC. Relevant design considerations, such as constant frequency PWM or Triangular Current Mode (TCM) operation of the bridge-legs, selection of power semiconductor technology, interleaving of bridge-legs, active compensation of the twice mains-frequency power pulsation and sizing of the buffer capacitor, limitation of ground/leakage currents, etc., to achieve an ultra-compact implementation are discussed in detail. Subsequently, two promising inverter concepts to overcome the GLBC, (i) a H-bridge based inverter with DC-link referenced output filter and (ii) a DC/|AC| buck-stage with series-connected low-frequency (LF) |AC|/AC unfolder inverter, are analyzed in detail. Based on a multi-objective $\eta\rho$-Pareto optimization, it is shown that with the DC/|AC| buck-stage operated with 140 kHz PWM and |AC|/AC H-bridge unfolder inverter a power-density of 14.7 kW/dm^3 (240 W/in^3) with a maximum efficiency of 98.1 % at 2 kW output power can be achieved.
- **Chapter 3** describes the analysis and comparative evaluation of two promising power buffer concepts selected from the applicable topologies presented in Chapter 2. First, a full-power processing buck-type

converter active buffer approach, also selected by the 1st prize winner of the Little Box Challenge (LBC), which shifts the power pulsation away from the DC-link to a dedicated buffer capacitor is analyzed in detail. Being relieved from strict voltage ripple requirements, a larger voltage ripple is allowed across the buffer capacitor significantly reducing the capacitance requirement. Second, a partial-power active buffer approach, selected by the 2nd prize winner of the LBC, where conventional passive capacitive buffering of the DC-link is combined with a Series Voltage Injector (SVI) converter to compensate the remaining 120 Hz voltage ripple is analyzed in detail. Both selected concepts are comparatively evaluated in terms of achievable efficiency, power-density and ripple compensation performance under both stationary and transient conditions. Novel control schemes and optimally designed hardware prototypes for both considered buffer concepts are presented and accompanied with experimental measurements to support the claimed efficiency and power-density and assess the performance of the implemented control systems. Finally, by means of comparison with conventional passive DC-link buffering using only electrolytic capacitors, it is determined at what voltage ripple requirement it actually becomes beneficial in terms of volume to employ the considered active buffer concepts.

- **Chapter 4** presents the hardware implementations and novel control concepts of two GaN-based inverter concepts designed and implemented over the course of this dissertation: (i) Little Box 1.0 (LB 1.0), a H-bridge inverter with two interleaved bridge-legs both operated with Triangular Current Mode (TCM) modulation which features a power-density of 8.18 kW/dm^3 (134 W/in^3) and a nominal efficiency of 96.4 % and (ii) Little Box 2.0 (LB 2.0), an inverter topology with single bridge-leg DC/|AC| buck-stage operated with constant frequency PWM and a subsequent |AC|/AC H-bridge unfolder, which features a remarkable power-density of 14.8 kW/dm^3 (243 W/in^3) and a nominal efficiency of 97.4 %. Extensive experimental measurements are provided to verify that all GLBC specifications are met by the implemented prototypes. Moreover, a performance benchmark with other GLBC finalist systems is provided illustrating the outstanding performance of the Little Box 2.0 inverter developed in this dissertation.

- **Chapter 5** describes another use-case of the PPSVC concept discussed in Chapter 3 where the partial-power auxiliary converter is used to

tightly regulate the output voltage of a series-resonant LLC DC/DC converter despite varying input voltage. By means of adjusting the effective input voltage applied to the input of the LLC converter, the output voltage can be stabilized even under harsh load and input voltage transients. High efficiency is achieved because the resonant converter is kept in its optimal operating point and the SVC auxiliary converter, processing only a small share of the total power, has a marginal impact on the overall efficiency. The proposed control concept is verified by means of a 380 V/48 V DC/DC converter prototype. The implemented system is rated for 1.5 kW and features a power-density of 8.6 kW/dm^3 (141 W/in^3).

- **Chapter 6** discusses the origin and quantification of increased core loss in MnZn ferrite caused by surface layer deterioration during machining and manufacturing of thin ferrite plates. In collaboration with Fraunhofer IZM and the Slovenian company Fraza (Fraza d.o.o.), novel ultra-compact multi-gap core foil winding inductors were developed for the first version of the Little Box prototype (LB 1.0). Unfortunately, excessive losses in the multi-gap core limb of the implemented inductors resulted in a much lower quality factor than expected from simulations. In this chapter, the methodology and experimental setup to quantify the encountered excess core losses and pinpoint the origin to shallow surface layers with deteriorated magnetic properties is described thoroughly. Because no effective technique or mechanism (e.g. etching, polishing, annealing) could be identified to restore the magnetic properties in the surface layers of the multi-gap core limb, a conventional HF inductor design with single-gap core and HF litz wire was employed in the revised version of the Google Little Box inverter (Little Box 2.0).

- **Chapter 7** concludes this work and summarizes the key lessons learned and take away messages from the participation in the Google Little Box challenge and the research carried out over the course of this dissertation. Finally, an outlook on the future power-density improvements is provided and the necessary advances and future requirements of the involved component technologies are discussed.

- **Appendix A** provides additional insight on the origin of the observed excess cores losses in multi-gapped MnZn ferrite. Besides the deteriorated surface layers as described in Chapter 6, flux crowding in the core due to tolerances and imperfections in machining and assembly of the ferrite plates was identified as a further cause for the observed increase

in core loss and is analyzed in detail in this chapter. Furthermore, besides the preferred calorimetric surface loss measurement technique used to obtain the experimental results in presented in Chapter 6, an alternative technique to determine surface related core losses based on electrical measurements with the widely accepted two-winding wattmeter method with reactive power compensation is presented in this chapter.

- **Appendix B** presents a large-signal characterization of two promising ceramic capacitor technologies to implement ultra-compact power buffer capacitors, namely TDK's class II/X6S MLCC with $BaTiO_3$ ceramic and TDK's CeraLink with PLZT ceramic. The actual prevailing capacitance of these two types of ceramics strongly depends on the operating point, that is, a DC bias voltage and a superimposed large-signal amplitude AC voltage ripple at twice the mains-frequency. In order to accurately size the buffer capacitor and predict the power losses during operation, a capacitance- and loss-density map is derived from experimental measurements. The obtained capacitance and loss map is used for the virtual prototyping of the active power buffer concepts analyzed in Chapter 3.

2

Key Design Challenges & Solutions to Implement the Google Little Box

Chapter Abstract

In this chapter, the key technical challenges to implement the Google Little Box inverter and the technologies and concepts selected in this dissertation among different options are described in detail. Relevant design considerations, such as constant frequency PWM or Triangular Current Mode (TCM) operation of the bridge-legs, selection of power semiconductor technology, interleaving of bridge-legs, active compensation of the twice mains-frequency power pulsation and sizing of the buffer capacitor, limitation of ground/leakage currents, etc., to achieve an ultra-compact implementation are discussed. Subsequently, two promising inverter concepts to tackle the GLBC, (i) a H-bridge based inverter with DC-link referenced output filter and (ii) a DC/|AC| buck-stage with series-connected low-frequency (LF) |AC|/AC unfolder inverter, are then analyzed in detail. Based on a multi-objective $\eta\rho$-Pareto optimization, it is shown that with the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter operated with 140 kHz PWM a power-density of $14.7\,\mathrm{kW/dm^3}$ ($240\,\mathrm{W/in^3}$) with a maximum efficiency of 98.1 % at 2 kW output power can be achieved.

2.1 Introduction

This chapter explores the 5 key design challenges – component miniaturization, compensation of the 120 Hz DC voltage ripple, EMI and ground current limits, 60 °C maximal surface temperature, and the very short competition time-frame – to implement the Google Little Box inverter, and highlights the design choices and numerous novel concepts proposed in this dissertation. In

Section 2.2, relevant design considerations such as constant frequency PWM or Triangular Current Mode (TCM) operation of the bridge-legs, selection of power semiconductor technology, 2-level vs. multilevel implementation of the bridge-legs, etc., to achieve a component miniaturization are described. In order to drastically shrink the volume of the energy storage required to cope with the twice mains-frequency (120 Hz) pulsating power at the AC side while meeting the stringent 2.5 % DC input voltage ripple, several active power buffering approaches and the dimensioning of the buffer capacitor are discussed in Section 2.3. To meet the specified EMI and ground current limits while minimizing EMI filter volume, different strategies are described in Section 2.4. The implementation of a fan and blower based forced-air cooling system required to dissipate the component losses and keep the temperature of the enclosure and any accessible part of the converter below 60 °C is described in Section 2.5. The benefit of employing virtual prototyping, i.e. carrying out a multi-objective Pareto optimization to identify the best set of system parameters, to meet the short competition time-frame is pointed out in Section 2.6

Subsequently, based on the provided overview of suitable technologies and concepts, two promising inverter topologies, a (i) H-bridge based inverter with DC-link referenced output filter and a (ii) DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter, both equipped with a buck-type Parallel Current Injector (PCI) active power buffer, are then analyzed in detail. In order to comparatively evaluate the performance of the selected inverter concepts, the main findings of a multi-objective $\eta\rho$-Pareto optimization are described in Section 2.7.1. The claimed performance of the optimized inverter systems is then verified and compared to the approaches and achievements of other GLBC finalists by means of implemented hardware prototypes as presented in Chapter 4 of this dissertation.

2.2 Component Miniaturization / High Frequency Operation

In order to drastically shrink the size of the converter bridge-legs and EMI filter passives and break through the status quo in power-density, a high switching frequency in the range of 100 kHz-1 MHz, constituting a factor 10 – 100 increase compared to state-of-the-art Si-IGBT based inverter systems, was selected.

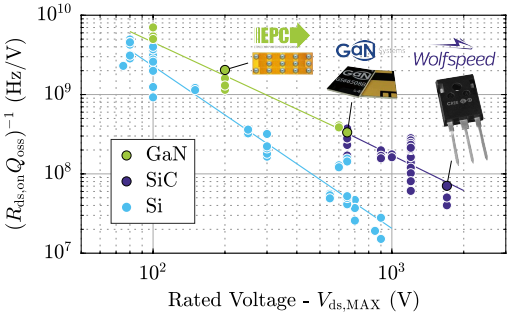


Fig. 2.1: FoM = $\frac{1}{R_{\mathrm{ds,on}}Q_{\mathrm{oss}}}$ for the majority of commercially available Si, SiC and GaN power semiconductors in dependency of the rated blocking voltage [9].

2.2.1 WBG Semiconductors

The unprecedented performance of WBG semiconductor technology enables high switching frequencies and is therefore considered as one of the key technologies for an ultra-compact converter design. To compare the performance of different power semiconductors, the Figure Of Merit (FOM) proposed in [8],

$$\mathrm{FOM}(V) = \frac{1}{R_{\mathrm{ds,on}}Q_{\mathrm{oss}}|_V}, \tag{2.1}$$

is a very useful metric. The charge stored in the transistor's output capacitance, Q_{oss}, allows to roughly estimate the resulting (capacitive) switching losses for hard-switching and the on-state resistance, $R_{\mathrm{ds,on}}$, is representative for the conduction losses. In [9], (2.1) was calculated for over hundred commercially available Si, SiC and GaN power semiconductors and plotted as a function of their rated blocking voltage $V_{\mathrm{ds,max}} = 75\,\mathrm{V} \ldots 1.7\,\mathrm{kV}$ as depicted in Fig. 2.1. It is worth noting that GaN and SiC devices at 650 V rated voltage are comparable in performance and that they clearly outperform Si as a result of their superior physical material properties. So it comes at no surprise that the majority of the GLBC finalist teams employed WBG technology in their converter prototypes: 10 teams were using normally-off GaN High Electron Mobility Transistors (HEMTs) including both p-type gate structure [10] and gate injection technique [11] (Gate Injection Transistor – GIT) devices, 3 teams were using SiC MOSFETs and only 2 teams were using Si MOSFETs. Interestingly, the performance advantage decreases with decreasing voltage

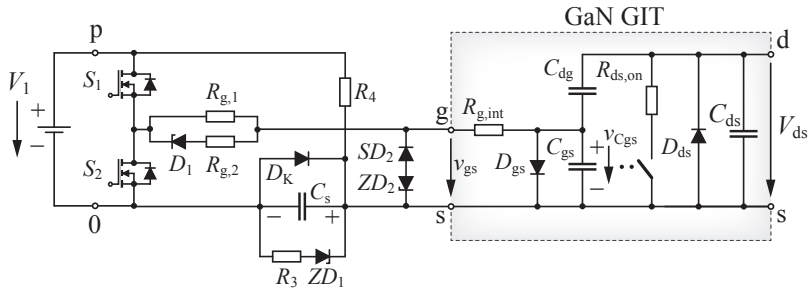


Fig. 2.2: Proposed improved GaN GIT gate drive circuit [6, 7] to guarantee a reliable gate drive operation with consistent performance regardless of duty-cycle and switching frequency.

blocking capability and at 100 V rated voltage, GaN and Si devices are showing similar performance.

Eventually, GaN was selected over SiC in this dissertation, because GaN HEMT technology was available in ultra-compact SMD packages (8 mm × 8 mm × 1.3 mm) allowing to minimize parasitic loop inductances (e.g. power and gate-source loop inductance) and, in combination with an adequate gate drive, achieving lowest possible switching losses. In particular, due to a close collaboration with a large power semiconductor manufacturer, 600 V/70 mΩ GaN GIT devices were at the authors disposal throughout the competition. The very high switching speeds (high $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$), the very low gate-source threshold voltage of $V_{\mathrm{gs,th}} \approx 1.2\,\mathrm{V}$ and the diode characteristic of the gate-source terminals, required a sophisticated and reliable gate drive circuitry which was not met with state-of-the-art concepts. Thus, a new GaN GIT gate drive circuit as depicted in Fig. 2.2 was proposed [6, 7] which (i) allows to generate a bipolar ($\approx +4\,\mathrm{V}/-6\,\mathrm{V}$) gate drive voltage from a single supply voltage, (ii) ensures the required quiescent current of 10 mA to keep the device safely in the on-state, and (iii) enables operation of the gate drive independent of duty-cycle and switching frequency. The performance of the gate drive was verified for switching frequencies up to 1 MHz and the reliability was successfully tested under hard switching conditions with $\mathrm{d}v_{\mathrm{ds,max}}/\mathrm{d}t$ stresses above 500 kV/µs. The reader is referred to [6] for a detailed explanation of the working principle and experimental results.

Although the performance of the latest generation of power devices (including Si) is ever improving, still no “ideal switch” is available on the market.

It is known that GaN HEMTs still suffer from the dynamic on-state resistance phenomena, where the actual on-state resistance of a device during operation is much higher compared to the static $R_{\mathrm{ds,on}}$ specified in the datasheet. This phenomena can be explained by stored and/or trapped charges in the channel of GaN devices, which causes a temporary increase of the drain-source resistance after the transistors are turned on. The magnitude of this temporary resistance increase is to a large extent determined by the applied blocking voltage and becomes worse at high switching frequencies since there is less effective time for the de-trapping process when the on-state resistance returns back to the nominal value. Novel high-fidelity on-state resistance probing circuits were developed in [12, 13] which allow to characterize this behavior of GaN devices. It is e.g. reported in [12], that 200 V GaN HEMTs can exhibit a dynamic on-state resistance of up to a factor of 2.5 higher than what is actually specified in the datasheet provided by the manufacturer. Similar observations are reported in [14] for normally-off 600 V GaN HEMTs.

At 400 V DC-link voltage and 15 A hard-switched current, a dissipated energy in the order of 50 µJ – 60 µJ per totem-pole bridge-leg and switching cycle must be expected for GaN GIT technology [6] which clearly prohibits switching frequencies in the MHz range. With Zero Voltage Switching (ZVS), however, the dissipated energy can be reduced by a factor of about 10 to $\approx$ 5 µJ per bridge-leg and switching cycle [15, 16]. As described in [15, 17, 18], lossy charging and discharging of the power transistor's parasitic output capacitance, C_{oss}, is the reason behind the observed power loss at very high switching frequencies despite employing a soft-switching modulation scheme. In the work presented in [15], ZVS losses of a 600 V GaN HEMT (Infineon CoolGaN) were determined by means of a sophisticated calorimetric measurement setup. It was identified that the dissipated energy per switch and cycle, E_{sw}, is depending approximately linear on the slope of the drain-source voltage, $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$, as shown in Fig. 2.3. By adding an external capacitance $C_{\mathrm{ext}} = 100$ pF (C0G MLCC, considered lossless) in parallel to the tested GaN transistor, the voltage slope across the device is reduced for the same switched current I_{sw}. Still, as can be seen from the figure, the E_{sw} measurements are well aligned. The measured loss of a subsequent experiment with permanently turned off test devices (GaN transistors with negative gate bias connected in parallel to the transistors of an active bridge-leg in order to cycle C_{oss} in a typical manner with high $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$) was in excellent agreement with E_{sw} shown in Fig. 2.3, pinpointing the observed soft-switching losses to the lossy charging/discharging process of C_{oss}. Hence, for a very high switching frequency in the MHz range, the loss contribution of ZVS cannot be neglected: A GaN half-bridge circuit

operating at 1 MHz with a switched current of 15 A (corresponds to 50 V/ns in Fig. 2.3), suffers from a power loss of $P_{sw} \approx 2 \times 1\,\text{MHz} \times 2.7\,\mu\text{J} = 5.4\,\text{W}$. At an operation of several MHz, the switching losses would be detrimental to the efficiency and, because of the increased cooling effort, also to the power-density. On top of that, a potential increase of conduction losses due to the mentioned dynamic $R_{ds,on}$ phenomena must be taken into consideration when operating at very high switching frequencies. Consequently, as will be further elaborated in Chapter 4, high power densities were achieved by many GLBC finalists with moderate switching frequencies of a few hundreds of kHz and, given the super-fast switching characteristics of GaN power transistors without reverse recovery, strictly ensuring ZVS throughout the entire mains period turned out to be not necessary to achieve an ultra-compact inverter design.

2.2.2 Bridge-Leg Control Strategies

By means of the widely accepted Triangular Current Mode (TCM) control technique [19, 20], ZVS of a bridge-leg can be achieved in every operating point throughout the AC period and switching frequencies up to $\approx 1\,\text{MHz}$ can be attained. Depending on the input and output voltage of the bridge-leg (cf. Fig. 2.4(a)), the turn-on and turn-off intervals are computed such that a triangular shape of the filter inductor current results, which features on average over a switching cycle the required output current $\bar{i}_L = i_o$. In addition, the output current direction is reversed before each second switching

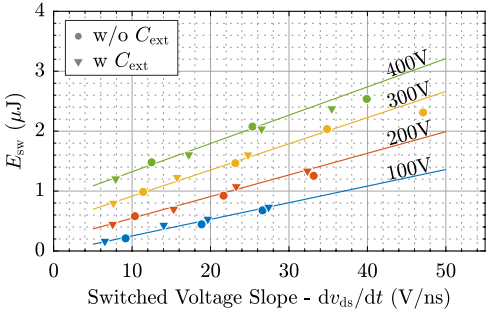


Fig. 2.3: E_{sw} reported in [15] as function of $\mathrm{d}v_{ds}/\mathrm{d}t$ obtained for several switched currents I_{sw} (5 A . . . 20 A) for different V_{DC} voltage levels (100 V . . . 400 V). E_{sw} without (dots) and with (triangles) added capacitance $C_{ext} = 100\,\text{pF}$ are well aligned.

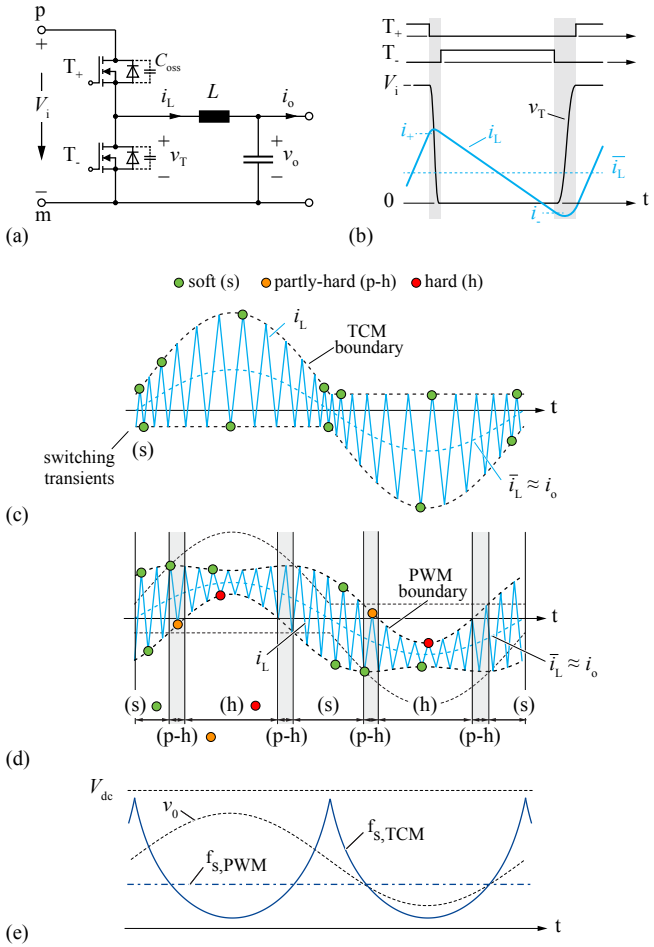


Fig. 2.4: (a) Bridge-leg with DC-link referenced filter (synchronous buck-type converter) explicitly showing the parasitic output capacitance C_{oss} of the power transistors. (b) Detail of the TCM current waveform within a switching cycle. Schematic inductor current waveform over the course of an AC period for (c) TCM control of the bridge-leg where the current to perform ZVS (turn on of T_+/T_- in the positive/negative AC half-cycle) is kept constant and (d) PWM control of the bridge-leg where the constant switching frequency envelope of the inductor current results in different switching transitions: soft-switching (s), partial hard-switching (p-h) and hard-switching (h). (e) Varying and constant switching frequency over the course of the AC period in case of TCM and PWM, respectively.

transition, such that after turning off the previously conducting switch the output current i_L leads to a switching node voltage transition by charging/discharging the parasitic output capacitances, C_{oss}, of the switches and thus the complementary switch can be softly turned-on (cf. Fig. 2.4(b)). To account for the changing operating point, that is output voltage and current, the timing intervals of a switching cycle are adjusted throughout the AC period. One strategy is to keep a constant minimum switched current needed to perform a complete resonant transition within a defined maximum dead time interval as depicted in Fig. 2.4(c). In case of the positive AC half-cycle this minimum current has negative polarity and vice versa. The resulting switching frequency varies over time as illustrated in Fig. 2.4(e).

One of the major challenges is to reliably implement TCM control with switching frequencies up to the MHz range. The difficulty is that (i) there are no compact current transducers available which would satisfy the bandwidth requirements and (ii) conventional microcontrollers are often too slow (difficulty to achieve controller executions at several 100 kHz), are lacking enough PWM resolution and simply don't offer enough flexibility to reliably implement TCM control in the MHz range. For this reason, an approach was implemented in this dissertation where the basic timing intervals (turn-on, turn-off, dead-time) of the bridge-legs are computed by means of a conventional microcontroller at a repetition rate of around 20 kHz and the actual TCM control was then performed by means of an additional FPGA device running at above 200 MHz. Besides the timing signals coming from the microcontroller, the information of the inductor current zero-crossing (ZC) is also considered in the FPGA to cope with measurement and parameter inaccuracies, and delays introduced by the control electronics (gate drive, ZC detector, etc.).

Among several concepts, a magnetic induction based Zero Crossing Detection (ZCD) concept as depicted in Fig. 2.5 was implemented since it features isolation, low complexity and a high Signal-to-Noise Ratio (SNR). In order to saturate the magnetic core already at low currents, a ferrite core material with low saturation flux density, high permeability over a wide frequency range, and a core shape without air gap should be selected. Furthermore, for minimizing losses, the core volume should be as small as possible. The implemented ZCD, based on a R4 toroidal core (R4 $\times$ 2.4 mm $\times$ 1.6 mm) using N30 ferrite from EPCOS and a pick-up coil with $N_s = 10$ turns, was successfully tested at switching frequencies up to 2.5 MHz. Depending on the inductor current slope (di_L/dt), the induced voltage reaches values from 20 V up to 160 V, which makes the ZCD circuit robust against electric disturbances.

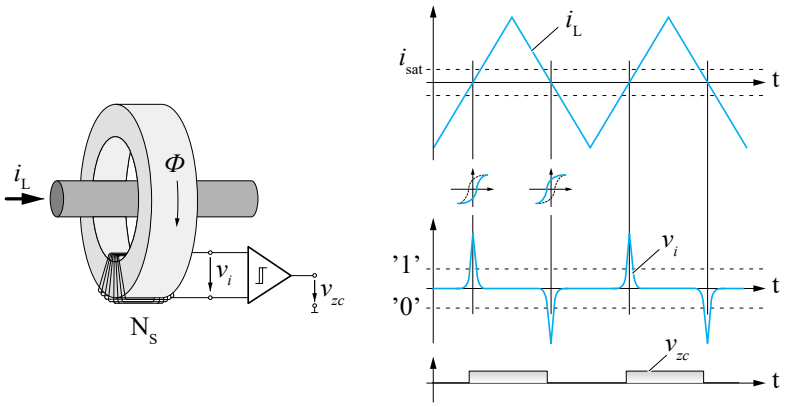


Fig. 2.5: Zero Crossing Detection (ZCD) by means of voltage v_i induced in the pick-up coil (10 turns) when the magnitude of current i_L falls below the saturation threshold i_{sat} of the employed magnetic core.

In contrast to TCM control, conventional PWM features a constant switching frequency (cf. Fig. 2.4(e)) but suffers from high turn-on switching losses which limits the maximal feasible switching frequency. However, this drawback is mitigated by the fact that with a relatively large current ripple, i.e. a design with small filter inductance value, also for PWM the average switching losses can be considerably reduced. As can be seen in Fig. 2.4(d), due to the high current ripple, soft-switching during turn-on and turn-off can be achieved around the fundamental current ZCs also with PWM as long as the switched current maintains a certain minimum value to completely charge/discharge the parasitic output capacitances of the half-bridge (cf. (s) in Fig. 2.4(d)). If the switched current still shows the correct polarity for a resonant transition, but the amplitude is not large enough to complete the resonant voltage transition within the specified dead time, a partial hard turn-on occurs (cf. (p-h) in Fig. 2.4(d)). However, this still causes much lower turn-on switching losses than full hard-switching (cf. (h) in Fig. 2.4(d)) [21]. In this way, switching frequencies of a few hundreds of kHz can be applied for constant frequency PWM with the advantage that typically a microcontroller suffices (no need for ZCD circuitry and FPGA for generating switching signals).

2.2.3 2-Level vs. Multilevel Bridge-Leg

In the past, multilevel converters have been employed primarily in high-voltage/high-power applications to overcome the blocking voltage and current limitations of the involved power semiconductors. Recently, multilevel converters became also a popular choice in low-voltage (400 V) applications, since the higher component count and realization effort can be justified by two key features beneficial to achieve a high power-density: A first major advantage of the multilevel converter is the reduction of volt-seconds applied to the filter inductor and the resulting drastic reduction in filter size. Since the amplitude of the voltage steps applied to the filter inductor is only $\frac{V_{\mathrm{dc}}}{(N-1)}$ and the effective pulse frequency is $(N-1)f_{\mathrm{sw}}$, where N is the number of voltage levels, a multilevel inverter can have an $(N-1)^2$ times smaller filter inductor compared to a 2-level converter at same filter inductor current ripple. Second, the performance of Si and WBG power devices with respect to the FOM given by (2.1) (cf. Section 2.2.1), is inversely proportional to the rated blocking voltage raised to the power of 1.4 – 2.0. According to this scaling law and for the same total switching loss, a multilevel converter can exhibit lower total on-state conduction loss compared to a 2-level implementation, despite that several low-voltage devices are connected in series [22]. In order to implement a larger number of voltage levels (> 5), the cascaded H-bridge, the Multiple Point Clamped (MPC) and the Flying Capacitor (FC, cf. Fig. 2.6) topologies are commonly suggested in literature [23, 24]. Since only a single DC voltage source and no additional clamping diodes are required, the FC multilevel converter is particularly well suited to achieve a high power-density as was demonstrated by one of the GLBC finalists [25, 26].

However, a clear limitation of the multilevel approach is the extra volume occupied by the gate drive circuitry since the stacked power transistors comprising the multilevel bridge-leg require individual control signal and gate drive supply voltage isolation. Furthermore, the capacitor voltage balancing of multilevel converters is crucial as a deviation from the nominal values can lead to harmonics and distortions in the AC output voltage and/or can even lead to system failure. In case of the FC multilevel converter, it is known that with phase-shifted PWM (each switching cell has a dedicated phase-shifted carrier signal) the individual capacitor voltages are passively balanced during stationary operation (natural balancing). However, because of poor balancing dynamics under certain operating conditions, a deviation from the nominal FC voltages is likely to occur during critical operating modes such as load transients and system start-up, and can cause an over-voltage across the transistors and/or permanently damage the system [27]. For the above

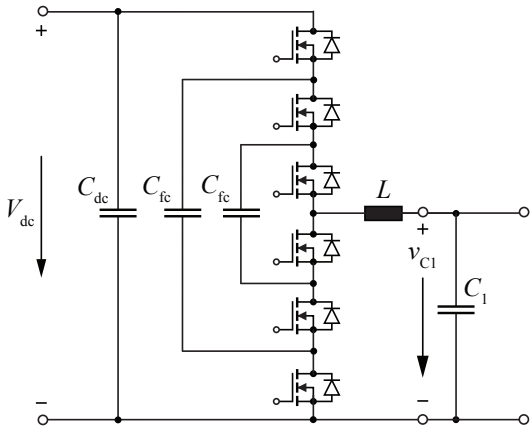


Fig. 2.6: 4-level flying capacitor bridge-leg with LC output filter.

mentioned reasons and due to the performance advantage of 600 V GaN over Si, eventually the conventional 2-level bridge-leg design was selected for the implementation of the Little Box in this dissertation.

2.2.4 Multi-Gap Inductor Design

With reference to Section 2.2.2, the likely operating conditions of a high-frequency (HF) filter inductor in a high power-density inverter – large current ripple and high frequency – demand for a sophisticated design to keep the winding and core losses to a minimum and achieve a low component volume. The large current ripple dictates a very high copper filling factor and the high switching frequencies up to the MHz range demand MnZn ferrite core materials with very low specific core loss density (e.g. DMR51, N87, PC200, 3F4). Inductors realized with highly permeable ferrite materials require a discrete air gap in the magnetic circuit to prevent saturation of the core material and/or to tune the inductance value, unlike iron-powder cores with an inherently distributed gap. This large discrete air gap can be divided into several partial gaps in order to reduce the air gap fringing field and consequently reduce the proximity losses in the winding to promote a very compact design. If the partial gaps are distributed over the entire length of the inner limb of e.g. an E-type or pot core, the H-field in the winding

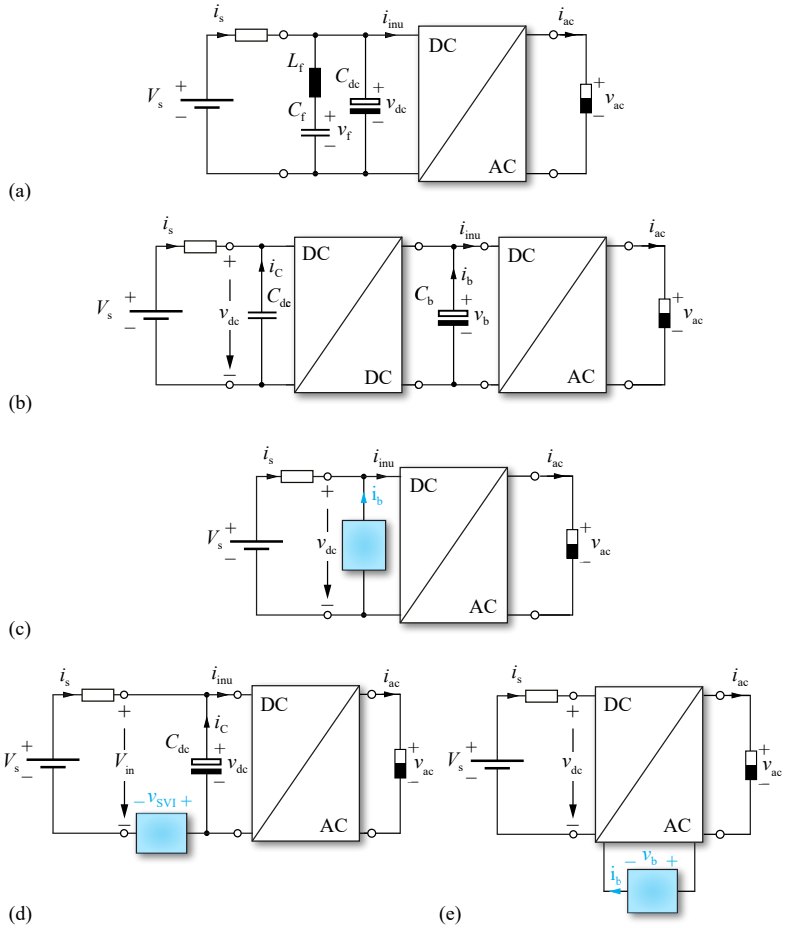


Fig. 2.7: Several passive and active power pulsation buffer approaches to meet the GLBC input voltage V_{in} (= V_{dc}, dependent on the employed power buffer concepts) ripple requirement and reduce the size of the buffer capacitor. (a) Double-line frequency notch-filter. (b) Two-stage approach with preceding DC/DC stage. (c) Parallel Current Injector (PCI) buffer approach. (d) Series Voltage Injector (SVI) compensating the residual fluctuation of the DC-link voltage. (e) Inverter with built-in active power buffer (AC-side).

window shows a quasi one-dimensional distribution running in parallel to the inner limb [28–30]. This promotes to use copper foil for the winding since the individual layers of the foil are aligned in parallel with the H-field and excessive eddy current losses can be avoided. Due to the higher filling factor of foil compared to HF litz wire, a lower winding resistance can be achieved. Unfortunately, as documented in detail in [31] and Chapter 6 of this dissertation, it was identified that the manufacturing of a multi-gap core structure – composed of multiple stacked MnZn ferrite plates – can lead to a large increase of core loss which potentially outweighs the saving in winding loss due to the fringing field reduction.

As a consequence, the number of partial gaps in the implemented multi-gap inductors used in the Little Box 1.0 prototype (LB 1.0, cf. Section 4.2) was reduced from originally 50 to only 24 gaps in the final inductor design in order to lower the resulting core losses. Since no effective measure could be identified to minimize the surface related core losses [31], a conventional single-gap inductor design with HF litz wire (instead of foil) was adopted for the implementation of the Little Box 2.0 (LB 2.0, cf. Section 4.3 of Chapter 4).

2.3 Compensation of the 120 Hz Power Pulsation

One of the key technical challenges in the implementation of the Google Little Box was to shrink the volume of the energy storage required to cope with the twice mains-frequency (120 Hz) pulsating power at the AC side while meeting the stringent 2.5 % DC input voltage ripple. In a conventional inverter design, typically bulky electrolytic capacitors C_{dc} are installed to continuously absorb and release energy,

$$\Delta E = \int_0^{\pi} S \cdot \sin(\varphi) \cdot \frac{1}{2\omega} \mathrm{d}\varphi = \frac{S}{\omega} = 5.3\,\mathrm{J}, \tag{2.2}$$

where S is the apparent power as listed in Tab. 1.1. This fluctuating energy can also be expressed as a function of the capacitor voltage ripple Δv,

$$\begin{aligned} \Delta E &= \frac{1}{2} C_{\mathrm{dc}} \left((V_{\mathrm{dc}} + \Delta v/2)^2 - (V_{\mathrm{dc}} - \Delta v/2)^2 \right) \\ &= C_{\mathrm{dc}} \cdot \Delta v V_{\mathrm{dc}}, \end{aligned} \tag{2.3}$$

which allows to determine the minimum DC-link buffer size as

$$C_{\mathrm{dc}} \geq \frac{\Delta E}{\Delta v V_{\mathrm{dc}}} = \frac{5.3\,\mathrm{J}}{(2.5\,\% \cdot 400\,\mathrm{V}) \cdot 400\,\mathrm{V}} = 1.3\,\mathrm{mF}, \tag{2.4}$$

in order to meet the voltage ripple specification. However, conventionally installed electrolytic capacitors are poorly utilized since only $\frac{\Delta E}{\frac{1}{2} C_{\mathrm{dc}} V_{\mathrm{dc}}^2} = \frac{5.1\,\mathrm{J}}{104\,\mathrm{J}} = 4.9\,\%$ of the average stored energy is actually used for the buffering process.

As an alternative concept to suppress the input voltage ripple, a series resonance $L_{\mathrm{f}} C_{\mathrm{f}}$-circuit constituting a notch-filter at twice the AC frequency could be installed in parallel to the DC-link as shown in Fig. 2.7(a). However, besides the unreasonably large inductance value L_{f}, the main disadvantages of this approach are the high voltages occurring across the filter components and the comparably high losses occurring in L_{f}.

Fig. 2.7(b) shows the typical two-stage configuration known from PV inverter systems, where the first DC/DC stage decouples the buffer capacitor C_{b} from the system input and regulates the input voltage V_{dc} such that the PV module is operated at it's Maximum Power Point (MPP). Since the maximal voltage swing across the buffer capacitor C_{b} is not restricted by the specified 2.5 % input ripple requirement anymore, the size of C_{b} can be significantly reduced. However, the buffer capacitor voltage v_{b} cannot fall below 340 V for a proper operation of the inverter. A clear disadvantage in terms of overall efficiency is that the entire power flowing from the DC-source to the load is being processed by two converter stages.

In order to only cope with the fluctuating power, the usage of additional auxiliary converters in various configurations, typically equipped with a dedicated buffer capacitor exhibiting a wide voltage fluctuation, has been thoroughly studied in literature and a comprehensive overview is given in [32–36].

Main concepts relevant for and/or employed in the GLBC are briefly described in the following. Fig. 2.7(c) depicts the Parallel Current Injector (PCI) approach [37–41], where the buffer converter connected in parallel at the converter DC input injects a current i_{b} to compensate the fluctuating portion of current $i = p_{\mathrm{ac}}/V_{\mathrm{dc}}$ which ideally results in a constant input current i_{s} and consequently in a constant voltage V_{in} at the converter input.

In a different approach as described in [42], depicted in Fig. 2.7(d), and employed by one of the GLBC finalists [43,44], conventional passive capacitive buffering of the DC-link is used, however, the total installed capacitance value is less then what would actually be needed to comply with the 2.5 % voltage ripple requirement. In order to meet the specified input voltage ripple, an

additional Series Voltage Injector (SVI) converter impresses voltage v_{SVI} which compensates the residual 120 Hz voltage ripple still present in v_{dc} resulting in a constant input voltage V_{in}. The key advantage of this concept is that the SVI converter can be implemented with low-voltage (LV) components and only processes a small share of the entire fluctuating power, $\hat{p}_{\mathrm{SVI}} = I_{\mathrm{s}} \cdot \hat{v}_{\mathrm{Cf}} \approx 100\,\mathrm{W}$, since, for a defined DC-link capacitance of around 400 µF – 600 µF, the amplitude of v_{Cf} required to compensate the remaining voltage ripple only amounts to approximately 20 V and $I_{\mathrm{s}} = 5\,\mathrm{A}$ in the nominal operating point (cf. Tab. 1.1). As described in [33, 45, 46], i.e. publications of another GLBC finalist, also the PCI buffer concept (cf. Fig. 2.7(c)) can be realized by means of a partial-power processing auxiliary converter if an additional DC-blocking capacitor (stacked on top of the auxiliary converter and jointly forming the parallel branch) is employed.

Fig. 2.7(e) depicts the AC-side or built-in power buffer concept presented in [35, 47–51], where part of the main inverter circuit and control system is shared with the active power buffer. To give a specific example, in the concept presented in [35, 47], a virtual, unbalanced 3-phase system in established by introducing an additional inverter bridge-leg and connecting the buffer capacitor to the neutral phase of the inverter. Depending on the output power level and power factor, the amplitude and phase-shift of the buffer capacitor voltage v_{b} is adjusted such that the pulsating AC power is compensated.

It should be noted, that regardless of the employed buffer approach, at least 15 µF – 20 µF of capacitance C_{dc} is installed in the DC-link in order to eliminate switching noise and to reduce the commutation loop inductance of the bridge-legs of the inverter stage.

The synchronous buck-type implementation of the PCI buffer concept [37, 40] shown in Fig. 2.8(a) was selected in this dissertation due to several reasons as will be discussed in the following. First, only a single capacitor is needed for the implementation of the buck-type PCI buffer and, as can be seen from the characteristic buffer capacitor voltage waveform of the buck-type PCI in Fig. 2.8(b), operating the auxiliary converter with the minimum buffer capacitance value of

$$C_{b,\mathrm{min}} = \frac{2S_b}{\omega V_{\mathrm{dc}}^2} = 66.3\,\mu\mathrm{F} \tag{2.5}$$

results in a perfect utilization of the buffer capacitor. In order to provide voltage margin to cope with load transients, it is more reasonable to install at least $2 \cdot C_{\mathrm{b,min}}$ which reduces the voltage swing at the buffer capacitor (cf. Fig. 2.8(b)). Second, the GaN bridge-leg design of the main inverter can

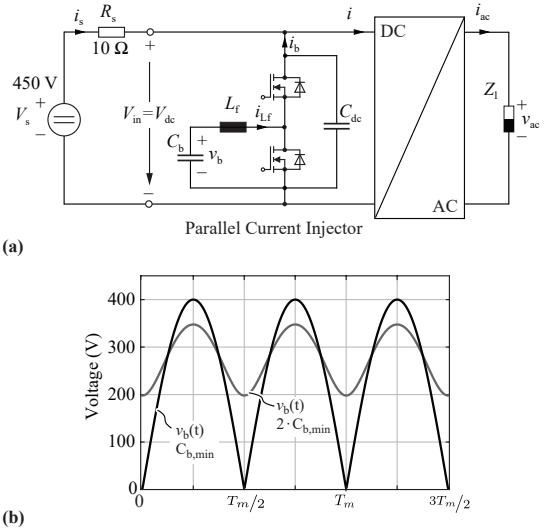


Fig. 2.8: (a) Synchronous buck-type implementation of the Parallel Current Injector (PCI) power buffer concept. (b) Characteristic buffer capacitor voltage waveforms for different capacitance values.

be reused for the implementation of the PCI buffer which keeps the overall engineering effort and system complexity reasonable. Moreover, the stand-alone architecture allows to design and test the PCI buffer independent from the inverter and, due to the feasible DC-bias voltage, is expected to perform better during abrupt load transients since there is always energy stored in the capacitor as opposed to the built-in/AC-side active power buffer concept.

2.3.1 Buffer Capacitor Design

As a consequence of the large feasible buffer voltage ripple of the considered buck-type PCI (cf. Fig. 2.8(b)), comparably small capacitance values in the range of 100 µF – 200 µF are needed, thus realizing the buffer capacitor with ceramic capacitor technology becomes a viable option. Since the effective energy density of electrolytic capacitors is reduced due to lifetime related current stress constraints, 2.2 µF/450 V class II X6S MLCC and 2 µF/500 V CeraLink capacitors were identified to be the most promising candidates for realizing an ultra-compact power buffer [52–54]. Striving for maximal compactness in the GLBC, film capacitors were not considered in the power buffer design because of their low energy density compared to ceramic capacitors. However, film capacitors could be an interesting option if the main motivation for the replacement of electrolytic capacitors are reliability concerns and not a high compactness. Generally, class II ceramics feature a high relative permittivity and are therefore well suited for energy storage application. Adversely, the relative permittivity is not constant but strongly depends, among several other factors, on the applied DC bias voltage. With increasing the DC bias voltage, the effective capacitance of class II ceramics drastically drops, decreasing the capacitance density at higher operating voltage levels. On the contrary, the capacitance of a CeraLink capacitor is increasing with DC bias voltage, resulting in the highest capacitance at DC-link voltage levels around 400 V for 500 V rated voltage [55]. Besides the bias voltage dependency, the capacitance value of ceramic capacitors also depends on the prevailing large-signal AC ripple. In order to capture this non-linear behavior and correctly dimension the active power buffer capacitor, a capacitance and loss density map as illustrated in Fig. 2.9 was determined empirically as described in more detail in Appendix B. Shown are contour plots of the measured capacitance (µF/cm^3) and loss density (W/cm^3) at 60 °C operating temperature as a function of applied DC bias and large-signal 120 Hz AC ripple. As will be explained in more detail in Chapter 3 of this dissertation, a DC bias of 300 V and a superimposed AC voltage with 130 V_{pp} amplitude is a typical

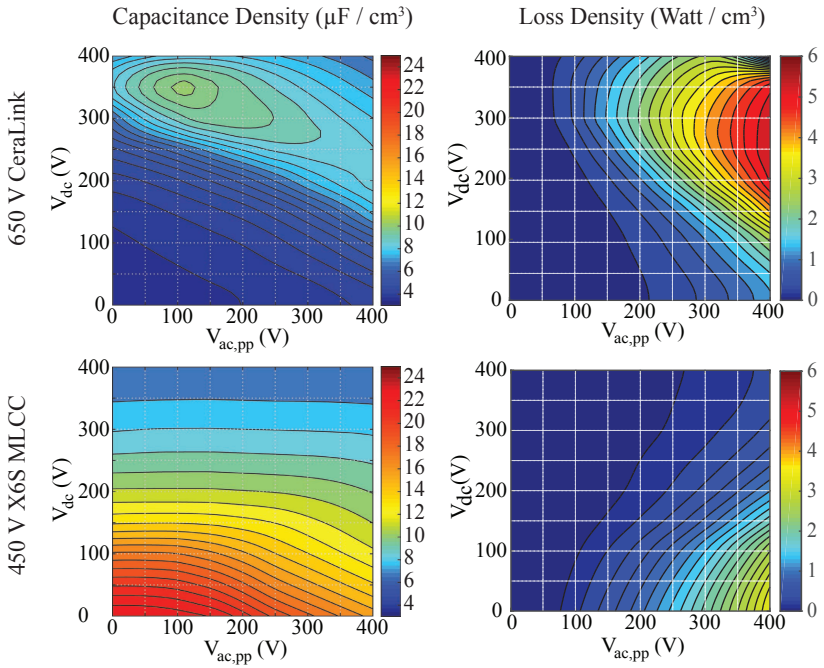


Fig. 2.9: Contour plot of capacitance density and loss density of a 500 V CeraLink and 450 V class II/X6S capacitor technology with respect to DC bias V_{dc} and 120 Hz AC excitation $V_{\mathrm{ac,pp}}$ at 60 °C operating temperature.

operating point of a 2 kW buck-type active power buffer equipped with a 150 µF buffer capacitor. In this operating point, the X6S MLCC features a capacitance density of 8.4 µF/cm^3, as opposed to the slightly higher 9.5 µF/cm^3 of the CeraLink. However, the loss density of the X6S MLCC amounts to just 56 mW/cm^3. By contrast, the CeraLink dissipates roughly 1 W/cm^3 in the very same operating point. It can be concluded, that although the CeraLink features a slightly higher capacitance density, the power losses caused by the 120 Hz voltage ripple are by a factor of 18 higher than those of the X6S MLCC which translates in lower efficiency and larger cooling volume. However, an undisputable advantage of the CeraLink is the higher maximum rated operating temperature of 125 °C (as compared to 105 °C of the class II/X6S MLCC) and the advanced packaging options – available in a package with 20 chips mounted in parallel by means of a silver sintered connection onto a

common lead-frame – for an uncomplicated and reliable mechanical assembly. On the contrary, the class II/X6S MLCC is only available as single chips which makes the assembly of large capacitor blocks very challenging. Moreover, stacking of several MLCC chips to achieve a very tight packaging poses a major reliability risk.

To minimize the risk of mechanical failure during assembly or during the 100 hour testing (cf. Section 1.1), it was decided to use the CeraLink capacitor technology for the implementation of the buffer capacitor employed in the Little Box 1.0 (LB 1.0, cf. Section 4.2), despite the higher losses since the resulting overall efficiency of the inverter still meets the GLBC requirements. Eventually, aiming for highest possible performance, the class II/X6S MLCC technology was used for the implementation of the Little Box 2.0 prototype (LB 2.0, cf. Section 4.3).

2.3.2 Control System for the Active Power Buffer

One drawback of using an active approach to cope with the 120 Hz power pulsation is the required control system which significantly increases the overall complexity of the inverter system compared to purely passive DC-link buffering with electrolytic capacitors. The objectives of the envisioned buffer control system are (a) the compensation of the fluctuating AC power by proper DC-link current injection, (b) a tight control of the DC-link voltage during load transients, and (c) the control of the mean/bias voltage of the buffer capacitor. A comprehensive review and comparison of different active power buffer control methods is provided in [56, 57].

The cascaded control system proposed in this dissertation for the buck-type PCI buffer [40], which combines all aforementioned control objectives into a single reference value for the underlying filter inductor current controller, will be described in more detail in Section 3.2.3.

2.4 EMI & Ground Current Limits

As mentioned in Section 1.1, the parasitic capacitance (≈ 120 nF) formed between the positive and negative terminals of the specified DC source and ground turned out to be larger than first anticipated. For this reason, Google relaxed the originally specified 5 mA ground current limit to 50 mA at a very late point of the competition. This decision was heavily criticized by many contestants because this suddenly allowed inverter concepts which are causing a Low-Frequency (LF) Common-Mode (CM) voltage at the output because

the higher required CM attenuation of the EMI filter could be achieved fairly easy without significant additional volume by an increase of the installed CM capacitance (Y-capacitors). Since the new 50 mA limit was posted just 1 month before the deadline for the submission of the final technical approach document, it was not possible to revise the converter design and competitors which did not select their inverter concept based on preventing the generation of a LF CM voltage at the inverter output perhaps had a strategic advantage.

Interestingly, the parasitic capacitance formed between actual PV cells and the grounded metallic module case, is in the range of 50 nF/kW – 150 nF/kW for crystalline-Silicon PV cells [3, 4], i.e. in the same order of magnitude as specified in the GLBC. To provide galvanic isolation for safety reasons and prevent the flow of ground currents between the PV panels and the utility grid, PV converter systems typ. either incorporated HF transformers at the DC-side or LF transformers at the AC side in the past. However, the demand for converters with higher efficiency, higher power-density and lower cost, eventually led to the adoption of transformerless inverter designs. Due to the high parasitic capacitance of the PV modules, the ground current problem in single-phase PV inverter systems was thoroughly investigated both in industry and academia [58–61]. As detailed in [58], both the selected modulation technique (unipolar vs. bipolar PWM) and the inverter topology (half-bridge vs. H-bridge inverter design) affects the generation of CM voltages.

It is well known that the 2-level H-bridge inverter (cf. Fig. 2.10) can be operated with bipolar PWM which results in a constant CM voltage, $v_{\mathrm{cm}} = \frac{V_{\mathrm{dc}}}{2}$, throughout the PWM cycle, i.e. no switching frequency component of v_{cm} occurs, but utilizes both voltage polarities, $v_{\mathrm{dm}} = \{+V_{\mathrm{dc}}, -V_{\mathrm{dc}}\}$, to generate the desired output voltage. This effectively solves the issues of leakage currents but results in a larger current ripple and larger Differential-Mode (DM) EMI noise, as opposed to unipolar PWM which utilizes also the zero-voltage state, $v_{\mathrm{dm}} = \{+V_{\mathrm{dc}}, 0, -V_{\mathrm{dc}}\}$. Because of the resulting 3-level voltage waveform with twice the effective switching frequency which reduces the output filter size and potentially improves efficiency (smaller current ripple), unipolar PWM is widely accepted in industry. However, by introducing a zero-voltage state where either both high-side or both low-side switches of the H-bridge are turned on, HF pulsed CM voltage is being generated at the output.

With the aim of using unipolar PWM and still preventing the generation of CM voltage, inverter topologies with additional decoupling circuits have been proposed which disconnect the switching stage from the DC source during the free-wheeling state. Relevant DC-based decoupling topologies include but are not limited to the H5 inverter [62], the active clamped H6

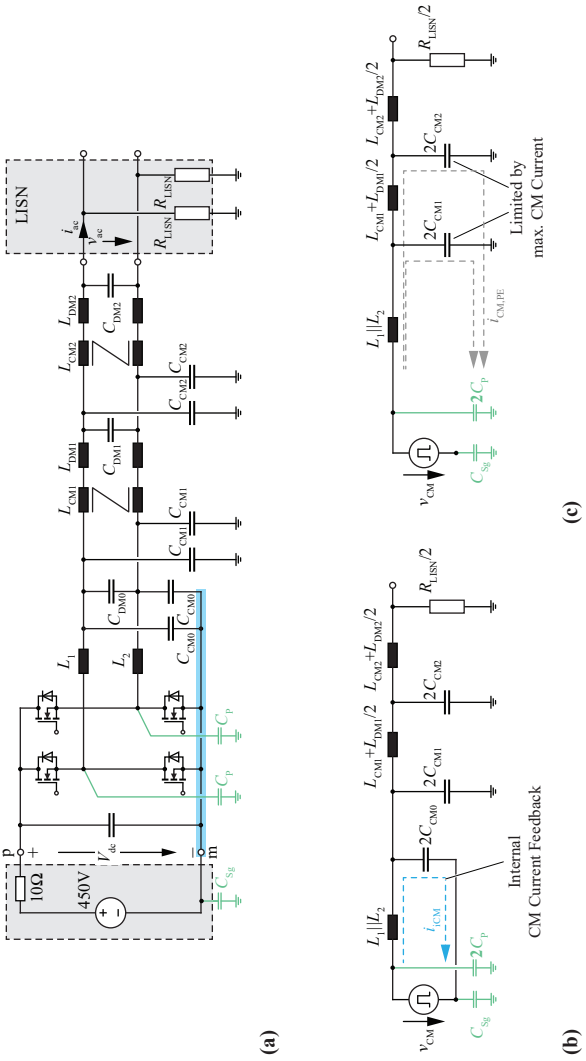


Fig. 2.10: (a) H-bridge inverter with DC-link referenced filter for combined DM and CM filtering. (b) CM equivalent circuit of H-bridge inverter with DC-link referenced filter showing the internal CM current feedback introduced by C_{CM0}. (c) CM equivalent circuit of H-bridge inverter with conventional DM output filter.

inverter [63] and the passive clamped H6 inverter [64]. Relevant AC-based decoupling topologies include the HERIC inverter [65] and the HBZVR-D inverter [66]. Since the additional power semiconductors utilized in the DC- or AC-based decoupling networks cause additional power losses, increase the volume of the switching stage, and because 3rd party IP was not permitted as stated in the legal terms and conditions of the GLBC, a different approach based on the conventional H-bridge inverter but with a new output filter arrangement for the combined attenuation of DM and CM noise was adopted in this dissertation and will be described in the following.

2.4.1 DC-Link Referenced Output Filter

Fig. 2.10(a) shows the H-bridge inverter with the proposed DC-link referenced filter arrangement and subsequent 2-stage EMI filter. As can be seen, each bridge-leg is equipped with an individual LC filter, where the filter capacitor, C_{CM0}, is connected between the respective phase and the negative DC-link terminal m. The corresponding CM equivalent circuit of the H-bridge inverter with proposed DC-link referenced output filter and conventional DM output filter is illustrated in Fig. 2.10(b) and Fig. 2.10(c), respectively. It can be seen that the filter capacitor C_{CM0} introduces a CM current feedback in the equivalent circuit. Since the capacitance of the C_{CM0} is not limited by the maximal allowed ground current, a large portion of the ground current can be confined already within the switching stage which contributes to a reduction of the EMI filter volume (smaller CM chokes). It is of course also possible to include additional filter capacitors referenced towards the positive DC-link terminal, p (cf. Fig. 4.3 in Chapter 4). The reference to both DC-link terminals promotes a quasi constant effective filter capacitance even if ceramic capacitors are employed because the configuration counteracts the non-linear dependency of capacitance on voltage.

2.4.2 1 vs. 2 HF Bridge-Leg Inverter Designs

The inverter with LF unfolder discussed in [67–70] and shown in Fig. 2.11(a), employs a single HF bridge-leg with LC output filter (synchronous DC/|AC| buck converter) to generate a rectified sinusoidal voltage, $v_{\mathrm{C1}} = |\hat{V}_{\mathrm{o}} \cdot \sin(\omega t)|$, and subsequently performs |AC|/AC unfolding by means of a LF H-bridge. Since this inverter concept only requires a single HF bridge-leg with HF filter inductor, as opposed to the H-bridge inverter (cf. Fig. 2.10(a)) with two HF bridge-legs and two HF filter inductors, potentially a higher power-density can be achieved.

Considering a reversed power flow direction, one can immediately notice that the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter topology actually corresponds to a well-known conventional PFC boost rectifier [71], where the input diode bridge is substituted by an active unfolder H-bridge. In order to prevent voltage/current distortions around the AC voltage ZCs known from such PFC rectifier systems, to allow a proper control of the output current during transients, and to support current control for reactive loads where voltage and current are out of phase, a mode of operation is proposed where the buck-stage output voltage is kept above a defined minimum voltage, $v_{\mathrm{C0,min}} \approx 25\,\mathrm{V} - 50\,\mathrm{V}$, and the unfolder H-bridge is temporarily operated with HF PWM to ensure the correct AC output voltage. In Fig. 2.12(a) & (b) characteristic waveforms are depicted for bipolar and unipolar PWM operation of the unfolder stage, respectively. Since only a low voltage level is switched during a short interval of the AC period, switching losses of the unfolder H-bridge are negligible.

However, compared to the H-bridge inverter with two HF bridge-legs, a clear drawback of the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter is that a LF CM component of the output voltage,

$$v_{\mathrm{CM}} = \frac{v_{1-\mathrm{m}} + v_{2-\mathrm{m}}}{2} = \hat{V}_{\mathrm{ac}}/2 \cdot |\sin(\omega t)|, \tag{2.6}$$

with spectral components at even multiples of the AC frequency is being generated as illustrated in Fig. 2.11(b). However, since it is possible to employ the combined DM and CM filter structure as described previously in Section 2.4.1 (cf. Fig. 2.10(a)), where the DC-link referenced filter capacitors allow to confine a large portion of the CM current within the converter, and because of the reduced size of the required CM chokes the implementation of a compact EMI filter is feasible.

As known from totem-pole bridgeless PFC rectifiers, the line-frequency unfolding can also be performed utilizing one of the two bridge-legs of the H-bridge inverter as shown in Fig. 2.13(a). During the positive half-cycle of the AC voltage, the LF bridge-leg connects phase 2 to the negative input terminal m and during the negative AC half-cycle to the positive input terminal p. It follows that the HF bridge-leg must generate the voltage,

$$\overline{v_1} = \begin{cases} \hat{V}_{\mathrm{ac}} \sin(\varphi), & \text{for } 0 \leq \varphi \leq \pi \\ V_{\mathrm{dc}} - \hat{V}_{\mathrm{ac}} \sin(\varphi), & \text{else} \end{cases} \tag{2.7}$$

as output of phase 1 with respect to m in order to obtain the desired sinusoidal output voltage as shown in Fig. 2.13(b). Accepting a more challenging control

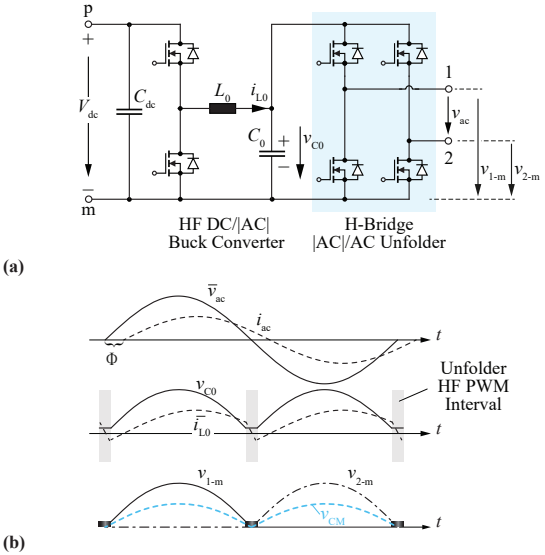


Fig. 2.11: (a) Topology of the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter; Synchronous DC/|AC| buck converter stage generating a rectified sinusoidal voltage and subsequent H-bridge performing the |AC|/AC unfolding. (b) Characteristic waveforms and resulting low-frequency CM voltage.

due to the rapid change of the phase voltage reference around the ZCs, lower conduction losses are achieved as compared to the H-bridge unfolder (cf. Fig. 2.11(a)) with two switches in the conduction path. However, the half-bridge unfolder inverter has a clear drawback concerning the generated LF CM voltage and/or the CM filter effort. The LF CM voltage shown in Fig. 2.13(b) exhibits high $^{dv}/_{dt}$ transitions around the ZCs and therefore, a DC-link referenced filter cannot be applied, which means that the CM filter capacitors (Y-capacitors) are limited to a maximum allowed value to comply with the specified ground current limits which in turn results in larger CM chokes of the EMI filter. Hence, the larger EMI output filter effort has to be weighted against the slightly lower efficiency and higher circuit complexity of the H-bridge unfolder approach.

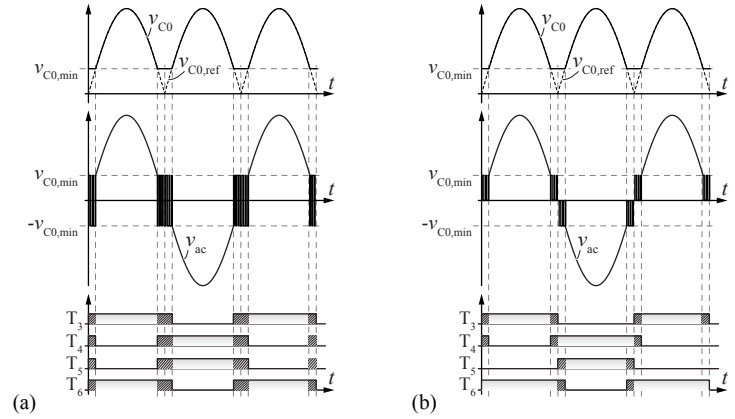


Fig. 2.12: Clamping of the DC/|AC| buck-stage output voltage of Fig. 2.11(a) to $v_{C0,min} > 0$ and temporary operation of the unfolder H-bridge with (a) bipolar and (b) unipolar HF PWM to prevent distortions around the zero-crossing of the AC voltage.

2.4.3 4D-Interleaving of Bridge-Legs

In order to decrease conduction losses and/or reduce the size of the output filter and/or EMI filter, parallel connection and phase-shifted operation of multiple HF bridge-legs as depicted in Fig. 2.14 is a well known concept. If the two bridge-legs ($T_{+,A}$, $T_{-,A}$ and $T_{+,B}$, $T_{-,B}$) are operated with half a pulse interval phase shift, i.e. the switching frequency ripple components of the inductor currents $i_{L,A}$ and $i_{L,B}$ are phase-shifted by $\Delta\varphi = 180°$, which is referred to as symmetric interleaving (in general $\Delta\varphi = {}^{360°}/_{n}$ for n interleaved bridge-legs), the harmonics of $i_L = i_{L,A} + i_{L,B}$ are cancelled at odd multiples of the switching frequency and the size of the output filter can be reduced [72,73].

For the case of having two bridge-legs in parallel it can be argued that the conduction losses are halved but the total switching losses remain, since two bridge-legs are switched at half the current. However, this only holds if the dissipated energy per switching cycle is linear with respect to the switched current, i.e. $E_{loss}(I_{sw}) \approx kI_{sw}$. Depending on the semiconductor technology, performance of the employed gate drive and commutation loop inductance, in practice there is often a more quadratic dependency on switched current with capacitive switching loss offset [15]. It therefore can be argued that at low and moderate output power levels with comparably low conduction losses it can be beneficial in terms of total converter losses to operate only a single

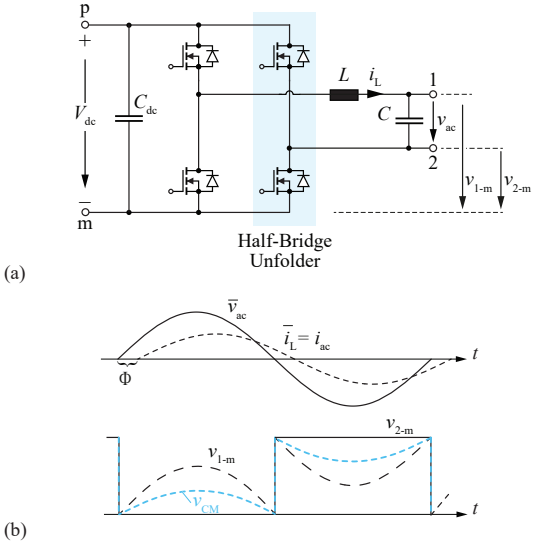


Fig. 2.13: (a) Half-bridge unfolder based inverter topology resembling an H-bridge inverter with asymmetrical bridge-leg filter configuration (only the HF bridge-leg is equipped with a filter inductor). (b) Characteristic waveforms and resulting low-frequency CM voltage.

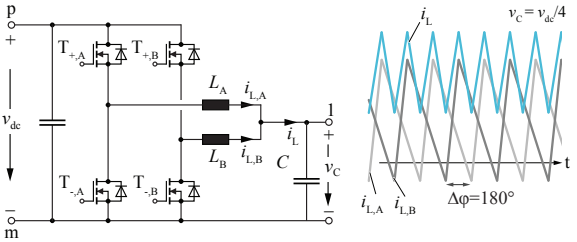


Fig. 2.14: Interleaving of bridge-legs in order to decrease conduction losses and/or reduce the size of the output and EMI filter due to current ripple cancellation and increase of the effective switching frequency.

bridge-leg. In order to still share the losses between both bridge-legs and thus keep the operating temperature of the power transistors as low as possible, alternating operation of the interleaved bridge-legs over an equal interval

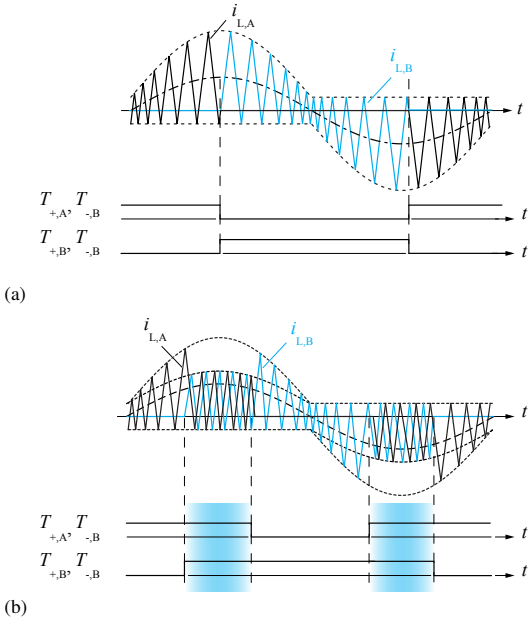


Fig. 2.15: Schematic of the current waveforms for the proposed/implemented 4D-interleaving scheme [74] in order to achieve high converter efficiency and low cooling system volume. (a) No interleaving but alternating operation of two bridge-legs at low output power. (b) Interleaved operation of the bridge-legs around the current maximum (peak instantaneous power) at high (average) output power. The width of the interleaving interval in which both bridge-legs are operated is adjusted depending on the actual load.

within the AC period as indicated in Fig. 2.15(a) is advantageous. At higher output power levels, when conduction losses start to become dominant, both bridge-legs are operated simultaneously as shown in Fig. 2.15(b). Naturally, the overlapping interval when both bridge-legs are active is centered around the peak value of the output current (maximum instantaneous power for $\cos \phi_0 = 1$) and broadens with increasing output power. Since the bridge-legs are located at different positions in space (3D) and the interleaving interval is a function of time (1D), this novel concept proposed/adopted in this dissertation for the implementation of the Little Box 1.0 (cf. Section 4.2) is denominated as 4D-interleaving [74, 75]. The optimal overlap resulting in highest efficiency while meeting EMI limits, can be predetermined for all operating points and

Tab. 2.1: Parameter of Forced-Air Cooled Heat Sink

Sunon Micro Fans	UF3A3-700, UF3C3-700, UF3F3-700, UF3H3-700 (υ = 10 mm – 17 mm)
Sunon Micro Blowers	UB393-700, UB3C3-700, UB3F3-700, UB3H3-700 (υ = 9 mm – 17 mm)
Heat sink type	Extruded parallel-fin heat sink
Material	Copper
Min. Fin Thickness	$t_{\min} = 0.2\,\text{mm}$
Min. Fin Spacing	$s_{\min} = 0.5\,\text{mm}$
Baseplate Thickness	$b = 1\,\text{mm}$

stored in a Look-Up Table (LUT) or can be calculated online by means of a learning algorithm.

2.5 60 °C Temperature Limit

Arranging all converter components tightly to achieve a minimum construction volume is challenging and typically an iterative design process. Bulky components of different shape and size such as the output and EMI filter passives must be arranged to achieve minimum volume while facilitating a good electrical layout of the PCB. At the same time, a cooling system is required for dissipating the component losses and/or to keep the temperature of the enclosure and any accessible part of the converter below 60 °C for a maximal ambient temperature of 30 °C, as stated in the GLBC technical requirements. The component arrangement must also allow for air ducts to cool components which are not directly connected to the baseplate of the heat sink or additional heat conduction elements, e.g. copper plates or heat pipes, must be incorporated to enable heat transfer from the lossy components to the heat sink.

As depicted in Figs. 2.17(a) & (b), either a fan, characterized by comparably low pressure difference and high air flow rate, or a blower, characterized by comparably high pressure difference and low air flow rate can be used to implement basic heat sink building blocks. The performance of these building blocks as a function of total length of the cooling system is compared in Fig. 2.17 by means of the cooling system performance index, i.e. the thermal

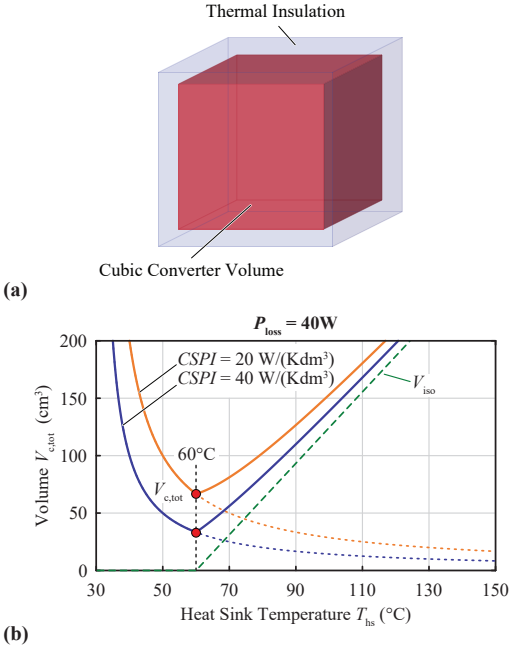


Fig. 2.16: (a) Heat sink with additional thermal isolation layer to allow operating temperatures above 60 °C. (b) Total volume of cooling system as a function of heat sink temperature.

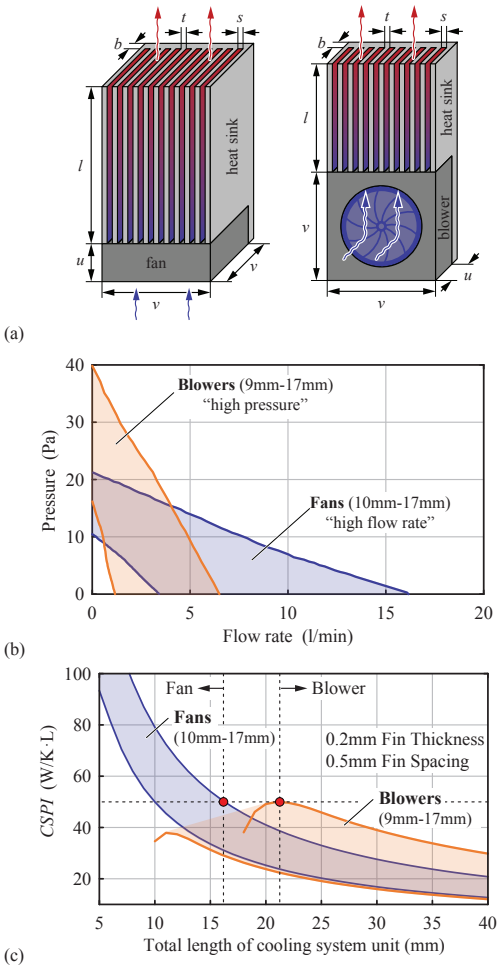


Fig. 2.17: Characteristics and cooling system performance index (CSPI) of forced-air cooled heat sinks. (a) Fan and blower based heat sink building blocks. (b) Pressure difference in dependency of air flow rate. (c) CSPI $\left(\mathrm{W}/(\mathrm{K\,dm}^3)\right)$ of the heat sinks as a function of total length, $l_{\mathrm{tot}} = u + l$, for the fan and $l_{\mathrm{tot}} = v + l$ for the blower as indicated in (a).

conductance G_{th} per volume,

$$\text{CSPI} = \frac{G_{\text{th}}}{\text{Vol}_{\text{c}}} = \frac{1}{R_{\text{th}} \cdot \text{Vol}_{\text{c}}}, \tag{2.8}$$

where Vol_{c} is the volume occupied by the heat sink and the fans/blowers and R_{th} is the thermal resistance of the heat sink to ambient, computed with the model described in [76] and the technical parameters listed in Tab. 2.1. For the parallel-fin type heat sink, it can be seen that a combination of heat sink and blower performs best when the total length ($l_{\text{tot}} = v + l$ for the blower and $l_{\text{tot}} = u + l$ in case of the fan, cf. Fig. 2.17(a)) of the cooling unit is comparably long (>20 mm in Fig. 2.17(c)) with a large baseplate area for direct component attachment. Because of the small height, u, a sandwich like arrangement with two heat sinks at the top and bottom and the converter in the center is possible. On the other hand, the combination of heat sink and fan performs best when the total length of the cooling unit is short and very high CSPI values can be achieved. This is well suited for a component arrangement where only the power transistors are attached to the heat sink and the filter passives are cooled by the air flow exiting the heat sink.

Besides the conventional parallel-fin type heat sink, more advanced duct structures, such as e.g. the hexagon (honeycomb) duct adopted by the winning team of the GLBC (CE+T Power), can further increase the CSPI but require advanced and more expensive manufacturing capabilities [77, 78]. Furthermore, thanks to the recent advances in metallurgy, 3D printing of aluminium allows to create customized heat sinks of almost arbitrary shape as demonstrated by another GLBC finalist [79].

As will be described in Section 4.2, a dual-sided cooling system based on ultra-flat blowers is employed in the Little Box 1.0 (LB 1.0) prototype. The baseplate of the heat sinks covers the entire cross-section of the converter (top and bottom) and theoretically achieves a CSPI of $\approx 35\,\text{W}/(\text{K}\,\text{dm}^3)$. However, additional heat distribution elements are needed to conduct the heat from the lossy components, e.g. the power inductors, to the baseplate of the respective heat sink, which reduces the effective CSPI to $\approx 25\,\text{W}/(\text{K}\,\text{dm}^3)$. In case of the Little Box 2.0 (LB 2.0) prototype described in Section 4.3, a fan based design with a single heat sink placed in front of the power inductors was adopted. Only the power transistors are attached to the baseplate of the heat sink and the power inductor are cooled with the air exiting the fins. Without the need of additional heat distribution elements inside the converter, the CSPI could be increased to $\approx 37\,\text{W}/(\text{K}\,\text{dm}^3)$.

Now, for a cooling system with given performance, the questions arises whether it can be beneficial to allow a heat sink temperature above 60 °C

and to introduce an additional thermal insulation layer as schematically shown in Fig. 2.16(a). This question is quantitatively addressed in Fig. 2.16(b), where the total volume of the cooling system (including insulation layer) to dissipate 40 W of losses is depicted as a function of the heat sink temperature for two different CSPI values and cubic shape of the heat sink (worst case consideration with minimum surface per volume ratio). As can be seen clearly, to achieve a minimum volume of the cooling system it is best to select a heat sink temperature of 60 °C, and to exclude the thermal insulation layer.

2.6 Time-to-Market

On July 2nd, 2015, exactly one year after the technical requirements of the GLBC were posted, the technical approach document with details about the selected concept and the achieved prototype performance had to be submitted by the participants. In this respect, another key challenge was the comparably short given time-frame of just one year to design, implement and test a complete cutting-edge converter system from scratch. This comparably short time-to-market did only allow for hardware iteration cycles and might also explain why none of the presented prototypes [5] relied on advanced 3D integration techniques such as PCB embedding of active and passive components [80].

In order to overcome this challenge and expedite the development process, a multi-objective Pareto optimization, also referred to as virtual prototyping, was carried out in this dissertation to obtain the best set of system parameters in a very short period of time. The comparative evaluation of the $\eta\rho$-performance of two selected inverter concepts will be presented in the next section.

2.7 Comparative Evaluation of Selected Inverter Concepts

Based on the main considerations to overcome the design challenges of the GLBC described in the previous sections, two inverter concepts, namely the H-bridge inverter with DC-link referenced output filter as shown in Fig. 2.18(a) and the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter topology as shown in Fig. 2.18(b) are selected for further studies and a comparative evaluation. The H-bridge topology was selected because ideally no LF CM voltage is generated at the output and the originally specified

ground current limit of 5 mA can be met without the need for bulky CM chokes. In order to further reduce the size of the EMI filter, the DC-link referenced output filter configuration is employed which facilitates a combined DM and CM filtering (cf. Section 2.4.1). As mentioned previously, the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter topology is also considered for further analysis because, compared to the H-bridge inverter, almost half the volume of the entire switching stage can be saved (neglecting the volume contribution of the H-bridge unfolder) with the downside of generating a LF CM voltage at the output (cf. Section 2.4.2). The H-bridge unfolder was preferred over the half-bridge unfolder (cf. Fig. 2.13(a)) as it allows to utilize the DC-link referenced filter configuration and therefore reduces the size of the CM chokes in the EMI filter. As can be seen from Fig. 2.18(a) & (b), both selected inverter concepts are based on 2-level bridge-legs. As outlined previously in Section 2.2.3, a multilevel implementation of the bridge-legs was not considered because of the anticipated increase in volume introduced by the higher semiconductor count, the increased gate driving requirement (supply voltage and gate signal isolation), and because of the more involved control system to facilitate capacitor balancing under all operating conditions.

For both inverter concepts, as discussed before in Section 2.3, the buck-type PCI buffer is selected to cope with the pulsating AC power since (i) it features excellent capacitor utilization and (ii) allows to employ the same bridge-leg design as used in the main inverter to achieve maximal performance with minimal increase of overall complexity.

2.7.1 $\eta\rho$-Performance Comparison

In the following, the $\eta\rho$-Pareto optimization procedure of the inverter system is described. The optimization of the power buffer was performed separately from the inverter as described in detail in Section 3.2.2 and the results, i.e. losses and volume of the power buffer design with highest power-density, are included in the results of the inverter optimization described in the following. The only interface (common variable) between the inverter and the power buffer optimization procedure is the additional reactive power consumption of the inverter's EMI filter. This means that the power buffer not only delivers the 120 Hz AC-power component of the load, but also the additional reactive (capacitive) power drawn by the EMI filter, which depends on the actual value of the DM-capacitors employed in the filter design. A worst-case of 250 VAr of additional reactive power was considered in the power buffer optimization.

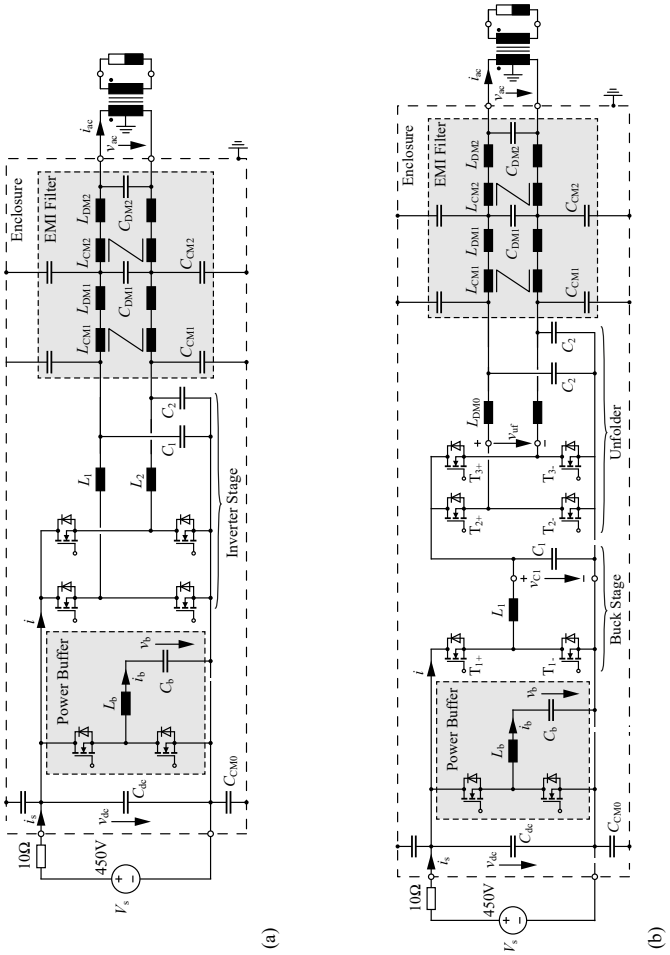


Fig. 2.18: (a) H-bridge based inverter (HF operation of both bridge-legs) with DC-link referenced output filter, buck-type PCI power buffer and 2-stage EMI filter. (b) DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter with buck-type PCI power buffer and 2-stage EMI filter. The H-bridge based unfolder is equipped with DC-link referenced output filter and is temporarily operated with HF PWM around the ZCs of the AC voltage (cf. Section 2.4.2). The inverters are embedded in the test setup according to the GLBC specification with split-winding grounding scheme of the isolation transformer.

Tab. 2.2: System Parameters & Design Space of the Little Box Pareto Optimization

Feature	Range/Option	Description / Comment
S_{ac}	2 kW	Optimization carried out for rated power ($\cos\phi_0 = 1$).
Q_{filt}	250 VAr	Reactive power considered in optimization of power buffer.
V_s	400 V	Nominal input voltage at rated power.
Semiconductor	600 V/70 mΩ GaN HEMT (GIT)	Infineon CoolGaN.
	650 V/25 mΩ GaN HEMT	GaN Systems (considered for the H-bridge unfolder).
# Parallel Devices	1 – 2	1 – 2 devices in parallel per switch.
C_{ext}	[0 pF, 600 pF]	Capacitor in parallel to C_{oss} to reduce $\mathrm{d}v_{ds}/\mathrm{d}t$ related soft-switching losses (only in case of TCM).
Modulation	TCM	Frequency variation depends on inductance value.
	PWM	Current ripple envelope depends on inductance value and switching frequency.
$f_{s,TCM}$	[30 kHz, 1.5 MHz]	Acceptable range of frequency variation for TCM.
$f_{s,PWM}$	[50 kHz, 500 kHz]	Range of applicable constant switching frequencies for PWM.
HF Inductor Technology	Custom single-gap core inductor design	MnZn ferrite core N87; solid, foil and HF-litz wire winding.
# Interleaved Bridge-Legs	1 – 2	4D-interleaving with variable overlap only considered for TCM.
$L_{1/2}$, L_b	[5 µH, 100 µH]	Range of bridge-leg filter inductance value.
Capacitor Technology	2.2 µF, 450 V class II/X6S MLCC	Considered for C_b, $C_{1/2}$, and DM filter capacitors in the EMI filter.
	2.0 µF, 500 V CeraLink	EPCOS/TDK 2nd gen. CeraLink, considered for C_b and C_{dc}.
C_b	[120 µF, 350 µF]	Range of buffer capacitance value.
$V_{b,0}$	$\frac{1}{2}C_b \cdot V_{b,0}^2 \in [E_{0,min}, E_{0,max}]$	Range of buffer bias voltage / avg. stored energy.
EMI Filter	1- and 2-stage custom filter design	VITROPERM 500F toroidal core, solid wire winding, 450 V class II X6S MLCC for X-capacitors (DM) and 630 V / X7R MLCCs for Y-capacitors (CM).
Heat Sink	CSPI = 25.7 W/(K dm^3)	Value obtained from experimentally verified forced-air cooled heat sink.

The available technologies and design considerations presented in this chapter are considered in the design space of the $\eta\rho$-Pareto optimization and are summarized in Tab. 2.2. For the sake of completeness, also design space variables related to the power buffer optimization, e.g. capacitance range of C_{b}, are included in the table. In the $\eta\rho$-Pareto optimization all available degrees of freedom, i.e. all design space variables, are considered for both inverter topologies and modulation schemes (cf., Fig. 2.19). For the full-bridge topology with TCM modulation, for example, the number of interleaved bridge-legs, the number of parallel GaN HEMT devices/chips per switch, the bridge-leg filter inductance value, $L_1 = L_2$, and the filter capacitor value, $C_1 = C_2$, can be iterated, while for PWM operation additionally the switching frequency f_{s} can be selected independently within the specified range. Furthermore, as discussed in Section 2.2.1, reducing the $\mathrm{d}v/\mathrm{d}t$-related soft-switching losses by means of additional ceramic capacitors C_{ext} in parallel to the GaN transistors was, in case of TCM operation, also considered in the design space of the optimization.

Based on the selected inverter topology, modulation scheme and design space parameters, the resulting current and voltage waveforms are calculated for each component and then used in sub-routines to optimize the semiconductors, the bridge-leg output inductors and the EMI filter, while additional circuit components such as the measurement and control circuit or the auxiliary supply are also considered. An overview of the implemented optimization routine to map the considered design space into the $\eta\rho$-performance space is depicted in the flowchart in Fig. 2.19. As can be seen, each component is optimized independently with an iterative temperature/loss calculation, in order to take the temperature dependent losses into account. For the calculation of the semiconductor losses, which consist of conduction, switching and gate-drive losses, for example, the conduction losses are calculated based on the temperature and current-dependent on-state resistance $R_{\mathrm{ds,on}}$ given in the manufacturer's datasheet; for the switching losses a loss map obtained from experimental measurements [6,16] is used. For the design of the bridge-leg HF inductor, different core shapes with MnZn ferrite core material N87 and different air gap sizes as well as different winding types, such as HF litz, foil or solid wire with different numbers of turns, are considered, while the optimal inductor design is again determined by calculating the losses and temperatures of the core and the winding iteratively. As mention in Section 2.2.4, multi-gap inductor designs were not considered in the optimization because of the encountered unexpected high core losses which will be further discussed in Chapter 6 of this dissertation. Similarly, after calculating the quasi peak

noise spectrum, the optimal EMI filter to meet the specified CISPR 11 Class B limits is found by searching through all parameters for the CM/DM-inductors and CM/DM-capacitors. For example, with the iteration of the reactive power consumption of the EMI filter, the maximum total DM-capacitance can be directly calculated and thus, the DM-inductance values needed to achieve the required filter attenuation are also given. Based on the determined filter values, the inductors and capacitors can then be designed independently considering again volume, power losses and temperature. Besides the 2-stage EMI filter structure shown in Fig. 2.18(a) and (b), also a single-stage EMI filter is included in the design space. The feasible size of the Y-capacitors (C_{CM1}, C_{CM2}) is limited to meet the 50 mA ground current requirement. Finally, also the additional circuit components, such as the measurement circuits (voltage, current and zero crossing measurement), control circuits (DSP/FPGA), auxiliary supply, fans, PCB, connectors and housing, have to be taken into account, since these circuit parts are needed in any converter design and thus, with their initial volume and losses, already define the maximum achievable efficiency and power-density. An overview of the employed mathematical models to map the design space into the $\eta\rho$-performance space is provided in Tab. 2.3.

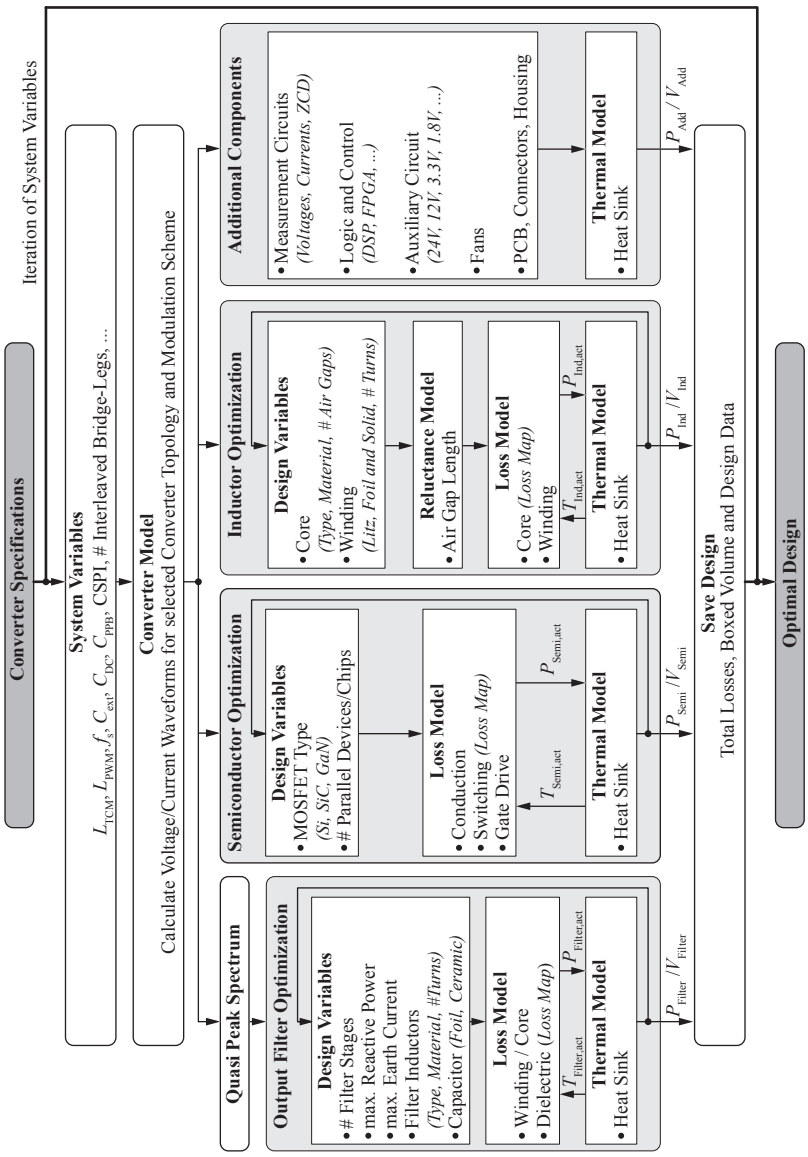


Fig. 2.19: Flowchart of the implemented optimization routine to calculate the $\eta\rho$-performance of the the considered LBC inverter concepts.

Tab. 2.3: Overview of Utilized Component Models

Component	Feature	Description	Reference
HF Inductors	Winding losses	$P_\mathrm{w} = \sum R_\mathrm{ac}(f) I_\mathrm{w}(f)^2$ with frequency dependent winding resistance.	[81–83]
	Core Losses	According to iGSE with operating point dependent coefficients (loss-map).	
	Volume	Boxed volume of core and winding assembly.	
DM/CM Inductors	Winding losses	$P_\mathrm{w} = R_\mathrm{dc} I_\mathrm{ac}^2$ with DC winding resistance and RMS value of AC output current.	[84]
	Volume	Boxed volume of core and winding assembly.	
Capacitors	Ohmic and Dielectric Losses	$I_\mathrm{c}^2 R_\mathrm{ESR}$ for HF ripple, with ESR from manufacturer datasheet. Exp. determined loss-map for large signal excitation of power buffer.	[52, 53]
	Volume	Based on volume of individual ceramic capacitor chips. Operating point (DC bias and AC ripple amplitude) dependent capacitance value considered.	
Transistors	Conduction losses	$I_\mathrm{T}^2 R_\mathrm{ds,on}$ with temperature and current dependent on-state resistance from datasheet.	[6, 15, 16, 81]
	Switching losses	Loss-map obtained from experimental switching loss measurements.	
	Gate Drive Losses	$P_\mathrm{g} = Q_\mathrm{g,tot} V_\mathrm{gs} f_\mathrm{s}$, total gate charge $Q_\mathrm{g,tot}$ from datasheet.	
Miscellaneous	Power Losses	Power loss/consumption of cooling fans, control electronics (voltage and current sensing, DSP, digital signal and supply voltage isolation, etc.) and 12 V auxiliary supply.	
	Volume	Estimated from initial proof of concept system and engineering experience.	
Heat sink	Volume	Estimated volume for exp. verified CSPI based on cooling system building blocks (cf., Subsection 2.5) and maximum feasible ΔT.	[76, 81]

In Fig. 2.20(a) the calculated performance and the designs with highest power-density (S1)-(S5) are visualized for the two described inverter concepts for different operating modes (TCM/PWM) and with/without interleaving of bridge-legs. The Pareto optimal PCI buffer design with TCM modulation and buffer capacitor comprised of 450 V / X6S MLCCs (cf., (P2) in Fig. 3.3), is considered in the optimization of the overall inverter system. The performance of inverter designs employing the PCI buffer with TCM modulation and CeraLink capacitors (cf., (P4) in Fig. 3.3) is also included in the figure. It can be noticed that compared to the full-bridge inverter topology (S1-S3), with the DC/|AC| buck & LF unfolding inverter topology (S4, S5) approximately a 15 % – 20 % higher power-density at even higher efficiency (around +0.5 %) can be achieved. Furthermore, for both circuit topologies, PWM (S3, S5) results in a slightly higher power-density than TCM (S1, S2, S4). Interestingly, interleaving of bridge-legs (S1) is not beneficial for the given GLBC specifications and the objective of achieving maximum power-density. From Fig. 2.20(b) it can be clearly seen that it is advantageous to employ an active power buffer instead of a conventional capacitive buffered DC-link, since a power-density improvement of around 35 % is possible.

A more detailed comparison of the designs with highest power-density (S1)-(S5) with respect to the volume and loss distribution of each design is given in Fig. 2.21. Considering the full-bridge topology, TCM modulation and interleaving of two bridge-legs results in the highest efficiency, however, also in the largest volume. This can be explained by the fact that, due to the interleaving, twice the number of semiconductors devices and inductors is used and thus, on the one hand the volume is increased (cf., Fig. 2.21(a)), but on the other hand the output current is shared between the bridge-legs resulting in lower power transistor losses (cf., Fig. 2.21(b)). The highest power-density is obtained with PWM modulation, however, with the drawback of the lowest efficiency. Compared to TCM modulation, the volume is mainly saved in the electronics, since with PWM no ZC detection circuits and FPGA are needed, and in the EMI filter, since the (constant) switching frequency of the optimal design is just below the lower FCC/CISPR limit of 150 kHz and thus only higher-order harmonics have to be attenuated. In contrast, the volume occupied by the inductor and heat sink slightly increases due to the higher losses. For the DC-|AC| buck converter & unfolder topology, the gain in power-density is mainly achieved with the volume reduction of the power transistors and the output inductors, since only one HF bridge-leg is needed for the implementation of the buck-stage and the volume contribution of the LF full-bridge is comparably low. Interestingly, despite the additional

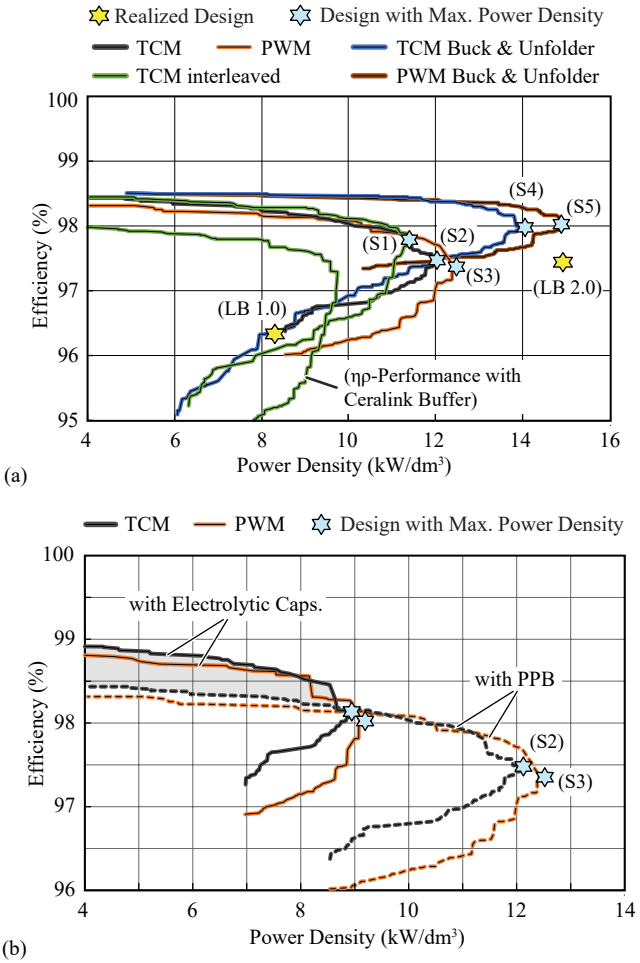


Fig. 2.20: (a) Computed $\eta\rho$-performance of selected inverter concepts including an active power buffer for different operating modes (TCM/PWM) and with/without interleaving of bridge-legs. (b) Impact of employing an active power buffer on the overall $\eta\rho$-performance.

conduction losses of the LF unfolder, the DC-|AC| buck converter & unfolder topology achieves the highest overall converter efficiency and therefore the lowest heat sink volume. The difference in system performance between TCM modulation and PWM is again found in the electronics and EMI filter.

Also indicated in Fig. 2.20(a) is the actual $\eta\rho$-performance achieved with the implemented hardware prototypes described below in Section 4.2 and Section 4.3. It should be noted, that the optimization results presented in this section were obtained with component models which were updated and revised after the first hardware prototype was implemented and the GLBC was completed. As addressed in Chapter 2.2.4 and will be discussed further in Section 4.4.1, the achievable efficiency of the Little Box 1.0 was strongly decreased because of high losses in the multi-gap inductors and the CeraLink buffer capacitor and the consequently large heat sink volume resulted in a lower power-density. Furthermore, the actual switching and conduction losses were higher than predicted by the initial models of the optimization routine. Taking these factors into account, a (re-)optimization of the TCM inverter with interleaved bridge-legs and CeraLink power buffer resulted in the $\eta\rho$-performance as indicated Fig. 2.20(a).

The lower efficiency of the 2$^{\text{nd}}$ implemented prototype, Little Box 2.0 with buck-unfolder topology and PWM, compared to the target design (S5) can be mainly explained by unaccounted losses in the PCBs and in the ceramic DM capacitors of the EMI filter, and a sub-optimal implementation of the bridge-leg filter inductors using HF litz wire with a lower number of strands and therefore increased winding losses. Furthermore, as described in Section 4.3.6, a fan-based heat sink arrangement (cf., Section 2.5) was ultimately chosen for the implementation of the Little Box 2.0. Equipped with ultra high speed fans, a higher cooling performance was achieved compared to the value used in the optimization (cf., Cooling System Performance Index (CSPI) in Tab. 2.2) which explains why, despite the lower efficiency, a power-density similar to optimal design (S5) was achieved.

2.8 Summary

In this chapter, the key design challenges and the technical concepts adopted in the dissertation at hand to implement an ultra-compact single-phase inverter and overcome the Google Little Box Challenge were described in detail. Relevant design considerations such as the selection of the power semiconductor technology, comparison of different bridge-leg control strategies, 2-level vs. multilevel bridge-leg implementation, etc., to achieve a miniaturization

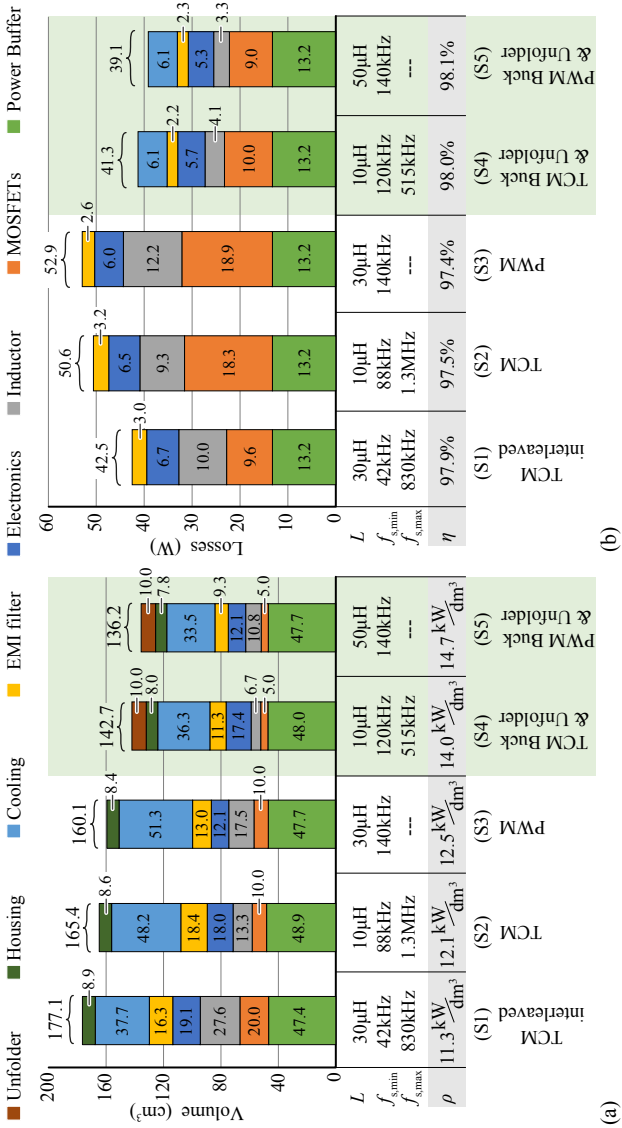


Fig. 2.21: (a) Volume distribution and (b) loss distribution of all designs achieving the respective highest power-density (S1-S5).

of a high-frequency (HF) operated bridge-leg with LC output filter, which constitutes the fundamental building block of the inverter system, were addressed. In order to reduce the size of the energy storage required to cope with the 120 Hz power pulsation intrinsic to single-phase DC/AC converter system, the advantage of replacing bulky electrolytic DC-link capacitors with an additional auxiliary converter and well utilized buffer capacitors was emphasized. Regarding the specified ground current requirements, the difference between a 1 or 2 HF bridge-leg inverter design regarding the generation of a Low-Frequency (LF) CM output voltage component was analyzed and the merits of a DC-link referenced filter structure which allows a combined DM and CM filtering in a single-stage was highlighted. Concerning the EMI requirements of the GLBC, the new concept of 4D-interleaving was introduced which allows to operate the interleaved bridge-legs with an optimal overlapping interval (with respect to the AC period) for maximal conversion efficiency while meeting the EMI requirements. Two promising inverter concepts, namely the H-bridge inverter with DC-link referenced output filter of each bridge-leg and the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter, both equipped with a buck-type Parallel Current Injector (PCI) active power buffer, were selected for further study and comparative evaluation. Based on the results of a multi-objective $\eta\rho$-Pareto optimization incorporating the described design considerations, it is shown that, despite of higher switching losses, operation with constant switching frequency just below 150 kHz PWM achieves a higher power-density compared to TCM control. This is explained by the fact that, for the given GLBC specifications and the performance of the employed GaN semiconductor technology, the loss savings of operating with Zero Voltage Switching (ZVS) throughout the AC period are less compared to the added conduction losses caused by the high RMS current and remaining ZVS switching losses resulting from the TCM control. Furthermore, it is shown that with the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter operated with PWM and a comparably large current ripple (small buck-stage filter inductance value) a power-density of 14.7 kW/dm^3 (240 W/in^3) with an efficiency of up to 98 % at 2 kW output power is possible. Compared to the H-bridge inverter concept, this inverter therefore features a $\approx$ 15 % – 20 % higher power-density and a 1.7 % higher efficiency at 2 kW rated power.

In Chapter 4, the claimed performance, particularly the almost factor 5 higher power-density compared to the minimum GLBC requirement (50 W/in^3), is verified by means of prototype implementations and experi-

mental measurements. The achieved $\eta\rho$-performance is then compared to the achievements of other GLBC finalists.

3

Comparative Evaluation of a Full- and Partial-Power Processing Active Power Buffer

Chapter Abstract

One of the key technical challenges of the Google & IEEE Little Box competition was to shrink the volume of the energy storage required to cope with the twice mains-frequency (120 Hz) pulsating power at the single-phase AC side and meet the stringent 2.5 % input voltage ripple at the DC side. In this chapter, first, a full-power processing buck-type converter active buffer approach, selected by the 1st prize winner of the Little Box Challenge (LBC) and the team of ETH Zurich, which shifts the power pulsation away from the DC-link to a dedicated buffer capacitor is analyzed in detail. Being relieved from strict voltage ripple requirements, a larger voltage ripple is allowed across the buffer capacitor significantly reducing the capacitance requirement. Second, a partial-power active buffer approach, selected by the 2nd prize winner of the LBC, where conventional passive capacitive buffering of the DC-link is combined with a series-connected auxiliary converter used to compensate the remaining 120 Hz voltage ripple across the DC-link capacitor is studied in detail. In this chapter, both selected concepts are comparatively evaluated in terms of achievable efficiency, power-density and ripple compensation performance under both stationary and transient conditions. Novel control schemes and optimally designed hardware prototypes for both considered buffer concepts are presented and accompanied with experimental measurements to support the claimed efficiency and power-density and assess the performance of the implemented control systems. Finally, by means of comparison with conventional passive DC-link buffering using only electrolytic capacitors, it is determined at what voltage ripple requirement it actually becomes beneficial in terms of volume to employ the considered active buffer concepts.

3.1 Introduction

One of the key technical challenges in the implementation of the Google Little Box was to shrink the volume of the energy storage required to cope with the twice mains-frequency (120 Hz) pulsating power at the AC side while meeting the stringent 2.5 % (10 V pk-pk) maximum admissible input voltage ripple. As mentioned in Section 1.2, the additional challenging technical requirements (cf. Tab. 1.1) and the attractive prize money created a remarkable interest in the power electronics community, which led to the participation of 2000+ teams – companies, research institutes, consultants and universities – in the GLBC. Out of 100+ teams which submitted technical description of realized systems, 18 finalists [5] were selected to present their technical approaches and hand over their prototypes to the National Renewable Energy Laboratory (NREL), Golden (CO), USA, for final testing. The team from the Belgian company CE+T Power was finally awarded the grand prize of $1 million for the most compact inverter passing all tests, e.g. also the 100 hours testing, achieving a power-density of 8.72 kW/dm^3 (142.9 W/in^3) and a CEC weighted efficiency of 95.4 %. The 2$^{\text{nd}}$ and 3$^{\text{rd}}$ place were awarded to the team from Schneider Electric for achieving a power-density of 6.1 kW/dm^3 (100 W/in^3) and to the team from Virginia Tech for achieving a power-density of 4.3 kW/dm^3 (70 W/in^3) with their converter prototypes, respectively.

One strategy followed by the majority of the GLBC finalists to reduce the size of the energy storage, conventionally realized with passive capacitive DC-link buffering using bulky electrolytic capacitors, was to employ an additional converter with dedicated buffer capacitor to enable a wide feasible capacitor voltage fluctuation Δv_b which, according to

$$\Delta E = C_\text{b} \cdot V_\text{b} \Delta v_\text{b}, \tag{3.1}$$

wherein ΔE denominates the alternately stored and released energy of the buffer, results in a significantly reduced buffer capacitance size C_b and thus lower overall converter volume despite the additional power electronic components. The winning team from CE+T Power selected the Parallel Current Injector (PCI) approach as shown in Fig. 3.1(a), where the buffer converter connected in parallel at the inverter DC input injects current i_b to compensate the fluctuating portion of current $i_\text{inu} = p_\text{ac}/V_\text{dc}$ which results in a constant input current i_s and consequently in a constant voltage at the converter input. The depicted setup with $V_\text{s} = 450\,\text{V}$ DC source and $R_\text{s} = 10\,\Omega$ input resistor was specified in the testing requirements of the GLBC [2, 5]. The synchronous buck-type implementation of the PCI converter with totem-pole

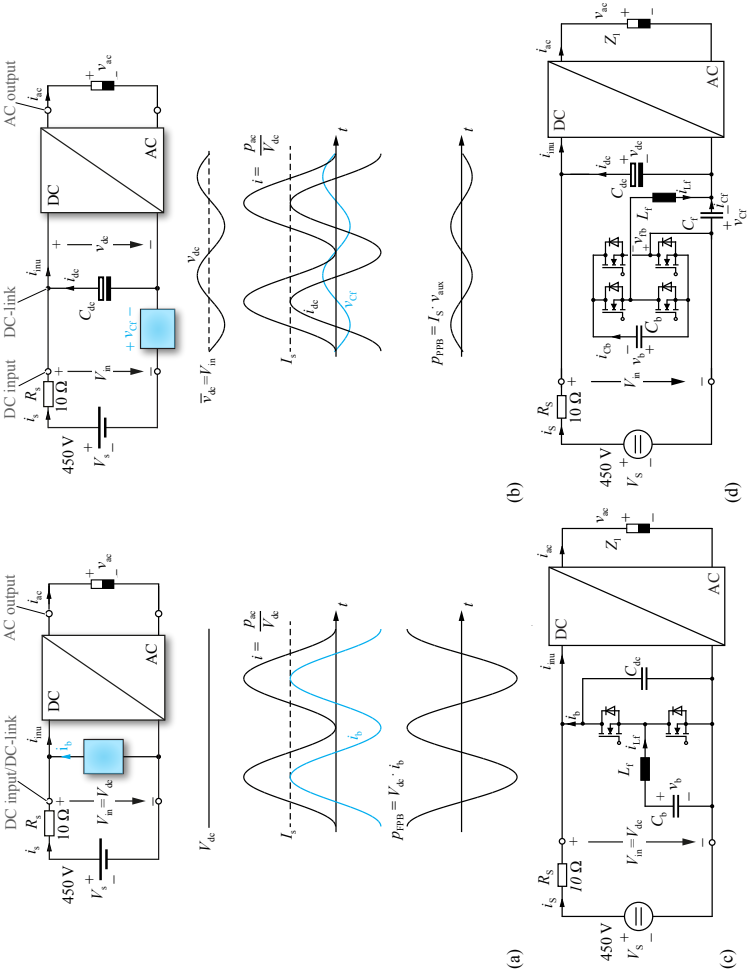


Fig. 3.1: (a) Full-power processing Parallel Current Injector (PCI) active power buffer concept with characteristic waveforms. (b) Partial-power processing Series Voltage Injector (SVI) buffer concept with characteristic waveforms. (c) Synchronous buck converter implementation of the PCI converter. (d) H-bridge based implementation of the SVI converter. The depicted setup with $V_s = 450\,\text{V}$ DC source and $R_s = 10\,\Omega$ input resistor is in accordance with the technical testing requirements of the Google Little Box Challenge (GLBC) [2, 5].

bridge-leg, HF filter inductor and buffer capacitor as shown in Fig. 3.1(c) was chosen by the team of CE+T Power from several available options discussed in literature [37–41, 85, 86].

A different approach as depicted in Fig. 3.1(b) was followed by the 2nd prize winner of the GLBC [42–44]. In this approach, conventional passive capacitive buffering of the DC-link is used, however, the total installed capacitance value is less then what would be actually needed to comply with the 2.5 % voltage ripple requirement. In order to meet the specified input voltage ripple, an additional Series Voltage Injector (SVI) converter impresses voltage v_{Cf} which compensates the 120 Hz voltage ripple still present in v_{dc} resulting in a constant input voltage V_{in}. Fig. 3.1(d) shows the implementation of the SVI converter based on a H-bridge with LC output filter and flying buffer capacitor C_{b} selected by the team from Schneider Electric.

The key advantage of this concept is that the SVI converter can be implemented with low-voltage (LV) components and only processes a small share of the entire fluctuating power, $\hat{p}_{\mathrm{SVI}} = I_{\mathrm{s}} \cdot \hat{v}_{\mathrm{Cf}} \approx 100\,\mathrm{W}$, since, for a defined DC-link capacitance size of around 400 µF – 600 µF, the amplitude of v_{Cf} required to compensate the remaining voltage ripple only amounts to approximately 20 V and $I_{\mathrm{s}} = 5\,\mathrm{A}$ in the nominal operating point (cf. Tab. 1.1). For the remainder of this work, [SVI\C] denominates the combination of the partial-power SVI converter and the DC-link capacitor which jointly perform the buffering of the 120 Hz pulsating power.

On the contrary, the PCI buffer concept selected by the winning team processes the entire fluctuating portion of the AC power, $\hat{p}_{\mathrm{PCI}} = V_{\mathrm{dc}} \cdot \hat{i}_{\mathrm{b}} = V_{\mathrm{dc}} \cdot I_{\mathrm{s}} = 2\,\mathrm{kW}$, resulting in a lower overall conversion efficiency particularly at light load of the overall converter system. However, only a (non-electrolytic) single buffer capacitor is required which could result in a more compact design compared to the SVI approach where both a DC-link capacitor and an additional buffer capacitor C_{b} are needed. It should be noted that $C_{\mathrm{dc}} \approx 15\,\mu\mathrm{F}$ shown in Fig. 3.1(b) is only intended to filter HF switching noise. Also note that, unlike in case of the [SVI\C] buffer, there is no distinction between the denomination "buffer" and "converter" in case of the full-power PCI approach, i.e. "PCI buffer" and "PCI converter" are synonyms for the remainder of this work.

Although the use of active power buffer concepts in various configurations to cope with the 120 Hz pulsating power in single-phase system has already been studied in literature in recent years [32, 34, 34–36, 46, 56, 87–90], a direct multi-objective performance comparison of a full-power PCI buffer and a [SVI\C] buffer approach, particularly for the technical requirement of the

GLBC (cf. Tab. 1.1), has not been presented so far. For this reason, the main contribution of the work presented in this chapter is the comparative evaluation of the PCI and [SVI\C] buffer concepts in terms of achievable efficiency, η, power-density, ρ, and input voltage variation compensation performance under both stationary and transient conditions and consequently to assess whether the team from CE+T Power had a significant advantage by choosing the PCI concept for their Google Little Box inverter design.

Due to the numerous degrees of freedom in the design of the buffer converters, e.g. capacitance value and capacitor technology (aluminum electrolytic and ceramic capacitor technology), bridge-leg control (conventional PWM or zero voltage switching Triangular Current Mode [19]), switching frequency, etc., a design optimization is carried out and the $\eta\rho$-Pareto fronts are determined for both considered concepts in order to estimate the maximal achievable performance and allow a fair comparison. In the following, the Pareto optimization and the hardware implementation of the PCI concept, complemented with latest experimental results, is described in Section 3.2.2 - Section 3.2.4. Likewise to the PCI approach, a mathematical model of the capacitor voltages is derived in Section 3.3.1 for the [SVI\C] buffer and subsequently used in the design optimization outlined in Section 3.3.2. A control system for the SVI converter is proposed in Section 3.3.3 and the implemented hardware demonstrator is described in detail in Section 3.3.4 including experimental measurements to assess the achieved performance under stationary and transient conditions. The obtained optimization results and the achieved $\eta\rho$-performance of the implemented prototypes of both considered concepts are then discussed and comparatively evaluated in Section 3.4. Moreover, a comparison between conventional passive buffering with solely electrolytic DC-link capacitors and the investigated optimally designed PCI and [SVI\C] buffer concepts is provided, indicating at which voltage ripple limit it actually becomes beneficial to implement an active power buffer. Furthermore, a short discussion on the implementation cost of the investigated active power buffer concepts will be provided. Section 3.5 concludes the chapter and summarizes the most important findings.

3.2 Full-Power Parallel Current Injector (PCI) Power Buffer

3.2.1 Mathematical Model of the PCI Converter

In principle, the design of the PCI converter is independent of the implemented inverter topology, however the reactive power consumption of the installed EMI filter on the AC-side also has to be considered. The PCI is controlled to fully compensate the fluctuating power resulting from the load and the EMI filter of the inverter stage. As a consequence, only a constant power P_s must be provided by the power supply V_s and v_{dc} is relieved from the twice mains-frequency voltage ripple. Accordingly, the PCI must be dimensioned to cope with the apparent power

$$S_{\mathrm{b}} = \sqrt{P_{\mathrm{ac}}^2 + (Q_{\mathrm{ac}} + Q_{\mathrm{filt}})^2}, \tag{3.2}$$

wherein Q_{filt} is the reactive power of the main DC/AC converter's EMI filter (not shown in Fig. 3.1(c)). The instantaneous power provided by the PCI buffer can be calculated according to

$$p_b = v_b \cdot i_{\mathrm{Lf}} + v_{\mathrm{L,b}} \cdot i_{\mathrm{Lf}} = v_b \cdot i_{\mathrm{Lf}} + L_{\mathrm{f}} \cdot \frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{Lf}} \cdot i_{\mathrm{Lf}} \approx v_b \cdot i_{\mathrm{Lf}}. \tag{3.3}$$

Neglecting the power contribution of the PCI inductor is reasonable, because when a mean buffer capacitor voltage of $V_b = 300\,\mathrm{V}$ and a reasonable inductor value of 20 µH is considered, then the peak power in the inductor only amounts to

$$\hat{p}_{\mathrm{L,f}} = \omega L_{\mathrm{f}} \hat{i}_{\mathrm{L,f}}^2 = \omega L_{\mathrm{f}} \left(\frac{2\,\mathrm{kW}}{300\,\mathrm{V}} \right)^2 = 335\,\mathrm{mW}. \tag{3.4}$$

The fluctuating power is fully compensated if

$$v_b(t) \cdot i_{\mathrm{Lf}}(t) = p_{\mathrm{out,ac}}(t) = S_{\mathrm{b}} \cos(2\omega t - \tilde{\phi}), \tag{3.5}$$

where $\tilde{\phi} = \arctan\left((Q_{\mathrm{ac}}+Q_{\mathrm{filt}})/P_{\mathrm{ac}}\right)$. Inserting the voltage/current relationship of the buffer capacitor yields the differential equation

$$v_b \cdot C_b \frac{\mathrm{d}v_b}{\mathrm{d}t} = S_{\mathrm{b}} \cos(2\omega t - \tilde{\phi}), \tag{3.6}$$

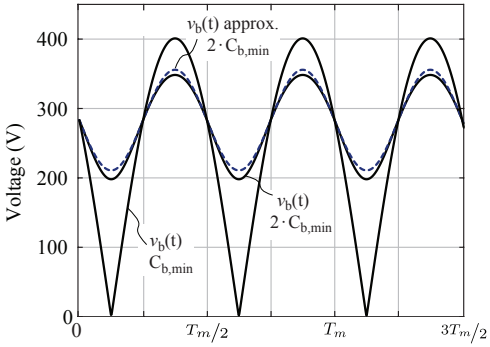


Fig. 3.2: Full-power Parallel Current Injector (PCI) converter buffer capacitor voltage for different capacitance values.

with the analytical solution

$$v_b(t) = \sqrt{V_{\mathrm{b},0}^2 - \frac{S_\mathrm{b} \sin(2\omega t - \tilde{\phi})}{\omega C_b}}, \tag{3.7}$$

wherein $V_{\mathrm{b},0}$ is the RMS value of $v_\mathrm{b}(t)$ and also corresponds to the initial buffer capacitor voltage at $t = \frac{\tilde{\phi}}{2\omega}$ (cf. $t = 0$ in Fig. 3.2). Now, if the capacitance is chosen much larger than the minimum requirement,

$$C_b >> C_{\mathrm{b,min}} = \frac{2S_b}{\omega V_\mathrm{dc}^2} = 66.3\,\mu\mathrm{F}, \tag{3.8}$$

(3.7) can be approximated by means of

$$v_b(t) \approx V_{\mathrm{b},0} - \frac{1}{2}\frac{S_b \sin(2\omega t - \tilde{\phi})}{\omega C_b V_{\mathrm{b},0}}, \tag{3.9}$$

as shown in Fig. 3.2 for $C_b = 2 \cdot C_{\mathrm{b,min}} \approx 130\,\mu\mathrm{F}$ and $V_{\mathrm{b},0} \approx 280\,\mathrm{V}$.

The large feasible amplitude of the voltage ripple enables the use of thin-film and ceramic capacitors because of the much smaller needed capacitance values compared to conventional passive capacitive DC-link buffering. On the other hand, the large voltage ripple and the DC bias makes the design of the buffer capacitor more challenging especially in case of ceramic capacitor technology with non-linear capacitance-voltage relationship.

3.2.2 PCI Converter Pareto Optimization

Despite the reduced capacitance requirement, the buffer capacitor still comprises a large portion of the active buffers overall volume. Thus, the selected capacitor technology defines to a large extend the resulting power-density and plays a critical role in the design of the full power (FP)-PCI converter. Since much smaller capacitance values are needed compared to a conventional passive capacitive DC buffering, thin-film and ceramic capacitors become a viable option. The performance of class II ceramic capacitors with various temperature characteristics (X6S, X7R, ...), metalized polyester (PEN), metalized polypropylene (PP) and electrolytic capacitors subject to large voltage swing operation was comprehensively studied in [52], revealing that 2.2 µF/450 V/X6S class II ceramic capacitors from TDK's C575 series feature by far the highest energy density. As discussed in Section 2.3.1, class II ceramics are characterized by a high relative permittivity and are therefore well suited for energy storage application. Adversely, the relative permittivity is not constant but strongly depends, among several other factors, on the applied DC bias voltage. With increasing DC bias voltage, the effective capacitance of class II ceramics drastically drops, decreasing capacitance density at operating voltage levels. Quite on the contrary, the capacitance of the recently launched CeraLink capacitors (EPCOS/TDK) comprised of an antiferroelectric Pb-Lanthanum-Zirconium-Titanate (PLZT) ceramic, is increasing with DC bias voltage offering the highest capacitance at DC-link voltage levels [55]. Identified as the two most promising ceramic capacitors for large voltage swing buffer applications, a capacitance and loss density map of TDK's 2.2 µF/450 V class II X6S capacitor and EPCOS/TDK's 2 µF/650 V 2$^{\text{nd}}$ generation CeraLink capacitor was obtained from experimental measurement at several operating temperatures as documented in detail in Appendix B of this dissertation. Reconsidering the approximation of $v_b(t)$ in (3.9) and a particular value of C_b and $V_{b,0}$ from the design space listed in Tab. 3.1, the operating point of the buffer capacitor can be calculated. Given the operating point and a ceramic material from the design space, the prevailing large-signal capacitance density is extracted from the empirical capacitance and loss density map (cf. Fig. B.8). This allows to accurately calculate the number of single capacitor chips mounted in parallel to meet the requested value C_b in the given large-signal operating point, despite the non-linear behavior of the considered ceramic materials. Likewise, the power losses occurring in the capacitor assembly caused by continuously storing and releasing $\Delta E = \frac{S_b}{\omega} = 5.31\,\text{J}$ is extracted from the loss map (cf. Fig. B.9). Additional losses due to the high frequency current ripple in i_{Lf} is negligible, since the

Tab. 3.1: System Parameters & Search Locus of the PCI Converter Pareto Optimization

Feature	Range/Option
Capacitor Technology	450 V class II/X6S 500 V 2nd generation CeraLink
C_b	[110 µF, 350 µF]
$V_{\mathrm{b},0}$	$1/2 C_b \cdot V_{\mathrm{b},0}^2 \in \left[E_{0,\min}, E_{0,\max}\right]$
E_{m}	5 % – 30 %
Inductor Technology	N87 MnZn ferrite, HF litz wire
L_f	[10 µH, 60 µH]
Modulation	TCM, f_s from 200 kHz to 1 MHz PWM, f_s = 140 kHz
Heat sink	CSPI = 25.7 W/(K dm^3)

ESR of the buffer capacitor assembly is vanishingly low at the considered switching frequencies. Moreover, $V_{b,0}$, the RMS value of the buffer capacitor voltage or the mean buffer voltage according to (3.9), can be adjusted by the employed control system as proposed in Section 3.2.3 and is considered a further degree of freedom in the design. Depending on the large-signal ripple and bias properties of the respective capacitor technology, different bias voltages might lead to the optimal design. However, in order to have enough energy margin to cope with load transients, the bias voltage must be kept within certain bounds. Specifically, given C_b then $V_{\mathrm{b},0}$ must be chosen such that

$$1/2 C_b \cdot V_{\mathrm{b},0}^2 \in \left[E_{0,\min}, E_{0,\max}\right], \tag{3.10}$$

where the interval boundaries of the mean energy E_0 are given by

$$E_{0,\min} = E_m + \frac{\Delta E}{2}, \quad E_{0,\max} = E_{\max} - E_m - \frac{\Delta E}{2}, \tag{3.11}$$

with the maximal energy

$$E_{\max} = 1/2 C_b V_{\mathrm{dc}}^2 \tag{3.12}$$

and an empirically chosen energy margin in the range of

$$E_m = (5\,\% - 30\,\%\text{ of } \Delta E). \tag{3.13}$$

Besides the buffer capacitor, a compact implementation of the PCI half-bridge and the HF filter inductor is also vital. In Chapter 2 GaN was identified as

the key power semiconductor technology for the implementation of ultra-compact converter designs for the Google Little Box Challenge. For the implementation of the half-bridge, 600 V / 70 mΩ CoolGaN devices form Infineon in combination with a novel high-performance gate drive circuit [75] are considered. The bridge-leg is operated with a Triangular Current Mode (TCM) modulation scheme [19], where the on/off intervals of the power transistors are adjusted such that a triangular current is impressed in the bridge-leg filter inductor and Zero Voltage Switching (ZVS) is achieved in all operating points. Due to reduced switching losses and accordingly reduced heat sink volume, a higher efficiency and higher power-density is expected when TCM is applied. Moreover, a rather high switching frequency in the range of 200kHz-1MHz results in a significantly reduced volume of the inductor. However, as outlined in [75], the required large HF current ripple leads to increased conduction losses which reduces the gain of soft-switching resulting from TCM. Therefore also conventional PWM is considered for the bridge-leg, since the large turn-on switching losses associated with PWM can be reduced when a relatively high current ripple is allowed (ZVS around the fundamental current zero crossings). In [91], advanced models for winding and core loss calculation and thermal models for HF inductor design are presented. Adopting these models to a large variety of available core geometries, N87 MnZn ferrite material and available HF-litz wires, an optimal inductor in terms of volume can be identified for a given inductance value and current waveform. The generated power losses are extracted by means of an optimized forced-air cooled heat sink with a experimentally verified Cooling System Performance Index (CSPI) of 25.7 W dm^3/K as described in more detail in Chapter 2.

Given the design space as summarized in Tab. 3.1 and elaborate loss and volume models of the utilized components, the performance of several PCI converter configurations was calculated. Fig. 3.3 displays the performance of the calculated designs in the $\eta\rho$-performance space. In particular, PCI converter designs with class II and CeraLink capacitors, both either with TCM or conventional PWM operation, are distinguished by color. As reference, the $\eta\rho$-performance of a conventional DC-link assembly, which will be introduced later in Section 3.4, is also shown. Clearly noticeable, designs with class II/X6S ceramic outperform those with CeraLink capacitors. The highest power-density of 41.3 kW/dm^3 (677.1 W/in^3) and an efficiency of 99.4 % (P2) is achieved with TCM modulation, C_b = 110 µF with class II/X6S capacitors, and L_f = 30 µH. As discussed previously, the CeraLink capacitors exhibits much higher 120 Hz losses compared to the class II/X6S capacitors which explains the drop in efficiency of the PCI converter designs with CeraLink

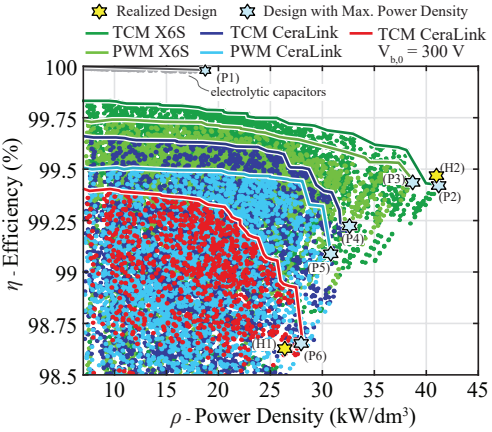


Fig. 3.3: $\eta\rho$-plot of the calculated designs with indicated Pareto fronts. For volume and loss distribution of the optimal desings (P2)-(P6) see Fig. 3.4. (H1) and (H2) are indicating realized designs.

capacitors as shown in Fig. 3.3, and the reduction in power-density due to the higher cooling effort. As a consequence, power-density optimal designs with class II/X6S (P2), (P3) feature a low total buffer capacitance around 110 µF, accordingly a large 120 Hz voltage ripple with $\approx 180\,\mathrm{V_{pp}}$ amplitude, and a mean voltage $V_{\mathrm{b},0}$ of 300 V. On the other hand, optimal designs employing the CeraLink capacitor, feature comparably high total capacitance values of $\approx 200\,\mu\mathrm{F}$ and a consequently low voltage ripple with $\approx 80\,\mathrm{V_{pp}}$ amplitude in order to keep the losses small. Moreover, since the capacitance density of the CeraLink capacitors increases with applied bias, optimal results (P4), (P5) exhibit increased bias voltages $V_{\mathrm{b},0} \approx 330\,\mathrm{V} - 340\,\mathrm{V}$. In order to show the impact of the bias voltage on the overall performance of the CeraLink PCI buffer and better reflect the performance of the actually realized prototype (cf. Section 3.2.4), the optimization results for a fixed bias voltage of $V_{\mathrm{b},0} = 300\,\mathrm{V}$, which corresponds to a more conservative energy margin of $E_{\mathrm{m}} = 30\,\%$, are also included in Fig. 3.3 and Fig. 3.4.

Also noticeable in the $\eta\rho$-space, designs using TCM modulation feature higher efficiency compared to PWM operation with $f_s = 140\,\mathrm{kHz}$. Naturally, designs (P2)-(P5) with maximum power-density tend towards the lowest energy margins as specified in the design space (cf. Tab. 3.1).

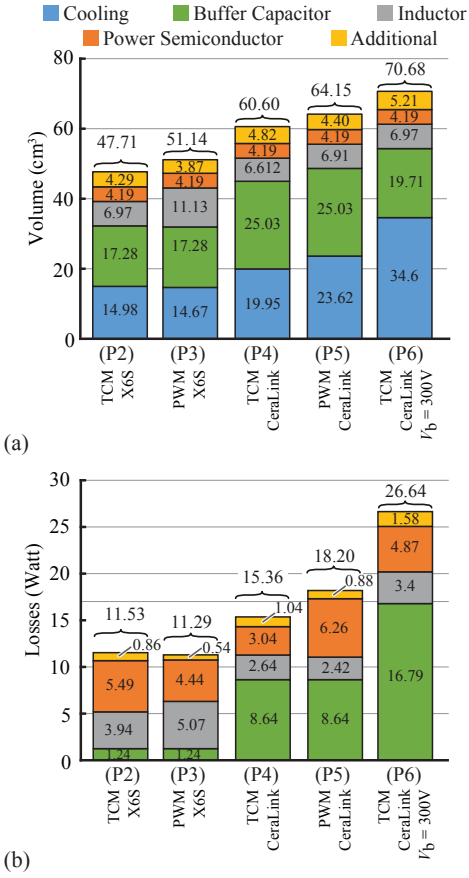


Fig. 3.4: Results of the FP-PCI converter design optimization. (a) Volume distribution of the optimal designs (P2)-(P6). (b) Loss distribution of the optimal designs (P2)-(P6).

The volume of the PCI converter is clearly dominated by the buffer capacitor as shown in Fig. 3.4. Also the volume required for cooling is significant, especially in the case of design (P6). As stated earlier, optimal designs using CeraLink capacitors feature a higher total buffer capacitance, consequently occupying more volume. The loss distribution of the optimal designs is given in Fig. 3.4(b), revealing the almost negligible losses occurring in the class II/X6S designs (P2), (P3), and the almost 7 times higher losses in the CeraLink designs (P4), (P5). Surprising are the dominating losses in the CeraLink capacitor of the pragmatic design (P6), which drastically reduces efficiency and substantially increases the heat sink volume. Clearly, the buffer capacitor operating point occurring at steady-state in design (P6) is not optimal given the characteristics of the CeraLink capacitor. The category *Additional* shown in Figs. 3.4(a) & (b) includes the volume and loss data of the current zero-crossing detector (required for TCM operation), analog measurement circuits, metal enclosure of the PCI converter, and the power consumption of the heat sink fans, respectively. Given the gained insights from the $\eta\rho$-space of the calculated designs, it is clearly advisable to realize a PCI converter using class II/X6S capacitors. However, practical manufacturing considerations have to be included in the decision making. In order to realize 110 µF roughly 150 single class II/X6S chips must be mounted in parallel. With the known issue of ceramic cracking due to mechanical and thermal stress, this certainly requires advanced packaging techniques in order to achieve a reliable assembly. On the other hand, the CeraLink capacitor is available in a package with 20 chips mounted in parallel by means of a silver sintered connection onto a common lead-frame which is able to absorb mechanical stress.

Two different PCI converter designs were selected from the presented Pareto optimization results for hardware implementation: (i) Due to the easier and more reliable assembly of the buffer capacitor, it was decided to realize the 28 kW/dm^3 (458.8 W/in^3) design (P6) in hardware, with $C_b = 150\,\mu\text{F}$ comprised of individual 2 µF CeraLink capacitors despite the higher losses, the conservative energy margin of $E_\text{m} = 30\,\%$ ($V_{\text{b},0} = 300\,\text{V}$) and TCM modulation of the bridge-leg. (ii) Aiming at maximum power-density, the 38.4 kW/dm^3 (629.3 W/in^3) design (P3) with $C_b = 110\,\mu\text{F}$ comprised of individual 2.2 µF/450 V class II/X6S capacitors, a bias voltage $V_{\text{b},0} = 280\,\text{V}$ and 140 kHz PWM operation of the bridge-leg, was also selected for hardware implementation despite the more challenging buffer capacitor assembly. The actually achieved 26.12 kW/dm^3 (428 W/in^3) power-density and 98.65 % efficiency of the implemented CeraLink-TCM prototype, is indicated with label (H1) in Fig. 3.3. Likewise, the implemented class II/X6S-PWM prototype with

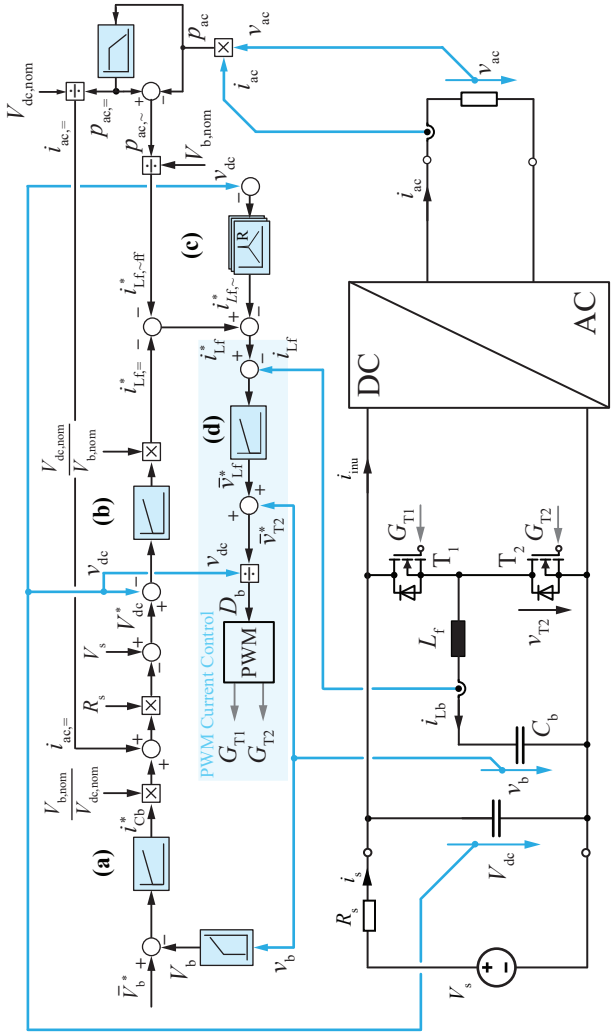


Fig. 3.5: Proposed cascaded control structure of the PCI converter. (a) Control of the average buffer capacitor voltage. (b) Control of the DC-link voltage. (c) Compensation of the pulsating power by means of feed-forward control and resonant compensators. (d) Inner loop PWM current control of the inductor current.

an achieved $\eta\rho$-performance of 99.4 % and 41.3 kW/dm^3 (676.8 W/in^3) as indicated with label (H2). Both implemented PCI converter prototypes will be described in detail in Section 3.2.4.

3.2.3 Control System of the PCI Converter

One of the downsides of using an active approach to cope with the 120 Hz power pulsation, is the required control system which increases the overall complexity of the DC/AC converter. The cascaded control system for the PCI converter proposed in [40] is depicted in Fig. 3.5 and contains dedicated subsystems with the objective to (a) control the mean/bias voltage of the buffer capacitor, (b) achieve a tight control of the DC-link voltage during load transients, (c) compensate the fluctuating AC power by proper current injection, and (d) combine all control objectives into a single reference value for the underlying inductor current control. In order to completely eliminate the DC-link voltage ripple, feed-forward control of the fluctuating portion of the AC power and an additional resonant controller [92] tuned at even multiples of the AC frequency are employed as shown in Fig. 3.5(c). If only control aspects are considered, then the reference of the mean PCI converter capacitor voltage V_b^* is set to a voltage level

$$V_{b,\mathrm{mid}} = {}^{V_{dc}}/\sqrt{2} = 282.8\,\mathrm{V} \tag{3.14}$$

corresponding to half of the maximal stored energy. Maintaining the bias of the buffer capacitor at $V_{b,\mathrm{mid}}$ results in symmetrical energy margins, and load step-up and step-down can be handled equally well. However, as outlined in Section 3.2.2, the DC bias of the buffer capacitor strongly affects the $\eta\rho$-performance results since (i) the prevailing capacitance density of the considered ceramic capacitors is strongly dependent on the DC bias and (ii) the amplitude of current i_{Lf} is inversely proportional to v_b. Therefore, a compromise between transient handling capability and $\eta\rho$-performance must be made. In case of the realized Ceralink-TCM and class II/X6S-PWM PCI converter prototypes presented in Section 3.2.4, the reference voltage V_{b}^* is set to 300 V and 280 V, respectively. The inner loop of the cascaded control structure (cf. Fig. 3.5(b)) is required to tightly regulate the average DC-link voltage under all load conditions. Due to the cascaded structure, controlling the DC-link voltage has always priority over the mean buffer capacitor voltage. This has significant advantages in case of abrupt load changes, since the average buffer capacitor voltage V_{b} can be temporarily deflected from the reference V_b^*, keeping v_{dc} tightly controlled. As can be seen, the individual current reference values computed by the control subsystems (a)-(c) are

then combined in a single current reference i^*_{Lf} and forwarded to the inner PWM current control loop (cf. control subsystem (d)). If TCM modulation is employed (not shown in Fig. 3.5), the turn-on and turn-off times of the power transistors are computed such that, on average over one switching cycle, the current in the inductor meets i^*_{Lf} and ZVS of the bridge-leg applies. The interested reader is referred to [40] for more details.

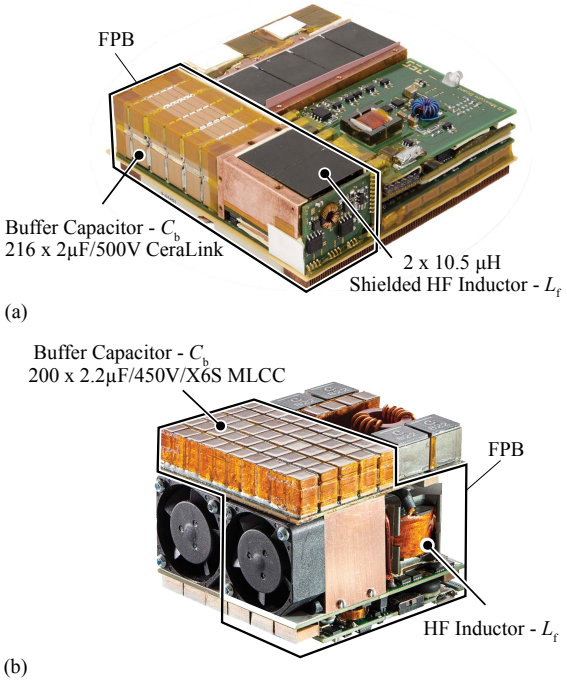


Fig. 3.6: (a) Picture of the Google Little Box 1.0 (1st version of the Little Box inverter developed at ETH Zurich) with PCI converter using CeraLink capacitors and TCM control of the bridge-leg. (b) Picture of the Google Little Box 2.0 (2nd further optimized version of the Little Box inverter) with PCI converter using class II/X6S MLCC and constant 140 kHz PWM. FPB indicates that the active power buffer is processing the full fluctuating power.

Tab. 3.2: Technical Details of the CeraLink-TCM PCI Converter.

Feature	Value	Description
Volume (no cooling)	47.3 cm^3 (2.9 in^3)	Boxed volume of the constructed PCI converter without cooler
Volume (with cooling)	76.6 cm^3 (4.7 in^3)	Total boxed volume of the PCI converter with a CSPI = 25.7 W/(K dm^3) heat sink
Capacitor volume	24.6 cm^3 (1.5 in^3)	Total volume of the installed buffer capacitor
η	98.65 %	Efficiency at 2 kW
L_f	21 µH	Foil winding and custom shape, multi-gap MnZn ferrite core with 2 times 10.5 µH in series
C_b	150 µF	Equivalent large signal capacitance of the installed CeraLink capacitors

3.2.4 Hardware Implementation and Experimental Verification

Version 1 - CeraLink Capacitors and TCM Modulation

The first implemented prototype (Version 1) of the PCI converter concept is shown in Fig. 3.6(a). As mentioned before, the half-bridge is implemented with 600 V/70 mΩ CoolGaN devices. In order to reduce reverse conduction losses of the GaN transistors during the dead-times, 600 V SiC Schottky diodes from Wolfspeed are mounted in parallel to the power transistors. The bridge-leg is operated with a TCM modulation scheme with variable switching frequency in the range of 200 kHz – 1000 kHz that enables ZVS transitions in all operating points. The inductor $L_\mathrm{f} \approx 21\,\mu\mathrm{H}$ of the power buffer was realized by a series connection of two 10.5 µH inductors implemented based on a novel multiple-gap multiple parallel foil winding design using the DMR51 low-loss HF MnZn Ferrite core material from DMEGC. The buffer capacitor, C_b, with a large-signal equivalent capacitance of 150 µF, was implemented by means of 108 individual 2 µF/500 V CeraLink capacitors. By the courtesy of EPCOS/TDK, a custom package with 18 capacitor chips mounted together on silver coated copper lead frames was available. The design parameters and selected features of the realized system are summarized in Tab. 3.2.

Combined with a 2 kW high power-density inverter stage designed for the Google Little Box Challenge (cf. Fig. 3.6(a)), the constructed PCI converter was experimentally tested. As can be seen from the picture, the power buffer was designed as a stand-alone module which allowed to directly substitute

Tab. 3.3: Technical Details of the Class II/X6S-PWM PCI Converter.

Feature	Value	Description
Volume (no cooling)	$34.0\,\mathrm{cm}^3$ ($2.1\,\mathrm{in}^3$)	Boxed volume of the constructed PCI converter without cooler
Volume (with cooling)	$48.4\,\mathrm{cm}^3$ ($3.0\,\mathrm{in}^3$)	Total boxed volume of the PCI converter with a CSPI = $37.5\,\mathrm{W/(K\,dm^3)}$ heat sink
Capacitor volume	$19.9\,\mathrm{cm}^3$ ($1.5\,\mathrm{in}^3$)	Total volume of installed buffer capacitor
η	99.4 %	Efficiency at 2 kW
L_f	40 µH	HF litz wire and RM 10 MnZn ferrite core (N87)
C_b	120 µF	Equivalent large signal capacitance of the installed $200 \times 2.2\,\mu\mathrm{F}/450\,\mathrm{V}$ MLCC

the electrolytic capacitor bank of a preliminary version of the initial Google Little Box converter developed at ETH Zurich. In order to extract the power losses, an optimized forced-air cooled dual-sided heat sink with an effective CSPI of $25.7\,\mathrm{W/(dm^3\,K)}$ is utilized. The heat sink has a height of only 4.5 mm and employs 6 Sunon 5 V DC micro blowers ($30 \times 30 \times 3$ mm) per element (UB5U3-700). It should be noted that in Fig. 3.6(a) the top-side heat sink is removed. The novel control system presented in Section 3.2.3 is implemented on a *TMS320F28335* from Texas Instrument's C2000 32-bit family of microcontrollers. As mentioned previously in Section 3.2.3, the PWM current control highlighted in Fig. 3.5 is substituted with a cycle-by-cycle TCM control, whereby the turn-on and turn-off intervals of the power transistors are computed on the microcontroller and then forwarded to a modulator implemented on a Lattice XP2 FPGA.

Version 2 - Class II/X6S Capacitor and PWM

Benefiting from the gained insights of the design optimization in Section 3.2.2 carried out in the aftermath of the GLBC, a second prototype of the PCI converter (Version 2) was implemented and the design parameters and selected features of the realized system are summarized in Tab. 3.3. For the sake of maximum power-density, the implemented power pulsation buffer is, unlike before, not designed as stand-alone module but instead incorporated in the inverter stage as can be seen from the picture in Fig. 3.6(b) of the 2^{nd} version of the Google Little Box inverter developed at ETH Zurich. The bridge-leg of the PCI converter Version 2 prototype is implemented with the same 600 V/70 mΩ CoolGaN technology, but uses two parallel connected

transistors per switch and is operated with an EMI friendly constant 140 kHz PWM instead of TCM modulation. The inductor of the active power buffer, $L_f = 40\,\mu H$, is implemented on a RM 10 core using the MnZn ferrite material N87 from TDK. The winding is realized with 20 turns of a $225 \times 71\,\mu m$ HF litz wire without additional silk insulation. The limbs of the RM 10 core were shortened with a diamond wheel precision saw to achieve a total air gap length of 2 mm (1 mm per limb) while keeping the total height of the core unchanged. The buffer capacitor, C_b, features an effective large-signal equivalent capacitance of $\approx 120\,\mu F$, and was realized by means of 200 individual 2.2 µF/450 V class II/X6S MLCC. As can be seen from Fig. 3.6(c), 200 of these chip capacitors were soldered together on a PCB which is on the one hand a very challenging assembly task and on the other hand bears the risk of electrical failures due to micro-cracks in the ceramic material caused by mechanical stress during assembly and/or operation.

The novel control system presented in Section 3.2.3 is entirely implemented on the *TMS320F28335* microcontroller. Because conventional PWM current control is employed (cf. Fig. 3.5), no additional FPGA is needed which simplifies soft- and hardware development of the digital control system.

PCI converter $\eta\rho$-performance

The conversion efficiency of the active power buffer is defined according to

$$\eta = 1 - \frac{P_v}{S_b} \tag{3.15}$$

where P_v denominates the losses of the PCI buffer when processing the apparent power S_b of the main inverter with ohmic load (cf. (3.2)). The efficiency measured with a Yokogawa WT3000 precision power analyzer of the CeraLink-TCM prototype at 2 kW rated power is 98.65 % as depicted in Fig. 3.7 which corresponds to 27 W of losses. The total volume of the realized PCI converter including cooling volume amounts to 76.6 cm^3 which corresponds to a power-density of 26.1 kW/dm^3 (428 W/in^3).

The measured efficiency of the class II/X6S-PWM prototype, as also depicted in Fig. 3.7, is around 99.4 % at close to 2 kW which corresponds to only about 12 W of losses at rated power. The total volume of the realized PCI converter Version 2 including cooling volume amounts to 48.4 cm^3 which corresponds to a power-density of 41.3 kW/dm^3 (677 W/in^3).

As described in Section 3.2.2, the main reason for the significantly higher efficiency of the second implemented version of the PCI converter, is that compared to the CeraLink capacitor technology, the class II/X6S MLCCs

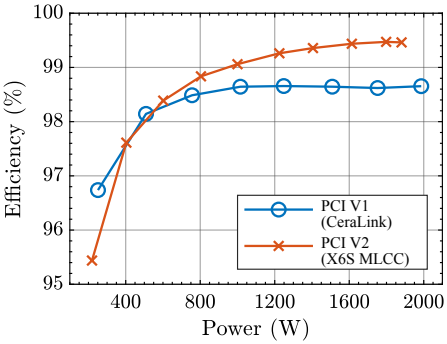


Fig. 3.7: Measured efficiency of the constructed PCI converter prototypes as a function of the peak value of the processed apparent power S_b.

exhibit a much lower power loss (≈ 1.5 W instead of ≈ 17.3 W at 2 kW) when cycled at low frequency (120 Hz) with a large amplitude voltage swing.

Experimental Waveforms

Since both versions of the PCI converter are using the same control systems and exhibit very similar stationary and transient behavior, for the sake of brevity, only the experimental waveforms of the CeraLink-TCM prototype are presented in the following.

The steady-state performance at 2 kW rated power of the implemented PCI converter controller is illustrated in Fig. 3.8. It can be seen from the recorded DC-link voltage and the converter input current (cf. i_s in Fig. 3.1(c)), that the power pulsation was successfully shifted from the DC-link to the buffer capacitor which features a distinctive 100 V_{pp}, 120 Hz voltage ripple. The inductor current waveform is a result of the employed TCM modulation, clearly showing the envelope of the double-line frequency charging currents. In order to verify the dynamic performance of the implemented control system, the inverter was subject to load variations. The transient performance of the PCI converter subject to a load step from 0 W to 700 W is depicted in Fig. 3.9(a). Triggered by the load step, the average buffer capacitor voltage drops 50 V below the 300 V at steady-state. Simultaneously, the control system of the PCI converter starts to compensate the power pulsation by means of injecting an appropriate current i_b in the DC-link. As a consequence, a distinct 120 Hz voltage ripple develops at the buffer capacitor immediately after the load

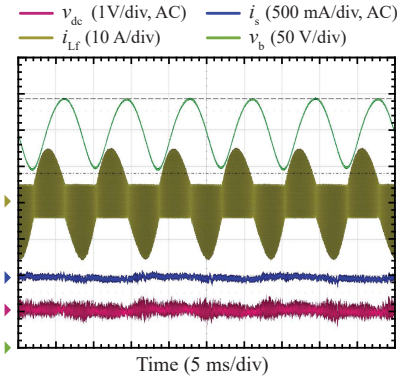


Fig. 3.8: Steady-state performance of the realized PCI converter at 2 kW rated power. The timebase of the measurement is 5 ms/div. Probes for measuring the converter input current and the DC-link voltage are AC coupled in order to highlight the excellent ripple cancellation.

step. After a transient time of 60 ms, the average buffer capacitor voltage has recovered and the intrinsic single-phase power pulsation is completely compensated by the PCI converter. During the transient, a small ripple is visible in the DC-link voltage. Take note that because of the $R_s = 10\,\Omega$ input resistor (cf. Fig. 3.1(c)), the average DC-link voltage decreases with increasing power and therefore settles at a lower value after the transient. The reactive power drawn by the EMI filter of the inverter stage is also compensated by the PCI converter, thus a small ripple is present in the buffer capacitor voltage prior to the load step although no load is connected to the inverter. Analogously, a step down from 700 W to 0 W is depicted in Fig. 3.9(b). Prior to the load step, the converter system was operating in steady-state exhibiting a 50 V peak-to-peak voltage ripple in the buffer capacitor. Triggered by the load drop, the average buffer capacitor voltage temporarily increases up to 350 V and settles after approximately 60 ms to the reference value. The DC-link voltage remains tightly controlled during the entire transient, showing virtually no overshoot but a small voltage ripple of ≈ 5 V during the transient.

This surpasses the required performance specified in the GLBC technical requirements [2], where load steps of maximal 500 W had to be handled within 1 s. Due to the 10 Ω resistor of the application, the DC-link voltage settles at a higher value after the transient.

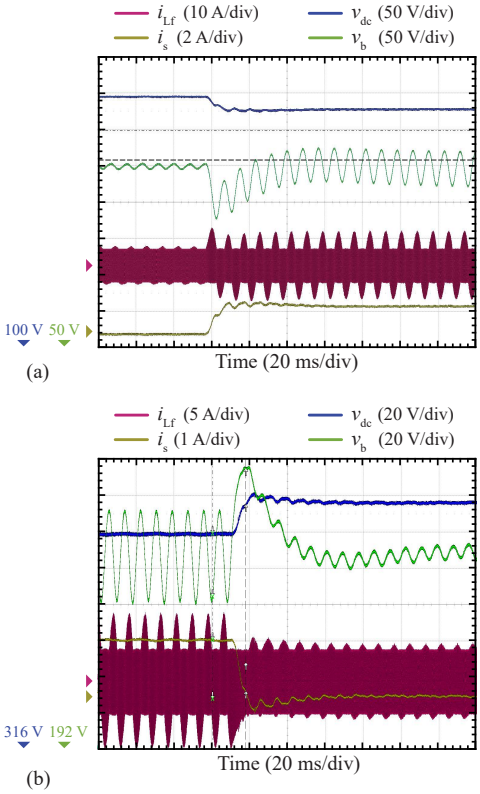


Fig. 3.9: PCI converter transient response to (a) an abrupt load step from 0 W to 700 W and (b) an abrupt load drop from 700 W to 0 W. The timebase of the measurement is 20 ms/div.

3.3 [SVI\C] Power Buffer

3.3.1 Mathematical Model of the [SVI\C] Buffer

For the setup of the [SVI\C] buffer as depicted in Fig. 3.1(d), the DC-link capacitor voltage is, likewise to (3.7), given by

$$v_{dc}(t) = \sqrt{V_{dc,0}^2 - \frac{S_b \sin(2\omega t - \tilde{\phi})}{\omega C_{dc}}}, \tag{3.16}$$

wherein $V_{\mathrm{dc},0}$ is the RMS value of $v_{\mathrm{dc}}(t)$ and also corresponds to the initial voltage at $t = \frac{\tilde{\phi}}{2\omega}$. Moreover, referring to Fig. 3.1(b), it must hold that

$$\bar{v}_{\mathrm{dc}} = \frac{1}{T}\int_0^T v_{\mathrm{dc}}(t)\mathrm{d}t \stackrel{!}{=} V_{\mathrm{s}} - I_{\mathrm{s}} \cdot R_{\mathrm{s}}. \tag{3.17}$$

Because the voltage ripple of the DC-link capacitor is compensated by means of the SVI converter, a much wider voltage swing across the DC-link is feasible. The actual minimum size of the DC-link capacitor is limited by the voltage requirement of the inverter to generate v_{ac} at the output. For this reason, $v_{\mathrm{dc}}(t) > v_{\mathrm{ac}}(t)$ has to be ensured at all times which requires a minimum capacitance of

$$C_{\mathrm{dc,min}} \geq \max_t \frac{S_b \sin(2\omega t - \tilde{\phi})}{\omega\left(V_{\mathrm{dc},0}^2 - (\hat{V}_{\mathrm{ac}}\cos(\omega t))^2\right)}. \tag{3.18}$$

For $\tilde{\phi} = 0$, (3.18) can be expressed analytically in a compact form,

$$C_{\mathrm{dc,min}} \geq \frac{S_b}{\omega V_{\mathrm{dc},0}\sqrt{V_{\mathrm{dc},0}^2 - \hat{V}_{\mathrm{ac}}^2}}. \tag{3.19}$$

The operation of the system with minimal DC-link capacitance, which amounts to $C_{\mathrm{dc,min}} \approx 62.66\,\mu\mathrm{F}$ for the given system parameters, is shown in Fig. 3.10(a).

From a practical point of view it is not reasonable to design the power buffer with $C_{\mathrm{dc,min}}$ since there is no voltage margin and the large resulting voltage ripple of $\pm 100\,\mathrm{V}$ requires the SVI converter to generate high voltages and process power levels of up to 500 W at rated output power. Following a more conservative approach,

$$\min_t v_{\mathrm{dc}}(t) \geq \frac{\hat{V}_{\mathrm{ac}}}{m_{\mathrm{inu,max}}}, \tag{3.20}$$

the minimum DC-link capacitance is given by

$$\begin{aligned}\widetilde{C}_{\mathrm{dc,min}} &= \frac{S_{\mathrm{b}}}{\omega(V_{\mathrm{dc},0}^2 - (\hat{V}_{\mathrm{ac}}/m_{\mathrm{inu,max}})^2)} \\ &= 298.4\,\mu\mathrm{F}\ (\approx 5 \cdot C_{\mathrm{dc,min}}),\end{aligned} \tag{3.21}$$

whereby $|m_{\mathrm{inu}}| \leq m_{\mathrm{inu,max}} = 0.9$ is the maximum allowed modulation index of the inverter. Note, that (3.20) is more demanding compared to the condition

$$\min_t v_{\mathrm{dc}}(t) \geq \frac{v_{\mathrm{ac}}(t)}{m_{\mathrm{inu,max}}}. \tag{3.22}$$

As can be seen from Fig. 3.10(a), assuming a design according to (3.21), the peak value of the varying voltage only amounts to $\approx \pm 20\,\mathrm{V}$ and consequently the SVI converter only processes up to 100 W at rated output power of the inverter and can be implemented with low voltage (100 V) components. Likewise to (3.9), selecting a more conservative DC-link capacitor size ($C_{\mathrm{dc}} > 5 \cdot C_{\mathrm{dc,min}}$) allows to approximate the square root function in the analytical expression of the DC-link voltage,

$$v_{\mathrm{dc}}(t) \approx V_{\mathrm{dc},0} - \frac{1}{2}\frac{S_b \sin(2\omega t - \tilde{\phi})}{\omega C_{\mathrm{dc}} V_{\mathrm{dc},0}}. \tag{3.23}$$

In order to compensate the remaining DC-link voltage ripple and meet the technical specifications, the required voltage across the filter capacitor C_{f} is given by

$$v_{\mathrm{Cf}}(t) = -\frac{1}{2}\frac{S_b \sin(2\omega t - \tilde{\phi})}{\omega C_{\mathrm{dc}} V_{\mathrm{dc},0}}. \tag{3.24}$$

The current in the filter inductor L_{f} averaged over the switching cycle can then be expressed by

$$i_{\mathrm{Lf}}(t) = C_{\mathrm{f}} \cdot \frac{\mathrm{d}v_{\mathrm{Cf}}}{\mathrm{d}t} - I_{\mathrm{s}} \approx -I_{\mathrm{s}}. \tag{3.25}$$

Typically for a small filter capacitance, $C_{\mathrm{f}} \approx 10\,\mu\mathrm{F}$, the amplitude of the capacitive charging currents to meet the low-frequency (LF) sinusoidal compensation voltage is negligible compared to the ideally constant DC source current I_{s}. Interestingly, for the sizing of the buffer capacitor this approximation also holds for much larger filter capacitor values. Fig. 3.10(b) depicts the switching cycle averaged buffer capacitor current, $i_{\mathrm{Cb}} = m_{\mathrm{b}} i_{\mathrm{Lf}}$, with constant filter inductor current ($i_{\mathrm{Lf}} \approx -I_{\mathrm{s}}$) and with pronounced ripple at twice the AC frequency considering a large filter capacitor, $C_{\mathrm{f}} = 100\,\mu\mathrm{F}$. Because of the averaging introduced by the duty cycle variation to generate the sinusoidal voltage at the SVI converter output, the resulting buffer capacitor charging currents are nearly identical. This also explains why the buffer capacitor does not exhibit a voltage ripple at a quadruple of the AC frequency while

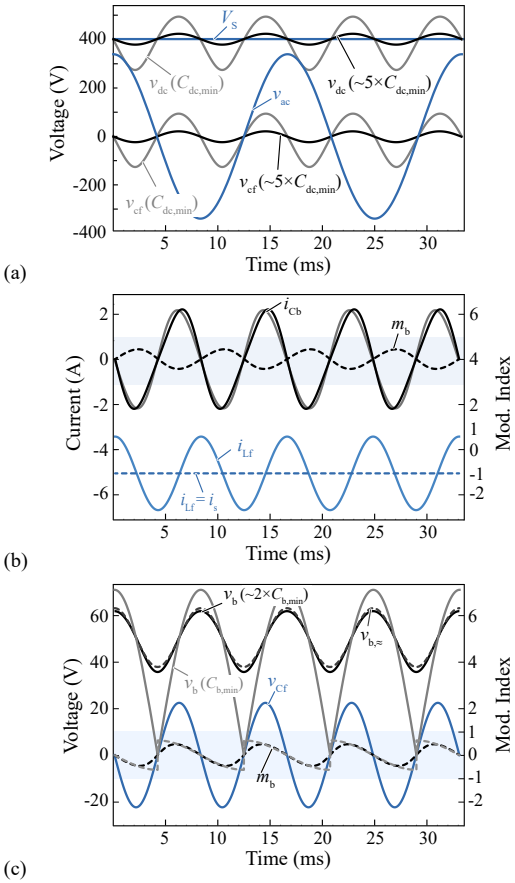


Fig. 3.10: Simulated waveforms of the derived mathematical model of the [SVI\C] buffer for different component values. (a) Operation with theoretical minimal installed DC-link capacitance $C_{\mathrm{dc,min}}$ according to (3.19) and more practical relevant dimensioning with $\tilde{C}_{\mathrm{dc,min}} = 5C_{\mathrm{dc,min}}$. (b) Impact of the size of the switching ripple filter capacitor C_{f} on average buffer capacitor current i_{Cb}. (c) Operation with theoretical minimal installed buffer capacitance $C_{\mathrm{b,min}}$ and more practical relevant dimensioning with $\tilde{C}_{\mathrm{b,min}} \approx 1.4C_{\mathrm{b,min}}$. m_{b} indicates the modulation index of the SVI converter.

generating a sinusoidal voltage with twice the fundamental AC frequency at the SVI converter output. In order to ensure v_{Cf} according to (3.24), the

H-bridge circuit must generate

$$v_{\mathrm{fb}} = v_{\mathrm{Cf}} - v_{\mathrm{Lf}} = v_{\mathrm{Cf}} - L_f \frac{\mathrm{d}i_{\mathrm{Lf}}}{\mathrm{d}t} \approx v_{\mathrm{Cf}}, \tag{3.26}$$

at its output terminals on average with respect to the switching cycle. Even for a large filter inductance, $L_{\mathrm{f}} = 100\,\mu\mathrm{H}$, and a large peak value of the 120 Hz superimposed charging current of $\approx 1.5\,\mathrm{A}$ (cf. Fig. 3.10(b)), the amplitude of the voltage drop across the inductor only amounts to around 100 mV and is therefore negligible compared to v_{Cf}. Based on these approximations, the differential equation governing the buffer capacitor voltage can be expressed as

$$C_{\mathrm{b}} \frac{\mathrm{d}v_{\mathrm{b}}}{\mathrm{d}t} = m_{\mathrm{b}} \cdot i_{\mathrm{Lf}} = -\frac{v_{\mathrm{cf}}}{v_{\mathrm{b}}} I_{\mathrm{s}}, \tag{3.27}$$

with the analytical solution

$$v_{\mathrm{b}}(t) = \sqrt{V_{\mathrm{b},0}^2 + \frac{I_{\mathrm{s}} S_{\mathrm{b}} \cos(2\omega t - \tilde{\phi})}{2\omega^2 C_{\mathrm{b}} C_{\mathrm{dc}} V_{\mathrm{dc},0}}}, \tag{3.28}$$

whereby $V_{\mathrm{b},0}$ is the RMS value of the buffer capacitor voltage and represents the initial voltage at $t = \frac{\tilde{\phi} - \pi/2}{2\omega}$. Similar to the derivation of the minimum DC-link capacitance, it must hold that $v_{\mathrm{b}}(t) \geq v_{\mathrm{Cf}}(t)$ at all times which allows to calculate the theoretical minimum value of the installed buffer capacitance,

$$C_{\mathrm{b,min}} = \frac{I_{\mathrm{s}} S_{\mathrm{b}}}{2\omega^2 C_{\mathrm{dc}} V_{\mathrm{b},0}^2 V_{\mathrm{dc},0}}, \tag{3.29}$$

resulting in $C_{\mathrm{b,min}} = 117.9\,\mu\mathrm{F}$ for a given bias voltage of $V_{\mathrm{b},0} = 50\,\mathrm{V}$. Similar to the PCI power buffer concept, the offset or average voltage of the buffer capacitor is a degree of freedom which will be exploited in the design optimization described in the next section. The simulated waveforms for operation with minimal buffer capacitance are depicted in Fig. 3.10(c). The buffer capacitor is fully utilized since its voltage drops to zero after every buffer cycle. As pointed out previously, for a practical implementation it is by far more reasonable to dimension the buffer capacitor to meet

$$\min_t v_{\mathrm{b}}(t) \geq \frac{\hat{V}_{\mathrm{cf}}}{m_{\mathrm{b,max}}}, \tag{3.30}$$

whereby $|m_{\mathrm{b}}| \leq m_{\mathrm{b,max}} = 0.9$ is the maximal allowed modulation index of the H-bridge (cf. Fig. 3.1(d)) and $\hat{V}_{\mathrm{cf}}$ is the crest value of the filter capacitor

voltage v_{cf}. With this condition, the minimum buffer capacitor size is given by

$$C_{\mathrm{b},\approx} = \frac{2m_{\mathrm{b,max}}^2 C_{\mathrm{dc}} V_{\mathrm{dc},0} I_{\mathrm{s}} S_{\mathrm{b}}}{4m_{\mathrm{b,max}}^2 \omega^2 C_{\mathrm{dc}}^2 V_{\mathrm{dc},0}^2 V_{\mathrm{b},0}^2 - S_{\mathrm{b}}^2} = 155.9\,\mu\mathrm{F}. \tag{3.31}$$

As can be seen from the waveforms in Fig. 3.10, installing at least $2 \cdot C_{\mathrm{b,min}} \approx 240\,\mu\mathrm{F}$ of buffer capacitance allows to approximate the exact buffer capacitor voltage (3.28) with

$$v_{\mathrm{b},\approx}(t) \approx V_{\mathrm{b},0} - \frac{1}{4}\frac{I_{\mathrm{s}} S_{\mathrm{b}} \cos(2\omega t - \tilde{\phi})}{\omega^2 C_{\mathrm{b}} C_{\mathrm{dc}} V_{\mathrm{dc},0} V_{\mathrm{b},0}}. \tag{3.32}$$

Likewise to the PCI converter, the dimensioning and loss calculation of the DC-link and buffer capacitor of the [SVI\C] buffer relies on the approximated waveforms given by (3.23) and (3.32).

3.3.2 [SVI\C] Pareto Optimization

As described in the previous section, the minimum DC-link voltage requirement of the inverter stage defines the minimum feasible capacitor size. Moreover, depending on the selected capacitor technology, also the maximum allowed ripple current imposes a restriction on the minimum feasible capacitance size. With decreasing size of the installed DC-link capacitance, the amplitude of the 120 Hz voltage ripple and thus the power and voltage rating of the SVI converter increases. In this work, the DC-link capacitance is chosen large enough such that the SVI converter only processes up to maximal 150 W and can be implemented with LV technology. In order to accomplish a cost-effective and reliable implementation of the [SVI\C] buffer, 450 V ultra-compact aluminum electrolytic capacitors from TDK (B43630 series) in the range of 390 µF – 680 µF are considered in the design optimization for the implementation of the DC-link capacitance. It would be in principle possible to implement the DC-link capacitance with ceramic capacitor technology, however, the prohibitively high cost and the large number of over 400 MLCC chips renders this design approach impractical and unreliable. Also, the minimum available electrolytic capacitor 390 µF is reasonably close to the theoretical minimum given by (3.21) for a maximum modulation index of 0.9 of the inverter.

For the implementation of the H-bridge, 100 V/7 mΩ E-Mode GaN transistors from EPC (EPC2001C) with unipolar PWM and a switching frequency

in the range of 50 kHz – 300 kHz are considered in the design optimization. Similar to the design space of the PCI converter, for the design of the HF filter inductor L_f various E-type core geometries with N87 MnZn ferrite material and available HF-litz wires are considered in the optimization. For the implementation of the buffer capacitor C_b both 100 V/15 µF class II/X7S MLCC and 200 V ultra-compact aluminum electrolytic capacitors (also from TDK's B43630 series) are considered. For cost and assembly related restrictions as mentioned previously, a buffer capacitance range of 200 µF – 1000 µF is considered in case of the buffer capacitance implementation with MLCCs. The effective capacitance for the class II/X7S buffer capacitor subject to a DC bias was obtained from the datasheet provided by the manufacturer [93]. Furthermore, the power loss due to the LF voltage ripple was calculated based on the extrapolated Equivalent Series Resistance (ESR) value of the

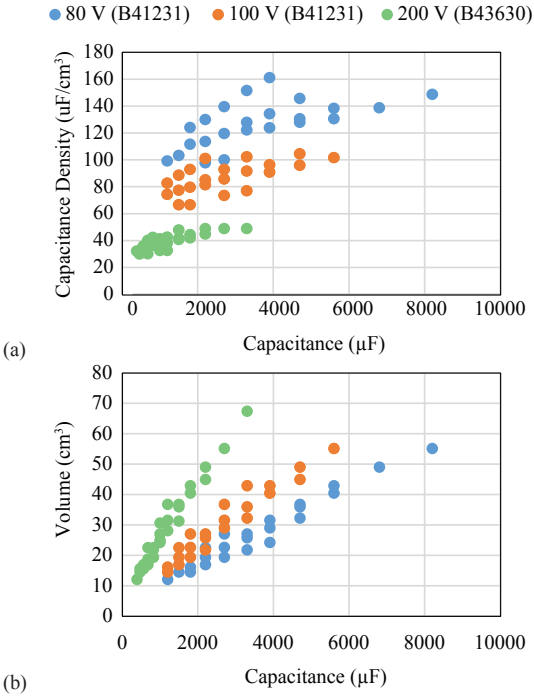


Fig. 3.11: (a) Capacitance density and (b) boxed volume as a function of available capacitance of TDK's B43630 and B41231 electrolytic capacitor series.

Tab. 3.4: System Parameters & Search Locus of the [SVI\C] Converter Pareto Optimization.

Feature	Range/Option
DC-link Cap. Technology	450 V ultra-compact aluminum electrolytic (TDK B43630-Series)
C_{dc}	[390 µF, 680 µF]
Buffer Cap. Technology	100 V X7S/class II (TDK C5750X7S2A156M250KB)
	200 V ultra-compact aluminum electrolytic (TDK B43630-Series)
C_b	[200 µF, 1 mF] (MLCC)
	[390 µF, 3.3 mF] (electrolytic cap.)
$V_{b,0}$	$m_{b,0} = [0.35, 0.65]$, $V_{b,0} = \hat{V}_{Cf}/m_{b,0}$
Inductor Technology	N87 ferrite, E-core, round and HF litz wire
L_f	[1 µH, 100 µH]
Semiconductor	100 V/7 mΩ GaN e-HEMT (EPC 2001C)
f_s	[50 kHz, 300 kHz] (PWM w/ const. f_s)
Heat sink	CSPI = 25.7 W/(K dm^3)

class II/X7S MLCC specified at 1 kHz in the datasheet (minimum frequency with specified ESR value). In accordance with the available capacitance values of the 200 V B43630 series, a capacitance in the range of 390 µF – 3300 µF is considered in the design space. As shown in Fig. 3.11(a), capacitors with lower voltage rating typically feature higher capacitance per volume. However, as can be seen from Fig. 3.11(b), for very low capacitance values in the range of 390 µF – 1000 µF, the effective boxed volumes of 80 V, 100 V and 200 V electrolytic capacitors are very similar. Thus, in order to limit the modeling effort, the same electrolytic capacitor technology (B43630 ultra-compact series) is considered for the implementation of the DC-link (450 V model) and the buffer capacitor (200 V model). As described in the previous section, the bias voltage of the buffer capacitor is a further degree of freedom in the optimization and is adjusted by means of varying the average modulation index of the SVI converter,

$$m_{b,0} = \frac{\hat{V}_{Cf}}{V_{b,0}}, \tag{3.33}$$

in the range of 0.35 – 0.65 for a given size of the DC-link capacitor and resulting output voltage amplitude $\hat{V}_{Cf}$. The design space variables are summarized

in Tab. 3.4. Given the described design space and elaborate loss and volume models of the utilized components, a large number of possible [SVI\C] designs was calculated. Figs. 3.12(a) & (b) display the $\eta\rho$-performance of the designs with aluminum electrolytic and ceramic buffer capacitor, respectively. Designs with different DC-link capacitor sizes are distinguished by color.

As can be seen in Fig. 3.12(a), using electrolytic capacitors to implement the buffer capacitance, a maximal power-density of about 35 kW/dm^3 (574 W/in^3)

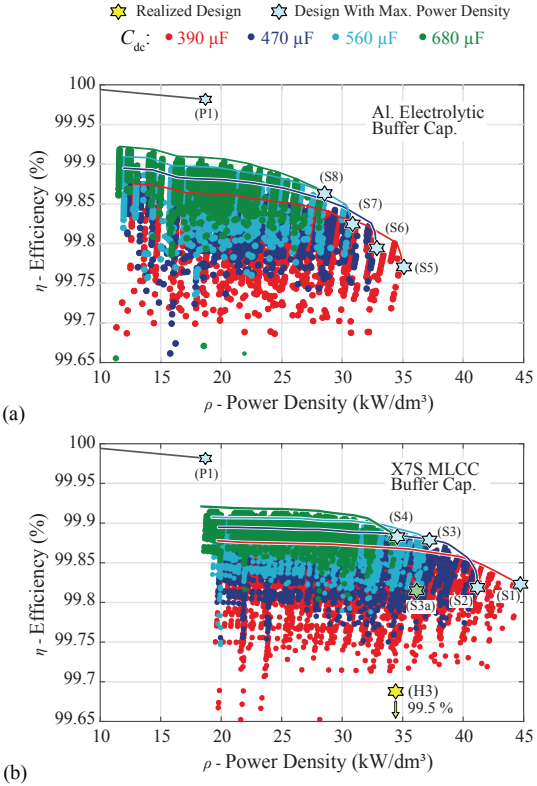


Fig. 3.12: $\eta\rho$-plot of the calculated [SVI\C] designs with indicated Pareto fronts. (a) Both DC-link and buffer capacitor are implemented with 450 V and 200 V electrolytic capacitor technology, respectively. (b) The DC-link is implemented with 450 V electrolytic capacitor technology and the buffer capacitor is implemented with 100 V class II/X7S MLCC technology.

at an efficiency of 99.77 % is achieved for design (S5) with the smallest considered DC-link capacitance of 390 µF. As can be seen from Fig. 3.12(b), the power-density can be further increased if the buffer capacitor is implemented with 100 V/X7S ceramic capacitors. For the smallest available DC-link capacitance, a maximal power-density of almost 45 kW/dm^3 (737 W/in^3) at a nominal efficiency of 99.83 % of design (S1) is possible according to the optimization results.

The volume and loss distribution of several selected Pareto optimal designs is shown in Figs. 3.13(a) & (b), respectively. From the volume balance it can be clearly seen that the size of the DC-link capacitor is dominating the overall volume. Comparing the two designs with maximal power-density (S1) and (S5)

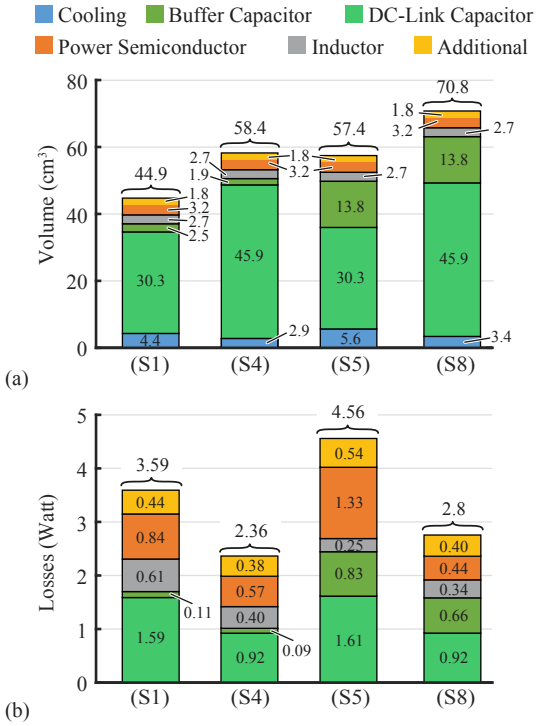


Fig. 3.13: (a) Volume and (b) loss distribution of selected Pareto optimal [SVI\C] designs.

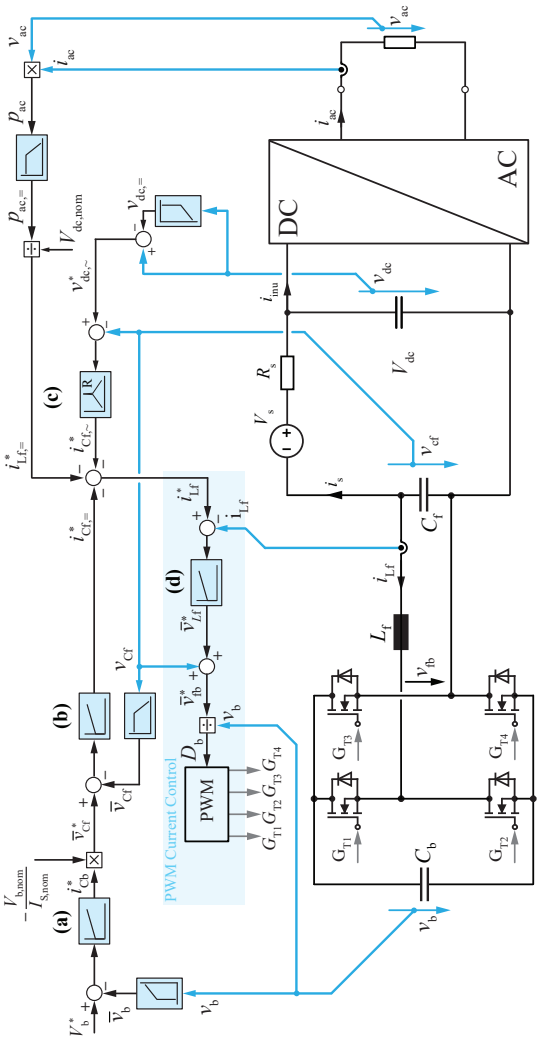


Fig. 3.14: Proposed cascaded control structure of the SVI converter of the [SVI\C] power buffer. (a) Control of the average buffer capacitor voltage $\overline{v}_\mathrm{b}$. (b) Feed-forward control of the average AC power (real power). (c) Compensation of the DC-link voltage ripple. (d) Inner loop control of filter inductor current i_Lf with PWM.

using ceramic and electrolytic capacitor, it can be seen that the higher power-density of design (S1) is mainly ascribed to the more compact implementation of the buffer with X7S MLCCs. As can be seen from Fig. 3.13(b), the electrolytic buffer capacitor also exhibits higher power loss.

The realized design indicated with label (H3) in Fig. 3.12(b) and described in detail in Section 3.3.4 achieves a power-density of 34.5 kW/dm^3 (565 W/in^3) at an efficiency of 99.5 %.

3.3.3 Control System of the SVI Converter

The control system proposed to regulate the SVI converter is depicted in Fig. 3.14. The installed DC-link capacitor is large enough to prevent severe overshoots and sags in the DC-link voltage during load transients. For this reason, there is less demand on the dynamic performance of the control system which allows to omit the feed-forward control of the fluctuating AC power and the cascaded DC-link voltage control. Referring to Fig. 3.14, control subsystem (c) cancels the 120 Hz voltage ripple present in v_{dc}. The reference $v^*_{\mathrm{dc},\sim}$ of the auxiliary converter output voltage control is obtained by means of subtracting the average DC-link voltage, $v_{\mathrm{dc},=}$, from the measured value v_{dc}. In order to extract the average DC-link voltage $v_{\mathrm{dc},=}$ a moving-average low-pass filter with window size of one 120 Hz period is employed. A purely resonant compensator (proportional gain set to zero) tuned at 120 Hz is employed to regulate the output voltage v_{cf} to precisely track the reference $v^*_{\mathrm{dc},\sim}$ and thus completely cancel the 120 Hz voltage ripple present in v_{dc}. Likewise to the PCI converter controls presented in the Section 3.2.3, control subsystem (a) is employed to keep the mean value of the buffer capacitor voltage $\bar{v}_{\mathrm{b}} = V_{\mathrm{b}}$ at a chosen reference. The output of the PI controller, current reference i^*_{Cb}, is multiplied with the constant scaling factor $-V_{\mathrm{b,nom}}/I_{\mathrm{s,nom}}$ to obtain voltage reference $\bar{v}^*_{\mathrm{cf}}$. This scaling factor relates the charging/discharging power of the buffer capacitor, $v_{\mathrm{b}} \cdot i_{\mathrm{b}}$, to the power which must be provided/absorbed at the output of the SVI converter $\approx v_{\mathrm{cf}} I_{\mathrm{s}}$. According to the voltage/current directions as shown in Fig. 3.14 and the condition $I_{\mathrm{s}} \geq 0$, a positive/negative bias in v_{Cf} discharges/charges the buffer capacitor over time, respectively. During idle mode of the converter, when no real power is transferred to the AC side and I_{s} is essentially zero, the buffer capacitor voltage cannot be kept at its desired bias voltage level. For this reason it is crucial to include an anti-windup logic in the series compensating voltage PI controller. The average filter capacitor bias voltage $\bar{v}_{\mathrm{Cf}}$ is then regulated to meet the reference $\bar{v}^*_{\mathrm{Cf}}$ by means of an inner-loop PI controller which outputs current reference $i^*_{\mathrm{Cf},=}$ (cf.

Tab. 3.5: Technical Details of the Realized [SVI\C] Buffer.

Feature	Value	Description
Volume (no cooling)	54.0 cm^3 (2.1 in^3)	Boxed component volume of the [SVI\C] buffer without heat sink
Volume (with cooling)	58 cm^3 (3.5 in^3)	Total volume of the constructed [SVI\C] buffer with a CSPI = 27.5 $W/(K\,dm^3)$ heat sink
Capacitor volume	42.9 cm^3 (2.6 in^3)	Total volume of installed buffer capacitor and DC-link capacitor volume (boxed)
η	99.52 %	Efficiency at 2 kW
L_f	33 µH	Coilcraft XAL1510-333MED
C_f	60 µF	4 × 15 µF 100 V/X7S MLCC
C_b	260 µF	Equivalent large signal capacitance of the installed 45× 15 µF/100 V/X7S MLCC
C_{dc}	560 µF	Ultra-compact aluminum electrolytic capacitor technology (EPCOS B43991-X0009-A224)

Fig. 3.14(a)). Similar to the PCI converter controls described previously, the control objectives are combined in a single reference for the filter inductor current, i^*_{Lf}. Note that the source current I_s must flow entirely through L_f since it holds that $\bar{i}_{Cf} = 0$ in steady-state. For this reason, $i^*_{Lf,=}$ is calculated based on the real power of the AC load and added to the filter current reference (cf. Fig. 3.14(b)). A satisfying initial set of control parameters for the PI and Resonant compensators was empirically determined with the aid of extensive circuit simulations and then fine tuned during testing of the converter prototype (cf. Section 3.3.4).

3.3.4 Hardware Implementation and Experimental Verification

Benefiting from the gained insights of the design optimization in Section 3.3.2, a prototype of the [SVI\C] buffer as shown in Fig. 3.15 was implemented in hardware. The design parameters and selected features of the realized system are summarized in Tab. 3.5. By the courtesy of TDK, a custom 560 µF/450 V aluminum electrolytic capacitor with ≈ 40 % higher capacitance density but reduced lifetime compared to B43630 series (cf. Section 3.3.2) was available. The buffer capacitor C_b was implemented with a total of 45 single 15 µF/100 V, class II/X7S MLCC chips. With a bias voltage of the buffer capacitor set to 55 V

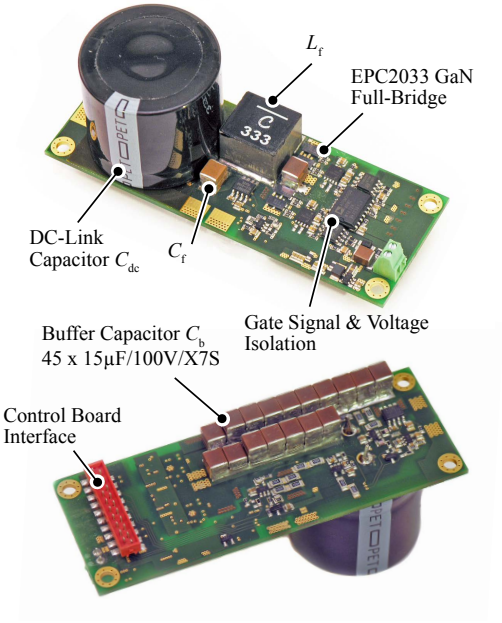


Fig. 3.15: Picture of the implemented [SVI\C] buffer. The shown aluminum electrolytic capacitor is buffering the DC-link and the buffer capacitor of the SVI converter is implemented with ceramic capacitors.

in the control system (cf. Section 3.3.3), the effective large-signal capacitance amounts to 260 µF.

Since the EPC2001C 7 mΩ/100 V GaN transistors were unavailable at the time of the prototype design, the H-bridge was implemented with EPC2033 7 mΩ/150 V e-mode GaN transistors from EPC which feature similar $R_{ds,on}$ values but higher output capacitance C_{oss}. The switching frequency per bridge-leg is set to 70 kHz which, in case of the employed unipolar PWM, corresponds to an effective switching frequency of 140 kHz and matches the switching frequency of the 2nd version of the Little Box inverter operated with PWM (cf. Fig. 3.6(b)). The gate-drive is implemented based on the LM5113 half-bridge driver IC with bootstrap supply of the high-side transistors. In addition, power and gate-signal isolation is implemented with the ADuM500 and SI8620 ICs, respectively. The filter inductor, $L_f = 33$ µH, was implemented by means of an off-the-shelf available inductor from Coilcraft's XAL1510

series (XAL1510-333MED, 12 A, $R_{dc} = 20\,m\Omega$). The maximum current ripple amounts to approximately 2.5 A peak-to-peak and occurs at the maximum of the output voltage v_{Cf}. The control system proposed in the previous section was also implemented on the *TMS320F28335* microcontroller from Texas Instruments which was located on an external control PCB (cf. Fig. 3.15, control board interface). All necessary analog measurement circuits to sense v_{dc}, v_{cf}, i_{Lf}, and the buffer voltage v_b are placed on the prototype PCB. The inner current feedback loop is executed with a frequency of 140 kHz and the voltage feedback loops and feed-forward control are executed at 28 kHz.

The efficiency according to (3.15) of the [SVI\C] buffer measured with a Yokogawa WT3000 precision power analyzer is depicted in blue in Fig. 3.16. For comparison, the efficiency curves of the two variants of PCI converter presented in Section 3.2.4 are shown in grey. At rated output power of 2 kW, the [SVI\C] buffer exhibits an efficiency of 99.52 %. As can be seen, at high output power > 1.7 kW, the efficiency of the PCI converter with class II/X6S capacitors is just slightly lower. However as mentioned before, one of the major advantages of the [SVI\C] approach is the excellent partial-load efficiency. The measured peak efficiency amounts to 99.8 % at about 578 W output power. Even at a very low output power of around 200 W, the efficiency of the buffer remains above 99.2 %. The achieved power-density based on aggregated boxed component volume amounts to 34.5 kW/dm^3 (565 W/in^3). Since the [SVI\C] buffer prototype was designed to facilitate

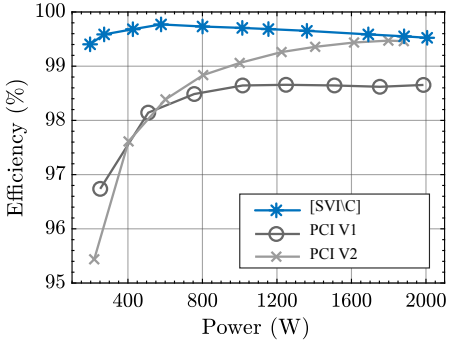


Fig. 3.16: Measured efficiency of the constructed [SVI\C] buffer prototype as a function of apparent power S_b. For reference, the efficiency of the PCI converter prototypes is shown in grey.

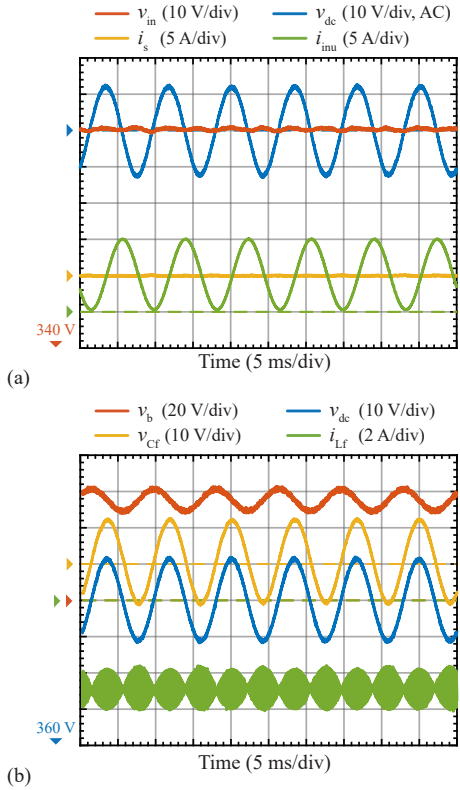


Fig. 3.17: Steady-state performance of the realized [SVI\C] buffer at 2 kW rated power. (a) Characteristic waveforms of the SVI converter. (b) Elimination of DC-link voltage ripple and resulting constant input voltage, v_{in}, and source current i_s.

testing in the laboratory, the components were not arranged to fit tightly in a rectangular enclosure and using the boxed volume of the entire prototype would lead to wrong conclusions regarding the achieved power-density of the implemented [SVI\C] buffer.

The steady-state performance at 2 kW rated power of the proposed control system is illustrated by the experimental measurements shown in Fig. 3.17. It can be seen from the recorded converter input voltage (cf. v_{in} in Fig. 3.17(a)) that the 120 Hz voltage ripple in the DC-link voltage v_{dc} is almost entirely compensated. Note, that the ripple of v_{dc} with an amplitude of around 22 V_{pp}

would violate the GLBC technical specification of 12 V_{pp} (3 % of 400 V). Although the current provided to the inverter, i_{inu}, exhibits the characteristic squared sinusoidal shape with a peak current of 10 A for delivering 2 kW of real power to the inverter, the current coming from the source i_s is perfectly constant due to the operation of the SVI converter. The characteristic waveforms of the auxiliary converter during stationary operation at rated power are shown in Fig. 3.17(b). As discussed in Section 3.3.1, because of the source current bias of i_{Lf} and the small amplitude of the required 120 Hz charging current such that v_{Cf} compensates the voltage ripple present in v_{dc}, the buffer capacitor voltage v_b exhibits only a distinct 120 Hz voltage ripple and no 240 Hz component. In order to verify the dynamic performance of the implemented control system, the main DC/AC converter was subject to load variations. The corresponding transient performance of the [SVI\C] buffer for a load step from 1 kW to 2 kW is depicted in Fig. 3.18(a). Triggered by the load step, the average SVI buffer capacitor voltage drops only roughly 10 V below the 55 V at steady-state and recovers within 20 ms. The voltage controller immediately adapts v_{Cf} to the increased amplitude of the DC-link voltage ripple which facilitates a very smooth transition of both the input voltage v_{in} and input current i_s. As already pointed out before, because of the 10 Ω input resistor (cf. Fig. 3.1), the input voltage v_{in} decreases with increasing power and therefore settles at a lower value after the transient. As a consequence of the increase in power being processed by the SVI converter, the amplitude of the characteristic 120 Hz voltage ripple across the buffer capacitor becomes more pronounced immediately after the load step. Analogously, a step down from 1250 W to 500 W is depicted in Fig. 3.18(b). Triggered by the load drop, the input voltage and current attains the new steady-state value smoothly without any overshoot. The output voltage v_{Cf} is immediately adjusted by the control system and therefore no considerable voltage fluctuation is present in v_{in} even during the transient which is approximately settled within 15 ms – 20 ms. This also clearly surpasses the required performance of the GLBC technical specifications.

3.4 Discussion

Fig. 3.19 summarizes and compares the Pareto optimization results of the PCI buffer presented in Section 3.2.2 and the [SVI\C] buffer presented in Section 3.3.2. In general, both the PCI converter equipped with 450 V class II/X6S MLCCs and the [SVI\C] buffer equipped with 100 V class II/X7S MLCCs and a 390 µF electrolytic DC-link capacitor can reach power densities above

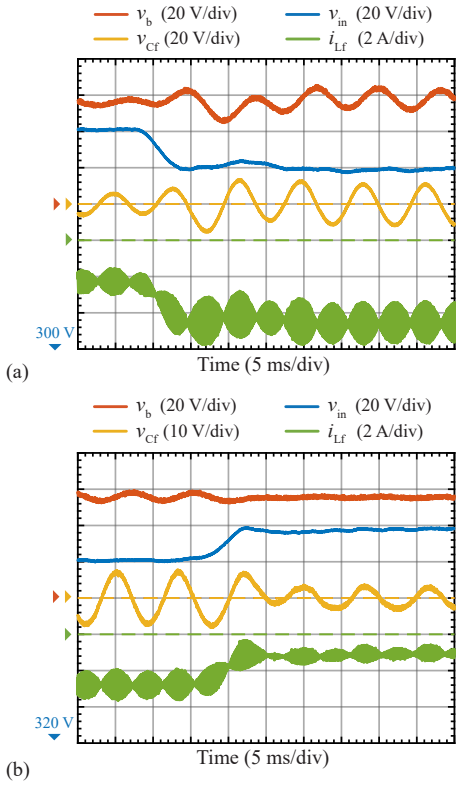


Fig. 3.18: [SVI\C] buffer transient response to (a) an abrupt load step from 1000 W to 2000 W and (b) an abrupt load drop from 1250 W to 500 W.

40 kW/dm^3 (656 W/in^3) and high efficiencies above 99.4 % at rated power. Based on the Pareto optimization results, it seems that the [SVI\C] buffer approach can potentially outperform the PCI converter both in terms of power-density and conversion efficiency. However, in accordance with the experimental results presented in the previous chapter, this has not been demonstrated in hardware so far. The maximum power-density of 41.3 kW/dm^3 (677 W/in^3) was achieved with the PCI converter prototype equipped with 450 V class II/X6S MLCCs and operated with 140 kHz PWM. Moreover, the implemented [SVI\C] buffer prototype (cf. Fig. 3.15) is a first, proof-of-concept implementation primarily designed to facilitate experimental testing and

verify the proposed control system described in Section 3.3.3. For this reason, the components have not been arranged to fit tightly into a cuboidal shape with minimum volume as it is the case for the PCI converter prototypes (cf. Fig. 3.6), which are already in a later, refined stage of development. As mentioned before, for a fair comparison, the sum of all boxed component volumes was used to calculate the power-density of the [SVI\C] buffer prototype rather than the boxed rectangular volume of the entire system shown in Fig. 3.15.

It is worth noting that, by employing aluminum electrolytic capacitors to implement both the DC-link and the buffer capacitance, the [SVI\C] buffer can still potentially reach high power densities up to 35 kW/dm^3 which outperforms the PCI converter with TCM modulation and CeraLink capacitors. This is particularly of interest regarding a cost-effective realization of the active power buffer. To exemplify, the 2nd version of the presented PCI converter uses 200 pieces of the 2.2 µF/450 V class II/X6S MLCCs which amounts to $290 of component cost for the buffer capacitor (order quantities above 1000 pieces considered). In contrast, a 390 µF/450 V electrolytic capacitor costs $4 and a 390 µF/200 V electrolytic capacitor costs just $2. Hence, the capacitor component cost of the all-electrolytic [SVI\C] buffer design (S5) amounts to only about $6. Striving for maximum power-density, the buffer capacitor can be implemented with 35× 15 µF/100 V X7S MLCCs (S1) which amounts to $62.3 and therefore results in a total capacitor component cost of about $66.3 for the [SVI\C] system. From this point of view, the [SVI\C] buffer and in particular the all-electrolytic [SVI\C] buffer is a very cost competitive approach and

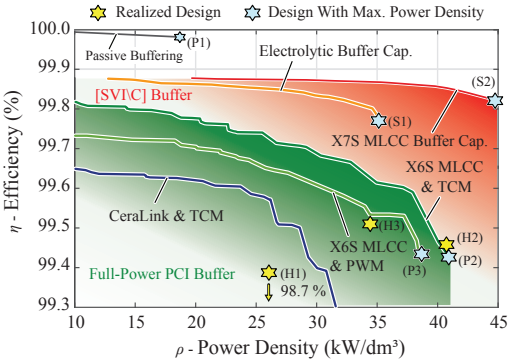


Fig. 3.19: Comparison of calculated $\eta\rho$-Pareto fronts of the PCI buffer and the [SVI\C] buffer.

clearly outperforms the PCI converter in this regard. Although it was not considered in the optimization of the PCI converter, it is in principle also possible to use aluminum electrolytic capacitors to implement C_b and thus achieve a significantly lower cost. However, because of the imposed lifetime related ripple current limitations, the minimum feasible buffer capacitor size results in a comparably low capacitor utilization (small amplitude of the buffer voltage swing) and it is therefore unlikely that this approach would actually yield a $\eta\rho$-competitive design.

As can be seen from the measured efficiencies of the implemented buffer prototypes (cf. Fig. 3.16), the [SVI\C] approach features the highest efficiency of 99.5 % at rated output power as opposed to the efficiency of 99.4 % of the PCI converter with class II/X6S MLCCs. It is important to mention that the worst case power measurement accuracy of the employed Yokogawa WT3000 power analyzer [94] amounts to ±8 W which corresponds to an uncertainty of the measured efficiency of up to ±0.4 %. This also suggests that the discrepancy between the efficiency of the Pareto optimal design (S1) and the realized hardware (H3) (cf. Fig. 3.19) is, besides a suboptimal implementation of the SVI converter and imperfections in the underlying component models of the optimization, attributed to uncertainty in the power measurements.

Due to the nature of the partial-power approach, the auxiliary converter only processes a small share of the entire fluctuating power and thus exhibits a very low power loss which explains the high efficiency. In this regard, one of the clear advantages of the [SVI\C] buffer is its excellent partial-load efficiency. At 500 W output power, the efficiency of the implemented [SVI\C] system amounts to around 99.7 % in contrast to the substantially lower efficiency of 98 % of the implemented PCI converter. The high partial-load efficiency is in particular beneficial to achieve a high CEC or European weighted efficiency of the inverter equipped with active buffer.

The presented experimental waveforms of the implemented prototypes are clearly demonstrating that the proposed control systems in Section 3.2.3 and Section 3.3.3, both achieve excellent mitigation of the 120 Hz DC-link voltage ripple and also clearly meet the transient response requirements specified in [2]. Because of the still comparably large capacitance of the installed aluminum electrolytic capacitor in case of the [SVI\C] buffer, abrupt load changes are handled with much less demand on the dynamic performance of the control system because the DC-link capacitance provides enough passive buffering to temporarily accommodate the power mismatch between DC and AC side without pronounced sags or overshoots in the DC-link voltage. On

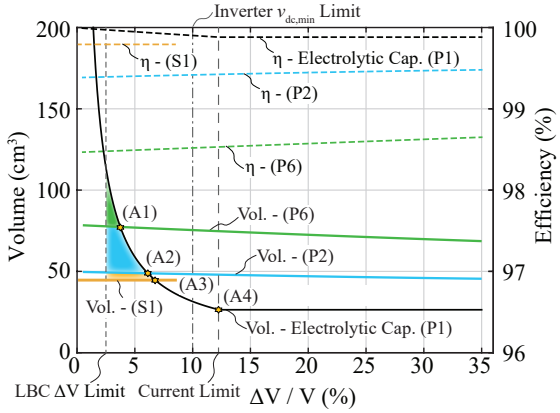


Fig. 3.20: Volume and efficiency comparison between conventional DC-link with electrolytic capacitors and optimally designed current or voltage injection power buffers with respect to the 2.5 % ΔV limit specified in [2].

the contrary, the small remaining DC-link capacitor of around 15 µF in case of the PCI converter concept, intended as commutation capacitor to reduce the parasitic inductance of the power loop, requires active stabilization of the DC-link voltage which leads to a somewhat more complicated control system. From this perspective, it can be argued that the [SVI\C] buffer in combination with the proposed control system for the SVI is more robust and exhibits better transient performance.

It is also interesting to compare the performance of the power buffers based on parallel current or series voltage injection with a conventional passive DC-link comprised of electrolytic capacitors and to determine the voltage ripple $\frac{\Delta V}{V}$ limit when it actually becomes beneficial in terms of volume to employ a converter based buffer concept and accept the increased hardware effort. A volume model was extracted by means of a least-square fit to the calculated boxed volumes of all possible DC-link assemblies generated with the ultra-compact 450 V electrolytic capacitors from TDK considered in this work [95], allowing at maximum five capacitors to be connected in parallel. The resulting volume of the DC-link with respect to the voltage ripple limit is depicted in Fig. 3.20. Decreasing ΔV results in a larger volume since more electrolytic capacitors have to be installed to meet the more stringent requirement. Likewise, relaxing the voltage ripple limit results in a volume reduction until the specified ripple current limitation of the

electrolytic capacitor prevents a further reduction in volume (A4). Given the calculated ESR for each capacitor assembly obtained from the data provided in [95,96], the power losses caused by the 120 Hz charging current is calculated and the resulting efficiency is depicted in Fig. 3.20. The Pareto optimal design (P2) with TCM and class II/X6S capacitors, and the optimal design (P6) with TCM and CeraLink capacitors were chosen from the PCI converter designs for the volume benchmarks. Typically, the proposed control system as proposed in Section 3.2.3 achieves complete ripple cancellation, but can be modified to tolerate a certain ΔV across C_{dc}, which slightly changes the rated power of the PCI converter design according to $\tilde{S}_b = S_b - \Delta E_{\mathrm{dc}}\omega$. The performance of the designs (P2) and (P6) were recalculated for several voltage ripple limits. Likewise, the Pareto optimal [SVI\C] buffer design (S1) is also included in the benchmark. For the 390 µF DC-link capacitor employed in (S1), the voltage ripple at the input, if the SVI converter compensation reference is set to zero, amounts to $\Delta V = 34\,\mathrm{V}$ and explains why the trace stops at $\frac{\Delta V}{V} \approx 8.5\,\%$. As indicated by intersection (A2) between the total volume of design (P2) and the electrolytic capacitor, it becomes beneficial (only considering volume) to employ a PCI converter if a $^{\Delta V}/_{V} = 6\,\%$ or less is demanded. For the design (P6) with CeraLink capacitors the intersection (A1) occurs at $^{\Delta V}/_{V} = 3.7\,\%$. Considering the intersection (A3) between the total volume of the optimal [SVI\C] buffer design (S1) and the electrolytic capacitor, it becomes beneficial to employ an [SVI\C] buffer (with ceramic buffer capacitor) if a $^{\Delta V}/_{V} = 6.8\,\%$ or less is demanded. Also indicated in the plot is the admissible 2.5 % voltage ripple limit specified in [2] (cf. Section 3.1), which reveals that roughly 35 cm^3 of volume were saved with the PCI converter (CeraLink/TCM) in the 1st version of the Google Little Box and about 65 cm^3 of volume were saved with the PCI buffer (class II/X6S-PWM) in case of the 2nd implementation of the Little Box. Concerning efficiency, Fig. 3.20 shows that passive capacitive DC-link buffering with electrolytic capacitors always achieves a higher efficiency compared to an optimal designed buffer employing current or voltage injection stages regardless of the specified voltage ripple limit.

3.5 Summary

In order to shrink the volume of the energy storage required in single-phase inverter systems to cope with the 120 Hz fluctuating AC power, the power pulsation buffer concepts selected by the 1st and 2nd prize winner of the Google Little Box Challenge (GLBC) were analyzed in detail and compara-

tively evaluated in this chapter. Based on Pareto optimization results, the full-power processing Parallel Current Injector (PCI, approach of the 1st prize winner) can reach power densities as high as 41.3 kW/dm^3 (677.1 W/in^3) mainly because of the small feasible buffer capacitance values. The [SVI\C] buffer (approach of the 2nd prize winner) employing a partial-power Series Voltage Injector (SVI) converter equipped with 100 V class II/X7S ceramic capacitors can reach power densities as high as 45 kW/dm^3 (737 W/in^3) and mainly benefits from the low heat sink volume due to its very high efficiency. Experimental results obtained from three prototype implementations of the considered concepts were presented. The first version of the PCI converter employing CeraLink capacitors features an efficiency of 98.7 % at rated power and an overall volume of 76.6 cm^3 (4.7 in^3) which corresponds to a power-density of 26.1 kW/dm^3 (428 W/in^3). The second version of the PCI converter employing 450 V class II/X6S capacitors features an efficiency of 99.4 % at rated power and an overall volume of 48.4 cm^3 (3.0 in^3) which corresponds to a power-density of 41.3 kW/dm^3 (676.8 W/in^3). The implemented [SVI\C] buffer prototype achieved an efficiency of 99.5 % at rated power and an overall volume of 58 cm^3 (3.5 in^3) which corresponds to a power-density of 34.5 kW/dm^3 (565 W/in^3). Clearly, one major advantage of the presented [SVI\C] buffer is the remarkable partial-load efficiency with a measured peak value of 99.8 % at ≈ 580 W output power. According to the comparison with a conventional capacitive buffered DC-link using only electrolytic capacitors, it becomes beneficial in term of volume to employ an optimized active power buffer if a ripple requirement of $^{\Delta V}/_{V} = 6 - 7\,\%$ or less is demanded by the application. The outstanding performance of the presented cascaded control structures for the PCI and [SVI\C] buffer under stationary conditions (120 Hz voltage ripple compensation) and subject to stepwise load changes was demonstrated by means of experimental waveforms which showed that the technical requirements of the Google Little Box Challenge (GLBC) were clearly met. Because of the still comparably large capacitance provided by the installed electrolytic capacitor in case of the [SVI\C] buffer approach, abrupt load changes are handled with much less demand on the dynamic performance of the digital control system. With respect to cost, it is possible to implement an all-electrolytic [SVI\C] buffer design with, according to the conducted Pareto optimization, still high power-density of ≈ 35 kW/dm^3 (574 W/in^3) and at a very low expense of only $ 6 of total capacitor cost as opposed to the $ 290 needed to implement the class II/X6S buffer capacitor of the presented PCI buffer approach.

4

The Google Little Box Inverter

Chapter Abstract

Guided by the results of a preceding multi-objective $\eta\rho$-Pareto optimization (cf. Section 2.7), this chapter presents the hardware implementations and novel control concepts of two GaN-based inverter concepts to overcome the Google Little Box Challenge (GLBC): (i) Little Box 1.0 (LB 1.0), a H-bridge inverter with two interleaved bridge-legs both operated with Triangular Current Mode (TCM) modulation which features a power-density of $8.18\,\mathrm{kW/dm^3}$ ($134\,\mathrm{W/in^3}$) and a nominal efficiency of $96.4\,\%$ and (ii) Little Box 2.0 (LB 2.0), an inverter topology with single bridge-leg DC/|AC| buck-stage operated with constant frequency PWM and a subsequent |AC|/AC H-bridge unfolder, which features a remarkable power-density of $14.8\,\mathrm{kW/dm^3}$ ($243\,\mathrm{W/in^3}$) and a nominal efficiency of $97.4\,\%$. Implemented using latest GaN power semiconductor technology, Zero Voltage Switching (ZVS) throughout the AC period and a variable switching frequency in the range of 200 kHz – 1 MHz in order to shrink the size of filter passives, the LB 1.0 was ranked among the top 10 out of 100+ teams actively participating in the GLBC. The LB 2.0 is the result of further research and considers lessons learned from the GLBC and achieves despite moderate 140 kHz constant frequency PWM and hard-switching around the peak of the AC output current a higher power-density ρ and a higher efficiency η. For both implemented prototypes experimental results are provided to confirm that all GLBC technical requirements are met. The experimental results include steady-state and step-response waveforms, EMI and ground current measurements, as well as efficiency and operating temperature measurements. The reason for the $\eta\rho$-performance improvement of LB 2.0 over LB 1.0 are then discussed in detail. Furthermore, the solutions of other GLBC finalists are described and then compared to the performance achieved with the hardware prototypes presented in this paper. This leads to findings of general importance and provides key guidelines for the future development of ultra-compact power electronic converters.

4.1 Introduction

In Chapter 2, the key design challenges and the technical concepts adopted in this dissertation to implement an ultra-compact single-phase inverter and overcome the Google Little Box Challenge (GLBC, [2]) were described in detail and are briefly summarized in the following. In order to drastically shrink the size of the converter bridge-legs and EMI filter passives and break through the status quo in power-density, GaN wide bandgap (WBG) semiconductor technology was selected to enable a high switching frequency in the range of 100 kHz-1 MHz [6]. By means of the widely accepted Triangular Current Mode (TCM) control technique [19, 20], Zero Voltage Switching of a bridge-leg can be achieved in every operating point throughout the AC period which results in low switching losses despite the high switching frequencies but requires a Zero Crossing Detection (ZCD) circuitry and sophisticated FPGA control for a robust implementation. In contrast to TCM control, conventional PWM features a constant switching frequency but suffers from high turn-on switching losses which limits the maximal feasible switching frequency. However, this drawback is mitigated by the fact that with a relatively large current ripple, i.e. a design with small filter inductance value, also for PWM the average switching losses can be considerably reduced and a switching frequency of up to a few hundreds of kHz is feasible. As GaN semiconductor technology enables both soft- and hard-switching in a totem-pole bridge-leg configuration (as opposed to Si MOSFETs), both bridge-leg control strategies were considered for the implementation of the Google Little Box inverter. Furthermore, a 2-level implementation of the bridge-legs was selected over a multilevel implementation in this dissertation because of the anticipated increase in volume introduced by the higher semiconductor count, the increased gate driving requirement (supply voltage and gate signal isolation), and because of the more involved control system to facilitate capacitor balancing under all operating conditions. In order to reduce the size of the energy storage required to cope with the 120 Hz power pulsation intrinsic to single-phase DC/AC converter system, the advantage of replacing bulky electrolytic DC-link capacitors with an additional auxiliary converter and well utilized buffer capacitor was emphasized in Section 2.3 and Chapter 3. Among several concepts presented in literature, the buck-type Parallel Current Injector (PCI) buffer as depicted in Fig. 4.1(a) & (b) (cf. Fig. 4.3 and Fig. 4.12) [37–40], was selected to cope with the pulsating AC power since (i) it features excellent capacitor utilization and (ii) allows to employ the same bridge-leg design as used in the main inverter to achieve maximal performance with minimal increase of overall complexity.

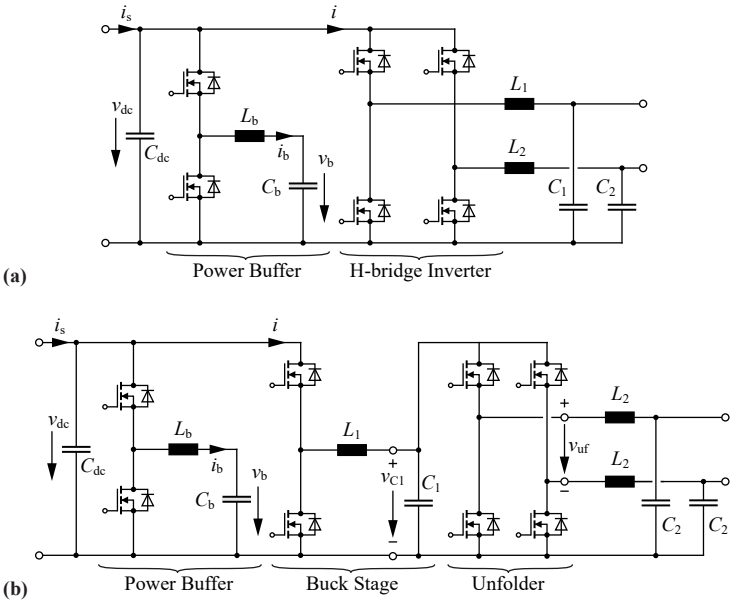


Fig. 4.1: (a) H-bridge inverter with DC-link referenced output filter and buck-type Parallel Current Injector (PCI) active power buffer (Little Box 1.0). (b) DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter with PCI active power buffer (Little Box 2.0).

As a consequence of the large feasible buffer voltage ripple, comparably small capacitance values in the range of 100 µF – 200 µF are needed, thus realizing the buffer capacitor with ceramic capacitor technology becomes a viable option. Since the effective energy density of electrolytic capacitors is reduced due to lifetime related current stress constraints, 2.2 µF/450 V class II X6S MLCC and 2 µF/500 V CeraLink capacitors were identified to be the most promising candidates for realizing an ultra-compact power buffer and are adopted for the implementation of the buffer capacitor [52–54]. Regarding the specified ground current requirements of 50 mA (revised from initially specified 5 mA), the difference between a 1 or 2 HF bridge-leg inverter design regarding the generation of a Low-Frequency (LF) Common-Mode (CM) output voltage component was analyzed and the merits of a DC-link referenced filter structure which allows a combined DM and CM filtering in a single stage was highlighted in Section 2.4.2. Concerning the EMI requirements of the GLBC, the concept of 4D-interleaving [21] was introduced which allows to operate the interleaved bridge-legs with an optimal overlapping interval (with respect to the AC period) for maximal conversion efficiency while meeting the EMI requirements. Furthermore, to dissipate the generated power losses during operation of the inverter, a parallel-fin type heat sink with both ultra-flat blowers and conventional fans was considered in this dissertation for the optimal implementation of the forced-air cooling systems. It was identified that a heat sink using blowers performs best for comparably long cooling units offering a large baseplate area for direct component attachment. Because of the flat dimensions of the blower, a sandwich-like arrangement with two heat sinks at the top and bottom and the converter in the center is possible (cf. Fig. 4.4). A heat sink design using fans performs best when the total length of the cooling unit is comparably short. Thus, this configuration is well suited for a component arrangement where only the power transistors are attached to the heat sink and the filter passives are cooled by the air flow exiting the heat sink (cf. Fig. 4.13).

Based on these key design considerations, two inverter concepts, (i) the H-bridge inverter with DC-link referenced output filter as shown in Fig. 4.1(a) (denominated as Little Box 1.0, LB 1.0, in the following) and (ii) the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter topology as shown in Fig. 4.1(b) (denominated as Little Box 2.0, LB 2.0, in the following), both equipped with a buck-type PCI buffer to cope with the pulsating AC power, were selected for further analysis and a comparative evaluation. The results of a comprehensive multi-objective $\eta\rho$-Pareto optimization described in Section 2.7.1 indicate that, despite of higher switching losses, operation with

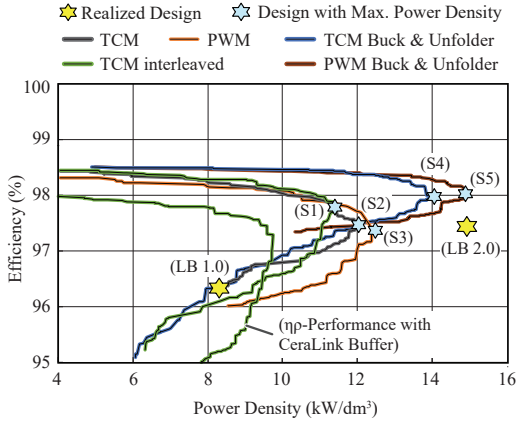


Fig. 4.2: Computed $\eta\rho$-performance of selected inverter concepts including the active power buffer for different operating modes (TCM/PWM) and with/without interleaving of bridge-legs. Also indicated is the actual performance achieved with the implemented hardware prototypes as presented in this chapter.

constant switching frequency just below 150 kHz PWM achieves a higher power-density compared to TCM control. This is explained by the fact that, for the given GLBC specifications and the performance of the employed GaN semiconductor technology, the loss savings of operating with Zero Voltage Switching (ZVS) throughout the AC period are less compared to the added conduction losses caused by the high RMS current and remaining ZVS switching losses resulting from the TCM control. Furthermore, it is shown that with the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter operated with PWM and a comparably large current ripple (small buck-stage filter inductance value) a power-density of 14.7 kW/dm^3 (240 W/in^3) with an efficiency of up to 98 % at 2 kW output power is possible. Compared to the H-bridge inverter concept, this inverter therefore features a $\approx$ 15 % – 20 % higher power-density and a 1.7 % higher efficiency at 2 kW rated power.

In this chapter, the claimed $\eta\rho$-performance of the considered inverter concepts is confronted with the actually achieved performance figures of realized hardware prototypes (cf. LB 1.0 and LB 2.0 in Fig. 4.2). In Section 4.2, the hardware prototype and results of experimental measurements on the LB 1.0, i.e. a 2-level H-bridge based inverter topology with interleaved bridge-legs, TCM operation with variable switching frequency in the range

of 250 kHz – 1000 kHz, and a buck-type PCI buffer employing CeraLink capacitor technology, are presented. The LB 1.0 was presented at the GLBC finals and, with a power-density of 8.18 kW/dm^3 (134 W/in^3) and a nominal efficiency of 96.4 %, was ranked among the top 10 out of 100+ contestants. In Section 4.3, the hardware prototype and results of experimental measurements on the LB 2.0, i.e. a DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter which considers all findings and lessons learned from the GLBC, are presented. Compared to the LB 1.0 presented at the GLBC finals, a further volume reduction of 40 % is achieved while at the same time the power losses are reduced by almost 25 %. Subsequently, in Section 4.4 the main reasons for the performance improvement of the LB 2.0 over the LB 1.0 are discussed in detail. Afterwards, the solutions of other GLBC finalist are briefly described and the claimed efficiency and power-density is compared to the experimentally verified $\eta\rho$-performance of the inverter concept selected in this dissertation. Finally, Section 4.5 concludes this chapter and summarizes important findings which are providing key guidelines for the future power-density improvements of industrial ultra-compact converter systems.

4.2 Little Box 1.0 Demonstrator

As mentioned in the introduction of this chapter, a 2-level H-bridge topology was selected because ideally no low-frequency (LF) Common Mode (CM) voltage is generated at the output and thus the specified ground current limit can be met without the need for bulky CM chokes. As depicted in Fig. 4.3, each of the two output phases is implemented by means of two interleaved 2-level totem-pole bridge-legs and, to further reduce the size of the EMI filter, a DC-link referenced bridge-leg filter configuration is employed which facilitates a combined DM and CM filtering in a single stage. Furthermore, a buck-type PCI power buffer is employed to compensate the fluctuating AC power and mitigate the DC-side voltage and current ripple to meet the specified requirements. In contrast to passive DC-link buffering with electrolytic capacitors, the power buffer capacitor C_b can be cycled to a significant extent (large voltage ripple) and thus a much smaller capacitance value is required which translates into a reduced volume of the energy storage even though additional semiconductors, an additional filter inductor L_b, and auxiliary circuits are needed. In Fig. 4.4, a photograph of the built LB 1.0 hardware prototype with a nominal efficiency of 96.4 % and an overall volume of 240 cm^3 resulting in a power-density of 8.18 kW/dm^3 (134 W/in^3) is shown. In the

following, details of the implementation will be described along with the presentation of experimental results.

4.2.1 Bridge-Leg Implementation

For the implementation of the bridge-legs of the system, 600 V/70 mΩ normally-off Gallium Nitride (GaN) Gate Injection Transistors (CoolGaN, samples from Infineon, [97]) are used in combination with a novel high-performance gate drive circuit [6, 7]. In order to reduce reverse conduction losses of the GaN transistors during the dead times, 600 V SiC Schottky diodes from Wolfspeed are mounted in parallel to the power transistors. Each of the bridge-legs is operated with a TCM modulation scheme that enables zero voltage switching (ZVS) transitions in all operating points throughout an AC period [19, 20]. Since ZVS results in lower switching losses, the selected high (variable) switching frequency in the range of 200 kHz – 1 MHz results in a small volume of the passive components, e.g. of the power stage filter inductors L_{1A}-L_{2B}. Furthermore, the high switching frequency in combination with the interleaving of two bridge-legs per output phase decreases the current ripple in the bridge-leg filter capacitors $C_{1/2}$ and doubles the effective switching frequency. Thus a higher cut-off frequency of the output filter is possible which in turn results in a reduced overall volume.

However, a high switching frequency also demands for suitable core materials and sophisticated inductor design in order to keep the high-frequency core and winding losses to a minimum. Addressing these challenges, the four output inductors of the inverter are realized based on a novel type of multiple-gap multiple parallel foil winding inductor [30, 98–100]. Since the multiple small air gaps are evenly distributed over the full length of the inner core limb, the H-field in the winding window shows a quasi 1D distribution running in parallel to the inner limb. Consequently, a foil winding enabling a high filling factor can be used, since the H-field is aligned with the foil winding and thus ideally no eddy currents are induced. In order to counteract the skin effect at these high frequencies, the foil winding is realized with four parallel 20 µm thin copper foils which are mutually isolated with a 7 µm thin layer of Kapton. Furthermore, a sophisticated winding arrangement is used, which forces the current to flow evenly distributed in all four parallel copper layers, thus counteracting the proximity effect [30, 98]. The four output inductors of the inverter are realized based on this approach, where DMR51 MnZn Ferrite form DMEGC is used as high frequency core material. The inner limb of each output inductor has 24 air gaps surrounded by the four parallel copper foils

with totally 16 turns, which gives an inductance value of around 10 µH. The inductor $L_b = 20\,\mu H$ of the power pulsation buffer was realized by connecting two 10 µH multi-gap inductors in series. Unfortunately, as analyzed in detail in Chapter 6, the mechanical manufacturing and assembly of the thin ferrite plates resulted in excessive core losses in the inner limb which resulted in a relatively low quality factor of the implemented multi-gap inductors.

The capacitor of the PCI power buffer, C_b, with an effective large-signal equivalent capacitance of 150 µF, was realized by means of 108 individual 2 µF/500 V CeraLink capacitors. By courtesy of EPCOS/TDK, a custom package with 18 capacitor chips mounted together on silver coated copper lead frames was available which drastically simplified the construction of the buffer capacitor. A summary of the employed power electronic components is provided in Tab. 4.1.

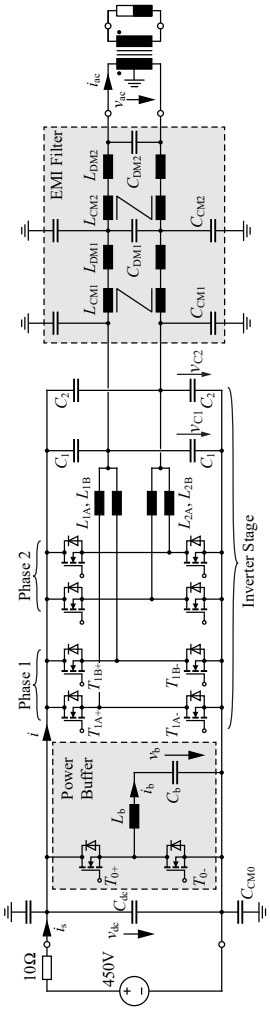


Fig. 4.3: Topology of the inverter denominated as Little Box 1.0 (LB 1.0) realized according to the Google Little Box Challenge (GLBC) technical specifications (cf. Tab. 1.1 in Section 1.1) with the original 5 mA ground current limit. The systems consists of a H-bridge inverter with two interleaved bridge-legs per phase and a subsequent EMI output filter. The DC-side energy storage to compensate the fluctuating AC power is realized with a buck-type Parallel Current Injector (PCI) active power buffer.

Fig. 4.4: Photograph of the realized LB 1.0 hardware (without housing) presented by the team from ETH Zurich, FH-IZM, and Fraza company, at the finals of the Google Little Box Challenge (8.8 cm × 8.9 cm × 3 cm, 3.46 in × 3.5 in × 1.18 in).

Tab. 4.1: Technical Details of the Implemented Little Box 1.0 Hardware Prototype

	Feature	Parameter/Value	Description	Part Number
Power Devices	T_{0+}, T_{0-}	600 V / 70 mΩ GaN HEMT/GIT, 600 V / 1.7 A SiC diode	Infineon CoolGaN, Wolfspeed Schottky diode, 1 transistor per switch in schematic, 1 diode in parallel per GaN HEMT, add. 600 pF C0G MLCC in parallel	IGLD60R070D1, C3D1P7060Q
	T_{1A+}, T_{1A-}, T_{1B+}, . . . T_{2B-}	600 V / 70 mΩ GaN HEMT/GIT, 600 V / 1.7 A SiC diode	Infineon CoolGaN, Wolfspeed Schottky diodes, 2 transistors in parallel per switch in schematic, 1 diode in parallel per GaN HEMT, add. 600 pF C0G MLCC in parallel	IGLD60R070D1, C3D1P7060Q
	Modulation	TCM	Soft-switching throughout mains period with constant 5 A reverse polarity switching current	
	f_s	250 kHz – 1000 kHz	Variable switching frequency of inverter and power buffer bridge-legs	
Power Stage Filter	$L_{1,A}$, $L_{1,B}$, $L_{2,A}$, $L_{2,B}$	10.5 µH	Multi-gap inductor with foil winding; DMR 51 MnZn ferrite with 24 × 80 µm gaps in the center limb realized by stacking 0.61 mm thick ferrite plates; for more details see [31]	
	L_b	2 × 10.5 µH	Two multi-gap inductor connected in series	
	C_{dc}	6 × 2 µF	650 V CeraLink from EPCOS/TDK, customized version with lower voltage rating but higher capacitance per chip	
	C_b	108 × 2 µF	650 V CeraLink from EPCOS/TDK, 18 individual chips mounted on lead frame	
	C_1, C_2	4 × 2.2 µF	450 V class II/X6S MLCC from EPCOS/TDK	C5750X6S2W225K250KA
EMI Filter	L_{DM1}, L_{DM2}	10 µH	Coilcraft XAL1010, 15.5 A	XAL1010-103MED
	L_{CM1}, L_{CM2}	1.2 mH	VAC Vitroperm 500F toroid core (L2012-W498), 5 turns with ⌀1 mm enameled copper wire	T60006-L2012-W498
	C_{CM0}, C_{CM1}, C_{CM2}	1 × 100 nF	630 V/X7R MLCC from TDK	C3225X7T2J104K160AC
	C_{DM1}, C_{DM2}	3 × 2.2 µF	450 V class II/X6S MLCC from TDK	C5750X6S2W225K250KA
Cooling System	l	10 mm	Length of the fins	
	t	0.2 mm	Width of the fins	
	u	3 mm	Height of the fins	
	s	0.5 mm	Space between individual fins	
	b	1.5 mm	Thickness of the baseplate	
	Fan Type	Blower	Sunon 5 V DC Micro Blower, 30 × 30 × 3 mm	UB5U3-700
	CSPI	37 W/(K dm^3)	Cooling performance of dual sided cooling system with 2 × 6 micro blowers; without heat distribution elements inside converter	

4.2.2 Digital Control

For the generation of the AC output voltage v_{ac}, the two phase voltages are actively controlled to values symmetric around half of the DC-link voltage, i.e. $v_{C1} = 1/2(v_{ac} + v_{dc})$ and $v_{C2} = 1/2(-v_{ac} + v_{dc})$ (cf. Fig. 4.3). Since the sum of these phase voltages is constant, no LF CM output voltage is generated and hence LF ground currents are suppressed. The overall structure of the employed control system is shown in Fig. 4.5 and is composed of two subsystems dedicated to control the active power buffer and the inverter, respectively. To achieve a low THD and good transient performance, a cascaded voltage and current control feedback loop with Proportional-Resonant (PR) compensators [92] tuned at 60 Hz is used to regulate the AC output voltage. This control loop uses the AC quantities measured in the first EMI filter stage which is represented in a simplified manner by components L_3 and C_3 as shown in Fig. 4.5. Based on the output of the AC voltage control loop,

$$v^*_{C1-2} = \bar{v}_{L3} + v_{ac}, \tag{4.1}$$

wherein $\bar{v}_{L3}$ is the local average of the inductor voltage v_{L3}, the reference value for the capacitor voltage of the two bridge-legs,

$$v^*_{C1} = 1/2(v^*_{C1-2} + v_{dc}), \tag{4.2}$$
$$v^*_{C2} = 1/2(-v^*_{C1-2} + v_{dc}), \tag{4.3}$$

is derived. As can be seen, PI-compensators are used to control the voltages at C_1 and C_2. The reference current for L_1 and L_2 is then obtained by adding or subtracting the feed-forward term i_{L3} to the output of the PI-compensators, respectively. Based on the measurements of the DC-link voltage v_{dc} and the bridge-leg output voltages v_{C1} and v_{C2}, circuit parameters such as the inductance value and the transistor output capacitances (C_{oss}), a predictive current control algorithm calculates the turn-on, turn-off and dead time interval of each bridge-leg such that the resulting inductor current features the characteristic triangular shape to achieve ZVS at both turn-on and turn-off of the bridge-leg while ensuring the correct average value $i^*_{L1/2}$. To achieve a complete resonant transition at every switching instant throughout the AC period for a defined maximum dead time interval and limits imposed by the range of the variable switching frequency, a minimum constant reverse current of 5.0 A is used. The information of the inductor current Zero-Crossing (ZC) is used to update the remaining turn-on and turn-off interval to cope with measurement and parameter inaccuracies. To implement the digital control

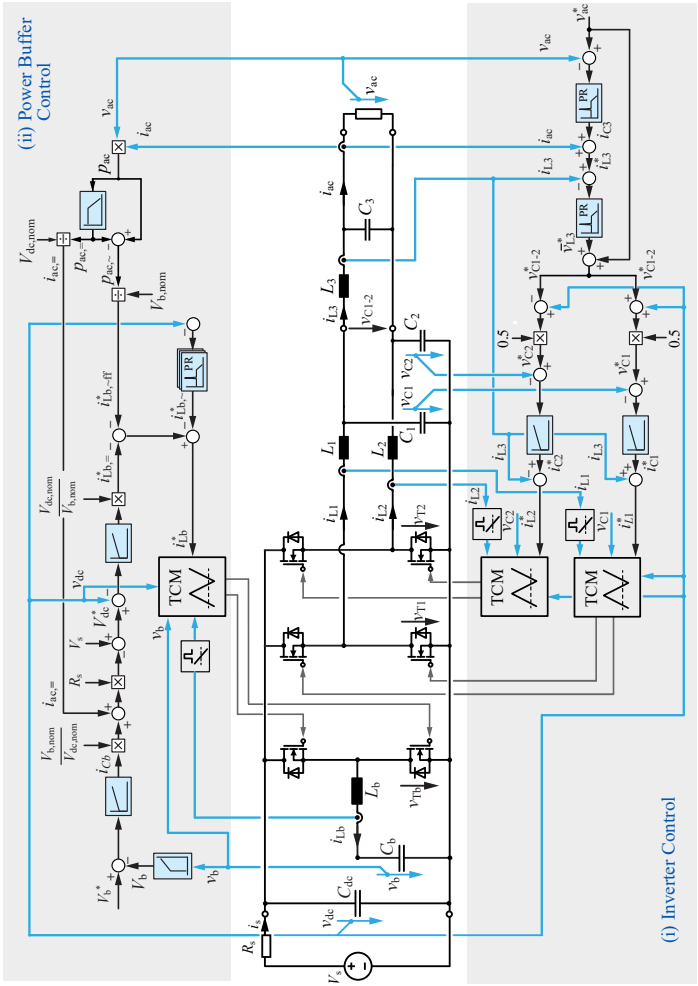


Fig. 4.5: Implemented digital control system of the Little Box 1.0 (LB 1.0). The inverter control structure is located below and the power buffer control structure is located above the power circuit diagram of the converter. For the sake of simplicity, the interleaved bridge-legs and the EMI filter are not included in the circuit diagram. The AC output voltage is controlled in the first DM filter stage which is represented by the components L_3 and C_3.

structure in hardware, a combination of a TI C2000 Delfino real-time microcontroller (TMS320F28335ZJZS) and a Lattice FPGA (LFXP2-5E-5MN132I) is used. The analog signal measurements, the feedback control system as depicted in Fig. 4.5, and the computation of the TCM timing intervals are implemented on the microcontroller and are executed with the fastest possible rate of 20 kHz. The timing intervals from the microcontroller and the current ZC signals are forwarded to the FPGA where the TCM modulator with a resolution of 5 ns (200 MHz) is implemented. Thus, for the given switching frequency range of 200 kHz – 1 MHz, the TCM timing variables from the microcontroller are updated only every $\approx 10 - 50$ switching cycles which justifies the twice per cycle occurring ZC feedback and adjustment of timing intervals. The TCM modulator also features the synchronization capability for the correct interleaving of the two bridge-legs for each output phase (cf. Fig. 4.3) in order to ensure the desired cancellation of the first switching frequency harmonic in the current. The commands to activate and deactivate the individual bridge-legs depending on the position within the AC period and actual output power level (4D-interleaving, as described in Section 2.4.3 are determined on the microcontroller and are then forwarded to the FPGA.

The selected magnetic saturation based Zero Crossing Detection (ZCD, cf. Fig. 2.5, [101]) is implemented by means of a small toroidal core with an outer diameter of 4 mm (R4 × 2.4 mm × 1.6 mm, B64290P0036X830 from EPCOS). The selected core material is N30 which features a low saturation flux density and high permeability over a wide frequency range. The number of turns of the secondary (measurement) winding is set to $N_s = 10$. Depending on the inductor current slope ($\mathrm{d}i_L/\mathrm{d}t$), with this number of turns the induced voltage reaches values from 20 V up to 160 V, which makes the ZCD circuit robust against electric disturbances. However, with the variability of the induced voltage also the time delay of the detection of the current zero crossings slightly changes. The induced voltage is tracked with a fast comparator circuit (TLV3501, 4.5 ns propagation delay) in order to keep the signal delay short and is then digitally filtered in the FPGA.

The control system of the buck-type PCI power buffer is also depicted in Fig. 4.5. The main objective of the power buffer control system is to exactly compensate the pulsating power caused by the single-phase AC load, such that only a constant power $P_s = V_s \cdot i_s$ is drawn from the DC source. The interested reader is referred to Section 3.2.3 for a detailed description of the power buffer control system.

4.2.3 Experimental Waveforms

Fig. 4.6 shows the measured characteristic waveforms of the LB 1.0 prototype at steady-state and rated output power. Considering v_{dc} (yellow trace) in Fig. 4.6(a), it can be seen that the PCI power buffer effectively compensates the fluctuating AC power and successfully mitigates the 120 Hz voltage ripple. The resulting voltage swing present in the buffer capacitor voltage v_b, amounts to 110 V and is superimposed to the bias or offset voltage $V_b = 300$ V. The characteristic TCM shape of the PCI buffer inductor current is also shown in Fig. 4.6(a). Fig. 4.6(b) displays the sinusoidal AC output current and the current in the inductor $L_{1,A}$ and $L_{1,B}$ of the two interleaved bridge-legs of output phase 1. Clearly visible is the outcome of the implemented 4D-interleaving, where both bridge-legs are only operated simultaneously at high instantaneous output power, i.e. around the peak value of i_{ac} in case of ohmic loads. The total overlap duration of the interleaved bridge-legs as shown in Fig. 4.6(b) amounts to 158°. The actual overlap duration in every operating point was determined empirically with the objective to increase the overall conversion efficiency while complying with the specified EMI regulations. Fig. 4.7 shows the measured waveforms of the LB 1.0 converter during a transient caused by a stepwise increase in output power. Fig. 4.7(a) shows the AC output waveforms during a load step from 230 W to 700 W. It can be seen that the transient is settled in less than 50 ms which clearly complies with the specified settling time of 1 s for a maximum specified load step of 500 W. Fig. 4.7(b) shows the PCI buffer and DC-side related waveforms for a load step from 0 W to 700 W. Triggered by the step, the average buffer capacitor voltage drops 50 V below the 300 V at steady-state. Simultaneously, the PCI buffer controller starts to compensate the power pulsation by means of injecting an appropriate current into the DC-link. As a consequence, a distinct 120 Hz voltage ripple develops at the buffer capacitor immediately after the load step. After a transient time of 60 ms, the average buffer capacitor voltage has recovered and the fluctuating AC power is completely compensated by the active power buffer. Take note that the PCI is achieving a smooth transition of the DC-link voltage level which settles at a lower value after the transient due to the inserted 10 Ω resistor R_s between the 450 V DC source and the DC-link (cf. Fig. 4.3). The reactive power drawn by the EMI filter (DM capacitors) of the inverter stage is compensated by the power buffer, thus a small ripple is present in the buffer capacitor voltage prior to the load step although no load is connected to the inverter.

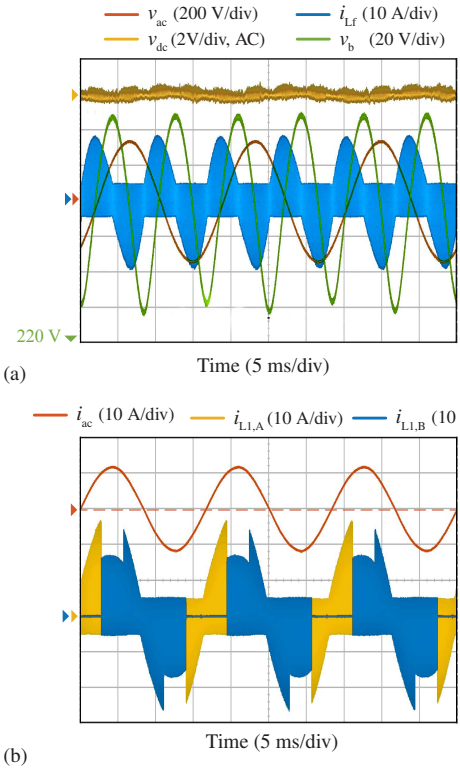


Fig. 4.6: Measured steady-state waveforms of the Little Box 1.0 (LB 1.0) prototype operated at the rated 2 kW output power. (a) The active power buffer eliminates the 120 Hz voltage ripple of the DC-link voltage v_{dc}. The buffer voltage swing at rated power is designed to be around 110 V. (b) Filtered output current and corresponding high-frequency Triangular Current Mode (TCM) modulated current $i_{L1,A}$ and $i_{L1,B}$ in the power stage inductors $L_{1,A}$, $L_{1,B}$ with 4D-interleaving (cf. Section 2.4.3). The measurements were performed at unity power factor ($\cos\phi_0 = 1$) but the waveforms depicted in (a) and (b) were not captured simultaneously which explains the phase-shift between v_{ac} and i_{ac}.

4.2.4 EMI Compliance

In order to achieve a high filter attenuation while still keeping the filter components small, for the given circuit structure and selected frequency

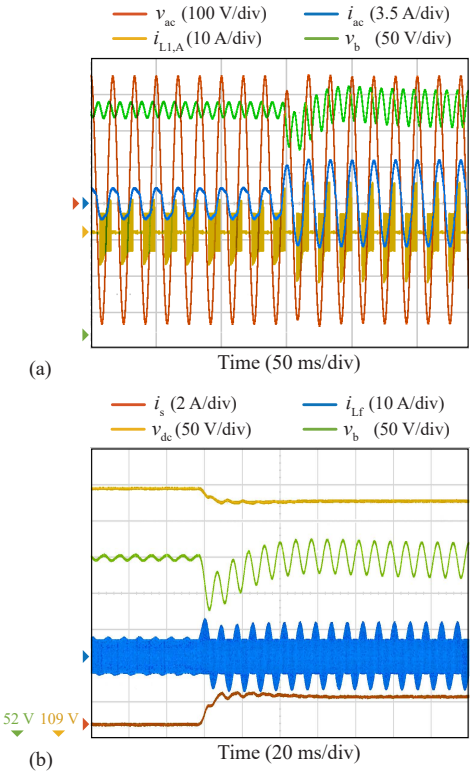


Fig. 4.7: Transient waveforms of the Little Box 1.0 (LB 1.0) subject to a stepwise increase in output power. (a) Measured AC output waveforms v_{ac} and i_{ac}, and filter inductor current $i_{L1,A}$ subject to a stepwise load increase from 230 W to 700 W. (b) Measured DC-side and power buffer waveforms subject to a stepwise load increase from 0 W to 700 W. The small ripple present in the buffer capacitor voltage prior to the load step despite 0 W of output power is due to the reactive power drawn by the EMI filter (DM capacitors). Note that the waveforms depicted in (a) and (b) were not captured simultaneously and exhibit a different time scale.

range a two-stage EMI output filter topology is employed as shown in Fig. 4.3. As can be noticed, although with the H-bridge topology ideally no LF CM voltage is generated at the inverter output, the CM inductors L_{CM1} and L_{CM2} as well as the CM capacitors C_{CM1} and C_{CM2} are still needed to filter the remaining HF CM components. Note, that the bridge-legs of output phases

1 and 2 cannot be synchronized because of the TCM control and thus the CM noise elimination known from the H-bridge topology with bipolar PWM does not apply. In the given filter configuration, the output capacitors C_1 and C_2 not only help to attenuate the Differential Mode (DM) noise but also the CM noise, which means that if C_1 and C_2 are increased, the needed CM inductance can be decreased. Furthermore, since $C_{1/2}$ are either connected to the positive or negative DC-rail and thus no ground currents are generated, $C_{1/2}$ can be designed in the µF-range which is much larger than the CM capacitor values of C_{CM1} and C_{CM2} which are more in the tens of nF-range. The only limiting factor for the capacitance of C_1, and also for the other DM capacitors C_{DM1} and C_{DM2}, is the additional reactive power demand that causes larger currents and higher losses in the whole system. For the built prototype each C_1 is realized with four parallel and C_{DM1} and C_{DM2} with three parallel 2.2 µF, 450 V class II/X6S Multi-Layer Ceramic Capacitors (MLCC, C5750X6S2W225M250KA from EPCOS/TDK), since ceramic capacitors feature a much higher capacitance per unit volume than the conventionally used film capacitors. On the contrary, the dielectric material of the class II/X6S MLCCs exhibits substantial power loss when excited with a large-voltage swing at low frequencies (cf. Section 2.3.1 and Appendix B). Based on experimental measurements, the dissipated power per volume of the class II/X6S dielectric material is in the order of 4.7 W/cm^3 for an AC excitation with $2\times\sqrt{2}\times240$ V = 678.8 V peak-to-peak voltage at 60 Hz excitation frequency. Considering the voltage- and temperature-dependent capacitance of the selected components, the effective capacitance drops to approximately 650 nF per piece which results in an additional reactive output filter power of around 200 VAr. The CM inductors L_{CM1} and L_{CM2} are built with toroidal cores from Vacuumschmelze which are based on the core material VITROPERM 500F that offers a high permeability and high saturation flux density (core type: T60006-L2012-W498, winding: 11 turns, 1 mm-Ø). Even if the leakage inductance of the CM inductors contributes to the DM inductances, separate DM inductors, L_{DM1} and L_{DM2} are added to achieve the required DM attenuation. For all DM inductors the commercially available 10 µH-inductors from Coilcraft (XAL1010-103MED) are used. The CM capacitors C_{CM0}, C_{CM1} and C_{CM2} are implemented with 3×100 nF, 630 V/X7R MLCCs from TDK (C3225X7T2J104K160AC).

The quasi-peak EMI spectrum of the LB 1.0 hardware prototype with aluminium enclosure at 2 kW output power is depicted in Fig. 4.8(a). The results where obtained with the R&S ESPI7 test receiver and the R&S ENV216 single-phase LISN which was installed between the AC output of the converter and the resistive load bank. It can be clearly seen that the FCC Part 15 B

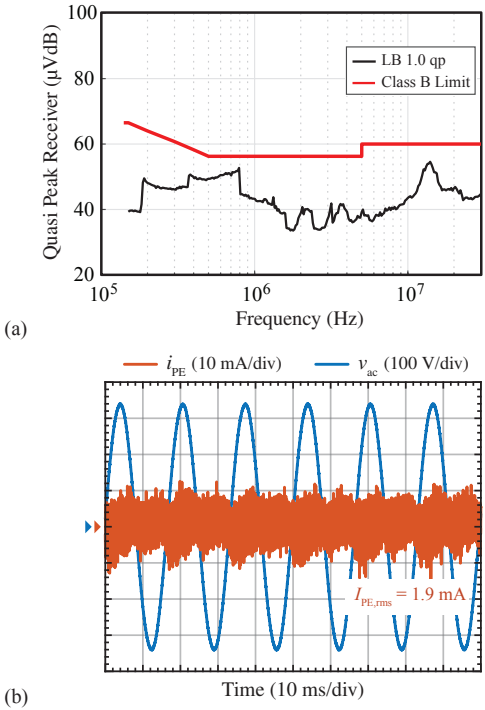


Fig. 4.8: (a) EMI noise spectrum of Little Box 1.0 (LB 1.0) at 2 kW output power measured with R&S ENV216 single-phase LISN and R&S ESPI7 test receiver. (b) Ground current of the LB 1.0 measured by means of inserting both AC output wires simultaneously into the clamp of a current probe (Teledyne CP030).

conducted EMI limits are met. Due to the implemented TCM control with resulting variable switching frequency, the noise spectrum does not exhibit distinct peaks but instead is spread out over a wide frequency range.

In a preceding calibration test, the DC output terminals of the employed laboratory voltage source were connected directly to the resistive load bank. In a characteristic operating point, that is 450 V DC and 5 A, around 7.4 mA of ground current was measured by means of inserting both wires in the clamp of a Teledyne CP030 current probe. If the chassis of the supply was, in addition to the always persistent ground connection through the AC supply cable, also connected directly to the local ground/PE terminals of the EMI

test setup, approximately 30 mA of ground current were detected. For this reason, a CM choke of ≈ 2 mH @ 10 kHz of nominal inductance, implemented with 5 turns around a toroidal VITROPERM 500F core (T60006-L2045-V102), was inserted between the DC supply (Sorensen SGI 600/17) and the converter input. Keep note that because of the low-impedance path provided by the CM capacitor C_{CM0} at the input of the converter (cf. Fig. 4.3), a fair assessment of the ground current caused by the device under test is still possible.

The recorded ground current in the nominal operating point is depicted in Fig. 4.8(b) and was measured by inserting both AC output wires simultaneously into the clamp of the current probe (Teledyne CP030). The ground wire of the converter was connected to the local ground/PE terminal of the EMI test setup. The RMS value of the ground current amounts to only 1.9 mA and confirms the effectiveness of the designed CM filter and the symmetrical H-bridge inverter topology. It should be emphasized, that the LB 1.0 converter therefore complies to the original more stringent 5 mA ground current limit of the GLBC which was later relaxed to 50 mA (cf. Section 1.1).

4.2.5 Efficiency

The measured efficiency of the LB 1.0 prototype as a function of output power is depicted in Fig. 4.9. As indicated by the blue line with circle markers, the efficiency of the system with active power buffer exhibits a peak efficiency of 96.3 % at rated output power. The corresponding CEC weighted efficiency amounts to 95.07 %, meeting the minimum efficiency requirements (95 %) of the GLBC. The red line with cross markers represents the measured efficiency of only the inverter with passive DC-link buffering by means of high-density electrolytic capacitors ($3 \times 493\,\mu F/450\,V$, B43991-X0009-A223 from EPCOS/TDK). The peak efficiency amounts to 97.5 % and the resulting CEC efficiency amounts to 96.3 %. The substantial reduction in efficiency by the operation of the PCI can be ascribed to the additional HF bridge-leg with multi-gap filter inductor and CeraLink buffer capacitor. In fact, as will be further discussed in Section 4.4, roughly 60 % of the PCI power losses are caused by the CeraLink buffer capacitor.

4.2.6 Cooling and Operating Temperature

A dual-sided cooling arrangement (cf. Fig. 4.4) with ultra-flat custom-machined heat sink elements is used to extract the 74 W of power loss in the nominal operating point. The heat sink has a height of only 4.5 mm and employs 6 Sunon 5 V DC micro blowers ($30 \times 30 \times 3$ mm) per element. The

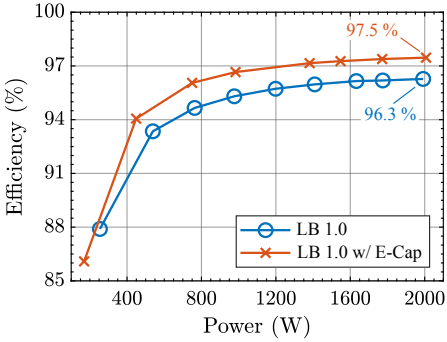


Fig. 4.9: Conversion efficiency of the Little Box 1.0 (LB 1.0) with respect to output power measured with a Yokogawa WT3000 precision power analyzer. The red curve with cross markers represents the measured efficiency of the inverter using passive DC-link buffering with electrolytic capacitors instead of the active power buffer.

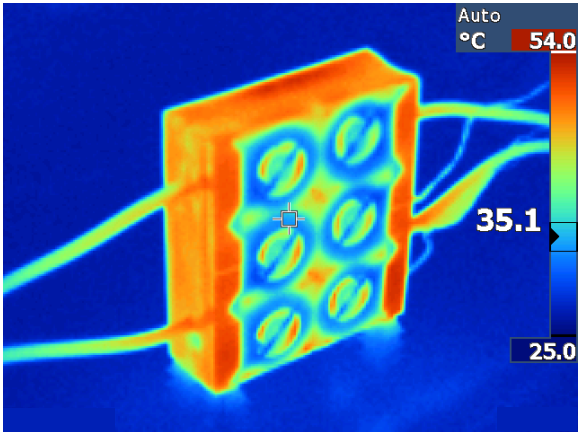


Fig. 4.10: Thermography image of the Little Box 1.0 (with housing) recorded with a FLUKE Ti10 infrared camera showing the steady-state temperature distribution at rated 2 kW output power.

effective cooling system performance index (CSPI) amounts to 25 W/(K dm^3) and also considers the heat distribution elements (thin copper pieces within the converter) needed to conduct the heat from the lossy components, e.g.

Tab. 4.2: Technical Details of the Auxiliary Supply.

Feature	Description	Part Number
S_{1+} / S_{1-}	600 V / 1.5 Ω Si-MOSFET	STL3NM60N
$D_1 \ldots D_4$	40 V / 2 A	PMEG4020EPASX
n_p	130 turns with ⌀0.15 mm solid wire	
n_s	8 turns with custom wire comprised of 4 strands with ø0.2 mm	
Core	EFD 12/6/3.5, 3F36 ferrite, 0.4 mm air gap	EFD12/6/3.5-3F36-S
Control IC	IRS27952, 465 kHz switching frequency	IRS27952STRPBF

the power inductors, to the baseplate of the respective heat sink. The thermography image in Fig. 4.10, recorded with a FLUKE Ti10 infrared camera, shows the steady-state temperature distribution of the LB 1.0 at 2 kW output power. As it can be clearly seen, the implemented cooling system is sufficient to meet the maximum allowed surface temperature requirement of 60 °C.

4.2.7 Auxiliary Power Supply

In order to supply the measurement and control electronics (≈ 2 W – 3 W), the gate drivers (≈ 3 W – 4 W), and the fans of the cooling system (≈ 2 W – 3 W) of the Little Box inverter, an auxiliary supply capable of providing around 10 W of power at low output voltage in the range of 12 V – 18 V is needed. Based on the specified test setup as described in Section 1.1, i.e. a 450 V DC source with a series resistor of 10 Ω, the actual DC-link voltage applied to the input varies in dependency of the power converter's input power and/or current. In idle operation of the converter, a maximum input voltage $v_{dc,max}$ of 450 V occurs and, accordingly, at rated output power of 2 kW (PF = 1) a minimum DC-link voltage of around 390 V is present (considering 95 % efficiency and the maximum allowed peak-to-peak DC-link voltage ripple of 3 %). Adding some margin, a input voltage range of 380 V – 450 V is considered in the design of the auxiliary supply. In order to attain a low volume and maintain a high efficiency, the ZVS half-bridge topology shown in Fig. 4.11(a) is adapted to implement the auxiliary supply. The half-bridge ZVS diode rectifier topology features low switching losses due to ZVS and can thus be operated with 600 V switches at very high switching frequencies. This in turn allows

minimizing the volume of the transformer being required. In order to enable soft-switching even under no-load (idle) conditions, a certain magnetizing current is needed to charge/discharge the parasitic capacitances. In addition, and in contrast to a e.g. flyback converter, a high-side switch is needed requiring an isolated gate driver. The implemented hardware prototype of the auxiliary supply is depicted in Fig. 4.11(b), showing also a match for size comparison. The power transformer is placed in a PCB cut out which allows attaining an overall converter height of only 4.5 mm. In conjunction with the needed PCB area of about 1.8 cm × 2.5 cm the total volume of the auxiliary supply is about $V_{\text{aux}} = 2\,\text{cm}^3$. Technical details of the used components are summarized in Tab. 4.2. Fig. 4.11(c) shows the output voltage of the implemented auxiliary supply with respect to the output power for different DC-link voltage levels. As can be seen, at 10 W maximum output power, the output voltage varies in the range of 13.8 V – 16.8 V for the specified input voltage range. Fig. 4.11(d) shows the measured efficiency as a function of output power at 400 V DC-link voltage. For output power levels above 4 W the efficiency of the supply exceeds 80 %, and at nominal output power of 10 W the efficiency is even above 87.5 %. With the possible extension of synchronous rectification, where the secondary side diodes are replaced with active MOSFETs (extended circuit not shown in Fig. 4.11(a)), the efficiency increases only marginally by about 1.14 % at maximal output power.

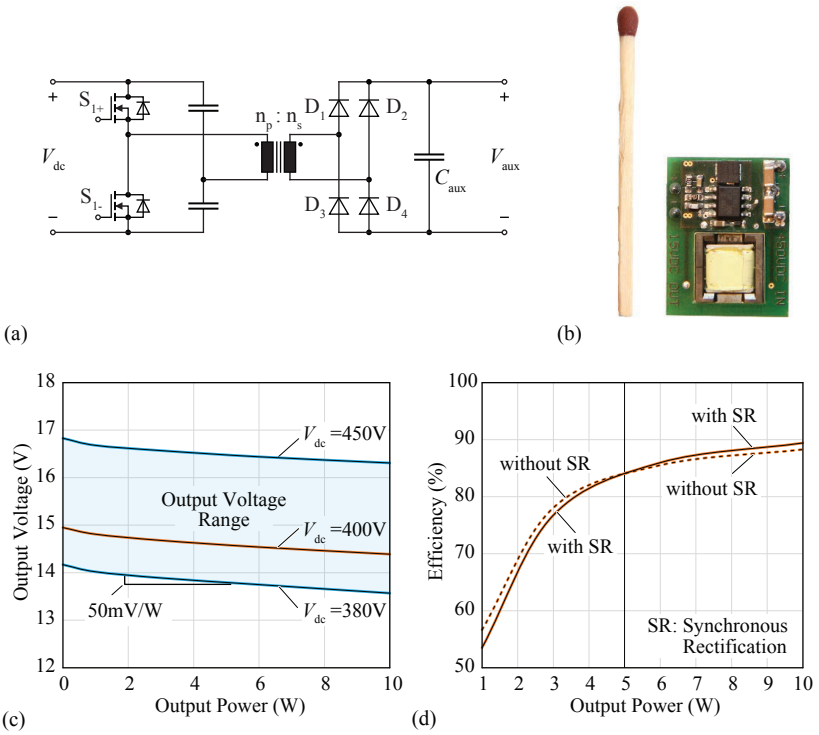


Fig. 4.11: Proposed auxiliary supply to power measurement and control electronics of the Little Box converter. (a) ZVS half-bridge topology with secondary side diode rectifier. (b) Picture of the implemented hardware prototype. (c) Auxiliary voltage range with respect to output power and the specified DC-link voltage range. (d) Efficiency with respect to output power of the implemented hardware prototype.

4.3 Little Box 2.0 Demonstrator

The inverter topology of the Little Box 2.0 (LB 2.0) as shown in Fig. 4.12 is based on a conventional DC/|AC| buck converter which generates a rectified sinusoidal voltage $v_{C1} = |\hat{V}_{ac} \cdot \sin(\omega t)|$ with respect to the negative DC-link rail and a subsequent |AC|/AC H-bridge unfolder which generates the actually desired sinusoidal output voltage v_{uf} [67]. Likewise to the LB 1.0 system, the DC-side energy storage to compensate the fluctuating AC power is realized with a buck-type PCI power buffer. Compared to the H-bridge topology of the LB 1.0 (cf. Fig. 4.3), the major advantage of this topology is that one half of the previously described inverter stage including bridge-leg filter inductors and capacitors can be completely omitted, thus volume and losses are saved and the system complexity is reduced. However, a higher ground current is to be expected since a LF CM voltage with a peak voltage equal to half the AC amplitude, i.e. $v_{CM} = \hat{V}_{ac}/2 \cdot \sin(\omega t)$, is generated at the output (cf. Fig. 2.11 in Chapter 2). The H-bridge unfolder was selected because, unlike the half-bridge unfolder (totem-pole inverter) as described in Section 2.4.2, high $\mathrm{d}v/\mathrm{d}t$ transitions in the LF CM voltage are prevented and it is furthermore possible to utilize the DC-link referenced filter configuration and therefore reduce the size of the EMI filter. In this regard, the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder concept became truly viable once the specified ground current limit was relaxed from 5 mA to 50 mA because of the expected volume reduction of the CM chokes due to the comparably high permissible total CM capacitance of $\approx \frac{50\,\mathrm{mA}}{2\pi 60\,\mathrm{Hz} \cdot 1/2 \cdot 240\,\mathrm{V}} = 1.1\,\mu\mathrm{F}$.

In Fig. 4.13, a picture of the built LB 2.0 hardware prototype with an overall boxed volume of 135 cm^3 (without housing) resulting in a remarkable power-density of 14.8 $\mathrm{kW/dm}^3$ (243 $\mathrm{W/in}^3$) and a nominal efficiency of 97.4 % is shown. In the following, details of the implementation will be described along with the presentation of experimental results. A summary of the employed power electronic components is provided in Tab. 4.3. The LB 2.0 hardware prototype employs the same auxiliary power supply as described previously in Section 4.2.7.

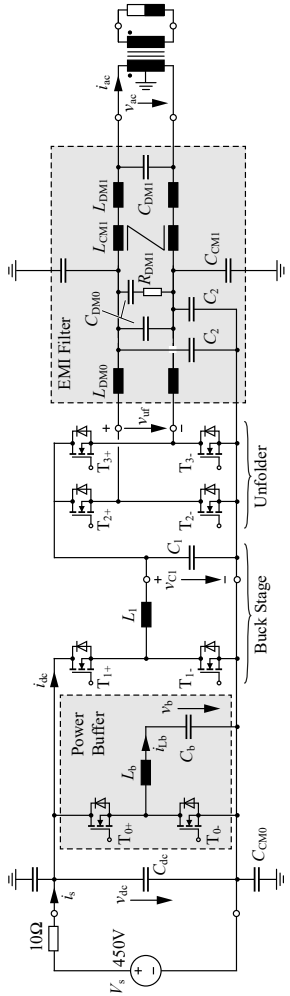


Fig. 4.12: Topology of the 2nd inverter realized according to the Google Little Box Challenge (GLBC) technical specifications with revised 50 mA earth current limit (Little Box 2.0, LB 2.0). The inverter is comprised of a DC/|AC| buck-stage with |AC|/AC H-bridge unfolder and a subsequent EMI output filter. The DC-side energy storage to compensate the fluctuating AC power is also implemented with a buck-type Parallel Current Injector (PCI) active power buffer.

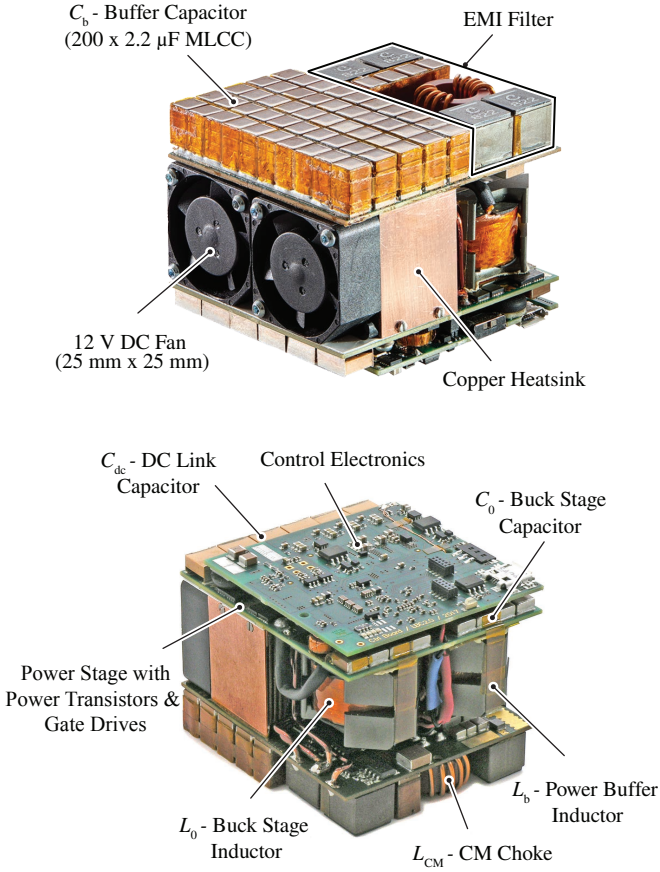


Fig. 4.13: Photograph of the realized Little Box 2.0 (LB 2.0) hardware (without housing) (5.9 cm × 5.0 cm × 4.5 cm, 2.32 in × 1.97 in × 1.77 in).

Tab. 4.3: Technical Details of the Implemented Little Box 2.0 Hardware Prototype

	Feature	Parameter/Value	Description	Part Number
Power Devices	T_{0+}, T_{0-}, T_{1+}, T_{1-}	600 V / 70 mΩ GaN HEMT/GIT, 600 V / 1.7 A SiC diode	Infineon CoolGaN, Wolfspeed Schottky diodes, 2 transistors in parallel per switch in schematic, 1 diode in parallel per GaN HEMT	IGLD60R070D1, C3D1P7060Q
	T_{2+}, T_{2-}, T_{3+}, T_{3-}	650 V / 25 mΩ GaN E-HEMT, 600 V / 1.7 A SiC diode	GaNSystems, Wolfspeed Schottky diodes, 2 transistors in parallel per switch in schematic, 1 diode in parallel per GaN transistor	GS66516T, C3D1P7060Q
	Modulation	PWM	Soft and hard-switching occurs within an AC period	
	f_s	140 kHz	Constant switching frequency	
Power Stage Filter	L_b	40 µH	N97, RM 10 MnZn ferrite core, 2 mm tot. gap length, 20 turns with 225 × 71 µm HF litz wire without silk insulation	B65813J0000R097
	L_1	45 µH	N97, RM 10 MnZn ferrite core, 6 mm tot. gap length, 30 turns with 180 × 71 µm HF litz wire without silk insulation	B65813J0000R097
	C_{dc}	6 × 2 µF	650 V CeraLink from EPCOS/TDK, customized version with lower voltage rating but higher capacitance per chip	
	C_b	200 × 2.2 µF	450 V X6S/MLCC from EPCOS/TDK	C5750X6S2W225K250KA
	C_1	8 × 2.2 µF	450 V class II/X6S MLCC from EPCOS/TDK	C5750X6S2W225K250KA
EMI Filter	L_{DM1}, L_{DM2}	8.2 µH	Coilcraft XAL1010, 17.1 A	XAL1010-822MED
	L_{CM1}	2.6 mH	VAC Vitroperm 500F toroid core (L2009-W914), 10 turns with Ø 1 mm enameled copper wire	T60006-L2009-W914
	C_{CM0}, C_{CM1}	3 × 100 nF	630 V X7R MLCC from TDK	C3225X7T2J104K160AC
	C_2, C_{DM1}	4 × 2.2 µF	450 V class II/X6S MLCC from TDK	C5750X6S2W225K250KA
	C_{DM2}	3 × 2.2 µF	450 V class II/X6S MLCC from TDK	C5750X6S2W225K250KA
	R_{DM1}	1.25 Ω	4 × 5 Ω chip resistor (SMD 0805) in parallel	
Cooling System	l	20 mm	Length of the fins	
	t	0.5 mm	Width of the fins	
	u	18 mm	Height of the fins	
	s	0.8 mm	Space between individual fins	
	b	4 mm	Thickness of the baseplate	
	Fan Type	Sunon 12 V DC fan	25 × 25 × 10 mm	MF25101V1-1000U-A99
		WTF 8.4 V DC fan	25 × 25 × 10 mm, 20 000 RPM @ 7.2 V	
	CSPI	53 W/(K dm^3)	Cooling performance with Sunon 12 V DC fan; theoretical value without considering air duct / heat distribution inside the converter	

4.3.1 Bridge-Leg Implementation

For the implementation of the PCI and inverter buck-stage bridge-legs, also 600 V/70 mΩ CoolGaN technology is used with two transistors in parallel per switch. In order to reduce losses during reverse conduction of the GaN transistors, 600 V SiC Schottky diodes are used. The inductor of the buck-stage converter, $L_1 = 45\,\mu H$ is implemented on a RM 10 core using the MnZn ferrite material N97 from TDK. The winding is realized with 30 turns of a $180 \times 71\,\mu m$ HF litz wire without additional silk insulation to achieve a higher copper filling factor. The limbs of the RM 10 core were shortened with a diamond wheel precision saw to achieve a total air gap length of 6 mm (3 mm per limb) while keeping the total height of the core unchanged. The inductor of the PCI, $L_b = 40\,\mu H$, is also implemented on a N97/RM 10 core. The winding is realized with 20 turns of a $225 \times 71\,\mu m$ HF litz wire also without additional silk insulation. The limbs of the RM 10 core were also shortened to achieve a total air gap length of 2 mm (1 mm per limb) while keeping the total height of the core unchanged. To minimize the conduction losses of the H-bridge unfolder, 650 V/25 mΩ enhancement-mode GaN transistors from GaNSystems (GS66516T) were employed as they feature best-in-class on-state resistance. Because the hardware design does not allow for a direct heat sink connection, two 25 mΩ transistors are connected in parallel per switch to further reduce the conduction losses and virtually render cooling unnecessary. The PCI and inverter buck-stage are operated with an EMI friendly constant 140 kHz switching frequency. The unfolder H-bridge is operated with 120 Hz except, as described in more detail in the next section, during temporary 140 kHz unipolar PWM operation around the ZCs of the AC voltage (cf. Fig. 2.12 in Chapter 2).

The capacitor of the PCI C_b, with an effective large-signal equivalent capacitance of $\approx 120\,\mu F$, was realized by means of 200 individual 2.2 µF, 450 V class II/X6S MLCCs. As can be seen in Fig. 4.13, 200 of these chip capacitors were soldered together on a PCB which is on the one hand a very challenging assembly task and on the other hand bears the risk of electrical failures due to micro-cracks in the ceramic material caused by mechanical stress during assembly and/or operation.

4.3.2 Digital Control

The deployed control system of the LB 2.0 prototype is depicted in Fig. 4.14. The structure of the implemented PCI control system is identical to the LB 1.0 prototype (cf. Fig. 4.5) except that the current in inductor L_b is now regulated

by a conventional PI-feedback loop and fixed frequency PWM instead of TCM control. Likewise to the LB 1.0 control scheme, the AC output voltage is tightly regulated with a cascade of outer-loop voltage and inner-loop current feedback control using PR-controllers as shown in the bottom right of Fig. 4.14. The output voltage of the buck-stage, v_{C1}, is regulated with a PI-compensator to follow the rectified unfolder voltage reference $|v^*_{uf}|$ until it falls below the minimum defined value $\underline{V}_{C1}$,

$$v^*_{C1} = \max(|v^*_{uf}|, \underline{V}_{C1}). \tag{4.4}$$

As described in Section 2.4.2, during the time interval when $|v^*_{uf}| < \underline{V}_{C1}$, the buck output voltage reference is kept constant at $\underline{V}_{C1}$ and the duty-cycle of the unfolder, operated with 140 kHz unipolar PWM during this interval, is adjusted such that the voltage at the output of the unfolder v_{uf} follows precisely the sinusoidal reference v^*_{uf}. Preventing v_{C1} to fall below a minimum value, prevents distortions in the output current during the ZC of the voltage, which is particularly of concern for reactive loads when the output voltage and current are not in phase, and also allows to adopt TCM modulation in the buck-stage if desired ($v_{C1} > 0$ needed at any time for $\mathrm{d}i_{L1}/\mathrm{d}t < 0$ during turn-off interval). Since, the time interval in which the unfolder H-bridge is operated with PWM is very short compared to the AC period and because the switched voltage is also low (= $\underline{V}_{C1}$), the occurring switching losses of the unfolder H-bridge are negligible. The experimental waveforms to illustrate the described inverter control concept are shown in Fig. 4.15 and were recorded during commissioning of the LB 2.0 hardware. Fig. 4.15(a) shows how v_{C1} does not fall below the specified minimum voltage of $\underline{V}_{C1} = 25\,\mathrm{V}$ and the unfolder H-bridge engages in unipolar PWM during this period. As can be seen in Fig. 4.15(b), this effectively prevents distortions during the ZCs of the AC output voltage typically present in PFC rectifier systems.

In order to tightly control v_{C1}, particularly at the transitions between rectified sinusoidal and constant voltage reference, a cascade of PI-controllers with outer-loop voltage and inner-loop current feedback is employed. Likewise to the PCI power buffer, conventional constant frequency PWM is employed to generate the switching signals for the DC/|AC| inverter buck-stage.

The entire digital control system of the LB 2.0 depicted in Fig. 4.14, is implemented on a TI C2000 Delfino real-time microcontroller (TMS320F28335ZJZS) and no additional FPGA is employed. The currents are measured with Hall-effect current sensors from Allegro featuring 1 MHz bandwidth (ACS730).

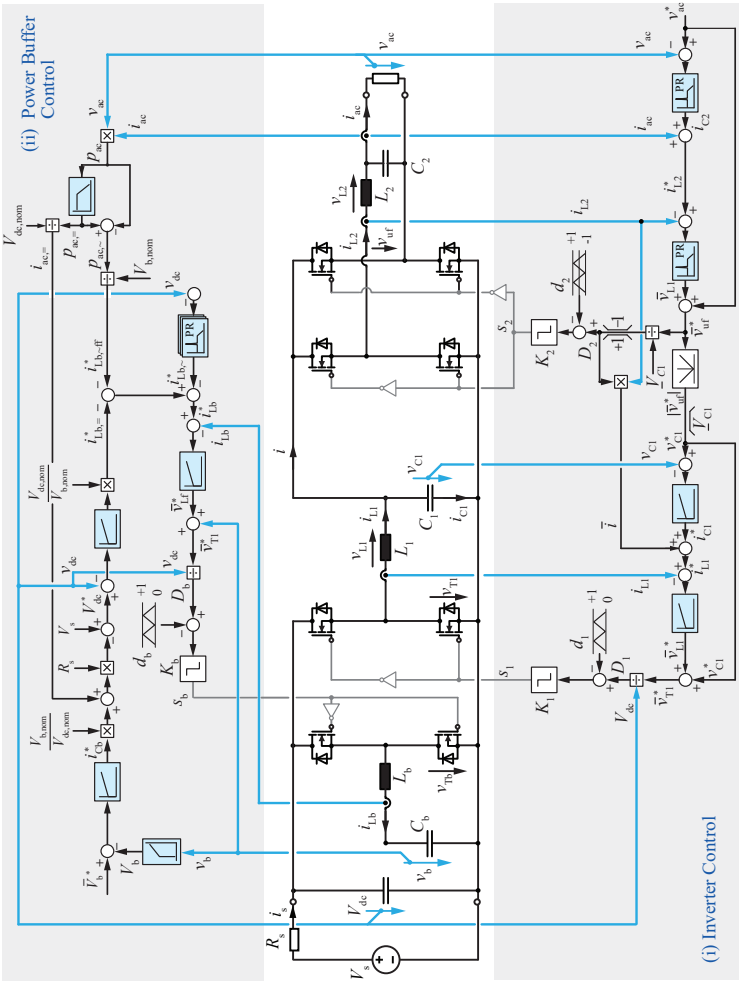


Fig. 4.14: Implemented digital control system of the Little Box 2.0 (LB 2.0). The inverter control structure is located below and the power buffer control structure is located above the power circuit diagram of the converter. For the sake of simplicity, the complete EMI filter is not included in the circuit diagram. The AC output voltage is controlled in the DM filter at the unfolder output, which is represented by components L_2 and C_2.

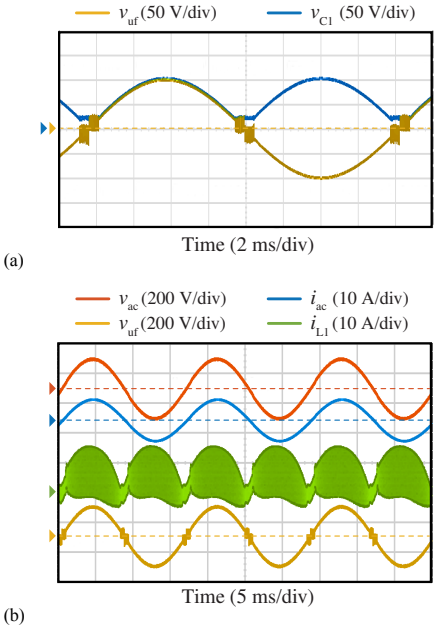


Fig. 4.15: Experimental measurements (a) demonstrating the temporary PWM operation of the unfolder and the corresponding constant DC/|AC| buck-stage output voltage v_{C1} which (b) prevents distortion in the AC output current during ZCs of the output voltage.

4.3.3 Experimental Waveforms

Fig. 4.16 shows the measured characteristic waveforms of the LB 2.0 prototype at steady-state and rated output power. The sinusoidal output voltage and current and the HF current in the DC/|AC| buck-stage inductor L_1 are shown in Fig. 4.16(a). The waveforms of the PCI and the DC-side of the converter are depicted in Fig. 4.16(b). Considering v_{dc} (red trace) and converter input current i_s (blue trace), it can be seen that the PCI effectively compensates the fluctuating AC power and the specified DC-link voltage and input current ripple limits are clearly met. Note, that the measurement of v_{dc} was performed with AC coupling. The resulting peak-to-peak voltage swing present in the buffer capacitor voltage v_b amounts to 180 V and is superimposed to the bias or offset voltage $V_b = 280$ V. Because of the lower AC excitation losses of the class II/X6S capacitors (cf. Section 2.3.1 and Appendix B), a much larger

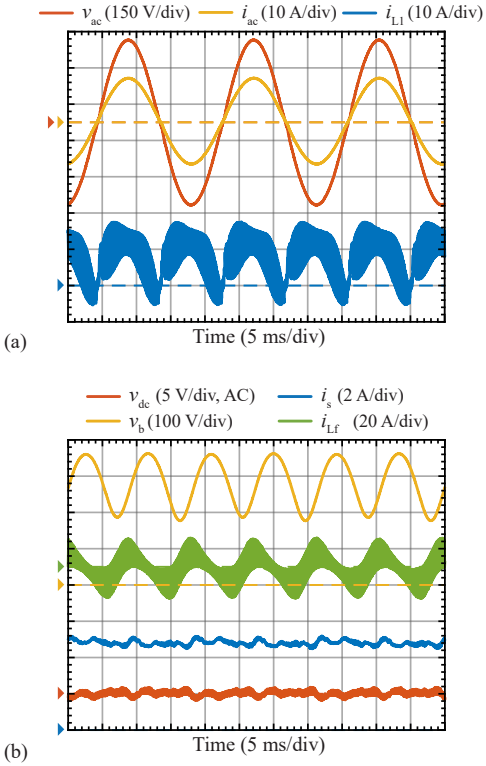


Fig. 4.16: Measured steady-state waveforms of the Little Box 2.0 (LB 2.0) operated at rated 2 kW output power ($\cos\phi_0 = 1$). (a) shows the AC output waveforms v_{ac} and i_{ac}, and the high-frequency current in the buck-stage inductor L_1. (b) The active power buffer clearly eliminates the double-line frequency voltage ripple.

voltage swing is feasible compared to the CeraLink power buffer (cf. Section 4.2.3, peak-to-peak voltage swing of 110 V). Fig. 4.17 shows the measured waveforms of the LB 2.0 converter during a transient caused by a stepwise increase in output power. Fig. 4.17(a) shows the AC output waveforms and Fig. 4.17(b) shows the corresponding PCI power buffer and DC-side related waveforms during a load step from 1.35 kW to 2 kW. The amplitude of the AC output voltage and current are settled quickly after one period which can be attributed to the high bandwidth of the underlying DC/|AC| buck-stage current control (cf. Section 4.3.2 of this chapter). Triggered by the step,

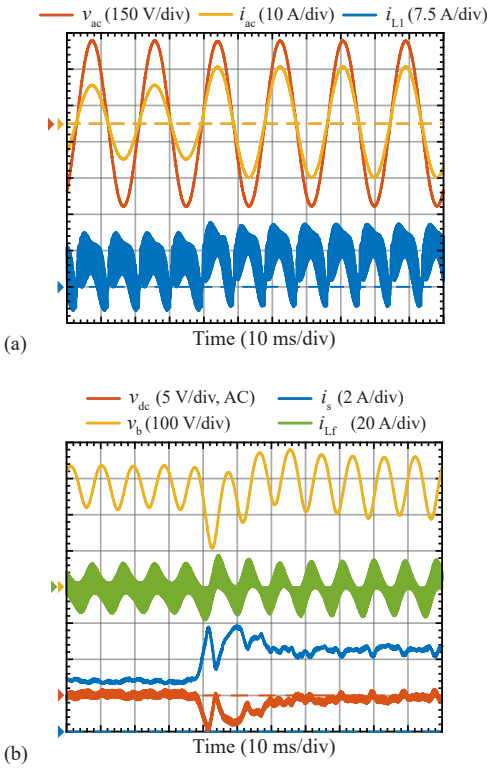


Fig. 4.17: Transient waveforms of the Little Box 2.0 (LB 2.0) subject to a stepwise increase in output power. (a) Measured AC output waveforms v_{ac} and i_{ac}, and filter inductor current i_{L1} and (b) measured DC-side and power buffer waveforms resulting from a stepwise load increase from 1.35 kW to 2 kW.

the average buffer capacitor voltage drops around 100 V below the 280 V at steady-state and recovers after 35 ms when the transient is settled. Naturally, the buffer capacitor voltage exhibits a larger amplitude of the 120 Hz voltage ripple once the load is increased. Note that the DC-link voltage settles at the same level after the load step because of the AC coupling of the voltage measurement. As it can be inferred from the shorter settling time and the overshoot of the input current i_s, the DC-link controller is tuned more aggressively compared to the LB 1.0 implementation (cf. Section 4.2.3). In any case, the transient performance of the deployed control system clearly complies

with the specified settling time of 1 s for the maximum required step size of 500 W.

4.3.4 EMI Compliance

Because of the intermittent HF PWM operation of the unfolder, a dedicated output filter for each leg of the H-bridge is provided. Since only a low voltage, $\underline{V}_{C1} = 25\,\text{V}$, is switched with 140 kHz, a comparably small DM filter inductor $L_{DM0} = 8.2\,\mu\text{H}$ (Coilcraft XAL1010-822MED) is sufficient at the output of the unfolder. The filter capacitors placed between the output phases, C_{DM1}, and between the respective output phase and the negative DC-Link terminal, C_2, are implemented with $4 \times 2.2\,\mu\text{F}$ 450 V/X6S MLCC. In order to dampen transients possibly triggered at the beginning and end of the recurring unfolder PWM operation interval, an additional damping branch is included in the first filter stage. The damping resistor $R_{DM1} \approx 1.25\,\Omega$ is implemented with 8 parallel 10 Ω 0805 SMD resistors. It should be pointed out again, that the output capacitors C_2 help to attenuate not only DM noise but also CM noise which allows to place only a single dedicated CM inductor in the EMI filter. L_{CM1} is realized with a toroidal VITROPERM 500F core (T60006-L2009-W914) with 10 turns using 1 mm-Ø solid copper wire. To achieve the required DM attenuation, additional DM inductors L_{DM1} are placed in the second filter stage. Likewise to L_{DM0}, the same commercially available 8.2 µH inductors from Coilcraft are used. The CM capacitors C_{CM0} and C_{CM1} are implemented with 3×100 nF, 630 V class II/X7R MLCCs from TDK (C3225X7T2J104K160AC).

As it became evident during the experimental EMI measurements, the implemented filter as shown in Fig. 4.12 was not sufficient to meet the FCC Part 15 B limits at frequencies below 1 MHz. By means of measurements with a DM/CM noise separator auxiliary equipment, inserted between the LISN RF output and the test-receiver input, CM noise was identified as the main problem. To meet the EMI requirements, an additional tiny CM choke was inserted at the DC input of the converter as shown in Fig. 4.18. The additional choke L_{CM0} was realized with a toroidal core with outer diameter of 13.7 mm and height of 3.6 mm using also VITROPERM 500F (T60006-L2012-V217). The CM winding was realized with 5 turns of 0.8 mm-Ø) solid copper wire resulting in a nominal CM inductance of around 250 µH. The boxed volume of this additional CM choke is in the order of only 1.3 cm^3 (< 1.0 % of the total LB 2.0 volume) and there is virtually no impact on the overall efficiency.

Since it was only intended to test the LB 2.0 hardware prototype in the laboratory, no explicit enclosure was designed. However, for the conducted

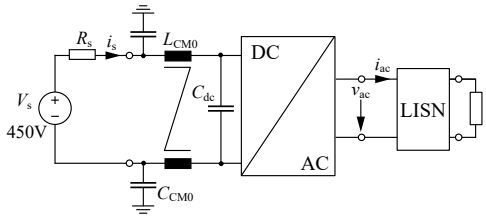


Fig. 4.18: Additional tiny CM choke L_{CM0} inserted at the DC input to meet the EMI limits.

EMI measurements presented next, the converter was placed on top of an aluminum baseplate which was connected to the ground/PE terminal of the EMI test setup. The ground terminal of the prototype was directly connected to the aluminum plate. The measured quasi-peak EMI spectrum of the LB 2.0 hardware prototype at 2 kW output power is depicted in Fig. 4.19(a). The results where again obtained with the R&S ESPI7 test receiver and the R&S ENV216 single-phase LISN which was installed between the AC output of the converter and the resistive load bank. It can be clearly seen that at low frequencies up to 20 MHz the FCC Part 15 B conducted EMI limits are met. Compared to the spectrum of the LB 1.0 prototype (shown in light grey), distinct peaks are visible at multiples of the switching frequency. As can be seen, at very high frequencies between 20 MHz – 30 MHz, the measured noise just remains below the limit. Since parasitics are detrimental to the available filter attenuation at these high frequencies, it is expected that with a complete metal enclosure several dB µV of safety margin could be gained.

As described previously in Section 4.2.4 of this chapter, for the ground current measurement an additional external decoupling CM choke was inserted between the DC supply (Sorensen SGI 600/17) and the input of the converter. The nominal inductance value of this decoupling CM choke is almost a factor of 9 larger compared to L_{CM0}. The measured ground current at the nominal operating point is depicted in Fig. 4.19(b) and its RMS value amounts to 5.7 mA which would exceed the initial strict ground current limit of 5 mA. Clearly visible are the current peaks up to 100 mA located around the zero crossings of the AC voltage which are triggered by imperfections in the transition to temporary PWM operation of the H-bridge unfolder and deviations of the DC/|AC| buck-stage output voltage v_{C1} from its reference. Without adding the additional (external) CM choke between the DC supply and the input of

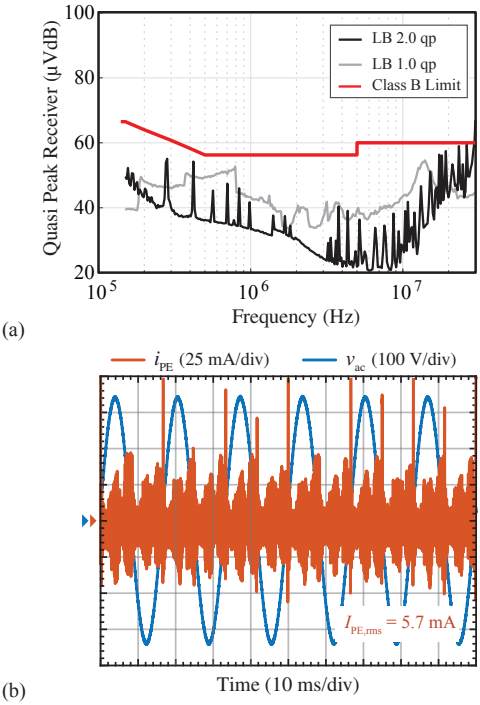


Fig. 4.19: (a) EMI noise spectrum of the Little Box 2.0 at 2 kW output power measured with R&S ENV216 single-phase LISN and R&S ESPI7 test receiver. (b) Ground current of the Little Box 2.0 measured by means of inserting both inverter output conductors simultaneously into the clamp of the current probe (Teledyne CP030).

the converter, the RMS value of the measured ground current amounts to 14.93 mA which is still in accordance with the revised GLBC specifications.

4.3.5 Efficiency

The measured efficiency of the LB 2.0 prototype as a function of output power is depicted in Fig. 4.20(a). The blue line with circle-type markers represents the efficiency of the system if two Sunon 12 V DC fans (MF25101V1-1000U-A99) are employed. The peak efficiency at 2 kW amounts to 97.4 %. The red line with cross-type markers represents the measured efficiency if two 8 V

high-speed fans are employed (WTF, 20 000 RPM @ 7.2 V). The total power consumption of the WTF fans amounts to ≈ 6 W which explains the drop in efficiency to 97.2 % at full output power. As indicated, this is still significantly higher than the 96.3 % peak efficiency achieved with the LB 1.0 converter. The CEC weighted efficiency of the LB 2.0 amounts to 96.12 % with conventional fans (Sunon). Since the increased cooling performance achieved with the high-speed fans is actually only needed at high loads above ≈ 1.7 kW and the CEC weighting coefficient at rated power is only 0.05, the lower nominal efficiency when using the high-speed fans has virtually no affect on the CEC weighted efficiency. In practice, the fan speed can be adjusted according to the output load level and/or the corresponding cooling demand (this was not considered during the experimental testing), thus it is reasonable to report a weighted efficiency of 96 %. The yellow line with star-type marker depicted in Fig. 4.20(b) represents the efficiency of only the PCI without the inverter. For this purpose, an electronic load (Chroma 63201) was used to emulate the pulsating power caused by the inverter. It can be seen that the peak efficiency at close to rated output power exceeds 99 % efficiency. Displayed in red with cross-type markers is the measured efficiency of the LB 2.0 if only the inverter is operated and the DC-link is passively buffered with high-density electrolytic capacitors ($3 \times 493\,\mu$F, 450 V, B43991-X0009-A223 from EPCOS/TDK). As can be seen in the plot, the peak efficiency then almost reaches 98 % at full output power. Due to the high efficiency of the PCI close to rated power, replacing the electrolytic capacitors with the active power buffer only reduces the overall efficiency by roughly 0.5 %. In case of the LB 1.0 (cf. Section 4.2.5), substituting the electrolytic capacitors with the more compact PCI resulted in a reduction of 1.2 % in overall efficiency. The main reason for this is that compared to the CeraLink technology utilized in the LB 1.0 to realize the buffer capacitor, the X6S MLCC exhibits a much lower power loss (≈ 1.5 W instead of ≈ 17.3 W at 2 kW).

4.3.6 Cooling and Operating Temperature

As can be seen from the picture of the LB 2.0 hardware in Fig. 4.13, the cooling system consists of a single custom machined copper heat sink and two 25 mm × 25 mm × 10 mm DC fans. The fans are directly attached to the fins of the heat sink without an additional duct. The 4 mm thick baseplate extracts the losses from the power transistors (cooling through the PCB). The air stream exiting the heat sink, is then cooling the power inductors L_1 and L_b which are located directly after the heat sink. The fin dimensions

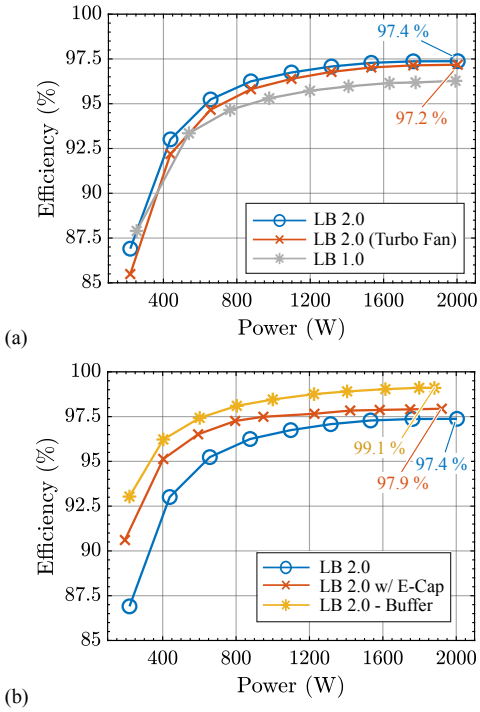


Fig. 4.20: Conversion efficiency of the Little Box 2.0 (LB 2.0) with respect to output power measured with a Yokogawa WT3000 precision power analyzer. (a) Efficiency with normal and high-speed DC fan and comparison with results from Little Box 1.0. (b) Efficiency with respect to output power of only the active power buffer (tested with electronic load), only the inverter equipped with electrolytic capacitors and the complete system.

are 20 mm × 18 mm × 0.5 mm and the channel width (distance between fins) amounts to 0.8 mm. Since manufacturing from a single copper block was not possible due to mechanical limitations, all fins were first cut from a thin 0.5 mm copper sheet and then inserted into machined channels in the base-plate and afterwards soldered for permanent fixation. Considering Sunon 12 V DC fans (MF25101V1-1000U-A99), the calculated cooling system performance index (CSPI, cf. Section 2.5) is in the order of 53 W/(K dm^3). Treating the free

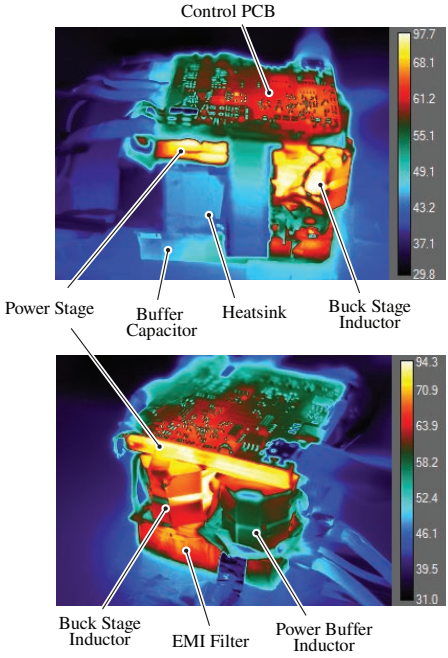


Fig. 4.21: Thermography images of the Little Box 2.0 (without enclosure) recorded with a FLIR A655sc infrared camera showing the steady-state temperature distribution at rated 2 kW output power.

space around the power inductors as air duct (cf. Fig. 4.13), the performance reduces to 37.5 $\mathrm{W/(K\,dm^3)}$.

In order to further increase the airflow passing by the power inductors and/or to limit the maximal winding temperature of the power inductors, the Sunon fans were replaced with more powerful ultra-high speed fans from WTF (20 000 RPM, re-purposed from RC model car applications) to provide better cooling in the nominal operating point as discussed previously.

The thermography image in Fig. 4.21 was recorded with a FLIR A655sc HD infrared camera and shows the steady-state temperature distribution of the LB 2.0 at 2 kW output power from two perspectives. The average temperature of the power stage (power transistor, gate drives, etc.) is approximately 80 °C. The power inductor of the inverter generates more losses and therefore, exhibits a higher steady-state operating temperature. The temperature of

the winding reaches approximately 84 °C. However, it should be noted that surfaces exposed to the outside which would directly touch the metallic enclosure, such as the core of the power inductors, the buffer capacitor, the EMI filter, the heat or the control PCB, exhibit operating temperatures of only 50 °C – 65 °C.

4.4 Discussion & Performance Benchmark

Based on the experimental results for the two hardware demonstrators provided in the previous sections, it can be concluded that both systems meet the technical specifications of the GLBC. Fig. 4.22 shows the calculated loss and measured volume distribution at 2 kW output power of the realized prototypes. As the total volume and loss figures indicate, 18 W of losses and about 103 cm^3 of volume are saved in case of the improved LB 2.0 compared to the LB 1.0. Because of the reduced power loss of the components and the higher cooling system performance, the cooling volume of the LB 2.0 was reduced from 95 cm^3 (39.6 %) to 46.5 cm^3 (33.7 %). Due to the installed ultra-high speed fans for improved cooling of the LB 2.0, the power consumption of the auxiliary electronics has almost doubled.

4.4.1 Main Reasons for the Higher Performance of the LB 2.0

As can be noticed by comparing Fig. 4.22(a) & (b), the power loss of the buffer capacitor (shown in dark blue) was significantly reduced. As described in Section 4.2 of this chapter, the buffer capacitor of the LB 1.0 was implemented with 120 x 2 µF, 600 V CeraLink capacitors from EPCOS/TDK. These ceramic capacitors can be operated with a large current ripple and feature a high capacitance density which, in contrast to class II ceramics, even increases with applied bias voltage and/or temperature [53]. Furthermore, the capacitors are available in compact 20 µF or even custom-made packages making the system assembly much easier and more reliable. From this perspective, the CeraLink technology seemed to be the right choice to implement the PCI buffer in the course of the GLBC, however, it turned out that these capacitors unfortunately generate high losses when subjected to a LF AC voltage with large amplitude such as present across the PCI buffer capacitor. For this reason, in the PCI buffer of the LB 2.0 system, class II/X6S MLCCs were utilized resulting in a reduction of the buffer capacitor losses by 15.8 W. Because of the lower loss density it is also possible to operate the buffer capacitor with a larger LF

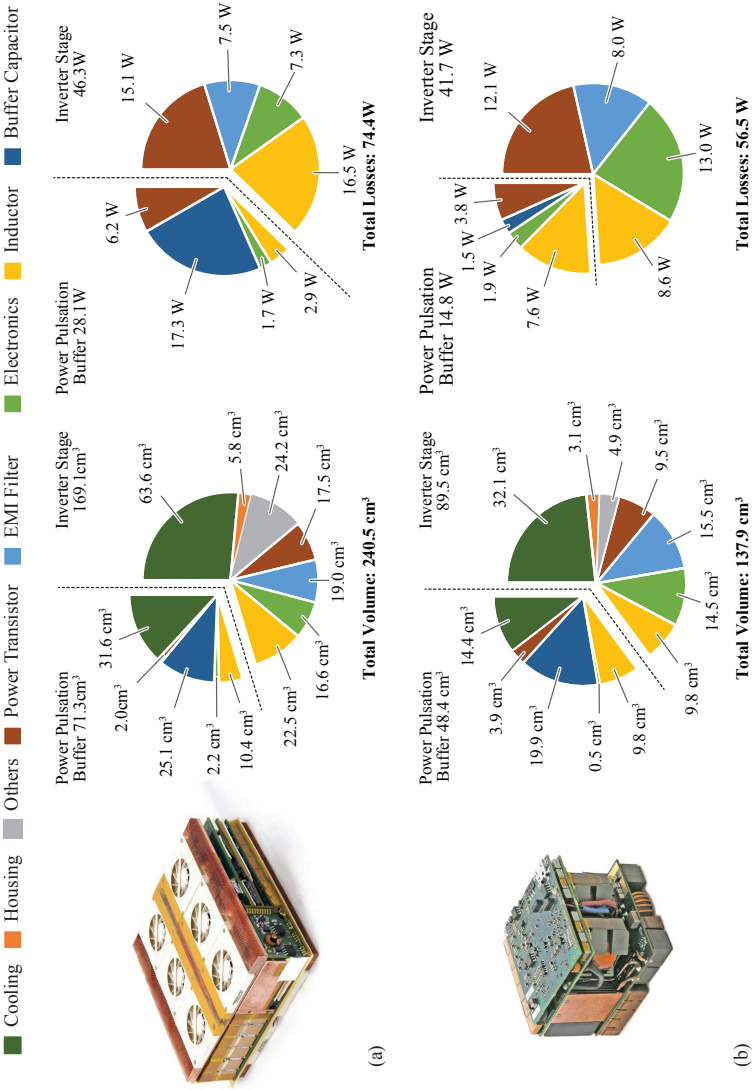


Fig. 4.22: Volume and power loss balance at 2 kW output power of the realized hardware prototypes: (a) Little Box 1.0 (LB 1.0) and (b) Little Box 2.0 (LB 2.0).

AC voltage amplitude of the voltage ripple which results in a slightly lower volume despite the fact that the capacitance density of the X6S MLCCs is slightly lower compared to CeraLink capacitors.

The LB 1.0 H-bridge inverter with 4D-interleaving was implemented with a total of 4 bridge-legs each with a dedicated HF inductor. In contrast, the LB 2.0 inverter DC/|AC| buck-stage was realized with a single bridge-leg and a single HF inductor. Therefore, despite the much lower switching frequency of the LB 2.0, 140 kHz as opposed to 250 kHz – 1 MHz of the LB 1.0, the total volume of the inverter's power stage – mainly determined by the power transistors and filter inductors – was reduced by roughly 50 % from 40 cm^3 to 19.3 cm^3. Interestingly, despite ZVS throughout the AC period and 4D-interleaving in case of the LB 1.0, the total losses in the power transistors are considerable due to the much higher switching frequency. As analyzed in [15] and discussed in Section 2.2.1, for the employed 600 V/70 mΩ GaN Gate Injection Transistor (GIT), soft-switching of 10 A at 400 V causes 2 µJ of energy dissipation per transistor and switching cycle. To exemplify, for a switching frequency of 1 MHz, this translates into 4 W of losses per bridge-leg and thus ZVS losses cannot be neglected at very high switching frequencies even if the latest GaN semiconductor technology is employed. It has been identified [15], that the lossy charging and discharging of the transistors' output capacitance (C_{oss}) during the resonant transition is the origin of the experienced ZVS losses and that the dissipated energy is a function of applied $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ rather than switched current. For this reason, practically lossless class I/C0G MLCC capacitors $C_{\mathrm{ext}} = 600\,\mathrm{pF}$, were added in parallel to the high-side and low-side GITs (charge equivalent parasitic output capacitance $C_{\mathrm{oss,Qeq}} = 114\,\mathrm{pF}$), which allowed to reduce the turn-off losses by around 30 % [6]. However, due to the higher effective output capacitance $C_{\mathrm{oss,eff}}$, now for the ZVS transient a higher amount of charge $Q_{\mathrm{oss,eff}}$ is needed to charge/discharge the effective output capacitances $C_{\mathrm{oss,eff}}$. This means that for a defined maximum dead time interval of $T_{\mathrm{dt}} \approx 125\,\mathrm{ns}$ (for two transitions this corresponds to 25 % of a 1 MHz switching cycle), a large current of 5 A is required to charge $C_{\mathrm{oss,eff}}$ from 0 V to 400 V and vice versa. This increases the peak-to-peak amplitude of the TCM current and therefore the RMS value and the associated conduction losses. Moreover, because of the remaining ZVS losses, a permanently interleaved operation of the bridge-legs at low power turned out to be no more beneficial in terms of efficiency. For this reason, the 4D-interleaving scheme as introduced in Section 2.4.3 with simultaneous operation of both bridge-legs only around the peak of the instantaneous output power was adopted.

In contrast, the inverter of the LB 2.0 with just a single bridge-leg and conventional PWM exhibits similar power transistor losses. This can be explained by the lower RMS value of the inductor current as opposed to the TCM modulation which results in lower conduction losses and the moderate 140 kHz switching frequency which limits the occurring hard-switching losses.

4.4.2 Benchmark with Google Little Box Challenge Finalists

Out of 100+ teams worldwide which submitted detailed descriptions of their technical approaches, 18 teams were selected to submit their converter to Google for final testing at the National Renewable Energy Laboratory (NREL) in Golden, Colorado, back in October 2015. The 1st price of the GLBC was awarded in February 2016 to the team of the Belgian company CE+T Power. Their converter achieved a power-density of 8.72 kW/dm^3 (142.9 W/in^3) which is - not surprisingly - only slightly higher than the power-density of the LB 1.0 converter system presented in Section 4.2 of this chapter, 8.18 kW/dm^3 (134 W/in^3), since CE+T Power and ETH Zurich were following the same technical approach (interleaved, H-bridge TCM inverter and buck-type PCI buffer). Among the 18 finalists, there were three categories: 7 teams were affiliated with technical consulting firms, 7 teams were affiliated with electrical engineering companies and only 4 teams were affiliated with universities. Moreover, 3 out of the 18 finalists did not show up at the final event. Most of the teams used either a H-bridge or a DC/|AC| buck-stage and |AC|/AC H-bridge unfolder topology to implement the inverter but overall no fundamentally new approach was presented. One of several innovative approaches worth mentioning, is the topology presented by the University of Illinois at Urbana-Champaign (UIUC), where the DC/|AC| buck-stage was realized with a 7-level flying capacitor topology using 100 V GaN transistors [25, 26]. Overall, 11 teams employed GaN power transistors, 2 teams used SiC and 2 teams relied on Si power transistors. Both, TCM modulation with ZVS throughout the AC period and variable switching frequency as well as conventional PWM with ZVS only around the ZC of the AC current and constant switching frequency were adopted by the finalists. Moreover, the majority of finalists used an active power buffer to cope with the fluctuating power at the AC side. The buck-type PCI buffer presented in the thesis at hand was employed by many finalists but also the partial-power stacked and series-connected active power buffer concepts were adopted [33, 44]. The majority

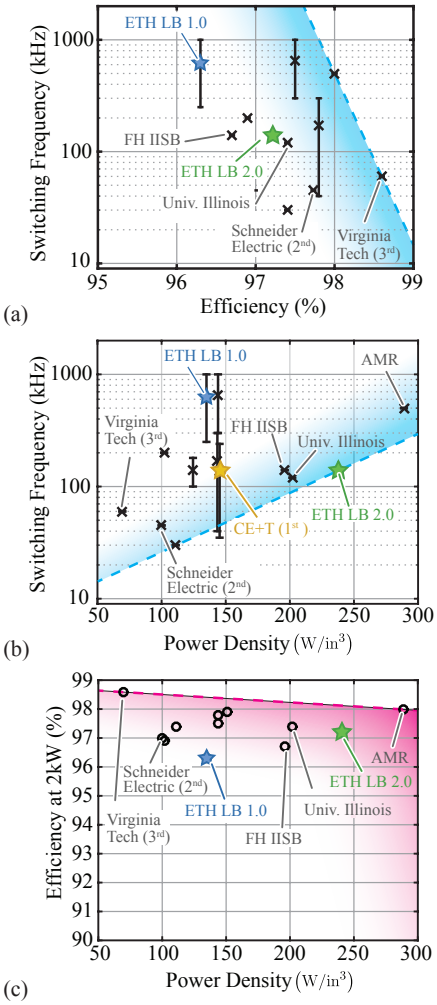


Fig. 4.23: Performance benchmark of the Google Little Box Challenge (GLBC) finalists concepts. The data was gathered from the technical approach documents of the finalists published by Google. (a) Switching frequency with respect to efficiency at 2 kW. (b) Switching frequency with respect to power-density. (c) Efficiency at 2 kW with respect to power-density. Note that the nominal efficiency at 2 kW of the inverter from CE+T Power is not known.

of contestants selected the 2.2 µF, 450 V, class II/X6S MLCC technology for the implementation of the buffer capacitor, in the bridge-leg output filters and for the DM capacitors in the EMI filter. To implement the HF filter inductors, a conventional approach using HF litz wire and MnZn ferrite core material was adopted by most of the finalists. Only two teams, including the author, employed a multi-gap inductor design.

Likely due to the short competition time-frame of just 15 months, none of the presented prototypes relied on advanced 3D-integration techniques such as PCB-embedding of active and/or passive components [80]. Instead, the presented hardware prototypes were altogether hand crafted engineering jewels with stacked, multi-board SMD-technology-based PCB designs with careful 3D CAD mechanical arrangement of components and a sophisticated heat management. More technical details of the individual concepts of the finalists are presented in the survey in [5].

The data for the benchmark shown in Fig. 4.23 was gathered from the publicly available technical approach documents of the GLBC finalists. Note, that some teams did not publish the achieved peak efficiency values and are therefore not included in Figs. 4.23(a) & (c). Figs. 4.23(a) & (b) show the switching frequency with respect to the efficiency at 2 kW and with respect to the achieved power-density, respectively. The interval marker indicates the variable switching frequency resulting from TCM modulation. Several teams selected a design with comparably high switching frequency in the range of 250 kHz – 1 MHz, others with a much lower switching frequency in the range of 35 kHz – 300 kHz. Irrespective of the frequency range, as can be seen in Fig. 4.23(b), the systems employing TCM reached similar power densities around 8.54 kW/dm^3 (140 W/in^3). Interestingly, two teams, i.e. Fraunhofer Institute for Integrated Systems and Device Technology (FH IISB) and the UIUC, achieved a remarkable power-density around 200 W/in^3 with a comparably low switching frequency between 120 kHz – 140 kHz. In case of the 7-level flying-capacitor converter, 120 kHz represents the switching frequency of a single converter cell and the effective switching frequency is actually 720 kHz. The data in Figs. 4.23(a) & (b) agrees with the well known tendency that increasing the switching frequency results in higher power-density at the cost of a lower efficiency. The achieved efficiency with respect to power-density is depicted in Fig. 4.23(c) and shows a clear trade-off between efficiency η and power-density ρ. The majority of the teams achieved a nominal efficiency in the range of 97 % – 98 %. Indicated with a blue and green star-type marker is the performance of the LB 1.0, described in Section 4.2, and the improved LB 2.0, described in Section 4.3, respectively. The yellow star

marker indicates the $\eta\rho$-performance of the GLBC winners (CE+T Power). It can be seen that by means of the DC/|AC| buck-stage based inverter topology and several improvements discussed previously, the LB 2.0 converter clearly outperforms the winning team from CE+T Power in terms of power-density. Interestingly, several teams including AMR (cf. Fig. 4.23(c)), OKE-Services and Cambridge Active Magnetics [5], claimed even higher power densities in the range of 300 W/in^3, however, no rigorous experimental evidence was published to support these claims.

4.4.3 A Critique of Little Box Challenge Inverter Designs - Revisited

In [102] a well written and comprehensive analysis of the GLBC inverter designs is provided. However, especially considering the latest progress achieved with the LB 2.0 hardware prototype presented herein, certain statements are questioned in the following. Fig. 4.24 shows the CEC weighted efficiency with respect to power-density of selected GLBC participants. The empirical trend-line of the observed trade-off between efficiency and power-density of the GLBC inverter designs proposed in [102],

$$\eta = 100 - (0.04 \times \rho), \tag{4.5}$$

whereby ρ is the power-density in W/in^3 and η is in %, is indicated by the dashed red line in Fig. 4.24. Although the proposed $\eta\rho$-trend-line is valid for many of the implemented designs, it fails to characterize the inverter designs with maximal power-density and does not distinguish between the H-bridge based and DC/|AC| buck-stage based inverter topologies. Therefore, based on the insights gained from the conducted Pareto optimization (cf. Section 2.7.1), two additional $\eta\rho$-trend-lines (4.6) and (4.7) are proposed, which better describe the inverter designs of the GLBC finalists with highest power-density, i.e. FH IISB for the H-bridge based inverter and UIUC for the DC/|AC| buck-stage based inverter concept, as indicated with the dashed blue and green lines in Fig. 4.24, respectively.

$$\eta = 98.3 - (0.0105 \times \rho), \tag{4.6}$$

$$\eta = 98.75 - (0.0105 \times \rho), \tag{4.7}$$

It should be noted that this trend-lines are just hypothetical and have yet to be confirmed.

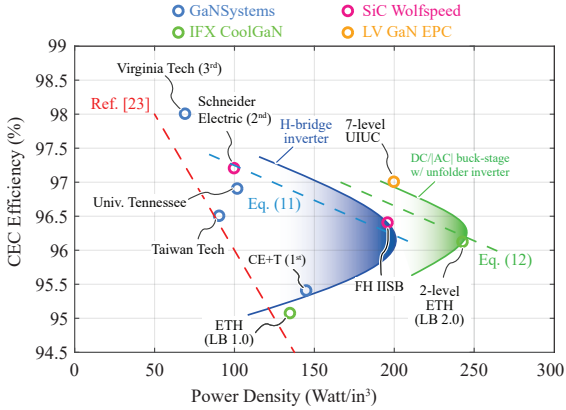


Fig. 4.24: CEC efficiency with respect to power-density of selected Google Little Box Challenge (GLBC) participants. The efficiency and power-density trade-off trend-line proposed in [102] is indicated by the dashed red line. Based on the insights gained from the Pareto optimization as presented in Chapter 2, two additional hypothetical trend-lines for the H-bridge (dashed blue line) and the DC/|AC| buck-stage (dashed green line) based inverter concepts, more characteristic for the designs of the GLBC finalists with highest power-density are proposed. Note, that only the inverter of GLBC participants with known CEC efficiency figures are shown.

It is therefore important to underline, that the 7-level flying capacitor inverter design should not be considered as an outlier with respect to the H-bridge based designs as stated in [102] but rather as a design which follows the $\eta\rho$ trade-off characteristic of the DC/|AC| buck-stage based inverter topologies.

Furthermore, the statement in [102] that employing Infineon CoolGaN devices in the inverter results, in low efficiency and just slightly higher power-density compared to other GaN-based H-bridge designs is clearly challenged. It can be seen from Fig. 4.24, that in case of the LB 2.0 inverter which employs the same CoolGaN devices as the LB 1.0 prototype, both η and ρ was increased. In this respect, it is important to emphasize that a holistic consideration of the employed topology and of all power electronic constituents is necessary to get a complete picture and thus understand the main driver of system performance. The consideration of only the power semiconductors is not sufficient. This is also exemplified by the $\eta\rho$-Pareto front simulation study depicted in Fig. 4.25 carried out for the H-bridge

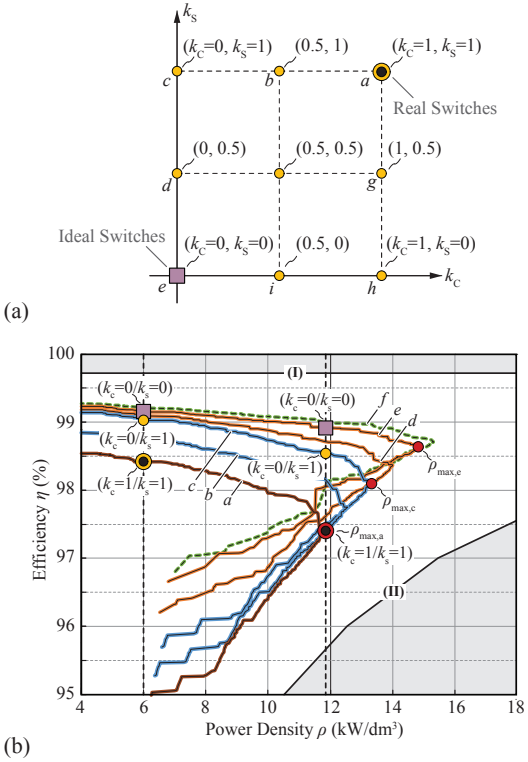


Fig. 4.25: (a) Scaling factors $k_c \in [0,1]$ and $k_s \in [0,1]$ of the conduction and switching losses, respectively, used to gradually idealize the power transistor properties; ($k_c = 1$, $k_s = 1$) represents the real GaN transistors (Infineon CoolGaN), ($k_c = 0$, $k_s = 0$) represents idealized switches without any conduction and switching losses. (b) The $\eta\rho$-Pareto fronts associated with the inscribed coordinates (k_c, k_s) for the H-bridge inverter with Triangular Current Mode (TCM) operation (cf. Fig. 4.3 of this chapter).

TCM inverter. In this study, scaling factors $k_c \in [0,1]$ and $k_s \in [0,1]$ of the transistor conduction and switching losses, respectively, are introduced to gradually idealize the power semiconductor properties. ($k_c = 1$, $k_s = 1$) represents the real GaN transistors (Infineon CoolGaN) and ($k_c = 0$, $k_s = 0$) represents idealized switches without any conduction and switching losses. It can be seen in Fig. 4.25(b) how idealizing the GaN transistors gradually improves both η and ρ. Once conduction, switching and gate drive losses

of the power semiconductors are completely excluded (ideal switches), the $\eta\rho$-Pareto front is exclusively determined by the filter passives, heat sink and auxiliary electronics. Naturally, if these components are implemented poorly, the resulting $\eta\rho$-performance is moderate even if ideal semiconductors would be at one's disposal.

4.4.4 Concerning an Industrial Implementation

The components of the realized hardware prototypes presented in this chapter are all operated within their safe operating area recommended by the manufacturers. The electrical distances in the PCB layouts satisfy laboratory requirements but do not comply with industrial creepage distance requirements. However, this can be addressed with a higher level of integration and advanced packaging. Although the employed high energy density ceramic capacitors significantly improve power-density, they are by no means an option for a cost-sensitive application. To exemplify, the active power buffer of the LB 2.0 uses 200 pieces of the 2.2 µF class II/X6S MLCC which amounts to $290 of component cost for the buffer capacitor (Digikey, order quantities above 1000 pieces). In contrast, using electrolytic capacitors for passive buffering of the DC-link amounts to only $14.85 of component cost ($3 \times 470\,\mu F$ from TDK's ultra-compact 450 µF B43640 series, at least 1.1 mF needed to satisfy the voltage ripple requirement). This cost consideration is likely also the reason behind Schneider Electrics' series-connected partial-power buffering approach which only relies on electrolytic capacitors [44]. In case of the LB 2.0, if electrolytic capacitors are employed instead of the active power buffer, then the power-density would drop from $14.8\,kW/dm^3$ ($243\,W/in^3$) to approximately $9.48\,kW/dm^3$ ($155.4\,W/in^3$) considering a boxed volume of $121.5\,cm^3$ of the electrolytic capacitor assembly. Based on this consideration, a power-density in the range of $6 - 9\,kW/dm^3$ ($100 - 150\,W/in^3$) is reasonable for a cost-constraint industrial inverter implementation in accordance with the GLBC specifications.

4.5 Summary

In this chapter the experimental results of two GaN-based converter concepts in accordance with the Google Little Box challenge (GLBC) specifications were presented. The first realized inverter, a 2-level H-bridge based inverter topology with interleaved bridge-legs, Triangular Current Mode (TCM) modulation with variable switching frequency in the range of 250 kHz - 1 MHz,

and a buck-type Parallel Current Injector (PCI) power buffer, achieved a power-density of 8.18 kW/dm^3 (134 W/in^3), a nominal efficiency of 96.4 % and a California Energy Commission (CEC) weighted efficiency of 95.07 %. This inverter, termed Little Box 1.0 (LB 1.0), was presented at the GLBC finals and was ranked among the top 10 out of 100+ contestants. The second realized hardware prototype (Little Box 2.0, LB 2.0) brings together all research findings and lessons learned during and after the GLBC and is composed of a 2-level DC/|AC| buck-stage operated with constant 140 kHz PWM and a subsequent |AC|/AC H-bridge unfolder. Because of the inherently generated low-frequency Common Mode (CM) voltage, this topology was not considered initially but became a truly viable option once the specified ground current limit was relaxed from 5 mA to 50 mA at a very late point during the competition. The LB 2.0, is also equipped with a buck-type PCI buffer but is realized with a more efficient buffer capacitor technology and exhibits a staggering power-density of 14.8 kW/dm^3 (243 W/in^3), a nominal efficiency of 97.2 % and a CEC weighted efficiency of 96.1 %. Compared to the other GLBC finalists as reported in [5, 102], the LB 2.0 inverter therefore sets a new experimentally supported benchmark with respect to power-density for a single-phase inverter in accordance with the GLBC specifications.

5

P^3DCT - Partial-Power Pre-Regulated DC Transformer

Chapter Abstract

In this chapter a new approach to regulate the output voltage of a resonant, constant voltage transfer ratio 380 V/48 V isolated DC/DC converter is presented. Rather than applying variable frequency control to the resonant converter which would result in reactive power processing and a more complicated EMC filter design, the converter remains in its optimal operating point all time and an additional partial-power (PP) processing auxiliary converter, closely related to the PP series voltage compensator concept discussed in Chapter 3, is used to tightly regulate the output voltage.

The PP converter, supplied through a tertiary winding of the resonant converter's transformer, regulates the output by adding or subtracting voltage from the DC input and has only a marginal impact on the overall efficiency of the DC/DC converter. The principal of operation is explained in detail including Sankey diagrams to illustrate the power processing of the converter and a feedback control system is proposed to tightly regulate the 48 V output voltage. A hardware demonstrator rated at 1.5 kW is implemented to cope with input voltage variations between 340 V – 420 V and experimental results are provided showing that the output voltage can be kept within ±1 % of the nominal 48 V even under harsh input voltage and load transients. The realized DC/DC converter with PP pre-regulation features an overall efficiency of 97.7 % at rated power and a power-density of 8.6 kW/dm^3 (141 W/in^3).

5.1 Introduction

The series-resonant LLC DC/DC converter is widely accepted in the IT and telecom industry due to several desired features such as high efficiency, low EMI and high power-density. The converter is typically employed to step down from 380 V and to supply a 48 V power distribution bus. When operated exactly at the resonance frequency of the LLC tank, the voltage transfer ratio

becomes ideally independent of the actual load [103]. At this point, the LLC converter is self-regulated and adjusts its current automatically according to the load condition, essentially behaving like a DC transformer (DCT). If regulation of the output voltage is required, fixed duty-cycle and variable frequency control could be applied which shifts the LLC tank operating point out of resonance into inductive operation in case a lower voltage transfer ratio is needed [104–107]. However, besides the reduced efficiency due to the additionally processed reactive power, the arising load dependency and the potential loss of Zero Voltage Switching (ZVS), variable frequency control is often depreciated as it complicates the EMC filter design. An alternative method which keeps the resonant converter in its optimal operating point is to employ an additional partial-power (PP) auxiliary converter to regulate the output voltage [108–115]. This auxiliary converter is dimensioned for just a small fraction of the rated power of the resonant converter and therefore has only marginal impact on the overall efficiency of the converter system. The PP regulation approach has also been thoroughly analyzed in PV applications for high-efficiency maximum-power-point tracking (MPPT) and/or PV string balancing [116–119]. In [110,115] a PP post regulator as shown in Fig. 5.1(a) is proposed, where the output of a PP DC/DC converter is connected in series with the output of the main converter and the load. The input of the PP DC/DC regulator is connected to an intermediate DC-link supplied by means of a tertiary transformer winding and subsequent rectifier. Unidirectional buck, boost and buck-boost DC/DC converters are suggested to implement the post-regulator. In [113,114] the topology shown in Fig. 5.1(b) is described. In this configuration, the primary winding of a separate auxiliary transformer (two separate cores) is connected in series with the primary winding of the main transformer and the output of the PP DC/DC converter is connected in parallel to the output of the main converter. In order to regulate the output voltage, the partial-power converter (PPC) is used to adjust the voltage across the primary side of the main converter. A similar approach is presented in [108], however, there the DC-side of the PPC is connected in parallel to the DC input (V_{in}) by means of a boost converter. In the topology suggested in [112], an auxiliary DC/DC converter is inserted between the rectifier bridge-legs of the main converter as illustrated in Fig. 5.1(c). The auxiliary converter alters the power-flow across the preceding rectifier bridge-leg by means of adjusting the rectifier voltage (voltage across the capacitor C_{aux} between the rectifier and the auxiliary DC/DC converter) in order to regulate V_{out}. However, since the auxiliary DC/DC converter processes approximately half the rated power of the main converter, the proposed topology constitutes

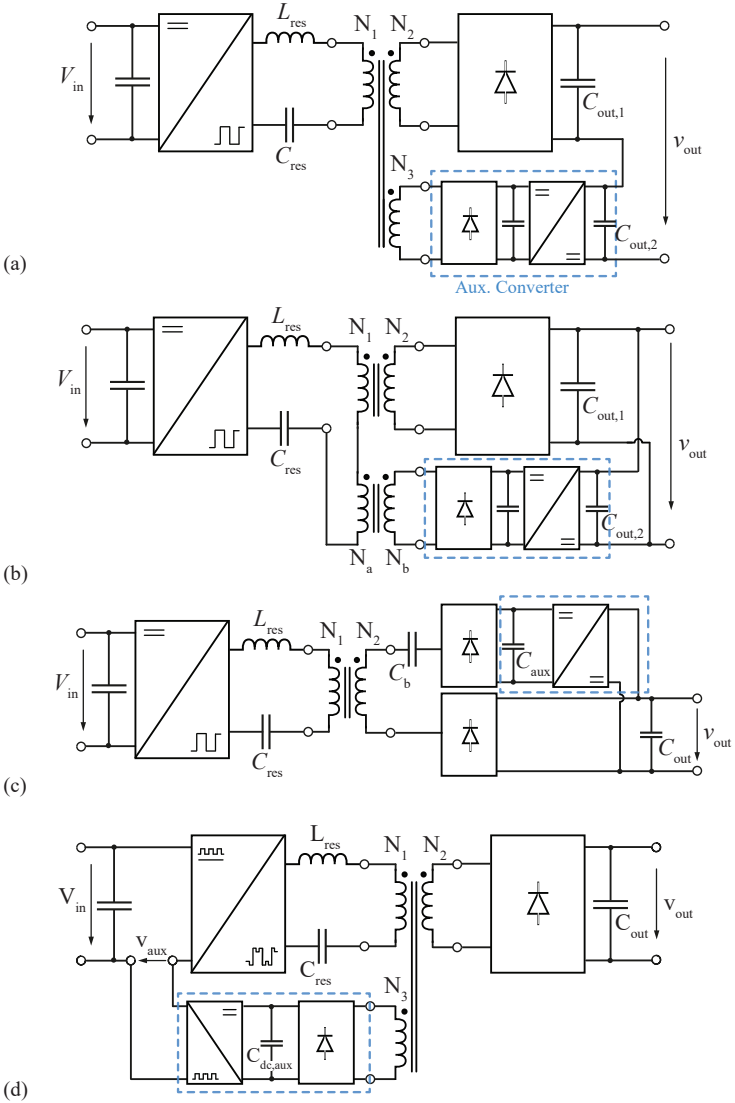


Fig. 5.1: (a)-(c) Several approaches to provide a regulated output voltage by means of an additional partial-power (PP) converter and (d) the filter-less, PP, pre-regulation approach proposed in this chapter. The PP converter is highlighted by means of the frame with blue, dashed lines.

Tab. 5.1: Design Specification of the Converter

Parameter	Value	Description
$V_{\text{in,nom}}$	380 V	Nominal DC input voltage
$V_{\text{in},\Delta}$	340 V – 420 V ($\approx$ 380 V $\pm$ 10.0 %)	Input voltage range
$V_{\text{out,nom}}$	48 V	Nominal DC output voltage
$V_{\text{out},\Delta}$	$\pm$500 mV ($\approx \pm$1.0 %)	Max. output voltage deviation in steady-state and during transients
P_{r}	1.5 kW	Rated power
η^*	98 %	Target efficiency 98 % and maximum power-density

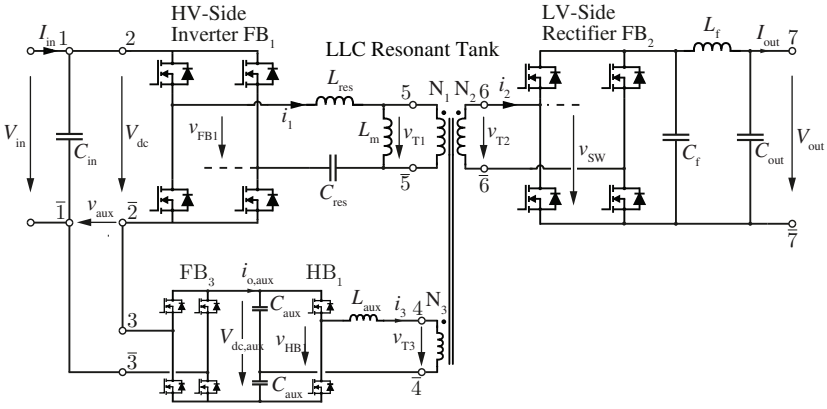
a $1^1/_2$ stage converter rather then an unregulated main converter with PP regulation.

The filter-less, pre-regulation approach proposed in this chapter is depicted in Fig. 5.1(d). Here, the output voltage V_{out} is regulated by adjusting the average voltage applied to the input of the main converter. Omitting additional filter components at the output of the PPC, a pulse width modulated voltage with certain local average value is impressed between the negative terminal of the DC input (V_{in}) and the main converter. It follows that the square wave voltage applied to the resonant tank of the DCT exhibits a superimposed high frequency PWM pattern which allows to adjust the average amplitude of the fundamental square wave voltage applied to the LLC tank by adopting the PPC modulation index.

In the following the proposed converter topology is presented in detail and the basic theory of operation is discussed (Section 5.2). Subsequently, in Section 5.3 a control system for the proposed converter is designed. In order to demonstrate the basic concept and verify the claimed performance of the proposed PP pre-control, a hardware demonstrator is implemented as described in detail in Section 5.4. The implemented 380 V/48 V DC/DC converter is rated at 1.5 kW and has been designed to cope with input voltage variations in the range of 340 V – 420 V. The design specifications are summarized in Tab. 5.1. Subsequently, in Section 5.5 experimental results are presented showing the performance of the implemented prototype in steady-state and during transients. Finally, Section 5.6 concludes this chapter.

5.2 Partial-Power Pre-Regulated (P^3) DC Transformer

The proposed topology shown in Fig. 5.2 consist of an unregulated resonant LLC converter and an additional PPC employed to tightly control output voltage V_{out} by pre-regulating the voltage applied to the input of the LLC converter. The full-bridge input stage, FB_1, of the LLC converter processes the main share of the output power and the resonant tank is dimensioned to feature a resonance frequency typ. in the range of 70 kHz - 250 kHz in order to achieve a high power-density. Since the resonant converter is always operated exactly at the resonance frequency regardless of input voltage and load conditions, a very efficient transfer of real power to the 48 V output is possible because only the reactive power to enable ZVS of full-bridge FB_1 must be processed. The stepped-down rectangular AC voltage appearing at the secondary side of the transformer, v_{T2}, is then rectified by means of a diode rectifier or a low-voltage MOSFET full-bridge (shown in Fig. 5.2) for increased conversion efficiency (sync. rectification) and/or bidirectional power-flow support. When operated at resonance, the LLC converter is



Partial-Power Pre-Regulation (P^3) Converter

Fig. 5.2: Schematic of the proposed 380 V/48 V DC/DC converter comprised of a unregulated, resonant LLC converter operating as DC Transformer (DCT) and an additional Partial-Power (PP) Pre-Regulation (P^3) auxiliary converter dedicated to tightly control output voltage V_{o}.

capable of autonomously adapting the current in case of a load step in order to keep the output voltage at its nominal value according to the voltage transfer ratio defined by the transformer turns ratio. Thus, the control system of the pre-regulation converter just has to ensure a proper input voltage level of FB_1 to compensate for ohmic voltage drops and other non-idealities in the main converter in order to keep V_{out} tightly regulated to the desired 48 V reference value.

5.2.1 Partial-Power Pre-Regulation Auxiliary Converter

As shown in Fig. 5.2 a PPC with bidirectional power-flow and bipolar voltage generation capabilities is proposed. The rectifier-side terminals of the PPC (cf. $4 - \overline{4}$) are connected to a tertiary winding of the isolation transformer (N_3) and the output terminals of the inverter (cf. $3 - \overline{3}$) are connected between the negative terminal of the input capacitor, C_{in}, and the negative rail of the full-bridge FB_1 of the main converter. The PPC DC-link, $V_{dc,aux}$, formed by two stacked capacitors C_{aux} is supplied from the LLC converter transformer through the low-voltage rectifier half-bridge HB_1 operated with the switching frequency of the main converter. For the given input voltage range (cf. Tab. 5.1), the level of $V_{dc,aux}$ is regulated typically to 50 V – 60 V by adjusting the phase-shift between HB_1 and the leading-leg of full-bridge FB_1 of the main converter.

One of the novelties of this approach is that the switched voltage v_{aux}, generated from pulse width modulation of $V_{dc,aux}$, is directly impressed between the terminals $\overline{1} - \overline{2}$ (cf. Fig. 5.2), taking advantage of the bandpass transfer characteristic of the LLC resonant tank and omitting additional filter elements. The waveforms of a circuit simulation with preliminary system parameters according to Tab. 5.2 are provided in Fig. 5.3(a) and (b) in order to illustrate the basic operation of the proposed converter system. Given that the switching frequency of FB_3 is a multiple of the resonance frequency (typically factor 4-10) of the main converter a rectangular waveform with modulated amplitude due to the superimposed pulse pattern is applied to the LLC tank of the main converter. It follows that the average amplitude of the square wave voltage applied to the resonant tank can be adjusted by means of the modulation index of FB_3, although the switched voltage v_{aux} causes the resonant current i_1 to slightly deviate from it's ideal sinusoidal shape. Given a converter input current $I_{in} \geq 0$ for unidirectional operation of the main converter, the polarity of the average pre-regulation voltage, $\overline{v}_{aux}$, defines the direction of power-flow in the PPC as illustrated by the Sankey diagrams in Fig. 5.4. In case of $\overline{v}_{aux} > 0$, a fraction of the output power $P_{7\overline{7}}$

Tab. 5.2: Parameters of the P^3DCT Circuit Simulation (Fig. 5.3).

System		P^3DCT			
V_{in}	380 V	C_{res}	150 nF	C_{aux}	125 µF
V_{out}	48 V	C_{in}	400 µF	$f_{s,FB,1}$	120 kHz
$V_{dc,aux}$	50 V	C_{out}	5.4 mF	$f_{s,HB,1}$	120 kHz
P_r	1.5 kW	L_{res}	10 µH	$f_{s,FB,3}$	720 kHz
P_{aux}	60 W	L_m	400 µH	$N_1 : N_2 : N_3$	14:2:1

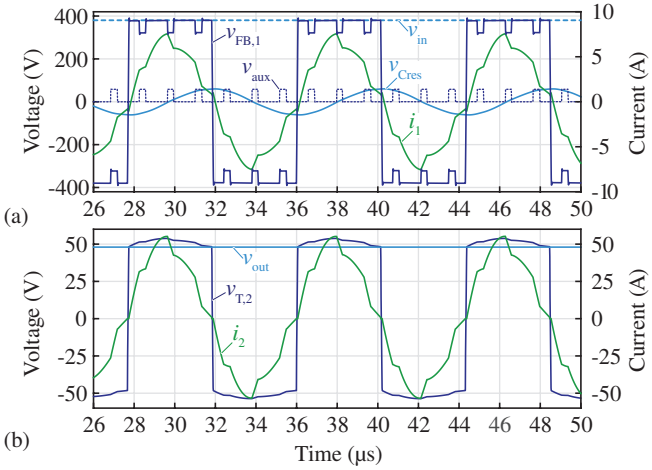


Fig. 5.3: Switching frequency waveforms of the simulated P^3DCT converter operating at rated power (1.5 kW). Primary side related voltage and current waveforms are shown in (a), secondary side related waveforms in (b).

(index $7\bar{7}$ denotes the respective power-flow interface according to the terminal labels in Fig. 5.2) is actually provided by the PPC as depicted in Fig. 5.4(a). On the contrary, for $\bar{v}_{\text{aux}} < 0$, power $P_{3\bar{3}}$ circulates within the PPC and the

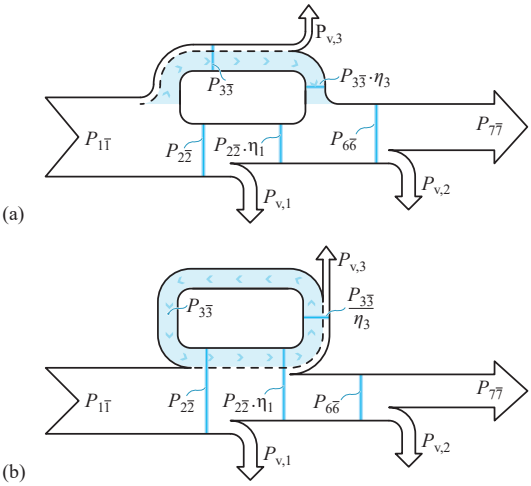


Fig. 5.4: Sankey diagram of the power-flow inside the P^{3}DCT for pre-regulation voltage (a) $\bar{v}_{\text{aux}} > 0$ and (b) $\bar{v}_{\text{aux}} < 0$. The indices denote the power-flow through the respective interfaces labeled in Fig. 5.2. Power loss $P_{\text{v},1}$ and $P_{\text{v},2}$ is caused by the inverter and rectifier stage of the main converter, respectively. $P_{\text{v},3}$ are the losses associated with the processing of the pre-regulation power-flow.

inverter stage of the DCT and does not contribute to the output power $P_{7\bar{7}}$. Consequently, an operation of the P^{3}DCT with $\bar{v}_{\text{aux}} > 0$ is advantageous in terms of efficiency.

5.2.2 Power Rating and Efficiency Impairment

Assuming loss-less operation, the power requirement of the PPC is given by

$$P_{\text{aux}} = \frac{\bar{v}_{\text{aux}}}{V_{\text{in}}} P_{\text{out}} = \frac{V_{\text{in}} - nV_{\text{out}}}{V_{\text{in}}} P_{\text{out}} = \left(1 - n\frac{V_{\text{out}}}{V_{\text{in}}}\right) P_{\text{out}}, \tag{5.1}$$

where, $n = \frac{N_1}{N_2}$, is the primary-to-secondary winding turns-ratio of the isolation transformer. Expression (5.1) is plotted in Fig. 5.5 with respect to the input voltage, V_{in}, and different transformer turns-ratios. It can be seen that

depending on n, unipolar operation is feasible, e.g. $\overline{v}_{\text{aux}} \leq 0$ for $n > 8.75$ considering the given input voltage range, which would allow to further simplify the topology of the PPC (half-bridge instead of FB_3 and diode rectifier instead of HB_1). However, as a consequence of unipolar operation, the total power to be processed by the PPC increases substantially due to the additional bias in $\overline{v}_{\text{aux}}$ at nominal input voltage which reduces the overall conversion efficiency of the P^3DCT although operation with circulating power (cf. Fig. 5.4(b)) could be completely omitted if $\overline{v}_{\text{aux}}$ remains positive for $n < 7.0$.

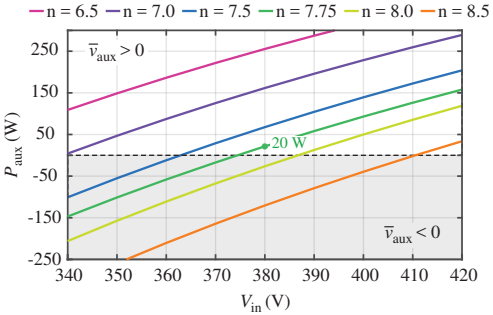


Fig. 5.5: Power requirement of the PPC as a function of the input voltage V_{in} and the transformer turns ratio, $n = N_1 : N_2$, at 1.5 kW output power.

For the implemented hardware demonstrator described in detail in Section 5.4 of this chapter, a turns-ratio of $n = 7.75$ was chosen (cf. green line in Fig. 5.5) which results in a maximum power requirement of approximately 150 W. At rated output power and nominal input voltage, $V_{\text{in}} = 380$ V, the PPC processes only around 20 W. Thus, the PPC must only be dimensioned for a fraction of the nominal output power processed by the main converter.

A numerical example based on efficiency measurements of the hardware demonstrator presented later in Section 5.5 should illustrate the marginal impairment of the overall conversion efficiency due to the PPC. The total conversion efficiency of the P^3DCT can be derived from the Sankey diagrams (cf. Fig. 5.4) and is given by

$$\eta = \begin{cases} \eta_1\eta_2 \cdot (1+k) - \frac{\eta_2}{\eta_{\text{aux}}} \cdot k, & \overline{v}_{\text{aux}} < 0 \\ \eta_1\eta_2 \cdot (1-k) + \eta_2\eta_{\text{aux}} \cdot k, & \overline{v}_{\text{aux}} > 0 \end{cases} \tag{5.2}$$

wherein η_1 and η_2 denotes the efficiency of the inverter and the rectifier stage, respectively. Accordingly, the efficiency of the main converter is given by

$\eta_m = \eta_1\eta_2$. The efficiency of the PP pre-regulator is denoted with η_3 and factor $k = {}^{P_{aux}}/_{P_1}$ is the ratio between the power processed by the pre-regulator and the DCT. Given the efficiency of the main converter, $\eta_m = 99.25\,\% \cdot 98.75\,\% = 98.0\,\%$, a power ratio $k = {}^{20\,W}/_{1.5\,kW} = 0.013$ and an efficiency $\eta_{aux} = 82\,\%$ at 20 W of the PPC, then according to (5.2), $\eta = 97.7\,\%$ results if $\bar{v}_{aux} < 0$ and $\eta = 97.8\,\%$ if $\bar{v}_{aux} > 0$. Hence, the (very) low efficiency (82 %) of the PPC reduces the overall conversion efficiency of the converter at rated power only by $0.2\,\% - 0.3\,\%$ at rated power and nominal input voltage.

5.3 Control System

In order to tightly regulate the output voltage to 48 V and reject load and input voltage disturbances, the control system depicted in Fig. 5.6 is proposed. Two feedback control loops are employed to regulate v_{out} and the partial-power DC-link voltage $v_{dc,aux}$. As it will become evident from the experimental results presented in Section 5.5, the DC-link of the PPC is sized large enough and/or the bandwidth of the $v_{dc,aux}$ control loop suffices such that coupling between the control loops can be neglected and, for the sake of simplicity, two individual Single-Input Single-Output (SISO) designs are considered in the following. The proposed small-signal feedback loop of the output voltage is shown in Fig. 5.6(a). A first-order low-pass filter with 1 kHz corner frequency, M_{vout}, is employed to take both analog and digital implemented low-pass filters of the output voltage measurement into consideration. The control error, the difference between reference V^*_{out} and $v_{out,m}$, is passed on to the PI controller,

$$\mathrm{PI}_{out}(s) = K_{p,out}\frac{(sT_{i,out}+1)}{s}. \tag{5.3}$$

Deviations of the input voltage from the nominal $V^*_{in} = 380\,V$ are directly compensated by means of the feed-forward term, $\bar{v}_{aux,ff}$. The transfer function M_{in} represents a first-order low-pass with 10 kHz corner frequency and captures the phase-delay introduced by the measurement and conditioning of v_{in}. A derivative term can be included to better cope with abrupt input voltage changes but was finally not implemented on the Digital Signal Controller (DSC) of the hardware demonstrator. The parameter V^*_{offset}, added to the measured input voltage, is used to adjust $\bar{v}^*_{aux}$, such that the nominal input voltage results in the desired 48 V output voltage for a specific transformer turns-ratio. According to the polarity of the auxiliary voltage $\bar{v}_{aux}$ in Fig. 5.2, $\bar{v}_{aux}$ must be decreased in order to increase the output voltage, which explains why the

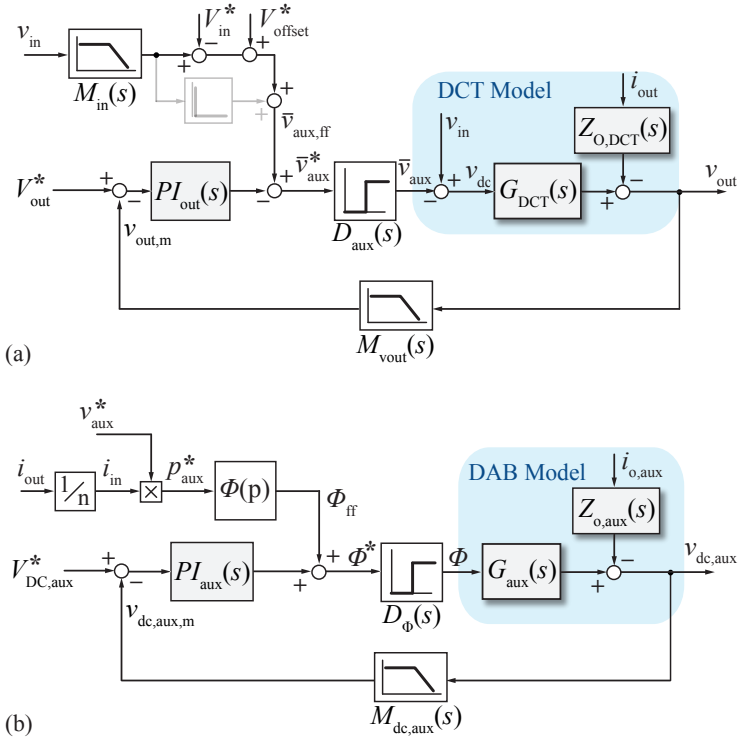


Fig. 5.6: Schematic of the control system to regulate (a) the output voltage, v_{out}, of the main converter and (b) the DC-link voltage of the auxiliary converter, $v_{\mathrm{dc,aux}}$.

Tab. 5.3: Controller Parameters.

Controller	Parameter	Value
$\mathrm{PI}_{\mathrm{out}}$	$K_{\mathrm{p,out}}$	$17.0 \times 10^3 \ \frac{1}{\mathrm{s}}$
	$T_{\mathrm{i,out}}$	2.94×10^{-6} s
$\mathrm{PI}_{\mathrm{aux}}$	$K_{\mathrm{p,aux}}$	$1.5 \ \frac{\mathrm{rad}}{\mathrm{Vs}}$
	$T_{\mathrm{i,aux}}$	0.02 s
$\Phi(p)$	m	$3.641 \times 10^{-3} \ \frac{\mathrm{rad}}{\mathrm{W}}$
	q	6.9×10^{-2} rad

output of $\mathrm{PI}_{\mathrm{out}}$ is subtracted from the feed-forward term, $\bar{v}_{\mathrm{aux,ff}}$. The dead time introduced by the pulse width modulator (PWM) of FB_3 is considered by means of a second-order Padé approximation of the delay $D_{\mathrm{aux}}(s) = \mathrm{e}^{-s\frac{T_{\mathrm{s,aux}}}{2}}$, where $T_{\mathrm{s,aux}}$ is the switching period of FB_3. In order to determine suitable coefficients for the PI controller, a small-signal model of the DCT including the CLC filter (cf. Fig. 5.2) was derived based on the analysis presented in [103]. The PI controller parameter (5.3) for a conservative design with 400 Hz bandwidth and 60° phase-margin are listed in Tab. 5.3.

The proposed feedback loop to control the PPC DC-link voltage, $v_{\mathrm{dc,aux}}$, is depicted in Fig. 5.6(b). By means of another PI controller,

$$\mathrm{PI}_{\mathrm{aux}}(s) = K_{\mathrm{p,aux}} \frac{(sT_{\mathrm{i,aux}} + 1)}{s}, \tag{5.4}$$

the phase-shift Φ between the leading-leg of FB_1 and HB_3 is regulated in order to control the correct power-flow at the terminals of the transformer tertiary winding (cf. $4 - \overline{4}$ in Fig. 5.2) such that $v_{\mathrm{dc,aux}}$ meets the reference value $V^*_{\mathrm{dc,aux}}$. A first-order low-pass filter with 1 kHz corner frequency, $M_{\mathrm{dc,aux}}$, is employed to model the measurement and conditioning of the DC-link voltage. The dead time introduced by the PWM of HB_1 is considered by means of a second-order Padé approximation of the delay $D_{\phi}(s) = \mathrm{e}^{-s\frac{T_{\mathrm{s}}}{2}}$, where T_{s} is the switching period of FB_1. In order to determine proper parameters for $\mathrm{PI}_{\mathrm{out}}(s)$, a small-signal model of the PPC rectifier, $G_{\mathrm{aux}}(s) = \frac{v_{\mathrm{dc,aux}}(s)}{\Phi(s)}$, was derived according to the work in [120, 121]. The PI controller parameter (5.4) for a conservative design with 100 Hz bandwidth and 135° phase-margin are listed in Tab. 5.3.

By estimating the power processed by the PPC,

$$p^*_{\mathrm{aux}} = \bar{v}_{\mathrm{aux}} I_{\mathrm{in}} \approx \bar{v}^*_{\mathrm{aux}} I_{\mathrm{in}} = \bar{v}^*_{\mathrm{aux}} \frac{I_{\mathrm{out}}}{n}, \tag{5.5}$$

a feed-forward phase-shift term, Φ^*_{ff}, is added to the output of controller $\mathrm{PI}_{\mathrm{aux}}$. The phase-shift in the range $[-\pi/2, \pi/2]$ as a function of power is given by [121],

$$\Phi(p^*_{\mathrm{aux}}) = \frac{\pi}{2}\left(1 - \sqrt{1 - \frac{8 f_{\mathrm{s,FB1}} L_{\mathrm{aux}} |p^*_{\mathrm{aux}}|}{(1/2 v_{\mathrm{dc,aux}}) \cdot (N_3/N_2 v_{\mathrm{out}})}}\right) \cdot \mathrm{sign}(p^*_{\mathrm{aux}}), \tag{5.6}$$

and is linearized around the nominal operating point ($P_{\mathrm{out}} = 1.5\,\mathrm{kW}$, $P_{\mathrm{aux}} = 20\,\mathrm{W}$) in order to facilitate implementation on the DSC of the hardware prototype,

$$\Phi(p^*_{\mathrm{aux}}) \approx m \cdot p^*_{\mathrm{aux}} + q, \tag{5.7}$$

with parameters m and q listed in Tab. 5.3.

In order to implement the designed controllers on the DSC of the hardware prototype (cf. Section 5.4), $\mathrm{PI}_{\mathrm{out}}(s)$ and $\mathrm{PI}_{\mathrm{aux}}(s)$ were discretized using the Tustin z-transformation with a sample frequency of $F_{\mathrm{ctrl}} = 25\,\mathrm{kHz}$. In addition, the designed PI controllers were augmented with output limitation and anti-windup capability.

5.4 Hardware Prototype

In order to verify the proposed converter topology shown in Fig. 5.2 and assess the performance of the suggested control system, a hardware prototype was realized as will be described in this section. The implemented 380 V/48 V $\mathrm{P^3DCT}$ is depicted in Fig. 5.7. The system is rated for 1.5 kW and exhibits a total volume of $175\,\mathrm{cm^3}$ which corresponds to a power-density of $8.6\,\mathrm{kW/dm^3}$ ($141\,\mathrm{W/in^3}$). Only 10 % – 15 % of the total converter volume is occupied by components related to the PPC. The component parameter values of the realized hardware are listed in Tab. 5.4 and have been obtained from a comprehensive Pareto design optimization, seeking maximum power-density at a minimum target efficiency of around 98 %.

As can be seen from the picture, the converter system is realized by means of two individual power PCBs, the first PCB is equipped with power electronic components of the HV-side (380 V) and the PPC and the second PCB with the power electronics of the LV-side (48 V). In addition, a third dedicated digital control and auxiliary supply board is connected to both power PCBs. In order to extract the losses from the power electronics, both power PCBs are attached to the baseplates of a double-sided forced-air cooled

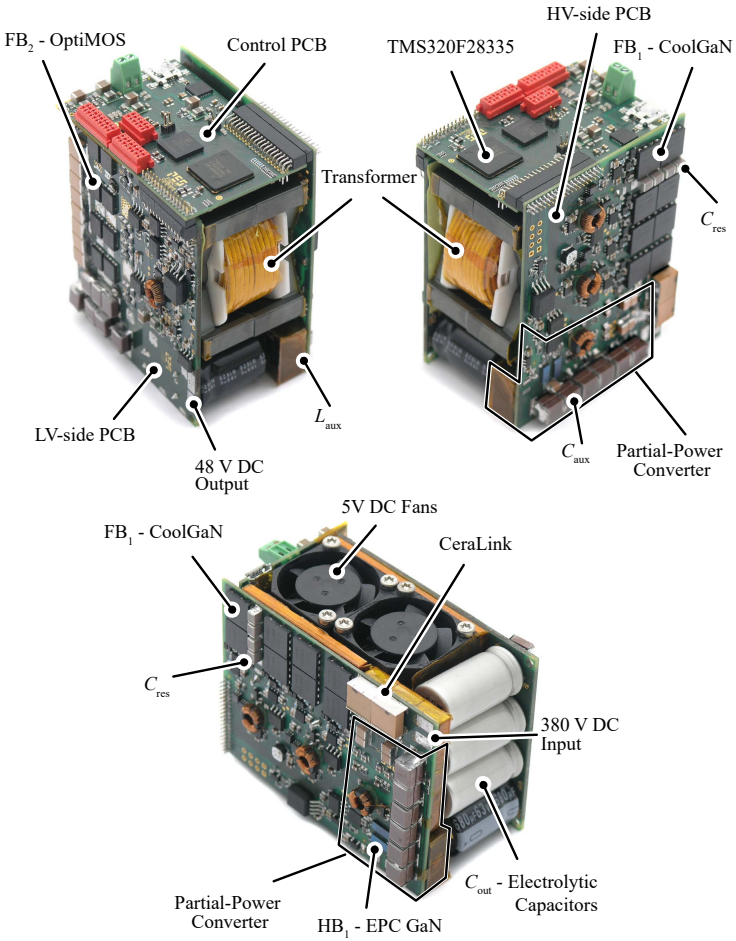


Fig. 5.7: Pictures of the implemented P^{3}DCT hardware prototype taken from different perspectives.

Tab. 5.4: Technical Details of the Implemented P^{3}DCT Hardware Prototype.

	Component	Parameter	Description	Part Number
Power Semiconductors	FB_1	600 V, 70 mΩ Infineon CoolGaN	HV-side full-bridge, 2 transistors in parallel	
	FB_2	60 V, 2.5 mΩ Infineon OptiMOS	LV-side full-bridge, 2 transistors in parallel	BSC028N06NS
	HB_1	100 V, 3.0 mΩ EPC GaN	Transformer-side half-bridge	EPC2022
	FB_3	100 V, 5.6 mΩ EPC GaN	HV-side full-bridge	EPC2001C
	F_s	100 kHz	Switching frequency of FB_1, FB_2, HB_1	
	$F_{s,aux}$	600 kHz	Switching frequency of FB_3	
Transformer & Resonant Tank	Core	PQ 40/40, MnZn ferrite N97	Customized 30 mm height and 100 µm gap	B65883A0000R097
	N_1	31 turns	120 × 71 µm HF-litz wire	
	N_2	4 turns	630 × 71 µm HF-litz wire	
	N_3	2 turns	120 × 71 µm HF-litz wire	
	L_σ	18 µH	Stray inductance of transformer	
	L_m	950 µH	Magnetizing inductance of transformer	
	C_{res}	4 × 33 nF	630 V C0G MLCC	C3225C0G2J333J250AA
Filter Passives	C_{in}	5 × 2 µF	650 V CeraLink	
	C_{aux}	5 × 22 µF	100 V class II/X7S MLCC	CKG57NX7S2A226M500JJ
	L_{aux}	3.0 µH	Coilcraft power inductor 43 A I_{sat}	XAL1580-302
	C_f	14 × 22 µF	100 V class II/X7S MLCC	CKG57NX7S2A226M500JJ
	L_f	150 nH	Inductor 50 A I_{sat}	FP0906R1-R15-R
	C_{out}	3 × 560 µF	63 V Electrolytic capacitor	EGPD630ELL561MK25H
		1 × 680 µF	63 V Electrolytic capacitor	UHW1J681MHD6TN
Cooling System	Length	11 mm	Length of the heat sink	
	Width	50 mm	Width of the heat sink	
	Height	25 mm	Height of the fins	
	Channel Width	0.7 mm	Space between individual fins	
	Baseplate Thickness	4 mm		
	Fan Type	5 V DC Fan	Dimension: 25 mm x 25 mm	MC25060V2-000U-A99

heat sink. The implemented cooling system with 25×25 mm, 5 V DC fans achieves a R_{th} of around 0.49 K/W at a volume of roughly 33 cm^3 which corresponds to a Cooling System Performance Index (CSPI, [122]) of roughly 62 W/(K dm^3). The primary-side full-bridge (cf. FB_1) is realized with 600 V, 70 mΩ E-mode GaN from Infineon, whereby two physical transistors are connected in parallel per switch. The employed gate-drive employs the LM5114 IC and the MAX13256 full-bridge transformer driver IC for galvanic isolation of the high-side supply voltage and is described in detail in [6]. The secondary-side full-bridge (cf. FB_2) is realized with 60 V, 2.5 mΩ OptiMOS from Infineon, also with two physical transistors per switch, and employs the UCC27211A gate-drive IC with bootstrapping supply of the high-side gate voltage. The switching frequency of FB_1 and FB_3 is 100 kHz which corresponds to the natural frequency of the series resonant tank comprised of L_σ, the stray inductance of the transformer, and C_{res}. The employed three-winding transformer, encompassed by the PCBs and cooled by the air-flow exiting the heat sink, is implemented by means of a PQ 40/40, N97 MnZn ferrite core with custom-machined total height of 30 mm. In order to adjust the magnetizing current to achieve Zero Voltage Switching (ZVS) of FB_1, a total air gap of 200 µm is introduced resulting in a magnetizing inductance of 950 µm. HF-litz wire according to the specifications in Tab. 5.4 is used to implement the three windings of the transformer, whereby $N_1 = 31$ and $N_2 = 4$ results in a turns ratio of $n = 7.75$ and $N_3 = 2$ results in a turns ratio of $n_{\text{aux}} = 15.5$. The stacked DC-link capacitors of the PPC, C_{aux}, are assembled from 5×22 µF /100 V MLCCs, and $V_{\text{dc,aux}}$ is regulated to 50 V by means of adjusting the phase-shift between $\text{FB}_{1/2}$ and HB_3. An additional discrete inductor, $L_3 = 3.0$ µH, is added which results in a linearized power-transfer to phase-shift ratio of $\frac{P_{\text{aux}}}{\Phi} \approx 4.795\,\text{W}/^\circ$ (cf. (5.7) and Tab. 5.3). The PPC is designed to process peak powers up to 150 W in order to cope with the specified input voltage range (340 V – 420 V) up to the rated power of the converter. At nominal DC input voltage, $V_{\text{in}} = 380$ V, and 1.5 kW output power, the PPC processes just 20 W which corresponds to a phase-shift of roughly 4.2°. The rectifier half-bridge, HB_3, and the inverter full-bridge, FB_3, of the PPC, are implemented using 100 V E-mode GaN HEMT from EPC in combination with Si8274 gate-drive IC from Silicon Labs. The switching frequency of the inverter is set to $f_{\text{s,aux}} = 600$ kHz. The output filter at the 48 V side of the converter was designed to meet the 100 mV steady-state ripple requirement and confine output voltage deviation during load and input voltage transients to ±500 mV (≈ ±1 % of 48 V). The implemented CLC filter structure (cf. Fig. 5.2) is comprised of 100 V MLCCs at the output of FB_3,

C_f = 308 µF, a subsequent 150 nH inductor and an 2.4 mF output capacitance assembled from individual 560 µF / 63 V aluminum electrolytic capacitors.

The developed control system presented in Section 5.3 was implemented on a TMS320F28335 Digital Signal Controller (DSC) from Texas Instruments Delfino series, located on the designated control PCB. The DSC generates the constant 50 % duty-cycle gate signals for full-bridge FB_1, FB_2 and the phase-shift adjusted half-bridge HB_3 and the varying duty-cycle gate signals for the inverter full-bridge, FB_3. The control board is supplied by means of a 12 V laboratory voltage source and is equipped with 12 V/5 V DC/DC converters (LMZ21701) to provide auxiliary power to the HV and LV power boards. The ground potential of the control board is connected to the DC- rail of the HV full-bridge FB_1 (cf. terminal $\overline{2}$ in Fig. 5.2).

The DC input voltage, V_{in}, is measured by means of a differential amplifier with a corner frequency set to 12 kHz employing the AD8615 operational amplifier from Analog Devices. The 48 V output voltage, V_{out}, is measured by means of a differential amplifier with a corner frequency set to 48 kHz employing the AD8615 operational amplifier. Subsequently, the precision isolation amplifier ACPL-C79B from Broadcom is employed to provide galvanic isolation between control board and LV-side. The output current, I_{out}, is measured with the current sensor ACS722 from Allegro featuring a 80 kHz bandwidth. The DC-link voltage of the PPC, $V_{dc,aux}$, is sensed by means of a differential amplifier with a corner frequency of 30 kHz employing the AD8615 operational amplifier and subsequently the ACPL-C87BT isolation amplifier from Broadcom to provide galvanic isolation between PPC and control board.

5.5 Experimental Results

In this section the experimental measurement results of the implemented P^{3}DCT prototype are presented. First, the performance of the converter system under steady-state conditions is presented and subsequently the effectiveness of the proposed topology and control system is confirmed by step response waveforms. The output voltage is tightly regulated to 48 V and the DC-link of the PPC is regulated to 50 V.

5.5.1 Steady-State Measurements

The waveforms of the P^{3}DCT operating in steady-state at 350 W output power ($P_r/4$) and 380 V nominal input voltage are shown in Fig. 5.8(a) and (b) and at

1.5 kW output power in Fig. 5.9(a) and (b). The high frequency ac waveforms of the converter are shown in Fig. 5.8(a) and Fig. 5.9(a) with a time resolution of 5 µs/division and the DC waveforms are depicted in Fig. 5.8(b) and Fig. 5.9(b) with a time resolution of 5 ms/division. The waveforms are labeled according to the circuit schematic shown in Fig. 5.2. Clearly visible is the superimposed pulse pattern in v_{FB1} and the deviation of current i_1 from its ideal sinusoidal shape which is more pronounced under light load condition. The power processed by the PPC increases from 9 W at 350 W output power to around 20 W at rated output power also indicated by the increased amplitude of i_3. Moreover, the V_{out} voltage ripple requirement of ±100 mV is met as can be inferred from Fig. 5.8(b) and Fig. 5.9(b).

The conversion efficiency of the P^{3}DCT was determined with the Yokogawa WT3000 power analyzer and also considers the 12 V auxiliary and 5 V fan supply power. Fig. 5.10(a) depicts the measured conversion efficiency with respect to output power of the P^{3}DCT (blue line) and the DCT without regulation (red line). The realized P^{3}DCT exhibits an efficiency of 97.7 % at 1.5 kW and shows a peak efficiency of 97.9 % around 1.0 kW. In comparison, the DCT transformer without regulation (PPC disabled and/or bypassed) reaches 98.0 % efficiency at 1.5 kW and a peak efficiency of 98.1 % around 1.0 kW. It must be mentioned, that in case of the unregulated DCT, the input voltage V_{in} was slightly adjusted (3 % maximum deviation from nominal input voltage) to ensure 48 V at the output. It can be concluded that the additional PPC leads to a reduction of efficiency by approximately 0.25 % for an output power above 1 kW and to a reduction of 0.3 % – 1 % in the low output power range. At rated output power, the reduction of 0.25 % in efficiency corresponds to an additional power loss of roughly 3.75 W caused by the PPC assuming that the loss of the DCT is unchanged. The PPC processes around 20 W at the input terminal (cf. $3-\overline{3}$ in Fig. 5.2) in this operating point which results in an estimated efficiency of approximately 82 %. The efficiency with respect to output power for the minimal and maximal specified input voltage, $V_{\mathrm{in}} = 340$ V and $V_{\mathrm{in}} = 420$ V is depicted in red (cross marker) and in yellow (star marker) in Fig. 5.10(b), respectively. Since the PPC processes a larger share of the output power if the input voltage deviates from the nominal 380 V, the overall converter efficiency deteriorates as the PPC exhibits a lower efficiency. At 340 V and 420 V, the overall efficiency at the rated power drops to 96.7 % and 97.13 %, respectively. As discussed in Section 5.2.1, for lower than nominal input voltage the power processed by the PPC only circulates within the system and is not provided to the output which explains why the overall efficiency at $V_{\mathrm{in}} = 340$ V is lower compared to $V_{\mathrm{in}} = 420$ V. Moreover,

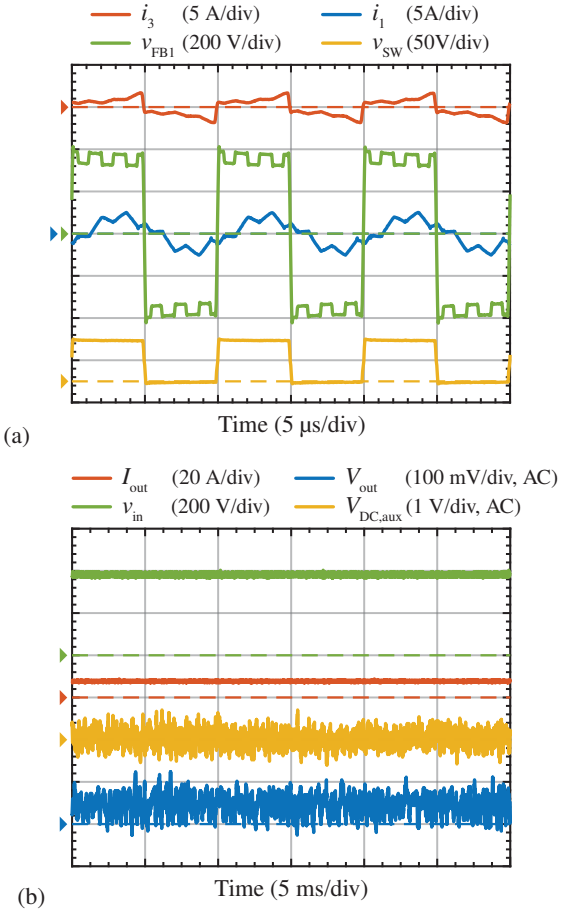


Fig. 5.8: Measured steady-state waveforms of the P^{3}DCT hardware demonstrator operating at a quarter of the output power, $P_r/4 = 350\,\mathrm{W}$. The waveforms of the HF link are depicted in (a) and the DC waveforms are shown in (b). The waveforms are labeled according to the circuit schematic shown in Fig. 5.2.

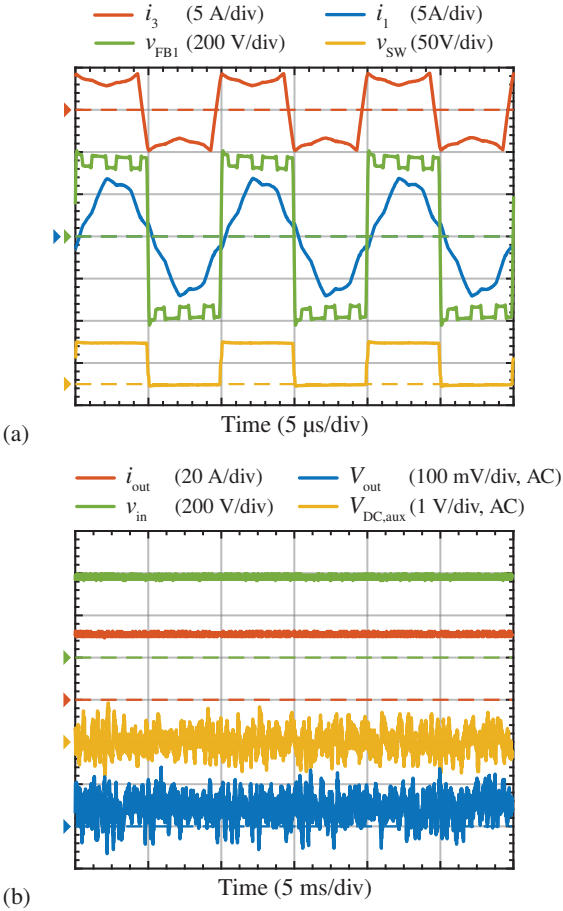
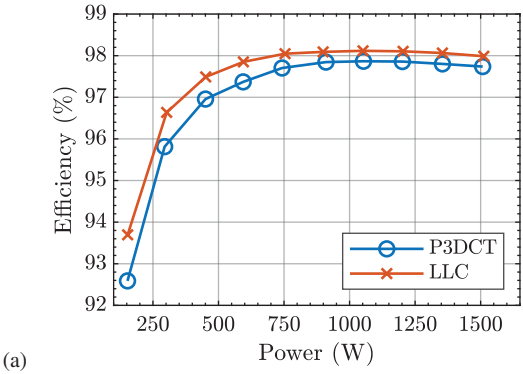
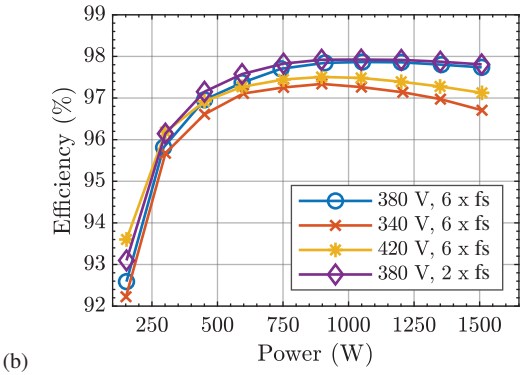


Fig. 5.9: Measured steady-state waveforms of the P^{3}DCT hardware demonstrator operating at rated output power, $P_r = 1.5\,kW$. The waveforms of the HF link are depicted in (a) and the DC waveforms are shown in (b). The waveforms are labeled according to the circuit schematic shown in Fig. 5.2.



(a)



(b)

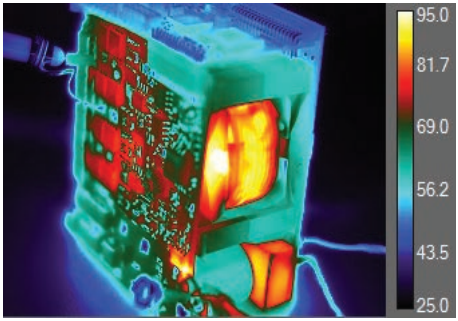
Fig. 5.10: Efficiency of the P^{3}DCT with respect to output power determined with Yokogawa WT3000 power analyzer. (a) shows the efficiency of the P^{3}DCT for nominal input voltage, $V_{\text{in}} = 380\,\text{V}$, opposed to the efficiency of the unregulated DCT (main converter) without PPC. (b) shows the efficiency of the P^{3}DCT with respect to output power for different input voltages and switching frequencies of FB_3 (cf. Fig. 5.2)

the efficiency of the P^{3}DCT with inverter full-bridge FB_3 operating at only 200 kHz (only twice the DCT switching frequency,F_s) is depicted in purple (diamond marker). It can be seen that the overall efficiency marginally improves, most notably at light load conditions. The infrared (IR) images in Fig. 5.11 show the steady-state temperature distribution of the P^{3}DCT operating at 1.5 kW output power with 100 W being processed by the PPC. The captured temperature distribution of the converter with the LV-side and HV-side fac-

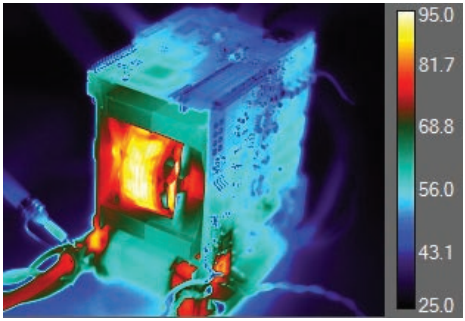
ing the IR camera is depicted in Fig. 5.11(a) and (b), respectively, and reveals that permanent operation at rated power can be sustained by the realized hardware. It can be seen that the maximum measured surface temperature of 95 °C is attained by the transformer winding. The LV-side power transistors (OptiMOS) and the rectifier of the PPC attain a steady-state temperature of around 80 °C. The HV-side power transistors (CoolGaN) and the inverter of the PPC exhibit a surface temperature in the 60 °C range.

5.5.2 Step Response Measurements

In order to assess the performance of the converter with proposed control system, stepwise input voltage and output load variations were applied. The output load was adjusted with a Chroma 63202 electric load and the input voltage steps were applied using a Xantrex XDC 600-10 DC supply. The current and voltage slew-rates of the electronic load and of the DC supply were set to their maximum supported values for the conducted step response experiments. Figs. 5.12(a) and (b) depict the output voltage and PPC DC-link voltage of the P^{3}DCT subject to a stepwise change of output load between 0 W and 750 W. Likewise, the response to a stepwise change of output load between 750 W and 1.5 kW is shown in Fig. 5.13(a) and (b). It can be seen from the measurements, that stepwise load changes up to half the rated power are causing a V_{out} deviation of less than ±500 mV ($\approx$ ±1 % of 48 V) which is eliminated by the control in less than approximately 5 ms. The deviation in DC-link voltage, $V_{\text{dc,aux}}$, remains within ±3 V and settles within 3 ms. The responses of the P^{3}DCT subject to a 50 V stepwise change in input voltage amplitude between 350 V and 400 V are shown in Fig. 5.14 and Fig. 5.15, whereby in Fig. 5.14(a) and (b) the input voltage steps are performed at 750 W output power and in Fig. 5.15(a) and (b) at 1.5 kW output power. It can be seen from the experimental waveforms, that the maximum V_{out} deviation resulting from input voltage steps with 50 V magnitude is also around ±500 mV and settles in less than approximately 8 ms. The deviation in DC-link voltage, $V_{\text{dc,aux}}$, remains within ±7 V and settles within 8 ms. Note that because of the limited current sink capability of the employed DC supply, the input voltage slope is mainly governed by the actual load of the converter which explains the different slew rates in Fig. 5.15(a) and (b), and consequently there is an undershoot of roughly 20 V present in V_{in}.



(a)



(b)

Fig. 5.11: Steady state infrared image of the P^{3}DCT operating at 1.5 kW output power. The PPC processes 100 W in the selected operating point. The low-voltage side of the converter facing the IR camera is shown in (a) and the high-voltage side in (b).

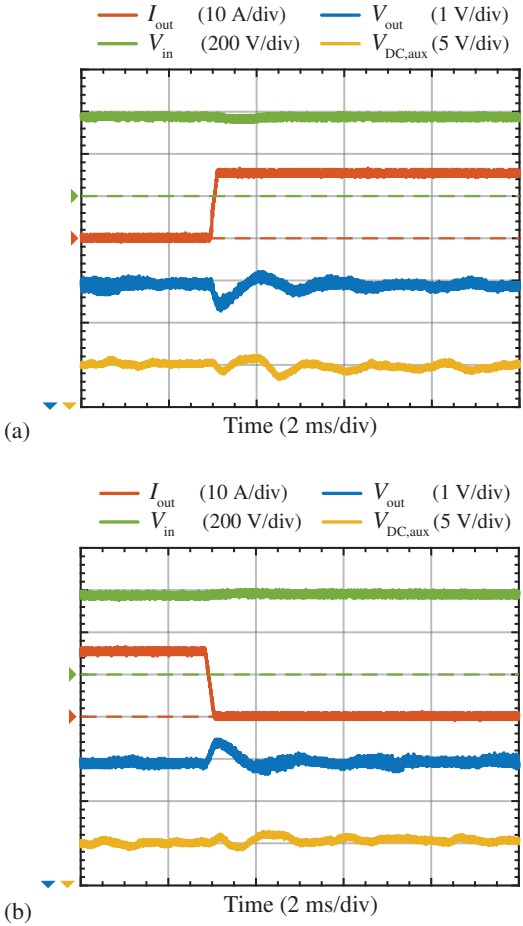
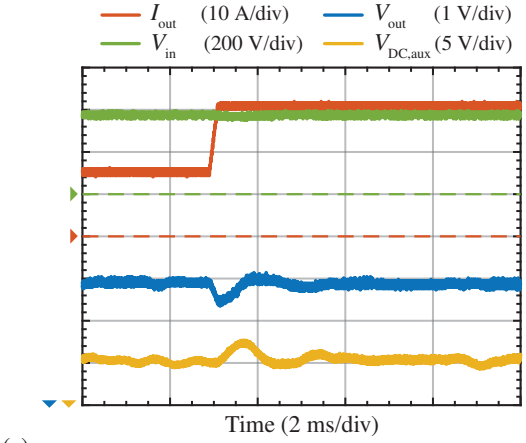
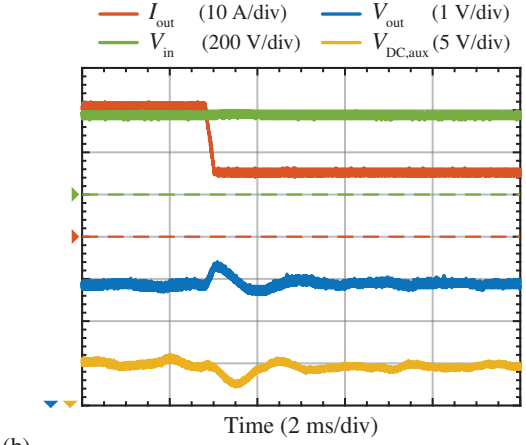


Fig. 5.12: Measured output voltage V_{out} and PPC DC-link time behavior of the P^{3}DCT hardware demonstrator subject to a stepwise output load change between 0 W and 750 W shown in (a) and (b). The waveforms are labeled according to the circuit schematic shown in Fig. 5.2.



(a)



(b)

Fig. 5.13: Measured output voltage V_{out} and PPC DC-link time behavior of the P^{3}DCT hardware demonstrator subject to a stepwise output load change between 750 W and 1.5 kW shown in (a) and (b). The waveforms are labeled according to the circuit schematic shown in Fig. 5.2.

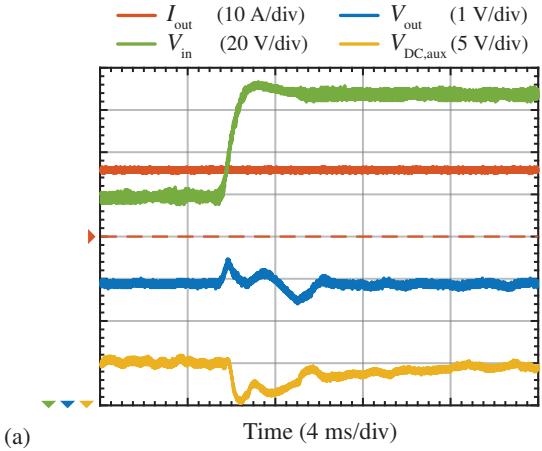


Fig. 5.14: Measured output voltage V_{out} and PPC DC-link time behavior of the P^{3}DCT hardware demonstrator subject to a stepwise change of the input voltage V_{in} between 350 V and 400 V for 750 W output power. The waveforms are labeled according to circuit schematic in Fig. 5.2.

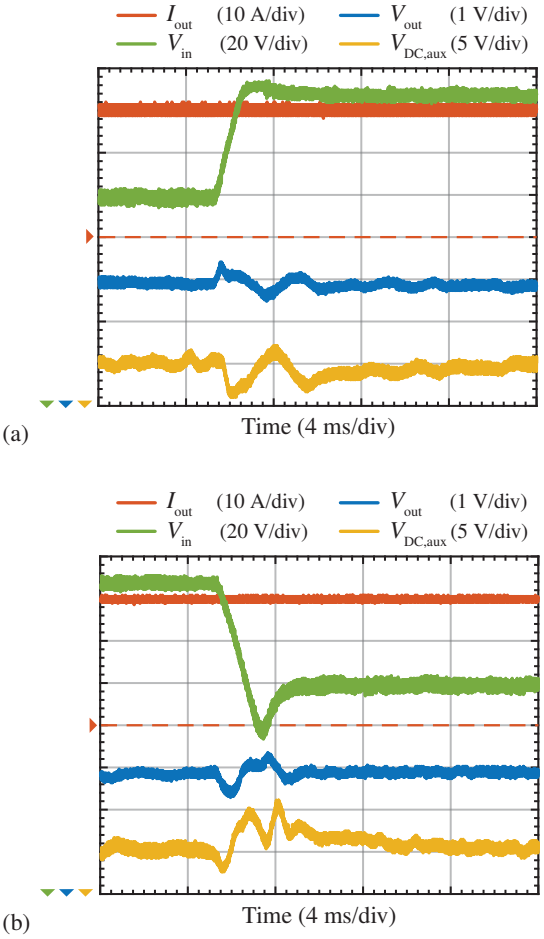


Fig. 5.15: Measured output voltage V_{out} and PPC DC-link time behavior of the P^{3}DCT hardware demonstrator subject to a stepwise change of the input voltage V_{in} between 350 V and 400 V for 1.5 kW output power. The waveforms are labeled according to circuit schematic in Fig. 5.2.

5.6 Summary

In this chapter a novel approach to realize a compact, high efficiency 380 V to 48 V DC/DC converter with output voltage regulation was presented. A main DC/DC converter, implemented by means of an unregulated resonant LLC converter operating as DC transformer (DCT), is accompanied by a partial-power auxiliary converter (PPC) dedicated to tightly regulate the output voltage by means of adjusting the average input voltage of the main converter. Taking advantage of the transfer characteristic of the DCT, a filter-less implementation of the PPC was proposed where the pulse-width modulated auxiliary DC-link voltage is superimposed to the DC input voltage of the main converter. Since the PPC processes only a fraction of the rated power, the overall efficiency is only marginally affected. A prototype of the proposed converter rated at 1.5 kW was implemented and specified to cope with input voltage variations between 340 V – 420 V. The hardware demonstrator features an overall conversion efficiency of 97.7 % at rated power and a power-density of 8.6 kW/dm^3. The performance of the partial-power regulator with proposed control system was assessed by means of input voltage and load step responses. A stepwise change of half the rated output power (750 W) and a 50 V stepwise variation of the input voltage are causing an output voltage deviation of less than ±500 mV which is settled within 8 ms. Adding output voltage control to an unregulated, series-resonant LLC DC/DC converter by means of a PPC adds roughly 10 % of volume to the converter while reducing the overall efficiency by 0.3 %.

6

Origin and Quantification of Increased Core Loss in MnZn Ferrite Plates of a Multi-Gap Inductor

Chapter Abstract

Inductors realized with highly permeable MnZn ferrite magnetic core require, unlike to iron-powder cores with an inherent distributed gap, a discrete air gap in the magnetic circuit to prevent saturation of the core material and/or tune the inductance value. This large discrete gap can be divided into several partial gaps in order to reduce the air gap stray field and consequently the proximity losses in the winding. The multi-gap core, realized by stacking several thin ferrite plates and inserting a non-magnetic spacer material between the plates, however, exhibits a substantial increase in core losses which cannot be explained from the intrinsic properties of the ferrite. A new calorimetric measurement setup based on temperature rise monitoring is proposed in this chapter in order to quantify and differentiate between core losses associated with the bulk and the surface of the ferrite plates and therefore to pinpoint the measured excess core loss to shallow layers of ferrite with deteriorated magnetic performance. By means of the proposed measurement technique, the bulk and surface core loss density of the MnZn ferrite material 3F4 from FerroxCube was determined for sinusoidal flux density amplitude varying from 75 mT up to 200 mT and excitation frequencies ranging from 200 kHz to 1 MHz. The measured core loss densities (W/cm^3) show good agreement with the Steinmetz model provided by the manufacturer validating the proposed calorimetric core loss measurement technique. The measured surface loss density (W/cm^2) can also be well predicted with a Steinmetz model, whereby the frequency exponent α in the surface is slightly smaller and the flux density exponent β is slightly larger compared to the Steinmetz parameter of the bulk ferrite. It is shown that the ratio between surface and bulk core losses of a composite core assembled from individual plates is only a function of plate thickness and does not depend on the actual cross section area. A critical plate thickness is then defined to be reached when the total power loss in the composite core has doubled compared to a solid (single-piece) core sample. This new quantity provides a very helpful figure for multi-gap inductor designs.

6.1 Introduction

In high power-density converter systems, the switching frequency is increased substantially in order to strongly reduce the required inductance value and the volume of the employed power inductor. Very compact input inductors of PFC rectifiers and output inductors of inverters or DC/DC converters also feature a high current ripple which demands for suitable core materials – at high frequencies preferable ferrite – and sophisticated inductor designs in order to keep the core and winding losses to a minimum. Inductors realized with highly permeable ferrite materials require, unlike iron-powder cores with an inherent distributed gap, a discrete air gap in the magnetic circuit to prevent saturation of the core material and/or tune the inductance value. This large discrete air gap can be divided into several partial gaps in order to reduce the air gap fringing field and consequently the proximity losses in the winding, especially if copper foil is used to implement the winding (cf. Fig. 6.1(a) and (b)). If the partial gaps are distributed over the entire length of the inner limb of an E-type core, the H-field in the winding window shows a quasi one-dimensional field distribution running in parallel to the inner limb [28–30]. This allows to implement the winding with copper foil which achieves a higher filling factor compared to HF litz wire, since the individual layers of the foil winding are aligned in parallel with the H-field and excessive eddy current losses can be avoided.

Following this idea, ETH Zurich together with Fraunhofer Institute for Reliability and Microintegration (IZM) and Fraza company developed compact multi-gap foil winding inductors to realize a $8.2\,\mathrm{kW/dm^3}$ ($134\,\mathrm{W/in^3}$) single-phase, full-bridge based inverter for the GOOGLE Little Box Challenge (GLBC). In order to achieve soft-switching throughout the mains period, Triangular Current Mode (TCM) modulation was employed resulting in a variable switching frequency in the range of 200 kHz – 1 MHz for an inductance value of 10.5 µH. Further information regarding the hardware implementation of the so called Little Box 1.0 is provided in Chapter 4. A photograph of the realized inductor with the dimensions $14.5\,\mathrm{mm} \times 14.5\,\mathrm{mm} \times 22\,\mathrm{mm}$ is shown in Fig. 6.1(c). The inner limb of the inductor is composed of $24 \times 0.6\,\mathrm{mm}$ thick stacked ferrite plates with 80 µm partial air gaps between the plates, resulting in a total air gap length of 1.92 mm. The inner limb is surrounded by the foil winding with a total of 16 turns, where each turn is composed of four parallel 20 µm thin copper foils which are mutually isolated with a 7 µm thin layer of Kapton. Furthermore, a sophisticated winding arrangement is used as shown in Fig. 6.1(b), which forces the current to flow evenly distributed

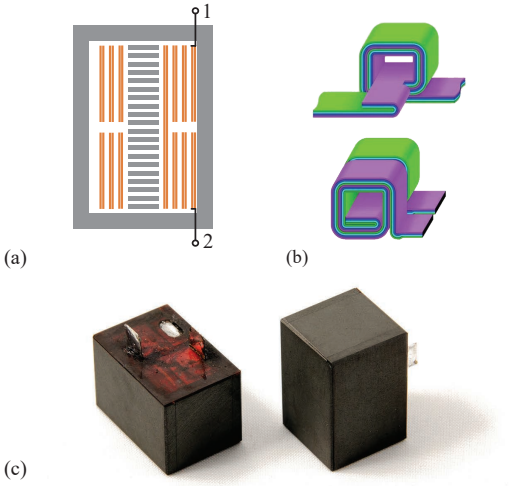


Fig. 6.1: (a) Structure of the foil winding multi-gap inductor with the center limb of the E-type core being composed of stacked ferrite plates. (b) Foil winding arrangement to achieve equal current sharing in parallel foils (shown for 2 parallel foils) which has both connection terminals at the outside of the winding [98, 123]. (c) Hardware photograph of the realized 10.5 µH multi-gap HF inductor employed in the Google Little Box Challenge converter (Little Box 1.0) [75].

Tab. 6.1: Technical Data of the Multi-Gap Foil Winding Inductor.

Inductance	10.5 µH
Quality factor	≈ 600 between 200 kHz – 1000 kHz
R_{AC}	14 mΩ – 120 mΩ between DC – 1 MHz
Dimension	$(14.5 \times 14.5 \times 22)\,\mathrm{mm}^3$
Foil Winding	2×8 turns 4 parallel 20 µm copper foils 7 µm Kapton layer isolation
Core	MnZn ferrite DMR 51 / DMEGC 24×80 µm air gaps 0.61 mm thick stacked plates $(6.6 \times 9.6 \times 17.5)\,\mathrm{mm}^3$ center limb dimension

in all four parallel copper layers, thus counteracting the skin and proximity effect [98–100, 123]. Moreover, the arrangement features both connection terminals at the outside of the winding where the magnitude of the H-field in the winding window is small, reducing losses caused by the termination of the foil winding, where it is difficult to keep the copper foil aligned with the H-field, to a minimum. The used core material is DMR 51 from the manufacturer DMEGC, a MnZn ferrite optimized for the frequency range of 1 MHz – 2 MHz (similar in performance to 3F4 from Ferroxcube or PC200 from TDK).

All technical specifications of the multi-gap inductor are summarized in Tab. 6.1 and impedance analyzer measurements are presented in Fig. 6.2. It can be seen that the implemented multi-gap foil winding inductor exhibits an excellent quality factor of 600 – 700 between 200 kHz – 1 MHz and a high resonance frequency of around 7.2 MHz.

Unfortunately, experimental measurements at an early stage of development of the Little Box 1.0 revealed substantially higher power loss in the inductors than expected. By means of core loss measurements and thermographic inspection, the origin of additional losses could be attributed to the stacked ferrite plates constituting the center limb of the core. For this reason, the number of partial gaps was reduced from initially 50 to just 24 in the final inductor design (cf. Tab. 6.1). Upon consultation of scientific literature and further experimental investigation, four main reasons for the increased core losses were identified:

- Formation of deteriorated ferrite layers at the plate surfaces due to mechanical stress introduced during machining.

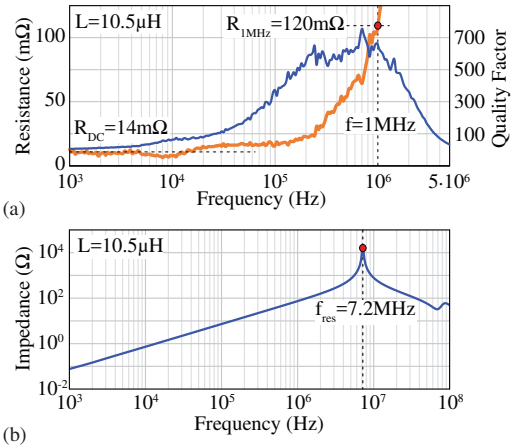


Fig. 6.2: Small-signal impedance analyzer measurements with Agilent 4294A of the multi-gap inductor depicted in Fig. 6.1(c). (a) Winding resistance and quality factor with respect to frequency. (b) Impedance with respect to frequency.

- Flux crowding in the multi-gap core due to tolerances and imperfections in machining and assembly (Appendix A.1).
- Deterioration of ferrite properties due to pressure buildup in the stack of plates during the curing of the employed epoxy resin [31].
- Ohmic loss in the ferrite associated with the current flowing in the conduction path provided by the low impedance of the ferrite material at high frequencies and the parasitic capacitance between the outer layer of the foil winding and the ferrite [31].

For the sake of brevity, only the surface loss related mechanism will be addressed in detail in this chapter since it is by far the most significant contributor to the excess core loss. However, the interested reader is referred to Appendix A where the impact of flux crowding due to assembly and machining tolerances on the core losses is analyzed, and to [31] where the impact of epoxy curing related pressure buildup and the parasitic winding-core capacitance on the core losses is discussed. The main scientific contribution of this work is an experimental method which allows to differentiate between core losses associated with the bulk and the surface of the ferrite plates required to implement the multi-gap inductor design and thus to pinpoint the measured

excess core loss to shallow surface layers of ferrite with deteriorated magnetic performance as suspected in scientific literature dating back to the '70s. Moreover, the proposed technique allows to assess modern ferrite materials regarding their applicability in multi-gap inductor designs.

In Section 6.2 of this chapter the most important analyses and findings shown in literature regarding the impact of mechanical processing such as cutting and grinding on the magnetic properties of ferrite are summarized and a microstructural analysis of the machined ferrite surface is presented. In Section 6.3, mathematical expressions are derived to quantify core and surface loss densities from experimental temperature rise measurements using multi-gap core samples assembled from machined ferrite plates with distinct thicknesses. Moreover, the employed experimental setup based on Infrared (IR) thermometry is outlined. The proposed technique is then applied to characterize the MnZn ferrite material 3F4 at several peak flux densities and frequency values, that is to say at operating points $\{\hat{B}, f\}$ which resemble the Google Little Box Challenge application. The obtained experimental findings are presented in Section 6.4 and subsequently discussed in Section 6.5 where the ratio between bulk and surface core loss is illustrated. Section 6.6 concludes the chapter and provides an outlook for future research.

6.2 Machining-Induced Increase of Core Loss

The correct dimensions of ferrite plates or cuboidal pieces needed to implement a multi-gap core are typically not off-the-shelf available and must be machined from a larger ferrite piece. One option is to cut the plates from a long sintered ferrite bar using a precision saw as depicted in Fig. 6.3(a). Since ferrite is a very hard and brittle ceramic, the saw must be equipped with a diamond blade (SiC is too soft). As a consequence of the cutting process with the abrasive diamond particles, a mechanical stress is introduced into the ground surface of the plate. As will be summarized in the following, it is claimed in the scientific literature that the exerted mechanical stress is deteriorating the magnetic properties of the ferrite in a thin layer just underneath the surface resulting in an increase of overall core loss (cf. Fig. 6.3(b)).

The first investigations regarding the impact of mechanical stress on the properties of ferrite were conducted by E. Stern and D. Temme back in 1964 [124]. They observed that mechanical pressure applied to a toroidal core changes the remanent magnetization, coercive force, and the shape of the BH-loop. They also claimed that compressive stress can result from abrasive machining and predominantly affects the ferrite close to the machined surface.

Investigating several materials such as Garnet, NiZn and MgMn ferrite, Stern and Themme concluded that only magnetostrictive core materials are strongly affected by mechanical stress.

In 1970 John E. Knowles investigated how uniaxial stress affects the initial permeability - temperature curve, $\mu_i(T)$, of MnZn ferrite with different MnO/ZnO ratios [125]. Knowles compared the $\mu_i(T)$ curve of sintered and ground toroid core samples and learned that the permeability of the machined toroids (abrasion with a belt grinder or sandpaper) was lowered at high temperatures and raised at lower temperatures resulting in a sharp bend in the $\mu_i(T)$ curve and that the samples with higher MnO/ZnO-ratio were more sensitive. Knowles argued that the immense local pressure exerted during the grinding process caused a compressive stress in the surface layer and, consequently, a tensile stress in the interior of the ferrite. He further argued that it was hence possible for the compressed surface to influence the

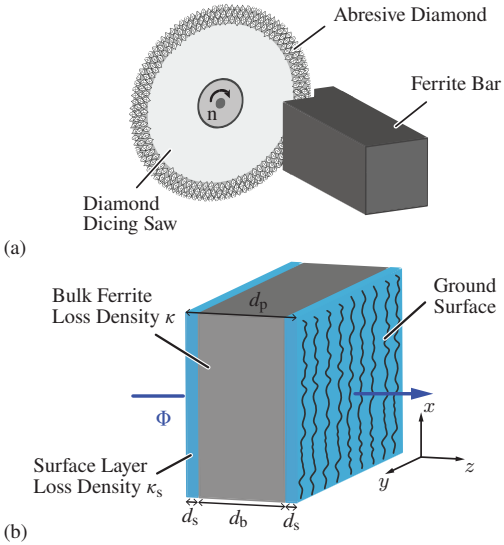


Fig. 6.3: (a) Cutting thin ferrite plates or cuboidal pieces from a long bar using a precision saw equipped with a diamond blade. (b) Abrasive machining causes residual mechanical stress in the ground surface; the magnetic properties of ferrite are degraded in these shallow layers and feature a much higher core loss density as opposed to the ferrite with intrinsic properties in the bulk of the plate.

magnetic properties of the bulk ferrite. However, how much the properties of the bulk are affected depends on the exerted stress in the interior of the ferrite which is a function of geometry and size. In a follow-up publication in 1974, Knowles found that the loss factor, $\tan\delta/\mu$, of a ferrite pot core at 100 kHz increased by up to 33 % after machining the mating and air gap surfaces with a diamond-wheel precision grinding machine [126]. Knowles experimentally determined that the grinding process causes a very large residual compressive stress in the surface layer with magnitude of up to 700 MN/m^2 (almost the ultimate compressive stress of the material) reducing almost linearly towards the interior of the sample, becoming negligible at a depth of 5 µm below the surface. In his experiment, Knowles waxed a thin ferrite plate which was initially machined at both sides to a support and then polished one side with colloidal silica suspension and a soft cloth to give a surface which is known to be essentially "free from stress". When released from the substrate, the slice adopted a curvature, showing that the machined face of the plate was in compression. In another experiment, Knowles applied manually a pressure to both flat faces of a toroidal core in order to investigate the dependency of the loss factor, permeability and coercitive force on the compressive stress in the ferrite. Based on the results, Knowles estimated that the average loss factor of the ground surface is roughly 350 times larger than the intrinsic loss factor of the examined MnZn ferrite material.

The magnetic properties of a ferrite rod subject to tensile and compressive stress were also studied by E. C. Snelling [127]. Snelling applied either a tensile or compressive stress and recorded the permeability, the residual and hysteresis loss factor and the coercitivity of the MnZn ferrite sample. In close agreement with Knowles, Snelling observed that above 30 °C tension reduces the permeability and compression increases it and below about −10 °C the opposite is true. Snelling could also show that for both compressive and tensile stress, the residual and hysteresis loss factors increase.

Kloholm et al. determined the magnetostrictive response of thin MnZn and NiZn ferrite plates (1 cm×4.2 cm×90 µm) as the applied magnetic field was decreased from saturation to magnetic remanence [128]. Additional abrasion of one side of the ferrite specimen with 180 grit SiC polishing paper caused a marked increase in magnetostrictive response of the sample, indicating that a deteriorated ferrite layer is formed underneath the machined surface. By knowing the magnetostriction constant of the investigated materials, Klokholm et al. estimated that the thickness of the deteriorated layer is approximately 40 µm - 50 µm in case of the MnZn ferrite and around 90 µm - 100 µm in the investigated NiZn ferrite.

The influence of machining on the properties of ferrite has also been studied extensively with respect to magnetic storage systems. NiZn and MnZn ferrite ceramics are widely used as recording head materials and are finished to a high degree of precision by diamond grinding and lapping. The finished ferrite surface is found to have a shallow magnetically inactive layer causing recording head performance to deteriorate [129–131].

For the sake of completeness it should furthermore be noted, that recently [132–134] reported that the cutting process has also a substantial influence on the ferromagnetic material properties of steel sheets used to manufacture laminated iron cores for electric machines.

6.2.1 Microanalysis of MnZn Ferrite Surface

From the review of the scientific literature it can be concluded that ferrite is extremely sensitive to mechanical stress and that machining likely deteriorates the magnetic properties. In order to find structural evidence of a deteriorated layer close to the surface and assess the surface condition of the machined MnZn ferrite plates, a Scanning Electron Microscopy (SEM) analysis was performed and the results are depicted in Fig. 6.4. In Fig. 6.4(a) the surface with clearly visible individual grains of a sintered MnZn ferrite sample (3F4) is shown where no subsequent (i.e. after sintering) machining process was applied. In contrast, the ground surface as a result of cutting the plate from a long ferrite bar with a diamond saw is depicted in Fig. 6.4(b), showing deformed grains and grooves formed by the abrasive diamond particles. In order to assess the morphology of the ferrite underneath the surface, Focused Ion Beam (FIB) milling was performed as shown in Fig. 6.4(c) to expose the bulk ferrite material. The close-up view in Fig. 6.4(d) clearly indicates micro cavities and cracks roughly 5 µm – 10 µm below the surface. Fig. 6.4(e) depicts the plate surface after removing roughly 500 µm of material by means of abrasive polishing with SiC grinding paper and gradually decreasing the grain size from 22 µm down to 5 µm, using water as a lubricant. The last polishing step was performed with colloidal silica suspension with a grain size of 60 nm and a soft polishing cloth. Fig. 6.4(f) depicts the lateral view (i.e. orthogonal to the machined surface) of the ferrite sample embedded in a Bakelite support after removing roughly 1 mm of material to expose the bulk. From Fig. 6.4(e) and (f) it becomes clear that the cavities and cracks identified in Fig. 6.4(c) are not caused by mechanical stress exerted during cutting, but are the result of imperfections in the sintering of the MnZn ferrite. It should be noted that this is not vendor but rather process or technology specific,

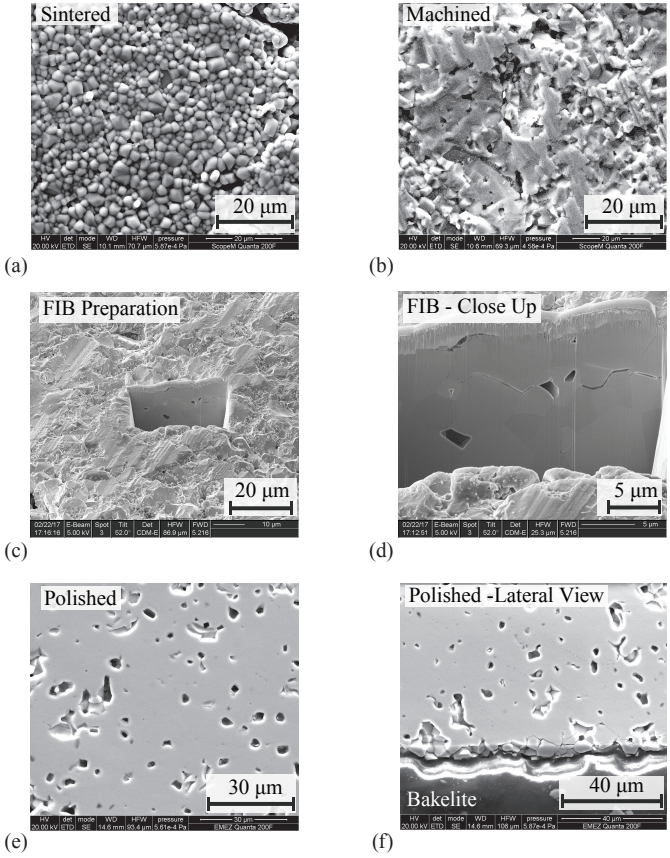


Fig. 6.4: Scanning Electron Microscopy (SEM) images of MnZn ferrite samples. (a) Surface of a ferrite plate after sintering (no machining). (b) Surface of a plate cut from a long ferrite bar with a diamond blade (c) Focused Ion Beam (FIB) milling to expose bulk material underneath surface (d) Close-up of the FIB prepared sample revealing cracks and cavities underneath surface. (e) Plate surface after removing roughly 500 µm of ferrite by means of polishing, gradually reducing grain size of SiC paper and surface finish with colloidal silica suspension and soft cloth. (f) Lateral view of plate embedded in Bakelite support after polishing.

since the same cavities and cracks were also visible in ferrite samples from other vendors.

However, the presented SEM microanalyses did not reveal any structural abnormality which would allow to actually pinpoint the excess core loss to shallow layers of ferrite with deteriorated magnetic performance as suspected in literature. Therefore, an experimental approach is derived in the following which allows to differentiate between core losses associated with the bulk and the surface of the examined ferrite plates.

6.3 Quantification of Surface Losses

The nonlinear characteristics of magnetic core materials require large-signal measurements to determine core losses accurately. It is a common technique to experimentally measure core losses for sinusoidal excitation of different amplitudes and frequencies and then obtain the parameters of the well known Steinmetz Equation (SE),

$$p = k f^{\alpha} \hat{B}^{\beta} \ (\mathrm{mW/cm^3}), \tag{6.1}$$

by means of least-mean-square regression. Using the SE with identified parameters k, α and β then allows to accurately predict core losses for a limited flux density and frequency range.

Considering again a ferrite plate with cross section A_p and thickness $d_\mathrm{p} = 2d_\mathrm{s} + d_\mathrm{b}$ as shown in Fig. 6.3(b), where d_s and d_b are the thicknesses of the deteriorated layers at the plate surfaces and the bulk ferrite with intrinsic properties, respectively. To keep the derivation simple, it is assumed that there is a strict separation of surface layer and intrinsic material and that these segments exhibit a strictly cuboidal shape as indicated in Fig. 6.3(b). It then follows that for homogenous flux density, ensured by the excitation circuit described in Section 6.3.2, the total core losses in the ferrite plate are given by

$$\begin{aligned} P_\mathrm{l} &= \underbrace{k f^{\alpha} \hat{B}^{\beta}}_{\kappa} \underbrace{d_\mathrm{b} A_\mathrm{p}}_{\mathrm{Vol}_b} + \underbrace{k_\mathrm{s} f^{\alpha_\mathrm{s}} \hat{B}^{\beta_\mathrm{s}}}_{\kappa_\mathrm{s}} \underbrace{2 d_\mathrm{s} A_\mathrm{p}}_{\mathrm{Vol}_s} \\ &= (\kappa \cdot d_\mathrm{b} + \kappa_\mathrm{s} 2 d_\mathrm{s}) A_\mathrm{p} = \left(\kappa + \kappa_\mathrm{s} \frac{2 d_\mathrm{s}}{d_\mathrm{b}} \right) d_\mathrm{b} A_\mathrm{p} \\ &\approx \left(\kappa + \kappa_\mathrm{s} \frac{2 d_\mathrm{s}}{d_\mathrm{p}} \right) d_\mathrm{p} A_\mathrm{p}, \end{aligned} \tag{6.2}$$

wherein $d_\mathrm{p} = d_\mathrm{b} + 2d_\mathrm{s} \approx d_\mathrm{b}$ is the fair assumption that the thickness of the surface layer is negligible compared to the thickness of the bulk.

It is presented in the following, how a calorimetric measurement approach can be applied to experimentally determine both bulk and surface loss densities of a multi-gap core assembled from thin ferrite plates. The technique is based on determining core losses in ferrites by means of precise temperature rise monitoring as reported in [135, 136].

A second experimental method based on electrical core loss measurements using ferrite samples with a distinct number of gaps is discussed in Appendix A.2. Since the calorimetric method fully excludes the loss of the test circuit required to adjust the magnetic excitation and therefore allows to capture the power loss in the sample directly, it features a significantly lower measurement error and is therefore the preferred choice in this study.

6.3.1 Linear Thermal Model

The power loss in the core given in (6.2) during continuous operation causes naturally a temperature rise of the ferrite plate over time which can be modeled by a lumped thermal network considering one-dimensional heat flow as shown in Fig. 6.5(a), wherein lumped parameters $C_\mathrm{th,s}$ and $C_\mathrm{th,b}$ capture the thermal capacitance of the surface layer and bulk material, respectively, and $R_\mathrm{th,b-s}$ models the virtual thermal resistance of the bulk-surface interface. Since the loss density in bulk and surface layer is homogeneous and a plate features a comparably low thermal conductivity towards ambient at its thin lateral faces in x, y-direction, i.e. $R_\mathrm{th,b-a} \to \infty$, it is sufficient to consider a strict one-dimensional heat flow in pos. and neg. z-direction (i.e. normal to the plate surface; cf. Fig. 6.3(b)). The power loss in bulk and surface region is captured with distinct current sources (cf. $\kappa d_\mathrm{b} A_\mathrm{p}$ and $\kappa_\mathrm{s} d_\mathrm{s} A_\mathrm{p}$) and a heat transfer to ambient in z-direction is taken into consideration with $R_\mathrm{th,s-a}$. Due to symmetry, the network can be simplified as shown in Fig. 6.5(b). As will become evident from the thermography images provided in Section 6.3.2, the thermal conductivity of the MnZn-ferrite (cf. Tab. 6.2) is sufficiently large to support a homogenous temperature distribution within the plate, i.e. $R_\mathrm{th,b-s} \to 0$. Accordingly, it is sufficient to consider the simplified first order thermal network with lumped parameters $R_\mathrm{th,p}$ and $C_\mathrm{th,p}$ as shown in Fig. 6.5(c), where the total dissipated power is combined in a single current source.

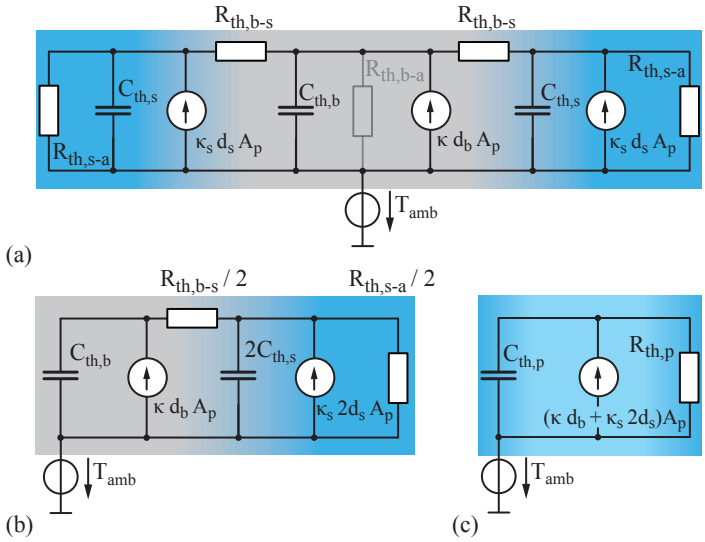


Fig. 6.5: (a) Thermal network of the ferrite plate considering one-dimensional heat flow in pos. and neg. z-direction (cf. Fig. 6.3(b)); lumped parameters $C_{\mathrm{th,s}}$ and $C_{\mathrm{th,b}}$ capture the thermal capacitance of the surface layer and bulk material, respectively, and $R_{\mathrm{th,b-s}}$ models the thermal resistance of the bulk-surface interface. The power loss in bulk and surface region is captured with distinct current sources $\kappa d_{\mathrm{p}} A_{\mathrm{p}}$ and $\kappa_{\mathrm{s}} d_{\mathrm{s}} A_{\mathrm{p}}$, and the transfer of heat to ambient is taken into consideration with $R_{\mathrm{th,s-a}}$ and $R_{\mathrm{th,b-a}}$. (b) Simplification of the circuit due to symmetry and neglecting heat transfer from bulk to ambient ($R_{\mathrm{th,b-a}} \to \infty$). (c) The thermal conductivity of ferrite is high enough to support a homogenous temperature distribution within the plate, further simplifying the thermal network.

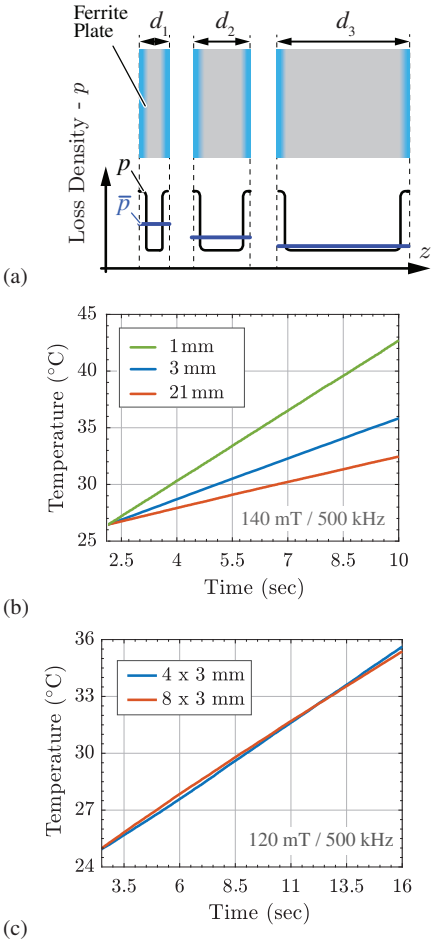


Fig. 6.6: (a) A thin plate (d_1) is more governed by the characteristics of the surface layer and features a higher avg. loss density, $\overline{p}$, as opposed to a fairly thick plate (d_3) which approaches the loss density of the bulk ferrite. (b) Experimental temperature rise measurement showing that a sample assembled from 1 mm plates results in a much steeper slope compared to 3 mm plates or the single-piece (21 mm) reference sample. (c) Experimental measurement showing that the slope of the temperature rise is not affected by the actual height of the stack (i.e. number of plates in the stack).

It follows from (6.2) that the average loss density in a plate of thickness d_p is given by

$$\overline{\kappa} = {}^{P_\mathrm{l}}/_{d_\mathrm{p} A_\mathrm{p}} = \kappa + \kappa_s {}^{2d_s}/_{d_\mathrm{p}}. \tag{6.3}$$

Thus, based on the hypothesis that the loss density is larger in the surface layer than in the bulk, the average loss density increases inverse proportional with the thickness of the plate. As illustrated in Fig. 6.6(a), a thin plate (d_1) is more governed by the characteristics of the surface layer and features a higher avg. loss density as opposed to a fairly thick plate (d_3) which approaches the loss density of the bulk ferrite.

If the heat transfer to ambient is negligible by means of sufficient thermal insulation (i.e. $R_{\mathrm{th,p}} \longrightarrow \infty$ in Fig. 6.5(c)), the temperature of the plate increases linearly over time,

$$T(t) = \frac{P_\mathrm{l}}{C_{\mathrm{th,p}}} \cdot t + T_\mathrm{amb}, \tag{6.4}$$

Tab. 6.2: Technical Details and Material Parameter.

Param.	Value	Unit	Description
A_p	7×6.4	mm^2	Cross section area of plate / sample
λ_m	0.154	W K/m	Thermal conductivity of Mylar
λ_fe	3.5 – 5	W K/m	Thermal conductivity of MnZn ferrite
$R_{\mathrm{th,b}}$	13 – 20	K/W	Thermal resistance of a 3 mm MnZn ferrite plate
$R_{\mathrm{th,m}}$	14.9	K/W	Thermal resistance of a 100 µm Mylar foil
$C_{\mathrm{th,p}}$	0.51	J/K	Thermal capacitance of a 3 mm MnZn ferrite plate calculated with specific heat capacity
$C_{\mathrm{th,m}}$	7.3	mJ/K	Thermal capacitance of 100 µm Mylar foil
c_m	1172	J kg/K	Specific heat capacity of Mylar
c_fe	800	J kg/K	Specific heat capacity of MnZn ferrite
ρ_fe	4800	$\mathrm{kg/m}^3$	Density of MnZn ferrite (3F45)
ρ_m	1390	$\mathrm{kg/m}^3$	Density of Mylar
$R_{\mathrm{th,a}}$	117.8	K/W	Thermal resistance of 3 mm polycarbonate (PC) air-gap lattice
R_th	37.8	K/W	Equivalent thermal resistance from calibration (cf. Fig. 6.13(b))
C_th	3.83	J/K	Equivalent thermal capacitance from calibration (cf. Fig. 6.13(b))

where it is assumed that the initial temperature of the ferrite plate at $t = 0$ equals the ambient temperature, T_{amb}. Inserting expression (6.2) in (6.4) yields

$$T(t) = (\kappa + \kappa_{\mathrm{s}}{}^{2d_{\mathrm{s}}/d_{\mathrm{p}}})\frac{d_{\mathrm{p}}A_{\mathrm{p}}}{C_{\mathrm{th,p}}}t + T_{\mathrm{amb}}. \tag{6.5}$$

The equivalent thermal capacitance of the plate, $C_{\mathrm{th,p}}$, can be determined from a calibration measurement as described later in Section 6.3.5 or calculated according to

$$\begin{aligned} C_{\mathrm{th,p}} &= (c_{\mathrm{f,s}}\rho_{\mathrm{f,s}}2d_{\mathrm{s}} + c_{\mathrm{f}}\rho_{\mathrm{f}}d_{\mathrm{b}})A_{\mathrm{p}} \\ &\approx c_{\mathrm{f}}\rho_{\mathrm{f}}d_{\mathrm{p}}A_{\mathrm{p}} = \tilde{c}_{\mathrm{f}}d_{\mathrm{p}}A_{\mathrm{p}}, \end{aligned} \tag{6.6}$$

where c_{f} and ρ_{f} is the specific heat capacity and density of MnZn ferrite as listed in Tab. 6.2, respectively. Note, that it is assumed that the thermal capacitance of the plate is predominantly governed by the bulk properties. Substituting (6.6) in (6.5) leads to

$$T(t) = \left(\frac{\kappa}{\tilde{c}_{\mathrm{f}}} + \frac{\kappa_{\mathrm{s}}}{\tilde{c}_{\mathrm{f}}}\frac{2d_{\mathrm{s}}}{d_{\mathrm{p}}}\right)t + T_{\mathrm{amb}}. \tag{6.7}$$

It can be seen that the temperature rise is governed by a constant contribution of the bulk material and a contribution of the power dissipation in the surface layer which depends on the actual ratio of surface to plate thickness. This trend is strongly supported by the experimental results depicted in Fig. 6.6(b), where it can be seen that a multi-gap sample assembled from thin 1 mm plates features a much steeper slope in contrast to thicker 3 mm plates and the (very thick) solid reference sample. Interestingly, since both total power loss and total thermal capacitance are increasing proportional to the number of stacked plates, the slope of the temperature rise is not affected by the actual height of the stack (i.e. number of plates in the stack) as confirmed by the measurement results depicted Fig. 6.6(c). This in turn allows to measure a stack rather than a single plate which is advantageous in accommodating the required flux sense winding and improves mechanical handling of the sample for a precise placement in the test circuit (cf. Section 6.3.2).

Since the properties of ferrite are strongly depending on temperature, the duration t_χ to reach a specified temperature difference, $\Delta T = T_{\mathrm{end}} - T_{\mathrm{amb}}$, is measured rather than a final temperature after a fixed time span Δt. Rearranging (6.7) leads to

$$t_\chi = \frac{\Delta T}{\frac{\kappa}{\tilde{c}_{\mathrm{f}}} + \frac{\kappa_{\mathrm{s}}}{\tilde{c}_{\mathrm{f}}}\frac{2d_{\mathrm{s}}}{d_{\mathrm{p}\chi}}} \tag{6.8}$$

for a plate with thickness $d_{\mathrm{p}\chi}$. Now, performing two consecutive measurements with identical operating point but using ferrite plates with different thicknesses, $d_{\mathrm{p}1}$ and $d_{\mathrm{p}2}$, allows to solve (6.8) to obtain the loss density of the bulk ferrite,

$$\kappa = \frac{(d_{\mathrm{p}1}t_2 - d_{\mathrm{p}2}t_1)}{(d_{\mathrm{p}1} - d_{\mathrm{p}2})t_1t_2}\tilde{c}_{\mathrm{f}}\Delta T, \tag{6.9}$$

and the loss per surface area,

$$\tilde{\kappa}_{\mathrm{s}} = \kappa_{\mathrm{s}}d_{\mathrm{s}} = \frac{1}{2}\frac{d_{\mathrm{p}1}d_{\mathrm{p}2}(t_1 - t_2)}{(d_{\mathrm{p}1} - d_{\mathrm{p}2})t_1t_2}\tilde{c}_{\mathrm{f}}\Delta T. \tag{6.10}$$

Note, that since the actual thickness of the surface layer d_{s} is unknown, it is more suitable to define power loss per surface area, $[\tilde{\kappa}_{\mathrm{s}}] = \mathrm{mW/cm^2}$.

6.3.2 Experimental Setup

An excitation circuit is needed which ensures a homogeneous flux density distribution in the sample, allows to characterize the core loss for different flux density amplitudes and frequencies, and facilitates an easy installation of different samples. A magnetic circuit resembling an E-type core with the multi-gap sample located in the center limb as depicted in Fig. 6.7 is chosen in this study, since it only requires a single sample as opposed to a U-type setup and can be assembled by individual off-the-shelf available ferrite cuboids minimizing custom machining effort. The multi-gap sample in the center as well as the individual ferrite cuboids are fixated by means of a 3D printed mounting fixture and fastening screws. Consistent pressure applied to the ferrite regardless of the inserted sample is guaranteed by means of a torque wrench adjusted to 0.02 N m. In Fig. 6.9, two multi-gap samples assembled with 1 mm and 3 mm thick plates, respectively, and a solid, single piece ferrite sample are shown. The equivalent circuit of the test setup is shown in Fig. 6.10, where the transformer equivalent circuit with open secondary winding represents the magnetic excitation circuit with flux sense winding. The reactive power of the magnetic circuit is compensated by means of a series connected capacitor in order to reduce the burden on the HF voltage source (Iwatsu IE-1125B) and attain all operating points $\{\hat{B}, f\}$ of interest given the output voltage limitation of the amplifier.

Since the outer magnetic circuit contributes to the total core losses (troublesome in case of the electrical loss measurement, cf. Appendix A.2) and heat generation in the test circuit can affect the sample temperature, the

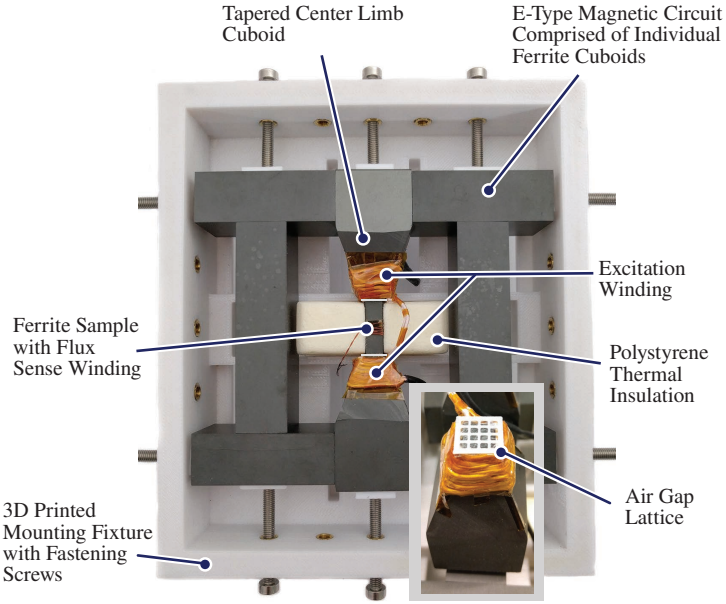


Fig. 6.7: Test circuit resembling an E-type core with a multi-gap core sample located in the middle of the center limb; fastening screws and a 3D printed mounting fixture keeping the individual ferrite cuboids of the outer magnetic circuit and the sample in position; splitting the turns of the excitation winding in two sections above and below the sample and employing tapered center limbs to accommodate the cross section difference between outer magnetic circuit and sample facilitates a homogenous flux density distribution in the sample; a dedicated tightly wound sense winding is placed around the center of the sample to correctly adjust the peak flux density; measures to increase the thermal resistance to ambient are the polystyrene casing and the air gap lattice inserted between sample and test circuit.

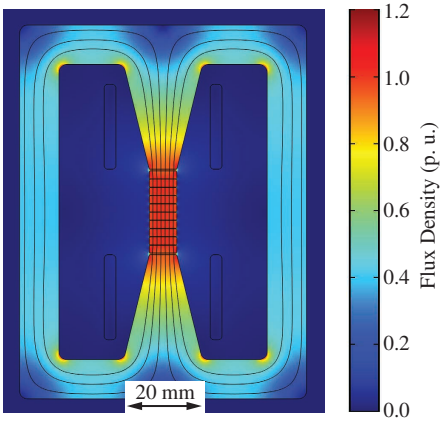


Fig. 6.8: FEM simulation result showing the homogenous flux density distribution in the sample.

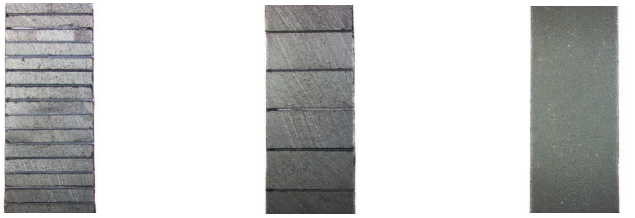


Fig. 6.9: Picture of multi-gap samples composed of 1 mm and 3 mm plates, respectively, and the single-piece solid reference sample. To adjust the partial gap length, 100 µm thick Mylar foil is inserted between the plates.

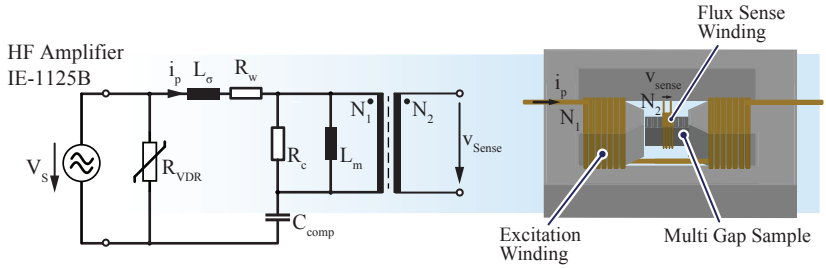


Fig. 6.10: Schematic of the employed excitation circuit; The dedicated sense winding with N_2 turns allows to precisely determine the flux density. The reactive power of the magnetic circuit is compensated by means of a capacitor bank to reduce the burden on the HF voltage source and attain all operating points $\{\hat{B}, f\}$ of interest despite the limited HF amplifier output.

dimensions of the outer magnetic circuit are chosen such that its losses are minimized while keeping the flux density in the sample homogeneous. This can be achieved by increasing the cross section of the magnetic path while minimizing its avg. magnetic length, since the sample-to-core loss ratio considering homogenous flux density in the setup is given by

$$\frac{P_{\text{sample}}}{P_{\text{test}}} \propto \left(\frac{A_{\text{test}}}{A_{\text{p}}}\right)^{\beta-1} \frac{l_{\text{m,sample}}}{l_{\text{m,test}}}, \tag{6.11}$$

where A_{test}, A_{p} and $l_{\text{m,test}}$, $l_{\text{m,sample}}$ denote the cross section area and avg. magnetic path length of the test circuit and sample, respectively. However, due to the distributed gap, the comparably large magnetic reluctance of the installed multi-gap sample in the center limb results in a significant leakage flux which potentially causes an inhomogeneous flux density distribution in the sample or bypasses it completely and only contributes to undesired loss in the test circuit. With the aid of magnetostatic field simulations (cf. Fig. 6.8), optimal dimensions based on readily available core shapes were obtained which maximize the sample-to-core loss ratio of the setup while keeping the flux density distribution in the sample homogenous. As shown in Fig. 6.7, two measures were employed which greatly contribute to a homogenous flux density distribution in the sample: (i) the turns of the excitation winding are split into two sections directly above and below the sample and (ii) tapered center limbs are employed to accommodate the cross section difference between test circuit and sample. In order to correctly adjust the desired flux density amplitude in

the multi-gap sample despite different cross section areas and leakage flux, a dedicated tightly wound sense winding is placed around the center of the sample as indicated in Fig. 6.7.

As mentioned previously in Section 6.3.1, due to the constant loss density and the low thermal conductivity towards ambient in lateral direction, a uniform temperature distribution in (x, y)-direction (cf. Fig. 6.3) is present throughout the sample which allows to infer the correct temperature from a measurement at one of the lateral surfaces. In this work, infrared thermography is the preferred temperature instrumentation since (i) it allows to compute the average temperature over the entire multi-gap sample as opposed to a single spot measurement provided by fiber optical temperature probes, thermistors (NTC, PTC) or thermocouples and (ii) is contactless, i.e. does not require to physically attach a probe to the delicate sample. Moreover, infrared thermography reveals non-uniform temperature distributions and the formation of hot spots and thus allows to detect inhomogeneous flux density distribution in the sample (flux crowding) caused by a potential sample misalignment and/or an excessive gap between sample and center limb pole pieces of the test circuit. Using thermography to determine core loss distribution in magnetic components has been reported in [137, 138] and to detect defects in ferromagnetic laminated sheets and soft magnetic composites in [139]. The authors in [140], applied infrared thermography to visualize the iron loss distribution in a permanent magnet motor.

A photograph of the experimental measurement setup is depicted in Fig. 6.11(a), showing the implemented test setup according to Fig. 6.10 with the magnetic circuit and capacitor bank and a FLIR A655sc high definition infrared camera pointed towards the multi-gap sample. The camera is equipped with an additional close-up lens to allow a working distance of around 6 cm – 7 cm between sample and camera lens and to provide a 50 µm spatial resolution. The lower ±2 °C absolute measurement accuracy of a microbolometer [141] is not relevant here, since according to (6.9) and (6.10) only a temperature difference must be determined and the standard deviation per detector pixel of a high-end infrared camera is typically 0.1 °C – 0.2 °C [142]. Compensating the reactance of the magnetic test circuit is necessary to attain all $\{\hat{B}, f\}$ operating points of interest given the limited voltage range of the employed IWATSU IE-1125B HF power amplifier. For a good agreement with the linear model derived in Section 6.3.1, the heat transfer from sample to ambient in the experimental setup must be reduced as much as possible. To prevent convective heat transfer from the lateral surfaces of each individual plate in the stack to ambient, the sample is encased in polystyrene except for the

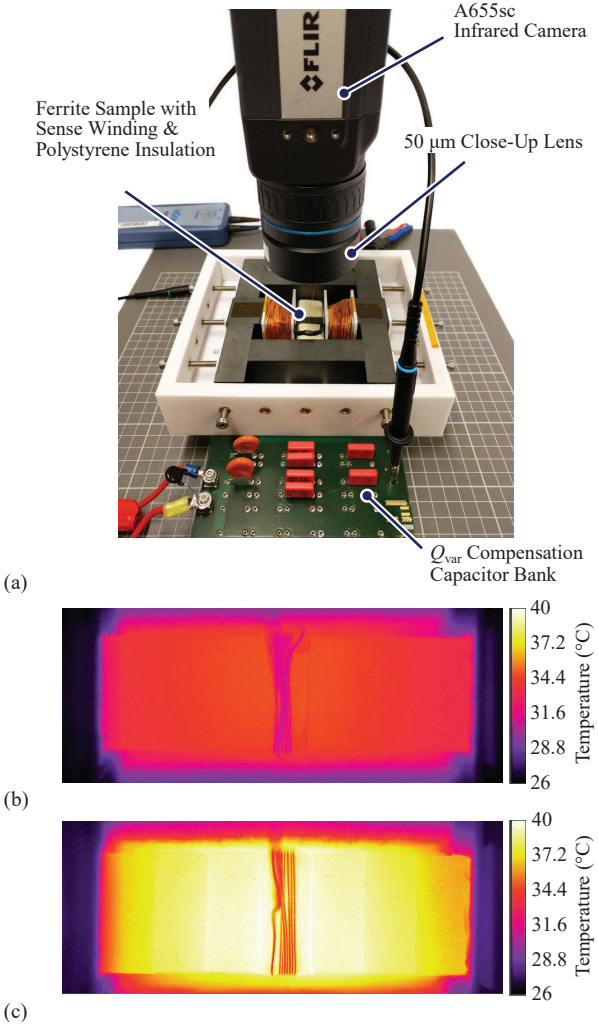


Fig. 6.11: (a) Picture of the experimental setup showing the magnetic test circuit with capacitor bank for reactive power compensation and the employed FLIR A655sc high definition infrared camera pointed towards the sample. Thermography image of the temperature rise of the solid (b) and multi-gap sample (c) subject to an excitation with 125 mT at 400 kHz exactly after 30 s of total elapsed measurement time. It is clearly visible that the multi-gap sample composed of 7×3 mm plates is heating up much quicker.

surface pointing towards the infrared camera as can be seen from Fig. 6.7 and Fig. 6.11(a). Furthermore, to minimize conductive heat transfer from the multi-gap sample to the two center limb core pieces of the E-type test circuit, an additional gap between sample and adjacent pole pieces is inserted. A gap length of around 0.5 mm is a still acceptable trade-off between minimizing conductive heat transfer and establishing a homogenous flux density in the sample close to the interfaces. In order to achieve the lowest possible thermal conductivity, the gap is realized by means of a 3D printed lattice made out of polycarbonate as depicted in the detail view of Fig. 6.7.

The experimental results presented in Section 6.4 of this chapter were obtained by relating the slope of the temperature rise of a multi-gap sample with 7 stacked 3 mm ferrite plates ($d_{\mathrm{p1}} = 3\,\mathrm{mm}$) to a solid, single-piece reference sample of 21 mm length ($d_{\mathrm{p2}} = 21\,\mathrm{mm}$). Mylar foil is inserted between adjacent plates to establish a gap length of 100 µm, which, in combination with 3 mm plates, completely alleviates loss contributions arising from flux crowding in the sample caused by assembly and mechanical tolerances as described in Appendix A.1.

At each operating point of interest, $\{\hat{B}, f\}$, the temperature rise after abruptly enabling the correctly adjusted power amplifier is recorded for both samples and the core and surface loss density are then computed according to (6.9) and (6.10). The elapsed time to reach a specific temperature difference ΔT starting from ambient temperature is extracted from the captured temperature rise in a subsequent post-processing step. Since the core loss and many other properties of ferrite depend strongly on operating temperature, a large temperature deflection would certainly have an impact on the results. However, the high frame rate of the infrared camera (up to 50 Hz with full resolution of 640×480) allows to determine the elapsed time even for a very small temperature difference of just a few °C. The experimental results presented in this chapter were obtained for $\Delta T = 2.5\,^{\circ}\mathrm{C}$.

A snapshot of the temperature rise of the solid and multi-gap sample subjected to an excitation with 125 mT at 400 kHz exactly after 30 s of total elapsed measurement time is shown in Fig. 6.11(b) and Fig. 6.11(c), respectively. Since both measurements were started from ambient temperature, $T_{\mathrm{amb}} = 26.4\,^{\circ}\mathrm{C}$, it can be clearly seen that the multi-gap sample heats up much faster showing a final temperature reading of around 38 °C in contrast to roughly 32 °C of the solid sample. Note the interruption of the uniform temperature distribution by the sense winding in the center of each sample.

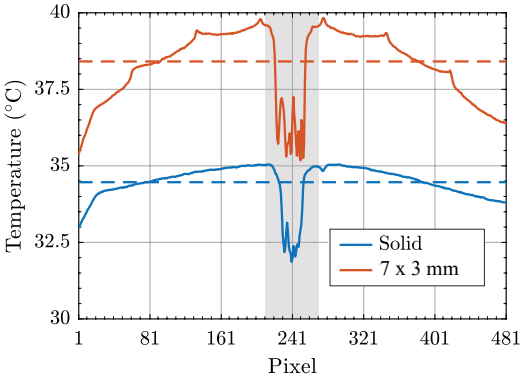


Fig. 6.12: Temperature profile in longitudinal direction of the IR images of solid and multi-gap sample shown in Fig. 6.11(b) and (c); the dashed line represents the average value of the IR sensor and is used to compute ΔT.

6.3.3 Longitudinal Temperature Gradient

Referring to Fig. 6.11(b) and (c), it is noticeable that both samples exhibit a temperature gradient in longitudinal direction with slightly lower temperatures at both ends where the sample connects to the outer magnetic circuit. Fig. 6.12 depicts the computed temperature profile of both infrared images in longitudinal direction, whereby the temperature reading at every camera pixel in the plot represents the mean temperature of all sensor pixels encompassing the sample in transversal direction (i.e. orthogonal to the direction of the flux). It becomes evident that the temperature gradient in the multi-gap sample is more pronounced ($\approx 3.75\,°\mathrm{C}$) compared to the solid reference sample ($\approx 1.25\,°\mathrm{C}$). Moreover, the temperature profile of the multi-gap sample exhibits a clear local maximum whenever two surfaces of adjacent ferrite plates meet, i.e. at the surfaces of the plates. Now, a representative thermal network of stacked plates is shown in Fig. 6.13(a) which is helpful to explain the more pronounced temperature gradient in case of the multi-gap sample. Note, that the simplified thermal model of a single plate according to Fig. 6.5(c) is considered. Since the thermal capacitance of a piece of Mylar foil is negligible compared to the ferrite plate (cf. Tab. 6.2) only the thermal resistance introduced by the gap material, $R_{\mathrm{th,m}}$, is included in the model. Although the thermal conductivity of Mylar is at least a factor 10 lower compared to MnZn ferrite, the resulting thermal resistance of foil and ferrite plate is in the same order of magnitude ($\approx 15\,\mathrm{K/W}$ as listed in Tab. 6.2). However, since the length

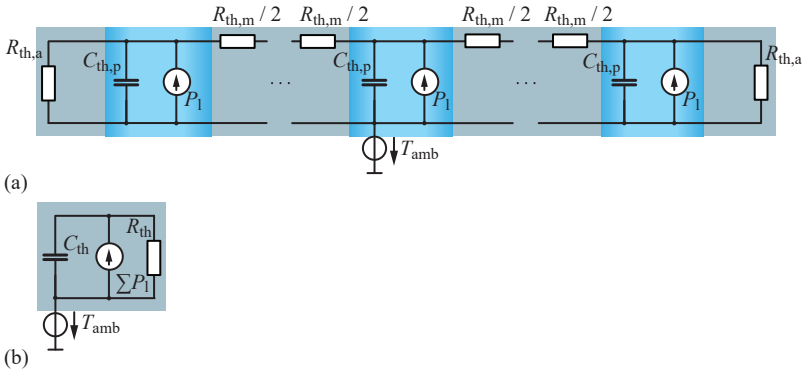


Fig. 6.13: (a) Representative thermal network of stacked plates using the simplified thermal model of a single plate according to Fig. 6.5(c) and considering the thermal resistance $R_{th,m}$ introduced by the gap material. (b) First order thermal model of a sample corresponding to averaged IR temperature reading in longitudinal direction.

of both samples examined in this study is equal per design and the Mylar foil has virtually no contribution, the effective thermal capacitance of both solid and multi-gap sample is identical. Ideally, if $R_{th,a} \rightarrow \infty$ then each plate will exhibit exactly the same temperature rise irrespective of the actual position in the stack as confirmed by a circuit simulation. However, the thermal resistance achieved with the air gap lattice is estimated to be $R_{th,a} \approx 117.8\,\mathrm{K/W}$ considering the thermal conductivity of polycarbonate (PC) and air (air gap lattice, cf. Fig. 6.7), and evidently not sufficiently large to support uniform heating in longitudinal direction. It follows that the temperature gradient is more pronounced in case of the stacked plate assembly since heat close to the center of the sample encounters an effectively larger thermal resistance in longitudinal direction towards both ends of the sample in comparison to the solid, single-piece sample. Now, in order to determine the elapsed time to reach a specific temperature difference, ΔT, the pragmatic way of averaging the IR sensor reading also in longitudinal direction is followed as indicated with dashed lines in Fig. 6.12, naturally excluding the distortion in the center of the sample caused by the flux sense winding. The corresponding first order thermal model is shown in Fig. 6.13(b) and the expression for the core and surface loss densities based on the linear model are refined in the following. Note that in the following R_{th} and C_{th} denote the equivalent thermal parameters of a stack of plates (cf. $R_{th,p}$ and $C_{th,p}$ of a single plate, Fig. 6.5(c))

6.3.4 Exponential Thermal Model For Multi-Gap Assembly

Based on the equivalent circuit shown in Fig. 6.13(b), the temperature rise of an assembly with m plates of thickness d_p starting from T_amb at $t = 0$ is given by

$$\begin{aligned} T(t) &= P_{\mathrm{l}\Sigma} R_\mathrm{th} \left(1 - e^{-\frac{t}{\tau}}\right) + T_\mathrm{amb} \\ &= \left(\kappa + \kappa_\mathrm{s} 2 d_\mathrm{s}/d_\mathrm{p}\right) m V_\mathrm{p} R_\mathrm{th} \left(1 - e^{-\frac{t}{\tau}}\right) + T_\mathrm{amb}, \end{aligned} \tag{6.12}$$

with the time constant $\tau = R_\mathrm{th} C_\mathrm{th}$ and the core volume of a plate $V_\mathrm{p} = d_\mathrm{p} A_\mathrm{p}$. It should be emphasized, that the total core volume $V_{\mathrm{p}\Sigma} = m V_\mathrm{p}$ is kept constant by adapting the plate thickness in accordance to the number of gaps such that the examined multi-gap samples feature equal thermal parameters $R_\mathrm{th}, C_\mathrm{th}$. Analogously to the derivation described in Section 6.3.1, measuring the elapsed time t_1 and t_2 of two samples with distinct plate thickness $d_{\mathrm{p}1}$ and $d_{\mathrm{p}2}$ to reach a specific ΔT allows to calculate the core loss density

$$\kappa = \frac{d_{\mathrm{p}1}(1 - e^{-\frac{t2}{\tau}}) - d_{\mathrm{p}2}(1 - e^{-\frac{t1}{\tau}})}{(d_{\mathrm{p}1} - d_{\mathrm{p}2})(1 - e^{-\frac{t1}{\tau}})(1 - e^{-\frac{t2}{\tau}})} \frac{\Delta T}{R_\mathrm{th} V_{\mathrm{p}\Sigma}}, \tag{6.13}$$

and the surface loss density

$$\tilde{\kappa}_s = \frac{1}{2} \frac{d_{\mathrm{p}1} d_{\mathrm{p}2} (e^{-\frac{t2}{\tau}} - e^{-\frac{t1}{\tau}})}{(d_{\mathrm{p}1} - d_{\mathrm{p}2})(1 - e^{-\frac{t1}{\tau}})(1 - e^{-\frac{t2}{\tau}})} \frac{\Delta T}{R_\mathrm{th} V_{\mathrm{p}\Sigma}}, \tag{6.14}$$

given that thermal parameters R_th and C_th are known from a preceding DC calibration measurement as described in the next subsection.

6.3.5 DC Calibration

By means of capturing the temperature response of the sample subject to a stepwise impressed power loss of predetermined value, the parameters of the model (6.12) can be identified by means of a least mean square regression. For good predictions of the model, it is crucial that the power range covered in the calibration actually resembles the core loss occurring in the respective operating point of interest, $\{\hat{B}, f\}$. Fig. 6.14(a) shows the excellent agreement between the measured temperature response obtained for the solid sample (blue) and the simulated response of the mathematical model with identified

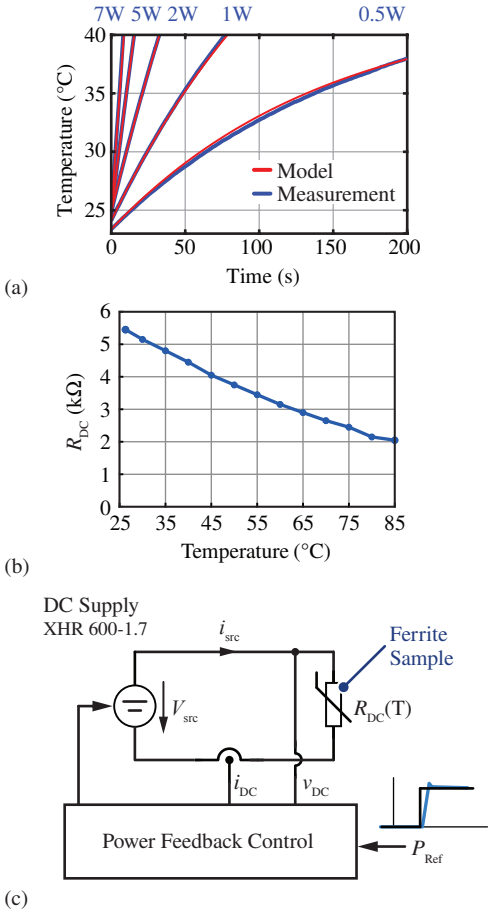


Fig. 6.14: (a) Measured temperature response obtained for the solid sample (blue) and the simulated response of the mathematical model with identified parameters (red) for several impressed power levels ranging from 0.5 W to 7 W. (b) Measured DC resistance of MnZn ferrite as a function of temperature. (c) Schematic of implemented power feedback control to impress constant power during calibration despite temperature dependent change of the ferrite DC resistance.

parameters (red) for several impressed power levels ranging from 0.5 W to 7 W. Treating the solid ferrite sample as an electric conductor with a DC resistance, R_{DC}, the power loss required for the calibration measurements can be impressed by means of Joule heating, $P_{\mathrm{DC}} = R_{\mathrm{DC}} I_{\mathrm{DC}}^2$. The measured DC resistance of the solid sample amounts to 5.5 kΩ at room temperature and varies strongly with temperature as shown in Fig. 6.14(b). Since the temperature of the sample rises during the measurement but the impressed power must be kept constant (step response), feedback control is employed to tightly track P_{DC} reference by means of adjusting the applied DC voltage as schematically depicted in Fig. 6.14(c). Since DC quantities are involved, the power instrumentation is trivial. Terminals to connect the leads of the DC supply are formed with narrow stripes of 50 µm thick copper foil glued to both ends of the sample using conductive silver epoxy. Using thin copper foil for the contacts allows the sample to be properly installed in the magnetic test circuit during the calibration which is crucial to correctly identify the thermal resistance to ambient. The identified parameters, $C_{\mathrm{th}} = 3.83\,\mathrm{J/K}$ and $R_{\mathrm{th}} = 37.8\,\mathrm{K/W}$ are in reasonable agreement with estimates based on material constants as listed in Tab. 6.2 ($7 \cdot C_{\mathrm{th,p}} \approx 3.6\,\mathrm{J/K}$, $1/2 \cdot R_{\mathrm{th,a}} = 58.9\,\mathrm{K/W}$).

6.3.6 Measurement Error

Consolidating (6.13) and (6.14), two main sources of error can be identified: (i) The IR camera's standard deviation of the temperature difference measurement ΔT denoted with $\sigma_{\Delta \mathrm{T}}$ and (ii) uncertainty in the parameters R_{th}, C_{th} of the underlying model represented with standard deviations σ_{R} and σ_{C}. Potential uncertainty in the measured time intervals due to sampling delay and/or jitter of the IR camera is neglected because of the high sampling frame rate relative to the measurement time. In order to calculate the error propagation, the non-linear equations of κ and κ_{S} are linearized around $\chi = (t_{1\chi}, t_{2\chi}, \kappa_\chi, \tilde{\kappa}_{\mathrm{s}\chi})$ resulting from a specific excitation $\{\hat{B_\chi}, f_\chi\}$. In the following the equations are only explicitly presented for κ for the sake of brevity. The standard deviation of κ around χ is then given by [143]

$$\sigma_\kappa(\chi) = \sqrt{J_\kappa(\chi) \Sigma J_\kappa(\chi)^T}, \tag{6.15}$$

where Σ denotes the covariance matrix and $J_\kappa(\chi)$ is the Jacobi-matrix of κ at χ,

$$J_\kappa(\chi) = \left[\left.\frac{\partial \kappa}{\partial \Delta T}\right|_\chi, \left.\frac{\partial \kappa}{\partial R_{\mathrm{th}}}\right|_\chi, \left.\frac{\partial \kappa}{\partial C_{\mathrm{th}}}\right|_\chi \right]. \tag{6.16}$$

The covariance matrix is given by

$$\Sigma = \begin{pmatrix} \sigma_{\Delta T}^2 & r_{\Delta T,R}^2 \sigma_{\Delta T}\sigma_R & r_{\Delta T,C}^2 \sigma_{\Delta T}\sigma_C \\ r_{\Delta T,R}^2 \sigma_{\Delta T}\sigma_R & \sigma_R^2 & r_{R,C}^2 \sigma_R \sigma_C \\ r_{\Delta T,C}^2 \sigma_{\Delta T}\sigma_C & r_{R,C}^2 \sigma_R \sigma_C & \sigma_C^2 \end{pmatrix} \tag{6.17}$$

where $r_{x,y}$ represents the correlation coefficient between stochastic variables x and y. From a physical standpoint, there is only a weak correlation between variations in R_{th} and C_{th} and also between variations in ΔT and R_{th}. However, there is a more pronounced negative correlation between variance in ΔT and C_{th}, since a larger ΔT during calibration with a specific impressed power and measurement time interval leads to smaller C_{th}.

Instead of presenting exhaustive analytical equations, some general facts should be highlighted. Naturally, a distinct difference in plate thickness between the examined multi-gap samples results in a significant difference in elapsed time to reach ΔT and thus supports a small measurement error. Since the measurement time $t_{1\chi}$ and $t_{2\chi}$ for a specific ΔT increases inversely proportional to the dissipated power in the ferrite plate, a small (large) absolute error must be expected at a low (high) loss operating point, respectively. In principle, allowing a larger temperature difference ΔT increases the measurement time and leads to a reduction in error. However, ΔT cannot be increased too much (here $\Delta T = 2.5\,°C$ cf. Section 6.3.2) since the ferrite properties are a strong function of temperature. In order to calculate a worst case bound on the measurement error a deviation of $\sigma_{\Delta T} = 0.3\,°C$ and a 15 % deviation of the thermal parameters from their expected values as listed in Tab. 6.2 is assumed. Moreover, since in (6.17) the exact correlation between the variables is unknown, a worst case error of κ and $\tilde{\kappa}_s$ is determined by varying the coefficient $r_{x,y}$ in a numerical study. It then follows from (6.15) that for the operating points of interest, the worst case relative measurement error is estimated to be

$$\frac{\sigma_\kappa}{\kappa}(\chi) \leq 20.3\,\% \quad \text{and} \quad \frac{\sigma_{\tilde{\kappa}s}}{\tilde{\kappa}_s}(\chi) \leq 19.9\,\%. \tag{6.18}$$

6.4 Experimental Results

In this section the bulk and surface core loss density of MnZn ferrite material 3F4 of Ferroxcube are presented. The experimental results were obtained by means of the thermometric measurement setup with IR camera as described in detail in Section 6.3.2 and expression (6.13) and (6.14) based on the exponential

thermal model. The measurements were carried out for a sinusoidal flux density with amplitudes varying from 75 mT up to 200 mT and excitation frequencies ranging from 200 kHz up to 1 MHz. For this range of operating points $\{\hat{B}, f\}$, the worst case relative measurement error of both bulk and surface core loss density is limited to 20 % as discussed in the previous section.

The bulk and surface core loss density at a fixed frequency of 400 kHz and varying flux density amplitudes is depicted in Fig. 6.15(a) and (b). The predictions obtained from the Steinmetz model (6.1) fitted to the experimental data and from parameters provided by the vendor are represented by the dashed blue and red line, respectively. The experimental and vendor parameter of the Steinmetz model are summarized in Tab. 6.3. In a similar manner, the bulk and surface core loss density at a fixed flux density amplitude of 100 mT

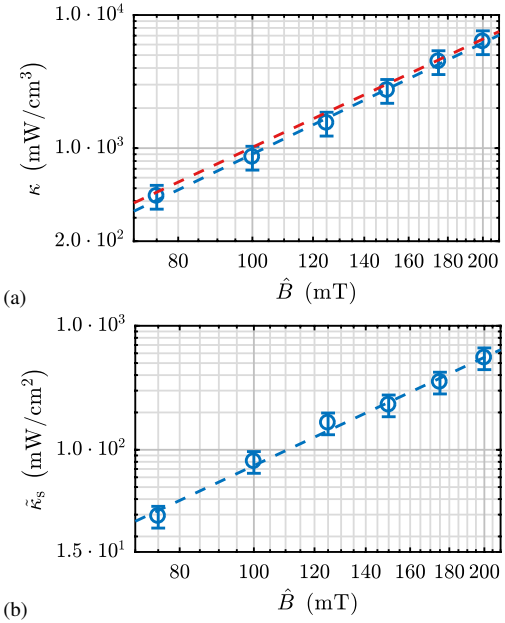


Fig. 6.15: Experimentally determined (a) bulk and (b) surface core loss density of MnZn ferrite material 3F4 at a fixed frequency of 400 kHz and varying flux density amplitude. The prediction obtained from the Steinmetz model fitted to the experimental data is indicated by the dashed blue line. In addition the prediction with Steinmetz parameters provided by the vendor (cf. Tab. 6.3, [144]) is indicated by the dashed red line in (a).

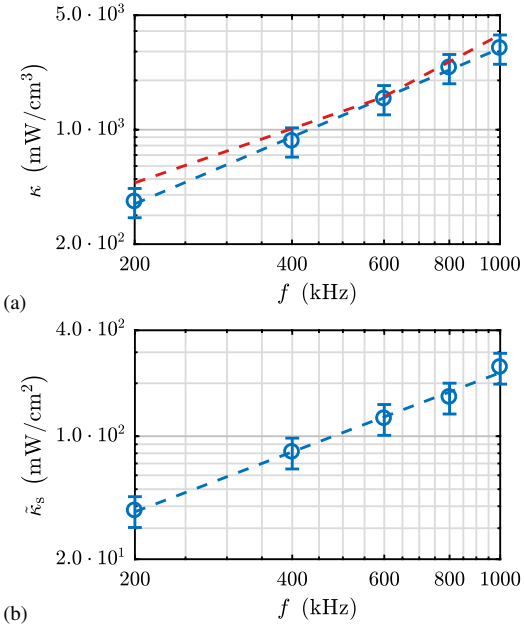


Fig. 6.16: Experimentally determined (a) bulk and (b) surface core loss density of MnZn ferrite material 3F4 at a fixed peak flux density of 100 mT and varying frequency. The prediction obtained from the Steinmetz model fitted to the experimental data is indicated by the dashed blue line. In addition the prediction with Steinmetz parameters provided by the vendor (cf. Tab. 6.3, [144]) is indicated by the dashed red line in (a).

Tab. 6.3: Steinmetz Parameters For MnZn Ferrite Material 3F4 From Ferroxcube $[\kappa] = \mathrm{mW/cm^3}$ and $[\kappa_s] = \mathrm{mW/cm^2}$

	k	α	β
κ	1.32×10^{-2}	1.36	2.77
$\kappa^{\dagger}$	35×10^{-2}	1.1	2.7
$\kappa^{\ddagger}$	1.2×10^{-4}	1.7	2.7
κ_s	2.72×10^{-2}	1.13	2.9

† [144], 100 kHz – 600 kHz and 30 °C
‡ [144], 600 kHz – 1000 kHz and 30 °C

and varying excitation frequency is depicted in Fig. 6.16(a) and (b). Note, that depending on the frequency range a different set of vendor Steinmetz parameter is employed which explains the slight kink in the dashed red line at 600 kHz as indicated in Fig. 6.16(a). However, the Steinmetz fit to the experimental data was performed over the entire frequency range which explains the discrepancy, especially in the frequency exponent α, between experimental and vendor parameters (cf. Tab. 6.3). It can be seen from Fig. 6.15(b) and Fig. 6.16(b) that the measured surface loss density varies from 30 $\mathrm{mW/cm^2}$ to 600 $\mathrm{mW/cm^2}$ for the considered operating points.

In order to assess whether the Mylar foil inserted between the plates has any contribution to the measured surface loss (e.g. by magnetostriction introduced friction), a multi-gap sample was prepared using Mylar foil with a punched round hole of approx. 5 mm diameter in the center of each foil as illustrated in the bottom right of Fig. 6.17. Punching a hole in the center ensures the desired gap distance and therefore still ensures equal flux distribution and/or prevents partial saturation while removing roughly 50 % of the gap material. The measured surface loss density of a multi-gap sample with punched Mylar foil is compared to the regular multi-gap sample in Fig. 6.17, showing no difference between the results.

To understand whether or not machining is actually the main cause of the increased core loss, ferrite plates directly sintered to the final dimension were provided by Ferroxcube in this study. These plates were manufactured by pressing and then machining ferrite powder into the appropriate dimensions before the actual sintering was performed (green grinding). Taking the size shrinkage caused by the sinter process into account, the correct final dimension of the plates has been immediately achieved eliminating the need of an additional machining step. The experimental measured surface loss density is also included in Fig. 6.17. It can be seen that $\tilde{\kappa}_\mathrm{s}$ has slightly reduced at low flux density amplitudes in comparison to the regular sample composed of machined ferrite plates and exhibits a steeper slope corresponding to a Steinmetz parameter of $\beta_\mathrm{s} = 3.4$.

6.5 Discussion

The measured core loss densities shown in Fig. 6.15(a) and Fig. 6.16(a) show good agreement with the Steinmetz model provided by the manufacturer validating the proposed calorimetric core loss measurement technique. With regard to the surface loss densities (cf. Fig. 6.15(b) and Fig. 6.16(b)), the experimental data can be also well predicted with the Steinmetz model. Interest-

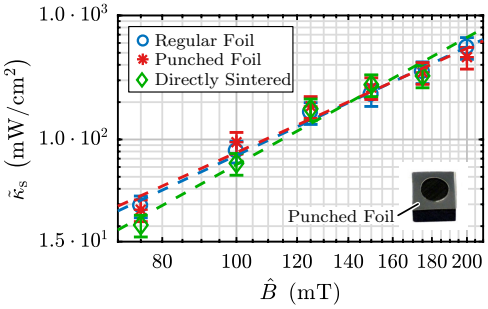


Fig. 6.17: Comparison of the surface loss density of different multi-gap samples at a fixed frequency of 400 kHz and varying flux density amplitude. The regular sample is composed of 7 × 3 mm plates with 100 µm Mylar foil in between. Roughly half of the Mylar foil area was removed in case of the punched foil sample. The green grinded sample was constructed from ferrite plates which were pressed and then sintered to the desired dimensions without machining.

ingly and as to be expected, the Steinmetz parameters of the surface layer are slightly different from the bulk material as listed in Tab. 6.3. Compared to the bulk ferrite, the frequency exponent α in the surface is smaller ($1.36 \rightarrow 1.13$) and the flux density exponent β is larger ($2.77 \rightarrow 2.9$). Since the loss in the deteriorated surface layer is more sensitive to variation in flux density than it is to variation in frequency (almost linear relationship with frequency), it can be argued that hysteresis losses are more pronounced in the surface layer.

In order to illustrate the impact of $\tilde{\kappa}_\mathrm{s}$ in more practical terms, the total power loss of a composite core assembled from individual d_p thick plates relative to the bulk core loss of a solid ferrite piece with d_bulk total length is computed,

$$\frac{P_\mathrm{tot}}{P_\mathrm{bulk}} \approx \frac{\left(\kappa d_\mathrm{bulk} A_\mathrm{p} + \kappa_\mathrm{s} 2 d_\mathrm{s} \frac{d_\mathrm{bulk}}{d_\mathrm{p}} A_\mathrm{p}\right)}{\kappa d_\mathrm{bulk} A_\mathrm{p}} = 1 + \frac{\kappa_\mathrm{s}}{\kappa} \frac{2 d_\mathrm{s}}{d_\mathrm{p}} = 1 + \frac{\tilde{\kappa}_\mathrm{s}}{\kappa} \frac{2}{d_\mathrm{p}}, \tag{6.19}$$

and depicted in Fig. 6.18(a) based on the experimental results obtained for 3F4 at 125 mT and 400 kHz. The reference sample is constructed from a single piece of ferrite with a total length of 20 mm exhibiting only bulk core loss. With decreasing height of the ferrite plate, more and more plates must be

stacked to reach the same length as the solid reference sample. Consequently, the total losses increase since more and more deteriorated surface layers are introduced in the sample. Note, that the ratio between total and bulk core loss given by (6.19) is a function of only the plate thickness, d_p, since both bulk and surface core losses increase proportional with the core cross section, A_p, and the total sample length, d_bulk, assuming that d_bulk is varied in multiples of d_p. To further clarify, two composite core samples with different cross section area and/or different total sample length will exhibit the same total to bulk loss ratio (6.19) if the samples are constructed of plates with identical thickness. The critical plate thickness $d_\mathrm{p,crit}$ is defined to be reached when the surface loss is equal to the bulk core loss, that is to say when the total power loss has doubled compared to the solid (single-piece) sample. In the case at hand, a composite core with 13 stacked 1.5 mm plates will exhibit roughly twice the core loss compared to the single-piece reference sample. Since κ and $\tilde{\kappa}_\mathrm{s}$ exhibit a different dependency on flux density amplitude and frequency (cf. Tab. 6.3), the critical plate thickness varies depending on the actual operating point $\{\hat{B}, f\}$ as depicted in Fig. 6.18(b). It should be noted that, the actual critical thickness depends not only on the properties of the ferrite but also on the exerted mechanical stress during the machining of the plates.

In an open discussion of the findings with the scientific community prior to this publication, it was argued that the measured excess core loss in the multi-gap core is actually the result of micro-vibrations causing friction between plate surface and gap material and that these micro-vibrations are excited by means of magnetostriction as discussed in detail in [145–147]. In this respect, if friction between plate surfaces and Mylar would indeed be the reason for the measured surplus core losses, then in case of the sample using punched Mylar foil, where roughly half of the interaction area was removed, a significant reduction in $\tilde{\kappa}_\mathrm{s}$ should be observable. However, as depicted in Fig. 6.17, the measured surface loss density of the multi-gap sample with punched and regular Mylar foil is essentially identical, which strongly contradicts the notion that micro-vibrations are the origin of the excess core losses. Furthermore, an experimental assessment with a laser vibrometer (Polytec CLV-2534) confirmed that within the considered excitation frequency range no micro-vibrations are excited.

Moreover, the idea was put forward that the measured excess core loss might be associated with machining and assembly tolerances. For instance, a pronounced tilt between the plates of the multi-gap assembly causes a non-uniform gap length which has a strong impact on the core loss due to flux

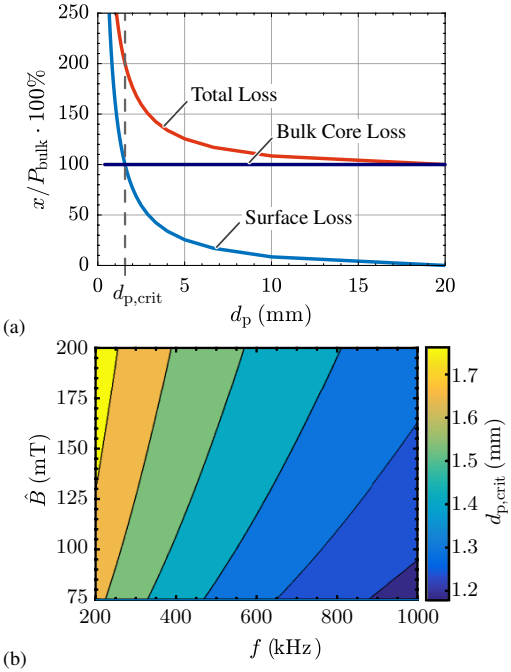


Fig. 6.18: (a) Surface losses and total core losses of a composite core assembled with individual d_{p} thick plates relative to the bulk core losses of a solid ferrite piece with $d_{\text{bulk}} = 20\,\text{mm}$ total length based on the experimental results obtained for 3F4 at 125 mT and 400 kHz. The critical plate thickness $d_{\text{p,crit}}$ is defined to be reached when the surface losses are equal to the bulk core losses. (b) Critical thickness of the examined 3F4 material depending on the actual operating point $\{\hat{B}, f\}$.

crowding, especially if the assembly is composed of very thin plates and/or features small gap lengths. However, as analyzed in Appendix A.1, for a worst case machining and assembly tolerance, the plate thickness and gap length can be chosen such to minimize the resulting impact of flux crowding. The combination of using 3 mm plates and 100 µm gap length to implement the multi-gap sample examined in this study, results in a negligible contribution of flux crowding to the measured excess core loss in the multi-gap sample.

Very intriguing is also the fact that directly sintered plates still exhibit excess core loss in the same order of magnitude as the machined plates which contradicts the hypothesis that mechanical stress during machining is introducing the excess loss. However, it can be argued that the directly sintered plates also feature a layer of deteriorated ferrite performance close to the surfaces. These deteriorated layers are not caused by mechanical stress introduced during machining but from an altered Fe^{2+} / Fe^{3+} ion concentration in the iron oxide close to the surface. Among other factors, the oxygen concentration in the atmosphere during sintering strongly affects the balance between Fe^{2+} and Fe^{3+} ions. Since the plate surfaces are directly exposed to the atmosphere inside the controlled temperature ferrite processing chamber in contrast to the bulk, and a deviation from the ideal, temperature dependent O_2 concentration is inevitable in a practical setting. Thus, a shallow ferrite layer close to the surface is likely to exhibit adverse magnetic properties which is an explanation why there is also excess core loss present in case of the directly sintered plates.

6.6 Summary

A multi-gap inductor design can potentially reduce winding losses due to a reduction in magnetic air gap leakage field. Unfortunately, the manufacturing of a multi-gap core - composed of multiple stacked MnZn ferrite plates - can lead to an increase of core loss which potentially outweighs the saving in winding conduction loss. Based on literature, the dominating cause of the excess core loss are shallow layers of deteriorated magnetic performance just underneath the plate surfaces. A sophisticated calorimetric measurement approach based on temperature rise monitoring was developed, allowing to differentiate between and quantify bulk and surface core loss densities. Experimental results were presented for the MnZn ferrite material 3F4 from Ferroxcube. Reasons for the deteriorated surface are mechanical stress exerted during machining of the plates as suspected in literature and non-ideal conditions during sintering as suspected by the vendor. Several post machin-

ing treatments proposed in literature – annealing, etching and stress-free polishing with colloidal silica – have been applied to the machined plates in order to restore the original ferrite properties and reduce core loss, unfortunately without significant success so far. Accordingly, more work needs to be done, especially considering an annealing treatment with defined atmosphere and temperature profile recommended by the vendor. For this reason, the HF inductors implemented for the enhanced Little Box 2.0 presented in Chapter 4 are based on a conventional single-gap design. Moreover, NiZn ferrite should be examined in future work since it is known from literature that low-μ materials are less sensitive to mechanical stress. Thus, a multi-gap design using NiZn ferrite might not suffer from increased core losses as also the recent work in [148] seems to indicate.

7 Conclusion and Outlook

7.1 Google Little Box

During the course of this dissertation, two ultra-compact inverter systems in accordance with the technical specifications of the Google Little Box Challenge (GLBC) were developed. The first realized system, a two-level full-bridge based inverter topology with interleaved bridge-legs, TCM modulation with variable switching frequency in the range of 200 kHz – 1000 kHz, and a buck-type active power buffer using CeraLink capacitor technology, achieved a power-density of 8.18 kW/dm^3 (134 W/in^3) and a nominal efficiency of 96.4 %. This system was ranked among the top 10 out of 100+ teams in the final round of the GLBC. All systems presented at the finals of the GLBC were essentially engineering "jewels" with careful component arrangement and mechanical design using multiple PCBs and a careful heat management, but no fundamentally new approach or topology was presented. Likely because of the short competition time frame, inverter designs making use of advanced integration techniques, e.g. PCB embedding of power semiconductors, were also not presented at the finals of the GLBC. The key lessons learned and take away messages from the research during and after the GLBC are summarized in the following:

- Both GaN and SiC power semiconductors can do the job. 200 W/in^3 was reached with 900 V SiC MOSFET (Fraunhofer IISB).

- GaN transistors with zero reverse recovery promote the combined operation of soft- and hard-switching during an AC period (combining the merits of TCM modulation and PWM).

- Constant frequency PWM with EMI friendly 140 kHz and a comparably large current ripple turned out to be the sweet spot of the Google Little Box inverter optimization.
- Because of the low threshold voltage, GaN transistors require a negative gate bias to prevent parasitic dv/dt turn-on.
- Implementation of TCM modulation requires a FPGA and a robust current zero-crossings detection circuitry.
- There is no ideal switch: Despite superior properties of WBG semiconductor, ZVS losses are certainly not negligible when operating at high frequencies in the MHz range. In GaN HEMT/GIT technology, the observed residual switching losses are attributed to the lossy charging of the parasitic output capacitance (C_{oss}). Furthermore, dynamic $R_{\mathrm{ds,on}}$ phenomenon, still present in commercial devices, imposes a clear limitation on the maximal feasible switching frequency because of the increase in conduction losses.
- Active buffering of the 120 Hz pulsating AC-side power fluctuating with twice the mains-frequency by means of additional auxiliary converters reduces the volume of the energy storage but requires a careful selection and dimensioning of the installed buffer capacitors.
- Certain ceramic capacitors feature a high energy density but suffer from high power loss when operated with a low-frequency, large-amplitude voltage ripple.
- Stacking of individual chip capacitors to realize the respective capacitance value is unreliable because of the risk of micro cracks due to thermo-mechanical stress (CTE mismatch) exerted during assembly (soldering) and operation.
- MnZn ferrite materials exhibit low core loss at high frequencies but are very sensitive to mechanical stress. Machining of ferrite to implement inductors with distributed gap (multi-gap) potentially results in a substantial increase in core loss. The individual ferrite plates composing the multi-gap core segment should not be thinner than 3 mm.
- The size and arrangement of passives and the cooler (heat sink and fans) are finally determining the size of the systems.

- A single PCB design would be preferred in order to avoid connectors (volume and reliability concerns) but is difficult to achieve in practice due to the given dimension of the passives and the fans.

Incorporating all lessons learned from the GLBC, the second realized Little Box inverter presented in this dissertation is based on a 2-level DC/|AC| buck-stage operated with constant 140 kHz PWM and a subsequent LF full-bridge unfolder. Because of the inherently generated LF CM voltage, this topology was not considered initially but became a truly viable option once the specified ground current limit was relaxed from 5 mA to 50 mA at a very late point during the competition. The implemented "Little Box 2.0" prototype is also equipped with a buck-type power buffer but utilizes a better suited ceramic capacitor technology (450 V / X6S MLCC) and features a staggering power-density of 14.8 kW/dm^3 (243 W/in^3) and a nominal efficiency of 97.2 %. This sets a new experimentally confirmed benchmark in terms of power-density for a single-phase inverter and exceeds the minimum power-density requirement of the GLBC (50 W/in^3) by almost a factor of 5.

7.2 Partial-Power Approach

The concept of partial-power processing was analyzed in two different applications in this dissertation. It was demonstrated in Chapter 3, that an active hybrid power pulsation buffer, a combination of a conventional but reduced size passive buffered DC-link and a partial-power series voltage compensator, can achieve an excellent $\eta\rho$-performance. Compared to the analyzed Full Power Parallel Current Injector (FP-PCI) buffer, a major advantage of the presented hybrid buffer is the remarkable partial-load efficiency and, because of the still comparably large capacitance provided by the installed electrolytic capacitance, the excellent response to abrupt load changes. With respect to cost, it is possible to implement an all-electrolytic hybrid buffer design with, according to the conducted Pareto optimization, still acceptable power-density but at a very low expense of only $ 6 of total capacitor cost as opposed to the $ 290 needed to implement the 450 V / X6S FP-PCI buffer employed in the Little Box 2.0.

In Chapter 5 of this dissertation, the partial-power concept was used to provide tight output voltage regulation to a series-resonant LLC 380 V / 48 V DC/DC converter. Since the partial-power converter processes only a fraction of the rated power, the overall efficiency of the implemented LLC converter was only slightly reduced by 0.3 % (compared to an unregulated system and/or

system with constant voltage transfer ratio) and the total volume was only slightly increased by 10 % because of the added auxiliary converter. The implemented 1.5 kW DC/DC converter prototype achieved a power-density of 8.6 kW/dm^3 and a nominal efficiency of 97.7 %.

7.3 Core Losses in Multi-Gap Inductor

A sophisticated calorimetric measurement approach based on temperature rise monitoring was developed in order to differentiate between and quantify bulk and surface core loss densities in MnZn ferrite material 3F4 from Ferroxcube. Reasons for the deteriorated surface are mechanical stress exerted during machining of the plates as suggested by literature and non-ideal conditions during sintering as suggested by the vendor. Treatments such as annealing, etching and stress-free polishing with colloidal silica - have been applied to the machined plates in order to restore the original ferrite properties and reduce core loss, unfortunately without significant success so far. For this reason, the foil-winding multi air-gap (MAG) inductor originally developed for the first version of the Little Box inverter was not utilized in the revised Little Box 2.0 inverter. There, the RMS current stress was lower due to the employed PWM (instead of TCM modulation) and a single-gap inductor design with HF litz wire was considered. Accordingly, more work needs to be done to find ways to implement a distributed air-gap with MnZn ferrite as known from iron powder cores. Also, more research is needed to determine whether this surface related loss mechanism is also critical in NiZn ferrite.

7.4 Outlook and Future Requirements

Based on the currently available technologies, a further improvement of power-density can be achieved with a multi-level approach to shrink the size of the bridge-leg filter inductors and the EMI filter. However, as it becomes evident from the work in [25–27], the volume contribution of providing voltage and signal isolation to the individual switching cells of the flying capacitor converter is, besides the performance limitation imposed by the ceramic capacitors, one of the barriers for achieving a higher power-density. With advanced packaging and a higher level of integration, e.g. monolithic integration of gate-drive and GaN transistor, it would not come at a surprise to see power-density values exceeding 300 W/in^3 for this type of converter in the near future. Another strategy to further improve the power-density is to

more tightly incorporate the power buffer into the operation of the inverter as presented in [149–151], because this would allow to eliminate the bridge-leg filter employed in the active power buffer. This approach is the subject of current research and could potentially allow to improve the power-density of the Little Box 2.0 by another 10 % – 15 %.

The passive materials seem to evolve at a much lower pace compared to semiconductor technology. To further improve power-density, low-loss ceramic capacitors which tolerate a large LF AC ripple and feature a very high energy density are needed. This ceramic capacitor technology also must facilitate the implementation of large capacitor blocks in the range of 100 µF – 200 µF at a reasonable cost. Equally important is the availability of high-frequency low-loss magnetic materials with high saturation flux density and low permeability (distributed gap) to implement ultra-compact low-loss power inductors for very high switching frequencies. With the continuing progress of the semiconductor industry, the ideal switch might soon be in reach, enabling switching frequencies in the range of 10 MHz – 20 MHz in kW-scale DC/AC power conversion. Then, with further advances in material sciences and process technologies such as the promising Low Temperature Cofired Ceramics (LTCC)-technology, it might be possible in the near future to completely integrate filter passives for multi-kW power conversion in a single, PCB surface mountable, functional unit. It might one day even become feasible to manufacture fully customized integrated passives based on a customer defined small- and large-signal impedance characteristic.

Besides suitable passive materials, new control electronics – DSPs offering sufficient duty cycle resolution, gate-drive ICs, and high bandwidth low-volume current sensors – are required which support switching frequencies in the tens of MHz. Moreover, the development of such compact power electronics demand for new probes and transducers suited to measure high voltages and currents in a very confined space. To facilitate testing and debugging of such highly integrated power electronic systems, sensors and diagnosis tools are envisioned to be fully integrated into the converter already in the design phase to later facilitate testing and debugging during the system commissioning.

Appendices

A

Further Considerations Regarding Core Losses in MAG Inductor

Chapter Abstract

A multi-gap inductor design can potentially reduce winding losses due to a reduction in magnetic air gap leakage field. Unfortunately, as analyzed in detail in Chapter 6, the manufacturing of a multi-gap core – composed of multiple stacked MnZn ferrite plates – can lead to an increase of core loss which potentially outweighs the saving in winding loss. Based on literature, the dominating cause of the excess core loss are shallow layers of deteriorated magnetic performance just underneath the plate surfaces. Besides the deteriorated surface layers, flux crowding in the core due to tolerances and imperfections in machining and assembly of the ferrite plates was identified as a further cause for the observed increase in core loss and is analyzed in detail in this chapter. Moreover, besides the preferred calorimetric surface loss measurement technique presented in Chapter 6, a further technique to determine surface related core losses based on electrical measurements utilizing the widely accepted two-winding wattmeter method with reactive power compensation is outlined in this chapter.

A.1 Influence of Assembly and Machining Tolerances

In the multi-gap inductor design described in the introduction of Chapter 6, the center limb of the E-type core is composed of thin ferrite plates stacked on top of each other. These plates are either cut from a long ferrite bar by means of a diamond saw or are manufactured by pressing ferrite powder into the desired shape prior to sintering. Due to mechanical tolerance in the manufacturing processes, it is possible that the plate surfaces exhibit a convex or concave curvature or are not ideally coplanar. In order to establish

the correct gap length, a non-magnetic spacer material is inserted between the plates. The spacer, also intended to glue adjacent plates together, can be realized by means of a plastic film (e.g. Kapton or Mylar) with double sided adhesive or by a mix of epoxy resin with spherical silica powder as outlined in [31], where the latter allows gap lengths below 30 µm. Due to mechanical tolerances, it is possible that the plates in the stack are not ideally coplanar but slightly tilted.

In order to estimate how much these machining and assembly tolerances affect the core losses, a 2D FEM study was conducted. The static flux density distribution within the stacked plates considering a linear core material ($\sigma = 0,\ \epsilon_r = 1, \mu_r = 3000$) is computed based on Ampères's Law. In Fig. A.1(a), the impact of several machining/assembly tolerances on the flux density distribution is shown. The ideal multi-gap core, composed of 15×1 mm thick plates with a 30 µm gap, is depicted at the very left indicating a homogeneous flux density distribution. The flux density component normal to the plate surface (y-direction) averaged with respect to the plate width (x-direction) in the very center of the stack (cf. red line in the image on the very left of Fig. A.1(a)) for one ampere-turn of excitation is chosen as benchmark for an insightful comparison in per unit values. Since the effective permeability of the composite core changes depending on the magnitude of the simulated non-ideality, the excitation current is adopted accordingly such that the avg. flux density in y-direction in the center of the stack is identical under all considered scenarios. Introducing variable d_Δ to model tilt, curvature and non-coplanarity arising from mechanical tolerances, leads to a pronounced flux crowding as can be seen from the FEM simulation results in Fig. A.1(a). The impact of flux crowding on the actual core loss is estimated considering $p \propto B_{\mathrm{pu}}^{\beta}$ according to (6.1), where $\beta = 2.4$ in this study. The avg. loss density of the multi-gap core is then given by,

$$\overline{p} = \frac{1}{A} \cdot \iint_A p \mathrm{d}A = \frac{1}{A} \cdot \iint_A B^{\beta} \mathrm{d}A, \tag{A.1}$$

where A denotes the total core area of the stack. Fig. A.1(b) shows the avg. loss density for a fixed plate thickness and gap length ($d_{\mathrm{p}} = 1$ mm, $d_{\mathrm{gap}} = 30$ µm) but for a varying deviation. A tilt between plates has the most significant impact and results in an increase of the avg. loss density up to a factor of 2.3 for the worst considered error of $d_\Delta = 50$ µm. Note that the effective difference in gap length measured at both ends of the plate is actually twice d_Δ as indicated in Fig. A.1(a). Fig. A.1(c) depicts the avg. core loss density as a function of the gap length d_{gap} for a fixed plate thickness and the worst case

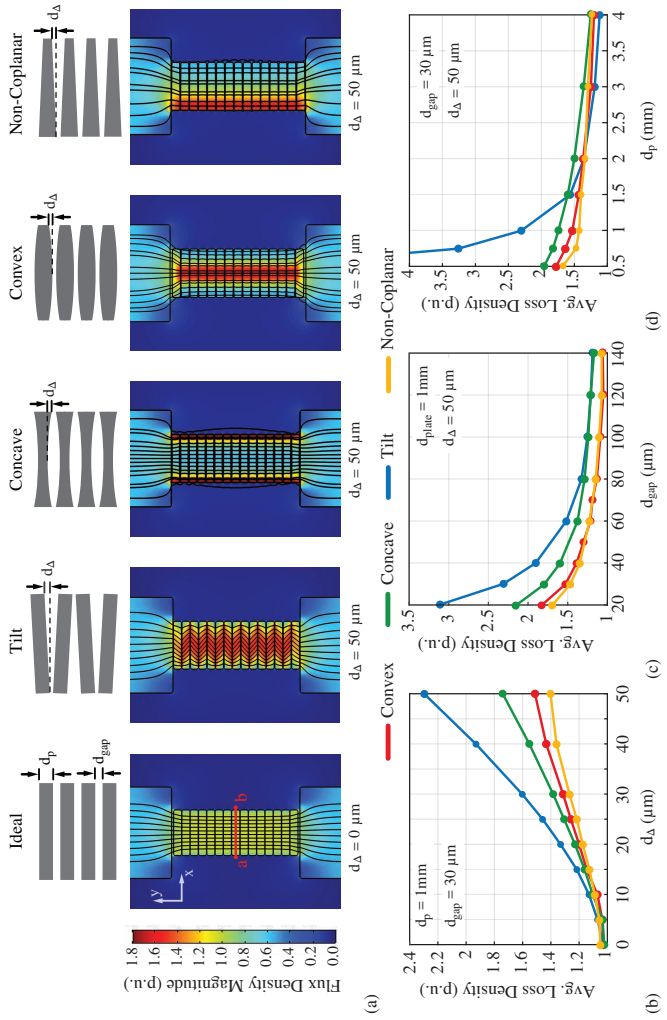


Fig. A.1: (a) 2D FEM field simulation results indicating the impact of several machining / assembly tolerances on the flux density distribution in the sample. (b) Avg. core loss density in the sample for a fixed plate thickness and gap length (d_p = 1 mm, d_gap = 30 µm) but for a varying deviation d_Δ. (c) Avg. core loss density in the sample as a function of the gap length d_gap for a fixed plate thickness d_p and the worst case error (d_Δ = 50 µm). (d) Avg. core loss density in the sample as a function of the plate thickness d_p for a fixed gap length d_gap and the worst case error (d_Δ = 50 µm).

error. It becomes evident, that increasing the individual gap length allows to mitigate the impact of the error on the loss density. Likewise, Fig. A.1 (d) depicts how the loss density reduces when the stack is composed of thicker plates. It can be concluded from this study that even if all plates feature undisturbed ferrite properties, an excess of core loss can still be observed in a multi-gap inductor due to machining and assembly tolerances. A deviation of $d_\Delta = 50\,\mu\text{m}$ might reflect a worst case scenario, but it is reasonable to expect a deviation of $d_\Delta = 10\,\mu\text{m} - 20\,\mu\text{m}$ in practice. For instance the standard deviation in plate thickness measured with a precision caliper at all four lateral faces amounts to 5 µm in case of the machined plates and to 23.7 µm in case of the direct sintered plates (cf. Section 6.4 and Section 6.5) provided by Ferroxcube for this study. In order to isolate and correctly quantify surface related core loss, the multi-gap samples employed to obtain the experimental data presented in Section 6.4 are constructed with 3 mm thick plates and 100 µm Mylar foil which limits the impact of mechanical tolerances on the measured core loss to less than 5 % for the (unlikely) worst case error.

A.2 Electrical Measurement of Surface Loss

Several electrical core loss measurement techniques have been presented in literature and a comprehensive overview is given in [152]. In the conventional two-winding wattmeter method, the core loss is calculated with the measured primary current and the induced voltage across a second auxiliary winding used to exclude ohmic losses of the excitation winding from the power measurement. The measurement error derived in [153] for a given phase-shift between voltage and current, φ_2, and a phase discrepancy introduced by the instrumentation, $\Delta\varphi$, is given by

$$\Delta = \tan(\varphi_2) \cdot \Delta\varphi \approx Q \cdot \Delta\varphi. \tag{A.2}$$

Thus, in order to minimize the potential measurement error caused by bandwidth limitations and/or uncompensated delays of the employed probes and to enable the characterization of high-Q, low-loss core materials at high frequencies, the sensitivity to phase errors is reduced by compensating the reactive impedance of the device under test (DUT) with a series connected capacitor or an air core inductor with opposing winding directions [153,154]. A disadvantage of this technique is that additional power loss from the resonance capacitor (or air core inductor) is included in the power measurement and must be subtracted from the total loss based on a loss model of the component. The basic circuit schematic of the two-winding method with resonance capac-

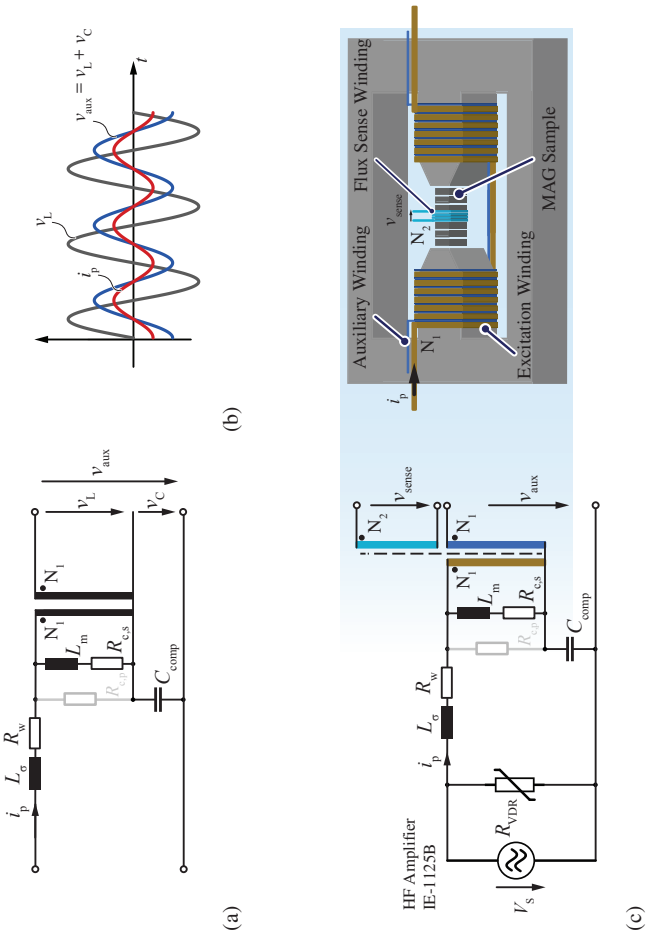


Fig. A.2: (a) Circuit schematic of the two-winding wattmeter method with resonance capacitor and (b) typical waveforms for sinusoidal excitation showing that the auxiliary voltage $v_{\mathrm{aux}} = v_{\mathrm{L}} + v_{\mathrm{C}}$ is in phase with the excitation current i_{p}. (c) Electrical core loss test circuit used in this study with additional sense winding with N_2 turns and a varistor at the input to protect the HF voltage source; for the two-winding wattmeter method to correctly exclude the winding loss, the excitation and auxiliary winding must feature close to ideal coupling. The sense winding in this work is not used for the power instrumentation but to ensure the correct flux density amplitude in the sample.

itor is shown in Fig. A.2(a) and typical waveforms for sinusoidal excitation are depicted in Fig. A.2(b), showing that the auxiliary voltage $v_{\mathrm{aux}} = v_{\mathrm{L}} + v_{\mathrm{C}}$ is in phase with the excitation current i_{p}. According to literature, the resistance modeling the core losses is typically drawn in series with the magnetizing inductance rather than in parallel since this facilitates a straightforward calculation of the losses for given primary current. Fig. A.2(c) shows the test circuit employed in this study with additional sense winding with N_2 turns and a varistor at the input to protect the HF voltage source (Iwatsu IE-1125B) from overvoltages. The sense winding is not used for the power instrumentation but to ensure the correct flux density amplitude in the sample as mentioned previously. For the two-winding wattmeter method to correctly exclude the winding losses, the excitation and auxiliary winding must feature close to ideal coupling. Now, the total losses measured with the test circuit are the sum of core losses in the E-type test circuit, P_{test}, the losses of the inserted multi-gap sample, P_{sample}, and the additional loss in the resonance capacitor, P_{cap},

$$\begin{aligned} P_{\mathrm{tot}} &= \frac{1}{T_{\mathrm{m}}} \int_0^{T_{\mathrm{m}}} v_{\mathrm{aux}} i_{\mathrm{p}} \mathrm{d}t \\ &= P_{\mathrm{sample}} + P_{\mathrm{test}} + P_{\mathrm{cap}}. \end{aligned} \tag{A.3}$$

As proposed at the beginning of Section 6.3, the total losses in the multi-gap core are the sum of the conventional core losses associated with the bulk ferrite material of the individual plates, $P_{\mathrm{sample,c}}$, and the surface related loss component, $P_{\mathrm{sample,s}}$. It follows that,

$$P_{\mathrm{tot}} = P_{\mathrm{sample,s}} + P_{\mathrm{sample,c}} + P_{\mathrm{core}} + P_{\mathrm{cap}}. \tag{A.4}$$

In order to extract $P_{\mathrm{sample,s}}$ from the total measured loss the following idea is proposed. For a specific operating point $\{\hat{B}, f\}$, two loss measurements using multi-gap samples with distinct number of gaps are carried out. The samples are constructed in such a way that the total ferrite core volume remains constant and the individual gaps are adjusted to achieve identical reluctance. An example of two samples with 5 and 15 plates is provided in Tab. A.1. It follows that for an identical reluctance of the two considered multi-gap samples, the equivalent reluctance of the entire magnetic test setup (test circuit and sample) remains constant and consequently the necessary excitation current to impress a specific flux density level in the sample will be equal. As a result, the losses of the test circuit and the resonance capacitor should ideally remain constant for a given operating point regardless of how

Tab. A.1: Two Distinct Samples With Identical Core and Total Gap Length

# Gaps	Plate Thickness	Gap Length	Sample Length
4	3 mm	175 µm	15.7 mm
14	1 mm	50 µm	15.7 mm

many gaps are present in the installed sample. Now, the difference of two loss measurements with samples featuring a total of u and v gaps, is given by

$$\Delta P^{(\mathrm{u},\mathrm{v})} = P^{\mathrm{u}}_{\mathrm{tot}} - P^{\mathrm{v}}_{\mathrm{tot}}, \tag{A.5}$$

$$\overset{(A.4)}{=} \left(P^{\mathrm{u}}_{\mathrm{sample,s}} + P^{\mathrm{u}}_{\mathrm{sample,c}} + P^{\mathrm{u}}_{\mathrm{test}} + P^{\mathrm{u}}_{\mathrm{cap}}\right) - \left(P^{\mathrm{v}}_{\mathrm{sample,s}} + P^{\mathrm{v}}_{\mathrm{sample,c}} + P^{\mathrm{v}}_{\mathrm{test}} + P^{\mathrm{v}}_{\mathrm{cap}}\right) \tag{A.6}$$

$$= P^{\mathrm{u}}_{\mathrm{sample,s}} - P^{\mathrm{v}}_{\mathrm{sample,s}}, \tag{A.7}$$

wherein $P^{\mathrm{u}}_{\mathrm{sample,c}} = P^{\mathrm{v}}_{\mathrm{sample,c}}$ because the samples are designed to feature identical bulk volume (neglecting minuscule surface layer volume difference between samples), and $P^{\mathrm{u}}_{\mathrm{core}} = P^{\mathrm{v}}_{\mathrm{core}}$, $P^{\mathrm{u}}_{\mathrm{cap}} = P^{\mathrm{v}}_{\mathrm{cap}}$ because of the identical reluctance and excitation current as mentioned previously. The surface loss in a sample with u gaps can furthermore be expressed as

$$P^{\mathrm{u}}_{\mathrm{sample,s}} = \tilde{\kappa}_{\mathrm{s}}(2(u+1)\cdot A_{\mathrm{p}}), \tag{A.8}$$

where $\tilde{\kappa}_{\mathrm{s}}$ is the surface loss density of plates with cross section A_{p}. Inserting (A.8) in (A.5) and rearranging yields

$$\tilde{\kappa}_{\mathrm{s}} = \frac{\Delta P^{(\mathrm{u},\mathrm{v})}}{2(u-v)\cdot A_{\mathrm{p}}}. \tag{A.9}$$

Thus by subtracting two measurements with identical operating point but using samples with different number of gaps the surface loss density can be extracted.

Unfortunately, the perfect cancellation of the test circuit power loss cannot be achieved in reality. Although it is quite challenging, it is possible to tune the gap length such that the impedance analyzer reads similar inductance values of the test circuit with either of the two samples installed. However, achieving a similar overall inductance value does not imply identical leakage flux conditions in the test circuit. Depending on the installed

sample (cf. Tab. A.1), a difference of up to 15 % – 20 % of required magnetization current for a specific flux density amplitude was observed during first preliminary measurements.

Now, from (A.8) and (A.9) it can be seen that the measurement error of the surface loss density is directly determined by the error in computing ΔP. The error in ΔP is not only affected by the error in the power instrumentation but also takes into account the systematic error arising from different leakage flux conditions in the test circuit and uncertainty in the ESR of the resonance capacitor which can be mitigated by using a large number of turns in the primary winding in order to keep current i_p low. Still, a rel. error of 15 % – 20 % in the P_tot loss measurement is a reasonable estimate. Furthermore, for a sample with 15 plates and a mid-range operating point {125 mT, 400 kHz} the actual surface loss amounts to just 20 % – 30 % of the total measured power, P_tot. It follows then that the relative measurement error of $\tilde{\kappa}_\mathrm{s}$ is likely in the range of

$$\frac{\sigma_{\tilde{\kappa}_\mathrm{s}}}{P_\mathrm{sample,s}} = \frac{(10\,\% - 15\,\%) \cdot P_\mathrm{tot}}{(20\,\% - 30\,\%) \cdot P_\mathrm{tot}} \approx 33\,\% - 75\,\%, \tag{A.10}$$

which is too pronounced to obtain robust experimental results for a comparison of different ferrite materials and to examine the impact of different machining/manufacturing techniques and post-machining treatments on the surface loss. Since a direct measurement of the sample loss reduces the relative measurement error significantly, the thermometric measurement technique based on accurate temperature rise monitoring as discussed in Section 6.3 of this dissertation was developed.

A.3 Summary

Due to mechanical tolerances, it is possible that the plates in the stack of a MAG core segment are not ideally coplanar but for instance exhibit a tilt. By means of a 2D FEM analysis, it was shown that for very thin plates (< 1 mm) and narrow gaps (< 50 µm), assembly imperfections can have a strong impact on the core losses due to flux crowding. However, if the thickness of the individual ferrite plates is larger than approximately 3 mm and the gap length between plates is larger than 100 µm, the impact of mechanical tolerances on the measured core loss is less than 5 % for the considered worst case assembly imperfection which allows to isolate and correctly quantify surface related core loss as presented in Section 6.4. Furthermore, it was explained that the electrical surface loss measurement technique based on the widely

known two-winding wattmeter method is not recommended for the accurate measurement of surface losses because of the high expected measurement error in the range of ≈ 33 % – 75 %.

B

Large-Signal Analysis of Ceramic Capacitors for Active Power Buffers

Chapter Abstract

In high power-density single-phase PV inverter systems, active auxiliary circuits are installed, shifting the double line-frequency power pulsation away from the DC-link to a dedicated buffer capacitor. Being relieved from strict voltage ripple requirements, a larger voltage ripple is allowed at the buffer capacitor, significantly reducing the capacitance requirements and consequently the overall volume of the converter system. Since the capacitance density of electrolytic capacitors must be derated because of imposed current limitations, ceramic capacitors become the preferred choice in power pulsation buffer applications. In particular, TDK's class II/X6S MLCCs with $BaTiO_3$ ceramic and the recently launched CeraLink capacitors with PLZT ceramic are promising candidates due to their high energy density. The actual prevailing capacitance of these two types of ceramics, strongly depends on the operating point, that is, a DC bias voltage and a superimposed large-signal amplitude AC voltage. Unfortunately, the large-signal behavior and performance of these ceramic capacitors is not specified by the manufacturer. In this chapter, a comprehensive characterization of the class II/X6S MLCC and the CeraLink capacitor large-signal performance is carried out by means of experimental measurements. The acquired data enables an accurate dimensioning of the power pulsation buffer capacitor and an estimate of the capacitor losses during operation. Since the device temperature has a strong impact on the ceramic properties, results for 30 °C, 60 °C and 90 °C are presented.

B.1 Introduction

In single-phase power electronic systems, typically bulky electrolytic capacitors are installed in order to cope with the intrinsic double line-frequency power pulsation. Aiming at the highest possible power-density of a single-phase PV inverter, active power decoupling techniques are applied [33, 34, 40], shifting the double line-frequency power pulsation away from the DC-link to a dedicated buffer capacitor. Being relieved from strict voltage ripple requirements, a much larger voltage swing is allowed at this buffer capacitor, resulting in drastically reduced capacitance requirements for the so called Power Pulsation Buffer (PPB) which also comprises a converter stage interfacing the buffer capacitor and the DC-link. In order to identify the most suited capacitor technology for PPB applications, a benchmark of selected class II ceramic capacitors, metalized polyester (PEN), metalized polypropylene (PP) and electrolytic capacitors with rated voltages between 50 V and 450 V is presented in [52]. Since the energy density of electrolytic capacitors must be derated because of lifetime associated current limitations, the benchmark revealed that 2.2 µF/450 V class II/X6S ceramic capacitors from TDK's C575 Multi Layer Ceramic Capacitor (MLCC) series feature by far the highest energy density.

Not included in the benchmark in [52] but considered in this chapter, is the recently launched CeraLink capacitor from TDK which is well suited for power electronic applications according to its promising properties [55, 155, 156]. In Chapter 3, a Pareto optimal design in terms of power-density of a 2 kW buck-type power buffer implemented according to the Google Little Box Challenge specifications is presented. In order to accurately dimension the employed ceramic buffer capacitor and calculate the losses associated with the power pulsation in each iteration of the optimization procedure as described in Section 3.2.2, operating point dependent large-signal performance data of the class II/X6S MLCC and the CeraLink capacitor are needed. More specifically, the capacitance and loss density as a function of applied DC bias $V_{\mathrm{dc}} \in [0, 400]$ and superimposed double line-frequency AC voltage $V_{\mathrm{ac}} \in [0, 130]$ is required. Unfortunately, comprehensive large-signal capacitance and loss data of ceramic capacitors is not provided by the manufactures and is also lacking in scientific literature. In [52] only a single operating point, 225 V DC bias and 450 V_{pp} AC excitation, is provided for the class II/X6S MLCC. Therefore, in this chapter experimentally determined large-signal performance data of the two most promising capacitor candidates, a 2.2 µF, 450 V class II/X6S MLCC and a 2 µF, 650 V 2$^{\mathrm{nd}}$ generation CeraLink capacitor are presented. Since the

performance of the considered ceramic materials is strongly affected by the operating temperature, the experimental results for 30 °C, 60 °C and 90 °C device temperature are provided. An introductory comparison between the two considered ceramic capacitor technologies considered in this work is given in Section B.2. The experimental setup, similar to the one presented in [52], and the measurement principle to determine the capacitance and loss density of the capacitors is presented in Section B.3. The obtained results are presented and discussed in Section B.4.

B.2 Class II/X6S MLCC vs. CeraLink Capacitor

MLCCs are divided in three application classes (according to IEC/EN 60384-1), depending on the relative permittivity and the stability with respect to voltage, temperature and frequency of the ceramic material. Class II ceramics are made of ferroelectric materials such as Barium Titanate ($BaTiO_3$) and are therefore well suited for energy storage application due to the high relative permittivity. Adversely, the relative permittivity of Barium Titanate based ceramics is not constant but strongly depends, among several other factors, on the applied DC bias and AC excitation [157], [158]. With increasing DC bias voltage, the effective capacitance of class II ceramics drastically drops, decreasing capacitance density at operating voltage levels. Depending on the used additives in the ceramic compositions, various temperature ranges such as X5R, X6S, Y5V etc. are available. The first letter of the code specifies the minimum operating temperature, the digit defines the upper temperature and the last letter defines the deviation from the nominal capacitance over the operating temperature range. The class II/X6S MLCC considered here can be operated from −55 °C to 105 °C with a change in capacitance of $^{\Delta C}/_{C} = \pm 22\,\%$.

By contrast, the novel CeraLink capacitor technology consists of a Lead-Lanthanum-Zirconate-Titanate (PLZT) ceramic composition whose crystal structure is tuned such to exhibit anti-ferroelectric behavior if no voltage is applied. By applying an electrical field, it is energetically more favorable for the anti-parallel polarized domains to switch into a parallel configuration. By switching the domains, additional energy can be stored which appears as an increase of the dielectric permittivity under field. When exceeding this maximum "switching level" by even stronger electrical fields, a ferroelectric behavior with decreasing permittivity is observed [55, 155, 156]. The level of the maximum permittivity can be adjusted by variation of the dielectric layer thickness of the multilayer capacitor's design. As a consequence, the CeraLink capacitor offers high capacitance at DC-link voltage levels.

Tab. B.1: Comparison of Class II/X6S MLCC and CeraLink Capacitor.

	TDK Class II/X6S MLCC	TDK CeraLink
Material	$BaTiO_3$	PLZT
Capacitance	2.2 µF [1]	2.0 µF [2]
Dimensions	5.7 x 5 x 2.5 mm	7.3 x 8 x 2.7 mm
Volume	0.07 cm^3	0.16 cm^3
Current Rating	1 A/µF, $f > 100$ kHz	5 A/µF, $f > 100$ kHz
Max. voltage	450 VDC	650 VDC
Max. temperature	105 °C	125 °C

[1] Nominal capacitance at 0 VDC bias.
[2] Typ. nominal capacitance at $V_{op} = 400$ VDC.

Several properties of a single capacitor class II/X6S MLCC and CeraLink chip are compared in Tab. B.1, emphasizing that the CeraLink capacitor is rated for voltages up to 650 VDC in contrast to the maximum permissible operating voltage of 450 VDC in case of the class II/X6S MLCC. The 2nd generation CeraLink prototypes provided by TDK for the implementation of the Little Box (cf. Chapter 4) were tuned such to exhibit the highest rel. permittivity around a bias of 375 V. The inner electrodes of the class II/X6S MLCC are made from Nickel (Ni), which is a standard material for inner electrodes in ceramic capacitors. CeraLink's PLZT ceramic is able to be cofired with copper inner electrodes, which enables optimal thermal conductivity and lowers electrical losses, especially in the high-frequency regime.

The class II/X6S MLCC comes in a monolithic SMD package where the outer terminations, a fired copper paste covered with plated Ni/Sn layers, are directly soldered onto the PCBs. In case of the CeraLink capacitor, individual ceramic chips are connected to a multilayered metal lead frame consisting of copper and invar steel with silver galvanics in order to increase the robustness with respect to mechanical load (PCB bending, mismatch of thermal expansion during soldering) and decrease thermomechanical stress by matching the resulting thermal expansion coefficients of the materials involved.

A sputter layer of chromium, nickel and silver is applied to the lapped PLZT surface which is then connected to the lead-frame by means of a μ-silver sinter process. This assembly process achieves a highly reliable connection with low ESR and ESL, optimized thermal conductivity and enables the construction of large modules (up to 100 µF). By contrast, since the class II/X6S MLCCs are only available as single chips, realizing a large capacitance value

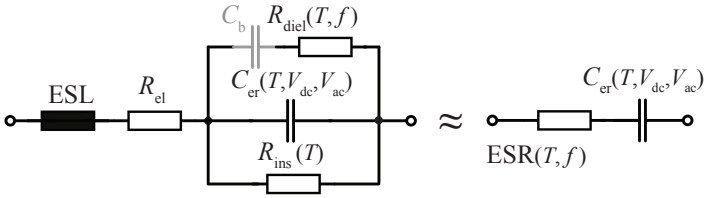


Fig. B.1: Lumped parameter circuit to model the losses in ceramic capacitors.

makes it necessary to mount a large number of individual capacitors onto the PCB.

A lumped parameter circuit can be used to model the different loss mechanisms in ceramic capacitors as presented in [156]. The basic model as shown on the left in Fig. B.1 includes a parasitic inductance ESL and several resistors to model the different loss mechanism in ceramic capacitors. Resistor R_{el} connected in series with the capacitor C_{er} models the losses caused by the resistance of the electrodes. The DC losses caused by the leakage current of the dielectric material are modeled with R_{ins} connected in parallel to C_{er}. The hysteresis losses which occur in the dielectric material when excited with a large voltage swing are modeled with $R_{\mathrm{diel}} = \frac{\alpha 2\pi}{\omega}$ with material constant α, connected in series with DC blocking capacitor C_b. According to [156], the total losses are given by

$$\begin{aligned} P_{\mathrm{tot}} &= \frac{U_{\mathrm{dc}}^2}{R_{\mathrm{ins}}} + I_{\mathrm{AC,rms}}^2 \cdot \underbrace{\left(R_{\mathrm{el}} + \frac{1}{\omega} \frac{\alpha \cdot 2\pi}{1 + (\alpha \cdot 2\pi C_{\mathrm{er}})^2} \right)}_{\mathrm{ESR}} \\ &\approx I_{\mathrm{AC,rms}}^2 \cdot \mathrm{ESR}, \end{aligned} \tag{B.1}$$

where the losses associated with the finite insulation resistance are typically negligible. In Fig. B.2 the ESR over frequency is shown for the class II/X6S MLCC and the CeraLink capacitor. At 25 °C, the class II/X6S capacitor has lower resistance at frequencies below 1 MHz, while the CeraLink prototype shows lower values at higher frequencies. Below 1 MHz, the ESR is dominated by the dielectric resistance R_{diel} which decreases with frequency. At higher frequencies the resistance of the conductors (inner electrodes, terminations, and junction resistances) exceed the dielectric resistance. As can be seen, the ESR starts to increase again at high frequencies which can be explained by the skin effect in the conductors of the capacitors [156]. The difference in ESR in the high frequency range are caused by the different inner electrode

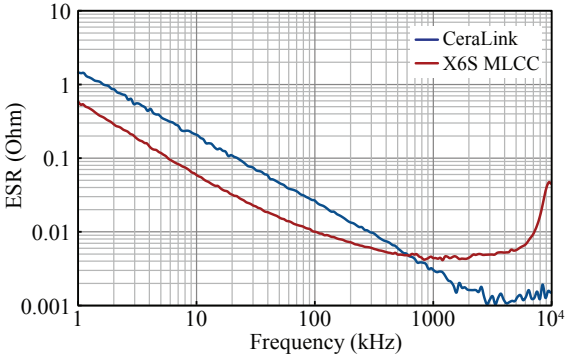


Fig. B.2: Comparison of small-signal ESR over frequency measured at 25 °C with 0 V DC bias and 0.5 V rms AC excitation.

material of the two capacitors. As mentioned above, the CeraLink prototype uses electrodes made out of copper, whereas the class II/X6S MLCC uses electrodes made out of nickel, and the specific resistance of copper is approx. a factor of 4 lower then nickel. Although the ESR of the CeraLink capacitor drops drastically with temperature as shown in Fig. B.3, the low-frequency dielectric losses are still substantial. This is also nicely illustrated in Fig. B.4 where the change in stored charge

$$\Delta Q_c(t) = \int_{t_0}^{t_0+t} i_c(\tau)\mathrm{d}\tau \tag{B.2}$$

with respect to the capacitor voltage is plotted for a 120 Hz cycle at 60 °C operating temperature. Clearly visible is the pronounced hysteresis of the CeraLink capacitor, which indicates significantly higher losses compared to the class II/X6S MLCC which features a much smaller width of the hysteresis loop. Furthermore, Fig. B.2 illustrates the change of relative permittivity with respect to applied DC bias of both ceramic materials considered herein. At low bias voltage the ferroelectric material exhibits a higher relative permittivity ($\epsilon_{\mathrm{X6S,I}} > \epsilon_{\mathrm{Cera,I}}$). Increasing the bias voltage to 350 V DC, significantly increases the relative permittivity of the PLZT ceramic while decreases the relative permittivity of the $BaTiO_3$ ($\epsilon_{\mathrm{Cera,II}} > \epsilon_{\mathrm{X6S,II}}$). As indicated in Fig. B.1, the lumped parameters of the capacitor model strongly depend on temperature, applied voltage amplitude and frequency. The dielectric losses modeled with $R_{\mathrm{diel}}(T, f)$ depend strongly on operating temperature and on the frequency of the applied AC voltage. The effective capacitance $C_{\mathrm{er}}(T, V_{\mathrm{dc}}, V_{\mathrm{ac}})$ depends

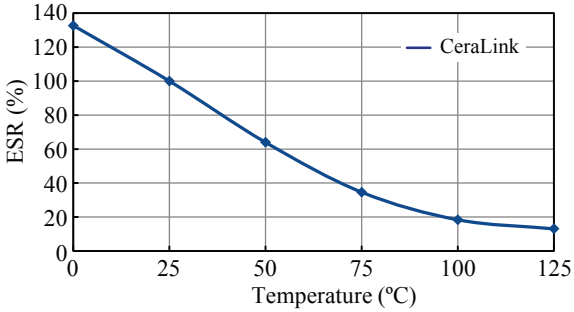


Fig. B.3: ESR over temperature of the CeraLink capacitor. Measurement conditions: 400 V DC bias, 0.5 Vrms, 1 kHz AC excitation.

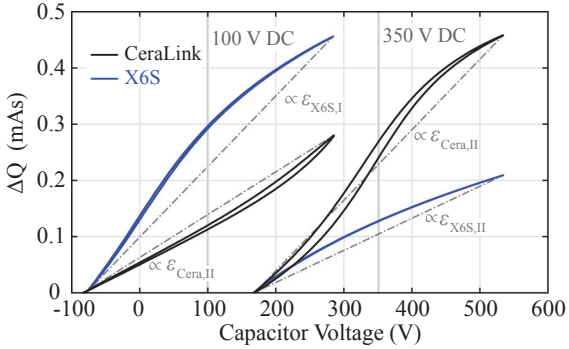


Fig. B.4: Change in stored charge in a single CeraLink and class II/X6S MLCC chip with respect to applied voltage at 60 °C for 100 V and 350 V DC bias. Clearly visible is the pronounced hysteresis of the CeraLink capacitor.

primarily on the applied DC bias but also on the AC voltage and the operating temperature. The experimental results presented in Section B.4 of this chapter confirm these dependencies.

The current rating listed in Tab. B.1 is determined by the self-heating of the capacitor

$$\Delta T = I_{\mathrm{AC,rms}}^2 \cdot \mathrm{ESR} \cdot R_{\mathrm{th}}, \tag{B.3}$$

where the thermal resistance R_{th} models the cooling of the capacitor and depends on the thermal resistance of the capacitor, the PCB and the applied cooling method (convection, forced-air cooling etc.). The specification of the class II/X6S MLCC is different from the CeraLink capacitor in terms of the allowed self-heating.

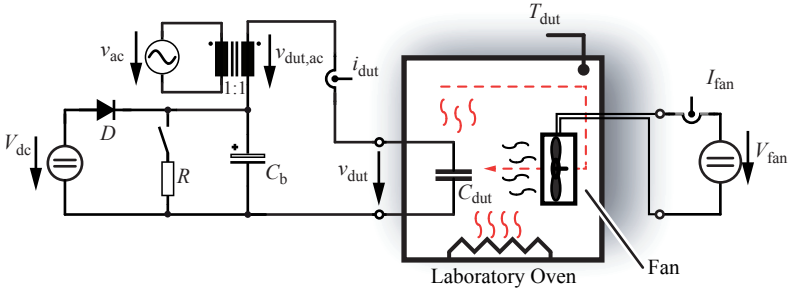
The class II/X6S MLCC is allowed to have a maximum operating temperature of 105 °C and a maximum ΔT of 20 °C [159]. The temperature rise is limited because due to self heating by ripple currents together with the comparably low thermal conductivity yielding temperature gradients within the ceramic body. As a result, the thermomechanically induced stress yields to cracking and ultimately to malfunction of the ceramic.

By contrast, the CeraLink capacitor's maximum permissible change in temperature ΔT is not restricted as long as the maximum operating temperature of 125 °C is not exceeded. Due to the good thermal conductivity of the whole module, no malfunction due to hotspot formation was observed so far.

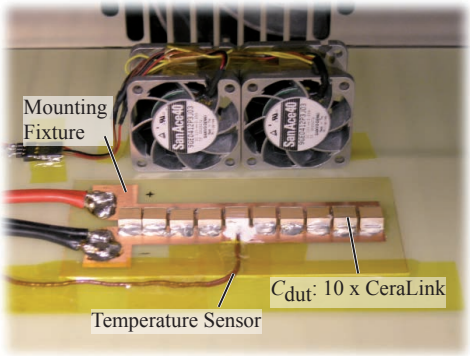
B.3 Experimental Setup and Measurement Procedure

As mentioned in the introduction, the performance of the device under test (DUT), here the class II/X6S MLCC and CeraLink capacitor, must be determined under operating conditions similar to those present in power pulsation buffers. The test setup used to adjust the operating point of the ceramic capacitors is schematically shown in Fig. B.5(a). The voltage applied to the capacitor under test C_{dut} is composed of a DC bias and a superimposed AC ripple voltage. A 600 V DC laboratory source is used to charge a large 1.9 mF electrolytic decoupling capacitor C_b. The output of an AC laboratory supply is connected in series with C_b and C_{dut} by means of a 1 : 1 isolation transformer. Since C_b is much larger than C_{dut}, the voltage across the capacitor under test is given by

$$v_{\mathrm{dut}}(t) = V_{\mathrm{dc}} + {}^{C_b}\!/_{(C_b+C_{\mathrm{dut}})} \approx v_{\mathrm{ac}} = V_{\mathrm{dc}} + v_{\mathrm{ac}}(t). \tag{B.4}$$



(a)



(b)

Fig. B.5: (a) Experimental setup to adjust the DC bias and AC ripple voltage applied to the ceramic capacitors under test. C_{dut} is enclosed in a laboratory oven in order to emulate different operating temperatures. (b) Picture of the test fixture with installed CeraLink capacitors inside the laboratory oven.

As shown in Fig. B.5(a), the DUT is enclosed in a laboratory oven in order to determine the performance of the DUT for several operating temperatures. In addition, a fan is used to extract the losses occurring in the ceramic capacitors during the experiments and facilitates heat distribution inside the oven. For each operating point $\{V_{\mathrm{dc}}, V_{\mathrm{ac}}\}$, the resulting voltage and current of the capacitor under test is measured with an oscilloscope equipped with appropriate voltage probe and current transducer. To increase measurement accuracy, specifically to increase signal-to-noise ratio of the current measurement at low AC voltage, and to average tolerances between individual capacitors, multiple capacitors (10 or more) were connected in parallel on a custom mounting fixture as depicted in Fig. B.5(b). Given the recorded measurements, the large-signal characteristics of the capacitor under test are calculated in Matlab. Fig. B.6 shows typical voltage and current waveforms and the calculated instantaneous power $p_{\mathrm{dut}}(t) = u_{\mathrm{dut}} \cdot i_{\mathrm{dut}}$ of a measurement performed with class II/X6S capacitors at 30 °C. In Fig. B.6(a) an operating point with significant DC bias and AC excitation such that $v_{\mathrm{dut}}(t) > 0,\ \forall t$, is depicted. Considering an energy-related capacitance model with large-signal equivalent capacitance $C_{\mathrm{er,dut}}$, the difference in stored energy

$$\Delta E_{\mathrm{dut}} = 1/2 \cdot C_{\mathrm{er,dut}} \left(\max(|v_{\mathrm{dut}}|)^2 - \min(|v_{\mathrm{dut}}|)^2 \right) , \tag{B.5}$$

is delivered by the AC source within the time interval $t_0 = 0$ and $T_m/2$

$$E_{\mathrm{src}} = \int_{t_0}^{T_m/2} p_{\mathrm{dut}}(t)\, \mathrm{d}t = \int_{t_0}^{T_m/2} u_{\mathrm{dut}} \cdot i_{\mathrm{dut}}\, \mathrm{d}t. \tag{B.6}$$

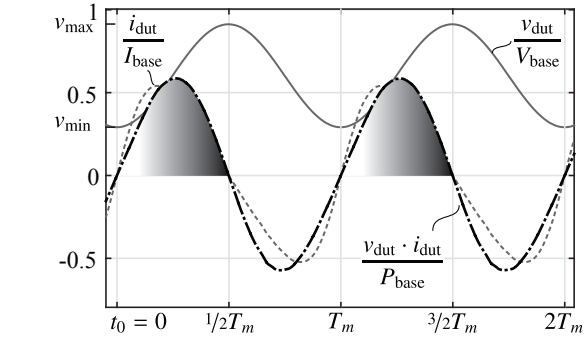
Expression (B.6) also includes the energy which is dissipated during the charging process. The total occurring power loss within one cycle is calculated according to

$$P_{\mathrm{loss,dut}} = \frac{1}{T_m} \int_0^{T_m} u_{\mathrm{dut}} \cdot i_{\mathrm{dut}}\, \mathrm{d}t. \tag{B.7}$$

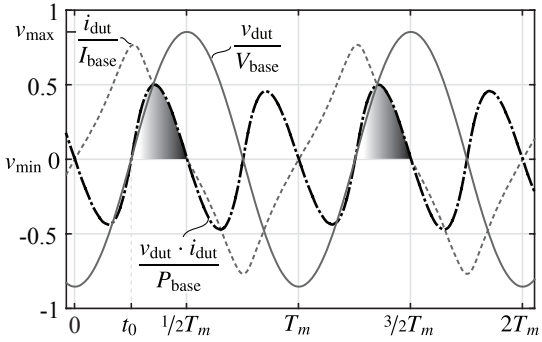
Assuming that the total power loss is equally distributed over the charging and discharging interval, the energy related large-signal capacitance at a given operating point is calculated by means of

$$C_{\mathrm{er,dut}} = \frac{2 \cdot \left(\int_{t_0}^{T_m/2} u_{\mathrm{dut}} \cdot i_{\mathrm{dut}}\, \mathrm{d}t - \frac{1}{2} T_m P_{\mathrm{loss,dut}} \right)}{\max(|u_{\mathrm{dut}}|)^2 - \min |(u_{\mathrm{dut}}|)^2}. \tag{B.8}$$

The integration of the power is started at t_0 when the capacitor voltage reaches minimum in case of $v_{\mathrm{dut}}(t) > 0,\ \forall t$ (cf. Fig. B.6(a)). If the applied



(a)



(b)

Fig. B.6: Measured voltage v_{dut} and current i_{dut} waveforms and calculated instantaneous power of the DUT, where v_{dut} exhibits a DC bias and superimposed AC voltage in (a) and solely an AC voltage in (b).

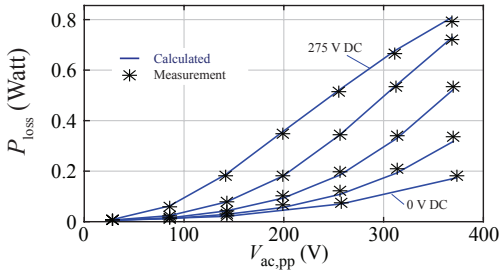


Fig. B.7: Comparison between calculated losses according to (B.7) and measured losses with Yokogawa power analyzer. Depicted are the losses that occur in a single CeraLink chip with respect to applied AC excitation and several DC bias voltages at 60° operating temperature.

AC voltage is large enough that the voltage across the DUT also becomes negative, then the start of integration t_0 is postponed to coincide with the zero crossing of the capacitor voltage as shown in Fig. B.6(b). Note, that in this case $\min(|u_{\text{dut}}|) = 0$. The power loss computed with equation (B.7) includes the ohmic losses in the electrodes and terminals of the capacitor, the losses caused by the leakage current and the losses in the dielectric material due to the large-signal voltage swing. It is essential to carefully deskew voltage and current probes before the measurement, since just a small error in phase-shift can lead to arbitrary wrong results when evaluating (B.7). In order to check the accuracy of the numerical loss calculation, the losses of the capacitor under test were also measured by means of a Yokogawa WT3000 power analyzer connected at the secondary side of the isolation transformer (not shown in Fig. B.5(a)). Fig. B.7 shows the excellent accordance between directly measured and calculated losses obtained for a single CeraLink capacitor at 60 °C operating temperature.

B.4 Empirical Large-Signal Capacitance and Power Loss

The measurement principle outlined in the previous section was carried out for a large number of discrete operating points. For each applied DC bias voltage in the discrete set $\{0, 100, 150, 200, 250, 300, 350, 400\}$ V, measurements at 120 Hz sinusoidal AC voltages with amplitudes in the set

$\{10, 30, 50, 70, 90, 110, 130\}$ V rms were performed. These measurements were carried out at 30 °C, 60 °C and 90 °C operating temperature. To refine the coarse grid of measurement points, a two-dimensional piecewise cubic interpolation was performed in MATLAB.

A contour plot of the interpolated large-signal capacitance obtained for the CeraLink capacitor and the class II/X6S MLCC is shown in Fig. B.8. Since the capacitors considered differ in volume, the capacitance per volume is plotted to allow a direct comparison. In the right column of Fig. B.8 the capacitance density of the class II/X6S MLCC is depicted, which strongly reduces with increasing DC bias as expected from a class II ceramic. At 30 °C operating temperature, a maximum capacitance density of $24.87\,\mu F/cm^3$ occurs at zero DC bias and small AC amplitude. Given the volume of a single class II/X6S chip of $0.07\,cm^3$, the capacitance of $24.9\,\mu F/cm^3 \cdot 0.07\,cm^3 = 1.7\,\mu F$ per chip was measured. The capacitance density is almost constant with respect to the applied AC voltage up to $100\,V_{pp}$, and then reduces significantly with increasing AC amplitude. However, if a DC bias larger than 250 V is applied, then the capacitance density becomes almost independent of the large-signal AC excitation. The elevated operating temperatures have only a small effect on the class II/X6S MLCC, but it can be noticed that for DC bias levels greater 150 V the capacitance density increases.

The contour plot of the capacitance density of the CeraLink capacitor, shown in the left column in Fig. B.8, illustrates the unique feature of increasing capacitance with DC bias as described earlier in Section B.2. At 30 °C operating temperature, the maximal capacitance density of $10\,\mu F/cm^3$ occurs at $V_{dc} = 350\,V$ and $V_{ac,pp} = 140\,V$. Given the volume of a single CeraLink chip of $0.16\,cm^3$ (roughly twice the volume of a single class II/X6S chip), a maximal capacitance of 1.6 µF per single chip was measured. Increasing the DC bias above 350 V reduces the effective capacitance again. Up to $V_{dc} \approx 280\,V$, the capacitance density of the CeraLink capacitor increases steadily with the amplitude of the applied AC voltage. Increasing the DC bias voltage further, an optimal AC amplitude in terms of capacitance emerges at $V_{ac,pp} = 140\,V$ in case of 30 °C operating temperature. Increasing the operating temperature of the CeraLink capacitor, shifts the maximum capacitance density to both smaller DC bias and AC amplitude. Furthermore, the peak of the capacitance density is slightly flattened when the operating temperature increases, clearly visible in the transition from 60 °C to 90 °C temperature.

The power loss per chip volume occurring in the CeraLink capacitor and class II/X6S MLCC during continuous operation with the respective applied DC bias and AC excitation is shown in Fig. B.9. Naturally, the highest loss

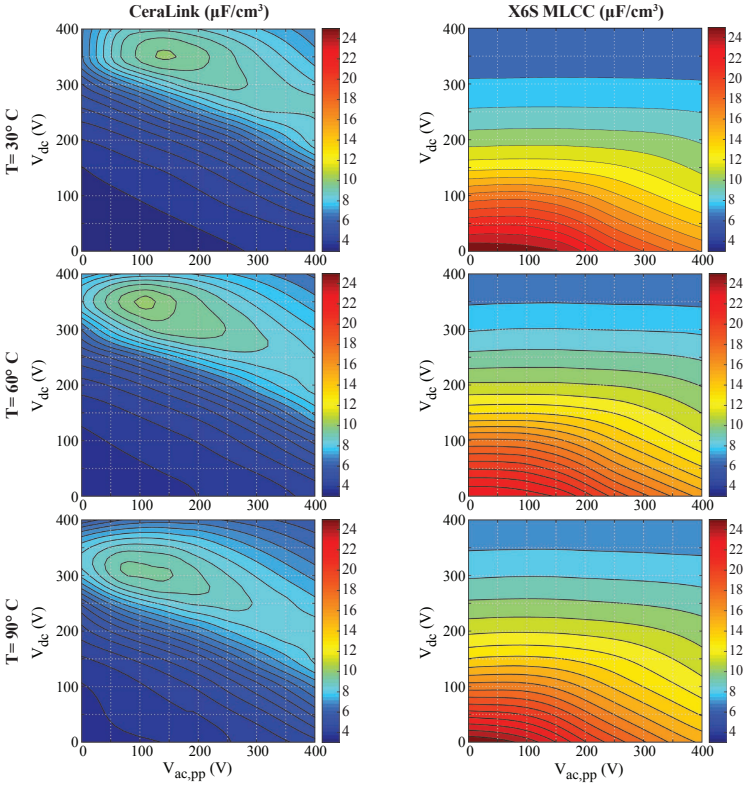


Fig. B.8: Contour plot of capacitance density with respect to DC bias V_{dc} and 120 Hz AC excitation $V_{\mathrm{ac,pp}}$ at 30 °C, 60 °C and 90 °C operating temperature.

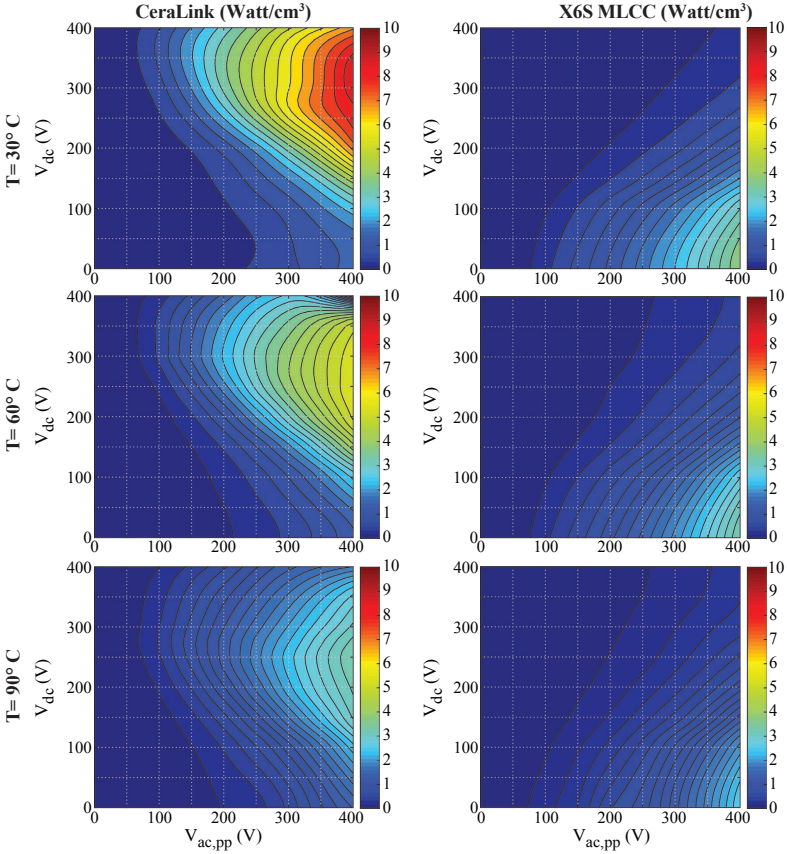


Fig. B.9: Contour plot of loss density with respect to DC bias V_{dc} and 120 Hz AC excitation $V_{\mathrm{ac,pp}}$ at 30 °C, 60 °C and 90 °C operating temperature.

density occurs in the region of the $\{V_{dc}, V_{ac}\}$ space where the combination of large prevailing capacitance and large applied AC voltage is present. At around zero DC bias, the dielectric loss density of the class II/X6S MLCC increases quadratically with applied AC voltage reaching its maximum of $3.9\,\mathrm{W/cm^3}$ at the largest applied ripple voltage ($400\,\mathrm{V_{pp}}$). Since the reactive power reduces with increasing DC bias due to the lower effective capacitance, the associated power losses reduce accordingly. Increasing the operating temperature of the class II/X6S MLCC has just a minor impact on the power losses. The peak loss density reduces by a factor of 0.89 to $3.5\,\mathrm{W/cm^3}$ at 90 °C operating temperature.

In case of the CeraLink capacitor, shown in the left column in Fig. B.8, the domain of high power loss shifts to larger DC bias voltages. At 30 °C device temperature, a maximal loss density of $9\,\mathrm{W/cm^3}$ occurs at $V_{dc} = 300\,\mathrm{V}$, $V_{ac,pp} = 400\,\mathrm{V}$. It can be clearly seen that the power losses strongly decrease with device temperature, which was anticipated from the behavior of the ESR with respect to temperature as depicted earlier in Fig. B.3. Increasing the temperature to 90 °C, decreases the peak power loss density by a factor of 0.38 to $3.4\,\mathrm{W/cm^3}$.

In order to directly compare the performance of both capacitors in a realistic active power buffer application, a typical buffer capacitor operating point is studied. One of the two implemented buck-type power buffer versions presented in Subsection 3.2.4 is equipped with a 150 µF buffer capacitor. The buffer capacitor is operated with a DC bias of 300 V and a superimposed AC voltage with $130\,\mathrm{V_{pp}}$ amplitude. Furthermore, the steady-state temperature at rated power of the converter is in the range of 60 °C. Considering the experimental results in Fig. B.8, the class II/X6S MLCC features a capacitance density of $8.4\,\mathrm{\mu F/cm^3}$, as opposed to the slightly higher $9.5\,\mathrm{\mu F/cm^3}$ of the CeraLink capacitor. The loss density of the class II/X6S MLCC at the considered operating point amounts to just $56\,\mathrm{mW/cm^3}$. By contrast, the CeraLink capacitor dissipates $1.15\,\mathrm{W/cm^3}$ in the very same operating point, which would reduce to $0.6\,\mathrm{W/cm^3}$ if a device temperature of 90 °C would be feasible. It can be concluded, that although the CeraLink capacitor features a higher capacitance density, the power losses caused by the 120 Hz voltage ripple are much higher than those of the class II/X6S MLCC.

B.5 Summary

Because of their high energy density, TDK's class II/X6S MLCCs and CeraLink capacitors were identified to be the most promising candidates for realizing

an ultra-compact power buffer. The prevailing capacitance of these two types of ceramics, $BaTiO_3$ and PLZT, strongly depends on the operating point, that is DC bias voltage and superimposed large-signal amplitude, double line-frequency AC voltage. In Section B.2 the basic properties of both capacitor technologies were compared. Despite the fact that the CeraLink capacitor was developed to be primarily used as DC-link snubber, and thus was optimized to feature a very low ESR at high frequency, high capacitance at DC-link voltage levels and a high current capability, it was chosen as a candidate for an active power buffer.

In this particular case, the ESR of the CeraLink capacitor at double line-frequency is significantly larger than that of the class II/X6S MLCC. Class II ceramics, $BaTiO_3$ in case of the X6S, exhibit a reduction in capacitance with increase in bias voltage. By contrast, the PLZT ceramic used in the CeraLink capacitor exhibits an increase in capacitance with applied DC voltage. Besides the DC bias, also the applied AC voltage affects the actual available capacitance of both ceramic capacitors. In order to accurately dimension a buffer capacitor in practice, the large-signal performance of the class II/X6S MLCC and CeraLink capacitor was experimentally determined in this chapter. Both the energy related capacitance density and the power loss density with respect to applied DC bias and superimposed AC voltage were determined for 30 °C, 60 °C and 90 °C operating temperature.

Direct comparison at a typical operating point occurring in a PPB application revealed that the capacitance density of the CeraLink capacitor is just slightly higher compared to the class II/X6S MLCC, while the power losses associated with the double line-frequency voltage ripple are significantly higher in case of the CeraLink capacitor (factor 10 higher at 90 °C). Based on the measured large-signal performance, the class II/X6S MLCC is the preferred choice in 400 V power buffer applications if the operating temperature is < 105 °C and frequencies are kept low.

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