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SYSTEM-ORIENTED EFFICIENCY OPTIMIZATION OF VARIABLE SPEED DRIVES

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Abstract

Low-voltage variable speed drive (VSD) systems are among the most important consumers of electrical energy in industry. Such systems are subject to tremendous cost pressure and are traditionally built with the simplest possible power electronic converter satisfying the requirements. Enabling a bidirectional power flow, the 2-level voltage source back-to-back converter was and still is the standard industry choice due to its low purchase costs. Recently, there is a trend towards increasing electrical energy prices because of declining fossil energy reserves and the subsidies accelerating the change towards renewable energy sources. Therefore, the operating expenses of a VSD system become more and more important and lead to a reconsideration of the purchase costs, making systems with higher energy efficiencies more competitive.

The main goal of this thesis is to give a comprehensive, system oriented efficiency analysis and optimization of a modern low-voltage VSD system. This holistic approach includes all components of such a system, namely the EMI input filter, the power electronic converter, the load machine, possible interactions among them and impacts of control strategies. Consequently, loss models of all subsystems are developed and interconnected in order to consider mutual interactions.

State-of-the-art converter topologies that are uncommon in low-voltage applications, such as the 3-level T-type topology, or the 3-level NPC topology, have advantageous properties concerning converter efficiency and have additional beneficial impacts on the surrounding, such as harmonic losses in the load machine and in the filtering components. A detailed analysis reveals that despite the increased initial costs, these alternative topologies enable to build a modern VSD system outperforming the standard industry solution in several aspects, namely the system energy efficiency, the necessary semiconductor chip area and

the filtering effort. The complexity and the implementation effort are thoroughly compared to the standard 2-level converter solution.

Incorporating modern control concepts further increases the possible energy savings of the VSD system. The efficiency of the widely used induction machine can be increased by using an efficiency optimal control strategy for low torque operation. The rotor flux of the machine is decreased, which reduces iron losses and ohmic losses related to the magnetization current. Due to the changed operating point, the machine control concept has again an impact on the converter losses. Similarly, active damping concepts enable to remove passive damping branches of the EMI input filter and therefore can reduce losses, volume, and costs of the EMI filter. As these active damping methods change the converter behavior, the stability of the 3-phase system is analyzed carefully using MIMO system methods based on impedance matrices.

Finally, a modern, highly efficient, and competitive VSD system is proposed, using the 3-level T-type converter and incorporating enhanced control concepts to reduce the energy consumption throughout the whole drive system.

Kurzfassung

Niederspannungsantriebe gehören zu den wichtigsten industriellen Verbrauchern elektrischer Energie. Diese Systeme sind einem ständigen Kostendruck ausgesetzt und werden traditionellerweise mit den einfachsten leistungselektronischen Konvertern realisiert, welche die gestellten Anforderungen erfüllen. Der Zweipunkt-Spannungszwischenkreisumrichter ermöglicht einen bidirektionalen Energiefluss und ist wegen den niedrigen Anschaffungskosten zur Standardlösung im industriellen Umfeld geworden. Seit einiger Zeit sind jedoch steigende Strompreise zu beobachten, die hauptsächlich auf schwindende Reserven konventioneller Energieträger und auf die Finanzierung des Ausbaus erneuerbarer Energiequellen durch die Verbraucher zurückzuführen sind. Deshalb werden die laufenden Betriebskosten von Antriebssystemen immer wichtiger und führen zu einer Neubeurteilung der Anschaffungskosten, verbunden mit einer ökonomischen Verschiebung der Rentabilität zu hocheffizienten Systemen.

Das Hauptziel dieser Dissertation ist es, eine systemorientierte Analyse und Optimierung der Effizienz eines modernen Antriebssystems durchzuführen. Der ganzheitliche Ansatz berücksichtigt sämtliche Teilsysteme des Antriebssystems. Dazu gehören das EMV Eingangsfilter, der leistungselektronische Konverter und die Lastmaschine. Auch die gegenseitigen Zusammenhänge und die Einflüsse von modernen Regelkonzepten werden berücksichtigt. Konsequenterweise müssen Verlustmodelle von allen Teilsystem gefunden und miteinander verbunden werden, um die Wechselwirkungen korrekt abzubilden.

Modernste Konverterstrukturen werden kaum in Niederspannungsanwendungen eingesetzt. Dazu gehören etwa der 3-Punkt NPC Wechselrichter oder der 3-Punkt T-Typ Wechselrichter, welche eine hervorragende Energieeffizienz aufweisen. Zusätzlich haben diese modernen

Konverter einen positiven Einfluss auf die umgebenden Teilsysteme, da sie durch die verbesserte Spannungsform geringere Oberschwingungsverluste in der Lastmaschine und in Bauteilen des EMV Filters verursachen. Eine detaillierte Analyse zeigt auf, dass diese modernen Konverterstrukturen trotz höherer Anschaffungskosten den Bau eines modernen Antriebssystems ermöglichen, welches die Standardlösung im industriellen Umfeld bezüglich der Energieeffizienz, der notwendigen Halbleiterfläche und des Aufwands bei der Filterung übertrifft und verbessert. Dabei werden auch die Komplexität und der Implementierungsaufwand berÃ¼cksichtigt.

Werden moderne Regelverfahren eingesetzt, kann die Energieeffizienz des Antriebssystems weiter erhöht werden. Ein effizienzoptimales Regelverfahren kann die Verluste der häufig eingesetzten Asynchronmaschine bei niedrigem Lastmoment vermindern. Dazu wird der Rotorfluss der Maschine abgesenkt, was gleichzeitig die Eisenverluste und die ohmschen Verluste durch den Magnetisierungsstrom reduziert. Da sich dabei auch der Arbeitspunkt des Konverters verändert, hat die effizienzoptimale Maschinenregelung auch einen Einfluss auf die Konvertereffizienz. Auf ähnliche Weise kann der Einsatz von aktiven Dämpfungsmethoden zusätzliche physikalische Dämpfungszweige im EMV Filter überflüssig machen und so Kosten, Verluste und Bauvolumen des Filters reduzieren. Da aktive Dämpfungsmethoden das Verhalten des Konverters erheblich beeinflussen, muss die Stabilität des 3-phasigen Systems sorgfältig untersucht werden, wozu Verfahren aus der MIMO-Systemtheorie verwendet werden.

Schlussendlich wird ein modernisiertes, hocheffizientes Antriebssystem für Niederspannungsanwendungen vorgeschlagen, welches auf dem 3-Punkt T-Typ Wechselrichter beruht und moderne Regelmethoden zur Reduktion des Energieverbrauchs des Gesamtsystems einsetzt.

Notation

φ_1	Voltage to current displacement angle
φ_v	Angle of voltage space vector
ϕ	Flux
δ	Skin-depth
$\underline{\sigma}$	Minimum singular value
$\overline{\sigma}$	Maximum singular value
ω_0	Resonance angular frequency
$\omega_\mathrm{b,i}$	Current control bandwidth
$\omega_\mathrm{b,u}$	Voltage control bandwidth
ω_e	Synchronous electrical angular frequency
ω_K	Angular frequency of arbitrary reference frame
ω_m	Measurement angular frequency
ω_R	Mechanical rotor angular frequency
ω_sl	Angular slip frequency
ϵ_e	Electrical angle
ϵ_R	Rotor angle
Ψ_m	Mutual flux linkage
Ψ_r	Rotor flux linkage
$\Psi_\mathrm{r,n}$	Rated rotor flux linkage
$\Psi_\mathrm{r,opt}$	Optimal rotor flux linkage
$\Psi_\mathrm{r,opt,g}$	Global optimal rotor flux linkage
η	Efficiency
η_fric	Mechanical efficiency
η_i	Efficiency of the inverter stage
η_Lb	Efficiency of the boost inductors
$\eta_\mathrm{m,el}$	Efficiency of the machine (excluding friction)
η_r	Efficiency of the rectifier stage

η_{total}	Total system efficiency
$\eta_{\text{total,el}}$	Total system efficiency (excluding friction)
ρ	Power density
A	Chip area
B	Flux density
C	Capacitance
C_{d}	Damping capacitance
C_{dc}	DC-link capacitance
C_{f}	Filter capacitance
C_{sim}	Simulated virtual capacitance
d	Relative duty-cycle
E	Energy
f_0	Resonance frequency
f_{e}	Synchronous electrical frequency
f_{h}	Harmonic frequency
$f_{\text{h,s}}$	Harmonic stator frequency
$f_{\text{h,r}}$	Harmonic el. rotor frequency (harmonic slip frequency)
f_{R}	Mechanical rotor frequency
f_{sl}	Slip frequency
f_{sw}	Switching frequency
G	Transfer function
G_{t}	Approximate transfer function of the time delay
I	Current
$\hat{I}$	Current amplitude or peak value
I_1	Converter output current
I_{c}	Current of the eq. core loss resistance
I_{h}	Harmonic current
I_{inj}	Injected current
I_{m}	Current of the mutual inductance
I_{out}	Output current of a bridge-leg
I_{r}	Rotor current
I_{s}	Stator current
L	Inductance
L_{b}	Boost inductance
L_{f}	Filter inductance
L_{g}	Grid inductance
L_{m}	Mutual inductance
$L_{\sigma\text{s}}$	Stator stray inductance
$L_{\sigma\text{s}}$	Rotor stray inductance

L_σ	Total stray inductance
m	Modulation index
p	Pole-pair number
P_{cond}	Conduction losses
P_{eddy}	Eddy-current iron losses
P_{fric}	Friction and windage losses
P_{h}	Harmonic losses
$P_{\mathrm{h,i}}$	Harmonic iron losses
$P_{\mathrm{h,m}}$	Total harmonic losses of the machine
$P_{\mathrm{h,o}}$	Harmonic ohmic losses
P_{hys}	Hysteresis iron losses
P_{i}	Iron losses
$P_{\mathrm{i,r}}$	Iron losses of the rotor core
$P_{\mathrm{i,s}}$	Iron losses of the stator core
$P_{\mathrm{in,Lb}}$	Input power before the boost inductors
$P_{\mathrm{loss,i}}$	Total losses of the inverter stage
$P_{\mathrm{loss,Lb}}$	Total losses of the boost inductors
$P_{\mathrm{loss,m}}$	Total fundamental losses of the machine
$P_{\mathrm{loss,r}}$	Total losses of the rectifier stage
P_{o}	Ohmic losses
$P_{\mathrm{o,r}}$	Ohmic losses of the rotor windings
$P_{\mathrm{o,s}}$	Ohmic losses of the stator windings
$P_{\mathrm{out,i}}$	Output power of the inverter stage
$P_{\mathrm{out,Lb}}$	Output power after the boost inductors (input power of the rectifier stage)
$P_{\mathrm{out,m}}$	El. output power of the machine
$P_{\mathrm{out,mech}}$	Mech. output power of the machine (shaft power)
$P_{\mathrm{out,r}}$	Output power of the rectifier stage
P_{stray}	Stray-load losses
P_{sw}	Switching losses
R_{c}	Equivalent core loss resistance
R_{cs}	Case-to-sink thermal resistance
R_{d}	Damping resistance
R_{g}	Grid resistance
R_{i}	Transfer function of the current controller
R_{jc}	Junction-to-case thermal resistance
R_{js}	Junction-to-sink thermal resistance
R_{r}	Rotor resistance
R_{s}	Stator resistance

R_{sa}	Sink-to-ambient thermal resistance
R_{sim}	Simulated virtual resistance
R_{th}	Thermal resistance
R_{u}	Transfer function of the voltage controller
s	Laplace operator
sl	Relative slip
sl_{h}	Harmonic slip
t	Time
T_{amb}	Ambient temperature
T_{c}	Case temperature
T_{e}	Electrical torque
T_{fric}	Torque due to friction and windage
T_{j}	Junction temperature
T_{sink}	Temperature of the heat sink
T_{sw}	Switching period
T_{t}	Time delay (dead-time)
V	Volume
$\hat{V}$	Voltage amplitude or peak value
V_1	Converter output voltage
$V_{(1)}$	Fundamental component of the voltage
V_{b}	Bus voltage
V_{c}	Commutation voltage
V_{dc}	DC-link voltage
V_{g}	Grid voltage
V_{h}	Harmonic voltage
V_{ll}	Line-to-line voltage
V_{m}	Air-gap voltage (voltage across the mutual inductance)
V_{rms}	RMS voltage
ΔV_{rms}	RMS value of the ripple voltage
V_{s}	Stator voltage
V_{u}	Modulated rectifier voltage
Y	Admittance matrix
$\mathrm{Y}_{\mathrm{sim}}$	Simulated virtual admittance matrix
Z	Impedance matrix
Z_{g}	Grid impedance
Z_{in}	Input impedance
Z_{out}	Output impedance

Contents

Chapter 1

Introduction

Wasting electrical energy leads to an accelerated decline of fossil and non-regenerative energy reserves (such as oil, gas, and raw material for nuclear power plants). Obviously, this behavior should be avoided, assuming that regenerative energy sources will not be able to replace the complete energy demand in near future. Although most people would agree with this fundamental statement, there are further, more practical and economical reasons why energy should not be wasted.

It is assumed that the price of electrical energy will rise in the future for different reasons [1]. Producing electrical energy from conventional fossil sources, such as oil, gas, and coal becomes more expensive as the price of the raw materials is rising. Sophisticated and more expensive extraction methods are necessary as the easily accessible sources are declining. Additionally, international speculations on raw materials and political crises in the near east regularly drive up the price of oil, gas and coal. The extraction of coal is often connected with big impacts on the landscape and ecological problems. Due to the high amount of carbohydrate exhausts, new methods to filter the exhausts and pump back the carbohydrates into the ground are discussed. These methods could further rise the price of electrical energy.

Another reason for increasing prices are subsidiaries of renewable energy sources. E.g. in Germany, private customers have to finance the early integration of renewable energy with the bill for electrical energy [2]. Initially, photovoltaic installations have risen the price for private customers of electrical energy due to the guaranteed compensation for electricity fed into the grid. Industrial customers are often exempt from

this cross-financing approach and profit from low energy prices. Here, the impact of renewable energy can also lead to lower prices during sunny days for big industrial customers that can buy electrical energy closer to the actual market value [2]. It can be concluded that the price for electrical energy is not completely determined by the market but it is also affected by political decisions and subsidiaries.

The alternative of nuclear power is controversially discussed in different countries. Some countries (e.g. France and the U.S.) rely on the nuclear power as a source of cheap electrical energy. Others have decided (e.g. Germany and Switzerland) to turn-off the nuclear power plants within the next decades. This decision is based on the problems with the nuclear waste and the nuclear accident in Fukushima, Japan, a country that is technologically highly developed. Therefore, cheap electrical energy from nuclear power plants is not a reliable alternative and depends mostly on political decisions.

Concluding, the costs of electrical energy are the most important driver towards more efficient technologies. Wasting electrical energy is not economically lucrative. Even if the price of electrical energy would be zero, efficiency would still matter as wasted energy could be used to produce valuable goods. The higher the costs of energy are, the more important the running costs are compared to the initial purchase costs of a device. This leads to a reconsideration of the purchase costs as it may be economically lucrative to initially pay more for the device but save money during the operation of the device.

In the countries that decided to turn-off all nuclear power plants, besides installing and integrating more renewable energy sources, the energy efficiency was identified to be the most important enabling factor to bridge the possible energy gap [3]. Increasing the energy efficiency using the technologies available today in all fields, especially in heating, cooling, and thermal isolation of buildings is very important and is a key element of the future energy strategy. If the transition from fossil fuel based energy generation to renewable energy generation should be successful, efficient devices are of utmost importance.

In general, energy efficiency is a key technology factor, pushed by political decisions and scarcity of resources. In order to increase the energy efficiency, the consumers operating at low efficiency have to be identified and the losses have to be reduced, which is a major task of industrial and academic research [4, 5].

Variable speed drive (VSD) systems are the most important con-

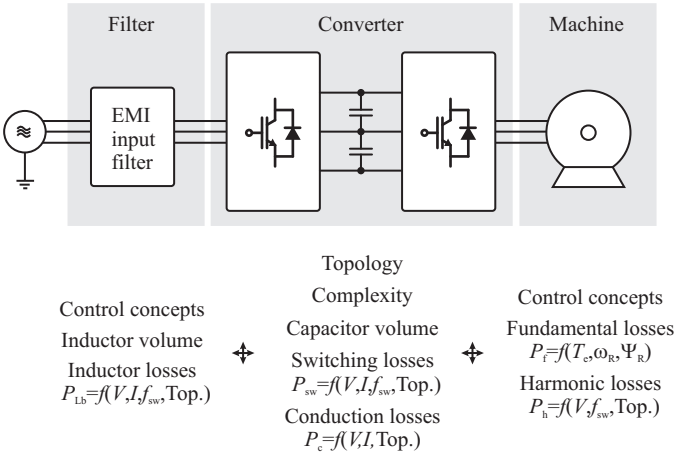

Figure 1.1: Variable speed drive system with its subsystems. Various interactions between the converter topology, the losses of the subsystems, the volume of the involved components and the applied control concepts can be identified.

sumers of electrical energy in the industry. In western countries, they consume up to 60% of the total electric energy [5]. They can be found in many different applications, such as ventilation, air-conditioning, drilling, mills, air compression, and many more. Another field is traction applications, such as in trains and electrical vehicles. Most of these VSD systems are actually supplied from the low-voltage grid and process a modest amount of power (up to 100 kW), but the total number of installed drive systems and the total processed energy is huge. Therefore, the potential benefit of improving the energy efficiency of these systems is clear.

Such a VSD system consists of several subsystems or parts, illustrated in Fig. 1.1. Starting from the load, there is the mechanical task that has to be performed and the processes that have to be controlled. As an electromechanical actuator, an electrical machine is used, such as an induction machine or a permanent magnet synchronous machine. It transforms the electric power directly into mechanical power and has a rather high nominal efficiency (85% - 95%) compared to combustion engines. The electrical machine is supplied by a modern power electronic inverter that is able to adjust the amplitude and the frequency

of the stator voltage. Usually, the inverter itself is supplied from an energy storage element, such as a dc-link capacitor or a dc-link inductor. This energy storage element is necessary for backup power during short voltage outages of the grid and allows to dynamically accelerate and decelerate heavy loads. Following, the grid voltage is rectified, using again a power electronic subsystem such as an active rectifier or a simple diode rectifier. The active rectifier allows to build up a bidirectional system that is able to feed energy back into the grid. This is advantageous if heavy loads are decelerated and allows to restore the mechanical energy in rotating or moving masses that would have to be wasted otherwise. Finally, in between the rectifier stage and the supply grid, a filtering structure has to be placed that smoothens the currents in order to comply with conducted EMI regulatory standards. It has to filter voltage harmonics that could disturb other sensitive electrical equipment connected to the grid.

Concerning the energy efficiency of this system, all subsystems have more or less losses that could be omitted to a certain extent. The mechanical process clearly has the biggest potential for efficiency improvement of all subsystems. It was recognized decades ago that replacing simple mechanical gearboxes and valves with a speed controlled drive system can improve the total efficiency considerably, especially in part load situations [5]. It can be compared to electrical systems where a simple series resistor used to reduce the output power delivered to the load is replaced with a modern switched-mode dc-dc converter.

The electrical motor itself is the second subsystem that exhibits high losses. The induction machine is the machine that is used most often in industry because it is cheap and robust. Traditionally, it was directly connected to the grid as a fixed frequency drive system as it has self-starting capability and good damping characteristics. It can be equipped with an inverter system to obtain variability of speed. The induction machine has ohmic losses in the windings and in the rotor cage, and also additional iron losses in the iron core. The efficiency of the induction machine can be improved with several design changes. Reducing the iron core lamination thickness could reduce the core losses, using copper instead of aluminum could reduce the rotor cage losses. Also better bearings and an improved cooling system could reduce the losses further, but most of these design changes are to expensive and are not implemented in low-cost induction machines. A permanent magnet synchronous machine is more efficient and could replace the induction

machine, but also this solution is more expensive due to the costly permanent magnets.

Furthermore, induction machines have a low efficiency during part load operation as some of the loss components such as the iron losses and the ohmic losses due to the magnetization current are independent of the load. Energy saving control algorithms are available that can reduce these loss components during part load operation and increase the efficiency.

The power electronic converter, consisting of the rectifier stage and the inverter stage is usually very efficient (a total converter efficiency of 94% - 97% is commonly reached), but still, the losses are not negligible. A costly cooling system with a heatsink and fans, or even a water cooling solution with water circulation and a heat exchanger are necessary to limit the junction temperatures of the semiconductors. If the maximum junction temperature of these devices is exceeded (for silicon based devices up to 175 °C), thermal failure may occur. The converter losses are composed of semiconductor conduction losses and switching losses, being dependent on the switching frequency of the devices, the switch technology and the converter topology. Apart from these loss components, the power electronic converter induces additional losses in the electrical machine as it produces a switched output voltage waveform with increased harmonic content. This leads to additional heating and reduced lifetime of the machine.

Finally, losses occur in the EMI filtering components, such as inductors and damping resistors. These losses lead to increased temperatures of the components and are a limiting factor for minimizing volume and weight of these components.

1.1 Contributions of this thesis

The efficiency of VSD systems has been the subject of industrial and academic research over the last decades [4, 6–11]. The various subsystems have mostly been analyzed and optimized independently. A holistic, system oriented analysis and efficiency optimization of the complete VSD system, considering new converter topologies and their impact on the surrounding subsystems, considering extended control methods such as energy saving controllers and active damping concepts, and considering the optimization potential of the complete system has not been performed yet.

In this thesis, a comprehensive system oriented efficiency optimization of low-voltage VSD systems, consisting of an EMI input filter, a bidirectional active rectifier stage, an inverter stage and an induction machine, is performed. The advantages of multi-level converter topologies for low-voltage VSD applications, their positive impact on the surrounding subsystems and their cost effective implementation are analyzed in detail. Multi-level topologies are known from medium voltage applications but are also a very interesting choice for low-voltage applications. The optimization potential concerning the necessary semiconductor chip area of the converter, the implementation effort, the passive filtering components, the converter losses, and the harmonic and fundamental losses of the machine is highlighted and compared to the standard industry VSD system used today, that is built with a simple 2-level voltage source converter. The implementation effort of energy saving controllers including automatic parameter detection routines, the possible machine efficiency gain and the impact on the converter losses is analyzed. Special attention is paid to the various interactions of the subsystems such as changed operating points that lead to changing fundamental and harmonic losses in the other subsystems. The possibility of using active damping algorithms to remove passive damping branches is investigated, with a special focus on stability issues of three-phase power electronic systems.

As a result, a modern, highly-efficient, and still cost competitive VSD system is proposed, based on the 3-level T-type converter topology and incorporating a loss-optimal machine control scheme. The complete system is optimized concerning fundamental and harmonic losses. A fair comparison of the T-type converter VSD system with the standard 2-level converter and with an alternative implementation using a 3-level neutral point clamped converter is given.

The main contributions of this thesis are

- Comparison and assessment of several converter topologies concerning their suitability as converters for low-voltage VSD systems. Among others, the 2-level converter, the 3-level neutral point clamped converter, the 3-level T-type converter, the 3-level coupled inductor converter, and the 3-level flying capacitor converter are considered.

- Analysis and modelling of the loss components of the 3-level T-type converter topology for low-voltage applications that combines dif-

ferent switch technologies.

- Investigation of the semiconductor chip area required for realizing the 2-level voltage source converter, the 3-level T-type converter and the 3-level neutral point clamped (NPC) converter.

- Investigation of energy saving machine control algorithms including the automatic detection of the necessary machine parameters. A sensitivity analysis of the parameter identification accuracy on the performance of the energy saving controller is given. The impact of the energy saving controller on the converter efficiency is analyzed.

- Implementation of a parameter identification method that is able to automatically detect the equivalent core loss resistance of the induction machine model from a no-load deceleration test.

- Experimental verification and comparison of models describing the harmonic losses in induction machines due to the PWM voltage waveform of 2-level and 3-level converters.

- Interlinking of the loss models of the converter, the machine, and the passive filter elements. Optimization of the VSD system efficiency.

- Investigation of active damping methods based on virtual impedances including the stability analysis of three-phase power electronic converters. Implementation and experimental verification of the resonance frequency shifting method.

1.2 Organization of this thesis

This thesis is organized following the order of the subsystems of the complete VSD system depicted in Fig. 1.1. Starting from the subsystem with the lowest efficiency, the induction machine, continuing with the power electronic converter and ending at the grid interface including the EMI filter, the models of the subsystems are developed first independent of each other and finally interlinked for a detailed system analysis. Instead of giving a literature review in the introduction of this thesis, the important literature of each topic is covered at the beginning

of each chapter. This improves the readability as three different topics are considered.

In **Chapter 2**, the loss components of the induction machine, a central part of all VSD systems, are investigated. First, the fundamental machine losses and their dependency on the rotor flux linkage are reconsidered. The impact of energy saving controllers, that reduce the rotor flux linkage during low torque operation in order to increase the part load efficiency of the machine, is investigated. Different implementations of these energy saving controllers, such as search controllers or model based controllers are briefly compared. As the model based approach relies on the knowledge of several induction machine parameters, the sensitivity of the reachable efficiency on the parameter detection accuracy is calculated.

In addition to the usual induction machine parameters also necessary for field oriented control algorithms, such as the mutual inductance, and the stator and the rotor resistance, the equivalent core loss resistance has to be detected. A simple detection method based on a deceleration test is presented.

A further important topic are the harmonic machine losses due to the PWM voltage waveform generated by the power electronic converter. The theoretical background is reconsidered and different models describing the harmonic losses are compared. The dependency on the stator voltage amplitude is modeled with an approximation valid for high converter switching frequencies and confirmed with measurements on a standard induction machine. The difference between the harmonic losses with a 2-level voltage waveform and a 3-level voltage waveform is evaluated.

In **Chapter 3**, several converter topologies are compared and evaluated for their application in low-voltage VSD systems. Three converter topologies are chosen for a deeper comparison, namely the 2-level converter (2LC), the 3-level neutral point clamped converter (3LNPC^2), and the 3-level T-type converter (3LT^{2}C). These three topologies are considered also in the system optimization presented in Chapter 5. Additionally, the 3-level flying capacitor converter, the 3-level active neutral point clamped converter, the 3-level coupled inductor converter, matrix converters, and multi-level converters are briefly evaluated. The implementation effort concerning hardware and software is compared. Switching and conduction losses of the three topologies are calculated with a general space vector modulation based loss calculation algo-

rithm. The loss distribution characteristics among the semiconductor devices and the thermal loading in the different operating points are discussed. As an extension, the required semiconductor chip area of the three topologies is calculated and compared.

The efficiency of the three topologies depending on the operating point and the switching frequency is calculated and compared. Especially the loss components of the 3-level T-type converter, that combines semiconductors with different blocking voltages, are carefully evaluated and experimentally verified. The preferred application areas of the three topologies are identified and their weaknesses and strengths are compared. As 3-level converters operate from a split dc-link, the balancing of the dc-link voltages is discussed in combination with loss-optimal discontinuous modulation schemes.

In **Chapter 4**, a simplified loss comparison of the EMI input filter components is given. The necessary boost inductance, its volume and losses are compared for the three different topologies.

As a second topic, the implementation of active damping algorithms is considered. Usually, passive damping branches are used to damp resonance peaks of the EMI input filter in order to guarantee stability. These passive damping branches can be replaced with a virtual damping impedance simulated by the converter. Related active damping methods are analyzed, such as virtual resistor damping or the resonance frequency shifting method. Volume and losses of the EMI filter can be reduced with the active damping methods as no passive damping branch is needed any more.

In order to compare the damping performance of these methods, the stability of the active rectifier system is analyzed with methods used in the MIMO system theory. A stability theory based on the comparison of impedance matrices in the synchronous reference frame is applied. The small-signal input admittance matrix of the active rectifier is derived analytically and verified with experimental measurements using a measurement system for impedance matrices in the synchronous reference frame. The measurement system is based on a resistive chopper circuit for line-to-line current injection and it allows the measurement of the small-signal impedance matrix components during operation of the power electronic converter.

In **Chapter 5**, the loss models derived in the previous chapters are interlinked and the efficiency of the complete VSD system is calculated, again for the three different converter topologies. The optimal switching

frequencies of the inverter stage and the rectifier stage that lead to minimal total switching frequency dependant losses in the complete system are derived. The impact of the energy saving machine control algorithm on the total system efficiency is analyzed, considering also the impact on the inverter stage. The achievable system efficiency with the energy saving machine controller is compared to a numerically found global system efficiency optimum.

Finally, a highly efficient VSD system based on the 3-level T-type converter is proposed. The achievable system efficiency and the implementation effort are compared against a conventional 2-level converter based VSD system.

In **Chapter 6**, two hardware prototypes are presented. A 99% efficient 10 kW 3-level T-type inverter and a 10 kW 3-level NPC back-to-back converter have been built to verify the basic operation principles, the implementation effort and the loss models.

Concluding, in **Chapter 7**, the results of this thesis are summarized and an outlook on future work is given.

1.3 Publications

The results of this thesis have partly been published in the publications listed below.

1. M. Schweizer and J.W. Kolar. Design and implementation of a highly efficient 3-level T-type converter for low-voltage applications. IEEE Transactions on Power Electronics, vol. 28, no. 2, pages 899-907, Feb. 2013.

2. M. Schweizer, T. Friedli, and J.W. Kolar. Comparison and implementation of a 3-level NPC voltage link back-to-back converter with SiC and Si diodes. In Proc. of the 25th Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), pages 1527-1533, Feb. 2010.

3. M. Schweizer and J.W. Kolar. High efficiency drive system with 3-level T-type inverter. In Proc. of the 14th European Conf. on Power Electronics and Applications (EPE), pages 1-10, Aug. 2011.

4. M. Schweizer, I. Lizama, T. Friedli, and J.W. Kolar. Comparison of the chip area usage of 2-level and 3-level voltage source

converter topologies. In Proc. of the 36th Annual Conf. of the IEEE Industrial Electronics Society (IECON), pages 391-396, Nov. 2010.

5. M. Schweizer and J.W. Kolar. Shifting input filter resonances - An intelligent converter behavior for maintaining system stability. In Proc. of the International Power Electronics Conference (IPEC), pages 906-913, June 2010.

6. T. Soeiro, M. Schweizer, J. Linner, P. Ranstad, and J.W. Kolar. Comparison of 2- and 3-level active filters with enhanced bridge-leg loss distribution. In Proc. of the 8th IEEE International Energy Conversion Conf. and Exposition (ICPE ECCE), pages 1835-1842, June 2011.

7. J. Mühlethaler, M. Schweizer, R. Blattmann, J.W. Kolar, and A. Ecklebe. Optimal design of LCL harmonic filters for three-phase PFC rectifiers. In Proc. of the 37th Annual Conf. of the IEEE Industrial Electronics Society (IECON), pages 1503-1510, Nov. 2011.

8. J. Biela, M. Schweizer, S. Waffler, and J.W. Kolar. SiC versus Si - Evaluation of potentials for performance improvement of inverter and DC-DC converter systems by SiC power semiconductors. IEEE Transactions on Industrial Electronics, vol. 58, pages 2872-2882, July 2011.

9. A. Stupar, T. Friedli, J. Miniböck, M. Schweizer, and J.W. Kolar. Towards a 99% efficient three-phase buck-type PFC rectifier for 400V DC distribution systems. In Proc. of the 26th Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), pages 505-512, March 2011.

10. P. Cortes, D.O. Boillat, T. Friedli, M. Schweizer, J.W. Kolar, J. Rodriguez, and W. Hribernik. Comparative evaluation of control schemes for a high bandwidth three-phase AC source. In Proc. of the 7th International Power Electronics and Motion Control Conf. (IPEMC), vol. 1, pages 321-329, June 2012.

Chapter 2

Machine Interface

An optimized variable speed drive (VSD) system should be highly efficient and the easiest way to increase the system efficiency is to improve the subsystem with the highest losses. As the induction machine has clearly the highest losses, its efficiency should be increased first. Mechanical adaptations and optimization of the machine design are beyond the scope of this thesis. Therefore, only machine loss mechanisms which are influenced by the converter topology, the modulation strategy and the machine control are considered in this chapter.

Electrical machines have inherently a rather good efficiency compared to combustion engines, especially in the nominal operating point. If the induction machine is only partly loaded and the output power decreases, the efficiency drops considerably. This effect can be explained easily with the existence of loss components which are independent of the load, such as iron core losses and the ohmic losses related to the magnetizing current. An interesting method to overcome this drawback is to implement intelligent control algorithms, so called energy saving controllers. These controllers change the machine flux level depending on the operating point in order to decrease the machine losses during low torque operation. Their impact is mainly limited to the loss components related to the fundamental frequency of voltages, currents and fields. As such energy saving algorithms rely on a detailed model of the induction machine, several specific parameters of the machine have to be known or should ideally be detected directly by the converter itself. The derivation and implementation of such energy saving controllers including the detection of the necessary parameters are addressed in

Section 2.1.

A second category of losses in electrical machines occurs due to the pulsed stator voltages generated by modern power electronic PWM inverters. Harmonic currents and harmonic fields induce additional losses in the machine which are dependent on the converter topology, the modulation strategy and the switching frequency. Considering the total system efficiency optimization, the harmonic machine losses are an important factor as the order of magnitude of these losses is in the same range as the converter losses for low voltage applications. The theoretical background and the impacts of the converter, the modulation method and the operating point on the harmonic machine losses are considered in Section 2.2.

2.1 Optimization of fundamental machine losses

2.1.1 Literature review

The losses of electrical machines have been a central topic since the early days of their invention. The description and the calculation of the basic loss components of induction machines, especially for machine design purposes is summarized in many books and publications [12–15]. Machine losses are traditionally split into stator and rotor ohmic losses, iron losses due to the mutual flux, stray-load losses due to leakage fluxes, and mechanical losses due to friction and windage. The stray-load losses can further be separated into zig-zag losses, motor-end losses, skewing losses, and additional losses [15].

Optimization of the part load efficiency by means of active voltage and frequency control became possible with the success of power electronic converters. The part-load efficiency optimization was first analyzed in 1971 by Tsivitse et al. [16]. It was found that the standard control method for variable speed drives generates unnecessarily high losses during part-load operation. Induction machines are traditionally controlled with a constant V/f-ratio, leading to rated flux operation. The stator voltage is increased proportionally with the speed of the machine. If the load torque changes, the slip changes passively until a new steady-state is reached.

For low torque operation, keeping the rated flux operation is not required and not optimal concerning the machine losses. It is possible

to reduce the iron losses and the ohmic losses caused by the magnetizing current by reducing the stator voltage and the associated flux level during low torque operation. This is the basic principle of all energy saving controllers.

Tsivitse theoretically derived the optimal stator flux for maximum efficiency considering ohmic, iron, and stray-load loss components. With this optimal flux, an optimal slip speed can be derived which is constant for a linear machine. The slip speed can be regulated to be constant by adjusting the stator voltage amplitude, which is the operation principle of many energy saving controllers. As the optimal slip speed is constant, the input impedance of the machine appears to be constant and therefore the power factor and the efficiency is independent of the applied torque.

The topic found new interest in the beginning 80s. Nola presented a simple energy saving controller for single-phase and three-phase induction machines [17]. It is based on the principle of keeping the power factor of the machine constant. When the induction machine is only partly loaded, the voltage to current phase displacement angle increases from $\varphi_1 \approx 30°$ to $\varphi_1 \approx 80°$. If this angle is controlled to be a constant value near $\varphi_1 \approx 30°$ by adjusting the stator voltage, the efficiency of the machine can be kept high over the full torque range. The controller was implemented for a fixed frequency drive system with thyristors (TRIACs) in series to the mains. By adjusting the firing angle, the displacement angle can be influenced directly, although indirectly also the fundamental stator voltage is changed and implicitly the constant slip principle is applied. An improved version of the Nola controller using an autotransformer to have more voltage levels and therefore less harmonic losses was presented in [18].

The Nola controller was originally proposed for fixed frequency drives with a thyristor based soft starting circuit in series to the mains. Soon, the concept was criticized because the energy savings are small if the machine is not very often operated with partial load [19]. Due to the losses in the thyristors, the system efficiency at rated load decreases compared to direct mains connection of the machine. Depending on the load profile, there could be even more energy wasted with the Nola controller than without.

This argument is only valid for fixed frequency drives as a power electronic inverter is needed anyway for a variable frequency drive. Consequently, the concept of energy saving controllers gained more and more

importance with the spread of variable frequency drives and a variety of concepts and implementation options have been suggested. An extensive survey on the proposed concepts is given in [20].

The operating point of an induction machine, defined by output torque and rotor speed, can be achieved with several settings of stator voltage and stator frequency. If the stator frequency is changed, the stator voltage has to be adapted in order to keep the operating point. The slip speed and the various flux levels are directly related to the stator frequency and stator voltage. There is a degree of freedom in achieving the requested operating point which can be exploited to maximize the machine efficiency. Any of the variables: slip, stator frequency, stator voltage, stator-, rotor-, or mutual flux can be used for loss minimization. Only one of these variables can be changed freely, the remaining quantities are dependent and rely on the operating point. A detailed mathematical analysis is presented in Section 2.1.3.

Initially, the solutions for maximum efficiency operation were expressed with the optimal slip or the optimal stator voltage. This simplified the implementation on simple variable voltage and frequency inverters such as six-step inverters. The equation of the optimal slip for maximum efficiency depends on many specific machine parameters such as the equivalent core loss resistance, stator and rotor resistance, as well as magnetizing and leakage inductance. Therefore, also simplified expressions and control methods have been proposed, such as the slip for maximum torque per ampere or constant rated slip operation [6, 21, 22]. The performance was compared to the true optimal solutions. Both simplifications lead to suboptimal solutions, the reachable efficiency is below the theoretical maximum because the iron losses are neglected. This leads to a flux reference which is to high. For high speed and low torque operation, the deviation from the efficiency maximum is typically in the range of 1-3%.

The influence of saturation on the location of the loss minimum was analyzed in [21, 23, 24]. Whereas the optimal slip frequency is constant for a linear machine (assuming a fixed rotor speed), it is not any more if saturation is considered. The optimal slip including saturation can be found with numerical methods. Fortunately, the efficiency maximum is very flat and small deviations of the slip value from the optimum have only a little impact on the achievable efficiency (a sensitivity analysis is given in Section 2.1.3). Therefore, neglecting saturation gives still good results near the true maximum efficiency point.

The field oriented description of the induction machine and its associated field oriented control concepts (cf. [13]) gained importance with the improved calculation power of microprocessors. The findings for efficiency optimal control of induction machines were transformed to the field oriented concept [24–26]. As already mentioned, instead of controlling the slip also the flux (either stator-, mutual- or rotor-flux) can be controlled directly with the appropriate control scheme in order to minimize the induction motor losses in any operating point. Basically, for a linear machine, the mutual flux of the machine has to be reduced for low torque operation and can be increased above rated flux for high torque operation in order to reach the efficiency maximum. If saturation is considered, increasing the mutual flux above the rated value is suboptimal as the increased currents limit the reachable efficiency.

Further publications mainly dealt with the practical implementation of energy saving controllers. Besides the classical slip controllers, the approaches can be divided into two groups, namely search controllers and model-based controllers [6, 23], both having their strengths and weaknesses.

The search controller periodically perturbs a certain variable, such as the stator voltage, the stator frequency, or the flux and measures the corresponding change of the machine's input power [25, 27–30]. If the input power reduces, the control variable is changed in the same direction again in the next step, if it increases, the control variable is changed in the opposite direction. The input power slowly converges to its minimum and the maximum efficiency is found.

Search controllers have several advantages over model-based concepts. They can be implemented without the knowledge of any machine parameters, which are not easy to determine. Additionally, they can be implemented on simple scalar as well as on field-oriented controlled drives. A further positive aspect is the possibility to include the converter into the online efficiency optimization by measuring the power on the dc-link side or at the mains side in front of the rectifier circuit.

The main drawbacks of search controllers are the slow convergence and continuous oscillations around the optimal efficiency point because of the flat dependency of the input power on the flux level. Therefore, several workarounds have been proposed during the last decades. Kioskeridis [30] proposed to minimize the stator current instead of the input power because the stator current is more sensitive to flux changes. The search controller shows less oscillations around the optimal point,

but, as has been mentioned, minimum stator current is only a sub-optimal solution that does not yield maximum efficiency. Therefore, further improvements were suggested, all trying to decrease the convergence time and reduce oscillations around the minimum loss point. Basically, the search step size at the beginning of the optimization is large and is reduced when the minimum loss point is approached using advanced control strategies such as fuzzy-logic, neural-networks, or gradient-search [31–34]. A survey on different search algorithms is given in [35].

The model-based controllers constitute the second group. In contrast to the search controller, a model-based controller directly calculates the optimal reference value of the controlled variable such as the slip or the rotor flux. The optimal reference is calculated with the machine parameters and the measured or estimated machine working point. Therefore, sufficient computation power, an accurate loss model and the knowledge of the machine parameters are preconditions for a successful implementation. The machine parameters can be determined with standardized no-load and blocked-rotor tests (cf. [12]). Alternatively, in an intelligent drive system, the converter could determine these parameters online or during a commissioning run with appropriate algorithms. The advantages of a model-based controller are the fast convergence and the absence of oscillations around the efficiency maximum.

Basically, the early slip-frequency and power factor controllers already belong to the model-based controllers. There, the optimal slip frequency or power factor reference for a specific machine was calculated offline and implemented with analog electronics or with simple digital regulators. If the slip frequency is held constant, the rotor speed is regulated with an outer control loop that adapts the stator voltage. For variable speed drives, also lookup tables were used to set the optimal slip speed as in [36,37]. Alternatively, the speed can be controlled over the stator frequency and the stator voltage is set to be optimal according to a loss model as in [7]. The control performance of these simple scalar drives was not comparable to modern field-oriented controlled drives.

Direct implementations of model-based concepts for field-oriented drives were shown in [26,38–43]. It was shown that the loss components, including iron losses, can be assigned either to the field-producing stator current component I_{sd} or to the torque producing stator current

component I_{sq}. The total losses are minimal if the loss components assigned to I_{sd} are equal to the loss components assigned to I_{sq} as both depend on the squared current component. This principle was applied in [44] where an additional PI controller was used to equal the losses related to the two current components in order to achieve minimum losses. For minimum losses, the ratio between I_{sd} and I_{sq} is constant at a fixed rotor speed. This condition is equivalent to the condition for minimum losses in a dc-machine, where the ratio between armature and field current is constant for a given speed [23]. Equations for the optimal current components depending on the operating point and the machine parameters were derived. In a field oriented drive, these two components are usually directly controlled and the optimal current components can be used as references. If the two current components are set to be equal ($I_{sd} = I_{sq}$) the already mentioned suboptimal, iron loss neglecting maximum torque per ampere strategy is obtained.

Finally, direct equations for the optimal rotor flux linkage depending on the machine parameters and the operating point were derived in [42, 43] and implemented on a field oriented drive. The model based approach was also applied in [26] and [40] for a variable speed drive with direct torque control. There, the optimal stator flux linkage was calculated from the machine parameters and the operating point and directly used as a reference for the hysteresis stator flux controller.

Vukosavic et al. combined the search controller and the model based approach in [45]. There, the parameters of a generic loss model are updated online with measurements of the drive input power and using a sophisticated identification method. Therefore, the impacts of temperature changes on the loss-model parameters are correctly estimated. The loss-optimal flux is calculated with the generic loss model and a very fast convergence could be achieved without knowledge of the machine parameters. Basically, the positive aspects of the loss-model controller, such as fast convergence time and no oscillations are combined with the positive aspects of the search controller, such as independence of a knowledge of machine parameters.

The discussed energy-saving controllers are based on steady-state conditions. Therefore, the found solution will not be optimal in transient operation states. With the principles of optimal control or dynamic programming, it is possible to optimize a previously known repetitive load-cycle for minimum losses [46, 47]. An optimal flux trajectory is calculated offline and stored in a look-up table. During the load-cycle,

the flux reference is simply changed according to this optimized trajectory to maximize the total system efficiency also for transient states. This procedure is necessary if the load-cycle is characterized by continuously varying speeds and torques. If there are only sporadic changes of the working point with phases of constant operation in between, the energy-saving controllers for steady-state are appropriate.

2.1.2 Theoretical background of fundamental induction machine losses

In this section, the theory behind the fundamental loss components of induction machines is recapitulated. Understanding the loss components is a precondition for the successful implementation of energy saving control algorithms.

The losses of an induction machine are traditionally split into mechanical losses due to friction and windage, ohmic losses in the stator, and rotor windings, iron losses in the stator and rotor core and stray losses due to leakage fluxes,

$$P_{\mathrm{loss}} = P_{\mathrm{fric}} + P_{\mathrm{o,s}} + P_{\mathrm{o,r}} + P_{\mathrm{i,s}} + P_{\mathrm{i,r}} + P_{\mathrm{stray}}. \tag{2.1}$$

Friction and windage losses

The mechanical losses are caused by the air drag of the rotor and the friction losses in the bearings. They increase with the mechanical rotor frequency f_{R} and become especially important for high speed operation. As a first approximation the mechanical losses can be assumed to vary with

$$P_{\mathrm{fric}} = k_{\mathrm{fw}} \cdot f_{\mathrm{R}}^3, \tag{2.2}$$

but the exact behavior is usually determined with the standard no-load and blocked rotor measurements.

Ohmic losses

The fundamental ohmic losses of a three-phase induction machine are determined by the stator and rotor resistances according to

$$P_{\mathrm{o,s}} + P_{\mathrm{o,r}} = 3 \cdot R_{\mathrm{s}} \cdot I_{\mathrm{s}}^2 + 3 \cdot R_{\mathrm{r}} \cdot I_{\mathrm{r}}^2. \tag{2.3}$$

In a squirrel cage induction machine, the rotor windings are implemented using bars made of die-cast aluminium or copper. These are

subject to skin effect and therefore the resistance increases with the frequency. The frequency of the rotor currents is given with the slip frequency which is always very low in inverter-fed applications. Therefore, the skin effect can be neglected if only the fundamental frequency losses are considered. The stator windings are usually implemented with several wires per strand in order to reduce the skin effect. Again, for fundamental frequencies, the skin effect is negligibly small. Only if the losses due to harmonic currents are considered, the skin effect is important and should not be neglected. The harmonic losses are further considered in Section 2.2. Both resistances depend on the temperature. Especially the rotor resistance can change over a wide range during operation. Therefore, stator and rotor resistances are usually determined with the standard no-load and blocked-rotor tests after a certain period of rated operation in order to determine the values for a heated up machine.

Iron losses

Besides the ohmic losses in stator and rotor windings, also the iron losses in the stator- and rotor core have a significant share (up to 4% of the nominal power) of the total machine losses. Neglecting them always leads to a wrong prediction of machine efficiency and could also lead to a detuned control performance [48–50].

The iron losses can be separated into hysteresis losses and eddy-current losses. According to [51], the iron loss density can be approximated with

$$p_{\mathrm{i}} = p_{\mathrm{hys}} + p_{\mathrm{eddy}} = k_{\mathrm{hys}} \cdot fB^2 + k_{\mathrm{eddy}} \cdot f^2 B^2. \tag{2.4}$$

In an induction machine, the fields in the rotor fixed coordinate system, which are responsible for the iron losses in the rotor, rotate with the slip frequency f_{sl} given as

$$f_{\mathrm{sl}} = sl \cdot f_{\mathrm{e}}. \tag{2.5}$$

The relative slip is defined as

$$sl = \frac{f_{\mathrm{e}} - p \cdot f_{\mathrm{R}}}{f_{\mathrm{e}}}, \tag{2.6}$$

where p is the pole-pair number, f_{e} the stator frequency (the synchronous electrical frequency) and f_{R} the mechanical rotor frequency.

The iron losses are mainly caused by the mutual flux ϕ_{m}. If an average cross section for the mutual flux path is assumed, the total iron losses occuring in the stator and rotor core can be written as

$$P_{\mathrm{i,s}} + P_{\mathrm{i,r}} = k^*_{\mathrm{hys}} \cdot (1 + sl) f_{\mathrm{e}} \phi^2_{\mathrm{m}} + k^*_{\mathrm{eddy}} \cdot (1 + sl^2) f^2_{\mathrm{e}} \phi^2_{\mathrm{m}}. \tag{2.7}$$

The mutual flux is related to the air-gap voltage V_{m} (the voltage across the mutual inductance) according to

$$\phi_{\mathrm{m}} = c_1 \cdot \frac{V_{\mathrm{m}}}{f_{\mathrm{e}}}. \tag{2.8}$$

In an inverter-fed variable speed drive, the relative slip is small (1% - 4%) and the fundamental iron losses in the rotor can be neglected. Therefore, the total iron losses can be written as

$$P_{\mathrm{i}} = c^2_1 (k^*_{\mathrm{hys}} \cdot \frac{1}{f_{\mathrm{e}}} + k^*_{\mathrm{eddy}}) \cdot V^2_{\mathrm{m}}. \tag{2.9}$$

The iron losses are represented in the equivalent circuit of the induction machine with a resistance in parallel to the mutual inductance. The value of the equivalent core loss resistance is given as

$$R_{\mathrm{c}}(f_{\mathrm{e}}) = \frac{V^2_{\mathrm{m}}}{P_{\mathrm{i}}/3} = 3 \cdot \frac{1}{c^2_1 \left(\frac{k^*_{\mathrm{hys}}}{f_{\mathrm{e}}} + k^*_{\mathrm{eddy}} \right)}. \tag{2.10}$$

The equivalent core loss resistance is not constant as it depends on the stator frequency. It is usually determined with the standard no-load and blocked-rotor tests and is assumed to be independent on the load.

Stray load losses

The stray losses are the loss components in conductors and iron construction elements associated with stray fluxes and field pulsations due to the slotting and the associated non-ideal magnetic field distribution in the air-gap [15]. They are divided further into stray no-load losses and into additional stray load losses due to the changed stray flux paths because of local saturation during loaded operation. The stray no-load losses are already included in the conventional iron losses determined with the standard no-load and blocked-rotor tests. Therefore, the stray load losses are defined as the remaining loss component during loaded

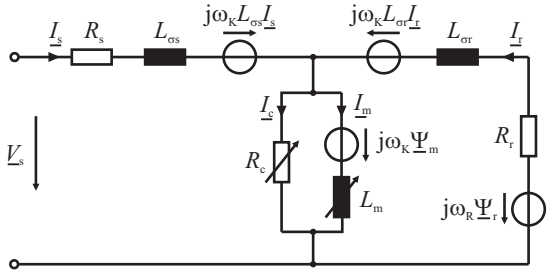

Figure 2.1: Dynamic induction machine equivalent circuit.

operation if all conventional losses are subtracted from the total measured losses as

$$P_{\text{stray}} = P_{\text{in}} - P_{\text{out}} - (P_{\text{fric}} + P_{\text{o}} + P_{\text{i}}). \tag{2.11}$$

The amount of the stray load losses depends heavily on the machine design and is in the range of 0.5% - 2% of the nominal power. There is no widely accepted way to model the dependency of the stray load losses on fundamental machine quantities. The international standards (IEEE 112-B, IEC 34-2, JEC 37) are inconsistent considering the measurement and description of the stray load losses [52]. According to IEEE 112-B, the stray load losses depend quadratically on the torque for a fixed frequency, whereas according to IEC 34-2, the stray load losses depend quadratically on the stator current. Therefore, it is also not clear how to represent the stray load losses in the equivalent circuit of the machine. Boglietti et al. suggested to include an additional resistance in series to the stator resistance [53, 54] to represent the stray load losses, whereas Levi et al. suggested to use a resistance in parallel to the rotor leakage inductance [55].

Concluding, if the dependency on the squared load torque is assumed, the stray load losses are only dependent on the operating point and can be neglected in the efficiency optimization as they would not change the optimal flux for a fixed operating point. This was also suggested in [23], where the stray load losses are considered to be not controllable.

2.1.3 Model based efficiency optimization

In this section, first the machine efficiency depending on the operating point (defined by the torque T_e and the angular rotor frequency ω_R) and on the rotor flux linkage Ψ_r is calculated. Using this expression, the optimal rotor flux linkage $\Psi_{\mathrm{r,opt}}$ maximizing the efficiency is derived which can be used in a model based controller in a field-oriented drive.

The efficiency analysis is based on the dynamic equivalent circuit rotating in an arbitrary reference frame with angular velocity ω_K depicted in Fig. 2.1. Amplitude invariant transformation is used. So the lengths of all space vectors are equal to the amplitudes of the corresponding phase quantity in the three phase system.

Some assumptions have been made in order to simplify the analysis:

- Only the mutual inductance L_m could be saturated, i.e. shows an inductance depending on the magnetizing current.
- The equivalent iron loss resistance R_c is frequency dependent.
- The stray load losses are neglected.
- The temperature dependency of stator and rotor resistances is neglected.

These simplifications allow to focus on the basic properties of the machine if it is controlled with the optimal rotor flux linkage. Especially the terminal behavior is of importance as it is the interface to the connected inverter. Compared to rated flux operation, the supplied stator voltage, the stator current, and the current to voltage phase displacement angle change considerably. This has an influence on the converter operating point and the associated losses in the semiconductors. Therefore, the total system efficiency will change. The main focus of this thesis is to reveal these interactions between converter and machine. The total system efficiency optimization is further considered in Chapter 5.

Although the efficiency analysis and the derivation of the optimal rotor flux linkage are carried out analytically, the shown graphics and plots are generated using the parameters of a specific induction machine. It is a standard 7.5kW machine (ecoDrives ACA 132 SB-2/HE) of efficiency class 1 characterized by the parameters summarized in Table 2.1. The parameters were determined with standard quasi no-load and blocked rotor tests with a sinusoidal supply voltage.

Table 2.1: Parameters of the induction machine.

Parameter	Variable	Value
Nominal power	P_n	7.5 kW
Nominal efficiency	η_n	89.6 %
Nominal voltage	V_n	230 V
Nominal current	I_n	13.7 A
Nominal torque	T_n	24.7 Nm
Nominal speed	n_n	2900 rpm
Mutual inductance	L_m	169.6 mH
Stator stray inductance	$L_{\sigma\mathrm{s}}$	3 mH
Rotor stray inductance	$L_{\sigma\mathrm{r}}$	3 mH
Stator resistance	R_s	0.46 Ω
Rotor resistance	R_r	0.59 Ω
Core loss resistance	$R_\mathrm{c,n}$	830 Ω
Friction losses	$P_\mathrm{fric,n}$	285 W
Pole pair number	p	1
Rated rotor flux linkage	$\Psi_\mathrm{r,n}$	0.986 Wb

The core loss resistance is modelled with a simple linear dependency on the stator frequency as suggested in [56]. In an inverter-fed machine, the slip frequency is small, therefore the stator frequency can also be replaced with the mechanical rotor frequency without significant loss of accuracy. With this approach, the core loss resistance is only dependent on the operating point what simplifies the derivation of the optimal rotor flux. Therefore, the core loss resistance is given as

$$R_\mathrm{c}(\omega_\mathrm{R}) = 50\,\Omega + 2.48\Omega/(rad/s)\cdot\omega_\mathrm{R}. \tag{2.12}$$

In a first step the mutual inductance is assumed to be constant. The influence of saturation is considered afterwards and the results are compared to the unsaturated case.

Machine efficiency with rated rotor flux linkage

In order to drive the induction machine in an efficiency optimal way, several control variables such as the slip frequency, the stator voltage, the stator, mutual, or rotor flux linkage could be used. Only one of these variables can be changed independently and the others are then

defined by the working point. Without lack of generality, the independent variable used for efficiency optimization in this work is the rotor flux. Therefore, the efficiency dependency on the working point and rotor flux linkage,

$$\eta = f(T_\mathrm{e}, \omega_\mathrm{R}, \Psi_\mathrm{r}), \tag{2.13}$$

has to be found. If a synchronously rotating reference frame with $\omega_\mathrm{K} = \omega_\mathrm{e}$ is assumed, the machine equations in steady-state simplify to the equation system 2.14.

$$\begin{aligned} V_\mathrm{sd} &= R_\mathrm{s} I_\mathrm{sd} - \omega_\mathrm{e} L_{\sigma\mathrm{s}} I_\mathrm{sq} - \omega_\mathrm{e} \Psi_\mathrm{mq} \\ V_\mathrm{sq} &= R_\mathrm{s} I_\mathrm{sq} + \omega_\mathrm{e} L_{\sigma\mathrm{s}} I_\mathrm{sd} + \omega_\mathrm{e} \Psi_\mathrm{md} \\ 0 &= -R_\mathrm{c} I_\mathrm{cd} - \omega_\mathrm{e} \Psi_\mathrm{mq} \\ 0 &= -R_\mathrm{c} I_\mathrm{cq} + \omega_\mathrm{e} \Psi_\mathrm{md} \\ 0 &= R_\mathrm{r} I_\mathrm{rd} - \omega_\mathrm{sl} \Psi_\mathrm{rq} \\ 0 &= R_\mathrm{r} I_\mathrm{rq} + \omega_\mathrm{sl} \Psi_\mathrm{rd} \end{aligned} \tag{2.14}$$

The flux linkages are given as

$$\begin{aligned} \Psi_\mathrm{md} &= L_\mathrm{m} \cdot (I_\mathrm{sd} + I_\mathrm{rd} - I_\mathrm{cd}) \\ \Psi_\mathrm{mq} &= L_\mathrm{m} \cdot (I_\mathrm{sq} + I_\mathrm{rq} - I_\mathrm{cq}) \\ \Psi_\mathrm{rd} &= L_{\sigma\mathrm{r}} I_\mathrm{rd} + \Psi_\mathrm{md} \\ \Psi_\mathrm{rq} &= L_{\sigma\mathrm{r}} I_\mathrm{rq} + \Psi_\mathrm{mq}. \end{aligned} \tag{2.15}$$

The synchronous electrical angular frequency is related to the mechanical angular rotor frequency and the angular slip frequency according to

$$\omega_\mathrm{e} = p \cdot \omega_\mathrm{R} + \omega_\mathrm{sl}. \tag{2.16}$$

The developed torque is given by the product of rotor flux linkage and rotor current as

$$T_\mathrm{e} = \frac{3}{2} p \left(\Psi_\mathrm{rq} I_\mathrm{rd} - \Psi_\mathrm{rd} I_\mathrm{rq} \right). \tag{2.17}$$

The constituting machine equations are in an arbitrary oriented reference frame. It can be defined to be rotor flux oriented without lack of generality. In that case, the d-axis of the reference frame is aligned in the direction of the rotor flux linkage space vector. Therefore, the q-component of the rotor flux linkage is equal to zero. The equations simplify accordingly and can be solved for the stator voltage and the stator current depending only on the working point and the rotor flux

linkage. This allows finally to solve for the input power and the electrical efficiency. The important quantities are summarized in the following

$$\begin{aligned}
\Psi_{\mathrm{rq}} &= 0 \\
I_{\mathrm{rd}} &= 0 \\
I_{\mathrm{rq}} &= -\frac{2}{3p}\frac{T_{\mathrm{e}}}{\Psi_{\mathrm{rd}}} \\
\omega_{\mathrm{sl}} &= \frac{2R_{\mathrm{r}}}{3p}\frac{T_{\mathrm{e}}}{\Psi_{\mathrm{rd}}^2} \\
\omega_{\mathrm{e}} &= p \cdot \omega_{\mathrm{R}} + \omega_{\mathrm{sl}} \\
\Psi_{\mathrm{md}} &= \Psi_{\mathrm{rd}} \\
\Psi_{\mathrm{mq}} &= \frac{2L_{\sigma\mathrm{r}}}{3p}\frac{T_{\mathrm{e}}}{\Psi_{\mathrm{rd}}} \\
I_{\mathrm{cd}} &= -\frac{\omega_{\mathrm{e}}}{R_{\mathrm{c}}}\Psi_{\mathrm{mq}} \\
I_{\mathrm{cq}} &= \frac{\omega_{\mathrm{e}}}{R_{\mathrm{c}}}\Psi_{\mathrm{md}} \\
I_{\mathrm{sd}} &= \frac{\Psi_{\mathrm{md}}}{L_{\mathrm{m}}} + I_{\mathrm{cd}} \\
I_{\mathrm{sq}} &= \frac{\Psi_{\mathrm{mq}}}{L_{\mathrm{m}}} - I_{\mathrm{rq}} + I_{\mathrm{cq}} \\
V_{\mathrm{sd}} &= R_{\mathrm{s}}I_{\mathrm{sd}} - \omega_{\mathrm{e}}L_{\sigma\mathrm{s}}I_{\mathrm{sq}} - \omega_{\mathrm{e}}\Psi_{\mathrm{mq}} \\
V_{\mathrm{sq}} &= R_{\mathrm{s}}I_{\mathrm{sq}} + \omega_{\mathrm{e}}L_{\sigma\mathrm{s}}I_{\mathrm{sd}} + \omega_{\mathrm{e}}\Psi_{\mathrm{md}} \\
T_{\mathrm{e}} &= -\frac{3}{2}p\Psi_{\mathrm{rd}}I_{\mathrm{rq}}.
\end{aligned} \tag{2.18}$$

The active input power is defined with

$$P_{\mathrm{in}} = \frac{3}{2}\left(V_{\mathrm{sd}}I_{\mathrm{sd}} + V_{\mathrm{sq}}I_{\mathrm{sq}}\right) = f(T_{\mathrm{e}}, \omega_{\mathrm{R}}, \Psi_{\mathrm{rd}}). \tag{2.19}$$

Finally, the machine efficiency can be calculated as

$$\eta = \frac{T_{\mathrm{e}}\omega_{\mathrm{R}}}{P_{\mathrm{in}}} = f(T_{\mathrm{e}}, \omega_{\mathrm{R}}, \Psi_{\mathrm{rd}}). \tag{2.20}$$

The resulting pure electrical machine efficiency plane plotted over the operating points is shown in Fig. 2.2 for rated rotor flux linkage. The efficiency drops considerably for low torque and low speed operation.

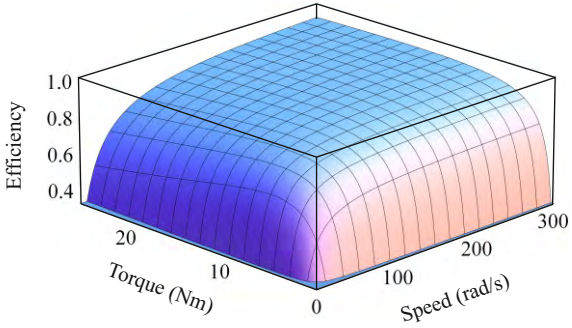

Figure 2.2: Electrical machine efficiency for operation with the rated rotor flux linkage.

Machine efficiency with optimal rotor flux linkage

In the following, the optimal rotor flux linkage is derived. From the viewpoint of machine efficiency, operation with rated flux is not optimal. During low torque operation, it leads to an unnecessarily high magnetizing current with associated ohmic losses as well as high iron losses. These can be reduced if the rotor flux linkage is adapted accordingly. If the machine efficiency is plotted over the rotor flux linkage (cf. Fig. 2.3) for different load torques, it is obvious that the efficiency maxima occur at rotor flux linkages different from the rated value ($\Psi_{\mathrm{r,n}} = 0.986\,\mathrm{Wb}$).

Actually, there is an optimal rotor flux linkage $\Psi_{\mathrm{r,opt}}$ leading to maximum efficiency over the full operating range. It can be found by differentiating the efficiency with respect to the rotor flux linkage and equating the derivative to zero as

$$\left.\frac{d\eta}{d\Psi_{\mathrm{r}}}\right|_{\Psi_{\mathrm{r,opt}}} = 0. \tag{2.21}$$

The exact equation for the machine efficiency resulting from the equation system 2.18 is complex and does not allow to find a simple closed form solution for $\Psi_{\mathrm{r,opt}}$. Considering the values of the machine parameters (cf. Table 2.1), it is reasonable to assume $L_{\sigma\mathrm{r}}^2 = 0, R_{\mathrm{c}}+R_{\mathrm{s}} = R_{\mathrm{c}}, R_{\mathrm{c}} + R_{\mathrm{r}} = R_{\mathrm{c}}$, what simplifies the machine efficiency equation to

$$\eta \approx \frac{6L_{\mathrm{m}}^2\omega_{\mathrm{R}}p^2\Psi_{\mathrm{r}}^2R_{\mathrm{c}}T_{\mathrm{e}}}{9p^2\Psi_{\mathrm{r}}^4R_{\mathrm{c}}R_{\mathrm{s}}+8L_{\sigma\mathrm{r}}L_{\mathrm{m}}R_{\mathrm{c}}R_{\mathrm{s}}T_{\mathrm{e}}^2+L_{\mathrm{m}}^2(3\omega_{\mathrm{R}}p^2\Psi_{\mathrm{r}}^2+2R_{\mathrm{c}}T_{\mathrm{e}})(3\omega_{\mathrm{R}}p^2\Psi_{\mathrm{r}}^2+2(R_{\mathrm{r}}+R_{\mathrm{s}})T_{\mathrm{e}})}. \tag{2.22}$$

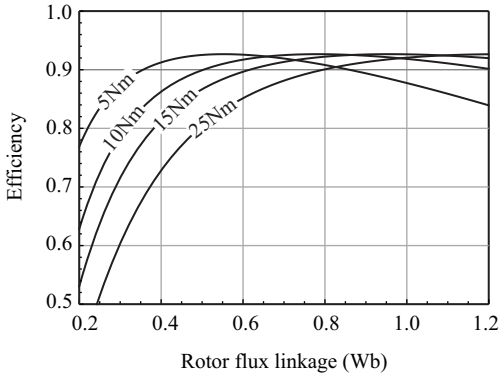

Figure 2.3: Electrical machine efficiency over the rotor flux linkage for different load torques and rated rotor speed.

This expression can now be differentiated. The optimal rotor flux linkage maximizing the machine efficiency results in

$$\Psi_{\mathrm{r,opt}} = \sqrt{\frac{2}{3p}} \cdot \left[\frac{L_{\mathrm{m}}^2 R_{\mathrm{c}}(R_{\mathrm{r}} + R_{\mathrm{s}}) + 2L_{\mathrm{m}} L_{\sigma\mathrm{r}} R_{\mathrm{c}} R_{\mathrm{s}}}{p^2 L_{\mathrm{m}}^2 \omega_{\mathrm{R}}^2 + R_{\mathrm{c}} R_{\mathrm{s}}} \right]^{\frac{1}{4}} \cdot \sqrt{T_{\mathrm{e}}}. \tag{2.23}$$

The rotor leakage inductance can be neglected if it is small and the equation reduces to

$$\Psi_{\mathrm{r,opt}} \approx \sqrt{\frac{2}{3p}} \cdot \left[\frac{L_{\mathrm{m}}^2 R_{\mathrm{c}}(R_{\mathrm{r}} + R_{\mathrm{s}})}{p^2 L_{\mathrm{m}}^2 \omega_{\mathrm{R}}^2 + R_{\mathrm{c}} R_{\mathrm{s}}} \right]^{\frac{1}{4}} \cdot \sqrt{T_{\mathrm{e}}}. \tag{2.24}$$

The optimal rotor flux linkage over the full operating range is depicted in Fig. 2.4 and Fig. 2.5. As expected, $\Psi_{\mathrm{r,opt}}$ is lower than the rated value for low torque operation. The optimization suggests to increase the rotor flux linkage above rated for high torque and low speed operation. This would decrease the torque producing current component and its associated losses. Nevertheless, if the saturation characteristics are considered, the magnetization current and its associated losses increase rapidly for a rotor flux linkage larger than rated and the optimum stays near the rated value.

The machine efficiency becomes independent of the load torque if it is controlled with $\Psi_{\mathrm{r,opt}}$. Obviously, this is only true for the linear machine neglecting saturation. As can be seen in Fig. 2.6, the machine efficiency stays constantly high over the complete torque range.

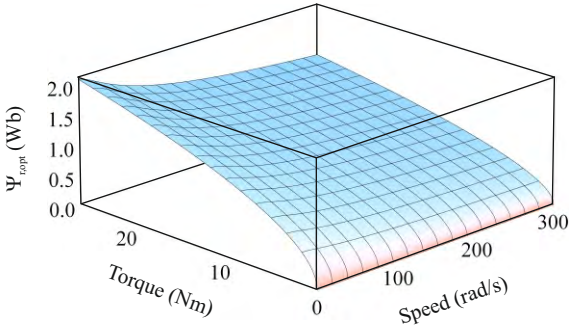

Figure 2.4: Optimal rotor flux linkage over the full operating range.

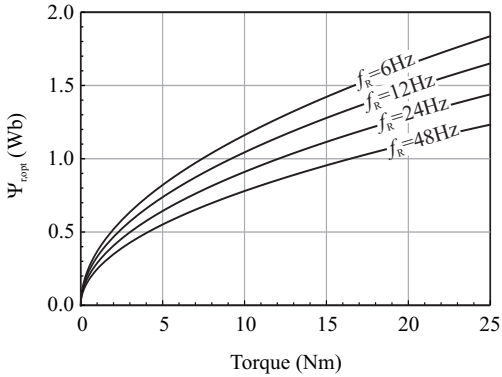

Figure 2.5: Optimal rotor flux linkage for different rotor speeds.

Constraints on rotor flux linkage reference

As already mentioned, the rotor flux linkage should not be increased above the rated value due to saturation effects. Standard induction machines are designed in such a way, that the mutual inductance is already slightly saturated in the nominal operating point. Therefore, an upper limit for $\Psi_{\mathrm{r,opt}}$ is introduced according to

$$\Psi_{\mathrm{r,max}} = \Psi_{\mathrm{r,n}}. \tag{2.25}$$

If the machine is operated with a reduced rotor flux linkage, the

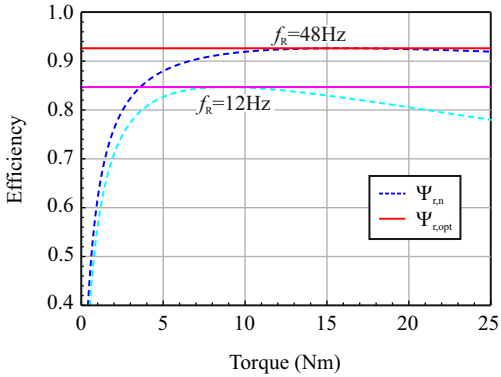

Figure 2.6: Machine efficiency with optimal rotor flux linkage.

transient torque response is detuned. The torque is given by

$$T_e = -\frac{3}{2} p \Psi_{rd} I_{rq} = \frac{3}{2} p \frac{L_m}{L_r} \Psi_{rd} \cdot (I_{sq} - I_{cq}). \tag{2.26}$$

A reduced rotor flux linkage has to be compensated with an increased stator current q-component. A lower limit for $\Psi_{r,opt}$ should be introduced to guarantee a specific pull-out torque. In order to keep the dynamic response of the speed controller similar to the operation with rated flux, the gain of the speed controller can be adapted online. The minimum value is set to

$$\Psi_{r,min} = 0.3 \cdot \Psi_{r,n}. \tag{2.27}$$

The optimal rotor flux linkage including the constraints is shown in Fig. 2.7 and the reachable machine efficiency in Fig. 2.8. It is not possible any more to increase the efficiency for high torques as the rotor flux is constrained. This conclusion is in accordance to a numerical analysis of the reachable efficiency if the saturation characteristics are included in the machine model (cf. Section 2.1.4).

Terminal behavior of the induction machine with optimal rotor flux linkage

The terminal behavior of the machine, meaning the stator voltage and stator current amplitudes, as well as the voltage to current phase displacement angle, has a direct impact on the efficiency of the inverter

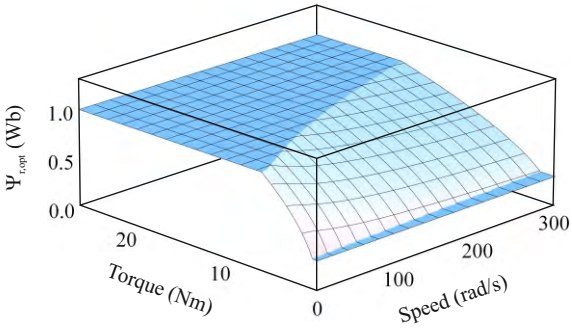

Figure 2.7: Optimal rotor flux linkage with limiting constraints.

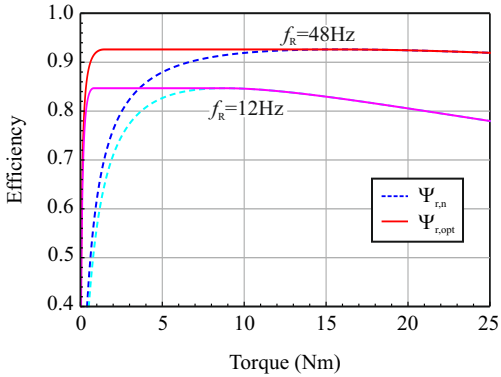

Figure 2.8: Reachable machine efficiency with constrained optimal rotor flux linkage.

supply. The terminal behavior is mainly dependent on the machine working point but it is also influenced by the rotor flux linkage. It is known that the power factor $\cos(\varphi_1)$ of the induction machine is low for part load operation and can be increased by the implementation of energy saving controllers.

In the following, stator voltage, stator current, and the voltage to current phase displacement angle are depicted for operation with rated and optimal rotor flux linkage.

Fig. 2.9 shows the reduction of the necessary stator voltage. Especially at high rotor speeds, the stator voltage can be reduced over a

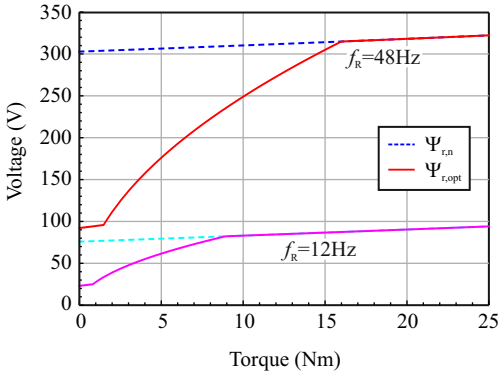

Figure 2.9: Stator voltage with rated and optimal rotor flux linkage.

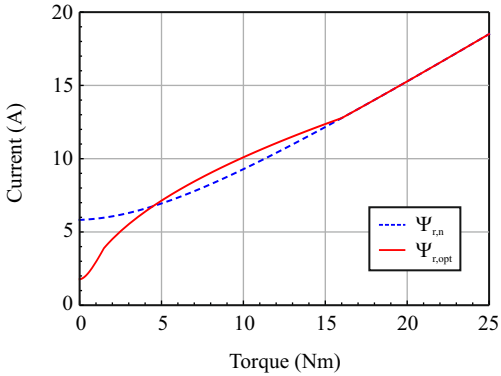

Figure 2.10: Stator current with rated and optimal rotor flux linkage.

wide torque range.

The supplied stator current is shown in Fig. 2.10. There is a certain torque range (5-15 Nm) where the decreased rotor flux linkage leads to an increase in the torque producing stator current q-component. The reduction of the field producing current d-component cannot completely compensate that effect and the total stator current increases. For very low torque ranges, the stator current is decreased compared to rated flux operation. The rotor speed has only a minor influence on the stator current behavior.

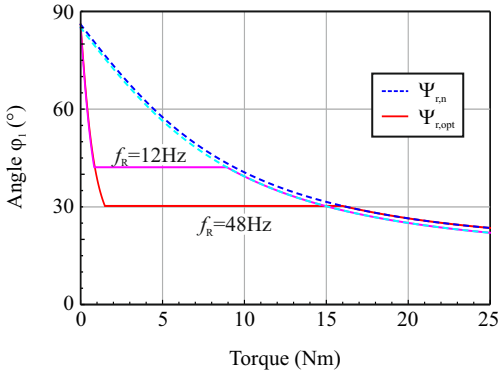

Figure 2.11: Voltage to current phase displacement angle with rated and optimal rotor flux linkage.

The voltage to current phase displacement angle φ_1 is depicted in Fig. 2.11. Again, for high speed operation, an impressive reduction of φ_1 can be observed. The phase displacement angle stays near 30° for a wide range of operation torques. This effect was exploited by the early energy saving controllers based on power factor control (cf. [17]).

The interactions of the machine terminal behavior and the converter efficiency are further analysed in Chapter 5.

Sensitivity analysis

In order to know how the model based maximum efficiency controller performs in a real implementation, a sensitivity analysis is necessary. Usually, the machine parameters are not known exactly but are prone to some estimation errors. Additionally, some parameters of the machine, such as the stator and the rotor resistance, vary during operation because of heating effects. The variation of the rotor resistance is more pronounced because the thermal connection to the enclosure of the machine is worse.

If the induction machine is controlled with $\Psi_{\mathrm{r,opt}}$, the efficiency reaches a maximum in all possible operating points. In a first step, the possible efficiency gain compared to operation with rated rotor flux

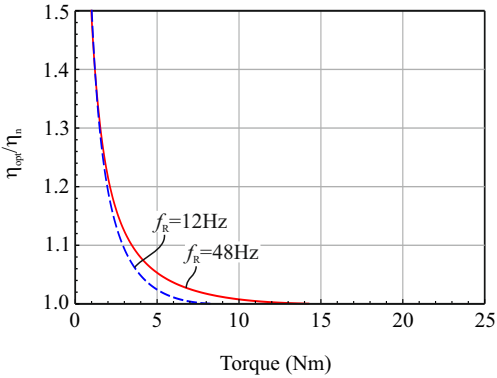

Figure 2.12: Gain in machine electrical efficiency due to operation with constrained optimal rotor flux linkage.

linkage can be calculated as

$$\frac{\eta_{\mathrm{opt}}}{\eta_n} = \frac{\eta\left(T_{\mathrm{e}}, \omega_{\mathrm{R}}, \Psi_{\mathrm{r,opt}}\right)}{\eta\left(T_{\mathrm{e}}, \omega_{\mathrm{R}}, \Psi_{\mathrm{r,n}}\right)} \tag{2.28}$$

$$\approx \frac{9p^2\Psi_{\mathrm{r,n}}^4 R_{\mathrm{c}}R_{\mathrm{s}} + L_{\mathrm{m}}^2\left(3\omega_{\mathrm{R}}p^2\Psi_{\mathrm{r,n}}^2 + 2R_{\mathrm{c}}T_{\mathrm{e}}\right)\left(3\omega_{\mathrm{R}}p^2\Psi_{\mathrm{r,n}}^2 + 2(R_{\mathrm{r}}+R_{\mathrm{s}})T_{\mathrm{e}}\right)}{6L_{\mathrm{m}}\Psi_{\mathrm{r,n}}^2\left(L_{\mathrm{m}}\omega_{\mathrm{R}}p^2(R_{\mathrm{c}}+R_{\mathrm{r}}+R_{\mathrm{s}}) + 2p\sqrt{R_{\mathrm{c}}(R_{\mathrm{r}}+R_{\mathrm{s}})\left(L_{\mathrm{m}}^2\omega_{\mathrm{R}}^2p^2 + R_{\mathrm{c}}R_{\mathrm{s}}\right)}\right)T_{\mathrm{e}}}. \tag{2.29}$$

For the given machine parameters, the machine electrical efficiency gain is plotted in Fig. 2.12 for operation with the constrained optimal rotor flux linkage. The efficiency gain is approximately 5 % for a load torque of $20\% \cdot T_{\mathrm{n}}$. Generally, the efficiency gain is greater for a low efficiency machine obtaining high iron losses than for a machine of the highest efficiency class. Alternatively, the total loss reduction could be considered (cf. Chapter 5).

The optimal rotor flux linkage depends on estimates of the stator and rotor resistance, the mutual inductance, and the core loss resistance. If one or several of these parameters are wrongly estimated, the calculated flux reference will differ from the ideal optimal flux. Therefore, the machine will not reach the maximum efficiency that would be possible for a given operating point.

As a performance criterion, the sensitivity is calculated as percentage of the maximum possible efficiency (if the exact machine parameters

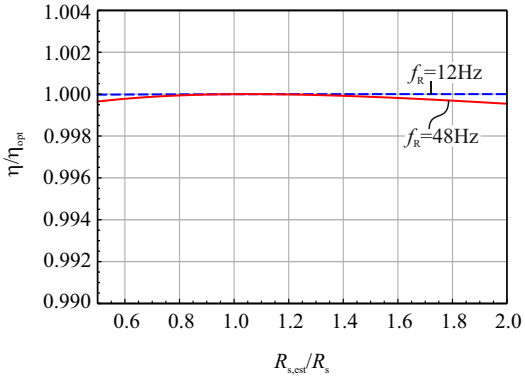

Figure 2.13: Sensitivity on stator resistance estimate.

would be known) to the actually reached efficiency with the optimal flux reference calculated using the estimated parameters as

$$\frac{\eta}{\eta_{\mathrm{opt}}} = \frac{\eta\left(T_{\mathrm{e}}, \omega_{\mathrm{R}}, \Psi_{\mathrm{r,opt}}\left(R_{\mathrm{s,est}}, R_{\mathrm{r,est}}, R_{\mathrm{c,est}}, L_{\mathrm{m,est}}\right)\right)}{\eta\left(T_{\mathrm{e}}, \omega_{\mathrm{R}}, \Psi_{\mathrm{r,opt}}\left(R_{\mathrm{s}}, R_{\mathrm{r}}, R_{\mathrm{c}}, L_{\mathrm{m}}\right)\right)}. \tag{2.30}$$

The reached efficiency is always below the maximum efficiency if one or several parameters are wrongly estimated.

The following figures show the performance if one parameter is mismatched and the others are correct. The sensitivity is independent of the load torque. From Fig. 2.13 it can be seen that the sensitivity to a wrongly estimated stator resistance is very low. In fact, the stator resistance can be mismatched by more than 100% and the reached efficiency is still more than 99.9% of the maximum possible value. This is because the stator resistance nearly cancels out of the optimal rotor flux equation if the numerical values of the machine parameters are inserted.

Also the sensitivity to a wrongly estimated rotor resistance is very low (cf. Fig. 2.14). The efficiency is still more than 99.6% of the maximum if the estimated value is mismatched by 100%. Since rotor resistance changes of 100% during warmup are common, it is a feasible approach to use a constant rotor resistance value equal to the resistance of the warmed up machine for the estimation. No online adaptation is needed.

From Fig. 2.15 it can be seen that also the sensitivity to a wrongly

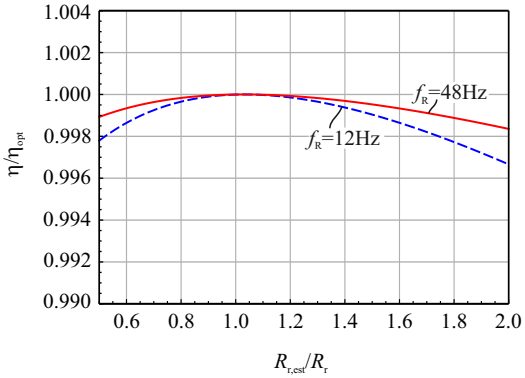

Figure 2.14: Sensitivity on rotor resistance estimate.

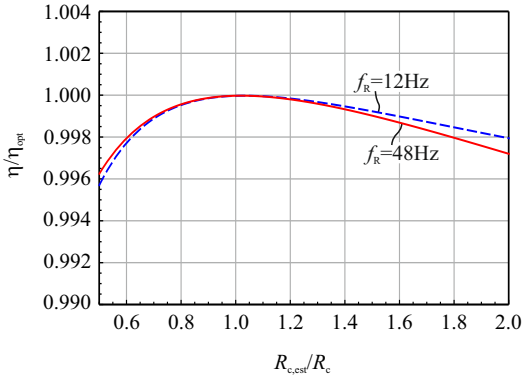

Figure 2.15: Sensitivity on core loss equivalent resistance estimate.

estimated equivalent core loss resistance is very low.

The only parameter which has to be estimated more accurately is the mutual inductance. A noteworthy decrease of the efficiency occurs if the estimated mutual inductance is mismatched by more than 50%, especially at low rotor speeds. As the mutual inductance is affected by saturation, an accurate estimation is necessary.

In a real implementation, all of the parameters could be wrongly estimated at the same time. A combination of different parameter mismatches leads in some cases to a stronger decrease in efficiency. However, if the mutual inductance is correctly estimated (±10%), all

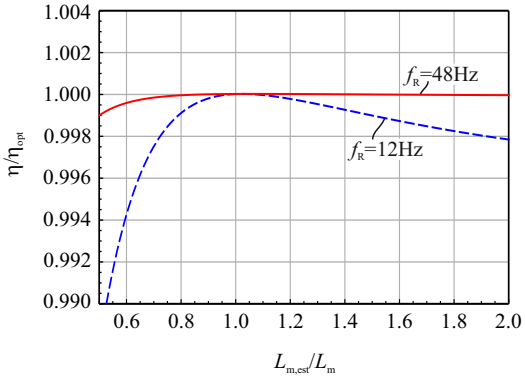

Figure 2.16: Sensitivity on mutual inductance estimate.

combinations of possible mismatches in a variation of ±40% will lead to an efficiency of 99% of the maximum value for low speed and even more than 99.5% of the maximum for high speed operation. Summing up, the sensitivity of the model based energy saving controller on parameter estimates is very low. Only the mutual inductance should be identified accurately to guarantee a good performance of the algorithm.

2.1.4 Impact of saturation of the mutual inductance

The saturation characteristics of an induction machine have direct impact on the optimal rotor flux linkage for maximum efficiency. As the magnetizing current rises sharply in the saturated machine, also the associated stator ohmic losses increase. The optimization of the linear machine model indicates that the efficiency can be increased during low speed and high torque operation if the rotor flux linkage is increased above its rated value (cf. Fig. 2.6 and Fig. 2.5). This finding is only partly valid for the saturated machine and depends also on the actual machine design. A high efficiency induction machine (efficiency class 1) is usually designed to operate at rated flux still in the linear magnetic range whereas a standard induction machine is designed to operate at rated flux already in the saturation knee.

According to [57], the mutual inductance saturation characteristic

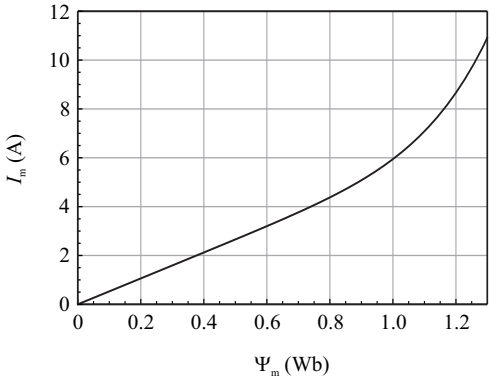

Figure 2.17: Saturation characteristic of the mutual inductance.

can be approximated with

$$\frac{I_{\mathrm{m}}}{I_{\mathrm{m,n}}} = \beta \frac{\Psi_{\mathrm{m}}}{\Psi_{\mathrm{m,n}}} + (1-\beta)\left(\frac{\Psi_{\mathrm{m}}}{\Psi_{\mathrm{m,n}}}\right)^{S} \tag{2.31}$$

For a high efficiency machine, the parameters $S = 7$ and $\beta = 0.9$ can be used to model the saturation curve. Fig. 2.17 shows the dependency of the magnetizing current on the mutual flux linkage.

In the rotor flux oriented machine model defined by the equation system 2.18, the inverse magnetizing characteristics given as

$$\frac{1}{L_{\mathrm{m}}} = \frac{|I_{\mathrm{m}}|}{|\Psi_{\mathrm{m}}|} \tag{2.32}$$

are necessary and they are separated into the d- and q-components as

$$\begin{aligned} I_{\mathrm{md}} &= \Psi_{\mathrm{md}} \cdot \frac{1}{L_{\mathrm{m}}\left(|\Psi_{\mathrm{m}}|\right)} \\ I_{\mathrm{mq}} &= \Psi_{\mathrm{mq}} \cdot \frac{1}{L_{\mathrm{m}}\left(|\Psi_{\mathrm{m}}|\right)}. \end{aligned} \tag{2.33}$$

If the saturation characteristic is included, the optimal rotor flux linkage $\Psi_{\mathrm{r,opt,sat}}$ can be found with numerical methods. A comparison between $\Psi_{\mathrm{r,opt}}$ and $\Psi_{\mathrm{r,opt,sat}}$ is given in Fig. 2.18. In the low torque range, the linear and the saturated model give the same results. As the high efficiency machine at hand is designed to operate mostly in

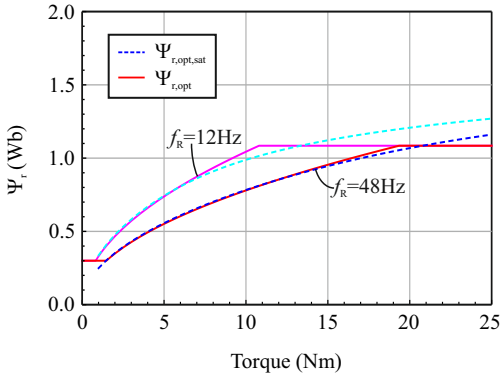

Figure 2.18: Optimal rotor flux linkage considering the saturation characteristic of the machine.

the linear magnetic region, the constrained optimal rotor flux linkage obtained with the linear model is a good approximation to the real optimum. The numerical solution suggests to increase the upper constraint for the rotor flux linkage slightly, as the optimum is still above the rated value for low speed and high torque operation. A reasonable compromise is setting $\Psi_{\mathrm{r,max}} = 1.1 \cdot \Psi_{\mathrm{r,n}}$.

If the optimal solution obtained with the saturated model is compared with the unconstrained solution from the linear model (cf. Fig. 2.5), the optimal rotor flux linkage is not increased that much for low speed and high torque operation. This is because of the increased magnetization current and the associated ohmic losses.

The reachable machine efficiency considering the saturation characteristic is shown in Fig. 2.19. Noteworthy is the efficiency increase for low speed and high torque operation if the rotor flux linkage is increased above its rated value. This effect would be less pronounced for a standard efficiency machine which is designed to have its rated flux value closer to the saturation knee.

The linear solution using the rated mutual inductance gives still good results and reaches the efficiency maximum in most operating points. Although it is possible to calculate the numerical optimum considering the saturation characteristics online with a DSP implementation (cf. [45]) it is suggested to implement the linear solution using Eq. 2.24 and to set a limit for the maximum rotor flux linkage of

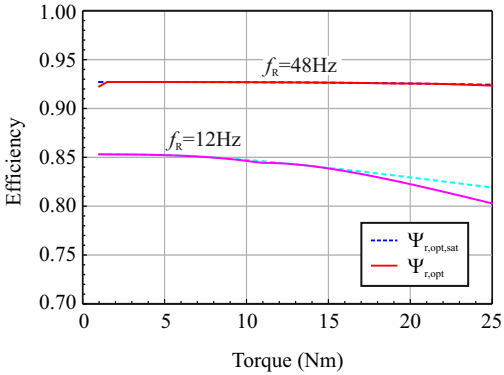

Figure 2.19: Machine efficiency with the optimal rotor flux linkage considering the saturation characteristic of the machine.

$\Psi_{r,max} = 1.1 \cdot \Psi_{r,n}$. This will lead to maximum efficiency operation in most operating points with considerably less implementation effort compared to a numerical solution accounting for the saturation characteristic. Another option, especially for a high power machine, would be to calculate $\Psi_{r,opt,sat}$ offline and store it in a lookup table.

2.1.5 Implementation

The optimal rotor flux linkage (Eq. 2.24) can be used to implement an energy saving controller based on a standard rotor flux oriented control scheme. The complete control block diagram is shown in Fig. 2.20. Usually, a rotor flux oriented controller consists of two current controllers for the direct and quadrature current components in the synchronous reference frame, a rotor speed controller and a rotor flux controller. The speed controller output is the reference for the torque producing q-component of the stator current whereas the flux controller output is the reference for the flux producing d-component of the stator current. Four PI-type controllers with anti-windup circuits have been implemented. The block "optimal flux calculation" is added to the control scheme. It generates the optimal rotor flux linkage reference using the machine parameters and the operating point variables torque and speed as inputs.

The electrical torque T_e, the synchronous frequency ω_e and the rotor

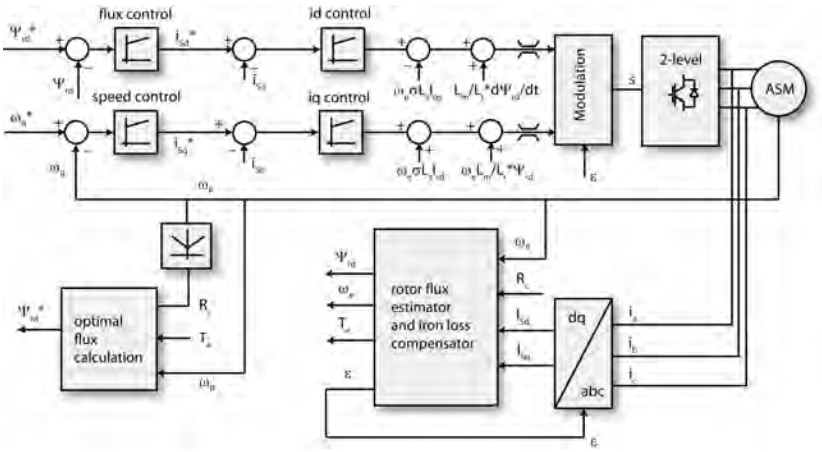

Figure 2.20: Control structure with rotor flux estimator and efficiency optimal rotor flux reference generation.

flux linkage $\Psi_{\mathrm{r,d}}$ are estimated with an enhanced model accounting for the iron losses, which is described in [50]. The iron losses lead to a reduced performance of the standard estimator as the rotor flux linkage, the torque and the slip frequency are wrongly estimated if the iron loss resistance is not included in the estimator model. Especially at nominal speed, the estimation error can be several percent of the actual value.

The estimated variables considering the equivalent iron loss resistance are given with

$$\Psi_{\mathrm{rd}} = \frac{L_{\mathrm{m}}}{1 + s \cdot \frac{L_{\sigma\mathrm{r}}}{R_{\mathrm{r}}}} \cdot I_{\mathrm{md}} \tag{2.34}$$

$$\omega_{\mathrm{sl}} = \frac{L_{\mathrm{m}} R_{\mathrm{r}}}{L_{\sigma\mathrm{r}}} \cdot \frac{I_{\mathrm{mq}}}{\Psi_{\mathrm{rd}}} \tag{2.35}$$

$$T_{\mathrm{e}} = \frac{3}{2} p \frac{L_{\mathrm{m}}}{L_{\sigma\mathrm{r}}} \Psi_{\mathrm{rd}} I_{\mathrm{mq}}. \tag{2.36}$$

The magnetizing current components can be expressed with the stator

current components as

$$\begin{aligned} I_{\mathrm{md}} &= \frac{L_{\sigma\mathrm{r}}}{L_{\mathrm{r}}} \frac{1}{1+s\tau_{\mathrm{c}}} \left(I_{\mathrm{sd}} + \frac{\Psi_{\mathrm{rd}}}{L_{\sigma\mathrm{r}}} + \frac{\omega_{\mathrm{e}} L_{\mathrm{m}}}{R_{\mathrm{c}}} I_{\mathrm{mq}} \right) \\ I_{\mathrm{mq}} &= \frac{L_{\sigma\mathrm{r}}}{L_{\mathrm{r}}} \frac{1}{1+s\tau_{\mathrm{c}}} \left(I_{\mathrm{sq}} - \frac{\omega_{\mathrm{e}} L_{\mathrm{m}}}{R_{\mathrm{c}}} I_{\mathrm{md}} \right) \\ \tau_{\mathrm{c}} &= \frac{L_{\sigma\mathrm{r}} L_{\mathrm{m}}}{L_{\mathrm{r}} R_{\mathrm{c}}}. \end{aligned} \tag{2.37}$$

As the time constant τ_{c} is very small, the low-pass element can be neglected and a direct solution for the magnetizing components is found as

$$\begin{aligned} I_{\mathrm{md}} &= \frac{L_{\sigma\mathrm{r}}}{L_{\mathrm{r}}} \left(I_{\mathrm{sd}} + \frac{\Psi_{\mathrm{rd}}}{L_{\sigma\mathrm{r}}} + \frac{\omega_{\mathrm{e}} L_{\mathrm{m}}}{R_{\mathrm{c}}} I_{\mathrm{mq}} \right) \\ I_{\mathrm{mq}} &= \frac{L_{\sigma\mathrm{r}}}{L_{\mathrm{r}}} \left(I_{\mathrm{sq}} - \frac{\omega_{\mathrm{e}} L_{\mathrm{m}}}{R_{\mathrm{c}}} I_{\mathrm{md}} \right). \end{aligned} \tag{2.38}$$

Eq. 2.38 can directly be used together with Eqs. 2.34-2.36 to build the enhanced estimator. The implementation effort is not considerably increased compared to the standard rotor flux estimator (cf. [13]). Because the equivalent core loss resistance is anyway required for the model based efficiency optimizer, no additional machine parameters have to be estimated.

In order to determine the control performance with the energy saving controller, several operating points and load steps were simulated with MATLAB/Simulink using a dynamic machine model including iron losses and saturation of the mutual inductance. The machine model was initialized with parameters of the test machine previously determined and summarized in Table 2.1.

The gain of the speed controller is adapted online in order to keep the control performance high and to ensure a decoupling from the variable rotor flux linkage. The proportional gain of the PI controller is adapted with

$$k_{\mathrm{p}} = k_{\mathrm{p,n}} \cdot \frac{\Psi_{\mathrm{r,n}}}{\Psi_{\mathrm{rd}}}. \tag{2.39}$$

As an example, the speed ramp from standstill to rated speed and subsequent changes of the load torque are shown here. The rotor speed is depicted in Fig. 2.21. As expected, the rated speed is reached with maximum acceleration limited only by the current limit of the inverter. The corresponding current of phase A is shown in Fig. 2.22.

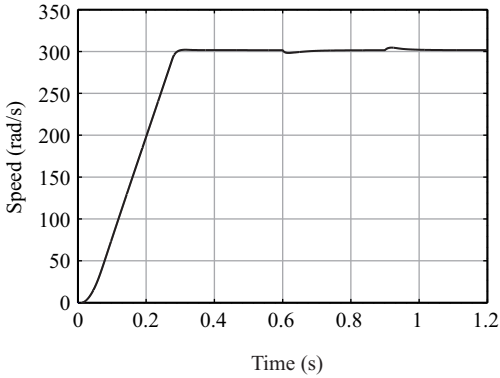

Figure 2.21: Simulated time behavior of the rotor speed.

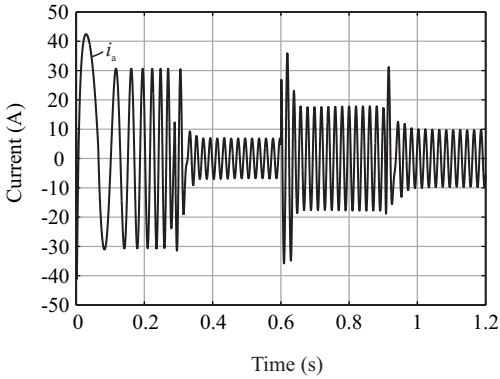

Figure 2.22: Simulated time behavior of the stator phase current.

The time behavior of the load torque is depicted in Fig. 2.24. Initially, the load torque is set to 5 Nm but the generated torque is much higher during the acceleration phase. At $t = 0.6\,\mathrm{s}$, the load torque is increased to nominal torque and finally decreased to 10 Nm at $t = 0.9\,\mathrm{s}$. The corresponding rotor flux linkage is shown in Fig. 2.23. Initially, it is set to the upper limit and is decreased afterwards in order to meet the optimal reference for a reduced load torque. As can be seen, the actual rotor flux linkage follows the reference value without much overshoot. Although no low-pass filter is applied for calculating the optimal rotor flux linkage, there are no stability problems and no noticeable detuning

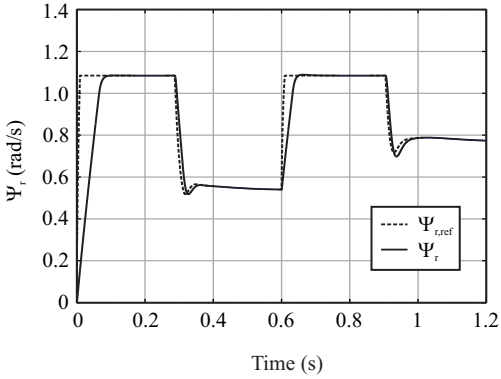

Figure 2.23: Simulated time behavior of the rotor flux linkage and its reference value.

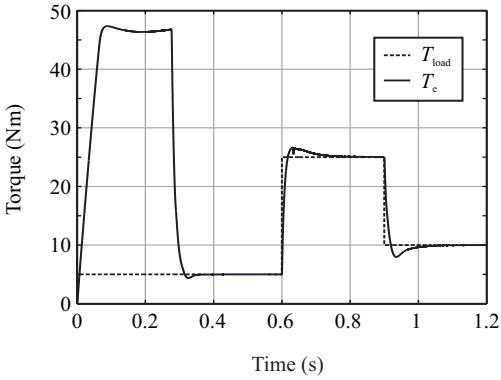

Figure 2.24: Simulated time behavior of the load torque and the electrical torque.

of the speed control loop occurs.

2.1.6 Detection of the equivalent core loss resistance

The model based energy saving controller requires several machine parameters. Among the standard equivalent circuit parameters, that are needed for every field oriented controller (mutual inductance, stator and rotor resistance), additionally the equivalent core loss resistance must

be determined.

Automatic determination of the induction machine parameters is a topic since the first variable speed drives were equipped with microcontrollers and especially since field oriented control concepts were applied. Therefore, hundreds of estimation algorithms and patents have been published for the automatic estimation of the machine parameters, either during an initial commissioning run or online during operation of the machine. Most of the publications concentrate uniquely on the determination of the standard induction machine parameters. The equivalent core loss resistance is usually not estimated as it is often neglected and not required for the simplified field oriented control structure.

As there are so many concepts developed and readily available, it is assumed that the standard parameters have already been estimated with a suitable algorithm and can be used for the efficiency optimized drive system. The sensitivity analysis presented previously revealed that the parameters do not have to be estimated with a high accuracy, except for the mutual inductance. Reviews on the available machine parameter estimation concepts are given in [58–61].

Only few publications consider the identification of the equivalent core loss resistance directly with the drive inverter. Usually, the core loss resistance is identified with the standard no-load or the quasi no-load test. There, the consumed active and reactive power for a given rotor speed and variable stator voltage are recorded and the core loss resistance can be reconstructed. In the quasi no-load test, the rotor is not driven by an external machine to synchronous speed but is allowed to rotate freely without external load torque applied. Accordingly, only friction and windage are acting which can be determined by interpolation of the recorded active power versus stator voltage curve towards $V_\mathrm{s} = 0$ where no core-losses occur. The inverter could be used to automatically conduct the quasi no-load test and determine the iron loss resistance as in [50]. A certain estimation error is usually made as there are additional rotor losses because the slip speed is not zero. A different approach was suggested in [56]. There, an estimator is used to calculate an error term very sensitive to the core-loss resistance. The core loss resistance is subsequently adapted to drive this error term to zero during operation.

Automatic core loss resistance estimation with a dynamic no-load deceleration test

Here, a further method to identify the core loss resistance during an initial commissioning run is presented. The method is based on a deceleration test. The rotor must be allowed to accelerate to rated speed and subsequently passively decelerate. It is anyway hardly possible to identify the core loss resistance at standstill as it represents the iron losses due to the rotational field during standard operation. The proposed method even works with an applied load torque although the estimation accuracy is better for a long deceleration phase.

The idea behind the estimation algorithm is to reach the true no-load condition in electrical quasi steady-state. Due to the moment of inertia of the rotor, the mechanical process of deceleration has a high time constant compared to the electrical processes in the machine. Therefore, during the slow deceleration process the machine appears to be in quasi steady-state for the electrical quantities.

The true no-load condition is characterized by a slip frequency of $f_{\mathrm{sl}} = 0\,\mathrm{Hz}$. As there are no currents induced in the rotor windings, the ohmic rotor losses are equal to zero and there is no transmitted mechanical power (except if there is a remanence rotor flux or a reluctance torque). The complete active input power is converted into stator ohmic losses and into core losses.

The algorithm can be summarized with the following steps:

1. The machine is accelerated to nominal speed.

2. The coordinate system is changed from the electrical synchronous system to the rotor synchronous system.

3. The rotor starts to decelerate.

4. The current amplitude must be kept constant with the current controller.

5. The active power, stator current, and stator voltage are recorded together with the stator frequency during the deceleration phase.

6. After subtracting the stator ohmic losses, the core losses are available and can be used to determine the frequency dependent equivalent core loss resistance.

If the input power is measured correctly, the iron losses can be calculated with

$$P_{\mathrm{i}} = P_{\mathrm{in}} - \frac{3}{2} R_{\mathrm{s}} |\underline{I}_{\mathrm{s}}|^2. \tag{2.40}$$

As the current in the no-load condition is mostly inductive, the amplitude of the voltage over the mutual inductance V_{m} can be approximated with

$$|\underline{V}_{\mathrm{m}}| \approx |\underline{V}_{\mathrm{s}}| - \omega_e L_{\sigma \mathrm{s}} |\underline{I}_{\mathrm{s}}|. \tag{2.41}$$

Finally, the equivalent core loss resistance is given as

$$R_{\mathrm{c}} = \frac{3}{2} \frac{|\underline{V}_{\mathrm{m}}|^2}{P_{\mathrm{i}}}. \tag{2.42}$$

The method was tested with the simulation of the drive system based on MALTAB/Simulink. The control is implemented with a discrete, triggered subsystem in order to model the behavior of a DSP implementation. The results of the estimation process are depicted in Fig. 2.25. At the time instant t_{Tr}, the algorithm is activated and the reference frame is changed to the rotor oriented reference frame. The rotor angle is usually measured with a resolver. As the slip speed is now equal to zero, the rotor current and the associated torque decays to zero with the rotor time constant defined as $\tau_{\mathrm{r}} = L_{\mathrm{r}}/R_{\mathrm{r}}$. The estimated core loss resistance $R_{\mathrm{c,est}}$ matches the actual core loss resistance as soon as the produced torque is equal to zero. The core loss resistance is decreasing with decreasing speed due to the dominance of the hysteresis iron losses (cf. Eq. 2.10). The machine should be accelerated to 10% above rated speed in order to provide enough time for the rotor current to decay and to allow an estimation of the equivalent core loss resistance at rated speed.

Alternatively, the torque-producing q-component reference of the current controller can be set to zero in order to force the torque to zero. Because of possible alignment errors of the rotor flux oriented control system, the actually generated torque can still deviate from zero. The reference frame should still be changed to the rotor oriented reference frame in order to guarantee zero slip frequency.

Although the basic concept is very simple, there are some details which have to be considered.

Changing the flux linkage of a three-phase coil is related to delivering active power as

$$P = \frac{dE(t)}{dt} = \frac{3}{4} L \frac{d\hat{I}^2}{dt} = \frac{3}{4} \frac{1}{L} \frac{d\hat{\Psi}^2}{dt}. \tag{2.43}$$

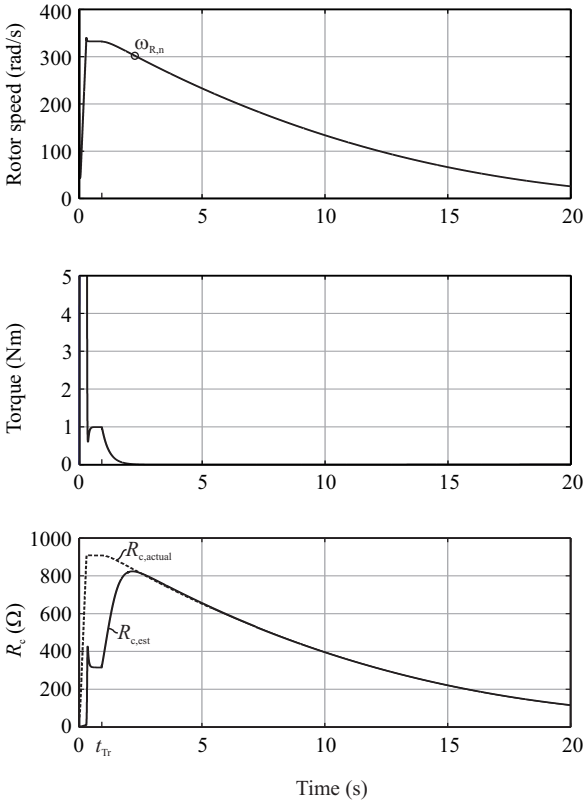

Figure 2.25: Rotor speed, torque and estimated core loss resistance during the deceleration phase.

Therefore, the amplitude of the phase currents should stay constant during the deceleration phase. This can be achieved by freezing the references of the current controllers at the beginning of the deceleration phase.

During the transition from the electrical synchronous reference frame to the rotor reference frame, a step in the stator voltage angle should be avoided. Such a step would lead to high current and torque oscillations which impact the deceleration process and disturb the estimation process. A smooth transition can be achieved by observing the electrical angle of the synchronous reference frame and the rotor angle. As

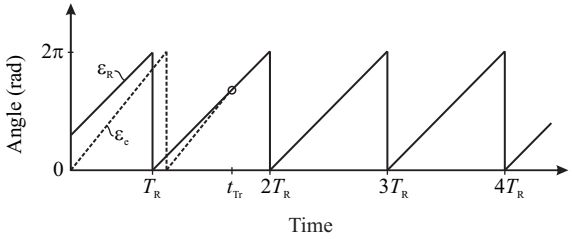

Figure 2.26: Smooth transition between the electrical synchronous reference frame and the rotor oriented reference frame.

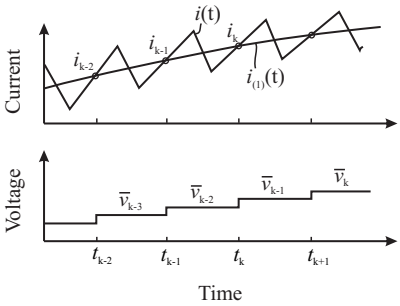

Figure 2.27: Timing diagram of current sampling and voltage generation.

the synchronous frequency is always slightly higher than the rotor frequency, these two angles will become equal periodically. At this point the reference system is switched to the rotor oriented reference frame and no voltage step is generated (cf. Fig. 2.26).

The most important and most critical point of the proposed algorithm is the accurate input power calculation. As the losses are quite small compared to the consumed reactive power, the power factor is nearly zero. Therefore, already small time shifts between voltage and current measurement points lead to considerable deviations in the calculated active power. Usually, the applied stator voltage is not measured but directly obtained from the current controller outputs. It has to be considered that the voltage space vector is applied not until the next sampling period, depending on the implemented update mode on the DSP.

Fig. 2.27 shows the exact timing diagram of a possible implementa-

tion. It has to be ensured that the measured mean current value during a sample period and the applied voltage belong effectively to the same time instant. Accordingly, for the depicted timing diagram, the input power at time instant k is calculated with

$$P_{\mathrm{k}} = \mathrm{Re}\left\{ \frac{\underline{I}_{\mathrm{s,(k)}} + \underline{I}_{\mathrm{s,(k\text{-}1)}}}{2} \cdot \underline{V}^{*}_{\mathrm{s,(k\text{-}2)}} \right\}. \tag{2.44}$$

The presented approach allows to identify the equivalent core loss resistance with low software effort and sufficient accuracy for usage with the energy saving controller. Experimental validation of the proposed estimation algorithm can be found in [61].

2.2 Harmonic machine losses

2.2.1 Literature review

The behavior of an electrical machine that is supplied by a distorted voltage source was first considered at the end of the 1920s [14]. It was found that low order current harmonics can produce parasitic steady-state torques which add or subtract (depending on the direction of rotation of the produced harmonic magnetic field) from the torque produced by the fundamental current component. As the parasitic torques occur pairwise with opposite sign and due the fact that their magnitude decays with the harmonic order, the resulting parasitic torque is very small and was assumed to be negligible [62, 63]. Besides steady-state parasitic torques, there are also pulsating torques due to interactions of fields with different harmonic orders [63]. The average value of the pulsating torques is zero.

It was further observed that the losses in the machine can increase if there are harmonics in the supply voltage. This effect gained attention at the end of the 1960s as first machines were supplied with the upcoming static frequency converters, often producing a simple six-step block shaped output voltage containing low-order harmonics with high magnitudes. Consequently, there are harmonic currents flowing that produce additional ohmic losses in the stator and rotor windings. Due to the skin effect, especially the ohmic losses in the rotor of squirrel cage induction machines can increase considerably [63–67]. The skin effect was intentionally fortified in induction machines with a deep bar cage rotor in order to limit the current during high slip operation at

start-up. These machines therefore showed a considerable increase of the harmonic losses.

The additional ohmic losses can not fully explain the observed increase of the machine losses when supplied from a distorted voltage source. There is also an increase in iron losses. Machine iron losses are traditionally split into core losses produced by the mutual flux and into stray-losses or stray load losses produced by the various leakage fluxes. The stray load losses can further be separated into zig-zag losses, motor-end losses, skewing losses and additional losses [15].

The main part of the increased iron losses is due to harmonic stray load losses. Harmonic stray fields increase the hysteresis and the induced eddy-current losses, especially in the stator and rotor teeth and in the end-regions [63,64,67]. Also skewing of the rotor bars can increase the harmonic stray load losses considerably [64]. Contrary, the increase in core losses due to the harmonic mutual flux components is small, as the harmonic currents induced in the rotor cancel the harmonic mutual flux [63, 64, 67].

A complete induction machine equivalent circuit incorporating all harmonic loss components was first presented by Honsinger [67]. There, resistors are placed in parallel to the leakage inductances in order to account for the harmonic stray load losses (cf. Fig. 2.28). All impedances of the model are frequency dependent in order to account for the skin-effect and the frequency dependency of the leakage inductances. The model is evaluated for each harmonic frequency and the machine response on the distorted voltage source is finally found by superposition. Also the total losses can be found by superposition although this is only an approximation because of nonlinearity due to saturation and the dependence of the iron loss components on the premagnetization. The loss model was refined in [68] and transformed into the synchronous reference frame in [69].

An impressive work to model the harmonic losses for a broad range of induction machines with different power ratings was presented in [70]. A semi-empirical loss model was constructed incorporating the harmonic ohmic stator and rotor losses as well as the harmonic iron losses. A loss factor was introduced describing the additonal harmonic losses depending on the power rating of the machine and the voltage or current spectrum. With the detailed models it was also concluded that the relative importance of the harmonic iron losses (mainly stray load losses) increase with the harmonic frequency and are dominating over

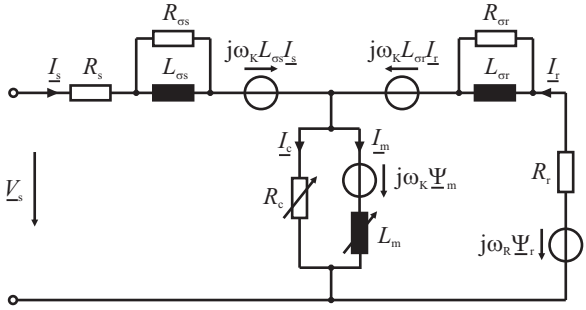

Figure 2.28: Complete machine equivalent circuit including resistors in parallel to the leakage inductances.

the harmonic ohmic losses for $f_h \geq 2.5\,\text{kHz}$ even if the skin effect is included.

A theoretical analysis on the frequency dependency of the various harmonic loss components was given in [71]. The harmonic ohmic losses decay approximately inversely with the frequency if a constant harmonic voltage amplitude is assumed. Due to various effects, the harmonic iron losses decay with the frequency for low frequencies, then stay nearly constant and finally would slightly increase with the frequency for very high frequencies. Therefore, a theoretical minimum of the total harmonic losses was postulated but measurements up to $f_h = 20\,\text{kHz}$ could not prove the loss increase for very high frequencies and rather showed a further slight reduction or a nearly constant behavior with increasing frequency [72].

The harmonic current components are approximately independent of the load because they are mainly determined by the leakage reactance. Therefore, it was concluded that the harmonic losses are independent of the load [63, 64, 70]. Newer measurements presented in [72, 73] however show a dependency of the harmonic losses on the load for lower harmonic frequencies ($f_h \leq 2.5\,\text{kHz}$). In this frequency range, the harmonic ohmic loss components are still important. Therefore the harmonic losses increase with the load due to a slight reduction of the leakage inductance with load caused by local saturation effects leading to slightly higher harmonic currents and an increased temperature of the stator and rotor windings leading to increased resistances. For higher harmonic frequencies, the harmonic losses are nearly inde-

pendent of the load.

Measuring the harmonic losses turned out to be a rather complex task. Determining the harmonic losses by subtracting the output power from the input power (input-output measurement) is inherently sensitive to measurement errors especially if the measurement is done at rated power [64, 74]. Small power losses have to be determined out of measured large power values, heavily dependent on the exact operating point. The problems are less pronounced if no-load measurements are conducted assuming that the harmonic losses are independent of the load. As the harmonic losses are a large fraction of the measured power under no-load operation, the measurement accuracy is increased. Still, the harmonic losses are determined by subtracting the fundamental losses (either calculated or measured with a sinusoidal source) from the total losses. If the fundamental losses are determined from measurements with a sinusoidal source, difficulties arise in maintaining the same operating temperature and the same fundamental operating point compared to the operation with a PWM modulated waveform.

Accordingly, considerable effort was put in sophisticated measurement setups. Chalmers et al. built a special inverted induction machine to measure the harmonic losses [64]. Search coils have been used to measure flux densities and isolating the several loss components. Later approaches used power electronic based inverters to generate single harmonics and record a frequency dependent loss factor curve [72, 75–79]. Boglietti et al. finally conducted and published several measurements over the last 20 years with increasing effort and precision in order to determine and separate the harmonic loss components in induction machines [53, 73, 80–83].

At the end of the 90s the calculation of harmonic machine losses was extended with computer based FEM analysis. The complete machine geometry is modelled and the flux densitiy in every part of the machine is calculated. This process is extremely time-consuming if not only sinusoidal but also PWM modulated waveforms and the rotation of the rotor are considered. Finally, the losses in the machine can be calculated by summing up the loss components caused by flux variations and currents in the different machine parts. Papazacharopoulos et al. tried to determine the elements of the enhanced machine equivalent circuit with FEM analysis [84–86]. Boglietti et al. tried to prove their loss measurements and loss models by comparing with calculations based on the FEM analysis [51, 53, 73, 87]. Both groups had good results but the

computational burden is very high and the complete construction details of the machine have to be known in order to use the methods. The FEM analysis supported the theoretical findings about the harmonic machine losses. Iron losses become dominant above a certain frequency ($f_\mathrm{h} \geq 2.5\,\mathrm{kHz}$) and the losses in the stator and rotor end-regions are not negligible as the eddy-currents induced by axial field components are not reduced by the laminations. Therefore, even the end-regions have to be modeled using 3D FEM analysis to reach an accurate loss prediction [86]. The harmonic iron losses concentrate in the stator and rotor tooth tips [88] as they are caused mainly by leakage fluxes which do not penetrate deep into the core.

With the deeper understanding of the harmonic loss mechanisms the question arose, if there are modulation strategies which are superior to others concerning the induced additional losses in the induction machine. The early adopted six-step modulation showed a low performance concerning pulsating torques with six times the fundamental frequency, and increased harmonic ohmic losses, especially under full load. Therefore, harmonic elimination methods (with rather low pulse numbers) were developed later in order to eliminate low order harmonics and their corresponding pulsating torques. The spectral lines are moved to higher frequencies with the drawback of a considerable increase of the remaining harmonic voltage amplitudes. It was shown in [89–91] that the harmonic machine losses can be decreased considerably if the switching angles of the harmonic elimination method are optimized under the aspect of minimizing the harmonic machine losses and accepting some small low order harmonics.

With the increased switching frequencies, harmonic elimination techniques became less important, and the simple sinusoidal PWM methods gained attention. The various sinusoidal PWM methods eliminate all harmonics below the switching frequency but the remaining voltage harmonics have high amplitudes. It was shown that the loss reduction potential of the loss optimized harmonic elimination modulation method compared to a standard sinusoidal PWM method vanishes with increasing pulse number [89].

Modern semiconductor technology allowed to further increase the switching frequency of PWM variable speed drives. Although this allows an increased control performance and a reduction of acoustic noise emissions, the harmonic machine losses cannot be reduced considerably by increasing the switching frequency above $f_\mathrm{h} \approx 10\,\mathrm{kHz}$. The

harmonic iron losses become dominant and are finally determined by eddy-current losses only. In this frequency range, the harmonic machine losses are approximately independent of the switching frequency. The obtainable loss reduction is very small if the switching frequency is further increased and the total system losses will again increase because of higher inverter losses (cf. Chapter 5).

2.2.2 Theoretical background of harmonic machine losses

In this section, the optimization potential of a variable speed drive concerning the harmonic machine losses is investigated. The impacts of the converter topology, the switching frequency, and the modulation strategy are analyzed. As the main goal of the analysis is to compare different converter topologies and modulation methods and not to give a very accurate prediction of harmonic machine losses, simplifications are made if possible.

First, the underlying models and assumptions for the analysis are presented. It will be shown that the harmonic machine losses can be characterized with a loss factor curve depending on the harmonic frequency. If the spectrum of the converter output voltage is known, the total harmonic losses can be obtained by summation of the losses caused by the individual harmonics. Here, a source of error is introduced as the additivity of the loss components is not given for the hysteresis losses. Nevertheless, it will be shown that in the frequency range considered for this comparison the harmonic losses are dominated by eddy-current losses which are additive if saturation is neglected.

The considered switching frequencies are restricted to $f_{\mathrm{sw}} \geq 5\,\mathrm{kHz}$ in order to achieve a satisfactory control performance and to minimize torque pulsations. The power rating of the machine is limited to values comparable to the used test machine ($P_{\mathrm{n}} = 7.5\,\mathrm{kW}$). As no detailed construction data of the machine are available, a qualitative discussion on the harmonic loss components and their importance depending on the harmonic frequency is given and proved with measurements.

Ohmic losses

The harmonic machine losses are composed of ohmic losses in the stator and rotor as well as iron losses in the stator and in the rotor,

$$P_{\mathrm{h}} = P_{\mathrm{o,s}} + P_{\mathrm{o,r}} + P_{\mathrm{i,s}} + P_{\mathrm{i,r}}. \tag{2.45}$$

First, the ohmic losses are considered in more detail. As the rotor is rotating, the frequency of the fields and currents occurring in the rotor-fixed coordinate system is shifted with

$$f_{\mathrm{h,r}} = sl_{\mathrm{h}} \cdot f_{\mathrm{h,s}}. \tag{2.46}$$

The harmonic slip is given with

$$sl_{\mathrm{h}} = \frac{f_{\mathrm{h,s}} \mp p \cdot f_{\mathrm{R}}}{f_{h,s}}, \tag{2.47}$$

where the - sign is used for harmonics with positive sequence and the + sign for harmonics with negative sequence. The relative slip converges to unity ($sl_{\mathrm{h}} = 1$) for high harmonic frequencies. Therefore, the frequencies can be assumed to be equal in the stator and in the rotor ($f_{\mathrm{h,s}} = f_{\mathrm{h,r}} = f_{\mathrm{h}}$).

As the harmonic frequency increases, skin- and proximity effect influence the resistance of the conductors. The rotor in a squirrel cage machine is often made of die-cast aluminium or die-cast copper bars. The resistance of these single rotor bars is heavily affected by the skin-effect and increases accordingly with the frequency. If the rotor bars are assumed to be rectangular conductors (with width b and height h, whereas $h \ll b$), the variation of the resistance can be described (cf. [92]) with

$$R_{\mathrm{h,r}} = R_{\mathrm{dc,r}} \cdot \frac{\epsilon}{2} \frac{\sinh \epsilon + \sin \epsilon}{\cosh \epsilon - \cos \epsilon}. \tag{2.48}$$

Here, the factor $\epsilon = h/\delta$ describes the relation between the conductor height h and the skin-depth

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f_{\mathrm{h}}}}. \tag{2.49}$$

If the skin depth is small compared to the conductor height, what is the case for the considered switching frequencies, Eq. 2.48 can be ap-

proximated with

$$R_{\mathrm{h,r}} \approx R_{\mathrm{dc,r}} \cdot \frac{\epsilon}{2} = R_{\mathrm{dc,r}} \cdot k_{\mathrm{s,r}} \cdot \sqrt{f_{\mathrm{h}}} \tag{2.50}$$

$$k_{\mathrm{s,r}} = \frac{h\sqrt{\pi\mu_0\sigma}}{2}. \tag{2.51}$$

The stator is normally wound with copper wires using several insulated wires per strand in order to reduce the skin effect. The skin-effect of round conductors can be described with Bessel functions (cf. [92]) as

$$\begin{aligned} R_{\mathrm{h,s}} =& R_{\mathrm{dc,s}} \cdot \frac{\epsilon}{2\sqrt{2}} \left(\frac{\mathrm{ber}_0(\epsilon)\,\mathrm{bei}_1(\epsilon) - \mathrm{ber}_0(\epsilon)\,\mathrm{ber}_1(\epsilon)}{\mathrm{ber}_1(\epsilon)^2 + \mathrm{bei}_1(\epsilon)^2} \right. \\ & \left. - \frac{\mathrm{bei}_0(\epsilon)\,\mathrm{ber}_1(\epsilon) + \mathrm{bei}_0(\epsilon)\,\mathrm{bei}_1(\epsilon)}{\mathrm{ber}_1(\epsilon)^2 + \mathrm{bei}_1(\epsilon)^2} \right). \end{aligned} \tag{2.52}$$

The factor $\epsilon = d/(\delta\sqrt{2})$ describes the relation between the conductor diameter d and the skin-depth δ. The stator resistance initially shows a f_{h}^2 dependency if the skin-depth is in the same range as the conductor diameter and finally also converges to the $f_{\mathrm{h}}^{0.5}$ dependency known from the rotor bars when the skin-depth is small compared to the conductor diameter. If a conductor diameter of $d = 2.5\,\mathrm{mm}$ is assumed this condition is already fulfilled for $f_{\mathrm{h}} > 5\,\mathrm{kHz}$ and the stator resistance can accordingly be approximated with

$$R_{\mathrm{h,s}} \approx R_{\mathrm{dc,s}} \cdot \frac{\epsilon}{2\sqrt{2}} = R_{\mathrm{dc,s}} \cdot k_{\mathrm{s,s}} \cdot \sqrt{f_{\mathrm{h}}}, \tag{2.53}$$

$$k_{\mathrm{s,s}} = \frac{d\sqrt{\pi\mu_0\sigma}}{4}. \tag{2.54}$$

The harmonic losses can then be derived with the stator current harmonics which are mainly determined by the leakage reactance. They are given as

$$P_{\mathrm{h,o}} = 3 \cdot I_{\mathrm{h}}^2 \cdot (R_{\mathrm{h,s}} + R_{\mathrm{h,r}}) = 3 \cdot \left(\frac{V_{\mathrm{h}}}{2\pi f_{\mathrm{h}} \cdot L_\sigma} \right)^2 \cdot (R_{\mathrm{h,s}} + R_{\mathrm{h,r}}). \tag{2.55}$$

Although the stator and rotor resistance increases due to the skin-effect, the current harmonics decay with the harmonic frequency squared. If it is assumed that both stator and rotor resistance already show a $f_h^{0.5}$

dependency, the harmonic ohmic loss component decreases with the frequency according to

$$P_{\mathrm{h,o}} \approx 3 \cdot \left(\frac{V_{\mathrm{h}}}{2\pi f_{\mathrm{h}} \cdot L_{\sigma}} \right)^2 \cdot (R_{\mathrm{dc,s}} k_{\mathrm{s,s}} + R_{\mathrm{dc,r}} k_{s,r}) \cdot f_{\mathrm{h}}^{0.5} = k_{\mathrm{o}} \frac{V_{\mathrm{h}}^2}{f_{\mathrm{h}}^{1.5}}. \quad (2.56)$$

Additionally, the leakage inductance is reduced slightly with increased frequency due to the skin-effect. For a single round conductor the inductance would reduce inversely to $f_h^{0.5}$ (cf. [71]) and can be approximated for high frequencies with

$$L_{\mathrm{h},\sigma} \approx L_{\sigma,\mathrm{LF}} \cdot \frac{2\sqrt{2}}{\epsilon} = L_{\sigma,\mathrm{LF}} \cdot k_{\sigma} \cdot \frac{1}{\sqrt{f_{\mathrm{h}}}}, \quad (2.57)$$

$$k_{\sigma} = \frac{4}{d\sqrt{\pi \mu_0 \sigma}}. \quad (2.58)$$

As the total leakage inductance is influenced by many construction details of the machine, the reduction of the inductance is less pronounced than Eq. 2.57 would indicate. According to [71], the leakage inductance can be approximated up to $f_{\mathrm{h}} = 20\,\mathrm{kHz}$ with

$$L_{\mathrm{h},\sigma} \approx k_{\sigma} \cdot f_{\mathrm{h}}^{-0.16}. \quad (2.59)$$

If this behavior is inserted in Eq. 2.56, the ohmic harmonic losses vary with

$$P_{\mathrm{h,o}} \approx k_{\mathrm{o}}^{*} \frac{1}{f_{\mathrm{h}}^{1.2}} \cdot V_{\mathrm{h}}^2. \quad (2.60)$$

A description of the harmonic ohmic losses depending on the square of the applied harmonic voltage component is obtained. If saturation is neglected (assuming the saturation state of the machine is determined by the fundamental current) the total ohmic losses can be obtained by superposition, summing up the loss components created by the individual voltage harmonics in the frequency spectrum of the applied stator voltage.

Iron losses

The second source of harmonic losses are iron losses in the stator and rotor core. Hysteresis and eddy-current losses increase the harmonic losses considerably. The squirrel-cage induction machine behaves for

harmonic frequencies similar to a transformer with the secondary winding short-circuited. Therefore, the mutual flux is ideally zero and only leakage fluxes are persistent in the machine. These leakage fluxes generate losses especially in the stator and rotor teeth and in the slot bridges as the flux density in this regions is very high. Additionally, magnetic fields from the stator end windings can enter the stator and rotor cores in axial direction and produce considerable eddy-currents as the lamination cannot limit the eddy-currents.

The exact amount and the distribution of the iron losses between stator and rotor core is difficult to calculate without FEM analysis, therefore a qualitative description is given. The total harmonic iron losses occuring in the stator and rotor core can be separated into hysteresis losses and eddy-current losses. According to [51], the harmonic iron loss density can be approximated with

$$p_{\mathrm{h,i}} = p_{\mathrm{hys}} + p_{\mathrm{eddy}} = k_{\mathrm{hys}} \cdot f_{\mathrm{h}} B_{\mathrm{h}}^{\alpha} + k_{\mathrm{eddy}} \cdot f_{\mathrm{h}}^2 B_{\mathrm{h}}^2. \tag{2.61}$$

The leakage flux is directly impressed by the stator voltage. If an average area for the different leakage flux pathes is assumed, the flux density is related to the applied harmonic stator voltage with

$$B_{\mathrm{h}} = k_{\mathrm{B}} \cdot \frac{V_{\mathrm{h}}}{f_{\mathrm{h}}}. \tag{2.62}$$

Therefore, the frequency dependency of the harmonic iron losses can be approximated with

$$P_{\mathrm{h,i}} = k_{\mathrm{hys}}^{*} \cdot f_{\mathrm{h}}^{1-\alpha} V_{\mathrm{h}}^{\alpha} + k_{\mathrm{eddy}}^{*} \cdot V_{\mathrm{h}}^2. \tag{2.63}$$

As the hysteresis coefficient α is usually greater than 1, the hysteresis losses decay with increased harmonic frequency. In order to simplify the equation, [69] suggests to set $\alpha = 2$. This leads to the following, simplified loss model

$$P_{\mathrm{h,i}} = \left(k_{\mathrm{hys}}^{*} \frac{1}{f_{\mathrm{h}}} + k_{\mathrm{eddy}}^{*} \right) \cdot V_{\mathrm{h}}^2. \tag{2.64}$$

Similarly to the ohmic losses, a description of the harmonic iron losses depending on the square of the applied harmonic voltage component is obtained. As already mentioned, the superposition of the iron loss components caused by several voltage harmonics is not strictly valid. Nevertheless, the error is usually small if the influence of a

large fundamental frequency flux component and a small superimposed switching frequency flux component is considered [76]. The eddy-current loss components are additive if saturation of the core material is neglected.

Total harmonic machine losses

Finally, the harmonic ohmic and iron losses can be combined. The total harmonic losses depending on the frequency and the square of the applied voltage component can be described with

$$P_{\mathrm{h}} = P_{\mathrm{h,o}} + P_{\mathrm{h,i}} = \left(k_{\mathrm{o}}^{*} \frac{1}{f_{\mathrm{h}}^{1.2}} + k_{\mathrm{hys}}^{*} \frac{1}{f_{\mathrm{h}}} + k_{\mathrm{eddy}}^{*} \right) \cdot V_{\mathrm{h}}^{2}. \tag{2.65}$$

This basic relationship led to the introduction of the experimental loss-factor curve [70, 75, 76]. It is assumed that the harmonic losses in a machine can be determined for an arbitrary shape of the applied stator voltage if the experimentally determined loss-factor curve and the frequency spectrum of the applied stator voltage are known. The principle was applied e.g. in [93] to determine the harmonic losses of a machine supplied by a matrix converter.

The loss-factor curve is defined as

$$LF\left(f_{\mathrm{h}}\right) = \frac{P_{\mathrm{h}}}{V_{\mathrm{h}}^{2}}, \tag{2.66}$$

and the total harmonic losses are obtained by summing up the harmonic losses caused by the individual voltage components according to

$$P_{\mathrm{h,tot}} = \sum_{h} LF\left(f_{\mathrm{h}}\right) \cdot V_{\mathrm{h}}^{2}. \tag{2.67}$$

The experimental loss factor links the harmonic machine losses with the spectrum of the applied stator voltage which allows the analysis of the impact of different topologies and modulation strategies. Although it is machine specific, some general conclusions can be made if the frequency dependency of the loss components are considered. According to [94], the experimental harmonic loss factor curve can be fitted with an expression containing two terms describing the low-frequency losses and the high-frequency losses as

$$LF\left(f_{\mathrm{h}}\right) = \frac{k_{\mathrm{a}}}{f_{\mathrm{h}}^{\alpha}} + \frac{k_{\mathrm{b}}}{f_{\mathrm{h}}^{\beta}}. \tag{2.68}$$

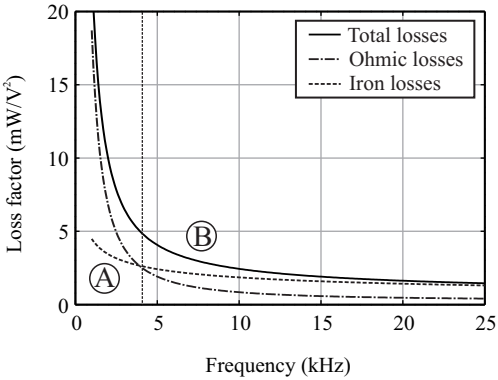

Figure 2.29: Experimental loss factor curve and its decomposition into conductor and core losses.

The factors α, β, k_a and k_b can be determined with a least-squares fit to the experimentally determined loss-factor curve. The first part containing $1/f^\alpha$, with $\alpha = 1.2...1.5$, describes the loss components decaying with the frequency such as the ohmic conductor losses. The second part containing $1/f^\beta$, with $\beta = 0.2...0.5$, represents the persisting high-frequency loss components dominated by eddy-current iron losses.

Fig. 2.29 shows an example loss-factor curve with the decomposition into conductor losses and core losses. The frequency range can be divided into a low-frequency range A and a high-frequency range B at the frequency where the conductor losses and the core losses are equal. The dominant loss mechanisms are different in these two frequency ranges with implications on the optimization of PWM methods and the determination of an ideal switching frequency.

In the low-frequency range A, the ohmic conductor losses dominate. The losses can be reduced considerably if a higher switching frequency is chosen, because the loss factor curve decays sharply. This also implies that the amplitudes of voltage harmonics at a lower frequency should be small whereas at high frequencies the amplitudes are allowed to be larger. The exact distribution of the voltage harmonics in the frequency spectrum matters. Therefore, loss optimized harmonic elimination methods can decrease the harmonic losses considerably. Applied to modern PWM methods, third harmonic injection and equivalently,

the placement and distribution of the zero states in SVM influences the harmonic machine losses in this frequency range, as the distribution of the voltage harmonics changes.

Interestingly, minimization of the harmonic machine losses in the frequency range A is very close to minimization of the RMS value of the phase current. The two approaches are identical if the increase of the conductor resistance due to the skin-effect is neglected. Therefore loss-factors based on the RMS current have been used in the literature in order to minimize the machine losses [90,91,95–97]. If iron losses and skin effect are neglected, the harmonic machine losses are given with

$$P_{\mathrm{h,tot}} = 3 \cdot (R_{\mathrm{s}} + R_{\mathrm{r}}) \cdot \sum_{h>1} \left(\frac{V_{\mathrm{h}}}{2\pi f_{\mathrm{h}} \cdot L_{\sigma}} \right)^2 = 3 \cdot (R_{\mathrm{s}} + R_{\mathrm{r}}) \cdot \sum_{h>1} I_{\mathrm{h}}^2. \quad (2.69)$$

The harmonic machine losses are then minimal if the total current loss factor

$$LFI = \sum_{h>1} I_{\mathrm{h}}^2 \quad (2.70)$$

is minimized, which is equivalent to minimizing the RMS current value. It was also shown that using a more sophisticated loss model for optimizing a harmonic elimination PWM method gives nearly the same results as minimizing the RMS current value [89–91]. This is not further surprising as the conductor losses are the dominant loss mechanism in frequency range A.

In the high-frequency range B, the iron losses dominate. The situation is different as the loss factor-curve decays very slowly and could be approximated to be constant for higher switching frequencies when the eddy-current losses dominate. Therefore, increasing the switching frequency would not reduce the harmonic machine losses considerably. The exact distribution of the voltage harmonics in the frequency spectrum is not important as all harmonics would be multiplied with a constant factor. Several papers show that different PWM methods and changing the switching frequency only has a marginal effect on the harmonic machine losses [53,82,98] in frequency range B.

If it is assumed that the harmonic machine losses in frequency range B are dominated by eddy-current losses, the total harmonic machine losses are given with

$$P_{\mathrm{h,tot}} = k_{\mathrm{eddy}}^{*} \cdot \sum_{h>1} V_{\mathrm{h}}^2. \quad (2.71)$$

The harmonic losses are then minimal if the voltage loss factor

$$LFV = \sum_{h>1} V_{\mathrm{h}}^2 \tag{2.72}$$

is minimized, what is equivalent to minimizing the RMS value of the phase voltage. It can be shown that the RMS voltage is not influenced by third-harmonic injection or placement of the zero states as long as the nearest three space vectors are chosen for the modulation [99]. As third-harmonic injection and the placement of zero states only affect the common-mode voltage, there are no currents flowing and therefore, no associated loss components can occur (assuming a disconnected star-point).

A further interesting observation from the loss factor curve is the dependency on the load (cf. [72]). The harmonic machine losses are influenced by the load mainly in the low-frequency range A, where the ohmic loss mechanism dominates. This is due to the decrease of the leakage inductance due to local saturation effects and therefore an increase in harmonic currents. Contrary, in the high-frequency range B, where iron losses dominate, the harmonic losses are not influenced by the load.

2.2.3 Analysis of the harmonic machine losses caused by 2-level and 3-level inverters

In order to compare the efficiency of low-voltage variable speed drives in a holistic way, not only the converter efficiency has to be considered. The harmonic machine losses have the same order of magnitude as the converter losses if a modern low-voltage drive system is considered. Based on the theoretical findings presented in the previous sections, the harmonic machine losses caused by a 2-level and a 3-level inverter are evaluated and compared to each others. Measurement made on a standard 7.5 kW induction machine are used to confirm the calculations.

Machine dependent loss-factor curve

First, the loss-factor curve is reconstructed from harmonic machine loss measurements conducted under quasi no-load condition on a standard induction machine. Usually, the loss-factor curve is recorded using harmonic injection methods [72]. The measurements that are presented

here were conducted in a different way. The machine was supplied with a prototype of the T-type inverter (cf. Chapter 6) which is able to generate a 2-level or a 3-level voltage waveform with an adjustable switching frequency. The total harmonic machine losses using a fixed switching frequency are recorded. Knowing the voltage spectrum of the stator voltage, the loss factor curve can be reconstructed.

The harmonic losses were measured with the high precision power analyzer Yokogawa WT3000 by directly subtracting the fundamental input power from the total measured input power according to

$$P_{\mathrm{h,tot}} = P_{\mathrm{in}} - P_{\mathrm{in},(1)}. \tag{2.73}$$

The harmonic power $P_{\mathrm{h,tot}}$ is completely due to harmonic losses. Although harmonics can generate steady-state torques, these are negligibly small at the high switching frequencies considered here ($f_{\mathrm{sw}} \geq 4\,\mathrm{kHz}$). The steady-state torques generated by the harmonics can be calculated with

$$T_{\mathrm{h}} = \frac{1}{\omega_{\mathrm{R}}} \cdot 3 \cdot I_{\mathrm{r,h}}^2 R_{\mathrm{r}} \frac{1 - s l_{\mathrm{h}}}{s l_{\mathrm{h}}} \tag{2.74}$$

$$\approx \frac{1}{\omega_{\mathrm{R}}} \cdot 3 \cdot \left(\frac{V_{\mathrm{h}}}{2\pi f_{\mathrm{h}} \cdot L_{\sigma}} \right)^2 R_{\mathrm{r}} \frac{1 - s l_{\mathrm{h}}}{s l_{\mathrm{h}}}. \tag{2.75}$$

For a switching frequency of 4 kHz with a 2-level inverter, the harmonic voltage at the first switching frequency harmonic has an effective value of 67 V. With the machine parameters given in Table 2.1, this would result in a steady-state torque of only 9.8 μNm and a corresponding mechanical power of 3.1 mW. Furthermore, the voltage harmonics occur in pairs around the switching frequency. For the implemented space vector modulation, the pairs occur at $f_{\mathrm{h}} = f_{\mathrm{sw}} \pm f_{\mathrm{e}}$. The harmonic voltage with frequency $f_{\mathrm{sw}} + f_{\mathrm{e}}$ has a positive sequence, therefore a field rotating in positive direction with a corresponding positive torque is generated. Contrary, the harmonic voltage with frequency $f_{\mathrm{sw}} - f_{\mathrm{e}}$ generates a field rotating in negative direction with a corresponding negative torque. For high pulse numbers, the two voltage peaks of these pairs are nearly identical in value. Therefore, the generated steady-state torques are compensated. It follows that the generation of mechanical output power due to harmonics can be completely neglected and the harmonic input power is completely due to machine losses.

Only interactions of harmonic main flux components with harmonic rotor currents of the same order produce a constant torque component,

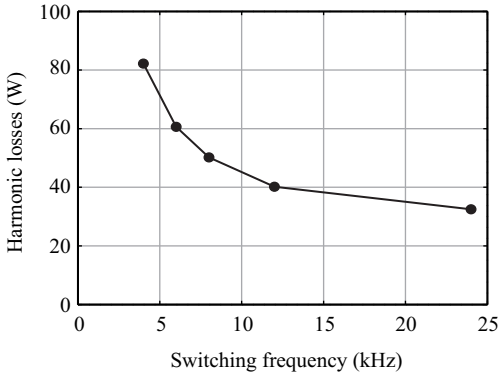

Figure 2.30: Measured harmonic machine losses with 2-level inverter and optimal clamping space vector modulation for several switching frequencies.

all other interactions between fields and currents of different orders produce pulsating torques with zero mean value.

The measured harmonic losses are depicted in Fig. 2.30. There are 5 measurements at different switching frequencies. Therefore, 5 points of the loss factor curve can be reconstructed. Considering the multiples of the applied switching frequencies, the equation system can be solved if it is assumed that the loss factor curve is constant for harmonics with frequencies $f_\mathrm{h} \geq 16\,\mathrm{kHz}$. The harmonics of the applied voltage waveform can be determined with a FFT algorithm. Although there are analytical equations describing the amplitude of the main switching frequency voltage harmonics for sinusoidal PWM (cf. [100]), these are not valid for the implemented space vector modulation. Therefore, the FFT algorithm is used to determine the voltage spectrum.

The voltage spectrum of the 2-level inverter with a switching frequency of $f_\mathrm{sw} = 6\,\mathrm{kHz}$, a fundamental output voltage of $V_\mathrm{n} = 230\,\mathrm{V}$, and a DC-link voltage of $V_\mathrm{dc} = 650\,\mathrm{V}$ is shown in Fig. 2.31. Only the differential mode (DM) voltage spectrum has to be considered as the common mode (CM) voltage does not produce any losses if the star-point is not connected. The voltage harmonics are grouped around integer multiples k of the switching frequency. For each group k, it is assumed that all voltage components belonging to this group occur at the same frequency $f_\mathrm{k} = k \cdot f_\mathrm{sw}$. All voltage components of a group are

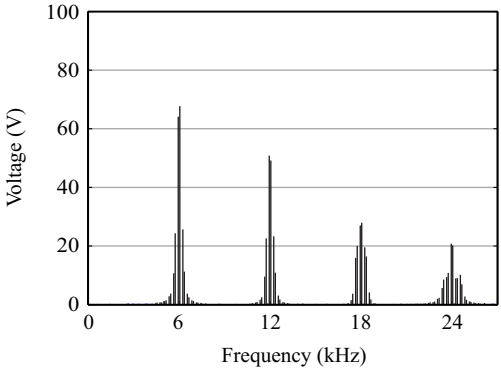

Figure 2.31: DM voltage spectrum of the 2-level inverter using SVM and a switching frequency of $f_{\mathrm{sw}} = 6\,\mathrm{kHz}$.

squared and summed up in order to get the multiplication factors h_k. The amplitudes of the voltage components in the frequency spectrum are approximately independent of the switching frequency for the high pulse numbers considered here. Therefore, the multiplication factors h_k are the same for each switching frequency but belong to different harmonic frequencies. The linear equation system given in Eq. 2.76 can be used to solve for the 5 points $(c_{4\mathrm{kHz}} - c_{24\mathrm{kHz}})$ of the loss-factor curve,

$$\begin{pmatrix} P_{4\mathrm{kHz}} \\ P_{6\mathrm{kHz}} \\ P_{8\mathrm{kHz}} \\ P_{12\mathrm{kHz}} \\ P_{24\mathrm{kHz}} \end{pmatrix} = \begin{pmatrix} h_1 & 0 & h_2 & h_3 & h_4{+}... \\ 0 & h_1 & 0 & h_2 & h_3{+}h_4{+}... \\ 0 & 0 & h_1 & 0 & h_2 + h_3{+}h_4{+}... \\ 0 & 0 & 0 & h_1 & h_2 + h_3 + h_4{+}... \\ 0 & 0 & 0 & 0 & h_1{+}h_2{+}h_3{+}h_4{+}... \end{pmatrix} \cdot \begin{pmatrix} c_{4\mathrm{kHz}} \\ c_{6\mathrm{kHz}} \\ c_{8\mathrm{kHz}} \\ c_{12\mathrm{kHz}} \\ c_{24\mathrm{kHz}} \end{pmatrix}. \tag{2.76}$$

The resulting loss-factor curve is depicted in Fig. 2.32. A least-squares fit is used to determine the parameters of Eq. 2.68 which can be given for the measured induction machine with $k_{\mathrm{a}} = 0.019, \alpha = 1.5, k_{\mathrm{b}} = 0.0045$, and $\beta = 0.35$.

Using the loss factor curve, the impact of different modulation schemes and different topologies can be evaluated easily. The spectrum of the applied phase voltage can be determined using a FFT algorithm from calculated or simulated voltage waveforms.

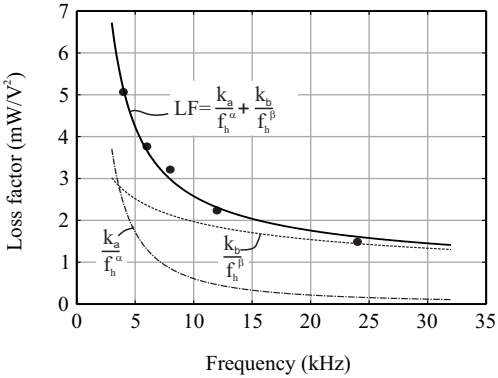

Figure 2.32: Determined loss factor curve for the induction machine under analysis.

Harmonic machine losses of 2-level and 3-level inverter depending on the modulation index

In the following, the harmonic machine losses generated with a 3-level inverter are calculated using the loss factor curve. A comparison with the measured harmonic losses induced by the 3-level inverter at a certain switching frequency proves the applicability of the loss-factor method. Afterwards, the impact of the modulation index on the harmonic losses of 2-level and 3-level inverters is analyzed. A simple approximation based on the assumption of dominant eddy-current losses is given. This allows to compare the additional harmonic losses induced in the load machine depending on the working point and the converter topology.

Similarly to the 2-level inverter, several modulation schemes exist for the 3-level inverter. Due to the redundant switching states, there are even more possibilities how the fundamental voltage can be generated. Among sinusoidal PWM with or without third harmonic injection, also SVM is an often used strategy. A SVM modulation strategy with switching loss optimal phase clamping (cf. [101]) is used here. In order to calculate the harmonic machine losses, the voltage spectrum of the 3-level waveform is necessary. It can be determined with a FFT algorithm and is shown in Fig. 2.33 for a fundamental output voltage of $V_{\mathrm{n}} = 230\,\mathrm{V}$ and a DC-link voltage of $V_{\mathrm{dc}} = 650\,\mathrm{V}$. The voltage harmonics are considerably reduced compared to the 2-level voltage spectrum as only steps with half of the DC-link voltage $V_{\mathrm{dc}}/2$ are applied to the

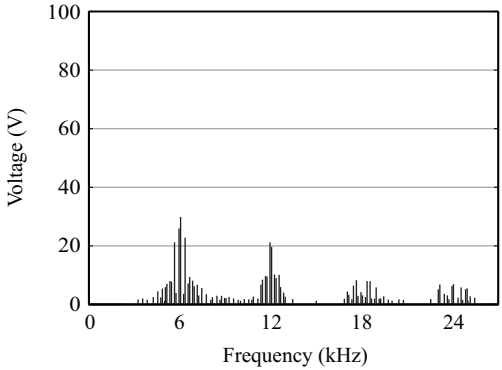

Figure 2.33: DM voltage spectrum of the 3-level inverter using SVM and a switching frequency of $f_{\mathrm{sw}} = 6\,\mathrm{kHz}$.

machine during the modulation process.

Using the previously determined loss-factor curve of the machine, the harmonic machine losses occurring for the 3-level inverter can be calculated with its voltage spectrum. A comparison between the calculated losses and the measured losses is given in Fig. 2.34. As can be seen, there is a very good agreement between calculated and measured losses. Although the calculation of the harmonic machine losses using the loss-factor curve is based on several simplifications, such as the additivity of the harmonic loss components, the results justify its application.

The harmonic machine losses obtained with the 2-level inverter are also plotted in Fig. 2.34. A significant loss reduction can be achieved with the 3-level inverter. The harmonic machine losses are reduced approximately by a factor of 4 compared to the 2-level waveform with the same switching frequency. Among the increased system efficiency and the corresponding achievable energy savings, reducing the harmonic machine losses has a further positive impact. The additional heating of the machine is reduced and therefore, the lifetime of the insulation is increased [66]. Ideally, no derating of the machine is necessary if it is operated with a 3-level inverter.

The induction machine is usually controlled with a constant rotor flux (corresponding to constant v/f control). Accordingly, the fundamental stator voltage is proportionally increased with the speed of the

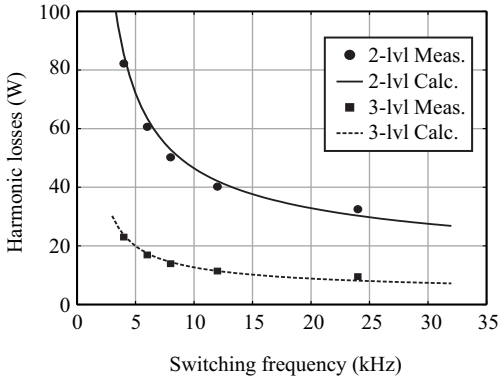

Figure 2.34: Measured and calculated harmonic machine losses of the 2-level and the 3-level inverter for different switching frequencies.

machine. The fundamental stator voltage is directly controlled with the modulation index. As the voltage spectrum is depending on the modulation index, also the harmonic machine losses change with the applied fundamental voltage.

Additionally, the loss-optimal machine control schemes presented in Section 2.1 usually reduce the stator voltage in order to increase the machine efficiency during part-load operation. In order to estimate the system efficiency under all these different operating conditions, it is important to determine the relationship between harmonic machine losses and the modulation index.

Basically, the approach is the same as before. The voltage spectrum is determined with the FFT method for different modulation indices. Together with the loss-factor curve, the expected harmonic machine losses can be calculated. Calculated and measured machine losses for the 2-level and the 3-level inverter at $f_{\mathrm{sw}} = 8\,\mathrm{kHz}$ are depicted in Fig. 2.35. The characteristic dependency of the harmonic machine losses on the modulation index is quite different for the 2-level and the 3-level inverter. Whereas there is a maximum at about m=0.6 for the 2-level inverter, there are two local maxima at m=0.3 and m=0.8 and a local minimum at m=0.55 for the 3-level inverter. Again, the agreement of calculated and measured losses is very good, especially with the 3-level inverter. For the 2-level inverter, the calculated losses are to high, but the relative error is always below 10%.

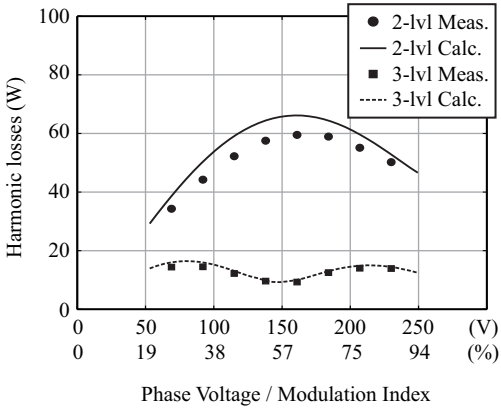

Figure 2.35: Measured and calculated harmonic machine losses, using the loss-factor curve, of the 2-level and the 3-level inverter for a variable modulation index and its corresponding fundamental phase voltage ($f_{\mathrm{sw}} = 8\,\mathrm{kHz}$).

Due to these different characteristics, the loss-optimal machine control schemes presented in Section 2.1 have different side-effects concerning the harmonic machine losses. Reducing the stator voltage below the rated value for low-torque operation increases the harmonic losses slightly for the 2-level inverter. This can counteract the achievable efficiency increase of the loss-optimal scheme. An opposite effect can be observed for the 3-level inverter, as the harmonic losses would decrease with a reduced stator fundamental voltage.

Approximation of harmonic machine losses for high switching frequency based on the inverter ripple voltage

According to [99], an analytical approximation for the dependency of the harmonic machine losses on the modulation index can be given. Based on the assumption of dominant eddy-current iron losses, the loss-factor curve can be assumed to be constant for higher switching frequencies. As already mentioned, the harmonic losses are then given as

$$P_{\mathrm{h,tot}} = k^{*}_{\mathrm{eddy}} \cdot \sum_{h>1} V_{\mathrm{h}}^{2}. \tag{2.77}$$

The sum of the squared voltage harmonics is related to the RMS

voltage squared as

$$V_{\mathrm{rms}}^2 = V_{(1)}^2 + \sum_{h>1} V_{\mathrm{h}}^2 = V_{(1)}^2 + \Delta V_{\mathrm{rms}}^2. \tag{2.78}$$

For the calculation of the harmonic losses, the fundamental voltage component is removed. The sum of the remaining squared harmonics $h > 1$ can be calculated considering only the ripple voltage Δv around its local mean value. Accordingly, the harmonic losses are dependent on the ripple voltage RMS value ΔV_{rms} as

$$P_{\mathrm{h,tot}} = k_{\mathrm{eddy}}^* \cdot \Delta V_{\mathrm{rms}}^2. \tag{2.79}$$

Because only the differential mode voltage is responsible for the harmonic machine losses, the calculation can be unified by considering the line-to-line voltage instead of the phase voltage. There, third harmonic injection has no influence as it is not visible in the line-to-line voltage. The maximum line-to-line fundamental peak voltage $\hat{V}_{\mathrm{ll,(1),max}}$ which can be generated with continuous switching (the line-to-line voltage is always continuously switched, even if discontinuous PWM schemes or equivalent SVM with phase clamping are applied) is always given with $\hat{V}_{\mathrm{ll,(1),max}} = V_{\mathrm{dc}}$. Therefore, it is useful to generally define the modulation index concerning the line-to-line voltage as

$$m = \frac{\hat{V}_{\mathrm{ll,(1)}}}{V_{\mathrm{dc}}}. \tag{2.80}$$

The modulation index is then limited to $0 \leq m \leq 1$ and is equal to the modulation index used in SVM. Correspondingly, the maximum fundamental phase voltage is

$$\hat{V}_{\mathrm{(1),max}} = \hat{V}_{\mathrm{ll,(1),max}}/\sqrt{3} = V_{\mathrm{dc}}/\sqrt{3}. \tag{2.81}$$

In the symmetric case, the differential mode phase voltage spectrum is obtained from the line-to-line voltage spectrum by dividing each voltage component by $\sqrt{3}$. Although the exact distribution of the voltage spectrum is dependent on the used modulation scheme, the RMS voltage value of the line-to-line voltage is independent of the modulation scheme, as long as the nearest three space vectors are used in a modulation cycle [99]. This condition is satisfied also for modern regular sampling, unipolar PWM methods.

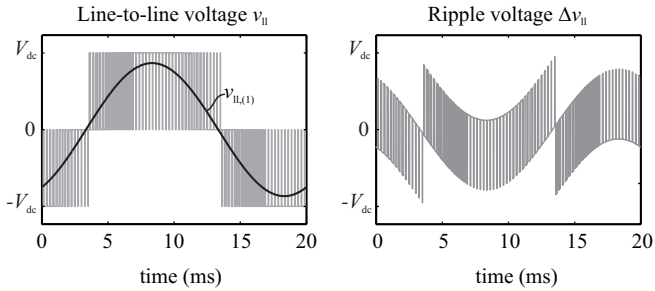

Figure 2.36: Line-to-line voltage of the 2-level inverter split into its fundamental component and the ripple voltage component.

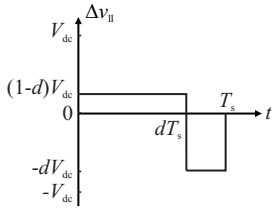

Figure 2.37: Detailed view on the local ripple voltage.

The line-to-line voltage can be splitted into its fundamental value and the ripple voltage as

$$v_{\mathrm{ll}} = v_{\mathrm{ll},(1)} + \Delta v_{\mathrm{ll}}. \tag{2.82}$$

Fig. 2.36 shows the corresponding waveforms over a fundamental period for the 2-level inverter. The local mean value over one switching period is given by

$$\bar{v}_{\mathrm{ll}} = v_{\mathrm{ll},(1)} = d \cdot V_{\mathrm{dc}}, \tag{2.83}$$

where d is the local duty-cycle. It is assumed to be constant over a switching period. The ripple voltage value during one switching period for the 2-level inverter is shown in Fig. 2.37. Depending on the modulation scheme, the pulse shape can look different than shown in Fig. 2.37, (e.g. having multiple transitions between the voltage levels during one switching period), but the mean value over a switching period has to stay the same and is equal to zero. The local mean value of the squared ripple voltage is therefore independent of the modulation scheme and

is given as

$$\begin{aligned}\overline{\Delta v_{\mathrm{ll,2lvl}}^2} &= \frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} \Delta v_\mathrm{ll}^2 dt = d(1-d)^2 V_\mathrm{dc}^2 + (1-d) d^2 V_\mathrm{dc}^2 \\ &= d(1-d) V_\mathrm{dc}^2.\end{aligned} \tag{2.84}$$

Now, the duty-cycle is varied with time to form the fundamental line-to-line voltage $v_{\mathrm{ll},(1)}$ and is replaced with

$$d(t) = m \cdot \sin(\omega t). \tag{2.85}$$

The global mean value of the squared ripple voltage is obtained by averaging the local mean value over a fundamental period. Due to the symmetry of the waveform it is sufficient to consider half of the fundamental period,

$$\begin{aligned}\Delta V_{\mathrm{ll,2lvl,rms}}^2 &= \frac{1}{T_\mathrm{n}/2} \int_0^{T_\mathrm{n}/2} \overline{\Delta v_{\mathrm{ll,2lvl}}^2}(t) dt \\ &= V_\mathrm{dc}^2 \left(\frac{2}{\pi} m - \frac{1}{2} m^2 \right).\end{aligned} \tag{2.86}$$

The ripple phase voltage squared is related to the ripple line-to-line voltage squared with

$$\Delta V_\mathrm{rms}^2 = \frac{1}{3} \cdot \Delta V_\mathrm{ll,rms}^2. \tag{2.87}$$

Finally, the harmonic machine losses obtained with the 2-level inverter under assumption of dominant eddy-current losses can be given with

$$\begin{aligned}P_{\mathrm{h,tot,2lvl}} &= k_\mathrm{eddy}^* \cdot \sum_{h>1} V_\mathrm{h}^2 = k_\mathrm{eddy}^* \cdot \frac{1}{3} \cdot \Delta V_{\mathrm{ll,2lvl,rms}}^2 \\ &= k_\mathrm{eddy}^* \cdot \frac{1}{3} V_\mathrm{dc}^2 \left(\frac{2}{\pi} m - \frac{1}{2} m^2 \right).\end{aligned} \tag{2.88}$$

The same procedure can be conducted for the 3-level inverter. There, the line-to-line voltage shows five voltage levels as depicted in Fig. 2.38. The ripple of the voltage around its local mean value during one switching period for the 3-level inverter is shown in Fig. 2.39. Again, the duty-cycle is assumed to be constant over a switching period. The local mean value of the squared ripple voltage is then given as

$$\overline{\Delta v_{\mathrm{ll,3lvl}}^2} = \begin{cases} d(\frac{1}{2} - d) V_\mathrm{dc}^2 & 0 \leq d < \frac{1}{2} \\ (d - \frac{1}{2})(1-d) V_\mathrm{dc}^2 & \frac{1}{2} \leq d < 1 \end{cases}. \tag{2.89}$$

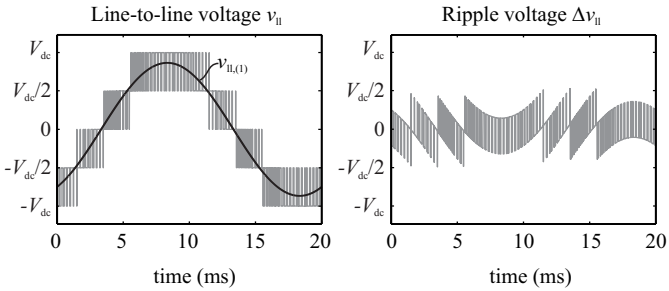

Figure 2.38: Line-to-line voltage of the 3-level inverter split into its fundamental component and the ripple voltage component.

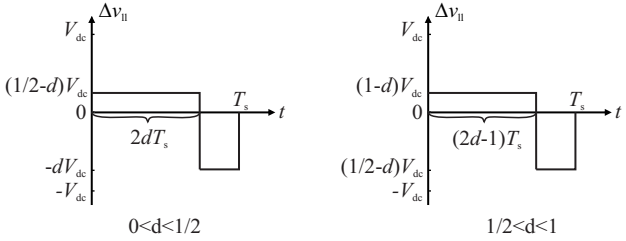

Figure 2.39: Detailed view on the local ripple voltage of the 3-level inverter.

Now, the duty-cycle d in Eq. 2.89 is replaced with the definition given in Eq. 2.85. The global mean value of the squared ripple voltage is obtained by averaging the local mean value over a half of the fundamental period. The result (cf. Eq. 2.90) contains two cases. If the modulation index m is less than 0.5, only the innermost hexagon in the space vector diagram is used for the modulation, which is equivalent to switching the line-to-line voltage only between $\{0, V_{\mathrm{dc}}/2\}$. If the modulation index m is greater than 0.5, also the outer space vectors are used,

$$\Delta V^2_{\mathrm{ll,rms,3lvl}} = \begin{cases} V^2_{\mathrm{dc}} \left(\frac{1}{\pi} m - \frac{1}{2} m^2\right) & 0 \le m < \frac{1}{2} \\ V^2_{\mathrm{dc}} \left(\frac{m}{\pi} - \frac{m^2}{2} - \frac{1}{2} + \frac{1}{\pi} \arcsin(\frac{1}{2m}) + \frac{2}{\pi} \sqrt{m^2 - \frac{1}{4}}\right) & \frac{1}{2} \le m < 1 \end{cases} . \tag{2.90}$$

Finally, the harmonic machine losses for the 3-level inverter can be

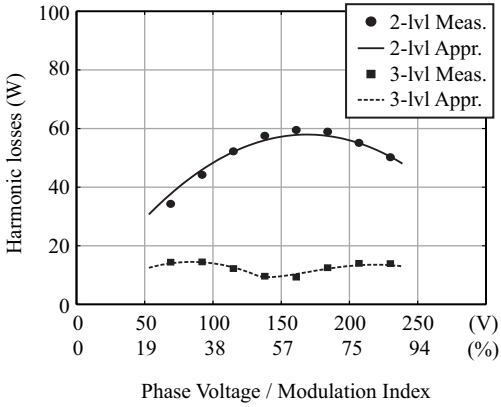

Figure 2.40: Comparison between measured and calculated harmonic machine losses using the ripple voltage based approximation ($f_{\mathrm{sw}} = 8\,\mathrm{kHz}$).

calculated with

$$P_{\mathrm{h,tot,3lvl}} = k^*_{\mathrm{eddy}} \cdot \frac{1}{3} \cdot \Delta V^2_{\mathrm{ll,3lvl,rms}}. \tag{2.91}$$

A comparison between the measured harmonic machine losses and the calculated ones using the approximations given in Eq. 2.88 and Eq. 2.91 is shown in Fig. 2.40. The constant $k^*_{\mathrm{eddy}} = 2.03\,\mathrm{mW/V^2}$ was adjusted to achieve the same losses as measured for the 2-level inverter at the nominal voltage of $V_{\mathrm{n}} = 230\,\mathrm{V}$. As can be seen, the approximations fit the measured data very well for 2-level and 3-level modulation. Naturally, there are some deviations from the measurement as the assumption of having only eddy-current losses is not completely fulfilled at a switching frequency of $f_{\mathrm{sw}} = 8\,\mathrm{kHz}$.

The ratio of the expected harmonic machine losses with a 3-level and a 2-level inverter supply is given with

$$\frac{P_{\mathrm{h,tot,3lvl}}}{P_{\mathrm{h,tot,2lvl}}} = \frac{\Delta V^2_{\mathrm{ll,3lvl,rms}}}{\Delta V^2_{\mathrm{ll,2lvl,rms}}}, \tag{2.92}$$

and is plotted in Fig. 2.41 over the modulation index. It is independent of the dc-link voltage V_{dc}, the eddy-current loss constant k^*_{eddy}, and the switching frequency f_{sw} as long as the frequency range with dominant

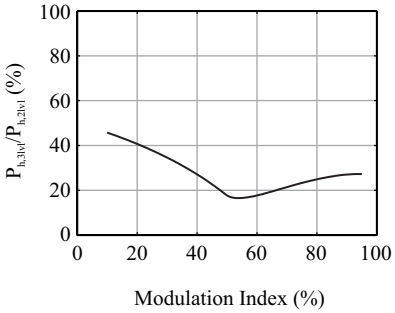

Figure 2.41: Ratio of harmonic machine losses for 2-level and 3-level inverter supply.

eddy-current losses is considered. The ratio reaches a minimum of 16.5% at $m = 0.55$ and it is approximately equal to 25% at $m = 0.8$, what is a modulation index typical for nominal output voltage operation.

Due to the good results achieved with this simple voltage ripple based approach it is suggested to determine the equivalent eddy-current loss constant k^*_{eddy} with measurement data of the harmonic machine losses obtained using a 2-level inverter at nominal voltage, and use the approximations given in Eq. 2.88 and Eq. 2.91 to estimate the expected harmonic machine losses for different modulation indices, different dc-link voltages and different topologies. The presented approach can be extended to inverters with more than three voltage levels. A generic solution for a N-level inverter is presented in [99].

For completeness, also the model describing the iron losses of induction machines fed with a PWM inverter proposed by Boglietti et al. in [51, 83, 102] is considered here. According to the authors, the total iron losses under non-sinusoidal voltage supply can be described with

$$P_{\text{i}} = \eta^2 \cdot P_{\text{hys,sin}} + \chi^2 \cdot P_{\text{eddy,sin}}. \tag{2.93}$$

Here, the expression $P_{\text{hys,sin}}$ describes the hysteresis losses under sinusoidal supply conditions and $P_{\text{eddy,sin}}$ are the eddy-current losses under

sinusoidal supply. The two remaining parameters are given as

$$\eta = \frac{|v|_{\text{avg}}}{|v_{(1)}|_{\text{avg}}} \approx 1 \tag{2.94}$$

$$\chi = \frac{V_{\text{rms}}}{V_{(1)}}. \tag{2.95}$$

They describe the ratio of the average rectified stator voltage to the average fundamental rectified stator voltage (η) and the ratio of the RMS voltage to the fundamental RMS voltage (χ). The factor η is approximately equal to one for high pulse numbers. Therefore, the hysteresis losses are not much influenced by the PWM switching and are basically equal to the sinusoidal case. The additional, harmonic iron losses are caused by additional eddy-current losses according to

$$\begin{aligned} P_{\text{h,tot,i}} &= P_{\text{i}} - P_{\text{hys,sin}} - P_{\text{eddy,sin}} \\ &= (\chi^2 - 1) \cdot P_{\text{eddy,sin}}. \end{aligned} \tag{2.96}$$

If the simple Steinmetz equation is used for the sinusoidal loss term it can be written as

$$P_{\text{eddy,sin}} = k^*_{\text{eddy}} \cdot V^2_{(1)}. \tag{2.97}$$

The factor χ^2 in terms of fundamental and ripple voltage RMS quantities is given as

$$\chi^2 = \frac{V^2_{\text{rms}}}{V^2_{(1)}} = \frac{V^2_{(1)} + \Delta V^2_{\text{rms}}}{V^2_{(1)}} = 1 + \frac{\Delta V^2_{\text{rms}}}{V^2_{(1)}}. \tag{2.98}$$

Inserting Eq. 2.98 and Eq. 2.97 into Eq. 2.96, one obtains

$$P_{\text{h,tot,i}} = \frac{\Delta V^2_{\text{rms}}}{V^2_{(1)}} \cdot P_{\text{eddy,sin}} = \Delta V^2_{\text{rms}} \cdot k^*_{\text{eddy}}, \tag{2.99}$$

which is the same result as obtained with the ripple voltage approximation for the harmonic machine losses (cf. Eq. 2.79) presented previously. This simplification assumes that the eddy-current loss constant does not change with frequency.

Chapter 3

Converter Topologies

The power electronic converter is the central energy control unit in a industrial variable speed drive (VSD) system. It has two main functions. First, it serves as an interface to the grid and possibly provides important functions such as power factor correction and sinusoidal input current shaping. Second, the motor has to be fed with a three-phase voltage of adjustable frequency and amplitude.

Although the main tasks of such a converter are well defined, there are many different converter topologies which could possibly be used to form a VSD system. All of them have specific strengths and weaknesses concerning functionality, efficiency, complexity, implementation effort and costs. Consequently, not all of them have the right characteristics for a low-voltage VSD system.

Converters for low-voltage applications are subject to a tremendous cost pressure. The simplest and cheapest solution which is able to fulfil all constraints is usually adopted. Therefore, these constraints have to be defined, starting from the basic properties such as unidirectional or bidirectional power flow and ending at additional features and optimization targets such as high bandwidth control or efficiency optimization. These additional targets are not only limited to the converter itself but can include interactions of the converter with its surrounding, such as the losses in passive components and in the load machine. Accordingly, defining the costs of a certain converter topology is complicated even more because of the possible influences on the surrounding, such as smaller and cheaper filtering components and possible energy savings during the operation of the complete system.

In this chapter, a comparison between different converter topologies suitable for a bidirectional, low-voltage VSD system is given. Several aspects are considered, such as the implementation effort, the converter efficiency, the semiconductor loss distribution and the necessary semiconductor chip area.

Although possible impacts on the surrounding of the converter are already anticipated in this chapter, the comparison is mainly limited to the converter topologies itself. A thorough analysis of the complete VSD system including the interactions between the single components is given finally in Chapter 5.

3.1 2-level and 3-level topologies for low-voltage VSD applications

A basic classification of a VSD system can be done concerning the power flow direction. Many systems need only unidirectional power flow, such as ventilators and compressors. Anyway, speed regulation is an important feature as it allows to regulate the power flow and to reduce losses in the mechanical subsystem in many cases [5].

Bidirectional power flow is required in many dynamical drive systems, such as dynamical lifts, drilling or machining processes and especially in traction applications (automotive, locomotive). If the reverse power flow is only small, the grid interface can be left unidirectional and the converter equipped with an additional break chopper.

In an unidirectional system, the grid interface is often implemented as a passive diode rectifier. This solution is characterized by low losses and low costs. Unfortunately, due to the diode bridge, the grid currents are highly distorted and passive filtering is necessary. The power factor is low, leading to additional losses in the power grid. As a further drawback, the dc-link voltage is defined by the line-to-line voltage of the grid and can not be increased to a higher voltage which is often necessary to dynamically control the load machine.

Alternatively, the unidirectional grid interface could be realized with a switched topology, such as the Vienna rectifier [103], the Swiss rectifier [104] or simple three-phase buck/boost converters [105]. These topologies are able to form sinusoidal input currents with low distortion and can perform power factor correction to a certain extent. Unidirectional interfaces are not further considered in this thesis, but a very

thorough analysis, comparisons and reviews can be found in [105–107].

A bidirectional VSD is most often required where excessive breaking energy should be recovered and fed into the grid. The standard industry solution consists of a 2-level topology at the grid side, a dc-link capacitor for transient energy storage and a second 2-level topology for the output stage directly connected to the load machine. This configuration is generically named a back-to-back converter because the same topology is used for the input stage and the output stage. There are a few alternative topologies which could be chosen to implement such a bidirectional converter topology. The most important ones are:

- 2-level voltage source converter (2LC)
- 3-level T-type converter (3LT^{2}C)
- 3-level neutral point clamped converter (3LNPC^2)
- 3-level flying capacitor converter (3LFC^2)
- 3-level active neutral point clamped converter (3LANPC^2)
- 3-level coupled inductor converter (3LCIC)
- Matrix converter (MC)
- Multi-level converter (MLC).

This wide range of converters with very different properties makes a fair comparison among them difficult. Therefore, a short qualitative assessment considering the suitability for low-voltage VSD applications with their unique requirements is given in order to make a preselection of the topologies. Finally, three topologies, namely the 2-level converter, the 3-level NPC converter and the 3-level T-type converter are chosen for a deeper comparison presented in Sections 3.3 - 3.6. They are considered to be the most competitive topologies for a low-voltage VSD system.

3.1.1 2-level converter (2LC)

The 2-level converter (2LC) has established itself as the standard industry solution for low-voltage VSD applications. The schematic of the

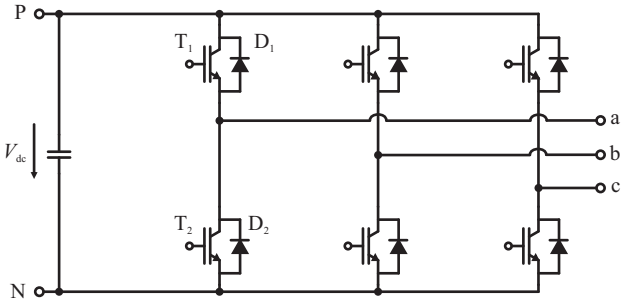

Figure 3.1: Schematic of the 2-level converter.

topology is depicted in Fig. 3.1. Often it is used in a back-to-back configuration, where the same topology is used at the grid side as a rectifier with PFC funtionality and at the output side as an inverter topology.

The main strengths are its simplicity and the low parts count. It is formed by only 6 diodes and 6 IGBTs. The number of isolated gate drive supplies can be minimized to only four if all three lower IGBTs $T_{2a,b,c}$ are fed with the same isolated voltage. The 2LC sets the lower limits concerning simplicity and material expenses for a bidirectional three-phase variable voltage and variable frequency interface.

The main drawbacks of the topology are the high switching losses. Although the switching performance of IGBTs is still improving continuously, the efficiency of the topology suffers considerably if the switching frequency is increased. The switching losses of the 2LC can be reduced either by implementing discontinuous PWM schemes with loss optimal clamping (cf. Section 3.3.1), or by employing SiC Schottky diodes [108]. The SiC Schottky diode shows approximately no turn-off losses. Additionally, the turn-on losses of the commutating IGBT is reduced because of the absence of the diode reverse recovery effect [109], which is responsible for typically 30% of the IGBT turn-on loss energy. Unfortunately, the SiC Schottky diodes are still quite expensive compared to conventional Schottky diodes if similar pulse current ratings are considered.

The second drawback considering a holistic system comparison is the high harmonic content of the output voltage. The 2-level voltage waveform is responsible for additional losses in passive components such as the boost inductor or the load machine (cf. Section 2.2).

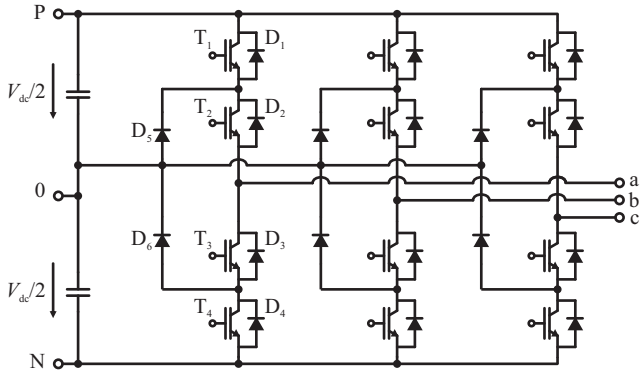

Figure 3.2: Schematic of the 3-level NPC converter.

Concluding, the 2LC is the low cost industry solution which has to be beaten by alternative solutions.

3.1.2 3-level neutral point clamped converter (3LNPC²)

The 3-level neutral point clamped converter (3LNPC²) was proposed in [110] and has been successfully implemented mainly for medium-voltage applications. The topology is depicted in Fig. 3.2.

The strengths of the 3LNPC² are the low switching losses and the ability to share the blocking voltage over two series-connected devices what is especially important for medium voltage applications. There, the blocking capability of the semiconductor devices was not sufficient to go for higher dc-link voltages and the associated higher inverter power levels. Therefore, the series connection of devices was the only possible way to increase the dc-link voltage. The clamping diodes (D_5, D_6) have a special function as they limit the necessary blocking voltage of the devices to $V_{dc}/2$ and allow to connect them in series without special voltage balancing circuits [111, 112].

The switching loss energy of IGBTs and diodes for a fixed rated blocking voltage scales approximately linearly with the commutation voltage. Additionally, it reduces with the rated blocking voltage due to changed semiconductor characteristics. Therefore, an overproportional reduction of the switching losses (up to a factor of 5) can be observed

when a converter for low-voltage applications can be built with 600 V devices instead of 1200 V devices [10].

A similar effect can be observed with the conduction losses. Due to different semiconductor characteristics of the 600 V devices, the forward voltage drop reduces slightly for the same rated current compared to a 1200 V device [10]. Although there is a series connection of two devices in the output current path of the 3LNPC², the forward voltage drop and the associated conduction losses are less than twice the ones of a single 1200 V device.

For high switching frequencies ($f_{sw} \geq 10...16\,kHz$), the reduction of the switching losses overcompensates the increase of the conduction losses and the efficiency of the 3LNPC² is higher than the efficiency of the 2LC. Additionaly, due to the 3-level output voltage, losses in passive components such as the boost inductors and the load machine can be reduced (cf. Section 2.2). A further positive impact of the 3-level output voltage are reduced overvoltages with long motor cables and smaller insulation stress of the machine [113].

The switching losses of the 3LNPC² could even be reduced further by implementing 600 V SiC Schottky diodes [114]. Due to the increased costs of SiC devices the application range is limited to high-speed drive systems with a very high switching frequency ($f_{sw} \geq 50\,kHz$). As the standard 600 V diodes have already a very small reverse recovery charge, the achievable efficiency improvement using SiC diodes is only small. For most VSD applications, more important than a further reduction of the switching losses is the reduction of the conduction losses, what is a strength of the 3-level T-type converter.

The drawbacks of the 3LNPC² are obviously the increased complexity and the increased number of semiconductors and associated gate-drive circuits. In total, 18 diodes and 12 IGBTs are necessary compared to only 6 diodes and 6 IGBTs of the 2LC. The number of isolated gate drive supplies increases by 6 compared to the 2LC. The number of PWM units is doubled.

Although the number of semiconductor devices is increased, the costs have to be carefully analyzed. It is usually possible to use semiconductors with reduced current ratings compared to the 2LC. Because the converter losses are distributed over many devices and lead only to a small increase of the junction temperatures, the chip area of the semiconductors can be reduced. This effect is analyzed in detail in Section 3.6. Additionally, in a holistic aspect, energy savings due to the

increased converter efficiency and lower losses in the passive elements might shift the cost balance in favour of the 3LNPC².

The modulation complexity of the 3LNPC² is increased considerably. It is necessary to balance the voltages of the split dc-link capacitor. This can be done passively with a balancing circuit or actively by choosing alternative voltage space vectors. If special discontinuous PWM strategies with switching loss optimal clamping are applied, the dc-link capacitors are principally not loaded evenly and depending on the implemented capacitance values, the modulation has to be adapted in order to compensate for the voltage unbalance [115].

Due to the low switching losses and the favourable 3-level output voltage, the 3LNPC² is considered to be a good choice for low-voltage VSD applications. It is therefore included in the detailed analysis following in the next sections.

3.1.3 3-level T-type converter (3LT²C)

The basic topology of the 3-level T-type converter (3LT²C) is depicted in Fig. 3.3. The conventional 2LC topology is extended with an active, bidirectional switch to the dc-link mid-point. The 3LT²C was initially presented in the late 70s and reconsidered during the 80s [110, 116–120]. Due to the success of the 3LNPC² in the medium-voltage market, the 3LT²C gained not much attention. This changed some years ago, during the booming phase of high efficiency solar inverter topologies [121].

For low-voltage applications (e.g. $V_{\mathrm{dc}} = 650\,\mathrm{V}$), the high-side and the low-side switches ($\mathrm{T}_1/\mathrm{D}_1$ and $\mathrm{T}_4/\mathrm{D}_4$) would usually be implemented with 1200 V IGBTs/diodes as the full dc-link voltage has to be blocked. Differently, the bidirectional switch to the dc-link mid-point has to block only half of the dc-link voltage. It can be implemented with devices having a lower voltage rating, in the case at hand two 600 V IGBTs including antiparallel diodes are used. Due to the reduced blocking voltage the middle switch shows low switching losses and acceptable conduction losses although there are two devices connected in series.

Contrary to the 3LNPC², there is no series connection of devices that has to block the whole dc-link voltage V_{dc}. Consequently, the conduction losses are reduced, if bipolar devices are considered. Whenever the output is connected to (P) or (N) the forward voltage drop of only one device occurs, contrary to the 3LNPC² topology where always two

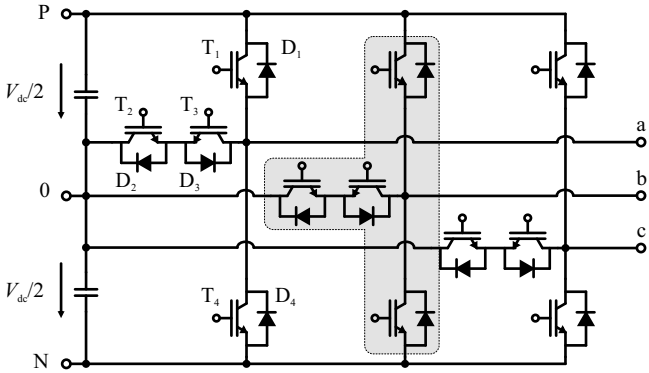

Figure 3.3: Schematic of the 3-level T-type converter. A single bridge-leg of the T-type VSC resembles the shape of a rotated character "T", accordingly the topology is denominated as T-type topology.

devices are connected in series.

The switching losses of the 3LT²C are reduced compared to the 2LC because the commutation voltage is only $V_{\mathrm{dc}}/2$. The switching loss energy of the IGBTs and the diodes is approximately proportional to the commutation voltage. Due to the combination of 1200 V and 600 V devices, the datasheet values for the switching losses are not accurate enough to calculate the switching losses. In IGBT datasheets, the switching losses are only specified for devices of the same blocking capability. Therefore, the switching loss energies have to be measured for the different transitions.

An additional benefit related to using single 1200 V devices to block the full dc-link voltage arises during switching transitions directly from the positive (P) to the negative (N) dc-link voltage level and vice versa. For the 3LNPC², the clamping diodes limit the voltage across the devices to $V_{\mathrm{dc}}/2$ in the static case. Nevertheless, direct transitions from the positive (P) to the negative (N) dc-link voltage level are usually omitted as there might occur an uneven share of the voltage to be blocked in the transient case when both IGBTs connected in series turn off at the same time. This undesirable effect can not occur in the 3LT²C. Accordingly, it is not necessary to implement low-level routines which prevent such transitions or ensure a transient voltage balancing among series connected IGBTs.

The T-type topology is also used in medium-voltage applications [122,123] where it is known as neutral point piloted (NPP) converter or transistor clamped converter (TCC). For medium-voltage applications, the voltage blocking capability of a single device is not sufficient to block the full dc-link voltage. Each of the switches T_1 and T_4 therefore has to be replaced by a series connection of two IGBTs. Special active gate drive units are necessary for transient and steady-state voltage balancing [111, 112]. The implementation effort is increased considerably and the conduction losses increase due the series connection of bipolar devices. Therefore, this configuration is not recommended for low-voltage applications. The available devices have sufficient voltage ratings and fast switching speeds, therefore it is not necessary to connect devices in series. An increased output power is achieved with increased phase currents. The conduction losses are an important factor limiting the power range and should be kept as small as possible. Historically, the 3-level topologies were developed for medium-voltage applications. There, it was necessary to place devices in series due to the limited voltage blocking capability of the available devices. The drawback of the increased conduction losses due to the series connected bipolar devices was overcompensated by the gain in voltage handling capability and the directly related gain in power handling capability. Contrary, for low-voltage applications this benefit does not exist.

Switch configuration

There are basically two ways the two 600 V IGBTs can be configured to form a bidirectional switch, either in common emitter configuration or in common collector configuration.

The common emitter configuration (cf. Fig. 3.4a) would require one additional isolated gate drive supply voltage for each bridge-leg, summing up to three additional gate drive supplies compared to the 2LC.

This number can be reduced even more if a common collector configuration (cf. Fig. 3.4b) is used. T_2 shares now a common emitter with the high-side switch T_1 and can be supplied with the isolated gate drive voltage of T_1. The emitter of the second 600 V IGBT is connected to the mid-point voltage level. If the 3-phase topology is considered, all three IGBTs $T_{3,a,b,c}$ share a common emitter and therefore only one isolated gate drive supply is necessary. In total, the complete 3LT^{2}C can be implemented with only one additional isolated gate drive supply

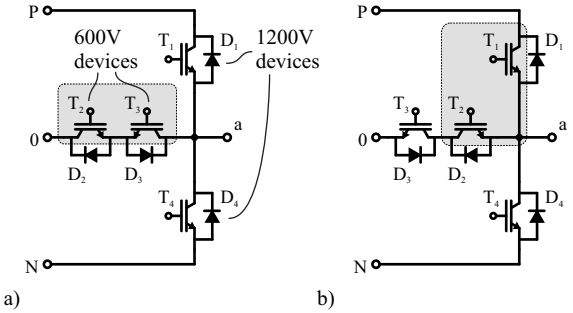

Figure 3.4: The bidirectional switch to the midpoint can be implemented with two IGBTs in a) common emitter configuration or b) in common collector configuration.

compared to the 2LC.

The necessary power rating of the isolated gate drive supply of the high-side switch T_1 is not increased if the gate charges of the 600 V and the 1200 V IGBT are approximately equal. Because of the implemented commutation and modulation strategy T_1 and T_2 are never switched both in the same modulation cycle.

It is still necessary to implement six additional gate drive ICs and six additional digital isolators for the switch signals which will increase the costs slightly. Compared to the 3LNPC², the removal of the clamping diodes reduces the necessary diodes from 18 to 12. Furthermore, the reduction of the additional isolated gate drive supplies from six to one is a clear improvement and can drive the costs down.

Alternatively, the bidirectional switch could be implemented with a single IGBT and 4 diodes as presented in [124, 125]. This has the drawback of increased conduction losses as always two diodes and the IGBT are connected in series if the output is connected to the neutral dc-link voltage level.

Commutation

The switch commutation has to be considered in detail for the 3LT²C. Basically, the output of a bridge-leg can be connected for both current directions to the positive (P), neutral (0) or the negative (N) dc-link voltage level as can be seen in Fig. 3.5. The positive voltage level, for instance, could be achieved by closing T_1, the neutral level by closing

Table 3.1: Switching states

State	$\boldsymbol{V}_{\text{out}}$	$\mathbf{T_1}$	$\mathbf{T_2}$	$\mathbf{T_3}$	$\mathbf{T_4}$
P	$+V_{\text{dc}}/2$	on	on	off	off
0	0	off	on	on	off
N	$-V_{\text{dc}}/2$	off	off	on	on

T_2 and T_3, and the negative level by closing T_4. However, this strategy would require a current dependent commutation sequence. Fortunately, there is a simpler commutation strategy which works independent of the current direction.

If we close not only T_1, but T_1 and T_2 for the positive voltage level, T_2 and T_3 for the neutral, and T_3 and T_4 for the negative voltage level, the current commutates naturally to the correct branch independent of the current direction. Table 3.1 describes which switches are closed to achieve the desired output voltage. A simple turn-on delay for all switches is sufficient to prevent a dc-link short circuit. If these switching signals are used, the modulation is identical to the 3LNPC² modulation.

As an example, we consider Fig. 3.5a, where the output phase is connected to the positive (P) voltage level (T_1 and T_2 are closed) for positive output current. In order to commutate to the neutral level (0) T_1 is opened and after the turn-on delay T_3 is closed additionaly. During the turn-off of T_1 the current naturally commutates to T_2 and D_3 and to the neutral level. For a negative phase current (cf. Fig. 3.5b), the current commutates to the neutral after T_3 is closed.

If we switch back from (0) to (P), first T_3 is opened and after the turn-on delay T_1 is closed. For a positive phase current (cf. Fig. 3.5c) during turn-off of T_3 the current continues flowing through D_3 and commutates to the positive voltage level after the turn-on of T_1. For a negative phase current (cf. Fig. 3.5d) the current commutates to D_1 during turn-off of T_3. This principle works for all remaining switching transitions.

The modulation strategies known from the 3LNPC² can also be applied to the 3LT²C. The modulation strategy is an important point for the converter efficiency [126]. Either space vector based modulation strategies [101] or phase oriented PWM [127, 128] can be used. In the detailed efficiency comparison presented in the next sections, a space vector modulation with loss optimal phase clamping is used.

The direct transition from (N) to (P) and vice versa is avoided by the

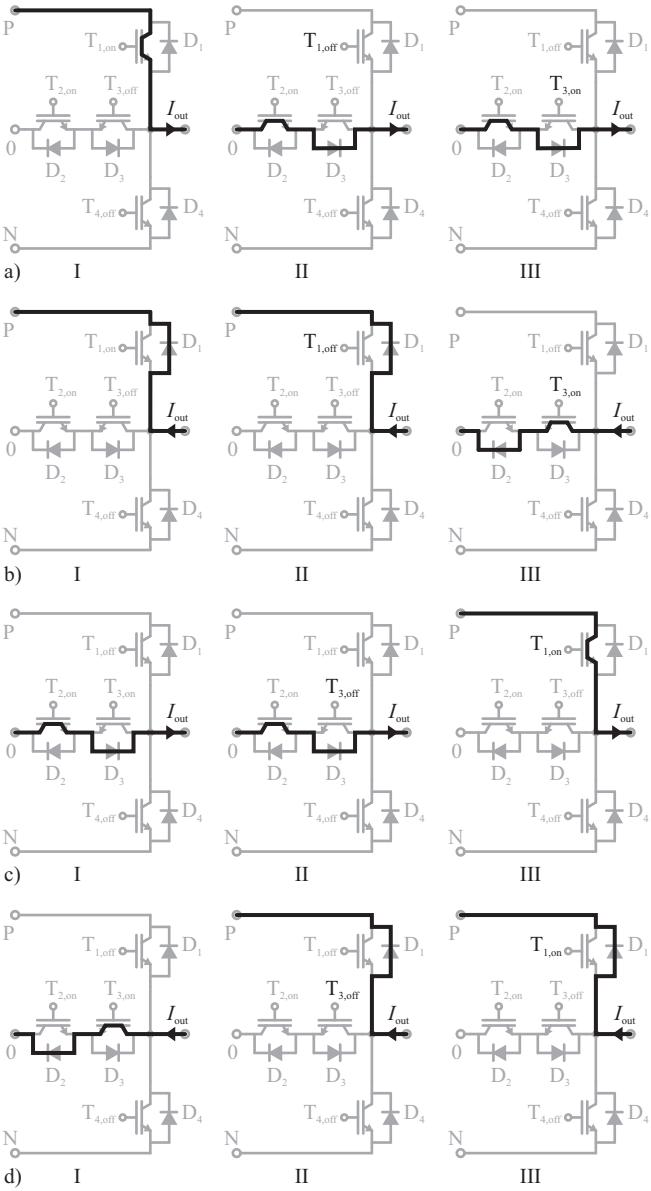

Figure 3.5: Current commutation during switching transition (P → 0) for a) positive and b) negative output current, and for transition (0 → P) for c) positive and d) negative output current.

implemented space vector modulation (and it is also avoided by standard sinusoidal PWM) and occurs only at sector borders. Although the transition is not a problem for the 3LT²C it produces additional losses in the 600 V diodes. A reverse recovery current pulse flows to the neutral voltage level because of the blocking voltage change from $-V_{\mathrm{dc}}/2$ to $+V_{\mathrm{dc}}/2$ over D_2 and D_3. This reverse recovery current produces additional losses in the diodes.

By omitting direct transitions from (N) to (P) and vice versa, the IGBTs T_1 and T_2 are not switched in the same modulation cycle. Therefore, as already mentioned, the necessary power rating of the isolated gate drive supply of the high-side switch T_1 is not increased if it is used to additionally power the gate drive unit of T_2.

Concluding, the 3LT²C has a couple of strengths that make it a competitive alternative to the 2LC for low-voltage VSD applications. The 3LT²C basically combines the positive aspects of the 2LC such as low conduction losses, small part count and a simple operation principle with the advantages of the 3LNPC² such as low switching losses and superior output voltage quality. It is therefore included into the detailed analysis.

3.1.4 Further alternative topologies

3-level active neutral point clamped converter (3LANPC²)

The 3-level active neutral point clamped converter (3LANPC²) is an extension of the 3LNPC². The six clamping diodes are replaced by bidirectional switches built with IGBTs and anti-parallel diodes. The schematic of the topology is depicted in Fig. 3.6.

The topology was initially proposed in [129,130] for medium-voltage applications. The additional IGBTs were introduced to overcome some drawbacks related to the characteristic loss distribution profile of the conventional 3LNPC².

It is known that in the conventional 3LNPC², depending on the operating point, some of the semiconductor devices obtain heavy losses whereas other devices are not stressed at all [114]. E.g. for inverter operation, the switching losses are concentrated in the outer switches T_1 and T_4 and in the clamping diodes D_5 and D_6. In medium-voltage applications, for the reason of simplicity and for failure cases, all installed semiconductors have the same current rating. The current rating of all semiconductor devices is chosen according to the device that ob-

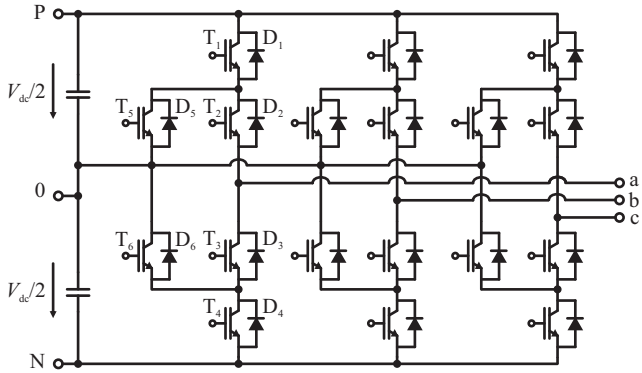

Figure 3.6: Schematic of the 3-level ANPC converter.

tains maximum losses. Therefore, the ratio of the output power to the installed switch power rating is rather low, i.e. most of the installed switches are not fully utilized.

The additional IGBTs T_5 and T_6 of the 3LANPC² introduce alternative switching states and allow to shift the switching losses to T_2/T_3 and to D_2/D_3. Therefore it is possible to distribute the losses more evenly among all semiconductor devices. The semiconductor utilization is increased, the losses of the most stressed device can be reduced. Consequently, either the switching frequency can be increased, the lifetime can be increased or semiconductors with a lower current rating can be chosen.

Although the losses can be distributed more evenly, the converter efficiency cannot be increased. The total losses of the 3LANPC² are equal to the losses of the conventional 3LNPC².

An application of the 3LANPC² as acitve filter was presented in [131]. There, the loss balancing principle was used in combination with an optimized clamping scheme adapted to the special current shapes of an active filter system. It was possible to share the losses equally among the semiconductors achieving a high semiconductor utilization and a high switching frequency.

Nevertheless, due to the additional six IGBTs and the associated gate drive circuits the costs of the 3LANPC² are considerably higher. Although the specific problem of uneven loss distribution can be solved, the gain is relatively small. Not only more semiconductors are necessary

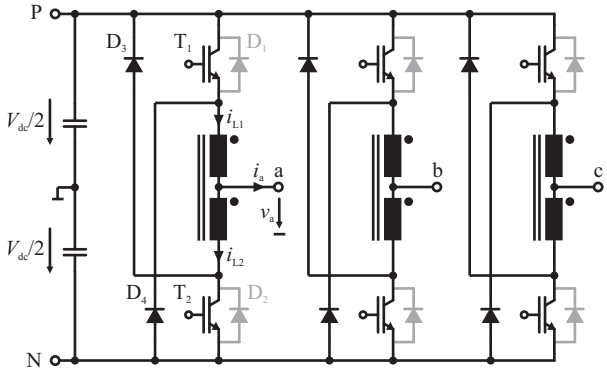

Figure 3.7: Schematic of the 3-level coupled inductor converter.

compared to the 3LNPC², but also more gate signals are necessary and the modulation complexity is increased again. Concluding, the 3LANPC² does not show enough advantages to justify its application in the low-voltage field. Therefore, it is not considered further in this thesis.

3-level coupled inductor converter (3LCIC)

The 3-level coupled inductor converter (3LCIC) was proposed in [132–134]. The basic 2LC is enhanced with a coupled inductor integrated into the bride-legs in order to form a third voltage level. A schematic of the converter is depicted in Fig. 3.7.

The coupled inductor converter has some interesting features. It allows to extend a 2-level topology to a 3-level topology without using additional switches. Therefore, no additional isolated gate drive supplies are necessary. Also, no additional gate signals, signal isolation chips and IGBT gate drivers are necessary. The third voltage level is achieved by introducing a coupled inductor in each bridge-leg and adding 6 additional free-wheeling diodes. It is also not necessary to split the dc-link capacitor into two series connected capacitors.

The functionality of the 3LCIC is quite simple. If T_1 is closed, the output is connected to $v_a = +V_{dc}/2$, if T_2 is closed, the output is connected to $v_a = -V_{dc}/2$. Additionally, the output terminal can be connected to a zero voltage ($v_a = 0$) level either by closing both T_1 and T_2 at the same time or by opening both T_1 and T_2 at the same

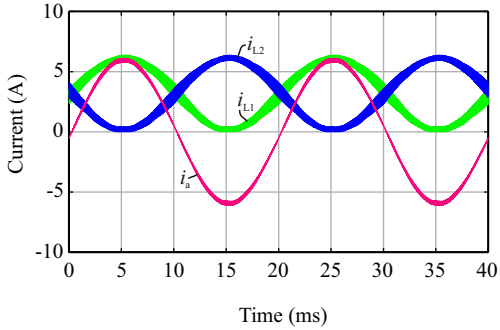

Figure 3.8: Simulated currents in a bridge-leg of the coupled inductor converter.

time. During these zero-states, the positive or negative dc-link voltage is connected across the magnetizing inductance of the coupled inductor. With two carriers having a phase shift of 180° it is ensured that no average dc voltage is applied over the coupled inductor. Interestingly, the current in the coupled inductor can only flow in one direction. The anti-parallel diodes D_1 and D_2 are actually not necessary and can be removed. A magnetizing current i_m of half the fundamental current amplitude is superimposed on the coupled inductor current and an associated dc-flux is present in the core. The currents flowing in the upper inductor, i_{L1}, and in the lower inductor, i_{L2} (cf. Fig. 3.8 and Fig. 3.7) are given as

$$i_{L1} = i_m + \frac{i_a}{2} \approx \frac{\hat{I}}{2}\left(1 + \sin \omega_e t\right) \tag{3.1}$$

$$i_{L2} = i_m - \frac{i_a}{2} \approx \frac{\hat{I}}{2}\left(1 - \sin \omega_e t\right). \tag{3.2}$$

The 3-phase coupled inductor converter can either be built with separate inductors for each bridge-leg or with a 3-limb core. If separate inductors are used for each phase, a dc-premagnetization exists in the core. Therefore, a low permeability core material has to be used [132] what makes the inductors bulky as high inductance values have to be implemented.

The maximum current ripple $\Delta i_{m,pp}$ of the magnetizing current, which is superimposed on the inductor currents, is given when the out-

put phase voltage is zero and V_{dc} and $-V_{\mathrm{dc}}$ are applied with 50% duty-cycle over the magnetizing inductance. It is given as

$$\Delta i_{\mathrm{m,pp}} = \frac{V_{\mathrm{dc}}}{L_{\mathrm{m}}} \frac{1}{2 f_{\mathrm{sw}}}. \tag{3.3}$$

For a sample 10 kW system, limiting $\Delta i_{\mathrm{m,pp}}$ to 20% of the output current amplitude $\hat{I}_{\mathrm{n}} = 20.5\,\mathrm{A}$, requires at a switching frequency of $f_{\mathrm{sw}} = 16\,\mathrm{kHz}$ and a dc-link voltage of $V_{\mathrm{dc}} = 650\,\mathrm{V}$ already a magnetizing inductance of 5 mH.

The 3-limb core has the advantage of canceling the dc-flux components and a core material with a higher permeability can be used instead [135]. Unfortunately, other difficulties arise with the 3-limb core. The modulation complexity increases considerably because certain switching states can force the flux associated with a limb to leave the iron path as the fluxes linked to the other two coils may be impressed to be constant [136]. In that case, only the leakage inductance instead of the magnetizing inductance is limiting the current rise during the zero-state. A special modulation scheme has to be introduced that avoids these switching states with the drawback of increasing the net switching frequency and using not the nearest three voltage space vectors for modulating the output voltage what has a negative impact on the output voltage quality and the associated losses in the load machine.

Passive components are usually rather expensive as they cannot be manufactured and assembled automatically.

Although the topology has some interesting features, there are also a couple of severe drawbacks. Besides the size and the costs of the coupled inductors, the most important drawbacks are the increased losses in the inverter and the losses in the coupled inductors.

In the following, a simple comparison between the semiconductor losses obtained with the standard 2LC and with the 3LCIC is given.

If the average and the RMS current flowing through a device are known, the average conduction losses can be calculated with

$$P_{\mathrm{cond}} = v_{\mathrm{f}} \cdot i_{\mathrm{avg}} + r_{\mathrm{f}} \cdot i_{\mathrm{rms}}^2, \tag{3.4}$$

where v_{f} denotes the constant voltage drop and r_{f} denotes the differential resistance of the piecewise linear forward characteristics of the device.

The average and RMS currents can be obtained by considering the actual current $i(t)$ flowing through the device, such as the current flowing through the upper IGBT of a standard 2-level bridge-leg depicted

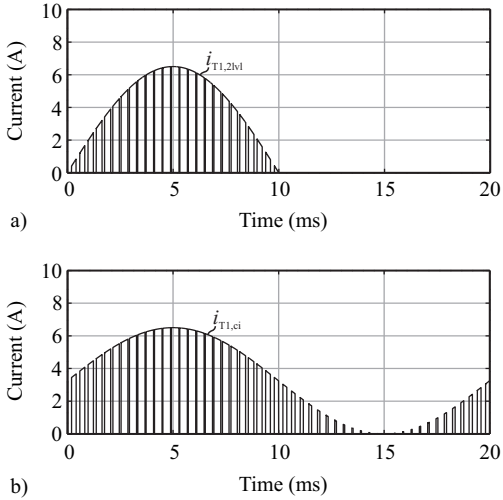

Figure 3.9: Comparison of the IGBT current stress over a fundamental period between a) the standard 2-level inverter and b) the coupled inductor inverter.

in Fig. 3.9a. For a simple comparison, continuous sinusoidal PWM is considered. A switching loss optimal clamping scheme for the 2LC is analyzed in Section 3.3.1.

According to [126], for the 2LC, the average and squared RMS current of the IGBTs is given as

$$i_{\mathrm{T,avg,2lvl}} = \hat{I}\left(\frac{1}{2\pi} + \frac{m}{8}\cos\varphi_1\right) \tag{3.5}$$

$$i^2_{\mathrm{T,rms,2lvl}} = \hat{I}^2\left(\frac{1}{8} + \frac{m}{3\pi}\cos\varphi_1\right), \tag{3.6}$$

where $m = \hat{V}/(V_{\mathrm{dc}}/2)$ is the modulation index and φ_1 denotes the voltage to current phase displacement angle. The average and squared RMS current of the diodes is given as

$$i_{\mathrm{D,avg,2lvl}} = \hat{I}\left(\frac{1}{2\pi} - \frac{m}{8}\cos\varphi_1\right) \tag{3.7}$$

$$i^2_{\mathrm{D,rms,2lvl}} = \hat{I}^2\left(\frac{1}{8} - \frac{m}{3\pi}\cos\varphi_1\right). \tag{3.8}$$

The switching loss energy E_n for a single turn-on or turn-off switching transient is usually given in the device datasheet and is measured at a nominal current I_n and a nominal commutation voltage V_n. As an approximation, the switching loss energy can be scaled linearly with the commutation voltage and with the switched current as

$$E_\mathrm{sw} = \frac{E_\mathrm{n}}{V_\mathrm{n} I_\mathrm{n}} \cdot v \cdot i. \tag{3.9}$$

The average device switching losses are found by averaging the local switching losses over a fundamental period and are given for the 2LC as

$$P_\mathrm{sw,T,2lvl} = \frac{1}{\pi} f_\mathrm{sw} \hat{I} \left(E_\mathrm{T,off} + E_\mathrm{T,on} \right) \tag{3.10}$$

$$P_\mathrm{sw,D,2lvl} = \frac{1}{\pi} f_\mathrm{sw} \hat{I} E_\mathrm{D,off}. \tag{3.11}$$

Due to the special current shapes of the 3LCIC shown in Fig. 3.8, the average and RMS currents in the switches and diodes are increased considerably. All semiconductor devices are not only stressed during half of the fundamental period, but over the complete fundamental period. The current i_L1 is continuously switched between T_1 and D_4, whereas i_L2 is switched between T_2 and D_3. The current flowing through the IGBT T_1 is depicted in Fig. 3.9b. The average and squared RMS current of the IGBTs is given as

$$i_\mathrm{T,avg,ci} = \hat{I} \left(\frac{1}{4} + \frac{m}{8} \cos \varphi_1 \right) \tag{3.12}$$

$$i^2_\mathrm{T,rms,ci} = \hat{I}^2 \left(\frac{3}{16} + \frac{m}{8} \cos \varphi_1 \right). \tag{3.13}$$

The average and squared RMS current of the diodes can be calculated with

$$i_\mathrm{D,avg,ci} = \hat{I} \left(\frac{1}{4} - \frac{m}{8} \cos \varphi_1 \right) \tag{3.14}$$

$$i^2_\mathrm{D,rms,ci} = \hat{I}^2 \left(\frac{3}{16} - \frac{m}{8} \cos \varphi_1 \right). \tag{3.15}$$

Table 3.2: Semiconductor losses of the 2-level converter and the coupled inductor converter for $\hat{V} = 325\,\mathrm{V}, \hat{I} = 20.5\,\mathrm{V}, \varphi_1 = 0°$.

Quantity	Variable	2LC	3LCIC
Switching losses	P_{sw}	219.2 W	344.3 W
Conduction losses	P_{cond}	51.4 W	78.6 W
Total losses	P_{total}	270.6 W	422.9 W
Efficiency	η	97.4 %	95.9 %

The average switching losses of the coupled inductor inverter are

$$P_{\mathrm{sw,T}} = \frac{1}{2} f_{\mathrm{sw}} \hat{I} \left(E_{\mathrm{T,off}} + E_{\mathrm{T,on}} \right) \tag{3.16}$$

$$P_{\mathrm{sw,D}} = \frac{1}{2} f_{\mathrm{sw}} \hat{I} E_{\mathrm{D,off}}. \tag{3.17}$$

The net switching frequency is doubled compared to the simple 2LC as in every modulation period, T_1 and T_2 are switched independently with two carrier signals having a phase-shift of 180°. The carrier frequency and the associated switching frequency of the single devices should actually be halved compared to the 2LC to get the same net switching frequency, but reducing the switching frequency is not favourable with the 3LCIC because either $\Delta i_{\mathrm{m,pp}}$ increases or the necessary inductance L_{m} has to be increased.

The total semiconductor losses for the 2LC and the 3LCIC are calculated for a sample 10 kW system with a dc-link voltage of $V_{\mathrm{dc}} = 650\,\mathrm{V}$ and a switching frequency of $f_{\mathrm{sw}} = 16\,\mathrm{kHz}$. The device characteristics are taken from the datasheet of the Infineon IKW40T120 package which combines an IGBT and a diode rated for 1200 V and 40 A. The losses are calculated for inverter operation ($\varphi_1 = 0°$) and are summarized in Table 3.2.

The total semiconductor losses of the 3LCIC increase by more than 50% compared to the 2LC. As already mentioned, the switching frequency could be reduced but this would require to increase the magnetizing inductance. Furthermore, the coupled inductors show considerable ohmic and iron losses that further reduce the efficiency of the converter.

The 3LCIC can generate a 3-level output voltage without additional semiconductors, but it misses a basic strength of the conventional 3-level converters (3LNPC² or 3LT²C). Usually, the switching losses of 3-level

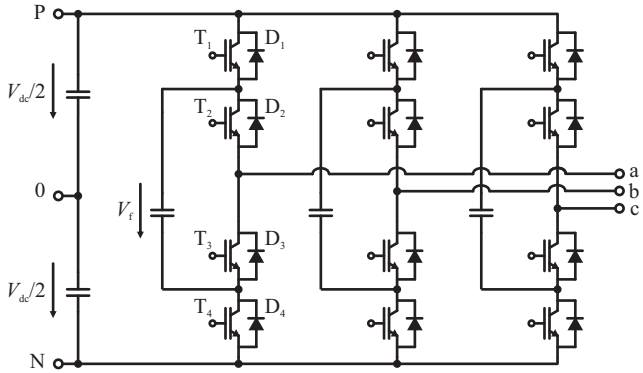

Figure 3.10: Schematic of the 3-level flying capacitor converter.

converters are reduced considerably, mainly because the commutation voltage of the devices is only $V_{dc}/2$. This is not the case with the coupled inductor converter, where always the full dc-link voltage is switched.

Concluding, considering all the weaknesses of this topology, such as the volume and the costs of the inductors, the increased losses in the inverter and in the inductors and the increased modulation complexity, the coupled inductor converter is not suitable for low-voltage VSD applications and seems to be only of academic interest.

3-level flying capacitor converter (3LFC²)

The 3-level flying capacitor converter (cf. Fig. 3.10) is a native 3-level topology and was presented initially in [137]. It removes the 6 clamping diodes known from the 3LNPC². As nothing comes for free, three additional capacitors have to be added across the bridge-legs. The number of IGBTs and associated isolated gate drive supplies, isolation chips and IGBT drivers is identical to the 3LNPC².

There are several papers comparing the 3LFC² with the 3LNPC² (cf. [138–141]).

There is one basic difference between the 3LFC² and the 3LNPC². In order to keep the value of the flying capacitors small, the modulation is changed. Two carrier signals phase-shifted by 180° are used to generate the switching signals in such a way that the average current over a modulation cycle flowing through the flying capacitors is zero. This principle is equivalent to the modulation scheme used for the 3LCIC,

but instead of having zero average voltage over the magnetizing inductance of the coupled inductors, zero average current is supplied to the flying capacitors.

Therefore, the properties of the 3LFC² are similar to the the 3LCIC, but with most of the weaknesses of the 3LCIC removed. Instead of using a magnetic component with its inherent high losses, a capacitive component is used to achieve the third voltage level. Contrary to the 3LCIC, there is no superimposed dc-current increasing the losses. The 3LFC² is a 3-level topology using impressed voltages. Therefore, the switching losses are reduced as the commutation voltage is only $V_{\mathrm{dc}}/2$ and devices with only half of the blocking voltage can be used.

Similar to the 3LCIC, using the phase-shifted carrier modulation doubles the net switching frequency as always two IGBTs are switched in a bridge-leg during a modulation period. To achieve the same switching losses as for the 3LNPC², the carrier frequency can be halved. Unfortunately, reducing the carrier frequency increases the value of the flying capacitor if the same voltage ripple should be maintained. Because the switching losses are very small with the 600 V devices, increasing the switching frequency is a feasible way to obtain small capacitors.

The reachable efficiency of the 3LFC² and the 3LNPC² is similar [141] if the carrier frequency is halved such that the net switching frequency is identical. There are no basic differences in the loss characteristics, except of a more uniform distribution of the losses among the semiconductors. For both topologies, the conduction losses are slightly increased compared to the 2LC because there are always two devices connected in series and the associated forward voltage drops are adding up. The switching losses are small because in both cases, the commutation voltage is reduced to $V_{\mathrm{dc}}/2$. Therefore, the 3LFC² is suitable for applications that require a high switching frequency.

Due to the similarity of the 3LNPC² and the 3LFC², only the 3LNPC² is included in the detailed comparison presented in the next sections. The basic findings concerning the performance of the 3LNPC² can more or less directly be transferred to the 3LFC².

Matrix converter

Matrix converters have been a research subject over the last decades, especially in the academic world [142–144]. The idea of the matrix converter is to generate the variable output voltage with a suitable switching network directly from the input voltage, without intermedi-

ate energy storage. For certain applications with low dynamic control requirements, the lack of an intermediate energy storage element can be an advantage. In the past, especially electrolytic capacitors were known to have a rather short lifetime. Therefore, the absence of such an element would increase the reliability and finally reduce costs. Modern foil capacitors are known to have a comparable lifetime to the semiconductor devices and do not have a reliability problem at all but are more expensive and need more volume compared to electrolytic capacitors for equal capacitance. Nevertheless, for dynamic VSD applications, an energy storage element is often required and is needed for ride-through capability in order to overcome short mains outages as well.

A weakness of the matrix converter is also the missing capability to boost the input voltage. The maximum output voltage amplitude is limited to 86.6% of the input voltage amplitude [143]. It is therefore difficult to feed an induction machine designed for direct grid application with the matrix converter as it would always run with less than rated flux and would not run in its optimal operating point. Additionally, less voltage reserve is available for controlling the machine unless it is designed for a reduced stator voltage.

The complexity of the matrix topology and of the modulation strategies have often been mentioned as weaknesses of the converter. A detailed analysis reveals that the complexity is not much increased compared to a back-to-back 2-level converter, especially not if the indirect sparse matrix converter topology [142] is used. Also the modulation complexity is not much increased compared to a simple space vector modulation and can be implemented easily on a standard DSP.

A very thorough analysis of matrix converters considering also the application as a VSD system is given in [143, 144]. Although there are some strengths of the matrix converters, such as a high power density and low losses, the intrinsic limitations mentioned previously prevent the matrix converter from being used in a general VSD system. Therefore, it is not considered any further in this comparison.

Multilevel Converter

Multi-level converters can be implemented using very different concepts. Here, the expression multilevel converter designates converters having more than three dc-link voltage levels. Two detailed reviews on multilevel converters have been lately presented in [145] and [123]. Basically, they can be separated into the integrated concept and into the modular

concept. With the integrated concept, a multilevel converter is built using a special topology, such as the 4-level or 5-level neutral point clamped converters or multilevel flying capacitor converters. These concepts are known from medium-voltage or even high-voltage applications, where it is necessary to share the dc-link voltage over several devices. The available semiconductors are often not capable to block the whole dc-link voltage, and therefore, a series connection of devices becomes necessary.

There are good reasons to go for this series connection of devices in medium-voltage applications. The first one already mentioned is the technological limit in achievable blocking voltages. Although new semiconductor technologies such as SiC devices can push this limit to higher voltages, these are still in an experimental stage and very expensive. Therefore, the series connection of devices is still the only feasible solution. Additionally, the output voltage quality is enhanced with every additional voltage level. The torque ripple and the losses in the load machine are reduced and less filtering effort is necessary. Very important is also the reduction of the switching losses as only the n^{th} fraction of the total dc-link voltage has to be switched.

As usual, there are also some drawbacks of the integrated multilevel topologies. First, the conduction losses are increased because of the series connection of bipolar devices (such as IGBTs) obtaining a diode-like output characteristics with an inevitable forward voltage drop. This problem cannot completely be solved by increasing the semiconductor chip area as a certain fraction which is independent of the chip area persists. Only unipolar devices (JFETs, MOSFETs) could solve this problem, where the conduction losses can be reduced proportionally with a larger chip area.

For medium-voltage applications, the drawback of the increased conduction losses due to the series connected bipolar devices is outperformed by the gain in voltage handling capability and the directly related gain in power handling capability. Contrary, for low-voltage applications this benefit does not exist. The available devices have sufficient voltage ratings and fast switching speeds, therefore it is not necessary to connect devices in series. An increased output power is achieved with increased phase currents. The conduction losses are an important factor limiting the power range and should be kept as small as possible. Therefore, multilevel topologies based on bipolar devices are generally not suitable for low-voltage applications, with the 3-level

converter being an exception under certain circumstances as it offers a compromise between switching loss reduction and conduction loss increase.

The second basic drawback of integrated multilevel converters is their implicit complexity. The number of semiconductor devices and supplementary circuits increases with every voltage level. The modulation complexity and related computation power increases, especially if all additional tasks such as voltage balancing and emergency concepts under all possible operating conditions are considered. Often the reliability of such topologies decreases due to the larger number of devices and the complexity. The directly related costs make integrated multilevel concepts unattractive for low-voltage VSD applications.

The modular multilevel concept was proposed recently by Marquardt et al. [146, 147] and aims to overcome most of the mentioned drawbacks of the integrated multilevel converters. The basic idea of the modular multilevel converter is to use identical modules for each voltage level. Every module increments the number of voltage levels by one. The complexity is reduced by the introduction of modularity. At the same time, reliability is increased, because the modular concept simplifies the definition of failure modes, maintenance schedules and replacement concepts. Even redundancy can be implemented. Second, the costs are reduced due to the aforementioned effects and due to the modularity itself as identical modules can be used which are subject to economy of scale.

Although being intended for medium-voltage applications, the modular multilevel concept could also be an interesting topology for certain low-voltage applications, such as battery connected converters. In electric vehicles, modern lithium ion battery packs are used for energy storage. These battery packs are made of parallel and series connected battery cells which have already the structure for the modular multilevel concept. A modular multilevel concept based on low-voltage MOSFETs could be used as a highly efficient bidirectional inverter / charging unit. Due to the approximately absent switching losses and the extremely low conduction losses (the MOSFET on-state resistance is approximately proportional to the squared rated blocking voltage [148] but the number of devices in series increases only linearly with the number of levels) a high efficiency converter could be implemented. The cooling effort reduces to minimal passive cooling and all optimization effort could be put into redundancy and reliability. Due to economy of scale effects,

low-voltage MOSFETs are produced in much higher quantities and to a much lower price than i.e. 650 V or 900 V MOSFETs and therefore the costs of such a modular multilevel converter concept are not necessarily higher than that of a simple 2-level inverter with additional battery balancing and charging units.

Concluding, due to the costs and complexity, integrated multilevel concepts are not suitable for low-voltage VSD applications. The analysis of the low-voltage modular multilevel concept is out of scope of this thesis and will not be considered further in this comparison.

3.2 Generic converter loss calculation approach

In order to compare several topologies with each other, the efficiency is an important criterion. It defines the total power losses and the wasted energy, corresponding to a main part of the operational costs of a power electronic converter. Additionally, the cooling effort is related to the total losses. A converter with high losses probably needs an expensive water cooling system, whereas as high efficiency converter can be cooled passively with a simple heat-sink or with additional fans.

The losses occurring in the specific semiconductor devices are an important design criterion as they define together with the thermal model the resulting device junction temperatures. The lifetime of the devices is influenced directly by the maximum junction temperature and also by the temperature cycles, as cyclic mechanical stress is related to the thermal cycling. Additionally, a specific maximum junction temperature should not be exceeded as immediate thermal failure of the semiconductor device is the result.

The 3-level converter topologies presented in Section 3.1 show more than two dc-link voltage levels. A given output voltage space vector can be generated in several alternative ways, i.e. using the nearest three space vectors or by using only the outer space vectors. Additionally, certain voltage space vectors can be generated with multiple switching states, i.e. the zero-voltage space vector can be obtained by connecting either all three phases to the positive (P), to the neutral (0) or to the negative (N) dc-link voltage level. Consequently, losses arise in completely different devices although the same output voltage is generated.

Historically, sinusoidal PWM was first implemented for the modulation of the 2LC. The conduction and the switching losses of the semiconductor devices in the 2LC can be obtained analytically for the carrier-based PWM. Even if the switching losses are minimized using special phase-clamping modulation schemes, the losses can be calculated in a phase-oriented way if the modulation function is adapted accordingly [126]. With the 3-level topologies, the possible alternatives concerning modulation strategies and space vectors, which could i.e. be used for generating the reference output voltage as well as for balancing the dc-link capacitor voltages, increase considerably. Most of these advanced modulation strategies implementing phase-clamping or balancing tasks are defined in a space vector modulation sense and it is often not straight-forward to find an equivalent carrier-based PWM scheme.

Therefore, a generic loss calculation algorithm incorporating the space vector modulation scheme is suggested for the calculation of the device losses and the converter efficiency. The algorithm is based on local averaging of the conduction and the switching losses. Contrary to the conventional carrier-based PWM approach, the losses are calculated for all devices of the topology at once.

In order to determine the losses, the space vector modulation scheme is repeated analytically. For a given topology, each discrete voltage space vector (including alternative and redundant, exchangeable space vectors) defines to which dc-link rail the output phases (a,b,c) are connected. Such a discrete voltage space vector is defined by a triple of switching states (a switching state vector), such as e.g. (PPP) or (NNN) for the two alternative zero-vectors of the 2LC. Together with the sign of the current flowing in the corresponding phase, it is well-defined in which elements of the bridge-leg the losses occur.

It is possible to define a matrix giving the conduction losses of all devices depending on the current space vector $\vec{I} = [i_\mathrm{a}\ i_\mathrm{b}\ i_\mathrm{c}]$ and the actually applied switching state vector $\overrightarrow{SV} = [S_\mathrm{a}\ S_\mathrm{b}\ S_\mathrm{c}]$,

$$P_\mathrm{cond}(\overrightarrow{SV}, \overrightarrow{I}) = \begin{pmatrix} P_\mathrm{c,T1a} & P_\mathrm{c,D1a} & \cdots & P_\mathrm{c,xa} \\ P_\mathrm{c,T1b} & P_\mathrm{c,D1b} & \cdots & P_\mathrm{c,xb} \\ P_\mathrm{c,T1c} & P_\mathrm{c,D1c} & \cdots & P_\mathrm{c,xc} \end{pmatrix}. \tag{3.18}$$

Each element of the matrix is defined as a piecewise function depending on the switching state and the output current sign. As an example, the first two elements of the 2LC (cf. Fig. 3.1) can be written

as

$$P_{\mathrm{c,T1a}} = \begin{cases} P_{\mathrm{cond,T1}}(i_{\mathrm{a}}) & i_{\mathrm{a}} \geq 0 \,\&\, S_{\mathrm{a}} = \mathrm{P} \\ 0 & \text{otherwise} \end{cases} \tag{3.19}$$

$$P_{\mathrm{c,D1a}} = \begin{cases} P_{\mathrm{cond,D1}}(\text{-}i_{\mathrm{a}}) & i_{\mathrm{a}} < 0 \,\&\, S_{\mathrm{a}} = \mathrm{P} \\ 0 & \text{otherwise} \end{cases} . \tag{3.20}$$

The functions $P_{\mathrm{cond,T1}}(i)$ and $P_{\mathrm{cond,D1}}(i)$ are arbitrary functions defining the conduction losses of the IGBT T_1 and the diode D_1, respectively. As a simple approximation, a piecewise linear function

$$P_{\mathrm{cond,T1}}(i) = v_{\mathrm{f,T1}} \cdot i + r_{\mathrm{f,T1}} \cdot i^2 \tag{3.21}$$

could be used.

If necessary, more complex functions can be defined. Because every semiconductor device has its own entry in the conduction loss matrix, it is no problem to introduce different conduction loss functions for different devices, such as with the 3LT²C where 1200 V and 600 V devices are mixed having different conduction loss characteristics.

The space vector modulation strategy defines the sequence of the switching state vectors and their relative on-times depending on the location and the amplitude of the reference output voltage space vector $\overrightarrow{V}$. With this information, the averaged conduction losses over one switching period can be calculated.

As an example, for the 2LC, in sector 1 of the space vector diagram (cf. Fig. 3.15), the output voltage can be formed with the three nearest discrete voltage space vectors, resulting in three different switching state vectors $\overrightarrow{SV_1}$, $\overrightarrow{SV_2}$ and $\overrightarrow{SV_7}$ with the corresponding on-times d_1, d_2 and d_7. The conduction losses averaged over one switching period are given as

$$\begin{aligned} P_{\mathrm{cond,avg}}(\overrightarrow{V}, \overrightarrow{I}) = & d_1 \cdot P_{\mathrm{cond}}(\overrightarrow{SV_1}, \overrightarrow{I}) + d_2 \cdot P_{\mathrm{cond}}(\overrightarrow{SV_2}, \overrightarrow{I}) \\ & + d_7 \cdot P_{\mathrm{cond}}(\overrightarrow{SV_7}, \overrightarrow{I}). \end{aligned} \tag{3.22}$$

It should be noted that the vector sequence as well as the relative on-times are functions of the reference output voltage space vector $\overrightarrow{V}$ and that they are calculated differently for each sector of the space vector diagram. They need to be described also as piecewise functions.

For the calculation of the switching losses, a similar approach is possible. The switching loss energy, occurring in each device of a given topology, is defined by the phase current and the voltage space vector

transition. It is possible to define a switching energy matrix giving the actual losses of all inverter devices depending on the output current space vector and the transition from the old switching state vector $\overrightarrow{SV_\mathrm{o}}$ to the new vector $\overrightarrow{SV_\mathrm{n}}$,

$$E_\mathrm{sw}(\overrightarrow{SV_\mathrm{o}}, \overrightarrow{SV_\mathrm{n}}, \overrightarrow{I}) = \begin{pmatrix} E_\mathrm{s,T1a} & E_\mathrm{s,D1a} & \cdots & E_\mathrm{s,xa} \\ E_\mathrm{s,T1b} & E_\mathrm{s,D1b} & \cdots & E_\mathrm{s,xb} \\ E_\mathrm{s,T1c} & E_\mathrm{s,D1c} & \cdots & E_\mathrm{s,xc} \end{pmatrix}. \tag{3.23}$$

Again each element of this matrix is a piecewise function returning the switching loss energies depending on the switching transition and the output current signs. As an example, the first two elements for the 2LC are given as

$$E_\mathrm{s,T1a} = \begin{cases} E_\mathrm{T1,off}(i_\mathrm{a}) & S_\mathrm{a,o} = \mathrm{P}\ \&\ S_\mathrm{a,n} = \mathrm{N}\ \&\ i_\mathrm{a} \geq 0 \\ E_\mathrm{T1,on}(i_\mathrm{a}) & S_\mathrm{a,o} = \mathrm{N}\ \&\ S_\mathrm{a,n} = \mathrm{P}\ \&\ i_\mathrm{a} \geq 0 \\ 0 & \text{otherwise} \end{cases} \tag{3.24}$$

$$E_\mathrm{s,D1a} = \begin{cases} E_\mathrm{D1,off}(\text{-}i_\mathrm{a}) & S_\mathrm{a,o} = \mathrm{P}\ \&\ S_\mathrm{a,n} = \mathrm{N}\ \&\ i_\mathrm{a} < 0 \\ E_\mathrm{D1,on}(\text{-}i_\mathrm{a}) & S_\mathrm{a,o} = \mathrm{N}\ \&\ S_\mathrm{a,n} = \mathrm{P}\ \&\ i_\mathrm{a} < 0 \\ 0 & \text{otherwise} \end{cases}. \tag{3.25}$$

As an approximation, the switching energies can be scaled linearly with the commutation voltage V_c and the device current i. If necessary, more complex functions for the switching energies can be used. The loss energies are given in the device datasheet, measured at a given commutation voltage V_n and current I_n. As an example, the IGBT turn-off energy depending on the switched current can be written as

$$E_\mathrm{T1,off}(i) = \frac{E_\mathrm{T1,off,n}}{V_\mathrm{n} I_\mathrm{n}} \cdot V_\mathrm{c} \cdot i. \tag{3.26}$$

The space vector sequence defined by the modulation scheme allows for calculating the average switching losses over one switching period. For the 2LC example, in sector 1, the center symmetric space vector sequence ($\overrightarrow{SV_1} - \overrightarrow{SV_2} - \overrightarrow{SV_7} - \overrightarrow{SV_2} - \overrightarrow{SV_1}$) can be used. Therefore, the switching losses averaged over a switching period are given as

$$\begin{aligned} P_\mathrm{sw,avg}(\overrightarrow{V}, \overrightarrow{I}) = & \frac{1}{T_\mathrm{sw}} \cdot \Big(E_\mathrm{sw}(\overrightarrow{SV_1}, \overrightarrow{SV_2}, \overrightarrow{I}) + E_\mathrm{sw}(\overrightarrow{SV_2}, \overrightarrow{SV_7}, \overrightarrow{I}) \\ & + E_\mathrm{sw}(\overrightarrow{SV_7}, \overrightarrow{SV_2}, \overrightarrow{I}) + E_\mathrm{sw}(\overrightarrow{SV_2}, \overrightarrow{SV_1}, \overrightarrow{I}) \Big). \end{aligned} \tag{3.27}$$

Finally, the average conduction and switching loss matrices contain the losses for each device depending on the output voltage, the output current and the modulation strategy. The modulation in terms of the vector sequence and the relative on-times depending on the reference output voltage vector $\vec{V}$ has to be defined. It is sufficient to do that for the first electrical 120° because of the inherent 3-phase symmetry.

As a result of the above calculation the conduction and the switching losses averaged over a switching period are available. The mean losses over a fundamental period in each device can be obtained by integrating the corresponding expressions over the full electric output angle of 360°,

$$\overline{P_{\text{cond}}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} P_{\text{cond,avg}} \cdot d\alpha \tag{3.28}$$

$$\overline{P_{\text{sw}}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} P_{\text{sw,avg}} \cdot d\alpha. \tag{3.29}$$

This framework basically allows to find analytical solutions for the mean conduction and switching losses of a device. Due to the complexity of some space vector modulation schemes, especially for the 3-level topologies, the analytical solutions are hard to derive and are not very useful because of their length. The described algorithm is most useful in a numerical implementation, i.e. using MATLAB.

A useful extension of the algorithm is introducing a temperature feedback in the loss equations. A thermal model is used to calculate the mean junction temperatures of each device depending on the previously calculated losses. The junction temperatures can be used to adjust the conduction and switching loss models. The algorithm is executed iteratively and the device losses and junction temperatures converge to their final values.

3.3 Characteristic loss distribution

Three topologies, namely the 2LC, the 3LNPC² and the 3LT²C, have been selected in Section 3.1 for a deeper comparison as they are considered to be the most competitive topologies for low-voltage VSD applications. In this section, the characteristic distribution of the overall losses to the devices and the efficiency of these three topologies are calculated and analysed in depth.

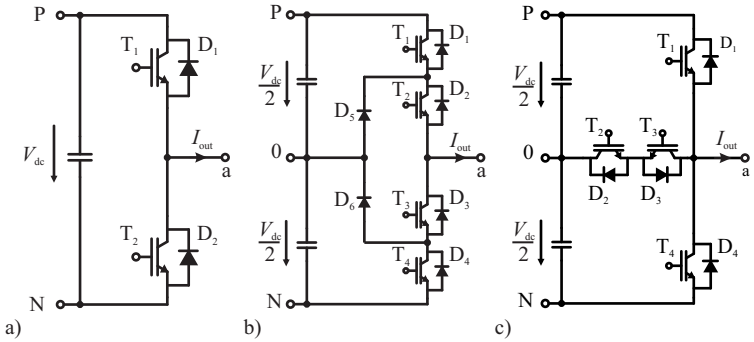

Figure 3.11: Bridge-legs of a) the 2LC, b) the 3LNPC², and c) the 3LT²C.

In a first step, the achievable efficiency of the three topologies for a power rating of $P_0 = 10\,\mathrm{kW}$, a dc-link voltage of $V_{\mathrm{dc}} = 650\,\mathrm{V}$, and for using the same switches is calculated. The operating point is set to an output voltage amplitude of $\hat{V}_1 = 325\,\mathrm{V}$, a current amplitude of $\hat{I}_1 = 20.5\,\mathrm{A}$ and a current to voltage phase displacement angle of $\varphi_1 = 0°$ or $180°$ depending on whether inverter or rectifier operation is considered. Although this comparison is not completely fair, it gives a first insight into the characteristics. A more balanced comparison is given in Section 3.6 where the chip sizes are adapted for each topology.

The Infineon Trench and Field Stop 1200 V IGBT4 and the 600 V IGBT3 series have been chosen as reference devices because of their good documentation and data availability. The 2LC is assumed to be built with Infineon IKW40T120 1200 V, 40 A IGBTs / diodes and the 3LNPC² is built with Infineon IKW50N60T 600 V, 50 A IGBTs / diodes. Unfortunately, no devices with equivalent current rating are available for the two voltage ratings. The 3LT²C is assumed to mix the two switch types mentioned before, so both, IKW40T120 and IKW50N60T, are used.

In order to use the algorithm described in the previous section, the loss models and the modulation schemes have to be specified. For each topology, it has to be determined in which devices conduction losses occur (depending on the switching state) and which devices are subject to switching losses (depending on the switching state transition).

Table 3.3: Conduction losses of the devices in the 2LC.

Switching State	Conduction losses
$I_{\text{out}} \geq 0$	
P	$P_{\text{cond,T1}}$
N	$P_{\text{cond,D2}}$
$I_{\text{out}} < 0$	
P	$P_{\text{cond,D1}}$
N	$P_{\text{cond,T2}}$

Table 3.4: Switching losses of the devices in the 2LC.

Switching Transition	Loss energies
$I_{\text{out}} \geq 0$	
P $\rightarrow$ N	$E_{\text{T1,off}}$, $E_{\text{D2,on}}$
N $\rightarrow$ P	$E_{\text{T1,on}}$, $E_{\text{D2,off}}$
$I_{\text{out}} < 0$	
P $\rightarrow$ N	$E_{\text{D1,off}}$, $E_{\text{T2,on}}$
N $\rightarrow$ P	$E_{\text{D1,on}}$, $E_{\text{T2,off}}$

3.3.1 2-level converter

For the 2LC bridge-leg depicted in Fig. 3.11a, the devices having conduction losses and switching losses are easily identified. The results are summarized in Table 3.3 and Table 3.4 respectively.

The conduction characteristics of the Infineon IKW40T120 1200 V, 40 A IGBTs and diodes have been measured with a test setup for several junction temperatures ($T_{\text{j}} = \{30\,^{\circ}\text{C}, 50\,^{\circ}\text{C}, 80\,^{\circ}\text{C}, 125\,^{\circ}\text{C}\}$) and currents. The self-heating effect of the semiconductors during the measurement is negligible because of the short duration ($T_{\text{p}} < 2\,\text{ms}$) of the applied current pulses. The current dependent conduction loss model was simply constructed with piecewise linear interpolation in between the experimental data points. The measured forward characterisics of the 1200 V IGBT and diode are depicted in Fig. 3.12 for two different junction temperatures. The typical temperature dependency can be observed. The forward voltage decreases and the differential resistance increases with higher junction temperature. In between the temperatures a piecewise linear interpolation is used for the calculation.

The switching energies have been taken from the datasheet values.

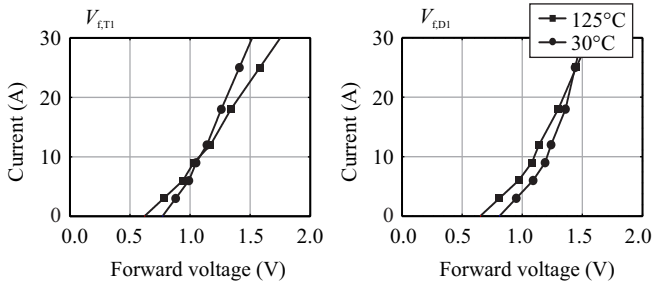

Figure 3.12: Measured forward voltage drop of the 1200 V IGBT and diode for two different junction temperatures.

There, the switching energies for a nominal commutation voltage and a nominal device current are given for two different junction temperatures ($T_\mathrm{j} = \{25\,^\circ\mathrm{C}, 150\,^\circ\mathrm{C}\}$). The switching energies are scaled linearly to the commutation voltage (the dc-link voltage $V_\mathrm{dc} = 650\,\mathrm{V}$) and the device current according to Eq. 3.26. The characteristics in between the measured operating temperatures are calculated using piecewise linear interpolation.

Using these models it is possible to calculate the losses over a fundamental period in each semiconductor device. A simple thermal model (cf. Fig. 3.13) was included in the calculation in order to determine the mean junction temperatures and adapt the loss models. The thermal model consists of a heatsink with forced air cooling ($T_\mathrm{amb} = 40\,^\circ\mathrm{C}$, $R_\mathrm{sa} = 0.12\,\mathrm{K/W}$, corresponding to a cooling system performance index [149] of $\mathrm{CSPI} = 15\,\mathrm{W/(K \cdot dm^3)}$ and a heatsink volume of $V_\mathrm{sink} = 0.55\,\mathrm{dm^3}$), an isolation foil (Bergquist Hi-Flow 300P phase change material, $R_\mathrm{cs} = 0.35\,\mathrm{K/W}$) for each discrete device (TO-247 package) and the thermal resistances of the semiconductors given in the datasheet ($R_\mathrm{jc,T1200V} = 0.45\,\mathrm{K/W}$, $R_\mathrm{jc,D1200V} = 0.81\,\mathrm{K/W}$). The junction temperatures converge to their final value after a few iterations of the loss calculation algorithm.

A modulation scheme with minimum switching loss phase clamping was used for the 2LC (discontinuous PWM, cf. [126]). For the considered cases (inverter and rectifier operation with $\varphi_1 = 0°$ or 180°), a symmetrical clamping in a window $\varphi_\mathrm{v} = -30\,^\circ ... 30\,^\circ$ minimizes the switching losses as the output phase with the momentarily highest current is not switched over an electrical angle of 60°. Fig. 3.14 shows the

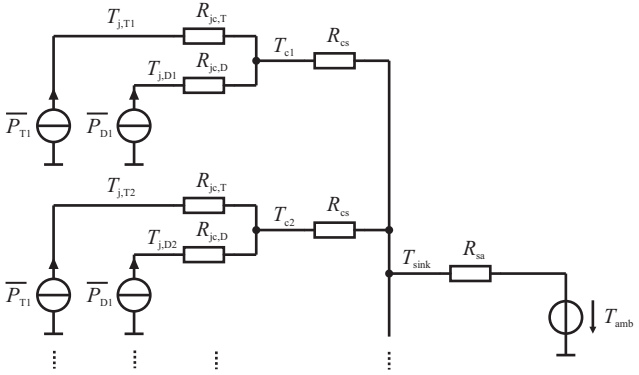

Figure 3.13: Steady-state thermal model used for the calculation of the average device junction temperatures ($T_{\mathrm{amb}} = 40\,^{\circ}\mathrm{C}$).

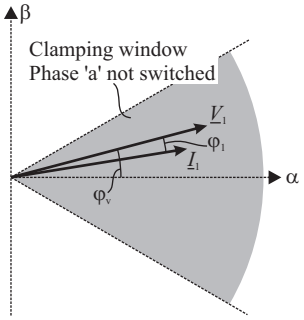

Figure 3.14: Space vector diagram showing the implemented clamping window.

implemented clamping window.

The symmetric clamping scheme is obtained by changing the vector sequence appropriately. In sector 1 of the space vector diagram (cf. Fig. 3.15), the vector sequence is changed at $\varphi_{\mathrm{v}} = 30\,^{\circ}$. The vector sequences obtained are

$$\text{(PNN) - (PPN) - (PPP) - (PPN) - (PNN)}\Big|_{\varphi_{\mathrm{v}}=0^{\circ}\ldots30^{\circ}} \tag{3.30}$$

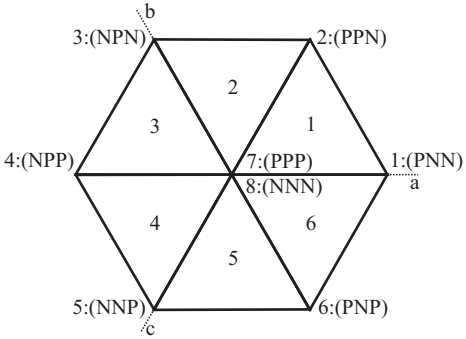

Figure 3.15: Discrete voltage space vectors of the 2LC.

in order to clamp phase a to the positive dc-link rail, and

$$\text{(PPN) - (PNN) - (NNN) - (PNN) - (PPN)}\Big|_{\varphi_\text{v}=30°...60°} \tag{3.31}$$

to clamp phase c to the negative dc-link rail.

The propagation of the switching losses, the conduction losses and the total losses over a fundamental period are depicted in Fig. 3.16 for inverter operation $\varphi_1 = 0\,°$ and a switching frequency of $f_\text{sw} = 16\,\text{kHz}$. The typical reduction of the total losses due to the absence of switching losses over an electrical angle of $60\,°$ can be observed. Compared to continuous modulation, the total switching losses are reduced by 50%. The total conduction losses are only slightly changed due to the different forward characteristics of the IGBTs and diodes (if they are equal, there is no change of the total conduction losses). The clamping window can be adapted to different current to voltage phase displacement angles φ_1 in order to minimize the switching losses. Up to a displacement angle of $\varphi_1 = 30\,°$, sequence 1 (Eq. 3.30) is simply extended to $\varphi_\text{v} = 0°...(30° + \varphi_1)$ and sequence 2 (Eq. 3.31 is reduced to $\varphi_\text{v} = (30° + \varphi_1)...60°$. For higher displacement angles, there are other optimal clamping schemes described in [150].

If these loss curves are averaged over the fundamental period, the mean losses of each semiconductor device are obtained. Together with the thermal model, the mean junction temperatures of the devices can be calculated. Fig. 3.17 shows the average device losses and the junction temperatures for inverter and rectifier operation. The conduction losses are concentrated in the IGBTs for inverter operation and in the

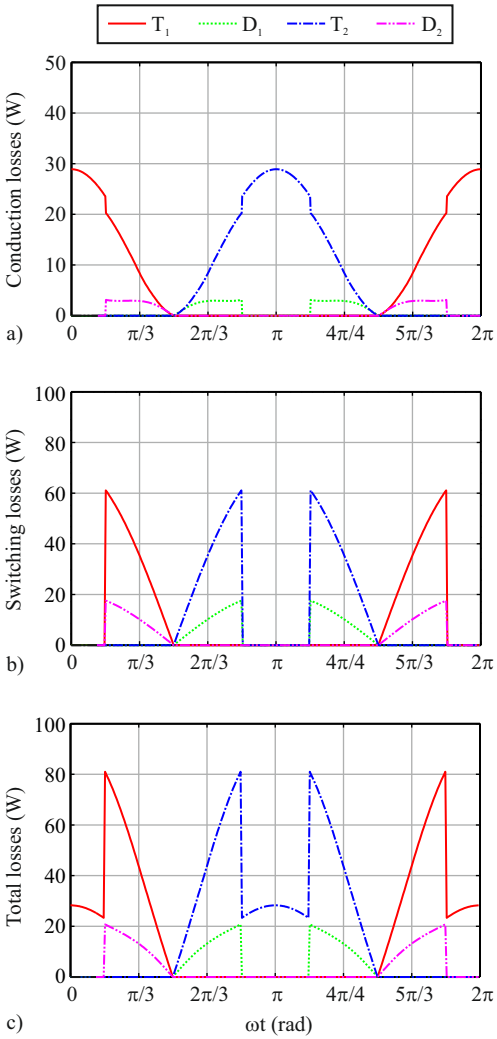

Figure 3.16: Characteristic loss curves of the 2LC for inverter operation ($\varphi_1 = 0\,^\circ$) and a switching frequency of $f_{sw} = 16\,\text{kHz}$. a) conduction losses, b) switching losses and c) total losses.

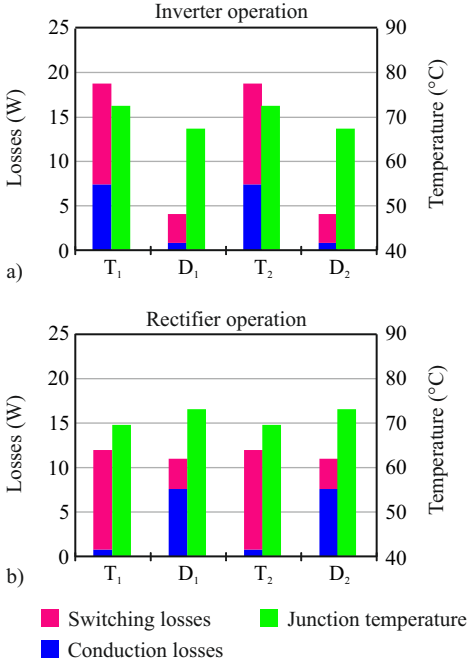

Figure 3.17: Average device losses and corresponding junction temperatures ($T_{\mathrm{amb}} = 40\,^{\circ}\mathrm{C}$) of the 2LC for a) inverter operation ($\varphi_1 = 0\,^{\circ}$) and b) rectifier operation ($\varphi_1 = 180\,^{\circ}$) at a switching frequency of $f_{\mathrm{sw}} = 16\,\mathrm{kHz}$.

diodes for rectifier operation, whereas in both cases, the IGBTs have more switching losses. Due to the smaller chip size of the diode in the package, the thermal resistance is increased and the junction temperature of the diode is higher than the junction temperature of the IGBT, although it still has lower average losses than the IGBT for rectifier operation.

3.3.2 3-level NPC converter

It is more difficult to find the devices having conduction and switching losses for the 3LNPC² bridge-leg depicted in Fig. 3.11b.

The devices having conduction losses can be identified by following the current path for a given switching state. The results are summarized

Table 3.5: Conduction losses of the devices in the 3LNPC².

Switching State	Conduction losses
$I_{\text{out}} \geq 0$	
P	$P_{\text{cond,T1}}$, $P_{\text{cond,T2}}$
0	$P_{\text{cond,D5}}$, $P_{\text{cond,T2}}$
N	$P_{\text{cond,D3}}$, $P_{\text{cond,D4}}$
$I_{\text{out}} < 0$	
P	$P_{\text{cond,D1}}$, $P_{\text{cond,D2}}$
0	$P_{\text{cond,T3}}$, $P_{\text{cond,D6}}$
N	$P_{\text{cond,T3}}$, $P_{\text{cond,T4}}$

Table 3.6: Switching losses of the devices in the 3LNPC².

Switching Transition	Loss energies
$I_{\text{out}} \geq 0$	
P → N	$E_{\text{T1,off}}$, $E_{\text{T2,off}}$, $E_{\text{D3,on}}$, $E_{\text{D4,on}}$
P → 0	$E_{\text{T1,off}}$, $E_{\text{D5,on}}$
N → P	$E_{\text{T1,on}}$, $E_{\text{T2,on}}$, $E_{\text{D3,off}}$, $E_{\text{D4,off}}$
N → 0	$E_{\text{T2,on}}$, $E_{\text{D4,off}}$
0 → P	$E_{\text{T1,on}}$, $E_{\text{D5,off}}$
0 → N	$E_{\text{T2,off}}$, $E_{\text{D4,on}}$
$I_{\text{out}} < 0$	
P → N	$E_{\text{D1,off}}$, $E_{\text{D2,off}}$, $E_{\text{T3,on}}$, $E_{\text{T4,on}}$
P → 0	$E_{\text{D1,off}}$, $E_{\text{T3,on}}$
N → P	$E_{\text{D1,on}}$, $E_{\text{D2,on}}$, $E_{\text{T3,off}}$, $E_{\text{T4,off}}$
N → 0	$E_{\text{T4,off}}$, $E_{\text{D6,on}}$
0 → P	$E_{\text{D1,on}}$, $E_{\text{T3,off}}$
0 → N	$E_{\text{T4,on}}$, $E_{\text{D6,off}}$

in Table 3.5.

The devices having switching losses were determined with measurements on a test setup. Only if a certain device has to block voltage before or after a switching transition, switching losses can occur. If not, the device changes its state under zero voltage switching without any significant losses. Table 3.6 summarizes the switching loss energies depending on the switching transition. The turn-on energy loss of the diodes is very small and can be neglected.

For the comparison of the converter topologies, the conduction char-

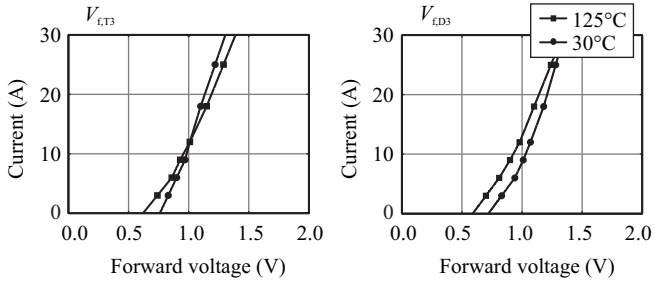

Figure 3.18: Measured forward voltage drop of the 600 V IGBT and diode for two different junction temperatures.

acteristics of the Infineon IKW50N60T 600 V, 50 A IGBTs and diodes have been measured with a test setup. The forward characterisics are depicted in Fig. 3.18 for two different junction temperatures. Equivalently to the 1200 V devices, the conduction loss model is built with piecewise linear interpolation in between the measured data points. Compared to the 1200 V devices, the forward voltage drop for the same current is slightly reduced, especially for higher temperatures.

The switching losses have been obtained from the device datasheet. In order to have the same data basis for the comparison, a linear approximation for the switching loss energy is used again (cf. Eq. 3.26). In between the temperature points, piecewise linear interpolation is used.

The same thermal model is used for the loss calculation as for the 2LC ($R_{\mathrm{sa}} = 0.12\,\mathrm{K/W}$, $R_{\mathrm{cs}} = 0.35\,\mathrm{K/W}$) only the thermal resistances of the semiconductors are slightly different ($R_{\mathrm{jc,T600V}} = 0.45\,\mathrm{K/W}$, $R_{\mathrm{jc,D600V}} = 0.8\,\mathrm{K/W}$). The ambient temperature is set to $T_{\mathrm{amb}} = 40\,^{\circ}\mathrm{C}$.

As for the 2LC, there are switching loss optimal clamping schemes available for the 3-level topologies (cf. [101]). The same symmetric clamping window already depicted in Fig. 3.14 should be implemented, what can be achieved by choosing the appropriate space vector sequences. The space vector diagram of the 3-level topologies is depicted in Fig. 3.19.

In each main sector of the space vector diagram 4 subsectors (E, F, G, H) can be identified. If the output voltage reference space vector is in one of these subsectors, the nearest three discrete space vectors are used for the modulation process. The clamping behaviour is changed by

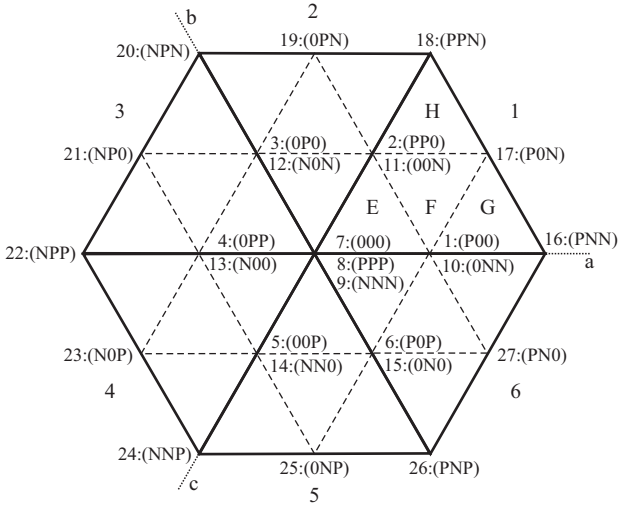

Figure 3.19: Space vector diagram of the 3-level topologies.

choosing the appropriate sequence and additionally changing between the redundant vectors of the inner hexagon. To obtain the symmetric clamping window around $\varphi_\mathrm{v} = -30\,^\circ ... 30\,^\circ$, the vector sequence has to be changed at $\varphi_\mathrm{v} = 30\,^\circ$. The vector sequences obtained in the corresponding subsectors are

$$\begin{aligned}
&\text{E: (P00) - (PP0) - (PPP) - (PP0) - (P00)}\Big|_{\varphi_\mathrm{v}=0^\circ ... 30^\circ}\\
&\text{F: (PP0) - (P00) - (P0N) - (P00) - (PP0)}\Big|_{\varphi_\mathrm{v}=0^\circ ... 30^\circ}\\
&\text{G: (PNN) - (P0N) - (P00) - (P0N) - (PNN)}\Big|_{\varphi_\mathrm{v}=0^\circ ... 30^\circ}\\
&\text{H: (P0N) - (PPN) - (PP0) - (PPN) - (P0N)}\Big|_{\varphi_\mathrm{v}=0^\circ ... 30^\circ}
\end{aligned} \tag{3.32}$$

in order to clamp phase a to the positive dc-link rail, and

$$\begin{aligned}
&\text{E: (00N) - (0NN) - (NNN) - (0NN) - (00N)}\Big|_{\varphi_\text{v}=30°\ldots60°}\\
&\text{F: (0NN) - (00N) - (P0N) - (00N) - (0NN)}\Big|_{\varphi_\text{v}=30°\ldots60°}\\
&\text{G: (P0N) - (PNN) - (0NN) - (PNN) - (P0N)}\Big|_{\varphi_\text{v}=30°\ldots60°}\\
&\text{H: (PPN) - (P0N) - (00N) - (P0N) - (PPN)}\Big|_{\varphi_\text{v}=30°\ldots60°}
\end{aligned} \tag{3.33}$$

to clamp phase c to the negative dc-link rail.

The resulting loss curves of one bridge-leg for the inverter operating point ($\hat{V}_1 = 325\,\text{V}$, $\hat{I}_1 = 20.5\,\text{A}$, $\varphi_1 = 0°$) and a switching frequency of $f_\text{sw} = 16\,\text{kHz}$ are depicted in Fig. 3.20. The switching loss optimal phase clamping strategy avoids switching losses over an electrical angle of 60° for each device (120° in total). However, as can be seen by comparing Fig. 3.20a and Fig. 3.20b, the conduction losses are dominant for the 3LNPC². Therefore, the clamping strategy is more important at higher switching frequencies and a continuous modulation scheme could be used instead.

The mean losses of the semiconductor devices are obtained by averaging the loss curves over the complete fundamental period. The average conduction and switching losses as well as the resulting junction temperatures are depicted in Fig. 3.21a for inverter operation and in Fig. 3.21b for rectifier operation. These two cases are characteristic for the special loss distribution in the 3LNPC².

The loss distribution over the devices is completely different for inverter and rectifier operation. During inverter operation, the losses are concentrated in the IGBTs T_1 - T_4 and in the clamping diodes D_5 and D_6. The remaining diodes D_1 - D_4 do not have losses at all. Still, they have an increased junction temperature because they are in the same TO-247 package as the IGBTs. For rectifier operation, the losses are concentrated in the diodes D_1 - D_4 and the outer IGBTs T_1 and T_4 are not loaded. Therefore, there is a distinct dependency of the loss distribution on the operating point.

Additionally, the switching losses are concentrated only in few components, such as in the outer IGBTs T_1 and T_4 for inverter operation. If all semiconductors have the same current ratings, the junction temperature of these two devices will limit the achievable switching frequency or the output power of the whole converter although the junc-

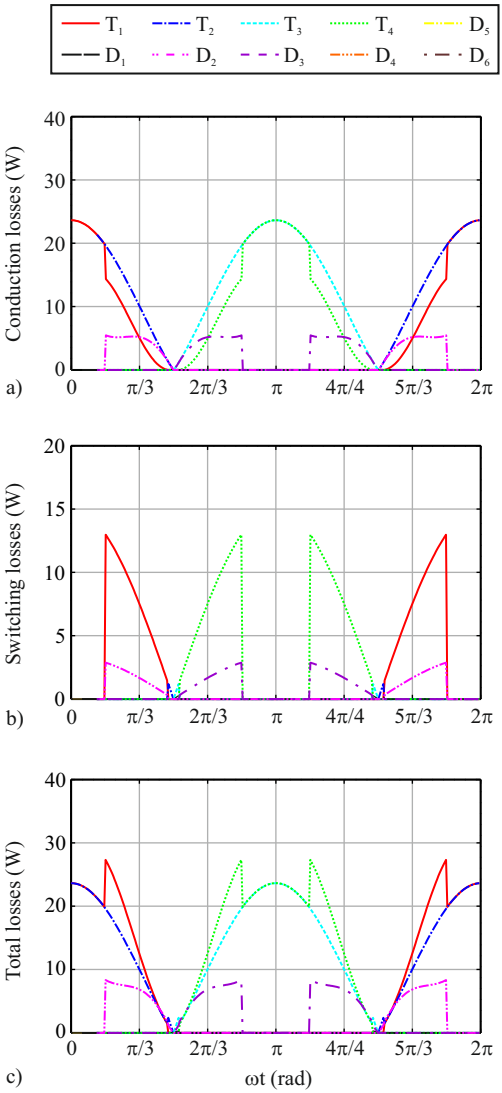

Figure 3.20: Characteristic loss curves of the 3LNPC^2 for inverter operation ($\varphi_1 = 0\,^\circ$) and a switching frequency of $f_{\mathrm{sw}} = 16\,\mathrm{kHz}$. a) conduction losses, b) switching losses and c) total losses.

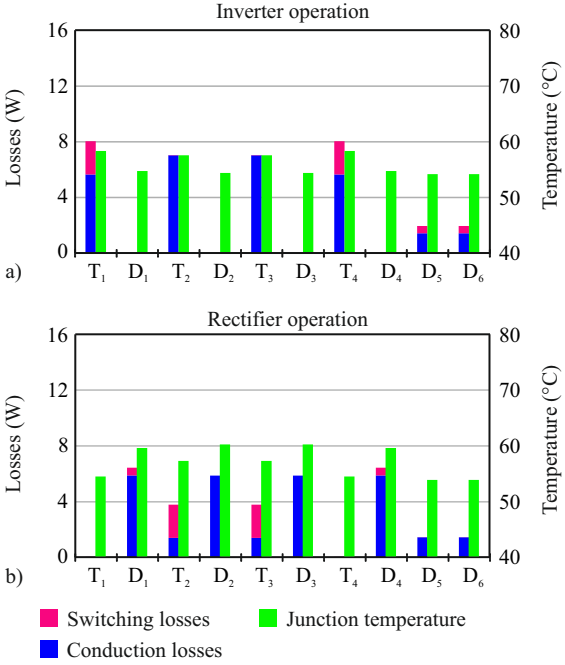

Figure 3.21: Average device losses and corresponding junction temperatures ($T_{\mathrm{amb}} = 40\,^{\circ}\mathrm{C}$) of the 3LNPC² for a) inverter operation ($\varphi_1 = 0\,^{\circ}$) and b) rectifier operation ($\varphi_1 = 180\,^{\circ}$) at a switching frequency of $f_{\mathrm{sw}} = 16\,\mathrm{kHz}$.

tion temperatures of the remaining semiconductors are still far below the maximum. The totally installed rated power of the switches (rated blocking voltage times rated current) is weakly utilized. This uneven distribution of the switching losses was the reason for the introduction of the 3LANPC² (cf. [129]) in medium-voltage applications. The additional switches in parallel to the clamping diodes D_5 and D_6 allow to distribute the switching losses over the IGBTs.

Due to the additional costs, the 3LANPC² is not a feasible solution for low-voltage applications. Anyway, because the switching losses are very low with the considered 600 V devices, the problem of loss concentration in T_1 and T_4 is not that severe. The conduction losses are more important, but these are also heavily dependent on the operating

point.

The distinct dependency of the loss distribution on the operating point could also be an opportunity. Instead of building general purpose bride-leg modules, it is possible to optimize a bridge-leg module for a certain application and reduce costs. For example, a PFC rectifier or a solar inverter operates always in the same operating point (concerning the modulation index and the current to voltage phase displacement angle). Therefore, for a pure inverter module optimized for mass production, the semiconductor chip area of the diodes D_1 - D_4 could be reduced to a minimum. If the module is optimized for rectifier operation, the semiconductor area of the outer IGBTs T_1 and T_4 can be minimized, maintaining the bidirectional power flow at a reduced reverse current. Alternatively, they can be removed completely resulting in one of the implementation variants of the unidirectional Vienna rectifier (cf. [103]).

The characteristic loss distribution of the 2LC (cf. Fig 3.16) is substantially different because there, all semiconductors generate losses in all operating points. The switching losses are always concentrated in the IGBTs, only the conduction losses vary with the operating point.

The idea of having a variable chip area for each device is further considered in the chip area based comparison presented in Section 3.6.

If the average switching losses of the 3LNPC² are further examined, it can be seen that the inner diodes D_2 and D_3 do not have any switching losses at all. A closer look on Table 3.6 reveals that these inner diodes have turn-off losses only for direct transitions between the positive (P) and negative (N) dc-link voltage (or from N to P). Usually, this direct transition is omitted by the standard modulation schemes such as sinusoidal PWM or SVM what explains the absence of switching losses. This effect can be exploited to design a NPC bridge-leg module for very high switching frequencies using SiC Schottky diodes. Instead of replacing all six diodes with SiC counterparts, it is sufficient to replace only D_1, D_4, D_5 and D_6. Still, the complete benefit of the SiC Schottky diodes in terms of switching loss reduction is reached. This not only saves costs as the SiC Schottky diodes are rather expensive, but additionally keeps the conduction losses on a low level. The forward voltage drop of the SiC Schottky diodes is usually increased compared to a Si diode with the same chip area. Therefore, the conduction losses can be reduced if only one SiC Schottky diode is in the current path, especially for rectifier operation.

Table 3.7: Conduction losses of the devices in the 3LT^{2}C.

Switching State	Conduction losses
$I_{\text{out}} \geq 0$	
P	$P_{\text{cond,T1}}$
0	$P_{\text{cond,T2}}$, $P_{\text{cond,D3}}$
N	$P_{\text{cond,D4}}$
$I_{\text{out}} < 0$	
P	$P_{\text{cond,D1}}$
0	$P_{\text{cond,D2}}$, $P_{\text{cond,T3}}$
N	$P_{\text{cond,T4}}$

Considering also the different loss distribution for inverter and rectifier operation, the number of SiC Schottky diodes can further be reduced. A PFC rectifier system can be built with optimized NPC bridge-leg modules where only the two outer diodes D_1 and D_4 are replaced with SiC devices. For a solar inverter bridge-leg module, it is sufficient to replace only the clamping diodes D_5 and D_6 with SiC Schottky diodes. As a part of the IGBT turn-on losses are due to the reverse recovery effect of the commutating diode, also the turn-on losses are reduced.

It has to be mentioned that the benefit of using SiC Schottky diodes is relatively small. The standard 600 V diodes already have a very low reverse recovery charge and therefore, the switching loss reduction with the SiC diodes is limited. Only applications that require highest switching frequencies $f_{\text{sw}} \geq 50\,\text{kHz}$ can justify the application of the expensive SiC diodes.

A prototype of a 3-level NPC back-to-back converter using custom bridge-leg modules with SiC Schottky diodes was built in order to test the performance and is presented in Chapter 6.

3.3.3 3-level T-type converter

Again, the devices in a 3-level T-type bridge-leg (cf. Fig. 3.11c) having conduction and switching losses depending on the switching state and switching transitions must be determined. The devices with conduction losses are easily found by following the current path for every switching state and current direction. The results are summarized in Table 3.7.

Switching losses occur in different semiconductors depending on the

Table 3.8: Switching losses of the devices in the 3LT²C.

Switching Transition	Loss energies
$I_{out} \geq 0$	
P → 0	$E_{\mathrm{T1,off}}$, $E_{\mathrm{D3,on}}$
0 → P	$E_{\mathrm{T1,on}}$, $E_{\mathrm{D3,off}}$
N → 0	$E_{\mathrm{T2,on}}$, $E_{\mathrm{D4,off}}$
0 → N	$E_{\mathrm{T2,off}}$, $E_{\mathrm{D4,on}}$
$I_{out} < 0$	
P → 0	$E_{\mathrm{T3,on}}$, $E_{\mathrm{D1,off}}$
0 → P	$E_{\mathrm{T3,off}}$, $E_{\mathrm{D1,on}}$
N → 0	$E_{\mathrm{T4,off}}$, $E_{\mathrm{D2,on}}$
0 → N	$E_{\mathrm{T4,on}}$, $E_{\mathrm{D2,off}}$

switching transition and the direction of the output current. It is important to analyze the commutation process in detail for every switching transition in order to find for which devices turn-on and turn-off losses or diode reverse recovery losses are occuring. The results are summarized in Table 3.8.

The same conduction loss models presented in the previous sections for the 1200 V devices (cf. Fig. 3.12) and the 600 V devices (cf. Fig. 3.18) were also used for the 3LT²C. Piecewise linear interpolation has been used in between the measurement points and the different junction temperatures.

However, the switching loss models have to be adapted. The 3LT²C is built with mixed semiconductor technology. 600 V IGBTs and diodes are combined with 1200 V IGBTs and diodes. It would be inadequate to assume that the datasheet switching losses with simple scaling to the actual commutation voltage would be accurate enough to determine the switching losses of the 3LT²C. The turn-on switching loss energy of the 1200 V IGBT is lower if the commutating diode is only 600 V rated with considerably lower reverse recovery charge. Furthermore, the current overshoot during turn-on of T_1 is considerably reduced if the commutating diode is 600 V rated (cf. Fig. 3.22a) compared to the case where the commutating diode is rated for 1200 V (cf. Fig. 3.22b). In the same manner the 600 V device turn-on loss energy will be higher if the commutating diode is 1200 V rated.

In order to determine the impact of this special device combination on the switching losses, several switching transients have been recorded

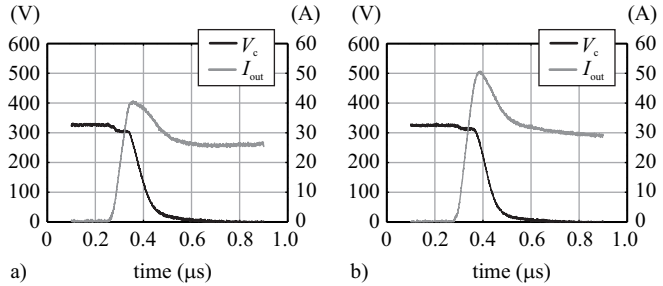

Figure 3.22: Recorded turn-on switching transients of T_1 for $V_c = 325\,V, I_{out} = 25\,A, T_j = 125\,°C$. a) commutating diode rated for 600 V, b) commutating diode rated for 1200 V.

directly at a prototype of the 3LT²C (cf. Chapter 6) over a range of commutation voltages, currents and temperatures. Passive voltage probes and passive AC current transformers directly mounted to the pins of the implemented discrete TO-247 packages enabled an accurate measurement with a minimum influence on the commutation inductance.

Due to the symmetry of the circuit the turn-on and turn-off energies of both 600 V devices are equal under the same conditions (i.e. $E_{T2,on} = E_{T3,on}$, $E_{T2,off} = E_{T3,off}$, $E_{D2,off} = E_{D3,off}$ and $E_{D2,on} = E_{D3,on}$). For the same reason this holds also for the 1200 V devices (i.e. $E_{T1,on} = E_{T4,on}$, $E_{T1,off} = E_{T4,off}$, $E_{D1,off} = E_{D4,off}$ and $E_{D1,on} = E_{D4,on}$).

In Table 3.9 the measured switching loss energies and the deviation from the datasheet values are summarized. It can be seen that the 1200 V IGBT turn-on energy is 24% lower and the 600 V IGBT turn-on energy is 94% higher than the datasheet values. The switching losses will still be lower than for the 2LC because the commutation voltage is only $V_{dc}/2$. The datasheet switching loss energies have been linearly interpolated to a commutation voltage of $V_c = 325\,V$, a phase current of $I_{out} = 25\,A$ and a junction temperature of $T_j = 125\,°C$ for this comparison. The datasheet diode turn-off energy loss was calculated from the given reverse recovery charge. The diode turn-on losses are very small and are usually not given in the datasheet.

The modulation scheme used for the 3LT²C is exactly the same SVM with switching loss optimal clamping already described in Section 3.3.2. No modifications are necessary.

Using the general loss calculation algorithm, the loss curves over

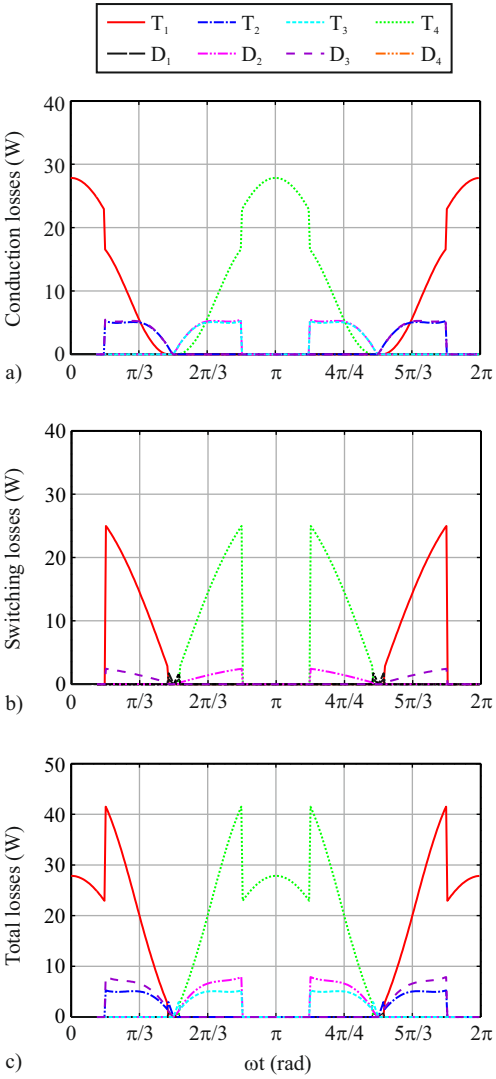

Figure 3.23: Characteristic loss curves of the 3LT^{2}C for inverter operation ($\varphi_1 = 0\,^\circ$) and a switching frequency of $f_{\mathrm{sw}} = 16\,\mathrm{kHz}$. a) conduction losses, b) switching losses and c) total losses.

Table 3.9: Measured switching loss energies for $V_c = 325\,\mathrm{V}$, $I_{out} = 25\,\mathrm{A}$, and $T_j = 125\,^\circ\mathrm{C}$.

Energy	Measurement	Datasheet	Difference
$E_{T1,on}$	1.20 mJ	1.58 mJ	−24 %
$E_{T1,off}$	1.59 mJ	1.68 mJ	−5 %
$E_{D1,on}$	0.17 mJ		
$E_{D1,off}$	1.13 mJ	1.12 mJ	+1 %
$E_{T3,on}$	1.26 mJ	0.65 mJ	+94 %
$E_{T3,off}$	0.72 mJ	0.68 mJ	+6 %
$E_{D3,on}$	0.06 mJ		
$E_{D3,off}$	0.34 mJ	0.41 mJ	−17 %

a fundamental period can be calculated. Conduction losses, switching losses and total losses of the semiconductor devices in a T-type bridge-leg are depicted in Fig. 3.23 for inverter operation ($\hat{V}_1 = 325\,\mathrm{V}$, $\hat{I}_1 = 20.5\,\mathrm{A}$, $\varphi_1 = 0°$, $f_{sw} = 16\,\mathrm{kHz}$). Again, the impact of the switching loss optimal phase clamping strategy on the switching losses can be observed. Differently to the 2LC and the 3LNPC², switching losses and conduction losses are approximately balanced for the considered switching frequency what is already a hint on the superior performance of the 3LT²C.

The averaged device losses and the junction temperatures are shown in Fig. 3.24a for inverter operation and in Fig. 3.24b for rectifier operation.

Again, there is a distinct dependency of the device losses on the operating point. The outer IGBTs T_1 and T_4 have high losses during inverter operation but show no losses for rectifier operation. Contrary, the diodes D_1 and D_4 are only loaded during rectifier operation. This loss distribution profile, directly caused by the 3-level modulation strategy, again allows to optimize a bridge-leg module for a certain operating point.

For inverter operation, the chip area (corresponding to the current rating) of the outer diodes D_1 and D_4 can be minimized. The IGBTs forming the bidirectional switch to the midpoint, T_2 and T_3, have no switching losses but their chip area should not be minimized in order to keep the conduction losses of the series connected devices low.

For pure rectifier operation, the chip area of the outer IGBTs T_1 and T_4 can be minimized. If they are completely removed, the T-type topol-

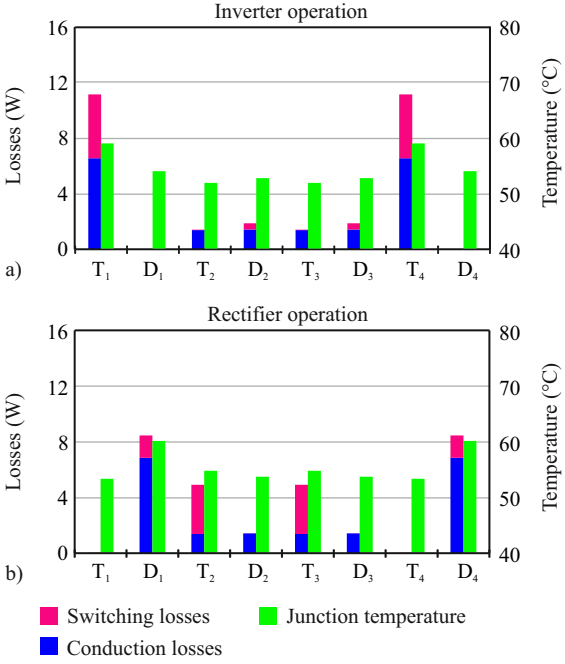

Figure 3.24: Average device losses and corresponding junction temperatures ($T_{\mathrm{amb}} = 40\,^{\circ}\mathrm{C}$) of the 3LT^{2}C for a) inverter operation ($\varphi_1 = 0\,^{\circ}$) and b) rectifier operation ($\varphi_1 = 180\,^{\circ}$) at a switching frequency of $f_{\mathrm{sw}} = 16\,\mathrm{kHz}$.

ogy directly transforms into the unidirectional Vienna rectifier [103].

The junction temperatures of the semiconductor devices are only slightly increased compared to the ambient temperature of $T_{\mathrm{amb}} = 40\,^{\circ}\mathrm{C}$ because the total losses are small and are spread over several devices.

Improving the efficiency of the 3LT^{2}C using SiC Schottky diodes makes only sense for rectifier operation. There, the relatively high reverse recovery charge of the 1200 V diode could be removed with a positive impact on the turn-on energy loss of the 600 V IGBT. The turn-on energy loss of the 600 V IGBT is considerably increased by the reverse recovery charge of the 1200 V diode, what is indicated by the measurements of the switching loss energies (cf. Table 3.9).

Contrary, for inverter operation, replacing the 600 V diodes with SiC Schottky diodes would not reduce the losses much. The reverse recovery charge of the standard 600 V diodes is already small and the turn-on energy loss of the 1200 V IGBT could not be reduced substantially. The increased conduction losses of the SiC Schottky diodes would approximately compensate for the reduced switching losses unless a large SiC semiconductor chip area or a high switching frequency would be used.

Due to the reduced switching losses and the low conduction losses, the total losses of the 3LT²C are very low compared to the 2LC and the 3LNPC². A prototype of the 3LT²C was built in order to test its performance and is presented in Chapter 6. It reached an efficiency of 99% at a switching frequency of $f_{\mathrm{sw}} = 8\,\mathrm{kHz}$ and an output power of $P_0 = 10\,\mathrm{kW}$. Although no expensive SiC devices are used, only 100 W of losses, distributed over several devices were generated. This would even allow for a passive cooling solution.

3.4 Junction temperature ripple and operation at stand-still

An important point for VSD applications is the operation at a very low fundamental frequency or even stand-still operation. This operating point is characterized by a small output voltage (modulation index in the range of $m = 5\%$), a nearly resistive load behaviour ($\varphi_1 = 0°$) and high peak losses in certain semiconductor devices. Instead of the average losses over a fundamental period, the maximum of the device losses occurring at a certain point in the output period determine the reached junction temperatures.

For normal operation with a fundamental frequency of $f_{\mathrm{n}} \geq 10\,\mathrm{Hz}$, the thermal capacitances effectively filter the obtained junction temperature profile in the time-domain. A temperature ripple in the range of approximately $10 - 20\,°\mathrm{C}$ around the mean junction temperature is typically obtained.

The temperature ripple can be calculated or simulated if the transient thermal model of the semiconductor devices is exactly known. The transient thermal model of the Infineon IKW40T120 and IKW50N60T devices is given in the datasheet as a simple cascaded RC-network according to Fig. 3.25.

Due to the lack of information on the transient thermal behaviour

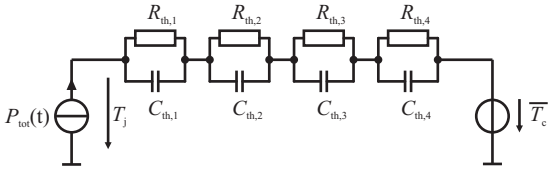

Figure 3.25: Simple transient thermal model.

of the isolation foil used in the steady-state model (a Bergquist Hi-Flow 300P phase-change material), it is assumed that both, isolation foil and heatsink have a very high thermal capacitance and therefore, the case temperature is constant and given by the average case temperature $\overline{T_c}$ obtained with the steady-state thermal model.

The junction temperature can be calculated with

$$T_j(t) = \mathcal{L}^{-1}\left\{\mathcal{L}\left\{P_{tot}(t)\right\} \cdot Z_{th}(s)\right\} + \overline{T_c}. \tag{3.34}$$

The transient thermal impedance is given by

$$\begin{aligned} Z_{th}(s) = &\frac{R_{th,1}}{sR_{th,1}C_{th,1}+1} + \frac{R_{th,2}}{sR_{th,2}C_{th,2}+1} + ... \\ &+ \frac{R_{th,n}}{sR_{th,n}C_{th,n}+1}. \end{aligned} \tag{3.35}$$

Because only the periodic case is of interest, the Fourier transform can be used instead of the Laplace transform in Eq. 3.34. The characteristic device loss curves presented in the previous sections can be processed with the FFT and the inverse FFT to obtain the junction temperature curves.

As an example, the time behavior of the junction temperature of the IGBT T_1 of the 2LC is plotted in Fig. 3.26 for a decreasing fundamental frequency. Down to a frequency of $f_n \approx 10\,\text{Hz}$, the temperature ripple is damped by the thermal capacitances. Reaching stand-still operation, the temperature curve converges to a shape directly related to the profile of the device losses in Fig. 3.16c.

The stand-still operation is the worst-case operating point and can be used as a design constraint for the power level and achievable switching frequency. The reached junction temperatures are even higher than Fig. 3.26 would indicate because the actual case temperature T_c can be higher during stand-still operation than the average case temperature

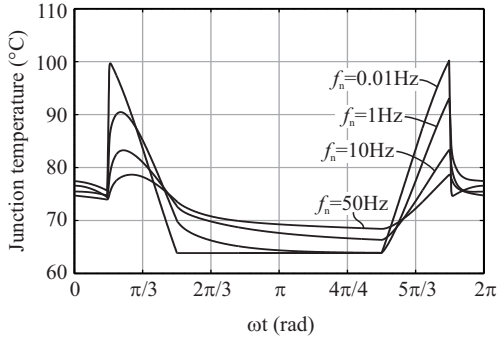

Figure 3.26: Time behavior of the junction temperature in T_1 of the 2LC for inverter operation ($\hat{V}_1 = 325\,\mathrm{V}$, $\hat{I}_1 = 20.5\,\mathrm{A}$, $\varphi_1 = 0°$, $f_{sw} = 16\,\mathrm{kHz}$).

$\overline{T_c}$ assumed for the calculation. In this case, the steady-state thermal model (cf. Fig. 3.13) can be used to find the actual junction temperatures. Then, the power loss sources have their values impressed not by the average losses, but by the losses at a certain point in the output period, determined from the actual loss curves. For a clamping window around $\varphi_v = -30\,°...30\,°$, the critical point is exactly at $\varphi_v = 30\,°$ when the devices start continuous switching again.

To have an upper constraint for the switching frequency at stand-still operation, the maximum switching frequency at a modulation index of $m = 5\,\%$ and an output current amplitude of $\hat{I}_1 = 20.5\,\mathrm{A}$ was determined under the constraint that the maximum junction temperature of $T_{j,max} = 150\,°\mathrm{C}$ is reached by the most stressed device. The steady-state thermal model is sufficient to find the device with the maximum junction temperature.

As a result, the maximum switching frequency at stand-still is restricted to $f_{sw,max} = 21\,\mathrm{kHz}$ for the 2LC, $f_{sw,max} = 58\,\mathrm{kHz}$ for the 3LT²C, and $f_{sw,max} = 90\,\mathrm{kHz}$ for the 3LNPC². These maximum switching frequencies are much lower than the maximum attainable switching frequencies if only the average device losses are considered.

3.5 Efficiency comparison

The framework presented in the previous sections allows to calculate the losses and the converter efficiency of each topology depending on the operating point. In this section, the efficiency of the 3LT²C is compared with the 2LC and the 3LNPC² for the given semiconductor devices (Infineon IKW40T120 and IKW50N60T). A reasonable switching frequency range of $f_{\mathrm{sw}} = 4 - 48\,\mathrm{kHz}$ is chosen for the comparison.

3.5.1 Converter efficiency in nominal operating points

The efficiency of the 3LT²C, the 2LC and the 3LNPC² is depicted in Fig. 3.27a for inverter operation, and in Fig. 3.27b for rectifier operation, respectively.

As loss measurements on the prototypes showed (cf. Chapter 6), there are additional loss components usually neglected in the calculation but getting more important if the converter reaches a high efficiency in the range of 99%. An important additional loss component is due to the contact resistances of the screw clamps ($R_{\mathrm{screw}} = 14.5\,\mathrm{m\Omega}$) implemented in the prototypes. Therefore, this resistance is included in the efficiency calculations for all converters.

The efficiency of the 3LT²C is outstanding for medium switching frequencies from $4 - 30\,\mathrm{kHz}$. The main benefit of the T-type topology comes from the reduced switching losses because the commutation voltage of the 1200 V devices is only 325 V instead of 650 V in the 2LC. Compared to the 3LNPC², the conduction losses are lower because of only two devices being in series in the current path. The difference between inverter operation (cf. Fig. 3.27a) and rectifier operation (cf. Fig. 3.27b) is very small.

If the load is partly inductive such as given for an induction machine, the loss optimal clamping interval can be adapted for all three topologies. Fig. 3.27c shows the achievable efficiencies for a current displacement angle $\varphi_1 = 30\,^\circ$ with a matched clamping interval.

For a switching frequency above 30 kHz, the 3LNPC² is superior. As the efficiency curves of the 3LNPC² and the 3LT²C are very flat, the switching frequency at which both topologies have equal efficiencies is very sensitive to variations of the semiconductor properties such as conduction and switching losses. If the dc-link voltage is increased, the

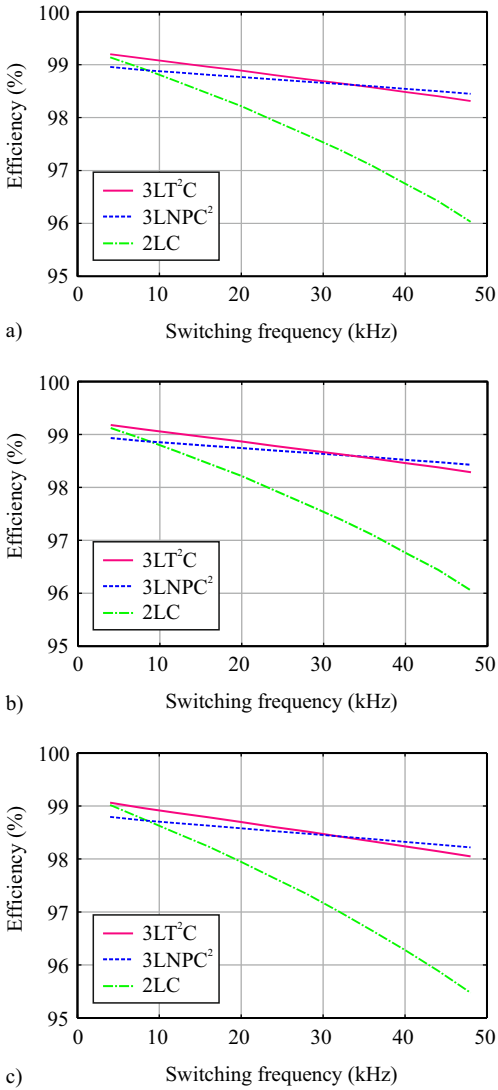

Figure 3.27: Comparison of calculated efficiencies for $S_{\text{out}} = 10\,\text{kVA}$, $\hat{V}_1 = 325\,\text{V}$, $\hat{I}_1 = 20.5\,\text{A}$. a) inverter operation with $\varphi_1 = 0°$, b) rectifier operation with $\varphi_1 = 180°$, c) inverter operation with load machine ($\varphi_1 = 30°$).

cross-over point is at a lower switching frequency because the switching losses of the T-type topology become more important.

The application area of the 3LNPC² is limited to special applications, where exceptionally high switching frequencies are necessary and where the increased costs due to the number of necessary semiconductors and gate drive units can be justified. For all other low-voltage applications the 3LT²C is the better choice if efficiency and costs are important. Naturally, for medium-voltage applications the 3LNPC² has its advantages and cannot be replaced by the 3LT²C.

3.5.2 Converter efficiency over the complete operating range

Considering the back-to-back converter configuration usually implemented for a VSD system, the rectifier stage is working in a well defined operating point. As it performs PFC operation, the modulation index and the current to voltage phase displacement angle are approximately constant, only the current amplitude is changing with the active power delivered to the output.

Contrary, the inverter stage has to work in a broad range of operating points, directly defined by the motor terminal values. In order to give an initial insight into the dependency of the converter efficiency on the operating point, defined as output voltage $\hat{V}_1$, output current $\hat{I}_1$ and current to voltage phase displacement angle φ_1, the converter efficiency is plotted over these three parameters.

A fixed clamping window around $\varphi_\mathrm{v} = 0\,°...60\,°$ is implemented what fits better the current to voltage displacement angle that is typical for an induction machine. The switching frequency is set to $f_\mathrm{sw} = 16\,\mathrm{kHz}$. The reachable efficiency is depicted in Fig. 3.28 for the three considered topologies. The efficiency is increasing with the output voltage (cf. Fig. 3.28a) because the output power is increased without changing conduction or switching losses significantly. The efficiency is decreasing with a higher output current because the ohmic component of the conduction losses quadratically increases with the output current (cf. Fig. 3.28b). Finally, the efficiency is decreasing with a higher current to voltage displacement angle, mainly due to the lower active output power (cf. Fig. 3.28c). The curves are similar for all three topologies, the basic characteristics are maintained.

Knowing the dependency of the converter efficiency on the operating

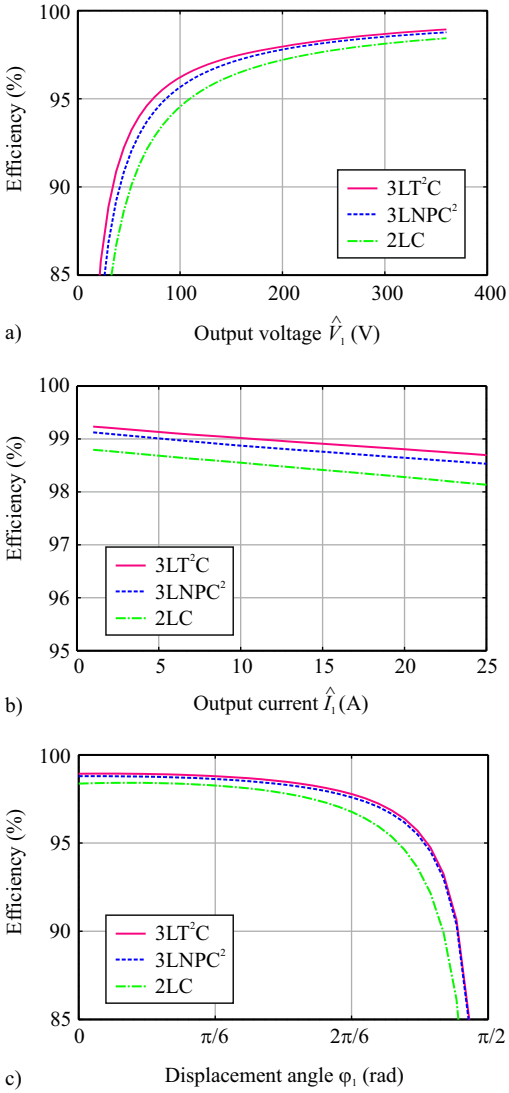

Figure 3.28: a) Converter efficiency over output voltage for $\hat{I}_1 = 20.5\,\mathrm{A}$, $\varphi_1 = 30°$, b) converter efficiency over output current for $\hat{V}_1 = 325\,\mathrm{V}$, $\varphi_1 = 30°$, c) converter efficiency over current to voltage phase displacement angle with $\hat{V}_1 = 325\,\mathrm{V}$, $\hat{I}_1 = 20.5\,\mathrm{A}$.

point is important for the determination of the total system efficiency and the influence of energy saving machine control algorithms. These algorithms change the machine's terminal behaviour and therefore have an impact on the converter efficiency as well what is further analyzed in Chapter 5.

3.6 Semiconductor chip area optimization

In Section 3.3 it was shown that the loss distribution over the individual semiconductor devices can be very uneven depending on the operating point if 3-level topologies are considered.

It is therefore advisable to reduce the chip sizes of the semiconductor chips with low power losses. Nowadays, the chip sizes in modules are over-dimensioned because they are designed as general purpose modules which could work in any operating point. Although this is a feasible way to design semiconductor modules for the output stage of a VSD converter, there are different applications where it is not necessary to have spare semiconductor chip area. E.g. solar inverter or active rectifier modules always work with nearly constant modulation index and phase lag. The fundamental frequency is fixed to 50 or 60 Hz so only the mean chip losses are important and no peak power losses due to electrical stand-still could occur. The same arguments hold for the rectifier stage of a VSD converter. Although optimizing the input stage modules for pure rectifier operation would make a bidirectional converter operation impossible, it is still feasible to restrict the regenerative breaking capability of the converter to e.g. $P_{\mathrm{break}} = 0.2 \cdot P_{\mathrm{n}}$ and the semiconductor chip area can be reduced to a certain point. If a manufacturer takes the decision for a converter topology as a mass product, it should account for the possibility to produce a module optimized for the application in order to reduce the semiconductor costs. Naturally, this makes only sense for fairly high product volume and if the converter failure modes are well defined. For many applications, pulse-current capability has to be guaranteed or failure currents have to be conducted during a certain time period what increases the necessary semiconductor area for all considered topologies.

The following chip area optimization has to be clearly understood as an optimization for the mentioned operating points, no reserves for fault cases are included.

The main idea is to adapt the chip sizes for each topology so that

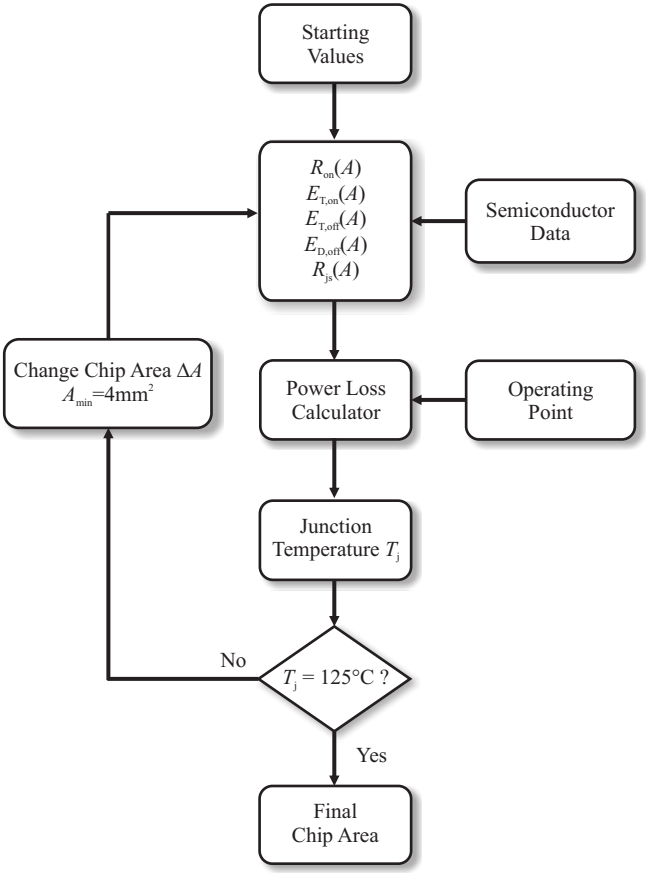

Figure 3.29: Diagram of the chip area optimization algorithm.

the junction temperature of each element reaches a mean value of $T_\mathrm{j} = 125\,^\circ\mathrm{C}$. Accordingly, the chip area for elements with low losses will be decreased and the area of elements with high losses will be increased. In order to perform this chip size optimization, the conduction loss model, the switching loss model, and the thermal model have to be adapted with the semiconductor chip area A. A flow-chart of the adaptation algorithm is depicted in Fig. 3.29.

The chip area of each element is limited to a minimum of $A_\mathrm{min} =$

Table 3.10: Parameters of the chip area dependent loss models.

Conduction loss model		
Device x	$V_{\mathrm{f,x}}$	$k_{\mathrm{c,x}}$
$T_{1200\mathrm{V}}$	0.8 V	$1.29\,\Omega\mathrm{mm}^2$
$D_{1200\mathrm{V}}$	0.8 V	$0.55\,\Omega\mathrm{mm}^2$
$T_{600\mathrm{V}}$	0.8 V	$0.52\,\Omega\mathrm{mm}^2$
$D_{600\mathrm{V}}$	0.8 V	$0.24\,\Omega\mathrm{mm}^2$
Switching loss model		
Transient y	m_{y}	q_{y}
$T_{\mathrm{on,1200V}}$	$-0.562\,\mathrm{nJ/(VAmm^2)}$	213 nJ/(VA)
$T_{\mathrm{off,1200V}}$	$-0.519\,\mathrm{nJ/(VAmm^2)}$	237 nJ/(VA)
$D_{\mathrm{off,1200V}}$	$-1.93\,\mathrm{nJ/(VAmm^2)}$	174 nJ/(VA)
$T_{\mathrm{on,600V}}$	$0.895\,\mathrm{nJ/(VAmm^2)}$	52.9 nJ/(VA)
$T_{\mathrm{off,600V}}$	$0.566\,\mathrm{nJ/(VAmm^2)}$	69.3 nJ/(VA)
$D_{\mathrm{off,600V}}$	$0.022\,\mathrm{nJ/(VAmm^2)}$	41.8 nJ/(VA)
$T^*_{\mathrm{on,1200V}}$	$-0.562\,\mathrm{nJ/(VAmm^2)}$	162 nJ/(VA)
$T^*_{\mathrm{on,600V}}$	$0.895\,\mathrm{nJ/(VAmm^2)}$	103 nJ/(VA)

$4\,\mathrm{mm}^2$. This is due to unmodeled side effects becoming dominant for small chip sizes and due to the limits of the bonding technology.

3.6.1 Chip area based loss modelling

The semiconductor loss models have to be adapted to account for a variable chip size. The approach is based on [151], where a semiconductor area based comparison of an indirect matrix converter, a current source converter and a 2-level voltage source converter is presented.

The chip areas of several devices from the Infineon Trench and Field Stop 1200 V IGBT4 and the 600 V IGBT3 series have been determined and linked to the conduction characteristics specified in the datasheets. The conduction characteristics can be approximated with a simple model consisting of a forward voltage drop V_{f} which is independent of the chip area and a differential resistance $R_{\mathrm{on}}(A)$ which is inversely proportional to the chip area A. Consequently, the conduction losses $P_{\mathrm{c,x}}$ of each device x can be modeled as

$$P_{\mathrm{c,x}}(A, i) = V_{\mathrm{f,x}} \cdot i + k_{\mathrm{c,x}} \cdot \frac{1}{A} \cdot i^2. \tag{3.36}$$

The parameters $V_{\mathrm{f,x}}$ and $k_{\mathrm{c,x}}$ are given in Table 3.10.

Similarly to the conduction losses, also the switching losses are adapted with the chip area. The datasheet values with the proposed gate resistors are linearly scaled to the same switched current and the same commutation voltage. The switching loss energies E_{y} for the relevant switching transients y (IGBT turn-on, IGBT turn-off and diode turn-off) of each device are approximated with simple linear models given by

$$E_{\mathrm{y}}(A, v, i) = (m_{\mathrm{y}} \cdot A + q_{\mathrm{y}}) \cdot v \cdot i. \tag{3.37}$$

The parameters m_{y} and q_{y} are given in Table 3.10. The constant part q_{y}, which is independent of the chip area A, is dominating for the considered chip sizes. In general, the switching loss energies scaled to the same current and the same commutation voltage do not vary much with the chip area A if IGBTs are considered.

For the T-type topology, the fitted switching loss energy curves have been simply shifted to the points determined with the test setup. As described in Section 3.3.3, it is assumed that only the turn-on switching transients $T^*_{\mathrm{on,1200V}}$ and $T^*_{\mathrm{on,600V}}$ are influenced by the combination of different switch types in the 3LT²C.

Finally, the thermal model was adapted and simplified. The same thermal behaviour for all chip types is assumed and according to [151], the thermal resistance is given by

$$R_{\mathrm{th,js}}(A) = 23.94 \, \frac{\mathrm{K}}{\mathrm{Wmm^2}} \cdot A^{-0.88}. \tag{3.38}$$

The heat sink is assumed to have a constant temperature of $T_{sink} = 80\,^{\circ}\mathrm{C}$. The junction temperature of each device can be calculated with

$$T_{\mathrm{j}} = T_{\mathrm{sink}} + R_{\mathrm{th,js}}(A) \cdot P_{\mathrm{tot}}(A). \tag{3.39}$$

The thermal and the loss models are all linear and very simple. As the main goal of this chip area comparison is not to give precise predictions of the achievable efficiencies but a relative comparison of the semiconductor effort of the considered converter topologies, the accuracy of the models is sufficient. The basic findings will not change significantly if more accurate models are used.

3.6.2 Chip area optimization results

The optimization algorithm calculates the losses for each topology and adapts the chip sizes until each element reaches a junction tempera-

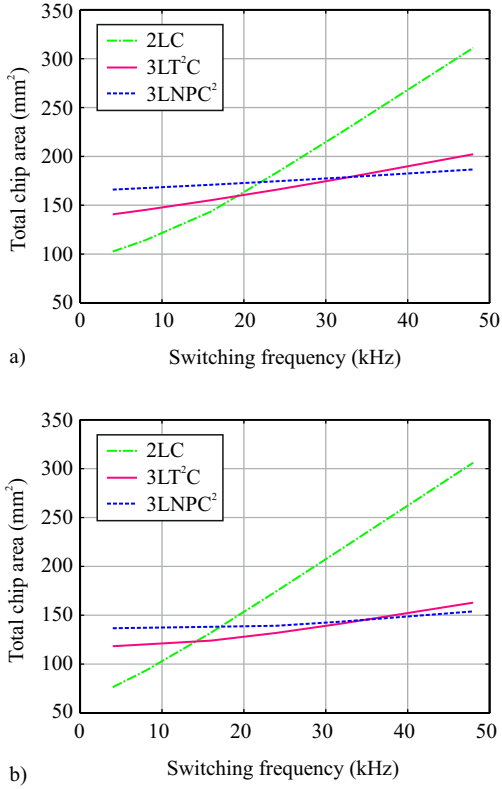

Figure 3.30: Comparison of the total semiconductor area depending on the switching frequency. a) inverter operation with $\hat{V}_1 = 325\,\mathrm{V}$, $\hat{I}_1 = 20.5\,\mathrm{A}$, $\varphi_1 = 0°$, b) rectifier operation with $\varphi_1 = 180°$.

ture of $T_\mathrm{j} = 125\,°\mathrm{C}$. This process also affects the total losses and the converter efficiency. Interestingly, the efficiency decreases only slightly because the chip area is reduced only for elements with low losses, and therefore, the absolute loss increase is very small.

If all chip sizes are summed up, the total chip area for a topology and the corresponding operating point is found. The total chip area is directly related to the costs of a power module.

The calculation results are depicted in Fig. 3.30. The total chip area is calculated for the three different topologies depending on the

switching frequency.

Surprisingly, the total chip area of the 3LT²C is lower than for the 2LC already for a switching frequency above 14 kHz in rectifier operation (cf. Fig. 3.30b). The increase of the area with the switching frequency is the lowest for the 3LNPC² because of the small switching losses. At a switching frequency of 48 kHz, the necessary chip area for the 2LC is nearly twice the area of the 3LNPC². A similar dependency for the total chip area can be observed for inverter operation (cf. Fig. 3.30a) although the chip area allocation to the different devices changes.

With Fig. 3.30, the general belief that a 3-level topology would need more silicon chip area than a corresponding 2-level topology is disproved. The part count and the count for external circuitry such as gate drives and isolated voltages is increased but the total chip area can be even lower for high switching frequencies. This finding shifts the converter comparison in favour of the 3-level converters as the semiconductor costs have to be reconsidered.

3.7 Dc-link voltage balancing and switching loss optimal clamping

Whereas there is no need to balance the dc-link voltage for the 2LC, balancing of the dc-link voltage is a central issue for the 3-level topologies. Over the last decades, several publications have been dealing with this topic ([152–157], to mention only a few). In this section, the contradicting requirements of switching loss optimal clamping strategies and dc-link voltage balancing strategies are briefly reconsidered. The possibilities arising from the back-to-back configuration are discussed and the constraints are highlighted.

The efficiency calculations presented in the previous sections were based on a switching loss optimal clamping strategy (cf. Section 3.3.2 and [101]), a so-called discontinuous modulation scheme. Although this modulation scheme can reduce the switching losses considerably, there is a negative impact on the balance of the dc-link voltages.

The shift of the dc-link voltages is determined by the current flowing into the mid-point formed by the series connection of the capacitors. Examining the 3-level space vector diagram, not all of the space-vectors have an impact on the neutral potential. Only the space vectors on the

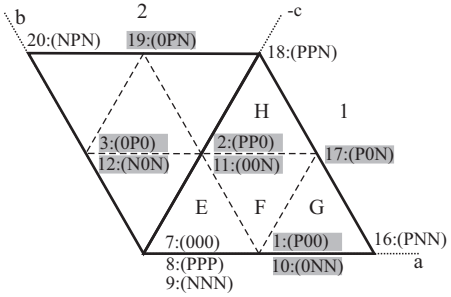

Figure 3.31: Voltage space vectors which have an impact on the current flowing into the dc-link mid-point.

inner hexagon (where always two redundant switching states can be used to form a voltage space vector) and the middle vectors on the outer hexagon result in a current flowing into the neutral point (cf. the shaded vectors in Fig. 3.31).

The redundant vectors on the inner hexagon result in inverse directions of the mid-point current and therefore allow to actively control the average current flowing into the neutral point within a switching cycle and accordingly allow to control the neutral point voltage.

Differently, the middle vectors on the outer hexagon lead to an uncontrollable mid-point current. This uncontrollable part of the mid-point current is depending on the modulation index, the output current amplitude and the current to voltage phase displacement angle.

Now, the switching loss optimal clamping scheme determines which of the space vectors are used and what vector sequence is applied. Unfortunately, it also determines which of the redundant vectors are used and therefore, the degree of freedom normally used to balance the dc-link voltages falls away. There is a single exception to this principle. If the modulation index is $m \leq 0.5$, only the space vectors of the inner hexagon are used. In this case, it is possible to obtain switching loss optimal clamping and dc-link voltage balancing at the same time. In the space vector diagram, the output voltage vector would be located in subsector E in this case. It is possible to define 4 different vector

sequences as

$$\begin{aligned}
&\mathrm{E_{a+}}\text{: (P00) - (PP0) - (PPP) - (PP0) - (P00)}\Big|_{\varphi_\mathrm{v}=0°\ldots30°}\\
&\mathrm{E_{a-}}\text{: (0NN) - (00N) - (000) - (00N) - (0NN)}\Big|_{\varphi_\mathrm{v}=0°\ldots30°}\\
&\mathrm{E_{c+}}\text{: (PP0) - (P00) - (000) - (P00) - (PP0)}\Big|_{\varphi_\mathrm{v}=30°\ldots60°}\\
&\mathrm{E_{c-}}\text{: (00N) - (0NN) - (NNN) - (0NN) - (00N)}\Big|_{\varphi_\mathrm{v}=30°\ldots60°}
\end{aligned} \tag{3.40}$$

Obviously, both sequences $\mathrm{E_{a+}}$ and $\mathrm{E_{a-}}$ don't switch phase a (it is clamped to (P) or (0)), but they lead to an opposite current into the dc-link midpoint. Similarly, the sequences $\mathrm{E_{c+}}$ and $\mathrm{E_{c-}}$ don't switch phase c (it is clamped to (0) or (N)), but result in a different current into the dc-link midpoint.

The average value over a switching cycle of the current flowing into the dc-link midpoint can be calculated with the power balance. For the sequences $\mathrm{E_{a+}}$ and $\mathrm{E_{c+}}$, only the upper capacitor is used for the modulation cycle. The average active power over a switching period has to come from the upper capacitor only and the mid-point current is calculated as

$$i_\mathrm{mid} = \frac{3}{2}\frac{\hat{V}_1\hat{I}_1\cos(\varphi_1)}{V_\mathrm{dc}/2}. \tag{3.41}$$

For inverter operation, the upper capacitor would be discharged and the lower capacitor would be charged as the input stage controls the total dc-link voltage to be constant. The other two sequences, $\mathrm{E_{a-}}$ and $\mathrm{E_{c-}}$, only use the lower capacitor over the modulation cycle. The average active output power is delivered by the lower capacitor and therefore, the mid-point current is given as

$$i_\mathrm{mid} = -\frac{3}{2}\frac{\hat{V}_1\hat{I}_1\cos(\varphi_1)}{V_\mathrm{dc}/2}. \tag{3.42}$$

As can be seen, the appropriate phases can be clamped and still, the mid-point current is completely controllable. In VSD applications, this feature can be used to balance the dc-link voltages during low-frequency or even stand-still operation where the modulation index is small ($m \leq 0.5$). The rectifier stage is operated with the switching loss optimal clamping scheme and the inverter stage is used to balance the

dc-link voltage by changing the sequences accordingly, e.g. with a hysteresis controller depending on the unbalance of the capacitor voltages. Naturally, the transition between the two sequences introduces additional switching transitions, but much less than the normal switching transitions due to the switching frequency itself.

If the modulation index is $m > 0.5$, the controllability of the dc-link voltages is restricted and it is basically not possible to obtain switching loss optimal phase clamping and balancing action at the same time. The medium vectors on the outer hexagon introduce an uncontrollable part of the mid-point current. Additionally, if the sequences are chosen such that the switching losses are minimized, also the redundant vectors on the inner hexagon cannot be chosen freely any more. Therefore, it is advisable to distribute the dc-link balancing task between the rectifier stage and the inverter stage.

The analysis in [154] showed that the uncontrollable part of the mid-point current is mainly due to the reactive current component (in a synchronous voltage oriented reference frame designated as i_q). The higher the modulation index is, the more important this uncontrollable mid-point current gets. It leads to a periodic mid-point current with three times the fundamental frequency having zero average value. The part of the mid-point current which could be influenced by choosing the redundant vectors of the inner hexagon is mainly due to the active current component (designated as i_d).

Therefore, in a back-to-back converter the balancing task during normal operation (the modulation index of the inverter stage is $m > 0.5$) is preferably done by the rectifier stage whereas the inverter stage is operated with a switching loss optimal clamping scheme. As the rectifier stage performs PFC operation, the reactive current component is small. Therefore, the mid-point current can effectively be controlled by choosing the appropriate redundant middle vectors.

If the rectifier stage operates with unity power factor and with a modulation index $m > 0.5$, the sequences

$$\begin{aligned}
&\mathrm{F}_+\text{: (PP0) - (P00) - (P0N) - (P00) - (PP0)}\Big|_{\varphi_\mathrm{v}=0°\ldots60°}\\
&\mathrm{G}_+\text{: (PNN) - (P0N) - (P00) - (P0N) - (PNN)}\Big|_{\varphi_\mathrm{v}=0°\ldots30°}\\
&\mathrm{H}_+\text{: (P0N) - (PPN) - (PP0) - (PPN) - (P0N)}\Big|_{\varphi_\mathrm{v}=30°\ldots60°}
\end{aligned} \tag{3.43}$$

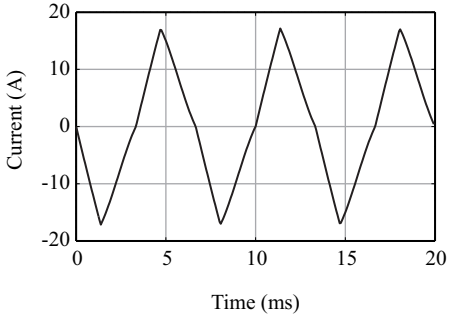

Figure 3.32: Local average current flowing into the dc-link mid-point for pure reactive output power ($f_\mathrm{n} = 50\,\mathrm{Hz}$).

charge the upper capacitor. Contrary, the sequences

$$\begin{aligned}
&\text{F_: (0NN) - (00N) - (P0N) - (00N) - (0NN)}\Big|_{\varphi_\mathrm{v}=0°\ldots60°}\\
&\text{G_: (P0N) - (PNN) - (0NN) - (PNN) - (P0N)}\Big|_{\varphi_\mathrm{v}=0°\ldots30°}\\
&\text{H_: (PPN) - (P0N) - (00N) - (P0N) - (PPN)}\Big|_{\varphi_\mathrm{v}=30°\ldots60°}
\end{aligned} \tag{3.44}$$

charge the lower capacitor. As can be seen, if the lower capacitor has to be charged, phase a is necessarily switched also during $\varphi_\mathrm{v} = 0°...30°$ where the current in phase a is the highest. Similarly, if the upper capacitor has to be charged, phase c is always switched.

The worst case concerning the variation of the mid-point voltage is obtained if the converter only supplies reactive power to the load, such as during no-load operation of an induction machine. The current at the rectifier stage is nearly zero. Therefore, the rectifier stage can not counteract the voltage unbalance. Additionally, even using the redundant vectors of the inverter stage is not sufficient to counteract the voltage ripple if the modulation index is high and the uncontrollable part of the mid-point current dominates [154]. This condition can be used as worst-case design constraint for the size of the dc-link capacitors. The mid-point current produced by the inverter stage for a purely inductive current of 20.5 A (corresponding to $S_\mathrm{out} = 10\,\mathrm{kVA}$) is depicted

in Fig. 3.32. The necessary dc-link capacitance can be calculated with

$$C_{\mathrm{dc,min}} = \frac{\int_0^{T_\mathrm{n}/6} i_\mathrm{mid}\, dt}{2 \cdot \Delta V_\mathrm{dc,max}}. \tag{3.45}$$

Assuming the peak-to-peak neutral point voltage ripple is restricted to $\Delta V_\mathrm{dc,max} = 0.1 \cdot V_\mathrm{dc}$, the necessary capacitance becomes $C_\mathrm{dc,min} = 220\,\mu\mathrm{F}$. The dc-link capacitance can be reduced even more if the reactive power capability of the converter is restricted. The magnetization current of an induction machine is much less than its rated current. For the 7.5 kW induction machine used in this work, the magnetization current is only $\hat{I}_\mathrm{m} = 6.1\,\mathrm{A}$ and the minimum dc-link capacitance could be reduced to $66\,\mu\mathrm{F}$.

The variation of the neutral point voltage by such large values ($\Delta V_\mathrm{dc,max} = 65\,\mathrm{V}$) has a direct impact on the modulated output voltage space vector. It is necessary to compensate the relative on-times of the space vectors used in a modulation cycle. A space vector modulation with feedforward compensation of the unbalanced dc-link voltages was presented in [115]. Using this modification, the output voltage vector can be modulated correctly although the dc-link voltages are unbalanced.

Summarizing, in a back-to-back converter configuration, the voltage balancing task is carried out by the rectifier stage during normal operation ($m > 0.5$). This implies that switching loss optimal clamping is possible only for the inverter stage. Therefore, the switching losses of the rectifier stage are slightly increased.

It has to be mentioned that the balancing task using the previously described sequences still leads to a discontinuous PWM scheme but it does not necessarily clamp the phase with the highest current. Whereas the switching loss optimal clamping scheme reduces the switching losses by 50%, the discontinuous balancing scheme can reduce the switching losses in the worst case only by 13.3% (if always the phase with the lowest current is clamped) compared to continuous modulation. At the sector boundaries and during the change of the balancing sequence, additional switching losses are introduced. These can be neglected for the rather high switching frequencies ($f_\mathrm{sw} \geq 4\,\mathrm{kHz}$) used for low-voltage applications as they contribute only a small part to the total switching losses.

If the modulation index is small ($m \leq 0.5$), such as for low-speed or stand-still operation, the balancing task is preferably carried out by

the inverter stage. In this case, it is possible to operate the rectifier stage and the inverter stage with switching loss optimal clamping, and to perform dc-link balancing at the same time.

Chapter 4

Grid Interface

A modern VSD system is equipped with an active grid interface, usually performing PFC operation. Passive input filters are necessary to attenuate conducted electromagnetic emissions in the high frequency range and to comply with regulatory standards. For low-voltage applications, the achieved switching frequencies and current control bandwidths are high enough to impress sinusoidal currents with low distortions. Therefore, the classic current and voltage THD requirements are easy to fulfill, but the EMI standards become more important.

In this thesis, efficiency and performance of a low-voltage VSD system are analyzed and optimized in a holistic way. Not only the machine and the power electronic converter, but also the passive components used in the EMI filter are sources of power losses. Although the absolute value of the losses in the EMI filter is small compared to the losses in the machine and the converter, they are not less important. The losses of the components are a limiting factor for the minimum component size and weight, indirectly related to the costs of a passive component. As the cost pressure is very high, the filter components should be as cheap as possible. Additionally, the total converter volume and weight are important criteria in many applications where the available space or the allowed weight is limited, such as for automotive or aircraft applications.

A holistic system comparison has to include these aspects. The necessary filter attenuation, and therefore the component values, volume, costs and losses are influenced by several factors.

On the one hand, the converter topology itself determines the EMI

disturbance level. 3-level converters switch only half of the dc-link voltage and directly reduce the noise level compared to conventional 2-level topologies. Also the switching frequency has a direct impact on the noise level, the necessary attenuation and the losses in the components.

On the other hand, intelligent control algorithms can be used to reduce the damping effort. Traditionally, EMI filter topologies are built using LC-filter stages with additional passive damping branches which considerably increase the total filter volume. New control concepts, such as active damping, can be used to remove the passive damping branches completely. However, in this case it has to be considered, that the damping action is then only available for system operation. In case damping is required also for the turn-off state, passive damping means have to be provided.

Whereas conventional converter and EMI filter designs rely on high boost inductances and high dc-link capacitances, these quantities can be reduced considerably in a optimized system. Directly related is a reduction of energy storage and a reduction of passive high frequency damping that is characteristic for large passive components. Therefore, it is often necessary to increase the switching frequency and the control bandwidths (i.e. the dc-link voltage regulation bandwidth) in order to have a satisfactory system performance. As a secondary effect of these measures, stability issues may arise which are most often no problem in conventional designs.

In this chapter, the active grid interface of a low-voltage VSD system is analyzed in detail. First, the impact of the converter topology on the necessary filter component values and losses is analyzed. This is performed on a simple, comparative level.

Second, the stability theory of 3-phase systems is summarized as unconventional combinations of filter component values and converter control concepts could lead to system instability. The stability theory using subsystem impedance matrices in the synchronous reference frame is presented which allows to assess the impact of active damping measures and to identify stability issues in a similar way as it is done for DC systems. The virtual impedance concept and related damping possibilities are presented as they allow to remove passive damping branches. A simple measurement system for impedance matrices in synchronous coordinates is built in order to show the impact of active damping measures on the converter input impedance and to verify the theoretical models.

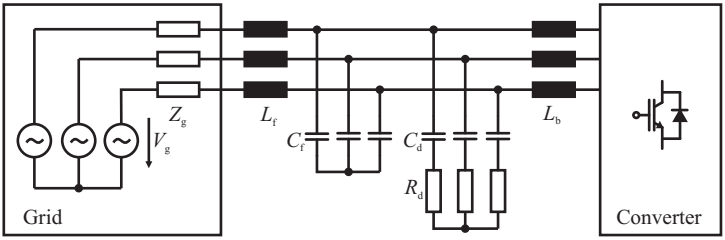

Figure 4.1: Sample system consisting of a weak source, LCL EMI filter and PFC rectifier.

4.1 EMI filter loss comparison

The aim of this section is to show the impact of the converter topology on the values and losses of the filter components on a comparative base. Accurate loss calculation of magnetic components under the special excitation present in PFC rectifiers (fundamental frequency sinusoidal current and a high frequency ripple) requires a detailed knowledge of the loss characteristics of the magnetic material. The values given in the manufacturers datasheets are usually insufficient for this case and only allow a rough estimation of the losses. Better results are achieved with sophisticated methods such as the "Improved Improved Generalized Steinmetz Equation (i²GSE)" [158] combined with experimentally determined loss maps [159]. A comparative evaluation is preferred, based on theoretical scaling laws of the inductor volumes and losses.

4.1.1 Filter topology

The comparison is based on the LCL filter topology depicted in Fig. 4.1. There are several possibilities how to design such a filter structure. Depending on the regulatory standards that have to be fulfilled, either current or voltage THD limitations or directly the distortion level in the high frequency conducted emissions band (such as CISPR Class A or Class B) define the required attenuation.

In practice, there are additional constraints and considerations that guide the selection of the filter components. Due to several reasons, the current ripple in the boost inductor L_b is usually limited to a fixed fraction of the fundamental current amplitude, such as $\Delta i_\mathrm{pp} = 0.2 \cdot \hat{I}_\mathrm{n}$. One reason is that it simplifies the sampling process of the current. If

SVM with switching loss optimal clamping and synchronous sampling is used, the sampling point is either on a rising current slope or on a falling slope, changing with the modulation sectors. Due to the conversion time of the ADC, a proportional current offset is visible in the sampled signals, changing at the sector boundaries. This distortion is getting higher with increasing current slope and therefore with the current ripple. A second reason are additional losses in the semiconductors and in the boost inductor itself.

A further reason why to choose a rather high boost inductance is related to stability issues. A high boost inductance leads to a high input impedance of the rectifier in the high frequency range what is beneficial for a stable converter operation.

If the value of the boost inductance is fixed, the remaining components (the filter capacitor C_f and the filter inductance L_f) are chosen such that the required attenuation is achieved. Again, there are further considerations that guide the selection of the components. Whereas the resonance frequency of the two components is given by the required attenuation, there is still a degree of freedom as one of the components can be chosen freely. A constraint limiting the value of the filter capacitors is the consumed reactive power. Although a bidirectional rectifier stage can compensate the reactive power of the capacitors completely, this leads to an increased current and therefore increased switching and conduction losses in the semiconductors. On the other side, the capacitance should be high enough to have a small voltage ripple.

In conventional filter designs, an additional passive damping branch ($C_\mathrm{d}, R_\mathrm{d}$) is placed, e.g. in parallel to the filter capacitance. This damping branch can be designed with the rule of optimal damping [160]. The damping branch limits the resonance peak of the LC filter stage in order to improve the stability margin.

Concerning the losses of the filter components, the inductive components are clearly dominant. The capacitors are usually built with foil capacitors having negligible losses. Only in the damping resistors some losses arise, mainly due to the capacitive current of the RC damping branch. In a properly designed damping branch, these losses are usually small compared to the losses in the inductive components and are neglected.

In order to simplify the comparison, the following design rule is applied. The boost inductance should be chosen such that the peak-to-peak current ripple is equal for the 2-level and the 3-level topologies.

If the boost inductance is designed in such a way, the remaining components of the EMI filter are not affected, as the necessary attenuation is equal for both topologies if the same regulatory standards should be fulfilled and the current ripple is equal. Therefore, the comparison is limited to the value, the volume and the losses of the boost inductor.

4.1.2 Boost inductance

In order to design the boost inductor, most often a maximum peak-to-peak current ripple $\Delta i_{\mathrm{pp,max}}$ relative to the current fundamental amplitude for rated power is specified. The location of the current ripple maximum is depending on the relation between the dc-link voltage and the phase voltage amplitude and also depends on the implemented modulation scheme. While it is simple to find the maximum current ripple for the 2-level topology, it is more involved for the 3-level topology, especially if space vector modulation with loss optimal clamping scheme is considered.

The current ripple in the boost inductors can be derived by considering the applied voltages over the boost inductance as depicted in Fig. 4.2. If the space vectors are split into their fundamental and harmonic components, the equation for the current is given with

$$L_{\mathrm{b}} \cdot \frac{d}{dt}(\underline{i}_{1,(1)} + \underline{i}_{1,\mathrm{h}}) = \underline{V}_{1,(1)} + \underline{V}_{1,\mathrm{h}} - \underline{V}_{\mathrm{g},(1)}. \tag{4.1}$$

Here, $\underline{V}_{\mathrm{g},(1)}$ denotes the grid voltage space vector, $\underline{V}_{1,(1)}$ is the fundamental and $\underline{V}_{1,\mathrm{h}}$ the harmonic content of the converter output voltage and $\underline{i}_{1,(1)}$ is the fundamental and $\underline{i}_{1,\mathrm{h}}$ the harmonic content of the current space vector. The current ripple is defined by the harmonic content according to

$$L_{\mathrm{b}} \cdot \frac{d}{dt}\underline{i}_{1,\mathrm{h}} = \underline{V}_{1,\mathrm{h}} = \underline{V}_{1} - \underline{V}_{1,(1)}. \tag{4.2}$$

It can be seen that the current ripple is driven by the difference between the applied discrete converter output voltage space vectors and the fundamental component. During a modulation cycle, the three closest voltage space vectors are used to generate the required fundamental component of the converter output voltage space vector. Considering the position of $\underline{V}_{1,(1)}$ depicted in Fig. 4.2, the space vector sequence

$$\mathrm{V}_1 - \mathrm{V}_2 - \mathrm{V}_0 - \mathrm{V}_2 - \mathrm{V}_1 \tag{4.3}$$

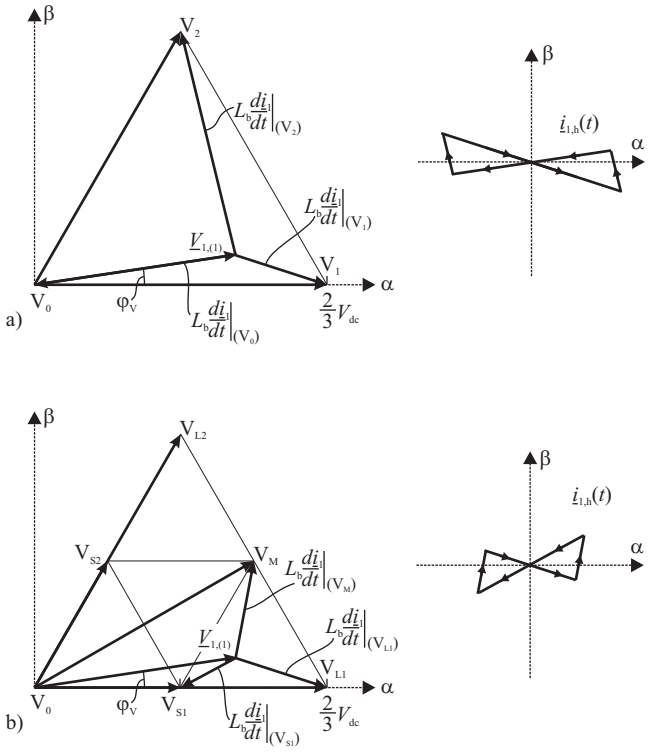

Figure 4.2: Space vector diagrams for a) 2-level and b) 3-level modulation. The diagram of the current ripple $\underline{i}_{1,\mathrm{h}}(t)$ can be constructed by considering the applied voltages over the boost inductance.

is applied for 2-level modulation and the space vector sequence

$$\mathrm{V_{L1}} - \mathrm{V_M} - \mathrm{V_{S1}} - \mathrm{V_M} - \mathrm{V_{L1}} \tag{4.4}$$

is applied for 3-level modulation. The trajectory of the current ripple, i.e. of $\underline{i}_{1,\mathrm{h}}(t)$ can therefore be constructed with the turn-on times of the corresponding voltage space vectors.

The current ripple can be found by projecting the current ripple

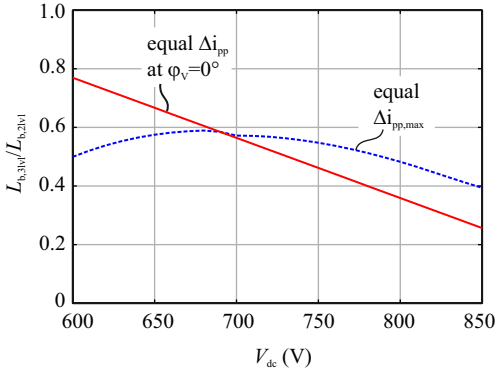

Figure 4.3: Reduction of the required boost inductance when changing from a 2-level topology to a 3-level topology if an equal current ripple has to be achieved.

diagram on the 3 single phases (a,b,c) using the following equations,

$$i_{1,\mathrm{h},a}(t) = i_{1,\mathrm{h},\alpha}(t) \tag{4.5}$$

$$i_{1,\mathrm{h},b}(t) = -\frac{1}{2} i_{1,\mathrm{h},\alpha}(t) + \frac{\sqrt{3}}{2} i_{1,\mathrm{h},\beta}(t) \tag{4.6}$$

$$i_{1,\mathrm{h},c}(t) = -\frac{1}{2} i_{1,\mathrm{h},\alpha}(t) - \frac{\sqrt{3}}{2} i_{1,\mathrm{h},\beta}(t). \tag{4.7}$$

The maximum of the current ripple $\Delta i_{\mathrm{pp,max}}$ is found by sweeping the electrical angle of the output voltage space vector φ_{V} over $0° - 60°$ and taking the maximum ripple value of the three phases. As the system is completely symmetrical, it is sufficient to consider only the first 60°. The location of the maximum is dependent on the relationship between V_{dc} and $\hat{V}_1$ and can be found nummerically.

Alternatively, the current ripple Δi_{pp} at the peak of the fundamental current is considered instead of the maximum current ripple $\Delta i_{\mathrm{pp,max}}$. This can be justified because the boost inductors are often designed near to the limit of saturation and already show a certain drop of the inductance (e.g. -20%) at the peak of the fundamental current. The inductor is then specified to have the required inductance at the peak current and often shows an increased inductance at a lower current.

For PFC operation and a sufficiently small boost inductance, the current space vector can be assumed to be approximately in phase with

the converter output voltage space vector. Therefore, the current ripple at the peak of the fundamental current occurs at an electrical angle of the output voltage space vector of $\varphi_\mathrm{V} = 0°$. The required inductances for a given Δi_pp can be calculated with Eq. 4.8 for a 2-level topology and with Eq. 4.9 for a 3-level topology respectively,

$$L_\mathrm{b,2lvl} = \frac{1}{f_\mathrm{sw}} d_\mathrm{V1on,2lvl} \frac{2/3 V_\mathrm{dc} - \hat{V}_1}{\Delta i_\mathrm{pp}} \tag{4.8}$$

$$L_\mathrm{b,3lvl} = \frac{1}{f_\mathrm{sw}} d_\mathrm{VL1on,3lvl} \frac{2/3 V_\mathrm{dc} - \hat{V}_1}{\Delta i_\mathrm{pp}}. \tag{4.9}$$

The parameter $d_\mathrm{V1on,2lvl}$ specifies the relative on-time of the active voltage space vector V_1 (cf. Fig. 4.2a) whereas $d_\mathrm{VL1on,3lvl}$ specifies the relative on-time of the active voltage space vector V_L1 (cf. Fig. 4.2b). Due to the 3-level modulation, $d_\mathrm{VL1on,3lvl}$ is smaller than $d_\mathrm{V1on,2lvl}$. If the same peak-to-peak current ripple is allowed at $\varphi_\mathrm{V} = 0°$ for the 2-level and the 3-level topology, the reduction of the boost inductance can be calculated directly as

$$\frac{L_\mathrm{b,3lvl}}{L_\mathrm{b,2lvl}} = \frac{d_\mathrm{VL1on,3lvl}}{d_\mathrm{V1on,2lvl}} = \frac{2M \sin(\pi/3) - 1}{M \cos(\pi/6)} = \frac{2}{3} \cdot \frac{3\hat{V}_1 - V_\mathrm{dc}}{\hat{V}_1}. \tag{4.10}$$

For $V_\mathrm{dc} = 650\,\mathrm{V}$ and $\hat{V}_1 = 325\,\mathrm{V}$ the ratio is given with

$$\frac{L_\mathrm{b,3lvl}}{L_\mathrm{b,2lvl}} = 66\%. \tag{4.11}$$

For a given output voltage fundamental amplitude $\hat{V}_1$, the achievable reduction of the inductance is dependent on the dc-link voltage as depicted in Fig. 4.3. There, also the achievable reduction of the boost inductance for an equal maximum peak-to-peak current ripple $\Delta i_\mathrm{pp,max}$ is shown.

4.1.3 Component volumes and losses

As already mentioned, only the boost inductance changes if the guideline of equal current ripple is applied for the different converter topologies. Therefore, the only difference in the EMI filter component volume and losses is due to the different boost inductors.

The inductor volume for a thermally limited design for a given core material theoretically scales linearly with the inductance [161] and with

the square of the peak current. As the peak current does not change, the inductor volume can be reduced by the same amount,

$$V_{\mathrm{Lb,3lvl}} = 0.66 \cdot V_{\mathrm{Lb,2lvl}}. \tag{4.12}$$

The losses of inductive components are rather difficult to calculate accurately. There are also no good approximations such as with the induction machine, where the iron losses usually are dominant for high switching frequencies. This is not necessarily true for inductive components as there are many different materials such as powder cores with low specific losses.

Therefore, again the thermally limited inductor design described in [161] is considered. The losses can increase only proportional to the inductor surface. As the inductance scales with the volume, the losses are related to the inductance by

$$P_{\mathrm{L}} \propto L^{2/3}. \tag{4.13}$$

Accordingly, the relative reduction of the inductor losses can be calculated with Eq. 4.14.

$$\frac{P_{\mathrm{loss,Lb,3lvl}}}{P_{\mathrm{loss,Lb,2lvl}}} = \left(\frac{L_{\mathrm{b,3lvl}}}{L_{\mathrm{b,2lvl}}}\right)^{2/3} = 0.66^{2/3} = 0.76 \tag{4.14}$$

The losses in the boost inductors can be reduced approximately by 25% when changing from a 2-level topology to a 3-level topology. Again, the loss reduction is increased for a higher dc-link voltage, i.e. a loss reduction of 33% can be achieved for $V_{\mathrm{dc}} = 700\,\mathrm{V}$. This values are only true if the same core material is used.

In summary, the choice of the converter topology has only a limited impact on the volume and losses of the EMI filter. Mainly the boost inductance is changed, the remaining components stay the same. The only degree of freedom left is choosing the switching frequency. As it has an impact on both, the converter losses and the losses in the boost inductors, an optimal switching frequency leading to minimum system losses can be identified. This is further considered in Chapter 5.

4.2 Stability of power electronic systems

The combination of the active rectifier with the EMI input filter can lead to an unstable system if the resonance peaks of the filter are not

properly damped. Mathematical tools are necessary to determine the stability margins and the origin of negative interactions. A further reason to analyze the converter stability is the implementation of active damping algorithms that allow to eliminate the passive damping branch of the input filter. The damping performance of these algorithms can be studied with the tools developed for stability studies.

4.2.1 Literature review

A short literature review on the stability of power electronic systems is given in this section. It is a starting point for the further analysis of active damping measures that can be used instead of the passive damping branch of the EMI input filter.

Stability studies of power electronic converters were initially conducted for DC-DC converters with line input filters [162]. It was observed that the converter can become unstable if connected to the line input filter, although it is working correctly if the line filter is left away. As such converters control the output voltage to be constant, they have a constant power sink behavior for low frequencies. This specific behavior leads to a negative differential input impedance at the input terminals of the converter which is able to amplify resonances of the line filter [163].

Following this observation, the well-known analysis tool of state-space averaging [160] was introduced to derive an analytical model of the switching converter. This model is valid for frequencies below the switching frequency as it relies on the values averaged over a switching period. Subsequently, the model is linearized around the operating point and a small-signal model is obtained, suitable for the stability analysis with methods known from linear, time-invariant (LTI) system theory.

There are basically two different methods to determine the closed-loop stability of the combination of the converter with the input filter. With the first method, the filter can be included into the system equations and a closed-loop state-space model of high order is obtained. The system is small-signal stable if the state matrix has no eigenvalues in the right half plane of the $\underline{s}$ domain. With a parameter sweep, the eigenvalue loci can be observed and stability limits can be defined. This method can be extended to analyze the stability of systems where multiple converters are interconnected [164, 165]. All converter models,

interconnections and passive elements are incorporated into a single state-space matrix and an eigenvalue analysis shows the stability limits of the system.

The second method is based on the analysis and comparison of the open-loop behaviour of the interconnected subsystems, in this simple case the line input filter and the dc-dc converter. It is known as Middlebrook's impedance criterion [162], where the small-signal output impedance of the filter Z_{out} and the small-signal input impedance Z_{in} of the converter are compared. The impedance criterion is derived from the Nyquist plot of the transfer functions of the two subsystems. In the Nyquist plot, the loop gain $Z_{\text{out}}/Z_{\text{in}}$ is plotted in the complex plane and the encirclements of the critical point -1 are observed. The system is stable if the critical point is not encircled, assuming the involved subsystems are open-loop stable.

Now it is possible to introduce criteria based on the comparison of the two impedances. They restrict the allowed region of the Nyquist plot. All of the impedance criteria are sufficient, but not necessary for stability, what means that the system can still be stable although the criterion is not fulfilled. The unity circle criterion restricts the loop gain to be less than one, accordingly

$$|Z_{\text{out}}| < |Z_{\text{in}}| \quad \forall\omega. \tag{4.15}$$

The unity circle criterion is of conservative nature because it excludes most of the Nyquist plane. Middlebrook's impedance criterion ($|Z_{\text{out}}| << |Z_{\text{in}}|$) is even more conservative, as it introduces a gain margin to get a very stable and well damped system.

In order to reduce the conservatism, not only the modulus of the impedances but also the phase information has to be considered [166–168]. This can be done by introducing a gain margin and a phase margin such that the loop gain is allowed to be in an extended region of the Nyquist plane.

Both methods, the analysis of the closed-loop state matrix and the analysis of the subsystem impedances have its strengths and weaknesses. The advantage of the impedance based comparison is the possibility to measure the subsystem impedances. Design issues leading to an unstable closed-loop system, such as undamped filter resonances or wrong controller gains can be identified by inspecting the impedance plots. Consequently, conflicts can be resolved by introducing damping branches or tuning the controller gains, what finally leads to an

impedance shaping process. The impedance criterion can be used to examine the stability of several paralleled converters connected to a single bus [166, 169]. It is also possible to extend the impedance criterion to microgrids containing several interconnected converters, but the impedance criterion has to be applied to every single connection interface to guarantee stability of the complete system [170, 171].

Therefore, in case of large interconnected microgrids with several converters, the analysis of the closed-loop state matrix is preferred [164, 165]. There, often simplified large-signal models are used and also small-signal techniques can be applied.

The stability analysis of power electronic AC-DC converters is much more elaborate, especially in the case of single-phase AC systems. A review on the topic is given in [172].

Stability problems with active PFC rectifiers were reported in [173, 174]. If they are connected to transformers with high series inductance, subharmonic oscillations of the voltage and complete instability was observed. Again, the problem was identified to result from the constant power sink behaviour of the rectifier at low frequencies.

The main problem arising with the stability analysis of single-phase AC systems is the periodic, time-varying nature of the systems. It basically prohibits the application of LTI system theory, as there is no constant operating point which can be used for linearization and a subsequent small-signal analysis. Initially, it was tried to overcome these difficulties with reduced order models which are valid only in certain frequency ranges.

For dynamics below the fundamental frequency, only the envelopes of the AC signals are considered, and all other dynamics are neglected [174–177]. This approach leads to simple reduced-order models suitable for stability analysis. These models are obtained by averaging over the fundamental period and are only valid for frequencies below the fundamental frequency. The obtained envelope impedances [173, 178] describe the response of the converter to an amplitude modulated input signal and should not be interpreted as conventional impedances as this might lead to wrong conclusions [179].

For dynamics above the fundamental frequency, again simplified reduced-order models have been proposed [180]. The main problem in this frequency range is finding an appropriate operating point for the system linearization. Often a set of points on the AC input voltage is chosen for linearization and small-signal stability is shown for all

these points.

These models are valid only in certain frequency ranges and were not able to explain all stability issues in single-phase systems in a satisfactory way. Therefore, sophisticated methods have been proposed over the last years in order to develop small-signal converter models that are valid over the complete frequency range.

The first method is called harmonic linearization [181,182]. A small-signal model is developed by adding a small perturbation to the fundamental input voltage. Subsequently, the current response at the perturbation frequency is measured or calculated. This requires to carry out all frequency convolutions to the dc side and back to the ac side of the converter. The approach is also possible with diode rectifiers [183]. Although the resulting small-signal impedance is conform to the impedance definition and valid over the complete frequency range, it is not able to describe the constant power sink behaviour of PFC converters in the low frequency range. This behaviour is clearly coupled to an amplitude modulation process, also known from three-phase power systems where the amplitude modulation is one of the natural physical origins of oscillations between generators and loads. Active PFC rectifiers control the dc-link voltage by adjusting the power consumption and this is usually done by changing the amplitude of the sinusoidal input current, what is equivalent to a multiplication of the fundamental waveform with a certain factor, in contrast to an addition of a single small-signal component to the fundamental waveform what is generally assumed in the harmonic linearization method.

A method that accommodates the physical origin of oscillations in power systems is the virtual q-axis approach [184]. Basically, the method is based on the analysis of three-phase AC systems. It introduces a virtual perpendicular axis to the main sinusoid with a mathematical transform. Subsequently, the system can be transformed into the synchronous reference frame and a steady-state operating point is obtained. It is necessary to use 2x2 impedance matrices to describe the small-signal behaviour of the converter. The same analysis tools available for three-phase AC systems described later can be used. An advantage of this method is that the system impedance matrices can also be measured directly for the single-phase case [185].

The last method suitable to describe and analyze the stability of single-phase AC systems is using linear time-periodic (LTP) system theory. It was applied to study stability issues of the single-phase rail-

way system including locomotives equipped with active rectifiers or diode rectifiers [186–190]. A harmonic transfer matrix is introduced to cover the dynamic behaviour of the converter. This transfer matrix catches all frequency convolutions and is possibly of infinite dimension, but it can be handled with conventional MIMO system theory in order to assess the stability of interconnected systems. The method is very sophisticated and not well-known but it gives accurate results. It provides the theoretical background for the small-signal analysis of time-periodic systems. The same theory was applied to find the steady-state response of an AC-DC-AC converter to an input voltage including harmonics [191, 192].

Summarizing, contrary to DC systems, there is not a well-established method to determine the stability of interconnected single-phase AC systems. The reduced order models are simple and give accurate results for certain scenarios but can not be used as a general model of the converter. The sophisticated methods involve an increased mathematical effort and are not well-known.

In this thesis, only three-phase AC systems are considered. Most often, three-phase AC converters work without connected star point and therefore behave slightly different than single-phase systems. The open star point causes a coupling between the three phases of the system, i.e. only two of them are independent. It is therefore not sufficient to work with a single-phase equivalent of the converter. Additionally, modern power electronic converters such as active rectifiers are not symmetric concerning their behaviour in the direct- and in the quadrature axis of a synchronous reference frame.

Neglecting the coupling of the three phases and treating the system as a single-phase system might work in some cases (i.e. for filter design). But the problems with finding an operating point for linearization still persist.

The better way is to include the coupling into the system description. The analysis could be done with 3x3 matrices which include all three phases and their couplings. Because there is redundancy in the system if the star point is not connected, the better way is working only with 2x2 matrices. In order to find a steady-state operating point, transformation into the synchronous reference frame is used. Subsequently, the system equations found with state-space averaging can be linearized and a small-signal model suitable for the analysis with LTI system theory is resulting [193–195].

System and converter modelling in the synchronous reference frame is well-established and widely used in machine control, converter control and also in power grid system modelling. With some effort, the converter models can be integrated into larger interconnected system models to form a closed-loop state matrix, what allows an eigenvalue based stability analysis [196–199].

System modelling in the synchronous reference frame is closely related to modelling in terms of amplitude and angle, what is often applied in conventional power system modelling [200]. In fact, both methods are interchangeably used in power system modelling. There, system stability is often expressed in terms of amplitude and angle stability. Because in the synchronous reference frame, the direct axis is related to the amplitude and the quadrature axis is related to the angle, both methods are equivalent.

As experience in power grid system analysis clearly shows [200], amplitude stability alone is not sufficient to guarantee system stability. Also the angle stability has to be considered, which is related to torsional oscillations. Equivalently, it is not sufficient to consider only the direct axis in the synchronous reference frame or treat the system as a single-phase equivalent. The quadrature axis is important as well, what is related in power electronic systems to PLL oscillations.

Similarly to DC system analysis, there is an alternative to the eigenvalue based stability analysis. Instead of using the closed-loop state matrix of the complete interconnected system, the subsystem impedance matrices at a specific connection interface could be used for stability assessment. An impedance based stability criterion equivalent to Middlebrook's criterion for DC systems was lately developed for three-phase AC systems [201]. There, the maximum and minimum singular value norms of the subsystem impedance matrices are compared in order to prove closed loop stability. This method is further explained in Section 4.2.2.

For completely linear and symmetric systems, instead of impedance matrices in the synchronous reference frame, also impedance matrices in stationary coordinates can be used. In this case, there is an equivalence between the description of the system with 2x2 impedance matrices and the description with two impedances, one for the positive sequence and one for the negative sequence behaviour [202, 203]. If there is an asymmetric dq-behaviour, such as for active rectifiers, there is no such equivalent (except if two complex valued impedances are allowed [203],

resulting again in four independent impedance components). The input impedance matrix in the synchronous reference frame has been used for stability studies, mainly concerning interactions of the active rectifier with the input filter [204–208].

The advantage of the impedance based stability criterion is the ability to measure the subsystem impedance matrices [185, 209, 210]. Based on the measured matrices it is possible to immediately identify problems such as filter resonances and converter interactions.

A drawback of the impedance based stability criterion is its conservative nature. Different to DC systems, there is no phase definition which could be used to reduce the conservatism [203]. Therefore, depending on the system to analyze, it is hardly possible to fulfil the impedance condition. Especially if there is distinct cross-coupling between the direct and the quadrature axis, the criterion is very conservative. Additionally, in order to guarantee the stability of a large interconnected system, the impedance criterion has to be checked at every interconnection interface [171].

4.2.2 Stability theory based on impedance matrices in synchronous coordinates

If the synchronous reference frame transformation is applied to a 3-phase system all variables transform to a stationary operating point. The system can now be described as a linear, time invariant MIMO system and all the rules for stability of MIMO systems apply. Such a system, consisting of two interconnected subsystems, is depicted in Fig. 4.4. The subsystems are represented with their small-signal Thevenin equivalent, respective Norton equivalent circuit.

The common bus voltage at the connection interface is given as

$$V_{\mathrm{b,dq}} = (I + Z_1 \cdot Y_2)^{-1} \cdot V_{1,\mathrm{dq}} + (I + Z_1 \cdot Y_2)^{-1} \cdot Z_1 \cdot I_{2,\mathrm{dq}}. \quad (4.16)$$

All impedances are transformed to 2x2 impedance matrices and the voltages and currents are 1x2 vectors containing the direct and quadrature axis component. The closed-loop system is stable if the sources V_1, I_2 are stable, Z_1 and Y_2 are stable (they don't have any MIMO poles in the right half plane) and additionally, the eigenvalues of the loop gain $Z_1 \cdot Y_2$ plotted in the complex plane over the complete frequency range do not encircle the critical point, i.e. (-1,0i). This condition is known as the generalized Nyquist criterion [201, 211]. It is very similar

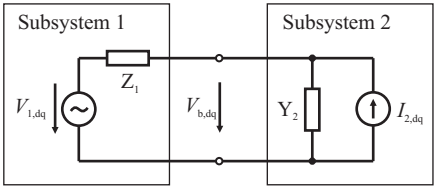

Figure 4.4: Two subsystems interconnected at a common bus.

to the conventional Nyquist criterion for SISO systems, but instead of plotting the modulus of $Z_1 \cdot Y_2$ in the complex plane, the eigenvalue loci are considered here.

The source V_1 is stable if the bus voltage is stable with the load disconnected. The source I_2 can be considered to be stable if the subsystem (e.g. an active rectifier) is stable if it is connected to an ideal voltage source. The number of open loop unstable poles in Z_1 and Y_2 is zero for passive networks and for most other practical systems that work in stand-alone operation without external stabilization measures. Actually, these side-conditions are the same as the ones implicitly assumed for the impedance criteria applied to DC systems.

As for the SISO case, we can now define a matrix norm which includes the maximum eigenvalues and limit them to be less than one, so that no eigenvalue plot can encircle the critical point -1. The following condition holds for the eigenvalues of a matrix G, whereas $\overline{\sigma}$ and $\underline{\sigma}$ denote the maximum respective minimum singular value of the matrix.

$$\underline{\sigma}(\mathrm{G}) \leq |\lambda_i(\mathrm{G})| \leq \overline{\sigma}(\mathrm{G}) \tag{4.17}$$

An appropriate impedance criterion for stability at the corresponding interface can be found with the condition

$$\overline{\sigma}(\mathrm{Z}_1 \cdot \mathrm{Y}_2) < 1. \tag{4.18}$$

An important property of the singular value norm is that the norm of a matrix product is greater or equal than the product of the matrix norms. Therefore, the condition can be tightened and written in a suitable way as

$$\overline{\sigma}(\mathrm{Z}_1) \cdot \overline{\sigma}(\mathrm{Y}_2) < 1, \tag{4.19}$$

and by separating the condition we obtain

$$\overline{\sigma}(\mathrm{Z}_1) < \frac{1}{\overline{\sigma}(\mathrm{Y}_2)}. \tag{4.20}$$

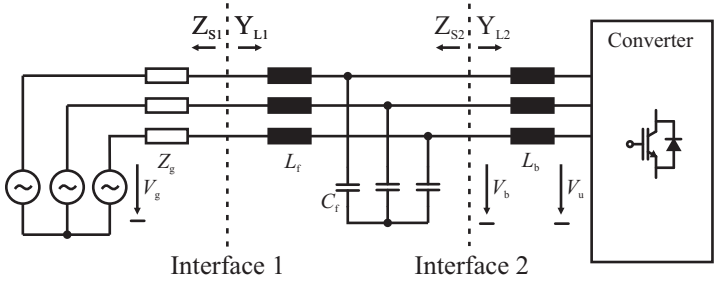

Figure 4.5: Active rectifier with input filter and two different interfaces.

By using the identity for the matrix inverse ($1/\overline{\sigma}(\mathrm{G}) = \underline{\sigma}(\mathrm{G}^{-1})$) the impedance criterion can also be expressed as

$$\overline{\sigma}(\mathrm{Z}_1) < \underline{\sigma}(\mathrm{Z}_2), \tag{4.21}$$

what is very similar to the unity circle impedance criterion for DC systems (cf. Eq. 4.15).

The maximum singular value norm is equal to the maximum gain of the matrix into a certain MIMO system direction. It is obvious that this impedance criterion has the same conservative nature as Middlebrook's impedance criterion because the major part of the complex plane is actually forbidden. The system is guaranteed to be stable if Eq. 4.21 and the side-conditions are fulfilled but it can still be stable even if the conditions are missed.

4.3 Stability assessment of an active rectifier system with an EMI input filter

In this section, the stability of an active rectifier with an EMI input filter is analyzed using the impedance criterion for three-phase systems. The basic results are forming the background for the development and analysis of active damping concepts. The characteristics of the rectifier input impedance depending on the control parameters and the PLL bandwidth are derived and compared with the characteristics of the filter output impedance.

4.3.1 Output impedance of the EMI filter

In order to apply the impedance criterion one has to compute or measure the source and load impedances at a specified interface. It is simple to calculate the impedance matrix of a passive network by introducing the matrices for the simplest possible elements, in particular a resistance, an inductance and a capacitance,

$$\mathrm{Z_R} = \begin{pmatrix} R & 0 \\ 0 & R \end{pmatrix} \tag{4.22}$$

$$\mathrm{Z_L} = \begin{pmatrix} sL & -\omega_\mathrm{e} L \\ \omega_\mathrm{e} L & sL \end{pmatrix} \tag{4.23}$$

$$\mathrm{Y_C} = \begin{pmatrix} sC & -\omega_\mathrm{e} C \\ \omega_\mathrm{e} C & sC \end{pmatrix}. \tag{4.24}$$

As with normal impedances, rules for series and parallel connection of impedance or admittance matrices apply. For series connection of elements, the impedance matrices add together and for parallel connection of circuit elements the admittance matrices add together,

$$\text{series:} \qquad \mathrm{Z_{sum}} = \mathrm{Z_1} + \mathrm{Z_2} \tag{4.25}$$

$$\text{parallel:} \qquad \mathrm{Y_{sum}} = \mathrm{Y_1} + \mathrm{Y_2}. \tag{4.26}$$

The impedance matrix is the inverse of the corresponding admittance matrix and vice versa,

$$\mathrm{Z} = \mathrm{Y}^{-1} \qquad \mathrm{Y} = \mathrm{Z}^{-1}. \tag{4.27}$$

Now, the interface impedance matrices can easily be computed. According to Fig. 4.5, two interfaces can be defined. Interface 1 is the point of common coupling, where the converter is connected with the grid. It is possible that other converters are connected to this interface and interfere with each other. Interface 2 is located between the EMI filter and the converter where mainly a stable current control is of interest. At interface 1, the grid output impedance, that can be modeled with a simple RL-branch, is given as

$$\mathrm{Z_{S1}} = \mathrm{Z_g} = \mathrm{Z_{Rg}} + \mathrm{Z_{Lg}} = \begin{pmatrix} R_\mathrm{g} + sL_\mathrm{g} & -\omega_\mathrm{e} L_\mathrm{g} \\ \omega_\mathrm{e} L_\mathrm{g} & R_\mathrm{g} + sL_\mathrm{g} \end{pmatrix}. \tag{4.28}$$

At interface 2, the output impedance is influenced by the EMI filter and can be calculated with

$$\mathrm{Z_{S2}} = \left[\left[\mathrm{Z_{Rg}} + \mathrm{Z_{Lg}} + \mathrm{Z_{Lf}} \right]^{-1} + \mathrm{Y_{Cf}} \right]^{-1}. \tag{4.29}$$

Table 4.1: Properties of the filter components.

Component	Value
R_g	$50\,\mathrm{m\Omega}$
L_g	$50\,\mu\mathrm{H}$
L_f	$500\,\mu\mathrm{H}$
C_f	$40\,\mu\mathrm{F}$
L_b	$600\,\mu\mathrm{H}$

The maximum singular value norm of the filter output impedance at interface 2, $\overline{\sigma}(\mathrm{Z_{S2}})$, is depicted in Fig. 4.6. The main properties of the filter components are summarized in Table 4.1. The EMI filter components are over-dimensioned but are suitable to show the impact of the active damping methods presented in Section 4.4. Such a combination of over-dimensioned EMI filter and converter could occur if a cheap standard filter stage is ordered from an external manufacturer.

It can be noticed that in the synchronous reference frame, the single phase filter resonance gets splitted into two separate resonance peaks. They are aligned at the frequencies $\omega_0 - \omega_\mathrm{e}$ and $\omega_0 + \omega_\mathrm{e}$ (ω_0: resonance frequency of single phase filter equivalent, ω_e: angular speed of dq-reference frame). This effect is directly related to the amplitude modulation process. If the amplitude of a signal is modulated with the frequency $\omega_0 - \omega_\mathrm{e}$, what corresponds to an injected sinusoidal signal with the frequency $\omega_0 - \omega_\mathrm{e}$ only in the direct axis of the synchronous reference frame, it gets transformed into a simultaneous injection of two signals with the different frequencies ω_0 (a positive sequence) and $-(\omega_0 - 2\omega_\mathrm{e})$ (a negative sequence) in the stationary reference frame. Therefore, the positive sequence signal will excite the filter resonance. Similarly, a sinusoid with the frequency $\omega_0 + \omega_\mathrm{e}$ in the synchronous reference frame is transformed into the simultaneous injection of two signals in the stationary reference frame, having the frequencies $-\omega_0$ (a negative sequence) and $\omega_0 + 2\omega_\mathrm{e}$ (a positive sequence). The filter with resonance frequency ω_0 will again be excited as its transfer function is symmetric for positive and negative sequences.

The filter output impedance matrix covers both, the reaction on excitation with positive and with negative sequence signals in the three-phase system. Positive and negative sequences get transformed to different MIMO directions in the synchronous reference frame representation. The maximum singular value norm limits the maximum gain in

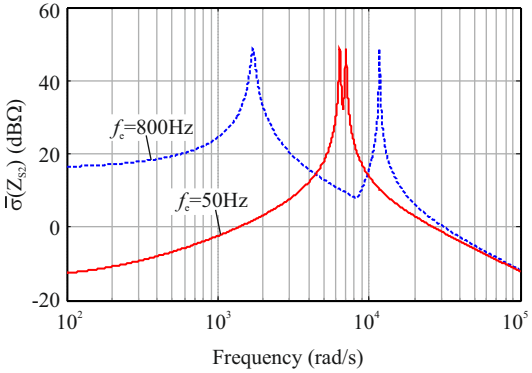

Figure 4.6: Maximum singular value norm of the filter output impedance Z_{S2} for two different angular frequencies of the synchronous reference frame.

all MIMO directions and therefore is an upper limit for the gain at a specific frequency, independent of the sequence of the signal.

4.3.2 Input admittance of the active rectifier

The input admittance matrix Y_{L2} of the active rectifier can be derived with some algebraic effort. The cascaded control structure is depicted in Fig. 4.7. An outer control loop regulates the dc-link voltage and two inner control loops regulate the input current d- and q-axis components. The transfer functions of the current controller R_i and of the dc-link voltage controller R_u are given with

$$R_i = k_{pi}\frac{1+sT_{ni}}{sT_{ni}},\ R_u = k_{pu}\frac{1+sT_{nu}}{sT_{nu}}. \tag{4.30}$$

The cross-coupling terms of the boost inductance and the grid voltage are considered with feedforward of the appropriate values. The PLL for tracking the input voltage reference angle is assumed to have a very low bandwidth and its dynamics are neglected in a first step. The steady-state angular frequency of the synchronous reference frame is fixed. In steady-state, the PLL reference frame d-axis is aligned to the synchronous reference frame and all variations are considered to be small-signal deviations.

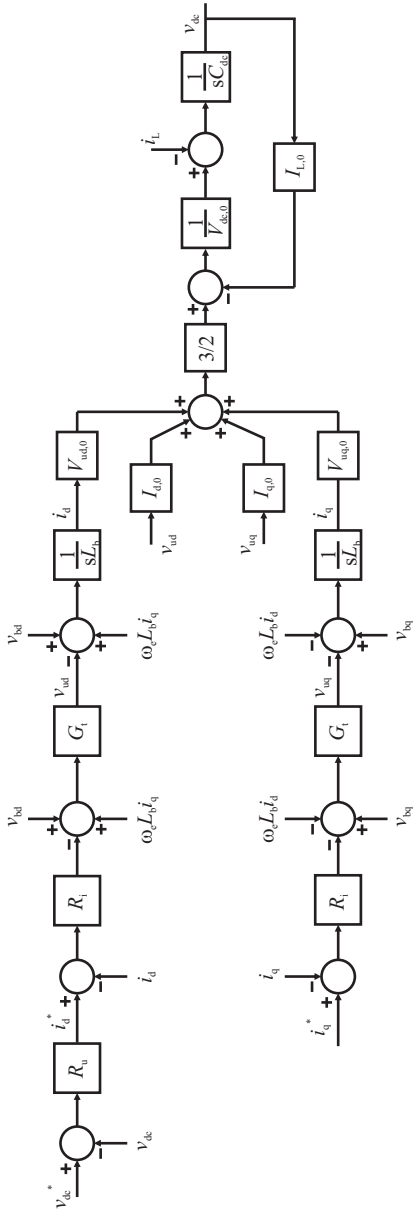

Figure 4.7: Block diagram of the control loops and the linearized plant.

As the converter model is based on the state-space averaging over a switching period, the model is valid for a frequency range below the switching frequency only. Nevertheless, for higher frequencies, the boost inductance mainly determines the input impedance of the converter. In practice, the current and voltage sensors have a limited bandwidth and often low-pass signal filters are used to prevent aliasing effects. It is assumed that their characteristics can be approximated with a total time-delay element that includes all further time delays.

In a real setup the PI-controllers are computed on a DSP with a fixed sampling rate. It is therefore inevitable to have a certain time delay in the control loop because of the calculation time and the sampling. The modulation of the converter output voltage introduces an additional time delay. Unfortunately, the space vector modulation (SVM) and PWM lead to a coupling between the d- and q-axis and the introduced time delay can be time-varying also in the synchronous dq-reference frame [212]. We neglect this cross-coupling (it is small anyway) and consider as the worst case the largest time delay consisting of computation time, sensor delays and SVM delay equally in d- and q-axis with the transfer function

$$G_{\mathrm{t}} = e^{-sT_{\mathrm{t}}} \approx \frac{1}{1+sT_{\mathrm{t}}}. \tag{4.31}$$

No further assumptions are made for the derivation of the VSC equations. In particular, there is no assumption about the converters q-axis current or voltage being zero.

The input admittance matrix is given with

$$\begin{pmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \end{pmatrix} = \begin{pmatrix} Y_{\mathrm{dd}} & Y_{\mathrm{dq}} \\ Y_{\mathrm{qd}} & Y_{\mathrm{qq}} \end{pmatrix} \cdot \begin{pmatrix} v_{bd} \\ v_{bq} \end{pmatrix}. \tag{4.32}$$

The system equations can be found with the control block diagram depicted in Fig. 4.7. The nonlinear power equation has to be linearized. For the power equation, the converter voltage v_{u} and not the bus voltage at the boost inductor v_{b} has to be considered. These assumptions

directly lead to the following equation system:

$$\begin{aligned}
i_\mathrm{d} &= \frac{1}{sL_\mathrm{b}}\left(v_\mathrm{bd} + \omega_\mathrm{e} L_\mathrm{b} i_\mathrm{q} - v_\mathrm{ud}\right) \\
i_\mathrm{q} &= \frac{1}{sL_\mathrm{b}}\left(v_\mathrm{bq} - \omega_\mathrm{e} L_\mathrm{b} i_\mathrm{d} - v_\mathrm{uq}\right) \\
v_\mathrm{ud} &= G_\mathrm{t}\left(v_\mathrm{bd} + \omega_\mathrm{e} L_\mathrm{b} i_\mathrm{q} - \left(i_\mathrm{d}^* - i_\mathrm{d}\right) R_\mathrm{i}\right) \\
v_\mathrm{uq} &= G_\mathrm{t}\left(v_\mathrm{bq} - \omega_\mathrm{e} L_\mathrm{b} i_\mathrm{d} - \left(-i_\mathrm{q}\right) R_\mathrm{i}\right) \\
i_\mathrm{d}^* &= -v_\mathrm{dc} R_\mathrm{u} \\
v_\mathrm{dc} &= G_\mathrm{p}\left(I_{\mathrm{d},0} v_\mathrm{ud} + V_{\mathrm{ud},0} i_\mathrm{d} + I_{\mathrm{q},0} v_\mathrm{uq} + V_{\mathrm{uq},0} i_\mathrm{q}\right) \\
G_\mathrm{p} &= \frac{3}{2}\frac{1}{V_{\mathrm{dc},0} s C_\mathrm{dc} + I_0}.
\end{aligned} \tag{4.33}$$

The input admittance matrix elements Y_dd and Y_qd are found by setting the input voltage v_bq to zero and solving for the currents i_d and i_q corresponding to v_bd according to

$$Y_\mathrm{dd} = \left.\frac{i_\mathrm{d}}{v_\mathrm{bd}}\right|_{v_\mathrm{bq}=0}, \quad Y_\mathrm{qd} = \left.\frac{i_\mathrm{q}}{v_\mathrm{bd}}\right|_{v_\mathrm{bq}=0}. \tag{4.34}$$

They can be expressed in the simple form

$$Y_\mathrm{dd} = \frac{1}{a_3 - a_1 \omega_\mathrm{e} L_\mathrm{b} + s L_\mathrm{b}}, \tag{4.35}$$

$$Y_\mathrm{qd} = \frac{a_1}{a_3 - a_1 \omega_\mathrm{e} L_\mathrm{b} + s L_\mathrm{b}}. \tag{4.36}$$

The parameters are defined as

$$\begin{aligned}
a_1 &= \frac{G_\mathrm{t} - 1}{G_\mathrm{t} R_\mathrm{i} + s L_\mathrm{b}} \omega_\mathrm{e} L_\mathrm{b}, \\
a_2 &= \frac{-G_\mathrm{t}\left(R_\mathrm{i} + s L_\mathrm{b}\right)}{G_\mathrm{t} R_\mathrm{i} + s L_\mathrm{b}} \omega_\mathrm{e} L_\mathrm{b}, \\
a_3 &= \frac{-G_\mathrm{t}\left(s L_\mathrm{b} + R_\mathrm{i}\left(1 + R_\mathrm{u} G_\mathrm{p}\left(V_{\mathrm{ud},0} + a_1 V_{\mathrm{uq},0} + a_2 I_{\mathrm{q},0}\right)\right)\right)}{\left(G_\mathrm{t} - 1\right) + G_\mathrm{t} R_\mathrm{i} R_\mathrm{u} G_\mathrm{p} I_{\mathrm{d},0}}.
\end{aligned} \tag{4.37}$$

Parameter a_1 describes the impact of the time delays resulting in an incomplete compensation of the cross coupling and parameter a_3 is related to the complete active power feedback through the outer dc-link voltage loop.

The remaining input admittance matrix elements Y_{qq} and Y_{dq} are found by setting the input voltage v_{bd} to zero and solving for the currents i_{d} and i_{q} corresponding to v_{bq} according to

$$Y_{\mathrm{qq}} = \left.\frac{i_{\mathrm{q}}}{v_{\mathrm{bq}}}\right|_{v_{\mathrm{bd}}=0}, \quad Y_{\mathrm{dq}} = \left.\frac{i_{\mathrm{d}}}{v_{\mathrm{bq}}}\right|_{v_{\mathrm{bd}}=0}. \tag{4.38}$$

Again, they can be expressed in a simple form as

$$Y_{\mathrm{qq}} = \frac{1}{b_3 + b_1\omega_{\mathrm{e}}L_{\mathrm{b}} + sL_{\mathrm{b}}}, \tag{4.39}$$

$$Y_{\mathrm{dq}} = \frac{b_1}{b_3 + b_1\omega_{\mathrm{e}}L_{\mathrm{b}} + sL_{\mathrm{b}}}. \tag{4.40}$$

The parameters are given as

$$b_1 = \frac{-G_{\mathrm{t}}R_{\mathrm{i}}R_{\mathrm{u}}G_{\mathrm{p}}\left(b_3 I_{\mathrm{q},0} + V_{\mathrm{uq},0} + \omega_{\mathrm{e}}L_{\mathrm{b}}I_{\mathrm{d},0}\right) + \left(1 - G_{\mathrm{t}}\right)\omega_{\mathrm{e}}L_{\mathrm{b}}}{G_{\mathrm{t}}R_{\mathrm{i}} + sL_{\mathrm{b}} + G_{\mathrm{t}}R_{\mathrm{i}}R_{\mathrm{u}}G_{\mathrm{p}}\left(V_{\mathrm{ud},0} - sL_{\mathrm{b}}I_{\mathrm{d},0}\right)} \tag{4.41}$$

$$b_3 = \frac{-G_{\mathrm{t}}\left(R_{\mathrm{i}} + sL_{\mathrm{b}}\right)}{G_{\mathrm{t}} - 1}. \tag{4.42}$$

Parameter b_1 describes the impact of the time delays and the coupling over the active power feedback loop and b_3 is related to the current loop in q-direction.

If we would assume no time delay ($G_{\mathrm{t}} = 1$) several simplifications would be possible: among others $Y_{\mathrm{qd}} = 0$ and $Y_{\mathrm{qq}} = 0$ would result due to the ideal decoupling and feedforward control. Y_{dq} would not equal zero because of the small coupling via the active power loop.

Properties of $\mathbf{Y_{L2}}$

In the following, the characteristics of the input admittance matrix of the active rectifier are analyzed. The numerical results are based again on the 10 kW system used throughout this thesis. An artificially high switching frequency of $f_{\mathrm{sw}} = 50\,\mathrm{kHz}$ is used in order to show the possibilities concerning active damping methods. The converter characteristics are summarized in Table 4.2. Principally, the impact of the active damping methods presented in Section 4.4 is limited to frequencies below the current control bandwidth. This implies that the resonance frequency of the filter topology has to be in the same frequency range as well. It can be concluded that the active damping

Table 4.2: Properties of the active rectifier.

Component	Value
P_0	10 kW
f_{sw}	50 kHz
C_{dc}	1 mF
V_{dc}	650 V
V_{g}	230 V

methods are only suitable for rather high switching frequencies that enable a high current control bandwidth. Such switching frequencies can be achieved with the discussed 3-level converter topologies.

The components of the input admittance matrix $\mathrm{Y_{L2}}$ are depicted in Fig. 4.8. The dc-link voltage control loop is designed to have a bandwidth of $\omega_{b,u} = 35\,\mathrm{Hz}$ with a phase margin of 80° whereas the current control loop is designed to have a bandwidth of $\omega_{b,i} = 5\,\mathrm{kHz}$ with a phase margin of 50°. A total dead-time of $T_{\mathrm{t}} = 20\,\mu\mathrm{s}$ is assumed.

One can notice the dominant magnitude of Y_{dd} and Y_{qq}. The negative differential resistance behaviour of Y_{dd} can be observed for frequencies below the dc-link voltage regulation bandwidth where the converter behaves as a constant power load. Therefore, the phase of Y_{dd} is near 180° in this frequency range. The cross-coupling terms Y_{dq} and Y_{qd} are very small because of the introduced decoupling loops in the control scheme.

In the previous derivation of the input admittance matrix elements, it was assumed that the PLL has a very low bandwidth. If the PLL is included, mainly the characteristics of Y_{qq} are influenced, as is shown in Fig. 4.9. The bandwidth of the PLL is designed to be $\omega_{\mathrm{b,pll}} = 25\,\mathrm{Hz}$. The derivation of the mathematical model can be found in the Appendix. Knowing the behavior of Y_{qq} would be important to identify the cause of frequency oscillations, that could occur e.g. because of interactions of the PLL loop with a synchronous generator.

In order to determine the closed-loop stability of the active rectifier including the EMI input filter, the minimum singular value norm of the rectifier input impedance has to be calculated. It is derived using $\underline{\sigma}(\mathrm{Z_{L2}}) = 1/\overline{\sigma}(\mathrm{Y_{L2}})$ and is depicted in Fig. 4.10.

The similarity between the plot of $\underline{\sigma}(\mathrm{Z_{L2}})$ and the input impedance of a DC-DC boost converter (cf. [160]) is obvious since the active rectifier actually is a 3-phase boost regulator. One can also observe the

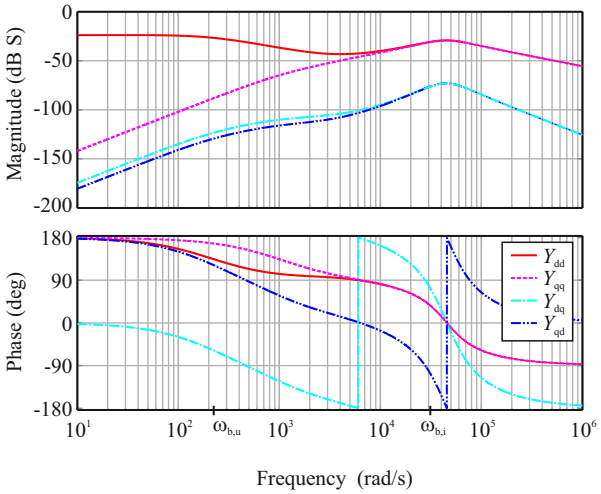

Figure 4.8: Input admittance matrix components of the active rectifier.

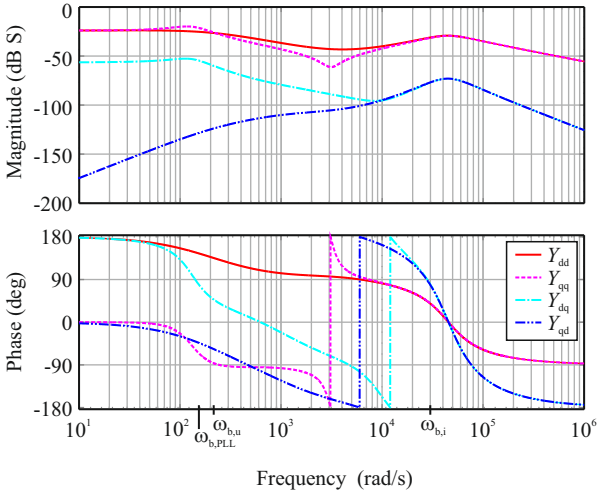

Figure 4.9: Input admittance matrix components of the active rectifier including the impact of the PLL designed with a bandwidth of $\omega_{\mathrm{b,pll}} = 25\,\mathrm{Hz}$.

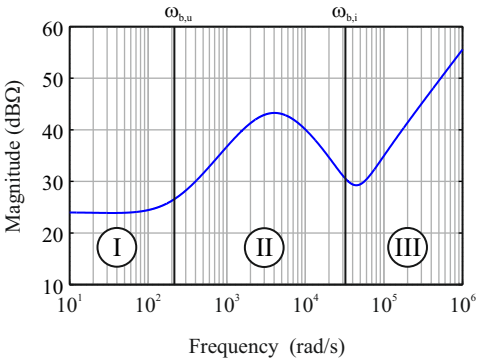

Figure 4.10: Minimum singular value norm of the rectifier input impedance matrix ($\underline{\sigma}(\mathrm{Z_{L2}}) = 1/\overline{\sigma}(\mathrm{Y_{L2}})$).

typical impedance sag caused by the time delays.

It is possible to identify three specific frequency ranges of the input impedance that are characteristic for the active rectifier.

In frequency range I, below the voltage regulation bandwidth, the constant power load behavior with negative input impedance is dominating. The impedance norm only depends on the consumed power. The impedance norm decreases with increasing power, possibly rendering the system unstable for a high source impedance in this frequency range. A good choice for a stable control is to select the voltage regulation bandwidth as low as possible to limit this critical constant power frequency range and to select the current regulation bandwidth as high as possible.

In frequency range II, between the voltage regulation bandwidth and the current regulation bandwidth, the converter has a very high input impedance. This is due to the grid voltage feed-forward and the current control, accordingly the input current does not react on changes of the input voltage. In this frequency range the basic behavior of the converter could be freely redefined without affecting the power transfer at the fundamental frequency.

In frequency range III, above the current regulation bandwidth, first the time delay influences the shape of the impedance norm and finally, the boost inductance is dominating. It is difficult to change the input impedance in this frequency range because of the controller bandwidth limits.

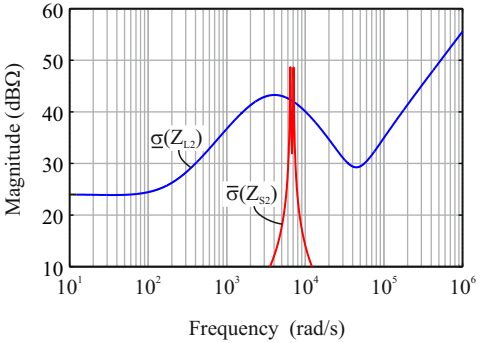

Figure 4.11: The impedance criterion at interface 1 indicates that closed-loop stability is not guaranteed with the undamped input filter.

The impedance criterion can be checked graphically if the impedance matrix norms are plotted in the same graph. Fig. 4.11 shows the maximum singular value norm of the filter output impedance matrix $\overline{\sigma}(\mathrm{Z_{S2}})$ and the minimum singular value norm of the converter input impedance matrix $\underline{\sigma}(\mathrm{Z_{L2}})$. As the impedance condition is not fulfilled, a stable closed-loop operation of the system cannot be guaranteed. This is mainly due to the weakly damped input filter. An additional damping branch in parallel to the filter capacitor or in series to the filter inductor is sufficient to solve this problem. Alternatively, active damping concepts could be used which are described in the next section.

The active damping concepts change the behaviour of the active rectifier in frequency range II. The converter can be used to achieve additional goals in this frequency range. The input impedance of the former unused frequency range is redefined and shaped in an appropriate way.

4.4 Active damping concepts

In order to guarantee a stable current control with an input filter, the resonances of the filter have to be damped. Conventionally, this is obtained with an additional passive damping branch included in the filter topology. However, the damping branch leads to additional components, an increased filter volume and weight, additional costs and increased losses.

Modern power electronic converters use high switching frequencies in order to reduce weight and volume of passives components. A high switching frequency basically allows increasing the bandwidth of control loops and therefore new possibilities concerning additional control tasks arise. For most conventional converter applications the increased control bandwidth is not necessary. The power transfer usually takes place at the nominal grid frequency. The control task is to carry sinusoidal currents in phase to the input voltages. In the high frequency range the control behaviour has no specific requirements. In this frequency range the control variable is usually forced to follow the more or less constant reference what results in a high input impedance and disturbance rejection.

Active damping concepts exploit this unused frequency range and redefine the converter behaviour. This is a new insight as it allows for a different converter behaviour depending on the frequency range. The PFC rectifier behaviour is maintained only in the low frequency range.

An interesting concept in this context is the virtual resistor [213–215]. It is easy to implement and its damping effect can be understood intuitively. The rectifier emulates the characteristics of a resistor at its input terminals. The filter resonance is damped actively and the stability margins are increased. The virtual resistor damping concept can be found in both active rectifiers with input filter and inverters with output filter stage.

In the next sections, the virtual resistor damping concept is extended to a virtual impedance damping concept. The control of the converter can be adapted to emulate a resistive, capacitive or inductive behaviour at its input terminals. Even a combination of several components is possible. The extension to reactive elements allows to have an impact on the resonance frequency of the input filter. This leads to the damping method called "Resonance Frequency Shifting" (RFS).

4.4.1 Virtual impedance damping

The resonance of the input filter is only weakly damped by the winding resistance of the inductors and the grid resistance. This deteriorates the performance of the rectifier system in several ways. First, the resonance can be excited by external disturbances from the grid what would result in large amplitude voltage ringing and a protective shutdown of the rectifier. Second, the undamped resonance is known to lead to an

unstable closed loop system together with the active rectifier operated as a constant power sink. The negative differential resistance of the constant power sink amplifies the resonance and makes it impossible to run the system. Therefore, the filter resonance peak has to be damped, passively or actively.

The main idea of the virtual impedance concept is simple. The current control loop is enhanced with additional equations implementing a damping element (cf. the gray blocks in the control diagram depicted in Fig. 4.12). The converter mimics the behaviour of an additional circuit element or even a combination of circuit elements at its input terminals whose effect can be described with an admittance matrix as

$$\begin{pmatrix} i_{\mathrm{sim,d}} \\ i_{\mathrm{sim,q}} \end{pmatrix} = \begin{pmatrix} Y_{\mathrm{sim,dd}} & Y_{\mathrm{sim,dq}} \\ Y_{\mathrm{sim,qd}} & Y_{\mathrm{sim,qq}} \end{pmatrix} \cdot \begin{pmatrix} v_{bd} \\ v_{bq} \end{pmatrix}. \tag{4.43}$$

Here, $i_{\mathrm{sim,d}}$ and $i_{\mathrm{sim,q}}$ designate the current components generated by the virtual element in response to the input voltage components v_{bd} and v_{bq} at interface 2 (cf. Fig. 4.5). The current references for the current controller loops can now be augmented with the equations

$$\begin{aligned} i^*_{\mathrm{d,new}} &= i^*_{\mathrm{d}} + Y_{\mathrm{sim,dd}} \cdot v_{\mathrm{bd}} + Y_{\mathrm{sim,dq}} \cdot v_{\mathrm{bq}} \\ i^*_{\mathrm{q,new}} &= i^*_{\mathrm{q}} + Y_{\mathrm{sim,qd}} \cdot v_{\mathrm{bd}} + Y_{\mathrm{sim,qq}} \cdot v_{\mathrm{bq}}. \end{aligned} \tag{4.44}$$

Designated by i^*_{d} and i^*_{q} are the current references of the conventional active rectifier. The virtual admittance should be simulated in a frequency range where it does not change the basic function of the converter. Therefore a bandpass filter should be used to process the reference signals of the virtual element. This also prevents from amplification of high frequency noise. The lower frequency limit is set to be higher than the dc-link voltage regulation bandwidth so that the power transfer is not influenced.

The new input admittance matrix $\mathrm{Y}_{\mathrm{L2,new}}$ can now be calculated, considering the impact of the additional control loops. The admittance matrix will consist of a superposition of the conventional rectifier input admittance matrix Y_{L2} and the actually simulated virtual admittance matrix $\mathrm{Y}^*_{\mathrm{sim}}$ as

$$\mathrm{Y}_{\mathrm{L2,new}} = \mathrm{Y}_{\mathrm{L2}} + \mathrm{Y}^*_{\mathrm{sim}}. \tag{4.45}$$

The resulting equations are very long but can be processed with mathematics software. The obtained components of the admittance matrix $\mathrm{Y}^*_{\mathrm{sim}}$ for a virtual capacitance of $C_{\mathrm{sim}} = 100\,\mu\mathrm{F}$ are depicted in Fig. 4.13.

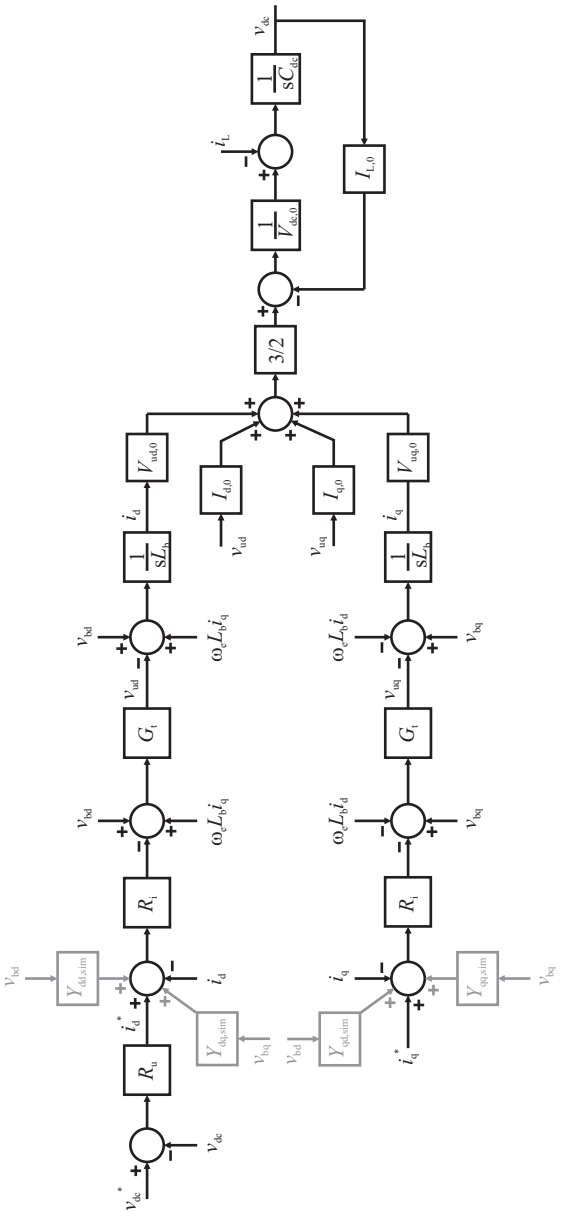

Figure 4.12: Block diagram of the control loops including the extensions for the emulation of a virtual impedance.

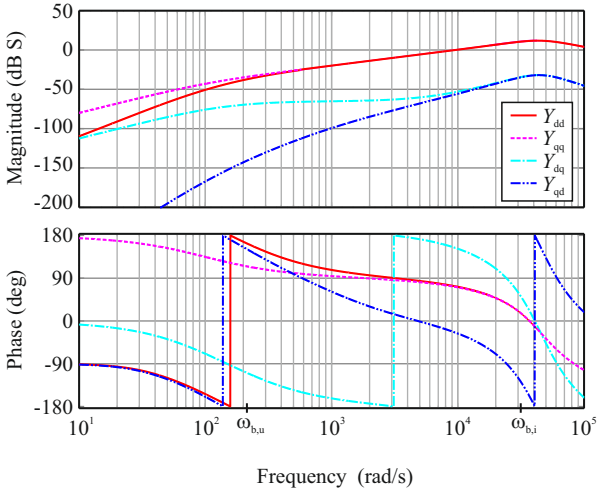

Figure 4.13: Components of the admittance matrix $\mathrm{Y}^{*}_{\mathrm{sim}}$ for a virtual capacitance of $C_{\mathrm{sim}} = 100\,\mu\mathrm{F}$.

The simulated circuit element exhibits the desired behavior mainly in the frequency range between the dc-link voltage regulation bandwidth $\omega_{\mathrm{b,u}}$ and current regulation bandwidth $\omega_{\mathrm{b,i}}$. Therefore, the virtual impedance method is constrained concerning the applicability. A virtual circuit element can only be simulated for frequencies below the current regulation bandwidth. Additionally, it should be avoided to simulate it in a frequency range below the voltage regulation bandwidth or even at the fundamental frequency as this would influence the current shape and voltage regulation behavior and/or the power transfer.

If a reactive element is simulated there exist also cross-coupling terms such as in the admittance matrix of a capacitor. As the frequency range where the virtual element should be simulated is usually higher than the frequency of the synchronous reference frame ω_{e}, the direct terms are dominant. Therefore, the cross-coupling terms $Y_{\mathrm{sim,dq}}$ and $Y_{\mathrm{sim,qd}}$ can be set to zero and have not to be included in the control loops without losing the positive impact of the virtual element.

The damping behaviour of the virtual circuit element is determined with the impedance criterion. The virtual circuit element can be thought to belong to the output impedance of the EMI filter and an artificial interface 2b is introduced. Accordingly, the new filter output impedance

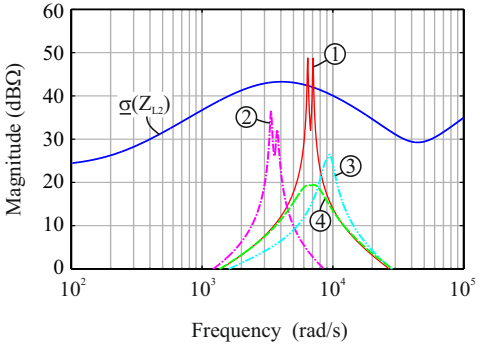

Figure 4.14: Impedance criterion at the artificial interface 2b. The maximum singular value norm of the output impedance matrix of the filter is changed by the simulated virtual element. 1: original undamped filter, 2: $C_{\mathrm{sim}} = 100\,\mu\mathrm{F}$, 3: $L_{\mathrm{sim}} = 600\,\mu\mathrm{H}$, 3: $R_{\mathrm{sim}} = 10\,\Omega$.

matrix is given by

$$\mathrm{Z}_{\mathrm{S2,new}} = \left[\left[\mathrm{Z}_{\mathrm{Rg}} + \mathrm{Z}_{\mathrm{Lg}} + \mathrm{Z}_{\mathrm{Lf}} \right]^{-1} + \mathrm{Y}_{\mathrm{Cf}} + \mathrm{Y}^{*}_{\mathrm{sim}} \right]^{-1} . \tag{4.46}$$

The virtual impedance could be of resistive, inductive or capacitive type or even a combination of elements. In Fig. 4.14 the effect of the virtual element on the maximum singular value norm of the filter output impedance matrix is depicted. The undamped filter (cf. curve no. 1) is not guaranteed to be stable in closed-loop what can be seen on the intersection with the minimum singular value norm of the converters input impedance matrix. A damping resistor is necessary to achieve a stable operation. The simulation of a virtual resistor $R_{\mathrm{sim}} = 10\,\Omega$ changes the filter output impedance norm to a damped one (curve no. 4) and stable operation is now guaranteed with a gain margin of more than 20 dB.

It is not only possible to damp the filter resonance but also to change the resonance frequency. The resonance frequency is decreased if a virtual capacitance is simulated (cf. curve no. 2) or it is increased if an inductance is simulated (cf. curve no. 3). Due to inevitable time delays in the control loop, the virtual elements cannot be simulated perfectly, what leads to a slight damping effect. Therefore, the virtual capacitance not only shifts the resonance peaks to a lower center frequency but also dampens them slightly. If the virtual capacitance is

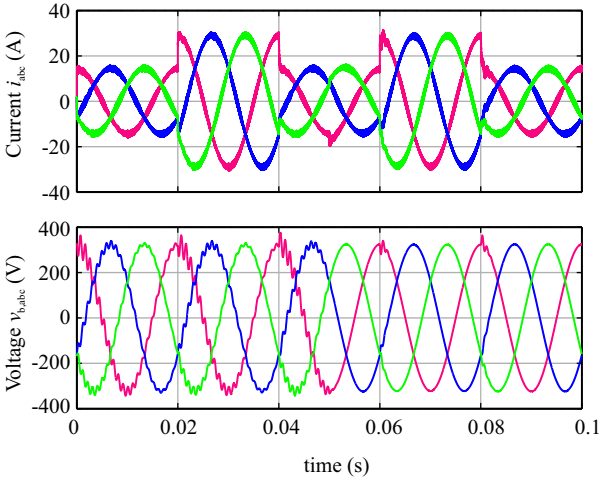

Figure 4.15: Time domain simulation of the active rectifier with virtual resistor damping.

combined with a virtual resistance in series, the gain margin can be increased compared to the simple virtual resistance damping, especially if the filter resonance frequency is located near the current control bandwidth. A further application of this resonance frequency shifting ability is presented in the next section, where it is used to mitigate external disturbances injected by converters connected into the point of common coupling.

Depicted in Fig. 4.15 are the results of a time-domain simulation of the active rectifier implementing the virtual resistor damping method. The input filter values given in Table 4.1 lead to a resonance of the filter impedance at $f_0 = 1.1\,\mathrm{kHz}$ which is only weakly damped by the grid resistance. The grid resistance was increased to $R_\mathrm{g} = 100\,\mathrm{m\Omega}$ to obtain a system near the stability boundary. At the beginning of the simulation a weakly damped ringing of the bus voltage v_b at interface 2 can be observed. At simulation time $t = 0.02\,\mathrm{s}$ a load step is executed and the resonance is excited again. The virtual resistor damping method with $R_\mathrm{sim} = 10\,\Omega$ is activated at $t = 0.05\,\mathrm{s}$ and the same load step is executed at $t = 0.06\,\mathrm{s}$. Now the distortion in the input voltage is rapidly damped and a smooth input voltage persists.

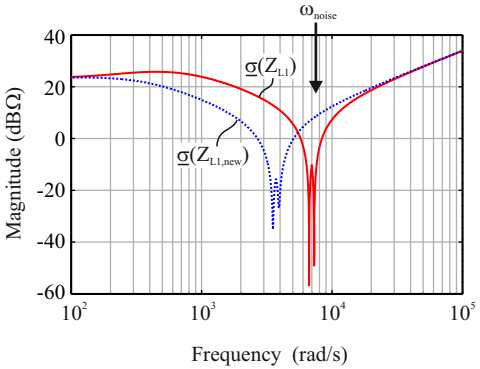

Figure 4.16: Minimum singular value norm of the load impedance matrix at interface 1. The filter resonance frequency can be shifted actively by simulating a virtual capacitance (dotted curve).

4.4.2 Resonance frequency shifting (RFS)

A further interesting stabilization concept that arises from the virtual impedance method is the ability to shift the resonance frequency of the EMI input filter. The simulated impedance is connected in parallel to the filter capacitor. With a virtual reactive element this capacitor value can be increased or decreased what results in a shifted resonance frequency.

At interface 1 (the point of common coupling, cf. Fig. 4.5) the visible converter impedance shows an impedance drop at the resonance frequency what is depicted in Fig. 4.16. If the grid structure comprises additional converters injecting noise with a frequency near this resonance (i.e. a higher order harmonic of a diode rectifier or a high power converter with a very low switching frequency), the active rectifier at hand can be disturbed significantly what could result in a protective shutdown.

With the resonance frequency shifting (RFS) feature it is possible to move the resonance to a different frequency where the noise will not interact and the converter works perfectly fine.

This feature was tested with a time domain simulation. The input filter parameters are given with $C_\mathrm{f} = 40\,\mu\mathrm{F}$, $L_\mathrm{f} = 500\,\mu\mathrm{H}$, $L_\mathrm{g} = 50\,\mu\mathrm{H}$ and $R_\mathrm{g} = 200\,\mathrm{m}\Omega$ what leads again to a resonance of the filter impedance at $f_0 = 1.1\,\mathrm{kHz}$ which is only weakly damped by the grid re-

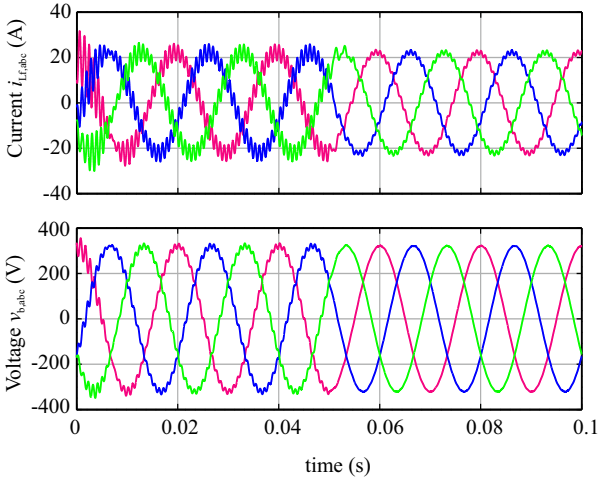

Figure 4.17: Time domain simulation of the active rectifier with the resonance frequency shifting (RFS) feature enabled.

sistance. A noise source is assumed to inject currents with an amplitude of 10 A and a frequency of 1200 Hz at the point of common coupling. The simulation results are depicted in Fig. 4.17.

The previously highly distorted bus voltage shows a smooth shape once the resonance frequency shifting feature is activated at $t = 0.05\,\mathrm{s}$ which simulates an additional capacitance of $C_{\mathrm{sim}} = 100\,\mu\mathrm{F}$. The harmonic currents are redirected to the remaining part of the grid since the impedance ratio has changed. Also the current in the filter inductance L_{f} is less distorted.

The filter performance is actually not changed by the virtual circuit element. The filter is designed to have the necessary attenuation in the EMI frequency range. This frequency range is far above the current control bandwidth and therefore, the virtual impedance has no influence on the achieved attenuation.

The implementation of the RFS concept in practice would need some additional features. First of all, it has to be detected fast enough that the input variables are distorted by an external noise source. This could be done with a PLL structure locked at the filter resonance frequency or with a method in the frequency domain such as a FFT or DFT.

If a resonance problem has been detected, the filter resonance should

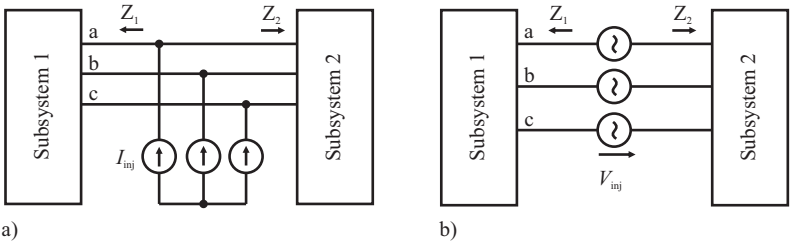

Figure 4.18: a) Parallel current injection, b) series voltage injection.

be slowly shifted in one or another direction. A search controller could move the resonance into the appropriate direction by altering the simulated impedance value. If the value change results in a decrease of the resonance amplitude, the impedance value is changed in the same direction again until an acceptable distortion level is achieved.

Additional constraints exist on the maximum achievable reactive element value. It is limited by the converter current limit and by the current control loop bandwidth.

4.5 Measurement system for impedance matrices in synchronous coordinates

Measuring the impedance matrices of subsystems is of major importance to determine system stability. Especially if no detailed design data of the involved converters is available a statement about stability is difficult to make. Measured impedances can help to resolve instability issues arising from resonance effects which could occur due to slightly damped filter resonances or interacting control loops of interconnected power electronic subsystems. In this chapter a measurement system is presented which is able to identify the subsystem impedance matrices in the synchronous reference frame. It is used to confirm the analytical model of the active rectifier derived in the last section and also to confirm the impact of the virtual impedance damping concept.

The implemented measurement system and the following derivation is based on the work of Huang et al. [185, 209, 210, 216].

There are basically two ways to inject a small signal disturbance into the three-phase system in order to obtain the necessary data for

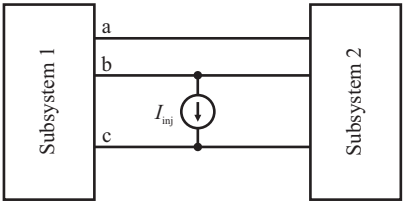

Figure 4.19: Parallel line-to-line current injection.

impedance identification: series voltage injection or parallel current injection (cf. Fig. 4.18).

This could be done with controlled linear amplifiers. Isolation is necessary what could be achieved with injection transformers or alternatively, the linear amplifiers have to be isolated on the supply side. Both concepts are very cost intensive due to the high necessary power rating. For series voltage injection, possibly large nominal currents of the system have to be considered and for parallel current injection the line voltage has to be tolerated. If injection transformers are used there is a limitation in the minimum frequency which can be injected [216].

It is simpler to rely on switched power electronics to generate the necessary disturbance. Parallel current injection could easily be implemented with a current regulated, PWM modulated three phase inverter. The switching frequency should be about a decade higher than the maximum measurement frequency. Therefore there is a certain limitation in the achievable measurement frequency.

An alternative to a current controlled inverter is a resistive chopper circuit. Here, the switching frequency can be chosen to be basically equal to the injection frequency. The measurement range can be increased roughly by a factor of 10 if the same switch technology as for the current controlled inverter is used. Huang showed in [216] that it is sufficient to use line-to-line current injection to identify all impedance elements (cf. Fig. 4.19). A chopper circuit is therefore very simple to implement and applicable even for medium voltage systems. The line-to-line chopper is chosen as the favourable injection device and implemented.

As a further option power electronics could be used to generate voltage or current steps in the direct and quadrature axis by connecting or disconnecting resistive or capacitive loads [217]. Sophisticated algo-

rithms for MIMO systems are necessary to identify the system parameters from the step responses. This procedure is not further considered here.

4.5.1 Theoretical background of impedance matrix identification in synchronous coordinates

In order to identify the 4 elements of an impedance matrix in the synchronous reference frame two independent measurements are necessary. Each measurement delivers two equations, one in d-direction and one in q-direction. The linear equation system that has to be solved is given by

$$\begin{aligned} v_{\mathrm{d},1} &= Z_{\mathrm{dd}} i_{\mathrm{d},1} + Z_{\mathrm{dq}} i_{\mathrm{q},1} \\ v_{\mathrm{q},1} &= Z_{\mathrm{qd}} i_{\mathrm{d},1} + Z_{\mathrm{qq}} i_{\mathrm{q},1} \\ v_{\mathrm{d},2} &= Z_{\mathrm{dd}} i_{\mathrm{d},2} + Z_{\mathrm{dq}} i_{\mathrm{q},2} \\ v_{\mathrm{q},2} &= Z_{\mathrm{qd}} i_{\mathrm{d},2} + Z_{\mathrm{qq}} i_{\mathrm{q},2}. \end{aligned} \tag{4.47}$$

There are several possibilities to get two linear independent measurements in the synchronous reference frame. The injected current space vector can either be a non-rotating vector with a cosine-modulated length or a rotating vector with fixed length. In the first case, two different angles relative to the reference frame can be chosen to get the independent measurements what corresponds to an input in two different directions of the MIMO system. In the second case, the rotation direction (positive or negative sequence) is changed to get the independent measurements. Also this type of excitation is related to different directions in the MIMO system.

If line-to-line injection is used, the injected currents are unbalanced. First, a current with the frequency $\omega_{\mathrm{m}} + \omega_{\mathrm{e}}$ is injected as

$$\begin{aligned} i_{\mathrm{inj,a}} &= 0 \\ i_{\mathrm{inj,b}} &= -\hat{I} \cos\left(\left(\omega_{\mathrm{m}} + \omega_{\mathrm{e}}\right) t\right) \\ i_{\mathrm{inj,c}} &= \hat{I} \cos\left(\left(\omega_{\mathrm{m}} + \omega_{\mathrm{e}}\right) t\right). \end{aligned} \tag{4.48}$$

The angular frequency of the synchronous reference frame is designated as ω_{e} and the measurement frequency is denoted as ω_{m}. If these currents are transformed to the synchronous reference frame, a positive sequence with frequency ω_{m} and a negative sequence with frequency

$(\omega_\mathrm{m} + 2\omega_\mathrm{e})$ are injected simultaneously given as

$$\begin{aligned} i_{\mathrm{inj,d}} = & \quad \frac{1}{\sqrt{3}}\hat{I}\sin\left(\omega_\mathrm{m} t\right) \; - \frac{1}{\sqrt{3}}\hat{I}\sin\left(\left(\omega_\mathrm{m} + 2\omega_\mathrm{e}\right) t\right) \\ i_{\mathrm{inj,q}} = & \underbrace{-\frac{1}{\sqrt{3}}\hat{I}\cos\left(\omega_\mathrm{m} t\right)}_{\text{pos. sequence}} \; \underbrace{-\frac{1}{\sqrt{3}}\hat{I}\cos\left(\left(\omega_\mathrm{m} + 2\omega_\mathrm{e}\right) t\right)}_{\text{neg. sequence}}. \end{aligned} \tag{4.49}$$

Assuming a linear small-signal behaviour of the subsystem, the voltage response will have the same frequency components in the synchronous reference frame. For the measurement only the component at frequency ω_m is of interest and it can be extracted using a FFT algorithm. In order to get the second, linear independent measurement, the currents

$$\begin{aligned} i_{\mathrm{inj,a}} &= 0 \\ i_{\mathrm{inj,b}} &= -\hat{I}\cos\left(\left(\omega_\mathrm{m} - \omega_\mathrm{e}\right) t\right) \\ i_{\mathrm{inj,c}} &= \hat{I}\cos\left(\left(\omega_\mathrm{m} - \omega_\mathrm{e}\right) t\right) \end{aligned} \tag{4.50}$$

are injected. In the synchronous reference frame, this is equivalent to injecting simultaneously a negative sequence with frequency ω_m and a positive sequence with frequency $(\omega_\mathrm{m} - 2\omega_\mathrm{e})$ given as

$$\begin{aligned} i_{\mathrm{inj,d}} = & \quad -\frac{1}{\sqrt{3}}\hat{I}\sin\left(\omega_\mathrm{m} t\right) \; - \frac{1}{\sqrt{3}}\hat{I}\sin\left(\left(\omega_\mathrm{m} + 2\omega_\mathrm{e}\right) t\right) \\ i_{\mathrm{inj,q}} = & \underbrace{+\frac{1}{\sqrt{3}}\hat{I}\cos\left(\omega_\mathrm{m} t\right)}_{\text{neg. sequence}} \; \underbrace{-\frac{1}{\sqrt{3}}\hat{I}\cos\left(\left(\omega_\mathrm{m} + 2\omega_\mathrm{e}\right) t\right)}_{\text{pos. sequence}}. \end{aligned} \tag{4.51}$$

Again, only the component at frequency ω_m is important and is extracted with the FFT. The two measurement sets are linearly independent and can be used to solve equation system 4.47 for the impedance matrix elements.

Now, the line-to-line injection current source is replaced by a resistive chopper circuit. The injected current will be rectangular and its amplitude is cosine-modulated with the fundamental frequency (cf. Fig. 4.20). The peak value is given by the implemented resistor value and the line-to-line voltage as

$$\hat{I} = \frac{\hat{V}_\mathrm{ll}}{R_\mathrm{chop}}. \tag{4.52}$$

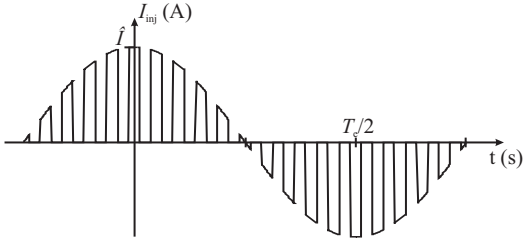

Figure 4.20: Injected current waveform with the resistive chopper circuit.

The injected current waveform can be described as a multiplication of the fundamental frequency current with the T_{sw}=$\omega_{sw}/2\pi$ periodic switching function $g_{sw}(t)$ as

$$I_{inj} = \hat{I} \cos(\omega_e t)\, g_{sw}(t), \tag{4.53}$$

with the switching function defined by

$$g_{sw}(t) = \begin{cases} 1 & -\frac{\pi}{2} \le \omega_{sw} t < \frac{\pi}{2} \\ 0 & -\pi \le \omega_{sw} t < -\frac{\pi}{2} \\ 0 & \frac{\pi}{2} \le \omega_{sw} t < -\pi \end{cases}. \tag{4.54}$$

The periodic switching function $g_{sw}(t)$ can be described with its Fourier expansion:

$$g_{sw}(t) = \frac{a_0}{2} + \sum_{k=1}^{\infty} a_k \cos(k\omega_{sw} t), \tag{4.55}$$

$$a_k = \frac{2}{T_{sw}} \int_{-T_{sw}/2}^{T_{sw}/2} g_{sw}(t) \cos(k\omega_{sw} t)\, dt = \begin{cases} \frac{2}{k\pi} \sin\left(\frac{k\pi}{2}\right) & k \neq 0 \\ 1 & k = 0 \end{cases}. \tag{4.56}$$

Therefore, the injected current can be written as

$$\begin{aligned} I_{inj} =& \hat{I} \cos(\omega_e t) \left(\frac{1}{2} + \frac{2}{\pi} \cos(\omega_{sw} t) - \frac{2}{3\pi} \cos(3\omega_{sw} t) + ... \right) \\ =& \hat{I} \left(\frac{1}{2} \cos(\omega_e t) + \frac{1}{\pi} \left(\cos\left((\omega_{sw} - \omega_e) t \right) + \cos\left((\omega_{sw} + \omega_e) t \right) \right) \right. \\ & \left. - \frac{1}{3\pi} \left(\cos\left((3\omega_{sw} - \omega_e) t \right) + \cos\left((3\omega_{sw} + \omega_e) t \right) \right) + ... \right). \end{aligned} \tag{4.57}$$

It was explained previously that for line-to-line injection, the two independent measurements are achieved by injecting subsequently currents with frequencies $(\omega_\mathrm{m} + \omega_\mathrm{e})$ and $(\omega_\mathrm{m} - \omega_\mathrm{e})$. With the chopper circuit, this can be achieved by setting the switching frequency of the chopper to $\omega_\mathrm{sw} = \omega_\mathrm{m} + 2\omega_\mathrm{e}$ and $\omega_\mathrm{sw} = \omega_\mathrm{m} - 2\omega_\mathrm{e}$.

Setting the chopper switching frequency to $\omega_\mathrm{sw} = \omega_\mathrm{m} + 2\omega_\mathrm{e}$, the injected current is given with

$$\begin{aligned} I_\mathrm{inj} =& \hat{I} \left(\frac{1}{2} \cos\left(\omega_\mathrm{e} t\right) + \frac{1}{\pi} \left(\cos\left(\left(\omega_\mathrm{m} + \omega_\mathrm{e}\right) t \right) + \cos\left(\left(\omega_\mathrm{m} + 3\omega_\mathrm{e}\right) t \right) \right) \right. \\ & \left. - \frac{1}{3\pi} \left(\cos\left(\left(3\omega_\mathrm{m} + 5\omega_\mathrm{e}\right) t \right) + \cos\left(\left(3\omega_\mathrm{m} + 7\omega_\mathrm{e}\right) t \right) \right) + \ldots \right). \end{aligned} \tag{4.58}$$

It is composed of several components, including among others the required component with frequency $(\omega_\mathrm{m} + \omega_\mathrm{e})$, which will be transformed into a positive sequence with frequency ω_m in the synchronous reference frame. Due the assumption of a linear small-signal behaviour of the system, the voltage response will have the same frequency components in the synchronous reference frame. For the measurement the component at frequency ω_m is important and is extracted with the FFT. The second injected current is obtained using the chopper frequency $\omega_\mathrm{sw} = \omega_\mathrm{m} - 2\omega_\mathrm{e}$ as

$$\begin{aligned} I_\mathrm{inj} =& \hat{I} \left(\frac{1}{2} \cos\left(\omega_\mathrm{e} t\right) + \frac{1}{\pi} \left(\cos\left(\left(\omega_\mathrm{m} - \omega_\mathrm{e}\right) t \right) + \cos\left(\left(\omega_\mathrm{m} - 3\omega_\mathrm{e}\right) t \right) \right) \right. \\ & \left. - \frac{1}{3\pi} \left(\cos\left(\left(3\omega_\mathrm{m} - 5\omega_\mathrm{e}\right) t \right) + \cos\left(\left(3\omega_\mathrm{m} - 7\omega_\mathrm{e}\right) t \right) \right) + \ldots \right). \end{aligned} \tag{4.59}$$

Again, the injected current is composed of several frequency components including the required component with frequency $(\omega_\mathrm{m} - \omega_\mathrm{e})$, which will be transformed into a negative sequence with frequency ω_m in the synchronous reference frame. The component at frequency ω_m is extracted with the FFT.

With these two linearly independent measurements the equation system can finally be solved for the impedance matrix components. For measurement frequencies where $\omega_\mathrm{sw} = \omega_\mathrm{m} - 2\omega_\mathrm{e}$ is negative, the absolute value $\omega_\mathrm{sw} = |\omega_\mathrm{m} - 2\omega_\mathrm{e}|$ gives the desired second independent measurement (cf. [216]).

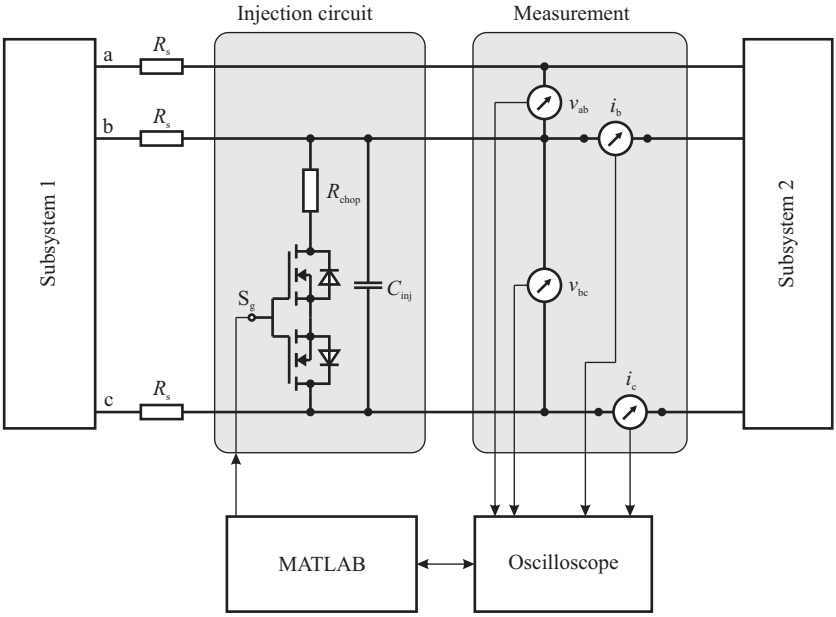

Figure 4.21: Implemented measurement system.

4.5.2 Measurement system setup

The implemented measurement system is based on the line-to-line chopper circuit proposed in [216]. It consists of an injection circuit, an oscilloscope capturing the measurement values and a laptop running MATLAB for data processing (cf. Fig. 4.21). Both, oscilloscope and the injection circuit are directly controlled by custom software based on MATLAB. A maximum measurement frequency of 150 kHz can be reached.

The injection circuit consists of two antiserial MOSFETs forming a bidirectional switch, low parasitic inductance power chopper resistors and a DSP platform controlling the switches and maintaining the communication with the control software.

The chosen MOSFETs (Infineon CoolMOS IPW90R800C3, 900V, 15A) are suitable for high speed switching and obtain very low switching losses. A small passive heatsink is sufficient to cool the switches. The MOSFETs are avalanche rated, therefore possible overvoltage spikes will

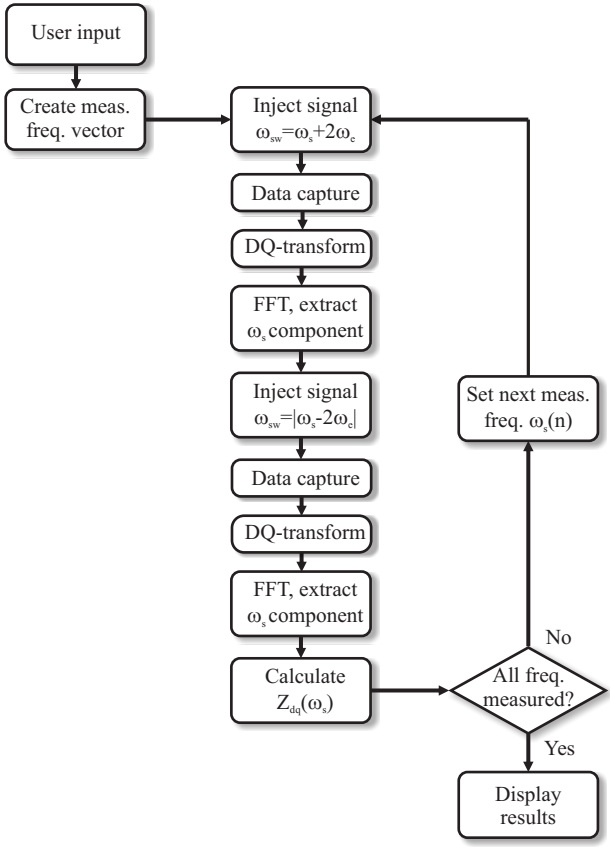

Figure 4.22: Control flow diagram of the measurement process.

not destroy the switches immediately. Additionally, a parallel branch of TVS diodes is able to limit the occurring overvoltage.

The chopper resistance R_{chop} is built with two high power resistors (Vishay RPS 500, 100 Ω, 500 W) mounted on a heatsink with forced air cooling. They can be connected in series or parallel to adapt the injected current amplitude in the range of $\hat{I} = \{2.8\,\text{A}, 5.6\,\text{A}, 11.2\,\text{A}\}$. Low inductance resistors ($L < 50\,\text{nH}$) are selected in order to reduce the overvoltage spikes during the switching transients. Additionally, a small capacitor $C_{\text{inj}} = 10\,\text{nF}$ was implemented in parallel to the injection

circuit in order to limit the overvoltage if both subsystems have an inductive input impedance.

In case the source is very stiff, the measurement of the load impedance is difficult and the resistors R_s can be connected in series to the source. Low inductance power resistors (Vishay RPS 500, 1 Ω, 500W) can be configured to build a resistance in the range of $R_\mathrm{s} = \{0.5\,\Omega, 1\,\Omega, 2\,\Omega\}$ what is sufficient for most applications.

The measurement process is controlled by software in MATLAB. The control flow diagram of the program is depicted in Fig. 4.22. An important point is the accurate data acquisition. Better results are obtained if a high sampling rate is used but the whole capturing process slows down considerably. A data set of 1MS for each trace has proven to be a good compromise between accuracy and processing time. It is necessary to capture an integer multiple of the fundamental period and the switching frequency period, therefore the measurement period and the sampling rate are adapted automatically during the measurement process.

There are several factors that impact the measurement accuracy. The most important ones are:

Mismatch between source and load impedance. If the source is very stiff with a low output impedance, it is difficult to measure the load impedance matrix. The injected current will only flow through the source and the voltage response is below the measurement tolerance. The problem is most often observed for low measurement frequencies. This problem can be solved by placing the resistors R_s in series to the source.

Different impedance component magnitudes. If some impedance matrix components are dominant (i.e. for the active rectifier $|Z_\mathrm{dd}| >> |Z_\mathrm{dq}|$ because of the decoupling terms in the control loop) it is difficult to measure the other components. The signal to noise ratio is not sufficient to get an accurate estimation of the small components. A better measurement can be achieved by increasing the injected current amplitude.

Low frequency harmonics in the bus voltage at multiples of the fundamental frequency. If there are low frequency harmonics in the measured voltage which are not related to the injected signal, the measurement results will be affected. However, the software allows to analyze the ground noise floor in order to automatically

compensate the low frequency harmonics and increase the measurement accuracy. As a second option, it is possible to omit all measurement frequencies which are multiples of the fundamental grid frequency.

High frequency noise in the bus voltages or currents. If there are high frequency harmonics related to the switching frequency of converters, the measurement results will be affected. The automatic noise analysis detects the affected frequency ranges and excludes them from the measurement.

Converter switching frequency. At measurement frequencies near and above the switching frequency of power electronic converters, the measurement is not correct because the impedance matrix in the synchronous reference frame will become time dependent.

Strong non-linear behavior. The non-linear behavior of the subsystems can impact the measurement accuracy. The theoretical solution is reducing the injected current amplitude in order to get closer to the small-signal approximation. Unfortunately, this reduces also the signal-to-noise ratio what adversely affects the measurement accuracy.

4.6 Experimental results

4.6.1 Impedance measurement

In this section some practical measurement results obtained with the impedance measurement system are presented in order to confirm the analytic converter models and the impact of the active damping methods.

Initially, a simple measurement with a passively damped LC-branch (cf. Fig. 4.23) has been conducted to test the basic functionality and the achievable accuracy. The values of the components are given with $L_\mathrm{f} = 2.54\,\mathrm{mH}$, $C_\mathrm{f} = 5.4\,\mu\mathrm{F}$, $C_\mathrm{d} = 5.4\,\mu\mathrm{F}$, $R_\mathrm{d} = 9\,\Omega$.

The comparison between the calculated (solid lines) and the measured (stars) characteristics of the LC-branch is depicted in Fig. 4.24. The impedance matrix components are identified with a good accuracy. In the high frequency range, the cross-coupling terms Z_dq and Z_qd are difficult to identify because the signal-to-noise ratio is not sufficient.

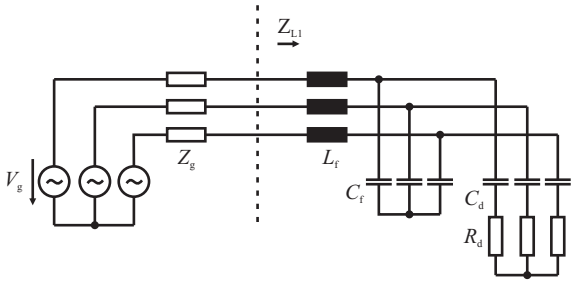

Figure 4.23: Damped LC branch used for the test measurement.

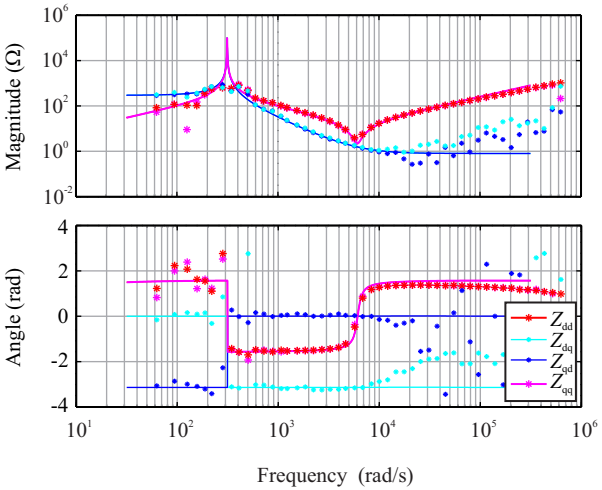

Figure 4.24: Calculated (solid lines) and measured (stars) components of the impedance matrix.

There are also some deviations in the low-frequency range because of the low source impedance of the regulated laboratory power supply, a linear amplifier with a voltage control bandwidth above 1 kHz. Consequently, the voltage response to the injected current is small and the signal-to-noise ratio is not sufficient to get an accurate estimation of the load impedance in this frequency range. The measurement accuracy could be increased by placing the resistors R_s in series to the source.

In a second step, the input impedance matrix components of the

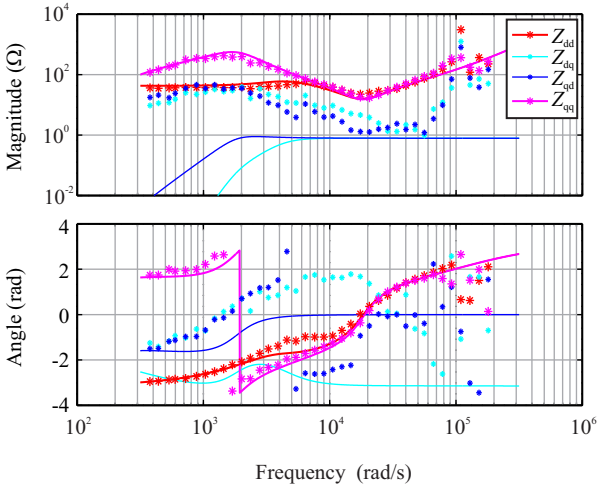

Figure 4.25: Calculated (solid lines) and measured (stars) components of the input impedance matrix of the active rectifier.

active rectifier were identified. The prototype of the 3LT²C (cf. Chapter 6) was configured to work as an active rectifier, using a boost inductance of $L_\mathrm{b} = 2.5\,\mathrm{mH}$ and a switching frequency of $f_\mathrm{sw} = 24\,\mathrm{kHz}$. The current control bandwidth was designed to be $\omega_\mathrm{b,i} = 2\,\mathrm{kHz}$ and the dc-link voltage control bandwidth was designed to be $\omega_\mathrm{b,u} = 300\,\mathrm{Hz}$. The operating point was set to $P_0 = 3.6\,\mathrm{kW}$.

The comparison between the calculated (solid lines) and the measured (stars) characteristics of the active rectifier is depicted in Fig. 4.25. Due to the decoupling control, the magnitude of the cross-coupling terms Z_dq and Z_qd is several times lower than that of the direct terms, and could not be identified accurately. Nevertheless, Z_dd and Z_qq show a good coincidence with the analytical model, except for the high frequency range near and above the switching frequency where the averaged analytical model is not valid. The small-signal model of the active rectifier is confirmed.

Finally, the impact of the active damping methods is confirmed with measurements of the input impedance matrix $\mathrm{Z_{L1}}$ at the point of common coupling (cf. interface 1 in Fig. 4.5). The implemented values of the input filter (cf. Fig. 4.1) are given with $L_\mathrm{f} = 2.5\,\mathrm{mH}$, $C_\mathrm{f} = 15.4\,\mu\mathrm{F}$, $C_\mathrm{d} = 5.4\,\mu\mathrm{F}$, $R_\mathrm{d} = 5.6\,\Omega$. With these values, the filter

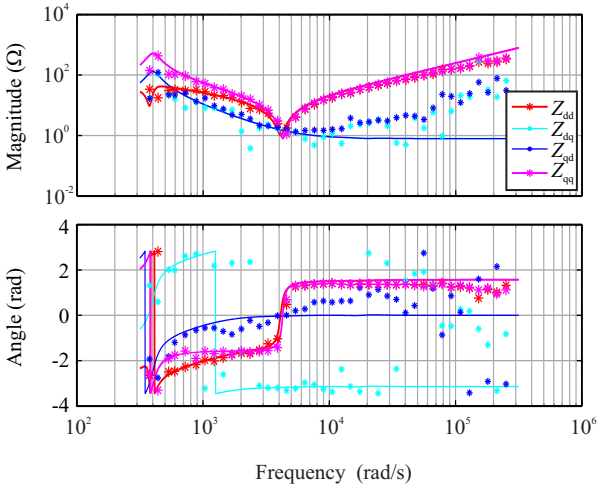

Figure 4.26: Calculated (solid lines) and measured (stars) components of the input impedance matrix Z_{L1} at interface 1.

resonance frequency is at $f_0 = 700\,\text{Hz}$, below the current controller bandwidth of 2kHz. As can be seen in Fig. 4.26, the components have been identified with a good accuracy, except of the cross-coupling terms in the high frequency range.

The series resonance frequency at the point of common coupling is shifted from $f_0 = 700\,\text{Hz}$ to $f_{0,\text{new}} = 500\,\text{Hz}$ with the simulation of an additional RC damping branch with $C_{\text{d,sim}} = 20\,\mu\text{F}$ and $R_{\text{d,sim}} = 7.5\,\Omega$. The measurement depicted in Fig. 4.27 confirms the calculated results. The shift in the resonance frequency can be seen in the direct and quadrature terms of the impedance matrix Z_{dd} and Z_{qq}.

The impact of active damping with the virtual resistance is depicted in Fig. 4.28. The impedance drop in Z_{dd} and Z_{qq} at the resonance frequency is reduced considerably. Again, the analytical model and the measured curves show a good coincidence.

4.6.2 Damping performance

The damping performance of both methods has also been verified experimentally in the time domain. In order to test the damping behaviour of the resonance frequency shifting method, a disturbing current was in-

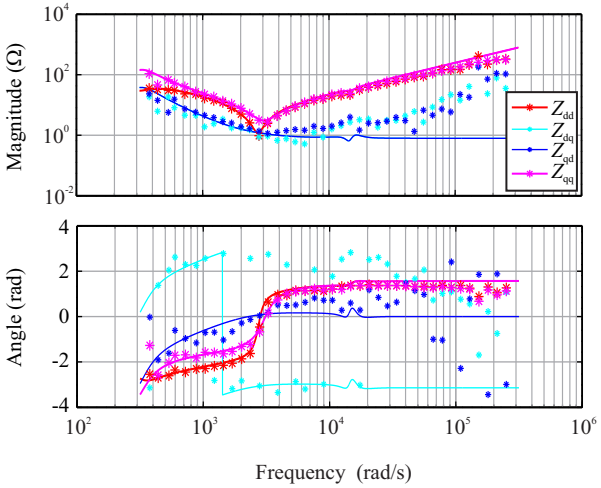

Figure 4.27: Calculated (solid lines) and measured (stars) components of the input impedance matrix $\mathrm{Z_{L1}}$ at interface 1 with the active rectifier simulating an additional RC damping branch of $C_{\mathrm{d,sim}} = 20\,\mu\mathrm{F}$ and $R_{\mathrm{d,sim}} = 7.5\,\Omega$.

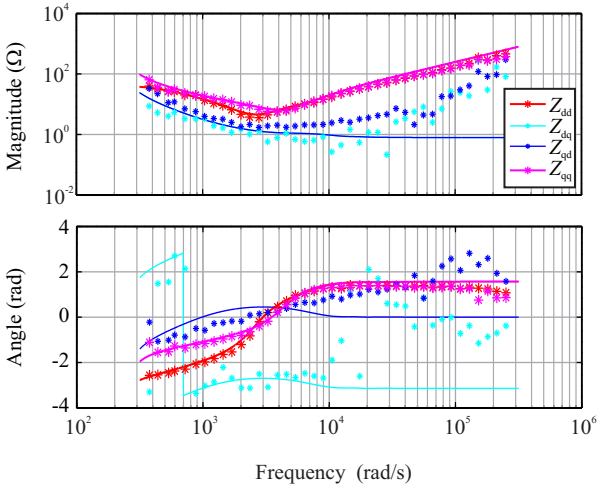

Figure 4.28: Calculated (solid lines) and measured (stars) components of the input impedance matrix $\mathrm{Z_{L1}}$ at interface 1 with the active rectifier implementing virtual resistor damping with $R_{\mathrm{d,sim}} = 20\,\Omega$.

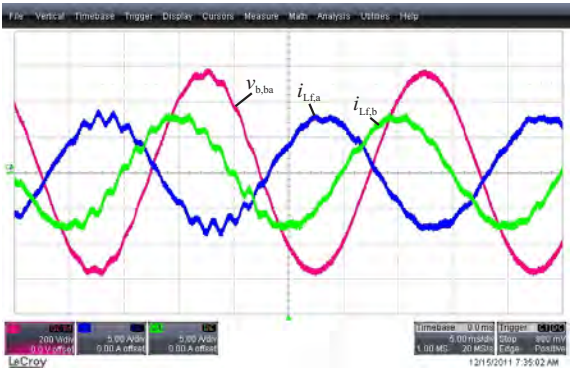

Figure 4.29: Experimental damping performance of the resonance frequency shifting method (time: 5 ms/div, currents: 5 A/div, voltage: 200 V/div).

jected at interface 1 with a frequency of $f_1 = 700\,\text{Hz}$. Initially, the line-to-line bus voltage $v_{\text{b,ba}}$ at interface 2 is heavily distorted (cf. Fig. 4.29). The active rectifier is still running but in a real application a protective shutdown of the converter could be initiated due to the excessive voltage harmonics. The virtual capacitor control loop is activated at the trigger point. The filter resonance frequency is shifted and the changed impedance ratio redirects the harmonic currents to the grid source. The bus voltage at interface 2 is smooth again and the operation of the active rectifier can continue.

The damping behaviour of the virtual resistor method was tested with a load step. First, the test was conducted with deactivated damping loop. The adapted EMI input filter is only minimally damped and therefore the line-to-line bus voltage at interface 2 shows severe oscillations after the load step at the trigger point (cf. Fig. 4.30).

For the second load step depicted in Fig. 4.31 the virtual resistor damping loop was activated. A virtual resistor of $R_{\text{sim}} = 20\,\Omega$ is simulated. As can be seen, the oscillations decay very fast after the load step. Even before the load step, the grid currents are much smoother and show lower distortion. The virtual resistor damping method has a convincing performance and is considered to be a practical alternative to passive damping networks.

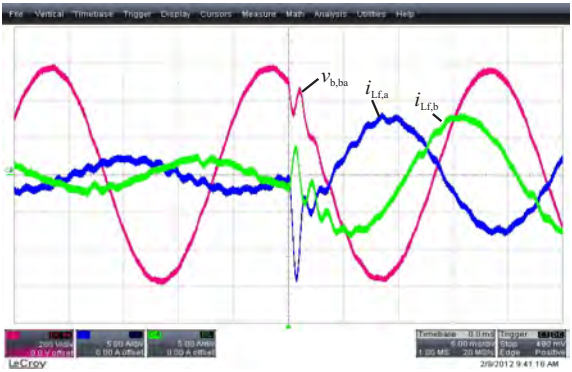

Figure 4.30: Severe oscillations of the bus voltage after the load-step with the weakly damped input filter (time: 5 ms/div, currents: 5 A/div, voltage: 200 V/div).

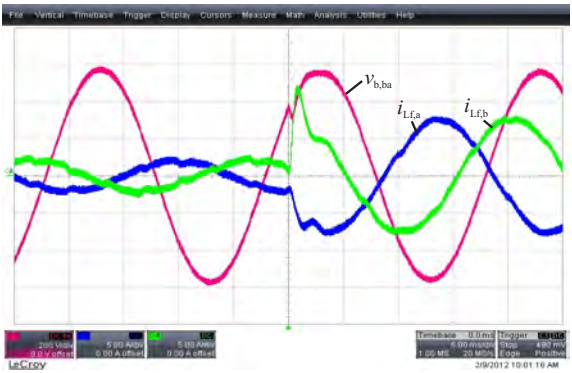

Figure 4.31: Experimental damping performance of the virtual resistor damping method (time: 5 ms/div, currents: 5 A/div, voltage: 200 V/div).

Chapter 5

System efficiency optimization

In the previous chapters it was shown that losses occur in all parts of a variable speed drive system.

There are loss components which are dependent on the switching frequency, such as the harmonic losses in the boost inductors, the harmonic losses in the induction machine and the switching losses of the converter. The harmonic losses in the boost inductors and in the induction machine decrease with increasing switching frequency whereas the switching losses increase with a higher switching.

Other loss components are more or less independent of the switching frequency if the influence of the changed system temperatures is neglected. The fundamental losses in the boost inductors belong to these loss components, furthermore the fundamental losses in the induction machine and the conduction losses of the converter. The fundamental losses of the machine can be influenced by loss optimal control schemes, especially in the low torque operating range. The loss optimal control scheme changes the terminal behaviour of the machine considerably as the stator voltage, the stator current and the current to voltage phase displacement angle are reduced. Therefore, there is a direct impact on the losses of the converter because its operating point is changed.

Additionally, the changed stator voltage amplitude has not only an impact on the fundamental machine losses but also on the harmonic machine losses due to a changed voltage spectrum. The optimal rotor

flux linkage derived in Chapter 2 considers only the fundamental losses in the induction machine, although various other loss components are affected. The question arises if the expression for the optimal rotor flux linkage is changed considerably by the inclusion of the other loss components.

Finally, also the converter topology itself has an impact on several loss components. The three different topologies suitable for low-voltage VSD systems presented previously have special characteristics concerning their fundamental losses and the output voltage spectrum. Therefore, also the choice of the converter topology has an impact on the losses in the remaining parts of the system.

In the previous chapters, the different loss components have been analyzed independently. As all models are available now, it is possible to combine them and minimize the total system losses. The holistic analysis of the complete system finally leads to the proposal of a modern, highly efficient low-voltage VSD system that combines a state-of-the-art converter topology with modern control methods, keeping the tradeoffs concerning complexity and costs in mind.

5.1 Optimal switching frequency

The choice of the converter switching frequency is influenced by several constraints. Among others, there is the audible noise emission, the filtering effort, the control performance requirements and finally, the losses of the total system. The losses of the boost inductors decrease with a higher switching frequency as well as the harmonic losses in the induction machine. Contrary, the switching losses of the converter increase. Therefore, there must be a certain switching frequency where the total system losses reach a minimum.

In a back-to-back converter configuration, the switching frequency of the rectifier stage and the inverter stage can be set independent of each other. Accordingly, it makes sense to treat both frequencies as independent variables that can be set freely.

In the following sections, the optimal switching frequency minimizing the losses is determined for the rectifier and the inverter stage. This is done in a pragmatic, numerical way as the location of the optimum and the absolute value of the obtained losses is dependent on experimentally determined loss characteristics of the induction machine and the boost inductors.

5.1.1 Rectifier stage

In order to find the switching frequency giving minimum total losses of the rectifier stage, mainly the losses in the boost inductors and the switching losses of the converter itself have to be considered. The losses in the remaining parts of the EMI filter are neglected, although changing the switching frequency also changes the required filter attenuation. It is assumed that the filter capacitance C_f is adapted to obtain the required attenuation and the filter inductance L_f is left unchanged. Therefore, the losses of the LC-filter stage are approximately independent of the switching frequency as the losses in the filter capacitors are very small anyway and the losses in the unchanged filter inductors are determined mainly by the fundamental values as the current ripple is small.

The boost inductance is designed according to Eq. 4.8 for the 2LC and with Eq. 4.9 for the 3LT²C and the 3LNPC². The current ripple Δi_pp is set to 20% of the nominal current.

In order to find scaling laws for the volume and losses of the boost inductors which are valid also for a variable switching frequency, first the derivation of the basic scaling laws for a thermally restricted inductor design presented in [161] is reconsidered. Although these scaling laws are valid for fundamental frequency excitation only, they provide the basis for the derivation of an extended model that includes switching frequency harmonic losses and consequently is valid also for a variable switching frequency. This extended model will be derived in a second step.

Considering only fundamental frequency excitation, the scaling laws for the boost inductor volume and losses can be found starting from the basic inductor design equation depending on the area product as

$$A_\mathrm{fe} \cdot A_\mathrm{w} = \frac{L \cdot \hat{i} \cdot I_\mathrm{rms}}{\hat{B} \cdot k_\mathrm{w} \cdot J_\mathrm{rms}}. \tag{5.1}$$

It means that if the peak current $\hat{i}$ is increased with letting the peak flux density $\hat{B}$ constant, the core cross-sectional area A_fe has to be increased. Similarly, if the rms current I_rms is increased with leaving the current density J_rms constant, the winding window A_w has to be increased (assuming the filling-factor k_w to be constant) as wires with a higher cross-sectional area are necessary. The design equation can also

be written as

$$L = \frac{\hat{B} \cdot k_\mathrm{w} \cdot J_\mathrm{rms}}{\hat{i} \cdot I_\mathrm{rms}} \cdot A_\mathrm{fe} \cdot A_\mathrm{w} \propto l^4. \tag{5.2}$$

The achievable inductance is proportional to l^4, where l is the basic length of the inductor. Without having further constraints, the inductance increases over-proportional to the inductor volume $V = l^3$.

Now, additional constraints concerning the allowed losses and the heat exchange with the environment are introduced. A very simple appoximation assumes that the thermal resistance is inversely proportional to the surface area of the inductor. Therefore, if a constant maximum surface temperature has to be kept, the losses are only allowed to increase proportional to the surface area of the inductor.

The ohmic losses can be expressed using the current density J_rms and the volume of the winding (skin effect and proximity effect are neglected)

$$P_\mathrm{o} = J_\mathrm{rms}^2 \cdot \rho \cdot k_\mathrm{w} \cdot A_\mathrm{w} \cdot l_\mathrm{w} \propto J_\mathrm{rms}^2 \cdot l^3. \tag{5.3}$$

For sinusoidal excitation, the iron losses can be approximated with the Steinmetz equation as

$$P_\mathrm{i} = k \cdot f^\alpha \cdot \hat{B}^\beta \cdot A_\mathrm{fe} \cdot l_\mathrm{e} \propto f^\alpha \cdot \hat{B}^\beta \cdot l^3. \tag{5.4}$$

For fundamental frequency excitation only, the frequency $f = 50\,\mathrm{Hz}$ is fixed, and the equation reduces to

$$P_\mathrm{i} \propto \hat{B}^\beta \cdot l^3. \tag{5.5}$$

The total losses are given by the sum of the core and the ohmic losses. Due to the thermal constraint, the total losses are allowed to increase only proportional to the inductor surface area as

$$P_\mathrm{tot} = P_\mathrm{o} + P_\mathrm{i} \propto l^2. \tag{5.6}$$

If the sum is restricted to be proportional to the surface area, each component is also restricted to be proportional to the surface area. The thermally restricted current density can then be written as

$$\begin{aligned} J_\mathrm{rms,tr}(l)^2 \cdot l^3 &\propto l^2, \\ J_\mathrm{rms,tr}(l) &\propto \frac{1}{\sqrt{l}} = l^{-1/2}. \end{aligned} \tag{5.7}$$

Similarly, for the thermally restricted flux density

$$\begin{aligned} \hat{B}_{\mathrm{tr}}(l)^{\beta} \cdot l^3 &\propto l^2, \\ \hat{B}_{\mathrm{tr}}(l) &\propto \frac{1}{l^{1/\beta}} = l^{-1/\beta}, \end{aligned} \tag{5.8}$$

applies. Interestingly, the peak flux density and the current density have to be reduced slightly when the inductor basic length is increased in order to keep the surface temperature constant.

The thermally restricted peak flux density and the current density can now be inserted into the design equation as

$$\begin{aligned} L \cdot \hat{i} \cdot I_{\mathrm{rms}} &= \hat{B}_{\mathrm{tr}} \cdot k_{\mathrm{w}} \cdot J_{\mathrm{rms,tr}} \cdot A_{\mathrm{fe}} \cdot A_{\mathrm{w}} \\ &\propto l^{-1/2} \cdot l^{-1/\beta} \cdot l^4 = l^{7/2-1/\beta}. \end{aligned} \tag{5.9}$$

Using $\beta = 2$ and a sinusoidal current the known proportionality of the volume to the inductance and the squared current (cf. [144]) is obtained as

$$V = l^3 \propto L \cdot I_{\mathrm{rms}}^2. \tag{5.10}$$

Consequently, with the applied constraints, the losses in the boost inductors for a fixed current are proportional to

$$P_{\mathrm{L}} \propto V^{2/3} \propto L^{2/3}. \tag{5.11}$$

In a second step, the impact of a switching frequency harmonic loss component can be analyzed. If the total losses of the inductor are restricted to grow only with the surface area, all summed loss components are restricted to grow only with the surface area.

The ohmic losses can be separated into low frequency and high frequency losses. Although the iron losses cannot be separated strictly into frequency components, the results obtained by doing so are sufficiently accurate if the switching frequency is much higher than the fundamental frequency. In [144], it is suggested to split the losses into the fundamental part and an additional part calculated with the harmonic flux density component at the switching frequency only, using the same Steinmetz parameters and neglecting the premagnetization due to the fundamental flux wave. The total losses are then given as

$$P_{\mathrm{tot}} = P_{\mathrm{o,LF}} + P_{\mathrm{i,LF}} + P_{\mathrm{o,HF}} + P_{\mathrm{i,HF}} \propto l^2. \tag{5.12}$$

The idea behind the next step is to make two inductor designs, one for the fundamental excitation and one for the switching frequency excitation. The fundamental frequency scaling law was already determined. All values are replaced with the fundamental frequency component as

$$L = \frac{\hat{B}_{(1),\mathrm{tr}} \cdot k_\mathrm{w} \cdot J_{(1),\mathrm{rms,tr}}}{\hat{\hat{i}}_{(1)} \cdot I_{(1),\mathrm{rms}}} \cdot A_\mathrm{fe} \cdot A_\mathrm{w} \propto l^4. \tag{5.13}$$

For the high frequency design, the values of the design equation are replaced with the switching frequency harmonic component as

$$L = \frac{\hat{B}_{(\mathrm{h}),\mathrm{tr}} \cdot k_\mathrm{w} \cdot J_{(\mathrm{h}),\mathrm{rms,tr}}}{\hat{\hat{i}}_{(h)} \cdot I_{(\mathrm{h}),\mathrm{rms}}} \cdot A_\mathrm{fe} \cdot A_\mathrm{w} \propto l^4. \tag{5.14}$$

While the unrestricted design equation stays the same also for the high frequency design, the loss components differ. The ohmic losses are determined by the high frequency content of the current density and are given as

$$\begin{aligned} J_{(\mathrm{h}),\mathrm{rms,tr}}(l)^2 \cdot l^3 &\propto l^2, \\ J_{(\mathrm{h}),\mathrm{rms,tr}}(l) &\propto \frac{1}{\sqrt{l}} = l^{-1/2}. \end{aligned} \tag{5.15}$$

Similarly, for the thermally restricted flux density applies

$$\begin{aligned} f_\mathrm{sw}^\alpha \cdot \hat{B}_{(\mathrm{h}),\mathrm{tr}}(l)^\beta \cdot l^3 &\propto l^2, \\ \hat{B}_{(\mathrm{h}),\mathrm{tr}}(l) &\propto l^{-1/\beta} \cdot f_\mathrm{sw}^{-\alpha/\beta}. \end{aligned} \tag{5.16}$$

This results in the high frequency design proportionality law as

$$\begin{aligned} L \cdot \hat{\hat{i}}_{(h)} \cdot I_{(\mathrm{h}),\mathrm{rms}} &= \hat{B}_{(\mathrm{h}),\mathrm{tr}} \cdot k_\mathrm{w} \cdot J_{(\mathrm{h}),\mathrm{rms,tr}} \cdot A_\mathrm{fe} \cdot A_\mathrm{w} \\ &\propto f_\mathrm{sw}^{-\alpha/\beta} \cdot l^{-1/2} \cdot l^{-1/\beta} \cdot l^4 = f_\mathrm{sw}^{-\alpha/\beta} \cdot l^{7/2-1/\beta}. \end{aligned} \tag{5.17}$$

Setting $\alpha = 1.5$ and $\beta = 2$, and considering the sinusoidal component at the switching frequency, the scaling law is

$$V_\mathrm{HF} \propto f_{sw}^{3/4} \cdot L \cdot I_{(\mathrm{h}),\mathrm{rms}}^2. \tag{5.18}$$

In contrast to the volume scaling law of the low frequency inductor design,

$$V_\mathrm{LF} \propto L \cdot I_{(1),\mathrm{rms}}^2, \tag{5.19}$$

the necessary volume not only increases with the inductance but also with the switching frequency. The inductance is designed to have a constant peak-to-peak current ripple. Therefore, the inductance is changed inversely proportional to the switching frequency as

$$L \propto \frac{1}{f_{\mathrm{sw}}}. \tag{5.20}$$

This leads to two different volume scaling laws for a variable switching frequency between the low frequency design, that actually neglects switching frequency harmonic losses and the high frequency design. Assuming constant fundamental current amplitude and constant switching frequency harmonic current amplitude, the two volume scaling laws depending on the switching frequency take the following forms

$$V_{\mathrm{HF}} \propto f_{sw}^{3/4} L \propto \frac{1}{\sqrt[4]{f_{\mathrm{sw}}}}, \tag{5.21}$$

$$V_{\mathrm{LF}} \propto L \propto \frac{1}{f_{\mathrm{sw}}}. \tag{5.22}$$

A more conservative volume scaling law is obtained if the switching frequency harmonic losses are considered, as the inductor volume cannot be reduced inversely proportional to the switching frequency anymore. Now, the high frequency and low frequency loss scaling laws can be deduced straightforward as

$$P_{\mathrm{HF}} \propto V_{\mathrm{HF}}^{2/3} \propto L^{2/3} f_{sw}^{1/2} \propto f_{sw}^{-1/6}, \tag{5.23}$$

$$P_{\mathrm{LF}} \propto V_{\mathrm{LF}}^{2/3} \propto L^{2/3} \propto f_{sw}^{-2/3}. \tag{5.24}$$

The two designs can be superimposed and the total losses are given as

$$P_{\mathrm{tot}} = P_{\mathrm{LF}} + P_{\mathrm{HF}} = k_{\mathrm{LF}} \cdot L^{2/3} + k_{\mathrm{HF}} \cdot L^{2/3} f_{sw}^{1/2}. \tag{5.25}$$

The constants $k_{\mathrm{LF}} = 1208\,\mathrm{W/H}^{2/3}$ and $k_{\mathrm{HF}} = 13.5\,\mathrm{W/(H}^{2/3} \cdot \mathrm{Hz}^{1/2})$ were determined from [218], where an optimized EMI filter design was presented including experimental measurements. A standard shape boost inductor with laminated steel sheets (grain-oriented steel M165-35S) was designed for $L_{\mathrm{b}} = 2.54\,\mathrm{mH}$ and tested under 2-level rectifier operation with $f_{\mathrm{sw}} = 8\,\mathrm{kHz}$ and $\hat{I}_{\mathrm{n}} = 20.5\,\mathrm{A}$, giving the desired current ripple of 4 A. The losses in one boost inductor were calculated to be 45 W and confirmed with measurements. The calculation showed that

the high frequency losses and the low frequency losses have approximately the same value. Therefore, the total losses have been partitioned equally to the high frequency and the low frequency losses to determine the two constants.

The total losses of the three boost inductors, the converter switching losses, and their sum are depicted in Fig. 5.1a for the 2LC, in Fig. 5.1b for the 3LT²C and in Fig. 5.1c for the 3LNPC². The switching losses have been calculated for PFC rectifier operation at nominal operating point ($P_0 = 10\,\mathrm{kW}$, $V_\mathrm{dc} = 650\,\mathrm{V}$, $\hat{I}_\mathrm{n} = 20.5\,\mathrm{A}$, $\hat{V}_\mathrm{n} = 325\,\mathrm{V}$), using the switching loss optimal clamping scheme. The minimum of the total losses depending directly on the switching frequency are obtained with $f_\mathrm{sw,opt} = 9\,\mathrm{kHz}$ for the 2LC, with $f_\mathrm{sw,opt} = 16\,\mathrm{kHz}$ for the 3LT²C and with $f_\mathrm{sw,opt} = 22\,\mathrm{kHz}$ for the 3LNPC². Due to the smaller switching losses, the optimal switching frequency for minimum losses shifts towards higher values for the 3-level converters. It has to be mentioned that for higher switching frequencies $f_\mathrm{sw} > 22\,\mathrm{kHz}$, a different core material could lower the inductor losses.

The exact location of the optimum is dependent on the switching loss energies of the switches, the phase current, the dc-link voltage, the modulation index, and the materials and manufacturing method of the boost inductors. The numerical results obtained here have been calculated for rated power of the system and can be seen as a guideline for choosing the switching frequency of the rectifier stage for systems having similar power ratings.

Choosing the optimal switching frequency and adapting the boost inductance to obtain the same current ripple for all three topologies allows to reduce the losses in the boost inductors by 39% for the 3LT²C and by 46% for the 3LNPC² compared to the 2LC in this specific case. This is much more than the 25% obtained when the switching frequency is chosen to be equal for all topologies (cf. Section 4.1). The value of the boost inductors could be reduced by 63% for the 3LT²C and even by 73% for the 3LNPC² compared to the 2LC. This is again much more than the reduction of 33% if the switching frequency is equal for all topologies. The reduction of the boost inductor volume can be directly obtained with

$$V \propto P_\mathrm{tot}^{3/2}. \tag{5.26}$$

Therefore, the volume of the boost inductors can be reduced by 52% for the 3LT²C and by 60% for 3LNPC² compared to the 2LC.

If the power density of the rectifier stage is considered, not only the

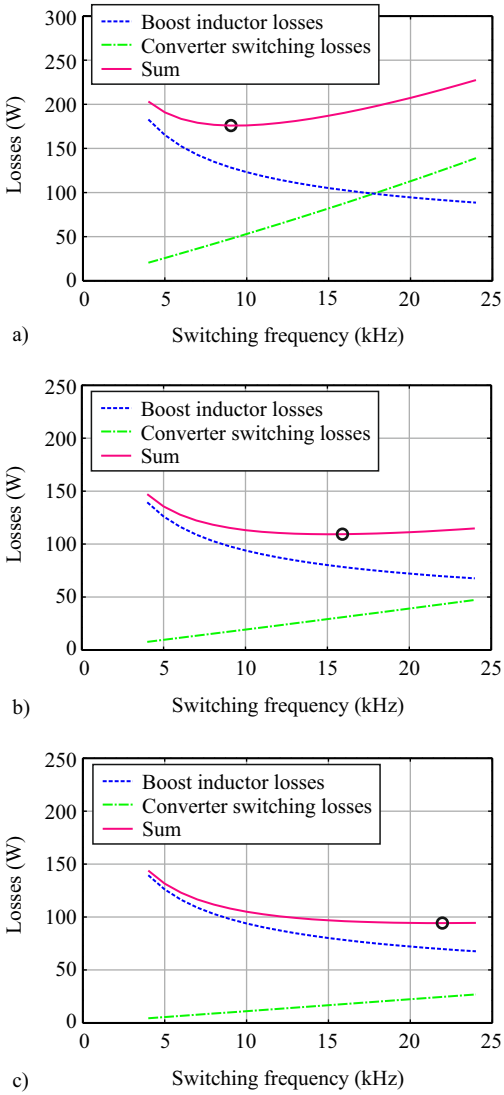

Figure 5.1: Optimization of the switching frequency dependent loss components of the rectifier stage for a) 2LC, b) 3LT^{2}C, and c) 3LNPC^2.

volume of the boost inductors but also the volume of the remaining parts of the EMI filter cannot be neglected. Changing the switching frequency also changes the necessary attenuation. A multidomain optimization of the EMI filter of a rectifier stage was presented in [218]. The result is a Pareto-front with optimal designs weighting filter losses and filter volume differently. In a further step, also the volume of the rectifier stage, mainly determined by the heatsink volume and the dc-link capacitors volume could be included into the optimization but this is beyond the scope of this thesis.

5.1.2 Inverter stage

In a similar way, the optimal switching frequency of the inverter stage can be determined. The loss components depending on the switching frequency are given by the harmonic machine losses and the switching losses of the converter. The harmonic machine losses have been extensively discussed in Section 2.2. It was shown that the harmonic losses decrease with a higher switching frequency but stagnate on a certain level due to the dominant eddy-current based iron losses (cf. Fig. 2.34).

The exact loss characteristics are different for each machine. Therefore, the optimal switching frequency is determined with the experimentally measured data of the 7.5 kW test induction machine. In order to find the optimal switching frequency, which results in minimum losses of the overall system, the harmonic machine losses, the converter switching losses, and their sum are depicted in Fig. 5.2a for the 2LC, in Fig. 5.2b for the 3LT²C and in Fig. 5.2c for the 3LNPC². The switching losses have been calculated for rated speed and torque using a fixed loss optimal clamping modulation scheme for a current lag of 30°. The harmonic machine losses have been measured at no-load condition. Although there are some variations of the harmonic losses if the machine is working under a certain load condition, they are small for higher switching frequencies and therefore are neglected (cf. [72]).

The minimum of the total switching frequency dependent losses is at $f_{\mathrm{sw}} = 6\,\mathrm{kHz}$ for the 3LT²C, at $f_{\mathrm{sw}} = 7\,\mathrm{kHz}$ for the 2LC, and at $f_{\mathrm{sw}} = 8\,\mathrm{kHz}$ for the 3LNPC². The minimum occurs for all converters at a relatively low switching frequency. A higher switching frequency therefore does not reduce the total losses, what can be explained with the constant part of the harmonic machine losses due to the eddy-current iron losses.

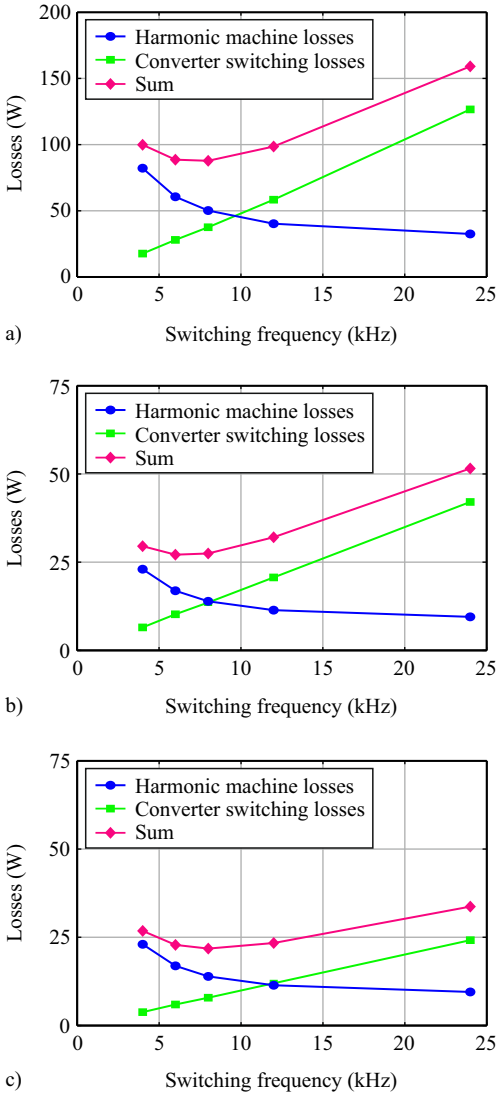

Figure 5.2: Optimization of the switching frequency dependent loss components for a) 2LC, b) 3LT^{2}C, and c) 3LNPC^2. The harmonic machine losses are measured during nearly no-load condition and the switching losses are calculated for nominal operation.

In the boost inductor case, the necessary inductance can be decreased with increasing switching frequency, and therefore the losses in the iron core and the conductors are also decreased as the whole component can be built with fewer turns and less core material. Not only the harmonic losses due to the switching frequency are reduced, but also the fundamental losses of the boost inductor are reduced. Contrary, the machine design is left unchanged and increasing the switching frequency has only a small effect on the total losses. The physical dimensions of the machine are mainly determined by the torque requirement and cannot be reduced if a higher switching frequency is chosen. Consequently, there is also no reduction of fundamental losses.

A higher switching frequency should only be chosen if necessary for improving the dynamic performance or reducing the acoustic noise (the acoustic noise emission of the load machine is already reduced with the 3-level converter waveform compared to the 2-level converter waveform with the same switching frequency). A further reason for choosing a higher switching frequency is the operation of high speed machines where an output voltage with a high fundamental frequency has to be generated. There, the power density of the machine is increased with higher rotor speeds.

If only standard induction machines are considered and output filers are neglected, the power density of the inverter stage is adversely affected by a higher switching frequency. As the switching losses increase, the volume of the heatsink has to be increased. The dc-link capacitance can not be changed as it is determined by the energy storage requirement for ride-through operation or by balancing considerations.

Although this approach allows no statements for the optimal switching frequency of an arbitrary machine and converter combination, the results will potentially be similar for comparable machines and power ratings.

5.2 Loss optimal control

The major part of the overall system losses is given by the machine losses at the fundamental frequency that can be minimized using loss optimal control schemes. These control schemes have again an impact on the inverter efficiency because the operating point is changed.

It was explained in Section 2.1 that reducing the rotor flux during low torque operation can reduce the fundamental losses $P_{\mathrm{loss,m}}$ in the

machine. They are a function of the operating point and the rotor flux level defined as

$$P_{\mathrm{loss,m}} = f(\omega_{\mathrm{R}}, T_{\mathrm{e}}, \Psi_{\mathrm{r}}). \tag{5.27}$$

At the same time, the supplied stator voltage is reduced, the stator current is reduced and the voltage to current phase displacement angle is reduced (cf. Fig. 2.9 - Fig. 2.11). This has a direct impact on the inverter losses $P_{\mathrm{loss,i}}$ as the operating point of the inverter stage is changed according to

$$P_{\mathrm{loss,i}} = f(\hat{V}_1, \hat{I}_1, \varphi_1) = f(\omega_{\mathrm{R}}, T_{\mathrm{e}}, \Psi_{\mathrm{r}}). \tag{5.28}$$

During the analysis of the converter efficiency in Section 3.5, it was shown that the converter efficiency is negatively affected if the output voltage is reduced, as the efficiency decreases (cf. Fig. 3.28). Contrary, the converter efficiency increases if the output current and the voltage to current phase displacement angle are reduced. Therefore, to a certain extent, there will be a compensation of these two effects.

A further aspect are the harmonic machine losses $P_{\mathrm{h,m}}$. As was shown in Section 2.2, the harmonic machine losses are also dependent on the stator voltage as

$$P_{\mathrm{h,m}} = f(\hat{V}_1) = f(\omega_{\mathrm{R}}, T_{\mathrm{e}}, \Psi_{\mathrm{r}}). \tag{5.29}$$

If the stator voltage is reduced starting from the nominal voltage, there will be initially an increase of the harmonic losses for the 2LC, whereas a decrease of the losses for the 3LT^{2}C and the 3LNPC^2 will occur (cf. Fig. 2.40).

As can be seen, the optimal rotor flux linkage that minimizes only the fundamental machine losses is not necessarily the best choice. If the complete VSD system is considered, there are additional loss components that are indirectly affected by changing the rotor flux level. The question arises if it is necessary to include these additional loss components in the efficiency optimization. There is no useful analytical solution to this optimization problem but the system wide optimal rotor flux linkage can be found with numerical methods and could be stored in a lookup table of the DSP. Alternatively, a search controller could be used that minimizes the input power of the converter and therefore in principle includes all loss components of the complete system (cf. Section 2.1).

It has to be mentioned that the converter losses and the harmonic machine losses are small compared to the fundamental machine losses,

especially for the 3-level topologies. E.g. the 3LT²C reaches 99% efficiency at $f_{sw} = 8\,\text{kHz}$ over a wide operating range and the induced harmonic machine losses would be below 15 W. The fundamental losses of the induction machine are much higher and can be reduced considerably, especially for the low torque range $T_e \leq 20\%T_n$. There, it is possible to increase the electrical efficiency of the machine from 85% to 92% at rated speed.

It is shown in the next sections that the missed loss reduction potential when using the optimal rotor flux linkage for maximum machine efficiency instead of the true solution for maximum system efficiency is very small. It is therefore acceptable to neglect the additional loss components and operate the machine with the analytical optimal rotor flux linkage according Eq. 2.24.

5.2.1 Inverter efficiency in machine operating points

The inverter efficiency in the operating points defined by the machine can be calculated with the loss calculation algorithm.

The switching frequency was set to $f_{sw} = 8\,\text{kHz}$ what is near the optimal switching frequency of the inverter stages for all three topologies. The inverter efficiency is depicted in Fig. 5.3a for the 2LC, in Fig. 5.3b for the 3LT²C, and in Fig. 5.3c for the 3LNPC², for operation with the rated rotor flux linkage and with the optimal rotor flux linkage for maximum machine efficiency.

For low torques, the inverter efficiency is positively affected by using the optimal rotor flux linkage. For high rotor speeds, there is a torque range ($T_e = 5 - 15\,\text{Nm}$) where the inverter efficiency is slightly reduced. The effect can be explained with the reduction of the stator voltage and a slight increase of the stator current in this torque range (cf. Fig. 2.10), both leading to a reduced inverter efficiency. The reduction of the phase displacement angle cannot fully compensate this negative effect.

It can be further noticed that the efficiency of the 3LT²C is also very high in the low power range when operating at reduced speeds.

5.2.2 Loss optimal control including inverter stage

Combining the inverter efficiency η_i and the electrical machine efficiency $\eta_{m,el}$ (excluding friction), the total efficiency (excluding rectifier stage)

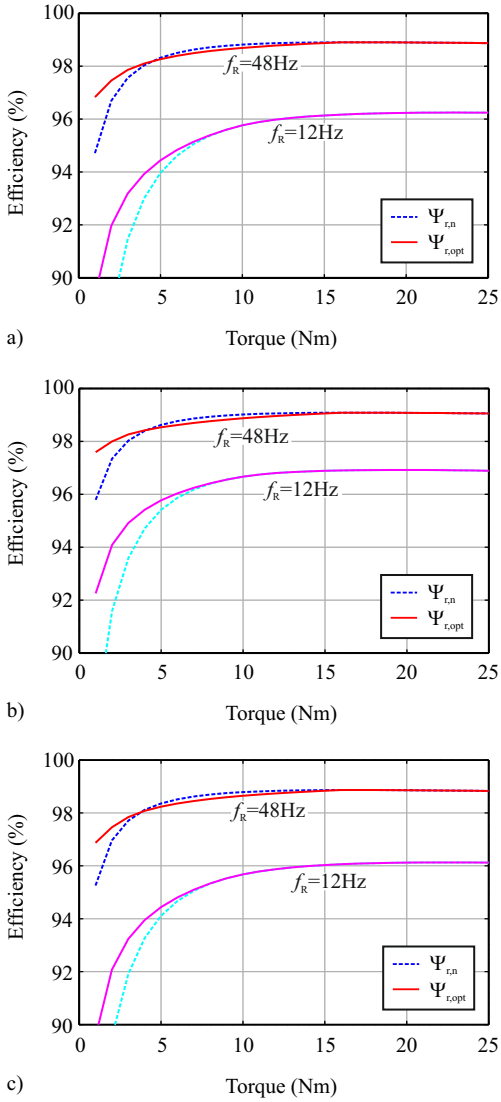

Figure 5.3: Inverter efficiency in machine operating points for a) 2LC, b) 3LT^{2}C, and c) 3LNPC^2.

is obtained with

$$\eta_{\text{total}} = \eta_{\text{i}} \cdot \eta_{\text{m,el}} = \frac{P_{\text{out,i}}}{P_{\text{out,i}} + P_{\text{loss,i}}} \cdot \frac{P_{\text{out,m}}}{P_{\text{out,i}}}. \tag{5.30}$$

Obviously, the inverter has to supply the electrical output power $P_{\text{out,m}}$ of the machine, the fundamental machine losses $P_{\text{loss,m}}$ and the harmonic machine losses $P_{\text{h,m}}$ and is given as

$$P_{\text{out,i}} = P_{\text{out,m}} + P_{\text{loss,m}} + P_{\text{h,m}}. \tag{5.31}$$

Alternatively, the harmonic machine losses can be accounted to the inverter efficiency what results in the same total efficiency as the above definition. By doing so, the electrical machine efficiency is defined by the fundamental losses only and is consistent with the definition used to derive the optimal rotor flux linkage $\Psi_{\text{r,opt}}$. The total efficiency is then given as

$$\begin{aligned} \eta_{\text{total}} &= \eta_{\text{i}}^{*} \cdot \eta_{\text{m,el}}^{*} \\ &= \frac{P_{\text{out,m}} + P_{\text{loss,m}}}{P_{\text{out,m}} + P_{\text{loss,m}} + P_{\text{h,m}} + P_{\text{loss,i}}} \cdot \frac{P_{\text{out,m}}}{P_{\text{out,m}} + P_{\text{loss,m}}} \\ &= \frac{P_{\text{out,m}}}{P_{\text{out,m}} + P_{\text{loss,m}} + P_{\text{h,m}} + P_{\text{loss,i}}}. \end{aligned} \tag{5.32}$$

Using a numerical approach, it is possible to find the global optimal rotor flux linkage $\Psi_{\text{r,opt,g}}$ that maximizes the total system efficiency. This was done for all three topologies. As already anticipated, the difference between $\Psi_{\text{r,opt,g}}$ and $\Psi_{\text{r,opt}}$ is very small and the difference in achievable efficiency is even smaller. As an example, the achievable total efficiency with the 2LC is depicted in Fig. 5.4. The difference is nearly not visible.

The absolute efficiency difference is defined as

$$\Delta\eta = \eta_{\text{total}}(\Psi_{\text{r,opt,g}}) - \eta_{\text{total}}(\Psi_{\text{r,opt}}) \tag{5.33}$$

It is found that an efficiency improvement of only $\Delta\eta \leq 0.2\%$ could be achieved with the 2LC and of $\Delta\eta \leq 0.1\%$ with the 3LT^{2}C and the 3LNPC^2 over the interesting range of machine operating points. To visualize the difference, the machine efficiency, the converter efficiency and the total efficiency are plotted in Fig. 5.5 for the 2LC at a rotor frequency of $f_{\text{R}} = 48\,\text{Hz}$ and a torque of $T_{\text{e}} = 8\,\text{Nm}$ and a variable rotor

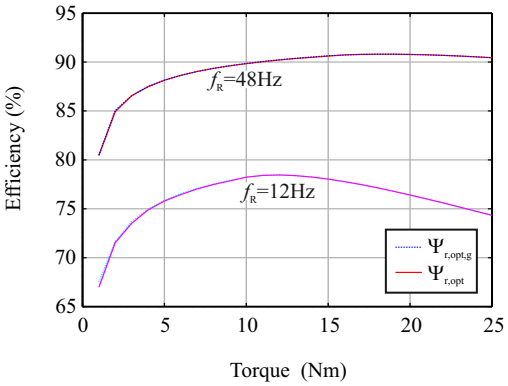

Figure 5.4: Difference between reachable total efficiency with the global optimal rotor flux linkage and the machine optimal rotor flux linkage for the 2LC.

flux linkage. The chosen operating point is in the middle of the torque range where the inverter efficiency actually decreases when using the optimal rotor flux linkage. The total efficiency is dominated by the subsystem with the lower efficiency what is clearly the induction machine. Therefore, $\Psi_{r,opt,g}$ is very close to $\Psi_{r,opt}$. As the efficiency maximum is very flat, the difference in the achievable efficiency is negligibly small. Although the inverter efficiency is decreased in some operating points, the total system efficiency is still maximized with the optimal rotor flux linkage.

Concluding, the optimal rotor flux linkage $\Psi_{r,opt}$ defined by Eq. 2.24 is suitable to optimize the machine efficiency and the converter efficiency as well. For low-voltage VSD systems, it is not necessary to include the losses of the inverter stage in the optimization as the efficiency gain is negligibly small.

5.3 Total VSD system efficiency

In order to calculate the total VSD efficiency, additional loss components have to be considered. These are the losses in the rectifier stage, the losses in the boost inductors and the mechanical friction and windage losses of the machine. No further loss components are considered.

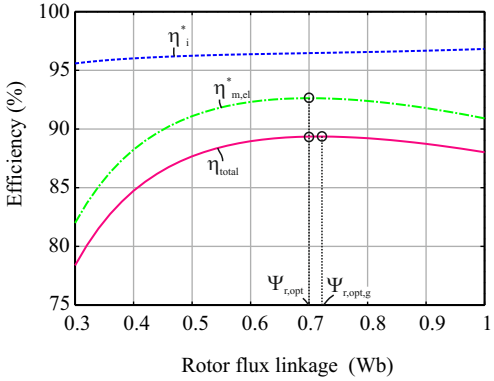

Figure 5.5: Machine efficiency, inverter efficiency and total efficiency depending on the rotor flux linkage for the 2LC at $f_\mathrm{R} = 48\,\mathrm{Hz}$ and $T_\mathrm{e} = 8\,\mathrm{Nm}$.

The efficiency improvements achieved for the machine and for the inverter stage have a positive impact on the efficiency of all following subsystems in the supply chain. If less power has to be processed, the current amplitude of the rectifier is reduced and therefore, the efficiency increases. The same effect can be observed with the losses in the boost inductors. There is a kind of multiplication effect increasing the efficiency gain throughout the whole energy flow chain.

The losses in the boost inductors are adapted in order to get the dependency on the fundamental current amplitude. As the current ripple is not affected, only the low-frequency loss component is changed. A simple quadratic dependency is assumed as the low-frequency losses are mainly due to ohmic losses. Accordingly, the boost inductor losses are modelled as

$$P_\mathrm{loss,Lb} = 3 \cdot \left(k_\mathrm{LF} \cdot L_\mathrm{b}^{2/3} \cdot \frac{\hat{I}_1^2}{\hat{I}_\mathrm{n}^2} + k_\mathrm{HF} \cdot L_\mathrm{b}^{2/3} f_\mathrm{sw}^{1/2} \right). \tag{5.34}$$

In a first step, the pure electrical efficiency (excluding friction and windage losses) of the VSD system is calculated for operation with the rated and with the optimal rotor flux linkage for all topologies. The

total VSD system efficiency is then defined as

$$\begin{aligned}\eta_{\text{total,el}} &= \underbrace{\frac{P_{\text{out,Lb}}}{P_{\text{in,Lb}}}}_{\eta_{\text{Lb}}} \cdot \underbrace{\frac{P_{\text{out,r}}}{P_{\text{out,Lb}}}}_{\eta_{\text{r}}} \cdot \underbrace{\frac{P_{\text{out,i}}}{P_{\text{out,r}}}}_{\eta_{\text{i}}} \cdot \underbrace{\frac{P_{\text{out,m}}}{P_{\text{out,i}}}}_{\eta_{\text{m,el}}} \\ &= \frac{P_{\text{out,m}}}{P_{\text{out,m}} + P_{\text{loss,m}} + P_{\text{h,m}} + P_{\text{loss,i}} + P_{\text{loss,r}} + P_{\text{loss,Lb}}}.\end{aligned} \tag{5.35}$$

The total efficiency (excluding friction and windage) is depicted in Fig. 5.6. The switching frequency of the inverter stage is set to $f_{\text{sw,i}} = 8\,\text{kHz}$ for all three topologies whereas for the rectifier stage, the switching frequency is set to $f_{\text{sw,r}} = 8\,\text{kHz}$ for the 2LC, to $f_{\text{sw,r}} = 16\,\text{kHz}$ for the 3LT²C and to $f_{\text{sw,r}} = 24\,\text{kHz}$ for the 3LNPC², what is near the optimal switching frequency in all three cases. The boost inductance is adapted accordingly to obtain a peak-to-peak current ripple of 4 A with all three topologies.

As described in Section 3.7, it is not possible to have switching loss optimal clamping at the same time for the rectifier stage and for the inverter stage if the two 3-level topologies are considered. This is due to the necessity to balance the partial dc-link voltages, either with the rectifier stage or with the inverter stage. To account for this condition, switching loss optimal clamping (with a fixed 30° lagging clamping window) is assumed only for the inverter stage. The losses of the rectifier stage are calculated as the mean value of the losses between optimal clamping and worst case clamping (always the phase with the highest instantaneous current value is switched). This is a reasonable assumption as due to the different fundamental frequencies of the input stage and the output stage, these two conditions will occur repetitively over time and the switching losses can be determined as their average value. Accordingly, the switching losses of the rectifier stage will increase slightly for the 3LT²C and the 3LNPC². Differently, the losses of the 2LC are calculated with switching loss optimal clamping for both, the rectifier and the inverter stage as there is no need to balance the dc-link voltages.

As could be expected, the total VSD system efficiency is further reduced for all three topologies, although the additional loss components are small. Especially the rectifier stage works with a high efficiency as the voltage is fixed to the nominal grid voltage and the power factor is near unity.

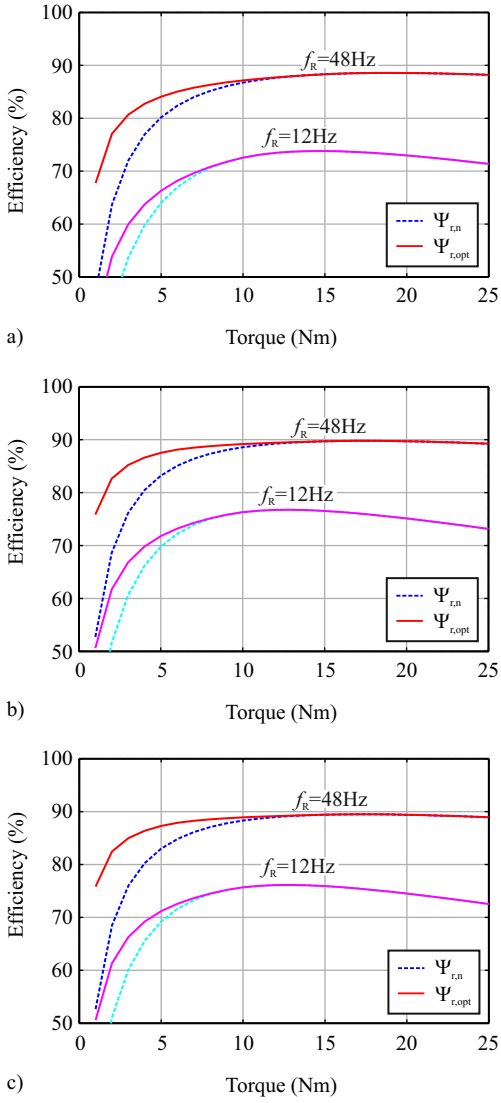

Figure 5.6: Total VSD system efficiency excluding friction and windage losses for a) 2LC, b) 3LT^{2}C, and c) 3LNPC^2.

The efficiency gain with the optimal rotor flux linkage is remarkable in the low torque range. For all three topologies, the total VSD system efficiency can be increased by more than 5% in the low torque range ($T_\mathrm{e} \leq 20\% \cdot T_\mathrm{n}$) at rated speed. Comparing the three converter topologies, the VSD system based on the 3LT²C shows the highest efficiency over all operating points. Also in the low power range at reduced rotor speeds, the efficiency can be kept high.

Friction and windage losses

Conventional electrical machines suffer from friction losses. Additionally, many induction machines are equipped with a shaft-mounted fan for self-cooling. These friction and windage losses are relatively high, especially at rated speed, and reduce the machine efficiency and the total VSD system efficiency.

Friction and windage losses of the induction machine at hand have been measured to be $P_\mathrm{fric,n} = 285\,\mathrm{W}$ at rated speed. The dependency on the rotor speed was determined experimentally and can be modelled with

$$P_\mathrm{fric}(\omega_\mathrm{R}) = P_\mathrm{fric,n} \cdot \left(\frac{\omega_\mathrm{R}}{\omega_\mathrm{R,n}} \right)^{1.613} \tag{5.36}$$

Considering this additional loss component, the total VSD system efficiency is reduced further and is finally given with

$$\eta_\mathrm{total} = \underbrace{\frac{P_\mathrm{out,Lb}}{P_\mathrm{in,Lb}}}_{\eta_\mathrm{Lb}} \cdot \underbrace{\frac{P_\mathrm{out,r}}{P_\mathrm{out,Lb}}}_{\eta_\mathrm{r}} \cdot \underbrace{\frac{P_\mathrm{out,i}}{P_\mathrm{out,r}}}_{\eta_\mathrm{i}} \cdot \underbrace{\frac{P_\mathrm{out,m}}{P_\mathrm{out,i}}}_{\eta_\mathrm{m,el}} \cdot \underbrace{\frac{P_\mathrm{out,mech}}{P_\mathrm{out,m}}}_{\eta_\mathrm{fric}} . \tag{5.37}$$

The mechanical shaft output power is defined as

$$P_\mathrm{out,mech} = P_\mathrm{out,m} - P_\mathrm{fric} = \omega_\mathrm{R} \cdot (T_\mathrm{e} - T_\mathrm{fric}) . \tag{5.38}$$

The total VSD system efficiency including friction and windage losses is depicted in Fig. 5.7 for operation with rated rotor flux and optimal rotor flux. The curves are plotted over the electrical torque T_e as in the previous graphics. The shaft torque would be reduced by the friction torque T_fric. Especially at high rotor speeds, the friction and windage losses diminish the system efficiency considerably as a constant loss component exists that is not depending on the torque.

Therefore, in order to further increase the efficiency of VSD systems, more effort should be put into bearings with low losses and efficient

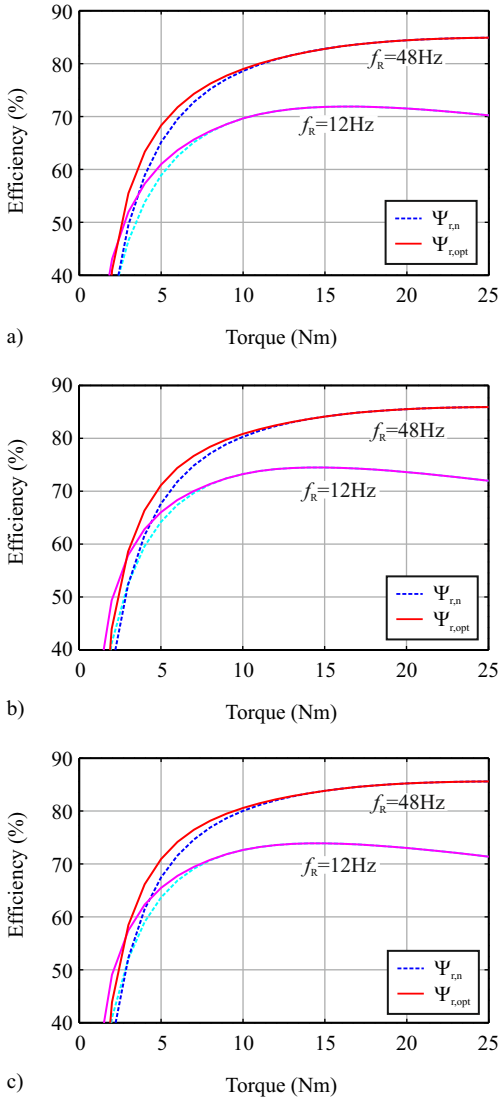

Figure 5.7: Total VSD system efficiency including friction and windage losses for a) 2LC, b) 3LT^{2}C, and c) 3LNPC^2.

cooling systems, possibly based on integrated water cooling solutions. The shaft mounted fan seems not to be an efficient cooling solution as the air flow path and the cooling fins are not optimized at all and are very inefficient.

5.4 Proposal of a highly efficient VSD system

In the previous sections, the loss components of the VSD system have been analyzed for three different converter topologies. The advantages and disadvantages of the converter topologies have been discussed, considering several factors, such as the converter loss characteristics, the induced harmonic losses in the induction machine and the necessary boost inductance and corresponding losses. Implementation details such as the number of isolated gate-drive voltages, the necessary semiconductor chip area, the dc-link voltage balancing, and the modulation complexity have been discussed. It was already highlighted in the comparison of the converter topologies (cf. Chapter 3) that the 3LT²C seems to be the most suitable candidate to build a highly efficient, modern low-voltage VSD system at justifiable additional costs and reasonable complexity.

As all loss models are readily available now, the achievable VSD system efficiency of a standard 2LC based solution using constant rated flux control can be compared to a modern solution based on the 3LT²C and using the optimal rotor flux control method. As before, the inverter stages of both topologies operate with $f_{\mathrm{sw,i}} = 8\,\mathrm{kHz}$ and the rectifier stage operates with $f_{\mathrm{sw,r}} = 8\,\mathrm{kHz}$ for the 2LC and with $f_{\mathrm{sw,r}} = 16\,\mathrm{kHz}$ for the 3LT²C. The achievable electrical efficiency without friction and windage losses is compared Fig. 5.8 and the total VSD system efficiency including friction and windage losses is shown in Fig. 5.9.

At rated torque and speed, an absolute efficiency increase of approx. 1% can be observed. In the low torque range ($T_{\mathrm{e}} \leq 20\% \cdot T_{\mathrm{n}}$) an absolute efficiency increase of more than 6% can be observed.

Finally, the characteristics of the two VSD systems, the standard 2LC solution and the 3LT²C solution with optimal rotor flux control, are summarized in Table 5.1.

The boost inductances and the switching frequencies of the rectifier stages were chosen to obtain minimum losses as described in the previous sections. The total volume of the boost inductors was determined

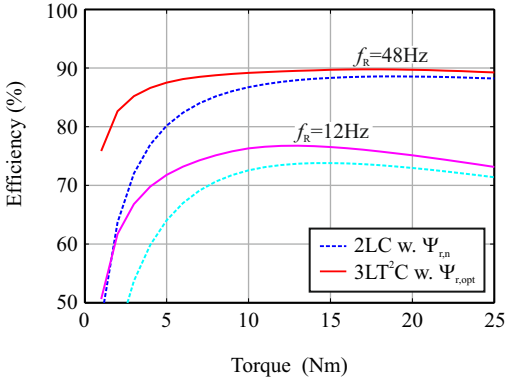

Figure 5.8: Comparison of the VSD system efficiency between a standard 2LC based system using constant flux control and the optimized 3LT^{2}C based system using optimal rotor flux control.

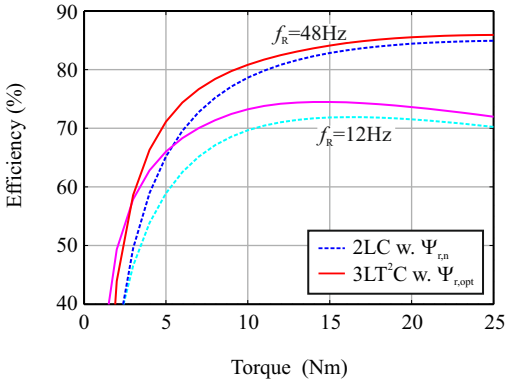

Figure 5.9: Comparison of the total VSD system efficiency including friction and windage losses between a standard 2LC based system using constant flux control and the optimized 3LT^{2}C based system using optimal rotor flux control.

from the volume of the 2.54 mH inductor design presented in [218] and using the volume scaling law (cf. Eq. 5.26).

The total volume of the capacitors has been calculated using extrapolated data of the EPCOS MKP foil dc-link capacitor series (B32774, B32776). For the 2LC, 800V dc-link foil capacitors have been cho-

sen with a linear volumetric density of $1.66\,\mathrm{cm}^3/\mu\mathrm{F}$ and for the 3LT²C, 450V dc-link foil capacitors with a linear volumetric density of $1\,\mathrm{cm}^3/\mu\mathrm{F}$ have been chosen. The 3-level topology requires two times $320\,\mu\mathrm{F}$ in series in order to obtain the same stored energy as the 2LC. The capacitance was chosen such that the worst case dc-link voltage unbalance of the 3LT²C stays below 50 V (cf. Section 3.7). The modulation has to be adapted accordingly to account for this unbalance. Alternatively, electrolytic capacitors could be chosen. As the maximum voltage rating of standard electrolytic capacitors is limited to 450 - 500 V, a series connection is necessary also for the 2LC and no advantage in volume and costs can be achieved if the same energy has to be stored.

The losses have been calculated for rated speed of the machine and two different torque settings. For nominal torque operation, the total losses can be reduced approximately by 8% and for low torque operation, the losses can be reduced by more than 25%. In both cases, the remaining losses are mostly due to friction and windage losses, as well as fundamental machine losses that can not be reduced any further without changing the machine design. Therefore, in order to further reduce the losses of this optimized VSD system, the cooling system of the machine has to be changed or the machine has to be replaced with a more efficient permanent magnet synchronous machine. Both measures would increase the total costs of the VSD system considerably.

Additional losses arise in the control platform, the fans for cooling of the heatsink and the remaining EMI filtering components. These loss components sum up to approx. $P_{\mathrm{ext}} \approx 50\,\mathrm{W}$.

Concluding, the advantages and the disadvantages of the 3LT²C compared to the 2LC are:

- The number of necessary IGBT's and diodes doubles, but half of them are 600 V devices that are cheaper than 1200 V devices.
- The number of gate-drive ICs, signal isolation ICs, gate signals and PWM units doubles.
- At minimum, only two additional isolated gate-drive voltage supplies are necessary for the complete back-to-back converter if the common collector switch configuration is chosen.
- The modulation complexity is slightly increased.
- The losses of the inverter stage and the rectifier stage are reduced because of lower switching losses. Contrary to the 3LNPC², there

Table 5.1: Comparison of the two VSD systems.

Parameter	Variable	2LC	3LT²C
Control method		$\Psi_{\mathrm{r,n}}$	$\Psi_{\mathrm{r,opt}}$
Inverter switching frequency	$f_{\mathrm{s,i}}$	8 kHz	8 kHz
Rectifier switching frequency	$f_{\mathrm{s,r}}$	8 kHz	16 kHz
Boost inductance	L_{b}	2.54 mH	850 μH
Dc-link capacitance	C_{dc}	160 μF	320 μF x2
Tot. inductor volume	V_{Lb}	1500 cm^3	663 cm^3
Tot. capacitor volume	V_{Cdc}	265 cm^3	640 cm^3
$T_{\mathrm{e}} = T_{\mathrm{n}}$			
Fund. machine losses	$P_{\mathrm{loss,m}}$	660 W	660 W
Harm. machine losses	$P_{\mathrm{h,m}}$	51 W	13 W
Inverter losses	$P_{\mathrm{loss,i}}$	94 W	78 W
Rectifier losses	$P_{\mathrm{loss,r}}$	87 W	87 W
Inductor losses	$P_{\mathrm{loss,Lb}}$	114 W	68 W
Total el. losses	$P_{\mathrm{el,tot}}$	1006 W	906 W
Friction losses	P_{fric}	285 W	285 W
Total losses	P_{tot}	1291 W	1191 W
$T_{\mathrm{e}} = 20\% \cdot T_{\mathrm{n}}$			
Fund. machine losses	$P_{\mathrm{loss,m}}$	206 W	120 W
Harm. machine losses	$P_{\mathrm{h,m}}$	53 W	11 W
Inverter losses	$P_{\mathrm{loss,i}}$	29 W	24 W
Rectifier losses	$P_{\mathrm{loss,r}}$	14 W	13 W
Inductor losses	$P_{\mathrm{loss,Lb}}$	70 W	47 W
Total el. losses	$P_{\mathrm{el,tot}}$	372 W	215 W
Friction losses	P_{fric}	285 W	285 W
Total losses	P_{tot}	657 W	500 W

is no remarkable increase of the conduction losses what makes the topology suitable also for low switching frequencies.

- The dc-link capacitor volume approx. doubles if foil capacitors are used. If electrolytic capacitors are used instead, no difference can be observed as due to the limited voltage capability, a series connection is necessary also for the 2LC.

- The necessary boost inductance can be reduced by more than

65% due to the increase of the rectifier switching frequency and the advantageous 3-level voltage waveform. The inductor volume and the losses can be reduced considerably.

- The harmonic losses in the machine due to the pulsed voltage waveform are reduced approx. by 75% what leads to less additional heating and lower insulation stress.
- The fundamental losses in the machine can be reduced in the low torque operating range if the optimal rotor flux control is implemented.
- Due to the increased switching frequency of the rectifier stage, active damping measures can be implemented what allows to replace passive damping branches of the EMI input filter with the virtual impedance damping concept.

Chapter 6

Hardware Prototypes

In this chapter, two hardware prototypes, namely a 3-level T-type inverter and a 3-level NPC back-to-back converter, are presented that have been developed in order to verify the theoretical considerations of this thesis. The motivation to build the prototypes is briefly discussed and the key performance figures are presented.

6.1 3LT²C prototype

The 3-level T-type inverter prototype (cf. Fig. 6.1) was implemented with discrete Infineon switches (IKW40T120 1200 V, 40 A IGBTs / diodes and IKW50N60T 600 V, 50 A IGBTs / diodes) also used for the calculations presented in the previous chapters. The schematic of the power circuit is depicted in Fig. 6.2.

Two main reasons have led to the development of this prototype. First, it allowed to measure the switching losses of the special switch configuration used in the 3LT²C directly in the hardware prototype. Therefore, the influence of the hardware layout on the commutation inductances and on the switching losses is contained in the measurements.

Second, the prototype can generate 2-level and 3-level output voltage waveforms. It has also the ability to change the switching frequency during operation. These features were used to measure the harmonic losses in the machine and to determine the impact of the voltage waveform and the switching frequency. Changing the modulation and the

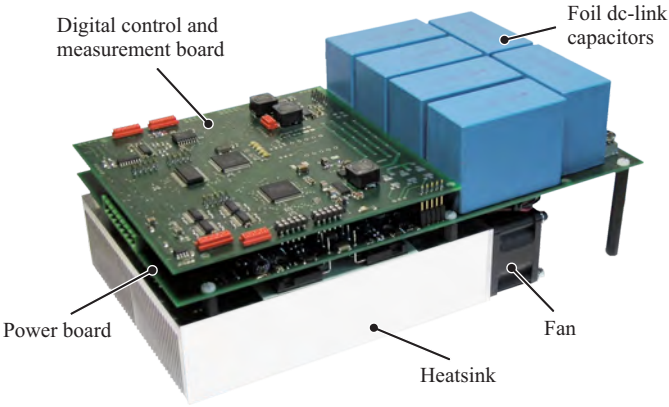

Figure 6.1: Prototype of the 3LT^{2}C.

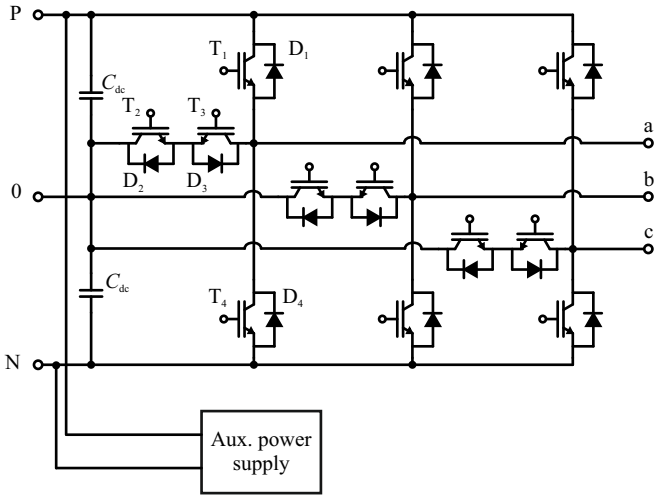

Figure 6.2: Schematic of the 3LT^{2}C power circuit.

switching frequency during operation is important, as the harmonic machine losses can be measured without stopping the machine. The thermal conditions can be maintained and therefore, the measurement results are more significant.

The key performance data of the 3LT^{2}C prototype is summarized in

Table 6.1: Design details of the main components.

Component	Comments
DC-link capacitors	2 x 240 μF in series, each built with 3 parallel EPCOS MKP B32778 80uF, 450V foil capacitors
Heatsink	$R_{\mathrm{th}} = 0.12\,\mathrm{K/W}$, 130x130x40mm 40 fins, 1mm fin thick., 2mm distance
Fans	Sanyo SanAce 9GA0412P3J01 12V, 6W, 18000 rpm

Table 6.2: Parameters of the 3LT²C prototype.

Parameter	Variable	Value
Nominal output power	P_{n}	10 kW
Nominal efficiency	η_{n}	99.0 %
Switching frequency	f_{sw}	8 kHz
DC-link voltage	V_{dc}	650 V
DC-link capacitance	C_{dc}	$2 \times 240\,\mu$F in series
Volume	V	$3\,\mathrm{dm}^3$
Weight	m	2 kg
Power density	ρ	$3.3\,\mathrm{kW/dm}^3$
Power weight	σ	5 kW/kg

Table 6.2. The converter is designed for an output power of 10 kW and allows the switching frequency to be set in a range from $4 - 24$ kHz. At the nominal switching frequency of 8 kHz, the converter reaches a pure semiconductor efficiency of 99 %. Digital control, gate drive circuits and forced air cooling consume 20 W in addition. The power density is given with $3.3\,\mathrm{kW/dm}^3$. Design details for the main components are given in Table 6.1.

The converter is controlled with a digital signal processing board employing a 100 MHz DSP from TI (TMS320F2808) and a FPGA from Lattice (LCMXO2280) as well as filtering and amplification circuitry. The control board is mounted on top of the power board which holds the gate drive circuits and the power semiconductors.

The efficiency of the 3LT²C has been measured with a Yokogawa WT3000 precision power analyzer (basic power measurement accuracy

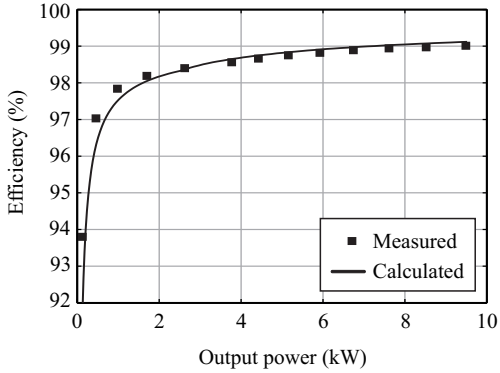

Figure 6.3: Calculated and measured efficiency of the 3LT^{2}C prototype supplying a RL-load ($R = 20\,\Omega, L = 2.5\,\text{mH}$) with the losses of power terminals and power cables considered.

of 0.02%). The measurements were conducted with a fixed RL-load ($R = 20\,\Omega, L = 2.5\,\text{mH}$) and the output voltage was increased in small steps. The clamping interval was set to symmetric clamping around 0° in order to match the only small current phase displacement angle φ_1 resulting from the mainly resistive RL-load.

Fig. 6.3 shows the measured and the calculated efficiency over the output power. The initial efficiency calculation resulted in a slightly higher efficiency than measured. Further measurements revealed additional loss components caused by cabling resistances and contact resistances of the implemented screw clamps at the power terminals of the converter. Although these loss components are very small ($P_{\text{cable}} = 12.8\,\text{W}$ and $P_{\text{screw}} = 13.8\,\text{W}$ at the nominal output power), their influence is not negligible if high efficiencies are measured. If the additional losses are included, calculations and measurements show a very good agreement.

6.2 3LNPC² prototype

The 3LNPC SiC back-to-back converter prototype (cf. Fig. 6.5) was developed with the main focus on building a complete bidirectional converter system with an increased switching frequency for applications that require a high control bandwidth, such as high speed drilling

drives, or that need to generate increased fundamental frequencies of up to 1 kHz. Such fundamental frequencies are required in high speed drive systems or in modern aircraft applications where the fundamental frequency of the internal power grid can vary up to 800 Hz. As a side condition, the efficiency should be kept high compared to a 2LC solution. Therefore, the implementation of 600 V SiC Schottky diodes to improve the efficiency of the 3-level NPC topology was tested.

The schematic of the 3-level NPC back-to-back converter power circuit is depicted in Fig. 6.4. The prototype was built using custom 3-level NPC bridge-leg modules from Microsemi (APTGT50TL60T3G with 600 V, 50 A IGBTs / diodes). As was already explained in Section 3.3.2, it is sufficient to replace only 4 of the 6 diodes of a bridge-leg with SiC Schottky diodes to gain the full benefit (cf. the diodes that are shaded with gray color in Fig. 6.6a). Each diode is replaced with three parallel connected 600 V, 10 A SiC diode dies from Cree (cf. Fig. 6.6b) in order to ensure comparable conduction losses as with the normal Si diodes.

The key performance data of the 3LNPC² prototype is summarized in Table 6.3. It was designed for an output power of 10 kW and a switching frequency of $f_{\mathrm{sw}} = 48\,\mathrm{kHz}$. At this switching frequency, it was calculated that the SiC Schottky diodes reduce the total losses by 50 W what leads to an absolute efficiency increase of 0.5%.

A gate-drive board populated with 26 isolated gate drive circuits and 5 current sensors for the input and output currents is directly mounted on the 3-level modules. A digital signal processing board with a 100 MHz DSP from Texas Instruments (TMS320F2808) and a FPGA from Lattice (LCMXO2280) as well as filtering and amplification circuitry is mounted on top of the gate-drive board.

An EMI input filter was designed to fulfill the CISPR Class A conducted emission limits following the simulation based filter design approach described in [144]. The schematic of the EMI filter is depicted in Fig. 6.7 and the filter component values are summarized in Table 6.4.

Special attention was paid to reach a high power density of the converter including the heatsink with forced air cooling. Three iron powder core boost inductors with an inductance of only $L_{\mathrm{b}} = 300\,\mu\mathrm{H}$ have been employed. They limit the unfiltered current ripple at the rectifier stage to $\Delta i_{\mathrm{pp}} = 4\,\mathrm{A}$. A minimum total dc-link capacitance of $33\,\mu\mathrm{F}$ has been calculated, limiting the voltage overshoot in case of a sudden load drop from nominal power to zero to an acceptable value

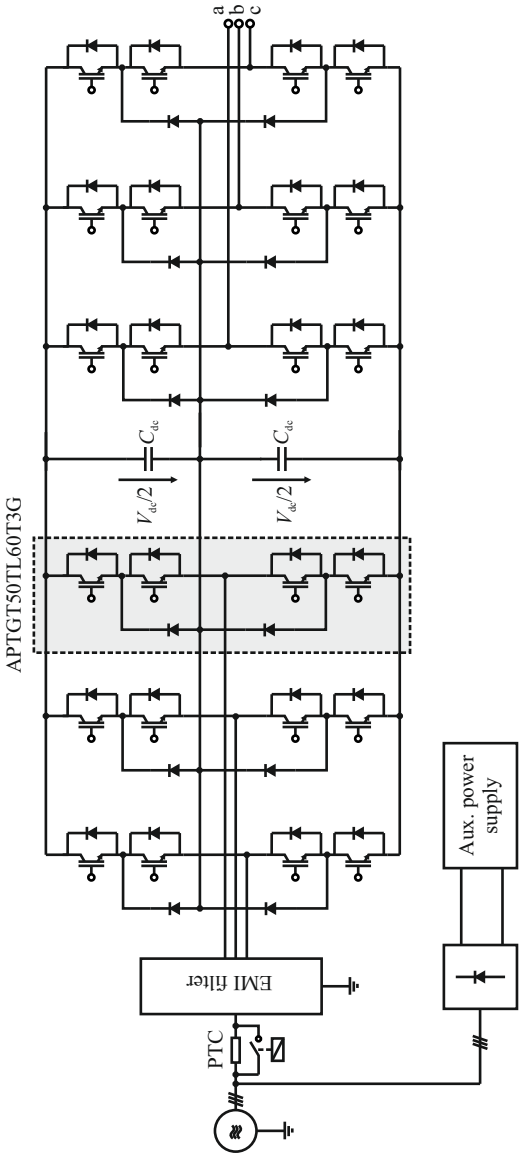

Figure 6.4: Schematic of the 3-level NPC back-to-back converter.

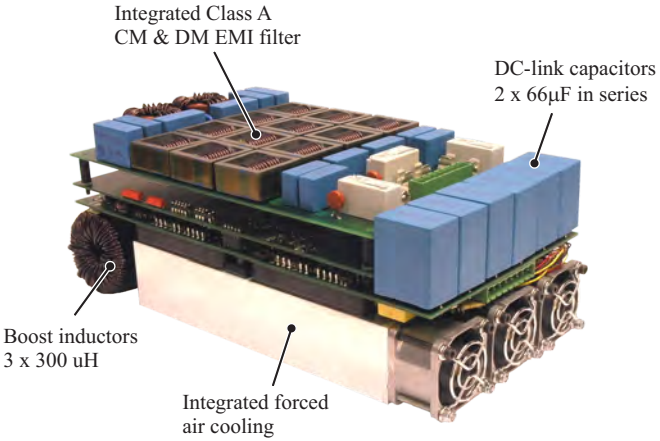

Figure 6.5: Compact 10 kW, 3LNPC back-to-back converter prototype with a switching frequency of $f_{sw} = 48$ kHz.

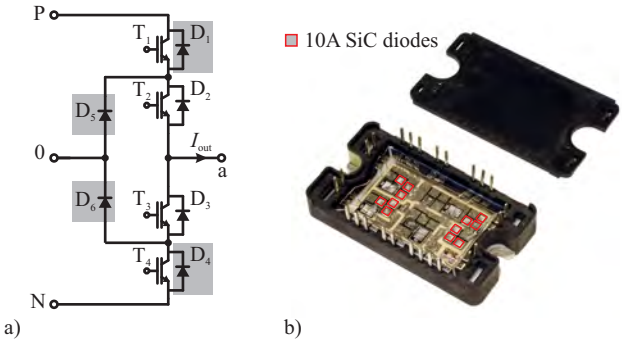

Figure 6.6: a) The diodes of the NPC bridge-leg which are replaced with SiC Schottky diodes are shaded with gray color. b) Custom NPC bridge-leg module with the SiC Schottky diode chips highlighted in red.

of $\Delta v = 10\% \cdot V_{dc}$. Two times 66 μF in series have been implemented with reliable foil capacitors. As already mentioned in Section 3.7, the modulation has to be adapted to consider the voltage unbalance that is inevitable with this low dc-link capacitance. Design details for the main components can be found in Table 6.5.

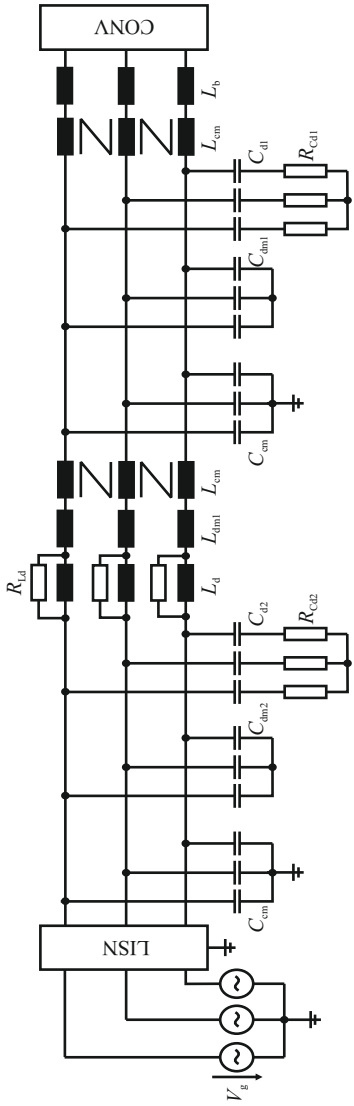

Figure 6.7: Schematic of the EMI input filter.

Table 6.3: Parameters of the 3LNPC² prototype.

Parameter	Variable	Value
Nominal output power	P_n	10 kW
Nominal voltage	V_n	230 V
Fundamental frequency	f_n	50 Hz / 800 Hz
Switching frequency	f_sw	48 kHz
DC-link voltage	V_dc	650 V
DC-link capacitance	C_dc	2 x 66 μF in series
Boost inductance	L_b	3 x 300 μH
Power density	ρ	2.9 kW/dm^3
Power weight	σ	2 kW/kg
Nominal efficiency	η_n	95.5%
Weight	m	5 kg

Table 6.4: EMI filter component values.

Component	Value
C_dm1	3 μF
C_d1	1.5 μF
R_Cd1	12 Ω
L_dm1	13 μH
L_d	39 μH
R_Ld	1.36 Ω
C_dm2	0.68 μF
C_d2	0.68 μF
R_Cd2	6 Ω
C_cm	4.7 nF
L_cm	1.6 mH

A forced air cooling system and an optimized heatsink have been dimensioned for a maximum junction temperature of $T_j = 125\,^\circ$C. The power density of the total converter including cooling system and EMI filter is 2.9 kW/dm^3.

The measured converter efficiency reaches 95.5% (cf. Fig. 6.8) including the losses in the EMI input filter (in total 10 W), the losses in the boost inductors (in total 50 W) as well as the losses in the connectors and due to the cabling setup (in total 25 W).

Table 6.5: Design details of main components.

Component	Comments
DC-link capacitors	2 x 66 μF in series, each built with 3 parallel EPCOS MKP B32744 22uF, 450V foil capacitors
Boost inductors	3 x 300 μH, each built with 2 stacked Micrometals T184-14 iron powder cores, 68 turns with 1.8mm diam. copper wire
Heatsink	$R_{\text{th}} = 0.08\,\text{K/W}$, 180x130x40mm 40 fins, 1mm fin thick., 2mm distance
Fans	Sanyo SanAce 9GA0412P3J01 12V, 6W, 18000 rpm

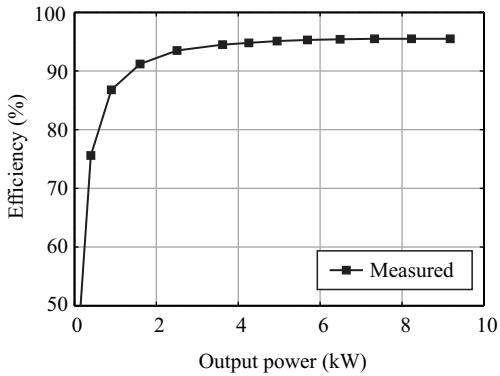

Figure 6.8: Measured efficiency of the 3LNPC^2 prototype supplying a RL-load ($R = 20\,\Omega, L = 2.5\,\text{mH}$).

Chapter 7

Summary & Outlook

7.1 Summary and Conclusions

In this thesis, the achievable improvement of the total system efficiency of a low-voltage VSD system using modern converter topologies and enhanced control concepts has been investigated.

A detailed comparison of the implementation effort and the loss characteristics of the 2LC, the 3LT²C, and the 3LNPC² was given. It showed that both 3-level topologies have considerably lower switching losses and are therefore suitable for applications that require increased switching frequencies, such as high speed drives. The drawbacks of the 3LNPC² are not only the increased complexity and/or the higher implementation effort, but also the increased conduction losses. As always two devices are connected in series, the forward voltage drops of the bipolar devices sum up and lead to higher losses. Contrary to unipolar devices (such as MOSFETs), increasing the semiconductor area of the IGBTs and diodes can not reduce the conduction losses consequently as always a minimum forward voltage drop will remain. This property prohibits its application in the majority of industry applications, where no special requirements concerning control performance or high fundamental frequencies are required and therefore often 2LCs with a low switching frequency ($f_{\mathrm{sw}} \leq 16\,\mathrm{kHz}$) are employed. In this switching frequency range, the increased conduction losses and the increased complexity are good arguments against the application of the 3LNPC².

For these applications, the alternative 3LT²C has its strengths. This

topology extends the standard 2LC to a 3-level topology with a bidirectional switch to the dc-link mid-point. For low-voltage applications, it can be built combining 1200 V IGBTs / diodes and 600 V IGBTs / diodes what allows to use single semiconductor devices to connect the output to the positive and the negative dc-link voltage. Consequently, there is a reduction of the conduction losses compared to the 3LNPC² where always two devices are in series. The conduction losses can be kept on about the same level as for the 2LC, although there is a very small increase. As the topology is a true 3-level topology, the switching losses are reduced considerably and therefore, the 3LT²C has a higher efficiency than the 2LC even at low switching frequencies. Measurements at a prototype of the 3LT²C showed an efficiency of 99% at a switching frequency of $f_{sw} = 8\,\text{kHz}$ without employing costly advanced semiconductor materials such as SiC.

As the cost pressure for low-voltage VSD applications is very high, there must be additional advantages of the 3LT²C to be a real alternative to the 2LC. These have been found in the implementation effort and in positive impacts on the surrounding subsystems. First, it was shown that the 3LT²C needs less semiconductor devices than the 3LNPC² and that it can be built with only one additional isolated gate drive supply compared to the 2LC. This is a significant improvement. Furthermore, the 3LT²C is very simple in operation and needs no transient voltage balancing circuits.

A detailed analysis of the loss distribution characteristics of the three topologies showed that the losses of the 3-level topologies are small and always spread over several semiconductor devices. Therefore, the junction temperature increase is less pronounced compared to the 2LC. Consequently, smaller semiconductor chips can be used. With a comparison of the necessary semiconductor chip area it was shown that for increased switching frequencies ($f_{sw} \geq 16\,\text{kHz}$), the 3-level topologies need in total less semiconductor chip area than the 2LC. This can be directly translated into a cost reduction as devices with a lower current rating can be employed which are usually cheaper.

The loss comparison was extended to the impact on the surrounding subsystems. First, the losses in the induction machine, most often used in industry applications due to its low costs, have been analyzed in detail. These losses can be divided into fundamental frequency losses and harmonic losses due to the PWM voltage waveform.

Approximate models describing the harmonic machine losses have

been considered and compared to experimental measurements. The most important findings are the frequency dependency of the harmonic losses and the differences between 2-level and 3-level modulated voltage waveforms. Although the harmonic machine losses decrease if the switching frequency is increased, they stagnate on a certain level because of dominant eddy-current based iron losses that are mostly independent of the switching frequency. It is therefore not necessary to increase the switching frequency above a certain value ($f_{\mathrm{sw}} \geq 16\,\mathrm{kHz}$) as the harmonic losses cannot be decreased significantly any more. Considering also the switching losses of the inverter stages, it was shown that minimum total losses are obtained at $f_{\mathrm{sw}} \approx 8\,\mathrm{kHz}$ for all three compared inverter topologies in this specific case. Additionally, the measurements and the analytical approximations showed that the harmonic machine losses can be reduced by 75% with the 3-level topologies compared to the 2LC. Especially for older machines with thicker iron laminations, this reduction is significant as the harmonic machine losses obtained with the 2LC are significant and lead to additional heating of the machine what reduces its lifetime. Sometimes, even a reduction of the rated machine output power is necessary [219] if it was fed with an inverter supply compared to a sinusoidal supply.

Also the fundamental machine losses have been analyzed in detail. The impact of energy saving machine control algorithms was investigated. The idea behind these control algorithms is to reduce the rotor flux linkage of the induction machine during low torque operation. Usually, the induction machine is controlled with a constant rotor flux linkage what leads to unnecessarily high iron losses and ohmic losses due to the magnetizing current. These can be reduced using the optimal rotor flux linkage that leads to maximum machine efficiency. There are basically two different concepts to implement the energy saving machine controllers. Either a search controller can be used that periodically alters a control variable, such as the rotor flux linkage, and actively finds the point of minimum losses. This controller can also be used to minimize the total system losses, including the converter losses, if the input power of the converter is minimized instead of the input power of the machine. The main drawbacks of the search controllers are their slow convergence and continuous oscillations around the point of minimum losses.

Another way to implement an energy saving controller is with a model based approach. The optimal rotor flux linkage is directly calcu-

lated based on the machine parameters and the actual operating point. The method is very fast but its accuracy depends on the estimated machine parameters. A sensitivity analysis showed that the model based approach is not very sensitive to the exact knowledge of the machine parameters. The only parameter that has to be estimated accurately ($\pm 10\%$) is the mutual inductance, the other parameters (the stator and rotor resistances, and the equivalent core loss resistance) don't lead to a noteworthy detuning if estimated with an accuracy of $\pm 40\%$. Because three of the four parameters that are necessary for the model based efficiency maximizer are used in field oriented control and many estimation algorithms exist for their determination, only the detection of the equivalent core loss resistance was considered in more detail. A method based on a deceleration test that can be performed directly with the inverter was proposed.

The efficiency of the induction machine can be increased by several percent during low torque operation. Under the operation with the optimal rotor flux linkage, the terminal behavior of the induction machine changes, as the supplied stator voltage, the stator current, and the current to voltage phase displacement angle are reduced. The changed operating point has an impact on the losses and the efficiency of the inverter stage. It was shown in Chapter 5 that it is not necessary to include the inverter losses in the derivation of the optimal rotor flux linkage. Neglecting them leads only to a negligibly small reduction of the reachable system efficiency but simplifies the expression for the optimal rotor flux linkage considerably.

Further losses occur in the rectifier stage and in the EMI input filter. An analysis of the necessary boost inductance for the different rectifier topologies showed the potential for volume and loss reduction with the 3-level topologies. There is an optimal switching frequency of the rectifier stage that leads to minimal total losses in the boost inductors and the rectifier stage. As the boost inductance can be reduced with the 3-level topologies, the optimal switching frequency shifts towards higher values, such as 16 kHz for the 3LT^{2}C and 24 kHz for the 3LNPC^2 compared to 8 kHz for the 2LC. This is not only because of the lower switching losses in the 3-level topologies, but also because of the reduced inductance and related lower volume and losses of the components.

Additionally, active damping concepts have been investigated. Usually, passive damping branches are necessary to damp the resonances

of the EMI input filter in order to guarantee stable operation of the active rectifier. These passive damping branches increase the volume and the costs of the EMI filter. The control structure of the active rectifier can be modified such that it emulates the behaviour of an additional virtual circuit element at its input terminals. With a virtual resistor, the resonance peak of the input filter can be dampened effectively. With a virtual reactive element, the resonance frequency can be shifted actively. The resonance frequency shifting method was proposed to mitigate stability problems triggered by several converters connected to the same grid at a point of common coupling.

The impact of the active damping methods was analyzed with the stability theory based on impedance matrices in the synchronous reference frame. A detailed literature review was given that covers the different approaches for stability assessment of single-phase and three-phase AC systems. A measurement system was built that allows to determine the small signal impedance matrices of converters experimentally. It was used to prove the models of the active rectifier that have been derived analytically.

Finally, the results of the analysis of the different subsystems have been interlinked. A complete VSD system is optimized concerning the total system efficiency and compared to the standard solution based on the 2-level converter. Under full load operation, the total system efficiency can be increased absolutely by 1% with the optimized system based on the 3LT²C and under part load operation ($T_\mathrm{e} \leq 20\% \cdot T_\mathrm{n}$), the total system efficiency can be increased by more than 6%. Although this seems not to be very much, these results can be interpreted differently if it is highlighted that the remaining losses are mostly due to mechanical friction and windage losses as well as fundamental machine losses that can be reduced further only with a different machine design, such as a permanent magnet synchronous machine. Furthermore, improved bearings and an improved cooling system could reduce the losses of the induction machine.

The holistic, system oriented optimization allowed to identify the various interactions of the different subsystems. Changing the converter topology has impacts on the surrounding subsystems that are usually not considered in the cost and efficiency calculations and the decisions in favour of a certain topology. If all these aspects are considered, the low-voltage VSD system based on the 3LT²C is a real alternative to the low-cost 2LC based system.

7.2 Outlook

In this Thesis, the holistic, system oriented efficiency analysis of a low-voltage VSD system was presented. Due to the variety of topics covered, there are several aspects that could be addressed more deeply in the course of further research. Some open tasks are listed in the following.

- The analysis of modular multilevel converter concepts for low-voltage applications. The extremely low conduction and switching losses, as well as the low costs of low-voltage MOSFETs should be considered in the design of battery-cell based inverters, such as automotive applications based on lithium-ion batteries.
- A holistic VSD system volume optimization is missing, considering also the heatsink volume and the volume of the load machine, especially in combination with high-speed machines.
- The costs of the VSD system have been mentioned only superficially. A detailed cost analysis of the involved subsystems could further clarify the competitiveness of 3-level or multilevel converter topologies for low-voltage applications. However, this is more a task for industrial than for academic research as the exact purchase costs depend heavily on the manufacturer and on scaling effects, i.e. the number of purchased components.
- The advantages and drawbacks of active damping concepts should be analyzed in a more systematic way. The application scenarios should be defined and tested experimentally. The switching frequency range where active damping concepts make sense should be determined considering also the EMI attenuation requirements.

Appendix A

Rectifier input impedance with PLL

The equation system derived from Fig. 4.7 can be extended with the linearized PLL equations. The variables θ (angle of internal reference frame) and v_{bq} denote deviations from the steady-state operating point and are small-signal values,

$$\theta = G_{\mathrm{pll}} v_{\mathrm{bq}} \tag{A.1}$$

$$G_{\mathrm{pll}} = \frac{R_{\mathrm{pll}} \frac{1}{s}}{1 + V_{\mathrm{bd},0} R_{\mathrm{pll}} \frac{1}{s}} \tag{A.2}$$

$$R_{\mathrm{pll}} = k_{\mathrm{p,pll}} \frac{1 + sT_{\mathrm{n,pll}}}{sT_{\mathrm{n,pll}}}. \tag{A.3}$$

R_{pll} designates the PI regulator transfer function of the PLL where $k_{\mathrm{p,pll}}$ and $T_{\mathrm{n,pll}}$ are the corresponding proportional and integral gains. G_{pll} is the closed loop transfer function from input voltage variations v_{bq} to changes in the internal reference frame angle θ and $V_{\mathrm{bd},0}$ is the steady state grid voltage amplitude. The transformation of the measurement variables into the internal reference frame can be described with

$$\begin{aligned} X_{\mathrm{d,int}} &= \cos(\Theta) X_{\mathrm{d}} + \sin(\Theta) X_{\mathrm{q}} \\ X_{\mathrm{q,int}} &= -\sin(\Theta) X_{\mathrm{d}} + \cos(\Theta) X_{\mathrm{q}}. \end{aligned} \tag{A.4}$$

Variables in the internal reference frame are denoted as x_{int}. The transformation equations can be linearized around the steady-state values as

$$\begin{aligned} x_{\mathrm{d,int}} &= x_{\mathrm{d}} + X_{\mathrm{q},0}\theta \\ x_{\mathrm{q,int}} &= x_{\mathrm{q}} - X_{\mathrm{d},0}\theta. \end{aligned} \tag{A.5}$$

The same procedure can be used to find the inverse transformation of the internal variables into the external variables. The inverse transformation is given with

$$\begin{aligned} X_{\mathrm{d}} &= \cos(\Theta)\, X_{\mathrm{d,int}} - \sin(\Theta)\, X_{\mathrm{q,int}} \\ X_{\mathrm{q}} &= \sin(\Theta)\, X_{\mathrm{d,int}} + \cos(\Theta)\, X_{\mathrm{q,int}}. \end{aligned} \tag{A.6}$$

These equations can again be linearized around the steady-state values as

$$\begin{aligned} x_{\mathrm{d}} &= x_{\mathrm{d,int}} - X_{\mathrm{q},0}\theta \\ x_{\mathrm{q}} &= x_{\mathrm{q,int}} + X_{\mathrm{d},0}\theta. \end{aligned} \tag{A.7}$$

The additional equations for the PLL extend the equation system. The conventional control structure contains a feedforward path of the grid voltage and a decoupling path for the cross-coupling currents,

$$i_{\mathrm{d}} = \frac{1}{sL_{\mathrm{b}}}\left(v_{\mathrm{bd}} + \omega_{\mathrm{e}} L_{\mathrm{b}} i_{\mathrm{q}} - v_{\mathrm{ud}}\right) \tag{A.8}$$

$$i_{\mathrm{q}} = \frac{1}{sL_{\mathrm{b}}}\left(v_{\mathrm{bq}} - \omega_{\mathrm{e}} L_{\mathrm{b}} i_{\mathrm{d}} - v_{\mathrm{uq}}\right) \tag{A.9}$$

$$v_{\mathrm{ud,int}} = v_{\mathrm{bd,int}} + \omega_{\mathrm{e}} L_{\mathrm{b}} i_{\mathrm{q,int}} - \left(i_{\mathrm{d}}^{*} - i_{\mathrm{d,int}}\right) R_{\mathrm{i}} \tag{A.10}$$

$$v_{\mathrm{uq,int}} = v_{\mathrm{bq,int}} - \omega_{\mathrm{e}} L_{\mathrm{b}} i_{\mathrm{d,int}} - \left(-i_{\mathrm{q,int}}\right) R_{\mathrm{i}} \tag{A.11}$$

$$i_{\mathrm{d}}^{*} = -v_{\mathrm{dc}} R_{\mathrm{u}} \tag{A.12}$$

$$v_{\mathrm{dc}} = G_{\mathrm{p}}\left(I_{\mathrm{d},0} v_{\mathrm{ud}} + V_{\mathrm{ud},0} i_{\mathrm{d}} + I_{\mathrm{q},0} v_{\mathrm{uq}} + V_{\mathrm{uq},0} i_{\mathrm{q}}\right) \tag{A.13}$$

$$G_{\mathrm{p}} = \frac{3}{2}\frac{1}{V_{\mathrm{dc},0} sC_{\mathrm{dc}} + I_0} \tag{A.14}$$

$$v_{\mathrm{ud}} = G_{\mathrm{t}}\left(v_{\mathrm{ud,int}} - V_{\mathrm{uq},0}\theta\right) \tag{A.15}$$

$$v_{\mathrm{uq}} = G_{\mathrm{t}}\left(v_{\mathrm{uq,int}} + V_{\mathrm{ud},0}\theta\right) \tag{A.16}$$

$$i_{\mathrm{d,int}} = i_{\mathrm{d}} + I_{\mathrm{q},0}\theta \tag{A.17}$$

$$i_{\mathrm{q,int}} = i_{\mathrm{q}} - I_{\mathrm{d},0}\theta \tag{A.18}$$

$$v_{\mathrm{bd,int}} = v_{\mathrm{bd}} + V_{\mathrm{bq},0}\theta \tag{A.19}$$

$$v_{\mathrm{bq,int}} = v_{\mathrm{bq}} - V_{\mathrm{bd},0}\theta \tag{A.20}$$

$$\theta = G_{\mathrm{pll}} v_{\mathrm{b,q}}. \tag{A.21}$$

G_t is an approximation for the time delay, R_i is the current controller and R_u the voltage controller transfer function. In order to find the input admittance matrix elements, the equation system has to be solved for the corresponding variables. Y_dd and Y_qd can be found by setting v_bq to zero and solving for i_d and i_q. Similarly Y_qq and Y_dq are found if v_bd is set to zero and the equations are solved for i_q and i_d.

The detailed equations of the input admittance matrix elements are not given here as they are to long, but they can be handled with mathematics software such as MATLAB or Mathematica.

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