DISS. ETH NO. 20944

HIGH TEMPERATURE / POWER DENSITY / OUTPUT FREQUENCY SIC DC-AC CONVERTER SYSTEM FOR HYBRID ELECTRIC VEHICLES

A dissertation submitted to
ETH ZURICH

for the degree of
Doctor of Sciences

presented by
Benjamin Tobias Wrzecionko
Dipl.-Ing., RWTH Aachen University
born 16 June 1983
citizen of Germany

accepted on the recommendation of
Prof. Dr. Johann W. Kolar, examiner
Prof. Dr. Hans-Peter Nee, co-examiner

2013

Acknowledgments

First of all, I would like to thank Prof. Dr. Johann W. Kolar for offering me the opportunity to perform my Ph. D. research in his Power Electronic Systems Laboratory at ETH Zurich as well as for the excellent guidance and collaboration throughout the work. He has established a leading power electronics institute with an outstanding and highly challenging research atmosphere which is an ideal chance for the first full-time job.

Prof. Dr. Hans-Peter Nee from KTH Stockholm has showed great interest for my Ph. D. research since a visit at ETH Zurich and invited me to present my work in a very interesting workshop in Sweden. I feel honored and I am much obliged for having won him as a co-examiner of this Ph. D. dissertation.

Special thanks go to our Japanese industry partner for funding the work and the exemplary cooperation, involving numerous videoconferences, reports, and two visits despite the large geographical distance.

The entire staff of the institute has a significant share in the success of this Ph. D. dissertation:

I would like to express my sincere thanks for their valuable input as post-doctoral researchers to Dr. Jürgen Biela and Dr. Dominik Bortis, and for productive discussions and great mutual help at any time to my fellow Ph. D. students Daniel Christen, Thomas Friedli, Philipp Karutz, Ivana Kovačević, Florian Krismer, Andreas Looser, Christoph Marxgut, Jonas Mühlethaler, Gabriel Ortiz, Mario Schweizer, and Bernhard Warberger who I both enjoyed to work with and had an unforgettable time with outside the office.

Likewise, Peter Seitz contributed with the assembly of industry-oriented demonstrator systems in the electronics laboratory, Peter Albrecht as purchasing and materials manager, Roswitha Coccia and

Dr. Beat Seiler as industry relations managers, Monica Kohn-Müller as secretary, and Markus Berger and Claudia Stucki as IT administrators providing a high-level infrastructure.

Big thanks are due to my master students, Stefan Käch and Lukas Steinmann, who conducted their work with a very high level of motivation and complemented my research with their ambitious and eminent master's theses.

Finally, I am deeply indebted to my family, my close friends and my girlfriend Linda Koller for their invaluable support anytime throughout my work on this Ph. D. dissertation.

Benjamin Wrzecionko
Zurich, September 2013

Contents

Abstract

In this Ph. D. dissertation, a compact power electronic SiC inverter system with high output frequencies and direct air-cooling for use in hybrid vehicles at an ambient temperature of 120 °C is investigated in detail.

The research and development of hybrid and electric vehicles has intensified significantly in recent years and still continues to grow. The focus is on power electronic converters as links between the electrical energy storage on the one hand and the electrical machine or conventional 12 V loads on the other hand. The use of power electronics in vehicles is subject to specific requirements concerning power density, power to weight ratio, efficiency and cost. Furthermore, a high resistance to harsh environmental conditions, e.g. extreme ambient temperatures and vibrations, is required. In addition, a trend towards the use of compact electrical machines with high rotational speeds, which require significantly higher output and switching frequencies of the supplying power electronics converters, can be identified. Novel semiconductor devices based on silicon carbide (SiC), allow high switching speeds as well as the operation at high junction temperatures and can thus potentially contribute to the fulfillment of these requirements. However, so far highly compact converters with SiC switches and diodes for high ambient temperatures have attracted relatively little attention in the literature.

First, current SiC power switches are thoroughly evaluated regarding their potential use in the described inverter system in terms of area-specific conduction properties in forward and reverse direction, switching behavior, thermal behavior, ability for parallelization, reliability, and safety in case of a fault. Because of the one order of magnitude higher breakdown electrical field of SiC compared to silicon (Si), unipo-

lar devices — offering fast switching and with possible parallelization (reduction of the conduction losses) an additional degree of freedom — can be used advantageously in the considered blocking voltage class of 1.2 kV and at elevated junction temperatures. Particular reliability considerations lead to benefits for junction field effect transistors (JFETs) against the background of the current state of the SiC semiconductor technology. For voltage source converters, normally-off devices are favorable. Due to high junction temperatures above the technological limit of Si, a full-SiC solution and therefore the novel normally-off JFET is preferred for the investigated system.

A detailed analysis of the loss behavior over the temperature with respect to given converter parameters such as dc-link voltage, switching frequency, and thermal resistance from the power semiconductor junction to the ambience shows that a junction temperature of 250 °C allows a utilization of the JFET by more than 90 % at an ambient temperature level of 120 °C.

Subsequently, new gate drive circuit topologies for the control of the employed normally-off JFETs are researched taking into account parasitic effects and the individual requirements of the novel SiC switch that excel the requirements of today's Si devices in their complexity in terms of sequencing and value of the necessary voltage levels (e.g., 3 V during on-state, a high noise immunity during the off-state due to a threshold voltage of only 0.7 V, which, due to the inherently high gate-drain capacitance, is a severe challenge, and ±15 V during switching). As a result, a novel ac-coupled gate driver is presented and experimentally verified, that allows a safe operation of the normally off JFETs with minimum switching and conduction losses without the limitations mentioned in the literature, such as frequency restrictions or self-heating.

With respect to the dc-ac converter itself, a mechanical concept of the inverter with 50 kHz switching frequency is investigated, which includes new ways to solve electrical and thermal trade-offs. In particular, the operation of the signal electronics and the gate driver for power semiconductors with a junction temperature of 250 °C within the specified operating temperature range is ensured by appropriate placement and cooling methods while taking the electrical requirements for limits on the wiring inductances and symmetry requirements regarding the component placing into account. The analysis includes an accurate thermal model of the converter and an optimized active cooling of the signal electronics using a Peltier cooler.

For the direct air-cooling of the employed power semiconductors, a high temperature fan with a comparable fluid dynamic performance at 120 °C as commercial high performance fans at 20 °C is investigated which can be operated advantageously for high temperature applications as described in this dissertation up to a temperature of 250 °C at a rotational speed of $19'000\,\mathrm{min}^{-1}$. The research includes the mechanical fan assembly, the magnetic and mechanical design of the electrical machine taking thermal expansion and maximum allowable operating temperature of the materials into account, the geometry of the blades as well as the choice of the materials for the shaft, bearings, bearing housings, laminations, magnets, and windings.

For the control of the presented converter system with SiC semiconductors that reach a junction temperature of up to 250 °C under full load, a new concept for electrically isolated current measurement at ambient temperatures of 250 °C is found and realized after an in-depth analysis of known concepts concerning high accuracy, large bandwidth for measurements of alternating currents with frequencies up to 1 kHz and direct currents as well as noise immunity at steep voltage transients of $30\,\mathrm{V/ns}$.

Finally, the investigated novel concepts for a safe control with minimum losses of the employed JFETs, for the design of the inverter, the direct air-cooling using the new high temperature fan and the galvanically isolated high temperature current measurement are validated in an experimental system analysis of a demonstrator system at temperature levels up to 250 °C. The presented work is completed by putting the technical achievements in a broader automotive context.

Kurzfassung

In der vorliegenden Doktorarbeit wird das Gesamtsystem eines kompakten leistungselektronischen Wechselrichters auf Basis von SiC-Halbleitern mit hoher Ausgangsfrequenz und direkter Luftkühlung für den Einsatz in Hybridfahrzeugen bei Umgebungstemperaturen von 120 °C detailliert untersucht.

Die Forschung und Entwicklung im Bereich Hybrid- und Elektrofahrzeuge hat sich in den letzten Jahren stark intensiviert und wächst von Jahr zu Jahr weiter. Leistungselektronische Umrichter als Bindeglieder zwischen dem Energiespeicher einerseits und dem elektrischem Antrieb oder Verbrauchern im Niederspannungsbordnetz andererseits stehen hier im Vordergrund. Der Einsatz von Leistungselektronik im Automobil ist durch besondere Anforderungen an Leistungsdichte, Leistungsgewicht, Effizienz und Kosten gekennzeichnet. Weiterhin wird eine hohe Resistenz gegen widrige Einsatzbedingungen, z. B. extreme Umgebungstemperaturen und Vibrationen, gefordert. Darüber hinaus gibt es einen Trend zum Einsatz kompakter hochdrehender elektrischer Maschinen, die signifikant höhere Ausgangs- und Schaltfrequenzen leistungselektronischer Konverter erfordern. Neueste Halbleiterbauelemente auf Basis von Siliziumkarbid (SiC) ermöglichen hohe Schaltgeschwindigkeiten und einen Betrieb bei hoher Sperrschichttemperatur und können so potentiell einen Beitrag zur Erfüllung dieser Anforderungen leisten. Allerdings haben bisher hochkompakte Konverter mit SiC-Schaltern und -Dioden für hohe Umgebungstemperaturen in der Literatur relativ wenig Beachtung gefunden.

Zu Beginn dieser Arbeit werden daher aktuelle SiC-Leistungsschalter umfassend für ihren möglichen Einsatz im beschriebenen Wechselrichter im Hinblick auf flächenbezogenes Leitverhalten in Vorwärts- und Rückwärtsrichtung, Schaltverhalten, Temperaturverhalten, Paral-

lelisierbarkeit, Zuverlässigkeit und Sicherheit im Fehlerfall evaluiert. Auf Grund der um eine Größenordnung höheren Durchschlagsfeldstärke von SiC im Vergleich zu Silizium (Si) können auch in der betrachteten Sperrspannungsklasse von 1,2 kV und bei erhöhter Sperrschichttemperatur unipolare Bauelemente mit niedrigeren Schaltverlusten und dem zusätzlichen Freiheitsgrad der Parallelisierung (Verringerung der Leitverluste) vorteilhaft eingesetzt werden. Insbesondere Zuverlässigkeitsüberlegungen beim aktuellen Stand der SiC-Halbleitertechnik führen zu Vorteilen für «*junction field effect transistors*» (JFETs), wobei für spannungseingeprägte Konverter wie im vorliegenden Fall ein selbstsperrendes Bauelement favorisiert wird. Wegen der auftretenden hohen Sperrschichttemperaturen über dem technologischen Limit von Si wird eine reine SiC-Lösung und daher ein neuartiger selbstsperrender JFET bevorzugt.

Eine detaillierte Analyse des Verlustverhaltens über der Temperatur in Bezug auf gegebene Konverterparameter wie Zwischenkreisspannung, Schaltfrequenz und thermischer Widerstand von der Halbleitersperrschicht zur Umgebung zeigt, dass eine Sperrschichttemperatur von 250 °C eine Ausnutzung des Halbleiters zu mehr als 90% bei einer Umgebungstemperatur von 120 °C erlaubt.

Im Folgenden werden neue Schaltungstopologien zur Ansteuerung der eingesetzten selbstsperrenden JFETs unter Berücksichtigung parasitärer Effekte sowie individueller Anforderungen des neuartigen SiC-Schalters erforscht, die in ihrer Komplexität hinsichtlich der Abfolge und Dimensionierung der notwendigen Spannungsniveaus die Anforderungen heutiger Si-Bauelemente übersteigen (z. B. 3 V im eingeschalteten Zustand, Sicherstellung einer äußerst geringen Störempfindlichkeit im ausgeschalteten Zustand, was bei einer Schwellenspannung von nur 0.7 V und einer inhärent hohen Miller-Kapazität eine große Herausforderung darstellt, und ±15 V während der Schaltvorgänge). In diesem Zusammenhang wird eine neue wechselstromgekoppelte Ansteuerschaltung vorgestellt, die einen sicheren schalt- und leitverlustminimalen Betrieb des selbstsperrenden JFETs ohne die bisher in der Literatur erwähnten Einschränkungen in Bezug auf Schaltfrequenz oder Wärmeentwicklung erlaubt.

Im Hinblick auf den DC-AC-Konverter selbst wird ein mechanisches Gesamtkonzept des Inverters mit 50 kHz Schaltfrequenz erforscht, das neue Wege zur Lösung von elektrischen und thermischen Zielkonflikten beinhaltet. Insbesondere der Betrieb der Ansteuer- und Regelelektro-

nik für Leistungshalbleiter mit einer Sperrschichttemperatur von 250 °C innerhalb des spezifizierten Betriebsbereichs (Temperaturbelastung der Komponenten) wird durch geeignete Platzierung und Kühlmethoden sichergestellt, unter gleichzeitiger Berücksichtigung der elektrischen Anforderungen im Hinblick auf Obergrenzen der Zuleitungsinduktivitäten und Symmetrieanforderungen hinsichtlich der Komponentenanordnung. Eine optimierte aktive Kühlung der Signalelektronik mit Hilfe eines Peltierelements wird hierzu effizienzoptimal ausgelegt und eingesetzt.

Zur volumenminimalen Luftkühlung der eingesetzten Leistungshalbleiter wird ein Hochtemperaturlüfter mit vergleichbaren fluiddynamischen Eigenschaften bei 120 °C wie kommerzielle best-in-class Lüfter bei 20 °C untersucht, der vorteilhaft für in dieser Dissertation beschriebene Hochtemperaturanwendungen bis zu einer Lufttemperatur von 250 °C bei einer Drehzahl von $19'000\,\mathrm{min}^{-1}$ betrieben werden kann. Dies beinhaltet den mechanischen Lüfteraufbau, das magnetische und mechanische Design der elektrischen Maschine unter Rücksicht auf Wärmedehnungen und zulässige Maximaleinsatztemperaturen der Materialien, die Schaufelradgeometrie sowie die Materialwahl für Welle, Lager, Lagergehäuse, Blechpaket, Magnete und Wicklungen.

Zur Regelung des Konvertersystems mit SiC-Halbleitern, die unter Volllast eine Sperrschichttemperatur von bis zu 250 °C erreichen, wird ein Konzept zur potentialgetrennten Strommessung bei Umgebungstemperaturen von 250 °C in Bezug auf hohe Genauigkeit, Breitbandigkeit für Messungen von Wechselströmen mit Frequenzen bis 1 kHz und Gleichströmen sowie Störunempfindlichkeit bei auftretenden Potentialänderungen des den zu messenden Strom führenden Leiters von $30\,\mathrm{V/ns}$ erforscht und realisiert.

Abschließend werden die erforschten, neuartigen Konzepte zur sicheren und verlustminimalen Ansteuerung der eingesetzten JFETs, zum Inverterdesign, zur volumenminimalen Kühlung mittels eines neuen Hochtemperaturlüfters und zur potentialgetrennten Hochtemperaturstrommessung im Rahmen einer experimentellen Systemanalyse an Hand eines Demonstratorsystems bei bis zu 250 °C verifiziert. Eine Einordnung der technischen Ergebnisse in den automobilen Gesamtkontext rundet die Arbeit ab.

Chapter 1

Introduction

1.1 Motivation

1.1.1 Hybrid Electric Vehicles

The commercial success of a product in a free market economy is determined to a large extent by the result of the sovereign consumer's alternative evaluation of competing products [1]. In the automotive industry, the customer typically compares several features such as driving dynamics, equipment, comfort, individuality, design, brand image, quality of workmanship, load capacity as well as acquisition and operating costs when buying a passenger or commercial vehicle. The order of these characteristics does not represent a weighting — depending on vehicle segment and target group, large differences in the priorities set by the customer are possible [2].

Almost all vehicle and consumer groups, however, have the importance of fuel consumption in common, which is reflected in several of the features mentioned. In particular, fuel consumption has continuously increased the operating costs of a vehicle for decades and this fact is immediately brought home to the consumer on a regular basis when refueling, in contrast to, e.g., the cost of capital needed to buy the vehicle. Besides fuel prices, public awareness about potential consequences of burning fossil fuels in terms of environmental effects and security of supply is increasing which leads to a higher social acceptance of vehicles with lower fuel consumption and associated lower Carbon Dioxide

(CO_2) emissions. As a result, legal limits for the CO_2 emissions within a given test cycle have been set [3] and the legal framework of important markets might become even more restrictive in the future [4].

A reduction of the energy demand resulting in setbacks with respect to the features outlined at the beginning, e.g. in the driving dynamics or comfort, is — in the best case — only hardly accepted by the customer. On the contrary, when purchasing a new vehicle, significant progress is generally expected in these areas. Hence, the objective of a lower fuel consumption has to be achieved mainly with increased efficiency. A large variety of profound measures concerning all areas of vehicle development has been taken so far.

With respect to the drive train, it has been found that hybrid electric vehicles (HEVs), which are typically driven by a combination of the conventional internal combustion engine (ICE) and an electrical machine, can be capable of reducing the fuel consumption [5] as well as combining a higher mileage and improved longitudinal dynamics at the same time, thus allowing an increased fuel efficiency [6]. All resulting benefits as well as drawbacks of HEVs are specific to the vehicle category and also depend on the technological advancements in the area of the components needed for HEVs. Hence, a concluding evaluation of HEVs is currently still subject to a comprehensive discussion.

As a result, HEVs launched to the market up to now show different degrees of hybridization. For the main degrees, power electronic converters are used to drive the electrical machine in the vehicle's drive train or to supply electrical energy to loads on different voltage levels from a high voltage traction battery. As of today, automotive power electronics face technological limitations that put their use under several constraints leading to an increased amount of weight, volume, complexity, and thus costs which are currently added to HEVs, as shown in Section 1.1.2, compared to their conventional counterpart.

This dissertation presents — enabled by the availability of novel power semiconductor devices based on silicon carbide (SiC) — generic research on power electronics that contribute to a significant reduction of the system complexity of the electrical part of the drive train by meeting inherent requirements for power electronic traction inverters employed in HEVs in terms of higher ambient temperature rating and power density. In addition, the investigated traction inverter is designed for driving electrical machines with increased power density and specific power by providing ac currents with higher output frequencies.

1.1.2 Fundamental Power Electronic Challenges in HEVs

High Power Density

In general, both weight and volume are key performance indicators for automotive components: A higher vehicle mass leads to higher energy demand when accelerating or going uphill (which can never be fully recovered, if it can be at all), reduced vehicle dynamics and a stronger chassis construction including suspension, brakes, and tyres or a reduced payload for the same chassis construction [7]. In a similar way, a higher volume demand of a particular component leads to higher restrictions for designing the vehicle, placing this component, or a lower loading space.

Especially for vehicles that are offered as both, conventional and hybrid electrical vehicles, the additional volume and weight introduced by the components of the electrical part of the drive train should not affect the vehicle characteristics or performance such that the advantages of having two propulsion systems finally turn into a disadvantage when customers compare the hybrid model to its direct conventional counterpart. As with today's technology the traction battery needed for the hybrid alternative adds a significant portion of weight and volume compared to conventional vehicles, it is even more important for the other main components of the hybrid type, such as the power electronics (and the electrical machine) to be as lightweight and as small as possible for a given output power.

High Output Frequency of Traction Inverters

The volume of an electrical machine is determined by the rated torque M of the machine for a given magnetic excitation, machine current, and number of turns [8]. According to Equation (1.1), the torque and thus volume of the machine can be reduced by the same amount as the mechanical machine speed n_m is increased for a constant mechanical output power rating P_m,

$$P_\mathrm{m} = \omega_\mathrm{m} \cdot M = 2\pi \cdot n_\mathrm{m} \cdot M. \tag{1.1}$$

As a result, a trend towards electrical machines for HEVs with higher rotational speeds and a reduction gear can be observed [9]. An industrial example of this trend can be given by comparing the Toyota Prius

models of the second (model year 2004) and actual third generation (model year 2010): The maximum speed of the permanent magnet synchronous machine at which the machine is able to provide its rated torque is increased by a factor of 2.3 from 1'190 min^{-1} to 2'770 min^{-1} and the power by 1.2 from 50 kW to 60 kW. This leads directly to a torque reduction by a factor of 1.9 from 400 Nm to 207 Nm [10], which is also in agreement with Equation (1.1).

Due to efficiency considerations and in order to make full use of the dc-link voltage which increases from a maximum value of 500 V in the 2004 Prius to 650 V in the 2010 model, the machine design is slightly changed, e.g. the stator current is reduced by 26%, the number of stator turns is increased by 18% and magnets with an 8% higher remanence flux density are used [5, 10]. Because of the changes which result in a 15% lower torque density for the model year 2010 machine, the volume (and the mass) of the 2010 Prius is not exactly cut in half compared to the 2004 model: The outer diameter of the machine is virtually unchanged (1.9% lower), but the axial length of rotor and stator and thus the volume of the machine is reduced to 60% of the model year 2004 machine which is mainly achieved with 230% higher speed and a reduction of the torque to 52% leading to an increase of the power level to 120%.

A tyre of a typical dimension for a compact car such as the Toyota Prius, e.g. 195/65 R 15, has got a rolling circumference of approximately 2 m and thus rotates at a vehicle speed of 120 $\mathrm{km/h}$ with 1'000 min^{-1}. Larger tyres for larger cars rotate with lower speed. The rotational speed of an ICE employed in road vehicles is between 600 min^{-1} and 8'000 min^{-1}. To reduce a high rotational speed of the electrical machine, a reduction gear can be employed, as it is done in the 2010 Prius [10].

Limits to the machine speed are in general set by the mentioned reduction gear, high frequency losses, air friction as well as the material strength and thus depend on the power rating of the machine. For typical power levels of around 100 kW for HEV traction machines, machines with a maximum rotational speed of around 60'000 min^{-1} are known in other application areas [11]. The maximum speed of the 2010 Prius is 13'500 min^{-1} and in the literature, electrical machines for HEVs rotating at 20'000 min^{-1} with a power of 90 kW are shown [9].

A high speed electrical machine requires the dc-ac inverter to drive the machine with an ac current having a frequency f_O that at least equals the rotational speed n_m of the machine, if the machine has got

one pole pair p, according to Equation (1.2). A higher number of pole pairs allows a proportional reduction of the machine flux for the same torque. Hence, the iron cross-section conducting the flux can be decreased for a constant flux density within the iron. In this way, the amount of iron and thus the machine weight and volume can be further decreased,

$$f_{\mathrm{O}} = n_{\mathrm{m}} \cdot p. \tag{1.2}$$

A high converter output frequency f_{O} makes a high switching frequency of the power semiconductors necessary for a sinusoidal output current which is desired to reduce the losses in the machine caused by the harmonic content of the current fed into the machine [12]. A high switching frequency, however, leads to higher switching losses. The switching frequency of 50 kHz of the converter system investigated in this dissertation covers a wide speed range for electrical machines employed in HEVs and keeps the volume and weight of passive filter components, such as common mode output inductors, low. It also allows to extend the potential area of application to other industrial sectors where high speed drives are employed.

High Ambient Temperature

The main portion of the heat generated by the combustion process in ICEs employed in (hybrid electrical) vehicles is today typically transferred by a liquid coolant (a mixture of water and ethylene-glycol) to the ambient air around the car. The temperature level of the coolant is found as a trade-off between on the one hand the efficiency of the ICE that is to be maximized and on the other hand the temperature limits of the construction materials and the coolant, taking its boiling point into account. Usually coolants are operated between 90 °C and 120 °C after warm-up of the engine; their specified operating temperature range is between -40 °C and 120 °C [13, 14]. Hence, also the air underneath the engine hood can heat up to an ambient temperature of $T_{\mathrm{A}} = 120\,^{\circ}\mathrm{C}$ and even further to higher values close the exhaust system [13, 15].

Today's power electronic converters for HEVs feature silicon (Si) power semiconductors which corresponds to the state of the art of power electronics in the vast majority of application areas. Si though has got a high intrinsic charge carrier concentration which increases further with temperature (*cf.* Figure 1.1) due to random thermal oscillation

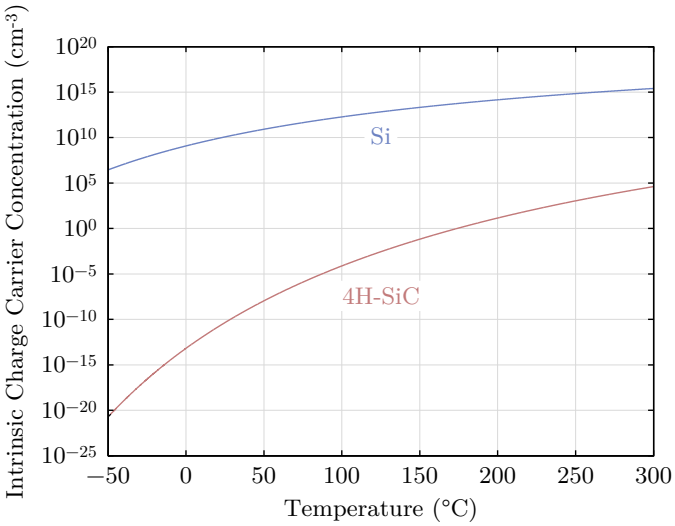


Figure 1.1: Intrinsic charge carrier concentration of silicon and silicon carbide over temperature [17,18]. The intrinsic charge carrier concentration of SiC is below the respective value of Si up to the melting point of Si at 1420 °C, making significantly higher operating temperatures up to more than 400 °C possible for SiC compared to typically 175 °C for Si (*cf.* Equation (2.1)).

of Si atoms leading to broken interatomic bonds such that intrinsic conduction begins at a certain threshold temperature which depends also on the blocking voltage. Thus, the junction temperature of high voltage Si semiconductors is typically subject to an upper temperature limit between 150 °C and 175 °C [16].

In order to effectively remove the heat dissipated by the power semiconductor switches, a sufficiently large temperature difference between the semiconductor junction, where the switching and conduction losses of the switches occur, and the coolant has to be maintained. That is, the temperature of the coolant for the power electronic converter based on Si semiconductors has to be well below the temperature level of the cooling circuit of the Ice, and is typically around 65 °C [19]; thus today two separate water-ethylene-glycol circuits are needed. The hybrid models of the Volkswagen Touareg (model year 2010), Porsche Cayenne (model year 2010) and Panamera (model year 2011) [5,6] as well as pre-

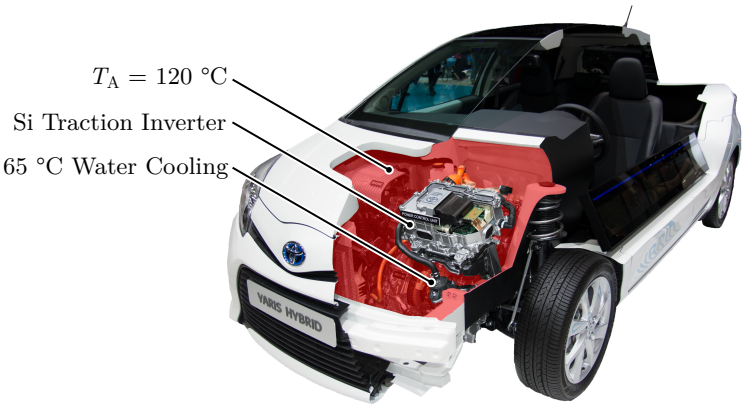


Figure 1.2: Toyota Hybrid Synergy Drive in a Yaris Hybrid of the model year 2012: Industrial example of a traction inverter with Si IGBTs which is placed under the engine hood with ambient temperatures up to 120 °C and hence requires a low temperature water cooling circuit. (Photograph taken at the world premiere of the Toyota Yaris Hybrid at the 82nd Geneva International Motor Show in March 2012.)

vious and actual generations of the Toyota Hybrid Synergy Drive (*cf.* Figure 1.2) used for most of the Toyota and Lexus HEVs [10, 20–22] can be given as industrial examples of this concept.

With silicon carbide (SiC), a group III-IV compound semiconductor material, a new option has become available, that can be used for power semiconductor switches [23]. The intrinsic charge carrier concentration of its crystal structure 4H, that is today mainly used for power semiconductor devices made of SiC (*cf.* Section 2.2), is also depicted in Figure 1.1. Up to the melting point of Si at 1410 °C, the intrinsic charge carrier concentration of SiC is always lower than the respective value for Si which is mainly due to the larger band-gap of SiC compared to Si (*cf.* Section 2.2). At 995 °C, 4H-SiC reaches the intrinsic charge carrier concentration which Si shows at 175 °C. Compared to Si, SiC switches are thus capable of significantly higher operating temperatures of (theoretically) more than 400 °C [24].

Junction temperatures exceeding today's limit of 175 °C of course affect the efficiency of the converter due to rising losses with increasing temperate as will be shown in Chapter 3 and require significant advancements in the packaging of power semiconductors. Novel join-

ing and bonding technologies such as low temperature sintered silver die attachment and copper bonding instead of aluminium bonding are currently investigated and promise considerably improved reliability for thermal cycling with increased temperature swing [25–27].

The benefit of a higher junction temperature of power semiconductors in converters for HEVs is the chance to make the separation of the cooling circuits obsolete as the junction temperature can be increased beyond 175 °C and thus a significant temperature difference to the ICE coolant at 120 °C can be established which is increasingly highlighted by car manufacturers such as Toyota [19, 28, 29]. Hence, some high ambient temperature converter concepts with SiC have been presented in the literature [30–34] and research centers of car manufacturers work on the production of SiC devices [35, 36]. Furthermore, alternative cooling concepts such as pure air-cooling even in hot environments become feasible. Ambient-air-cooled converter systems can reduce the overall system complexity compared to water cooling as pumps, water pipes, the water-ethylene-glycol fluid itself and heat exchangers are not needed any more. For this reason, other components of the electrical drive train, e.g. the traction battery, are already air-cooled. This can significantly increase the flexibility in arranging the converters within the vehicle, helping both, to turn conventional models into HEVs and to develop novel car concepts [13, 14].

Accordingly, air-cooled power electronic converters can already be found in current HEVs, e.g. in the 2006 Honda Civic Hybrid model. As these drive inverters still feature Si power semiconductors, the ambient air used for cooling needs to be of low temperature. Hence, the gain in arrangement flexibility is not as high as with SiC because they cannot be placed, for example, in the engine compartment: For the Honda Civic, the drive inverter is placed behind the rear seat to ensure a low ambient air temperature level [37,38] — in contrast to many other HEVs, such as the Toyota or Lexus hybrid models, where the low-temperature-water-cooled converter is placed in the engine compartment. Additionally, placing the drive inverter close to the electrical machine (which means for many of today's HEVs in the engine compartment) is favorable in terms of electromagnetic interference (EMI) as the switched high voltages do not need to be transmitted for a long distance within the car.

Hence, in this dissertation, a compact three-phase dc-ac inverter system for HEVs using SiC semiconductors is investigated in detail that is directly cooled with ambient air of up to 120 °C and thus offers a sig-

nificantly increased flexibility regarding its mounting location without the need for a complex and costly water cooling circuit. Due to its high switching frequency, the converter is able to drive high speed electrical machines with increased power density.

Besides the SiC power semiconductors, further critical components needed for the realization of the high temperature converter system are identified: The specific temperature ranges as well as functional requirements of dc-link capacitors, current, voltage, and temperature measurement, control electronics, auxiliary power supplies, and heat sinks with fans to cool the power semiconductors are taken into account when designing the inverter system. In some cases, such as the cooling fans and the current measurement, no adequate component or concept was found on the market or in the literature and hence, research on these components leading to the design and realization of a high temperature current measurement and a high temperature fan, is also part of this dissertation.

1.1.3 Further Application Areas

Compact converters with high ambient temperature and output frequency rating are also requested in other application areas than the automotive industry, e.g. in the aerospace industry: Possible astronautical applications include the exploration of the surface or atmosphere of other planets with more hostile environmental conditions [39]. The aviation industry is currently working towards More Electric Aircraft in order to substitute the heavy and inflexible hydraulic infrastructure. As the energy in an aircraft is converted by a combustion process of fossil fuels, the ambient temperatures for power electronic converters are likely to be in a comparable range like for automotive or also military applications [40]. Downhole applications in the oil and gas industry also have to deal with harsh environmental conditions such as high pressure and high ambient temperature [41, 42].

1.2 Outline

Chapter 1

At the beginning of this dissertation, the research on the investigated high temperature / power density / output frequency SiC dc-ac con-

verter system for hybrid electric vehicles is motivated and the specifications and challenges of the system are demonstrated.

Chapter 2

First, a comprehensive evaluation of state-of-the-art SiC power semiconductors is conducted regarding their potential use in the described inverter system in terms of area-specific conduction properties in forward and reverse direction, switching behavior, thermal behavior, ability for parallelization, reliability, and safety in case of a fault. The 1200 V normally-off SiC JFET manufactured by SemiSouth Laboratories, Inc. is selected for the investigated inverter system.

Chapter 3

The temperature behavior of the conduction and switching losses of two different SiC JFETs is analyzed, leading together with converter parameters such as dc-link voltage, switching frequency, thermal resistance from the power semiconductor junction to the ambience and ambient temperature to the exemplary derivation of an inherent temperature limit for the thermally stable operation of SiC power semiconductors. It is shown, how this junction temperature, that also allows best utilization of the expensive SiC power semiconductor die area in terms of current carrying capability, can be derived for given system parameters, and the influence of these parameters on the temperature limit and thus the die utilization is analyzed.

Chapter 4

The requirements of the JFET with respect to the gate driver are analyzed in detail and existing gate driver concepts including their shortcomings mentioned in the literature are reviewed. A novel ac-coupled driving circuit is presented that allows a safe operation of normally-off SiC JFETs with minimum switching and conduction losses.

Chapter 5

A design methodology for the compact forced air-cooled high temperature inverter with a switching frequency of 50 kHz allowing high output frequencies is shown, analyzing and taking electrical and thermal tradeoffs into account. As a result, an overall design concept is presented that

includes active cooling of the signal electronics using a Peltier cooler and allows power semiconductor junction temperatures of 250 °C. The need for essential converter subsystems such as a high temperature fan for the air-cooling and a high temperature current measurement is identified.

Chapter 6

Research on a high performance fan for high ambient temperatures is conducted in order to be able to efficiently cool the power semiconductors employed in the high temperature inverter. This work leads to a fan that has got a comparable fluid dynamic performance at 120 °C as commercial best-in-class fans at 20 °C and can be operated from -40 °C to 250 °C with its full rated power at a rotational speed of $19'000\,\mathrm{min}^{-1}$.

Chapter 7

A galvanically isolated current measurement concept is researched that allows to measure both dc and sinusoidal ac currents up to 1 kHz at an ambient temperature of 250 °C. This enables measurement of (inverter output) currents directly at the power semiconductors with a maximum junction temperature of 250 °C.

Chapter 8

The novel concepts investigated in Chapter 4 to Chapter 7 are validated in a comprehensive experimental system analysis of an industry-oriented demonstrator system at temperature levels up to 250 °C.

Chapter 9

A final consideration puts the technical achievements of the presented work in a broader automotive context.

1.3 Scientific Publications and Awards Related to this Ph. D. Dissertation

Different research topics presented in this dissertation (DOI: 10.3929/ethz-a-009943735) have already been published in international scientific journals, conference proceedings and workshops or are protected by a patent.

1.3.1 Journal Papers

- B. Wrzecionko, A. Looser, J. W. Kolar, and M. Casey, "High-temperature (250 °C / 500 °F) 19'000 min^{-1} BLDC fan for forced air-cooling of advanced automotive power electronics," *IEEE/ASME Transactions on Mechatronics*, accepted for publication in 2014.

- B. Wrzecionko, L. Steinmann, and J. W. Kolar, "High-bandwidth high-temperature (250 °C / 500 °F) isolated dc and ac current measurement: Bidirectionally saturated current transformer," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5404–5413, November 2013. DOI: 10.1109/TPEL.2013.2247632

- B. Wrzecionko, D. Bortis, J. Biela, and J. W. Kolar, "Novel ac-coupled gate driver for ultrafast switching of normally off SiC JFETs," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3452–3463, July 2012. DOI: 10.1109/TPEL.2011.2182209

1.3.2 Conference Papers

- B. Wrzecionko, L. Steinmann, and J. W. Kolar, "Fast high-temperature (250 °C / 500 °F) isolated dc and ac current measurement: Bidirectionally saturated current transformer," in *Proceedings of the 7th International Power Electronics and Motion Control Conference (IPEMC ECCE Asia)*, vol. 1, Harbin, China, 2–5 June 2012, pp. 480–487. DOI: 10.1109/IPEMC.2012.6258777

- B. Wrzecionko, A. Looser, J. W. Kolar, and M. Casey, "High-temperature (250 °C / 500 °F) 19'000 rpm BLDC fan for forced air-cooling of advanced automotive power electronics," in *Proceedings of the 37th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Melbourne, Australia, 7–10 November 2011, pp. 4162–4169. DOI: 10.1109/IECON.2011.6119769

- D. Bortis, B. Wrzecionko, and J. W. Kolar, "A 120 °C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system," in *Proceedings of the 26th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Ft. Worth, TX, USA, 6–10 March 2011, pp. 1282–1289. DOI: 10.1109/APEC.2011.5744758

- B. Wrzecionko, S. Käch, D. Bortis, J. Biela, and J. W. Kolar, "Novel ac coupled gate driver for ultra fast switching of normally-off SiC JFETs," in *Proceedings of the 36th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Glendale, AZ, USA, 7–10 November 2010, pp. 605–612. DOI: 10.1109/IECON.2010.5675214

- B. Wrzecionko, J. Biela, and J. W. Kolar, "SiC power semiconductors in HEVs: Influence of junction temperature on power density, chip utilization and efficiency," in *Proceedings of the 35th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Porto, Portugal, 3–5 November 2009, pp. 3834–3841. DOI: 10.1109/IECON.2009.5415122

- J. Biela, M. Schweizer, S. Waffler, B. Wrzecionko, and J. W. Kolar, "SiC vs. Si — evaluation of potentials for performance improvement of power electronics converter systems by SiC power semiconductors," in *Proceedings of the 13th International Conference on Silicon Carbide and Related Materials (ICSCRM)*, Nuremberg, Germany, 11–16 October 2009, pp. 1101–1106. DOI: 10.4028/www.scientific.net/MSF.645-648.1101

1.3.3 Workshops

- J. W. Kolar, and B. Wrzecionko, "Advanced dc-ac power conversion for automotive applications," International Workshop "Recent Advances on Electrical Machines, Drives and Power Electronics" (in Memoriam of Prof. Alfio Consoli), Catania, Italy, 28 January 2013.

- B. Wrzecionko, D. Bortis, and J. W. Kolar, "Novel gate driver for normally-off SiC JFET and general high temperature SiC converter technology," International SiC Power Electronics Application Workshop (ISiCPEAW), Kista/Stockholm, Sweden, 29–30 May 2012.

1.3.4 Patents

- B. Wrzecionko, J. W. Kolar, L. Steinmann, H. Ertl, S. Sasaki, and H. Tojima,

– "Verfahren zur Messung von elektrischem Strom," Swiss Patent No. 00679/13, 27 March 2013.
– "Electric current measurement method," US Patent No. 13/851,733, 21 March 2013.
– "A method for measurement of electric current," Japanese Patent No. 2012-082382, 30 March 2012.

1.3.5 Awards

- B. Wrzecionko, "A 120 °C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system," Best Presentation Award of the 26th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Ft. Worth, TX, USA, 6–10 March 2011.

1.4 Summary

The introduction motivates the research on hybrid electric vehicles by showing the need for an increased drive train efficiency of passenger or commercial vehicles. With respect to packaging issues of the whole hybrid electric vehicle, it is beneficial to have a high arrangement flexibility of the individual components. This means that the power electronic traction inverter could be placed underneath the engine hood as it is realized in many of today's HEVs in order to avoid a transmission of ac voltages with large transients through the car. The ambient temperature of the inverter can thus be up to 120 °C and hence most of the inverters are today cooled by a separate water cooling circuit of around 65 °C water temperature.

The system complexity of the electrical part of the HEV drive train can be reduced by using the cooling circuit of the internal combustion engine or by directly cooling the inverter with ambient air. With an ambient temperature of 120 °C in both cases, nonzero converter losses and the requirement of a small air-cooling system, the junction temperature needs to increased above today's limit of 175 °C for Si based power semiconductors.

Furthermore, a trend towards electrical machines with higher rotational speeds leading to an increased power density can be observed. This means for the inverter driving the machine that it has to be able to provide ac currents with increased output frequency.

Consequently, in this Ph. D. dissertation a compact traction inverter system for the use in hybrid electric vehicles that can be operated with a switching frequency of 50 kHz at an ambient temperature level of 120 °C is investigated in detail.

Chapter 2

SiC Power Semiconductor Technology

2.1 Power Semiconductor Switches

The basic electrical functionality of the dc-ac inverter for HEVs investigated in this dissertation is the conversion of direct current (dc) drawn from the traction battery of the HEV to alternating current (ac) with a variable frequency and a variable (fundamental) output voltage amplitude in order to drive the electrical machine and thus propel the vehicle. Also, reversed energy flow, i.e. ac to dc conversion, is required when the vehicle decelerates to convert the kinetic energy into chemical energy stored in the battery via the electrical machine and the dc-ac inverter which then operates as a rectifier.

To realize the inverter, controllable switches as the basic building blocks are required that connect the ac output of the inverter to either the positive or negative rail of the dc supply according to the switching signals obtained from the digital control unit. Such switches are nowadays realized using power semiconductors with few exceptions only. The characteristics of an ideal power semiconductor switch include

- conducting arbitrarily large currents in the on-state in the forward or reverse direction with zero voltage drop across the device,

- blocking (infinite) forward and reverse voltage in the off-state with zero leakage current,
- toggling the on- and off-state infinitely fast, and
- requiring no power for the switch drive to control the device.

As such an ideal switch does not exist, an application dependent trade-off has to be made between the different non-ideal power semiconductor device characteristics to match the requirements of a specific application in an optimum way.

With respect to the physical principle of operation, blocking voltage, and current carrying capability, a large variety of power semiconductor switches made of doped silicon (Si) is available and used in the vast majority of applications. The availability and commercialization of switches made of the group III-IV compound semiconductor silicon carbide (SiC) has further increased the diversity of power semiconductor devices and opens up new application areas.

As outlined in Section 1.1.2, the need for higher junction temperatures makes the use of SiC power semiconductors inevitable for the inverter system at hand. In order to understand the differences between Si and SiC as well as the specific needs coming with SiC devices, in this chapter the material properties of Si and SiC are compared with respect to the use in drive inverters for HEVs and selected SiC devices are introduced.

2.2 Comparison between Si and SiC

SiC appears with a single crystalline, poly-crystalline or amorphous structure. For power semiconductors, only the single crystalline structure is of interest which contains more than 200 different polytypes. Recently, research has been concentrated on the 4H-SiC and 6H-SiC hexagonal polytype [43, 44]. Wafers of the 6H-SiC structure were the first to be reproducibly manufactured (a diameter of 1 inch for 6H-SiC in 1989). 4H-SiC though features a higher and nearly isotropic carrier mobility in contrast to 6H-SiC and hence, today the leading SiC device manufacturers prefer to use 4H-SiC for their state-of-the-art switches independent of the type of switch.

Table 2.1: Silicon and silicon carbide material properties [43–50]

Property		Si	4H-SiC	6H-SiC
Band-gap E_G in eV		1.12	3.28	3.08
Breakdown electrical field E_{BD} in $^{MV}/_{cm}$ @ doping level $N_A = N_D = 10^{17}\,cm^{-3}$		0.29	3.0 ($\parallel$ c)	3.2 ($\parallel$ c) > 1 ($\perp$ c)
Intrinsic charge carrier concentration n_i in cm^{-3}		10^{10}	$5 \cdot 10^{-9}$	$1.6 \cdot 10^{-6}$
Charge carrier mobility μ_n, μ_p in $^{cm^2}/_{Vs}$ @ doping level $N_{A/D} = 10^{16}\,cm^{-3}$	Electrons	1430	900 ($\parallel$ c) 800 ($\perp$ c)	60 ($\parallel$ c) 400 ($\perp$ c)
	Holes	480	115	90
Saturated electron drift velocity v_D in $10^7\,^{cm}/_{s}$ @ doping level $N_D = 4.8 \cdot 10^{16}\,cm^{-3}$		1	2	2
Static relative dielectric constant ϵ_r		11.9	10.3 ($\parallel$ c) 9.8 ($\perp$ c)	10.0 ($\parallel$ c) 9.7 ($\perp$ c)
Thermal conductivity λ in $^{W}/_{cm \cdot K}$		1.31	4.9	4.9
Coefficient of linear thermal expansion α_{CTE} in $^{10^{-6}}/_{K}$		4.1	3.25	3.15
Commercial wafer diameter (Status Dec. 2012) in mm		300	150	100

Table 2.1 compares important physical properties of Si and 4H-SiC as well as 6H-SiC. All physical properties are given for a material temperature of $T = 300\,K = 27\,°C$. The expressions "($\parallel$ c)" and "($\perp$ c)" indicate the direction "parallel" and "orthogonal", respectively, to the c-axis which denotes the axis being perpendicular to the hexagonal footprint of the crystal.

The significantly higher energy difference between the conduction and the valence band, termed band-gap E_G, of SiC (approximately a factor of 3) is the essential physical difference between Si and SiC that leads to a large difference in intrinsic charge carrier concentration n_i at

a given temperature (*cf.* Figure 1.1) due to the exponential correlation between n_i and E_G as can be seen from

$$\begin{aligned} n_\mathrm{i} &= \sqrt{n_\mathrm{n} n_\mathrm{p}} = \sqrt{N_\mathrm{C} N_\mathrm{V}} \cdot \mathrm{e}^{-\frac{E_\mathrm{G}}{2 k_\mathrm{B} T}} \\ &= T^{3/2} \cdot 10^{16}\,\mathrm{cm}^{-3}\mathrm{K}^{2/3} \begin{cases} 3.87 \cdot \mathrm{e}^{-\frac{7.02 \cdot 10^3\,\mathrm{K}}{T}} & \text{for Si} \\ 1.70 \cdot \mathrm{e}^{-\frac{2.08 \cdot 10^4\,\mathrm{K}}{T}} & \text{for 4H-SiC} \end{cases} \end{aligned} \tag{2.1}$$

where a slight temperature dependency of E_G is neglected [18] and n_n and n_p denote the electron and hole density, respectively, N_C and N_V the density of states in the conduction and valence band, respectively, k_B the Boltzmann's constant and T the material temperature [17]. This is — amongst other properties, like resistance against diffusion, erosion, and corrosion at high temperatures — the fundamental physical reason for the high temperature capability of SiC power semiconductors [44].

High temperature capability of SiC enables the research of this dissertation, but SiC offers further benefits for the application in a dc-ac drive inverter and power electronic converters in general: The ten times higher breakdown electrical field E_BD, sometimes also called critical field E_c, compared to Si (for a given acceptor or donator doping concentration N_A or N_D) allows to fabricate power semiconductors with drift regions that can be thinner and/or more heavily doped. Both measures lead to a lower area-specific on-resistance r_on of the load current path compared to Si devices with the same blocking voltage rating. At the same time, the lower r_on allows for unipolar devices made of SiC which are not manufactured in Si because they would be outperformed by Si bipolar devices for most applications (*cf.* Section 2.3). An overview of the different attempts to exactly quantify the advantage of SiC over Si in terms of r_on also taking the charge carrier mobility and the saturated electron drift velocity into account can be found in [18].

The three times higher thermal conductivity of SiC compared to Si helps to reduce the overall thermal resistance from the power semiconductor junction to the ambience, even though the share of the thermal resistance of the power semiconductor die is typically small compared to the package and heat sink resistance. A more important advantage of the higher thermal conductivity is the increased lateral heat flow which can help to reduce lateral temperature differences within a single die, so called “hot spots”: Small deviations from an ideally even current distribution across the semiconductor die (e.g. due to local differences in the impedances of the switching cells) lead to an un-

even loss distribution and thus to lateral temperature differences. The increased lateral heat flow leads to a better heat spreading for these hot spots. Furthermore, if the converter design is such that the semiconductor is almost fully utilized in terms of current density during full load operation, low lateral temperature differences in the die can prevent local thermal runaway in some die sections (*cf.* Chapter 3).

SiC is still behind state-of-the-art Si technology in the fields of

- material cost [48, 51],
- defect density [51], and
- wafer size [48, 49],

with the latter two reducing yield. All this leads to higher area-specific costs of SiC. However, due to the above mentioned superior physical properties of SiC compared to Si, a smaller semiconductor area can be sufficient for the same application. Furthermore, advantages such as the higher junction temperature capability can lead to complexity and thus cost reduction on a system level as outlined in Section 1.1.1. Other benefits including loss reduction and switching frequency capability that can lead to volume and thus cost reduction have to be taken into account when comparing the system costs for a solution based on Si or SiC.

2.3 Unipolar vs. Bipolar Power Semiconductors

In bipolar power semiconductors like the pn-diode, the bipolar junction transistor (BJT) or the insulated gate bipolar transistor (IGBT), crystal junctions of n- and p-doped power semiconductors in the main current path are reverse and forward biased during device operation. Under forward bias, two main physical aspects influence the conduction and switching behavior of a bipolar device: First, a voltage drop across the junction occurs due to the potential barrier of a pn-junction, which is in a power BJT or IGBT only partially canceled out by the anti-series connection of pn-junctions due to different doping levels of each junction. Second, minority carriers are injected into the drift region leading to an excess charge carrier density and thus to a significant decrease in the resistance of the drift region during the on-state of the device. This effect is sometimes referred to as conductivity modulation [52].

In unipolar devices, the pn-junction in the main current path is eliminated during the on-state of the device by a n-channel caused by the field effect (in the case of a n-MOSFET) or there is no pn-junction at all in the current path (in case of a JFET, where the channel is blocked in the off-state only by depletion caused by an adjacent pn-junction which is not in the switch current path, or in a Schottky diode). In this case, the only charge carriers are majority carriers and the conduction losses are caused by the resistivity of the channel and drift region except for Schottky diodes, which also show a forward voltage drop due to a potential barrier (which is lower than that of a pn-junction).

The first effect appearing in bipolar devices means that in contrast to unipolar devices an (especially for bipolar SiC devices) non-negligible voltage drop remains for non-zero switch currents. Due to the decreasing diffusion coefficients with increasing temperature, this voltage drop is lower at higher junction temperatures. The second effect leads to the fact, that the resistivity of the drift region of bipolar devices is typically lower than for unipolar devices for the same blocking voltage. Additionally, the increase in resistivity of the drift zone with the junction temperature is not as distinct as it is for unipolar devices, because the decrease of the charge carrier mobility with increasing temperature is opposed by the increased carrier lifetime leading to an increase in the stored excess minority charge carriers enhancing the conductivity modulation [53].

Both effects together mean for bipolar devices, that the conduction losses can be modeled as a first approximation by the switch current flowing through the series connection of a voltage source and a resistor. Thus, a parallelization of several devices in order to reduce the current density in each device does not pay off in the same way as it does for unipolar switches with purely resistive behavior. Additionally, most unipolar devices are able to conduct current in the reverse direction (often referred to as synchronous rectification) in contrast to bipolar devices, so that the conduction losses of an anti-parallel diode can be reduced in some converter topologies. Hence, with respect to the overall conduction losses of a power semiconductor employed in a certain power electronic converter, it depends on the resistivity and thus blocking voltage class, junction temperature levels and/or maximum allowed semiconductor area whether bipolar or unipolar semiconductors offer lower losses.

With respect to the switching losses, the conductivity modulation of bipolar devices turns into a disadvantages as the minority carriers need to be removed by recombination and/or negative switch currents from the drift region. This leads to slower switching transients with increased losses compared to unipolar devices which only require stray and depletion layer capacitances to be charged.

Together with the considerations in terms of the conduction losses, it can be said, that generally, for low voltages, unipolar devices are preferred, and for high voltages, bipolar devices are chosen. A universal, exact voltage limit cannot be given as it depends on converter characteristics, for instance the mission profile leading to certain junction temperature levels as discussed or the switching frequency, and also on the semiconductor material the switches are made of. For Si the range of uncertainty ranges for most application from around 400 V to 900 V [52]. The dc-link voltage of the dc-ac inverter system investigated in this dissertation is below 1 kV because of partial discharge problems within the machine (among other issues) occurring for higher voltage levels.

With SiC, the voltage range changes for two reasons: First, the height of the described potential barrier depends on the band-gap, which is significantly higher for SiC than for Si according to Table 2.1 leading to a high on-state voltage drop for bipolar devices. Second, the resistance of the drift region is smaller as shown in Section 2.2 reducing the on-resistance of unipolar devices in SiC compared to unipolar Si devices.

Hence, with SiC, the majority of devices that are introduced and attract interest in the 1200 V blocking voltage class is unipolar, namely Schottky diodes (*cf.* Section 2.4), junction field effect transistors (JFETs, *cf.* Section 2.6), and metal-oxide-semiconductor field effect transistors (MOSFETs, *cf.* Section 2.5). In the literature, a blocking voltage of 3 kV to 5 kV is seen as a rough border between unipolar and bipolar power semiconductors for SiC [18] which is more than a factor of three higher than the dc-link voltage of the inverter system at hand. The high switching frequency of 50 kHz is a second reason to further consider only unipolar devices.

2.4 Schottky Diodes

Schottky diodes are made of a Schottky junction of a doped semiconductor material and a metal. In contrast to bipolar pn-junction diodes, Schottky diodes are thus unipolar devices as only majority carriers are involved in the basic operation of the diode. In most diodes n-type semiconductors are used due to their higher electron mobility (*cf.* Table 2.1). The on-state losses of Schottky diodes are also lower than of pn-junction diodes because of the lower potential barrier height of a metal-semiconductor (Schottky) contact. The drawback of this low barrier is increased reverse leakage current compared to pn-diodes which further increases with junction temperature. This drawback can be weakened by the design of the diode — at the expense of higher forward voltage drop though [44]. The absence of a pn-junction and therefore of a space charge region in a Schottky diode leads to far lower switching losses compared to a pn-junction diode as no reverse recovery transients occur and only the capacitive charge of the junction has to be taken into account.

With Si, Schottky diodes are not available for blocking voltages above a few hundred volts due to the low breakdown electrical field of Si [52]. The large breakdown electrical field of SiC, however, allows the fabrication of high voltage Schottky diodes (up to 10.8 kV [54]). The forward voltage drop is due to the large band-gap higher for SiC than for Si.

2.5 Metal Oxide Semiconductor Field Effect Transistors

In Si, the most popular unipolar controllable power semiconductor is the MOSFET [17]. In SiC though, the silicon dioxide (SiO_2) isolating the gate from the channel suffers from interfacing issues to the semiconductor material as of today: First, the electric field in the oxide exceeds the reliability limit if the higher breakdown electrical field of SiC (*cf.* Table 2.1) is utilized in the drift region. Second, a high interface state density leads to a lower channel mobility and thus increased on-resistance of the device. Third — this is especially important for high junction temperature operation — the high band-gap of SiC compared to Si (*cf.* Table 2.1) leads to a smaller band offset between the

conduction band edges of SiC and SiO_2 leading to instability of the threshold voltage and decreased dielectric reliability of the gate oxide due to hot electron injection from SiC into SiO_2 [17, 18, 55, 56].

The area specific electrical resistance of the drain-source path in the on-state, $r_{DS,on}$, is higher than for JFETs. Due to the high costs of SiC dies (*cf.* Section 2.2), this is together with the previously mentioned interfacing issues especially at high temperatures a significant decision criterion when selecting a power semiconductor for the investigated automotive drive inverters system.

2.6 Junction Field Effect Transistors

Power Junction Field Effect Transistors (JFETs) belong to the emerging devices benefiting from the progress made in SiC technology: In general, the gate-source voltage V_{GS} applied to the JFET should on the one hand be lower than the built-in voltage V_{bi} of the pn-junction as otherwise the device starts to operate in its bipolar mode which leads to significant hole injection into the channel [57]. On the other hand, V_{GS} must be higher than the threshold voltage $V_{GS,th}$ for the device to conduct. With increasing temperature, $V_{GS,th}$ shifts towards smaller values [58].

Si pn-junctions feature a very low V_{bi}, which would lead to a very small range of allowed voltages for V_{GS}, if $V_{GS,th}$ was still expected to be above zero. Hence, Si JFETs are normally-on or depletion mode devices, which makes them less desirable for most applications than MOSFETs which can be manufactured much more easily in Si than in SiC (*cf.* Section 2.5).

Because of the very low intrinsic charge carrier concentration of SiC (*cf.* Figure 1.1) the built-in voltage of SiC pn-junctions is — compared to Si — very high, i.e. around 3 V at 25 °C [57]. This makes normally-off or enhancement mode JFETs feasible with SiC. Figure 2.1 visualizes the constraints and resulting voltage ranges for V_{GS}. It is worth mentioning, that for normally-off devices the threshold voltage, which makes the device conduct, is usually referred to as $V_{GS,th}$ analog to the situation with MOSFETs, while with normally-on JFETs the critical voltage, which makes the JFET block, is called pinch-off voltage $V_{GS,po}$.

SiC JFETs are available in several blocking voltage classes, e.g., 650 V, 1200 V and 1700 V [59–63]. In the 1200 V blocking voltage class relevant for the investigated converter system, different manufacturers provide normally-on and -off JFETs with different device structures.

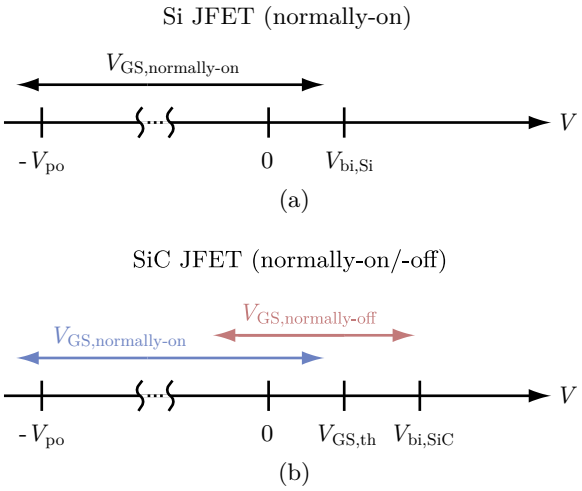


Figure 2.1: Gate-source voltage ranges for (a) normally-on JFETs in Si as well as (b) normally-on and -off JFETs in SiC.

2.6.1 Purely Vertical vs. Lateral-Vertical JFETs

The JFET manufactured by Infineon Technologies AG shows a vertical device structure like most power semiconductors, and a lateral channel like basic MOSFETs [57, 64] whereas the normally-on JFET offered by SemiSouth Laboratories, Inc. is a purely vertical JFET, i.e. it is — in addition to the vertical device structure — also built with a vertical channel [65, 66].

An inherently high gate-drain (sometimes referred to as "Miller") capacitance comes with the purely vertical design [57] and is disadvantageous in terms of a safe turn-off of the device and concerning the required gate charge when switching as shown in Chapter 4.

The lateral-vertical JFET structure entails an intrinsic pn-junction diode, which can be used for freewheeling purposes during the dead-time interval in a half-bridge setup. The conduction losses in the reverse direction can be reduced by synchronous rectification (the intrinsic SiC body diode shows a high forward voltage drop of around 3 V); still, the reverse recovery charge of the diode can have a significant impact on the switching losses, especially for high current levels or high temperatures, as can be seen from Figure 2.2 [67] and is — up to a junction

temperature of 75 °C — also shown in [56]. Nonetheless, it has been demonstrated that the purely vertical JFET is able to be operated in the reverse direction (despite the lack of an intrinsic diode) during the dead-time interval [65, 68].

2.6.2 Normally-Off vs. Normally-On JFETs

In the 1200 V blocking voltage class, the normally-off JFET is designed by SemiSouth as a purely vertical JFET whereas the normally-on JFET is manufactured both as a purely vertical (SemiSouth, pinch-off voltage of 5 V [61]) and lateral-vertical (Infineon, pinch-off voltage of 16 V [70]) JFET.

Inherent advantages of normally-on compared to normally-off JFETs include a higher channel transconductance for an identical ratio of the gate width to gate length [57]). Infineon's normally-on JFET shows higher $r_{DS,on}$ at 25 °C but a smoother increase with junction temperature which is almost linear. This is surprising in the first instance, as the decrease in charge carrier mobility is typically more than linear. The reason for that can be found in the semiconductor physics: 4H-SiC shows a hexagonal and a cubic lattice site. With an activation energy of 50 meV and 90 meV, respectively, not all dopants are ionized at 25 °C. A higher semiconductor material temperature results in a higher ionization degree among the dopants leading to a higher amount of charge carriers available which in turn partially compensates the exponential decrease of charge carrier mobility [57]. The on-resistance of the normally-off JFET shows a steeper increase in contrast to the normally-on device. Further details on the on-resistance of the normally-off JFET can be found in Section 4.1.

The manufacturing of normally-off JFETs requires accurate process control in terms of channel height and doping density as these characteristics have a huge impact on the saturation current which is anyway typically lower for purely vertical JFETs [57, 64] but could be improved by advanced non-uniform channel doping [71]. Furthermore, channel height and doping density need to be controlled precisely as they influence the threshold voltage which needs to be adjusted in a small voltage range (*cf.* Figure 2.1(b)). This small gate-source voltage range for normally-off JFETs also requires advanced gate drivers which will be investigated in detail in Section 4.1.

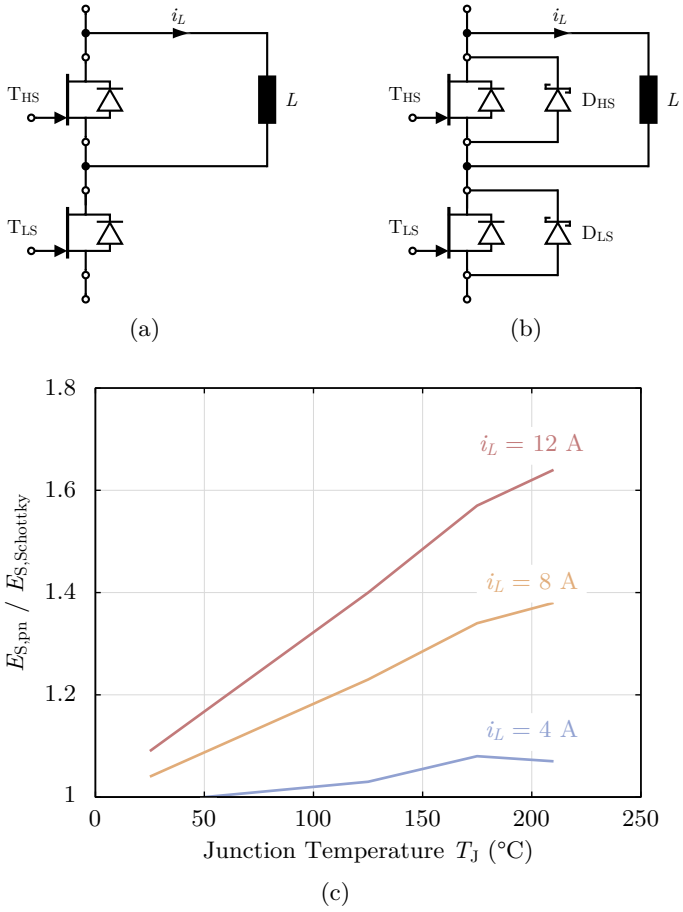


Figure 2.2: Influence of the reverse recovery charge of the intrinsic pn-diode of a 1200 V and 25 A lateral-vertical normally-on SiC JFET on the switching energies: Half-bridge measurement setup with an inductive load and (a) with only JFETs T_{HS} and T_{LS} as well as (b) with JFETs and anti-parallel SiC Schottky diodes (Cree "C2D10120" [69]). The sum of the turn-on and -off energies of T_{LS} is measured in setup (a), denoted as $E_{S,pn}$ and in (b), denoted as $E_{S,Schottky}$. (c) Ratio $E_{S,pn}/E_{S,Schottky}$ as function of junction temperature with load current i_L as parameter. The typical drain current slope during turn-on of T_{LS} is $0.8\,^{A}/_{ns}$ in both setups.

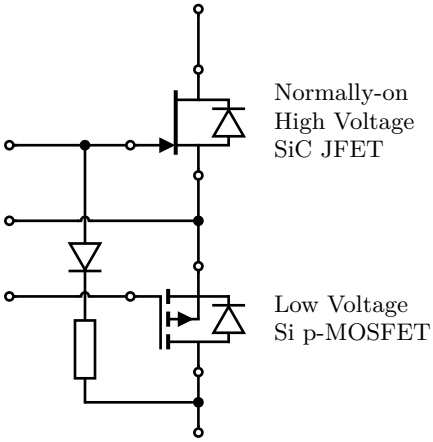


Figure 2.3: Modified cascode configuration for normally-on SiC JFET by Infineon (marketed as "Direct Drive Technology").

A significant advantage of the normally-off JFET during start-up and during a fault for most power electronic converter systems is that it blocks its full rated drain-source blocking voltage with no bias at the gate, provided that no interference caused by other switching components within the circuit causes the gate-source voltage to exceed the low threshold voltage (*cf.* Figure 2.1(b)). To achieve this normally-off behaviour also for the normally-on JFET, the combination (known as "cascode" configuration) of a normally-on SiC JFET with a low-voltage normally-off Si MOSFET that is controlled by a conventional gate driver and controls the gate-source voltage of the JFET with the inverse of its drain-source voltage, has attracted large interest in the literature [72–74].

SemiSouth also suggests the use of a slightly modified cascode for their normally-on JFETs [75] and Infineon considers a commercial device based on a modified cascode structure, denoted as "Direct Drive Technology" and shown in Figure 2.3 [62, 76]. The modifications are such that the 30 V Si p-channel MOSFET still conducts the full load current, but is turned-on continuously during normal operation and only the JFET is switched. During converter start-up or fault, the MOSFET blocks its source-drain voltage and thus ensures a turn-off state of the JFET.

As can be seen from the previous descriptions of the cascode and its derivations, the low-voltage Si MOSFET conducts the full switched current. Hence, from a converter design point of view, this power MOSFET is not regarded as part of the signal electronics but as a component of the power part. Due to the large current transients occurring in the current switched by the JFET, it should be placed very close to the JFET, so for applications with normally-on SiC switches that do not exceed the maximum junction temperature of conventional Si power semiconductors, the cascode approach is very promising.

However, in power electronic converters employing SiC power semiconductors with junction temperatures significantly above 175 °C, only special high temperature Si MOSFETs based on the silicon-on-insulator (SOI) technology can be operated on a junction temperature level close to that of the SiC JFETs. These Si MOSFETs are specified for junction temperatures up to 300 °C but their on-resistance is with 250 mΩ at 225 °C for a TO-254-packaged device (in the best case) significantly larger than that of the high voltage JFET and also of conventional Si MOSFETs in this blocking voltage class [77, 78]. Hence, for the investigated high temperature converter system, a full-SiC solution is preferred and the SemiSouth 1200 V normally-off SiC JFET is chosen.

2.7 Summary

This chapter shows a solution to the question which power semiconductor can be favorably employed in an automotive drive inverter system with a power level of up to a few hundred kilowatts and a junction temperature significantly above 175 °C by comparing the material properties of Si and SiC as well as comparing available bipolar and unipolar power semiconductor switch concepts taking their implications for the overall inverter system into account.

As the maximum dc-link voltage will be below 1 kV and the switching frequency of the inverter is 50 kHz, only unipolar devices are considered despite the high junction temperature. Their losses can be additionally reduced — in contrast to those of bipolar devices — by paralleling more devices which gives further flexibility in designing the cooling system.

The high junction temperature of the investigated converter system makes reliable use of today's SiC MOSFETs questionable. Due to described safety concerns, normally-on JFETs typically require a cascode

configuration for which a low-voltage Si MOSFET is missing at junction temperatures above 175 °C. Thus, a full-SiC solution with normally-off JFETs is chosen for the high temperature and high output frequency inverter conceptualized and investigated in this dissertation.

Chapter 3

Maximum Junction Temperature of SiC Power Semiconductors

3.1 Impact of Junction Temperature

It is shown in Section 1.1.2, that the junction operating temperature limit imposed by the increase of the intrinsic charge carrier density with temperature is significantly higher for SiC power semiconductors than for Si semiconductors. SiC switches have been operated at more than 400 °C [24]. Hence, the choice of the junction temperature is an additional degree of freedom in the design of a power electronic converter employing SiC power semiconductors. Accordingly, it has to be clarified which aspects influence the choice of the junction temperature and how they can be quantified.

First, the semiconductor packaging technology has been adapted to the Si temperature limit of 175 °C and thus needs further advancements in order to be able to deal with a higher absolute junction temperature level and higher temperature swing (*cf.* Section 1.1.2).

Second, the main reason for the need for higher junction temperatures at high ambient temperatures is the aim toward low-volume cooling systems: The higher the junction temperature, the smaller the cooling system for the same amount of dissipated power.

The third aspect is in conflict with the second: In general, the losses of SiC power semiconductors increase with device temperature and thus the converter efficiency decreases. This general trade-off gives rise to an optimization procedure because the power, that can be dissipated by the cooling system, rises linearly with temperature while the losses typically show a steeper increase. That is, for a given converter at a certain temperature, the device current cannot be increased any more even though the junction temperature increases but must be decreased in order to prevent the device from a thermal runaway [79].

This point, where the maximum allowable device current starts to decrease with increasing temperature, can be viewed as the optimum junction temperature with respect to the utilization of the power semiconductor switch because this is the point, where the admissible device current reaches its maximum for a given converter system (*cf.* Figure 3.4). Even more important, this temperature is also the maximum allowed junction temperature as this is the highest junction temperature possible for a thermally stable operation of the power semiconductor. This essentially means, that there is a temperature limit for semiconductor devices with high operating temperature capability, that is not mainly given by material parameters like the intrinsic charge carrier concentration, but by the loss behaviour of the device and the cooling system of the converter. This chapter shows exemplarily which physical quantities of the converter system and the employed switches need to be specified (Section 3.2 and Section 3.3), how this maximum junction temperature can be calculated (Section 3.4) and how it is influenced by different converter parameters such as the switching frequency f_{S}, ambient temperature T_{A} and the overall thermal resistance $R_{\mathrm{th,JA}}$ from the power semiconductor junction to the ambience (Section 3.5).

The flow chart in Figure 3.1 illustrates how the maximum junction temperature $T_{\mathrm{J,max}}$ for SiC power semiconductors is derived.

3.2 Converter Specifications

The input parameters of the algorithm calculating the maximum junction temperature with respect to maximum switch current consist of the following predefined specifications:

- The ambient temperature T_{A} is around 120 °C for power electronic converters placed under the engine hood of hybrid electric vehicle

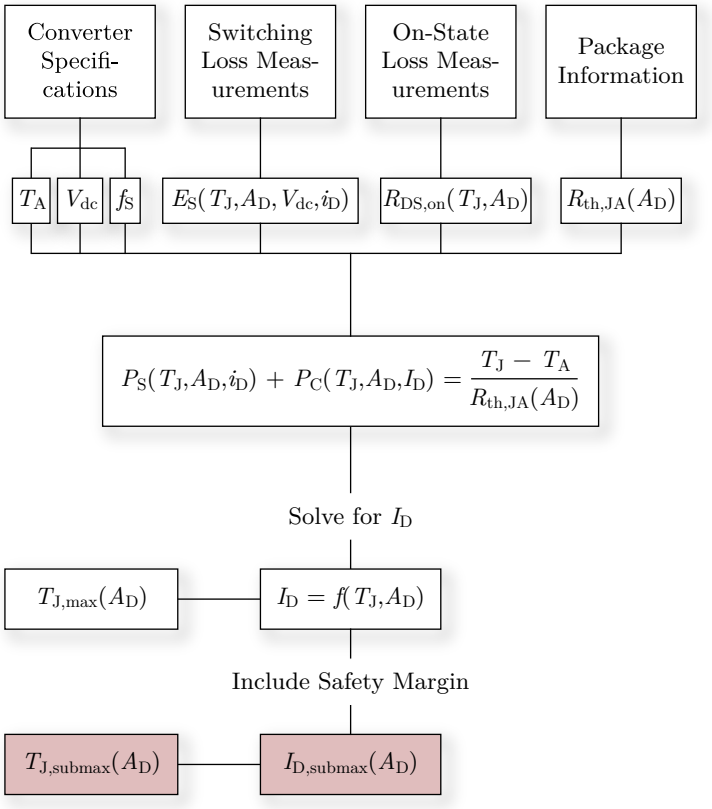


Figure 3.1: Flow chart illustrating the way of determining the maximum junction temperature $T_{J,max}$ of SiC power semiconductors with respect to thermally maximum admissible switch current: Input parameters (ambient temperature T_A, dc-link voltage V_{dc} of the inverter, switching frequency f_S, thermal resistance $R_{th,JA}$ from the power semiconductor junction to the ambience as well as device characteristics on-state resistance $R_{DS,on}$ and switching losses P_S, each as a function of the die area A_D) are used to derive an equation for the thermally stable operation of the converter. This equation is solved for the device current in order to calculate the junction temperature that maximizes the rms value I_D of the device drain current. For a safe operation of the converter, the calculated maximum current is reduced by a safety margin leading to the junction temperature $T_{J,submax}$.

if they are cooled by ambient air or by the cooling circuit of the internal combustion engine (*cf.* Section 1.1.2).

- A high dc-link voltage V_{dc} on the one hand helps to minimize the current for a certain power level so that the ohmic losses — which are proportional to the square of the current rms value — in the switches, supply lines, and the electrical machine can be decreased. On the other hand, a high dc-link voltage adds to the problem of capacitively coupled bearing currents which can reduce the lifetime of the bearings. The choice of V_{dc} also depends on the maximum voltage that can be applied to the electrical machine. Accounting also for potential partial discharge issues in the machine, V_{dc} is chosen to 700 V for this inverter system.

- The switching frequency f_{S} is specified depending on requirements regarding EMI filtering, harmonic losses in the electrical machine, and the desired rotational speed of the electrical machine. Here, f_{S} is chosen to 50 kHz (*cf.* Section 1.1.2).

- The thermal resistance $R_{\mathrm{th,JA}}$ from the power semiconductor junction to the ambience is determined by the particular package configuration. Furthermore, it will not stay constant for different die sizes A_{D} as the heat spreading (for a given semiconductor area) of several small dies is better than that of a single larger die. Hence, a correlation between $R_{\mathrm{th,JA}}$ and the die area A_{D} is required for precise results. This can be obtained by measuring or simulating the package configuration with different die sizes. A curve fitting algorithm using the correlation

$$R_{\mathrm{th,JA}}(A_{\mathrm{D}}) = \frac{a_{R\mathrm{th}}}{A_{\mathrm{D}}^{b_{R\mathrm{th}}}} \tag{3.1}$$

usually gives good fitting results because for very small die sizes, the thermal resistance approaches infinity, and for die sizes close to the maximum (i.e. a size equal to the area of the surface where the dies are soldered onto and that is feeding the heat into the cooling system) $R_{\mathrm{th,JA}}$ reaches its minimum. The coefficients $a_{R\mathrm{th}}$ and $b_{R\mathrm{th}}$ take positive real values. For the exemplary calculations using the SemiSouth 1200 V normally-off SiC JFET, 4 dies are connected in parallel for each switch leading to an estimate of $R_{\mathrm{th,JA}} = 1\,\mathrm{K/W}$.

3.3 Device Characteristics

In addition to these predefined parameters, the device characteristics of the considered power semiconductors need to be identified, as the temperature behavior of the on-resistance and the switching energies determine the maximum junction temperature with respect to a maximum utilization of the semiconductor area.

3.3.1 On-Resistance

Most power semiconductors feature a positive temperature coefficient of their drain-source on-state resistance, i.e. the on-resistance increases with rising device temperature. This can be advantageous as it ensures an even current distribution among dies which are connected in parallel. The temperature dependency of the drain-source on-resistances $R_{\mathrm{DS,on}}$ of the chosen SemiSouth 1200 V normally-off SiC JFET "SJEP120R100" with a die area of 4.5 mm^2 [80] and of a Infineon 1200 V normally-on JFET with a four times larger die area [64] as a comparison is shown in Figure 3.2. Further details on the on-resistance of the normally-off JFET can be found in Section 2.6.2 and Section 4.1.

For the following calculations, analytic expressions of the on-resistances need to be derived with curve fitting algorithms. Second order polynomial functions give better fittings than power functions due to the side effects mentioned in Section 2.6.2 that superimpose the change in charge carrier mobility.

3.3.2 Switching Energies

As for the on-resistance, an analytic expression must be derived for the measured switching energies in order to be able to analytically calculate the maximum junction temperature. When measuring the switching energies, the turn-off and turn-on energies can be summed up and the load conditions should be as close as possible to the later application especially with respect to the parasitic capacitance of the load that needs to be charged and/or discharged for each switching transition.

Figure 3.3 shows the measured switching energies with anti-parallel Schottky diodes (*cf.* Figure 2.2 for the measurement setup) and the curve fitting results. At high junction temperatures, the device current has to be decreased for the normally-off JFET in order not to exceed the saturation current limit of the device (*cf.* Section 2.6.2).

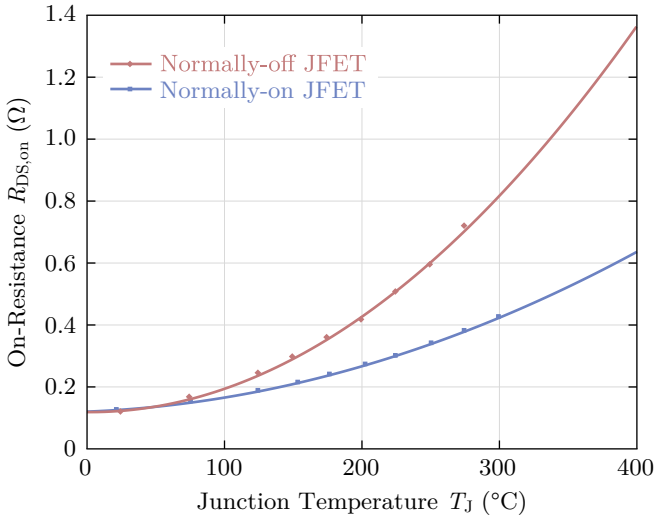


Figure 3.2: Measured and curve fitted temperature dependency of the on-state resistance of the SemiSouth 1200 V normally-off SiC JFET "SJEP120R100" and of the Infineon 1200 V normally-on JFET as a comparison.

The measurement results (*cf.* Figure 3.3) show that as a good approximation, the temperature dependency of the switching energies is independent of the drain current; the dependency of the switching energy on the drain current is similar for all measured temperatures. Hence, the impact of the drain current and the impact of the temperature on the switching energy can be calculated independently and the resulting function describing the switching energy is a product of two independent functions,

$$E_S(I_D, T_J) \sim g_E(I_D) \cdot h_E(T_J). \tag{3.2}$$

The function $g_E(I_D)$ represents the normalized dependency on the drain current and can be derived using the measured switching energies at a constant temperature, e.g. at 25 °C for the normally-off JFET as it is the only temperature where measured values up to 10 A are available. (In Equation (3.2) and Equation (3.3), the drain current is denoted by I_D as it is not time dependent within these measurements of a single switch in a half-bridge setup, in contrast to Figure 3.1 and

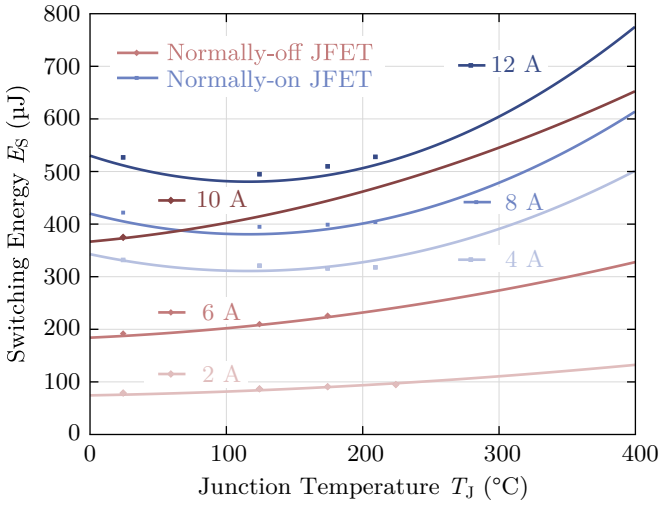


Figure 3.3: Measured and curve fitted switching energies (turn-on and turn-off) for different temperatures and drain currents of the 1200 V normally-off SiC JFETs with an antiparallel SiC diode (Cree "C2D10120") [69] and an inductive load. The normally-on JFET has got a four times larger die area than the normally-off JFET. The switched voltage is 700 V for both devices.

Equation (5.7) where the switching losses of the inverter with time dependent currents i_D are considered.) The function $h_E(T_J)$ forms the normalized temperature behavior which can be determined using the measured switching energies at constant drain current level. Both functions, h_E and g_E, are second-order-polynomials of the form

$$g_E(I_D) = a_E + b_E \cdot I_D + c_E \cdot I_D^2 \tag{3.3}$$

and

$$h_E(T_J) = d_E + e_E \cdot T_J + f_E \cdot T_J^2, \tag{3.4}$$

where a_E and d_E, b_E and e_E, c_E and f_E denote the constant zeroth, first and second order coefficients for $g_E(I_D)$ and $h_E(T_J)$, respectively.

The switching energies depicted in Figure 3.3 are measured with a single JFET, i.e. not multiple devices in parallel. If larger currents than measured are conducted through several dies connected in parallel, an ideal current distribution can be assumed for a symmetric module

structure due to the above mentioned positive temperature coefficient of the on-resistance of the JFETs. Accordingly, for i paralleled switches, $i \in \mathbf{N}$, the switching losses can be calculated as for one switch but considering only $1/i$ of the overall current. These switching losses are then multiplied by i to obtain the switching losses for all dies. For the following calculations, four devices (four normally-off and four normally-on JFETs, respectively) are assumed to be connected in parallel, which is represented with $i = 4$.

3.4 Calculation of the Maximum Junction Temperature

Having derived all input parameters according to Figure 3.1, the calculation of the maximum junction temperature can now be started by equalizing the power losses and the power, that can be dissipated by the package. The losses in the off-state due to leakage currents (less than 100 µA per die at 700 V and 250 °C for both devices) and the losses arising at the gate (less than 1 W per device) are neglected here. Hence, the power losses consist only of the conduction and switching losses, which leads to an implicit equation for the drain current of the switch,

$$I_{\mathrm{D}}^2 R_{\mathrm{DS,on}}\left(T_{\mathrm{J}}\right) + f_{\mathrm{S}} \cdot E_{\mathrm{S}}\left(T_{\mathrm{J}}, i_{\mathrm{D}}\right) = \frac{T_{\mathrm{J}} - T_{\mathrm{A}}}{R_{\mathrm{th,JA}}}, \tag{3.5}$$

in the thermal equilibrium where I_{D} denotes the rms value of the drain current corresponding to a sinusoidal output phase current of the inverter (*cf.* Equation (5.1)) and i_{D} the instantaneous value of the drain current which is needed to calculate the switching losses.

Using Equation (3.2), the junction temperature, where the drain current reaches its maximum, can be calculated based on an equation for I_{D} derived from Equation (3.5) first,

$$\begin{aligned} I_{\mathrm{D}} = & \frac{1}{2(R_{\mathrm{DS,on}}(T_{\mathrm{J}}) - c_E f_{\mathrm{S}} h_E(T_{\mathrm{J}}))} \cdot \Bigg(- b_E f_S h_E(T_{\mathrm{J}}) \\ & + \sqrt{b_E^2 f_{\mathrm{S}}^2 h_E^2 - 4(R_{\mathrm{DS,on}} - c_E f_{\mathrm{S}} h_E)(a_E f_{\mathrm{S}} h_E - \left(\frac{T_{\mathrm{J}} - T_{\mathrm{A}}}{R_{\mathrm{th,JA}}}\right)} \Bigg). \end{aligned} \tag{3.6}$$

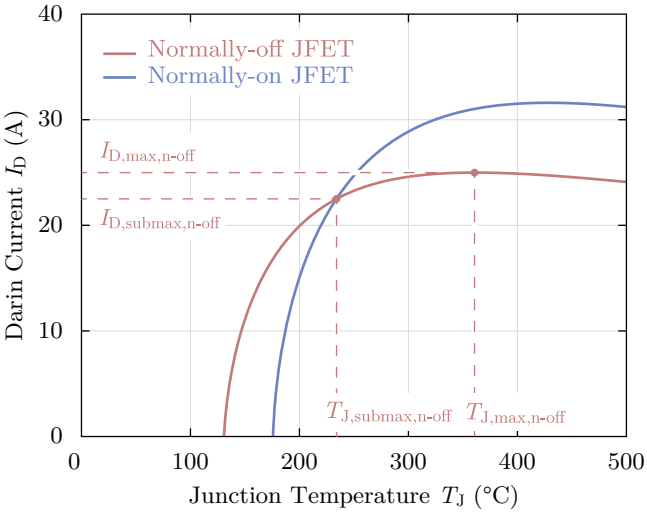


Figure 3.4: Maximum admissible rms drain current values of the SemiSouth 1200 V "SJEP120R100" normally-off [80] and Infineon 1200 V normally-on [64] SiC JFET (each with four single devices in parallel) in dependency of the junction temperature for the values of Section 3.2 and Section 3.3. Characteristic values of the junction temperature are shown for the example of the normally-off JFET. The differences in maximum drain current and maximum junction temperature between the two devices are mainly due to the differences in the temperature behavior of the on-resistance. For very low drain currents, the junction temperature does not exactly equal the ambient temperature due to the (at low currents high) portion of switching losses, which are not close to zero for drain currents close to zero, especially for the normally-on JFET with a four times larger die area for a similar value of the on-resistance (*cf.* Figure 3.2) compared to the normally-off device.

Figure 3.4 shows a plot of Equation (3.6) for both the normally-on and normally-off JFET.

It can clearly be seen from Figure 3.4, that there is a junction temperature $T_{J,max}$ which allows a maximum drain current for each device. This maximum $I_{D,max}$ can be calculated by differentiating Equation (3.6) with respect to T_J and setting the derivative to zero. For the conditions of Section 3.2 and Section 3.3, the maximum junction

temperature for the normally-off JFET is

$$T_{\mathrm{J,max,n\text{-}off}} = 361\,^{\circ}\mathrm{C}, \tag{3.7}$$

assuming that the extrapolation of the device characteristics is valid in this temperature range.

If the junction temperature stays below this value, the JFET is not fully utilized. This is disadvantageous with respect to the material cost of the converter as a larger die area is used than needed but is advantageous in terms of the power module reliability and the achievable efficiency as at a higher temperature the conduction and switching losses will be higher.

If the junction temperature rises above its allowed maximum, the semiconductor switch is operated with far lower efficiency and lower utilization due to lower current that can be conducted. If the current is not decreased quickly enough at temperatures above $T_{\mathrm{J,max}}$, a positive feedback mechanism could be triggered leading to a thermal runaway which finally results in a thermal destruction of the device.

This consideration regarding the operational stability of the power electronics converter can be further explained using Figure 3.5: The solid straight black line in Figure 3.5 is the characteristic of the cooling system. It cannot dissipate any power, if the junction temperature T_{J} equals the ambient temperature T_{A}. With increasing temperature difference between the power semiconductor junction and the ambience, the power that can be dissipated increases linearly with $1/R_{\mathrm{th,JA}}$. (Actually, a constant $R_{\mathrm{th,JA}}$ is only an approximation as $R_{\mathrm{th,JA}}$ is not completely temperature independent due to temperature dependent material properties, e.g., the thermal conductivity or the density of the cooling fluid.)

The solid red lines represent the losses in one of the six inverter switches (in this example each made of four paralleled 1200 V normally-off SiC JFETs, in contrast to the inverter design shown in Chapter 5 where two dies are paralleled in one single package for each of the six inverter switches) for the specifications mentioned in terms of V_{dc} and f_{S} and for two different drain current levels, $I_{\mathrm{D,max,n\text{-}off}}$ and $I_{\mathrm{D,submax,n\text{-}off}}$. The intersections between the cooling system characteristic and the temperature dependence of the loss characteristic for a given drain current define steady-state operating points. The first intersection at $T_{\mathrm{J,submax,n\text{-}off}} = 230\,^{\circ}\mathrm{C}$ for $I_{\mathrm{D,submax,n\text{-}off}}$ is the only thermally stable operating point for this current level.

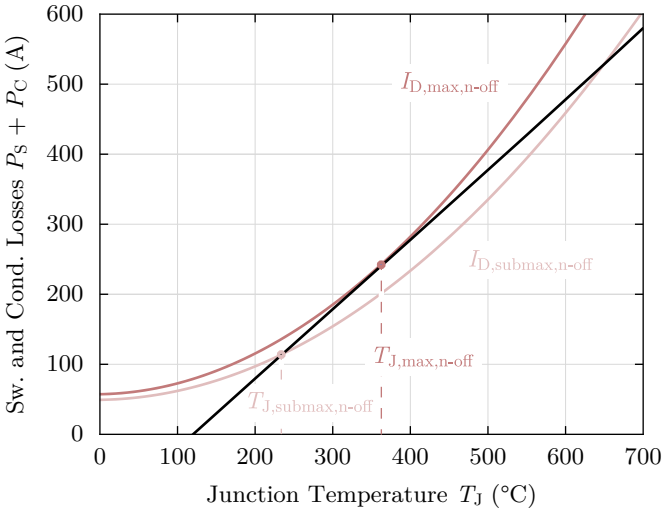


Figure 3.5: Illustration of the "thermal runaway" phenomenon setting a junction temperature limit to the operation of SiC power semiconductor devices: The actual junction temperature depends on the drain current in steady state operation and can be found as intersection between the cooling system characteristic (straight black line) and the loss characteristics of a semiconductor switch for different drain currents (red lines). All thermally stable operating points are located below $T_{J,max,n\text{-}off}$ on the characteristic of the cooling system.

For disturbances like, e.g., a short deviation in the current level or ambient temperature, the operating point will always return to this intersection: If the junction temperature decreases due to such a short disturbance, the power loss is higher than the power that can be dissipated by the cooling system. This difference in power flow will heat up the power semiconductor junction. If the junction temperature is higher than $T_{J,submax,n\text{-}off}$ due to a disturbance, the power loss is lower than the heat transferred by the cooling system, and hence, the junction cools down back to $T_{J,submax,n\text{-}off}$.

With the same reasoning, it can be shown, that the second intersection of the cooling system characteristic and the curve for $I_{D,submax,n\text{-}off}$ at $T_J = 640\,°C$ is inherently unstable. A small disturbance causing a lower junction temperature will lead to a continuously decreasing tem-

perature until $T_{\mathrm{J,submax,n\text{-}off}}$ is reached, a disturbance leading to a higher junction temperature will heat up the semiconductor until it is thermally destroyed ("thermal runaway") because the loss curve and the cooling system curve do not have another intersection. (After thermal breakdown, the switch conducts zero drain current and has no more power loss corresponding to an intersection with the cooling system characteristic and an "operating" point at $T_{\mathrm{J}} = T_{\mathrm{A}} = 120\,^{\circ}\mathrm{C}$.)

The dark red curve in Figure 3.5 for $I_{\mathrm{D,max,n\text{-}off}}$ corresponds to the maximum rms drain current that the device is able to conduct in steady state operation without thermal runaway: For higher currents, there would be no intersection with the cooling system characteristic. Accordingly, a thermal runaway could occur. Therefore, the drain current level must always remain below this level.

This leads directly to the conclusion, that all stable operating points lie between $T_{\mathrm{J}} = T_{\mathrm{A}}$ and $T_{\mathrm{J}} = T_{\mathrm{J,max,n\text{-}off}}$ and hence $T_{\mathrm{J,max,n\text{-}off}}$ constitutes the operating junction temperature limit. A reduction of only 10% from the maximum drain current $I_{\mathrm{D,max,n\text{-}off}}$ to $I_{\mathrm{D,submax,n\text{-}off}}$ furthermore brings a large reduction in junction temperature, which significantly improves the reliability and on the efficiency. (With Si, the considerations are exactly the same. However, for typical converter designs, the 175 °C material temperature limit is below the temperature limit for thermal runaway.)

With this safety margin for the drain current of 10%, the junction temperature is in this case

$$T_{\mathrm{J,submax,n\text{-}off}} = 234\,^{\circ}\mathrm{C}, \tag{3.8}$$

which is with 127 K significantly below the maximum junction temperature $T_{\mathrm{J,max,n\text{-}off}}$ because I_{D} shows a very flat maximum (*cf.* Figure 3.4). This flat maximum becomes particularly interesting when the trade-off between current utilization of the die and reliability is considered. By reducing the junction temperature by 127 °C the reliability rises by orders of magnitude while the maximum current is decreased by only 10%.

For the normally-on JFET, the effect of the slower increase in on-resistance with junction temperature can be seen: The maximum junction temperature

$$T_{\mathrm{J,max,n\text{-}on}} = 428\,^{\circ}\mathrm{C}, \tag{3.9}$$

is reached significantly later, and thus the drain current at the junction temperature

$$T_{\mathrm{J,submax,n\text{-}on}} = 293\,^{\circ}\mathrm{C}, \tag{3.10}$$

can be larger with 28.4 A.

Due to the larger die area of the normally-on JFET, its switching losses are higher compared to the normally-off JFET (*cf.* Figure 3.3). Figure 3.4 shows, that the (capacitive) switching losses account for a high portion of the overall losses at small drain currents, leading to a temperature difference between the ambience and junction temperature also for zero drain current.

3.5 Sensitivity of the Maximum Junction Temperature

Equation (3.6) shows, that the maximum admissible drain current and thus the maximum junction temperature depend on

- the absolute value and the temperature behavior of the on-resistance and the switching energies of the power semiconductor,
- the dc-link voltage,
- the die size,
- the switching frequency,
- the ambient temperature, and
- the thermal resistance from the junction to the ambience.

Most of these parameters become fixed at a certain point in the design process of a power electronic converter. The resulting value is the consequence of a trade-off consideration between different impacts on the converter properties of a particular parameter. This section presents the impact of three parameters on the maximum junction temperature and the maximum admissible device current for the example of the normally-off JFET.

Figure 3.6 and Figure 3.7 show, that the switching frequency f_{S} exhibits the lowest impact on $T_{\mathrm{J,max}}$ and $I_{\mathrm{D,max}}$. A change in f_{S} changes the portion of switching and conduction losses in the overall losses. As

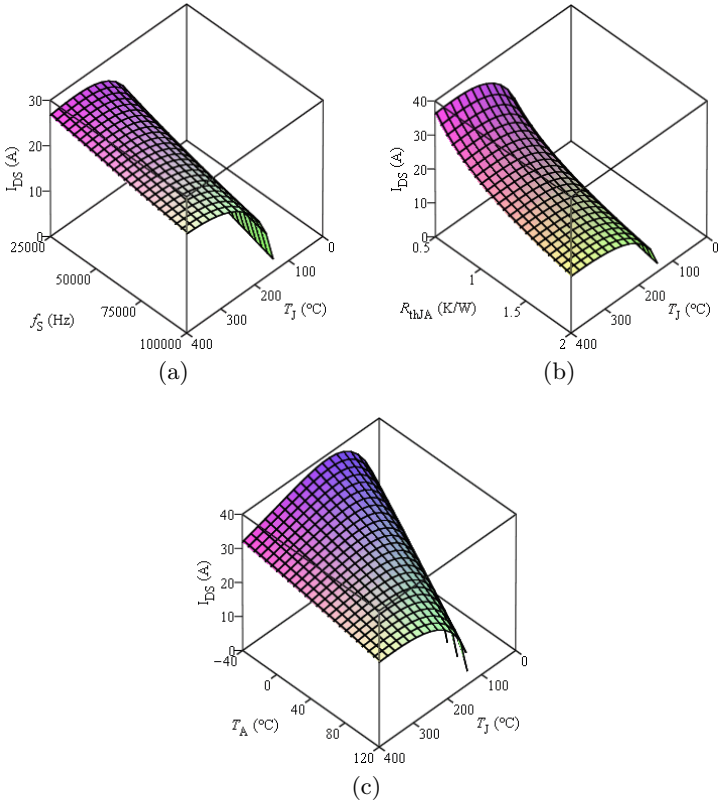


Figure 3.6: Admissible drain current as a function of the junction temperature as well as (a) ambient temperature, (b) switching frequency, and (c) thermal resistance for four 1200 V normally-off SiC JFET connected in parallel.

the switching losses increase slightly less with temperature compared to the conduction losses (*cf.* Figure 3.2 and Figure 3.3), $T_{J,max}$ increases slightly with an increasing portion of switching losses. Due to the overall higher losses at higher f_S, $I_{D,max}$ decreases with rising f_S.

With the switching losses considered in Equation (3.5), the thermal resistance $R_{th,JA}$ from the semiconductor junction to the ambience does not cancel out, if Equation (3.6) is differentiated and set to zero. There-

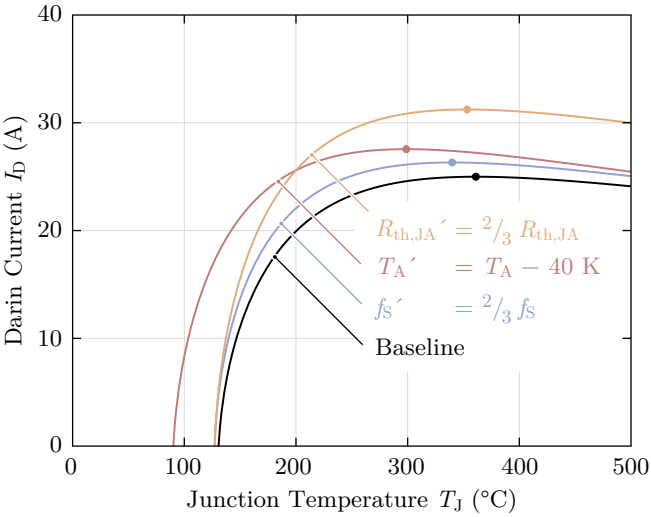


Figure 3.7: Drain current as a function of junction temperature with variations in the ambient temperature T_A, the switching frequency f_S, and the thermal resistance $R_{th,JA}$ for four paralleled dies of the 1200 V normally-off SiC JFET. The respective values for the maximum drain current and corresponding junction temperature is indicated by a dot.

fore, an increased $R_{th,JA}$ shifts $T_{J,max}$ slightly towards higher values and drastically decreases the maximum device current.

The ambient temperature T_A has by far the largest influence on the maximum junction temperature $T_{J,max}$. The lower T_A, the lower $T_{J,max}$ and the higher $I_{D,max}$ because at lower junction temperatures, the on-resistance and switching losses are lower. Hence, more current can be conducted at constant losses. The correlation between T_A and $T_{J,max}$ is linear with a slope of approximately unity, i.e. every degree of reduction in T_A reduces $T_{J,max}$ likewise.

Precise values of the change in admissible maximum device current and maximum junction temperature due to the change in the parameters can be derived from Figure 3.7 by comparing the respective curves with the baseline curve for the exemplary parameter changes given.

3.6 Summary

The high junction temperature capability of SiC offers a further degree of freedom for the power electronic converter design. With the loss characteristic and die size of the employed power semiconductors, the dc-link voltage, the switching frequency, the ambient temperature, and the thermal resistance from the junction to the ambience, the junction temperature allowing maximum device current can be calculated. A 10% decrease in the maximum current leads to a large decrease in junction temperature, increasing both efficiency and reliability. For the SemiSouth 1200 V normally-off SiC JFET and the given boundary conditions, this temperature which allows the device to handle 90% of the maximum current is calculated to 234 °C for an ambient temperature level of 120 °C.

The sensitivity of the maximum junction temperature is also investigated: A lower maximum junction temperature can be achieved by decreasing the ambient temperature. 1 K lower ambient temperature means 1 K lower maximum junction temperature as a good approximation. The most effective way to increase the admissible device current, is to reduce the thermal resistance of the package and cooling system. Cutting the thermal resistance in half corresponds to an approximately 50% higher device current.

Chapter 4

AC-Coupled Gate Driver for Normally-Off SiC JFETs

4.1 Analysis of Requirements for the Gate Driver

The 1200 V 40 A normally-off SiC JFET manufactured by SemiSouth Laboratories, Inc. is chosen for the investigated converter system (*cf.* Section 2.6). This device makes special demands on the gate driver circuit compared to other unipolar SiC or Si devices. To fully exploit the potential of normally-off SiC JFETs, conventional gate driver circuits for unipolar switches need to be adapted for use with these switches. In the literature, several concepts for adapted gate drivers have been presented so far. Some still have certain limitations, e.g., with respect to switching frequencies and possible duty cycles, and some of them are very complex with the need for several integrated circuits, own dc-dc converters or additional cooling due to high losses [81–88].

In this chapter, a novel gate driver topology is presented that overcomes the current limitations while still having a low circuit complexity using one gate driver IC and passive components only. First, the special gate driver requirements of the normally-off JFET are explained and described in detail in order to reveal the differences to driving con-

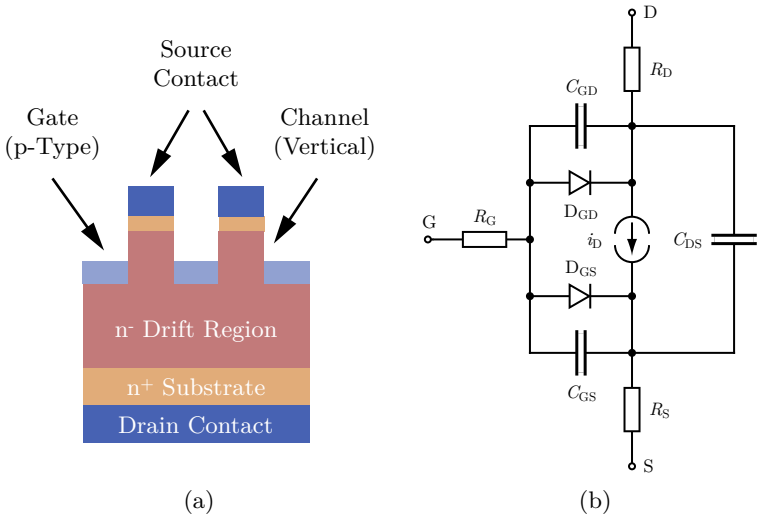


Figure 4.1: 1200 V normally-off SiC JFET: (a) cross-section and (b) equivalent circuit diagram. Notable is with respect to the gate driver design in particular the pn-junction diode at the gate as well as the purely vertical structure of the device leading to an inherently high gate-drain capacitance (*cf.* Section 4.1.1 and Section 4.1.2).

ventional power semiconductors, followed by a short summary of the state-of-the-art concepts (Section 4.2) before the proposed novel gate driver concept is presented in detail (Section 4.3). In Chapter 8 (Section 8.1), the theoretical considerations are validated in a half-bridge test setup showing experimental waveforms of the switching transients under different conditions.

Figure 4.1 shows the cross-section and equivalent circuit diagram of the 1200 V normally-off SiC JFET. Compared to other power semiconductors such as MOSFETs and IGBTs, the structure of the investigated normally-off JFET involves special requirements for its gate driver.

4.1.1 On-State

From the cross-section in Figure 4.1(a) the major difference between a *junction* FET and a *metal-oxide-semiconductor* FET becomes obvious:

The gate is not insulated from the channel by an oxide, but forms a pn-junction with the source (diode D_{GS} in the JFET model in Figure 4.1(b)) and the drain (D_{GD}), respectively. The resulting depletion layer in the channel makes sure, that the device can block its nominal drain-source voltage, for the normally-off JFET without any reverse biasing of the pn-junction (and thus further extending the depletion region), i.e. with a gate-source voltage $V_{GS} = 0$.

Forward biasing the gate-source pn-junction reduces the width of the space charge region. The gate-source threshold voltage $V_{GS,th}$ of the device is typically around 1 V, decreasing with temperature at the rate of approx. $1.5\,^{mV}/_{K}$ to less than 0.7 V at 250 °C. If V_{GS} exceeds the built-in potential of the pn-junction $V_{bi} \approx 3\,V$ at 25 °C, a significant amount of holes is injected into the channel. Figure 4.2 shows the temperature dependent forward characteristic of the gate-source diode. The consequence for the gate driver is the limitation, that during the on-state not more than 3 V should be applied to the JFET's gate with respect to the source (or to the drain, e.g. during synchronous rectification) in order to avoid large currents and thus unnecessarily high power flowing into the gate.

The correlation between the drain-source on-resistance $R_{DS,on}$ and the applied gate bias to D_{GS} (in this case in terms of the current, which can be translated into a respective voltage using the diode characteristic in Figure 4.2) is shown in Figure 4.3 for different drain currents I_D and junction temperatures T_J. It can be seen, that $R_{DS,on}$ depends on T_J *and* on I_D. The latter dependency increases with temperature and the drain current saturation limit can be observed in Figure 4.3 for junction temperatures of 175 °C and higher: While $R_{DS,on}$ increases at 175 °C for $I_D = 16\,A$ by 14% compared to $I_D = 7\,A$, a drain current level of 24 A at a junction temperature of 175 °C (not shown in Figure 4.3 for the sake of clarity) leads to a more than 50% increase in $R_{DS,on}$, even for gate currents of 600 mA and more. For lower gate currents, the on-resistance is even higher.

The resulting requirement for the gate driver can be extracted from Figure 4.4(a). It shows the required gate current for drain currents from 4 A to 30 A and junction temperatures from 25 °C to 225 °C, if a minimum $R_{DS,on}$ is desired. This gate current varies from 100 mA for $I_D = 4\,A$ at 25 °C to 400 mA for $I_D = 16\,A$ at 175 °C.

As can be seen from Figure 4.3, the $R_{DS,on}$ curve is very flat for a broad range of gate currents. Figure 4.4(b) shows the required gate

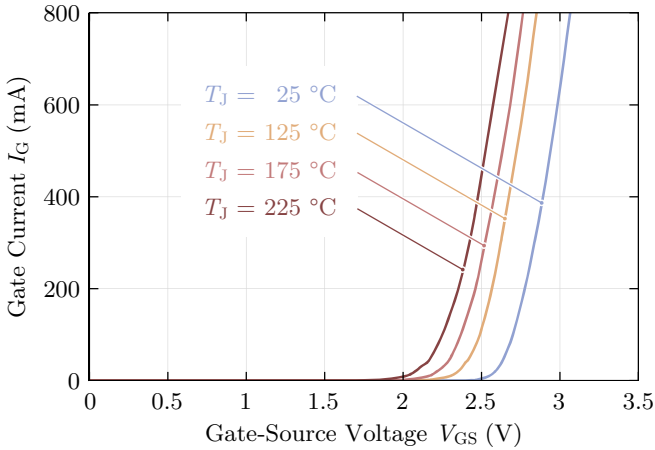


Figure 4.2: Measured gate-source dc characteristic of the 1200 V 40 A normally-off SiC JFET for different junction temperatures T_J. During the on-state of the normally-off SiC JFET, the gate-source voltage V_{GS} should not exceed 3 V in order to avoid large currents flowing into the gate.

current for drain currents from 4 A to 30 A and junction temperatures from 25 °C to 225 °C, if a 10% increase in the on-resistance is allowed. This leads to a significant reduction in gate current, much larger than only a factor of 1.1: I_G varies from 50 mA for $I_D = 4$ A at 25 °C to 200 mA for $I_D = 16$ A at 175 °C.

Here, the drain current limit is chosen to $I_D = 10$ A at $T_J = 225$ °C (*cf.* Figure 4.3) and the upper limit of the gate current is chosen for minimum on-resistance at this operating point to 300 mA (*cf.* Figure 4.4(a)) corresponding to a gate-source voltage of 2.42 V at $T_J = 225$ °C (*cf.* Figure 4.2).

This choice allows the design of a gate driver in Section 4.3 that has challenging requirements meeting the needs of the normally-off SiC JFET at high temperature operation while being significantly different to those for MOSFET drivers. Additionally, choosing these values, a design is introduced that can be easily adapted for other applications, i.e. for lower or higher gate currents, for other on-resistances or the parallelization of several chips.

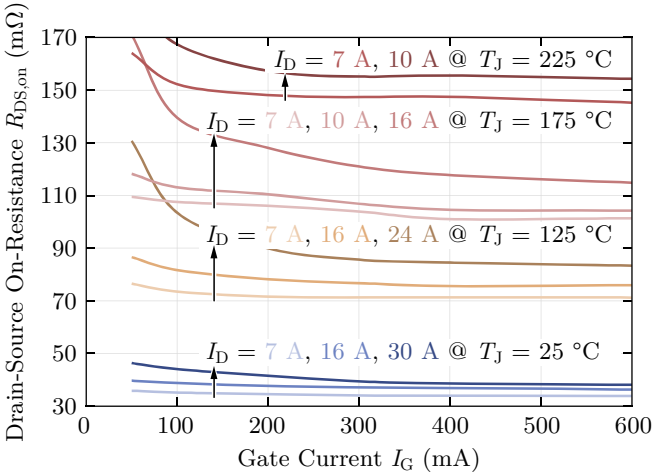
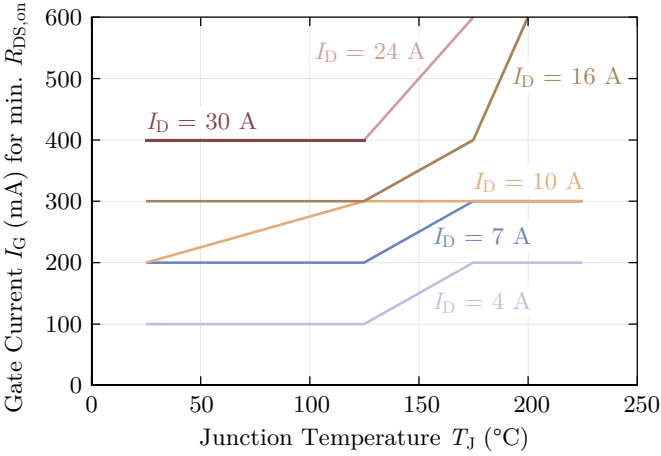


Figure 4.3: Measured drain-source on-resistance $R_{DS,on}$ of the 1200 V 40 A normally-off SiC JFET for different drain currents I_D and different junction temperatures T_J against the gate current I_G. It can be clearly seen, that a significant amount of gate current is necessary to operate the device with its minimum on-resistance. With increasing junction temperature, the difference in $R_{DS,on}$ for different I_G increases. At high junction temperatures, a high drain current leads to very high values of $R_{DS,on}$ and hence, $R_{DS,on}$ at $T_J = 225\,°C$ is only shown up to $I_D = 10\,A$.

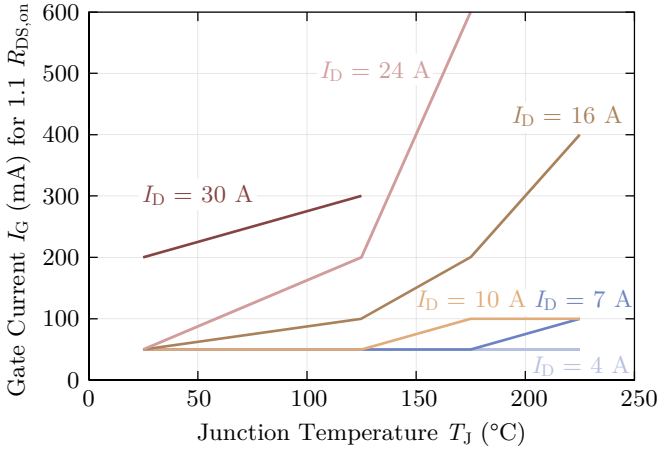
4.1.2 Off-State

The so called "Miller" effect results in special demands on the gate driver during the off-state: After turn-off of the JFET's channel, i.e. after discharging the gate-source capacitance C_{GS} from approx. 3 V to a value below the threshold voltage and thus turning the JFET completely off, it can happen in half-bridge configurations, as given for the investigated inverter system or also depicted in Figure 8.1(a), that the gate-drain capacitance C_{GD} is charged to the actual blocking voltage V_{dc} significantly later than the turn-off of the switch.

This time delay between the turn-off of the high-side JFET T_{HS} and the voltage rise across it occurs typically in the following situation: The inductor current i_L in Figure 8.1(a) is freewheeling in T_{HS}, before the channel of T_{HS} is turned off. The current i_L will continue to freewheel



(a)



(b)

Figure 4.4: Gate current I_G required to operate the JFET for different levels of drain current I_D and junction temperature T_J with (a) lowest possible drain-source on-resistance $R_{DS,on}$ and (b) a value for $R_{DS,on}$ that is 10% higher than the lowest possible value. Here, a limit of $I_D = 10\,A$ at 225 °C is assumed leading to (a) $I_G = 300\,mA$ for lowest possible $R_{DS,on}$ and (b) $I_G = 100\,mA$, if a 10% increase in $R_{DS,on}$ is accepted (due to the flat shape of the characteristic of $R_{DS,on}$ in Figure 4.3), reducing the gate power requirement to one third.

in D_{HS} after turn-off of T_{HS}, until the low-side JFET T_{LS} is turned on. Once T_{LS} is turned on, the source of T_{HS} (and thus also its gate, if the negative gate bias is negligible compared to V_{dc}) will be clamped by T_{LS} to the negative supply voltage rail, while the drain of T_{HS} remains at V_{dc}, resulting in quick charging of C_{GD} to approximately V_{dc}. Depending on the gate driver design, a certain portion of the capacitive current charging C_{GD} flows via C_{GS} or via the gate driver circuit to the source of the JFET.

Three factors increase the risk that this capacitive current leads to a voltage rise across C_{GS} above the threshold voltage resulting in an accidental turn-on of T_{HS} which would short circuit the dc-link voltage:

As can be seen from the cross-section in Figure 4.1(a), the investigated normally-off JFET has a vertical channel in contrast to typical SiC normally-on JFETs [57] as well as (Si and SiC) MOSFETs [89]. This purely vertical structure leads first to a comparably low gate-source capacitance C_{GS} and second to an inherently high gate-drain (Miller) capacitance C_{GD}. This fact is illustrated by Figure 4.5, which compares C_{iss} and C_{rss} of the 1200 V 40 A normally-off SiC JFET with the C_{iss} and C_{rss} characteristics of a typical SiC MOSFET with similar voltage and current rating. C_{rss} is C_{GD} in the JFET model, and is significantly higher for the JFET compared to the MOSFET (by a factor of 3 to 10 depending on the drain-source voltage V_{DS}). C_{iss} as the sum of C_{GS} and C_{GD} is lower for the JFET (by a factor of approximately 1.5), i.e. the JFET's C_{GS} is much smaller than that of the MOSFET, as expected from the device cross-section. Third: Even though, the direct comparison of C_{GS} and C_{GD} of the JFET reveals still a ratio of $C_{GS}/C_{GD} \approx 10$, the charge of C_{GD} can increase the gate-source voltage of the JFET as the voltage across the charged gate-drain capacitance is typically three orders of magnitude higher than the threshold voltage of the JFET which goes down to 0.7 V at 250 °C.

Hence, the gate driver circuit has to provide a low impedance path for the capacitive current from the gate connection to the source of the normally-off JFET to turn it reliably off. As this path will have parasitic resistances and inductances, a negative gate bias with respect to the source during the off-state is thus also needed. (This negative gate bias is not necessary during start-up of the converter and hence makes an important difference to the use of normally-on devices.)

Figure 4.6 shows the measured characteristic of the gate-source diode in reverse direction. Bearing in mind that the leakage currents

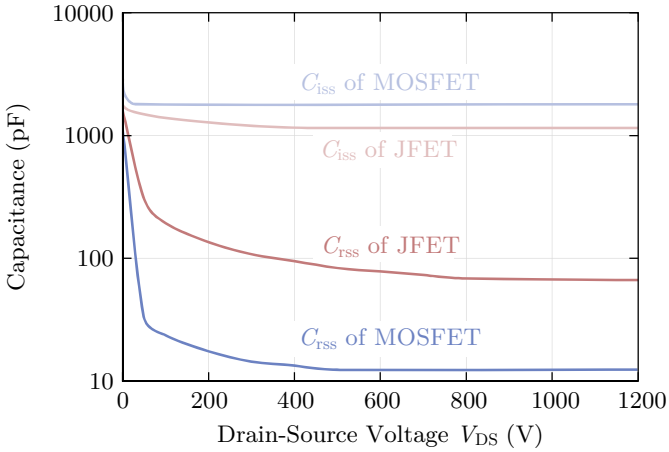


Figure 4.5: Comparison of the measured input and reverse transfer capacitance (C_{iss} and C_{rss}, respectively) of a 1200 V 40 A normally-off SiC JFET and a typical SiC MOSFET (type: Cree, Inc. "CMF20120D" [90]) with similar voltage and current rating showing the high gate-drain and low gate-source capacitance of the JFET.

occur in the off-state of the device and that the device may remain in the off-state for a longer time than only a few microseconds if for example the overall converter is in standby, the losses in the diode should be limited to a low level. Hence, the off-state bias at the gate-source terminal is chosen to $V_{GS} = -15\,V$ leading to a leakage current of less than 1 mA.

4.1.3 Switching

During the switching transients, the gate driver must deliver the charge required by the parasitic input capacitance C_{iss}, which is the sum of the gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} of the JFET model in Figure 4.1(b). To turn the device on, C_{GS} must be charged to approximately 3 V (*cf.* Section 4.1.1) and C_{GD} (charged to approximately V_{DS} in the off-state of the device) must be discharged by feeding current from the gate terminal to the drain. To turn the device off, the opposite action is necessary: The gate driver must sink current in order to discharge C_{GS} and charge C_{GD} to approximately V_{DS}.

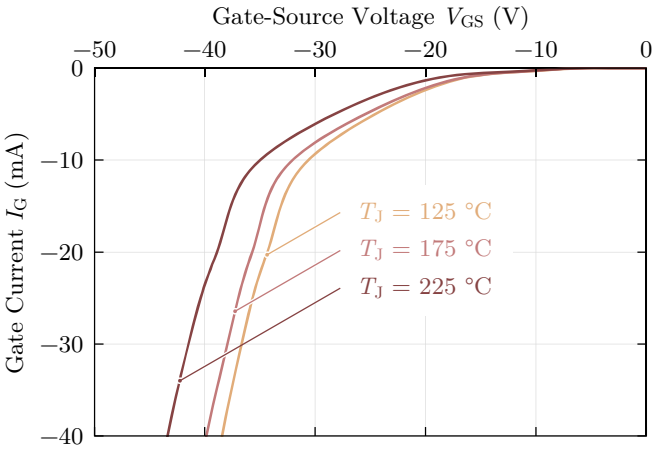


Figure 4.6: Measured reverse gate-source dc characteristic of the 1200 V 40 A normally-off SiC JFET for different junction temperatures T_J. A bias exceeding -15 V should not be applied to the gate in order to limit the losses during the off-state.

However, the finite conductivity of the bond wires and of the p- and n-doped SiC paths to the respective junction within the device leads to resistive portions R_D, R_S, and R_G of the impedance between the device terminals, as depicted in the JFET model in Figure 4.1(b). The exact value depends on the operating point: The value during the on-state of the device can be extracted from the gate-source characteristic in Figure 4.2 as a differential resistance. For the switching behavior, the resistivity for voltages between the threshold voltage and the negative bias during the off-state and frequencies up to the MHz range (corresponding to the harmonics contained in the step function of the gate signal at turn-on or -off) are significant. The precise measurement of the resistance under this circumstances using an impedance analyzer with bias is possible only for frequencies above 1 MHz due to the small series capacitance in the JFET model leading to a load angle of close to 90° for lower frequencies and reveals a resistivity of approximately 3 Ω from the gate to the source with the drain shorted to the source to achieve a defined drain potential.

Due to this *RC* low-pass characteristic at the gate, the achievable switching speed of the JFET is limited. In order to be able to

reach the desired voltage levels during turn-on ($V_{GS} \geq V_{GS,th}$) and -off ($V_{GS} \leq V_{GS,th}$) fast, the gate driver should apply voltages significantly higher than these steady state values for a short period of time at each switching state transition so that C_{GS} is rapidly charged to the desired voltage level with a higher current. SemiSouth allows transient gate-source voltages for turn-on of up to +15 V for a duration of less than 200 ns [60], for turn-off a voltage of −15 V equals the voltage level during the off-state in this gate driver design (*cf.* Section 4.1.2).

For applications with limitations regarding the switching speed due to requirements set by EMI, common mode currents or insulation issues, a further gate driver requirement concerning the switching transients is the ability to switch with a pre-set, less than the maximum achievable speed.

4.1.4 Temperature Behavior

Some of the requirements for the gate driver set by the switch characteristics investigated so far are temperature dependent, especially with respect to the gate current. Ideally, the gate driver behaves over the operating temperature range of the power semiconductor switch such that it adapts to the changing requirements of the switch and does not induce any additional temperature variations itself, i.e. shows only a negligible temperature dependence of its internal resistance. In this case, it is especially important with respect to the power loss of the gate driver, that the gate current is always just as high as needed. I.e., if due to lower junction temperatures a gate current lower than the above determined 300 mA is needed, the gate driver should supply less current.

To illustrate this requirement, the following example can be considered: If a converter design is such, that the nominal rms-value of the drain current is 10 A and the nominal junction temperature is 225 °C, the junction temperature is likely to be well below the nominal value of 225 °C at part load (i.e. at drain currents of less than 10 A), lowering also the gate current needed according to Figure 4.4(a). It is assumed, that a nominal drain current of 10 A leads to a nominal junction temperature of 225 °C and a part load drain current of 7 A leads to a junction temperature of only 125 °C, mainly due to the decreasing conduction losses. This means for the gate current supplied by the gate driver, that

300 mA are needed at 225 °C ($I_D = 10$ A) and only 200 mA at 125 °C ($I_D = 7$ A) for minimum on-resistance (*cf.* Figure 4.4(a)).

4.1.5 Standard Requirements

All of the above mentioned requirements are present for the investigated gate driver due to the properties of the normally-off SiC JFET. A novel, ubiquitous gate driver has to fulfill also standard requirements that apply to any gate driver used in power electronic converters, i.e.

- low power consumption,
- qualification for switching frequencies in the investigated voltage range up to around 100 kHz,
- applicability for arbitrary duty cycles from 0% to 100%,
- robustness against steep voltage changes,
- performance invariance against spread for factory standard models (of the gate driver IC itself as well as the switch), and
- low (circuit) complexity and cost.

4.2 Existing Gate Drivers for Normally-Off JFETs

Against the background of the summarized gate driver requirements for the normally-off SiC JFET, existing solutions are very shortly reviewed.

4.2.1 Existing Two-Stage Gate Drivers

To meet the different requirements for transient turn-on and -off on the one hand and the steady on-state on the other hand, two-stage gate drivers have been introduced [81–85]: One stage supplies a short pulse with a high voltage (around 15 V) for turn-on and a second stage delivers the dc gate current for the on-state (at a gate-source voltage $V_{GS} \approx 3$ V) from the same supply voltage rail via a resistor (causing high losses in that resistor due to a high voltage drop of approximately 12 V across the resistor and high gate current flowing through the resistor). The second stage is either realized by a second output of a dual gate driver

IC or by low-voltage transistors connected to the supply voltage of the gate driver. The control of the second stage is realized by an additional logic IC.

To limit the power loss in the resistor during on-state, a dc-dc converter can be deployed that steps down the high voltage needed for turn-on to a lower value (e.g. around 6 V) and thus decreases the voltage drop across the resistor. Still, the power loss can become significant for this concept at duty cycles close to 100% and switching frequencies higher than 25 kHz [82]. This frequency limitation can be overcome with the newest implementation of this gate driver concept which, however, still shows a high circuit complexity, a high part count and a large PCB footprint [83].

4.2.2 Existing AC-Coupled Gate Drivers

To reduce the high complexity of the two-stage gate drivers, ac-coupled gate drivers have been published [84–88] where the supply voltage is fed through a capacitor to the gate during the turn-on and -off and through a resistor (in parallel to the capacitor) during the on-state. The limitations of this concept include frequency and duty cycle limitations as the coupling capacitor needs to discharge during turn-off via a high impedance path [84], a high power loss in the dc current resistor and the need for an external gate-source capacitor that can sink the current arising from the high gate-drain capacitance of the JFET [84, 88].

4.3 Proposed Novel AC-Coupled Gate Driver

The proposed gate driver for the normally-off SiC JFET is shown in Figure 4.7. Based on the following description of the basic operation principle, detailed analytical expressions will be given for the dimensioning of the particular circuit elements and voltage levels.

4.3.1 Basic Operation Principle

A standard gate driver IC is supplied with a differential voltage $V_{CC} - V_{EE}$ with the midpoint (0 V) connected to the source of the JFET, with V_{CC} close to the desired gate-source voltage $V_{GS} \approx 3\,V$ and V_{EE} in the

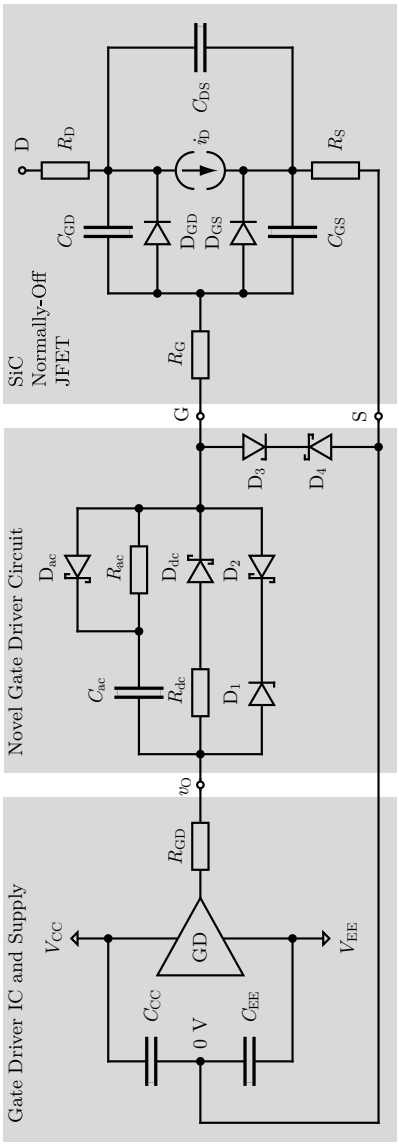


Figure 4.7: Proposed novel ac-coupled gate driver for ultra fast switching of normally-off SiC JFETs. During the on-state of the JFET, a dc current flows through R_{dc} and D_{dc} causing very low losses in these devices due to the low voltage drop. During turn-off and the off-state, $V_{Z,D3}$ is applied to the gate for a high noise immunity making this gate driver together with D_1 and D_2 resistant against the Miller effect. During turn-on the sum of V_{CC} and V_{Cac} is applied to the gate for fast turn-on.

range of $-27\,\mathrm{V}$ (*cf.* Section 4.3.3 and Section 4.3.6 for derivation of the exact values).

During the on-state of the switch, V_{CC} is applied to the gate through the output resistance R_{GD} of the gate driver IC, a resistor R_{dc} and a Schottky diode $\mathrm{D_{dc}}$ in order to provide the required dc gate current to the JFET (*cf.* Figure 4.4(a)). A value around $1\,\Omega$ results for the sum of the resistors R_{GD} and R_{dc} (*cf.* Section 4.3.3), compared to more than $5\,\Omega$ for the two-stage solution [83] and around $40\,\Omega$ for the existing ac-coupled drivers [86] mentioned in Section 4.2. As the gate current depends on the desired on-resistance, it is the same for the different gate driver topologies; accordingly, the ohmic losses in the resistor scale directly with the resistor value and are thus at least a factor of 5 lower for the novel gate driver.

During the off-state of the device, the output v_{O} of the gate driver IC is at V_{EE}. The Zener voltage $V_{\mathrm{Z,D3}}$ of the Zener diode $\mathrm{D_3}$ determines the sharing of the voltage V_{EE} between the gate-source input of the JFET and the capacitor C_{ac}. $V_{\mathrm{Z,D3}} \approx 15\,\mathrm{V}$ fulfills the requirement of negative bias at the gate during the off-state (*cf.* Section 4.1.2) and $\mathrm{D_{dc}}$ makes sure, that no current flows through R_{dc} during the off-state.

To make sure, that the Miller effect is sufficiently attenuated and thus a large portion of the current charging C_{GD} during the off-state of the device can flow to the source of the JFET without flowing through C_{GS} (*cf.* Section 4.1.2), the proposed gate driver has an anti-series connection of a Zener diode $\mathrm{D_1}$ and a Schottky diode $\mathrm{D_2}$. As the negative gate bias during the off-state is limited by leakage currents, the inductance from the gate to the source through the $\mathrm{D_1}$-$\mathrm{D_2}$ path has to be so low, that the gate potential does not increase up to the threshold voltage of the JFET for nanoseconds.

During turn-on of the JFET, the voltage $V_{C\mathrm{ac}} = -V_{\mathrm{EE}} - V_{\mathrm{Z,D3}} \approx 12\,\mathrm{V}$ across C_{ac} is added to V_{CC}, making sure that a positive voltage around $15\,\mathrm{V}$ is applied to the gate terminal for fast charging of the JFET's input capacitance while discharging C_{ac}. To dampen oscillations or to slow down the switching speed, a resistor R_{ac} can be connected in series to C_{ac}.

During turn-off, the required negative bias can be applied to the gate by V_{EE} (limited to $-15\,\mathrm{V}$ by $\mathrm{D_3}$), and the diode $\mathrm{D_{ac}}$ provides with C_{ac} a low impedance path for fast turn-off of the channel.

The state of charge of C_{ac} does not impose any duty cycle or frequency limitations in contrast to existing ac-coupled gate drivers as

mentioned in Section 4.2.2: If the on-time of the JFET is low, C_{ac} is still fully discharged as it is connected to D_{GS} through a low impedance path. D_4, D_3, and D_{ac} form a low impedance path that allows charging of C_{ac} also for very short off-times of the JFET (*cf.* Section 8.1).

Having explained the basic functionality of the proposed gate driver and its elements, the design of appropriate components, and the derivation of their physical values is conducted in the following subsections.

4.3.2 Choice of Gate Driver IC

When choosing the gate driver IC for the proposed gate driver circuit, the output resistance R_{GD} is of special importance: During the on-state, the gate driver IC has to deliver a certain amount of current between 200 mA and 300 mA. During the switching transients, the IC has to deliver or sink current in order to charge or discharge C_{GS} and C_{GD} via a resistive path.

To limit the self-heating of the IC during the on-state of the JFET as well as during the large current peaks when switching the JFET and to minimize the RC time constant during the switching transients, R_{GD} should ideally be zero. However, the output stage of real gate driver ICs consists typically of p- and n-channel MOSFETs with nonzero on-resistance around 1 Ω. The maximum allowed value of R_{GD} can be calculated for a certain design by determining the maximum allowed temperature rise of the gate driver IC due to the described losses depending on the ambient temperature, the maximum IC junction temperature, and the thermal resistance from the IC junction to its ambience.

The maximum output current that must be delivered or sunk by the IC is the second design criterion. During the on-state, a maximum of 300 mA is required here. During the off-state, only leakage currents in the single-digit mA-range occur, caused by the leakage currents of the JFET (*cf.* Section 4.1.2) and the diodes D_{dc}, D_1 as well as D_3. During switching, the capacitances C_{GS} and C_{GD} must be charged or discharged via a path with the total resistance R_{tot} consisting (during the switching transients) of R_{GD} (around 1 Ω), R_{ac} (assumed to 0 Ω to make sure that the chosen gate driver IC is also applicable for designs where fastest switching is needed) and the internal resistances of the JFET (accounting for approximately 3 Ω, *cf.* Section 4.1.3). Hence, the

maximum output current I_O can be calculated as

$$I_O = \frac{V_{CC} - V_{EE}}{R_{tot}} \approx \frac{30\,V}{4\,\Omega} = 7.5\,A, \tag{4.1}$$

if R_{ac} is chosen to zero for fast switching in this design and for determining the maximum output current that can occur in this topology. Typically, the output resistance R_{GD} of the gate driver IC decreases with increasing output current rating and hence, it can pay off to choose a gate driver IC with a higher output current rating than calculated in Equation (4.1).

The differential gate driver IC supply voltage of 30 V is not an uncommon value for gate drivers, but it is close to the recommended upper limit of many commercially available ICs. One advantage of a supply voltage level close to the upper limit is the fact that the output resistance of the IC is typically smallest at this operating point. Here, the driver IC IXYS "IXDE514SIA" in a SO-8 package is chosen: Its peak output current is 14 A, the maximum output resistance for the high and low state is 1.25 Ω up to an IC junction temperature of 150 °C of the IC and the maximum supply voltage is 35 V [91].

4.3.3 Determination of V_{CC}, R_{dc}, D_{dc}

The components R_{dc} and D_{dc} as well as V_{CC} determine together with R_{GD} and D_{GS} the gate current supplied to the JFET during the on-state and thus the on-resistance of the JFET. The gate driver must deliver 300 mA at $T_J = 225\,°C$ and 200 mA at $T_J = 125\,°C$ for the design at hand according to Section 4.1.1 and Section 4.1.4, respectively.

For the choice of D_{dc} a low forward voltage drop at a current level close to the on-state gate current is important to minimize the JFET on-state losses, which is why a Schottky diode has been selected.

However, the Schottky diode shows a leakage current, which causes losses when the diode is blocking in the off-state of the JFET. Hence, the leakage current should ideally be zero but is typically higher for Schottky diodes than for pn-diodes. Still, Schottky diodes are available that have a leakage current $I_L \leq 3$ mA for the maximum reverse voltage $V_{r,Ddc}$ occurring in this gate driver circuit. $V_{r,Ddc}$ is given by

$$V_{r,Ddc} = -V_{EE} - V_{F,D4}(I_L) - V_{Z,D3} - I_L(R_{dc} + R_{GD}). \tag{4.2}$$

The forward voltage drop $V_{\mathrm{F,D4}}(I_{\mathrm{L}})$ of diode $\mathrm{D_4}$ as well as the voltage drop across the resistors R_{dc} and R_{GD} are negligible due to the low leakage current I_{L} and hence Equation (4.2) can be simplified and calculated to

$$V_{\mathrm{r,Ddc}} \approx -V_{\mathrm{EE}} - V_{\mathrm{Z,D3}} = 12\,\mathrm{V}. \tag{4.3}$$

using the numerical results of Section 4.3.6 and Section 4.3.5.

An oversized 60 V 1 A Schottky diode (type: International Rectifier "10BQ060") is chosen because of the low forward voltage drop of 0.3 V for currents around 300 mA and the low leakage current of 3 mA for voltages around $V_{\mathrm{r,Ddc}}$ [92].

If the gate driver circuit acted during the on-state of the switch as an ideal voltage source connected to the gate-source terminal of the JFET, it would supply significantly less current to its load $\mathrm{D_{GS}}$ at lower junction temperatures than at higher temperatures (*cf.* Figure 4.2). If it behaved as an ideal current source, it would supply the same current for all temperature levels, i.e. the gate driver would not fulfill the requirement of Section 4.1.4 to supply a gate current that is only as high as needed for the respective temperature level.

Using the $\mathrm{D_{GS}}$ characteristic (*cf.* Figure 4.2, the values of the internal resistances R_{G} and R_{S} for dc current are already included as R_{G}, R_{S}, and $\mathrm{D_{GS}}$ can hardly be measured separately under dc conditions) and considering $\mathrm{D_{dc}}$ as part of the load the gate driver has to supply, V_{CC} as the no load voltage of a real voltage source and the sum of R_{GD} and R_{dc} as the internal resistance of this voltage source, the required values for V_{CC} and R_{dc} can be obtained graphically from Figure 4.8: The two load lines, each one consisting of the Schottky diode $\mathrm{D_{dc}}$ and the impedance of the JFET from the gate to the source terminal, are shown for a diode junction temperature of 125 °C to facilitate gate driver operation even at high ambient temperatures, while one load line is based on a junction temperature of the JFET of 125 °C and the other one on a temperature of 225 °C.

V_{CC} and the sum of R_{GD} and R_{dc} can now be derived by drawing the gate driver supply line from the 300 mA point of the load line for a JFET junction temperature of 225 °C to the 200 mA point of the load line for a JFET junction temperature of 125 °C. The voltage axis intersection of the supply characteristic reveals $V_{\mathrm{CC}} = 3.1\,\mathrm{V}$ and the negative inverse of the slope gives 0.9 Ω for the sum of R_{GD} and R_{dc}. As R_{GD} is already in this range ($R_{\mathrm{GD}} = 1.25\,\Omega$ of the chosen gate driver is its maximum value, *cf.* Section 4.3.2), R_{dc} can be chosen to zero here. Figure 4.8

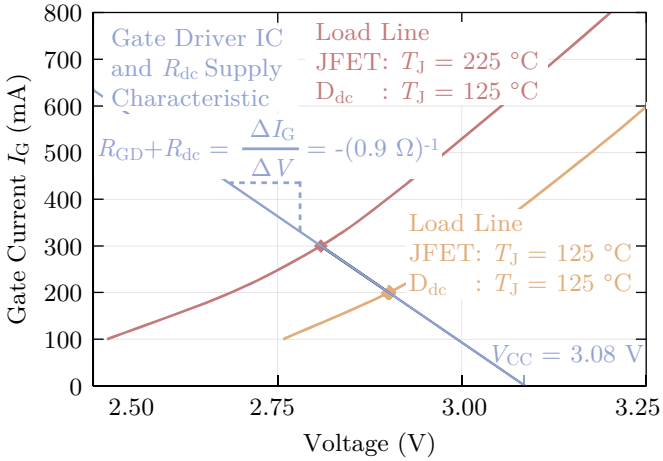


Figure 4.8: Characteristic of series connection of gate-source diode D_{GS} and Schottky diode D_{dc} at junction temperatures of 125 °C and 225 °C for the JFET as well as 125 °C for diode D_{dc}. The voltage on the abscissa is the sum of the gate-source voltage V_{GS} of the JFET and the forward voltage V_F of D_{dc}. From these characteristics, the required gate driver supply characteristic (straight line) in terms of V_{CC} and R_{dc} can be derived.

allows also to directly analyze the impact of a slight change in V_{CC}, R_{GD} or R_{dc} on the gate current and thus together with Figure 4.3 on the on-resistance of the JFET.

Besides this intuitive graphical approach, analytical expressions can also be derived using formulae corresponding to the graphical approach: With the gate-source voltage V_{GS} of the JFET at the nominal junction temperature $T_{J,n}$ (in this design 225 °C) and nominal gate current $I_{G,n}$ (300 mA) as well as at the part load junction temperature $T_{J,p}$ (125 °C) and part load gate current $I_{G,p}$ (200 mA) and the forward voltage V_F of diode D_{dc} at gate driver temperature level T_{GD}, R_{dc} and V_{CC} can be calculated as

$$R_{dc} = \frac{V_{GS}(I_{G,n}, T_{J,n}) + V_F(I_{G,n}, T_{GD})}{I_{G,p} - I_{G,n}} - \frac{V_{GS}(I_{G,p}, T_{J,p}) + V_F(I_{G,p}, T_{GD})}{I_{G,p} - I_{G,n}} - R_{GD}, \tag{4.4}$$

$$V_{\mathrm{CC}} = V_{\mathrm{GS}}(I_{\mathrm{G,n}}, T_{\mathrm{J,n}}) + V_{\mathrm{F}}(I_{\mathrm{G,n}}, T_{\mathrm{GD}}) + I_{\mathrm{G,n}} \cdot (R_{\mathrm{GD}} + R_{\mathrm{dc}}). \quad (4.5)$$

The values for V_{GS} and for V_{F} for different temperature and current levels can be extracted from Figure 4.2 and [92], respectively, or the sum of both can be read directly from Figure 4.8. Equation (4.4) and Equation (4.5) then reveal the same values as obtained graphically, $R_{\mathrm{dc}} = 0$ and $V_{\mathrm{CC}} = 3.1\,\mathrm{V}$.

4.3.4 Selection of $\mathrm{D_{ac}}$, $\mathrm{D_2}$, $\mathrm{D_4}$

To minimize the losses in the particular diode is the most important design criterion for the diodes $\mathrm{D_{ac}}$, $\mathrm{D_2}$, and $\mathrm{D_4}$. Even though the diodes conduct current (apart from leakage currents) only during turn-off and not during the on- or off-state of the JFET (in contrast to $\mathrm{D_{dc}}$, *cf.* Section 4.3.3), a low forward voltage drop is desired, which is why again Schottky diodes are chosen. The blocking voltages of the three diodes are smaller than V_{CC} and hence the leakage currents are negligible for typical Schottky diodes; 40 V International Rectifier "10MQ040NPBF" diodes in are selected [93].

4.3.5 Selection of $\mathrm{D_3}$

The Zener diode $\mathrm{D_3}$ determines the negative bias at the gate during the turn-off of the JFET. It is limited to $-15\,\mathrm{V}$ due to leakage currents of $\mathrm{D_{GS}}$. The Zener voltage $V_{\mathrm{Z,D3}}$ should be chosen to this voltage level, so that the immunity against the Miller Effect is as high as possible and a high voltage can be applied to the unavoidable inductances in the $\mathrm{D_1}$-$\mathrm{D_2}$ path in order to feed the Miller charge through this path (and not through C_{GS}). $\mathrm{D_4}$ inhibits operation of $\mathrm{D_3}$ in the forward direction.

4.3.6 Determination of V_{EE}, $\mathrm{D_1}$, R_{ac}

V_{EE} sets together with $V_{\mathrm{Z,D3}}$ the voltage $V_{C\mathrm{ac}}$ that C_{ac} is charged to during the off-state for typical off-times during normal operation of power electronic converters. (For off-times longer than several tens of microseconds the voltage distribution of the diodes $\mathrm{D_1}$ and $\mathrm{D_3}$ will be determined by their voltage-over-current characteristic and no longer simply by V_{EE} and $V_{\mathrm{Z,D3}}$, leading to a matching of their leakage currents.) During turn-on $V_{C\mathrm{ac}}$ is applied to the gate in addition to V_{CC}. Hence, to calculate V_{EE}, first $V_{C\mathrm{ac}}$ is calculated using the desired ac

voltage $V_{\mathrm{GS,ac}} = 15\,\mathrm{V}$ during turn-on that can be applied to the gate (*cf.* Section 4.1.3),

$$V_{C\mathrm{ac}} = V_{\mathrm{GS,ac}} - V_{\mathrm{CC}} = 12\,\mathrm{V}. \tag{4.6}$$

(During turn-off, the gate-source voltage is limited by the Zener voltage of diode D_3.) Now, the negative supply voltage level can be determined to

$$V_{\mathrm{EE}} = -V_{C\mathrm{ac}} - V_{\mathrm{Z,D3}} = -27\,\mathrm{V}. \tag{4.7}$$

$V_{\mathrm{Z,D1}}$ should not be chosen to a significantly higher value than $-V_{\mathrm{EE}} - V_{\mathrm{Z,D3}} = 12\,\mathrm{V}$, otherwise a larger portion of the capacitive current charging C_{GD} during the off-state (*cf.* Section 4.1.2) would flow through C_{GS} to the source and not via D_1 and D_2 leading to a larger increase in the gate-source voltage. Hence, the Zener voltage $V_{\mathrm{Z,D1}}$ is chosen to 12.5 V and thus only slightly above $-V_{\mathrm{EE}} - V_{\mathrm{Z,D3}} = 12\,\mathrm{V}$ in order to make sure, that no continuous current will flow through diodes D_1 to D_4 during the off-state.

The differential resistance in reverse direction of diode D_1 should be as small as possible to guarantee a voltage drop across D_1 close to $V_{\mathrm{Z,D1}}$ if the gate-drain capacitance is charged.

If the switching speed has to be limited, R_{ac} can be increased starting from its current value of $0\,\Omega$.

4.3.7 Dimensioning of C_{ac}

To guarantee a fast switching, the parasitic capacitances C_{GS} and C_{GD} of the JFET must be charged by the capacitor C_{ac}. If a freewheeling diode connected in antiparallel to the JFET is already conducting the load current before the JFET is switched, the difference in the voltage across C_{GD} before and after the switching action and thus the charge required for the voltage change across C_{GD} is low and C_{ac} must deliver the gate-source charge only. If the gate-drain potential difference increases rapidly when the devices switches, the charge in C_{ac} must equal the sum of the gate-source and gate-drain charge. This means for turn-on of the JFET, that the capacitive current needed to charge C_{GS} and discharge C_{GD} should be able to flow through C_{ac}, which makes the voltage $V_{C\mathrm{ac}}$ decrease from its value during the off-state (12 V) to the voltage drop across R_{dc} (0 V in this design) and D_{dc} (approximately 0.3 V). Dur-

ing turn-off, the capacitive current discharging C_{GS} and charging C_{GD} should also be able to flow through C_{ac}, increasing its voltage from the voltage drop across R_{dc} and D_{dc} to 12 V.

For a switched voltage of 600 V, the gate charge of the JFET is $Q_G = 60\,\text{nC}$ [60]. The required capacitance and thus the lower limit for C_{ac} can be calculated as

$$C_{ac} = \frac{Q_G}{V_{Cac}} \approx 6\,\text{nF}. \tag{4.8}$$

The upper limit of the charge stored in C_{ac} is given by efficiency considerations, as the energy stored in C_{ac} is dissipated in the resistances when switching. A capacitance value larger than the lower limit calculated in Equation (4.8) helps slightly to achieve a faster turn-on as the voltage across C_{ac} decreases less fast in this case. Furthermore, a larger value for C_{ac} improves the gate driver's robustness against the Miller effect, as it leads to a smaller increase in the gate-source voltage when C_{GD} is charged. Here, C_{ac} is chosen to 6 nF.

4.4 Summary

Appropriate gate drivers for the already commercialized 1200 V 40 A normally-off SiC JFET with very promising performance in terms of device losses have been of large interest and subject to many recent publications. These publications mention certain limitations of the proposed and partly very complex gate drivers with respect to noise immunity, possible duty cycles and switching frequencies as well as high losses leading to significant self-heating.

To fully exploit the potential of the normally-off SiC JFET and to make sure that it can also be used in power electronic converters with high switching frequencies, a novel gate driver topology is presented and dimensioned in this chapter, after the exact demands are identified and analyzed in detail. The proposed gate driver meets the requirements of the normally-off SiC JFET while using only one standard gate driver IC, one capacitor, two resistors, and six diodes: It delivers the required charge very fast during turn-on of the switch by means of a pre-charged capacitor. During turn-off, a low impedance path quickly removes the charge from the gate and negative biasing during the off-state allows the gate-drain capacitance to be charged via the low impedance path

without the risk of turning the JFET on unintentionally. During on-state, the gate driver delivers up to 300 mA at a gate-source voltage of only 2.4 V without significant self-heating to make sure that the JFET is operated with lowest possible on-resistance.

In Chapter 8, Section 8.1, measurement results are presented verifying that this gate driver offers fast turn-on and -off of the switch while still having a high noise immunity and allowing operation at all duty cycles and at high switching frequencies which is especially important for the investigated inverter system with a switching frequency of 50 kHz.

Chapter 5

High Temperature Converter Design Methodology

5.1 120 °C-Ambient-Air-Cooled, 50 kHz Compact Automotive Inverter System

This chapter shows the design process of a compact automotive traction inverter, that is directly cooled with ambient air at a maximum temperature level of 120 °C. According to Chapter 3, a junction temperature of 250 °C ensures a close to maximum utilization of the current handling capability of the employed power semiconductors, the SemiSouth 1200 V 40 A normally-off SiC JFETs with an on-resistance of 50 mΩ at 25 °C. Infineon 1200 V 15 A SiC Schottky diodes [94] are connected antiparallel to the switches. To keep the output current and thus the chip size related costs low, the dc-link voltage is chosen to 700 V, which is a similar voltage level compared to actual HEVs [16]. The switching frequency is chosen to 50 kHz (*cf.* Section 1.1.2). Table 5.1 gives on overview over the inverter system specifications.

Besides the SiC power semiconductors, a dc-link capacitor, a current, voltage, and temperature measurement, control electronics, an auxiliary power supply, and heat sinks with fans to cool the power semiconductors are the main critical components needed for the real-

Table 5.1: Overview over SiC inverter system specifications

High Temperature / Power Density / Output Freq. Inverter		
Maximum Inverter Output Power	10	kW
Maximum Ambient Temperature	120	°C
Max. Power Semiconductor Junction Temp. (for first prototype with discrete devices)	175	°C
Max. Power Semiconductor Junction Temp. (for design process)	250	°C
DC-Link Voltage	700	V
SiC Power Semiconductors Voltage Class (normally-off JFETs & Schottky diodes)	1200	V
Switching Frequency	50	kHz

ization of the converter system. The main challenge in designing the inverter system for an ambient temperature of 120 °C and a maximum junction temperature of 250 °C, is to make sure that the individual devices are operated within their specified temperature ranges by proper placing and, if necessary, active cooling of the components.

After a short overview over the allowed operating temperatures of the different components in Section 5.2, the inverter system is designed in Section 5.3 and possible geometrical arrangements of the power semiconductors, the heat sinks, the fans, the signal electronics, and the dc-link capacitors are analyzed with respect to power density and modularity. It is shown that in any case an active cooling of the control electronics is needed. The optimization of the design of the Peltier cooling [95–97] with respect to volume and power consumption is shown in Section 5.4 using a detailed thermal equivalent circuit diagram. In Chapter 8 (Section 8.4), a testing environment and experimental results are presented using a demonstrator system with discrete power semiconductor devices and thus with a junction temperature limit of 175 °C.

5.2 Operating Temperature Ranges of Inverter Components

To consider different inverter designs and possible options for placing the components, it has to be analyzed first, for which temperature levels the components needed are available. Figure 5.1 gives an overview over the operating temperature ranges.

Often, there are devices for specialized industries such as military, downhole or aerospace applications available that have partially significantly extended operating temperature ranges at the expense of reduced performance or functionality.

The high temperature power FET technology by Honeywell can exemplify this: The n-channel FET is fabricated using a SOI process in order to reduce the leakage currents at high temperatures. The device is rated up to 225 °C, i.e. the device shows a significantly higher upper temperature limit than conventional Si power semiconductors [78]. Disadvantageous are the higher component costs and the derated performance of the device, e.g. in terms of the chip area specific on-resistance, which is with 43 $m\Omega cm^2$ in the same range as the specific on-resistance of conventional Si power semiconductors, that have an order of magnitude higher blocking voltage (55 V compared to 650 V) [98].

Against the background of industrial practicability, therefore, no special components with derated performance will be chosen for this inverter system.

5.3 Inverter Design with Active Electronics Cooling

The first prototype of the inverter system is designed for and built with discrete power semiconductor devices with an upper junction temperature limit of 175 °C in Section 5.3.1. Therefore, the system will be operated either at the nominal ambient temperature of 120 °C with reduced output power or at the nominal power level of 10 kW at reduced ambient temperature. The power level is chosen to 10 kW as this allows laboratory testing on the one hand and scaling the power up to larger values using the same generic concepts on the other hand.

The arrangement of the main components and the thermal design of the encapsulation of the control and gate drive electronics is conducted

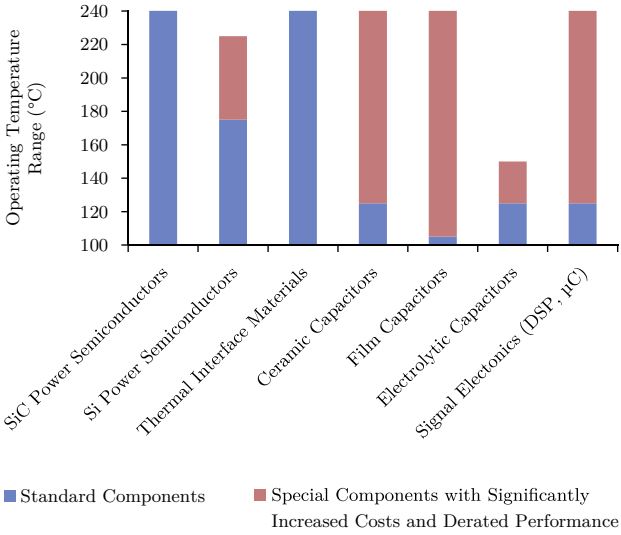


Figure 5.1: Overview over operating temperature ranges of the main components of the investigated inverter system. The significantly derated performance of special components refers to the much higher on-resistance of silicon-on-insulator-type Si power semiconductors, the much lower energy density of high temperature capacitors or the limited signal processing capability of high temperature DSPs.

for power semiconductors with junction temperatures up to 250 °C, as will be shown in Section 5.3.3. This makes it possible to replace the discrete power semiconductors with a customized power semiconductor module having a junction temperature limit of 250 °C while maintaining the concepts developed in this dissertation.

5.3.1 Power Semiconductors

The instantaneous value of the output phase current i_{ph} is either carried by the high-side or the low-side switch (instantaneous current i_{D}, *cf.* Figure 5.2). During steady state converter operation, the rms current values of the high- and low-side switches are the same for symmetric modulation schemes. Apart from currents charging the parasitic capacitances of the switches during the switching transients, the switches do

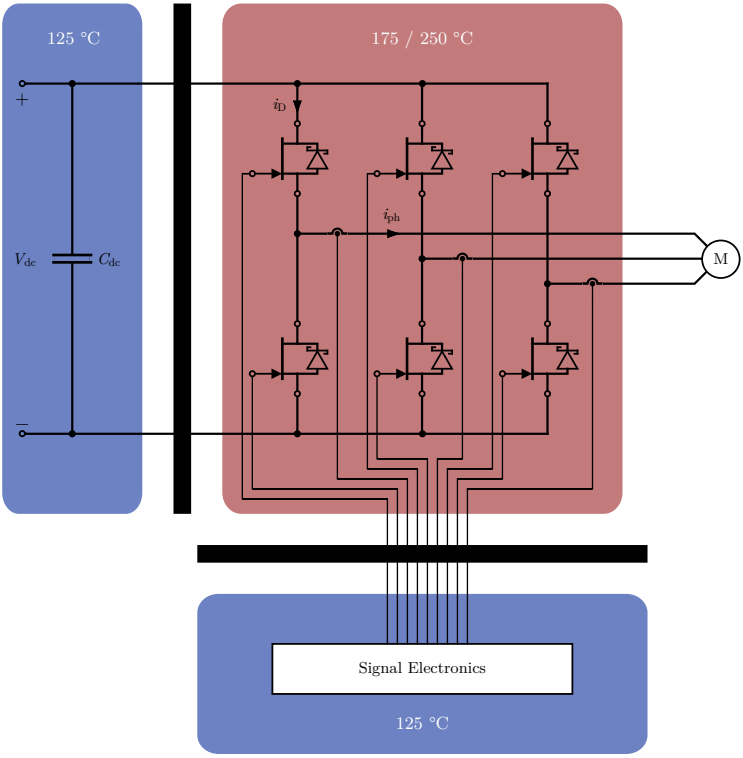


Figure 5.2: Concept of thermal design of high temperature inverter system: The dc-link capacitors with an upper temperature limit of 125 °C are thermally isolated from the hot power semiconductors (junction temperature up to 250 °C) by placing them below the heat sinks (distance: 45 mm). The control electronics need to be very close to the gate connections of the switches to allow fast switching and low switching losses. Thus, a special thermally isolating material is used to isolate the control electronics from the hot switches. Additionally, the signal electronics are actively cooled by a Peltier cooler.

not conduct currents at the same time and hence

$$I_D = \frac{I_{ph}}{\sqrt{2}} \tag{5.1}$$

applies for the rms values.

The correlation between the real output power P of the 3-phase inverter and I_{ph} is

$$P_{\mathrm{O}} = 3 \cdot V_{\mathrm{ph}} I_{\mathrm{ph}} \cos \Phi, \tag{5.2}$$

where V_{ph} denotes the rms value of the output phase voltage and $\cos \Phi$ the phase shift between V_{ph} and I_{ph}.

PWM modulation with third harmonic injection or space vector modulation leads to a maximum modulation index of $m_{\max} = 2/\sqrt{3}$ without overmodulation and thus, the maximum amplitude $\hat{V}_{\mathrm{ph,max}}$ of the phase voltage fundamental is

$$\hat{V}_{\mathrm{ph,max}} = m_{\max} \cdot \frac{V_{\mathrm{dc}}}{2} = \frac{2}{\sqrt{3}} \frac{V_{\mathrm{dc}}}{2} \tag{5.3}$$

with V_{dc} being the dc-link voltage of the voltage source inverter. In order to supply the output power P_{O} at this voltage, a phase current I_{ph} according to

$$I_{\mathrm{ph}} = \frac{P_{\mathrm{O}}}{\sqrt{3} \frac{V_{\mathrm{dc}}}{\sqrt{2}} \cos \Phi} \tag{5.4}$$

(*cf.* Equation (5.2)) has to be impressed. With Equation (5.1) this results in an rms current of each switch of

$$I_{\mathrm{D}} = \frac{P_{\mathrm{O}}}{\sqrt{3} V_{\mathrm{dc}} \cos \Phi} = 10.3\,\mathrm{A} \tag{5.5}$$

with an assumed displacement power factor of $\cos \Phi = 0.8$ for a high-speed permanent magnet synchronous machine as employed on the test bench in Section 8.4.

The normally-off JFET is available in a TO-247 discrete package with either a single $4.5\,\mathrm{mm}^2$ die having a nominal on-resistance of $100\,\mathrm{m\Omega}$ at $25\,^{\circ}\mathrm{C}$ [80] or two dies of the same size in parallel cutting also the on-resistance in half [60]. For this design, the latter $50\,\mathrm{m\Omega}$ switch is chosen as this promises increased efficiency while keeping the package size and thus volume constant.

The switches are operated at their specified maximum junction temperature of $175\,^{\circ}\mathrm{C}$. For a drain current of 10 A, the measured drain-source on-resistance of a switch with $37\,\mathrm{m\Omega}$ at $25\,^{\circ}\mathrm{C}$ and a gate current of 25 mA increases at $175\,^{\circ}\mathrm{C}$ to $113\,\mathrm{m\Omega}$ despite a gate current of 100 mA (*cf.* Section 4.1). As the maximum specified on-resistance of these switches is with $50\,\mathrm{m\Omega}$ at $25\,^{\circ}\mathrm{C}$ 35% higher than for the measured switch, this additional margin has to be considered for the conduction

loss calculation in order to make sure, that this calculation covers the highest possible on-resistance of the switch leading to $R_{\mathrm{DS,on}} = 153\,\mathrm{m\Omega}$. Hence, the conduction losses for one of the six switches in the inverter under full-load condition at 175 °C can be calculated to

$$P_{\mathrm{C}} = I_{\mathrm{D}}^2 \cdot R_{\mathrm{DS,on}} = 16\,\mathrm{W}. \tag{5.6}$$

The total switching energy E_{S} for a switch in a half-bridge setup with an inductive load is measured for different junction temperatures, dc-link voltages, and load currents in Section 3.3. As the output phase current and hence also the current switched by one of the six switches varies sinusoidally, the switching losses for one switch can be calculated using Equation (3.2) and Equation (3.3) by integrating the switching losses occurring of a single pulse period over one half-wave of the output current,

$$\begin{aligned} P_{\mathrm{S}} &= \frac{1}{2\pi} \int_{-\frac{\pi}{2}+\Phi}^{\frac{\pi}{2}+\Phi} E_{\mathrm{S}}(i_{\mathrm{D}}, T_{\mathrm{J}}) f_{\mathrm{S}}\, \mathrm{d}\varphi \\ &= h_E(T_{\mathrm{J}}) f_{\mathrm{S}} \left(\frac{1}{2} a_E + \frac{1}{\pi} \hat{I}_{\mathrm{ph}} b_E + \frac{1}{4} \hat{I}_{\mathrm{ph}}^2 c_E \right) = 14\,\mathrm{W}. \end{aligned} \tag{5.7}$$

5.3.2 DC-Link Capacitor

Important characteristics of the dc-link capacitor for this inverter system include the dc voltage, current ripple, and maximum allowable ambient and/or operating temperature as well as the capacitance needed.

A comprehensive study of the available capacitors (foil, ceramic, and electrolytic capacitors) for 120 °C ambient temperature reveals, that film capacitors suffer from significant voltage derating (between $4\,\mathrm{V/K}$ and $8\,\mathrm{V/K}$) as soon as the temperature rises above 85 °C. If the operating voltage at high ambient temperature is half of the nominal voltage, four capacitors are needed to achieve the same capacitance as the capacitance is cut in half by a series connection of two capacitors.

Ceramic capacitors suffer from a decreasing capacitance at high ambient temperatures and at high dc voltages. Furthermore, they have a low capacitance per device, leading to a high number of devices needed while the reliability of the devices is questioned due to cracks potentially occurring at the caps.

With respect to electrolytic capacitors, reduced lifetime especially at elevated temperatures is often seen as disadvantageous. This is particularly the case for many power electronic applications with specified lifetimes of significantly more than 10'000 h. For automotive requirements, the lifetime of properly designed electrolytic capacitors is sufficient. Therefore, electrolytic capacitors are considered for this inverter system.

The required dc voltage rating is given by the dc-link voltage of the inverter system (700 V) and the ambient temperature of 120 °C defines the operating temperature in a first step. The capacitance is given by the allowed dc-link voltage variation depending on capacitor current and switching frequency, by the duration of a supply failure that has to be compensated as well as the dynamic response of the supply to load variations and is chosen to 50 µF. The most essential parameter for choosing the right electrolytic capacitor is the rms value I_C of the capacitor current, that can be calculated by

$$I_C = \frac{P_O}{\sqrt{3}\frac{V_{dc}}{\sqrt{2}}\cos\Phi}\sqrt{2m\frac{\sqrt{3}}{4\pi} + \cos^2\Phi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{116}m\right)} = 8.4\,\text{A} \quad (5.8)$$

for $\cos\Phi = 0.8$ and $m = 0.68$, which is the value where the maximum current ripple occurs for $\cos\Phi = 0.8$ [99]. The electrolytic capacitor Epcos "B43693A2476" with a capacitance of 47 µF, a rated dc voltage of 250 V and a ripple current capability of 3.38 A at 125 °C is chosen [100]: Three capacitors are connected in series and 4 in parallel, leading to an overall capacitance of 63 µF and 13.5 A rms current carrying capability. The volume consumed by the 12 capacitors is 0.19 l.

5.3.3 Arrangement of Main Components

The arrangement of the main components of the inverter system is subject to certain, partially conflicting, electrical, and thermal constraints.

First, the setup is required to be symmetric (identical for each phase) with respect to the gate drive inductances of the three half-bridge legs in order to facilitate equal switching times and hence equal switching losses. The air flow for cooling the power semiconductors has also to be symmetric to make sure that the thermal resistance of the power semiconductor switches and diodes, respectively, is equal.

Second, the connections between the power semiconductors and the control electronics including the gate driver as well as between the power semiconductors and the dc-link capacitors have to be of very low inductance in order to allow fast switching without excessive gate ringing (*cf.* Chapter 4) and to avoid oscillations of the dc-link voltage.

Third, the main components operate at significantly different temperature levels, as can be seen from Figure 5.1. The SiC power semiconductor switches and diodes have to be operated at junction temperatures up to 250 °C under full load condition in order to fully utilize them at ambient temperatures of 120 °C (*cf.* Chapter 3). The temperature of the power semiconductor package surfaces that are not attached to the heat sink (i.e. the top side and shoulders of the package) is very close to the junction temperature of the semiconductor as the thermal resistance from this surface to the surrounding air is significantly higher than from the junction to the surface. The upper temperature limit of the control electronics and dc-link capacitors that are available as standard components is 125 °C. Hence, it has to be made sure, that the required temperature drop from the power semiconductors to the control electronics and dc-link capacitors of $250\,^{\circ}\mathrm{C} - 125\,^{\circ}\mathrm{C} = 125\,\mathrm{K}$ is maintained.

Figure 5.3 shows two of the considered setups. In Figure 5.3(a) the power semiconductors are mounted horizontally on heat sinks with vertical fins, whereas in Figure 5.3(b) the switches and diodes are mounted vertically on heat sinks with horizontal fins. The dimensions of both concepts are determined by the footprint of the power semiconductor packages and the height of the cooling fans. The semiconductors of a bridge leg are assembled adjacent to each other in a row, determining the length of the heat sink. The two high temperature fans (*cf.* Chapter 6) placed in front of the heat sinks match with a width of 80 mm the width of the three bridge legs in Figure 5.3.

The PCBs for the control electronics and the dc-link capacitors are mounted on top and underneath the power semiconductors, heat sinks and fans. It is also possible to place both together either on top or underneath the heat sinks. If they are placed at the sides of the heat sinks in parallel to the fins, a symmetric connection to the three half-bridge legs will not be possible.

In the concept shown in Figure 5.3(b), the power semiconductor packages with surface temperatures close to 250 °C are not placed directly underneath the PCB containing the control electronics in contrast

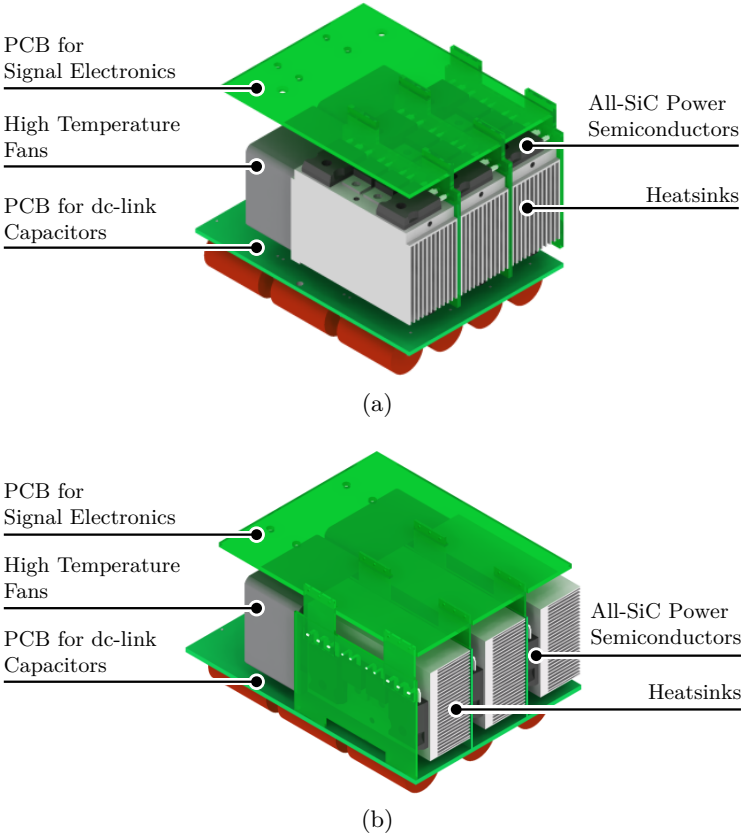


Figure 5.3: Considered arrangement of SiC power semiconductors, heat sinks, fans, control, and dc-link capacitor PCBs. For the (b) vertical arrangement, the hot power semiconductors are not placed close to the signal electronics in contrast to the (a) horizontal concept. The disadvantage of (b) compared to (a) is the 10% higher thermal resistance for the same overall volume. Hence, the setup according to (a) is chosen for this inverter system.

to Figure 5.3(a). Furthermore, the air flow generated by the fans makes sure, that the surface of the packages as well as the pins are cooled so that only a negligible amount of heat is fed into the connecting PCB and thus to the gate drivers and dc-link capacitors. Hence, the dis-

sipated power is not directly induced into the control electronics PCB while the gate driver and dc-link parasitic inductances are the same for both concepts.

Finally, Figure 5.3(a) is chosen for this inverter system because of the 10% lower thermal resistance of this arrangement for equal overall volume. As can easily be seen, the length of the fins has to be decreased for the version shown in Figure 5.3(b) and the baseplate area of the heat sinks is not fully utilized as it is larger (60 mm × 44 mm) than the area consumed by the power semiconductor packages (two TO-247 packages containing each two 4.5 mm^2 SiC JFET dies and two TO-220 packages containing each a 8 mm^2 SiC Schottky diode die). Accordingly, the outer fins of the heat sink do not contribute significantly to the cooling. Furthermore, in concept Figure 5.3(b), the packages of the power semiconductors including their pins are located directly in the air-flow leading to an increased risk of dielectric breakdown caused by small dust particles that might be contained in the air-flow.

In the final concept of Figure 5.3(a), the dc-link capacitor board is placed underneath the heat sinks. The bottom end of the heat sinks shows a temperature of +10 K to +20 K (depending on whether the junction temperature is 175 °C or 250 °C) above ambient temperature level. PCBs with broad (60 mm) and close (distance between a pair of tracks only 0.5 mm) tracks make sure, that the connection shows a low parasitic inductance. The thermal management of the control electronics is described in Section 5.4.

5.3.4 Design of Power Semiconductor Heat Sinks

An optimum fin geometry can be calculated for the physical dimensions of the heat sink derived in Section 5.3.3 and the fluid dynamic performance of the fan (*cf.* Figure 6.2) [101]. The results of this optimization for an aluminium heat sink with a width of 80 mm (thus matching the cross-section of two fans) and a length of 83 mm (62 mm for the heat sink of the power semiconductors and 21 mm for the heat sink of the Peltier cooler) are as follows: A minimum thermal resistance of 0.14 K/W can be achieved for 46 fins with a thickness of 0.52 mm. Such thin fins can be manufactured by wire eroding. In the case at hand, the heat sinks are milled and thus the thickness is subject to a limit of 0.9 mm to avoid destruction of the fins during machining. The spacing is limited to values larger than 1.6 mm due to the availability of saw blades with a

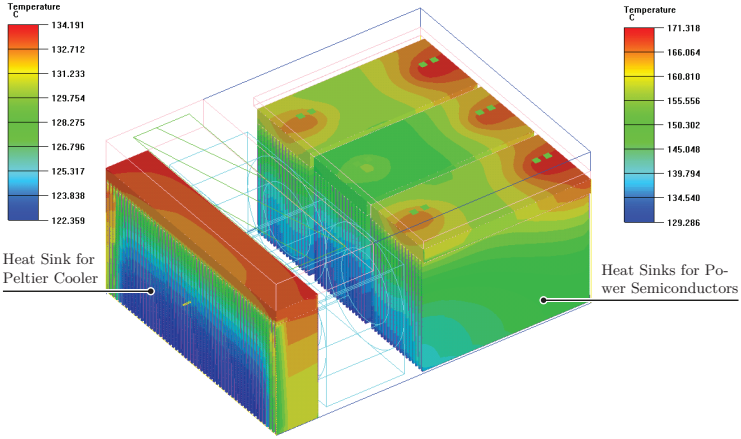


Figure 5.4: Thermal simulations of the cooling of the power semiconductors and the Peltier cooler. The ambient temperature is 120 °C, the junction temperature of the power semiconductors is set to 250 °C (relevant operating point for the design of the electronics cooling) and the power dissipated by the Peltier device is 50 W.

thickness of 1.6 mm and a diameter of more than 40 mm. This leads to 30 fins and a thermal resistance for this heat sink of 0.15 K/W. Due to a rather flat optimum of the thermal resistance, the thermal resistance increases only by 10% even though the number of fins is reduced by a factor of more than 1.5. The thermal resistance of each of the three heat sinks for the power semiconductors depicted in Figure 5.3 is then calculated to $3 \cdot \frac{83\,\mathrm{mm}}{62\,\mathrm{mm}} \cdot 0.15\,\mathrm{K/W} = 0.6\,\mathrm{K/W}$. The resulting temperature distribution for the heat sink of the Peltier device and the power semiconductor heat sinks is simulated with Icepak and shown in Figure 5.4.

5.4 Signal Electronics Cooling

5.4.1 Concept of Signal Electronics Box

For the control electronics with an upper temperature limit of 125 °C, which are according to Figure 5.3(a) placed directly above the hot power semiconductors and heat sink baseplate, a thermal isolation, and cooling concept is developed. The key ideas are shown in Figure 5.5. The hot

surface of the power semiconductors as well as their gate and source connections cause a heat input into the control board. Additionally, heat is dissipated by the control electronics (e.g. by the DSP and the gate drivers delivering 100 mA at a voltage level of 3 V to each switch during its on-state). At the same time, it has to be assumed as a worst case scenario in the later arrangement within the HEV, that the converter is encapsulated such that the control electronics experience a high thermal resistance to the 120 °C ambience. As the allowed temperature drop is only 5 K, the power that could be conducted to the ambience is very limited compared to the heat input. Therefore, an active cooling of the control electronics is needed. For this purpose, the control electronics are encapsulated in a thermally isolating box and cooled to a temperature level of 120 °C by a Peltier cooler. The power extracted from the electronics box and the heat dissipated by the Peltier device is fed into a heat sink. Ambient air (120 °C) is sucked through this heat sink by the fan located in between the heat sinks for the Peltier device and the power semiconductors, respectively. Then, the air slightly heated up by the Peltier cooler heat sink is blown through the heat sinks of the power semiconductors.

To limit the electrical power that has to be fed into the Peltier cooler, the heat induced into the control board has to be minimized. For a detailed analysis of the different heat sources, an equivalent circuit model is shown in Figure 5.6. A significant temperature reduction of the top sides of the power semiconductor packages can be achieved by means of copper clips mounted on the top side of the packages and attached to the heat sink baseplate (*cf.* Figure 5.7(a)). These clips (thickness: 2 mm) cover the top sides and a poor thermal contact to the packages (e.g., by a rough copper surface or isolating film between the packages and the clips leading to a high thermal resistance) together with a connection of low thermal resistance to the heat sink makes sure the temperature of the clips is comparable to the temperature of the heat sink baseplate. The clips are represented in Figure 5.6 by $R_{\mathrm{th,Cu,1}}$.

Furthermore, a thermal isolation material is mounted between the clips and the control electronics PCB (*cf.* Figure 5.7(a)). Frenzelit "novaplan 02980" sheets with a thermal conductivity of 0.1 $^{\mathrm{W}}/_{\mathrm{mK}}$, a temperature limit of more than 1000 °C and a thickness of 0.8 mm [102] are glued together with a distance of 0.8 mm to make use of the good thermal isolation capabilities of air (thermal conductivity: 0.026 $^{\mathrm{W}}/_{\mathrm{mK}}$). Loctite 5399 glue with a thermal conductivity of less than 0.3 $^{\mathrm{W}}/_{\mathrm{mK}}$ and

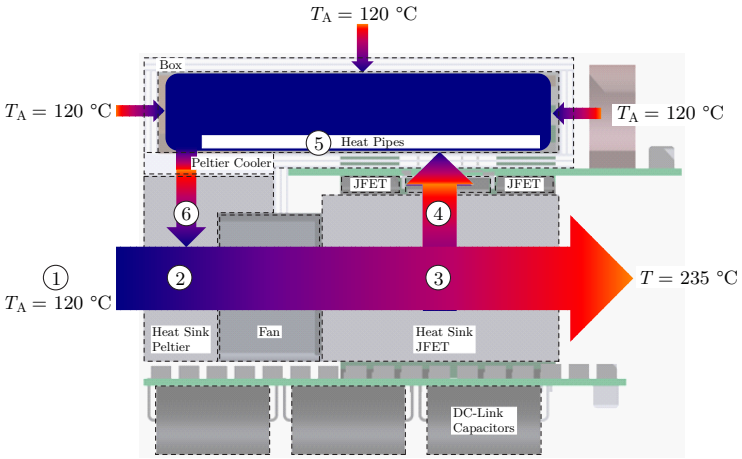


Figure 5.5: Illustration of heat flow within the inverter system: Ambient air (120 °C) ① is sucked through the heat sink ② for the Peltier cooler by the fans located in between the heat sinks for the Peltier device and the power semiconductors. Then, the air slightly heated up by the Peltier cooler heat sink is blown through the heat sinks ③ of the power semiconductors. The hot surface of the power semiconductors as well as their gate and source connections cause a heat input into the control electronics box ④; the heat is transferred within the box by horizontal heat pipes ⑤ to the thermoelectric cooler ⑥.

a maximum specified temperature of 275 °C is used [103]. This sandwich construction (total thickness of 4 mm) is also used for the faces of the electronics box. The resulting thermal resistances of the isolation are denoted in Figure 5.6 by $R_{\mathrm{th,iso},i}, 1 \leq i \leq 6, i \in \mathbf{N}$.

The heat fed into the electronics box by the pins can be significantly reduced by only feeding the required gate and source connections of the switches into the electronics box with 10 mil narrow, 35 µm thick and 10 mm long tracks ($R_{\mathrm{th,Cu,pins}}$ in Figure 5.6). This leads to an increase of the thermal resistance of each connection by a factor of 10 (27 K/W for each TO-247 pin compared to 300 K/W for each PCB track). Additionally, the drain and diode pins are interconnected on the vertical PCBs in between the heat sinks (*cf.* Figure 5.7) so that only 6 times 1 gate and source connection, 3 times 2 tracks for the current measurement signal and 1 times 2 tracks for the voltage measurement signal

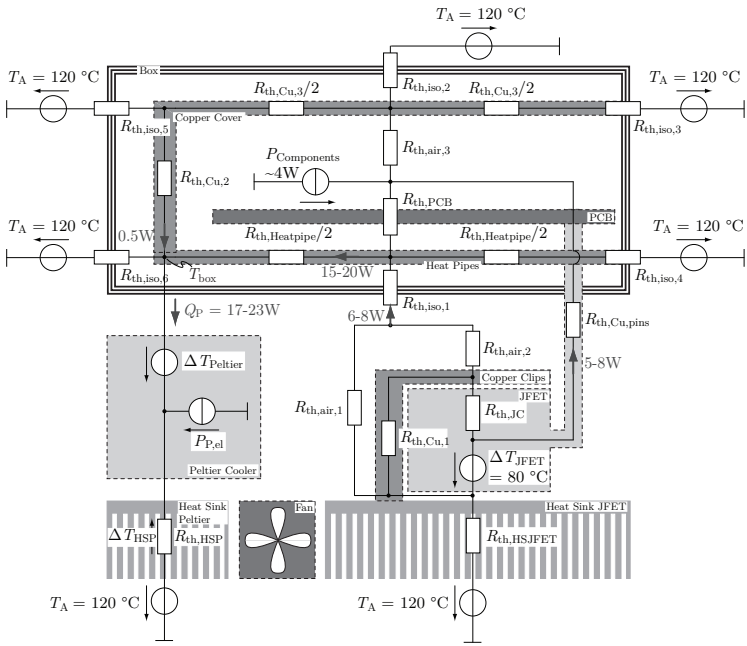
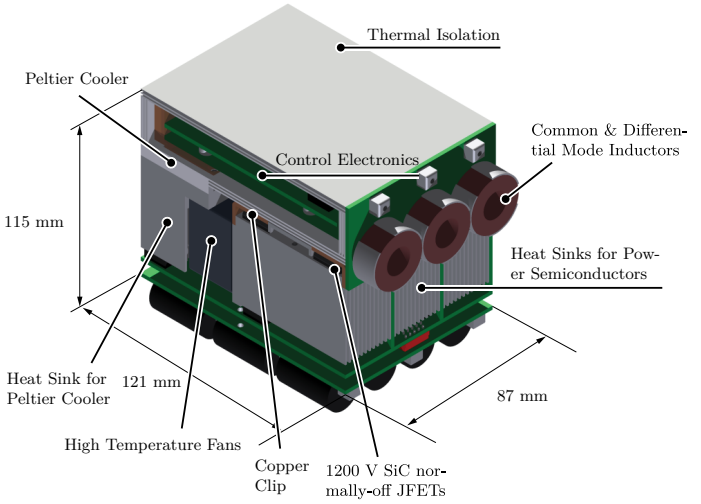


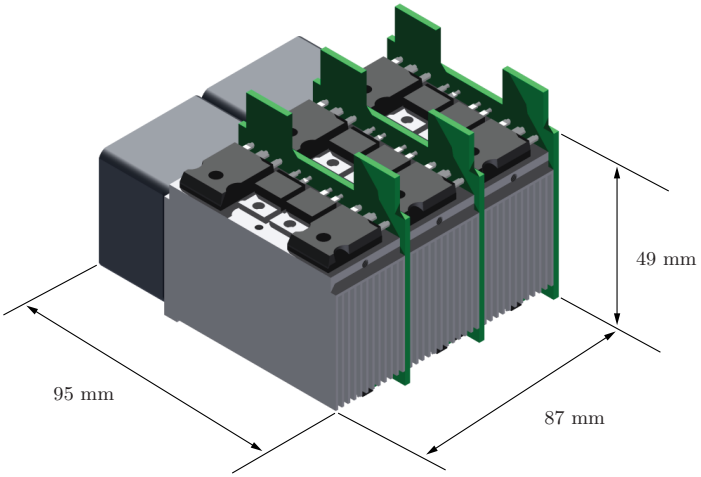
Figure 5.6: Equivalent circuit model to calculate the heat induced into the control electronics box (20 W) and to derive a model for the Peltier cooling.

(20 in total) need to be fed into the control electronics box. Overall, a total amount of 20 W needs to be pumped out of the electronics box. Including a safety margin, the Peltier cooler is designed in Section 5.4.2 for a removal of 30 W out of the electronics box.

As can be seen from Figure 5.5 and Figure 5.6, the largest portion of heat is fed into the box in the region above the power semiconductors (right hand side). On the left hand side, the Peltier cooler pumps the heat out of the box. To enable an even temperature distribution in the box, heat pipes are soldered on the bottom layer of the PCB in order to thermally short circuit the PCB to the Peltier device. Furthermore, an L-shaped copper cover is soldered to the upper control electronics PCB in order to provide a thermal shielding and a low thermal resistance path to the Peltier cooler.



(a)



(b)

Figure 5.7: (a) CAD representation of the investigated inverter system. The overall volume including dc-link capacitors and active control electronics cooling is 1.2 l leading to an overall power density of 8.3 kW/l. (b) CAD representation of the power part of the inverter system with a volume of 0.4 l (including the fans).

5.4.2 Design of Peltier Cooler for Optimum Cooling

By feeding electrical power $P_{\mathrm{P,el}}$ into the Peltier cooler, heat Q_{P} is transported from the cold side of the Peltier cooler to the hot side. At the hot side, the sum $P_{\mathrm{P,el}} + Q_{\mathrm{P}}$ has to be fed to a heat sink.

The characteristics of a Peltier device are shown in Figure 5.8 (solid lines) and include the maximum cooling power (only available at zero temperature difference $\Delta T_{\mathrm{Peltier}}$ between hot and cold side) and the maximum temperature difference $\Delta T_{\mathrm{P,max}}$ between the cold and hot side. At a constant supply current, the cooling power decreases with increasing $\Delta T_{\mathrm{Peltier}}$ linearly and is zero at $\Delta T_{\mathrm{P,max}}$. The electrical power $P_{\mathrm{P,el}}$ fed into the cooler is proportional to its supply voltage. With the supply current decreasing, the load line is shifted towards lower cooling power and $P_{\mathrm{P,el}}$ decreases. This can lead to a higher efficiency. Hence, the cooling system is not necessarily smallest at a maximum supply current I_{max}.

With increasing $\Delta T_{\mathrm{Peltier}}$ the cooling power and efficiency of the Peltier cooler decrease. To be able to use a small Peltier cooler, $\Delta T_{\mathrm{Peltier}}$ should be kept at a low level. This makes a small thermal resistance $R_{\mathrm{th,HSP}}$ of the heat sink necessary and thus leads to a bulky heat sink.

On the other hand, with a large $\Delta T_{\mathrm{Peltier}}$, a higher thermal resistance and thus a smaller heat sink is feasible, on the expense of a larger area Peltier cooler. The resulting optimum with respect to the volume of the heat sink can be calculated using a "temperature loop" in Figure 5.6,

$$\Delta T_{\mathrm{Peltier}} = T_{\mathrm{box}} - T_{\mathrm{A}} + \Delta T_{\mathrm{HSP}}, \tag{5.9}$$

as $T_{\mathrm{box}} = T_{\mathrm{A}} = 120\,^{\circ}\mathrm{C}$. $P_{\mathrm{P,el}}$ and Q_{P} depend on the chosen Peltier cooler. As similar Peltier devices show comparable characteristics, the calculation is conducted with the single-stage Peltier cooler "QC-31-1.4-8.5M" manufactured by Quick-Cool [104]. The following calculation leads to the total area needed for the Peltier devices. This area can be filled by several smaller Peltier devices or a single one having the required size.

$R_{\mathrm{th,HSP}}$ depends on the fan, the volume of the heat sink and choice of fin geometry. The width and height of the heat sink is given by the choice of power semiconductors and fans (*cf.* Section 5.3.1). To calculate the power that can be dissipated by the Peltier cooler, the thermal resistance $R_{\mathrm{th,HSP}} = 1.5\,\mathrm{K/W}$ of a heat sink having the same size as the Peltier cooler is determined like for the heat sinks of the power

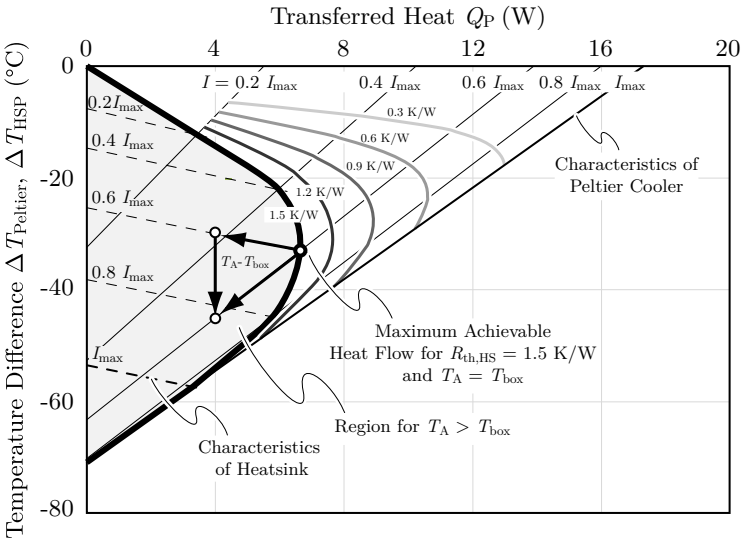


Figure 5.8: Characteristic curves of Peltier cooler (solid lines) and heat sink for the Peltier cooler (dashed lines). Intersections (thick solid line) mark the possible operating points where the temperature inside the box is at the same level as the ambient temperature. This front is shifted for different heat sink sizes. The most right point on each front designates the maximum achievable heat flow with a certain heat sink.

semiconductors (*cf.* Section 5.3.4). In addition to the characteristic curves depicted in Figure 5.8, the characteristic curves of the heat sink (shown as dashed lines in Figure 5.8) can be calculated according to

$$\Delta T_{HSP} = R_{th,HSP} \left(Q_P + P_{P,el} \right). \tag{5.10}$$

For this inverter system, T_{box} equals T_A, leading to $\Delta T_{Peltier} = \Delta T_{HSP}$. This corresponds to the intersections of the Peltier and heat sink characteristic curves (thick solid lines in Figure 5.8). This front is shifted for different thermal resistances and thus volumes of the Peltier heat sink. Here, the maximum heat flow of 7.5 W can be achieved for approximately $0.6 I_{max}$. With the required total heat flow of 30 W (*cf.* Section 5.4.1), four 20 mm × 20 mm coolers or one 40 mm × 40 mm sized Peltier cooler is needed.

Here, the current of $0.6I_{\mathrm{max}}$ is a fixed value. If the pumped heat is lower (e.g. 4 W instead of 7.5 W for each Peltier cooler), the operating point of the Peltier cooler is shifted away from the intersections line. The smaller amount of heat leads to a smaller temperature drop across the heat sink, but to a larger temperature drop $\Delta T_{\mathrm{Peltier}}$ across the Peltier device. This causes a temperature difference between the ambient air T_{A} and the box T_{box} such that the temperature level inside the box is lower. If the pumped heat Q_{P} increases to values larger than 7.5 W, the temperature in the box will be higher than the ambient air temperature.

5.5 Summary

The design of a 120 °C ambient temperature forced air-cooled automotive inverter with a switching frequency of 50 kHz is shown. It employs 1200 V normally-off SiC JFETs with anti-parallel Schottky diodes and allows the use of power semiconductors with junction temperatures up to 250 °C. To operate other inverter components such as the signal electronics and the dc-link capacitors within their specified temperature range a heat management concept is developed that includes active cooling with the help of a Peltier cooler. This is possible only at the expense of a significantly higher complexity and a reduced efficiency and power density of the overall converter. The volume needed for the active cooling of the signal electronics accounts for 20% of the overall converter volume. Experimental results are given in Chapter 8, Section 8.4, after research on high performance fans able to operate at high ambient temperatures (Chapter 6) and a current measurement system that allows to measure the switch current directly at the power semiconductors at 250 °C (Chapter 7).

Chapter 6

High Temperature Fan

6.1 High Temperature Capability of Available Fans

Most of the commercially available dc fans suitable for designing compact power electronic converters, i.e. those having a high pressurization and volume flow with respect to their volume, suffer from operating temperature limits below or equal 75 °C. The electrical and mechanical design of these fans might allow the manufacturer to test and specify the devices for somewhat higher ambient temperatures with only slight component changes. Still, the lifetime of the ball bearings used in e.g. Sanyo Denki fans with high performance concerning pressurization and volume flow related to the volume, is cut in half for each 15 K ambient temperature increase and the maximum operating temperature is 105 °C [105].

Other fan manufacturers sell fans for electronics cooling with temperature ratings up to 90 °C but these fans suffer from larger size and lower fluid dynamics performance compared to the Sanyo Denki models [106]. Other solutions available on the market are fans for ovens with recirculating air that are not equipped with an electrical machine in the hub but have it placed externally to reduce the ambient temperature for the electrical machine. The fan is then driven by a belt or a shaft which results in a more bulky setup and available rotational speeds are typically lower.

High ambient temperature electrical machines for integration into the fan hub are currently also investigated for other application areas, especially in the aerospace and downhole industry. Research for expeditions to the Venus have yield switched reluctance machines for up to 540 °C, but they are designed for an operational lifetime of only 50 days [39]. Furthermore, deeper oil reservoirs are currently explored, where electrical submersible pumps are used to provide a continuous flow of oil up to the surface [41]. The electrical machines used in such pumps can withstand temperatures up to 218 °C [42].

In this chapter, a high temperature brushless direct current (BLDC) machine fan withstanding an ambient temperature of 250 °C with a rotational speed of 19'000 min^{-1} for forced air-cooling of advanced automotive power electronics is designed. The BLDC electrical machine driving the fan is integrated into the hub of the fan and thus can withstand 250 °C ambient temperatures as well. The power electronic inverter for the BLDC machine can be realized on a separate PCB, that can be integrated into the main converter.

The fluid dynamic performance of the fan in terms of static pressure and volume flow at the nominal ambient temperature of 120 °C for power electronic converters placed under the engine hood in HEVs is comparable to that of commercial high performance fans at their nominal ambient temperature of 20 °C. The 250 °C specification gives designers of high-junction-temperature SiC power electronic converters more degrees of freedom for arranging the converter components as the fans can also be placed on the air outlet side of the heat sink so that they draw the hot air out of the heat sink rather than blowing it into the heat sink. Then, an arrangement with a fan in between two heat sinks is also possible

It is shown in detail in the next section Section 6.2, how the fan specifications, i.e. the dimensions, fluid dynamic performance, and machine characteristics are derived with respect to the needs induced by air-cooling of ultra compact automotive power electronic converters for high ambient temperatures. Subsequently, the design of the electrical machine and mechanical parts is carried out in Section 6.3 and Section 6.4, respectively. In Chapter 8 (Section 8.2), experimental results in terms of electrical voltage, current, and power as well as fluid dynamic and acoustical measurements are presented.

6.2 Fan Specifications

6.2.1 Air-Cooling of Power Electronics

In general, the cooling system of a power electronic converter has to dissipate the power loss of components within the converter via a thermally conductive path to the ambience, where a thermal resistance R_{th} should be as low as possible. At the same time, the cooling system is required to have a volume V_{CS} as small as possible in order to facilitate a high power density of the converter, leading to the definition of the *cooling system performance index* (CSPI) which is the inverse of the product of R_{th} and V_{CS} [107].

To make sure that the thermal resistance $R_{\mathrm{th,HA}}$ of the heat sink does not increase significantly throughout the operation of the power electronic converter due to dust congesting the heat sink air channels, an air filtering system has to be deployed. This filtering system should clean the air before it is blown through the heat sinks by the fans and can be similar to what is already well known in the automotive industry for use with internal combustion engines. Accordingly, considerations regarding ingress protection (IP) rating affect more the overall design of the complete power electronic converter system than the fans.

Furthermore, standard requirements for technical systems apply also for power electronic cooling systems: low system complexity, low manufacturing and maintenance cost, low size, low weight, low power consumption, low noise generation, and low performance invariance against deterioration or spread for standard factory models.

6.2.2 Air Flow Direction

The applicability of a certain fan for a forced air-cooling setup within a power electronic converter can be assessed based on the direction of the air flow it produces: Centrifugal or radial fans can hardly be integrated into a typical setup without modifications where lossy components, e.g. power semiconductors, are mounted on heat sinks with extruded fins. A modified centrifugal fan, that guides the radial air flow into a tangential direction, is called blower. These fans deliver high pressure and volume flow for a certain outlet cross-section of the fan compared to axial fans, but their overall volume is usually significantly larger.

The most common fans with the largest variety of models for power electronics cooling are diagonal and axial flow fans. The difference

between both fans is that for diagonal fans the housing and sometimes also the blades are conical with a larger diameter at the fan outlet so that the air is guided not only in axial direction out of the fan but also shows a small radial velocity component. This allows the fan to produce higher pressure at a higher volume flow for the same size and power rating. It has to be mentioned though, that it is strongly dependent on the geometry of the heat sink attached to the fan outlet and the attachment itself (e. g. spacing between fan outlet and heat sink) whether the diagonal component of the air flow is utilized or whether the air is directed back into the axial direction by the heat sink. In fact, most fans that are referred to as "axial" are constructed as slightly diagonal fans. Hence, in this dissertation the terminology will be the same as usual and these fans will be referred to as axial. Some of the axial fans have guide vanes at the outlet side of the housing to reduce the air spin produced by the rotating vanes.

Counter rotating axial fans are equipped with two rotors that rotate in opposite directions yielding a high pressurization. Optimizing the fin design of the heat sink for the use with such fans with respect to the thermal resistance of the heat sink leads to very thin fins with very small spacing in between them which makes the manufacturing process very expensive and is only available for small aspect ratios of fin height to fin thickness [107]. Therefore, the additional pressure does usually not pay off in terms of power density.

Hence, the high temperature fan is designed here as a single stage axial flow fan with guide vanes.

6.2.3 Physical Dimensions

The length of the outlet cross-section edges of the high temperature fan is set with regard to ubiquitous applicability as 40 mm × 40 mm (*cf.* Figure 6.1(a)). This corresponds to the largest fans that are commercially available while still being below the size of one rack unit, which is 1U = 1.75 in = 44.45 mm. For reference purposes and the sake of compatibility, the axial length of the high temperature fan is chosen to 28 mm which equals the length of the Sanyo Denki model "San Ace 40 Gv" [108] with best-in-class static pressure over volume flow characteristics.

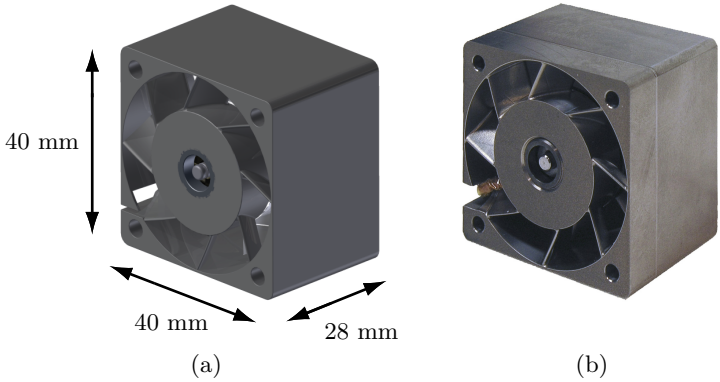


Figure 6.1: (a) CAD picture and (b) photograph of high temperature (250 °C / 500 °F) 19'000 min^{-1} BLDC fan for forced air-cooling of advanced automotive power electronics.

6.2.4 Static Pressure vs. Volume Flow at Increased Ambient Temperatures

The fluid dynamic characteristic of a fan as well as the heat sink fin and baseplate design determine the resulting thermal resistance $R_{\mathrm{th,HA}}$ from the heat sink surface (which carries the lossy components) to the ambience (to which the heat is dissipated). The fluid dynamic characteristic is usually given as a difference in static pressure Δp between the outlet and inlet side of the fan versus its volume flow $\dot{V}$ for a certain rotational speed n_{F} of the fan rotor.

This characteristic curve depends largely on the measurement conditions especially with respect to the air density ρ_{A}, which is mainly given by air temperature T and absolute air pressure p_{A}. Fan manufacturers often measure the curve according to the standard "AMCA 210-85", set by the Air Movement and Control Association (AMCA) International [109,110]. The reference air temperature is set to $T_{\mathrm{ref}} = 20\,^{\circ}\mathrm{C}$ and the absolute hydrostatic pressure of the air to $p_{\mathrm{A}} = 1.013 \cdot 10^5\,\mathrm{Pa}$ [109].

The curve of the commercial high performance fan Sanyo Denki San Ace 40 GV is given as an example for a rotational speed of $n_{\mathrm{RF}} = 16'500\,\mathrm{min}^{-1}$ in Figure 6.2 [108]. Also shown in this figure is the parabolic characteristic of the heat sink, i.e. the fluid dynamic load characteristic, which divides the characteristic curve of the fan into two parts:

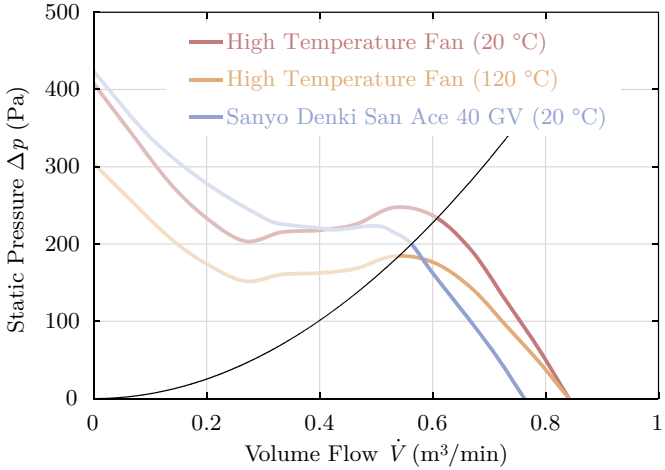


Figure 6.2: Static pressure over volume flow curves for the high temperature fan presented with 19'000 min^{-1} at 20 °C and 120 °C as well as for the Sanyo Denki reference fan with 16'500 min^{-1}. The fluid dynamic design criteria for the high temperature fan at 120 °C in terms of $\dot{V}_{\mathrm{max}}$ and Δp is fulfilled for the largest part of the characteristic curve given by the parabola of operation.

The right part starts at free air conditions with maximum volume flow $\dot{V} = \dot{V}_{\mathrm{max}}$ and shows a linear correlation between $\dot{V}$ and Δp. The intersection point of curve and parabola is advantageously selected in the region where the gradient of the curve changes and approaches zero and goes even positive, i.e. where Δp decreases (slightly) with decreasing $\dot{V}$. This happens for the Sanyo Denki San Ace 40 GV for $\dot{V}_{\mathrm{S}} = 0.56\,\mathrm{m}^3/\mathrm{min}$. In this region, airflow separation at the fan blades occurs and the fan stalls leading to a significantly affected air-side performance as well as noisy and surging air flow. For smaller volume flows, the blades move the air by centrifugal forces until zero air flow $\dot{V} = 0$. For a safe, reliable, and efficient operation of the fan, the fluid dynamic load (e.g. a heat sink) has to be chosen such that the intersection of the load line and the fan curve are in the right part of the fan curve [109]. As mentioned in Section 6.1, the design target is to have an equal or better fluid dynamic characteristic within the relevant part of the characteristic curve at the nominal operating air temperature, i.e. at $T_{\mathrm{nom}} = 120\,°\mathrm{C}$, than that of the San Ace 40 GV reference fan at $T_{\mathrm{ref}} = 20\,°\mathrm{C}$.

To analyze the impact of increased ambient temperature on the performance of a fan, first the correlation between air density ρ_A and air temperature T is found using the ideal gas law Equation (6.1). It is valid for vanishing absolute pressures $p_A \to 0$, but for almost all real gases, including dry air, deviations from the ideal behavior are negligible at atmospheric pressures [111]. The temperature independent gas constant is $R_c = 287.05\,\mathrm{J/kg{\cdot}K}$ for dry air and the absolute pressure is with $p_A = 101.325\,\mathrm{kPa}$ [112] the same as for standard conditions because the air underneath the engine hood in HEVs can expand when heated by the ICE and hence, this change of state is of isobar type [113],

$$\rho_A = \frac{p_A}{R_c \cdot T} = \begin{cases} 1.20 \\ 0.90 \\ 0.67 \end{cases} \mathrm{kg/m^3} \quad \text{for} \quad \begin{matrix} T = 20\,^\circ\mathrm{C} \\ T = 120\,^\circ\mathrm{C}. \\ T = 250\,^\circ\mathrm{C} \end{matrix} \tag{6.1}$$

The high temperature fan will be operated in speed controlled mode, hence the rotor speed n_F is constant within the operating temperature range of the fan. Even with varying air density, this leads to a constant volume flow $\dot{V} = \text{const}$ of the fan for $n_F = \text{const}$ [114].

However, $\Delta p(T)$ and the mechanical shaft power $P_{S,m}(T)$ of the fan scale proportionally with ρ_A leading to an inversely proportional correlation with T for $n_F = \text{const}$ [114],

$$\frac{\Delta p(T)}{\Delta p(T_{ref})} = \frac{P_{S,m}(T)}{P_{S,m}(T_{ref})} = \frac{T_{ref}}{T} = \begin{cases} 1 \\ 0.75 \\ 0.56 \end{cases} \quad \text{for} \quad \begin{matrix} T = 20\,^\circ\mathrm{C} \\ T = 120\,^\circ\mathrm{C}. \\ T = 250\,^\circ\mathrm{C}. \end{matrix} \tag{6.2}$$

The impact on the characteristic curve of the fan can be seen in Figure 6.2 where the fluid dynamic characteristic of the high temperature fan is shown for $T_{ref} = 20\,^\circ\mathrm{C}$ and $T_{nom} = 120\,^\circ\mathrm{C}$. With respect to the change in power, it has to be noted, that the input power $P_{F,el}$ of a fan may not decrease by the same amount as the mechanical shaft power does due to decreasing fan motor and inverter efficiency at higher temperatures.

The reduction in static pressure from the reference fan at $T_{ref} = 20\,^\circ\mathrm{C}$ to the high temperature at $T_{nom} = 120\,^\circ\mathrm{C}$ caused by an increased temperature can be compensated by increasing the rotor speed of the fan from n_{RF} of the San Ace 40 GV fan to n_{HTF} for the high temperature fan.

To derive the exact correlation between n_{RF} and n_{HTF}, the following fan scaling laws can be used for $T = \mathrm{const}$ [107],

$$\dot{V} = k_1 \cdot n_{\mathrm{F}} \cdot d_{\mathrm{F}}^3 \tag{6.3}$$

$$\Delta p = k_2 \cdot n_{\mathrm{F}}^2 \cdot d_{\mathrm{F}}^2 \tag{6.4}$$

$$P_{\mathrm{F,el}} = k_3 \cdot n_{\mathrm{F}}^3 \cdot d_{\mathrm{F}}^5. \tag{6.5}$$

The diameter of the fan rotor is denoted by d_{F} (which is often approximated by the edge length of the quadratic outlet or inlet cross-section), the electrical input power by $P_{\mathrm{F,el}}$ and $k_i, i = \{1, 2, 3\}$, represent factors of proportionality depending on the design of a specific fan. k_1 and k_2 vary only by a factor of two from one fan to another for most commercial fans [107]. Assuming a similar fluid dynamic design of the reference fan and the high temperature fan in terms of the fan dimensions as well as the rotor and stator guide vanes, k_1 and k_2, respectively, will be very similar for the two fans. In order to meet the fluid dynamic design target of the high temperature fan, the following constraint has to be fulfilled for volume flows $\dot{V}_{\mathrm{S}} = 0.56\,\mathrm{m^3/min} \leq \dot{V} \leq \dot{V}_{\mathrm{max}}$:

$$\Delta p_{\mathrm{HTF}}(T_{\mathrm{nom}} = 120\,^{\circ}\mathrm{C}) \overset{!}{\geq} \Delta p_{\mathrm{RF}}(T_{\mathrm{ref}} = 20\,^{\circ}\mathrm{C}) \tag{6.6}$$

It can be seen from Equation (6.2) that $\Delta p_{\mathrm{max,HTF}}(T_{\mathrm{ref}})$ of the new high temperature fan has to be higher by a factor of $T_{\mathrm{nom}}/T_{\mathrm{ref}}$ than the pressure $\Delta p_{\mathrm{max,RF}}(T_{\mathrm{ref}})$ of the reference fan in order to meet Equation (6.6). With Equation (6.4), n_{HTF} can be calculated to

$$\begin{aligned} n_{\mathrm{HTF}} &= n_{\mathrm{RF}} \sqrt{\frac{\Delta p_{\mathrm{max,HTF}}(T_{\mathrm{ref}})}{\Delta p_{\mathrm{max,RF}}(T_{\mathrm{ref}})}} = n_{\mathrm{RF}} \sqrt{\frac{T_{\mathrm{nom}}}{T_{\mathrm{ref}}}} \\ &= 16'500\,\mathrm{min^{-1}} \cdot \sqrt{\frac{393.15\,\mathrm{K}}{293.15\,\mathrm{K}}} \approx 19'000\,\mathrm{min^{-1}}. \end{aligned} \tag{6.7}$$

According to Equation (6.3), the increased speed n_{HTF} also leads to an increase in volume flow of the high temperature fan. The maximum volume flow $\dot{V}_{\mathrm{max,HTF}}$ can be calculated compared to the maximum volume flow $\dot{V}_{\mathrm{max,RF}}$ of the reference fan as

$$\dot{V}_{\mathrm{max,HTF}} = \frac{n_{\mathrm{HTF}}}{n_{\mathrm{RF}}} \cdot \dot{V}_{\mathrm{max,RF}} = 0.88\,\mathrm{m^3/min}. \tag{6.8}$$

Furthermore, the shaft power $P_{\mathrm{S,m}}$ is also increased for the high temperature fan as it scales with n^3 [114]. The rise in shaft power for the nominal operating point T_{nom} of the high temperature fan compared

to the nominal operating point T_{ref} of the reference fan is not as high as expected from the cubic correlation as the temperature rise from T_{ref} to T_{nom} reduces the required shaft power according to Equation (6.2). The exact increase in shaft power $P_{\mathrm{S,HTF}}$ for the high temperature fan can be derived as

$$\begin{aligned} P_{\mathrm{S,HTF}}(T) &= P_{\mathrm{S,RF}}(T) \cdot \left(\frac{n_{\mathrm{HTF}}}{n_{\mathrm{RF}}}\right)^3 = P_{\mathrm{S,RF}}(T_{\mathrm{ref}}) \cdot \sqrt{\frac{T_{\mathrm{nom}}^3}{T_{\mathrm{ref}}}} \cdot \frac{1}{T} \\ &= P_{\mathrm{S,RF}}(T_{\mathrm{ref}}) \begin{cases} 1.55 & T = \ 20\,^{\circ}\mathrm{C} \\ 1.16 \quad \text{for} & T = 120\,^{\circ}\mathrm{C}. \\ 0.87 & T = 250\,^{\circ}\mathrm{C} \end{cases} \end{aligned} \tag{6.9}$$

The shaft power $P_{\mathrm{S,RF}}(T_{\mathrm{ref}})$ of the reference fan and thus the output power of its electrical machine is unknown; the electrical input power $P_{\mathrm{el,RF}}$ is 10.1 W at T_{ref} [108]. If a similar efficiency of the electrical machine for both fans is assumed, the required input power $P_{\mathrm{el,HTF}}$ of the high temperature fan can be specified to 15 W. This makes the operation of the high temperature fan at rated speed n_{HTF} even at $T_{\mathrm{ref}} = 20\,^{\circ}\mathrm{C}$, i.e. 100 K below its nominal operating point $T_{\mathrm{nom}} = 120\,^{\circ}\mathrm{C}$, possible.

The results of this section will be validated along with other experimental data in Chapter 8, Section 8.2.

6.2.5 Electrical Machine

General

In order to achieve a compact fan design (*cf.* Section 6.2.1), the electrical machine has to be integrated into the hub of the high temperature fan. Hence, the machine must be able to withstand an ambient temperature of 250 °C plus the self-heating due to its losses. Typically, an internal fan motor is designed as a machine with an external rotor as this simplifies the mechanical construction and the usual drawbacks of external rotor machines such as higher rotational mass with a larger distance to the axis of rotation, both of which lead to a higher moment of inertia than for an internal rotor machine, are of less importance for fan operation where the moment of inertia smoothes a potential cogging torque and the speed control is not required to be highly dynamic.

The input power of the machine is determined in Section 6.2.4 to 15 W at its nominal operating point with a rated speed of 19'000 min^{-1}. As this fan is designed for cooling of automotive power electronics, the

machine should be able to be driven by an inverter supplied from a 12 V dc bus.

Machine Type

Possible types of electrical machines can be based on either electric or magnetic fields. With respect to the machine dimensions with an outer diameter of 23 mm and an axial length of 10 mm (restricted by the mechanical design, *cf.* Section 6.4), those using magnetic fields for the electromechanical energy conversion are preferable due to a higher energy and force density [11, 115]. Possible concepts are induction, permanent magnet, switched reluctance or conventional dc machines with brushes or brushless dc machines. At first sight, induction and switched reluctance machines appear as favorable choices for harsh environmental conditions as they are regarded as very robust without need for expensive and temperature sensitive permanent magnets.

Still, it has to be considered, that the motor torque is generated by the stator and rotor flux components which can both be electromagnetically excited; alternatively, one set of windings could be replaced by permanent magnets. The flux density caused by a permanent magnet is constant for varying machine dimensions while the rated current of an electrical machine decreases with decreasing machine dimensions. Hence, for small drives with diameters of less than 100 mm like given in this case, machines with permanent magnets, i.e. dc or synchronous machines, are the favorable choice if a high power density is needed [11, 116].

Conventional dc machines with brushes can be driven from a constant dc voltage source in their nominal operating point so that no additional inverter is necessary which is advantageous especially at such harsh environmental conditions. Still, the brushes suffer from significant wear and affect the reliability. If the fan is required to be speed controlled in order to make sure that the fluid dynamic performance varies only little over the complete temperature range of approx. 300 K, additional controls are needed. Furthermore, a dc machine with brushes designed as with an external rotor requires additional mechanical effort.

Hence, the integrated machine of the high temperature fan will be designed as a BLDC machine which is constructed as permanent magnet synchronous machines (the magnetic design can be slightly different to make the rotor produce a rectangular rather than a sinusoidal back electromotive force) but is driven with (in case of a 3-phase ma-

chine) 120° phase-shifted rectangular voltages instead of pulse-width modulated voltages which would allow to achieve a sinusoidal current waveform. This gives a slightly higher torque and allows to reduce the switching frequency of the inverter and thus its losses which is in a 120 °C ambient temperature environment with only 55 °C margin to the upper junction temperature limit of Si power semiconductors a significant advantage.

Number of Phases

1-phase BLDC machines need less complex inverters than machines with a higher phase count. Either an H-bridge inverter with two high-side switches and four switches in total supplying a single winding or two low-side switches supplying two separate windings connected in anti-series can be employed. This half-wave configuration needs only two switches, but the copper utilization is lower than for the H-bridge as each winding conducts only one half-wave. A significant drawback of 1-phase machines is the asymmetry of the magnetic design needed to make sure that the machine can be put into rotation from any rotor position.

2-phase BLDC machines having symmetric windings can be started from any rotor angle, but the drive inverter complexity is basically multiplied by two for the H-bridge or half-wave solution. It is also possible to use a single half-bridge for two windings if the midpoint of the series-connected windings is connected to the midpoint of supply. This solution though requires a supply voltage balancing and cuts the voltage that can be applied to the windings in half.

A 3-phase BLDC machine appears as a reasonable compromise between the request for a symmetric machine design on the one hand and low drive effort on the other hand as the H-bridge of the 1-phase machine needs to be extended by only one more bridge leg. Furthermore, a large variety of gate drivers for 3-phase inverters and control ICs for 3-phase BLDC machines is available as 3-phase BLDC machines are widely used in industry. Hence, the BLDC machine for the high temperature fan will be designed as a 3-phase machine.

6.3 Electrical Machine Design

6.3.1 Windings

The isolation of the windings has to withstand the sum of the maximum ambient temperature of 250 °C and the temperature rise due to ohmic losses in the windings as well as iron losses in the stator. High temperature versions of conventional enameled copper wire can continuously withstand temperatures up to only 245 °C [117,118]. A solution is copper wire, that is clad by nickel for increased oxidation resistance and coated by ceramic for electrical insulation. It can withstand temperatures up to 700 °C for more than 1'000 h and 425 °C for more than 5'000 h [119].

The resulting specific electrical resistance ρ_{CuNi} of the nickel clad copper wire can be calculated, if the fractions of nickel and copper cross sections are given. The "Kulgrid 28" wire used for this setup consists of $y_{\mathrm{Ni}} = 27\%$ nickel and $y_{\mathrm{Cu}} = 1 - y_{\mathrm{Ni}} = 73\%$ [120]. As the density of nickel is with $8.880\,\mathrm{g/cm^3}$ less than 1% smaller than that of copper with $8.960\,\mathrm{g/cm^3}$ at 20 °C [121], it is of negligible interest for the calculation of ρ_{CuNi} whether the volume or mass fractions are given. At higher temperatures, the densities match even better as copper expands with $16.4 \cdot 10^{-6}\,1/\mathrm{K}$ and nickel with $13.1 \cdot 10^{-6}\,1/\mathrm{K}$ only.

If the wire cross-section is ideal such that a round copper conductor is encapsulated with a nickel clad of constant thickness, the following formula and results can be calculated from Ohm's law of parallel conductors using the specific electrical resistances $\rho_{\mathrm{Cu}} = 16.9\,\mathrm{n\Omega \cdot m}$ and $\rho_{\mathrm{Ni}} = 71.9\,\mathrm{n\Omega \cdot m}$ of copper and nickel, respectively, as well as their coefficients of the linear increase in resistivity with temperature, $\alpha_{\mathrm{Cu}} = 0.0039\,1/\mathrm{K}$ and $\alpha_{\mathrm{Ni}} = 0.0066\,1/\mathrm{K}$ [121]:

$$\begin{aligned}
\rho_{\mathrm{CuNi}} &= \frac{\rho_{\mathrm{Cu}} \cdot \rho_{\mathrm{Ni}}}{y_{\mathrm{Ni}} \cdot \rho_{\mathrm{Cu}} + y_{\mathrm{Cu}} \cdot \rho_{\mathrm{Ni}}} \\
&= \begin{cases} 1.26 \cdot \rho_{\mathrm{Cu}}(\ 20\,^\circ\mathrm{C}) & T = \ \ 20\,^\circ\mathrm{C} \\ 1.29 \cdot \rho_{\mathrm{Cu}}(250\,^\circ\mathrm{C}) \quad \text{for} & T = 250\,^\circ\mathrm{C} \\ 2.44 \cdot \rho_{\mathrm{Cu}}(\ 20\,^\circ\mathrm{C}) & T = 250\,^\circ\mathrm{C} \end{cases} \\
&= \begin{cases} 21.3\,\mathrm{n\Omega \cdot m} \quad \text{for} & T = \ \ 20\,^\circ\mathrm{C} \\ 41.3\,\mathrm{n\Omega \cdot m} & T = 250\,^\circ\mathrm{C} \end{cases}
\end{aligned} \tag{6.10}$$

(The conductivity of the wire is further affected by diffusion of nickel into the copper core. After 500 h of operation at 600 °C, the resistivity increases by another 25% for a wire with a fraction of 27% nickel [122].)

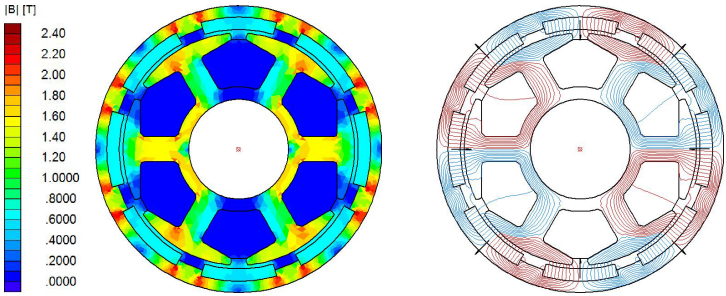


Figure 6.3: (a) Flux density distribution under full load condition. The flux density in the stator and yoke is less than 2.1 T which is below the saturation limit of 2.35 T of the employed iron cobalt material (*cf.* Section 6.3.2 and Section 6.3.4). (b) Magnetic field lines under no load condition of the BLDC machine.

To avoid cracks of the ceramic insulation, the minimum bending radius of the ceramic coated nickel clad copper wire has to be at minimum 10-times larger than the outer diameter of the wire, which influences the design of the stator iron sheet package significantly (*cf.* Section 6.3.2). For this setup, a wire with an external diameter of 0.1 mm is used that still can be machine wound [119].

6.3.2 Stator Iron Sheet Package

The minimum bending radius of the ceramic coated wire (*cf.* Section 6.3.1) means for the stator iron sheet package, that the tooth width has to be equal or larger than 2 mm. As higher numbers of teeth with a width of 2 mm would drastically reduce the winding area, the package is designed with 6 teeth (*cf.* Figure 6.3). The number of poles is chosen to 8, as with a lower number, the yoke would increase in radial thickness and the winding factor of 0.87 for this combination is better or equally good than for 10 or more poles.

Eligible materials include iron with silicon (FeSi), nickel iron (NiFe) or iron cobalt (FeCo). FeSi is the cheapest material but has a lower saturation flux density and higher losses. Lowest losses and highest permeabilities offers NiFe. Highest flux density and thus highest torque

and power density are possible with FeCo which makes it the favorable material for the high temperature fan.

"Vacoflux 48" by Vacuumschmelze shows a very narrow hysteresis loop ($H_C < 40\,{}^{A}/_{m}$) and a high saturation flux density of $B_{sat} = 2.35\,T$. The Curie temperature is $T_C = 950\,°C$ and the coefficient of linear thermal expansion is $\alpha_{CTE} = 9.5 \cdot 10^{-6}\,{}^{1}/_{K}$. For this setup, 100 individual 0.1 mm thick sheets are used leading to an axial length of the machine of 10 mm. The sheets are laminated together for easier manufacturing. The adhesive used by Vacuumschmelze is only specified up to 190 °C, at higher temperatures it looses its adhesive effect and transforms into carbon which influences the behavior of the package: The temperature of the material causes the hysteresis loop to shear so that the magnetic permeability decreases and the coercivity slightly increases. This leads to slightly higher losses (of about +5% for a temperature of 300 °C).

6.3.3 Permanent Magnets

The permanent magnets used in the high temperature fan need to have a sufficiently high remanence induction B_r and coercive force H_C at 250 °C. Hard magnetic materials with a high energetic product include neodymium iron boron (NdFeB) and samarium cobalt ($SmCo_5$ and Sm_2Co_{17}). For high temperature applications, the only possible material is SmCo. (Aluminium nickel cobalt (AlNiCo) is also possible, but has got a much lower energy product than SmCo.) Arnold Magnetics offers "Recoma" main grades as "Recoma HT" magnets, the latter for operating temperatures up to 520 °C. For the high temperature fan, "Recoma HT 420" magnets with a remanence of 0.9 T and an intrinsic coercive force of $1100\,{}^{kA}/_{m}$ at 250 °C are employed. The maximum demagnetization force applied to the magnets is $290\,{}^{kA}/_{m}$.

These magnets do not need to be protected against corrosion at 300 °C. At temperatures higher than 400 °C they could be either packaged in a steel housing, which increases the length of the air gap of the machine, or coated with aluminium (up to 500 °C) or with nickel (up to 550 °C).

The magnet segments can be fit into the yoke and are fixed only by their magnetic force. Alternatively, they can be laminated into the yoke with adhesive based on silicon or ceramics. These adhesives though cannot absorb high thermo-mechanical stresses. The thickness of the magnets should not be lower than the actual 1 mm in order to make

sure they do not break during manufacturing. If smaller thicknesses need to be realized, the magnets can be mounted into the yoke and then milled down to the desired thickness.

6.3.4 Yoke

The geometry of the yoke is chosen such that the flux density has a maximum value of 2 T. The air-gap is 0.3 mm. The material should have a relative permeability of 500 at this point for minimizing the reluctance of the magnetic path. Furthermore, the yoke's CTE should be close to that of the rotor as the yoke is directly fit into the rotor. The aforementioned cobalt iron alloy "Vacoflux 48" by Vacuumschmelze fulfills these criteria.

6.4 Mechanics Design

In this section, the mechanical design of the high temperature fan, especially the choice of different technologies such as the bearing technology and the selection of the design concept as well as the materials are described, each with respect to the high temperature rating, the resulting thermal expansion and reduced strength of the materials, and other constraints such as magnetic fields of the machine potentially causing eddy current losses.

The exploded view drawing in Figure 6.4 shows the assembly of the individual fan components. The fan housing is the structural part of the fan. On the outlet side, there is a center borehole with inside thread. The bearing case is screwed into that hole. The plain bearings are shrunk into the bearing case and carry the shaft. The stator iron sheet package is shrunk onto the bearing case and ceramic coated copper windings are wound onto the stator. The permanent magnets of the electrical machine are mounted in the steel yoke which is then shrunk into the rotor. The rotor itself is shrunk onto the shaft at the fan inlet. The axial position of the rotor is determined by the magnetic force of the permanent magnets. Additionally, it can be fixed with respect to the plain bearing on the fan outlet using a small spring and a snap ring.

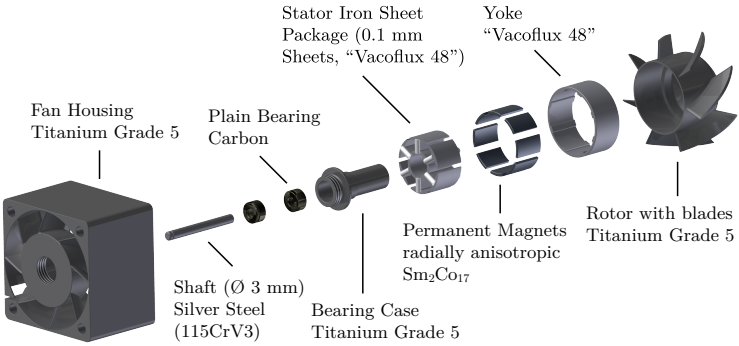


Figure 6.4: Exploded view drawing of high temperature (250 °C / 500 °F) 19'000 min^{-1} BLDC fan for forced air-cooling of advanced automotive power electronics.

6.4.1 Shaft

The shaft is carried by plain bearings and hence, it is very important that the thermal expansion of the shaft is close to that of the plain bearings, which is mainly determined by the bearing case (*cf.* Section 6.4.2). Otherwise for certain temperatures within the operating temperature range, either the bearing clearance has to be chosen very high resulting in high vibrations or the shaft gets stuck in the bearing.

In order to achieve a low coefficient of friction between the shaft and the bearing, the material is required to be harder than 40 HRC. Well suited material is steel (apart from chromium nickel steel and austenitic steel), e. g. chromium, nitrified or hard-chromium plated steel, or hard metal. Not suited is aluminium and its alloys or non-ferrous metal. The roughness of the material should be lower than 1 µm for low friction. Reduction of the surface roughness can be achieved by surface finishing and polishing. The diameter of the shaft is determined by the mechanical load due to unbalance of the rotor, desired vibration reduction, and mechanical resonance of the rotating shaft.

The shaft for this high temperature fan is made of a cylindrical pin, the material of this pin is steel 115CrV3 (also called steel 1.2210). It is hardened to 60±2 HRC and its roughness class is N6, corresponding to a roughness depth of less than 0.8 µm. The coefficient of linear thermal expansion of the material is $13.7 \cdot 10^{-6}$ 1/K for a temperature rise from 20 °C to 300 °C. The diameter of the pin is 3m6, i.e. 3 mm with a fit of

m6 which is in absolute numbers 3 mm $\binom{+0.008}{+0.002}$, and it is cut to a length 27.5 mm, i.e. the length of the shaft is reduced by 0.5 mm compared to the overall length of the fan in order to make sure that no rotating part overlaps the housing.

6.4.2 Bearing

The choice of the bearing is crucial for the fan operation under high temperature conditions and is identified as the main impact factor on the lifetime of the fan. Generally, the bearings can be realized as

- roller bearing,
- static or dynamic air bearing,
- magnetically levitated bearing or
- plain bearing.

Magnetically levitated and air bearings are very complex, costly, and not as compact as plain or roller bearings. Roller bearings need lubrication, and this is usually only used for temperatures below 200 °C. Some special greases are available up to 260 °C and very rarely greases for higher temperatures are applicable.

The more cost effective and easier solution for the high temperature bearing is a plain bearing. Different materials are available for standard conditions, e. g. metal or solid polymer, mono-, bimetallic or sintered bearings, fibre-reinforced plastic composite, bronze or (artificial) carbon. Most materials are not applicable due to the high temperature the bearings are exposed to (the bearing losses make the bearing heat up to even higher temperatures), only bronze and carbon are suitable.

The carbon bearing is the only suited plain bearing for this purpose, if the high rim speed v_r of the shaft is taken into account, which can be calculated using the shaft radius $r_\mathrm{S} = 1.5\,\mathrm{mm}$ to

$$v_\mathrm{r} = 2\pi \cdot n_\mathrm{F} \cdot r_\mathrm{S} = 2\pi \cdot 19'000\,\mathrm{min}^{-1} \cdot 1.5\,\mathrm{mm} = 3.0\,\mathrm{m/s}. \tag{6.11}$$

The dimensions of the bearing are determined by the requirements of the technology, i.e. the difference between the inner and outer radius is usually not less than 3 mm. For applications that have to be highly compact, the difference can be reduced to 2 mm because of the very small shaft diameter of 3 mm. This leads to an outer diameter of 7 mm and the axial length of the bearing is chosen to 4 mm.

The inner diameter of the bearing is given by the outer diameter of the shaft (3m6, i.e. 3 mm $\binom{+0.008}{+0.002}$, which will be reduced by approx. 6 µm by polishing the shaft). The inner diameter is furthermore influenced by the bearing clearance, that is given for dry operation from 0.3% to 0.5% of the shaft diameter. Lower clearances cause higher friction and thus higher losses and lower lifetime, higher clearance values cause higher vibrations. Also, the thermal expansion of the shaft (*cf.* Section 6.4.1) and the bearing has to be taken account when determining the inner bearing diameter. The bearing has a coefficient of linear thermal expansion of $5 \cdot 10^{-6}$ 1/K which is comparably low, but is shrunk into the bearing case at a temperature that is 150 °C higher than the maximum operating temperature and therefore its thermal expansion is given by the bearing case (*cf.* Section 6.4.3).

6.4.3 Bearing Case

The material for the bearing case is required to have a CTE similar to the shaft, because the bearing expands just as its case does and similar to the CTE of the stator iron sheet package that is shrunk onto the casing in order to avoid high thermal stresses.

Furthermore, the material has to be non-magnetic (i.e. should show a relative permeability $\mu_r \leq 1.0$, maintained also after cold working) in order to make sure that the time varying magnetic flux density in the stator is solely conducted by the stator iron sheet package and hence no eddy current losses in the bearing case occur.

The yield strength up to the maximum operating temperature has to be as high as possible because the carbon plain bearings are shrunk into the case. A high Young's Modulus makes sure, that the case even with a wall thickness of 0.5 mm at the inlet bearing is not widened excessively after shrinking in the bearings. This is important because the stator iron sheet package has to be shrunk onto the bearing case after mounting the bearings as the sheet package is not recommended to be exposed to higher temperatures than 400 °C which are necessary for shrinking in the bearing.

Titanium is available in many different alloys. The American organization ASTM International classifies 35 grades of different alloys. The most common grade is Titanium Grade 5 (also named by the material number 3.7164) which fulfills these requirements. Its coefficient of linear thermal expansion is $9.6 \cdot 10^{-6}$ 1/K.

The shape of the casing is defined by its function: It is screwed into the fan housing and thus needs a stopper to control the length of the screwing. The step on the outer diameter is needed to have a stopper for the stator iron sheet package when shrunk onto the case. The outer diameter is with 8 mm as small as possible; the difference between inner radius at the bearing collet and the outer radius of the case is only 0.5 mm. The length of the case is 24 mm, mainly given by the 28 mm overall length of the fan, again 0.5 mm clearance, and 3.5 mm for the shrink fit of rotor and shaft.

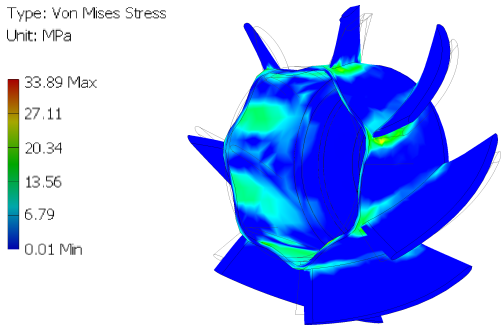
6.4.4 Rotor

The hub (24 mm outside) and blade (37 mm) diameter of the rotor as well as the blade shape are given by the fluid dynamic requirements (*cf.* Section 6.2.4). The clearance between the rotor blades and fan housing is chosen to 0.5 mm due to manufacturing tolerances.

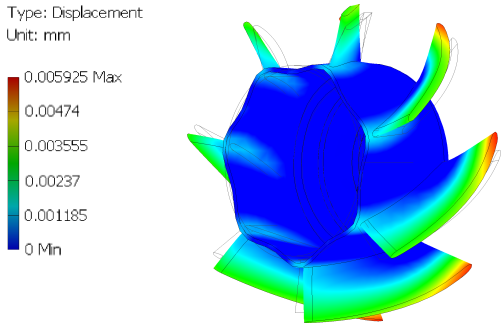
The material for the rotor must have high yield strength at high operating temperatures and a high resistance against fatigue cracks because of the high dynamic load caused by the rotations. The rotor is manufactured of Titanium Grade 5, just as the bearing case. The wall thickness is chosen to 0.5 mm as a trade-off between electrical machine diameter that has to be maximized and mechanical strength at high temperatures. It can be seen from the FEM simulations in Figure 6.5 that the areas of highest mechanical load are at the transitions between the inner cylinder and the blades. The maximum von Mises stress of 34 MPa at a rotational speed of 19'000 min^{-1} is more than a factor of 15 below the yield strength of Titanium Grade 5 at 300 °C. The maximum deformation is less than 6 µm at 19'000 min^{-1} and 300 °C and occurs at the blade tips.

6.4.5 Fan Housing

The stator guide vanes direct the air flow in a more axial direction to increase the efficiency of the heat sink. Their design is also given by the fluid dynamic requirements (*cf.* Section 6.2.4). The material for the stator should have a CTE close to the CTE of the bearing case in order to have a similar thermal expansion when the bearing case is screwed into the housing and hence, the bearing case is also made of Titanium Grade 5. For easier manufacturing of the housing, it is produced in two



(a)



(b)

Figure 6.5: FEM simulation of rotor (a) von Mises stress and (b) displacement at a rotational speed of 19'000 min^{-1} and an ambient temperature of 300 °C. A safety margin of more than 15 for the maximum stress is included for the designed Titanium Grade 5 rotor.

parts: The first part containing the guide vanes shows an axial length of 7 mm, the second part contains the bore for the rotor. These two parts are laser beam welded, as can be seen in Figure 6.1(b).

6.5 Summary

It is shown how the pressurization of a fan decreases at elevated temperatures and how the rotational speed can be increased to 19'000 min^{-1} to compensate this decline. Then, special focus is put on the design of

the integrated BLDC machine for an ambient temperature of 250 °C, including magnetic material selection (Sm_2Co_{17} permanent magnets for the rotor and FeCo sheets for the stator package) and choice of ceramic coated CuNi windings introducing further constraints due to their minimum bending radius. The mechanical design of the fan for 250 °C operation and rim speeds up to 180 $^{m}/_{min}$ with plain bearings is conducted. The selection of the materials for the different fan components has been done based on the evaluation of the material stresses, the material strength at 250 °C, and the thermal expansion in an operating temperature range of almost 300 K, from -40 °C to 250 °C.

In Chapter 8 (Section 8.2), experimental results are given and are in good agreement with the theoretical considerations: The fluid dynamic characteristics, the power consumption, the voltage and current waveforms at 25 °C and an elevated temperature of 250 °C as well as the acoustic noise generation of the fan are measured.

Chapter 7

High Temperature Current Measurement

7.1 Overview over Current Measurement Concepts

For a high-quality control of a power electronic converter, ideally the current is measured precisely, robust against dynamic changes of the potential of the current carrying conductor, without any time lag, and with a high bandwidth. To avoid a routing of the load current flow through the thermally shielded signal electronics part, the current should advantageously be directly measured at the power semiconductor packages, and hence the measurement circuit needs to withstand ambient temperatures of up to 250 °C. For the signal electronics of the current measurement system, an ambient temperature capability of around 120 °C is sufficient if the control of the current measurement system can be separated geometrically from the actual measurement at the power semiconductors.

In recently published high temperature converter systems like [123], the current is measured using shunts that operate at 250 °C. The analog-digital converter required for the digital control of the drive inverter can placed in a thermally shielded signal electronics box operating at 120 °C (*cf.* Section 5.4). Shunts offer an easy and cheap measurement of both dc and ac currents (providing the option of monitoring the dc current

drawn from the battery and the variable frequency ac output currents shaped by the inverter of an HEV using the same technology), but they are not galvanically isolated and thus their voltage signal must be isolated if the shunt potential can be different from that of the signal processing electronics. Additionally, shunts require for accurate operation over large temperature ranges a temperature compensation due to the temperature change of the resistance. Furthermore, the voltage measured at their terminals can easily be distorted by EMI occurring in switch mode power electronic converters, especially when mounted close to the power semiconductor switches. If the measured current ranges from small to very large values, the resistance has to be chosen sufficiently high so that small currents still lead to a measurable voltage while at the same time, large currents should not lead to high power losses and thus even higher temperatures of the resistor.

Alternative current measurement concepts are shown in Figure 7.1. For high ambient temperatures of 250 °C, Hall effect, magnetoresistive, and magnetoptical sensors cannot be used due to individual technological temperature limits. The concepts utilizing the magnetic flux in a coil or magnetic core caused by the current to be measured are generally more suitable for higher operating temperatures as the technology involved (windings and a ferro- or ferrimagnetic core) is available for these temperatures. However, some options suffer from other disadvantages: Rogowski coils and current transformers can only measure ac currents down to a lower cut-off frequency due to their operating principle based on the change of the magnetic flux. At low vehicle and thus rotational speeds of the electrical machine, the frequency of the output current in the range of less than 1 Hz is likely to be below the lower cut-off frequency of the coil or the transformer. A Fluxgate sensor can generally be used for dc and ac current measurement at high temperatures, but the upper cut-off frequency of the sensor is very limited by the control of the saturable inductor sensing the magnetic flux of the gapped core.

In this chapter, the novel current measurement concept is based on a "Bidirectionally Saturated Current Transformer" is presented, which allows fast measurement also of sinusoidal currents at high ambient temperatures of 250 °C for power electronic converters with medium switching frequencies and nearly sinusoidal output currents (e.g. due to a high load inductance). The specifications are listed in Table 7.1. The introduced concept shares some common features with the dc current transformer that is known for many years [124–126] but to make

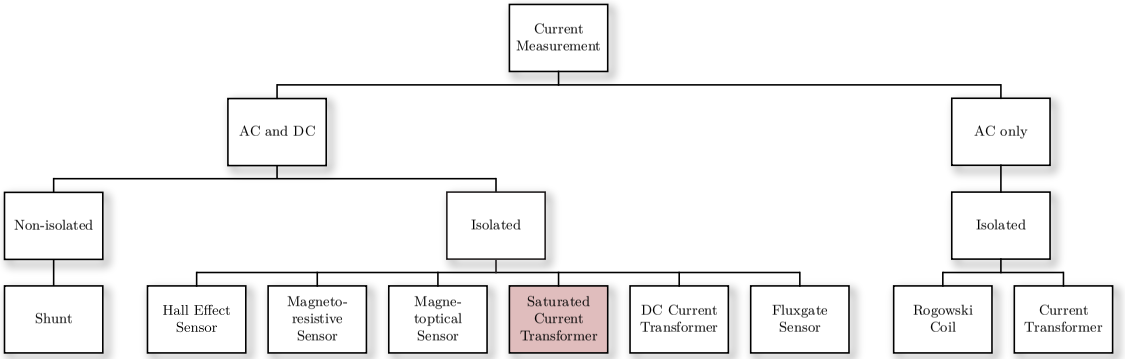


Figure 7.1: Overview of state of the art current measurement concepts: For ac and dc current measurement in high temperature applications, currently often shunts are used. Their measurement signal is not galvanically isolated, suffers from a temperature dependency and can easily be distorted by EMI. For high ambient temperatures of 250 °C, Hall effect, magnetoresistive, and magnetoptical sensors cannot be used due to individual technological temperature limits. Rogowski coils and current transformers can only measure ac currents down to a lower cut-off frequency. The concepts utilizing the magnetic flux in a coil or magnetic core caused by the current to be measured are generally more suitable for higher operating temperatures. The new concept introduced in this dissertation is the "Saturated Current Transformer", that is able to measure dc and sinusoidal ac currents up to 1 kHz and 50 A at an ambient temperature of 250 °C.

Table 7.1: Specifications of the current measurement system

Bidirectionally Saturated Current Transformer		
Current Measurement Range	-50 .. 50	A
Sinusoidal Current Frequency Range	0 .. 1	kHz
Min. Measurement Frequency	50	kHz
Max. Operating Temperature	250	°C
Outer Diameter[1]	6.5	mm
Inner Diameter[1]	2.9	mm
Height[1]	5.5	mm

[1] Including secondary winding

it suitable for measuring sinusoidal currents with frequencies of up to 1 kHz, it shows a modified magnetic design and is directly hardware controlled enabling significantly faster measurements than the usual dc measurement concepts and thus allowing to measure ac as well. The physical values measured to determine the current are also different to previously published concepts in order to eliminate any influence of the temperature [127]. In the next Section 7.2, the measurement principle, the differences to known concepts based on current transformers and the guidelines for selecting and dimensioning a magnetic core for this measurement system are shown in detail. The realization and experimental verification of the proposed measurement system is presented in Section 7.3 and Chapter 8, Section 8.3, respectively.

7.2 Measurement System

7.2.1 Measurement Principle

The basic physical setup of the current measurement system is shown in Figure 7.2(a). The current i_p which is to be measured is fed through a toroidal core made of ferro- or ferrimagnetic material with N_p primary turns. Provided the magnetic permeability μ of the core is by orders of magnitude higher than that of the surrounding medium (e.g. air), the unknown primary current i_p that is to be measured causes a magnetic

field strength that is given by

$$H_\mathrm{p} = \frac{i_\mathrm{p} \cdot N_\mathrm{p}}{l_\mathrm{m}} \tag{7.1}$$

where l_m denotes the average length of the magnetic path in the core. The core radius and the saturation magnetic field strength H_sat of the core material is chosen so small that the minimum current $i_\mathrm{p,min}$ that has to be measured leads to saturation of the core, i.e. to a value of $H_\mathrm{p} > H_\mathrm{sat}$.

As can be seen from Figure 7.2(b), H_p can be calculated using the differences ΔH_1 and ΔH_2 in the magnetic field strength from H_p to the coercive magnetic field strength H_c,

$$H_\mathrm{p} = \frac{\Delta H_1 + \Delta H_2}{2}. \tag{7.2}$$

The toroidal core also carries a secondary winding with N_s turns, driven by a full bridge (*cf.* Figure 7.3) causing a secondary current i_s and a secondary magnetic field strength H_s in the core. The H-bridge is controlled such that the full hysteresis loop is traversed within one pulse period of the H-bridge by the magnetic field strength H_s which is superimposed on H_p. During traversing the hysteresis loop, the currents i_s1 and i_s2 corresponding to $-H_\mathrm{c}$ and H_c, respectively, are measured using the shunt R_S and with

$$\begin{aligned} \Delta H_1 &= \frac{i_\mathrm{s1} \cdot N_\mathrm{s}}{l_\mathrm{m}} \\ \Delta H_2 &= \frac{i_\mathrm{s2} \cdot N_\mathrm{s}}{l_\mathrm{m}}, \end{aligned} \tag{7.3}$$

i_p can be finally calculated as

$$i_\mathrm{p} = \frac{N_\mathrm{s}}{N_\mathrm{p}} \cdot \frac{i_\mathrm{s1} + i_\mathrm{s2}}{2}. \tag{7.4}$$

Hence, the magnetic setup should be viewed more as sensing element that senses the primary magnetic field H_p, and thus the current i_p that is to be measured, by the use of a secondary magnetic field H_s caused by an impressed secondary current i_s than as an actual current transformer.

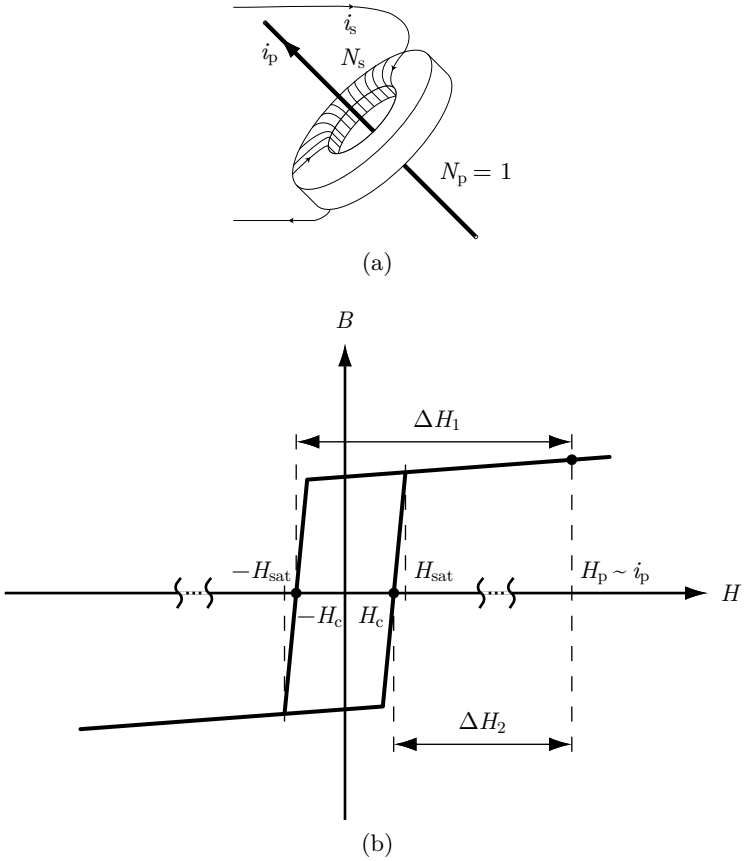


Figure 7.2: (a) Basic physical setup of the bidirectionally saturated current transformer: The (primary) current i_p to be measured is fed through a toroidal core that also carries a secondary winding. (b) Basic measurement principle: The primary current is determined using the mean value of the secondary currents that are needed to reach the coercive magnetic field strengths $\pm H_c$ of the hysteresis loop.

In Figure 7.4(a) and (b), the idealized traversing of the hysteresis loop is shown in detail. The single phase inverter in Figure 7.3 starts to apply the dc-link voltage V_{CC} to the secondary winding on the toroidal

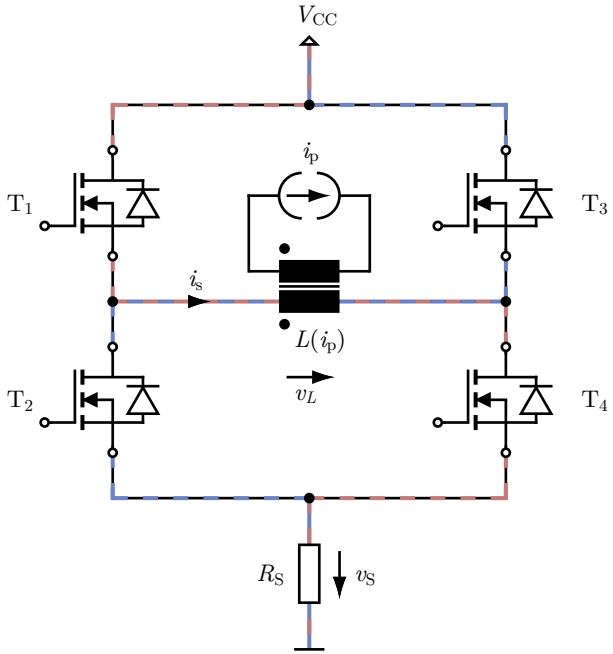


Figure 7.3: Circuit diagram of the current measurement setup: The bidirectionally saturated current transformer is magnetized by a primary current i_p. The secondary winding on the toroidal core of the transformer is connected to an H-bridge and the secondary current i_s is measured by a shunt R_S. The colored current paths correspond to a section of the current waveform shown in Figure 7.4(b).

core at t_0. Once the core is saturated by i_p and thus has a relative permeability close to unity, the current i_s will rise fast.

Assuming the direction of i_s leads to a flux that is opposing the flux caused by i_p, the increase will become less steep once the sums of H_p and H_s add up to a value in between $-H_c$ and H_c which happens at time instant t_1. At t_2, $i_s(t = t_2) = i_{s1}$ needs to be measured. With a further increase in i_s, the core will reach saturation again at t_3, leading to a steep increase in i_s until a predefined current limit is reached and the voltage applied to the secondary winding is reversed at t_4 and the hysteresis loop is traversed in the opposite direction,

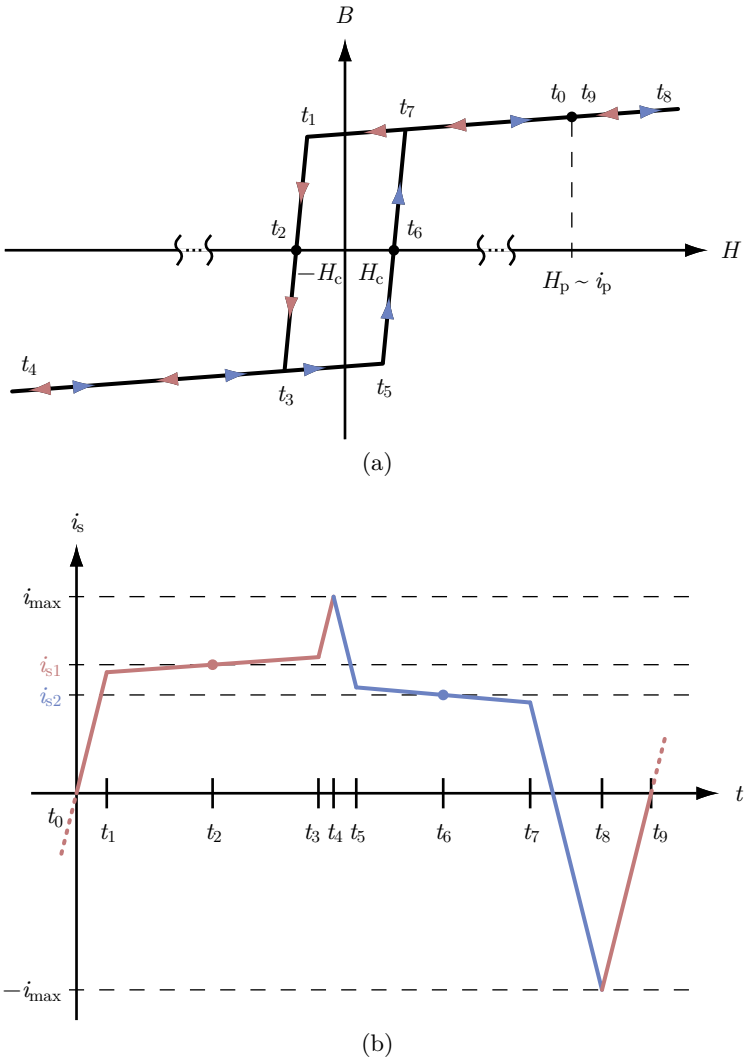


Figure 7.4: Traversing the $B(H)$ hysteresis loop by proper modulation of the H-bridge connected to the secondary side as shown in Figure 7.3: The different operating points of the bidirectionally saturated current transformer within one pulse period of the H-bridge are shown on the (a) hysteresis loop and (b) secondary current waveform.

measuring $i_s(t = t_6) = i_{s2}$ and having $i_s(t = t_9) = 0$ at t_9 where the switching period of the H-bridge starts again.

If the previous assumption that H_p and H_s are in opposite direction is wrong, the core will be saturated even further in the direction of H_p. Thus the current limit of i_s (either i_{max} or $-i_{max}$) will be reached without desaturation of the core and thus also without any measurement of the secondary current and the H-bridge reverses the voltage so that the measurement cycle can start as described previously.

It can be seen in Figure 7.4(b) that the time difference between t_7 and t_5 is smaller than between t_3 and t_1. The reason for this fact is illustrated in Figure 7.5: When V_{CC} is applied to the secondary winding such that i_s rises (*cf.* Figure 7.5(a)), the voltage drop caused by i_s across the parasitic resistances (drain-source on-resistance $R_{DS,on}$ of the MOSFETs in the H-bridge and the winding resistance R_{cu}) and across the shunt R_S reduces the voltage v_L applied to the secondary winding. Hence, it takes longer to build up the same inductor current, than it takes to make the inductor current decrease by applying V_{CC} in the opposite direction. This is true because i_s still flows in the same direction for both cases, but in the latter case, the voltage drop across the on-resistances of the other pair of switches and across R_S is added to V_{CC} and only the voltage drop across R_{cu} reduces v_L and thus the slope of i_s between t_1 and t_3.

This phenomenon can also be explained by the following consideration: The shunt is placed in the dc-link of the H-bridge, and the load is purely inductive, if losses are neglected. Hence, the current through (or voltage across) the shunt should be free of a direct component. The second lowest waveform in Figure 7.10 shows the shunt voltage for the secondary current as in Figure 7.4(b). It can be seen, that the direct component in the shunt voltage v_S is introduced only by the difference in time that is spent in the region where the core is not saturated, and is finally caused by the losses in the parasitic resistances.

7.2.2 Major Differences to Existing Current Transformer Concepts

Measuring the secondary current at $\pm H_c$ is a significant difference to [125] where the secondary current is measured when the core starts to saturate. The latter is difficult to realize with typical analog-digital-converters as the current rises very fast once the core is saturated.

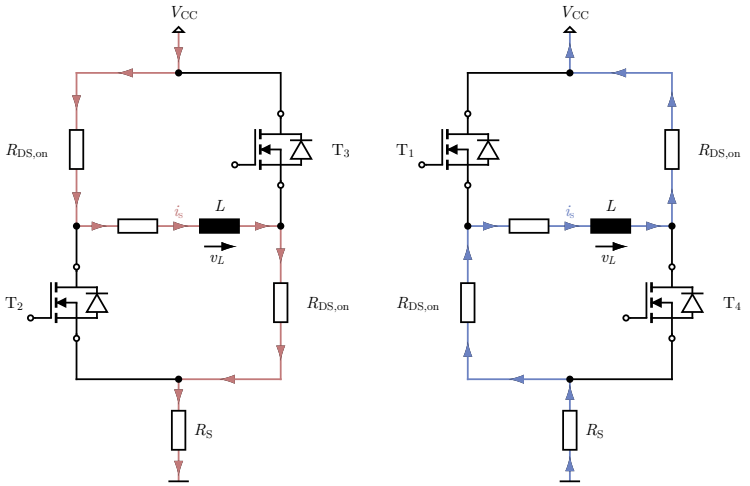


Figure 7.5: Difference in inductor voltage depending on the switching state of the H-bridge: For a given direction of the primary current i_p, the direction of the secondary current i_s is independent of the switching state of the H-bridge, when the core is not saturated (i.e. during the time interval between t_1 and t_3 as well as between t_5 and t_7). Hence, in one switching state (a), the voltage v_L applied to the inductor is V_{CC} *minus* the ohmic voltage drops occurring due to $R_{DS,on}$, R_S, and R_{cu} and in the other switching state (b) v_L is the negative *sum* of V_{CC} and the voltages over $R_{DS,on}$, R_S, and R_{cu}. This means that the absolute voltage applied to the inductor is larger between t_7 and t_5 than between t_3 and t_1 and hence, the time interval between t_7 and t_5 is smaller than between t_3 and t_1 in Figure 7.4.

How the crucial task of finding the right point in time to sample the secondary current for the measurement principle presented here can be tackled, is shown in Section 7.3.4.

In [125], it is proposed to calculate the primary current by measuring the time to saturation. The saturation flux density, which shows a significant temperature dependence for typical ferro- or ferrimagnetic core materials (*cf.* e.g. the hysteresis loop in Figure 7.7), is needed in the resulting equation for i_p though. It can be seen from Equation (7.4) that the measurement of i_p in the concept shown here is invariant against

temperature changes of the core as N_s and N_p are temperature independent.

For an ideally lossless core material, the area enclosed by the hysteresis loop would be zero leading to $H_\mathrm{c} = 0$ and the difference in $i_{\mathrm{s}1}$ and $i_{\mathrm{s}2}$ would vanish. In reality, measuring $i_{\mathrm{s}1}$ and $i_{\mathrm{s}2}$ to find the mean value can lead to a more precise calculation of i_p using Equation (7.4). Especially for high bandwidth and/or high excitation frequencies, this is particularly important due to $|H_\mathrm{c}|$ increasing with frequency. Taking the width of the hysteresis loop into account when calculating the primary current is one important difference to [126].

7.2.3 Transformer Core

The choice of the transformer core material and design is crucial for the fast and precise operation of the current measurement system at ambient temperatures of 250 °C. It must be made sure, that the important material parameters mentioned in this section are assessed in the whole temperature range from -40 °C to temperatures above 250 °C as the core heats up to temperatures higher than the ambient temperature due to the losses occurring when traversing the hysteresis loop.

Relative Permeability μ_r

As shown in Section 7.2.1, the current is determined by measuring the secondary current i_s at time instants t_2 and t_6, when the magnetic field strength in the core equals $\pm H_\mathrm{c}$. The increase in secondary current around H_c is small because the core is not saturated, hence its inductance value

$$L = \mu_\mathrm{r}\mu_0 N_\mathrm{s}^2 \cdot \frac{A_\mathrm{m}}{l_\mathrm{m}}, \tag{7.5}$$

where μ_0 is the magnetic constant and A_m is the cross section of the core, is proportional to the relative permeability μ_r. Hence, the slope of the secondary current,

$$\frac{\mathrm{d}i_\mathrm{s}}{\mathrm{d}t} = \frac{v_L}{L}, \tag{7.6}$$

can be reduced by increasing the relative permeability μ_r. This helps to decrease the measurement error, which is introduced if i_s is measured slightly too early or too late.

Coercive Magnetic Field Strength H_c

In many other current measurement concepts utilizing two-winding inductors, the coercive magnetic field strength H_c causes a measurement error [126]. As pointed out in Section 7.2.2, this error is compensated in the presented concept by measuring i_{s1} and i_{s2}. Still, $|H_c|$ should be chosen as small as possible in order to reduce the losses and thus the self-heating of the core when traversing the hysteresis loop.

Saturation Magnetic Field Strength H_{sat}

As explained in Section 7.2.1, the core needs to be saturated for a precise measurement of the primary current. Hence, H_{sat} should be as small as possible as can be shown by

$$i_p > i_{p,min} = \frac{l_m}{N_p} \cdot H_{sat}. \tag{7.7}$$

Saturation Flux Density B_{sat}

B_{sat} influences the time needed to traverse the full hysteresis loop and thus the measurement frequency f according to

$$f = \frac{1}{\Delta t} = \frac{v_L}{\Delta B A_m N_s}. \tag{7.8}$$

Assuming that it is not desired to provide a separate dc-dc converter for the current measurement system, v_L is given by V_{CC}, i.e. by the available voltage levels of the signal electronics. (Here, a value of $V_{CC} = 12\,V$, as typical for the automotive industry, is chosen.) Hence, for a fast current measurement, a small B_{sat} is desirable. The measurement frequency can also be adjusted using the product $A_m N_s$.

Number of Primary Turns N_p

It is desirable to design the measurement system such, that one primary turn $N_p = 1$ is sufficient as this allows to position the magnetic core easily on the pin of a power semiconductor package connected to a phase output (*cf.* Figure 7.6(a)).

Number of Secondary Turns N_s

For one primary turn, the number of secondary turns

$$N_\mathrm{s} = \frac{i_\mathrm{p}}{i_\mathrm{s}} \tag{7.9}$$

determines the level of the secondary current that is measured using the shunt R_S and needs to be switched by the H-bridge.

Core Cross Section A_m

A_m is inversely proportional to the measurement frequency as can be seen from Equation (7.8) and hence should be chosen as small as manufacturing issues and the minimum required mechanical strength allow.

Length of the Magnetic Path l_m

According to Equation (7.7), the length l_m of the magnetic path is directly proportional to the minimum current that can be measured and hence should be chosen as small as possible. Lower limits are introduced by the space consumed by the primary current carrying conductor and the secondary winding and by the required mechanical strength of the core.

7.3 Realization of Measurement System

Having presented the working principle and important design parameters of the current measurement, the realized measurement system (*cf.* Figure 7.6) is described in the following. The specifications of the realized systems include in addition to the temperature levels already mentioned in Section 7.1 a current measurement range from -50 A to 50 A and a measurement (sampling) frequency of at least 50 kHz for sinusoidal currents with up to 1 kHz fundamental frequency (*cf.* Table 7.1). The number of secondary turns is chosen to $N_\mathrm{s} = 50$ to limit the current in the H-bridge to 1 A. This allows a reasonable silicon chip size of the switches even at an ambient temperature of 120 °C (here, the two half-bridges are packaged each in a small outline package with eight pins (SOP-8) having an upper junction temperature limit of 175 °C). Furthermore, it reduces the wire diameter needed for the secondary winding and thus helps to achieve a low l_m.

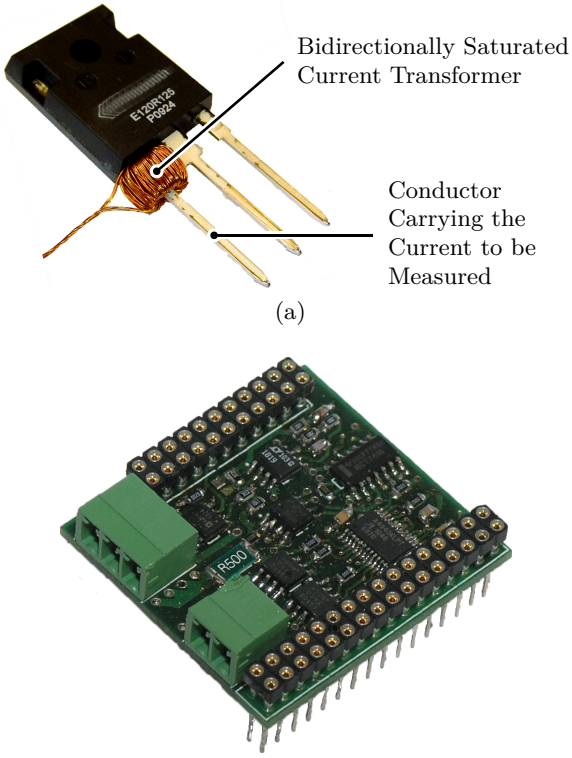


Figure 7.6: (a) Photograph of the bidirectionally saturated current transformer mounted on a discretely packaged SiC power semiconductor switch. (b) Photograph of the PCB with signal and low power electronics to magnetize the current transformer core from its secondary side. The PCB also contains the connectors to the current transformer and to the digital control platform of the overall converter system which employs the system for current measurement.

7.3.1 Choice of Core Material

The nanocrystalline material "Vitroperm 500F" manufactured by Vacuumschmelze is chosen for this example design as it features a high relative permeability up to $\mu_r = 150'000$, a low coercive and saturation magnetic field strength as well as a comparably high temperature

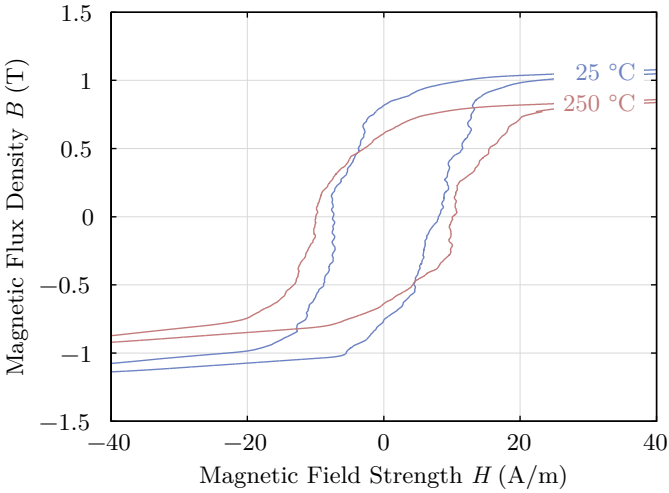


Figure 7.7: Digitally low-pass filtered hysteresis loop of "Vitroperm 500F" measured at 25 kHz and 25 °C and 250 °C using a "T60006-L2009-W914" core [128]. The material has been chosen because of a high μ_r of up to 150'000, a low coercive and saturation magnetic field strength as well as a high operating temperature capability of up to 300 °C and a comparably high temperature invariance of these magnetic parameters. Furthermore, the commercial cores available are tape wound and hence, the core dimensions can be easily adjusted to meet the needs of the experimental prototype of the bidirectionally saturated current transformer.

invariance of these magnetic parameters which is of great importance when designing a measurement system with a temperature difference during operation of more than 300 K (-40 °C to 250 °C ambient temperature plus self-heating due to losses). These characteristic values can be derived from Figure 7.7 showing the hysteresis loop measured at 25 kHz (which matches the excitation frequency of the hysteresis loop for a measurement (sampling) frequency of 50 kHz) and 25 °C and 250 °C using a "T60006-L2009-W914" core [128].

Even though the Curie temperature T_C of this material is higher than 600 °C, the manufacturer specifies an upper operating temperature limit of 155 °C for the "Vitroperm" cores. This is primarily due to the epoxy coating or plastic casing of the cores. At temperatures above

300 °C, which are still significantly below T_C, the material starts to loose its nanocrystalline structure resulting in derated performance especially with respect to eddy current losses and hence, it has to be made sure, that the material temperature does not rise significantly above 300 °C for a longer period of time.

7.3.2 Choice of Core Dimensions

The smallest commercially available "Vitroperm 500F" core ("T60006-L2009-W914", which has already been used for measuring the hysteresis loop in Figure 7.7), shows a magnetic path length of $l_m = 26\,\text{mm}$ and a cross section of $A_m = 6\,\text{mm}^2$. This leads to an undesirably high minimum current that can be measured and a relatively long time needed for traversing the hysteresis loop, as can be seen from Equation (7.7) and Equation (7.8), respectively.

However, the cores in the plastic casing can be opened and the tape wound core can be unwound and then re-wound with a smaller radius and less turns (leading to a lower l_m and A_m). For rewinding, the number N_t of tape turns can be calculated using Equation (7.8) to

$$N_t = \frac{A_m}{h_t d_t} = \frac{\Delta t v_L}{h_t d_t \Delta B N_s} = 21 \tag{7.10}$$

for $v_L \approx 11\,\text{V}$ (V_{CC} is reduced by ohmic voltage drops), $\Delta B = 2.3\,\text{T}$ (*cf.* Figure 7.7) and $\Delta t = 20\,\mu\text{s}$ (leading to a measurement frequency of 50 kHz due to the sampling scheme described in Section 7.3.4), a height of the tape of $h_t = 4.4\,\text{mm}$, and a thickness of $d_t = 20\,\mu\text{m}$. This results in $A_m = 1.9\,\text{mm}^2$ and $l_m = 13.8\,\text{mm}$ and leads with Equation (7.7) to a minimum measurable current of $i_{p,min} = 0.28\,\text{A}$ for $H_{sat} \approx 20\,\text{A/m}$ as a worst case scenario at 250 °C according to Figure 7.7.

7.3.3 Signal Electronics

The structure of the signal electronics of the realized current measurement system is shown in Figure 7.8: A PCB for the analog part containing the H-bridge (two Vishay Intertechnology "SI4946BEY" bridge legs [129]) and its gate drivers (Allegro Microsystems "A4940" [130]) is used to excite the core from the secondary side and a digital signal processor (DSP) mounted on a separate PCB samples at certain points in time (*cf.* Section 7.3.4) the scaled (to fit the input voltage range of

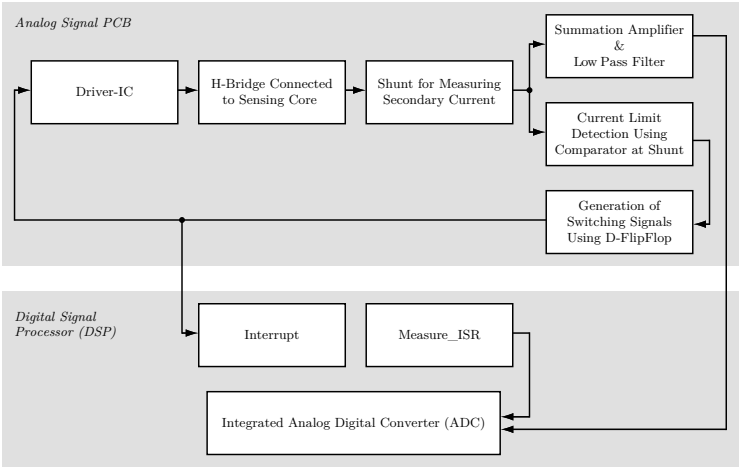


Figure 7.8: Signal flow diagram for the analog control of the current measurement system and for the measurement routine within a DSP.

the analog-digital-converter (ADC) of the DSP) and filtered shunt voltage v_S. The filtering of v_S is done by an active second order low pass filter and is essential as measurement noise will otherwise cause false switching signals to be generated by the comparator (*cf.* next paragraph). The voltage v_S itself and its scaled values (which correspond to the voltage v_{ADC} that is later filtered and applied to the ADC) are shown at the bottom of Figure 7.10.

The switching signals (input signals of the gate driver) need to be generated with minimum delay after the core reaches saturation as the current rises very fast once it is saturated. Hence, they are not generated by the DSP but by measuring the shunt voltage v_S and evaluating this voltage using a current limit detection circuit depicted in Figure 7.9: The shunt voltage is compared to a reference voltage at a comparator. ($V_{ref1} = 0.64\,\text{V}$ is chosen for this design, corresponding to a current through the $0.5\,\Omega$ shunt of 1.28 A making sure that even with a maximum primary current of 50 A the secondary current can saturate the core in the direction opposing the primary current with $N_s = 50$ turns.) The output of the comparator is fed to the clock input of a D flip-flop, the inverted output of which is connected to the D input of the flip-flop. Hence, every time the shunt voltage increases above V_{ref1},

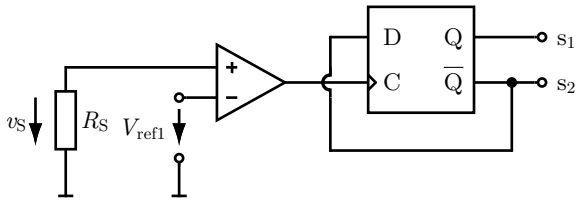


Figure 7.9: Generation of the switching signals for the H-bridge by comparing the shunt voltage v_S with a reference voltage V_{ref1}: The output of the comparator (National Semiconductor "LM360") is fed to the clock input of a D flip-flop (Texas Instruments "CD74HCT74M"), the inverted output of which is connected to the D input of the flip-flop.

the rising clock edge makes the flip-flop toggle the output which is used as the switching signals for the n-MOSFET pairs T_1 and T_4 as well as T_2 and T_3.

7.3.4 Measurement Algorithm

The correct time instants t_2 and t_6 to measure the secondary currents i_{s1} and i_{s2} (*cf.* Figure 7.4(b)), i.e. to sample the shunt voltage v_S, are determined by the interrupt service routine "Measure_ISR", which is started by an interrupt generated by the output toggling of the flip-flop. Right at the start of the routine, a timer is re-started to measure the time interval $\Delta t_i, 1 \leq i \leq 6, i \in \mathbf{N}$, between two consecutive interrupts (*cf.* Figure 7.10). The interval that has been measured two interrupts before is cut in half to determine when to sample v_S. E.g. in the interval Δt_3 in Figure 7.10, the secondary current is measured when $^{\Delta t_1}/_2$ has elapsed. Hence, a measured current value can be provided twice per switching cycle of the H-bridge, e.g. twice per bidirectional traversing of the hysteresis loop. Furthermore, at the beginning of the current measurement (e.g. during start-up of the power electronic converter), the routine needs 1.5 pulse periods of the H-bridge ($\approx 50\,\mu s$) to initialize the variables where the counter values are stored in.

This way of determining when to measure the secondary current relies on two assumptions, which are validated with experimental results showing the measurement error in Figure 8.10 in Section 8.3:

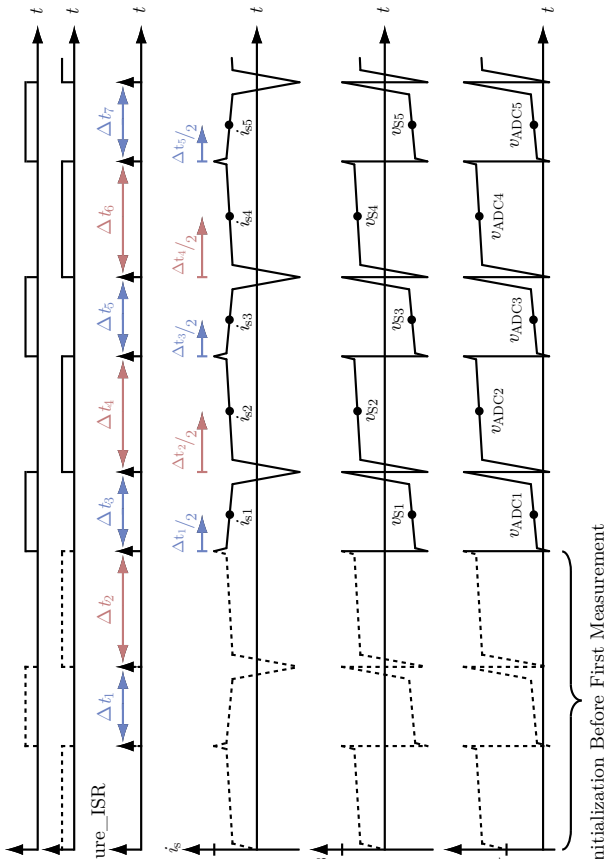


Figure 7.10: The switching signals s_1 and s_2 generated by the circuit shown in Figure 7.9 and the interrupts triggering the DSP routine "Measure_ISR" to start the counters needed to determine the correct point in time when to sample the level-adjusted shunt voltage applied to the analog-digital-converter of the DSP are shown. Furthermore, the secondary current i_s of the bidirectionally saturated current transformer, the shunt voltage v_S and the voltage $v_{ADC,bf}$ applied to a low-pass filter and then to the ADC, are depicted.

First, it is assumed that the time intervals when the core is saturated, i.e. from t_0 to t_1, from t_3 to t_5 and from t_7 to t_9 in Figure 7.4(b) are small compared to the intervals t_1 to t_3 and t_5 to t_7 when the core is not saturated. This is fulfilled if the employed core shows a high relative permeability (*cf.* Section 7.2.3). This allows also to use standard clocks and timers in the DSP as small inaccuracies in the timing will not introduce large errors. This is the main reason, why the switching signals are generated directly by the signal electronics (*cf.* Section 7.3.3) and not by the DSP.

Second, this way of determining the points $(\pm H_\mathrm{c}, 0)$ in the H-B-plane works precisely only if the current does not change significantly within the interval between 3 interrupts. As an interrupt occurs in the current design every 7 µs to 14 µs and the maximum frequency of the sinusoidal currents that are to be measured is 1 kHz, only very small errors are introduced (*cf.* Figure 8.10 in Section 8.3).

7.4 Summary

The measurement principle of a novel current measurement concept called "bidirectionally saturated current transformer", that is able to measure dc and sinusoidal ac currents up to 1 kHz and 50 A at an ambient temperature of up to 250 °C, is explained in detail.

The important design guidelines for choosing a core material (high μ_r, low H_c, H_sat, B_sat) and the magnetic design (high N_s, low N_p, A_m, l_m) are derived and an experimental prototype is designed accordingly. The required signal electronics consisting of an current limit detection that controls the H-bridge, which the secondary winding is connected to, and a circuit with a low-pass filter that also adjusts the level of the shunt voltage which is sampled by the analog-digital-converter of a DSP. In Chapter 8 (Section 8.3), measurements verifying the proposed concept are provided and show a relative error of 2.6% and less than 0.5% after calibration even at 250 °C.

Chapter 8

Experimental Analysis

8.1 AC-Coupled Gate Driver for Normally-Off SiC JFETs

The gate driver circuit presented in Chapter 4 has been tested in a half-bridge inductive test circuit with a SiC freewheeling diode as shown in Figure 8.1(a) and switching patterns as exemplarily shown in Figure 8.1(b) to validate the theoretical considerations.

The switching waveforms for turn-on and -off are shown in Figure 8.2. The switching times are 34 ns for turn-on and 24 ns for turn-off in Figure 8.2(a) and Figure 8.2(b), respectively. Hence, the novel ac-coupled gate driver circuit enables similarly fast switching performance of the normally-off SiC JFET as has been published for existing two-stage [81–85] and ac-coupled [86, 88] gate drivers. Thus, the gate driver leads to switching losses of the JFET in the same range for a comparable (especially with respect to the parasitic capacitances) system layout, but does not suffer from shortcomings in terms of circuit complexity and part count (for the two-stage gate drivers) and frequency or duty cycle limitation (as given for the existing ac-coupled gate drivers). The high power loss in the dc resistor R_{dc}, that all existing gate drivers suffer from, is avoided for this topology. This remains true even if a high gate current that is needed for operation of the device with lowest possible on-resistance is supplied to the JFET.

Two of the most important properties of the novel gate driver, the negative gate bias during the off-state and the significantly increased

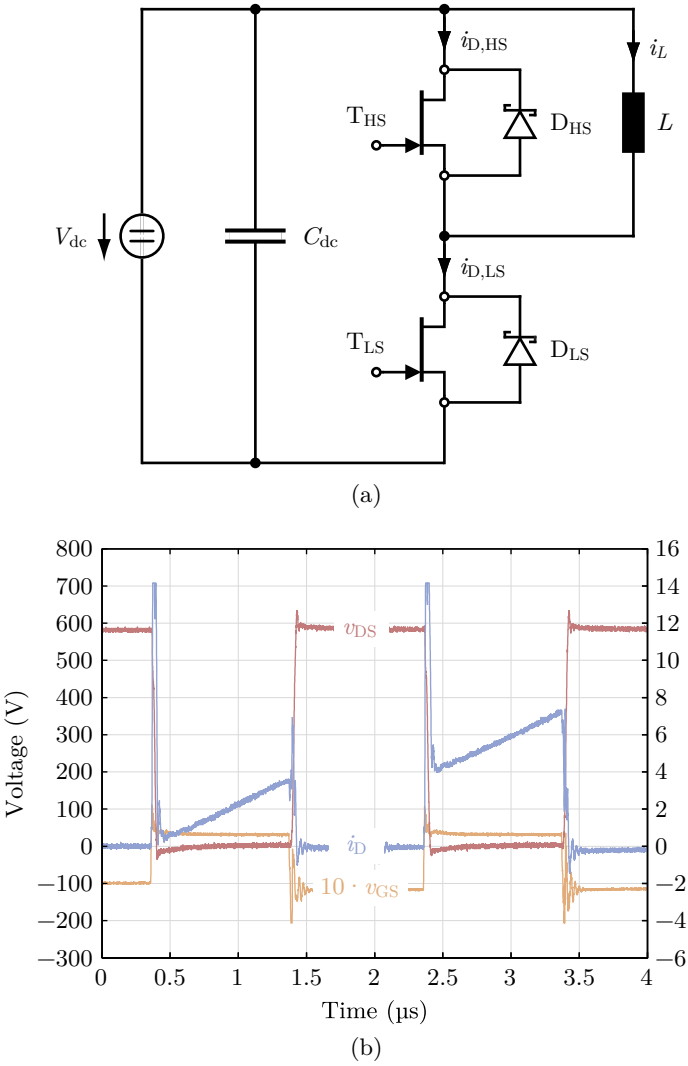
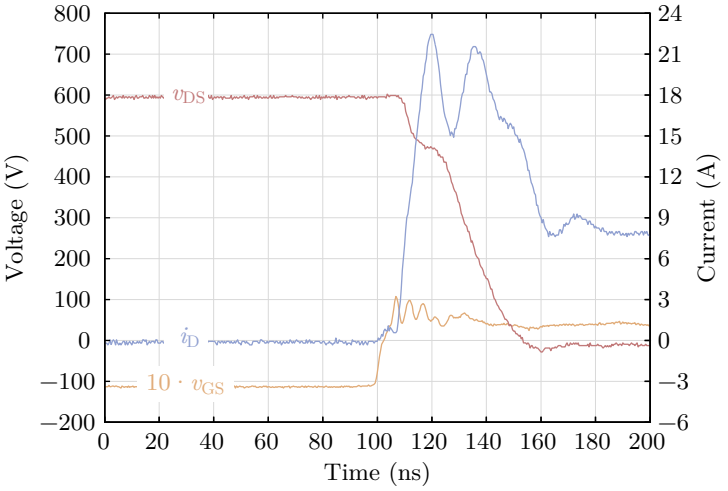
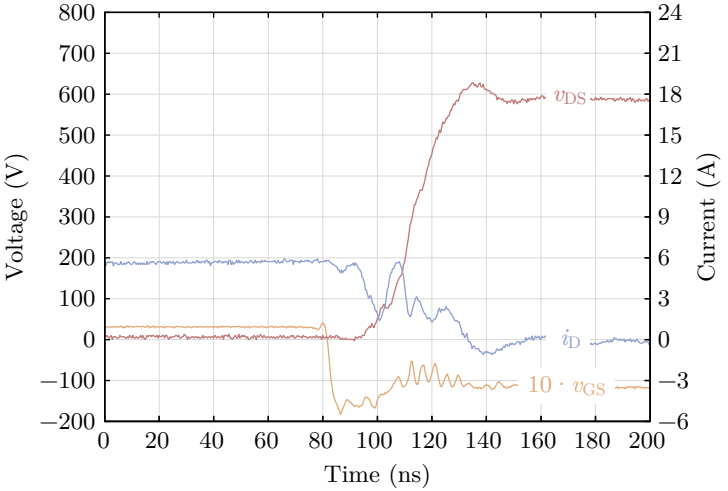


Figure 8.1: (a) Test setup for the validation of the gate driver circuit: Half-bridge connection of two 1200 V 40 A normally-off SiC JFETs with antiparallel freewheeling diodes (SiC Schottky Barrier Diodes Infineon IDH15S120 [94]) and an inductive load. (b) Time behavior of the drain current, drain-source and gate-source voltage of the low-side switch.



(a)



(b)

Figure 8.2: JFET switching transients with the proposed gate driver in a test circuit as shown in Figure 8.1. (a) Turn-on and (b) turn-off are finished after 34 ns and 24 ns, respectively. The gate-source voltage waveform shows the negative bias during the off-state and the significantly increased gate voltage during the switching transients.

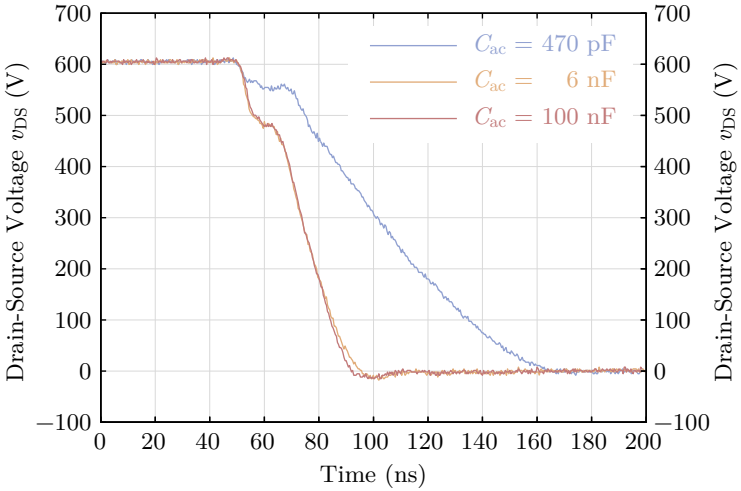


Figure 8.3: Drain-source voltage of T_{LS} during turn-on for different values of C_{ac} (*cf.* Figure 4.7). As expected, a smaller value than $C_{ac} = 6\,\text{nF}$ leads to a significantly slower turn-on while an increase does not yield a significant gain in switching speed.

gate-source voltage during the switching transients, can also be observed in Figure 8.2. As the gate-source voltage is measured directly at the TO-247 package, the inductive voltage drop resulting from the PCB tracks and the 10 mm long pin of the package reduces the measured gate-source voltage slightly to less than 15 V.

Figure 8.3 and Figure 8.3 show two examples of the experimental verification of the theoretical considerations and dimensioning in Section 4.3. In Figure 8.3 the dimensioning of C_{ac} is proven by measuring the drain-source voltage during turn-on of the JFET for different values of C_{ac}. As derived in Section 4.3.7, an increase in capacitance beyond the calculated value of $C_{ac} = 6\,\text{nF}$ yields only a slightly faster turn-on (especially at the end of the turn-on transient, when the voltage across a larger C_{ac} does not increase as fast as across a smaller C_{ac}), but does not make a relevant difference. The consideration, that a reduction significantly below 6 nF leads to a considerable extension of the switching time, is also clearly shown.

The robustness of the novel gate driver circuit against the Miller effect is shown in Figure 8.4 by turning T_{LS} off (negative gate-source

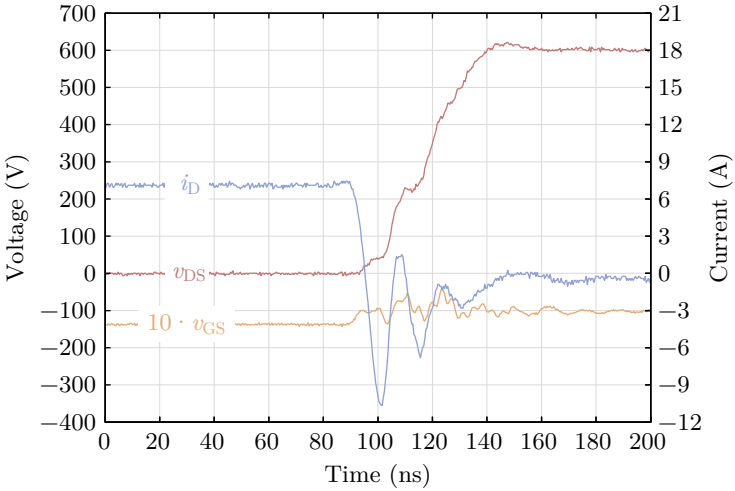


Figure 8.4: Robustness against the Miller effect: It can be seen, that the gate-source voltage is less than −5 V, so that a safety margin of more than 5 V to an accidental turn-on of the JFET is maintained in the whole switching interval.

voltage) and turning T_{HS} on so that the load current i_L commutates from D_{LS} to the upper switch charging C_{GD} of T_{LS}. Charging the gate-drain capacitance to 600 V does not lead to a significant change and/or increase of the negative gate-source voltage. Due to the presence of the low-impedance path to C_{ac} and the diodes D_1 and D_2, the gate-source voltage does not exceed −5 V at any time.

Furthermore, the optimized gate driver has been tested for varying JFET drain currents. No noticeable change in behavior was discovered. Switching speed is practically independent of drain current at turn-on, and turn-off is faster for increased currents, as they charge the intrinsic drain-source capacitance faster. Moreover, the JFET was subjected to elevated junction temperatures up to 250 °C in part showing reduced switching speed, e. g. slower turn-on transients of approximately 50 ns at 175 °C and 16 A, which is expected due to the on-resistance increasing with temperature and resulting in slower discharging of the drain-source capacitance at turn-on.

The positive temperature coefficient of the on-resistance of the normally-off SiC JFET helps to get the consequences of the parame-

ter spread under control when paralleling switches in order to increase current rating. The 40 A device is in fact a parallelization of two identical dies. Symmetrical setup is of great importance for balanced currents in the parallel connections. If more dies are to be driven in parallel, the value of C_{ac} has to be increased due to the increased gate charge according to Equation (4.8) and the design of V_{CC} as well as R_{dc} has to be conducted according to Section 4.3.3 for the additional gate current needed.

8.2 High Temperature Fan

To verify the theoretical considerations of the design of the high temperature fan, experimental results are given in this section and summarized in Table 8.1. The fan (*cf.* Figure 6.1(b)) is driven by a commercial inverter "CC-75-400" employing sensorless control for high-speed permanent magnet machines as manufactured by the company Celeroton [131]. The increased ambient temperature of up to 250 °C for the measurements is realized by a climate chamber "FD 53" by the company Binder [132]. All measurements are taken under stationary conditions, so that it is made sure that the temperature rise inside the fan due to its mechanical and electrical losses has reached is final value when measuring.

8.2.1 Fluid Dynamic Measurements

First, the fluid dynamic design target for the high temperature fan (similar characteristic at 120 °C as the Sanyo Denki reference fan at 20 °C) is validated on the fluid dynamic test bench of a large fan manufacturer. Figure 6.2 shows the measured curve for 20 °C and 19'000 min^{-1}. To assess the design target, the curve for 120 °C and 19'000 min^{-1} as well as for the reference fan at 20 °C and 16'500 min^{-1} are also shown: The constraint given in Equation (6.6) is fulfilled for the largest part of the operational curve the static pressure of the high temperature fan is significantly higher than for the reference fan with Δp_{HTF} dropping no more than 10% below Δp_{RF} very close to the region of stall.

It can also be seen, that the increased rotational speed does not only meet the requirements concerning Δp but also influences the volume flow according to Equation (6.8). Measured $\dot{V}_{\mathrm{max}}$ is with 0.84 $\mathrm{m}^3/\mathrm{min}$ only 4.5% lower than calculated in Equation (6.8).

Table 8.1: Measured high temperature fan specifications

High Temperature Fan		
Air Temperature (maximum) $T_{\mathrm{max,HTF}}$	250	°C
Max. Static Pressure (at 20 °C) $\Delta p_{\mathrm{max,HTF}}$	408	Pa
Max. Volume Flow (at 20 °C) $\dot{V}_{\mathrm{max,HTF}}$	0.84	$^{\mathrm{m}^3}/_{\mathrm{min}}$
Rotational Speed n_{HTF}	19'000	min^{-1}
Electrical Input Power $P_{\mathrm{el,HTF}}$	12	W
Terminal Voltage rms V_{HTF}	8.5	V[1]
Phase Current rms I_{HTF}	0.8	A
Electrical Frequency $f_{\mathrm{el,HTF}}$	1267	Hz
Mass m_{HTF}	96	g
Electrical Machine Type	3ph BLDC	

[1] A fan inverter dc input voltage of 12 V is sufficient to drive the fan with rated speed at nominal operating point.

8.2.2 Power Measurements

The considerations regarding the power rating of the fan are validated using a Yokogawa "WT3000" power analyzer [133]. Based on the data sheet value for the power of the reference fan (10.1 W) together with Equation (6.9), the high temperature fan is specified to 15 W (*cf.* Section 6.2.4).

In the first power measurement, the input power of the reference fan is determined to 8.9 W with 12.0 V applied to its dc input (corresponding to its rated speed of 16'500 min^{-1}) at 25 °C and different operating points in its pressure vs. volume flow curve (*cf.* Figure 6.2). The difference of 12% to the power value given in the data sheet is caused by a safety margin of the specifications of the reference fan. This means according to Equation (6.9), that the high temperature fan consumes 14.7 W at -40 °C and rated speed which is still below the design power consumption of 15 W. Hence, the fan can be operated at rated speed over the complete temperature range from -40 °C to 250 °C.

With this measurement, Equation (6.9) can now be verified. The expected value for the power of the high temperature fan is 13.6 W, and the measured value is 11.5 W. The difference of 15% is due to the fact, that first the measured power for the high temperature fan does not

include the power loss of the inverter driving the fan. Second the design of the electrical machine for both fans varies significantly and a higher efficiency of the machine used for the high temperature fan compared to the reference fan can be assumed due to the use of magnets with a higher energy density and a 3-phase design.

Measurements at higher temperatures proof Equation (6.2): At 120 °C, a power consumption of 8.2 W is measured, which is 71% of the power measured at 20 °C (compared to 75% calculated). At 250 °C, 6.3 W are 55% of the power needed at 20 °C (compared to 56% calculated).

8.2.3 Current and Voltage Waveforms

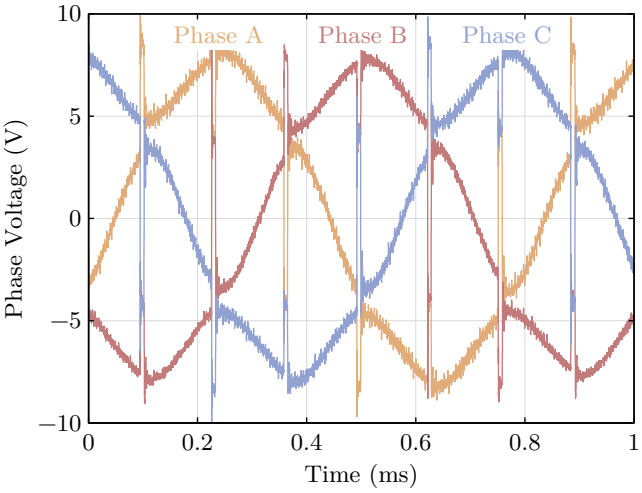
Figure 8.5 and Figure 8.6 show the phase voltages and currents, respectively, at 25 °C and at 250 °C under closed loop speed control. The 120° block shaped BLDC modulation scheme leads to clamped phase voltages during the short interval when all three phases conduct current due to non-zero phase inductance as can be seen from these figures. The amplitude of the phase voltages decreases slightly with temperature due to the decreasing remanence induction of the permanent magnets.

The current level is with an rms value of 0.8 A on the expected level, but shows a slight imbalance in phases A and C. This is due to small winding asymmetries leading to a slightly higher phase resistance in phase B. At high temperatures, the power level and thus the required torque and current decrease as has also been shown in Section 8.2.2. Furthermore, it can be directly seen from the time base, that the period of a phase current is 0.79 ms leading to a rotational speed of 19'000 min^{-1} for this machine having four pole pairs.

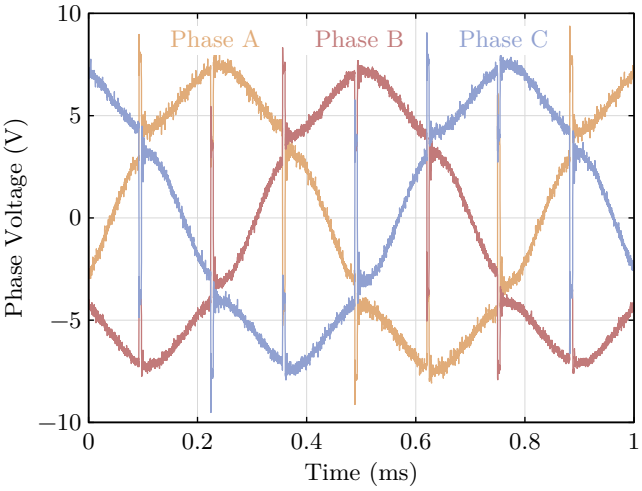
8.2.4 Acoustic Measurements

As mentioned in Section 6.2.1, the acoustic noise level of the high temperature fan is also of interest, especially as the rotational speed is increased by 15% compared to the commercial reference fan due to fluid dynamic requirements (*cf.* Section 6.2.4).

The sound pressure level emitted by commercially available fans is usually measured according to the Japanese industry standard "JIS B 8330": A noise meter is placed in a distance of 1 m from the inlet side of the fan under test operated at its rated speed in an anechoic room [134]. Figure 8.7 shows the sound pressure level over the audible

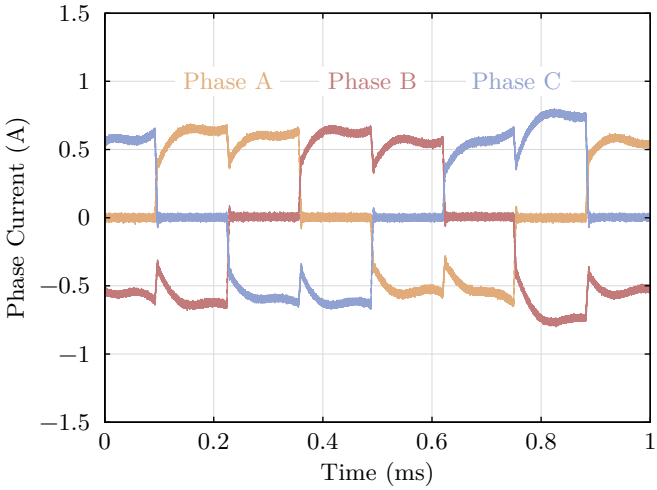


(a)

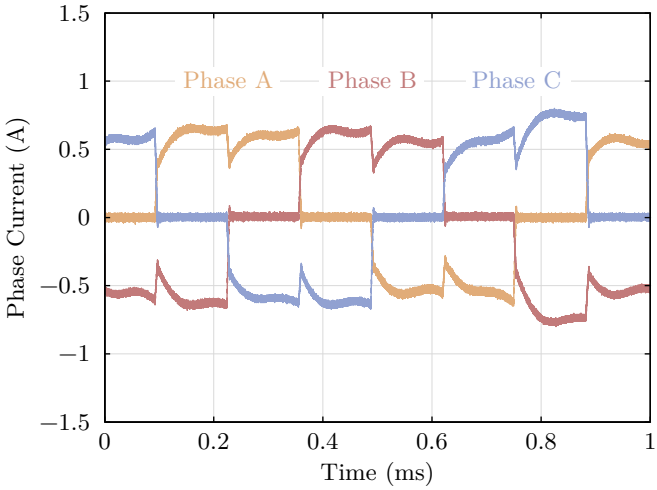


(b)

Figure 8.5: 3-phase voltages of the high temperature fan at an ambient temperature of (a) 25 °C and (b) 250 °C under closed loop speed control. The rotational speed is 19'000 min^{-1}.



(a)



(b)

Figure 8.6: 3-phase currents of the high temperature fan at an ambient temperature of (a) 25 °C and (b) 250 °C under closed loop speed control. The rotational speed is 19'000 min^{-1}.

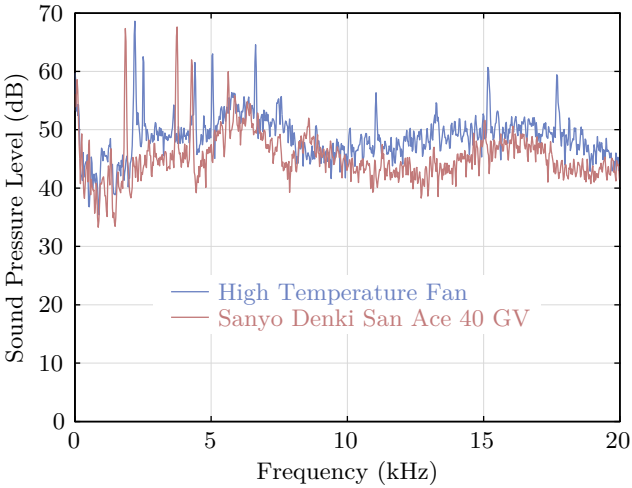


Figure 8.7: Measured sound pressure level over the audible frequency range at 25 °C for the high temperature fan and for the Sanyo Denki San Ace 40 Gv fan. (*cf.* Table 8.2 for calculated total sound pressure level).

frequency range measured at 25 °C for the high temperature fan and for the Sanyo Denki San Ace 40 Gv fan. Due to the physical dimensions of the anechoic chamber used for this measurement, the microphone was placed in a distance of 0.2 m from the fan. To be able to compare the measurement result with the data sheet value of 58 dBA for the Sanyo Denki fan [108], the sound pressure level (declining with the inverse of the distance) has been scaled such as it would have been measured at 1 m distance.

Table 8.2 lists the total sound pressure levels for both fans which are calculated from Figure 8.7 using a weighting of the different frequency components in order to take the properties of human hearing into account. The reason for the deviation is the air moving around the microphone in the test setup due to its small physical dimensions and the non-ideality of the sound absorption at the chamber walls. The important result for this research is the difference in the weighted sound pressure level between the high temperature fan and the reference fan of only 1.6 dBA. This difference cannot be easily recognized by humans [135].

Table 8.2: Weighted fan sound pressure levels measured at 25 °C

Measured A-Weighted Sound Pressure Level	
High Temperature Fan	66.6 dBA
Sanyo Denki San Ace 40 Gv	65.0 dBA

8.3 High Temperature Current Measurement

In this section, the design and the theoretical considerations of the high temperature current measurement are experimentally verified using the measurement setup described in Chapter 7 (Section 7.3). Figure 8.8 shows the measurement of a sinusoidal ac current. The theoretical waveforms shown in Figure 7.10 can be directly compared with the experimental waveforms in Figure 8.9(a) and Figure 8.9(b), measured at an ambient temperature around the magnetic core of 25 °C and 250 °C, respectively: The secondary current waveform shows the expected shape, the Adc voltage is for Figure 8.9(a) and Figure 8.9(b) directly measured at the Adc inputs (i.e. after the low-pass filter which is used to avoid voltage spikes on the signal) and the software trigger for starting the analog-digital conversion is shown in order to indicate the points in time when the shunt voltage is sampled. It can be seen that at 25 °C the software outputs an updated measurement value of the measured primary current every 18.6 µs, corresponding to a measurement frequency of 54 kHz. At 250 °C, these values change to 15.5 µs and 67 kHz, respectively, due to the decreasing saturation flux density B_{sat} of the core (*cf.* Equation (7.8) and Figure 7.7).

The measurement error is determined by a reference measurement of the primary current using a wide band power analyzer ("D6100" by Norma) with a 0.03% precision shunt. The absolute error of the described system scales linearly with the measured current, starting from an absolute error of 0.065 A at a primary current of 2.5 A to an error of 1.2 A at 47.5 A. Hence, the relative error is about constant at ≈ 2.5%. This error is mainly due to the resistors for the shunt and voltage level adjustment of the shunt voltage for the Adc (*cf.* Section 7.3.3) that have a resistance tolerance of ≈ 1% and parasitic resistances of Pcb tracks (a 10 mm long and 1 mm wide Pcb track shows a resistance of 4.8 mΩ, corresponding to 1% of the shunt resistor value).

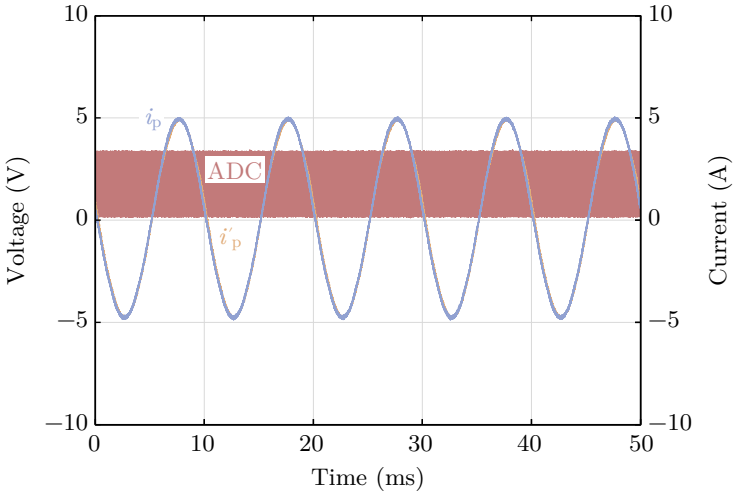


Figure 8.8: The primary current measured with a wide band power analyzer (waveform denoted with i_p) and with the presented bidirectionally saturated current transformer (waveform denoted with i'_p). Also shown is the signal triggering the ADC.

The primary current is calculated using the difference of two shunt voltages (despite the addition of the secondary currents $i_{\mathrm{s}1}$ and $i_{\mathrm{s}2}$ in Equation (7.4)) as the shunt current (in contrast to i_s) and the shunt voltage change their polarity with every switching transient as can be seen from Figure 7.3 and Figure 7.10. Hence, errors due to offsets of e.g. the operational amplifiers used cancel out to a large extent and the error of linearity can be compensated in the software. The resulting absolute and relative measurement errors are shown in Figure 8.10. The remaining error of less than 0.5% is due to the slight inaccuracies introduced by the measurement algorithm as expected in Section 7.3.4.

8.4 Inverter System

A hardware prototype of the inverter system designed in Chapter 5 is realized as shown in Figure 8.11. A comprehensive thermal and electrical test environment is built in order to operate the inverter system at 120 °C ambient temperature and to drive electrical machines, both

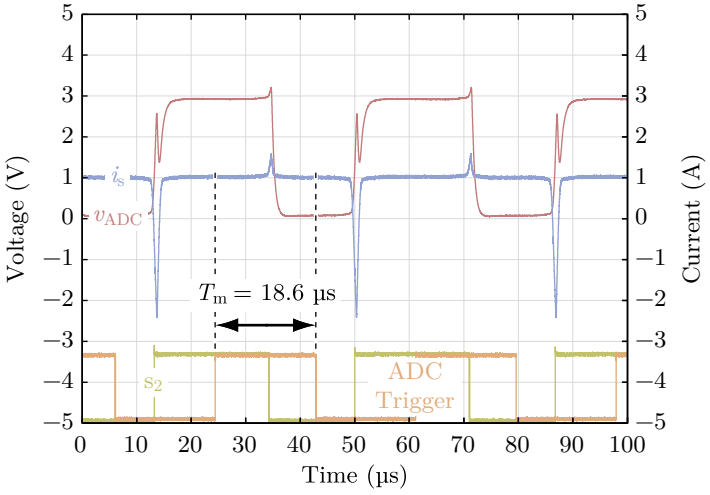


Figure 8.9: Measured waveforms at (a) 25 °C and (b) 250 °C ambient temperature of the magnetic core: v_{ADC} at the input of the ADC of the DSP, shunt current i_s, switching signal s_2 and software trigger starting the ADC conversion, with the latter two plotted with a negative offset of 5 V and scaled by a factor of 0.5 for the sake of clarity.

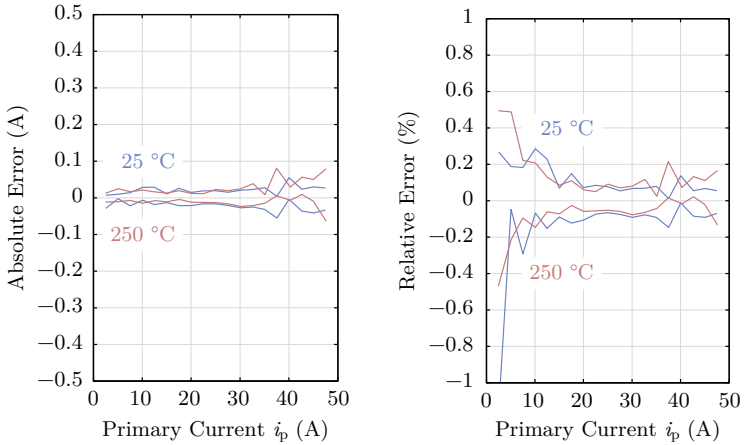
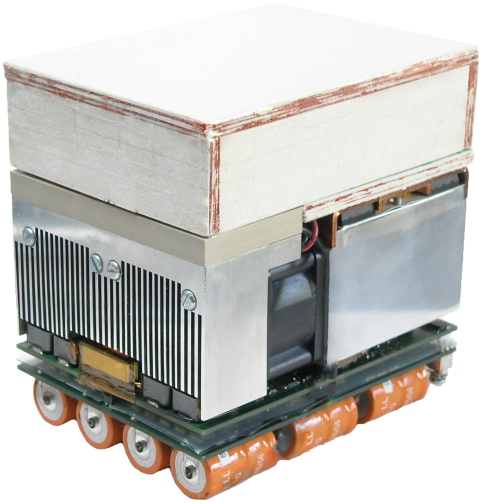


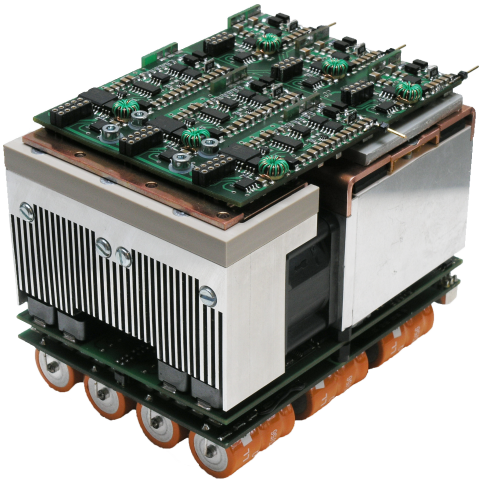
Figure 8.10: Minimum and maximum (a) absolute and (b) relative measurement error of the proposed current measurement system over the full measurement range after initial calibration of the setup to compensate for the linearity error introduced by tolerances of resistance values.

permanent magnet synchronous and induction machines, with the rated inverter power of 10 kW.

The design of the high temperature test environment includes the following considerations and challenges: On the one hand, the high temperature inverter system has to be placed in the thermal test chamber such that the ambient air around the signal electronics as well as the the air which the inverter takes to cool its power semiconductors is heated up to precisely 120 °C before it is blown through the heat sinks by the fans of the inverter. On the other hand, the test environment should at the same time not influence the performance of the inverter system by e.g. introducing an additional pressure drop for the cooling system of the inverter. Furthermore, separating the temperature controls for the ambient air around the signal electronics in the upper part of the converter (*cf.* Figure 5.7 and Figure 8.11) and the temperature around the power semiconductor heat sinks is helpful for testing purposes.

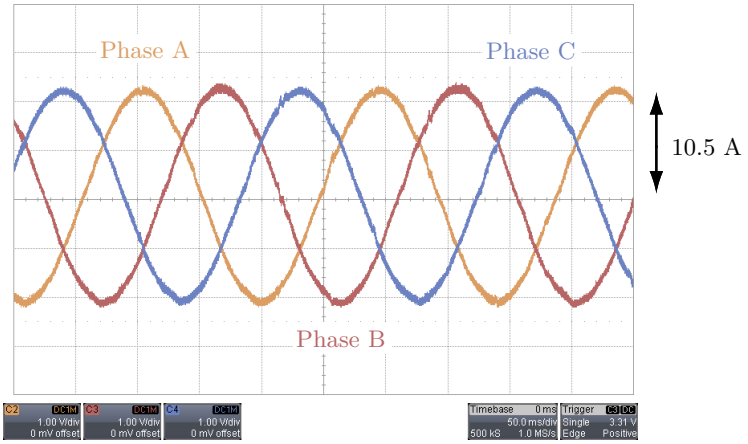


(a)

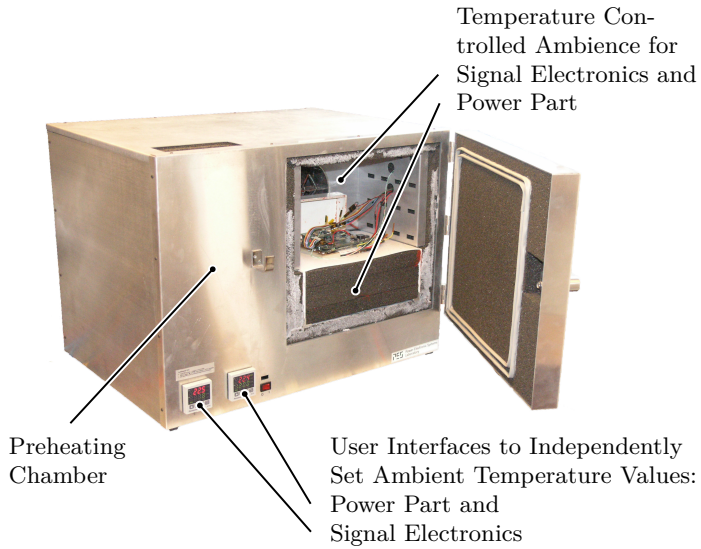


(b)

Figure 8.11: Hardware prototype of the 120 °C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system (a) with and (b) without the box that thermally isolates the actively cooled control and gate drive electronics from the ambience. The key specifications can be found in Table 5.1.



(a)



(b)

Figure 8.12: (a) 3-phase currents of the inverter driving the PMSM. The currents are almost sinusoidal with very low harmonic distortion due to the high inverter switching frequency of 50 kHz. (b) Photograph of the complete thermal chamber which is used to test the inverter system at 120 °C ambient temperature.

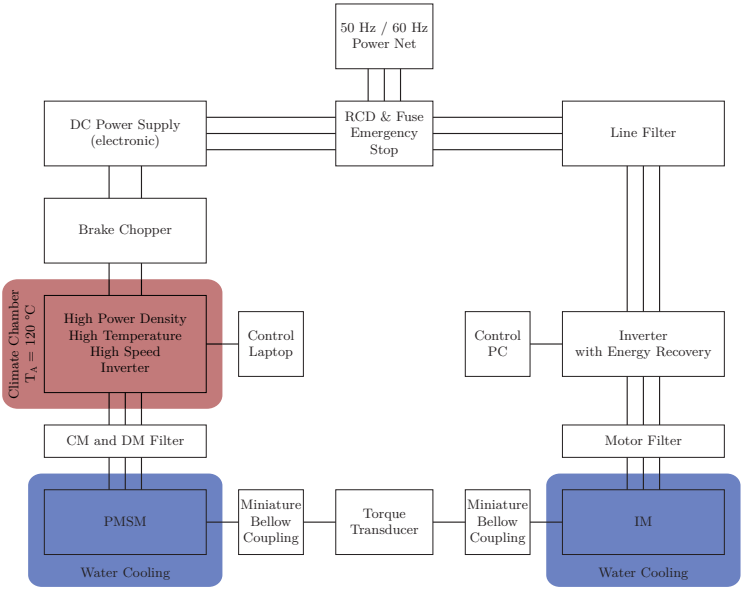


Figure 8.13: Block diagram of the test bench for the high temperature inverter system. The PMSM and IM have a rated power of 10 kW, four poles, and a maximum rotational speed of 30'000 min^{-1}.

Figure 8.12(b) shows a photograph of the developed thermal chamber. The inverter is placed in the chamber, and the isolation box covering the signal electronics is removed. The main compartment that can be seen surrounds the signal electronics. The left part of the chamber is used to preheat the air used for cooling the power electronics. The air is heated up and blown into the preheating chamber where the air temperature is monitored; the heater is automatically controlled to maintain the desired air temperature. The operating point of the fan blowing the air into the preheating box is calculated such that it compensates the additional pressure drop caused by the preheating box making sure that the influence of the test chamber on the cooling system performance of the inverter system is minimized. This air is then guided through a channel to the lower part of the inverter system. The temperature level for the ambient air around the signal electronics and for the power electronics can be set independently.

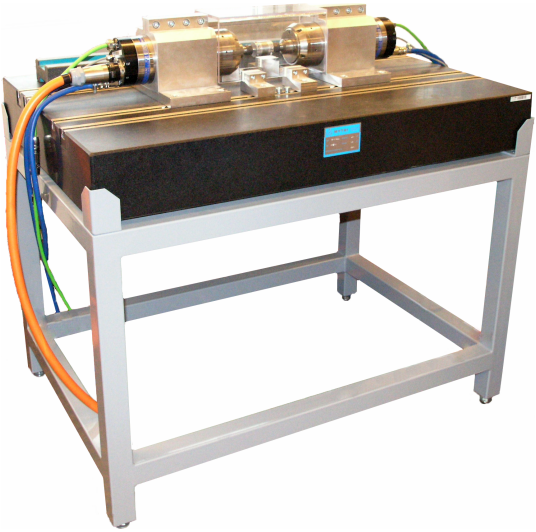


Figure 8.14: Photograph of the test bench equipped with a PMSM and an IM, a miniature bellow coupling, a transparent safety hood covering all rotating parts, a marble ruler as an adjustment fixture, and a marble machine base.

Electrical tests of the inverter system are conducted using a high speed drives test bench with a permanent magnet synchronous machine (PMSM) and an induction machine (IM), each with a rated power of 10 kW, four poles, and a maximum rotational speed of 30'000 min^{-1} in order to meet the trend towards higher rotational speeds in HEVs (*cf.* Section 1.1.2 in Chapter 1). Figure 8.13 shows the block diagram of the complete test setup, a photograph is shown in Figure 8.14. The inverter system is the device under test, which is supplied by a dc power supply and drives either the PMSM or the IM. The shafts of these water-cooled machines are mechanically coupled with a precisely balanced miniature bellow coupling [136]. A torque transducer can be placed in between the machines to be able to measure the mechanical power [137]. A commercial inverter feeds the energy of the load machine back to the dc supply of the device under test. This energy flow can also be reversed. Figure 8.12(a) shows the 3-phase currents of the inverter driving the PMSM. The currents are almost sinusoidal with very low harmonic distortion due to the high switching frequency of 50 kHz. Furthermore, tempera-

ture measurements are conducted using IC temperature sensors on the signal electronics PCB as well as thermocouples inside and outside of the signal electronics box. At a power level of only 30 W of the Peltier cooler, the temperature inside the box ranges from 5 K below ambient temperature (temperature at the outside of the signal electronics box) measured by the PCB sensor close to the Peltier device to 3 K above ambient temperature (outside of the box) measured by a thermocouple placed in "free air" inside the box.

8.5 Summary

In this chapter, experimental results are shown for the novel concepts investigated in Chapter 4 to Chapter 7. The test setup, switching transients demonstrating short switching times of 34 ns for turn-on and 24 ns for turn-off as well as measurements proving the high immunity against the Miller effect show a safe operation of the JFET with minimum switching and conduction losses. Electrical and temperature measurements for the inverter itself are given together with the concept and realization of a complete test environment consisting of a thermal test chamber and a test bench with a PMSM and an IM. For the high temperature fan, acoustic and especially fluid dynamic measurements are presented besides electrical measurements to show the operation and performance of the fan at speeds up to 19'000 min^{-1} at an ambient temperature level of up to 250 °C. The high temperature current measurement for dc and sinusoidal ac currents up to 1 kHz verifies a measurement error of less than 0.5% up to 50 A even at 250 °C.

Chapter 9

Conclusion and Outlook

A compact power electronic full-SiC inverter system with high output frequencies and direct air-cooling of SiC power semiconductors for use in hybrid electric vehicles at an ambient temperature of 120 °C is thoroughly investigated in this dissertation. Novel normally-off SiC JFETs with a switching frequency of 50 kHz and a novel gate driver for safe operation with minimum switching and conduction losses are employed and a junction temperature of 250 °C is shown to maximize the current carrying capability of the SiC power semiconductors (and thus fully utilize the semiconductor die area) for the given converter parameters. A converter setup with a power semiconductor junction temperature of 250 °C and active signal electronics cooling, a high performance fan as well as a current measurement prototype, both for 250 °C, are introduced.

The research work presented in this dissertation demonstrates the technical feasibility of significantly increasing the operating range of today's power electronic converters with respect to their ambient temperature rating and of meeting inherent needs for their use in HEVs. These advancements are mainly achieved by increasing the junction temperature of the employed power semiconductors which directly leads to the need for an according design of the whole inverter system. This design includes two approaches, the creation of new technology as well as transferring certain techniques from other domains to operate standard technology in harsh environments.

Creating new technology means with respect to this dissertation, that a new gate driver circuit is proposed and tested for normally-off SiC

JFETs. Furthermore, a novel high temperature fan which withstands an almost 200 K higher temperature than comparable commercial products today, and a high temperature current measurement concept are presented and validated.

Future work in the area of creating new technology for high (junction) temperature power electronic converters can include the continuation of efforts on the semiconductor packaging technology such that packages for 250 °C junction temperature can meet automotive reliability requirements, especially concerning thermal cycling. Advancements in the packaging of power semiconductors can also lead to new packaging solutions which provide reduced parasitic inductances for otherwise similar electrical and thermal behavior. This can help to reduce overvoltages during switching and thus offers the opportunity of reducing the safety margin between the maximum system voltage and the blocking voltages of the employed power semiconductors which would represent an additional or alternative way of reducing the power semiconductor losses.

The second approach mentioned above can be illustrated by the employed active cooling: It ensures that standard technology can be used for the signal electronics and and standard components for the gate drivers while still being placed very close to the hot semiconductors.

The price that has to be paid for the described advancements in terms of ambient temperature rating and high output frequency capability is slightly reduced efficiency (due to increased losses at high junction temperatures and high switching frequencies) and reduced power density due to the volume needed for the Peltier cooling. Second, and in very cost sensitive application areas like the automotive industry of special importance, increased cost for the power electronic converter by the use of SiC switches (which are likely to not reach the same price level as Si switches in the future), and for further high temperature components required e.g. for the fan, must be considered.

Taking these drawbacks into account, a detailed analysis of costs and benefits on a system level can reveal whether it is beneficial to manufacture more expensive components with less restrictions so that peripheral costs can be decreased. A typical question would be, if the overall system costs could be decreased by setting the additional costs of a low temperature water-cooling circuit aside and accepting the higher costs of a high temperature inverter. This sensitivity analysis will reveal an optimum for each application, which *could* mean for the example of

HEVs to surrender e.g. the direct air-cooling and thus also the high temperature fan, but keep all other aspects of the high temperature inverter system in order to be able to use the high temperature water cooling circuit of the internal combustion engine.

This trade-off analysis, whether certain advancements on a subsystem level that might make the subsystem more costly but can reduce acquisition and/or operating cost on the system level and can lead to even increased market value of the product, applies of course to all application areas of this high temperature converter system which are mentioned in the introduction, and can reveal different results for each industry investigated. For the automotive industry, this analysis should be applied to HEVs in general. Furthermore, in economic research, several theories or models describing the consumer exist. The sovereign customer, that has been mentioned in the introduction of this dissertation, finally decides whether the increase in efficiency for certain mission profiles or other aspects as mentioned in the introduction influencing the purchase decision are convincing to pay the additional price of a HEV. Accordingly, life cycle cost of HEVs need to be studied and published in continuation of research on only technical aspects of innovative passenger car concepts.

Glossary

Commonly Used Abbreviations

ac	Alternating current
ADC	Analog-digital converter
AlNiCo	Aluminium nickel cobalt
AMCA	Air movement and control association
BJT	Bipolar junction transistor
BLDC	Brushless direct current
CAD	Computer-aided design
const	Constant
CO_2	Carbon dioxide
CSPI	Cooling system performance index
CTE	Coefficient of thermal expansion
CuNi	Copper nickel
D_2, D_4	Schottky diodes used in the proposed gate driver
D_1, D_3	Zener diodes used in the proposed gate driver
D_{ac}, D_{dc}	Schottky diodes used in the proposed gate driver
dc	Direct current
D_{GD}	Gate-drain diode of a JFET
D_{GS}	Gate-source diode of a JFET
D_{HS}	High-side diode in a bridge leg
D_{LS}	Low-side diode in a bridge leg
DSP	Digital signal processor
EMI	Electromagnetic interference

FeCo	Iron cobalt
FEM	Finite element method
FeSi	Iron silicon
FET	Field effect transistor
HEV	Hybrid electric vehicle
IC	Integrated circuit
ICE	Internal combustion engine
IGBT	Insulated gate bipolar transistor
IM	Induction machine
IP	Ingress protection
ISR	Interrupt service routine
JFET	Junction field effect transistor
LVJFET	Vertical JFET with a lateral channel
NdFeB	Neodymium iron boron
NiFe	Nickel iron
MOSFET	Metal-oxide-semiconductor field effect transistor
PCB	Printed circuit board
PMSM	Permanent magnet synchronous machine
PWM	Pulse-width modulation
rms	Root mean square
Si	Silicon
SiC	Silicon carbide
SiO_2	Silicon dioxide
Sm_2Co_{17}	Samarium cobalt
$SmCo_5$	Samarium cobalt
SOI	Silicon on insulator
SOP	Small outline package
T_{HS}	High-side transistor in a bridge leg
T_{LS}	Low-side transistor in a bridge leg
TO	Transistor single outline
VJFET	JFET with a purely vertical structure

Commonly Used Designators of Physical Quantities

Latin Letters

A_D	Area of a power semiconductor die
a_E	Zeroth order coefficient of $g_E(I_\mathrm{D})$
A_m	Cross section of a magnetic core
$a_{R\mathrm{th}}$	Coefficient for the calculation of $R_{\mathrm{th,JA}}(A_\mathrm{D})$
b_E	First order coefficient of $g_E(I_\mathrm{D})$
$b_{R\mathrm{th}}$	Coefficient for the calculation of $R_{\mathrm{th,JA}}(A_\mathrm{D})$
B_sat	Saturation magnetic flux density
C_ac	AC-coupling capacitance used in the proposed novel gate driver circuit
C_DS	Drain-source capacitance of a unipolar power semiconductor switch
c_E	Second order coefficient of $g_E(I_\mathrm{D})$
C_GD	Gate-drain capacitance of a unipolar power semiconductor switch
C_GS	Gate-source capacitance of a unipolar power semiconductor switch
C_iss	Input capacitance of a power semiconductor switch
C_rss	Reverse transfer capacitance of a power semiconductor switch
d_E	Zeroth order coefficient of $h_E(T_\mathrm{J})$
d_F	Rotor diameter of a fan
E_BD	Breakdown electrical field of a semiconductor
e_E	First order coefficient of $h_E(T_\mathrm{J})$
E_G	Band-gap (energy difference between conduction and valence band) of a semiconductor
E_S	Switching energy (sum of turn-on and turn-off energy)
$E_\mathrm{S,pn}$	Switching energy (sum of turn-on and turn-off energy) of a SiC JFET without antiparallel SiC Schottky diode
$E_\mathrm{S,Schottky}$	Switching energy (sum of turn-on and turn-off energy) of a SiC JFET with antiparallel SiC Schottky diode

f_E	Second order coefficient of $h_E(T_\mathrm{J})$
f_O	Electrical output frequency (of the dc-ac inverter)
f_S	Switching frequency of a power electronic converter
g_E	Second-order-polynomial reflecting the dependency of E_S on I_D
h_E	Second-order-polynomial reflecting the dependency of E_S on T_J
k_B	Boltzmann's constant
H_C	Coercive magnetic field strength
H_p	Magnetic field strength caused by i_p
H_sat	Saturation magnetic field strength
I_C	Capacitor current (rms value)
I_D	Drain current (rms value) of a unipolar semiconductor switch
$I_\mathrm{D,max}$	Maximum I_D corresponding to $T_\mathrm{J,max}$ in the steady state
$I_\mathrm{D,submax}$	$I_\mathrm{D,max}$ reduced by a safety margin
I_G	Gate current during the on-state of a JFET
I_L	Leakage current of a (Schottky) diode
i_L	Inductor current (instantaneous value)
I_O	Maximum output current of a gate driver IC
i_p	Current of a primary conductor on a magnetic core
I_ph	Phase current (rms value) of an electrical machine
i_s	Current of a secondary conductor on a magnetic core
l_m	Average length of the magnetic path in a magnetic core
M	Torque (of an electrical machine)
m	Modulation index of a dc-ac inverter
N_A	Acceptor doping concentration of a semiconductor
N_C	Density of states in the conduction band of a semiconductor
N_D	Donator doping concentration of a semiconductor
n_F	Rotational speed of a fan (rotor)
n_i	Intrinsic charge carrier concentration of a semiconductor
n_m	Mechanical rotational speed of an electrical machine

n_n	Electron density of a semiconductor
N_p	Number of turns of a primary conductor on a magnetic core
n_p	Hole density of a semiconductor
N_s	Number of turns of a secondary conductor on a magnetic core
N_V	Density of states in the valence band of a semiconductor
p	Number of pole pairs (of an electrical machine)
p_A	Absolute air pressure
P_C	Conduction losses of a power semiconductor
$P_\mathrm{F,el}$	Electrical input power of a fan
P_m	Mechanical output power of an electrical machine
P_O	Electrical output power of a power electronic converter
$P_\mathrm{P,el}$	Electrical input power of a Peltier cooler
P_S	Switching losses of a power semiconductor
$P_\mathrm{S,m}$	Mechanical shaft power of a fan
Q_G	Gate charge of a power semiconductor switch
Q_P	Heat input at the cold side of a Peltier cooler
R	Electrical resistance
R_ac	Resistance connected in series with C_ac in the proposed novel gate driver circuit
R_c	Gas constant
R_DC	Resistance used in the proposed novel gate driver
$R_\mathrm{DS,on}$	Electrical resistance of the drain-source path in the on-state of a unipolar power semiconductor switch
$r_\mathrm{DS,on}$	Area specific $R_\mathrm{DS,on}$
R_GD	Output resistance of a gate driver Ic
r_on	Area specific electrical resistance of the load current path in the on-state of a power semiconductor device
R_S	Shunt
R_th	Thermal resistance
$R_\mathrm{th,HSP}$	Thermal resistance of the heat sink for a Peltier cooler
$R_\mathrm{th,JA}$	Thermal resistance from the power semiconductor junction to the ambience

R_{tot}	Sum of R_{GD}, R_{GD} and internal JFET resistances
T	Temperature
T_{A}	Ambient temperature
T_{box}	Temperature inside the signal electronics box
T_{C}	Curie temperature
T_{J}	Junction temperature of a power semiconductor switch
$T_{\mathrm{J,max}}$	Maximum T_{J} (limit imposed by material properties or operational requirements regarding thermal stability)
$T_{\mathrm{J,submax}}$	T_{J} corresponding to $I_{\mathrm{D,submax}}$ in the steady state
T_{nom}	Nominal operating air temperature of the high temperature fan
T_{ref}	Nominal operating air temperature of the reference fan
$\dot{V}$	Volume flow of a fan
V_{bi}	Built-in voltage of a pn-junction
$V_{C\mathrm{ac}}$	Voltage across C_{ac}
V_{CC}	Positive supply voltage
v_{D}	Saturated electron drift velocity of a n-doped semiconductor
V_{dc}	DC-link voltage of an inverter
v_{DS}	Drain-source voltage of a JFET or MOSFET
V_{EE}	Negative supply voltage
V_{F}	Forward voltage of a diode
V_{GS}	Gate-source voltage of a JFET or MOSFET
$V_{\mathrm{GS,po}}$	Gate-source pinch-off voltage of a JFET
$V_{\mathrm{GS,th}}$	Gate-source threshold voltage of a JFET or MOSFET
v_L	Voltage across an inductor (instantaneous value)
V_{ph}	Voltage (rms value) between two phases at the output of a 3-phase inverter
$V_{\mathrm{r,Ddc}}$	Maximum reverse voltage of D_{dc}
v_{S}	Voltage across a shunt (instantaneous value)
V_{Z}	Zener voltage of a Zener diode

Greek Letters

α_{CTE}	Coefficient of linear thermal expansion
Δp	Difference in static pressure between the outlet and inlet side of a fan
ΔT_{HSP}	Temperature drop across the heat sink for a Peltier cooler
$\Delta T_{\mathrm{Peltier}}$	Temperature difference between the hot and cold side of a Peltier cooler
ϵ_{r}	(Static) Relative dielectric constant
λ	Thermal conductivity
μ_0	Magnetic constant
μ_{n}	Electron (negative charge carrier) mobility
μ_{p}	Hole (positive charge carrier) mobility
μ_{r}	Relative magnetic permeability
ρ_{A}	Air density
Φ	Phase difference of voltage and current waveform
ω	Angular frequency
ω_{m}	Mechanical angular frequency of an electrical machine

List of Tables

List of Figures

Bibliography

[1] C. R. McConnell, S. L. Brue, and S. M. Flynn, *Economics: Principles, Problems, and Policies*, 19th edition. New York: McGraw-Hill/Irwin, 13 January 2011, ISBN: 978-0073511443.

[2] A. Peters and P. de Haan, "Der Autokäufer – seine Charakteristika und Präferenzen. Ergebnisbericht im Rahmen des Projekts 'Entscheidungsfaktoren beim Kauf treibstoffeffizienter Neuwagen'. Berichte zum Schweizer Autokaufverhalten Nr. 11." Institute for Environmental Decisions, Natural and Social Science Interface, ETH Zurich, November 2006. DOI: 10.3929/ethz-a-006123209

[3] European Parliament and Council, "Regulation (EC) no 443/2009 of the European Parliament and of the Council of 23 April 2009 setting emission performance standards for new passenger cars as part of the Community's integrated approach to reduce CO_2 emissions from light-duty vehicles," in *Official Journal of the European Union*, 23 April 2009.

[4] European Commission. Proposal for a regulation to define the modalities for reaching the 2020 target for reducing CO_2 emissions from new passenger cars. 11 July 2012.

[5] P. Hofmann, *Hybridfahrzeuge*. Wien: Springer-Verlag, February 2010. DOI: 10.1007/978-3-211-89191-9

[6] L. Spiegel, D. Kraxner, and H.-J. Neußer, "Das Hybridkonzept von Porsche," in *16. Aachener Kolloquium Fahrzeug- und Motorentechnik 2007*, Aachen, Germany, 9–10 October 2007.

[7] B. Heißing and M. Ersoy, Eds., *Fahrwerkhandbuch: Grundlagen, Fahrdynamik, Komponenten, Systeme, Mechatronik, Perspektiven (ATZ/MTZ-Fachbuch)*, 2nd edition. Wiesbaden: Vieweg+Teubner Verlag, 2008. DOI: 10.1007/978-3-8348-9493-9

[8] J. W. Kolar, *Skriptum zur Vorlesung Leistungselektronische Systeme II.* Power Electronic Systems Laboratory, ETH Zurich, June 2005.

[9] E. Sulaiman, T. Kosaka, and N. Matsui, "A novel hybrid excitation flux switching synchronous machine for a high-speed hybrid electric vehicle applications," in *Proceedings of the International Conference on Electrical Machines and Systems (ICEMS)*, Beijing, China, 20–23 August 2011, pp. 1–6. DOI: 10.1109/ICEMS.2011.6073505

[10] T. A. Burress, S. L. Campbell, C. L. Coomer, C. W. Ayers, A. A. Wereszczak, J. P. Cunningham, L. D. Marlino, L. E. Seiber, and H. T. Lin, "Evaluation of the 2010 Toyota Prius Hybrid Synergy Drive System," Oak Ridge National Laboratory (ORNL), Oak Ridge, TN, USA; Pacific Northwest National Laboratory (PNNL), Richland, WA, USA, March 2011.

[11] C. Zwyssig, J. W. Kolar, and S. D. Round, "Megaspeed drive systems: Pushing beyond 1 million r/min," *IEEE/ASME Transactions on Mechatronics*, vol. 14, no. 5, pp. 564–574, October 2009. DOI: 10.1109/TMECH.2008.2009310

[12] M. Schweizer, "System-oriented efficiency optimization of variable speed drives," Ph. D. dissertation, Power Electronic Systems Laboratory, ETH Zurich, Switzerland, November 2012. DOI: 10.3929/ethz-a-009864703

[13] F. Renken and R. Knorr, "High temperature electronic for future hybrid powertrain application," in *Proceedings of the European Conference on Power Electronics and Applications (EPE)*, Dresden, Germany, 11–14 September 2005. DOI: 10.1109/EPE.2005.219769

[14] T. Franke, H. Glonner, D. Nowak, and F. Österreicher, "Electrified power train - challenges and opportunities for the electrical industry," in *Proceedings of the European Conference on Power Electronics and Applications (EPE)*, Dresden, Germany, 11–14 September 2005. DOI: 10.1109/EPE.2005.219776

[15] S. Pischinger, M. Pischinger, H. Kemper, and S. Christiaens, "The challenges of system integration of the hybrid electric powertrain," in *Fachtagungsberichte VDE Kongress*, Aachen, Germany, 23–25 October 2006.

[16] S. Matsumoto, "Advancement of hybrid vehicle technology," in *Proceedings of the European Conference on Power Electronics and Applications (EPE)*, Dresden, Germany, 11–14 September 2005. DOI: 10.1109/EPE.2005.219775

[17] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. Springer Science + Business Media, 2008. DOI: 10.1007/978-0-387-47314-7

[18] D. Schröder, *Leistungselektronische Bauelemente*, 2nd edition. Berlin Heidelberg: Springer-Verlag, 2006. DOI: 10.1007/3-540-31735-X

[19] K. Hamada, "SiC device and power module technologies for environmentally friendly vehicles," in *Proceedings of the 7th International Conference on Integrated Power Electronics Systems (CIPS)*, Nuremberg, Germany, 6–8 March 2012, pp. 1–6.

[20] R. H. Staunton, C. W. Ayers, J. N. Chiasson, B. A. Burress, and L. D. Marlino, "Evaluation of 2004 Toyota Prius hybrid electric drive system," Oak Ridge National Laboratory (ORNL), Oak Ridge, TN, USA; Pacific Northwest National Laboratory (PNNL), Richland, WA, USA, May 2006. DOI: 10.2172/890029

[21] T. A. Burress, C. L. Coomer, S. L. Campbell, L. E. Seiber, L. D. Marlino, R. H. Staunton, and J. P. Cunningham, "Evaluation of the 2007 Toyota Camry Hybrid Synergy Drive System," Oak Ridge National Laboratory (ORNL), Oak Ridge, TN, USA; Pacific Northwest National Laboratory (PNNL), Richland, WA, USA, January 2008.

[22] H. Yasui, H. Ishiyama, M. Inagaki, K. Mamitsu, and T. Kikuchi, "Power control unit for high power hybrid system," in *Proceedings of the SAE World Congress*, Detroit, MI, USA, 16–19 April 2007. DOI: 10.4271/2007-01-0271

[23] J. Rabkowski, D. Peftitsis, and H.-P. Nee, "Silicon carbide power transistors: A new era in power electronics is initiated," *IEEE Industrial Electronics Magazine*, vol. 6, no. 2, pp. 17–26, June 2012. DOI: 10.1109/MIE.2012.2193291

[24] T. Funaki, J. C. Balda, J. Junghans, A. S. Kashyap, H. A. Mantooth, F. Barlow, T. Kimoto, and T. Hikihara, "Power conversion with SiC devices at extremely high ambient temperatures," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1321–1329, July 2007. DOI: 10.1109/TPEL.2007.900561

[25] J. G. Bai, J. Yin, Z. Zhang, G.-Q. Lu, and J. D. van Wyk, "High-temperature operation of SiC power devices by low-temperature sintered silver die-attachment," *IEEE Transactions on Advanced Packaging*, vol. 30, no. 3, pp. 506–510, August 2007. DOI: 10.1109/TADVP.2007.898628

[26] E. Schulze, C. Mertens, and A. Lindemann, "Pure low temperature joining technique power module for automotive production needs," in *Proceedings of the 6th International Conference on Integrated Power Electronics Systems (CIPS)*, Nuremberg, Germany, 16–18 March 2010, pp. 333–338.

[27] P. Hagler, P. Henson, and R. Johnson, "Packaging technology for electronic applications in harsh high-temperature environments," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2673–2682, July 2011. DOI: 10.1109/TIE.2010.2047832

[28] M. Kanechika, T. Uesugi, and T. Kachi, "Advanced SiC and GaN power electronics for automotive systems," in *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 6–8 December 2010, pp. 13.5.1–13.5.4. DOI: 10.1109/IEDM.2010.5703356

[29] R. Wang, P. Ning, D. Boroyevich, M. Danilovic, F. Wang, and R. Kaushik, "Design of high-temperature SiC three-phase ac-dc converter for 100 °C ambient temperature," in *Proceedings of the*

2nd IEEE Energy Conversion Congress and Exposition (ECCE), Atlanta, GA, USA, 12–16 September 2010, pp. 1283–1289. DOI: 10.1109/ECCE.2010.5617813

[30] A. Antonopoulos, H. Bangtsson, M. Alakula, and S. Manias, "Introducing a silicon carbide inverter for hybrid electric vehicles," in *Proceedings of the 39th IEEE Power Electronics Specialists Conference (PESC)*, Rhodes, Greece, 15–19 June 2008, pp. 1321–1325. DOI: 10.1109/PESC.2008.4592116

[31] R. Wang, D. Boroyevich, P. Ning, Z. Wang, F. Wang, P. Mattavelli, K. Ngo, and K. Rajashekara, "A high-temperature SiC three-phase ac-dc converter design for $> 100\,^{\circ}\mathrm{C}$ ambient temperature," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 555–572, 2013. DOI: 10.1109/TPEL.2012.2199131

[32] P. Godignon, X. Jorda, M. Vellvehi, X. Perpina, V. Banu, D. Lopez, J. Barbero, P. Brosselard, and S. Massetti, "SiC Schottky diodes for harsh environment space applications," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2582–2590, July 2011. DOI: 10.1109/TIE.2010.2080252

[33] J. M. Hornberger, E. Cilio, B. McPherson, R. M. Schupbach, A. B. Lostetter, and A. H. Mantooth, "A fully integrated $300\,^{\circ}\mathrm{C}$, 4 kW, 3-phase, SiC motor drive module," in *Proceedings of the 38th IEEE Power Electronics Specialists Conference (PESC)*, Orlando, FL, USA, 17–21 June 2007, pp. 1048–1053. DOI: 10.1109/PESC.2007.4342136

[34] M. Chinthavali, J. A. Tawfik, and R. V. Arimilli, "Design and analysis of a 55-kW air-cooled automotive traction drive inverter," in *Proceedings of the 3rd IEEE Energy Conversion Congress and Exposition (ECCE)*, Phoenix, AZ, USA, 17–22 September 2011, pp. 2345–2352. DOI: 10.1109/ECCE.2011.6064080

[35] H. Fujiwara, H. Naruoka, M. Konishi, K. Hamada, T. Katsuno, T. Ishikawa, Y. Watanabe, and T. Endo, "Impact of surface morphology above threading dislocations on leakage current in 4H-SiC diodes," *Applied Physics Letters*, vol. 101, no. 4, pp. 042 104–042 104–4, July 2012. DOI: 10.1063/1.4738886

[36] K. Hamada, "Toyota's activities on power electronics for future mobility," in *Proceedings of the 14th European Conference on Power Electronics and Applications (EPE)*, Birmingham, United Kingdom, 30 August – 1 September 2011, p. 1.

[37] H. Ohtsuka and F. Anraku, "Development of inverter for 2006 model year Civic Hybrid," in *Proceedings of the 4th Power Conversion Conference (PCC)*, Nagoya, Japan, 2–5 April 2007, pp. 1596–1600. DOI: 10.1109/PCCON.2007.373177

[38] R. H. Staunton, T. A. Burress, and L. D. Marlino, "Evaluation of 2005 Honda Accord hybrid electric drive system," Oak Ridge National Laboratory (ORNL), Oak Ridge, TN, USA; Pacific Northwest National Laboratory (PNNL), Richland, WA, USA, September 2006.

[39] G. A. Landis, "Robotic exploration of the surface and atmosphere of Venus," *Acta Astronautica*, vol. 59, no. 7, pp. 570–579, 2006. DOI: 10.1016/j.actaastro.2006.04.011

[40] J. A. Rosero, J. A. Ortega, E. Aldabas, and L. Romeral, "Moving towards a more electric aircraft," *IEEE Aerospace and Electronic Systems Magazine*, vol. 22, no. 3, pp. 3–9, March 2007. DOI: 10.1109/MAES.2007.340500

[41] A. König, "High temperature dc-to-dc converters for downhole applications," Ph. D. dissertation, Institute for Power Electronics and Electrical Drives, RWTH Aachen University, Germany, June 2009, ISBN: 978-3-8322-8489-3.

[42] Schlumberger Ltd., "REDA hotline high temperature ESP systems," 2007.

[43] G. Pensl, F. Ciobanu, T. Frank, M. Krieger, S. Reshanov, F. Schmid, and M. Weidner, *SiC Materials and Devices*, ser. Selected Topics in Electronics and Systems – Vol. 40. 5 Toh Tuck Link, Singapore 596224: World Scientific Publishing Co. Pte. Ltd., 2006, vol. 1, chapter SiC Material Properties, pp. 1–41. DOI: 10.1142/9789812773371

[44] M. B. J. Wijesundara and R. G. Azevedo, *Silicon Carbide Microsystems for Harsh Environments*. Springer Science + Business Media, 2011. DOI: 10.1007/978-1-4419-7121-0

[45] G. L. Harris, *Properties of Silicon Carbide*, ser. EMIS Datareviews, no. 13. Institution of Engineering and Technology, 1995, ISBN: 978-0863415548.

[46] T. Ayalew, "SiC semiconductor devices technology, modeling, and simulation," Ph. D. dissertation, Institute for Microelectronics, Technical University Vienna, Austria, January 2004.

[47] A. Melkonyan, "High efficiency power supply using new SiC devices," Ph. D. dissertation, Institute for Electrical Engineering – Efficient Energy Conversion, University of Kassel, Germany, February 2007, ISBN: 978-3-89958-302-1.

[48] P. Friedrichs and R. Rupp, "Silicon carbide power devices - current developments and potential applications," in *Proceedings of the 11th European Conference on Power Electronics and Applications (EPE)*, Dresden, Germany, 11–14 September 2005. DOI: 10.1109/EPE.2005.219736

[49] S. Dimitrijev, "SiC on Si as platform technology," in *Proceedings of the 26th International Conference on Microelectronics (MIEL)*, Niš, Serbia, 11–14 May 2008. DOI: 10.1109/ICMEL.2008.4559223

[50] Cree, Inc. Cree introduces 150 mm 4HN silicon carbide epitaxial wafers. 4600 Silicon Drive, Durham, NC 27703, USA. 30 August 2012.

[51] P. Friedrichs, "Silicon carbide power devices — status and upcoming challenges," in *Proceedings of the 12th European Conference on Power Electronics and Applications (EPE)*, Aalborg, Denmark, 2–5 September 2007. DOI: 10.1109/EPE.2007.4417782

[52] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics - Converters, Applications, and Design*, 3rd edition, B. Zobrist, Ed. John Wiley & Sons, Inc., 2003, ISBN: 978-0471226932.

[53] P. A. Ivanov, M. E. Levinshtein, A. K. Agarwal, S. Krishnaswami, and J. W. Palmour, "Temperature dependence of the current gain in power 4H-SiC npn BJTs," *IEEE Transactions on Electron Devices*, vol. 53, no. 5, pp. 1245–1249, May 2006. DOI: 10.1109/TED.2006.872701

[54] J. H. Zhao, K. Sheng, and R. C. Lebron-Velilla, *SiC Materials and Devices*, ser. Selected Topics in Electronics and Systems, Vol. 40. 5 Toh Tuck Link, Singapore 596224: World Scientific Publishing Co. Pte. Ltd., 2006, vol. 2, chapter Silicon Carbide Schottky Barrier Diode, pp. 117–162. DOI: 10.1142/9789812706850

[55] S. DasGupta, R. J. Kaplar, M. J. Marinella, M. A. Smith, and S. Atcitty, "Analysis and prediction of stability in commercial, 1200 V, 33 A, 4H-SiC MOSFETs," in *IEEE International Reliability Physics Symposium (IRPS)*, Anaheim, CA, USA, April 2012, pp. 3D.3.1–3D.3.5. DOI: 10.1109/IRPS.2012.6241817

[56] G. Deboy, H. Ludwig, R. Mallwitz, and R. Rupp, "New SiC JFET with integrated body diode boosts performance of photovoltaic systems," in *Proceedings of the International Power Conversion and Intelligent Motion Conference (PCIM Europe)*, Nuremberg, Germany, 17–19 May 2011, pp. 220–228.

[57] D. Stephani and P. Friedrichs, *SiC Materials and Devices*, ser. Selected Topics in Electronics and Systems, Vol. 43. 5 Toh Tuck Link, Singapore 596224: World Scientific Publishing Co. Pte. Ltd., 2006, vol. 2, chapter Silicon Carbide Junction Field Effect Transistors, pp. 75–104. DOI: 10.1142/9789812706850

[58] I. Sankin, D. C. Sheridan, W. Draper, V. Bondarenko, R. L. Kelley, M. S. Mazzola, and J. B. Casady, "Normally-off SiC VJFETs for 800 V and 1200 V power switching applications," in *Proceedings of the 20th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, Orlando, FL, USA, 18–22 May 2008, pp. 260–262. DOI: 10.1109/ISPSD.2008.4538948

[59] SemiSouth Laboratories, Inc., *Normally-On Trench Silicon Carbide Power JFET SJDA065R055*, SemiSouth Laboratories, Inc., 201 Research Boulevard, Starkville, MS 39759, USA, 2012, Rev. 1.0.

[60] SemiSouth Laboratories, Inc., *Normally-Off Trench Silicon Carbide Power JFET SJEP120R063*, SemiSouth Laboratories, Inc., 201 Research Boulevard, Starkville, MS 39759, USA, 2012, Rev. 3.0.

[61] SemiSouth Laboratories, Inc., *Normally-On Trench Silicon Carbide Power JFET SJDP120R045*, SemiSouth Laboratories, Inc., 201 Research Boulevard, Starkville, MS 39759, USA, 2012, Rev. 3.0.

[62] *Product Brief 1200 V CoolSiC™& Direct Drive Technology*, Infineon Technologies Austria AG, Villach, Austria, November 2012.

[63] SemiSouth Laboratories, Inc., *Normally-On Trench Silicon Carbide Power JFET SJDP170R1400*, SemiSouth Laboratories, Inc., 201 Research Boulevard, Starkville, MS 39759, USA, 2012, Rev. 1.0.

[64] W. Bergner, F. Bjoerk, D. Domes, and G. Deboy, *Infineon's 1200 V SiC JFET — The New Way of Efficient and Reliable High Voltages Switching*, 2011.

[65] D. C. Sheridan, K. Chatty, V. Bondarenko, and J. B. Casady, "Reverse conduction properties of vertical SiC trench JFETs," in *Proceedings of the 24th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Bruges, Belgium, 3–7 June 2012, pp. 385–388. DOI: 10.1109/ISPSD.2012.6229102

[66] D. Peftitsis, R. Baburske, J. Rabkowski, J. Lutz, G. Tolstoy, and H.-P. Nee, "Challenges regarding parallel connection of SiC JFETs," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1449–1463, March 2013. DOI: 10.1109/TPEL.2012.2206611

[67] S. Käch, "SiC-Leistungsschalterkonfigurationen für Wechselrichter in Hybridfahrzeugen und Simulation der Antriebsregelung einer PM-Synchronmaschine," Master's thesis, Power Electronic Systems Laboratory, ETH Zurich, February 2010.

[68] C. Cai, W. Zhou, and K. Sheng, "Characteristics and application of normally-off SiC-JFETs in converters without antiparallel diodes," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4850–4860, October 2013. DOI: 10.1109/TPEL.2012.2237417

[69] Cree, Inc., *C2D10120 Silicon Carbide Schottky Diode*, Cree, Inc., 4600 Silicon Drive, Durham, NC 27703, USA, October 2008, Rev. C.

[70] D. Domes and X. Zhang, "Cascode light - normally-on JFET stand alone performance in a normally-off cascode circuit," in *Proceedings of the International Power Conversion and Intelligent Motion Conference (PCIM Europe)*, Nuremberg, Germany, 4–6 May 2010, pp. 299–303.

[71] A. Ritenour, D. C. Sheridan, V. Bondarenko, and J. B. Casady, "Saturation current improvement in 1200 V normally-off SiC VJFETs using non-uniform channel doping," in *Proceedings of the 22nd International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, Hiroshima, Japan, 06–10 June 2010, pp. 361–364.

[72] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, and P. Friedrichs, "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter," in *Proceedings of the IEEE Industry Applications Society 40th Annual Meeting (IAS)*, vol. 1, Kowloon, Hong Kong, 2–6 October 2005, pp. 410–416. DOI: 10.1109/IAS.2005.1518341

[73] D. Aggeler, F. Canales, J. Biela, and J. W. Kolar, "$^{dv}/_{dt}$-control methods for the SiC JFET/Si MOSFET cascode," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 4074–4082, August 2013. DOI: 10.1109/TPEL.2012.2230536

[74] M. Treu, R. Rupp, P. Blaschitz, K. Ruschenschmidt, T. Sekinger, P. Friedrichs, R. Elpelt, and D. Peters, "Strategic considerations for unipolar SiC switch options: JFET vs. MOSFET," in *Proceedings of the 42nd IEEE Industry Applications Conference (IAS)*, New Orleans, LA, USA, 23–27 September 2007, pp. 324–330. DOI: 10.1109/07IAS.2007.10

[75] N. Springett, "Capacitor-clamped cascode normally-on SiC JFET operates as synchronous rectifier," in *Proceedings of the International Power Conversion and Intelligent Motion Conference (PCIM Europe)*, Nuremberg, Germany, 17–19 May 2011, pp. 995–999.

[76] Infineon Technologies AG, *News Release: Infineon Releases Revolutionary CoolSiC™1200 V SiC JFET Family with Direct Drive Technology: Efficiency Levels for Solar Inverters Scale New Dimensions*, Nuremberg, Germany, May 2012.

[77] CISSOID S. A., *CHT-NMOS40XX Datasheet: High-Temperature, 40 V N-channel Power MOSFET*, Rue Francqui, 3, 1435 Mont Saint Guibert, Belgium, March 2012.

[78] *High Temperature N-Channel Power FET HTNFET*, Solid State Electronics Center Honeywell, 12001 State Highway 55, Plymouth, MN 55441, Rev. D.

[79] K. Sheng, "Maximum junction temperatures of SiC power devices," *IEEE Transactions on Electron Devices*, vol. 56, no. 2, pp. 337–342, February 2009. DOI: 10.1109/TED.2008.2010605

[80] SemiSouth Laboratories, Inc., *Normally-Off Trench Silicon Carbide Power JFET SJEP120R100*, SemiSouth Laboratories, Inc., 201 Research Boulevard, Starkville, MS 39759, USA, 2012.

[81] R. L. Kelley, A. Ritenour, D. Sheridan, and J. Casady, "Improved two-stage dc-coupled gate driver for enhancement-mode SiC JFET," in *Proceedings of the 25th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Palm Springs, CA, USA, 21–25 February 2010, pp. 1838–1841. DOI: 10.1109/APEC.2010.5433483

[82] SemiSouth Laboratories, Inc., *Two-Stage Opto Coupled Gate Driver Demo Board*, SemiSouth Laboratories, Inc., 201 Research Boulevard, Starkville, MS 39759, USA, February 2010, Rev. 1.2.

[83] SemiSouth Laboratories, Inc., "Application note AN-SS05: Operation and intended use of the SGDR2500P2 dual-stage driver board," SemiSouth Laboratories, Inc., 201 Research Boulevard, Starkville, MS 39759, USA, April 2011.

[84] SemiSouth Laboratories, Inc., "Application note AN-SS01: Silicon carbide enhancement-mode junction field effect transistor and recommendation for use," SemiSouth Laboratories, Inc., 201 Research Boulevard, Starkville, MS 39759, USA, 2009.

[85] R. L. Kelley, R. Fenton, and D. Schwob, "Optimized gate driver for enhancement-mode SiC JFET," in *Proceedings of the International Power Conversion and Intelligent Motion Conference (PCIM Europe)*, Nuremberg, Germany, 12–14 May 2009, pp. 342–347.

[86] R. L. Kelley, M. S. Mazzola, S. Morrison, W. Draper, I. Sankin, D. Sheridan, and J. Casady, "Power factor correction using an enhancement-mode SiC JFET," in *Proceedings of the 39th IEEE Annual IEEE Power Electronics Specialists Conference (PESC)*, Rhodes, Greece, 15–19 June 2008, pp. 4766–4769. DOI: 10.1109/PESC.2008.4592724

[87] M. S. Mazzola and R. L. Kelley, "Application of a normally off silicon carbide power JFET in a photovoltaic inverter," in *Proceedings of the 24th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Washington, DC, USA, 15–19 February 2009, pp. 649–652. DOI: 10.1109/APEC.2009.4802728

[88] C. Wilhelm, D. Kranzer, and B. Burger, "Development of a highly compact and efficient solar inverter with silicon carbide transistors," in *Proceedings of the 6th International Conference on Integrated Power Electronics Systems (CIPS)*, Nuremberg, Germany, 16–18 March 2010, pp. 297–302.

[89] S.-H. Ryu, S. Krishnaswami, M. O'Loughlin, J. Richmond, A. Agarwal, J. Palmour, and A. R. Hefner, "10-kV, 123-mΩ·cm^2 4H-SiC power DMOSFETs," *IEEE Electron Device Letters*, vol. 25, no. 8, pp. 556–558, August 2004. DOI: 10.1109/LED.2004.832122

[90] Cree, Inc., *CMF20120D Silicon Carbide Power MOSFET*, Cree, Inc., 4600 Silicon Drive, Durham, NC 27703, USA, 2012, Rev. D.

[91] *14 Ampere Low-Side Ultrafast MOSFET Drivers*, IXYS Corporation, 3540 Bassett Street, Santa Clara, CA 95054, USA, 2006.

[92] *International Rectifier 10BQ060*, International Rectifier, 233 Kansas Street, El Segundo, CA 90245, USA, July 2004, Rev. G.

[93] *International Rectifier 10MQ040N*, International Rectifier, 233 Kansas Street, El Segundo, CA 90245, USA, July 2004, Rev. A.

[94] *thinQ!TM SiC Schottky Diode IDH15S120*, Infineon Technologies AG, 81726 Munich, Germany, April 2010, Rev. 2.0.

[95] S. Lineykin and S. Ben-Yaakov, "A simple and intuitive graphical approach to the design of thermoelectric cooling systems," in *37th IEEE Power Electronics Specialists Conference (PESC)*, Jeju, South Korea, 18–22 June 2006, pp. 1–5. DOI: 10.1109/PESC.2006.1712075

[96] S. Lineykin and S. Ben-Yaakov, "Modeling and analysis of thermoelectric modules," *IEEE Transactions on Industry Applications*, vol. 43, no. 2, pp. 505–512, March – April 2007. DOI: 10.1109/TIA.2006.889813

[97] J. Biela and J. W. Kolar, "Thermoelectric cooling for power density maximisation of power electronic converters," in *Proceedings of the 6th International Conference on Integrated Power Electronics Systems (CIPS)*, Nuremberg, Germany, 16–18 March 2010, pp. 17–36.

[98] J. Biela, M. Schweizer, S. Waffler, B. Wrzecionko, and J. W. Kolar, "SiC vs. Si — evaluation of potentials for performance improvement of power electronics converter systems by SiC power semiconductors," in *Proceedings of the 13th International Conference on Silicon Carbide and Related Materials (ICSCRM)*, Nuremberg, Germany, 11–16 October 2009, pp. 1101–1106. DOI: 10.4028/www.scientific.net/MSF.645-648.1101

[99] J. W. Kolar and S. D. Round, "Analytical calculation of the rms current stress on the dc-link capacitor of voltage-PWM converter systems," *IEE Proceedings – Electric Power Applications*, vol. 153, no. 4, pp. 535–543, 2006.

[100] Epcos AG, *Aluminum electrolytic capacitors - axial lead and soldering star capacitors, Series B43693, B43793*, November 2008.

[101] U. Drofenik, G. Laimer, and J. W. Kolar, "Theoretical converter power density limits for forced convection cooling," in *Proceedings of the International Power Conversion and Intelligent Motion Conference (PCIM Europe)*, Nuremberg, Germany, 7–9 June 2005, pp. 608–619.

[102] *Frenzelit Novaplan 02980 - Technical Data Sheet*, Frenzelit-Werke GmbH Co. KG, P. O. Box 1140, 95456 Bad Berneck, Germany, August 2012.

[103] *Loctite 5399 - Technical Data Sheet*, Henkel AG & Co. KGaA, Henkelstrasse 67, 40589 Düsseldorf, Germany, November 2004.

[104] *Quick-Cool QC-31-1.4-8.5M Peltier Cooler*, Quick-Ohm Küpper & Co. GmbH, Unterdahl 24B, 42349 Wuppertal, Germany.

[105] *Cooling Systems - Technical Material*, Sanyo Denki Co., Ltd., 1-15-1, Kita-otsuka, Toshima-ku, Tokyo 170-8451, Japan.

[106] *High Temperature Fans*, EVG Elektro-Vertriebs-Gesellschaft Martens GmbH & Co. KG, Trompeterallee 244-246, 41189 Mönchengladbach, Germany.

[107] U. Drofenik, A. Stupar, and J. W. Kolar, "Analysis of theoretical limits of forced-air cooling using advanced composite materials with high thermal conductivities," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 1, no. 4, pp. 528–535, April 2011. DOI: 10.1109/TCPMT.2010.2100730

[108] *San Ace 40 GV*, Sanyo Denki Co., Ltd., 1-15-1, Kita-otsuka, Toshima-ku, Tokyo 170-8451, Japan.

[109] G. Tan, "Fundamentals of brushless dc axial cooling fans," Sanyo Denki Co., Ltd., 468 Amapola Avenue, Torrance, California, 90501, USA, March 2008.

[110] ebm Industries, Inc., "Motor design, quality and performance are critical to reliable operation of fans & blowers," ebm Industries, Inc., 1999.

[111] K. Stephan and P. Stephan, *Taschenbuch für den Maschinenbau*, 22nd edition. Berlin Heidelberg: Springer-Verlag, 2007, chapter D Thermodynamik, p. D 10. DOI: 10.1007/978-3-642-64925-7

[112] M. Hecht, T. Keilig, U. Kleemann, O. Polach, U. Seiffert, and R. Voit-Nitschmann, *Taschenbuch für den Maschinenbau*, 22nd edition. Springer-Verlag, 2007, chapter Q Fahrzeugtechnik, p. Q 86. DOI: 10.1007/978-3-642-64925-7

[113] K. Stephan and P. Stephan, *Taschenbuch für den Maschinenbau*, 22nd edition. Berlin Heidelberg: Springer-Verlag, 2007, chapter D Thermodynamik, p. D 15. DOI: 10.1007/978-3-642-64925-7

[114] W. Wagner, *Lufttechnische Anlagen: Ventilatoren und Ventilatoranlagen*, 2nd edition. Würzburg, Germany: Vogel Buchverlag, 1997, ISBN: 978-3-8343-3095-6.

[115] P. L. Chapman and P. T. Krein, "Micromotor technology: electric drive designer's perspective," in *Proceedings of the 36th IEEE Industry Applications Conference (IAS)*, vol. 3, Chicago, IL, USA, 30 September – 4 October 2001, pp. 1978–1983. DOI: 10.1109/IAS.2001.955899

[116] U. Kafader and J. Schulze, "Similarity relations in electromagnetic motors - limitations and consequences for the design of small dc motors," in *9th International Conference on New Actuators (ACTUATOR)*, Bremen, Germany, 14–16 June 2004, pp. 309–312.

[117] Elektrisola. Enamelled copper wire acc to IEC - Europe. Online. Elektrisola Dr. Gerd Schildbach GmbH & Co. KG. In der Hüttenwiese 2–4, 51580 Reichshof-Eckenhagen, Germany. September 2011.

[118] Pack Feindrähte. Technical data table for fine wires. Online. Rudolf Pack GmbH & Co. KG. Am Bäuweg 9–11, 51645 Gummersbach, Germany. September 2011.

[119] Karl Schupp AG, *Winding wires with ceramic insulation*, Wilhofstrasse 3, 8125 Zollikerberg, Switzerland, Version 2.2.

[120] *Ceramawire High Temperature Magnet Wire Technical Specifications*, Ceramawire, 786 Pitts Chapel Rd., Elizabeth City, NC 27909, USA.

[121] R. B. Ross, *Metallic Materials Specification Handbook*, 4th edition. Chapman & Hall, 2-6 Boundary Row, London SE1 8HN, UK, 1992, ISBN: 978-0412369407.

[122] J. R. Howell, "Composite wires for operation as electrical conductors at elevated temperatures," in *Proceedings of the 7th Annual Wire and Cable Symposium*, Ashbury Park, NJ, USA, 2–4 December 1958.

[123] P. Ning, F. Wang, and K. D. T. Ngo, "250 °C SiC high density power module development," in *Proceedings of the 26th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Ft. Worth, TX, USA, 6–10 March 2011, pp. 1275–1281. DOI: 10.1109/APEC.2011.5744757

[124] J. R. Leehey, L. Kushner, and W. S. Brown, "DC current transformer," in *Proceedings of the 13th Annual Power Electronics Specialists Conference (PESC)*, Cambridge, MA, USA, 14–17 June 1982, pp. 438–444.

[125] D. Azzoni, W. Teppan, and M. Carpita, "An innovative low-cost, high performance current transducer for battery monitoring applications: Prototype preliminary results," in *Proceedings of the International Power Conversion and Intelligent Motion Conference (PCIM Europe)*, Nuremberg, Germany, 12–14 May 2009, pp. 443–449.

[126] J. A. Houldsworth, "Purpose-designed ferrite toroids for isolated current measurement in power electronic equipment," in *Proceedings of the 4th Annual Power Conversion International Conference (PCI)*, San Francisco, CA, USA, 29–31 March 1982, pp. 101–109.

[127] L. Steinmann, "Strommessung für Hochtemperaturumgebungen in Hybrid- und Elektrofahrzeugen," Master's thesis, Power Electronic Systems Laboratory, ETH Zurich, May 2011.

[128] *Nanocrystalline Vitroperm EMC Products*, Vacuumschmelze GmbH & Co. KG, Grüner Weg 37, 63450 Hanau, Germany, 2010.

[129] Vishay Intertechnology, Inc., *Dual N-Channel 60 V (D-S) 175° C MOSFET*, Vishay Intertechnology, Inc., 63 Lancaster Avenue Malvern, PA 19355-2143, USA, 16 November 2009.

[130] Allegro MicroSystems, Inc., *Automotive Full Bridge MOSFET Driver*, Allegro MicroSystems, Inc., 2009, Rev. 1.

[131] *Celeroton Converter CC-75-400*, Celeroton AG, Technoparkstrasse 1, 8005 Zurich, Switzerland, February 2012.

[132] *Binder FD series 53 Drying ovens / Heating ovens*, Binder GmbH, Im Mittleren Ösch 5, 78532 Tuttlingen, Germany, January 2013.

[133] H. Iwase, O. Itou, and K. Tachibana, *WT3000 Precision Power Analyzer*, Yokogawa Electric Corporation, 9-32, Nakacho 2-chome, Musashino-shi, Tokyo 180-8750, Japan, 2005.

[134] *Technical Material*, Sanyo Denki Co., Ltd., 1-15-1, Kita-otsuka, Toshima-ku, Tokyo 170-8451, Japan.

[135] G. Jones, "Noise effects of cooling fans and its measurement," ebm-papst Automotive & Drives (UK) Ltd, The Smithy, Fidlers Lane, RG20 7LG East Ilsley, Berkshire, UK, 2011.

[136] *Miniature Bellow Coupling Model MK2 - Technical Specifications*, R+W Antriebselemente GmbH, Alexander-Wiegand-Strasse 8, 63911 Klingenberg, Germany.

[137] *TM 301 – TM 308. In-Line Torque Transducers.*, Magtrol, Inc., 70 Gardenville Parkway, Buffalo, New York 14224, USA, June 2009.