Optimal Design of a 3.5 kV/11 kW DC-DC Converter for Charging Capacitor Banks of Power Modulators

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Abstract—For the generation of short high power pulses in many applications, power modulators based on capacitor discharge are used, where the peak power is drawn from the input capacitor bank. In order to continuously recharge the energy buffer during operation at a lower average power, usually power supplies connected to the mains are used. Due to the worldwide variation in mains voltages and the desired ability to adapt the capacitor voltage of the modulator, the power supply has to support a wide input and output voltage range, whereby the supply should draw a sinusoidal current from the mains due to EMI regulations. Additionally, depending on the modulator concept also a galvanic isolation has to be provided. In order to achieve the mentioned specifications for the considered power supply a combination of a AC-DC and DC-DC converter is proposed, whereas the mains voltage is rectified by a three-phase buck-boost converter to 400Vdc and thereafter an isolated DC-DC converter charges the input capacitor bank of the power modulator up to 3.5 kV. This paper focuses on the basic operation and the design of the 3.5kV/11kW isolated DC-DC converter, which includes transformer design, efficiency-volume optimization and components selection. There, compared to the well-known flyback converter the proposed full-bridge based topology results in a much higher efficiency and power density.

I. INTRODUCTION

Usually, in power modulators based on capacitor discharge, the energy buffer is continuously recharged during operation at a lower average power by a power supply connected to the mains. In order to enable a worldwide operation the AC-DC converter has to provide a wide input range, which can vary from 177 V to 528 V [1]. Due to this worldwide variation in mains voltages, the desired ability to adapt the capacitor voltage of the modulator from 0 V to 3.5kV, and the specified galvanic isolation between the converter output and the mains, for the power supply a combination of a AC-DC and DC-DC converter is proposed in this paper, as shown in Fig. 1.

There, the mains voltage is rectified by a three-phase buck-boost converter to the voltage V_{in} [1] and thereafter an isolated, full-bridge based DC-DC converter charges the input capacitor bank of the power modulator up to 3.5kV. The voltage V_{in} of the 3.5kV/11kW isolated, full-bridge



Figure 1: Block diagram of the charging unit, consisting of a three-phase AC-DC and a DC-DC converter, which interconnects the power modulator to the mains.

TABLE I: Specifications of the isolated DC-DC converter.

Parameter	Nominal value	Incl. range
Input voltage V_{in}	400 V	350450 V
Output voltage V_{out}	3500 V	31503850 V
Max output power P_{out}	11 kW	15 kW
Switching frequency $f_s=1/T_s$	30 kHz	-

based DC-DC converter is set to 400 Vdc, in order to use 600 V IGBT modules, which show the best performance regarding switching frequency and switching losses at these power levels.

In Table I the nominal specifications of the isolated DC-DC converter are given. Additionally, for the considered application the isolated DC-DC converter should also be able to deliver the nominal output power of 11 kW when a variation of the input and output voltage of $\pm 10\%$ is taken into account, which results at the nominal operating point in a maximum output power of 15 kW (cf. Table I).

This paper focuses on the operation and the design of the 3.5 kV/11 kW isolated, full-bridge based DC-DC converter, which includes the design of a high-frequency transformer, efficiency-volume optimization of the converter and the components selection like semiconductor switches or core materials. In Section II the basic operation principle of the full-bridge based converter is explained in detail. This operation is later translated into a converter model described by analytic equations in Section III. With these equations, in Section IV the DC-DC converter is optimized for minimal volume/losses whereas the resulting design performance, the final transformer/converter design, and experimental results are presented in Section V. As will be shown in Section V, compared to the well-known twoswitch flyback converter [2,3] the proposed full-bridge based DC-DC converter results in a much higher efficiency and power density.

II. CONVERTER OPERATION

In this section the basic operation and the modulation of the full-bridge based DC-DC converter, shown in Fig. 2, are explained in detail. Additionally, the design equations of the DC-DC converter will be derived for the main components like transformer and semiconductors. Thereafter, the design of the converter can be optimized concerning efficiency and power density.

A. Topology

The considered full-bridge topology (cf. Fig. 2) can be divided into three parts: the input stage, the HF-transformer



Figure 2: Schematic of the isolated, full-bridge based DC-DC converter.

and the rectifier stage. The inverter stage, which is a fullbridge configuration, consists of the four switches $T_1 - T_4$. At the input the full-bridge is connected to the DC voltage V_{in} (cf. Fig. 2). In order to provide the galvanic isolation and to step-up the input voltage V_{in} , a transformer is required. In addition to the transformer a series inductance is needed to enable the power transfer and to ensure soft switching of the four switches. The rectifier stage consists of the two diodes D_1 and D_2 as well as of the two capacitors C_1 and C_2 . There, the diodes D_1 and D_2 must be able to block the whole output voltage V_{out} , whereas the capacitors C_1 and C_2 are only charged to the half of the output voltage V_{out} (voltage doubler).

B. Basic operation principle

The operation of the full-bridge based DC-DC converter is now described upon the waveforms shown in Fig. 3.

In order to enable power transfer, the input voltage V_{in} has to be larger than the reflected output voltage $V'_{out} = V_{out}/2n$. In this case, when T_1 and T_4 are switchedon at the beginning of one switching cycle, the voltage at the output of the full-bridge equals the DC voltage V_{in} and due to $V_{in} > V_{out}/2n$ the diode D_1 starts to conduct. Consequently, at the transformer's input terminals the voltage V'_{out} is clamped to $V_{out}/2n$. Therefore, the difference between the reflected voltage V'_{out} and the DC input voltage V_{in} is applied to the series inductance L_s . If



Figure 3: Qualitative operation waveforms of the full-bridge based DC-DC converter.

constant input and output voltages are assumed, this leads to a linearly increasing current $i_{p1}(t)$ through the series inductance L_s and the load (cf. Fig. 3).

$$i_{p1}(t) = n \cdot i_{s1}(t) = \frac{V_{in} - V_{out}/(2n)}{L_s}t$$
 (1)

At the time instant DT_s the transistor T_1 is turned off and the current $i_p 1$ commutates to the antiparallel diode of T_3 . After a certain interlocking delay the switch T_3 can be turned on, whereby soft switching (ZVS) is achieved. Consequently, the voltage at the output of the full-bridge is zero and the reflected output voltage V'_{out} is fully applied to the series inductance L_s , which results in a linearly decreasing current $i_{p2}(t)$ (cf. Fig. 3).

$$i_{p2}(t) = i_{s2}(t)n = i_{1p}(DT_s) - \frac{V_{out}/(2n)}{L_s}t$$
 (2)

In the following, the converter is operated in discontinuous conduction mode, which means, that the current $i_{p2}(t)$ will reach zero before $t = T_s/2$. Thereby, the current $i_{p2}(t)$ stays at zero until the second half period is started at $T_s/2$ and switch T_4 can be turned off. The operation during $T_s/2 - T_s$ is analogous to $0 - T_s/2$, whereas, in order to obtain a negative primary current, the switches T_2 and T_3 are turned on. Accordingly, at $T_s/2 + DT_s$ switch T_3 is turned off and T_1 is turned on. There, only the reflected output voltage V'_{out} is applied to the transformer, which results in a linearly increasing current until it reaches zero.

III. CONVERTER MODEL

The first step in the design flow is to consider the design conditions shown in Table I. The degrees of freedom must be identified which in this case are: the turns ratio n, the transformer core geometry, the characteristics of the copper in primary and secondary regarding thickness or diameter.

A model of the losses in the semiconductors and in the transformer is now necessary to choose the appropriate values for each of the degrees of freedom. The first equations to be considered are (1), and (2). Equations to obtain the value of the duty cycle, the series inductance, the transformer losses and the semiconductors losses will be determined now.

A. Duty cycle

The described operation of the full-bridge converter allows to obtain an expression for the required duty cycle D depending on the operation conditions and the construction parameters.

Assuming discontinuous conduction mode, the freewheeling time t_{fw} , in which the current i_{p2} decreases towards zero, can be deduced from (1) and (2).

$$i_{p2}(t_{fw}) = i_{p1}(DT_s) - \frac{V_{out}/(2n)}{L_s} t_{fw} = 0$$

$$\Rightarrow \quad t_{fw} = \frac{V_{in} - V_{out}/(2n)}{V_{out}/(2n)} DT_s$$
(3)

Therewith, the output average current \bar{I}_{out} can be calculated by integrating the output current $i_s(t)$, which is given

by the primary current i_{p1} respectively i_{p2} and the turns ratio n.

$$\bar{I}_{out} = \frac{1}{T_s} \left(\int_0^{DT_s} \frac{i_{p1}(t)}{n} dt + \int_0^{t_{fw}} \frac{i_{p2}(t)}{n} dt \right)$$
$$= \frac{1}{2} \frac{(2V_{in}n - V_{out})V_{in}T_s}{nV_{out}L_s} D^2 = \frac{P_{out}}{V_{out}}$$
(4)

Hence, for a given output power P_{out} the duty cycle D can be obtained.

$$D = \frac{\sqrt{2V_{in}(2V_{in}n - V_{out})(1/T_s)nL_s}}{V_{in}(2V_{in}n - V_{out})} \sqrt{P_{out}}$$
$$= K \cdot \sqrt{P_{out}}$$
(5)

B. Series Inductance

The value of the series inductance L_s has to be kept below a certain value, since the converter will be operated in the discontinuous conduction mode within the whole operating range. Therefore, the sum of the duration of the duty cycle time DT_s and the freewheeling time t_{fw} has to be shorter than the $T_s/2$, whereas the parameter k = 0.95is used to establish an operation margin.

$$DT_s + t_{fw} = k \frac{T_s}{2} < \frac{T_s}{2} \tag{6}$$

Using (3), (5) and (6) the expression for the series inductance L_s can be determined.

$$L_s = \frac{1}{32} \frac{T_s k^2 V_{out}^2 (2V_{in}n - V_{out})}{V_{in} P_{out} n^3}$$
(7)

As can be seen from (7), the value of the series inductance L_s depends on the turns ratio n. As already mentioned, in order to enable power transfer, the input voltage V_{in} has to be larger than the reflected output voltage V'_{out} , which is $V_{out}/2n$. Considering the specifications given in Table I this results in a minimum turns ratio of $n_{min} = 6$. However, since for the following converter design the series inductance L_s will be partly integrated into the transformer, a final transformer design is necessary.

C. Transformer losses model

In order to determine the number of turns N_{pri} and the turns ratio n, the transformer will be optimized regarding the minimum transformer losses. There, the copper losses due to skin and proximity effects as well as the core losses have to be taken into account.

For the converter operation described previously, the maximum flux density \hat{B} can be found with the voltagetime product during the interval $0 - T_s/2$, where A_e is the effective cross sectional.

$$\hat{B} = \frac{V_{in}DT_s}{2N_{pri}A_e} + \frac{V_{out}t_{fw}}{4N_{pri}A_en} \tag{8}$$

The expression in (8) can now be solved for the number of turns N_{pri} in the primary, which yields:

$$N_{pri} = \frac{2V_{in}DT_s + V_{out}t_{fw}}{4\hat{B}A_e} = \frac{N_{sec}}{n} \tag{9}$$

Using (9), for a given transformer/core geometry the resulting conduction losses in the primary and secondary due skin and proximity effects can now be calculated either for foils depending on the foil thickness or for litz wires depending on the litz diameter and the number of strands [4, 5].

The core losses are calculated by using the Steinmetz equation for non-sinusoidal waveforms [6], whereas the Steinmetz parameter are extracted from the core manufacturer's datasheets.

D. Semiconductors losses model

In order to determine the switching and conduction losses of the IGBT modules and the diodes, data regarding output characteristics, turn-off energy, and reverse recovery, in the case of the diodes, is necessary. For the calculation of the switching losses only the hard switching transitions are considered. According to the converter operation explained in section II, hard switching occurs during turnoff for switch T_1 at DT_s respectively for switch T_3 at $T_s/2+DT_s$. Therefore, only two hard switching transitions has to considered during one switching period (cf. (10)). Additionally, the duration of conduction for each switch is assumed to be equal, which results in four times the conduction losses of one switch (cf. (11)).

$$P_{sw} = 2E_{off}(\hat{I}_C, v_{CE}) \cdot f_s \tag{10}$$

$$P_{con} = 4 \frac{1}{T_s} \int_0^{T_s} v_{CE}(I_C(t)) \cdot I_C(t) dt$$
(11)

There, $E_{off}(\hat{I}_C, v_{CE})$ is the hard switching turn-off loss energy for a given collector current \hat{I}_C and collectoremitter voltage v_{CE} . This information as well as the output characteristic $v_{CE}(I_C)$ is extracted from the IGBT datasheet.

Accordingly, the conduction losses for the output diodes are calculated in a same way as for the switches and the reverse recovery losses were calculated as described in [7].

IV. PARAMETER OPTIMIZATION AND DESIGN

Since the converter should operate in a wide power and voltage range (cf. Table I), different components of the converter have to be designed for different operating points, where their critical conditions are encountered. For example, in order to be able to transfer the specified power and to solely operate the converter in DCM, the series inductance has to be designed for the lowest input voltage and the highest output voltage, because in this point the lowest voltage is applied to the inductance. On the other hand, the highest input voltage results in highest semiconductor's losses as in this operating point the highest peak currents are obtained. Therefore, also the heat sink for these components should be designed for the same operating point. Consequently, a wide operating range reduces the maximum reachable efficiency and power density, since not all components can be optimized for a single operating point.

Due to stringent requirements regarding high converter efficiency, a HF-transformer concept employing E-cores (EPCOS E80/38/20 N87), according to Fig. 4, is selected. Ferrite core material is used, since it shows excellent highfrequency performance and enables a compact transformer design. In order to achieve the needed core area A_e , a certain number of core pairs N_{set} have to be stacked. For the primary a 35 mm wide copper foil and for the secondary a litz wire are employed. Due to the high output voltage, the output stage of the converter is built using four series connected rectifiers, whereas each rectifier is connected to an independent secondary winding. This results in a maximum output voltage of 963 V per diode respectively 482 V per capacitor. Additionally, in the transformer design the four secondary windings are embedded in a chambered bobbin in order to perform proper isolation (cf. Fig. 4).

Depending on the number of core pairs N_{set} , the turns ratio n, the copper foil thickness $d_{cu,p}$, and the secondary litz diameter $d_{cu,s}$ the converter can now be optimized regarding a low loss design in the whole operating range with the given transformer geometry.

According to Fig. 5 for the given specifications (cf. Table I), the lowest loss design, with respect to the whole operation range, is obtained for n = 7 and $N_{set} = 4$. For a maximum flux density of $\hat{B} = 250 \text{ mT}$, the number of turn for the primary and secondary is given with (9) to $N_p = 7$ and $N_s = 49$.

Considering (7), this leads to a maximum allowed series inductance of $L_s = 7.93 \,\mu\text{H}$, in order to operate the converter solely in DCM. Hence, using (1) and (5), the resulting peak current at DT_s for maximum input voltage and maximum power equals $\hat{i}_p = 131 \,\text{A}$ for the primary, respectively $\hat{i}_s = 18 \,\text{A}$ for the secondary. With this configuration the optimal foil thickness of the primary winding is $d_{cu,p} = 100 \,\mu\text{m}$. The optimal litz wire of the secondary winding consists of 420 strands with a diameter of $d_{cu,s} = 71 \,\mu\text{m}$ (Pack RUPALIT) [8].

Since the converter optimization is mainly determined by the transformer losses, for the switches and diodes, semiconductor devices with low switching respectively low reverse recovery losses have been selected.



Figure 4: Cross sectional view of the transformer.



Figure 5: Overall losses for different output voltages and turns ratio.

There, for each half bridge $(T_1\&T_3$ respectively $T_2\&T_3)$ two parallel connected 600 V half bridge IGBT-modules with non punch through technology and positive temperature coefficient (Vishay GB100TS60NPbF) are used, whereas each module can handle 40 Adc at 100 C°. For the output rectifiers fast recovery diodes (IXYS DSEP 8-12A) with a blocking capability of 1200 V and a DC current of 10 A were selected.

Due to the high current ripple, for the voltage stabilization at the input and output, film capacitor are employed, where the allowed maximum voltage ripple is specified to ± 5 %. This results in a total input and output capacitance of 200 µF respectively 170 nF. As a result of the series connection of four output rectifiers, which leads to a series connection of eight output capacitors, for each capacitor a value of 1.36 µF is needed, so 1.5 µF is suitable.

In order to partly integrate the series inductance L_s into the transformer, the leakage inductance was calculated as described in [9, 10]. The maximum achievable leakage inductance for the given transformer geometry is $L_{lk} = 2.09 \,\mu\text{H}$, which is 5.84 μH less than the required series inductance L_s . For that reason, an additional pair of E-cores was added to the transformer, whereas only the secondary is wound around the additional cores. By adjusting the air gap between these two cores, the required series inductance L_s can be obtained.

In Table II the design values of the optimized full-bridge based converter are summarized.

Accordingly, in Fig. 6 a picture of the designed prototype is shown. The size of the converter is defined by the two 120 mm fans in the front of the converter. One of these fans is attached to a 120x120x200 mm heat sink, on which the four IGBT-modules are mounted. The transformer is placed next to the heat sink, so it receives enough air flow from the second fan. Finally, the converter is covered with the PCB, which comprises the control and measurement electronics as well as the connections for the power electronic components.

To perform proper isolation for the transformer, the four secondary windings are enclosed by a chambered bobbin as shown in Fig. 4. Due to the tight construction, the windings are confined to small unventilated spaces, whereby a special cooling concept has to be incorporated. There, the cooling

TABLE I	I: Design	values	of the	optimized	full-bridge
		con	verter.		

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Parameter	Value
Series inductance L_s	7.93 μH
Maximum primary RMS current i_p, rms	58 A
Maximum primary peak current \hat{i}_p	131 A
Core material	E80/38/20 N87 E core
Number of cores pairs N_{set}	4+1
Maximum flux \hat{B}	250 mT
Turns ratio n	7
Turns primary N_p	7
Turns secondary N_s	49
Secondary windings	4
Pri. foil width/thickness $c_{cu,p} / d_{cu,p}$	35 mm / 0.1 mm
Sec. litz number/diameter $n_{ls} / d_{cu,s}$	420 / 0.71 mm
Leakage inductance L_{lk}	2.09 µH
Transformer volume	$0.616 \mathrm{dm^3}$
IGBT module	Vishay GB100TS60NPbF
Output diodes	IXYS DSEP 8-12A
Input capacitor type/capacitance	Film / unit[200]µF
Output capacitor type/capacitance (each)	Film / 8x1.5 μF
Overall volume	9 dm ³



Figure 6: Picture of the designed 3.5 kV/11 kW isolated full-bridge based DC-DC converter.

of the primary is achieved by inserting a bent copper plate between the bobbin and the winding (cf. Fig. 4). This copper piece conducts the heat to extruded heat sinks on the top and bottom of the transformer. With this cooling mechanism, for maximum copper losses in the primary (63 W), a temperature rise of $42 \,^{\circ}$ C is expected.

V. CONVERTER PERFORMANCE AND EXPERIMENTAL RESULTS

A. Efficiency and Loss Distribution

Based on the design performed in the previous section, the theoretical efficiency of the converter is shown in Fig. 8 considering the whole input and output voltage range at full output power.

The highest efficiency of about 97% is achieved at lowest input and highest output voltage ($V_{in} = 350$ V and $V_{out} = 3850$ V), due to the lowest output current and the lowest peak currents at this operating point. As a result of the increasing peak current for higher input and lower output voltages, the switching losses in the IGBT modules



Figure 7: Final transformer: Height: 115 mm, Width: 90 mm, Length: 165 mm.



Figure 8: (a) Efficiency of the converter in the whole input and output voltage range and (b) loss distribution for the two operating points $V_{in} = 350$ V, $V_{out} = 3850$ V and $V_{in} = 450$ V, $V_{out} = 3850$ V at maximum output power.

increase about 13 % (35 W) and therefore the efficiency decreases. Due to the same reason, also the copper losses in primary and secondary windings increase. Consequently, in the worst case, at $V_{in} = 450$ V and $V_{out} = 3150$ V, an efficiency of around 96.2 % is obtained.

In addition to the efficiency, Fig. 8 shows the loss distribution for the two operating points ($V_{in} = 350$ V, $V_{out} = 3850$ V and $V_{in} = 450$ V, $V_{out} = 3850$ V) at maximum output power. There, it can be seen that the IGBTs contribute with the largest portion of the overall converter losses for either operating point.

In Table III the loss distribution of the optimized fullbridge based converter is summarized. Additionally, compared to the well-known two-switch flyback converter (cf. Fig 9), the proposed full-bridge based topology results in a much higher efficiency and power density.



Figure 9: Schematic of the two switch flyback converter.

TABLE III: Characteristics of the optimized full-bridge and the flyback converter.

Parameter	Full-bridge	Flyback
Maximum primary RMS current Ip,rms	58 A	66 A
Maximum primary peak current \hat{I}_p	131 A	202 A
Maximum IGBT losses	250 W	421 W
Maximum output diodes losses	71 W	55 W
Turns ratio n	7	12
Maximum primary copper losses	63 W	42.92 W
Maximum secondary copper losses	48 W	41 W
Maximum core losses	96 W	223 W
Number of cores pairs N_{set}	4+1	12
Transformer volume	$0.63 dm^3$	$1.5 \mathrm{dm}^3$
Secondary windings	4	8

The considerable differences observed in peak currents are unavoidable, since the flyback is based on storing energy in the core during DT_s and providing it to the load during T_{fw} , whereas the full-bridge based converter transfers power during DT_s and t_{fw} . Therefore, larger peak currents increase the transformer losses and would have to be switched off by the two input switches, which also results in a larger heat sink and lower power density. In addition, the required number of secondary windings would increase from four to eight, if the same blocking voltage of the diodes is assumed. However, the number of diodes would be the same, since each output rectifier of the fullbridge requires two diodes compared to one diode for the flyback converter.

B. Experimental Results

In Fig. 10 the experimental results for an input and output voltage of $V_{in} = 400$ V and $V_{out} = 3850$ V at an output power of $P_{out} = 1800$ W is shown.

As can be seen, the current and voltage waveforms at the primary follow closely the behavior described in Fig. 3. The waveforms shown in Fig. 10-b) are measured from one of the four secondaries of the transformer. Here it can be seen that the secondary currents and voltages suffer from oscillations when the current reaches zero, which is mainly due to the reverse recovery effects and junction capacitances.

VI. CONCLUSION

In this paper the operation, design and optimization of a 3.5 kV/11 kW isolated full-bridge based DC-DC converter is presented. There, a complete model of the converter, focused on the transformer design, efficiency-volume optimization and component selection, was carried out. For the design of the transformer a special cooling concept



Figure 10: Experimental waveforms: (a) Primary voltage and current; (b) Voltage and current of one secondary.

is incorporated, due to the high output voltage and the needed isolation. Additionally, in order to obtain a high power density (1.54 kW/dm^3) the needed series inductance L_s of the converter is partly integrated into the transformer. With the presented design, a theoretical efficiency of 97% is achieved. The efficiency and the power density of the converter were affected by the given operating range as each component was designed for a different operating point. As shown in the paper, compared to the well-known flyback converter, the proposed full-bridge based topology results in a much higher efficiency and power density.

REFERENCES

- D. Bortis, S. Waffler, J. Biela, and J. W. Kolar, "25kW 3-phase unity power factor buck boost rectifier with wide input and output range for pulse load applications," in *Proc. 16th IEEE International Pulsed Power Conference*, vol. 2, 17–22 June 2007, pp. 1505–1508.
- [2] F. Wang, A. Kuthi, and M. A. Gundersen, "Compact high repetition rate pseudospark pulse generator," vol. 33, no. 4, pp. 1177–1181, Aug. 2005.
- [3] J. Elmes, C. Jourdan, O. Abdel-Rahman, and I. Batarseh, "Highvoltage, high-power-density DC-DC converter for capacitor charging applications," in *Proc. Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition APEC 2009*, 15–19 Feb. 2009, pp. 433–439.
- [4] J. Biela, U. Badstuebner, and J. W. Kolar, "Design of a 5-kW, 1-U, 10-kW/dm³ resonant DC-DC converter for telecom applications," vol. 24, no. 7, pp. 1701–1710, July 2009.
- [5] U. Badstuebner, J. Biela, and J. W. Kolar, "Power density and efficiency optimization of resonant and phase-shift telecom DC-DC converters," in *Proc. Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition APEC 2008*, 24–28 Feb. 2008, pp. 311–317.
- [6] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *Proc. IEEE Workshop* on Computers in Power Electronics, 3–4 June 2002, pp. 36–41.
- [7] K. A. Alberto Guerra and S. Fimiani, "Ultra-fast recovery diodes meet todays requirements for high frequency operation and power ratings in smps applications," International Rectifier, Tech. Rep., 2000.
- [8] C. R. Sullivan, "Optimal choice for number of strands in a litz-wire transformer winding," vol. 14, no. 2, pp. 283–291, March 1999.
 [9] D. Aggeler, J. Biela, and J. W. Kolar, "A compact, high voltage
- [9] D. Aggeler, J. Biela, and J. W. Kolar, "A compact, high voltage 25 kW, 50 kHz DC-DC converter based on sic jfets," in *Proc. Twenty-Third Annual IEEE Applied Power Electronics Conference* and Exposition APEC 2008, 24–28 Feb. 2008, pp. 801–807.
- [10] E. R. and M. D., Fundamehntals of Power Electronics. Springer Science+Business Media, LLC, 2001.