A New Single-Phase PFC Rectifier (*TOKUSADA Rectifier*) with Wide Output Voltage Control Range and High Efficiency

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ABSTRACT - This paper presents a new single-phase PFC rectifier that consists of a diode-bridge and a following new dual-switch dc-dc converter. Since the single-switch boost and buck dc-dc converters are integrated and connected in parallel-like in the new dual-switch dc-dc converter, it achieves a wide and continuous output voltage control range in buck-region to boost-region with high efficiency. Further, a fine control scheme is developed and applied to the new converter to obtain a precise PFC operation. In this paper, validity of the theory is confirmed through simulation study.

Key words : PFC rectifier, output voltage control, predictive control, pulse-integral-value modulation, dc-dc converter.

I. INTRODUCTION

Harmonic pollution caused by rectifiers has been our great concern. To mitigate this pollution, several PFC rectifiers based on high frequency switching technique have been proposed so far. In the case of unidirectional power flow, the combination of a diode bridge and a following single switch dc-dc converter of the boost-type or the buck-type with an instantaneous input current control results in an economical and efficient PFC rectifier. Though, the output voltage control range in these conventional single-switch PFC rectifiers is limited in boost-mode range (i.e., higher than the maximum ac input voltage) or buck-mode range (i.e., lower than a half of the maximum ac input voltage). Thus, these two topologies do not satisfy the demand for wide and seamless output voltage control. Further, the buck dc-dc converter requires an expensive, heavy and bulky dc-inductor. On the other hand, a wide control range of the output voltage is obtained by applying the single-switch buck-boost dc-dc converter instead. Though, much larger loss is dissipated in this topology since the dc inductor current in this converter is much larger than the others.

As a compact and efficient solution for the above problem, a dual-switch dc-dc converter was proposed in the past[1]. Since the single-switch boost-mode and buck-mode dc-dc converters are integrated and connected in series with a common small dc-inductor, this dual-switch scheme can obtain both the boost-mode and the buck-mode dc-dc converter operations. Thus, selecting appropriate operation mode by comparing the input and output voltages, this ***series-type*** obtains a wide control range of the output voltage with the least dc inductor, i.e., with a least initial cost and losses. On the other hand, this dual-switch series-type dc-dc converter has one great disadvantage; that is, the main current (i.e., the dc-inductor current) flows through the two converter parts in series since the boost-mode part and the buck-mode part are connected in series. Thus, the conduction losses and the current stresses of the power devices in this dual-switch series-type converter are larger than the conventional single-switch boost and buck dc-dc converters. This disadvantage is serious under condition with a higher output current.

As an alternative solution, the authors propose a new dual-switch dc-dc converter (***TOKUSADA*** converter). A single-switch boost and buck dc-dc converter parts are integrated with a common dc-inductor in the proposed *TOKUSADA* converter too. Thus, it achieves a wide control range of the output voltage with a least dc-inductor, as same as the series-type. Additionally, since the boost and buck dc-dc converter parts are connected in parallel-like, the main current (i.e., the dc-inductor current) flows through only one converter part in the *TOKUSADA*-type. Thus, conduction losses caused by the power devices and current stresses of the power devices can be greatly reduced than the series-type and nearly the same to the conventional single-switch dc-dc converters, especially under condition with a higher output current. Further, a new and fine instantaneous current control has been developed and applied so that sinusoidal ac input current is obtained under severe condition such as,

-distortion of utility voltage,

-ripples of dc inductor current,
-ripples of dc output voltage,
-fluctuation of rms-value of the utility voltage,
-fluctuation of the output voltage average-value.

The unique circuit topology and the fine current control technique are described in this paper. Then, simulation results are shown to confirm the validity of the theory.

II. CIRCUIT TOPOLOGY AND OPERATION

A. Circuit Topology

Fig.1(a) and (b) show the single-phase PFC rectifier consisting of the new dual-switch parallel-type *TOKUSADA* dc-dc converter and the previously proposed dual-switch series-type dc-dc converter[1]. Both rectifiers consist of a diode-bridge, a low-pass filter (L_F and C_F) to trap high-frequency current components caused by PWM switching, a buck-mode operation part, a boost-mode operation part, a common small dc-inductor L_d, a large dc-capacitor C_O and a load R_O. From Fig.1(a) and (b), it is easily understood that the two dual-switch dc-dc converters require the same number of switches and diodes, i.e., two switches and two diodes.

B. DC-DC Converter Operation

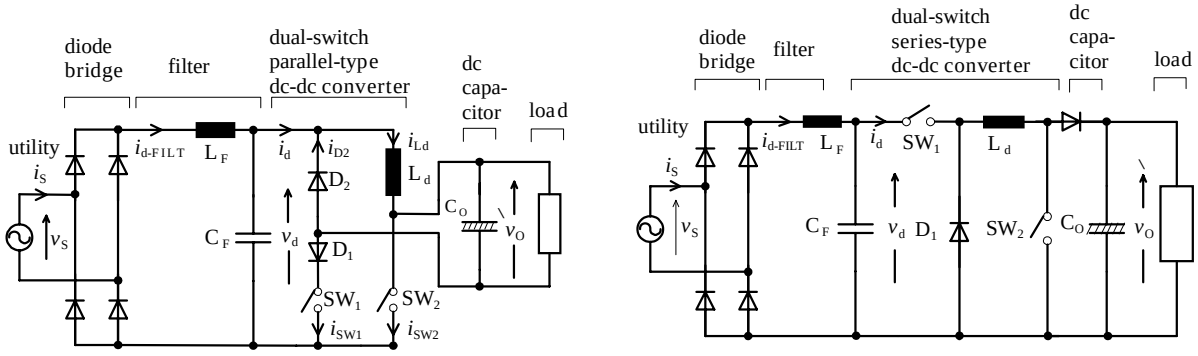
As shown in Table-I, both the two dual-switch dc-dc converters can obtain three circuit statuses (i.e., Status-A, B and C) by controlling the switches. Two of them, i.e., “Status-A and -C,” “Status-B and –C” or “Status-A and –B” are chosen alternately to achieve the boost-mode, buck-mode or buck-boost-mode dc-dc converter operation, respectively. From this table, it is known that the numbers of conduction switch(es) and diode(s) are less in the proposed *TOKUSADA* converter than the series-type in the all three circuit statuses. Thus, conduction losses caused by the power devices and current stress of the power devices are less in the proposed *TOKUSADA* converter than the series-type, especially under higher dc-current condition. Additionally, the number of conduction switch(es) and diode(s) of the *TOKUSADA* converter are only one in Status-A and –B. Thus, the conduction loss and the current stress of the converter are nearly the same to those of the conventional single-switch boost and buck converters.

C. PFC Operation

Fig. 2 shows the block diagram of the controller to achieve PFC operation and the seamless and wide-range output voltage control by means of the buck and boost hybrid operation. This PFC controller can be applied to both the *TOKUSADA*-type and the series-type dual-switch dc-dc converters. This controller consists of a current reference generator, two input current controllers (for buck-mode operation and boost-mode operation, respectively), an operation mode selector and a Gate-Logic circuitry. The function of the Gate-Logic circuitry is changed depending on the selected topology, i.e., the *TOKUSADA*-type or the series-type. In the following discussion of controller operation, the *TOKUSADA*-type is referred.

In the current reference generator, the template of the desirable ac input current i_S* is obtained by sensing the utility voltage v_S and adjusting the amplitude so that its rms-value becomes a unity. This signal is shown as v_S’ in Fig.2. By taking absolute-value of v_S’, the template of the reference i_d* of the dc input current is obtained as $|v_S'|$ as shown in Fig.2. In this discussion, however, the utility voltage v_S is assumed as purely sinusoidal.

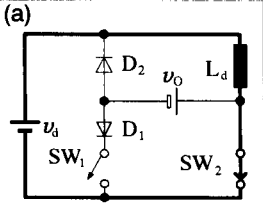
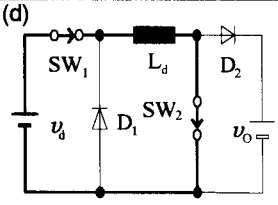
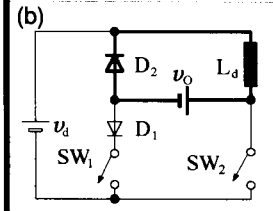
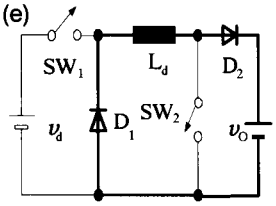
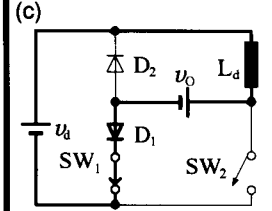
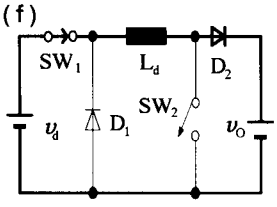
The amplitude or the rms-value of the input current i_d must be adjusted so that the output voltage V_O is controlled as desirable. To achieve this, rms-value of the reference i_d* is determined by referring to the output signal of an output voltage controller (not shown in Fig. 2). In Fig.2, this process is expressed as multiplying $|v_S'|$ by I_S*, where I_S* represents the rms-value of the desirable dc current i_d*. The



(a) New TOKUSADA-Type PFC Rectifier. **(b) Conventional Series-Type PFC Rectifier.**

Fig.1. 1-Phase PFC Rectifiers Using *TOKUSADA*-Type and Conventional Series-Type DC-DC Converter.

Table-I
Clucuit Statuses and Power Device(s) Connected to Ld and Conduction i_{Ld}.

New TOKUSADA-type	Conventional Series-type
Circuit Status-A (L_d is connected to input-side) (for boost-mode and buck-boost mode operations)	
(a)  (d) 	
Number of device(s) connected to L_d and conducting i_{Ld}	
One Switch and No Diode	Two Switches (in series) and no Diode
Circuit Status-B (L_d is connected to output-side) (for buck-mode and buck-boost mode operations)	
(b)  (e) 	
Number of device(s) connected to L_d and conducting i_{Ld}	
No Switch and one Diode	No Switch and two Diodes (in series)
Circuit Status-C (L_d is connected to input & output-side) (for boost and buck-mode operations)	
(c)  (f) 	
Number of device(s) connected to L_d and conducting i_{Ld}	
One Switch and one Diode (in series)	One Switch and one Diode (in series)

desirable rms-value I_S^* is obtained through an output voltage controller such as PI controller (not shown in Fig.2). This reference signal i_d^* is utilized in both the current controllers for the boost-mode and buck-mode operations.

However, a buck-boost operation can also be obtained using the *TOKUSADA* converter as described, but this operation produces larger losses even in the *TOKUSADA* converter. Thus, combination of buck and boost operations is the best to achieve the wide range and seamless control of the output voltage and PFC with high efficiency. The desirable rectifier operation can also be obtained by the combination of buck-mode and buck-boost-mode operations[2]. This scheme results in a simpler current controller but larger conduction losses and current stresses than the scheme proposed in this paper. The following discussion concentrates on the scheme with buck-mode and boost-mode hybrid operation.

i) Buck-Mode Operation

Fig.3 shows operating waveforms in a switching period T_{SWG} (=100[μs] in simulation shown later) of the current controller shown in Fig.2. Since the switching period T_{SWG} is very short, variation in the period of the dc inductor current i_{Ld} is omitted in the figure.

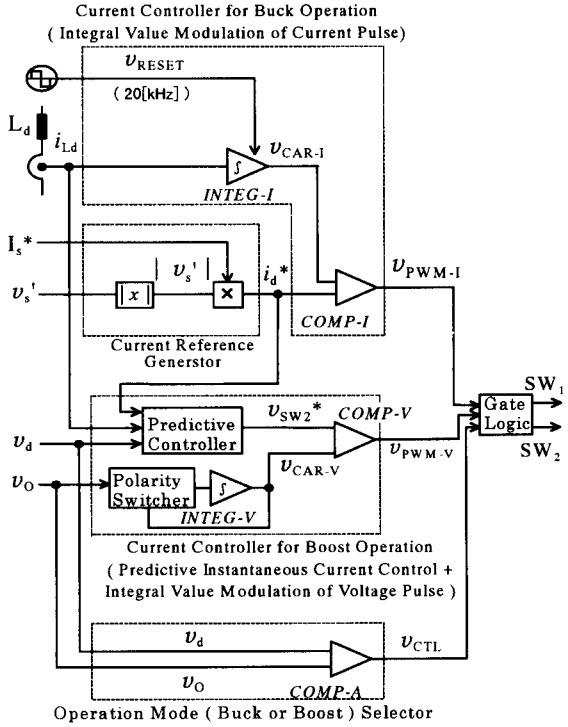


Fig. 2. Current Controller for Dual-Switch Single-Phase PFC Rectifier with Buck-Mode and Boost-Mode Hybrid Operation.

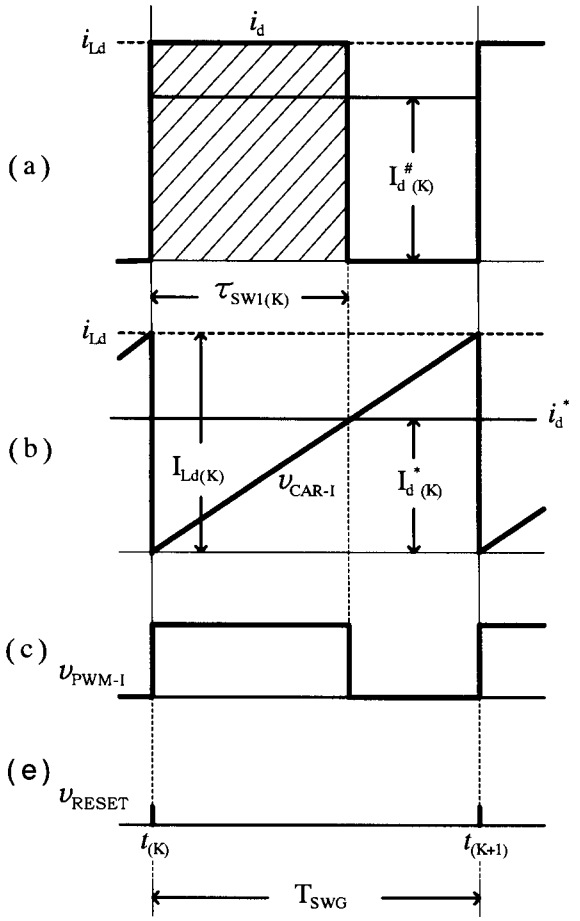


Fig. 3. Operating Waveforms of Pulse-Integral-Value Modulation for Buck-Mode Operation.

As described in part II-*B*, the Status-B and -C are alternately chosen in the buck-mode operation. The inductor current i_{Ld} is fed to the input in only the Status-C where the switch SW_1 remains in conduction-state and the switch SW_2 is in off-state. Thus, the amplitude $I_{Ld(K)}$ of the dc-inductor current i_{Ld} and the conduction period $\tau_{SW1(K)}$ of SW_1 in each switching period determine the local-average-value $I_d^{\#}{}_{(K)}$ ($=I_{Ld(K)}\tau_{SW1(K)}/T_{SWG}$) of the dc input current i_d in the switching period (refer to Fig.3). This local average value $I_d^{\#}{}_{(K)}$ can vary one by one of switching period, and the variation determines the waveform produced by low-frequency components of i_d. Thus, instantaneous values of the filtered dc input current $i_{d\text{-FILT}}$ and i_S are determined by variation of $I_d^{\#}{}_{(K)}$. Therefore, the local-average-value $I_d^{\#}{}_{(K)}$ must follow variation of the reference i_d^*.

If the dc inductor current i_{Ld} is constant, i.e., ripple-free, the variation of the local-average-value $I_d^{\#}{}_{(K)}$ or $i_{d\text{-FILT}}$ is proportional to the conduction period $\tau_{SW1(K)}$ of SW_1. In this case, the desirable waveform of the filtered dc input current $i_{d\text{-FILT}}$ or the ac input current i_S can be obtained directly by controlling only the conduction period $\tau_{SW1(K)}$ and without referring to i_{Ld}. The current control or current waveshaping is very easy in this case, but this control is effective under only a condition with a large dc inductor or ripple free dc inductor current.

A small dc inductor is employed in the proposed system to reduce the size, weight, losses and initial cost. Thus, the dc inductor current i_{Ld} produces large ripples and its amplitude $I_{Ld(K)}$ in each switching period varies. How to determine an appropriate conduction period $\tau_{SW1(K)}$ of the switch SW_1 in the buck-mode operation under a largely rippled dc-inductor current is the focus of the proposed current control. To solve this, the carrier signal v_{CAR-I} for the buck-mode operation is generated by integrating the dc-inductor current i_{Ld} in each switching period (refer to Fig.2).

The output of the integrator *INTEG-I* is reset at the end of every switching period (i.e., $t = t_{(K)}$, $t_{(K+1)}$ etc. in Fig.3) by means of a very narrow resetting pulse v_{RESET} with frequency of f_{SWG} ($=1/T_{SWG}$). Thus, the output v_{CAR-I} draws a saw-tooth waveform whose frequency is the same as v_{RESET}. The final value in each switching period of the integrator output (for example, $V_{CAR-I(K)}$ for $t = t_{(K)}$) is forced to be proportional to the amplitude $I_{Ld(K)}$ of the dc inductor current in that switching period. Thus, the variation of the final value $V_{CAR-I(K)}$ follows the variation of $I_{Ld(K)}$. Although it is assumed that "$V_{CAR-I(K)}=I_{Ld(K)}$" in Fig.3, only the proportional relation between $V_{CAR-I(K)}$ and $I_{Ld(K)}$ is important and necessary in this new modulation scheme. This carrier signal v_{CAR-I} and the current reference i_d^* are compared using a comparator *Comp-I* as shown in Fig.2. Then, the output v_{PWM-I} is set in High-Level or Low-Level while $v_{CAR-I} < i_d^*$ or $v_{CAR-I} > i_d^*$, respectively, as shown in Fig.3(c). This comparator output v_{PWM-I} is employed as the PWM signal in the buck-mode operation, and the switch SW_1 is set on conduction-state or off-state while the PWM signal remains in High-Level or Low-Level, respectively. However, local-average-value of the hatched area in Fig.3(a) or the value obtained by dividing the hatched area (or its integral value) by the switching period T_{SWG} equals $I_d^*{}_{(K)}$.

The switch SW_1 is controlled by the PWM signal v_{PWM-I}, and it turns-on at the initial instant (i.e., $t = t_{(K)}$) and turns-off at the instant when v_{CAR-I} reaches $I_d^*{}_{(K)}$, respectively. Thus, the current i_d flowing through the switch SW_2 and fed to the input side of the dc-dc converter draws a pulse with the same amplitude to the dc inductor current i_d, as shown in Fig.3(a). Thus, the average value in the switching period (or local average value) of this current pulse equals the reference $I_d^*{}_{(K)}$. Therefore, the low-frequency component of i_d or the filtered current $i_{d\text{-FILT}}$ draws the same waveform as the reference i_d^*.

As a result, the ac input current (i.e., the utility current i_S) draws a sinusoidal waveform with no displacement angle against the utility voltage v_S.

ii) Boost-Mode Operation

An appropriate reference for the voltage applied on the switch SW_2 must be obtained to control the input current as desirable (i.e., $i_d = i_d^*$). In the proposed scheme, this desirable voltage v_{SW2}^* is generated in the "Predictive (Instantaneous Current) Controller" by referring to the utility voltage v_S, the input current i_d, its reference i_d^*, inductance L_d and switching period T_{SWG}. In this process, the Predictive-Instantaneous-Current-Control theory [3] is applied so that the input current i_d obtains a fine response to the reference i_d^*. The voltage reference v_{SW2}^* is compared with a triangular carrier signal $v_{CAR\text{-}V}$ to produce an appropriate PWM switching signal $v_{PWM\text{-}V}$.

However, the carrier signal $v_{CAR\text{-}V}$ for the boost-mode operation is also generated by integrating the output voltage v_O (refer to Fig.2). Thus, local-average-value or low-frequency component of the switch voltage v_{SW2} exactly traces variation of the reference v_{SW2}^* even if the output voltage v_O produces large ripples and fluctuations. The PWM pulse of v_{SW2} must be located in the center in each switching period otherwise local-average-value $I_d^{\#}(K)$ of the input current i_d does not match the reference i_d^*. To achieve this, output voltage v_O is fed to an integrator *INTEG-V* through the *Polarity Switcher* so that the integrator output (i.e., the carrier) $v_{CAR\text{-}V}$ draws a triangular waveform. By comparing this triangular carrier $v_{CAR\text{-}V}$ and the reference v_{SW2}^*, a PWM signal $v_{PWM\text{-}V}$ located in the center in each switching period is obtained. As same as the relation between the carrier $v_{CAR\text{-}I}$ for the buck-mode operation and the dc-inductor current i_{Ld}, amplitude of this carrier $v_{CAR\text{-}V}$ exactly traces variation of the output voltage v_O in each switching period.

Although detail of how to obtain the reference v_{SW2}^* by means of the Predictive Control theory is omitted in this paper, it has been described in the previously published paper[3].

III. SIMULATION STUDY

To confirm the validity of the theory, operation of the proposed *TOKUSADA* rectifier has been simulated using *PSIM*. Under the circuit condition shown in Table-II, simulation waveforms shown in Fig.4 are obtained. This table-II also shows dominant measured data. The output voltage V_O for the case of Fig.4 (i.e., 197.5 [V_{AVE}]) is above the buck region (i.e., lower than 141 [V]) and below the boost region (i.e., higher than 282 [V]). Thus, the output voltage is obtained by only buck-mode and boost-mode hybrid operation and not by the boost-mode alone or the buck-mode alone.

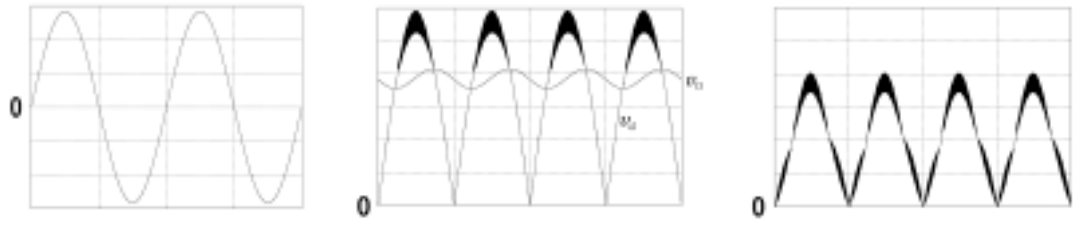
Table-II
Circuit Constants and Measured Data for Simulation Results in Fig.4.

Circuit Constants		
Energy Storage Components		
DC Inductor (+ series resistance)	L_d (r_{Ld})	0.5 [mH] (0.1 [Ω])
DC Capacitor	C_O	2,000 [μF]
Filter (to trap high-frequency component)		
Inductor (series resistance)	L_F (r_{LF})	0.3 [mH] (0.1 [Ω])
Capacitor	C_F	2,000 [μF]
Measured Data		
Utility Side		
Voltage (rms-value)	V_S	200.0 [V_{RMS}]
Current (rms-value)	I_S	19.75 [A_{RMS}]
Frequency	f_S	50 [Hz]
DC Output Side		
Voltage (average-value)	V_O	197.5 [V_{AVE}]
Current (average-value)	I_O	19.75 [A_{AVE}]
Power (average-value)	P_O	3.9 [kW]

Fig.4(a) and (b) show waveforms of the voltage v_S and the current i_S on the utility side, respectively. On the other hand, Fig.4(c) shows the output voltage v_O and dc-input voltage v_d. Additionally, Fig.4(d) shows the carrier signal $v_{CAR\text{-}V}$ (for the boost-mode operation) while Fig.4(e) and (f) show the dc-inductor current i_{Ld} and the carrier signal $v_{CAR\text{-}I}$ (for the buck-mode operation), respectively.

From Fig.4(a) and (b), it is known that the utility current i_S draws a sinusoidal waveform in phase with the voltage v_S. Thus, a PFC operation is achieved as mentioned in the theory. Fig.4(c) shows that the output voltage v_O and the dc-input voltage v_d are crossing each other twice a half cycle, i.e., 10 [ms]. This means that the boost-mode operation and the buck-mode operation (required when $v_O > v_d$ and $v_O < v_d$, respectively) must be chosen alternately in each half cycle to obtain PFC operation. Since the PFC operation is precisely achieved as mentioned, this requirement is satisfied in the proposed rectifier. Fig.4(c) and (e) show that both the output voltage v_O and the dc-inductor current i_{Ld} produce large ripples. Though, both the amplitudes of the carrier signal $v_{CAR\text{-}V}$ and $v_{CAR\text{-}I}$ shown in Fig.4(d) and (f) follow the rippled voltage and current, respectively. Thus, these carrier signals are generated as described in the theory.

The simulation results discussed here show that the proposed scheme offers both a PFC rectifier operation and a wide output voltage control range as described in the theory. Further, fine waveforms are obtained in other simulation results with output voltage of 100 [V_{AVE}] (in buck-mode range) and 300



(a) Utility voltage v_S (100 [V/div]) (c) DC input voltage v_d and output voltage v_O (50 [V/div]) (e) DC-inductor current i_{Ld}

(b) Utility current i_S (10 [A/div]) (d) Carrier Signal v_{CARV} for Boost-Mode Operation (f) Carrier Signal $v_{CAR\text{-}I}$ for Buck-Mode Operation

Fig.4. Operating Waveforms of New PFC Rectifier (obtained from simulation).
(time scale : 10 [ms/div])

[V_{AVE}] (in boost-mode range). Thus, the validity of the proposed theory is completely confirmed through these simulation results.

VI. CONCLUSION

A new single-phase PFC rectifier with a diode-bridge and a following dual-switch dc-dc converter (*TOKUSADA* converter) to obtain a wide control range of the output voltage and high efficiency under PFC operation is presented. The boost-mode operation part and the buck-mode operation part with a common dc-inductor are integrated and connected in parallel-like in the proposed *TOKUSADSA* dc-dc converter. Thus, the conduction losses produced by the switches and diodes and their current stresses can be greatly reduced comparing with the previously proposed dual-switch series-type scheme.

The circuit topology and the operating principle are described in detail. Also simulation results obtained by *PSIM* are shown and the validity of the operating theory is confirmed.

Loss comparison between the proposed and the series-type rectifiers remains. A part of the results has been obtained using simulation while experimental study on this item has been under preparation.

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