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Modeling and Optimization of Bidirectional Dual Active Bridge DC–DC Converter Topologies

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Kurzfassung

Die vorliegende Arbeit beschreibt die Realisierung eines bidirektionalen Gleichspannungswandlers, welcher über einen Hochspannungsanschluss mit einer Anschlussspannung im Bereich zwischen 240 V und 450 V und über einen galvanisch getrennten Niederspannungsanschluss mit einer Anschlussspannung im Bereich zwischen 11 V und 16 V verfügt. Die Nennleistung des Konverters beträgt 2 kW, unabhängig von der vorliegenden Energieflussrichtung.

Für die in **Kapitel 2** dargestellte Topologieübersicht zeichnet sich unter Verwendung der gegebenen Konverterspezifikationen eine Einschränkung der geeigneten Schaltungskonzepte ab. Die resultierende Auswahl beinhaltet neben einstufigen Konvertertopologien auch zweistufige Realisierungsvarianten (d.h. die Serienschaltung eines galvanisch getrennten Gleichspannungswandlers und eines Gleichspannungswandlers ohne Potentialtrennung). Unter den einstufigen Topologien zeichnet sich der Dual Active Bridge (DAB) Konverter als die am besten geeignete Wahl hinsichtlich der gewünschten Effizienz und hinsichtlich der erzielbaren Leistungsdichte ab. Ausserdem lassen sich, aufgrund der weiten Ein- und Ausgangsspannungsbereiche, weitere Wirkungsgradverbesserungen für zweistufige Schaltungsvarianten erwarten.

Im Anschluss an Kapitel 2 erfolgt eine detaillierte Beschreibung der DAB.

- **Kapitel 3** beschreibt die Funktionsweise der DAB; in diesem Zusammenhang werden drei verschiedene Convertermodelle erläutert. Dies beinhaltet ein verlustfreies Convertermodell, welches z.B. der vereinfachten Berechnung der Transformatorstromeffektivwerte dient; die resultierenden Zusammenhänge werden zur Synthese eines hinsichtlich Transformatorstromeffektivwerte optimalen Modulationsverfahrens verwendet. Die in diesem Kapitel ebenfalls erläuterten erweiterten Convertermodelle berücksichtigen die Auswirkungen der Leitverluste und des Magnetisierungsstromes auf die primär- und sekundärseitigen Transformatorströme.
- In **Kapitel 4** wird ein detailliertes Verlustmodell der DAB beschrieben,

welches der Berechnung der für eine zuverlässige Ermittlung des Wirkungsgrades relevanten Verlustanteile dient. Das Verlustmodell wird einerseits dazu verwendet, die in Kapitel 3 erstellten Konvertermodelle zu parametrisieren. Andererseits ermöglicht dieses Verlustmodell die in Kapitel 5 beschriebene Optimierung des Steuerverfahrens hinsichtlich maximalen Wirkungsgrades.

- **Kapitel 5** erläutert eine systematische Untersuchung der in Kapitel 3 vorgestellten Modulationsverfahren unter Verwendung des in Kapitel 4 beschriebenen Verlustmodells. Die aus dieser Untersuchung resultierenden Ergebnisse dienen der Synthese eines neuartigen Steuerverfahrens, welches den Betrieb der DAB nahe des maximal möglichen Wirkungsgrades erzielt.
- **Kapitel 6** beschreibt das transiente Verhalten des DAB Konverters. Dies beinhaltet neben einem arbeitspunktabhängigen Kleinsignalmodell der DAB auch die Übertragungsfunktionen des digitalen Steuerteils.
- In **Kapitel 7** werden möglichen Wirkungsgradverbesserungen untersucht, die sich durch die Verwendung einer zweistufigen Konvertervariante erzielen lassen würden. Es stellt sich jedoch heraus, dass der für den zweistufigen Konverter resultierende mittlere Wirkungsgrad ($\bar{\eta} = 93.0\%$) kleiner ist, als der der einstufigen DAB ($\bar{\eta} = 93.5\%$; die Berechnung von $\bar{\eta}$ erfolgt gemäss Anhang A.1).
- **Kapitel 8** schliesst die Arbeit mit einer Zusammenfassung der erarbeiteten Ergebnisse, abschliessenden Bemerkungen zu bidirektionalen und unidirektionalen DC–DC Wandlern und einem Ausblick bezüglich weiterer Forschungsmöglichkeiten auf dem Gebiet des DAB Konverters ab.

Messergebnisse bestätigen die in dieser Arbeit berechneten Ergebnisse.

Zur Ermittlung der experimentellen Ergebnisse wurde ein voll funktionsfähiger Prototyp des oben spezifizierten DAB Konverters entworfen (**Anhang A.2**) und realisiert. Der unter Verwendung des in Kapitel 5 erläuterten effizienzoptimierten Modulationsverfahrens gemessene Wirkungsgrad beträgt 94.5% (Eingangsspannung: 340 V, Ausgangsspannung: 12 V, Ausgangsleistung: 2 kW, Energietransfer in Richtung der Niederspannungsseite, Messung bei Raumtemperatur: 25°C).

Abstract

This thesis investigates different bidirectional and isolated DC–DC converters with a high voltage port (ranging from 240 V to 450 V), a low voltage port (11 V to 16 V), and a rated power of 2 kW.

The work starts with an overview on different bidirectional DC–DC converter topologies and investigates their applicability with respect to the given specifications (**Chapter 2**). Based on the findings of Chapter 2, the single-phase Dual Active Bridge (DAB) converter topology is considered most promising regarding the achievable converter efficiency and the achievable power density. Moreover, due to the wide input and output voltage ranges, two-stage DC–DC converters, i.e. the series connection of an isolated DC–DC converter and a DC–DC converter without galvanic isolation, are expected to facilitate an improved converter efficiency.

The subsequent Chapters discuss the single-phase DAB converter in detail.

- **Chapter 3** explains the working principle of the DAB converter based on 3 different simplified converter models. This includes a lossless model of the DAB, which facilitates basic analytical investigations and allows for a simplified synthesis of optimal modulation schemes (calculated with respect to minimum transformer RMS current). Moreover, two different refinements of the electric DAB converter model are included in order to consider the impacts of the conduction losses and the magnetizing current on the transformer currents.
- **Chapter 4** discusses a detailed loss model of the DAB, needed in order to parameterize the models developed in Chapter 3 and to develop the efficiency optimized modulation presented in Chapter 5. This loss model is used to calculate the losses in the most relevant converter components.
- **Chapter 5** presents a systematic investigation of efficiency improvements achievable for the given DAB converter, obtained with the use of optimized modulation schemes. Finally, with the suboptimal modulation schemes discussed in Section 5.2.2, converter operation close to its maximum possible efficiency is achieved (Figure 5.28).

- **Chapter 6** details a dynamic model of the complete converter system (including the digital control platform).
- **Chapter 7** investigates the most promising two-stage converter configurations in order to examine possible efficiency improvements. As a result, however, the average efficiency achieved with the two-stage converter ($\bar{\eta} = 93.0\%$) is less than the average efficiency achieved with the single-stage DAB ($\bar{\eta} = 93.5\%$; calculated according to Appendix A.1).
- **Chapter 8** concludes this work and presents an outlook regarding future research in the field of the DAB converter.

The calculated results are verified using experimental data.

A hardware prototype of the above specified DAB converter is realized according to **Appendix A.2**. With this converter prototype and with the optimized modulation schemes detailed in Chapter 5, a converter efficiency of 94.5% is measured (input voltage: 340 V, output voltage: 12 V, output power: 2 kW, power being transferred to the low voltage port, room temperature: 25°C).

Chapter 1

Introduction

1.1 Applications of Bidirectional DC–DC Converters

1.1.1 Automotive Applications

Today, conventional cars use combustion engines which burn fossil fuels (e.g. gasoline, diesel) to generate the required propulsion power. The products of the combustion process – mainly the nontoxic compounds H_2O and CO_2 – are exhaled into the air. CO_2 , however, is known as a greenhouse gas and partly accounts for global warming.¹ Besides that, excessive burning of fossil fuels causes environmental pollution and the resources to exhaust [2].

Different initiatives have been taken in order to attain a reduction of CO_2 emissions; prominent examples are the Kyoto Protocol [3] and the California Zero Emission Vehicle (ZEV) program [4].

Regarding automobiles, the most promising vehicle technologies with respect to an effective reduction in fuel consumption are hybrid electric vehicles, electric vehicles, and fuel cell vehicles [2]. Hybrid electric vehicles utilize an internal combustion engine (ICE) in combination with one or more electric machines in order to improve the overall efficiency. With a hybrid power train and a further optimized ICE, the ambitious target of the European Commission of a CO_2 output value of $90 \text{ g CO}_2/\text{km}$ (equivalent to a fuel consumption of $3.5 \text{ l}/100 \text{ km}$ or an efficiency of 67.2 MPG – US) after the year 2012 may become feasible [5]. The target of zero local CO_2 emissions can be achieved with battery powered electric vehicles and with fuel cell powered vehicles operated with hydrogen as fuel [6]; in that case, the fuel cell only emits water [7].

¹Water vapor acts as a greenhouse gas, too; however, the actual amount in the atmosphere is approximately 3%, much higher than that of CO_2 ($\approx 385 \text{ ppm}$) [1].

Hybrid Electric Vehicles (HEV)

A hybrid electric vehicle utilizes two or more energy sources for propulsion to increase the overall system efficiency. The power train of a HEV typically consists of an ICE and one or more electrically powered machines [8]. Additionally, the hybrid electric drive train allows for improved vehicle acceleration, which is an important argument regarding customer satisfaction [9, 10, 11].

According to the degree of hybridization (i.e. the complexity of the system architecture and the provided amount of electric power), the different HEV architectures can be classified into 3 categories (Table 1.1, [12, 13]):

- Micro hybrid: belt-driven starter-generator system, recuperative braking can be implemented up to a certain degree. The electric system is designed to provide a comparably low amount of the maximum traction power, which is economically achievable with a relatively low system voltage. Still, a considerable effort is required to upgrade an existing

<i>Category</i>	<i>Battery Power (Nom. Capacity if available)</i>	<i>Battery Voltage</i>	<i>Realization (if available)</i>	<i>Lit.</i>
Micro Hybrid	4 kW ... 5 kW	30 V ... 40 V	–	[11]
	10 kW	36 V	Saturn VUE Hybrid	[14]
Mild Hybrid	10 kW ... 20 kW	144 V	–	[11]
	up to 20 kW	–	–	[12]
	–	28 V ... 42 V	–	[15]
	10 kW (0.9 kWh)	144 V	Honda Insight (year 2000)	[16]
Full Hybrid	30 kW ... 50 kW	288 V	–	[11]
	21 kW (6.5 Ah)	202 V	Toyota Prius (year 2005)	[13]
	45 kW	288 V	Toyota Highlander Hybrid SUV	[13]

Table 1.1: Electric power and typical voltages or voltage ranges of HV batteries employed for HEVs; if available, the nominal energy storage capacity is given in paranthesis (either in kWh or in Ah).

conventional car to a micro hybrid vehicle, since a second battery and a second voltage bus are typically required (in addition to the existing 12 V battery and the 14 V bus) [11].

- Mild hybrid: starter-generator system, recuperative braking, and electric propulsion for a short time; the electric motor is directly flanged to the crankshaft [12]. The power provided from the electric system is typically between 10 kW and 20 kW. Again, a supply voltage higher than the installed 14 V is required in order to obtain technically reasonable battery and motor currents [17].
- Full hybrid or strong hybrid: starter-generator system, recuperative braking, and electric driving. There, the required electric power (up to 100 kW) demands for comparably high bus voltages of up to 800 V [15].

In another common approach, hybrid electric vehicles are classified into four different categories, with respect to the employed drive train [13, 15]:

- *Parallel HEV topology (Figure 1.1)*: both, the ICE and the electric machine are mechanically connected to the transmission. Thus, the system allows for the ICE and the electric motor to share the demanded torque while the revolution speed of the engine depends on the selected gear and the cruising speed what may implicate inefficient ICE operation [8, 18]. A clutch is installed between the ICE and the electric machine, which enables pure electric driving with the ICE being turned off [15].
- *Series HEV topology*: the ICE is connected to an electric generator which provides electric energy to a second electric machine for propulsion. Such a system allows for an optimized operation of the ICE at its best operating point, since the ICE revolution speed is independent of the cruising speed. However, compared to the parallel HEV drive topology, multiple stages of energy conversion are employed (mechanical \rightarrow electrical, AC, with frequency $f_1 \rightarrow$ electrical, AC, with frequency $f_2 \rightarrow$ mechanical) what causes the system efficiency to decrease. Furthermore, a much higher rated power of the electric system (generator, motor, power electronics) is required [18].
- *Series-parallel HEV topology*: allows for the operation with both, the parallel hybrid drive train and the series hybrid drive train and thus combines the advantages of both systems. Disadvantageous is the high system complexity [8, 13].
- *Complex HEV*: subsumes all HEV drive train topologies, which cannot be classified into the 3 categories discussed above [13].

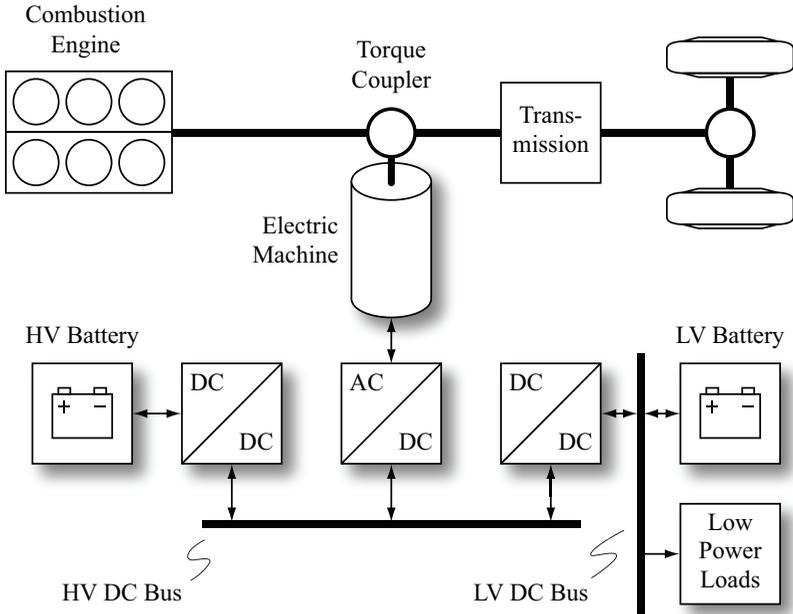


Figure 1.1: Example of a parallel HEV drive train architecture [8].

The electric power demand in a HEV is typically much higher than that of a conventional car (Table 1.1). Hence, a supply voltage considerably higher than the voltage provided from the existing 14 V bus (9 V...16 V at the battery terminals [6]) is required, whereas a high voltage (HV) DC bus² is typically employed in order to distribute the electric power (Figure 1.2). The HV DC bus (e.g. with a typical voltage between $200 \text{ V} \leq V_1 \leq 300 \text{ V}$ [10,13]³) primarily enables power transfer between the HV battery and the electric propulsion system. Moreover, high power ancillary loads (e.g. air conditioner, power assisted steering) are favorably supplied from the HV DC bus, since the ICE may be turned off during vehicle operation.

Even though, the proposed system architecture theoretically renders the

²Due to safety reasons, a voltage level of more than 60 V is often denoted a “high voltage” (HV) in automotive applications and for a voltage level below 60 V the term “low voltage” (LV) is used [9].

³Recently, many car manufacturers selected considerably higher voltages for the HV DC bus (e.g. 650 V for the Lexus GS 450h [13]) in order to reduce motor and inverter currents.

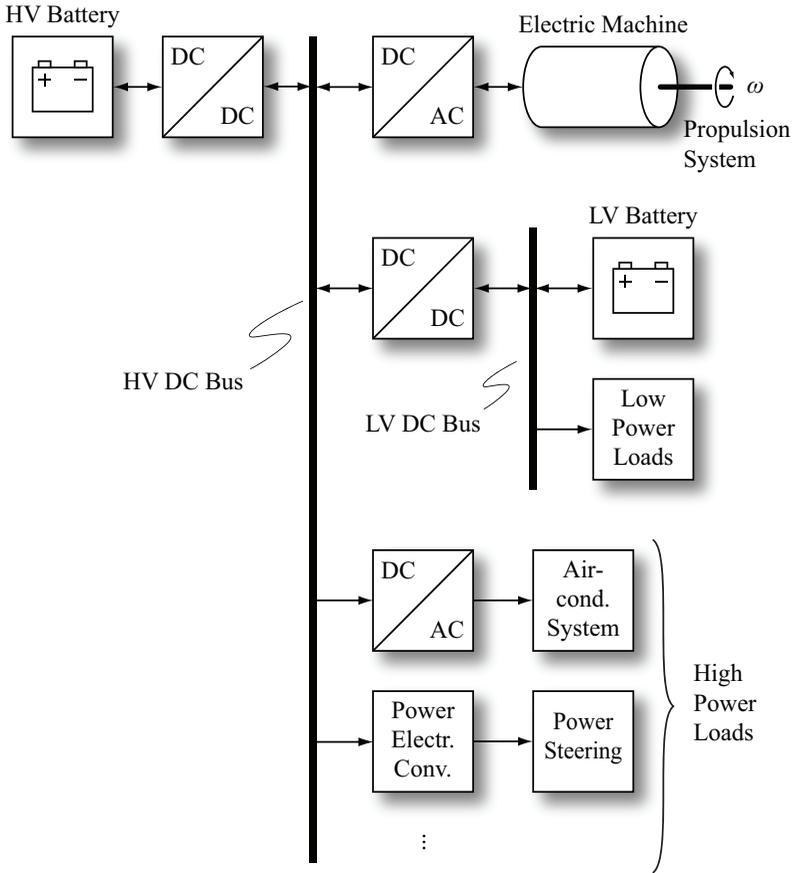


Figure 1.2: Typical HEV power system architecture [8].

conventional 14 V bus unnecessary, it is widely believed that the 14 V bus will coexist with the HV DC bus for a very long time, since all the conventional low power automotive loads (e.g. interior/exterior lighting, electric motor driven fans/pumps/compressors, instrumentation subsystems) are designed based on 14 V standards [6]. Thus, the 12 V battery will remain in order to provide a backup to the electric power supply of the 14 V bus.

Low Voltage DC–DC Converter. Instead of the conventional alternator – which cannot be used, since the ICE may be turned off during vehicle operation – a DC–DC converter is employed in order to provide electric power to the low power loads and the 12 V battery. For that application, a DC–DC converter designed for unidirectional power transfer would be sufficient. Still, practical reasons support the use of a bidirectional DC–DC converter [6, 13]:

- Jump-starting the car: with a conventional battery-jumper-cable, the 12 V battery is connected to another car’s 12 V battery in order to start the ICE [19]. For this mode of operation, a bidirectional DC–DC converter is required, since the starter is connected to the HV DC bus (e.g. the electric machine in Figure 1.2).
- Charging the HV battery: with a bidirectional DC–DC converter, the battery can be charged using an external power supply that is connected to the 12 V battery.
- Leaving a dangerous zone in case of a HV battery failure: the bidirectional DC–DC converter could be used to (slowly) drive the car out of a dangerous zone (e.g. road crossing) if the HV battery fails.

Current publications suggest a 14 V bus power demand of 1 kW . . . 2.5 kW [6, 15, 20, 21], which defines the nominal output power $P_{\text{out,nom}} = P_{2,\text{nom}}$ [cf. (3.14)] of the DC–DC converter when operated in buck mode (i.e. power is transferred from the HV bus to the 14 V bus). However, the nominal output power in boost mode (i.e. power transfer from the 14 V bus to the HV bus) is not specified in literature; due to the aforementioned boost mode applications, an output power of $-P_{\text{out,nom}} = -P_{1,\text{nom}} \approx 1 \text{ kW} \dots 1.6 \text{ kW}$ seems reasonable e.g. with respect to the power requirements of conventional starters (up to 1.6 kW [12]).

Table 1.2 summarizes typical specifications of the bidirectional DC–DC converter employed to transfer electric power between the HV DC bus and the LV DC bus in a HEV.

Electric Vehicles (EV)

The drive train of an EV is exclusively powered from an electric machine and a HV battery with high energy density typically provides the required electric energy [26, 27]. Thus, EVs allow for zero (local) emissions what makes them most interesting for the use in urban areas where traffic emissions considerably pollute the local environment.

The basic architecture of an EV drive train is similar to the drive train of a series HEV without ICE and electric generator (cf. Figure 1.1 and Figure 1.2): besides the existing 14 V bus, a HV DC bus is required in order to provide the

HV port voltage:	$200 \text{ V} < V_1 < 250 \text{ V}$ [10] $200 \text{ V} < V_1 < 300 \text{ V}$ [13] some publications mention even higher port voltages of up to 800 V [15]
LV port voltage range:	$V_2 \approx 9 \text{ V} \dots 16 \text{ V}$
Rated power, buck mode:	$P_{\text{out,nom}} \approx 1 \text{ kW} \dots 2.5 \text{ kW}$
Rated power, boost mode:	$-P_{\text{out,nom}} \approx 1 \text{ kW} \dots 1.6 \text{ kW}$
Galvanic isolation:	required due to safety reasons [15]
Other requirements:	low cost, high efficiency, high power density, low weight [22, 23, 24, 25]

Table 1.2: Specification of a bidirectional DC–DC converter for HEVs used to transfer electric power between the LV DC bus and the HV DC bus; the output power is defined with (3.14) (using $P_{\text{out,nom}} = P_{\text{out}}$).

electric power for vehicle propulsion and all the high power ancillary loads. Similar to the HEV, the EV employs a 14 V bus to power the conventional low power automotive loads.

Low Voltage DC–DC Converter. Since the electric system architectures of EVs and HEVs are rather similar, the DC–DC converter which provides power to the conventional 14 V components during normal operation is specified according to Table 1.2. Bidirectional power transfer is needed in order to allow for jump-starting the car, leaving a dangerous zone using the starter, and charging the HV battery via the terminals of the 12 V battery.

Fuel Cell Vehicles (FCV)

In a FCV, a fuel cell provides the required traction power [in literature, Proton Exchange Membrane Fuel Cells (PEMFC) or Solid Oxide Fuel Cells (SOFC) are typically considered for automobiles [8]]. FCVs allow for zero (local) CO₂ emissions and achieve a cruising range comparable to cars with ICE.

Figure 1.3 depicts a simple power train architecture of a FCV. Depending on the load, the fuel cell generates a voltage which ranges from 230 V to 450 V during normal vehicle operation [20]. It provides power for vehicle propulsion, all the auxiliary fuel cell components (compressors, pumps, etc.) as well as for the conventional 14 V bus (using a DC–DC converter). In this simple design, the HV battery is avoided; during the starting process of the vehicle, the 12 V

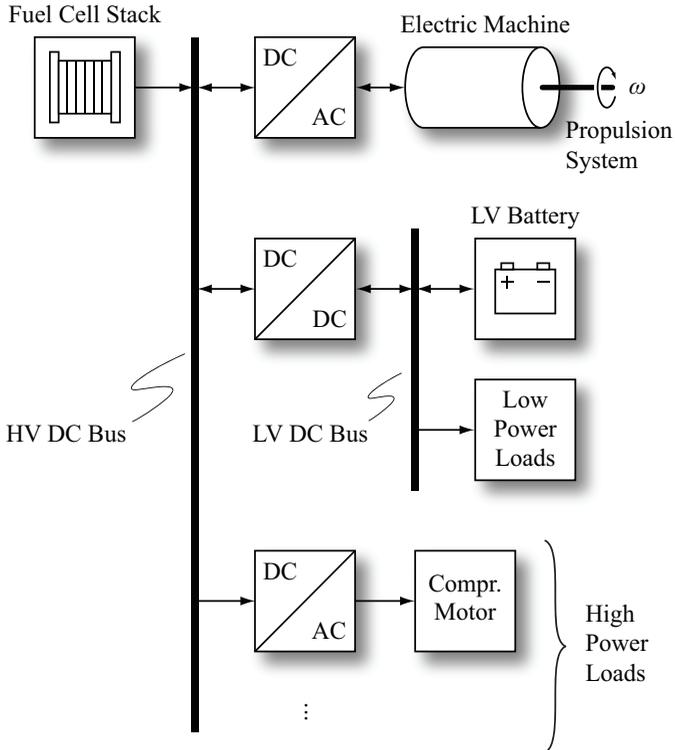


Figure 1.3: Simple power system architecture for a FCV [20]; the HV battery is avoided and thus the HV bus voltage varies within a wide voltage range (e.g. between 230 V and 450 V).

battery provides the required electric power to the fuel cell system.

Most documented systems, however, include a HV battery in order to stabilize the HV DC bus voltage during transient load conditions (Figure 1.4, [8, 28]). The fuel cell, the HV battery, and the 14 V bus are all connected to the HV DC bus using separate DC–DC converters. In such a system, the HV battery provides power when the car is started and thus the DC–DC converter between the HV DC bus and the 14 V bus must not be bidirectional any more.

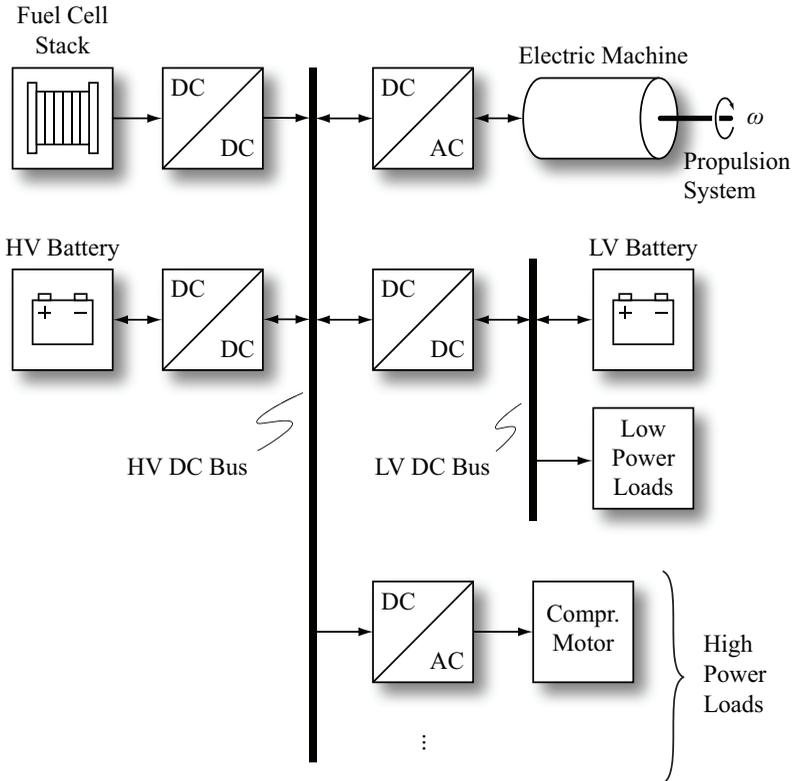


Figure 1.4: Extended power system architecture for a FCV [8, 28], including a HV battery, which stabilizes the HV bus voltage during transient load conditions.

Low Voltage DC–DC Converter. For FCVs without a HV battery, the 12V battery provides power to the HV DC bus and the fuel cell system when the vehicle is started. Therefore, a bidirectional DC–DC converter is needed to transfers power between the HV DC bus and the LV DC bus in both directions. Due to the slow dynamic properties of the fuel cell, a large voltage range applies for the HV DC bus voltage (Table 1.3).

In the case of an on-board HV battery, the electric system becomes similar to that of a series hybrid vehicle with the generator being replaced with a fuel cell. Thus, the specifications listed in Table 1.2 apply.

<i>Boost mode</i>	
HV port voltage range:	$V_1 = 230 \text{ V} \dots 450 \text{ V}$
LV port voltage range:	$V_2 = 8.5 \text{ V} \dots 16 \text{ V}$
Rated power, boost mode:	$P_{\text{out,nom}} = 3 \text{ kW}$ for 20 seconds
<i>Buck mode</i>	
HV port voltage range:	$V_1 = 230 \text{ V} \dots 450 \text{ V}$
LV port voltage range:	$V_2 = 13.3 \text{ V} \dots 14.4 \text{ V}$
Rated power, buck mode:	$P_{\text{out,nom}} = 2 \text{ kW}$, continuous
Galvanic isolation:	required due to safety reasons [5]
Other requirements:	low cost, high efficiency, high power density, low weight [22, 23, 24, 25]

Table 1.3: Specification of a bidirectional DC–DC converter for FCVs without HV battery (according to [20]); the output power, $P_{\text{out,nom}} = P_{\text{out}}$, is defined with (3.14).

1.1.2 Regenerative Power Systems

A variety of different applications of fuel cells (FCs), used to generate clean power from hydrogen and oxygen, exist. Besides the use in automobiles, typical applications include stand-alone residential power and small distributed power generation plants [29].

An ideal power generation system provides a sinusoidal voltage with constant magnitude and frequency, independent of load changes. The FC, however, represents a DC voltage source with a comparably high internal impedance and slow dynamics; varying power demand can only slowly be regulated by changing the flow-rate of supplied fuel. Thus, a typical power conditioning system (Figure 1.5) contains a battery which supports the fuel cell during transient power variations. FC and battery are both connected to a DC bus using different DC–DC converters in order to maintain a constant DC bus voltage (e.g. typically $\approx 400 \text{ V}$). For the FC, a unidirectional DC–DC converter is employed, for the battery, however, a bidirectional DC–DC converter is required in order to allow for charging and discharging modes of operations. The nominal battery voltage is typically selected according to the required power in order to obtain technically reasonable currents: for high power applications, e.g. higher than 5 kW, a HV battery may be selected, and for lower power requirements (e.g. below 5 kW), a low voltage battery with a nominal terminal voltage of 12 V, 24 V, 36 V or 48 V is typically used, due to higher reliability and lower cost [17, 27, 30, 31]. With a low voltage battery

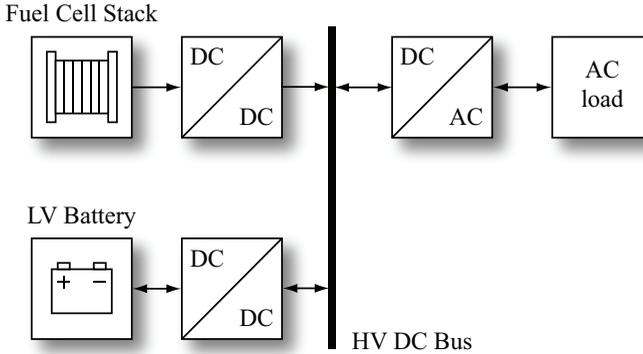


Figure 1.5: Power system architecture of a FC power generation system; the battery supports the fuel cell during transient load conditions [29].

being employed, it is reasonable to consider a bidirectional DC–DC converter with a transformer, by reason of the large voltage ratio between the DC bus voltage and the battery voltage [32].

In literature, similar power conditioning systems are described for stand-alone photovoltaic (PV) power generation systems; e.g., in [33], a battery and an ultra-capacitor interface to the HV DC bus via bidirectional DC–DC converters is proposed in order to provide a stable bus voltage (Figure 1.6). Since the solar panel cannot accept electric energy, a unidirectional DC–DC converter transfers power from the solar panel to the DC bus, whereas a bidirectional converter is used to charge and discharge the battery. Again, the battery may be selected according to the required power level. For a nominal power of up to 5 kW, a low voltage battery is typically used.

Thus, a bidirectional DC–DC converter similar to the converter employed in automotive applications can be used for FC power plants and PV power systems. However, different to the automotive applications, equal nominal power requirements apply to the two directions of power transfer (i.e. $P_{2,\text{nom}} = -P_{1,\text{nom}}$, cf. (3.14)).

1.1.3 Uninterruptible Power Supplies (UPS)

A UPS reliably provides electric power to important loads. One prominent UPS system is the so-called on-line UPS which contains a mains connected rectifier, a battery-buffered HV DC bus, and an inverter (Figure 1.7, [34]). During normal operation of the mains, the rectifier provides electric power to

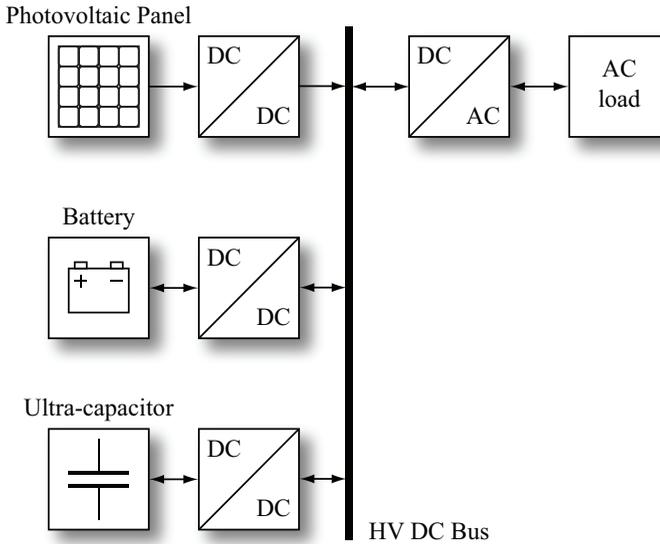


Figure 1.6: Power system architecture of a PV power generation system: the battery provides electric power during a shortage of electric power obtained from the PV panel, and the ultra-capacitor provides power during transient load conditions [33].

the HV DC bus and to the bidirectional DC–DC converter in order to charge the battery; a triac can be used to bypass the inverter. During a mains power failure, the battery provides power to the load (via the bidirectional DC–DC converter and the inverter).

Similar to regenerative power systems, different batteries may be used, depending on the required output power. If a low voltage battery is used (e.g. nominal voltage of 12 V, 24 V, 36 V, or 48 V), a bidirectional DC–DC converter with transformer is typically employed, due to the large ratio $V_1 : V_2$ of the DC bus voltages (e.g. 400 V : 12 V). Thus, for UPS applications and for regenerative power systems, basically the same specifications apply for the respective bidirectional DC–DC converters (cf. Section 1.1.2).

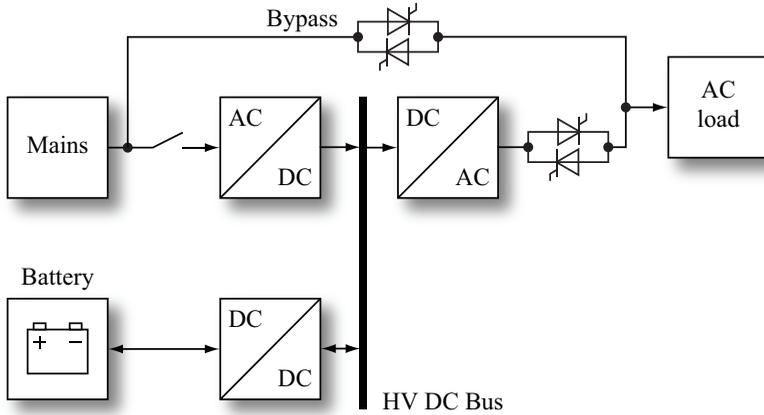


Figure 1.7: Power system architecture of the on-line UPS presented in [34].

1.2 Specifications of the Investigated DC–DC Converter

The specifications of the bidirectional DC–DC converter investigated in this work (Table 1.4) have been compiled in collaboration with industry partners. The DC–DC converter comprises of a high voltage (HV) port with the terminal voltage V_1 ($240\text{ V} \leq V_1 \leq 450\text{ V}$; nominal voltage $V_1 = 340\text{ V}$) and a low voltage (LV) port with the terminal voltage V_2 ($11\text{ V} \leq V_2 \leq 16\text{ V}$; nominal voltage $V_2 = 12\text{ V}$). A nominal output power P_{out} of 2 kW is required within the specified voltage ranges and in both directions of power transfer. Moreover, the low voltage port needs to be isolated from the high voltage port.

Further objectives regarding the selection and the design of the bidirectional DC–DC converter are (in the order of the considered priorities):

1. Converter efficiency $> 90\%$ at the nominal operating point ($V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$, $P_{\text{out}} = \pm 2\text{ kW}$),⁴
2. Converter efficiency $> 90\%$ within reasonable input and output voltage ranges and reasonable power ranges,
3. Low converter volume (i.e. high power density).

⁴Positive values P_{out} denote a power transfer from the HV port to the LV port and negative P_{out} denotes a power transfer from the LV port to the HV port, cf. (3.14).

An important design parameter to be defined in this Chapter is the switching frequency f_S . The selected value, $f_S = 100$ kHz, however, is rather based on general considerations than on an in-depth system optimization. Besides, a constant switching frequency is required by the industry partners in order to reduce potential EMI issues.

Provided that no thermal limitations apply, the volumes of inductors, transformers, and capacitors decrease with increasing switching frequency. Therefore, the power density of a converter can be increased by increasing the switching frequency [35]. However, the local conduction losses due to high frequency effects (skin and proximity effects), the local core losses, and the switching losses increase with increasing switching frequency. Thus, thermal limitations apply at high switching frequencies and the required total converter volume increases if the switching frequency becomes higher than the optimum switching frequency (calculated with respect to maximum total power density) [36, 37, 38, 39].

In [38, 39] two different DC–DC converters are optimized with respect to maximum power density. The following list summarizes the obtained results.

1. From [38]: resonant LCC DC–DC converter with unidirectional power flow, $V_1 = 320$ V, $V_2 = 26$ V, $P_2 = 3.9$ kW ($I_2 = 150$ A), considered heat sink: aluminum heat sink optimized with respect to low volume; calculated power density: $p = 7.48$ kW/dm³, calculated efficiency: $\eta = 93.9\%$, calculated optimum switching frequency: $f_S = 147.1$ kHz;
2. from [38]: resonant LCC DC–DC converter with unidirectional power flow, $V_1 = 320$ V, $V_2 = 26$ V, $P_2 = 3.9$ kW ($I_2 = 150$ A), considered heat sink: copper heat sink optimized with respect to low volume; calculated power density: $p = 13.3$ kW/dm³, calculated efficiency: $\eta = 93.7\%$, calculated optimum switching frequency: $f_S = 176$ kHz;
3. from [39]: DC–DC converter with unidirectional power flow (integrated current doubler topology), $V_1 = 400$ V, 48 V $\leq V_2 \leq 56$ V, $P_2 = 5$ kW (105 A $> I_2 > 89$ A), considered heat sink: copper heat sink optimized with respect to low volume; calculated power density: $p = 10.2$ kW/dm³, calculated efficiency: $\eta = 96.1\%$, calculated optimum switching frequency: $f_S = 92.9$ kHz (for $V_2 = 54$ V).

Besides the unidirectional power transfer capability, the specifications of the above listed DC–DC converters are similar to the required bidirectional DC–DC converter, i.e. optimum switching frequencies in the range ≈ 90 kHz $< f_S < 200$ kHz result.

The considered switching frequency, $f_S = 100$ kHz, is selected close to the lowest value of the above presented optimal switching frequencies, due to the expected impact of skin and proximity effects on the conduction losses of the

<i>Property</i>	<i>Value</i>	<i>Description</i>
V_1	$240 \text{ V} \leq V_1 \leq 450 \text{ V}$	minimum and maximum voltages at the high voltage (HV) port
	340 V	nominal HV port voltage
V_2	$11 \text{ V} \leq V_2 \leq 16 \text{ V}$	minimum and maximum voltages at the low voltage (LV) port
	12 V	nominal LV port voltage
P_{out}	2 kW	nominal output power, HV \rightarrow LV
	-2 kW	nominal output power, LV \rightarrow HV
f_s	100 kHz	switching frequency
Additional requirements:		
<ul style="list-style-type: none"> • galvanic isolation • high conversion efficiency (>90% at the nominal operating point) • low converter volume • constant switching frequency 		

Table 1.4: Specifications of the investigated bidirectional DC–DC converter.

LV side (Section 4.2 and Appendix A.2.3) and due to the expected switching losses on the LV side (Section 4.3.3)

1.3 Objectives and New Contributions of the Work

The objective of this work is to select a converter topology which is suitable to fulfill the requirements specified in Section 1.2. Furthermore, the selected converter topology is optimized with respect to a high converter efficiency in order to meet the target of a required converter efficiency of more than 90% within reasonable input and output voltage ranges and reasonable power ranges.

The new contributions of this work are:

- a comprehensive overview on bidirectional DC–DC converter topologies, including a comparison of the different converters that are suitable to fulfill the given specifications (Chapter 2); in that context, the extensions of the unidirectional resonant LCC and LLC converters with respect to bidirectional operation are investigated;
- an optimal modulation scheme for the lossless DAB converter (with

respect to minimum transformer RMS current; Section 3.1.3);

- a detailed model used to predict the power losses of the investigated DAB converter, which includes the impact of high frequency harmonic components on the conduction and copper losses, switching losses, and core losses (Chapter 4);
- an examination of the results obtained from a numerical optimization of the modulation parameters D_1 and D_2 of the DAB converter with respect to maximum converter efficiency and a synthesis of an efficiency optimized modulation scheme of the given DAB converter (Section 5.2);
- a detailed small-signal control-oriented model of the DAB converter, which includes the dynamic properties of the EMI filters connected to the converter ports (Chapter 6);
- a design procedure to determine appropriate values for the turns ratio n and the inductance L of the DAB converter (Appendix A.2).

Six scientific papers and one patent have been published in the course of this dissertation:

- F. Krismer, J. W. Kolar, “Accurate Small-Signal Model for the Digital Control of an Automotive Bidirectional Dual Active Bridge,” IEEE Transactions on Power Electronics, vol. 24, no. 12, pp. 2756–2768, Dec. 2009.
- F. Krismer, J. W. Kolar, “Accurate Power Loss Model Derivation of a High Current Dual Active Bridge Converter for an Automotive Application,” IEEE Transactions on Industrial Electronics, vol. 57, no. 3, pp. 881–891, March 2010.
- F. Krismer, J. W. Kolar, “Efficiency-Optimized High Current Dual Active Bridge Converter for Automotive Applications,” IEEE Transactions on Industrial Electronics, accepted for future publication, 2011.
- F. Krismer, J. Biela, J. W. Kolar, “A Comparative Evaluation of Isolated Bi-directional DC/DC Converters with Wide Input and Output Voltage Range,” in Conf. Rec. of the IEEE 40th Annual Industry Applications Conference IAS 2005, Hong Kong, China, 2–6 Oct. 2005, pp. 599–606.
- F. Krismer, S. Round, J. W. Kolar, “Performance Optimization of a High Current Dual Active Bridge with a Wide Operating Voltage Range,” in Proc. of the IEEE 37th Annual Power Electronics Specialists Conference PESC 2006, Jeju, Korea, 18–22 June 2006, pp. 1–7.

- F. Krismer, J. W. Kolar, “Accurate Small-Signal Model for an Automotive Bidirectional Dual Active Bridge Converter,” in Proc. of the 11th Workshop on Control and Modeling for Power Electronics COMPEL, Zürich, Switzerland, 17–20 Aug. 2008, pp. 1–10.
- F. Krismer, J.W. Kolar: „Verfahren zur schaltverlustminimalen Steuerung eines bidirektionalen nicht potentialgetrennten Gleichspannungswandlers mit überlappendem Ein- und Ausgangsspannungsbereich.“

1.4 Chapter Overview

Chapter 2 gives an overview on different bidirectional DC–DC converters and investigates the applicability of the different converter topologies with respect to the specifications given in Table 1.4. Based on the findings of Chapter 2, the single-phase DAB converter topology is considered most promising with respect to the achievable converter efficiency and the achievable power density. Moreover, due to the wide input and output voltage ranges, two-stage DC–DC converters, i.e. the series connection of an isolated DC–DC converter and a DC–DC converter without isolation, are expected to facilitate an improved converter efficiency.

In **Chapter 3**, the working principle of the DAB converter is explained based on different simplified converter models. This includes the lossless converter model (Figure 3.2), which facilitates basic analytical investigations and allows for a simplified synthesis of advanced modulation schemes. Moreover, two different refinements of the electric DAB converter model are presented in order to include the impacts of the conduction losses and the magnetizing current on the transformer currents.

Chapter 4 presents a detailed loss model of the DAB, needed in order to parameterize the models developed in Chapter 3 and to develop the efficiency optimized modulation presented in Chapter 5. This loss model is used to calculate the losses in the most relevant converter components, i.e. the semiconductor switches (conduction and switching losses), the transformer (copper and core losses), and the inductor (copper and core losses).

Chapter 5 details a systematic investigation of efficiency improvements achievable for the given DAB converter, obtained with the use of optimized modulation schemes. Finally, with the suboptimal modulation schemes discussed in Section 5.2.2, converter operation close to its maximum possible efficiency is achieved (Figure 5.28). The calculated results are verified using experimental data.

In **Chapter 6**, a detailed small-signal control-oriented model of the DAB and a dynamic model of the complete converter system (including the digital

control platform) are derived. Moreover, Section 6.2.6 illustrates an effective method to derive a simplified transfer function of a given DAB converter. The calculated results are verified using experimental data.

Chapter 7 investigates the most promising two-stage converter configurations (out of the configurations depicted in Figure 2.22) in order to compare the efficiencies achieved with the two-stage topologies to the efficiencies obtained with the single-stage DAB converter. However, the average efficiency achieved with the two-stage converter ($\bar{\eta} = 93.0\%$; calculated according to Appendix A.1) is less than the average efficiency achieved with the single-stage DAB ($\bar{\eta} = 93.5\%$). Thus, in average, the additional losses of the non-isolated DC–DC converter cannot outweigh the loss reduction achieved for the DAB converter.

Chapter 8 summarizes the obtained results and concludes this work. Furthermore, Chapter 8 presents an outlook regarding future research in the field of the DAB converter.

The **Appendices** include:

- details on the converter designs (**Appendix A**);
- the methods used to calculate the VA ratings needed for the converter comparison (**Appendix B**);
- the calculation of the Steinmetz parameters k , α , and β (**Appendix C**);
- an evaluation of suitable power MOSFETs (**Appendix D**);
- information regarding the practical implementation of the proposed modulation schemes (**Appendix E**);
- supplemental information on the small-signal control-oriented model of the DAB converter (**Appendix F**).

Chapter 2

Bidirectional and Isolated DC–DC Converter Topologies

2.1 Derivation of Bidirectional DC–DC Converters

In principle, bidirectional power transfer between two unipolar DC voltage sources may be established with two unidirectional DC–DC converters C_1

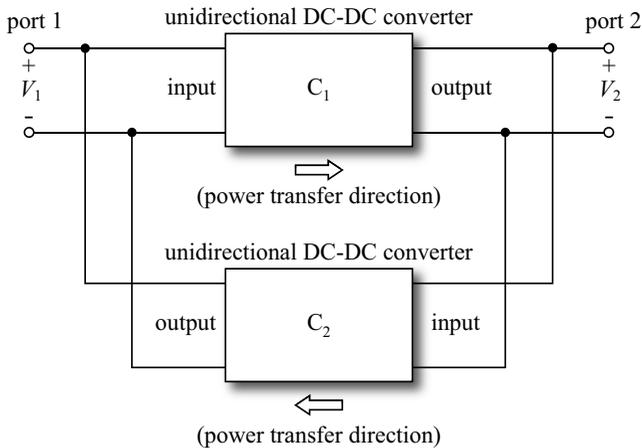


Figure 2.1: Principle construction of a bidirectional DC–DC converter using two unidirectional DC–DC converters.

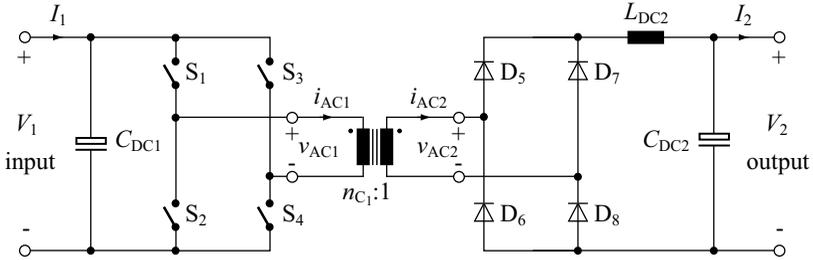


Figure 2.2: Unidirectional full bridge DC–DC converter with output inductor L_{DC2} . The converters C_1 and C_2 in Figure 2.1 can be replaced by the depicted unidirectional full bridge converter, however, for C_2 , the indices 1 and 2 need to be interchanged.

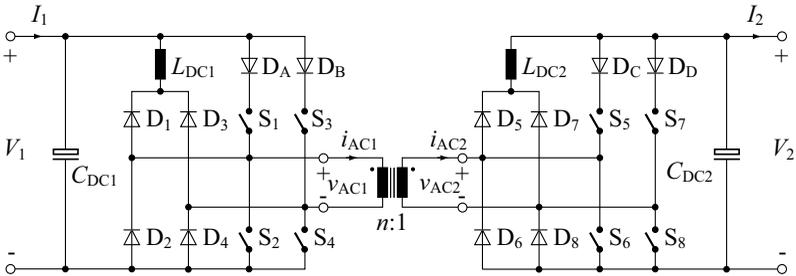


Figure 2.3: Bidirectional full bridge DC–DC converter topology, constructed from two unidirectional full bridge DC–DC converters C_1 and C_2 according to Figure 2.1 and Figure 2.2; the diodes D_A , D_B , D_C , and D_D are required in order to avoid reverse blocking voltages on $S_1 \dots S_8$ [40].

and C_2 according to Figure 2.1. There, C_1 is used to transfer power from port 1 to port 2 (forward direction, forward operating mode) and C_2 is needed to transfer power in the opposite direction (backward direction, backward operating mode). In order to illustrate an example of a practical converter realization including galvanic isolation, full bridge DC–DC converters with high frequency (HF) transformers and output inductors are employed for C_1 and C_2 (Figure 2.2).¹ According to [40], the inverter stages of C_1 and C_2 can

¹For the sake of clarity, the full bridge DC–DC converters C_1 and C_2 are considered lossless and without any parasitic inductive and capacitive components. Additionally, very large smoothing inductors (e.g. L_{DC2} in Figure 2.2) are considered and hence the characterization of the system functionality confines to the rectifiers being operated in

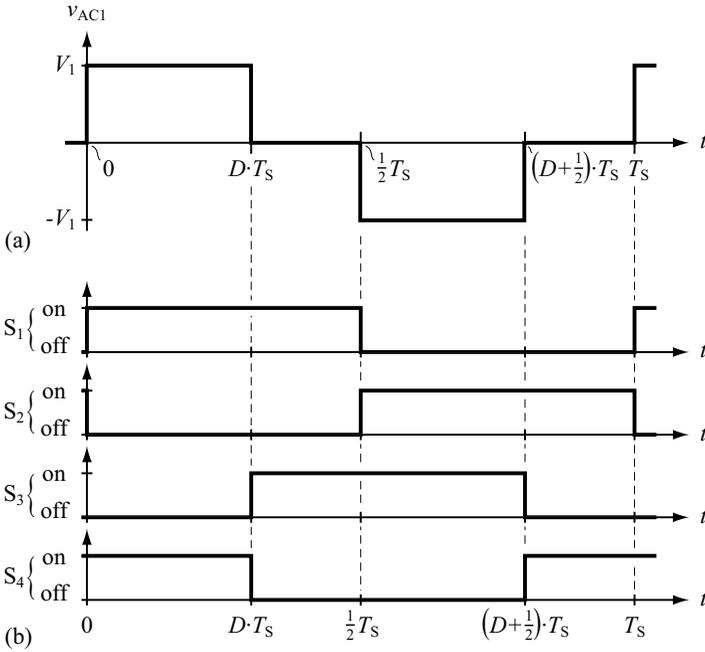


Figure 2.4: (a) Transformer voltage $v_{AC1}(t)$ generated with the inverter stage of the DC–DC converter depicted in Figure 2.2 and Figure 2.3 (for the assumption of an ideal HF transformer); (b) respective switching states of S_1 , S_2 , S_3 , and S_4 .

even be combined with the rectifier stages of C_2 and C_1 and thus, the resulting bidirectional DC–DC converter only contains a single HF transformer (Figure 2.3).

In forward mode of operation, i.e. power is transferred from port 1 to port 2 (cf. Figure 2.1), the converter C_1 is active and its inverter stage applies a rectangular AC voltage $v_{AC1}(t)$ with constant frequency $f_s = 1/T_s$ and arbitrary duty cycle $0 < D < 0.5$ to the primary winding of the HF transformer (Figure 2.4). The (ideal) HF transformer simply alters the AC voltage amplitude according to its turns ratio n_{C_1} , i.e. $v_{AC2}(t) = v_{AC1}(t)/n_{C_1}$, and applies v_{AC2} to the rectifier. On the assumption of ideal low-pass filtering and continuous conduction mode of operation, the rectified output voltage V_2

continuous conduction mode.

results:

$$V_2 = 2 \cdot D \cdot V_1 / n_{C_1}. \quad (2.1)$$

According to Figure 2.4, the duty cycle is limited to values between 0 and 0.5. Therefore, regarding (2.1), $V_2 < V_1 / n_{C_1}$ must hold true for all operating points within the required voltage ranges (Table 1.4) and thus, the transformer turns ratio of C_1 is limited according to

$$n_{C_1} < V_{1,\min} / V_{2,\max} = 240 \text{ V} / 16 \text{ V} = 15. \quad (2.2)$$

In the backward operating mode, the converter C_2 is active and feeds power from port 2 to port 1 (Figure 2.1). Similar to (2.1), V_1 is calculated from

$$V_1 = 2 \cdot D \cdot V_2 / n_{C_2}. \quad (2.3)$$

Hence, for operation within the specified voltage ranges,

$$n_{C_2} < V_{2,\min} / V_{1,\max} = 11 \text{ V} / 450 \text{ V} \approx 24.4 \cdot 10^{-3} \quad (2.4)$$

applies to the transformer turns ratio of the converter C_2 .

According to (2.2) and (2.4), the turns ratio n of the HF transformer employed for the bidirectional DC–DC converter depicted in Figure 2.3 must be changed if the direction of power transfer changes: during forward mode of operation, $n < 15$ is required and during backward mode of operation, $n > 1 / (24.4 \cdot 10^{-3}) \approx 41$ is needed. Thus, the converter shown in Figure 2.3 is considered to be inappropriate with respect to the required specifications (Table 1.4).

In a different approach, the switches and the diodes of a unidirectional full bridge DC–DC converter are modified according to Figure 2.5 in order to achieve bidirectional power transfer within the specified voltage ranges. There, the switches S_1 , S_2 , S_3 , and S_4 as well as the diodes D_5 , D_6 , D_7 , and

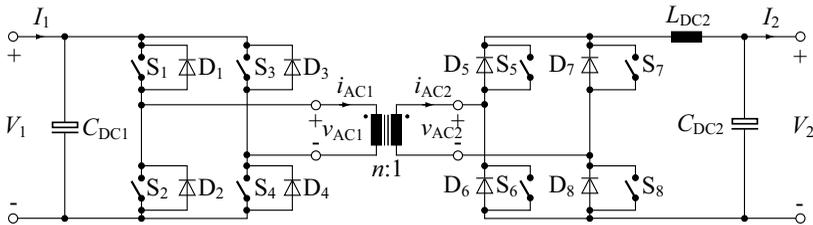


Figure 2.5: Bidirectional full bridge DC–DC converter, derived from the unidirectional DC–DC converter depicted in Figure 2.2.

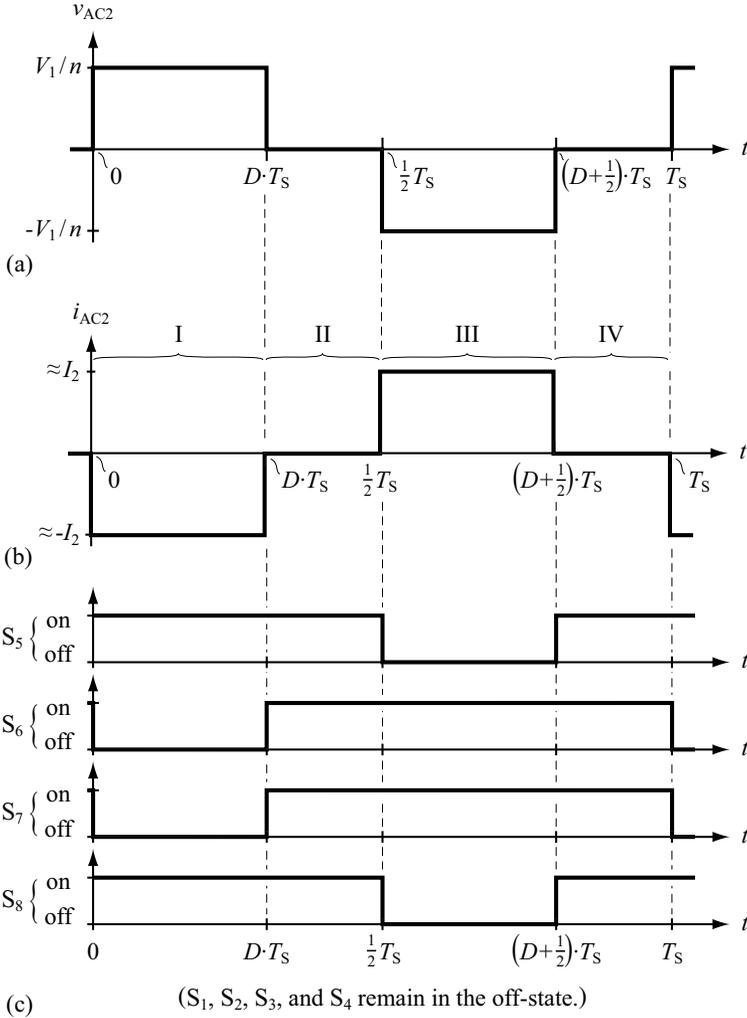


Figure 2.6: (a) Transformer voltage $v_{AC2}(t)$ and (b) transformer current $i_{AC2}(t)$ generated in backward mode (for the assumption of an ideal HF transformer); (c) respective switching states of $S_5, S_6, S_7,$ and S_8 (cf. Figure 2.5). During the time intervals II ($D \cdot T_s < t_{II} < T_s/2$) and IV [$(D + 1/2) \cdot T_s < t_{IV} < T_s$] the switches $S_5, S_6, S_7,$ and S_8 remain in the on-state in order to magnetize L_{DC2} ; hence, $v_{AC2}(t_{II}) = 0$ and $v_{AC2}(t_{IV}) = 0$. Thus, the rectifier diodes $D_1, D_2, D_3,$ and D_4 are blocking within the time intervals II and IV, i.e. $i_{AC2}(t_{II}) = i_{AC2}(t_{IV}) = 0$.

D_8 are extended with respective diodes and switches connected in parallel. With this modification, the operation in forward mode remains unchanged and the output voltage is still determined with (2.1). In backward mode of operation, the switching states shown in Figure 2.6 (c) are employed in order to impress a rectangular AC current $i_{AC2}(t)$ [Figure 2.6 (b)] on the secondary winding of the HF transformer. The primary side transformer current $i_{AC1}(t) = i_{AC2}(t)/n$ is then rectified with $D_1 \dots D_4$ and filtered with C_{DC1} ,

$$I_1 = 2 \cdot D \cdot I_2/n. \quad (2.5)$$

Due to the absence of losses, the same input and output power levels result, i.e. $V_2 \cdot I_2 = V_1 \cdot I_1$. This, together with (2.5), yields the voltage transfer ratio

$$V_1 = V_2 \cdot n/(2 \cdot D) \quad (2.6)$$

in backward mode, which is identical to the forward mode voltage transfer ratio (2.1). Thus, (2.2) determines the required transformer turns ratio for backward operation, as well; the given circuit allows for bidirectional power transfer according to the specifications given in Table 1.4.

2.2 Topological Overview

The different components of a bidirectional DC–DC converter with galvanic isolation are depicted in Figure 2.7:

- The *port 1 and port 2 filter networks* provide smooth terminal voltages and currents. For each filter network, at least a single capacitor or a single inductor is employed.
- The *DC–AC converter* is a switch network which provides AC power to the HF transformer and the *AC–DC converter* supplies DC power to the receiving port; both converters must allow for bidirectional power

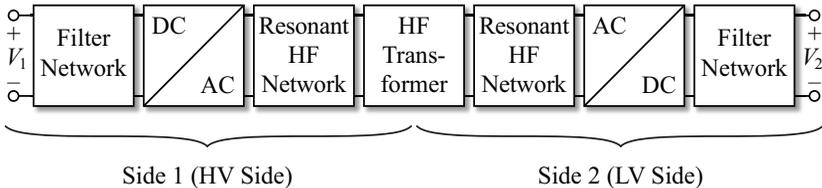


Figure 2.7: The different components required for an isolated, bidirectional DC–DC converter.

transfer. Typically, full bridge circuits, half bridge circuits, and push-pull circuits are employed. However, different solutions (e.g. the single switch networks used in a bidirectional flyback converter) are reported, as well [41, 42].

- The *reactive HF networks* provide energy storage capability within the HF AC part and are used to modify the shapes of the switch current waveforms in order to achieve low switching losses (cf. Section 4.3.2, [35, 43]). Even though, these parts are not necessarily required for a fully functional bidirectional DC–DC converter, they will always be present in practice due to the parasitic components of the HF transformer (e.g. stray and magnetizing inductances, parasitic capacitances).
- The *HF transformer* is required in order to achieve electric isolation; it further enables large voltage and current transfer ratios. The HF transformer is considered superior over a low frequency transformer, since transformer and filter components become smaller (and often less expensive) at higher frequencies [35].²

Bidirectional DC–DC converter topologies with a system configuration according to Figure 2.7, are called *Single-Stage Topologies* [45, 46] (Section 2.2.1), since they contain a minimum number of conversion stages. Accordingly, the total number of required components is comparably low. However, the operation within wide input and output voltage ranges causes ineffective transformer and switch utilization. Improved transformer and switch utilization is achieved with multi-stage topologies, which contain an additional power converter in order to adjust voltage and current levels (Section 2.2.2; the efficiencies obtained from different two-stage topologies are presented in Section 7.2.8).

2.2.1 Single-Stage Topologies

In the presented approach, single-stage topologies are grouped into

1. converters with a low number of switches,
2. dual bridge converters without resonant HF network, and
3. dual bridge converters with resonant HF network,

according to the increasing complexity of the investigated systems (Figure 2.8).

²However, the converter losses (e.g. magnetizing losses, switching losses, losses due to skin- and proximity-effects) increase with increasing frequency; depending on the requirements and on the employed topology, an optimum switching frequency can be determined [44].

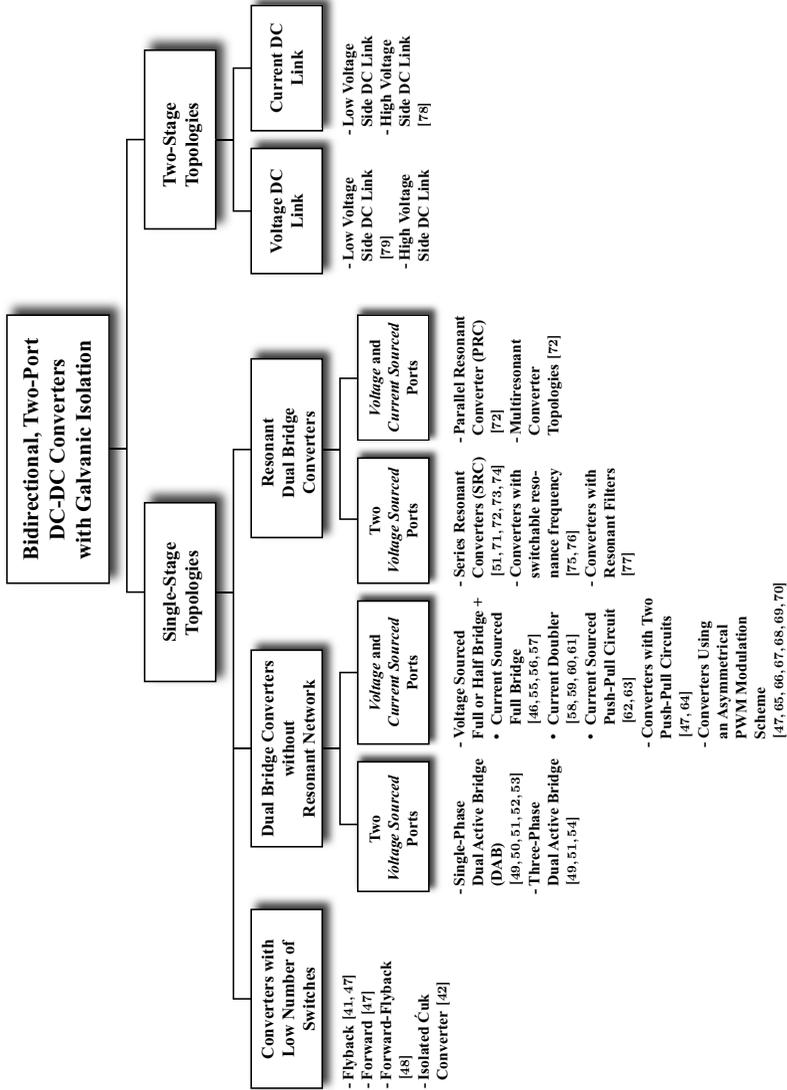


Figure 2.8: Topological overview of bidirectional DC–DC converter topologies. The topologies are classified according to the number of conversion stages, the employed switch circuits, the complexity of the HF network, and the port types (cf. Figure 2.7 and Figure 2.9).

The first group contains isolated and bidirectional flyback, forward, and Ćuk converter topologies which are typically employed for applications with an output power well below 2 kW. Main advantages of the forward and flyback converters are simple circuit structures and low numbers of required switches; however, ineffective transformer and switch utilizations render these topologies inappropriate with respect to the given specifications.

Improved utilization of the HF transformer is achieved with the Ćuk converter topology presented in [42], which has been designed according to the specifications given in Table 1.4 in order to investigate advantages and disadvantages (additional assumptions are listed in Table 2.1).³ The component stress values are calculated according to Appendix B and [42]; Table 2.1 lists the respective results. In anticipation of the results calculated for the final converter candidates (Table 2.2), very competitive VA ratings are found for the HF transformer and for the switches of the Ćuk converter. However, a number of major disadvantages render this converter less attractive:

- The switches are operated in a hard switching manner (cf. Section 4.3.2). In order to achieve a high efficiency and a high switching frequency, snubber networks are required [42].
- The switch stress is not distributed over a number of components: a single HV switch with a VA rating of 11.0 kVA and a single 10.2 kVA LV switch are needed. At the switching instant, high instantaneous voltages (HV: 754 V, LV: 40 V, with the voltage spikes during switching being neglected) and high instantaneous currents (HV: 21.4 A, LV: 407 A) occur.
- Two DC blocking capacitors are required and both carry the full transformer current (HV: 9.9 A, LV: 189 A). Thus, a capacitor with a very high current rating of 189 A is required on the LV side.
- Two filter inductors with a total magnetic energy storage capability of 89 mJ are required.

The converter topologies of the second group in Figure 2.8 contain DC–AC and AC–DC converters with more than a single switch: either full bridges, half bridges or push-pull converters are employed. Furthermore, a simple, non-resonant HF network – most often an inductor in series to the transformer stray inductance or the transformer stray inductance itself – is typically considered.

³The transformer turns ratio $n = 19$ has been selected in order to achieve an approximately balanced VA rating for the switches on the HV and on the LV side. Additionally, a maximum blocking voltage of 754 V results for the HV side switches and thus, MOSFETs with a breakdown voltage of 1000 V have to be employed.

<p><i>Assumptions</i></p> <p>Assumed efficiency at full load:</p> <p>Selected turns ratio $n = N_1 : N_2$:</p> <p>Peak-to-peak current ripple, HV side:</p> <p>Peak-to-peak current ripple, LV side:</p>	<p>90%</p> <p>19</p> <p>$\leq 40\%$ of full load DC curr.</p> <p>$\leq 40\%$ of full load DC curr. (selected in accordance to Appendix A.5.2)</p>
<p><i>HV side switches</i></p> <p>Peak voltage:</p> <p>Peak current:</p> <p>Max. RMS current:</p> <p>VA rating:</p> <p><i>LV side switches</i></p> <p>Peak voltage:</p> <p>Peak current:</p> <p>Max. RMS current:</p> <p>VA rating:</p>	<p>754 V</p> <p>21.4 A</p> <p>14.6 A</p> <p>11.0 kVA</p> <p>40 V</p> <p>407 A</p> <p>258 A</p> <p>10.2 kVA</p>
<p><i>Transformer</i></p> <p>Max. equiv. value of the HV side transf. voltage [cf. (B.5)]:</p> <p>Max. HV side RMS current:</p> <p>Max. equiv. value of the LV side transf. voltage [cf. (B.5)]:</p> <p>Max. LV side RMS current:</p> <p>VA rating:</p>	<p>403 V</p> <p>9.9 A</p> <p>21.2 V</p> <p>189 A</p> <p>4.0 kVA</p>
<p><i>HV side inductor</i></p> <p>Employed inductance:</p> <p>Peak current:</p> <p>Peak energy:</p> <p><i>LV side inductor</i></p> <p>Employed inductance:</p> <p>Peak current:</p> <p>Peak energy:</p>	<p>920 μH</p> <p>10.0 A</p> <p>46 mJ</p> <p>1.7 μH</p> <p>224 A</p> <p>43 mJ</p>

Table 2.1: Ćuk converter topology: assumed specifications and results.

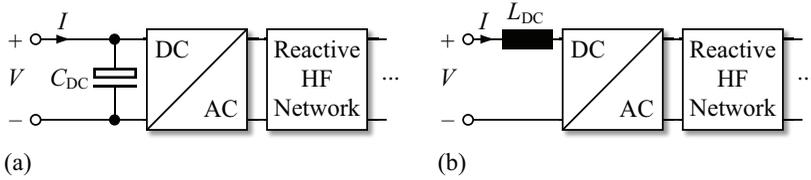


Figure 2.9: DC–AC converter with different terminations of the DC port: (a) voltage sourced port, (b) current sourced port.

Compared to the flyback and forward converters, the converters of the second group achieve a much more effective converter utilization. In particular, the semiconductor switches can be operated with low switching losses (soft switching, Section 4.3.2) and hence, a converter with a high power density is feasible.

Most prominent members of this second group are the aforementioned bidirectional full bridge DC–DC converter (Section 2.1) and the Dual Active Bridge converter (Figure 2.10, Chapters 3, 4 and 5).

The third group contains DC–DC converters with resonant HF networks (so-called resonant DC–DC converters), which, in particular, offer increased capabilities regarding the utilization of the semiconductor switches, since the resonant network modifies the waveforms of the switch currents; this property can be used to achieve low switching losses (cf. Section 4.3.2, [43]). Disadvantages are the higher converter complexity and the additionally required power components.

Besides the classification with respect to the complexity of the regarded power converter (3rd row in Figure 2.8), single-stage topologies may as well be classified with respect to the type of filter impedances which are directly connected to the DC ports of the DC–AC and AC–DC converters in Figure 2.7. In case of a capacitor, the port is denoted *voltage sourced* [Figure 2.9 (a)] and in case of an inductor, the port is denoted *current sourced* [Figure 2.9 (b), [80]]. If higher order filters are employed, the impedance directly connected to the switching network determines the port type. This second kind of classification is employed to further distinguish between the different converter topologies (4th row in Figure 2.8).

With respect to the given specifications (Table 1.4) and in anticipation of the findings obtained from the discussions given below, the following 6 converter topologies are considered to be the most relevant single-stage topologies.

- Single-phase Dual Active Bridge (DAB) converter (Figure 2.10, designed in Appendix A.2)
- Three-phase DAB converter (Figure 2.11, designed in Appendix A.3)
- LLC converter (Figure 2.18, designed in Appendix A.4)
- Bidirectional and isolated full bridge topology (Figure 2.12, designed in Appendix A.5)
- Bidirectional and isolated current doubler topology (Figure 2.13, designed in Appendix A.6)
- Bidirectional and isolated push-pull topology (Figure 2.14, designed in Appendix A.7)

In order to allow for a meaningful comparison, the different converter topologies have been designed separately. For this, the transformer turns ratios and the HF network component values, needed for the DAB converters (single-phase and three-phase) and the LLC converter, are optimized with respect to maximum average efficiency (cf. Appendix A.1). Moreover, for the single-phase DAB converter and the LLC converter, two different modulation schemes have been considered (conventional phase shift modulation and efficiency optimal modulation, cf. Section 3.1 and Section 5.2.1). For the isolated full bridge converter, the isolated current doubler topology, and the isolated push-pull converter, the transformer turns ratio is limited according to (2.2) and the assumptions listed in Table A.15 and Table A.17 are used to design the converters.

Table 2.2 lists the resulting component stress values obtained for the different DC–DC converters (only the power stages are considered; additionally required EMI filter components are discarded). The results of the converter designs outlined in Appendix A (i.e. component values, calculated average converter efficiencies) are given in Table 2.3.

Dual Bridge Converters without Resonant Network

Most prominent converter topologies within this group are the Dual Active Bridge (DAB) converter [49, 50, 51, 52, 53] and the bidirectional and isolated full bridge converter [46, 55, 56, 57] (including converter variants, e.g. with a current doubler circuit [58, 59] or a push-pull circuit [47, 62, 63, 65] being employed on the LV side).

Topologies	DAB (Conv. Mod., Section 3.1.2)	DAB (Opt. Mod., Section 5.2.1)	Three-Phase DAB [54]	LLC (Conv. Mod., Appendix A.4.3)	LLC (Opt. Mod., Appendix A.4.4)	Full Bridge Converter			
						Current Fed Full Bridge	Current Doubler	Current Fed Push Pull	
Circuit	Fig. 2.10						Fig. 2.12	Fig. 2.13	Fig. 2.14
No. of act. components	8	8	12	8	8	8	6	6	
<i>HV side</i>									
Switch peak volt.	450 V	450 V	450 V	450 V	450 V	450 V	450 V	450 V	
Switch peak curr.	29.0 A	23.9 A	14.2 A	23.2 A	22.2 A	22.6 A	25.9 A	22.6 A	
Max. switch RMS current	11.0 A	9.6 A	6.4 A	10.0 A	9.8 A	14.2 A	15.9 A	14.2 A	
\sum switches VA rating	19.8 kVA	17.3 kVA	17.4 kVA	18.0 kVA	17.6 kVA	25.5 kVA	28.6 kVA	25.5 kVA	
<i>LV side</i>									
Switch peak volt.	16 V	16 V	16 V	16 V	16 V	37.5 V	75 V	75 V	
Switch peak curr.	550 A	407 A	285 A	465 A	377 A	236 A	251 A	236 A	
Max. switch RMS current	208 A	163 A	129 A	203 A	164 A	157 A	159 A	157 A	
\sum switches VA rating	13.3 kVA	10.5 kVA	12.4 kVA	13.0 kVA	10.5 kVA	23.5 kVA	23.8 kVA	23.5 kVA	

Table 2.2: Converter topologies: semiconductor switches.

Topologies	DAB (Conv. Mod., Section 3.1.2)	DAB (Opt. Mod., Section 5.2.1)	Three-Phase DAB [54]	Full Bridge Converter		
	2	2		3	3	3
No. of magn. components	2	2	6	3	3	3
Transformer turns ratio	19 : 1	17 : 1	20 : 1	17 : 1	12 : 1	12 : 1
Max. equiv. transf. volt. (HV, LV) cf. (B.4), (B.5)	338 V, 17.8 V	302 V, 17.8 V	158 V, 7.9 V	304 V, 17.9 V	213 V, 17.8 V	213 V, 35.5 V
Max. RMS transf. curr. (HV, LV)	15.6 A, 294 A	13.6 A, 231 A	9.1 A, 182 A	13.8 A, 231 A	20.0 A, 241 A	22.5 A, 135 A
Transf. VA	5.2 kVA	4.1 kVA	4.3 kVA	4.2 kVA	4.3 kVA	4.8 kVA
Max. DC inductor currents	L : 0 A	L : 0 A	L : 0 A	L : 0 A L_M : 0 A	L : 0 A L_{DC2} : 202 A	L : 0 A L_{DC2a} : 101 A L_{DC2b} : 101 A
Max. RMS inductor currents	L : 15.6 A	L : 13.6 A	L : 9.1 A	L : 14.2 A L_M : 0.3 A	L : 20.0 A L_{DC2} : 202 A	L : 22.5 A L_{DC2a} : 102 A L_{DC2b} : 102 A
Peak inductor currents	L : 29.0 A	L : 23.9 A	L : 14.2 A	L : 23.2 A L_M : 0.5 A	L : 22.6 A L_{DC2} : 226 A	L : 25.9 A L_{DC2a} : 129 A L_{DC2b} : 129 A
Peak inductor energies	L : 11.2 mJ	L : 6.2 mJ	$3 \times L$: 6.7 mJ	L : 14.9 mJ L_M : 0.2 mJ	L : 1.6 mJ L_{DC2} : 21 mJ	L : 2.0 mJ L_{DC2a} : 14 mJ L_{DC2b} : 14 mJ
Inductor VA ratings	L : 4.1 kVA	L : 3.1 kVA	$3 \times L$: 3.8 kVA	L : 8.1 kVA L_M : 115 VA	L : 1.2 kVA	L : 1.6 kVA
				L : 5.2 kVA L_M : 0.3 kVA	L : 1.2 kVA	L : 1.2 kVA

Table 2.2 cont.: Converter topologies: magnetic components

<i>Topologies</i>	<i>DAB (Conn. Mod., Section 3.1.2)</i>	<i>DAB (Opt. Mod., Section 5.2.1)</i>	<i>Three-Phase DAB [54]</i>	<i>LLC (Conn. Appendix A.4.3)</i>	<i>LLC (Opt. Mod., Appendix A.4.4)</i>	<i>Full Bridge Converter +</i>		
						<i>Current Fed Full Bridge</i>	<i>Current Doubler</i>	<i>Current Fed Push Pull</i>
No. of capacitors	2	2	2	3	3	2	2	2
Peak capacitor voltages	$C_{Dc1}:450\text{ V}$ $C_{Dc2}:16\text{ V}$	$C_{Dc1}:450\text{ V}$ $C_{Dc2}:16\text{ V}$	$C_{Dc1}:450\text{ V}$ $C_{Dc2}:16\text{ V}$	$C_{Dc1}:450\text{ V}$ $C_{Dc2}:16\text{ V}$ $C:342\text{ V}$	$C_{Dc1}:450\text{ V}$ $C_{Dc2}:16\text{ V}$ $C:230\text{ V}$	$C_{Dc1}:450\text{ V}$	$C_{Dc1}:450\text{ V}$	$C_{Dc1}:450\text{ V}$
Peak cap. energies	$C_{Dc1}:333\text{ mJ}$ $C_{Dc2}:128\text{ mJ}$	$C_{Dc1}:333\text{ mJ}$ $C_{Dc2}:128\text{ mJ}$	$C_{Dc1}:333\text{ mJ}$ $C_{Dc2}:128\text{ mJ}$	$C_{Dc1}:333\text{ mJ}$ $C_{Dc2}:128\text{ mJ}$ $C:5.4\text{ mJ}$	$C_{Dc1}:333\text{ mJ}$ $C_{Dc2}:128\text{ mJ}$ $C:3.6\text{ mJ}$	$C_{Dc1}:333\text{ mJ}$	$C_{Dc1}:333\text{ mJ}$	$C_{Dc1}:333\text{ mJ}$
Cap. RMS currents	$C_{Dc1}:14.9\text{ A}$ $C_{Dc2}:244\text{ A}$	$C_{Dc1}:9.2\text{ A}$ $C_{Dc2}:125\text{ A}$	$C_{Dc1}:4.1\text{ A}$ $C_{Dc2}:66\text{ A}$	$C_{Dc1}:11.4\text{ A}$ $C_{Dc2}:271\text{ A}$ $C:14.2\text{ A}$	$C_{Dc1}:9.3\text{ A}$ $C_{Dc2}:122\text{ A}$ $C:13.8\text{ A}$	$C_{Dc1}:10.1\text{ A}$	$C_{Dc1}:10.7\text{ A}$	$C_{Dc1}:10.1\text{ A}$
Capacitor VA ratings				$C:3.4\text{ kVA}$	$C:2.2\text{ kVA}$			
Modulator complexity	low	high	low	low	high	low	low	low
Volt. range limitations	no	no	no	no	no	$V_1 > nV_2$	$V_1 > 2nV_2$	$V_1 > nV_2$
Const. freq. operation	yes	yes	yes	yes	yes	yes	yes	yes
Snubber required	no	no	no	no	no	yes	yes	yes

Table 2.2 cont.: Conv. topologies: capacitors & ancillary information.

Topologies	DAB (Conv. Mod., Section 3.1.2)	DAB (Opt. Mod., Section 5.2.1)	Three-Phase DAB [54]	LLC (Conv. Mod., Appendix A.4.3)	LLC (Opt. Mod., Appendix A.4.4)	Full Bridge Converter + Current Fed Full Bridge	Current Fed Push Pull	
Advantages	<ul style="list-style-type: none"> – lowest comp. count – avoids DC ind. – simple modulation 	<ul style="list-style-type: none"> – lowest comp. count – avoids DC ind. – reduced circ. curr. – reduced cap. RMS currents – HV side switches: full range ZVS – LV side switches: full range ZCS – achievable 	<ul style="list-style-type: none"> – comparatively low capacitor RMS curr. – avoids DC ind. – reduced circ. curr. 	<ul style="list-style-type: none"> – slightly reduced comp. stresses compared to the conv. DAB – avoids DC ind. – simple modulation 	<ul style="list-style-type: none"> – avoids DC ind. – reduced circ. curr. – reduced capacitor RMS curr. – HV side: full range ZVS – LV side switches: full range ZCS – achievable 	<ul style="list-style-type: none"> – LV side DC cap.: low RMS curr. – HV side: full range ZVS 	<ul style="list-style-type: none"> – lowest transf. curr.: low losses in contact resistances (e.g. transf. terminal) – lowest sw. curr.: better MOSFETs available (lower losses) – LV side: no high-side gate drivers – LV DC cap.: low RMS curr. – HV side: full range ZVS 	<ul style="list-style-type: none"> – LV side: no high-side gate drivers – LV side DC cap.: low RMS curr. – HV side: full range ZVS
Disadvantages	<ul style="list-style-type: none"> – limited ZVS range – transf.: large circ. curr. – LV DC capacitor: very large RMS curr. 	<ul style="list-style-type: none"> – LV DC cap.: large RMS curr. – complex modulation 	<ul style="list-style-type: none"> – limited ZVS range – high component count – LV DC capacitor: rather large RMS curr. 	<ul style="list-style-type: none"> – large L & C limited – ZVS range: transf.: large circ. curr. – LV DC capacitor: very large RMS curr. 	<ul style="list-style-type: none"> – rather large L & C – LV DC cap.: large RMS curr. – complex modulation 	<ul style="list-style-type: none"> – large DC ind. required – snubber may be needed – limited operating volt. range – limited operating volt. range 	<ul style="list-style-type: none"> – increased transf. VA rating – large DC ind. required – snubber may be needed – limited operating volt. range – limited operating volt. range 	<ul style="list-style-type: none"> – increased transf. VA rating – large DC ind. required – snubber may be needed – limited operating volt. range – limited operating volt. range

Table 2.2 cont.: Converter topologies: advantages and disadvantages.

The Single-phase Dual Active Bridge (DAB) converter (Figure 2.10) contains two voltage sourced full bridge circuits or half bridge circuits (or even push-pull circuits [72]) and a HF transformer. The reactive network simply consists of an inductor L connected in series to the HF transformer; hence, the DAB directly utilizes the transformer stray inductance. Due to the symmetric circuit structure, the DAB readily allows for bidirectional power transfer.

The main advantage of the DAB are the low number of passive components, the evenly shared currents in the switches, and its soft switching properties.⁴ With the DAB converter topology, high power density is feasible [50, 54].

However, the waveforms of the transformer currents $i_{AC1}(t)$ and $i_{AC2}(t)$ highly depend on the actual operating point (i.e. V_1 , V_2 , and the output power P_{out} ; cf. Chapter 3); for certain operating points, very high transformer RMS currents result. Moreover, high maximum capacitor RMS currents $I_{C_{DC1}}$ and $I_{C_{DC2}}$ occur.

⁴Soft switching denotes low-loss switching processes according to Section 4.3.2. For the DAB, the operating range with soft switching is limited; in particular at low load conditions, soft switching may be lost [50].

<i>Topologies</i>	<i>DAB (Conv. Mod., Chap- ter 3.1.2)</i>	<i>DAB (Opt. Mod., Chap- ter 3.1.3)</i>	<i>Three- Phase DAB [54]</i>	<i>LLC (Conv. Mod., Ap- pendix A.4)</i>	<i>LLC (Opt. Mod., Ap- pendix A.4)</i>
$N_1 : N_2 = n$	19 : 1	17 : 1	20 : 1	20 : 1	17 : 1
L	26.7 μH	21.7 μH	22.2 μH	55.4 μH	38.3 μH
C	–	–	–	93.3 nF	135 nF
L_M	–	–	–	1600 μH	400 μH
Average efficiency (cf. Appendix A.1)	89.5 %	93.7 %	90.9 %	90.0 %	93.9 %
Maximum losses	361 W at $V_1 = 240 \text{ V}$, $V_2 = 11 \text{ V}$, $P_2 = 2 \text{ kW}$, HV→LV	188 W at $V_1 = 240 \text{ V}$, $V_2 = 11 \text{ V}$, $P_2 = 2 \text{ kW}$, HV→LV	283 W at $V_1 = 240 \text{ V}$, $V_2 = 11 \text{ V}$, $P_2 = 2 \text{ kW}$, HV→LV	336 W at $V_1 = 240 \text{ V}$, $V_2 = 16 \text{ V}$, $P_2 = 2 \text{ kW}$, HV→LV	167 W at $V_1 = 450 \text{ V}$, $V_2 = 11 \text{ V}$, $P_2 = 2 \text{ kW}$, LV→HV

Table 2.3: Optimized results for the DAB and the LLC converters (cf. Appendix A).

Particularly high transformer and capacitor RMS currents result if the conventional modulation scheme – the so-called phase shift modulation – is employed. A considerable reduction of these RMS currents is achieved with the use of the efficiency optimized modulation schemes presented in Chapter 5.

According to Table 2.2, comparatively small VA ratings of the LV side switches, a low VA rating of the HF transformer, and a low total value of the magnetic energy storage capability already result for the DAB when operated with the conventional modulation scheme. Moreover, the DAB contains the lowest number of inductors. Expectedly, the total VA ratings and the required magnetic energy storage capability can even be reduced with the use of the efficiency optimal modulation scheme. However, the very large LV side RMS capacitor currents (≤ 244 A or ≤ 125 A, depending on the modulation scheme) present a considerable challenge regarding the practical realization of the DC capacitor C_{DC2} .

The actual DAB employs full bridge circuits on the HV side and on the LV side. Within the regarded DC–AC converter topologies (full bridge, half bridge, and push-pull), the full bridge circuits allow for the best converter utilization due to the following reasons.

- Only the *full bridge* can generate zero output voltage (i.e. the voltage applied to the HF network in Figure 2.7) and therefore enables the use of improved modulation schemes, cf. Chapter 5.
- The advantage of the *half bridge* is the lower amount of required switches (reduced hardware effort regarding gate drivers). For the half bridge, the switch RMS current ratings are twice the RMS current ratings of the switches used for the full bridge. Thus, similar total VA ratings result for the switches of the half bridge and the switches of the full bridge. However, the magnitude of the half bridge AC voltage is half

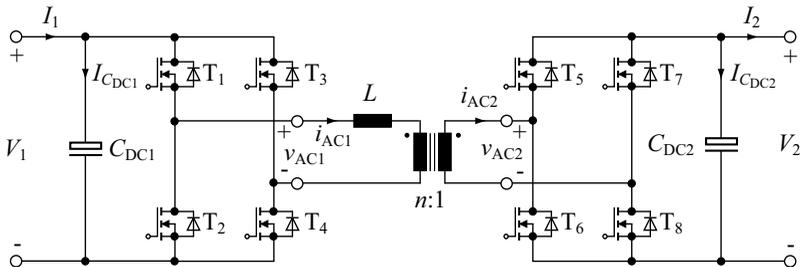


Figure 2.10: Dual Active Bridge (DAB) converter topology.

of the magnitude of the full bridge AC voltage. This presents a serious disadvantage with respect to the LV side circuitry: if a half bridge is employed on the LV side, transformer RMS currents of up to 590 A and switch RMS currents of up to 420 A occur (DAB, phase shift modulation, cf. Table 2.2).

- In order to connect the *push-pull* circuit, two transformer windings are required. Since each winding only conducts current during half a switching period, ineffective HF transformer utilization results (i.e. the transformer VA rating increases). However, the push-pull circuit only requires two low-side switches and thus, the hardware needed for the gate drivers is less complex. The current ratings of the employed switches are the same for the push-pull circuit and the full bridge circuit; the voltage rating of the switches of the push-pull circuits is twice the voltage rating of the switches used for the full bridge. Thus, similar total VA ratings are calculated for the full bridge and for the push-pull circuit. A comparison (full bridge vs. push-pull) is presented in [81].

The Three-Phase DAB (Figure 2.11) uses three half bridges on the HV side and another 3 half bridges on the LV side. It requires 3 converter inductors and 3 HF transformers (which can be consolidated on a single three-phase HF transformer [49, 54]). The three-phase DAB is operated with a modulation scheme similar to the conventional modulation scheme employed for the single-phase DAB (phase shift modulation, [54]). However, different to the single-phase DAB, further performance enhancements using alternative modulation schemes are not feasible for the three-phase DAB.

According to Table 2.2, very good overall performance is achieved with the

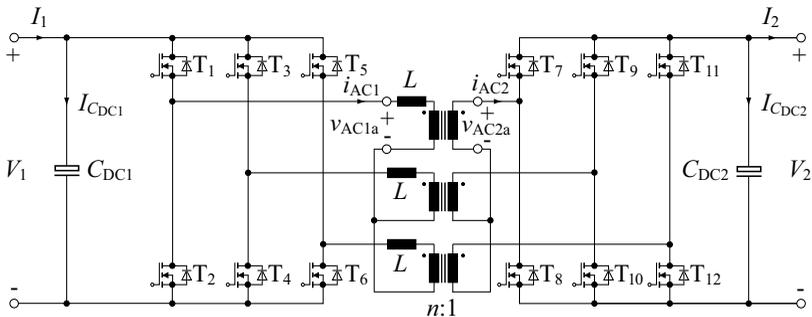


Figure 2.11: Three-phase Dual Active Bridge (DAB) converter topology.

three-phase DAB: a low total transformer VA rating, low switch VA ratings and a low magnetic energy storage capability. In particular, compared to the single-phase DAB, considerably smaller RMS capacitor currents result (66 A vs. 125 A on the LV side, Table 2.2).

A disadvantage of the three-phase DAB is the high number of active components needed: 12 semiconductor switches and, accordingly, 12 gate drivers (6 high-side gate drivers) are required. Moreover, high conduction and switching losses result for certain operating points if the converter is operated within wide voltage and power ranges, due to the restrictions regarding the employed modulation scheme.

The Bidirectional and Isolated Full Bridge Converter (Figure 2.12) contains a voltage sourced full bridge on the HV side and a current sourced full bridge on the LV side (using the DC inductor L_{DC2}). The power flow is typically controlled with the duty cycle D [cf. Figure 2.4 and (2.1)]. Additionally, the LV side full bridge needs to be appropriately controlled in order to allow for bidirectional power flow (e.g. Appendix A.5, [57, 58, 59, 61]). The bidirectional and isolated full bridge converter facilitates ZVS operation of the switches of the HV side; the switches of the LV side switch at zero current. Thus, a high switching frequency and a high power density are feasible (at low power levels, however, additional circuitry is needed; cf. [82, 83]).

Different to the DAB and the LLC converters, usable values for the transformer turns ratio are limited according to (2.2) (i.e. $V_1 > nV_2$; for operation with $V_1 \leq nV_2$, e.g. during system start-up, additional circuitry is required; cf. [55, 56]). Regarding the specifications given in Table 1.4, $n \leq 15$ results; due the additionally required commutation time interval, $n = 12$ is calculated in Appendix A.5 (Table 2.4 lists the design results). For the isolated full bridge converter, the VA ratings of the semiconductor switches – in par-

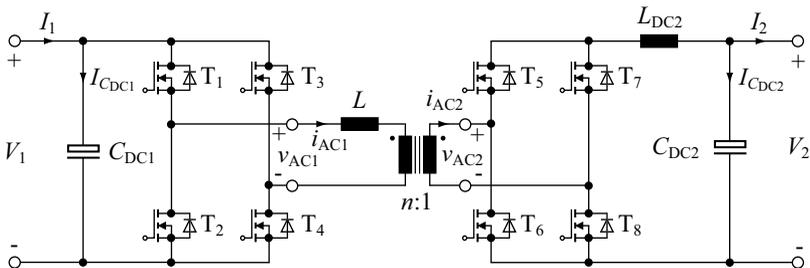


Figure 2.12: Bidirectional and isolated full bridge converter topology.

ticular on the LV side – are considerably higher than the VA ratings obtained for the DAB and the LLC converters (Table 2.2).

The isolated full bridge converter achieves a smooth current $i_{L_{DC2}}(t)$ (cf. Figure A.39) and therefore, compared to the DAB, a considerably lower capacitor RMS current $I_{C_{DC2}}$ results (≈ 16 A for the full bridge converters designed in Appendix A.5). A disadvantage is the additional volume required for the DC inductor. Furthermore, the LV side switches repeatedly connect the DC inductor L_{DC2} in series to the transformer stray inductance L and thus, a snubber circuit is needed in order to avoid voltage spikes when switching.

Instead of the LV side full bridge converter, different AC–DC converter topologies can be used; typical substitutes are the current doubler topology (Figure 2.13) or the push-pull topology (Figure 2.14). The advantages and the disadvantages of the three different AC–DC converters are summarized in the following.

- The switch current ratings and the sum of the switch VA ratings are similar for all three circuits.
- For the *full bridge* circuit, the highest transformer currents $i_{AC2}(t)$ occur (instantaneous and RMS values).
- For the *current doubler* circuit, two inductors are required instead of one. Still, due to partial ripple cancellation, the sum of the magnetic energy storage capabilities (28 mJ) is comparable to that of the DC inductors of the full bridge and the push-pull circuits (21 mJ). However, the AC magnitudes of $i_{L_{DC2a}}(t)$ and $i_{L_{DC2b}}(t)$ are considerably higher for the current doubler (provided that identical design assumptions are used; cf. Figure A.39 and Figure A.42); consequently, an increased transformer VA rating results.

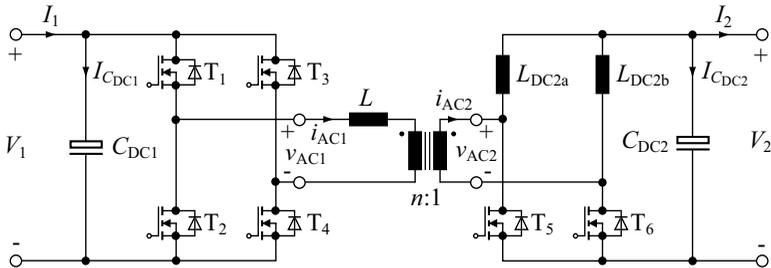


Figure 2.13: Bidirectional and isolated converter with a current doubler on the LV side (side 2).

Compared to the full bridge circuit, twice the transformer voltage $v_{AC2}(t)$ is needed for the current doubler and therefore, lowest transformer currents $i_{AC2}(t)$ are achieved. The current doubler requires two (low-side) switches with a rated voltage of twice the rated voltage of the full bridge switches.

- The *push-pull* circuit connects to a center-tapped transformer with two LV side transformer windings. Thus, each of these windings conducts current only during half a switching period and, consequently, ineffective transformer utilization and a higher VA rating occur (Table 2.2). For the push-pull circuit, two (low side) switches with a rated voltage equal to twice the rated voltage of the full bridge switches are required.

Other Converter Topologies without Resonant HF Network.

In [68], a DC–DC converter with minimum number of devices is discussed. It consists of a voltage sourced half bridge on the HV side and a modified voltage sourced half bridge on the LV side (Figure 2.15). Thus, the converter is a DAB converter with the LV side half bridge being additionally used as a bidirectional buck or boost converter (depending on the direction of power transfer). The transferred power is controlled with the phase shift between $v_{AC1}(t)$ and $v_{AC2}(t)$ (cf. conventional DAB converter).

With this converter, unequal RMS switch currents and higher maximum blocking voltages result for T_3 and T_4 (e.g. $2 \cdot V_{2,\max}$ for converter operation according to [68]). Additionally, the LV side capacitors are exposed to high RMS currents, similar to the DAB. Due to the employed half bridge circuits,

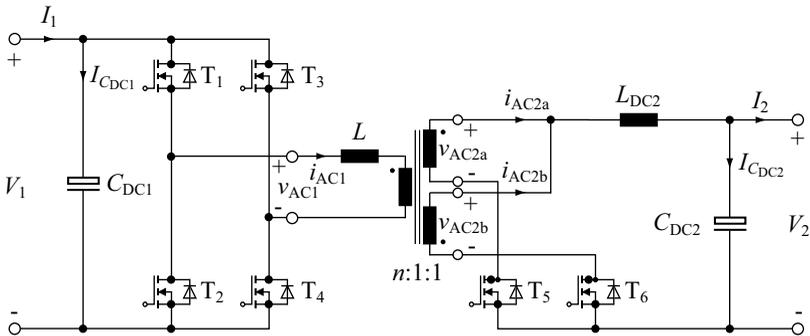


Figure 2.14: Bidirectional and isolated converter with a push-pull circuit on the LV side (side 2).

<i>Topologies</i>	<i>Full Bridge Converter</i>		
	<i>Current Fed Full Bridge</i>	<i>Current Doubler</i>	<i>Current Fed Push-Pull</i>
$N_1 : N_2 = n$	12 : 1	12 : 2	12 : 1
L (HV side referred)	6.4 μH	6.1 μH	6.4 μH
$L_{\text{DC}2}$ (LV side)	0.83 μH	–	0.83 μH
$L_{\text{DC}2\text{a}}$ and $L_{\text{DC}2\text{b}}$ (LV side)	–	1.65 μH	–

Table 2.4: Calculated component values for the isolated full bridge converter topologies.

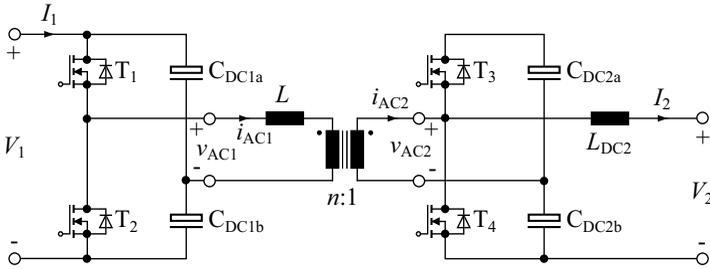


Figure 2.15: Bidirectional DC–DC converter with minimum number of devices [68].

no optimized modulation schemes – like the efficiency optimal modulation scheme for the DAB – can be applied to the isolation stage of the given converter. However, asymmetrical PWM waveforms may be generated in order to adjust V_2 ,⁵ which allows for a certain converter optimization. Still, the complex interaction of the DAB and the buck/boost stage, a limited soft switching range, high capacitor RMS currents and the additionally required DC inductor render this topology less suitable for the given application.

In a different approach, a voltage sourced half bridge circuit is used on the HV side and a current doubler circuit on the LV side [69]; an asymmetrical PWM modulation scheme is proposed to enable the control of the transferred

⁵The capacitors $C_{\text{DC}1\text{a}}$, $C_{\text{DC}1\text{b}}$, $C_{\text{DC}2\text{a}}$, and $C_{\text{DC}2\text{b}}$ keep the resulting DC component away from the HF transformer.

power. Consequently, uneven RMS currents occur in the LV side switches and in the LV side DC inductors. With this, comparably high current stresses result for all power components.⁶

Dual Bridge Converters with Resonant Network

Even though, resonant DC–DC converters with unidirectional power flow are thoroughly described in literature, only very few is found on bidirectional resonant converters. Reasons might be the higher converter complexity and the additional HF components needed. This section briefly summarizes advantages and disadvantages of the most common resonant DC–DC converters and discusses the extensions required to achieve bidirectional converter operation.

Series Resonant, Parallel Resonant, and Series-Parallel Resonant DC–DC Converters with unidirectional power flow belong to the most popular resonant converter topologies [35, 43, 84, 85]. With these converters, nearly sinusoidal waveforms of the transformer currents result. Thus, low switching losses are feasible, which facilitates the use of a high switching frequency to obtain a high power density of the converter [43]. The conventional resonant DC–DC converters are operated with variable switching frequency, i.e. the actual switching frequency depends on the supply voltage and on the load.

The main advantages and disadvantages of the most common unidirectional, resonant DC–DC converters are summarized in the following (according to [35]).

- The *Series Resonant Converter (SRC)* contains a capacitor in series to the transformer stray inductance, which acts like a DC blocking capacitor and prevents saturation of the HF transformer. Furthermore, the RMS currents in the switches and in the resonant network decrease with decreasing load. The main disadvantages of the SRC are related to wide operating voltage and power ranges, since the actual switching frequency strongly varies in dependence on the employed supply voltage and on the load; even more, the SRC cannot be regulated in case of no load (requires infinite switching frequency). The voltage-sourced output (e.g. LV side) is as well disadvantageous with respect to high RMS capacitor currents for applications with low output voltages.

⁶The converter presented in [69] is obviously not designed for operation within the voltage ranges specified in [69]; with respect to these voltage ranges, a transformer turns ratio of $n < 2.5$ would be needed, which would considerably decrease the converter efficiency and the achievable power density; with respect to the voltage ranges specified in Table 1.4, $n < 3.75$ results.

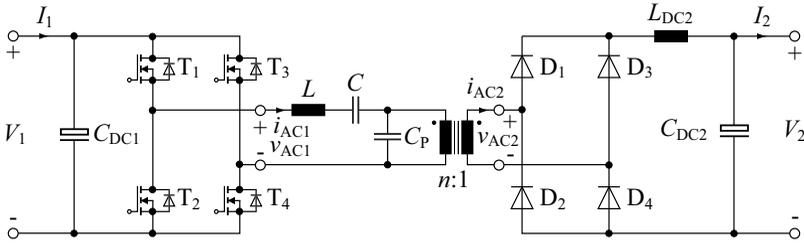


Figure 2.16: Unidirectional, series-parallel resonant *LCC* converter [35].

- The advantage of the *Parallel Resonant Converter (PRC)* is its ability to control the output voltage at no load. Additionally, with the employed output DC inductor, the PRC is better suited for applications with low output voltages and high output currents than the SRC is. However, for the PRC, the currents through the switches and through the resonant network do not substantially decrease with decreasing load. Thus, this converter is less suited for applications with large operating voltage and power ranges or for applications where the converter is most often operated considerably below its rated power.
- With the *Series-Parallel Resonant Converter (SPRC)*, the output voltage can be controlled at no load and the range of the required switching frequency is smaller than for the SRC. Still, compared to the PRC, considerably lower switch and transformer RMS currents are achieved at low load conditions.

The HF network of the SPRC may either consist of one inductor and two capacitors according to the circuit discussed in [35] (often called *LCC* converter, Figure 2.16) or of two inductors and one capacitor (*LLC* converter, Figure 2.17, [86]).

With a circuit modification according to Section 2.1, bidirectional power transfer can be achieved. For the resulting resonant DC–DC converters with two voltage sourced ports (i.e. the bidirectional SRC and the bidirectional LLC converter, Figure 2.18), no restrictions regarding the converter control emerge. In contrast, for the PRC and for the LLC converters (Figure 2.19 (a)), difficulties arise with respect to the LV side full bridge. Due to the inductor L_{DC2} and the capacitor C_P , only 4 different switching states are allowed on the LV side:

- T_5, T_6 : on; T_7, T_8 : off;

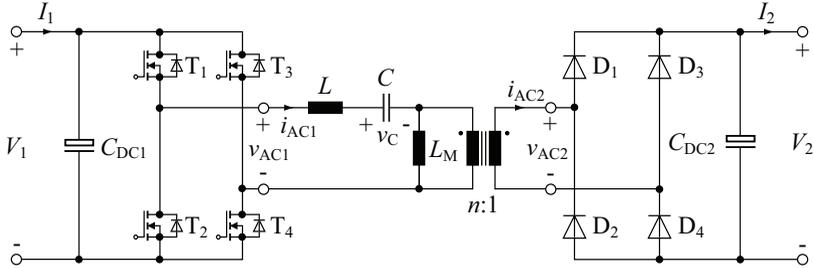


Figure 2.17: Unidirectional, series-parallel resonant *LLC* converter (cf. [86]).

- T_7, T_8 : on; T_5, T_6 : off;
- T_5, T_8 : on; T_6, T_7 : off;
- T_6, T_7 : on; T_5, T_8 : off.

All other switching states are forbidden, since they would either interrupt the inductor current $I_{L_{DC2}}$ (e.g. T_5, T_6, T_7 , and T_8 are turned off, for $I_{L_{DC2}} < 0$), cause a short circuit on C_P (e.g. T_5, T_6, T_7 , and T_8 : on), or both (e.g. T_6, T_8 : on; T_5, T_7 : off)—in particular during a state change of the LV side full bridge, it is very likely for the actual converter hardware to switch into one of the forbidden states for a short time. This issue can be overcome with the use of 4-quadrant switches on the LV side, according to Figure 2.19 (b), and an appropriate modulation scheme. The additional hardware effort, however, renders the PRC and the LCC converter topologies less attractive than the SRC and the LCC converters and thus, the bidirectional PRC and the bidirectional LCC converters are not considered any further.

The SRC can be considered as a special case of the LLC converter, therefore the presented discussion is confined to the bidirectional LLC converter. Due to the series capacitor, C , approximately sinusoidal transformer currents i_{AC1} and i_{AC2} are obtained (in contrast to the DAB, where triangular or trapezoidal currents occur); the parallel inductor L_M increases the reactive power generated with the HF network (L_M can be advantageously used to reduce the switching losses on the HV side and on the LV side). Compared to the DAB, reduced RMS transformer currents and reduced switching losses can be achieved with the LLC converter, especially with respect to the operation within wide input and output voltage ranges.

For the LLC converter, full bridge circuits are used on the HV side and on the LV side due to the same reasons as mentioned for the DAB above.

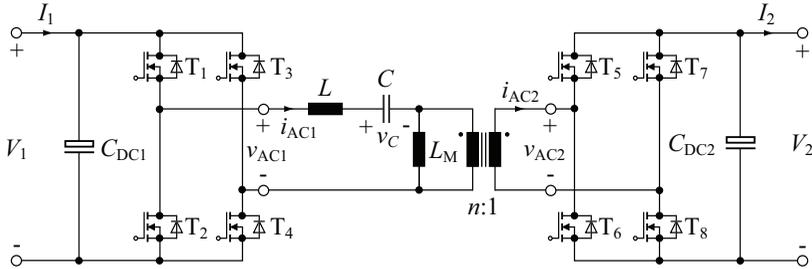


Figure 2.18: Bidirectional, series-parallel resonant *LLC* converter with two voltage sourced ports; for the depicted converter topology, no restrictions regarding the control of the converter apply.

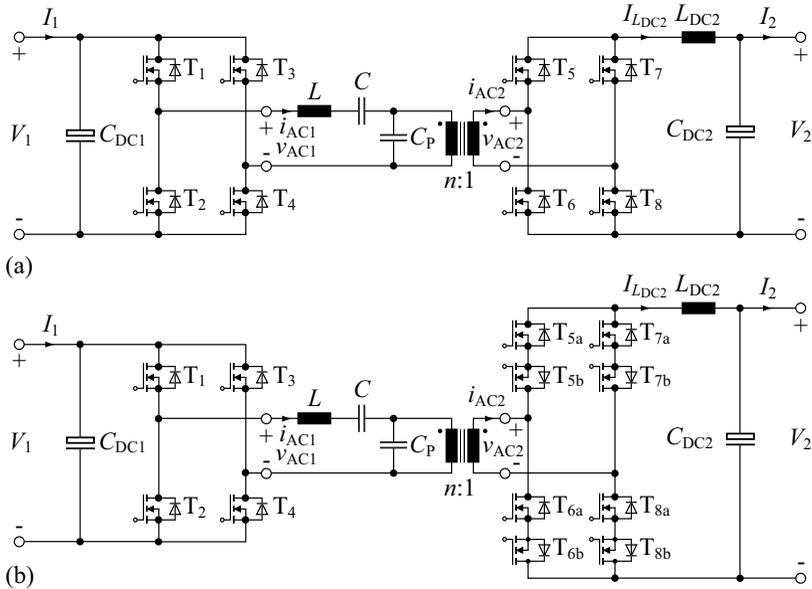


Figure 2.19: Bidirectional, series-parallel resonant *LCC* converter: (a) with 2-quadrant switches T_5 , T_6 , T_7 , and T_8 , the full bridge on the LV side (side 2) may reside in forbidden states, which cause a short circuit of C_P and/or an interruption of $I_{L_{DC2}}$; (b) with the LV side full bridge being equipped with 4-quadrant switches, the aforementioned forbidden states can be avoided.

The converter performance is analyzed using two different modulation schemes, which both allow for fixed frequency operation:

- The conventional modulation scheme operates the two full bridges with maximum duty cycle in order to generate purely rectangular voltages v_{AC1} and v_{AC2} . The power transfer is controlled with the phase angle φ between v_{AC1} and v_{AC2} , identical to the conventional operation of the DAB converter (Appendix A.4.3).
- The efficiency optimal modulation scheme utilizes the ability of the full bridges to generate zero output voltage (i.e. $v_{AC1} = 0$ or $v_{AC2} = 0$) in order to further reduce the transformer RMS currents and to achieve lower switching losses. The modulation parameters (D_1 , D_2 , and φ) with respect to maximum converter efficiency are obtained in the same way as for the DAB converter (Section 5.2.1, Appendix A.4.4).

The component values for the LLC converter (L , C , L_M , and n) have been optimized with respect to maximum average efficiency (Appendix A.1), the given converter specifications (Table 1.4) and for both modulation schemes.

If the LLC converter is operated with the conventional modulation scheme, the VA ratings for the HF transformer and the switches are slightly below the VA ratings obtained for the conventional DAB converter. However, an inductor L with a higher maximum energy storage capability is required (14.9 mJ for the LLC converter and 11.2 mJ for the DAB converter) and a series capacitor C is needed (the parallel inductor L_M can be neglected, since the optimization results in a very large value for L_M).

A better utilization of the LLC converter is achieved if the employed modulation parameters are optimized with respect to maximum converter efficiency. With this method, low VA ratings are obtained for the HF transformer (4.2 kVA) and for all switches (HV side: 17.6 kVA, LV side: 10.5 kVA, cf. Table 2.2). Among the considered DC–DC converters with two voltage sourced ports, the best average efficiency is achieved for the LLC converter (Table 2.3).

The LLC converter could as well be operated with a DC inductor on the LV side. The respective circuit is depicted in Figure 2.20 and is derived from the bidirectional, isolated full bridge converter. Similar to the isolated full bridge converter, this LLC converter repeatedly switches L and L_M in series to L_{DC2} , which causes voltage spikes on $v_{AC2}(t)$; a snubber circuit is needed to reduce these voltage spikes. Moreover, compared to the bidirectional full bridge converters, a considerably higher transformer VA rating is expected due to the increase of the reactive power in the high frequency network (in particular with respect to the required input and output voltage ranges and the required constant switching frequency operation, Table 1.4). Taking the additionally required power components C and L_M into account, the LLC

converter with DC inductor is considered to be less attractive than the bidirectional full bridge converter and is thus not investigated.

Other resonant DC–DC converters. Different to the SRC, PRC, and SPRC converter topologies, a bidirectional converter topology with switched resonance frequency is discussed in [75, 76] (Figure 2.21). The converter contains a voltage sourced half bridge on the HV side, a voltage sourced full bridge on the LV side, and a 4-quadrant switch to change the effective resonance capacitor.

With this configuration, high efficiency has been demonstrated for a wide load range.⁷ However, the LV port voltage V_2 of the proposed converter cannot exceed V_1/n [i.e. the constraint (2.2) applies]. Moreover, with the use of alternative modulation schemes, similar transformer currents (waveforms and RMS values) can be achieved with the LLC converter (Figure 2.18). In summary, a higher total VA rating is expected to result for the converter depicted in Figure 2.21 than for the LLC converter (in particular due to the additionally required 4-quadrant switch) and thus, a higher power density is expected to be achieved with the LLC converter.

In another approach, the capacitance values of C_{DC1} and C_{DC2} of the DAB converter are considerably reduced in order to form a resonant converter which allows for low switching losses. Therefore, however, additional EMI filter components are necessarily required, since the EMI filters become part of the HF resonant network [77]. The oscillation frequency of the currents in the filter capacitors is twice the switching frequency and, additionally, very low currents are desired at the switching instants at $t \approx k \cdot T_S/2$. Based on the switch current depicted in Fig. 11(b) in [77], the transformer current i_{AC1} can be

⁷In [75, 76] the switching frequency is reduced at low load conditions.

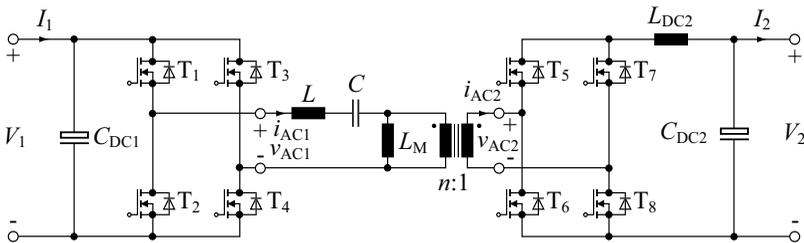


Figure 2.20: Bidirectional, series-parallel resonant *LLC* converter with a current sourced LV port.

approximated with

$$i_{AC1}(t) = \begin{cases} (I_{AC1,peak}/2) \cdot [1 - \cos(2 \cdot 2\pi f_s t)] & \forall \quad 0 \leq t < 1/(2f_s) \\ -(I_{AC1,peak}/2) \cdot [1 - \cos(2 \cdot 2\pi f_s t)] & \forall \quad 1/(2f_s) \leq t < 1/(f_s) \end{cases} \quad (2.7)$$

[$I_{AC1,peak}$ is the amplitude of $i_{AC1}(t)$]. Accordingly, the RMS value $I_{AC1} = I_{AC1,peak} \cdot \sqrt{3/8}$ and the rectified average value $\overline{|I_{AC1}|} = I_{AC1,peak}/2$ result. Compared to a purely rectangular transformer current $i_{AC1,rect}(t)$ (there, $I_{AC1,rect}/\overline{|I_{AC1,rect}|}$ is equal to 1), the conduction losses in the HF transformer and in the semiconductor switches will increase by a factor of $(I_{AC1}/\overline{|I_{AC1}|})^2 = 1.5$ due to the employed transformer current waveform.⁸

The converter with resonating filter capacitors is optimized with respect to low switching losses [77], however, comparably high conduction losses occur. Moreover, on the LV side, the resonating capacitors are exposed to very high RMS currents and therefore difficult to implement. This renders the topology less suitable with respect to the considered application.

2.2.2 Two-Stage Topologies

The isolated DC–DC converter topologies discussed in Section 2.2.1 are operated most efficiently if the input to output voltage ratio V_1/V_2 is close to the transformer turns ratio n . Thus, within the specified input and output voltage ranges, a more evenly distributed converter efficiency is expected for a two-stage solution which employs an additional buck and / or boost converter

⁸For a triangular current $(I_{AC1}/\overline{|I_{AC1}|})^2$ is equal to 1.33 (e.g. DAB HF transformer current at certain operating points, cf. Section 3.1.3) and for a sinusoidal current $(I_{AC1}/\overline{|I_{AC1}|})^2 = 1.23$ (e.g. achieved for the LLC converter at certain operating points).

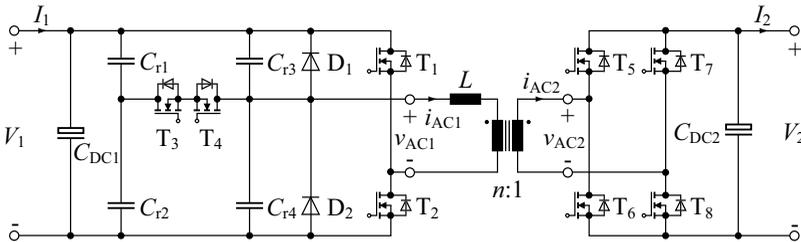


Figure 2.21: Bidirectional, resonant converter with switched resonance frequency [75, 76].

without galvanic isolation to adjust the voltage applied to the isolated DC–DC converter stage. However, the total number of required power components is higher for the two-stage converter. Thus, the additional DC–DC converter needs to be highly efficient in order to achieve a higher efficiency with the two-stage converter than with the respective single-stage converter.

In this thesis, a bidirectional buck or boost converter, which allows for buck operation in one power transfer direction and boost operation in the opposite direction, provides the converter stage without galvanic isolation. With this, the 4 different arrangements depicted in Figure 2.22 are feasible:⁹

- *HV side buck converter* [Figure 2.22 (a)]: with this arrangement, the given specifications, and a maximum duty cycle $D_{\text{buck,max}} = 95\%$ of the buck converter, the DC link voltage V_i approximately remains within the voltage range $150 \text{ V} \leq V_i \leq 225 \text{ V}$ and enables efficient operation of the isolated DC–DC converter stage at (or close to) $V_i/V_2 = n$ within the whole specified operation range (cf. Chapter 5). Due to the reduced DC link voltage V_i , MOSFETs with a maximum voltage rating of 300 V can be employed for the HV side DC–AC converter of the isolated converter stage (cf. Figure 2.7), however, a comparably high maximum port current $\max(I_i) \approx 15 \text{ A}$ results (for the assumption of 90% efficiency).
- With a *HV side boost converter* [Figure 2.22 (b)], the DC link voltage is larger than the HV port voltage. For the assumption of a minimum duty cycle $D_{\text{boost,min}} = 5\%$ of the boost converter, the DC link voltage range is $475 \text{ V} \leq V_i \leq 700 \text{ V}$ in order to enable efficient operation of the isolated DC–DC converter stage (i.e. $V_i/V_2 \approx n$). This exceeds the maximum voltage rating of the employed MOSFETs ($V_{(\text{BR})\text{DSS}} = 600 \text{ V}$). However, only for $V_{(\text{BR})\text{DSS}} \approx 600 \text{ V}$ highly optimized MOSFETs are available (Appendix D.1.2); Section 7 therefore presents a trade-off study on how to efficiently operate the isolated DC–DC converter stage and still reduce the maximum DC link voltage to $\max(V_i) = 475 \text{ V}$.
- The configuration with the *LV side buck converter* [Figure 2.22 (c)] allows for reduced currents in the LV side DC–AC converter (e.g. full bridge) of the isolated converter stage. However, the realization of a highly efficient low voltage and high current buck converter (e.g. 32 V and 200 A) is considerably more difficult than the realization of a 450 V and 15 A buck converter (cf. [25, 89]).

⁹A bidirectional buck and boost converter (allows for buck and boost operation in either direction [87, 88]) could be employed to achieve a more flexible converter topology. However, the 4 power switches required for the bidirectional buck and boost converter are considered as a disadvantage with respect to the converter cost and the achievable power density.

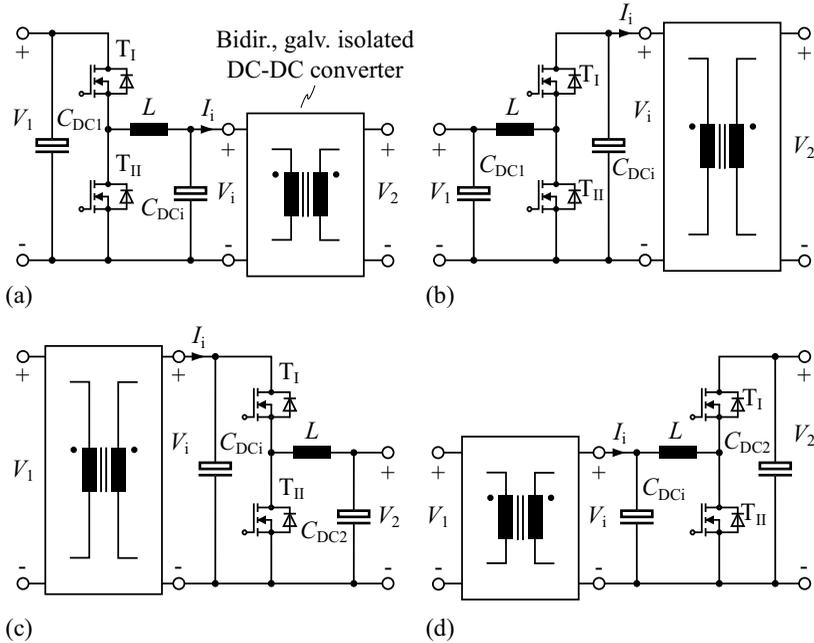


Figure 2.22: Four different arrangements of a bidirectional buck or boost converter and a single-stage isolated bidirectional DC–DC converter: (a) HV side buck converter, (b) HV side boost converter, (c) LV side buck converter, and (d) LV side boost converter.

- The *LV side boost converter* [Figure 2.22 (d)] requires the DC link voltage to be lower than the LV port voltage, $V_i < V_2$ which leads to increased currents in the LV side switches and in the HF transformer. This arrangement is thus less suitable with respect to high converter efficiency.

2.3 Conclusion

The advantages and the disadvantages of the considered single-stage, bidirectional, and isolated DC–DC converter topologies are summarized in the following.

- *DAB converter:* the DAB converter topology (Figure 2.10) contains only

one inductor, L , with a comparably low peak energy storage capability (6.2 mJ on the assumption of efficiency optimal modulation parameters, Table 2.2); it features low VA ratings of the semiconductor switches (HV side: 17.3 kVA, LV side: 10.5 kVA), ZVS operation (within certain limits, cf. [50,90,91]), and is highly flexible regarding the employed modulation scheme (cf. Section 3.1.3). The DAB converter enables power transfer for $V_1 \geq n V_2$ and for $V_1 \leq n V_2$ (n is the transformer turns ratio). Due to its symmetric circuit structure, the converter efficiency characteristics is independent of the actual power transfer direction.¹⁰ Disadvantages of the DAB converter are: the high maximum value of the RMS current through C_{DC2} (125 A), the high maximum transformer RMS current through the LV side winding (231 A), and the high complexity of the modulation algorithm required to generate the gate signals for the switches.

- *Three-phase DAB converter*: the three-phase DAB converter (Figure 2.11) features a low total value of the required peak magnetic energy storage capability ($3 \cdot 2.23 \text{ mJ} = 6.7 \text{ mJ}$), ZVS operation (within a limited operating range [54]), reduced capacitor RMS currents (66 A through C_{DC2}), and a symmetric circuit structure; the three-phase DAB converter can be operated with $V_1 \geq n V_2$ and with $V_1 \leq n V_2$. However, the system requires a high number of components (3 transformers, 3 inductors, and 12 switches). Moreover, the expected average efficiency, calculated according to Appendix A.1 ($\bar{\eta} = 90.9\%$), is less than the average efficiencies calculated for the single-phase DAB converter ($\bar{\eta} = 93.7\%$) and the LLC converter ($\bar{\eta} = 93.9\%$).
- *LLC converter*: compared to the DAB converter, a slightly higher average efficiency is calculated for the LLC converter (Figure 2.18); the semiconductor's VA ratings are similar (HV side: 17.6 kVA, LV side: 10.5 kVA). However, a larger value of the required magnetic storage capability occurs (9.4 mJ + 0.6 mJ) and an additional resonance capacitor, C , is needed for the resonant circuit (peak energy: 3.6 mJ). Thus, the resonant circuit of the LLC converter requires a larger volume than the inductor of the DAB converter (cf. [74]). Again, a large RMS current through C_{DC2} is calculated (122 A).

In contrast to the DAB converter, the electric energy stored in the resonance capacitor C forces the transformer current to change during the freewheeling time interval (i.e. for $v_{AC1} = v_{AC2} = 0$, cf. Figure 3.7), which causes the transformer RMS current to increase. Thus, for converter operation according to Appendix A.4 (i.e. continuous conduction

¹⁰Provided that parasitic effects, e.g. the impact of switching losses on the transformer current, are negligible; cf. Section 4.6.2.

mode operation), the LLC converter is more suitable if a variable switching frequency is permitted.

- *Full bridge converters with one or more DC inductors on the LV side*: all full bridge converters considered in Table 2.2 (Figure 2.12, Figure 2.13, and Figure 2.14) feature ZVS operation of the HV side semiconductors (at low power levels, additional circuitry is needed, cf. [82, 83]) and a low RMS current through C_{DC2} (≈ 10 A); moreover, the required gate signals can be generated in a straightforward manner (Appendix A.5). However, the energy storage capabilities of the DC inductors required for the full bridge converters are comparably large (21 mJ for the current fed full bridge and the push pull circuit; $2 \cdot 14$ mJ for the current doubler). For the semiconductor switches, high VA ratings result (HV side: ≈ 26 kVA, LV side: ≈ 24 kVA). Moreover, the operating voltages are limited according to (2.2), i.e. $V_1 > nV_2$. For operation with $V_1 \leq nV_2$, e.g. during system start-up, additional circuitry is required (cf. [55, 56]).

For all considered single-stage converter topologies, similar VA ratings are calculated for the HF transformers and thus, similar transformer volumes result [92].

Based on these findings, the single-phase DAB converter topology is considered most promising with respect to the achievable converter efficiency (cf. Table 2.3) and the achievable power density (due to the low number of inductors and due to the employed capacitive filters on the HV side and on the LV side [39], i.e. the DC capacitor C_{DC2} is used instead of the DC inductor L_{DC2}). Therefore, the DAB is investigated in detail in the following Chapters, where Chapter 3 describes the working principles of the DAB; Chapter 4 presents a loss model for the DAB, needed to develop the efficiency optimized modulation schemes presented in Chapter 5; in Chapter 6, a detailed small-signal control-oriented model of the DAB converter is presented, which characterizes the dynamic converter properties.

Due to the wide input and output voltage ranges, all isolated single-stage DC–DC converters listed above could be used in a two-stage arrangement according to Figure 2.22 in order to achieve a more efficient converter operation.

- The efficiencies obtained with the *single-phase DAB converter*, the *three-phase DAB converter*, and the *LLC converter* are very sensitive on the ratio of the input to output voltage: for $V_1/V_2 \ll n$ or $V_1/V_2 \gg n$, large transformer RMS currents occur (cf. Figure 3.6 and Figure 3.21 for $V_1 = 450$ V and $V_2 = 11$ V) and thus, large conduction losses result; this can be avoided in a two-stage arrangement which keeps the input voltage of the isolated DC–DC converter, V_i , close to nV_2 .
- For the isolated full bridge converters with one or two DC inductors, the peak voltage applied to the semiconductor switches of the LV side full

bridge can be reduced if a two-stage arrangement is used; consequently, MOSFETs with a lower on-state resistance can be used. Moreover, the VA ratings of the switches of the HV side full bridge, T_1 , T_2 , T_3 , and T_4 in Figure 2.12, become smaller.

In order to compare the efficiencies achieved with the two-stage topologies to the efficiencies achieved with the single-stage DAB converter, i.e. the two most promising converter configurations, the arrangements depicted in Figure 2.22 (a) and Figure 2.22 (b) are investigated in Chapter 7; there, the isolated DC–DC converter comprises of a DAB converter. As a result, it turns out that the average efficiency achieved with the two-stage converter ($\bar{\eta} = 93.0\%$) is less than the average efficiency achieved with the single-stage DAB ($\bar{\eta} = 93.5\%$),¹¹ i.e. in average, the additional losses of the buck-or-boost converter are higher than the loss reduction achieved for the DAB converter.

¹¹The respective average efficiencies, $\bar{\eta}$, are calculated according to Appendix A.1; the calculations assume the suboptimal modulation schemes to be used for the DAB, cf. Section 5.2.2.

Chapter 3

Steady-State Operation of the Dual Active Bridge (DAB)

3.1 Lossless DAB Model

In Section 2.3, the DAB converter topology is regarded most promising with respect to the achievable converter efficiency and with respect to a low converter volume. The DAB converter contains two voltage sourced full bridge circuits (cf. Section 2.2.1) that are connected to the inductor L and the high frequency transformer (Figure 3.1). In order to transfer power, time varying voltages $v_{AC1}(t)$ and $v_{AC2}(t)$ must be provided by the full bridge circuits to

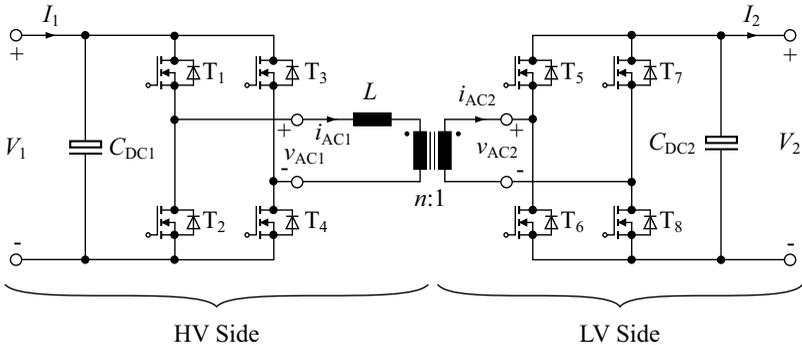


Figure 3.1: Dual Active Bridge (DAB) converter topology.

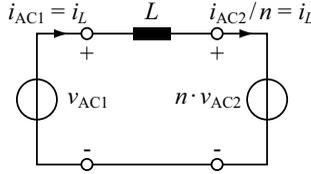


Figure 3.2: Lossless DAB model.

both, the high frequency transformer and the converter inductor L . Thus, the voltage sourced HV and LV side full bridge circuits can be replaced by the respective voltage sources v_{AC1} and v_{AC2} to simplify the analysis of the DAB converter; for the most simple electric DAB converter model

1. all losses are neglected,
2. the transformer magnetizing inductance and parasitic capacitances (e.g. transformer coupling capacitance between LV and HV sides) are neglected,
3. all LV side quantities are referred to the HV side, and
4. constant supply voltages V_1 and V_2 are considered.

The resulting lossless DAB model is depicted in Figure 3.2.

3.1.1 DAB Inductor Current and Power Transfer

With the HV side full bridge, three different voltage levels are possible for $v_{AC1}(t)$,

$$v_{AC1}(t) = \begin{cases} +V_1 & \text{for state I: } T_1, T_4 \text{ on, } T_2, T_3 \text{ off} \\ 0 & \text{for state II: } T_1, T_3 \text{ on, } T_2, T_4 \text{ off or} \\ & \text{for state III: } T_2, T_4 \text{ on, } T_1, T_3 \text{ off} \\ -V_1 & \text{for state IV: } T_2, T_3 \text{ on, } T_1, T_4 \text{ off} \end{cases} \quad (3.1)$$

(on the assumption of an ideal full bridge, i.e. switching transients are not considered). Similarly, $v_{AC2}(t)$ is equal to V_2 , 0, or $-V_2$ depending on the switching states of T_5 , T_6 , T_7 , and T_8 . The resulting voltage $v_R(t)$,

$$v_R(t) = v_{AC1}(t) - n v_{AC2}(t), \quad (3.2)$$

applied to the inductor of the simple DAB model (Figure 3.2), generates the current

$$i_L(t_1) = i_L(t_0) + \frac{1}{L} \int_{t_0}^{t_1} v_R dt \quad \forall \quad t_0 < t_1, \quad (3.3)$$

at the time t_1 , starting with an initial current $i_L(t_0)$ at time t_0 . The voltage sources v_{AC1} and v_{AC2} thus generate or receive the respective instantaneous powers

$$p_1(t) = v_{AC1}(t) \cdot i_L(t) \quad \text{and} \quad p_2(t) = n v_{AC2}(t) \cdot i_L(t). \quad (3.4)$$

In order to simplify the calculation of (3.3), it is reasonable to select t_0 and t_1 such that $v_{AC1}(t)$ and $v_{AC2}(t)$ are constant during the time interval $t_0 < t < t_1$.

The average power over one switching cycle T_S , $T_S = 1/f_S$, is finally calculated with

$$P_1 = \frac{1}{T_S} \int_{t_0}^{t_0+T_S} p_1(t) dt \quad (3.5)$$

for the HV side and

$$P_2 = \frac{1}{T_S} \int_{t_0}^{t_0+T_S} p_2(t) dt \quad (3.6)$$

for the LV side. Therefore, one switching period, $t_0 < t < t_0 + T_S$, is split up into m time intervals (numbered with the index counter i) with constant voltages $v_{AC1}(t)$ and $v_{AC2}(t)$,

$$\begin{aligned} \text{time interval I } (i = 1): & \quad t_0 < t < t_1, \\ \text{time interval II } (i = 2): & \quad t_1 < t < t_2, \\ & \quad \vdots \\ \text{final time interval } (i = m): & \quad t_{m-1} < t < t_m = t_0 + T_S. \end{aligned} \quad (3.7)$$

According to (3.4), (3.5), and (3.6) the waveforms $v_{AC1}(t)$ and $i_L(t)$ determine P_1 and the waveforms $v_{AC2}(t)$ and $i_L(t)$ determine P_2 ; further,

$$P_1 = P_2 \quad (3.8)$$

applies, since the considered DAB model is lossless. The power level of the DAB converter is thus typically adjusted using one or more out of the 4 control parameters depicted in Figure 3.3:

- the phase shift, φ , between $v_{AC1}(t)$ and $v_{AC2}(t)$ with $-\pi < \varphi < \pi$,
- the duty cycle, D_1 , of $v_{AC1}(t)$ with $0 < D_1 < 1/2$,
- the duty cycle, D_2 , of $v_{AC2}(t)$ with $0 < D_2 < 1/2$, and
- the switching frequency f_S .

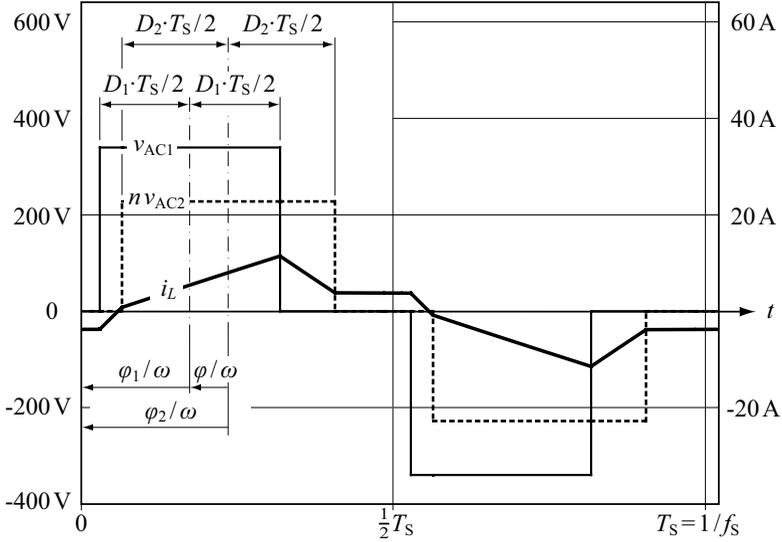


Figure 3.3: The 4 DAB control parameters: $\varphi = \varphi_2 - \varphi_1$ denotes the phase shift between v_{AC1} and v_{AC2} , D_1 and D_2 are the respective duty cycles, and f_s is the switching frequency.

It is important to note, that the average values of $v_{AC1}(t)$ and $v_{AC2}(t)$, evaluated over one switching period in steady-state converter operation, are zero (i.e. the DC components of $v_{AC1}(t)$ and $v_{AC2}(t)$ are zero) in order to avoid saturation of the high frequency transformer.

3.1.2 Phase Shift Modulation

The most common modulation principle, the so called phase shift modulation, operates the DAB with a constant switching frequency and with maximum duty cycles, $D_1 = D_2 = 1/2$; it solely varies the phase shift φ in order to control the transferred power. Hence, $v_{AC1}(t)$ is either $-V_1$ or $+V_1$ and $v_{AC2}(t)$ is either $-V_2$ or $+V_2$ (Figure 3.4). During steady-state operation, the voltages $v_{AC1}(t)$ and $v_{AC2}(t)$ and the inductor current repeat every half-cycle with reversed signs,

$$\begin{aligned} v_{AC1}(t + T_s/2) &= -v_{AC1}(t), \\ v_{AC2}(t + T_s/2) &= -v_{AC2}(t), \text{ and} \\ i_L(t + T_s/2) &= -i_L(t), \end{aligned} \quad (3.9)$$

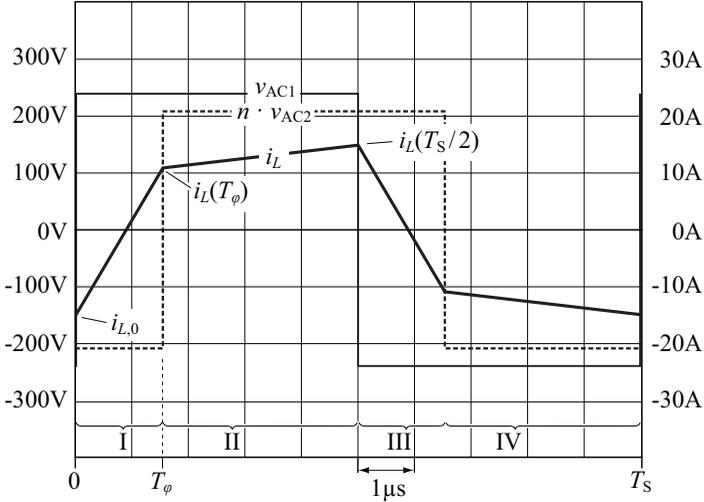


Figure 3.4: Transformer voltages and inductor current for phase shift modulation, $V_1 = 240$ V, $V_2 = 11$ V, and $P_2 = 2$ kW (LV port output power); the converter is designed according to Appendix A.2 with $n = 19$ and $L = 26.7$ μ H.

since the phase shift time T_φ and the DC supply voltages V_1 and V_2 remain the same during the first and during the second half-cycle (time intervals I, II and III, IV in Figure 3.4, respectively). For the calculation of the transferred power, therefore, only the first half-cycle (intervals I and II) needs to be considered. With $t_0 = 0$, (3.5) we have

$$P_1 = \frac{1}{T_s} \int_0^{T_s} p_1(t) dt = \frac{2}{T_s} \int_0^{T_s/2} v_{AC1}(t) \cdot i_L(t) dt = \frac{2V_1}{T_s} \int_0^{T_s/2} i_L(t) dt; \quad (3.10)$$

thus, in order to obtain an analytical expression for P_1 , the current $i_L(t)$ needs to be determined. In steady-state operation, a certain current $i_{L,0} = i_L(t_0)$ is presumed. The two different time intervals I and II occur during $0 < t < T_s/2$ (Figure 3.4). On the assumption of a positive phase shift, $0 < \varphi < \pi$, the resulting expressions for the inductor current are:

$$\begin{aligned} \text{time interval I: } i_L(t) &= i_{L,0} + (V_1 + nV_2)t/L & \forall \quad 0 < t < T_\varphi, \\ \text{time interval II: } i_L(t) &= i_L(T_\varphi) + (V_1 - nV_2)(t - t_1)/L & \forall \quad T_\varphi < t < T_s/2. \end{aligned} \quad (3.11)$$

Due to the half-cycle symmetry (3.9) and with $T_\varphi = \varphi/(2\pi f_S)$,

$$i_{L,0} = \frac{\pi \cdot (n V_2 - V_1) - 2\varphi n V_2}{4\pi f_S L} \quad (3.12)$$

results for positive phase shift, $0 < \varphi < \pi$, and a similar result is obtained for negative phase shift, $-\pi < \varphi < 0$. With (3.8) and (3.10), and by extending the results to the full phase shift range, $-\pi < \varphi < \pi$, the transferred power

$$P = P_1 = P_2 = \frac{n \cdot V_1 \cdot V_2 \cdot \varphi \cdot (\pi - |\varphi|)}{2\pi^2 f_S L} \quad \forall \quad -\pi < \varphi < \pi \quad (3.13)$$

results, where

$$\begin{aligned} P > 0 & \text{ denotes a power transfer from the HV to the LV port and} \\ P < 0 & \text{ denotes a power transfer from the LV to the HV port.} \end{aligned} \quad (3.14)$$

The achieved power transfer for the DAB converter designed in Appendix A.2 is depicted in Figure 3.5 and shows a maximum for a certain phase shift angle; maximum power occurs for $\partial P/\partial \varphi = 0$ with the solution

$$|P_{\text{PS,max}}| = \frac{n \cdot V_1 \cdot V_2}{8f_S L} \quad \text{for } \varphi = \pm\pi/2, \quad (3.15)$$

which presents an upper limit to the employed converter inductance L with respect to the specified output power.

The expression for the phase shift required to achieve a given power transfer is derived by rearranging (3.13):

$$\varphi = \frac{\pi}{2} \left[1 - \sqrt{1 - \frac{8f_S L |P|}{n V_1 V_2}} \right] \text{sgn}(P) \quad \forall \quad |P| < |P_{\text{PS,max}}|. \quad (3.16)$$

The great advantage of the phase shift modulation is its simplicity: according to (3.13), only a single control variable, the phase shift angle φ , is required to adjust the DAB power level (cf. Figure 3.5). The simplicity of this modulation method and the possibility of using half bridge circuits to generate the high frequency transformer voltages $v_{AC1}(t)$ and $v_{AC2}(t)$ are the main reasons for the wide use of this modulation method. Disadvantages are a limited operating range with low switching losses (soft switching range [50], cf. Section 4.3.2) and large RMS currents in the high frequency transformer for most operating points when the DAB is operated in wide voltage ranges (Figure 3.6). Even though, the calculated results depicted in Figure 3.6 are based on an efficiency optimized DAB design (cf. Appendix A.2), the loss-less DAB converter model predicts LV side transformer RMS currents of up to 283 A for $P = 2\text{ kW}$, $V_1 = 450\text{ V}$, and $V_2 = 11\text{ V}$ [Figure 3.6 (d)]. Figures 3.6 (a) and (b) depict the transformer RMS currents for $P = 1\text{ kW}$:

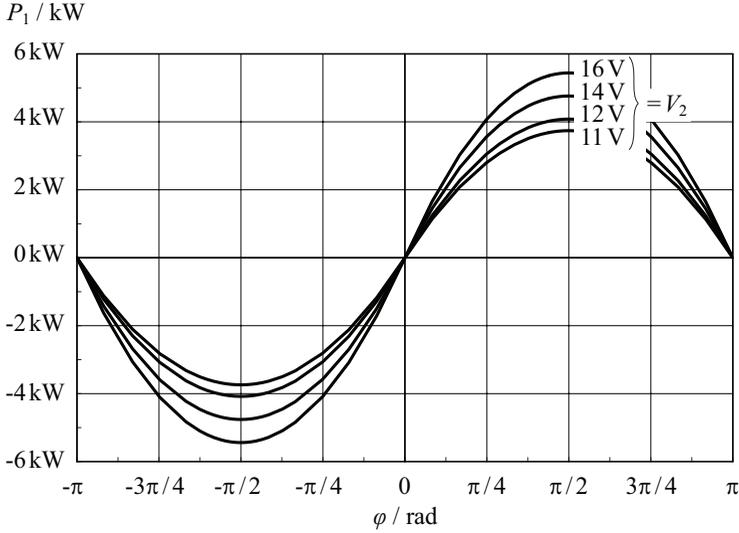


Figure 3.5: Transferred power for the DAB designed in Appendix A.2 ($n = 19$, $L = 26.7 \mu\text{H}$), phase shift modulation, $V_1 = 340 \text{ V}$ and different voltages V_2 . At $\varphi = \pm\pi/2$, maximum power transfer is achieved.

still currents of up to 256 A occur on the LV side. Merely for operating points close to $V_1 = n V_2$ [marked with dashed-and-dotted lines in Figures 3.6 (a) to (d)], effective transformer utilization is obtained.

With phase shift modulation, a reduced RMS value of the transformer current is only achieved with a different selection of n and L , since it is not possible to modify the shape of the transformer current;¹ the transformer current waveform solely depends on the DC voltages V_1 and V_2 and on the phase shift φ (for the assumption of a constant switching frequency f_s).

3.1.3 Alternative Modulation Methods

The disadvantages of phase shift modulation give reason to investigate alternative modulation methods which take advantage of the employed full bridges (Figure 3.1) and not only adjust the phase shift between $v_{AC1}(t)$ and $v_{AC2}(t)$

¹The presented design with $n = 19$ and $L = 26.7 \mu\text{H}$ is optimized with respect to maximum average efficiency (Appendix A.1, Appendix A.2). For a different selection of n and L , the maximum RMS value of the LV side transformer current can be reduced; as a result, however, the maximum switching losses increase.

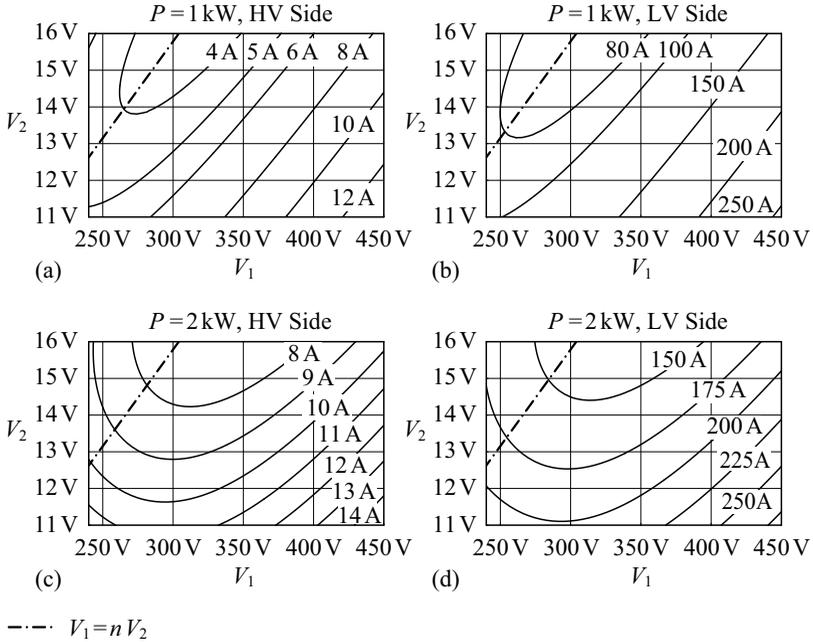


Figure 3.6: Transformer RMS currents for phase shift modulation and operation within the specified voltage ranges: (a) HV side and (b) LV side transformer currents for $P = 1\text{ kW}$, (c) HV side and (d) LV side transformer currents for $P = 2\text{ kW}$; $n = 19$, $L = 26.7\ \mu\text{H}$.

but as well change the duty cycles of $v_{AC1}(t)$ and $v_{AC2}(t)$ (Figure 3.3) in order to reduce the circulating transformer current and to achieve low switching losses. Thus, for the alternative modulation schemes, the desired attributes are:

1. Minimum RMS inductor current I_L in order to achieve low conduction losses, since the conduction losses dominate the total losses within a wide operating range.
2. Zero switch current during a switching process on the LV side: on the LV side, high currents lead to excessive switching losses due to the parasitic stray inductances of the packages of the switches (cf. Section 4.3.3, [89,93]).
3. Zero voltage switching (ZVS) operation of the HV side switches in order

to obtain low switching losses (Section 4.3.2, [85]).

First investigations on alternative modulation schemes are given in [94] for a bidirectional AC–DC converter: the proposed alternative modulation schemes extend the zero voltage switching (ZVS) range of the DAB and simultaneously reduce the transformer RMS currents (the principle of operation of ZVS is discussed in [43]). Detailed investigations of the modulation schemes discussed in [94] with either $D_1 \leq 0.5 \wedge D_2 = 0.5$ or $D_1 = 0.5 \wedge D_2 \leq 0.5$ are presented in [95,96]. The 1-D optimization problem (either D_1 or D_2 changes) with respect to maximum converter efficiency is solved in [95] (the analysis is based on the lossless electric DAB model [50] and an analytical converter loss model).

In a different approach, highly efficient operation of the DAB is reported with modulation schemes employing $D_1 \leq 0.5$ and $D_2 \leq 0.5$ [91,97,98,99]. However, compared to the above mentioned 1-D problem, it is considerably more complex to solve the resulting 2-D problem (D_1 and D_2 change simultaneously) with respect to maximal efficiency [100]. Therefore, a more intuitive method is typically used to determine D_1 and D_2 as described e.g. in [91,97], where D_1 and D_2 are selected in order to achieve a triangular or trapezoidal shape of the transformer current which results in low switching losses and low conduction losses. Further efficiency improvements are reported with the use of combined modulation schemes (in [101,102], either the conventional phase shift modulation or modulation schemes with triangular or trapezoidal transformer currents are employed, depending on the actual output power and the port voltages V_1 and V_2).

With the alternative modulation schemes discussed in [97], i.e. the triangular and trapezoidal current mode modulation schemes, considerable efficiency improvements are expected; moreover, comparably little computational effort is required to calculate the respective modulation parameters D_1 , D_2 , and φ . These modulation schemes are therefore first revisited in this Section; subsequently, a systematic optimization of the modulation parameters D_1 and D_2 with respect to minimal transformer RMS current is presented for the lossless DAB (with given D_1 and D_2 the operating voltages V_1 and V_2 and the required output power determine φ).²

Triangular Current Mode Modulation

In [97], the triangular current mode modulation is introduced; this modulation scheme enables LV side switching at zero transformer current. Furthermore, compared to phase shift modulation, a considerable reduction of the transformer RMS current is achieved.

²Improved and optimized modulation schemes considering the DAB converter losses are detailed in Chapter 5.

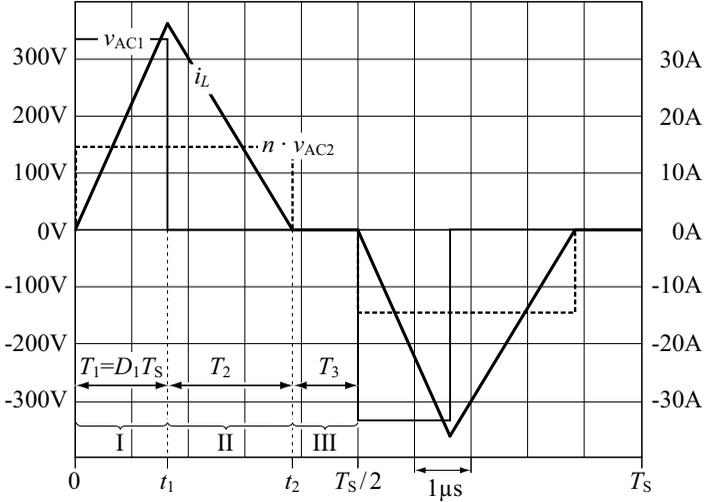


Figure 3.7: Transformer voltages and inductor current for triangular current mode modulation [97], $V_1 = 340$ V, $V_2 = 12$ V, $P = 2$ kW, $n = 12$, $L = 8.8$ μ H, and $f_s = 100$ kHz. In order to enable the operation of the DAB with the triangular current mode modulation within the operating range specified in Table 1.4, a transformer turns ratio $n < 15$ is required [cf. (3.29)]. A converter optimization with respect to maximum average efficiency (Appendix A.1) gives $n = 12$ and $L = 8.8$ μ H.

Figure 3.7 depicts typical voltage and current waveforms for the triangular current mode modulation, $V_1 > n V_2$, and $P > 0$ [power transfer from the HV port to the LV port, cf. (3.14)]. There, at $t = 0$, the inductor current, i_L , is zero and the DAB full bridges apply $v_{AC1}(t) = V_1$ and $v_{AC2}(t) = V_2$ to the HF transformer and the DAB inductor L . Due to $i_L(0) = 0$, low switching losses are expected for the respective switching operations.³ Subsequently, during $0 < t < t_1$, the inductor current increases according to

$$i_L(t) = 0 + \frac{V_1 - n V_2}{L} t \quad \forall \quad 0 < t < t_1. \quad (3.17)$$

At $t = t_1$, the state of the HV side full bridge changes with low switching losses, since the condition for ZVS is fulfilled (cf. Section 4.3.2), and during $t_1 < t < t_2$, the HV side full bridge generates $v_{AC1}(t) = 0$ while the LV side full

³In practice this is true for the LV side; however, considerable HV side switching losses occur due to the effects discussed in Section 4.3.2 (cf. Figure 4.14).

bridge state remains unchanged. Thus, the inductor current changes according to:

$$i_L(t) = i_L(t_1) - \frac{n V_2}{L} (t - t_1) \quad \forall \quad t_1 < t < t_2. \quad (3.18)$$

At the time t_2 the inductor current is zero and the LV side full bridge switches to $v_{AC2} = 0$. Consequently, the inductor current remains zero during $t_2 < t < T_S/2$,

$$i_L(t) = 0 \quad \forall \quad t_2 < t < T_S/2. \quad (3.19)$$

The durations T_1 and T_2 of the respective time intervals I and II determine the transferred power P according to

$$P = \frac{n V_2}{T_S L} [V_1 T_1 \cdot (2T_2 - T_1) - n V_2 T_2^2] \quad \forall \quad V_1 > n V_2; \quad (3.20)$$

moreover, T_2 depends on T_1 in order to achieve $i_L(t_2) = 0$:

$$T_2 = T_1 \frac{V_1 - n V_2}{n V_2}. \quad (3.21)$$

With

$$\varphi = 2\pi f_S [(T_1 + T_2)/2 - T_1/2] = \pi f_S T_2 \quad (3.22)$$

(cf. Figure 3.3), (3.20), and (3.21), the transferred power is solely controlled with φ ,

$$P = \frac{\varphi^2 V_1 (n V_2)^2}{\pi^2 f_S L (V_1 - n V_2)} \quad \forall \quad V_1 > n V_2 \quad \wedge \quad 0 < \varphi < \varphi_{\Delta, a, \max}, \quad (3.23)$$

so we have for φ , T_1 , and T_2 :

$$\varphi = \pi \sqrt{f_S L P \frac{V_1 - n V_2}{V_1 (n V_2)^2}} \quad \forall \quad V_1 > n V_2 \quad \wedge \quad 0 < \varphi < \varphi_{\Delta, a, \max}, \quad (3.24)$$

$$T_1 = \frac{\varphi}{\pi f_S} \frac{n V_2}{V_1 - n V_2}, \quad \text{and} \quad (3.25)$$

$$T_2 = \frac{\varphi}{\pi f_S} \quad (3.26)$$

in order to achieve a given power level. However, the maximum phase shift angle $\varphi_{\Delta, a, \max}$ must not be exceeded, since the duration $T_3 = T_S/2 - T_1 - T_2$ of time interval III decreases with increasing power P due to (3.21), (3.22), and (3.24). The maximum power transfer is achieved for $T_3 = 0$ and is equal to

$$P_{\Delta, a, \max} = \frac{n^2 V_2^2 (V_1 - n V_2)}{4 f_S L V_1}; \quad (3.27)$$

the respective maximum phase shift angle is

$$\varphi_{\Delta, a, \max} = \varphi(P_{\Delta, a, \max}) = \frac{\pi}{2} \left(1 - \frac{n V_2}{V_1} \right). \quad (3.28)$$

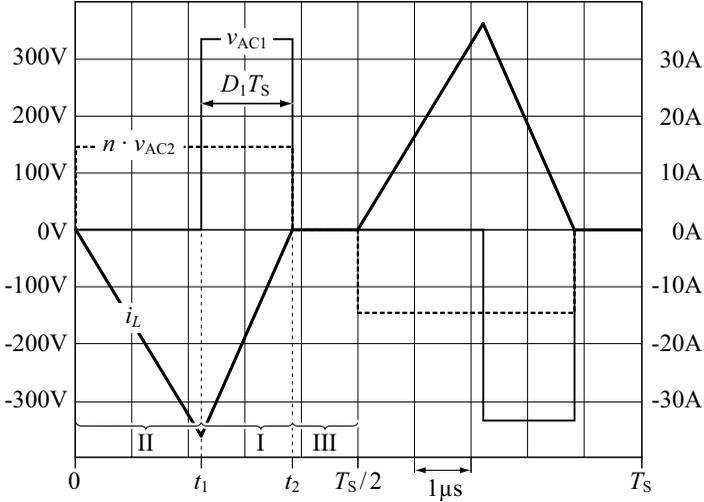


Figure 3.8: Transformer voltages and inductor current for triangular current mode modulation [97], $V_1 = 340$ V, $V_2 = 12$ V, $P = -2$ kW, $n = 12$, $L = 8.8$ μ H, and $f_s = 100$ kHz.

Obviously, $P_{\Delta,a,\max}$ is zero for $V_1 = nV_2$ and negative for $V_1 < nV_2$. The presented modulation scheme only allows for a power transfer for $V_1 > nV_2$ and for positive power $0 < P < P_{\Delta,a,\max}$. The transformer turns ratio n is thus limited to

$$n < \frac{V_{1,\min}}{V_{2,\max}} = 15. \quad (3.29)$$

A converter optimization with respect to maximum average efficiency (Appendix A.1) gives $n = 12$ and $L = 8.8$ μ H.

For $V_1 > nV_2$, power transfer from the LV port to the HV port, $0 > P > -P_{\Delta,a,\max}$, is achieved with negative φ (i.e. swapped time intervals I and II in Figure 3.7, cf. Figure 3.8):

$$P = -\frac{\varphi^2 V_1 (nV_2)^2}{\pi^2 f_s L (V_1 - nV_2)} \quad \forall \quad V_1 > nV_2 \quad \wedge \quad -\varphi_{\Delta,a,\max} < \varphi < 0. \quad (3.30)$$

With known transformer turns ratio n , (3.27) limits the maximum allowable

DAB inductance L according to

$$L < \min \left(\frac{n^2 V_{2,\min}^2 (V_{1,\min} - n V_{2,\min})}{4 f_S P_{\Delta,a,\max} V_{1,\min}}, \frac{n^2 V_{2,\max}^2 (V_{1,\min} - n V_{2,\max})}{4 f_S P_{\Delta,a,\max} V_{1,\min}} \right). \quad (3.31)$$

The resulting transformer RMS currents are shown in Figure 3.9 for $n = 12$, $L = 8.8 \mu\text{H}$, and $P = 1 \text{ kW}$ [Figures 3.9 (a) and (b)] or $P = 2 \text{ kW}$ [Figures 3.9 (c) and (d)]. For $P = 2 \text{ kW}$, the lossless DAB model predicts a maximum transformer RMS current of 242 A on the LV side, which is 14% less than the maximum RMS current obtained for phase shift modulation (283 A). For $P = 1 \text{ kW}$, the maximum RMS current decreases to 144 A (compared to 256 A for phase shift modulation). However, the usable transformer turns ratio, n , is limited according to (3.29), i.e. $V_1 > n V_2$ applies. Consequently, comparably high transformer RMS currents occur on the HV side, which considerably increase the HV side conduction losses (cf. Section 4.1); moreover, the DAB fails to operate in case of the abnormal operating condition $V_1 < n V_2$.

If LV side switching at zero inductor current is not mandatory, the operation with $V_1 < n V_2$ is easily achieved with a different triangular current mode modulation scheme, which employs the AC voltages $v_{AC1}(t)$ and $v_{AC2}(t)$ shown in Figures 3.10 and 3.11. The respective DAB power levels are:

$$P = \begin{cases} \frac{\varphi^2 V_1^2 n V_2}{\pi^2 f_S L (n V_2 - V_1)} & \forall V_1 < n V_2 \wedge 0 < \varphi < \varphi_{\Delta,b,\max} \text{ and} \\ & v_{AC1}(t), v_{AC2}(t) \text{ according to Figure 3.10,} \\ -\frac{\varphi^2 V_1^2 n V_2}{\pi^2 f_S L (n V_2 - V_1)} & \forall V_1 < n V_2 \wedge -\varphi_{\Delta,b,\max} < \varphi < 0 \text{ and} \\ & v_{AC1}(t), v_{AC2}(t) \text{ according to Figure 3.11,} \end{cases} \quad (3.32)$$

with the maximum phase shift angle

$$\varphi_{\Delta,b,\max} = \frac{\pi}{2} \left(1 - \frac{V_1}{n V_2} \right). \quad (3.33)$$

Maximum power transfer is again achieved for $t_2 = T_S/2$ (cf. Figure 3.10); with this, the upper power limit for the combined triangular current mode modulation schemes (Figures 3.7, 3.8, 3.10, and 3.11) becomes:

$$P_{\Delta,\max} = \begin{cases} \frac{n^2 V_2^2 (V_1 - n V_2)}{4 f_S L V_1} & \text{for } V_1 > n V_2, \\ 0 & \text{for } V_1 = n V_2, \\ \frac{V_1^2 (n V_2 - V_1)}{4 f_S L n V_2} & \text{for } V_1 < n V_2. \end{cases} \quad (3.34)$$

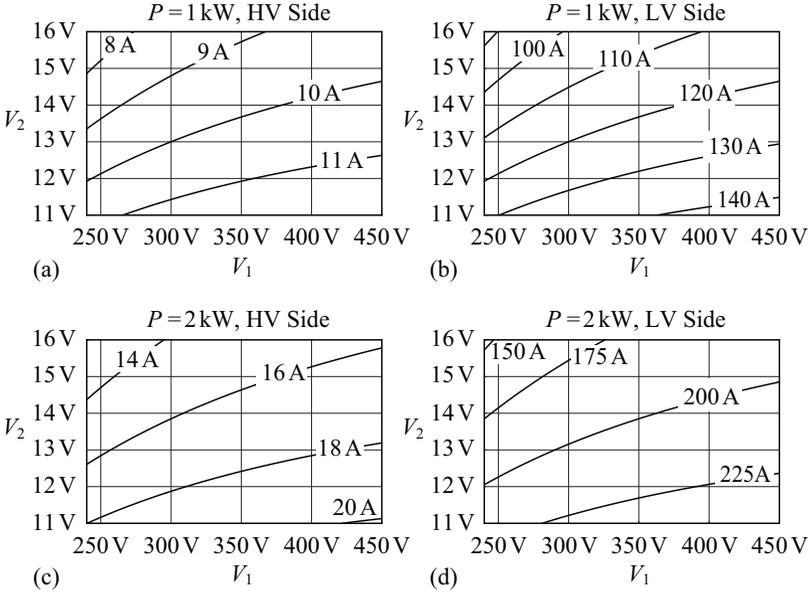


Figure 3.9: Transformer RMS currents for the triangular current mode modulation scheme and operation within the specified voltage ranges: (a) HV side and (b) LV side transformer currents for $P = 1\text{ kW}$, (c) HV side and (d) LV side transformer currents for $P = 2\text{ kW}$; $n = 12$, $L = 8.8\ \mu\text{H}$.

Trapezoidal Current Mode Modulation

With the triangular current mode modulation schemes, $|P| < P_{\Delta, \max}$ [cf. (3.34)] limits the DAB power level; this is particularly undesirable for $V_1 \approx n V_2$ where $P_{\Delta, \max}$ is either zero or close to zero. If switching at zero inductor current is not mandatory on the LV side, the operation of the DAB with $|P| > P_{\Delta, \max}$ is possible, e.g. with the trapezoidal current mode modulation scheme presented in [97]. Typical current and voltage waveforms are depicted in Figures 3.12 and 3.13. Since the inductor current is again zero at $t = k \cdot T_S/2$, $k \in \mathbb{Z}$, a seamless transition between trapezoidal and triangular current mode modulation is achieved.

For the trapezoidal current mode modulation, three different time intervals can be distinguished. During $0 < t < t_1$, $v_{AC1}(t) = V_1$ and $v_{AC2}(t) = 0$ apply and the absolute value of the inductor current, $|i_L(t)|$, increases from zero; at $t = t_1$, the voltage $v_{AC2}(t)$ changes to $v_{AC2}(t) = n V_2$ and remains constant

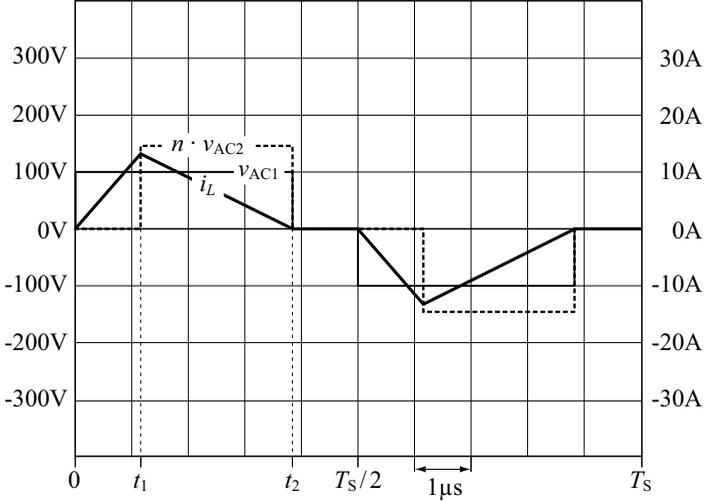


Figure 3.10: Transformer voltages and inductor current for triangular current mode modulation (cf. [97]) in case of $V_1 < n V_2$: $V_1 = 100$ V, $V_2 = 12$ V, $P = 500$ W, $n = 12$, $L = 8.8$ μ H, and $f_s = 100$ kHz.

during $t_1 < t < t_2$; during $t_2 < t < T_s/2$, $v_{AC1}(t) = 0$ and $v_{AC2}(t) = V_2$ apply and $|i_L(t)|$ decreases back to zero.

The transferred power is equal to

$$P = \text{sgn}(\varphi) \frac{nV_1V_2 \cdot [2nV_1V_2(\pi^2 - 2\varphi^2) - (V_1^2 + (nV_2)^2) \cdot (\pi - 2|\varphi|)^2]}{4\pi^2 f_s L \cdot (V_1 + nV_2)^2} \quad \forall \varphi_{\Delta, \max} < |\varphi| < \varphi_{\Delta, \max} \quad (3.35)$$

with

$$\varphi_{\Delta, \max} = \frac{\pi}{2} \left(1 - \frac{nV_1V_2}{V_1^2 + nV_1V_2 + (nV_2)^2} \right). \quad (3.36)$$

The solutions for the required phase shift angle φ and the durations T_1 , T_2 , and T_3 are:

$$\varphi = \frac{\pi}{2} \cdot \frac{\text{sgn}(P)}{V_1^2 + nV_1V_2 + (nV_2)^2} \cdot \left\{ V_1^2 + (nV_2)^2 - (V_1 + nV_2) \sqrt{nV_1V_2 \left[1 - \frac{4f_s L |P| (V_1^2 + nV_1V_2 + (nV_2)^2)}{(nV_1V_2)^2} \right]} \right\}, \quad (3.37)$$

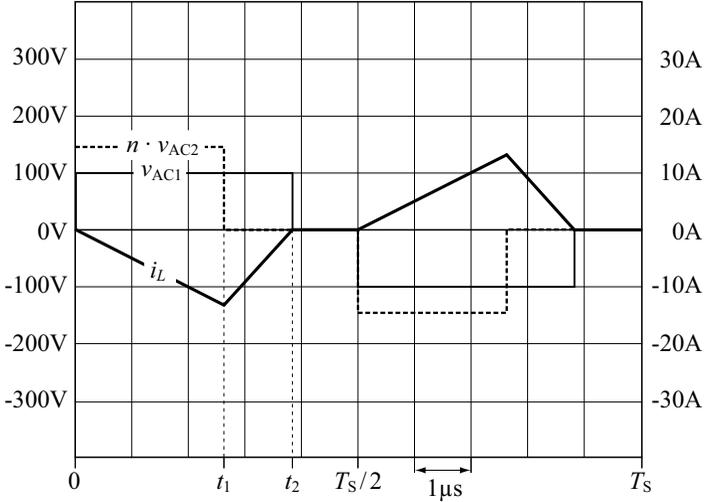


Figure 3.11: Transformer voltages and inductor current for triangular current mode modulation (cf. [97]) in case of $V_1 < n V_2$: $V_1 = 100 \text{ V}$, $V_2 = 12 \text{ V}$, $P = -500 \text{ W}$, $n = 12$, $L = 8.8 \mu\text{H}$, and $f_s = 100 \text{ kHz}$.

$$T_1 = \frac{n V_2 - V_1 + 2 V_1 \varphi / \pi}{2 f_s \cdot (V_1 + n V_2)}, \quad (3.38)$$

$$T_2 = \frac{1 - 2 \varphi / \pi}{2 f_s}, \quad (3.39)$$

$$T_3 = \frac{V_1 - n V_2 + 2 n V_2 \varphi / \pi}{2 f_s \cdot (V_1 + n V_2)}. \quad (3.40)$$

$$(3.41)$$

The maximum transferable power is:

$$P_{\Delta, \max} = \frac{(n V_1 V_2)^2}{4 f_s L \cdot (V_1^2 + n V_1 V_2 + (n V_2)^2)}. \quad (3.42)$$

Expression (3.42) determines the upper limit for L :

$$L < \frac{(n V_{1, \min} V_{2, \min})^2}{4 f_s P_{\Delta, \max} \cdot (V_{1, \min}^2 + n V_{1, \min} V_{2, \min} + (n V_{2, \min})^2)}. \quad (3.43)$$

The RMS values of the HV side and LV side transformer currents predicted with the lossless DAB model are shown in Figure 3.14 for the alternative

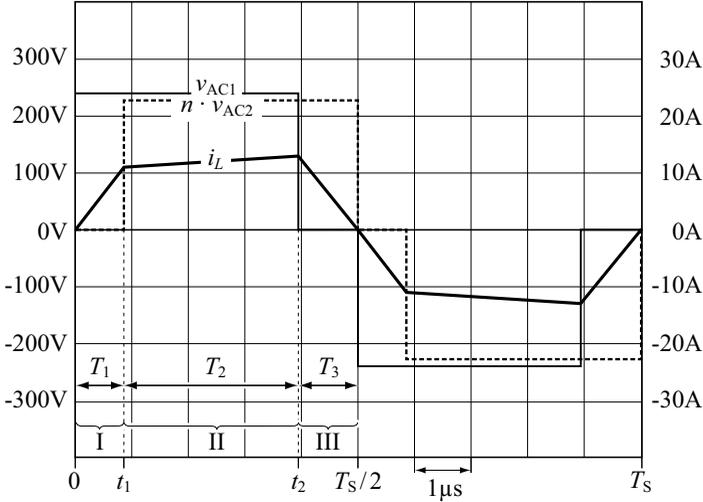


Figure 3.12: Transformer voltages and inductor current for trapezoidal current mode modulation [97], $V_1 = 240$ V, $V_2 = 12$ V, $P = 2$ kW, $n = 19$, $L = 18.7$ μ H, and $f_s = 100$ kHz [$n = 19$ is selected in order to allow for a direct comparison with the results obtained for phase shift modulation and $L = 18.7$ μ H is required in order to achieve the specified power transfer, cf. (3.43)].

modulation scheme. In order to allow for a comparison with the RMS currents obtained for phase shift modulation (Figure 3.6), $n = 19$ was selected, which requires a converter inductance $L = 18.7$ μ H.

Depending on the actual power level P and the operating voltages V_1 and V_2 , either the trapezoidal current mode modulation or the triangular current mode modulation is used; with (3.34) and (3.42), the appropriate modulation scheme is selected:

$$\begin{aligned}
 0 < |P| < P_{\Delta, \max}(V_1, V_2) &: && \text{triangular current mode,} \\
 P_{\Delta, \max}(V_1, V_2) < |P| < P_{\Delta, \max}(V_1, V_2) &: && \text{trapezoidal current mode.}
 \end{aligned} \tag{3.44}$$

In Figure 3.14, the borders between triangular and trapezoidal current mode modulations are marked with dashed lines.

With the alternative modulation scheme (the combined trapezoidal and triangular current mode modulation), the maximum transformer RMS current (235 A) is only slightly below the maximum RMS current obtained for exclusive triangular current mode modulation (242 A). However, on the HV side, a

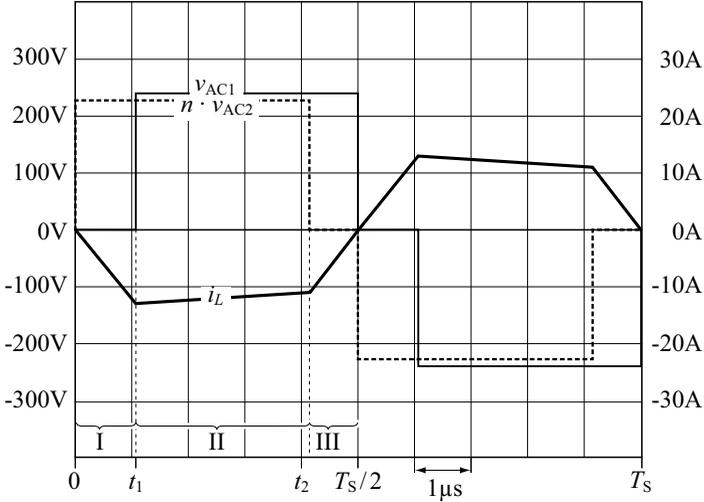


Figure 3.13: Transformer voltages and inductor current for trapezoidal current mode modulation [97], $V_1 = 240\text{ V}$, $V_2 = 12\text{ V}$, $P = -2\text{ kW}$, $n = 19$, $L = 18.7\text{ }\mu\text{H}$, and $f_s = 100\text{ kHz}$.

considerably lower maximum RMS current of 12.4 A is obtained (as opposed to 20.1 A for the exclusive triangular current mode modulation). Compared to phase shift modulation, lower maximum RMS currents are achieved (phase shift modulation: HV side: 14.9 A, LV side: 283 A). For $P = 1\text{ kW}$, the maximum transformer RMS currents decrease to 7.3 A on the HV side and to 140 A on the LV side with the alternative modulation scheme. Thus, compared to the phase shift modulation (Figure 3.6) or to the exclusive triangular current mode modulation (Figure 3.9), a considerable improvement is achieved.

Optimal Modulation

For the given DAB converter, the trapezoidal and the triangular current mode modulation schemes have been intuitively selected due to the low expected conduction and switching losses. A more systematic investigation is required in order to discover the modulation scheme that leads to the lowest value of the RMS current I_L (and thus to the lowest conduction losses, cf. Chapter 4), the lowest switching losses, and / or the lowest total losses. In this section, the discussion focuses on the minimization of I_L .

With the two full bridge circuits, 12 basic voltage sequences can be dis-

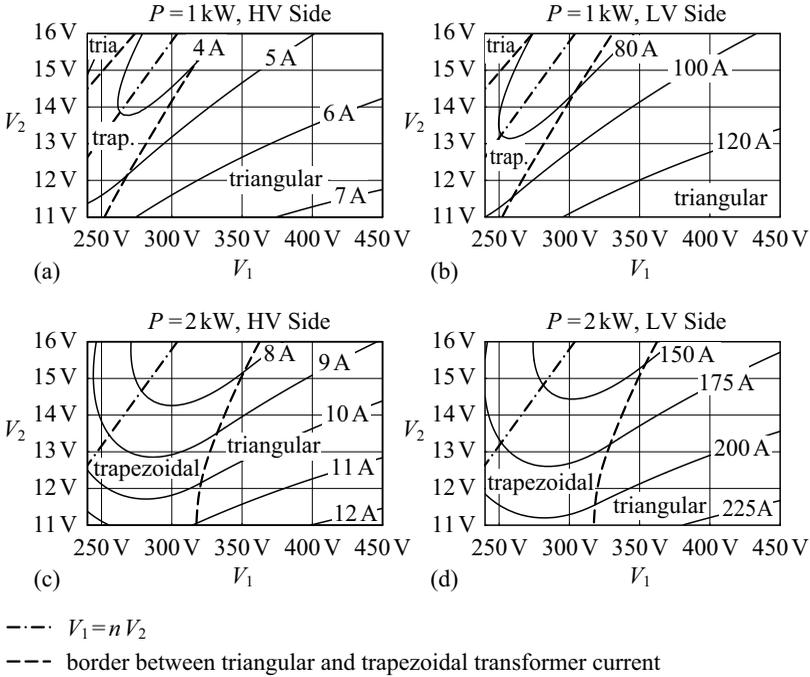


Figure 3.14: Transformer RMS currents for the trapezoidal and triangular current mode modulation schemes and operation within the specified voltage ranges: (a) HV side and (b) LV side transformer currents for $P = 1\text{ kW}$, (c) HV side and (d) LV side transformer currents for $P = 2\text{ kW}$; $n = 19$, $L = 18.7\ \mu\text{H}$.

tinguished with respect to the different sequences of rising and falling edges of v_{AC1} and v_{AC2} (Figure 3.15). The search towards the modulation scheme with minimum I_L , though, only considers the 6 sequences 1a, 1b, 2, 3b, 7b, and 8; the remaining 6 options lead to an increased RMS value of the inductor current I_L and do not result in a higher DAB power level (cf. Table 3.1 and Figure 3.15).

For the presented analysis, a set of 5 input parameters is required, which consists of V_1 , V_2 , P , D_1 , and D_2 . The optimization method further requires a certain mode discrimination (Table 3.2), since the expressions for the particular DAB power levels (Table 3.3), the phase shift angles (Table 3.4), and the inductor RMS currents (Table 3.5) are substantially different for the different

<i>Sequence Number</i>	D_1	D_2	φ	I_L	$P_1 = P_2$
1a	0.1	0.25	0°	3.5 A	0 W
2	0.1	0.25	45°	6.9 A	653 W
3a	0.1	0.25	90°	10.8 A	726 W
4	0.1	0.25	135°	13.5 A	653 W
5a	0.1	0.25	180°	14.7 A	0 W
6	0.1	0.25	-135°	13.5 A	-653 W
7a	0.1	0.25	-90°	10.8 A	-726 W
8	0.1	0.25	-45°	6.9 A	-653 W
1b	0.25	0.1	0°	9.3 A	0 W
5b	0.25	0.1	180°	17.0 A	0 W
3b	0.25	0.4	90°	17.7 A	2.58 kW
7b	0.25	0.4	-90°	17.7 A	-2.58 kW

Table 3.1: Resulting inductor RMS currents and power levels for the different voltage sequences depicted in Figure 3.15 ($V_1 = 340$ V, $V_2 = 12$ V, $L = 26.7$ μ H, $n = 19$, and $f_s = 100$ kHz).

voltage sequences depicted in Figure 3.15.

Table 3.2 summarizes the conditions that must be fulfilled for the respective voltage sequence and Figure 3.16 shows the active sequences for $V_1 = 340$ V, $V_2 = 12$ V, different duty cycles, and different power levels. With the preselected 6 sequences and with a specified set of input parameters only a single valid sequence number occurs—ambiguities are avoided.

The optimization procedure then minimizes the cost function, e.g. the value of the RMS current I_L , with respect to D_1 and D_2 for a fixed operating point (Figure 3.17) in order to determine the optimal modulation scheme.

(The text continues on page 81.)

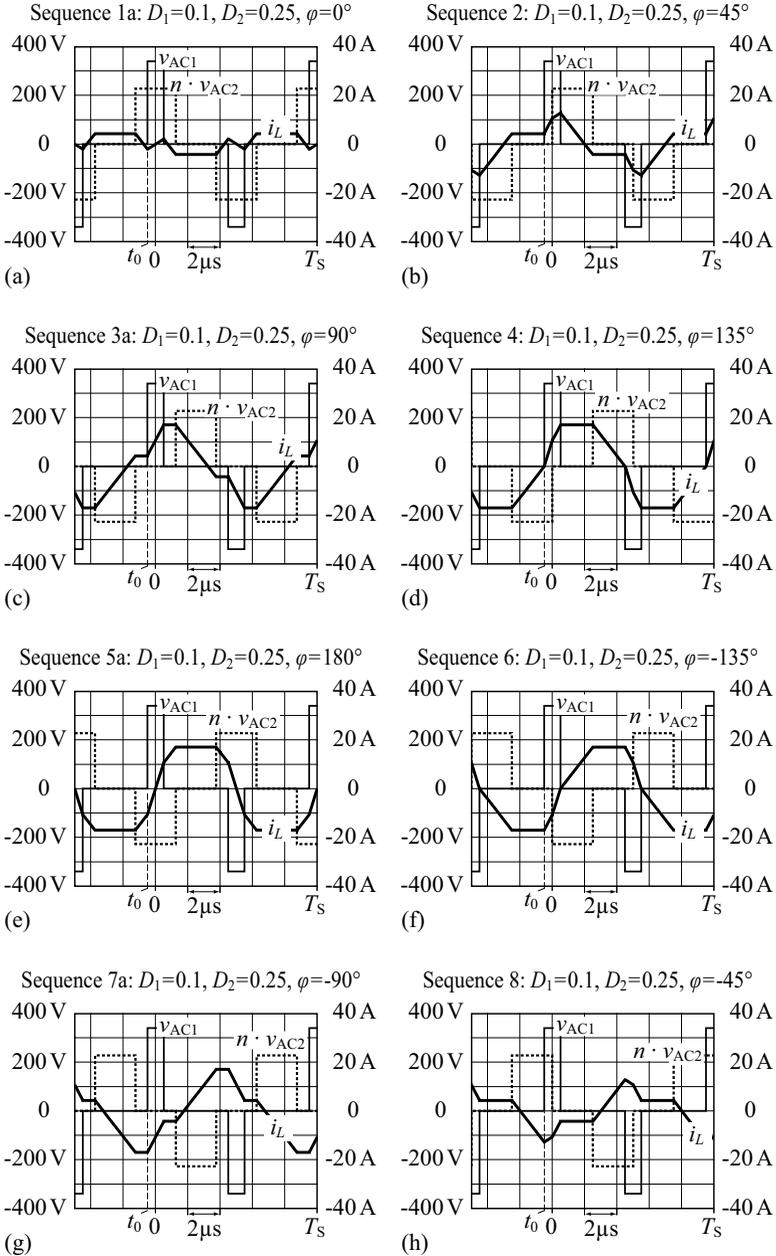


Figure 3.15: The 12 basic voltage sequences generated with the two full bridges (continued on the next page).

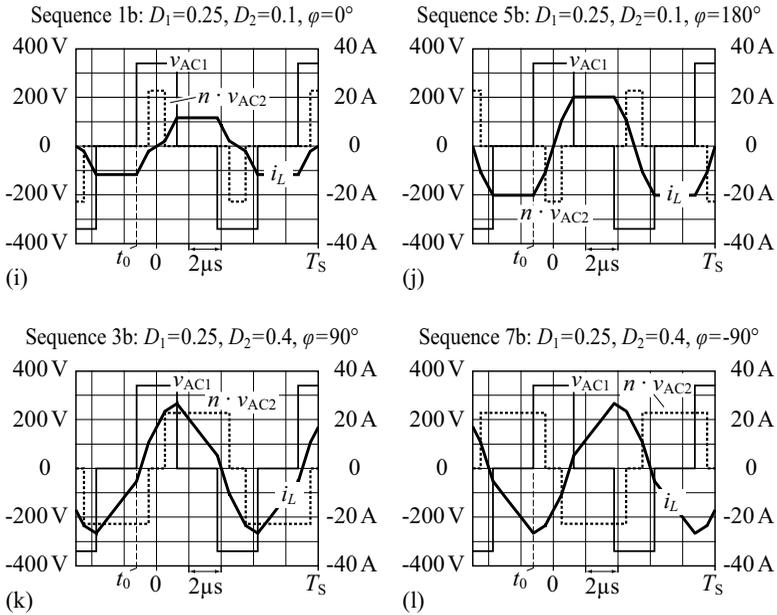


Figure 3.15 cont.: The 12 basic voltage sequences generated with the two full bridges. The respective transformer RMS currents and DAB power levels are given in Table 3.1; $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, $L = 26.7 \mu\text{H}$, $n = 19$, and $f_S = 100 \text{ kHz}$; t_0 denotes the time the steady-state inductor current expressions in Table 3.6 are given for. Again, $L = 26.7 \mu\text{H}$ and $n = 19$ are selected in order to allow for a straight comparison with the results obtained for phase shift modulation.

<i>Mode</i>	<i>Condition</i>
1a	$D_1 - D_2 < \varphi/\pi < -D_1 + D_2$
1b	$-D_1 + D_2 < \varphi/\pi < D_1 - D_2$
2	$ D_1 - D_2 < \varphi/\pi < \min [D_1 + D_2, 1 - (D_1 + D_2)]$
8	$ D_1 - D_2 < -\varphi/\pi < \min [D_1 + D_2, 1 - (D_1 + D_2)]$
3b	$1 - (D_1 + D_2) < \varphi/\pi < D_1 + D_2$
7b	$1 - (D_1 + D_2) < -\varphi/\pi < D_1 + D_2$

Table 3.2: Conditions required in order to enable the respective sequences.

<i>Mode</i>	<i>DAB power level</i>
All	$P = P_1 = P_2 = \frac{nV_1V_2}{f_{\text{SL}}L} e_P$
1a	$e_P = D_1 \frac{\varphi}{\pi}$
1b	$e_P = D_2 \frac{\varphi}{\pi}$
2	$e_P = -\frac{1}{4} \left[\frac{\varphi^2}{\pi^2} - 2\frac{\varphi}{\pi} (D_1 + D_2) + (D_1 - D_2)^2 \right]$
8	$e_P = \frac{1}{4} \left[\frac{\varphi^2}{\pi^2} + 2\frac{\varphi}{\pi} (D_1 + D_2) + (D_1 - D_2)^2 \right]$
3b	$e_P = -\frac{1}{2} \left\{ \frac{\varphi^2}{\pi^2} - \frac{\varphi}{\pi} + \left[\frac{1}{2} - D_1(1 - D_1) - D_2(1 - D_2) \right] \right\}$
7b	$e_P = \frac{1}{2} \left\{ \frac{\varphi^2}{\pi^2} + \frac{\varphi}{\pi} + \left[\frac{1}{2} - D_1(1 - D_1) - D_2(1 - D_2) \right] \right\}$

Table 3.3: Expressions for the DAB power level P for the considered voltage sequences.

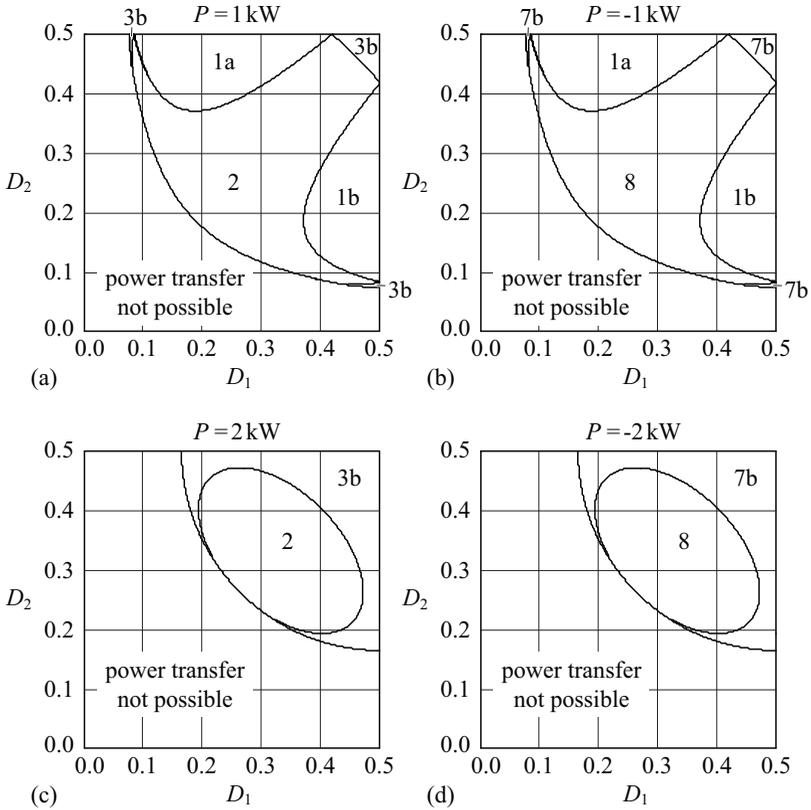


Figure 3.16: The employed voltage sequences, plotted against D_1 and D_2 , for fixed operating voltages ($V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$) and 4 different power levels; the required power transfer cannot be accomplished if D_1 and D_2 fall below a certain limit. DAB parameters: $n = 19$, $L = 26.7 \mu\text{H}$, $f_S = 100 \text{ kHz}$.

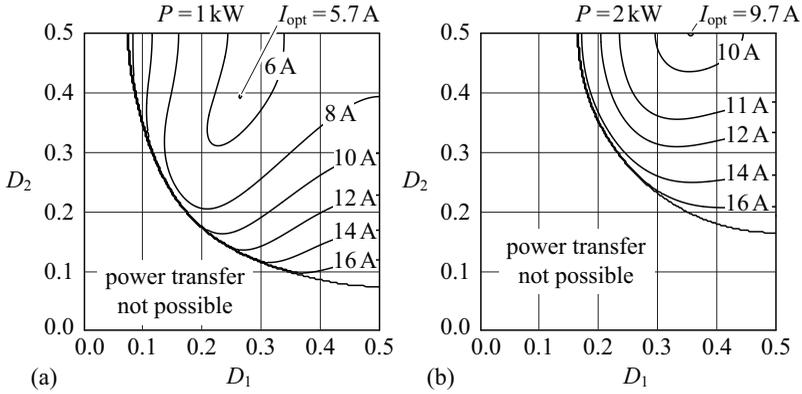


Figure 3.17: The resulting inductor RMS currents, I_L , for fixed operating voltages ($V_1 = 340$ V, $V_2 = 12$ V), 2 different power levels, and different combinations of D_1 and D_2 ; I_{opt} denotes the minimum RMS current. Employed DAB converter parameters: $n = 19$, $L = 26.7$ μH , $f_s = 100$ kHz.

Mode	φ
1a	$\varphi = \frac{\pi L f_s P}{n D_1 V_1 V_2}$
1b	$\varphi = \frac{\pi L f_s P}{n D_2 V_1 V_2}$
2, 8	$\varphi = \pi \operatorname{sgn}(P) \cdot \left(D_1 + D_2 - 2 \sqrt{D_1 D_2 - \frac{L P f_s}{n V_1 V_2}} \right)$
3b, 7b	$\varphi = \pi \operatorname{sgn}(P) \cdot \left[\frac{1}{2} - \sqrt{D_1(1-D_1) + D_2(1-D_2) - \frac{1}{4} - \frac{2f_s L P }{n V_1 V_2}} \right]$

Table 3.4: Required phase shift angle φ for a given power $P = P_1 = P_2$.

Mode	Inductor RMS current I_L
All	$I_L = \frac{1}{2f_s L} \sqrt{D_1^2 V_1^2 \left(1 - \frac{4}{3} D_1\right) + D_2^2 n^2 V_2^2 \left(1 - \frac{4}{3} D_2\right) + \frac{n V_1 V_2}{3} e_{\text{RMS}}}$
1a	$e_{\text{RMS}} = 6D_1 \left[\frac{\varphi^2}{\pi^2} + \left(D_2 (D_2 - 1) + \frac{D_1^2}{3} \right) \right]$
1b	$e_{\text{RMS}} = 6D_2 \left[\frac{\varphi^2}{\pi^2} + \left(D_1 (D_1 - 1) + \frac{D_2^2}{3} \right) \right]$
2	$e_{\text{RMS}} = D_1^3 + 3D_1^2 \left(D_2 - \frac{\varphi}{\pi} \right) + 3D_1 \left[\frac{\varphi^2}{\pi^2} - D_2 \left(2 - \frac{2\varphi}{\pi} - D_2 \right) \right] + \left(D_2 - \frac{\varphi}{\pi} \right)^3$
8	$e_{\text{RMS}} = D_1^3 + 3D_1^2 \left(D_2 + \frac{\varphi}{\pi} \right) + 3D_1 \left[\frac{\varphi^2}{\pi^2} - D_2 \left(2 + \frac{2\varphi}{\pi} - D_2 \right) \right] + \left(D_2 + \frac{\varphi}{\pi} \right)^3$
3b	$e_{\text{RMS}} = \left(1 - \frac{2\varphi}{\pi} \right) \left\{ 1 - \frac{\varphi}{\pi} + \frac{\varphi^2}{\pi^2} - 3 [D_1 (1 - D_1) + D_2 (1 - D_2)] \right\}$
7b	$e_{\text{RMS}} = \left(1 + \frac{2\varphi}{\pi} \right) \left\{ 1 + \frac{\varphi}{\pi} + \frac{\varphi^2}{\pi^2} - 3 [D_1 (1 - D_1) + D_2 (1 - D_2)] \right\}$

Table 3.5: Expressions for the inductor RMS current I_L for the considered voltage sequences.

Mode	Inductor current at $t = t_0$
1a, 8, 7b	$i_L(t_0) = \frac{1}{2Lf_s} \left[nV_2 \left(\frac{\varphi}{\pi} + D_1 \right) - D_1 V_1 \right]$
1b, 2	$i_L(t_0) = \frac{1}{2Lf_s} (nD_2 V_2 - D_1 V_1)$
3b	$i_L(t_0) = \frac{1}{2Lf_s} \left[nV_2 \left(1 - \frac{\varphi}{\pi} \right) - D_1 (V_1 + nV_2) \right]$

Table 3.6: Steady-state inductor current $i_L(t_0)$ (at t_0 , v_{AC1} changes from 0 to V_1 , cf. Figure 3.15).

The optimization with respect to minimum I_L suggests the triangular current mode modulation for $|P| < P_{\Delta, \max}$ [cf. (3.34)]. For $|P| > P_{\Delta, \max}$, however, a modulation scheme different to the trapezoidal current mode modulation results: the optimization identifies the voltage sequence 3b for $P > P_{\Delta, \max}$ (Figure 3.18) and 7b for $P < -P_{\Delta, \max}$ (Figure 3.19) as optimal. The respective values of the optimal duty cycles depend on the ratio $V_1/(nV_2)$:

1. $V_1 = nV_2$
2. $V_1 > nV_2 \wedge |P| > P_{a, \max}$
3. $V_1 < nV_2 \wedge |P| > P_{b, \max}$
4. $V_1 > nV_2 \wedge P_{\Delta, \max} < |P| < P_{a, \max}$: optimal transition mode;
 $D_{1, \text{opt}}$ is calculated with (3.45),
 $D_{2, \text{opt}} = 1/2$,
5. $V_1 < nV_2 \wedge P_{\Delta, \max} < |P| < P_{b, \max}$: optimal transition mode;
 $D_{1, \text{opt}} = 1/2$,
 $D_{2, \text{opt}}$ is calculated with (3.49)

[$P_{a, \max}$ and $P_{b, \max}$ are defined with (3.47) and (3.50), respectively].

For $P_{\Delta, \max} < |P| < P_{a, \max}$, a complicated expression results for $D_{1, \text{opt}}$ ($e_{a,1} \dots e_{a,7}$ denote interim values):

$$\begin{aligned}
 e_{a,1} &= \frac{V_1^2}{V_1^2 + n^2V_2^2} - 2, \\
 e_{a,2} &= \frac{n^2V_2^2}{V_1^2 + n^2V_2^2} + \frac{2L|P|f_S}{nV_1V_2}, \\
 e_{a,3} &= \frac{V_1^3}{f_S^6} [2V_1^3n^9V_2^9 + 3L^2P^2f_S^2V_1n^3V_2^3(V_1^2 + 4n^2V_2^2)(5V_1^2 + 8n^2V_2^2) + \\
 &\quad 3L|P|f_SV_1^2nV_2(-8n^7V_2^7 - 2V_1^2n^5V_2^5 + \\
 &\quad \sqrt{3}\{L|P|f_S[4V_1^5n^7V_2^7 - 256L^3|P|^3f_S^3(V_1^2 + n^2V_2^2)^3 - \\
 &\quad L|P|f_SV_1^2n^4V_2^4(V_1^2 + 4n^2V_2^2)(13V_1^2 + 4n^2V_2^2) + \\
 &\quad 32L^2P^2f_S^2nV_1V_2(V_1^2 + n^2V_2^2)^2(V_1^2 + 4n^2V_2^2)\}^{\frac{1}{2}}) + \\
 &\quad 16L^3|P|^3f_S^3(V_1^2 + n^2V_2^2)^2(V_1^2 - 8n^2V_2^2)], \\
 e_{a,4} &= \frac{\sqrt[3]{2}}{3\sqrt[3]{e_{a,3}}f_S^2nV_2(V_1^2 + n^2V_2^2)} [4L^2P^2f_S^2(V_1^2 + n^2V_2^2)(V_1^2 + 4n^2V_2^2) + \\
 &\quad V_1^2n^6V_2^6 - 2L|P|f_SV_1n^3V_2^3(V_1^2 + 4n^2V_2^2)],
 \end{aligned}$$

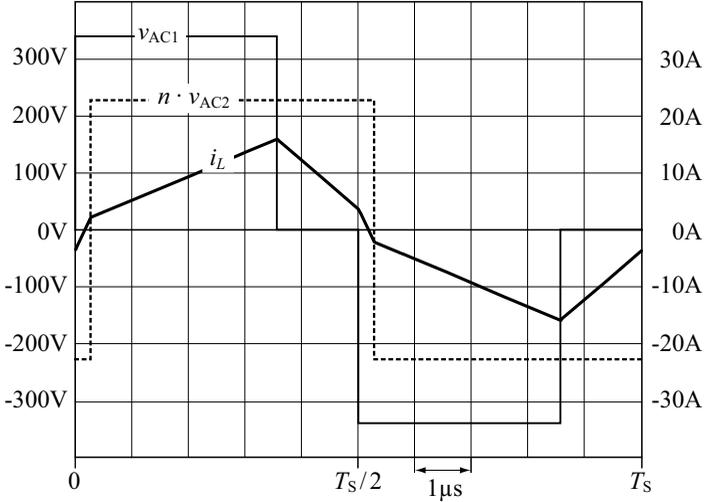


Figure 3.18: Voltage and current waveforms for minimum RMS current I_L , $V_1 = 340$ V, $V_2 = 12$ V, and $P = 2$ kW (corresponds to voltage sequence 3b in Figure 3.15); DAB parameters: $n = 19$, $L = 26.7$ μ H, $f_s = 100$ kHz.

$$e_{a,5} = -\frac{4 [n^3 V_2^3 (V_1^2 + 2n^2 V_2^2) + 2L|P|f_s V_1 (V_1^2 + n^2 V_2^2)]}{n V_2 (V_1^2 + n^2 V_2^2)^2},$$

$$e_{a,6} = \frac{f_s^2 \sqrt[3]{e_{a,3}}}{3\sqrt{2} (n V_2 V_1^4 + n^3 V_2^3 V_1^2)} + \frac{e_{a,1}^2}{4} + e_{a,4} - \frac{2e_{a,2}}{3},$$

$$e_{a,7} = \frac{1}{4} \left(3e_{a,1}^2 - 8e_{a,2} - 4e_{a,6} + \frac{e_{a,5} - e_{a,1}^3}{\sqrt{e_{a,6}}} \right),$$

$$D_{1,\text{opt}} = \frac{\frac{V_1^2 + 2n^2 V_2^2}{V_1^2 + n^2 V_2^2} + 2\sqrt{e_{a,6}} - 2\sqrt{e_{a,7}}}{4} \quad \forall P_{\Delta,\text{max}} < |P| < P_{a,\text{max}} \quad \wedge \quad V_1 > n V_2, \quad (3.45)$$

$$D_{2,\text{opt}} = \frac{1}{2} \quad \forall P_{\Delta,\text{max}} < |P| < P_{a,\text{max}} \quad \wedge \quad V_1 > n V_2, \quad (3.46)$$

$$P_{a,\text{max}} : D_{1,\text{opt}}(P_{a,\text{max}}) = \frac{1}{2} \quad \wedge \quad P_{\Delta,\text{max}} < P_{a,\text{max}} < P_{\text{PS,max}}. \quad (3.47)$$

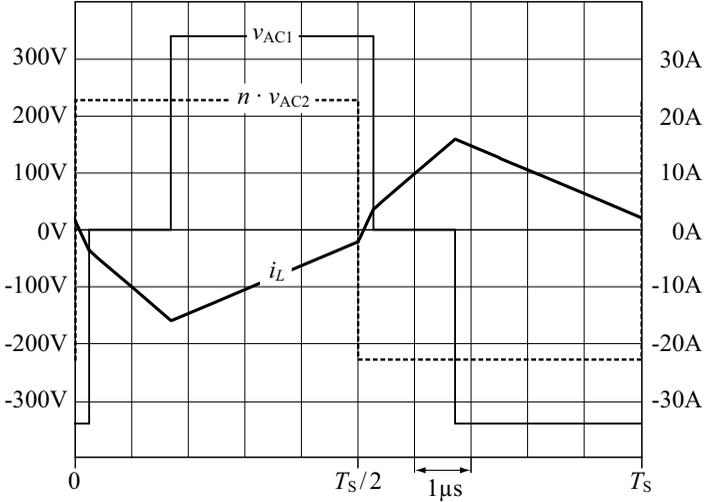


Figure 3.19: Voltage and current waveforms for minimum RMS current I_L , $V_1 = 340$ V, $V_2 = 12$ V, and $P = -2$ kW (corresponds to voltage sequence 7b in Figure 3.15); DAB parameters: $n = 19$, $L = 26.7$ μ H, $f_s = 100$ kHz.

For $P_{\Delta, \max} < |P| < P_{b, \max}$, $D_{1, \text{opt}}$ and $D_{2, \text{opt}}$ are:

$$e_{b,1} = \frac{n^2 V_2^2}{V_1^2 + n^2 V_2^2} - 2,$$

$$e_{b,2} = \frac{V_1^2}{V_1^2 + n^2 V_2^2} + \frac{2L|P|f_s}{nV_1V_2},$$

$$e_{b,3} = \frac{n^3 V_2^3}{f_s^6} \left[2n^3 V_2^3 V_1^9 + 3L^2 P^2 f_s^2 n V_2 V_1^3 (4V_1^2 + n^2 V_2^2) (8V_1^2 + 5n^2 V_2^2) + \right. \\ \left. 3L|P|f_s n^2 V_2^2 V_1 (-8V_1^7 - 2n^2 V_2^2 V_1^5 + \right. \\ \left. \sqrt{3} \left\{ L|P|f_s \left[4n^5 V_2^5 V_1^7 - 256L^3 |P|^3 f_s^3 (V_1^2 + n^2 V_2^2)^3 - \right. \right. \right. \\ \left. \left. L|P|f_s n^2 V_2^2 V_1^4 (4V_1^2 + n^2 V_2^2) (4V_1^2 + 13n^2 V_2^2) + \right. \right. \\ \left. \left. 32L^2 P^2 f_s^2 n V_1 V_2 (V_1^2 + n^2 V_2^2)^2 (4V_1^2 + n^2 V_2^2) \right\}^{\frac{1}{2}} \right) + \\ \left. 16L^3 |P|^3 f_s^3 (V_1^2 + n^2 V_2^2)^2 (n^2 V_2^2 - 8V_1^2) \right],$$

$$e_{b,4} = \frac{\sqrt[3]{2}}{3\sqrt[3]{e_{b,3}} f_s^2 V_1 (V_1^2 + n^2 V_2^2)} \left[4L^2 P^2 f_s^2 (V_1^2 + n^2 V_2^2) (4V_1^2 + n^2 V_2^2) + \right.$$

$$\begin{aligned}
e_{b,5} &= -\frac{n^2 V_2^2 V_1^6 - 2L|P|f_S n V_2 V_1^3 (4V_1^2 + n^2 V_2^2)}{4 [(2V_1^2 + n^2 V_2^2) V_1^3 + 2Ln|P|f_S V_2 (V_1^2 + n^2 V_2^2)]}, \\
e_{b,6} &= \frac{f_S^2 \sqrt[3]{e_{b,3}}}{\sqrt[3]{2} (3n^4 V_1 V_2^4 + 3n^2 V_1^3 V_2^2)} + \frac{e_{b,1}^2}{4} + e_{b,4} - \frac{2e_{b,2}}{3}, \\
e_{b,7} &= \frac{1}{4} \left(3e_{b,1}^2 - 8e_{b,2} - 4e_{b,6} + \frac{e_{b,5} - e_{b,1}^3}{\sqrt{e_{b,6}}} \right), \\
D_{1,\text{opt}} &= \frac{1}{2} \quad \forall \quad P_{\Delta,\text{max}} < |P| < P_{b,\text{max}} \quad \wedge \quad V_1 < n V_2, \tag{3.48}
\end{aligned}$$

$$\begin{aligned}
D_{2,\text{opt}} &= \frac{\frac{2V_1^2 + n^2 V_2^2}{V_1^2 + n^2 V_2^2} + 2\sqrt{e_{b,6}} - 2\sqrt{e_{b,7}}}{4} \\
&\quad \forall \quad P_{\Delta,\text{max}} < |P| < P_{b,\text{max}} \quad \wedge \quad V_1 < n V_2, \tag{3.49}
\end{aligned}$$

$$P_{b,\text{max}} : D_{2,\text{opt}}(P_{b,\text{max}}) = \frac{1}{2} \quad \wedge \quad P_{\Delta,\text{max}} < P_{b,\text{max}} < P_{\text{PS,max}}; \tag{3.50}$$

Figure 3.20 depicts the resulting duty cycles $D_{1,\text{opt}}$ and $D_{2,\text{opt}}$ for $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, and $0 < P < P_{\text{PS,max}}$ [cf. (3.15)]. With given $D_1 = D_{1,\text{opt}}$ and $D_2 = D_{2,\text{opt}}$, the required phase shift angle φ is calculated according to Table 3.4.

The upper limit for L is determined with (3.15), since phase shift modulation is employed for maximum power.

The transformer RMS currents obtained with the optimized modulation scheme are depicted in Figure 3.21 for the DAB with $n = 19$ and $L = 26.7 \mu\text{H}$, i.e. the DAB designed for phase shift modulation, Appendix A.2, in order to allow for a straight comparison with the results obtained for phase shift modulation. At $P = 2 \text{ kW}$, the LV side transformer RMS current is between 113 A (at $V_1 = 335 \text{ V}$, $V_2 = 16 \text{ V}$) and 215 A ($V_1 = 450 \text{ V}$, $V_2 = 11 \text{ V}$); at $P = 1 \text{ kW}$, the LV side transformer RMS current is between 65 A ($V_1 = 311 \text{ V}$, $V_2 = 16 \text{ V}$) and 128 A ($V_1 = 450 \text{ V}$, $V_2 = 11 \text{ V}$). Compared to phase shift modulation, the maximum RMS current is 24% lower (phase shift modulation: 283 A) and the respective maximum conduction losses are 42% lower. Compared to the combined triangular and trapezoidal current mode modulation scheme (maximum RMS current: 235 A), the maximum RMS current is 8.5% lower and, accordingly, 16% lower maximum conduction losses result. Table 3.7 lists the minimum and maximum transformer RMS current values, I_L , for the discussed modulation schemes.

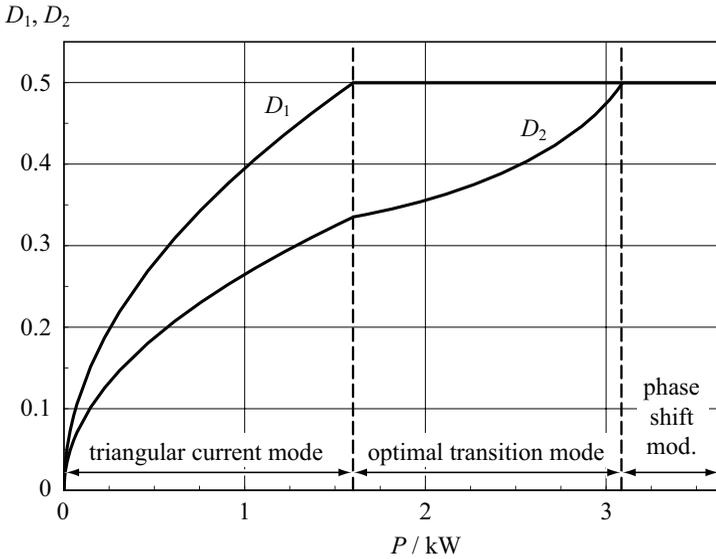


Figure 3.20: Duty cycles D_1 and D_2 , which minimize the inductor RMS current for $V_1 = 340 \text{ V}$ and $V_2 = 12 \text{ V}$: at low power levels, the triangular current mode modulation is optimal, at medium power levels, D_1 and D_2 are calculated according to (3.45) and (3.46), and at high power levels, phase shift modulation is optimal. Employed DAB parameters: $n = 19$, $L = 26.7 \text{ } \mu\text{H}$, $f_s = 100 \text{ kHz}$.

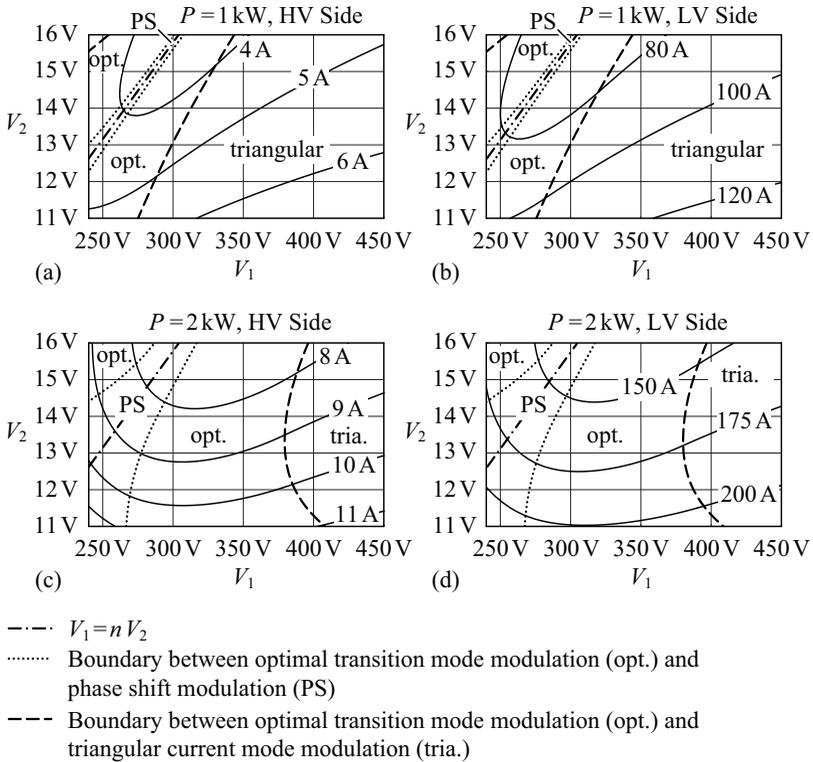


Figure 3.21: Transformer RMS currents for the modulation scheme with minimum inductor RMS current and operation within the specified voltage ranges: (a) HV side and (b) LV side transformer currents for $P = 1\text{ kW}$, (c) HV side and (d) LV side transformer currents for $P = 2\text{ kW}$; $n = 19$, $L = 26.7\ \mu\text{H}$, $f_s = 100\text{ kHz}$.

	I_L	$n I_L$	Respective operating conditions			
			V_1	V_2	n	L
Phase shift modulation						
min. I_L for $P = 1$ kW	3.4 A	65 A	311 V	16 V	19	26.7 μ H
min. I_L for $P = 2$ kW	7.0 A	134 A	333 V	16 V	19	26.7 μ H
max. I_L for $P = 1$ kW	13.5 A	256 A	450 V	11 V	19	26.7 μ H
max. I_L for $P = 2$ kW	14.9 A	283 A	450 V	11 V	19	26.7 μ H
Solely triangular current mode modulation						
min. I_L for $P = 1$ kW	7.2 A	87 A	240 V	16 V	12	8.8 μ H
min. I_L for $P = 2$ kW	12.2 A	146 A	240 V	16 V	12	8.8 μ H
max. I_L for $P = 1$ kW	12.0 A	144 A	450 V	11 V	12	8.8 μ H
max. I_L for $P = 2$ kW	20.1 A	242 A	450 V	11 V	12	8.8 μ H
Combined triangular and trapezoidal current mode modulation						
min. I_L for $P = 1$ kW	3.4 A	65 A	308 V	16 V	19	18.7 μ H
min. I_L for $P = 2$ kW	7.0 A	134 A	323 V	16 V	19	18.7 μ H
max. I_L for $P = 1$ kW	7.3 A	140 A	450 V	11 V	19	18.7 μ H
max. I_L for $P = 2$ kW	12.4 A	235 A	450 V	11 V	19	18.7 μ H
Modulation scheme with minimum transformer and inductor RMS current						
min. I_L for $P = 1$ kW	3.4 A	65 A	311 V	16 V	19	26.7 μ H
min. I_L for $P = 2$ kW	7.0 A	133 A	335 V	16 V	19	26.7 μ H
max. I_L for $P = 1$ kW	6.7 A	128 A	450 V	11 V	19	26.7 μ H
max. I_L for $P = 2$ kW	11.3 A	215 A	450 V	11 V	19	26.7 μ H

Table 3.7: Comparison of the resulting inductor RMS currents I_L for different modulation schemes; $f_S = 100$ kHz.

3.2 DAB Model Regarding Conduction Losses

The simplified converter model (Figure 3.2) allows for basic analytical investigations on the DAB, however, compared to measurement results, the obtained expressions [e.g. the power transferred with phase shift modulation, (3.13)] may compute considerably different values, mainly due to converter losses. As for any power converter, conduction losses, switching losses, and core losses of magnetic components form the total losses, which is explicated in Chapter 4. In this Section, conduction losses are considered in order to obtain a more precise but still simple electric DAB converter model.

The idealized HV side full bridge circuit (Figure 3.22), connected to an inductive load L_1 and its copper resistance R_{Cu1} , resides in one of four possible states and applies the voltage v_{AC1} to L_1 and R_{Cu1} , according to (3.1). On the HV side, only the switch resistances R_{S1} and the copper resistance R_{Cu1} are considered;⁴ PCB conduction losses and conduction losses due to the

⁴MOSFETs form the semiconductor switches of the DAB on the HV side and on the LV side (Appendix A.2.2, Appendix A.2.3, and Appendix D) and therefore, resistors are

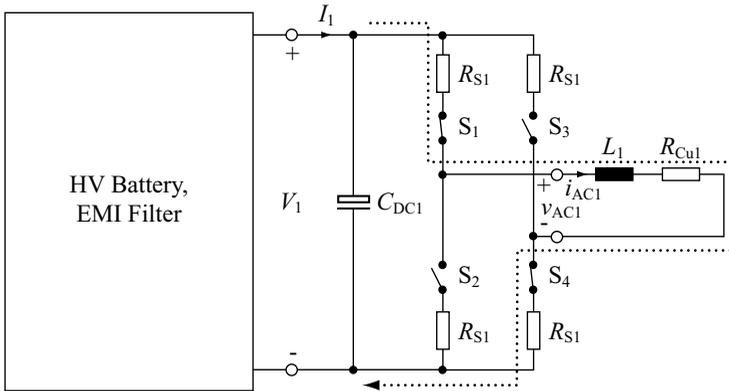


Figure 3.22: Idealized full bridge circuits, HV side; the switches S_1 to S_4 are composed of MOSFETs (Appendix A.2.2), the resistors R_{S1} represent the total of the respective MOSFET on-state resistances. With synchronous rectification and for the assumption of negligible dead time intervals, the MOSFET's body diodes never conduct and are thus neglected. The resistance R_{Cu1} models the inductor's AC (copper) resistance at f_s . The depicted full bridge is in state I (S_1 and S_4 are on); the dotted line indicates the associated current path.

capacitor's ESR are neglected.

For $v_{AC1} = V_1$, the switches S_1 and S_4 are turned on [state I in (3.1)] and thus, the inductor current path encloses $2R_{S1}$, L_1 , R_{Cu1} , C_{DC1} , the EMI filter, and the battery connected to the HV side. On the assumption of a constant voltage V_1 [i.e. negligible impedance of C_{DC1} at twice the switching frequency: $(2\pi(2f_s)C_{DC1})^{-1} \rightarrow 0$], the total resistance in series to L_1 ,

$$R_{1,I} = 2R_{S1} + R_{Cu1},$$

results for state I. A similar switch configuration exists for state IV with $v_{AC1} = -V_1$, so $R_{1,IV} = R_{1,I}$. For states II and III ($v_{AC1} \approx 0$) the switch configuration is different to states I and IV. However, according to Figure 3.22, the same resistance values result: $R_{1,II} = R_{1,III} = R_{1,I}$. Thus, for the HV side full bridge, the equivalent resistance

$$R_1 = 2R_{S1} + R_{Cu1} \quad (3.51)$$

is considered in series to L_1 .

The electric model regarding the LV side full bridge (Figure 3.23) is slightly more complex, since measurements reveal considerable PCB conduction losses on the LV side (Section 4.2). Thus, during states I and IV, the resistance values

$$R_{2,I} = R_{2,IV} = 2R_{S2} + R_{Cu2} + R_{PCB,a} + R_{PCB,b} \quad (3.52)$$

result. However, the resistances $R_{2,II}$ and $R_{2,III}$ during the freewheeling states II and III are less than $R_{2,I}$ and $R_{2,IV}$,

$$R_{2,II} = R_{2,III} = 2R_{S2} + R_{Cu2} + R_{PCB,a}. \quad (3.53)$$

Since the LV side full bridge mainly resides in states I and IV (cf. phase shift modulation) and since the difference due to $R_{PCB,b}$ is small for the considered design (at DC, $R_{PCB,b}$ is $160 \mu\Omega$, Figure 4.3, and thus, at 200 A a voltage error of 32 mV occurs), the equivalent resistance

$$R_2 = R_{2,I} = R_{2,IV} \quad (3.54)$$

is considered.

For the actual DAB converter (Figure 3.24), the copper resistances R_{Cu1} and R_{Cu2} are replaced by the respective inductor and transformer winding resistances (cf. Appendix A.2.4 and Appendix A.9):

$$R_{Cu1} = R_{L_{HV}} + R_{tr1}, \quad (3.55)$$

$$R_{Cu2} = R_{tr2}. \quad (3.56)$$

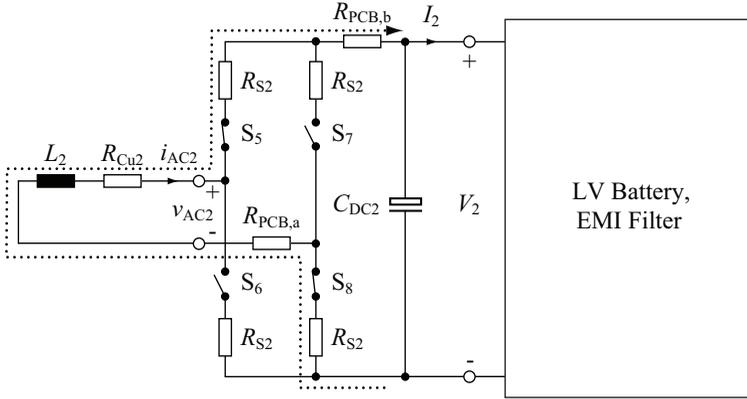


Figure 3.23: Idealized full bridge circuits, LV side; the switches S_5 to S_8 are composed of MOSFETs, the resistors R_{S2} represent the total of the respective MOSFET on-state resistances. With synchronous rectification and on the assumption of negligible dead time intervals, the MOSFET's body diodes never conduct and are thus neglected. The resistance R_{Cu2} models the inductor's AC (copper) resistance at f_s , and $R_{PCB,a}$ and $R_{PCB,b}$ model the PCB's AC resistances (Figure 4.3).

The total loss resistance, R , for the DAB depicted in Figure 3.24 results with (3.51), (3.54), (3.55), and (3.56):

$$R = R_1 + n^2 R_2 = 2R_{S1} + R_{L_{HV}} + R_{tr1} + n^2 \cdot (R_{tr2} + R_{PCB,a} + 2R_{S2} + R_{PCB,b}) \quad (3.57)$$

(Section 4 gives the values for R_{S1} , R_{S2} , $R_{PCB,a}$ and $R_{PCB,b}$, cf. Figure 4.3; in Appendix A.2.4, R_{tr1} and R_{tr2} are determined, cf. Table A.9; Appendix A.9 outlines the calculation of $R_{L_{HV}}$). Moreover, according to Figure 3.24 and without the stray inductances (transformer, PCB, switches) being considered,

$$L = L_1 + n^2 L_2 \quad (3.58)$$

results.⁵ The corresponding DAB converter model considers conduction losses and is depicted in Figure 3.25.

used to model the respective semiconductor conduction losses; the limitation of the on-state voltage due to the MOSFET's body diodes during reverse current conditions is neglected. If IGBTs are selected, the forward voltage drops of the IGBTs, V_s , and of the respective free-wheeling diodes, V_d , need to be considered separately [103].

⁵The more detailed DAB converter model discussed in Section 3.3 includes the different parasitic stray inductances, besides the transformer magnetizing inductance.

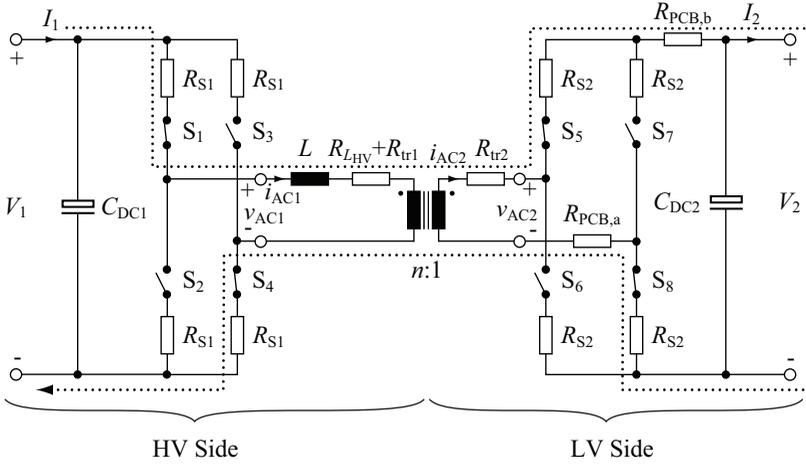


Figure 3.24: DAB converter with idealized full bridges; the resistors R_{S1} and R_{S2} represent the total of the respective MOSFET on-state resistances, $R_{L_{HV}}$ models the AC (copper) resistance of the inductor at f_S , R_{tr1} and R_{tr2} model the respective AC resistances of the primary and secondary transformer windings (cf. Appendix A.2.4 and Table A.9), and $R_{PCB,a}$ and $R_{PCB,b}$ model the PCB’s AC resistances (Figure 4.3).

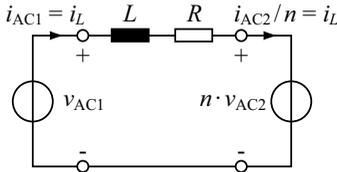


Figure 3.25: Improved DAB model, which considers conduction losses.

3.2.1 Inductor Current and Power Transfer

The voltage v_R [cf. (3.2)], applied to the series connection of L and R , generates the current

$$i_L(t_1) = i_L(t_0) + \frac{1}{L} \int_{t_0}^{t_1} [v_R(t) - i_L(t)R] dt \quad \forall \quad t_0 < t_1 \quad (3.59)$$

at the time t_1 , starting with an initial current $i_L(t_0)$ at t_0 . For constant supply voltages V_1 and V_2 and ideal full bridges, the inductor current

$$i_L(t_1) = e^{-\frac{T_1}{\tau}} i_L(t_0) + \left(1 - e^{-\frac{T_1}{\tau}}\right) \frac{v_R(t_{0+})}{R}, \quad (3.60)$$

$$T_1 = t_1 - t_0, \quad \tau = L/R, \quad (3.61)$$

results.

With rectangular voltages v_{AC1} and v_{AC2} , the calculation of P_1 and P_2 is again carried out with piecewise integration of (3.60), using (3.5) and (3.6); e.g. for phase shift modulation (Figure 3.4), P_1 and P_2 are calculated with:

$$P_1 = \frac{2}{T_S} \left(V_1 \int_0^{T_\varphi} i_L(t) dt + V_1 \int_{T_\varphi}^{T_S/2} i_L(t) dt \right) \text{ and} \quad (3.62)$$

$$P_2 = \frac{2}{T_S} \left(-n V_2 \int_0^{T_\varphi} i_L(t) dt + n V_2 \int_{T_\varphi}^{T_S/2} i_L(t) dt \right) \quad (3.63)$$

[for the assumption of half-cycle symmetry, cf. (3.10)]. Thus, with constant voltages V_1 and V_2 , the solution to the piecewise average inductor current is needed:

$$\int_{t_0}^{t_1} i_L(t) dt = \frac{v_R(t_{0+})}{R} \cdot T_1 + \tau \cdot \left(i_L(t_0) - \frac{v_R(t_{0+})}{R} \right) \cdot \left(1 - e^{-\frac{T_1}{\tau}} \right) \quad (3.64)$$

[using (3.61)].

Besides P_1 and P_2 , the inductor RMS current, I_L , is an important quantity with respect to the dissipated power (cf. Section 4.1). Its calculation as well requires piecewise integration, e.g. for the current waveform depicted in Figure 3.4:

$$I_L = \sqrt{\frac{2}{T_S} \left[\int_0^{T_\varphi} i_L(t)^2 dt + \int_{T_\varphi}^{T_S/2} i_L(t)^2 dt \right]}. \quad (3.65)$$

The solutions to the integrals employed in (3.65) are obtained as

$$\begin{aligned} \int_{t_0}^{t_1} i_L(t)^2 dt = & \\ & \tau \cdot \left[\frac{i_L(t_0)^2}{2} + \frac{i_L(t_0) v_R(t_{0+})}{R} + \left(\frac{T_1}{\tau} - \frac{3}{2} \right) \cdot \left(\frac{v_R(t_{0+})}{R} \right)^2 - \right. \\ & \left. 2 \cdot \frac{v_R(t_{0+})}{R} \cdot \left(i_L(t_0) - \frac{v_R(t_{0+})}{R} \right) \cdot e^{-\frac{T_1}{\tau}} - \right. \\ & \left. \frac{1}{2} \cdot \left(i_L(t_0) - \frac{v_R(t_{0+})}{R} \right)^2 \cdot e^{-\frac{2T_1}{\tau}} \right] \quad (3.66) \end{aligned}$$

and (3.61).

With the DAB model with conduction losses, the steady-state values of P_1 , P_2 , and I_L are always calculated based on (3.64) and (3.66), independent on the employed modulation scheme. However, the inductor current at $t = 0$ must be known in order to evaluate P_1 , P_2 , and I_L [i.e. (3.62), (3.63), and (3.65) for phase shift modulation with $0 < T_\varphi < T_S/2$, cf. Figure 3.4]. On the assumption of half-cycle symmetry, k different time intervals [e.g. $k = 3$ in Figure 3.7, cf. (3.7)], $t_0 = 0$, and with (3.61), the general expression

$$i_{L,0} = -\frac{i_L(T_S/2)|_{i_L(0)=0}}{1 + \prod_{i=1}^k e^{-T_i/\tau}} \quad (3.67)$$

is derived for the steady-state inductor current $i_{L,0} = i_L(t = t_0 = 0)$. In (3.67), $i_L(T_S/2)|_{i_L(0)=0}$ is the inductor current that results after a half-cycle if the current at the beginning of the half-cycle, $i_L(0)$, was zero and T_i is the duration of the i -th time interval.

3.2.2 Implications on the Modulation Schemes

Phase Shift Modulation

With phase shift modulation, two different time intervals occur during one half-cycle (cf. Section 3.1.2) and the inductor current

$$\begin{aligned} i_L(t) &= e^{-\frac{t}{\tau}} i_{L,0} + \left(1 - e^{-\frac{t}{\tau}}\right) \frac{V_1 + nV_2}{R}, & \forall \quad 0 < t < T_\varphi, \\ i_L(t) &= e^{-\frac{t-T_\varphi}{\tau}} i_L(T_\varphi) + \left(1 - e^{-\frac{t-T_\varphi}{\tau}}\right) \frac{V_1 - nV_2}{R}, & \forall \quad T_\varphi < t < T_S/2. \end{aligned} \quad (3.68)$$

results [$i_{L,0}$ is calculated with (3.67)].

Due to the losses $R \cdot I_L^2$, different power values P_1 and P_2 result. With (3.4), (3.5), (3.6), (3.60), (3.61) and (3.67), the expressions

$$\begin{aligned} P_{\text{in}} &= \left\{ \frac{(V'_{\text{in}})^2}{R} \left[1 - 4\tau f_S \tanh\left(\frac{1}{4\tau f_S}\right) \right] - \right. \\ &\quad \frac{V'_{\text{in}} V'_{\text{out}}}{R} \left[1 - \frac{2|\varphi|}{\pi} + 4\tau f_S \sinh\left(\frac{|\varphi|}{2\pi\tau f_S}\right) \right] - \\ &\quad \frac{4V'_{\text{in}} V'_{\text{out}} \tau f_S}{R} \left[2 \sinh\left(\frac{|\varphi|}{4\pi\tau f_S}\right) \sinh\left(\frac{|\varphi|}{4\pi\tau f_S}\right) \right] + \\ &\quad \left. \frac{4V'_{\text{in}} V'_{\text{out}} \tau f_S}{R} \left[e^{\frac{|\varphi|}{2\pi\tau f_S}} \tanh\left(\frac{1}{4\tau f_S}\right) \right] \right\} \cdot \text{sgn}(\varphi) \end{aligned} \quad (3.69)$$

and

$$\begin{aligned}
 P_{\text{out}} = & \left\{ \frac{(V'_{\text{out}})^2}{R} \left[4\tau f_S \tanh\left(\frac{1}{4\tau f_S}\right) - 1 \right] + \right. \\
 & \frac{V'_{\text{in}} V'_{\text{out}}}{R} \left[1 - \frac{2|\varphi|}{\pi} + 4\tau f_S \sinh\left(\frac{|\varphi|}{2\pi\tau f_S}\right) \right] - \\
 & \frac{4V'_{\text{in}} V'_{\text{out}} \tau f_S}{R} \left[2 \sinh\left(\frac{|\varphi|}{4\pi\tau f_S}\right) \sinh\left(\frac{|\varphi|}{4\pi\tau f_S}\right) \right] - \\
 & \left. \frac{4V'_{\text{in}} V'_{\text{out}} \tau f_S}{R} \left[e^{-\frac{|\varphi|}{2\pi\tau f_S}} \tanh\left(\frac{1}{4\tau f_S}\right) \right] \right\} \cdot \text{sgn}(\varphi)
 \end{aligned} \tag{3.70}$$

result for phase shift modulation, with

$$\left. \begin{aligned}
 V'_{\text{in}} &= V_1 \\
 V'_{\text{out}} &= n V_2 \\
 P_{\text{in}} &= P_1 \\
 P_{\text{out}} &= P_2
 \end{aligned} \right\} \text{power transfer HV} \rightarrow \text{LV} (\varphi > 0),$$

$$\left. \begin{aligned}
 V'_{\text{in}} &= n V_2 \\
 V'_{\text{out}} &= V_1 \\
 P_{\text{in}} &= P_2 \\
 P_{\text{out}} &= P_1
 \end{aligned} \right\} \text{power transfer LV} \rightarrow \text{HV} (\varphi < 0).$$
(3.71)

Figure 3.26 depicts P_1 and P_2 for the DAB with $L = 26.7 \mu\text{H}$, $R = 0.76 \Omega$ (according to the total conduction losses detailed in Sections 4.1 and 4.2), $n = 19$, $V_1 = 340 \text{ V}$, and $V_2 = 12 \text{ V}$. Obviously, maximum P_1 and P_2 are not obtained for $\varphi = \pm\pi/2$. Even more, the phase shift angle for maximum $|P_1|$, $\varphi_{1,\text{max}}$, is different to the phase shift angle $\varphi_{2,\text{max}}$ for maximum $|P_2|$. Depending on the power transfer direction, $\varphi_{1,\text{max}}$ and $\varphi_{2,\text{max}}$ are:

$$\text{HV} \rightarrow \text{LV}: \varphi_{1,\text{max},\text{A}} = \frac{2\pi f_S L \cdot \ln\left(\frac{1+e^{\frac{R}{2L f_S}}}{2}\right)}{R}, \quad \varphi_{2,\text{max},\text{A}} = \pi - \varphi_{1,\text{max},\text{A}},$$

$$\text{LV} \rightarrow \text{HV}: \varphi_{2,\text{max},\text{B}} = -\frac{2\pi f_S L \cdot \ln\left(\frac{1+e^{\frac{R}{2L f_S}}}{2}\right)}{R}, \quad \varphi_{1,\text{max},\text{B}} = -\pi - \varphi_{2,\text{max},\text{B}}.$$
(3.72)

The technically useful range for φ is $\varphi_{1,\text{max},\text{B}} < \varphi < \varphi_{2,\text{max},\text{A}}$. Outside these limits, the output power, P_{out} , decreases with increasing $|\varphi|$.

No closed-form expression exists for the phase shift angle φ with respect to a certain output power. Thus, φ is obtained with (3.70) using a numerical solver.

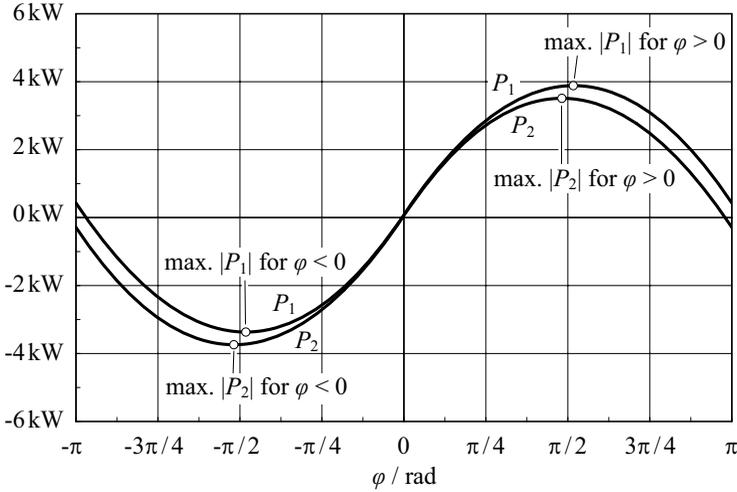


Figure 3.26: Transferred power for the DAB designed in Section A.2, phase shift modulation, $V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$, $n = 19$, $L = 26.7\text{ }\mu\text{H}$, and $R = 0.76\text{ }\Omega$ (according to the total conduction losses detailed in Sections 4.1 and 4.2). Due to the conduction losses, different power levels P_1 and P_2 occur and the maxima of $|P_1|$ and $|P_2|$ occur for $\varphi \neq \pm\pi/2$ [cf. (3.72)].

Due to the conduction losses, the RMS value of the inductor current, I_L , depends on the direction of power transfer (Figure 3.27). Further, a slightly higher maximum RMS current of 293 A occurs at $V_1 = 450\text{ V}$, $V_2 = 11\text{ V}$, and $P_1 = -2\text{ kW}$, compared to the lossless DAB model (283 A, Figure 3.6).

Alternative Modulation Schemes

For the triangular and trapezoidal current mode modulation schemes (cf. Section 3.1.3), closed-form expressions exist for the duty cycles D_1 and D_2 with respect to the phase shift angle φ ; however, no closed-form expression exists for the phase shift angle φ , required to obtain a certain output power [i.e. P_2 or P_1 depending on the direction of power transfer, cf. (3.71)]. In general, for the derivation of D_1 , D_2 , and φ , six different cases need to be considered:

1. triangular current mode modulation with $V_1 > n V_2$, HV \rightarrow LV,
2. triangular current mode modulation with $V_1 < n V_2$, HV \rightarrow LV,

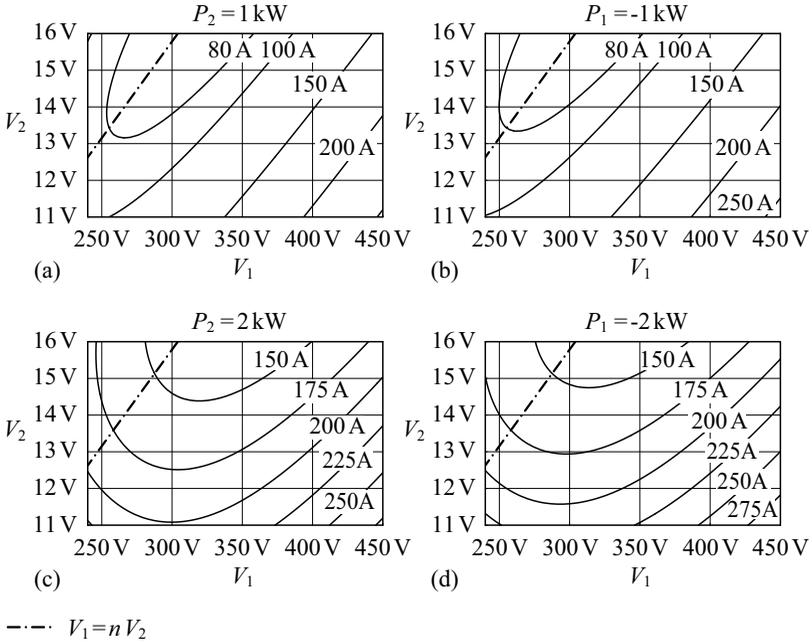


Figure 3.27: LV side transformer RMS currents for phase shift modulation and operation within the specified voltage ranges: (a) $P_2 = 1 \text{ kW}$, (b) $P_1 = -1 \text{ kW}$, (c) $P_2 = 2 \text{ kW}$, and (d) $P_1 = -2 \text{ kW}$; $n = 19$, $L = 26.7 \mu\text{H}$, and $R = 0.76 \Omega$.

3. trapezoidal current mode modulation, HV \rightarrow LV,
4. triangular current mode modulation with $V_1 > nV_2$, LV \rightarrow HV,
5. triangular current mode modulation with $V_1 < nV_2$, LV \rightarrow HV,
6. trapezoidal current mode modulation, LV \rightarrow HV.

However, due to the symmetry of the regarded DAB model, only one power transfer direction needs to be investigated (e.g. HV \rightarrow LV), and the equations for the reverse direction are obtained with

$$\begin{bmatrix} V_1 & V_2 & P_1 & P_2 & D_1 & D_2 & \varphi \end{bmatrix}^T \rightarrow \begin{bmatrix} nV_2 & V_1/n & -P_2 & -P_1 & D_2 & D_1 & -\varphi \end{bmatrix}^T. \quad (3.73)$$

Triangular Current Mode Modulation with $V_1 > nV_2$ (HV \rightarrow LV).

With the considered DAB model and with given phase shift angle φ , the duty cycles D_1 and D_2 become:

$$D_1 = \tau f_S \ln \left(\frac{V_1 - nV_2}{V_1 - nV_2 e^{\varphi/(\tau\pi f_S)}} \right), \quad (3.74)$$

$$D_2 = D_1 + \varphi/\pi. \quad (3.75)$$

The maximum phase shift angle for this operation mode is:

$$\varphi_{\Delta, \max, A} = \frac{\pi}{2} \left[1 - 2\tau f_S \ln \left(\frac{V_1 - nV_2 \cdot (1 - e^{1/(2\tau f_S)})}{V_1} \right) \right]. \quad (3.76)$$

The port 1 power level P_1 , the port 2 power level P_2 , and the inductor RMS current I_L are equal to:

$$P_1 = 2f_S V_1 \int_0^{D_1/f_S} i_L(t)|_{v_R=V_1-nV_2} dt, \quad (3.77)$$

$$P_2 = 2f_S nV_2 \left[\int_0^{D_1/f_S} i_L(t)|_{v_R=V_1-nV_2} dt + \int_{D_1/f_S}^{D_2/f_S} i_L(t)|_{v_R=-nV_2} dt \right], \quad (3.78)$$

$$I_L = \sqrt{2f_S \left[\int_0^{D_1/f_S} \left(i_L(t)|_{v_R=V_1-nV_2} \right)^2 dt + \int_{D_1/f_S}^{D_2/f_S} \left(i_L(t)|_{v_R=-nV_2} \right)^2 dt \right]}. \quad (3.79)$$

With (3.64), (3.66), and $i_L(0) = 0$, closed-form expressions are feasible, though, rather complicated expressions result. Moreover, neither for P_1 nor for P_2 closed-form expressions with respect to the phase shift angle φ exist and thus, the phase shift angle required for a certain output power P_2 is obtained using a numerical solver.

Triangular Current Mode Modulation with $V_1 < nV_2$ (HV \rightarrow LV).

With given phase shift angle φ , the duty cycles D_1 and D_2 are equal to

$$D_1 = \frac{\varphi}{\pi} + \tau f_S \ln \left(\frac{V_1 e^{-\varphi/(\tau\pi f_S)} - nV_2}{V_1 - nV_2} \right) \quad \text{and} \quad (3.80)$$

$$D_2 = D_1 - \varphi/\pi; \quad (3.81)$$

the expression for the maximum phase shift angle is:

$$\varphi_{\Delta, \max, B} = \pi\tau f_S \ln \left(\frac{V_1}{nV_2} + \frac{(nV_2 - V_1) \cdot e^{1/(2\tau f_S)}}{nV_2} \right). \quad (3.82)$$

P_1 , P_2 , and I_L are calculated according to:

$$P_1 = 2f_S V_1 \left[\int_0^{D_1/f_S} i_L(t)|_{v_R=V_1} dt + \int_{D_1/f_S}^{D_2/f_S} i_L(t)|_{v_R=V_1-nV_2} dt \right], \quad (3.83)$$

$$P_2 = 2f_S nV_2 \int_{D_1/f_S}^{D_2/f_S} i_L(t)|_{v_R=V_1-nV_2} dt, \quad (3.84)$$

$$I_L = \sqrt{2f_S \left[\int_0^{D_1/f_S} \left(i_L(t)|_{v_R=V_1} \right)^2 dt + \int_{D_1/f_S}^{D_2/f_S} \left(i_L(t)|_{v_R=V_1-nV_2} \right)^2 dt \right]} \quad (3.85)$$

with (3.64), (3.66), and $i_L(0) = 0$ and again, a numerical solver is needed in order to determine the phase shift angle φ required to obtain a certain output power P_2 .

Trapezoidal Current Mode Modulation (HV \rightarrow LV). With given phase shift angle φ , the duty cycles

$$D_1 = \frac{1}{2} - \frac{\varphi}{\pi} + \tau f_S \ln \left(\frac{V_1 + nV_2 e^{1/(2\tau f_S)}}{V_1 e^{(1/2-\varphi/\pi)/(\tau f_S)} + nV_2} \right) \quad \text{and} \quad (3.86)$$

$$D_2 = \frac{1}{2} - \frac{\varphi}{\pi} + \tau f_S \ln \left(\frac{V_1 + nV_2 e^{-(1/2-\varphi/\pi)/(\tau f_S)}}{V_1 e^{-1/(2\tau f_S)} + nV_2} \right) \quad (3.87)$$

result; maximum power transfer is achieved for

$$\varphi_{\Delta, \max} = \tau \pi f_S \left\{ \ln \left[V_1 (2nV_2 - V_1) + nV_2 (nV_2 - V_1) e^{1/(2\tau f_S)} \right. \right. \\ \left. \left. + \left(\left(V_1^2 + nV_1 V_2 (e^{1/(2\tau f_S)} - 2) - (nV_2)^2 e^{1/(2\tau f_S)} \right)^2 \right. \right. \\ \left. \left. + 4nV_1^2 V_2 \left(V_1 + nV_2 e^{1/(2\tau f_S)} \right) \right)^{\frac{1}{2}} \right] \right. \\ \left. - \ln (2nV_2) - \ln \left(V_1 e^{-1/(2\tau f_S)} + nV_2 \right) \right\}. \quad (3.88)$$

P_1 , P_2 , and I_L are calculated according to:

$$P_1 = 2f_S V_1 \left[\int_0^{(\frac{1}{2}-D_2)/f_S} i_L(t)|_{v_R=V_1} dt + \int_{(\frac{1}{2}-D_2)/f_S}^{D_1/f_S} i_L(t)|_{v_R=V_1-nV_2} dt \right], \quad (3.89)$$

$$P_2 = 2f_S nV_2 \left[\int_{(\frac{1}{2}-D_2)/f_S}^{D_1/f_S} i_L(t)|_{v_R=V_1-nV_2} dt + \int_{D_1/f_S}^{1/(2f_S)} i_L(t)|_{v_R=-nV_2} dt \right], \quad (3.90)$$

$$I_L = \left\{ 2f_S \left[\int_0^{(\frac{1}{2}-D_2)/f_S} \left(i_L(t)|_{v_R=V_1} \right)^2 dt + \int_{(\frac{1}{2}-D_2)/f_S}^{D_1/f_S} \left(i_L(t)|_{v_R=V_1-nV_2} \right)^2 dt + \int_{D_1/f_S}^{1/(2f_S)} \left(i_L(t)|_{v_R=-nV_2} \right)^2 dt \right] \right\}^{\frac{1}{2}} \quad (3.91)$$

with (3.64), (3.66), and $i_L(0) = 0$; a numerical solver is needed to determine the required phase shift angle φ for a certain output power P_2 .

Resulting Inductor RMS Currents. The operation with $n = 19$, $L = 18.7 \mu\text{H}$, and $R = 0.76 \Omega$ results in the LV side referred inductor RMS currents $n I_L$ depicted in Figure 3.28: compared to the lossless model (calculated maximum RMS current: 235 A), a maximum current of 245 A is calculated for $V_1 = 450 \text{ V}$, $V_2 = 11 \text{ V}$, and $P_1 = -2 \text{ kW}$. Moreover, due to the conduction losses, different inductor RMS currents result for the different directions of power transfer.

Optimal Modulation

Similar to the modulation with minimum inductor RMS current I_L , presented in Section 3.1.3, a modulation scheme with minimum I_L exists for the R-L model of the DAB (Figure 3.25). However, due to the higher model complexity, the control parameters D_1 and D_2 , required to obtain minimum I_L for a given phase shift angle φ , need to be determined using a numerical solver. With the numerical solver, though, not only the conduction losses but additional loss components (e.g. switching losses) can be considered in order to determine the control parameters required for minimum power dissipation. Thus, a more comprehensive optimization of the employed modulation scheme is presented in Section 5.2.

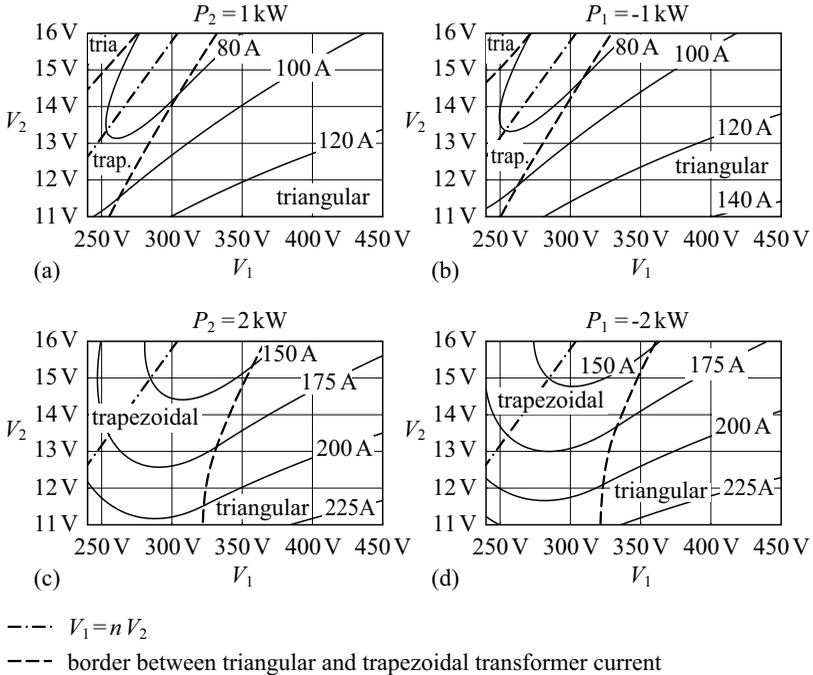


Figure 3.28: LV side transformer RMS currents for the combined triangular and trapezoidal current mode modulation and operation within the specified voltage ranges: (a) $P_2 = 1 \text{ kW}$, (b) $P_1 = -1 \text{ kW}$, (c) $P_2 = 2 \text{ kW}$, and (d) $P_1 = -2 \text{ kW}$; $n = 19$, $L = 18.7 \mu\text{H}$, and $R = 0.76 \Omega$.

3.3 Model Including the Magnetizing Inductance

The transformer magnetizing inductance L_M causes reactive power in the high frequency AC part of the DAB, in addition to the reactive power that originates from the main converter inductance L , and may considerably influence the DAB transformer currents i_{AC1} and i_{AC2} . The employed simplified transformer model depicted in Figure 3.29 disregards the effect of parasitic capacitances (winding capacitances, capacitance between primary and secondary side) and assumes equal (HV side referred) stray inductances

$$L_{tr1} = n^2 L_{tr2}; \quad (3.92)$$

the resistance values R_{tr1} and R_{tr2} are obtained from calculations and measurements (Appendix A.2.4, Table A.9). This transformer model replaces the transformer depicted in Figure 3.30. In Figure 3.30, however, two additional inductors, L_{LV} and L_{HV} , are shown: L_{LV} considers the LV side parasitic inductance of the high frequency path (Appendix A.2.4) and L_{HV} is needed in order to achieve the required total inductance L , i.e.

$$L_{HV} \approx L - L_{tr1} - n^2 (L_{tr2} + L_{LV}) \quad (3.93)$$

(for the assumption $L_{tr1} + n^2(L_{tr2} + L_{LV}) \ll L_M$). Accordingly, in the extended DAB model depicted in Figure 3.31, the inductors L_1 , L_2 , and L_M model the inductive nature of the HF network, the resistor R_M models the transformer core losses (cf. Section 4.1.2), and the resistors R_1 and R_2 con-

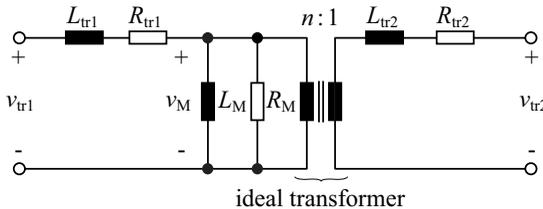


Figure 3.29: The considered transformer model with HV side stray inductance L_{tr1} , LV side stray inductance L_{tr2} and magnetizing inductance L_M . The resistors R_{tr1} and R_{tr2} model the winding losses and the resistor R_M models the core losses (cf. Appendix A.2.4 and Table A.9).

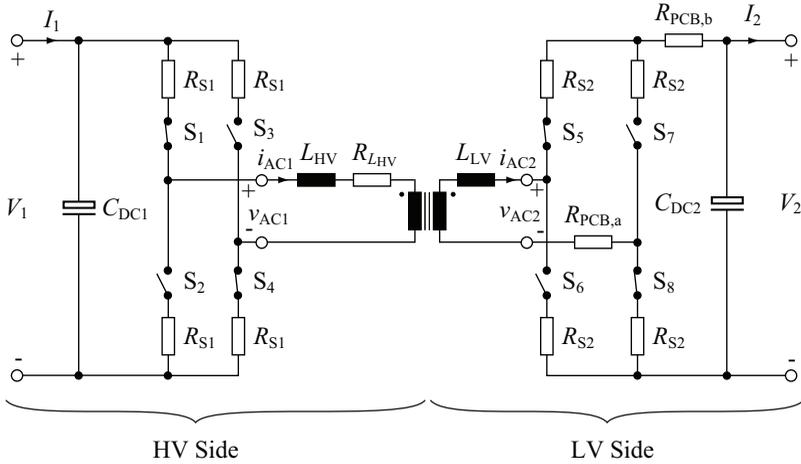


Figure 3.30: The DAB circuit used to obtain the DAB model depicted in Figure 3.31; the transformer needs to be replaced with the transformer model shown in Figure 3.29.

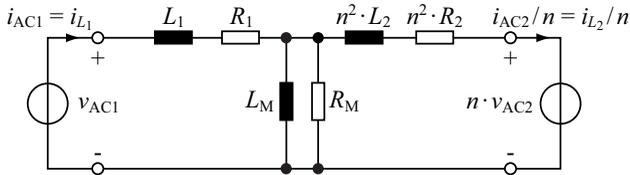


Figure 3.31: The extended DAB model, which includes the effects of the magnetizing inductance, conduction and copper losses, and core losses.

sider the conduction losses (cf. Section 3.2):

$$L_1 = L_{HV} + L_{tr1}, \quad (3.94)$$

$$R_1 = 2R_{S1} + R_{L_{HV}} + R_{tr1}, \quad (3.95)$$

$$L_2 = L_{tr2} + L_{LV}, \quad (3.96)$$

$$R_2 = R_{tr2} + 2R_{S2} + R_{PCB,a} + R_{PCB,b} \quad (3.97)$$

($R_{L_{HV}}$ is the copper resistance of the additional inductor L_{HV}).

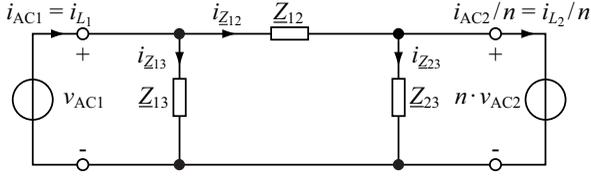


Figure 3.32: The reconfigured Delta model of the reactive HF network of the DAB.

3.3.1 Inductor Current and Power Transfer

The DAB power values at the HV port and at the LV port are again calculated using the instantaneous power values,

$$p_1(t) = v_{AC1}(t) \cdot i_{L1}(t) \quad \text{and} \quad p_2(t) = v_{AC2}(t) \cdot i_{L2}(t), \quad (3.98)$$

and the expressions (3.5) and (3.6). Obviously, different inductor currents i_{L1} and i_{L2} occur on the HV side and on the LV side, which need to be known prior to the calculation of P_1 and P_2 . However, third order differential equations need to be solved to determine $i_{L1}(t)$ and $i_{L2}(t)$; consequently, very complicated expressions result for $i_{L1}(t)$ and $i_{L2}(t)$.

In a more practical approach, the given reactive HF network is reconfigured using the Wye-delta transformation (Figure 3.32). This considerably reduces the effort to calculate i_{L1} and i_{L2} , since the voltages v_{AC1} , v_{AC2} , and $v_R = v_{AC1} - v_{AC2}$, applied to \underline{Z}_{13} , \underline{Z}_{23} , and \underline{Z}_{12} , are known in advance. The expressions for \underline{Z}_{12} , \underline{Z}_{13} , and \underline{Z}_{23} ,

$$\underline{Z}_{12} = R_1 + n^2 R_2 + s \cdot (L_1 + n^2 L_2) + \frac{n^2 (R_1 + s L_1) \cdot (R_2 + s L_2)}{R_M || (s L_M)}, \quad (3.99)$$

$$\underline{Z}_{13} = R_1 + s L_1 + (R_M || (s L_M)) \cdot \left(1 + \frac{R_1 + s L_1}{n^2 (R_2 + s L_2)} \right), \quad (3.100)$$

$$\underline{Z}_{23} = n^2 (R_2 + s L_2) + (R_M || (s L_M)) \cdot \left(1 + \frac{n^2 (R_2 + s L_2)}{R_1 + s L_1} \right), \quad (3.101)$$

however, contain higher order elements and need to be simplified. For the assumptions

$$R_1 \ll s L_1, \quad R_2 \ll s L_2, \quad R_M \gg s L_M, \quad (3.102)$$

\underline{Z}_{12} , \underline{Z}_{13} , and \underline{Z}_{23} become

$$\underline{Z}_{12} \approx R_1 + n^2 R_2 + s \cdot \left(L_1 + n^2 L_2 + \frac{n^2 L_1 L_2}{L_M} \right) = R_{12} + s L_{12}, \quad (3.103)$$

$$\underline{Z}_{13} \approx (R_1 + s L_1) \left(1 + \frac{L_M}{n^2 L_2} \right) + s L_M = R_{13} + s L_{13}, \quad (3.104)$$

$$\underline{Z}_{23} \approx n^2 (R_2 + s L_2) \left(1 + \frac{L_M}{L_1} \right) + s L_M = R_{23} + s L_{23}, \quad (3.105)$$

each being equal to a series connection of an inductor and a resistor. Consequently, the currents i_{L_1} and i_{L_2} are calculated with

$$i_{L_1} = i_{\underline{Z}_{12}} + i_{\underline{Z}_{13}} \quad \text{and} \quad i_{L_2} = n (i_{\underline{Z}_{12}} - i_{\underline{Z}_{23}}), \quad (3.106)$$

using the solutions to the first order differential equations for $i_{\underline{Z}_{12}}$, $i_{\underline{Z}_{13}}$, and $i_{\underline{Z}_{23}}$,

$$i_{\underline{Z}_{12}}(t_1) = e^{-\frac{T_1}{\tau_{12}}} i_{\underline{Z}_{12}}(t_0) + \left(1 - e^{-\frac{T_1}{\tau_{12}}} \right) \frac{v_R(t_{0+})}{R_{12}}, \quad (3.107)$$

$$i_{\underline{Z}_{13}}(t_1) = e^{-\frac{T_1}{\tau_{13}}} i_{\underline{Z}_{13}}(t_0) + \left(1 - e^{-\frac{T_1}{\tau_{13}}} \right) \frac{v_{AC1}(t_{0+})}{R_{13}}, \quad (3.108)$$

$$i_{\underline{Z}_{23}}(t_1) = e^{-\frac{T_1}{\tau_{23}}} i_{\underline{Z}_{23}}(t_0) + \left(1 - e^{-\frac{T_1}{\tau_{23}}} \right) \frac{v_{AC2}(t_{0+})}{R_{23}}, \quad (3.109)$$

$$T_1 = t_1 - t_0, \quad \tau_{12} = L_{12}/R_{12}, \quad \tau_{13} = L_{13}/R_{13}, \quad \tau_{23} = L_{23}/R_{23}. \quad (3.110)$$

Due to the discussed simplifications, a certain error results for the currents $i_{L_1}(t)$ and $i_{L_2}(t)$, illustrated in Figure 3.33 for the inductor RMS currents I_{L_1} and I_{L_2} , phase shift operation, $V_1 = 340$ V, $V_2 = 12$ V, and $P_2 = 2$ kW [$L = 26.7$ μ H, cf. (3.93), $n = 19$, $f_s = 100$ kHz]. There, for $L_M = 2.7$ mH and $R_M = 13.6$ k Ω , a relative error of -0.12% occurs for $i_{L_1}(t)$ and less than $\pm 0.01\%$ for $i_{L_2}(t)$,⁶ the error increases with decreasing L_M .

With the extended DAB model (Figure 3.31), due to the lossy components R_1 , R_2 , and R_M , different power values P_1 and P_2 are obtained, which are calculated using (3.5), (3.6) and (3.98):

$$P_1 = \frac{2}{T_S} \int_0^{T_S/2} v_{AC1}(t) i_{L_1}(t) dt \quad \text{and} \quad P_2 = \frac{2}{T_S} \int_0^{T_S/2} v_{AC2}(t) i_{L_2}(t) dt. \quad (3.111)$$

⁶ R_M is calculated for the assumption that solely $n v_{AC2}$ causes transformer core losses (cf. Appendix A.2.5). For phase shift operation and $V_2 = 12$ V, transformer core losses of 4.3 W are calculated and thus, the HV side referred resistance $R_M = 13.6$ k Ω results. The magnetizing inductance L_M is given in Appendix A.2.4.

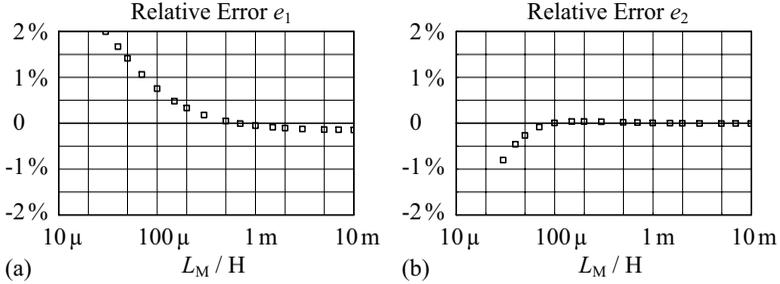


Figure 3.33: Relative errors of the calculated RMS currents I_{L_1} and I_{L_2} due to the simplifications (3.103), (3.104), and (3.105): (a) $e_1 = (I_{L_1,\text{calc}} - I_{L_1,\text{sim}})/I_{L_1,\text{sim}}$ and (b) $e_2 = (I_{L_2,\text{calc}} - I_{L_2,\text{sim}})/I_{L_2,\text{sim}}$. $I_{L_1,\text{calc}}$ and $I_{L_2,\text{calc}}$ denote the calculated inductor RMS currents that are subject to errors; the reference values $I_{L_1,\text{sim}}$ and $I_{L_2,\text{sim}}$ are obtained with a circuit simulator.

For the assumption of constant voltages V_1 and V_2 , the solutions to the integrals

$$\int_0^{T_S/2} i_{L_1} dt = \int_0^{T_S/2} i_{Z_{12}} dt + \int_0^{T_S/2} i_{Z_{13}} dt \quad \text{and} \quad (3.112)$$

$$\int_0^{T_S/2} i_{L_2} dt = \int_0^{T_S/2} i_{Z_{12}} dt - \int_0^{T_S/2} i_{Z_{23}} dt \quad (3.113)$$

are sufficient to solve for P_1 and P_2 using piecewise integration [cf. Section 3.2.1 and (3.64)]. The steady-state values

$$i_{Z_{12},0} = i_{Z_{12}}(t)|_{t=0}, \quad (3.114)$$

$$i_{Z_{13},0} = i_{Z_{13}}(t)|_{t=0}, \quad (3.115)$$

$$i_{Z_{23},0} = i_{Z_{23}}(t)|_{t=0}, \quad (3.116)$$

required to evaluate (3.112) and (3.113), are calculated with (3.67).

The RMS currents I_{L_1} and I_{L_2} are given with:

$$I_{L_1} = \sqrt{\frac{2}{T_S} \int_0^{T_S/2} i_{L_1}^2 dt} \quad \text{and} \quad I_{L_2} = \sqrt{\frac{2}{T_S} \int_0^{T_S/2} i_{L_2}^2 dt}, \quad (3.117)$$

$$\int_{t_0}^{t_1} i_{L_1}^2 dt = \int_{t_0}^{t_1} (i_{Z_{12}}^2 + 2i_{Z_{12}}i_{Z_{13}} + i_{Z_{13}}^2) dt, \quad (3.118)$$

$$\int_{t_0}^{t_1} i_{L_2}^2 dt = \int_{t_0}^{t_1} (i_{Z_{12}}^2 - 2i_{Z_{12}}i_{Z_{23}} + i_{Z_{23}}^2) dt. \quad (3.119)$$

The quadratic terms of (3.118) and (3.119) are solved with (3.66) and the solution to the remaining integral in (3.118) is:

$$\int_{t_0}^{t_1} i_{\underline{Z}_{12}} i_{\underline{Z}_{13}} dt = \frac{v_R(t_{0+})v_{AC1}(t_{0+})}{R_{12}R_{13}} \left\{ T_1 + \frac{1}{\tau_{12} + \tau_{13}} \cdot \left[\begin{aligned} &\tau_{12}^2 \left(\frac{i_{\underline{Z}_{12}}(t_0)R_{12}}{v_R(t_{0+})} - 1 \right) \right. \\ &+ \tau_{12}\tau_{13} \left(\frac{i_{\underline{Z}_{12}}(t_0)i_{\underline{Z}_{13}}(t_0)R_{12}R_{13}}{v_R(t_{0+})v_{AC1}(t_{0+})} - 1 \right) \\ &\left. + \tau_{13}^2 \left(\frac{i_{\underline{Z}_{13}}(t_0)R_{13}}{v_{AC1}(t_{0+})} - 1 \right) \right] \\ &- \tau_{12} \left(\frac{i_{\underline{Z}_{12}}(t_0)R_{12}}{v_R(t_{0+})} - 1 \right) e^{-\frac{T_1}{\tau_{12}}} \\ &- \tau_{13} \left(\frac{i_{\underline{Z}_{13}}(t_0)R_{13}}{v_{AC1}(t_{0+})} - 1 \right) e^{-\frac{T_1}{\tau_{13}}} \\ &- \frac{\tau_{12}\tau_{13}}{\tau_{12} + \tau_{13}} \left(\frac{i_{\underline{Z}_{12}}(t_0)R_{12}}{v_R(t_{0+})} - 1 \right) \left(\frac{i_{\underline{Z}_{13}}(t_0)R_{13}}{v_{AC1}(t_{0+})} - 1 \right) e^{-T_1 \left(\frac{1}{\tau_{12}} + \frac{1}{\tau_{13}} \right)} \right\}; \end{aligned} \quad (3.120)$$

the same expression results for $\int_{t_0}^{t_1} i_{\underline{Z}_{12}} i_{\underline{Z}_{23}} dt$ with τ_{13} , R_{13} , and $v_{AC1}(t_{0+})$ being replaced by τ_{23} , R_{23} , and $v_{AC2}(t_{0+})$.

3.3.2 Implications on the Modulation Schemes

Phase Shift Modulation

Similar to Section 3.2.2, analytical expressions exist for $P_1(\varphi)$ and $P_2(\varphi)$, however, these expressions are very complicated. Moreover, no closed-form expression exists for the phase shift angle φ required to obtain a certain value for P_1 or P_2 ; for this purpose, a numerical solver is needed.

With $L_M = 2.7$ mH, the resulting inductor RMS currents (Figure 3.34) are similar to the inductor RMS currents obtained in Section 3.2.2 (Figure 3.27). The maximum RMS current is 15.5 A on the HV side and 292 A on the LV side and occurs for $V_1 = 450$ V, $V_2 = 11$ V, and $P_1 = -2$ kW.

Considerably different inductor RMS currents result if a reduced magnetizing inductance, $L_M = 200$ μ H, is employed (Figure 3.35). Compared to Figure 3.34, a reduction of the maximum current is achieved on the LV side ($I_{L_2} = 275$ A at $V_1 = 450$ V, $V_2 = 11$ V, and $P_1 = -2$ kW), however, the HV side inductor RMS current, I_{L_1} , increases (maximal 15.8 A at $V_1 = 450$ V, $V_2 = 11$ V, and $P_1 = -2$ kW). Thus, with the selected transformer turns ratio,

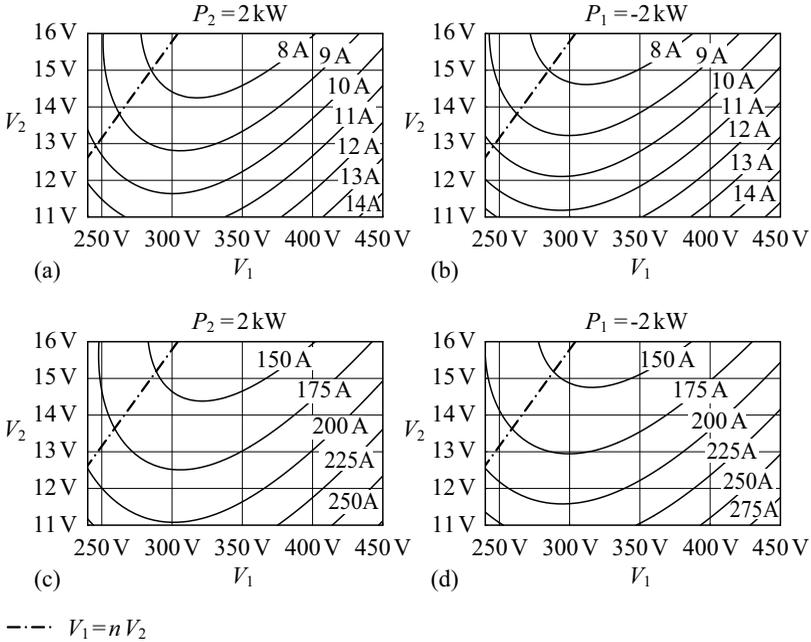


Figure 3.34: Inductor RMS currents for phase shift operation within the specified voltage ranges: (a) and (b) HV side, (c) and (d) LV side; $P_2 = 2\text{ kW}$ in (a) and (c); $P_1 = -2\text{ kW}$ in (b) and (d); $n = 19$, $L = 26.7\text{ }\mu\text{H}$ [cf. (3.93)], $L_M = 2.7\text{ mH}$.

the magnetizing inductance L_M facilitates a reduced maximum value of I_{L_2} at the expense of a higher maximum value of I_{L_1} .

Alternative Modulation Schemes

For the modulation parameters D_1 , D_2 , and φ , employed for the triangular and trapezoidal current mode modulation (cf. Section 3.1.3), no closed-form expressions exist any more; D_1 , D_2 , and φ need to be determined using a numerical solver. The employed numerical solver algorithm discussed in Section 4.6.1, however, allows to include the additional effects discussed in Chapter 4 in order to increase the accuracy of the calculated modulation parameters. Therefore, the alternative modulation schemes (i.e. the triangular current mode modulation, the trapezoidal current mode modulation, and the

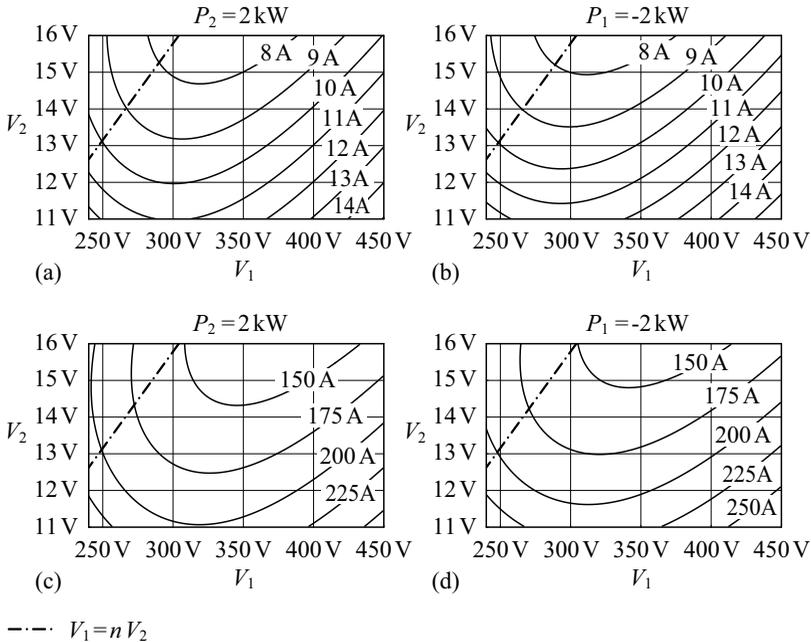


Figure 3.35: Inductor RMS currents for a reduced $L_M = 200\ \mu\text{H}$ and phase shift operation within the specified voltage ranges: (a) and (b) HV side, (c) and (d) LV side; $P_2 = 2\text{ kW}$ in (a) and (c); $P_1 = -2\text{ kW}$ in (b) and (d); $n = 19$, $L = 26.7\ \mu\text{H}$ [cf. (3.93)].

modulation scheme with minimum losses) are revisited in Chapter 5.

3.4 Conclusion

This Chapter explains the working principle of the DAB converter and details 3 different electric converter models: the lossless converter model, which facilitates a simplified calculation of the transformer currents and the transferred power, and two extended converter models which consider the impacts of the conduction losses and the magnetizing currents on the transformer current and on the converter's power transfer characteristics. Different modulation schemes are detailed; in particular, in Section 3.1.3, optimal modulation parameters D_1 , D_2 , and φ (with respect to minimum transformer RMS currents) are derived for the lossless DAB converter model.

The presented converter models enable the calculation of the transformer currents (instantaneous values and RMS value) and the calculation of the transformer flux density. The currents and the flux density calculated with the final electric model of the DAB (Figure 3.31) are input quantities to the converter loss model detailed in Chapter 4.

Chapter 4

Accurate DAB Loss Model

In order to facilitate a thorough optimization of the DAB (e.g. with respect to the employed modulation scheme and the converter design), the voltage and current stresses of the different DAB components (i.e. semiconductor switches, transformer, high current PCB, and DC capacitors) and the respective power dissipation need to be determined. Both, the voltage and the current stresses, are obtained using one of the previously presented DAB models (Chapter 3).

With a simple loss model, the calculated losses prove to be inaccurate (Section 4.1). Therefore, in Sections 4.2, 4.3, 4.4, and 4.5, different refinements of the loss model are discussed. In particular, the rapidly changing DAB transformer current is identified as the key property and needs to be determined precisely in order to allow for an accurate calculation of the converter losses (Section 4.6.1). In Section 4.6.2, a comparison of the predicted losses and the experimental results is presented and a high accuracy of the theoretical results is verified.

The converter loss model detailed in this Chapter is developed for the DAB converter designed in Appendix A.2. In summary, the basic technical data of the employed DAB converter is:

- PCB: four layer PCB, 200 μm copper on each layer,
- LV side:
 - DC capacitor: $96 \times 10 \mu\text{F}/25 \text{V}/\text{X7R}$ in parallel,
 - Switches: $8 \times \text{IRF2804}$ in parallel,

- HV side:
 - DC capacitor: $6 \times 470 \text{ nF}/630 \text{ V}$ in parallel,
 - Switches: SPW47N60CFD,
- Transformer core: two planar E58 cores (ferrite),
- Transformer turns ratio and DAB converter inductance:
 - phase shift modulation: $n = 19 : 1$, $L = 26.7 \text{ }\mu\text{H}$.
 - trapezoidal and triangular current mode modulation schemes: $n = 16 : 1$, $L = 15.5 \text{ }\mu\text{H}$.
 - minimal loss mode modulation: $n = 16 : 1$, $L = 22.4 \text{ }\mu\text{H}$.

For all calculations and measurements in this Chapter, a reference temperature ($T = 25^\circ\text{C}$) has been used to avoid that two effects, namely the electric losses and the additional influence on the total losses due to components with different temperatures, occur at the same time. With this, a clear distinction between the different losses (e.g. copper losses, conduction losses, switching losses) of the power components is achieved. The shown experimental efficiency results have therefore been obtained at 25°C with the run time of the converter being limited to 30 seconds in order to assure that no heating of the components occurs. In a future step, the discussed model can be extended with a coupled electro-thermal converter model that includes the influence of raised component temperatures on the efficiency in order to accurately calculate the expected component temperatures [104, 105].

4.1 Losses Calculated with a Simple Loss Model

The most simple loss model uses the lossless electric DAB model (Figure 3.2) to determine the converter stress values listed below.

- RMS currents in the semiconductor switches, the transformer windings, and the inductor windings;
- instantaneous currents during switching;
- peak inductor currents;
- voltage-time areas applied to the transformer core.

With known stress values, the respective losses are calculated.

4.1.1 Power Switches

The calculation of the power dissipated in the switches considers two different loss mechanisms: conduction losses and switching losses.

The RMS currents through the switches determine the respective conduction losses. In steady-state operation, every switch conducts current during half a switching cycle T_S and the waveform $i_L(t)$ (cf. Figure 3.2) repeats with negative sign after one half-cycle [i.e. $i_L(t) = -i_L(t - T_S/2)$]. Thus, each of the 4 switches on the HV side (T_1 , T_2 , T_3 , and T_4) carries the RMS current I_{S1} ,

$$I_{S1} = \frac{I_L}{\sqrt{2}}, \quad (4.1)$$

and each of the 4 switches on the LV side (T_5 , T_6 , T_7 , and T_8) carries the RMS current

$$I_{S2} = \frac{n I_L}{\sqrt{2}} \quad (4.2)$$

[I_L is the RMS value of $i_L(t)$].

According to (4.1), the switches on the HV side generate the total conduction losses

$$P_{S1,\text{cond}} = 4R_{S1}I_{S1}^2 \quad (4.3)$$

and due to (4.2) all switches on the LV side cause the total conduction losses

$$P_{S2,\text{cond}} = 4R_{S2}I_{S2}^2. \quad (4.4)$$

In power electronics, the influences of high frequency skin and proximity effects are typically neglected for power semiconductor devices. The DC switch resistances of the selected MOSFETs (cf. Appendix A.2) are obtained from the data sheet values:

$$R_{S1} = R_{DS(\text{on}),\text{SPW47N60CFD}} = 70 \text{ m}\Omega, \quad (4.5)$$

$$R_{S2} = R_{DS(\text{on}),\text{IRF2804}}/8 = 2.2 \text{ m}\Omega/8 = 275 \text{ }\mu\Omega \quad (4.6)$$

(on the LV side, 8 MOSFETs are operated in parallel; junction temperature considered for R_{S1} and R_{S2} : $T_j = 25^\circ\text{C}$).

The calculation of the switching losses is more demanding, since these not only depend on the selected power MOSFETs themselves; in particular, the surrounding parasitic components (e.g. PCB stray inductances) considerably affect the switching losses.

If ZVS (Zero Voltage Switching, Section 4.3.2) is achieved on the HV side, very low switching losses result. These can be neglected within the most simple loss model: $P_{S1,\text{sw}} = 0$. In contrast, hard switching operation of the HV MOSFETs leads to excessive semiconductor losses and must be avoided in any

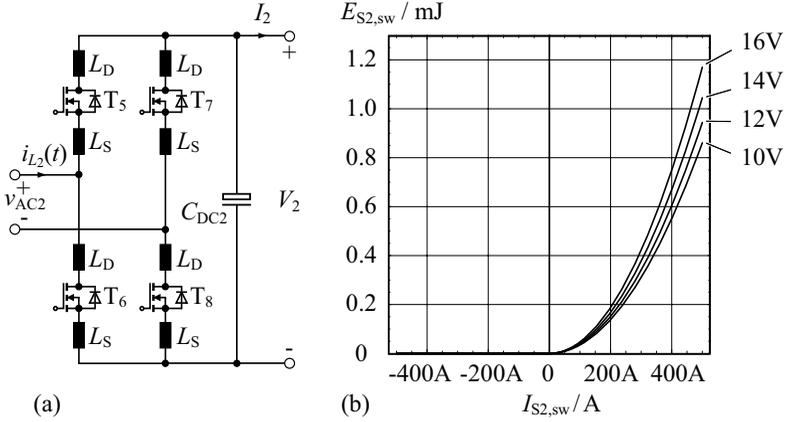


Figure 4.1: (a) LV side full bridge with the parasitic MOSFET lead inductances L_S and L_D ; (b) estimated switching losses on the LV side.

case (e.g. using advanced modulation methods, cf. Section 5, or additional circuitry [82, 106]).

On the LV side, soft switching (i.e. ZVS) is effectively not achieved, due to the energy stored in the parasitic drain and source lead inductances L_D and L_S . Accordingly, the switching losses which occur if the condition for ZVS is satisfied can be estimated with [93]

$$E_{S2,sw} = \frac{1}{2} 2(L_D + L_S) I_{S2,sw}^2 \frac{V_{pk}}{V_{pk} - V_2} \quad (4.7)$$

($I_{S2,sw}$ denotes the instantaneous MOSFET current at the switching instant). The parameters V_{pk} , L_D , and L_S , needed to evaluate (4.7), are determined with data sheet values, calculations (e.g. finite element simulations) or measurements; for the given setup, the total parasitic inductance $L_D + L_S = 2.4$ nH and the peak voltage $V_{pk} = 32.7$ V have been identified using measured switching losses. If the LV MOSFETs are operated with hard switching, comparably low switching losses occur, which is detailed in Section 4.3.3. Thus, regarding the most simple loss model, hard switching losses are neglected, there. The total estimated switching losses are shown in Figure 4.1 (b); there, $I_{S2,sw} \leq 0$ denotes hard switching and $I_{S2,sw} > 0$ denotes the operation with ZVS, cf. Section 4.3 and, in particular, Table 4.1, Figure 4.5, and Figure 4.10.

In steady-state, i_{L_2} [cf. Figure 4.1] repeats with negative sign after one half-cycle; thus, for the assumption of equal parasitic component values, T_5 and T_6 generate equal switching losses $E_{S2,a,sw}$; accordingly, T_7 and T_8 generate equal switching losses $E_{S2,b,sw}$ (for phase shift modulation $E_{S2,a,sw} = E_{S2,b,sw}$ applies). Consequently, for the full bridge depicted in Figure 4.1 (a), the total switching losses

$$P_{S2,sw} = 2f_S (E_{S2,a,sw} + E_{S2,b,sw}) \quad (4.8)$$

result.

4.1.2 Transformer, Inductor

With the elementary electric DAB model (Figure 3.2), the transformer copper losses are obtained from

$$P_{tr,cond} = (R_{tr1} + n^2 R_{tr2}) I_L^2 \quad (4.9)$$

(R_{tr1} and R_{tr2} denote the respective resistances of the HV side winding and of the LV side winding, determined at the switching frequency, cf. Appendix A.2.4 and Table A.9).

The transformer core losses are calculated with the Steinmetz equation,

$$P_{tr,core} \approx V_{tr,core} k f_S^\alpha B_{tr,peak}^\beta, \quad (4.10)$$

with the Steinmetz parameters k , α , and β (Appendix C: Table C.2 and Figure C.4), the total core volume $V_{tr,core}$, and the peak magnetic flux density $B_{tr,peak}$,

$$B_{tr,peak} = \frac{\max[\Phi_{tr}(t)] - \min[\Phi_{tr}(t)]}{2} \frac{1}{A_{tr,core}} \quad \forall \quad 0 < t \leq T_S \quad (4.11)$$

using

$$\Phi_{tr}(t) = \int_0^t \frac{v_M(t_{int})}{N_1} dt_{int} + \Phi(0) \quad (4.12)$$

(N_1 is the number of turns of the HV side winding, $A_{tr,core}$ is the core cross sectional area, and v_M denotes the voltage applied to the magnetizing inductance, i.e. $v_M \approx n v_{AC2}$ for the given DAB hardware prototype, since the predominant part of the DAB inductance L is placed on the HV side, cf. Appendix A.2.5).

The copper losses of the external inductor are calculated with

$$P_{L_{HV},cond} = R_{L_{HV}} I_L^2; \quad (4.13)$$

the calculation of the inductor copper resistance, $R_{L_{HV}}$, is outlined in Appendix A.9.4. The inductor core losses are estimated with the peak inductor current $I_{L1,peak}$ using the Steinmetz equation,

$$P_{L_{HV},core} \approx V_{L_{HV},core} k f_S^\alpha B_{L_{HV},peak}^\beta, \quad (4.14)$$

with

$$B_{L_{HV},\text{peak}} \approx \frac{\Phi_{L_{HV},\text{peak}}}{N_{L_{HV}} A_{L_{HV},\text{core}}} = \frac{L_{HV} I_{L_1,\text{peak}}}{N_{L_{HV}} A_{L_{HV},\text{core}}} \quad (4.15)$$

($N_{L_{HV}}$: number of turns, $A_{L_{HV},\text{core}}$: inductor core cross sectional area).

4.1.3 Total Losses – Predicted Efficiency

The total losses include all the discussed power losses as well as the auxiliary power required on the HV side ($P_{1,\text{aux}}$) and on the LV side ($P_{2,\text{aux}}$): the HV side auxiliary supply powers the DSP plus the HV side gate drivers and the LV side auxiliary supply provides power to the LV side gate drivers. Approximately constant power consumption has been measured ($f_S = 100$ kHz = const.),

$$P_{1,\text{aux}} = 6.2 \text{ W} \quad \text{and} \quad P_{2,\text{aux}} = 9.5 \text{ W}. \quad (4.16)$$

Thus, the total losses P_t are calculated with

$$P_t = P_{1,\text{aux}} + P_{S1,\text{cond}} + P_{S1,\text{sw}} + P_{L_{HV},\text{cond}} + P_{L_{HV},\text{core}} + P_{\text{tr},\text{cond}} + P_{\text{tr},\text{core}} + P_{S2,\text{cond}} + P_{S2,\text{sw}} + P_{2,\text{aux}}. \quad (4.17)$$

The most simple loss model evaluates all required characteristics (e.g. RMS current values) at a given input power, P_{in} , in order to include the impact of the losses on these quantities. The efficiency $\eta = P_{\text{out}}/P_{\text{in}}$ is then calculated with the output power $P_{\text{out}} = P_{\text{in}} - P_t$. The result (Figure 4.2, dotted lines) shows, that a very poor matching is obtained between the losses calculated with this simple model and measured losses. Main reasons are:

1. The converter quantities (e.g. switch RMS currents) calculated with the lossless DAB model (Figure 3.2) significantly deviate from measured values, since losses are completely neglected, there.
2. Inaccurate modeling of the conduction losses leads to a wrong estimation of the dissipated power. This occurs mainly on the LV side, where high currents at high frequencies generate considerably more losses than predicted with (4.17).
3. Switching losses cause a large part of the total losses and therefore the switching losses need to be known in detail. It further turns out, that, depending on the operating point, the switching action may change the transformer current considerably.
4. Due to losses that are not considered in the electric DAB model (e.g. switching losses, core losses), the input and output power levels P_{in} and P_{out} , calculated with the electric DAB model, are different to the input and output power levels obtained with the DAB hardware

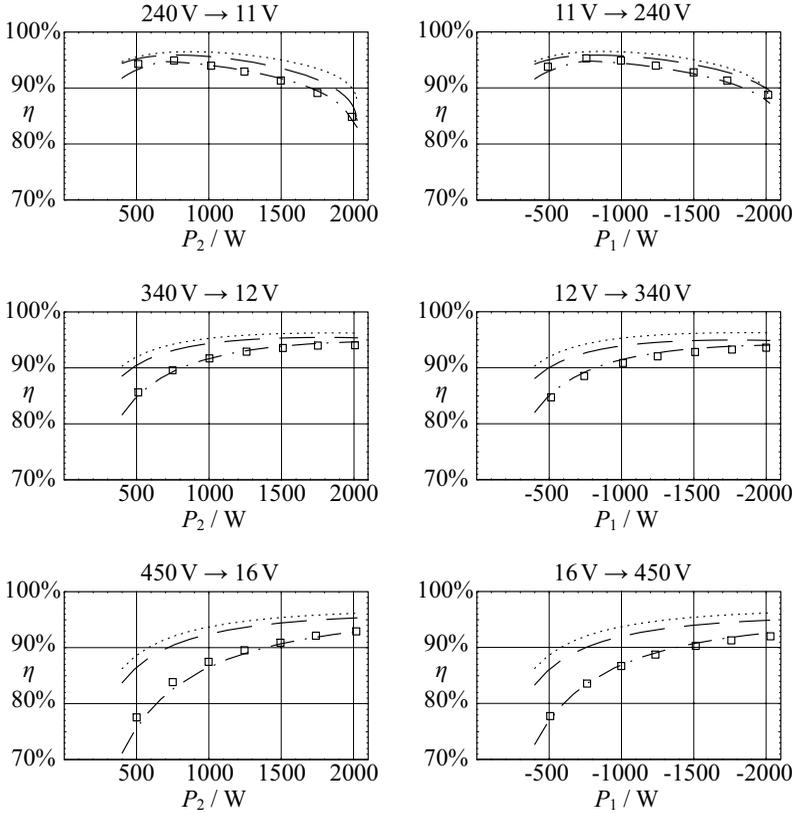


Figure 4.2: Calculated and measured DAB efficiencies for different operating points [negative power: power transfer from the LV port to the HV port, cf. (3.14)], phase shift operation, $L = 26.7 \mu\text{H}$, and $n = 19$; dotted lines: conventional analysis (Section 4.1), dashed lines: includes accurate conduction losses (Section 4.2), dashed and dotted lines: accurate conduction and switching losses (Section 4.3); the boxes, \square , indicate measured values.

prototype. Consequently, the calculation uses slightly different control parameters in order to obtain the specified output power, which results in inaccurate DAB converter quantities (e.g. switch RMS currents).

4.2 Accurate Conduction Losses, High Frequency Effects

The accurate calculation of the power dissipation employs the detailed DAB converter model depicted in Figure 3.31.

Still, the conduction losses of the HV MOSFETs are calculated using the on-state resistances of the selected MOSFETs and the RMS current I_{L_1} [cf. (4.1)]:

$$P_{S1,\text{cond}} = 4R_{S1}I_{S1}^2; \quad I_{S1} = \frac{I_{L_1}}{\sqrt{2}}. \quad (4.18)$$

Measurements confirm a considerable impact of high frequency effects on the resistances of the inductor winding, the transformer windings, the PCB, and the LV MOSFETs (Figure 4.3, Figure 4.4, and Figure A.21, Figure A.23, and Figure A.59). However, the copper losses generated by the inductor have a low proportion of the total losses and are calculated with the RMS current I_{L_1} and the DC resistance of the litz wire winding (cf. Appendix A.9.4):

$$P_{L_{\text{HV}},\text{cond}} = R_{L_{\text{HV}}}I_{L_1}^2. \quad (4.19)$$

The accurate loss model considers the current harmonics to determine the copper losses of the transformer and the PCB and the conduction losses of the LV MOSFETs:

$$P_{\text{tr}1,\text{cond}} = \sum_{k=1}^m R_{\text{tr}1}(k f_S) [I_{L_1}(k f_S)]^2 \quad (4.20)$$

$$P_{\text{tr}2,\text{cond}} = \sum_{k=1}^m R_{\text{tr}2}(k f_S) [I_{L_2}(k f_S)]^2 \quad (4.21)$$

$$P_{\text{PCB},\text{a},\text{cond}} = \sum_{k=1}^m R_{\text{PCB},\text{a}}(k f_S) [I_{L_2}(k f_S)]^2 \quad (4.22)$$

$$P_{S2,\text{cond}} = \sum_{k=0}^m R_{S2}(k f_S) [I_{S2}(k f_S)]^2 \quad (4.23)$$

$$P_{\text{PCB},\text{b},\text{cond}} = \sum_{k=0}^m R_{\text{PCB},\text{b}}(k f_S) [I_2(k f_S)]^2 \quad (4.24)$$

using

$$I_{S2} = \frac{I_{L_2}}{\sqrt{2}}. \quad (4.25)$$

[for $k > 0$, $I(k f_S)$ is the RMS value of the k -th harmonic of $i(t)$, i.e. $I(k f_S) = I_{\text{peak}}(k f_S)/\sqrt{2}$; $I(0)$ represents the DC component of $i(t)$]. The calculated

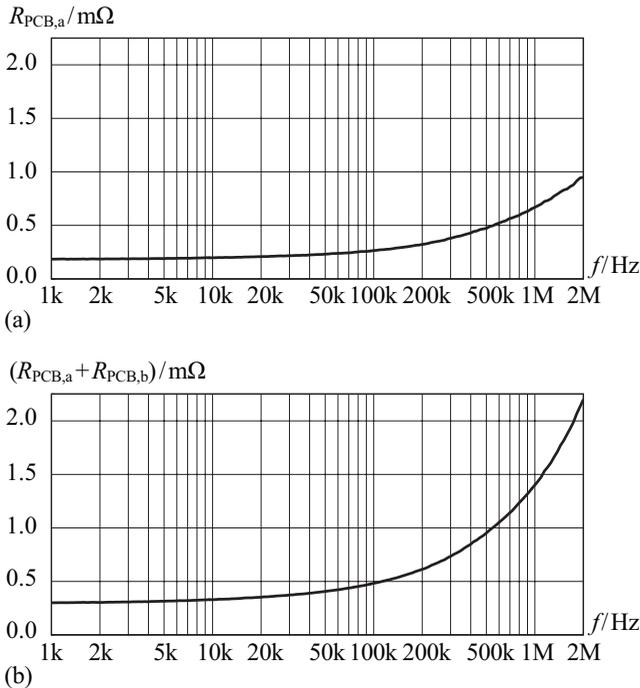


Figure 4.3: AC resistances measured at $T = 25^\circ\text{C}$ for (a) $R_{PCB,a}$ and (b) the sum $R_{PCB,a} + R_{PCB,b}$ ($R_{PCB,a}$ and $R_{PCB,b}$ are shown in Figure 3.24); the measurement employs a 13:1 measurement transformer in order to obtain reasonable impedance values for the Agilent 4294A Precision Impedance Analyzer; at 100 kHz the calculated maximum measurement error is $\pm 13\%$ for $R_{PCB,a}$ and $\pm 7\%$ for $(R_{PCB,a} + R_{PCB,b})$ (calculated according to [152]). The values shown for $R_{PCB,a}(f)$ are the average values of the resistances measured if T_5 and T_7 are replaced by a short circuit [$R_{PCB,a1}(f)$] and the resistances measured if T_6 and T_8 are replaced by a short circuit [$R_{PCB,a2}(f)$]; the measurement results obtained for $R_{PCB,a1}(f)$ and $R_{PCB,a2}(f)$ are nearly equal. The values shown for $R_{PCB,a}(f) + R_{PCB,b}(f)$ are the average values of $R_{PCB,ab1}(f)$ (T_5 and T_8 are replaced by a short circuit) and $R_{PCB,ab2}(f)$ (T_6 and T_7 are replaced by a short circuit); the measurement results obtained for $R_{PCB,ab1}(f)$ and $R_{PCB,ab2}(f)$ are nearly equal.

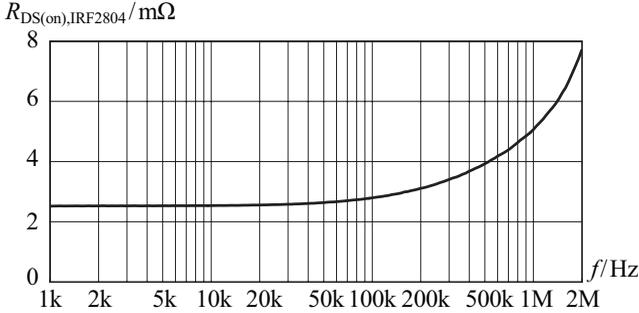


Figure 4.4: AC resistances measured at $T = 25^\circ\text{C}$ for the on-state resistance of a single IRF2804 MOSFET with a gate to source voltage of 10 V (provided from a battery); the on-state resistance is measured at the drain and source pins of the MOSFET, with a distance of 6 mm to the package; the measurement employs a 13:1 measurement transformer in order to obtain reasonable impedance values for the Agilent 4294A Precision Impedance Analyzer; at 100 kHz the calculated maximum measurement error of $R_{DS(on),IRF2804}$ is $\pm 3\%$ (calculated according to [152]).

results include the harmonic components up to $m = 20$. The calculation of the transformer winding resistances $R_{tr1}(kf_S)$ and $R_{tr2}(kf_S)$ is outlined in Appendix A.2.4 and is based on measurement values (Figure A.21, Figure A.23).

4.3 Accurate Switching Losses

4.3.1 Measurement Setups

Besides the conduction losses, the switching losses amount to a significant part of the total losses. Therefore, a precise description of the switching losses – obtained from measurements – is required in order to accurately determine the power dissipated in the semiconductor switches.

HV Side

The switching losses of a single half bridge [MOSFETs T_1 and T_2 in Figure 4.5 (a)] are measured on the final converter PCB to obtain accurate results. Moreover, the MOSFETs are mounted on a heatable metal plate (temperature controlled) in order to measure the switching losses at different

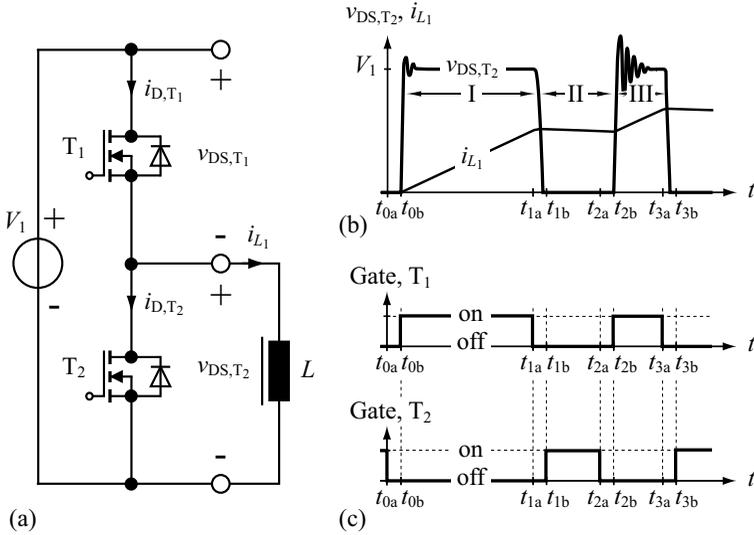


Figure 4.5: (a) Switching loss measurement setup, HV side; (b) employed double pulse signal; (c) respective gate signals for T₁ and T₂.

junction temperatures T_j (for the switching loss measurement, equal case and junction temperatures are assumed).

During the switching process, a significant amount of the stored energy may be transferred from one switch to another. Therefore, the drain currents $i_{D,T1}$ and $i_{D,T2}$ and the blocking voltages $v_{DS,T1}$ and $v_{DS,T2}$ of the respective half bridge need to be measured simultaneously in order to calculate the energies dissipated during switching:

$$E_{T1} = \int_{t_{\text{begin}}}^{t_{\text{end}}} v_{DS,T1} i_{D,T1} dt \quad \text{and} \quad E_{T2} = \int_{t_{\text{begin}}}^{t_{\text{end}}} v_{DS,T2} i_{D,T2} dt. \quad (4.26)$$

The instants t_{begin} and t_{end} denote the beginning and the end of the switching process, respectively; t_{begin} and t_{end} are selected such that a decrease of t_{begin} and an increase of t_{end} do not change the measured switching losses.

In steady-state operation each switch of the DAB converter is turned-on during one half-cycle; moreover, the signs of the transformer currents change after each half-cycle. Therefore, identical turn-on and turn-off switching operations of the MOSFETs of a single half bridge result (provided that equal

MOSFETs are used for a single half bridge). The proposed switching loss measurement correctly accounts for the generated switching losses:

- if stored energy is transferred from one MOSFET to another (soft switching, Section 4.3.2) the released energy, which has been absorbed in the preceding half-cycle, appears as negative switching losses and the absorbed energy as positive losses (Figure 4.12); for the assumption of equal MOSFETs, the difference between released and absorbed energies is the dissipated energy;
- during hard switching operation (Section 4.3.2) the measurement according to (4.26) does not account for the dissipation of the energy stored in the MOSFET that is turned on (e.g. T_1). However (4.26) includes the energy stored in the remaining MOSFET (e.g. in T_2), which will be dissipated during the switching operation of the subsequent half-cycle. Thus, for the assumption of equal MOSFETs, the correct total switching losses are measured.

The measurement of the switching losses employs the double pulse signal depicted in Figure 4.5 (b), which consists of 4 different time intervals.

- Time interval I is used to generate the required current $i_{L_1}(t_{1a})$; at $t = t_{1a}$, the condition for Zero Voltage Switching (ZVS, cf. Section 4.3.2) is fulfilled.
- During the freewheeling time interval II, the current i_{L_1} remains approximately constant.
- During time interval III, i_{L_1} increases again; at $t = t_{2b}$, the condition for hard switching is fulfilled (Section 4.3.2).
- For $t > t_{3b}$, the current i_{L_1} freewheels through T_2 and eventually decreases to zero.

In order to avoid a current shoot-through in the half bridge, a dead time, $T_{\text{deadtime}} = 200 \text{ ns}$, is used [Figure 4.5 (c)].

The switching loss measurement employs a digital oscilloscope (LeCroy WavePro 950) to determine the energy dissipated during the switching process, high voltage probes (100 : 1, 2 kV) to measure the drain-to-source voltages, and wide bandwidth current sensors to measure the drain currents. The schematics of the employed current sensors is depicted in Figure 4.6. With the employed MOSFETs (SPW47N60CFD), very fast voltage and current transients occur (cf. Figure 4.12) and therefore, the frequency response of the employed current sensors is measured using the measurement setup depicted in Figure 4.7. Figure 4.8 illustrates the equivalent circuit of this measurement

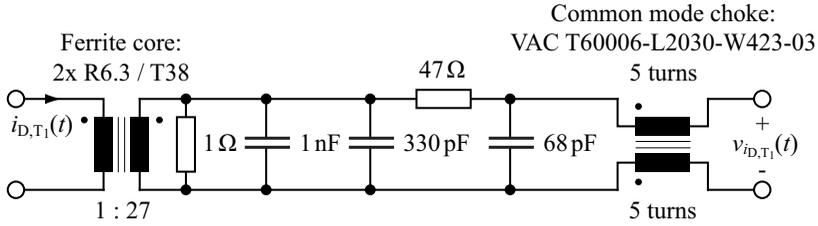


Figure 4.6: Schematics of the current sensors employed to measure the drain currents i_{D,T_1} and i_{D,T_2} . The current transformer is made of two stacked ferrite cores (R6.3, material: T38) and 27 turns (wire diameter: 0.3 mm) on the secondary side. The depicted capacitors are used to compensate the frequency response of the current sensor and a common mode choke is used to suppress common mode noise; the $47\ \Omega + 1\ \Omega$ resistors approximately provide a $50\ \Omega$ termination. The respective channels of the oscilloscope are operated with an input impedance of $50\ \Omega$.

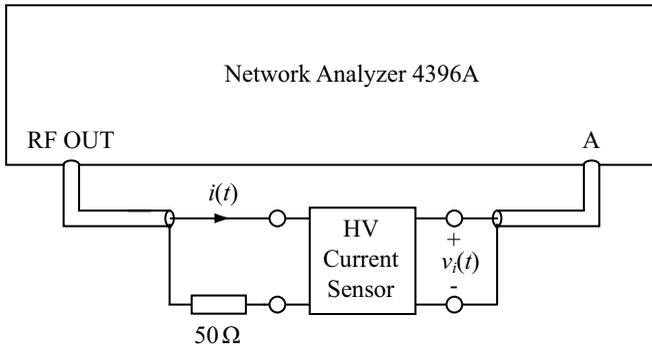


Figure 4.7: Measurement setup used to determine the frequency response of the employed current sensors: a network analyzer generates a frequency sweep and measures the output power of the current sensor at the excitation frequency (port A). Prior to the measurement, the network analyzer is calibrated with a coaxial cable of the correct length (i.e. the length of the coaxial cable connected between the oscillator and the primary side of the current sensor) in order to calibrate the magnitude measurement and to eliminate the effect of the propagation time delay caused by the input cable; the cable connected between the current sensor and port A is part of the current sensor circuit itself and thus, the respective propagation time delay needs to be considered.

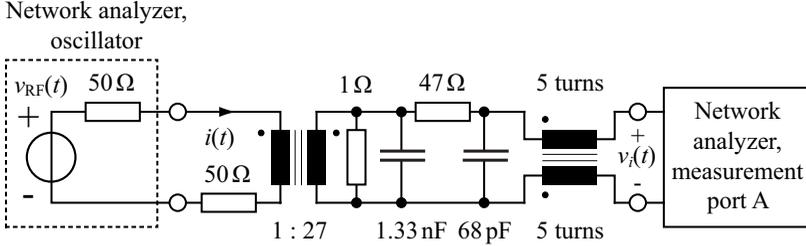


Figure 4.8: Equivalent circuit of the measurement setup depicted in Figure 4.7 including the current sensor circuit of Figure 4.6. The input impedance of measurement port A is 50 Ω .

setup: the oscillator of the network analyzer generates a frequency sweep and at the measurement port A the output voltage $v_i(t)$ is measured with respect to magnitude and phase. The primary side of the current sensor is terminated with 50 Ω since the primary side input impedance of the current sensor is much smaller than 50 Ω . The sensor gain, which is expected to be measured with this setup (oscillator power: $P_{RF} = 0$ dBmW) and with the employed current sensor, is calculated based on the equivalent circuit shown in Figure 4.8 using the RMS values I and V_i of $i(t)$ and $v_i(t)$, respectively:

$$I = \sqrt{\frac{P_{RF}}{50 \Omega}} = \sqrt{\frac{0 \text{ dBmW}}{50 \Omega}} = \sqrt{\frac{1 \text{ mW}}{50 \Omega}} = 4.47 \text{ mA}, \quad (4.27)$$

$$V_i = \frac{I}{27} \cdot 1 \Omega \cdot \underbrace{\frac{1}{2}}_{\substack{\text{resistive voltage} \\ \text{divider due to the} \\ 50 \Omega \text{ termination}}} = 82.8 \mu\text{V}, \quad (4.28)$$

$$\frac{P_i}{P_{RF}} = \frac{82.8 \mu\text{V}^2 / 50 \Omega}{1 \text{ mW}} = 137 \text{ nW} = -68.6 \text{ dB}. \quad (4.29)$$

The capacitors depicted in Figure 4.6 are used to improve the frequency response (Figure 4.9) of the employed current sensor: for frequencies below 50 MHz a gain error of less than ± 0.5 dB occurs; with a gain error of ± 3 dB being tolerated, the current sensor can be used for frequencies of up to 100 MHz.

The time skew between voltage and current measurements is measured with the same oscilloscope the switching losses are measured with. For the time skew, a value of 1 ns is determined (the current measurement slightly lags behind the voltage measurement).

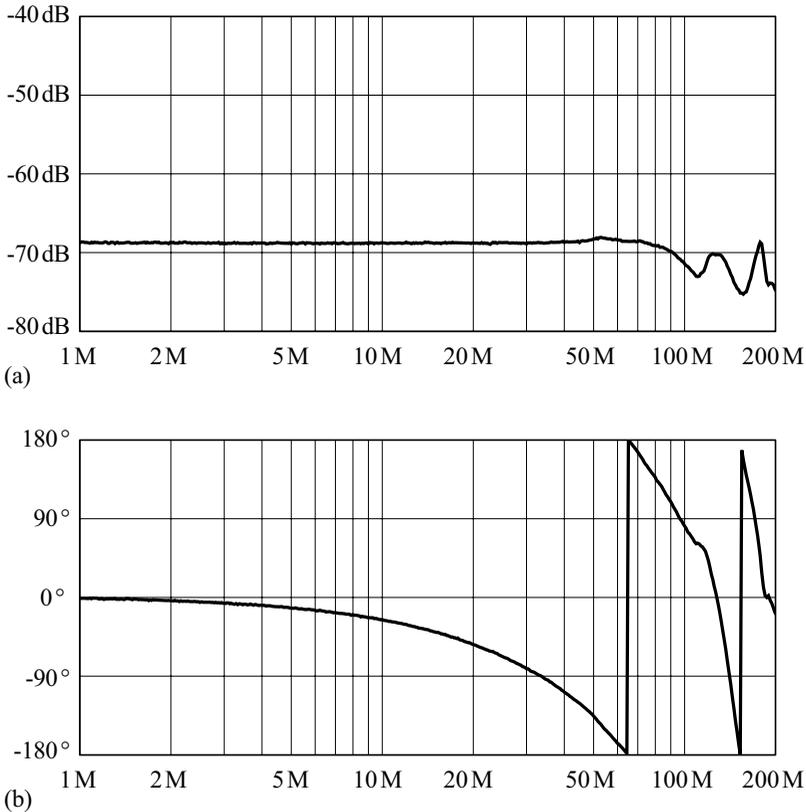


Figure 4.9: Frequency response of the current sensors (Figure 4.6) measured with the setup depicted in Figure 4.7; (a) gain response, (b) phase response.

LV Side

The LV side switching losses are measured using one of the two full bridges of the final converter with 4 MOSFETs being operated in parallel (Figure 4.10);¹ the MOSFETs are mounted on a heatable and temperature controlled metal plate. Again, the double pulse signal [cf. Figure 4.5 (b)] is employed with a dead time of 240ns. For each of the MOSFETs, the drain current and the

¹On the LV side, the final converter operates two full bridges in parallel, cf. Appendix A.2.3.

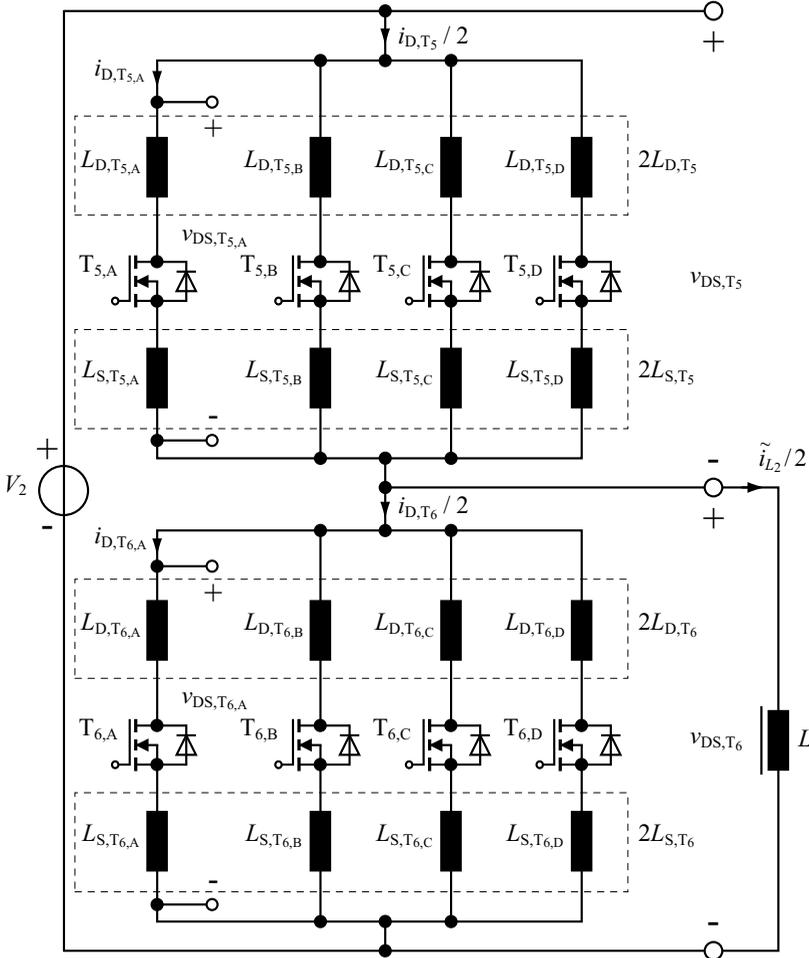


Figure 4.10: Switching loss measurement setup, LV side; for the switching loss measurement, one of the two full bridges (cf. Appendix A.2.3) is employed, i.e. 4 MOSFETs are connected in parallel to form one switch. On the assumption of equal MOSFETs $T_{5,A} \dots T_{5,D}$ and $T_{6,A} \dots T_{6,D}$, the parasitic inductances $2L_{D,T_5} = L_{D,T_{5,A}} \parallel L_{D,T_{5,B}} \parallel L_{D,T_{5,C}} \parallel L_{D,T_{5,D}}$, $2L_{S,T_5} = L_{S,T_{5,A}} \parallel L_{S,T_{5,B}} \parallel L_{S,T_{5,C}} \parallel L_{S,T_{5,D}}$ etc. result. Consequently, the total parasitic inductances are L_{D,T_5} , L_{S,T_5} , L_{D,T_6} , and L_{S,T_6} .

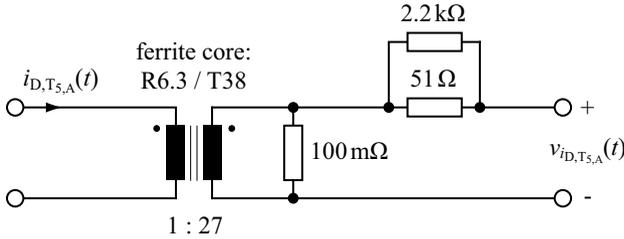


Figure 4.11: Schematics of the current sensors employed to measure the drain currents $i_{D,T_{5,A}}$, $i_{D,T_{5,B}}$, $i_{D,T_{5,C}}$, and $i_{D,T_{5,D}}$ and $i_{D,T_{6,A}}$, $i_{D,T_{6,B}}$, $i_{D,T_{6,C}}$, and $i_{D,T_{6,D}}$. The current transformer is made of a ferrite core (R6.3, material: T38) and 27 turns (wire diameter: 0.3 mm) on the secondary side. The $51\ \Omega||2.2\ \text{k}\Omega$ resistors provide a $50\ \Omega$ termination. The respective channels of the oscilloscope are operated with an input impedance of $50\ \Omega$.

drain-to-source voltage is measured simultaneously in order to determine the respective switching losses.

The switching loss measurement employs a digital oscilloscope (LeCroy WavePro 950) to determine the energy dissipated during the switching process, conventional voltage probes (10 : 1, 600 Vpk) to measure the drain-to-source voltages, and current sensors to measure the drain currents. The schematics of the employed current sensors is depicted in Figure 4.11.²

The time skew between voltage and current measurements is measured with the same oscilloscope the switching losses are measured with. For the time skew, a value of 2 ns is determined (the voltage measurement slightly lags behind the current measurement).

4.3.2 HV Side Switching: Results

Soft Switching (ZVS)

Soft switching occurs at $t = t_{1a}$ in Figure 4.5 (b). There, the upper switch, T_1 , is turned off with current i_{D,T_1} in forward direction and thus, its body diode blocks. Consequently, the inductor current, i_{L_1} , charges the drain-to-source capacitance of T_1 and discharges the respective capacitance of T_2 (Figure 4.12). This process continues until either the body diode of T_2 starts to conduct or until T_2 is turned on.

²The frequency response of these current sensors has not been compensated, since the employed LV MOSFETs (IRF2804) cause considerably slower voltage and current transients than the employed HV MOSFETs

Very low switching losses are achieved with this kind of operation, since T_1 is turned off with $v_{DS,T_1} \approx 0$ (zero voltage turn-off),³ and – on the assumption of $T_{\text{deadtime}} = t_{1b} - t_{1a}$ being selected long enough – T_2 is turned on with $v_{DS,T_2} = -v_D \approx 0$ (zero voltage turn-on; typically, the losses due to the forward voltage drop v_D of the body diode can be neglected during the short time the diode conducts). Thus, this switching operation is termed Zero Voltage Switching (ZVS) or soft switching (Figure 4.12).

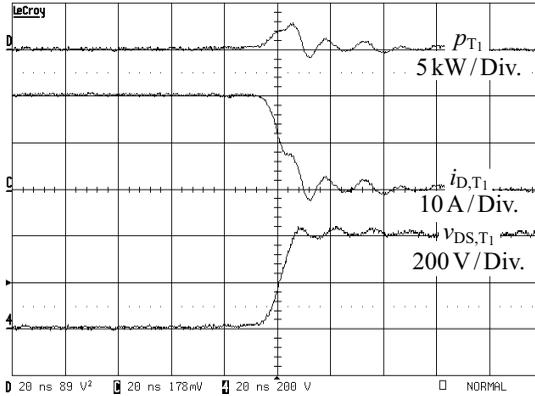
Hard Switching

At $t = t_{2a}$, the lower switch depicted in Figure 4.5, T_2 , is turned off, however, its body diode continues to conduct due to the negative value of i_{D,T_2} . The MOSFET T_1 is turned on at $t = t_{2b}$ and the drain current of T_1 starts to increase after the turn-on time delay expired at $t = t_{2c} > t_{2b}$ (Figure 4.13). The current through the body diode of T_2 accordingly decreases, crosses zero at $t = t_{2d} > t_{2c}$, becomes negative due to reverse recovery effects, and reaches the peak of its reverse recovery current at $t = t_{2e}$ in Figure 4.13. At $t = t_{2e}$ the diode starts to block and the reverse current, which is still present in T_2 , decreases to zero.

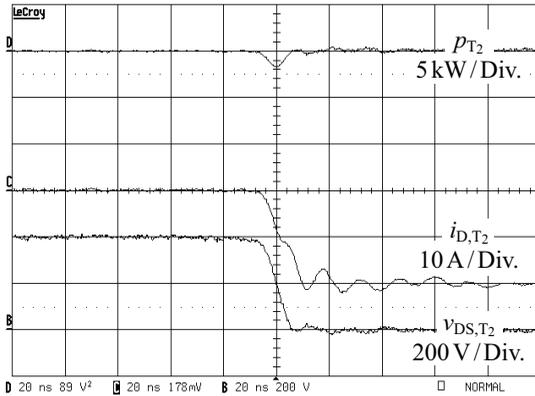
This switching operation is referred to as hard switching operation and typically generates high switching losses (cf. Figure 4.13: there, a maximum instantaneous power dissipation of more than 16 kW is measured at $t = t_{2e}$, $V_1 = 400$ V and $I_{S1,sw} = -10$ A). During hard switching, due to parasitic line inductance, quickly changing drain currents cause excess voltages superimposed on the nominal drain-to-source voltages of the blocking semiconductor switches, which may damage these semiconductors. Furthermore, high voltage slopes $dv_{DS,T_1}/dt$ and $dv_{DS,T_2}/dt$ (up to 80 kV/ μ s are observed with the given hardware setup) and ringing on v_{DS,T_1} and v_{DS,T_2} causes serious EMI issues.

Hard switching as well occurs if the inductor current i_{L_1} is zero during switching, since the drain-to-source capacitances of the respective MOSFETs need to be charged or discharged. Therefore, with $i_{L_1} = 0$, the drain-to-source voltages v_{DS,T_1} and v_{DS,T_2} remain constant during the dead time interval; after the dead time interval has elapsed, the activated switch provides the required current to change v_{DS,T_1} and v_{DS,T_2} , which particularly causes turn-on losses (Figure 4.14).

³Zero voltage turn-off is achieved due to the parasitic drain-to-source capacitances of the employed MOSFETs. The non-linear dependence of these capacitances on the respective drain-to-source voltages additionally supports the successful practical implementation of zero voltage turn-off.



(a)



(b)

Figure 4.12: HV side switch currents and voltage waveforms for soft switching operation, $V_1 = 400$ V and $I_{S1,sw} = 20$ A: (a) T_1 and (b) T_2 . During the switching process, negative switching losses occur for T_2 , since the inductor L discharges the parasitic drain-to-source capacitance of T_2 .

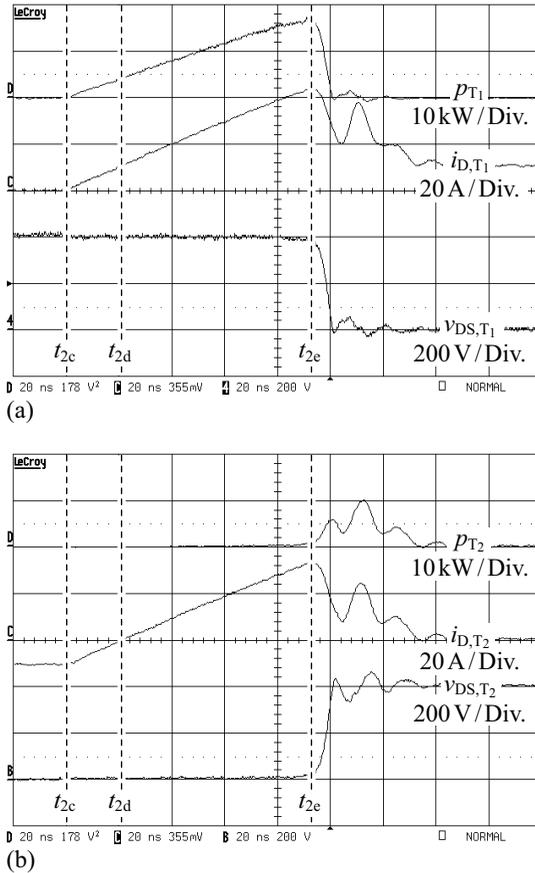
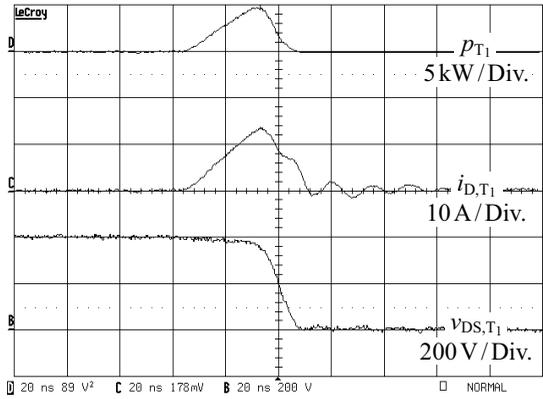
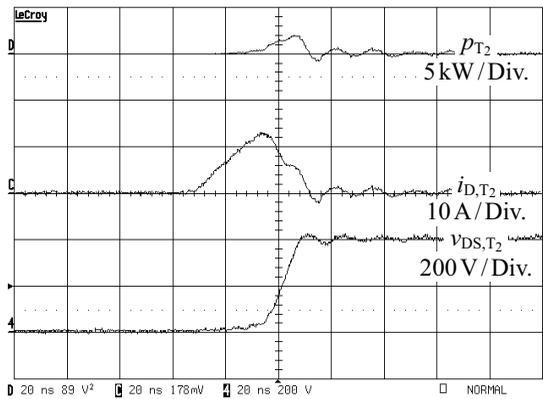


Figure 4.13: HV side switch currents and voltage waveforms for hard switching operation, $V_1 = 400$ V and $I_{S1,sw} = -10$ A: (a) T₁ and (b) T₂. The vertical dashed line indicates the turn-on time of T₁, t_{2c} [$> t_{2b}$ in Figure 4.5 (c)], identified from the rising switch currents. At $t = t_{2d}$ the switch current $i_{D,T2}$ approaches zero, thus diode reverse recovery occurs during $t_{2d} < t < t_{2e}$. At $t = t_{2e}$, the drain current $i_{D,T1} \approx 44$ A causes an instantaneous power dissipation of more than 16 kW in T₁; the peak voltage slope of $dv_{DS,T1}/dt$ reaches ≈ 80 kV/ μ s.



(a)



(b)

Figure 4.14: HV side switch currents and voltage waveforms for hard switching operation, $V_1 = 400\text{ V}$ and $I_{S1,sw} = 0$: (a) T_1 and (b) T_2 ; a peak drain current $i_{D,T1,max}$ of $\approx 14\text{ A}$ is required to charge the parasitic drain-to-source capacitance of T_2 , which causes a maximal instantaneous power dissipation of $\approx 5\text{ kW}$ in T_1 ; the peak voltage slope $dv_{DS,T1}/dt$ reaches $\approx 30\text{ kV}/\mu\text{s}$ (cf. Figure 4.13).

<i>HV Side, Edge Type of v_{AC1}</i>	$I_{S1,sw}$	s_{edge}
Rising edge of $v_{AC1}(t = t_{sw})$	$I_{S1,sw} = -i_{L1}(t_{sw})$	$s_{edge} = -1$
Falling edge of $v_{AC1}(t = t_{sw})$	$I_{S1,sw} = +i_{L1}(t_{sw})$	$s_{edge} = +1$
<i>LV Side, Edge Type of v_{AC2}</i>	$I_{S2,sw}$	s_{edge}
Rising edge of $v_{AC2}(t = t_{sw})$	$I_{S2,sw} = +i_{L2}(t_{sw})$	$s_{edge} = +1$
Falling edge of $v_{AC2}(t = t_{sw})$	$I_{S2,sw} = -i_{L2}(t_{sw})$	$s_{edge} = -1$

Table 4.1: Expressions required to obtain $I_{S1,sw}$ and $I_{S2,sw}$ from the respective instantaneous inductor currents $i_{L1}(t_{sw})$ and $i_{L2}(t_{sw})$ at a switching instant t_{sw} ; e.g. in Figure 3.4, at $t = 0$, a rising edge of v_{AC1} occurs and thus, the HV side full bridge switches the current $I_{S1,sw} = -i_{L1}(0) [\approx i_L(0)]$. The respective sign adjustment [e.g. in (4.30)] employs s_{edge} .

Measured Switching Losses

In Figure 4.15, the sum $E_{T1} + E_{T2} = E_{S1,a,sw}$ is shown for a single switching process and for different switching currents $I_{S1,sw}$, different operating voltages V_1 , and a junction temperature, T_j , of 25°C . Negative switching currents in Figure 4.15 indicate hard switching operation of the half bridge circuit where significant losses occur due to the slow MOSFET body diodes. For positive switching currents greater than 2 A, the circuit is successfully operated with ZVS giving very low switching losses. Low currents ($0\text{ A} \leq I_{S1,sw} \leq 2\text{ A}$) are insufficient to charge and discharge the respective drain-to-source capacitances within the dead time interval, which causes the turn-on losses to increase. Figure 4.16 depicts the switching losses measured at $T_j = 125^\circ\text{C}$; due to the raised component temperatures, the switching losses increase by $\approx 30\% \dots 40\%$. The instants t_{begin} and t_{end} , needed to evaluate (4.26), are selected such that neither a reduction of t_{begin} nor an increase of t_{end} changes the measured switching losses; the duration of the measurement time interval $t_{end} - t_{begin}$ is between 100 ns and 300 ns.

Table 4.1 summarizes the expressions required to determine $I_{S1,sw}$ from the actual inductor current $i_{L1}(t_{sw})$ at the switching instant t_{sw} .

Detailed Consideration of the Switching Losses

Depending on the switching current of the full bridge, two different polynomial functions – one for hard switching and one for soft switching – are fitted to the switching losses using a least mean square approximation. However, the switching losses are measured with constant inductor current $i_{L1}(t)$ during

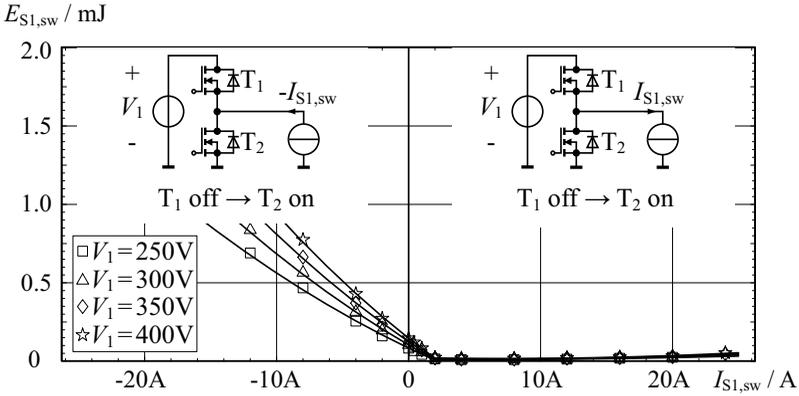


Figure 4.15: HV side switching losses measured at $T_j = 25^\circ\text{C}$ for a single switching action. $I_{S1,sw}$ is the instantaneous current during switching: $I_{S1,sw} < 0$ denotes hard switching and for $I_{S1,sw} > 0$ the ZVS condition is satisfied.

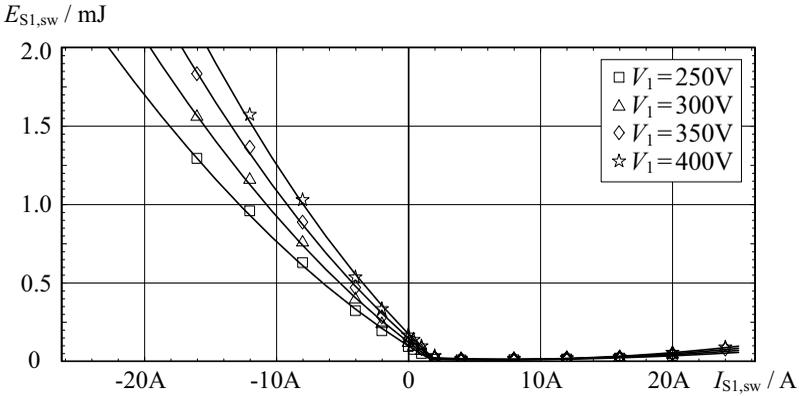


Figure 4.16: HV side switching losses measured at $T_j = 125^\circ\text{C}$ for a single switching action. $I_{S1,sw}$ is the instantaneous current during switching: $I_{S1,sw} < 0$ denotes hard switching and for $I_{S1,sw} > 0$ the ZVS condition is satisfied.

the dead time interval what may not be true in practice. Thus, wrong results are obtained for certain operating points, if the current calculated at the switching instant, $I_{S1,sw}$, is directly applied to the switching loss function [Figure 4.17 (c)]. In order to improve the results, the soft switching case and the hard switching case need to be looked at separately, due to essentially different switching processes.

For the soft switching case ($I_{S1,sw} > 2A$ in Figure 4.15), the voltage v_{AC1} changes within the dead time interval, whereas a certain charge must be supplied in order to achieve ZVS [i.e. to charge and discharge the respective MOSFET junction capacitances, Figures 4.17 (a) and (b)],

$$Q(V_1) = s_{edge} \cdot \int_{t_{off}}^{t_{edge}} i_{L1}(t) dt \quad (4.30)$$

(t_{off} denotes the MOSFET turn-off time and t_{edge} is the time when v_{AC1} changes; s_{edge} denotes the sign adjustment according to Table 4.1). The amount of charge depends on the employed power MOSFETs, e.g. $Q(V_1) \approx 220 \text{ nC} + V_1 \cdot 218 \text{ pF}$ for the SPW47N60CFD at room temperature (estimated using data sheet information). With known $Q(V_1)$, $i_{L1}(t)$, and t_{edge} , the turn-off time t_{off} , that is required in order to fully charge and discharge the MOSFET drain-to-source capacitances, can be calculated.⁴

For the hard switching case ($I_{S1,sw} < 0$ in Figure 4.15), the voltage v_{AC1} changes after the dead time interval has elapsed. On the assumption of negligible turn-on and turn-off delays, the MOSFET turn-off time is determined with $t_{off} = t_{edge} - T_{deadtime}$.

It finally turns out that the calculated switching losses become considerably more accurate if the switching loss function employs the average of the current i_{L1} , evaluated over the time interval $t_{off} < t < t_{edge}$ [Figure 4.17 (b) and (c)],

$$\bar{I}_{S1,sw} = \frac{s_{edge} \cdot \int_{t_{off}}^{t_{edge}} i_{L1}(t) dt}{t_{edge} - t_{off}} \quad (4.31)$$

The resulting switching losses of the HV side full bridge comprise of the switching losses caused by the two half bridges T_1, T_2 and T_3, T_4 ,

$$P_{S1,sw} = 2fs [E_{S1,sw} (\bar{I}_{S1,a,sw}) + E_{S1,sw} (\bar{I}_{S1,b,sw})] \quad (4.32)$$

($\bar{I}_{S1,a,sw}$ denotes the average switching current of T_1 and T_2 ; $\bar{I}_{S1,b,sw}$ denotes the average switching current of T_3 and T_4 ; for phase shift modulation $\bar{I}_{S1,a,sw} = \bar{I}_{S1,b,sw}$ applies).

⁴Whenever $t_{off} < t_{edge} - T_{deadtime}$ occurs, the injected charge during the dead time interval is not sufficient to achieve soft switching ($0 < I_{S1,sw} < 2A$ in Figure 4.15); consequently, t_{off} needs to be limited to $t_{edge} - T_{deadtime}$.

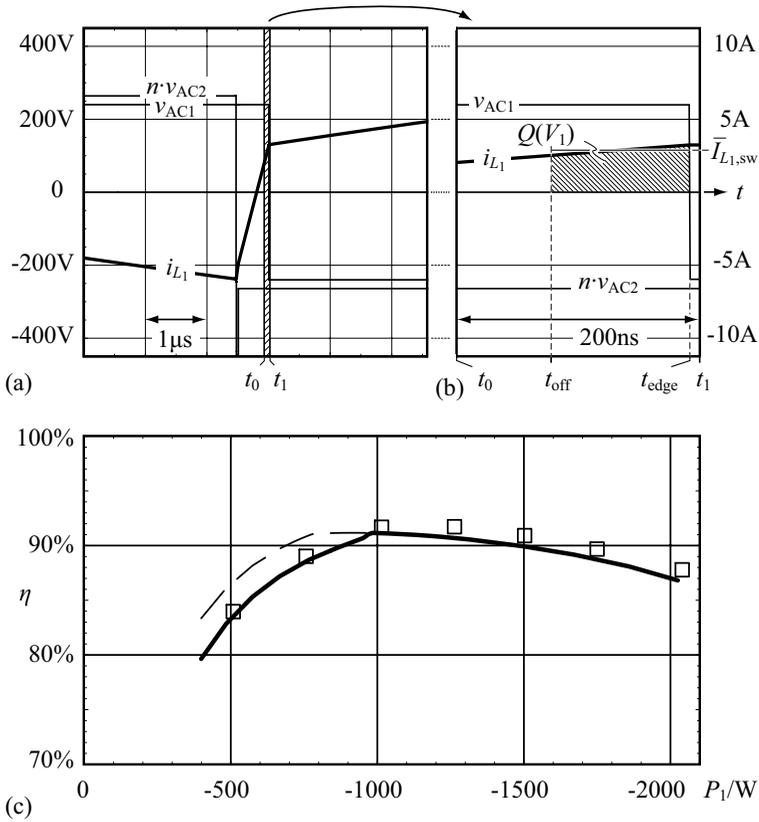


Figure 4.17: Implemented HV side switch current estimation, illustrated for the results obtained from a first converter design with $n = 24$ and $L = 30.8 \mu H$. There, at low power levels ($|P_1| < 1000 W$), the instantaneous inductor current during HV side switching is insufficient to fully charge and discharge the respective MOSFET drain-to-source capacitances, which causes the HV side switching losses to increase. (a) Calculated voltage and current waveforms for $V_1 = 240 V$, $V_2 = 11 V$, and $P_1 = -2 kW$ (power is transferred from the LV port to the HV port); (b) the magnified time interval $t_0 < t < t_1$ depicts the turn-off process for a HV MOSFET with involved charge $Q(V_1)$ and the current $\bar{I}_{S1,sw}$: the MOSFET gate is turned off at t_{off} and the drain-to-source voltage changes at t_{edge} ; (c) achieved improvement of the efficiency prediction (solid line: calculation uses $\bar{I}_{S1,sw}$, dashed line: $i_{L1}(t_{edge})$ is used to determine the switching losses).

Measured Time Delays

Gate driver delays, internal delays of the semiconductor switches, and capacitive charging processes cause a total time delay which needs to be considered in order to achieve the designated transformer currents and the required output power with the modulation parameters (D_1 , D_2 , and φ) of the modulation schemes discussed in Chapter 3 and Chapter 5 [103]. The employed measurement setup [Figure 4.18 (a)] allows the measurement of the total time delay between the initiation of the switching process and the actual change of the respective drain-to-source voltage, using the control signals depicted in Figure 4.18 (d).

The measured switching time delays predominantly depend on the switching current $I_{S1,sw}$ ($= I_{L1}$ in Figure 4.18); the minimal time delay, $T_{S1,d,min} \approx 100$ ns, is achieved for ZVS operation with maximal current (i.e. $I_{S1,sw} = 25$ A in Figure 4.19); maximal time delay, $T_{S1,d,max} \approx 350$ ns, occurs for hard switching operation with maximal negative current (i.e. $I_{S1,sw} = -10$ A in Figure 4.19). In the range $2\text{ A} < I_{S1,sw} < 7\text{ A}$, the relation between $T_{S1,d}$ and $I_{S1,sw}$ is highly non-linear, since the time to charge and discharge the drain-to-source capacitances of the MOSFETs increases with reduced currents $I_{S1,sw}$.

Measurements with different voltages V_1 within the specified voltage range, $240\text{ V} \leq V_1 \leq 450\text{ V}$, show virtually unchanged time delays $T_{S1,d}$; thus, $T_{S1,d}$ is considered independent of V_1 . Increased semiconductor temperatures cause the time delays to increase slightly, i.e. if the junction temperature rises from $T_j = 25^\circ\text{C}$ to $T_j = 125^\circ\text{C}$, the time delay increases by ≈ 20 ns in the soft switching range ($I_{S1,sw} > 0$) and by ≈ 15 ns in the hard switching range (Figure 4.19).

4.3.3 LV Side Switching: Results

Soft Switching

With the double pulse signal being applied to the half bridge depicted in Figure 4.10, the switch T_5 is turned off at $t = t_{1a}$ with positive drain current, $i_{D,T_5} > 0$. Thus, the body diode of T_5 blocks and the inductor current \tilde{i}_{L2} charges and discharges the parasitic drain-to-source capacitances of T_5 and T_6 , respectively. Due to the low voltage and high current operation, however, the parasitic stray inductances L_{D,T_5} , L_{S,T_5} , L_{D,T_6} , and L_{S,T_6} (sums of the lead inductances, the inductances of the bonding wires, and the inductances of the wiring on the PCB) cause the drain-to-source voltage of T_5 to considerably exceed the supply voltage (Figure 4.20). For T_5 , a large drain-to-source voltage and a large drain current occur simultaneously and thus, large turn-off losses result (Figure 4.22). Consequently, compared to the soft switching process on the HV side discussed in Section 4.3.2, ZVS operation is effec-

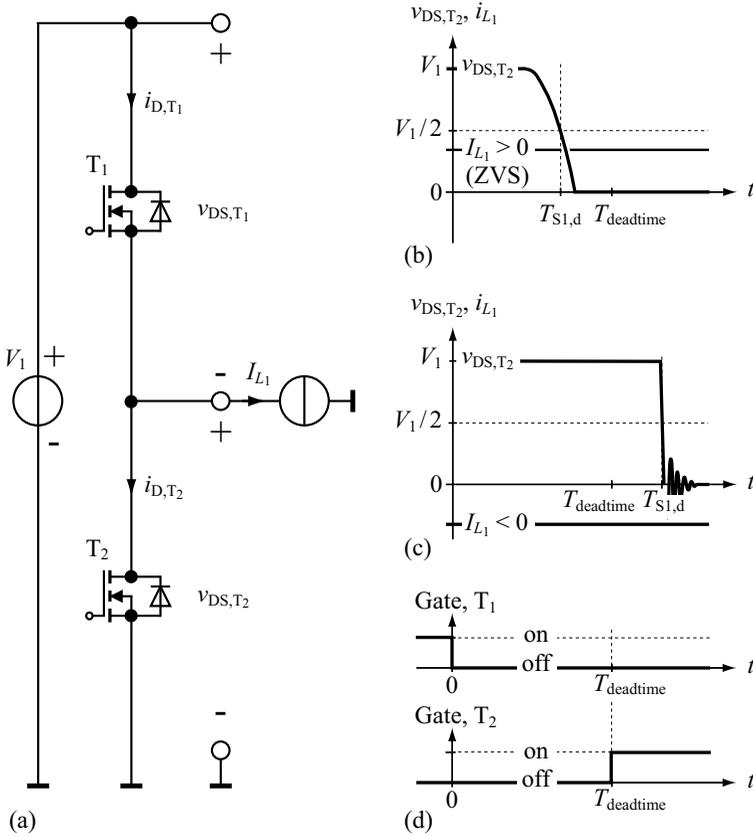


Figure 4.18: (a) Setup employed to measure the time delay between the turn-off gate signal (i.e. gate signal of T_1) and the edge of the bridge output voltage (i.e. $v_{DS,T1}$ or $v_{DS,T2}$); (b) typical waveforms, ZVS operation; (c) typical waveforms, hard switching operation; (d) employed gate signals for T_1 and T_2 .

tively not achieved for the LV side full bridge.⁵ For high switching currents,

⁵The switching losses in the ZVS range can be reduced by increasing the drain-to-source capacitances of the MOSFETs. However, since the inductances of bonding wires and connecting leads are a large proportion of the total parasitic inductances $L_{D,T5} + L_{S,T5}$, $L_{D,T6} + L_{S,T6}$, $L_{D,T7} + L_{S,T7}$, and $L_{D,T8} + L_{S,T8}$ (cf. Figure 4.10), the additional capacitances would be required to be closely placed to the chips of the MOSFETs. If the

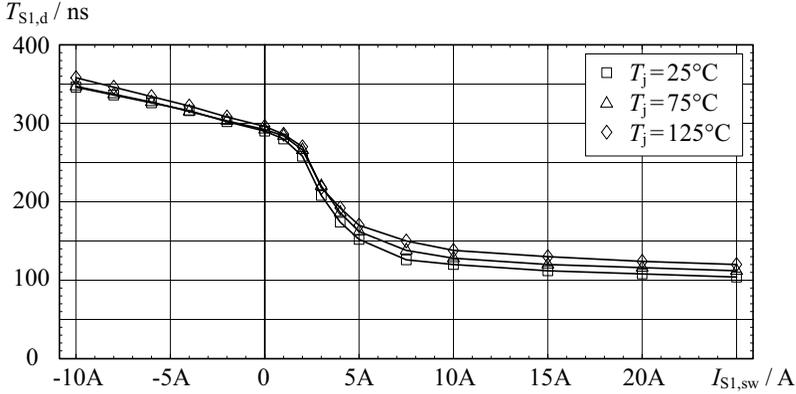


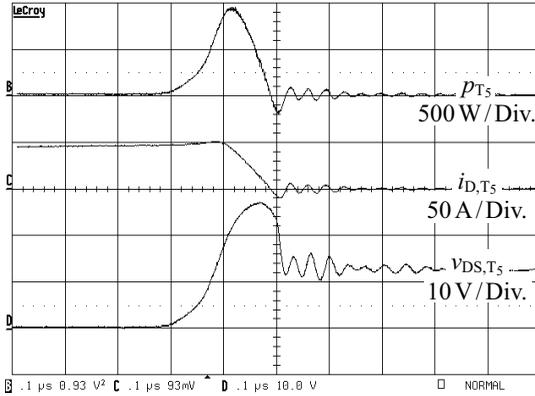
Figure 4.19: Measured HV side switching time delays with respect to the switching current $I_{S1,sw}$, constant supply voltage, $V_1 = 340$ V, and different junction temperatures T_j .

$\tilde{i}_{L_2}(t_{1a}) \gg 0$, the switching losses due to the parasitic inductances can be estimated with (4.7).

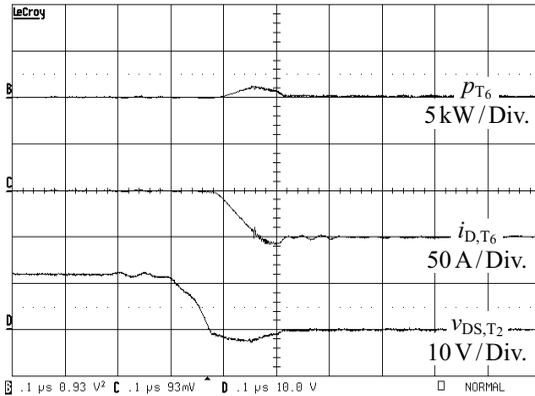
Hard Switching

At $t = t_{2a}$ [Figure 4.5 (b) and Figure 4.10], T_6 is turned off with negative drain current, $i_{D,T_6} < 0$; hence, the body diode of T_6 conducts during $t_{2a} < t < t_{2b}$. At $t = t_{2b}$, T_5 is turned on and, due to the parasitic stray inductances, $|i_{D,T_6}|$ decreases and $|i_{D,T_5}|$ increases (Figure 4.21), i.e. the magnetic energy stored in L_{D,T_6} and L_{S,T_6} is transferred to L_{D,T_5} and L_{S,T_5} . Reverse recovery effects still occur and mainly cause ringing; the resulting reverse recovery losses are comparatively small, due to the low operating voltage of the full bridge, the small MOSFET reverse recovery charge ($Q_{rr} \leq 100$ nC at room temperature and $di/dt = -100$ A/ μ s), and the parasitic stray inductances, which limit the slow rates of i_{D,T_5} and i_{D,T_6} . Thus, in contrast to the HV side (Section 4.3.2), the full bridge on the LV side generates low losses during hard switching (cf. Figure 4.22).

additional capacitors are solely placed in parallel to the packaged MOSFETs, only a minor improvement of the switching losses is achieved with the existing hardware prototype (e.g. with $C = 4.7$ nF in parallel to each LV MOSFET, the switching losses decrease by $\approx 10\%$).



(a)



(b)

Figure 4.20: LV side switch currents and voltage waveforms for soft switching operation, $V_1 = 12$ V and $I_{S2,sw} = 200$ A (50 A per switch): (a) T₅ and (b) T₆; the drain-to-source voltage of T₆, $v_{DS,T6}$, considerably exceeds the supply voltage due to parasitic stray inductances.

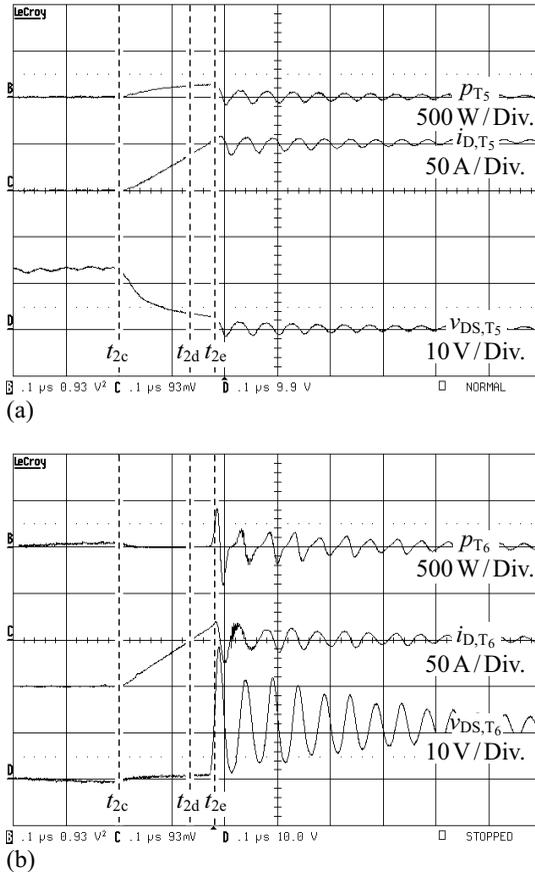


Figure 4.21: LV side switch current and voltage waveforms for hard switching operation, $V_2 = 12\text{ V}$ and $I_{S2,sw} = -200\text{ A}$ (-50 A per switch): (a) T_5 and (b) T_6 ; the vertical dashed line indicates the turn-on time of T_5 , t_{2c} ($> t_{2b}$ in Figure 4.5), identified from the rising switch currents. At $t = t_{2d}$ the switch current i_{D,T_5} is zero and during $t_{2d} < t < t_{2e}$, diode reverse recovery occurs and causes ringing. The drain-to-source voltage of T_5 , v_{DS,T_5} , is considerably larger than zero during $t_{2c} < t < t_{2e}$ (mainly due to the employed gate to source voltage of 10 V : with a higher gate voltage, a reduction of v_{DS,T_5} could be achieved during $t_{2c} < t < t_{2e}$ and therefore, lower turn-on losses would result).

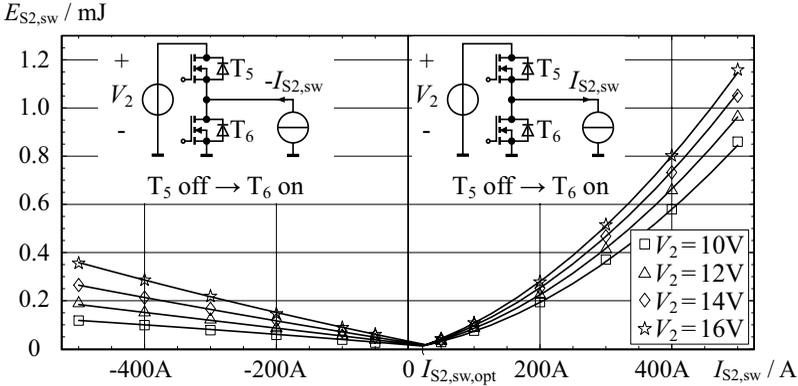


Figure 4.22: Measured switching losses at $T_j = 25^\circ\text{C}$ for a single LV side switching action. $I_{S2,sw}$ is the instantaneous current during switching; $I_{S2,sw} < 0$ denotes hard switching and for $I_{S2,sw} > 0$ the ZVS condition is satisfied; $I_{S2,sw,opt}$ denotes the switch current with respect to minimal switching losses, needed in Section 5.2.2.

Measured Switching Losses

Figure 4.22 presents the measured and scaled switching losses of one half bridge of the fully equipped LV side full bridge (i.e. 8 parallel MOSFETs per switch) for a junction temperature T_j of 25°C . Figure 4.23 presents the switching losses for $T_j = 125^\circ\text{C}$. Hard switching occurs for $I_{S2,sw} < 0$ and soft switching for $I_{S2,sw} > 0$. For $I_{S2,sw} > 0$, the switching losses are mainly caused by the energies stored in the parasitic lead inductances [cf. (4.7) and [93]] and are therefore almost independent of the MOSFETs' junction temperatures. The measurement results further show that, in case of hard switching operation ($I_{S2,sw} < 0$), the switching losses are almost independent of the MOSFETs' junction temperatures, too.⁶

In accordance to the switching processes discussed above, high switching losses result for $I_{S2,sw} > 0$ (soft switching) and comparably low switching losses occur for $I_{S2,sw} < 0$ (hard switching). With the LV side full bridge, lowest switching losses are achieved for $I_{S2,sw} \approx 0$.

⁶The lower and the upper integration limits t_{begin} and t_{end} , needed to determine the switching loss energy [cf. (4.26)], are selected such that neither a reduction of t_{begin} nor an increase of t_{end} changes the measured switching losses; the duration of the measurement time interval $t_{end} - t_{begin}$ is between 200 ns and 1 μs .

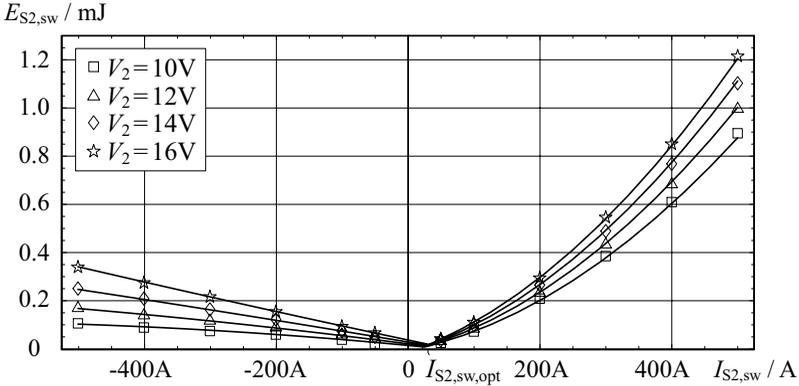


Figure 4.23: Measured switching losses at $T_j = 125^\circ\text{C}$ for a single LV side switching action. $I_{S2,sw}$ is the instantaneous current during switching (cf. Figure 4.22). For $I_{S2,sw} > 0$, the switching losses are mainly caused by the energies stored in the parasitic lead inductances [cf. (4.7) and [93]] and are therefore almost independent of the MOSFETs' junction temperatures. The depicted measurement results further show that, in case of hard switching operation ($I_{S2,sw} < 0$), the switching losses are almost independent of the MOSFETs' junction temperatures, too.

Detailed Consideration of the Switching Losses

Similar to the HV side, two different polynomial functions are fitted to the measured switching losses. Again, the switching losses are measured using a constant inductor current $\tilde{i}_{L_2}(t)$ during the dead time interval. However, due to high currents and low voltages, the switching process either commences directly after turn-off ($I_{S2,sw} > 0$ in Figure 4.22) or directly after turn-on ($I_{S2,sw} < 0$) and thus, the switching losses can be accurately evaluated using the instantaneous current $\tilde{i}_{L_2}(t_{sw})$ at the switching instant t_{sw} [cf. Table 4.1 with $\tilde{i}_{L_2}(t_{sw}) = -i_{L_2}(t_{sw})$].

Impact of the Switching Process on the Transformer Current

Due to the parasitic inductances connected in series to the semiconductor switches T_5 , T_6 , T_7 , and T_8 , a considerable voltage spike occurs on v_{AC2} if the LV side full bridge of the DAB is operated with ZVS (Figure 4.24); this voltage spike causes the absolute values of the inductor currents $|i_{L_1}|$ and $|i_{L_2}|$ to drop and decreases the converter efficiency.

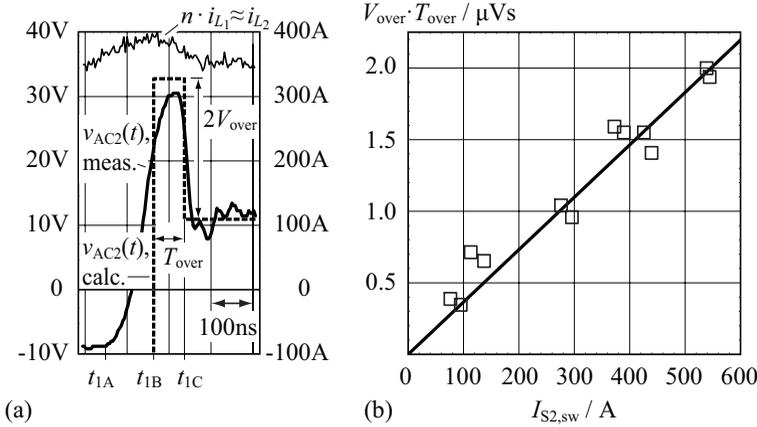


Figure 4.24: (a) LV side overvoltage due to the parasitic MOSFET and PCB inductances (magnified detail of the measured waveforms of a first design of the DAB with $n = 24$ and $L = 30.8 \mu\text{H}$, $V_1 = 240 \text{ V}$, $V_2 = 11 \text{ V}$, $P_2 = 2 \text{ kW}$ and power being transferred from the HV port to the LV port); (b) measured voltage time areas for different switch currents $I_{S2,sw}$ and phase shift modulation. The bold line denotes the voltage time area approximated for phase shift modulation: $2V_{\text{over}} \cdot T_{\text{over}} = 3.66 \text{ nVs/A} \cdot I_{S2,sw}$ (the factor 2 is due to the phase shift modulation: there, two half bridges switch simultaneously); for a switching process of a single half bridge, $V_{\text{over}} = 10.2 \text{ V}$ is considered.

The effect of the voltage spike on v_{AC2} is derived for a full bridge [Figure 4.25 (a)] operated with ZVS, a constant supply voltage V_2 , and a sufficiently large inductor current $|i_{L2}(t)| \gg 0$ within the considered time interval. The presented analysis considers the lossless electric DAB model depicted in Figure 3.2, i.e. $\tilde{i}_{L2} = -i_{L2} = -n i_L$, and assumes equal total parasitic inductances L_{DS} ,

$$L_{DS} = L_D + L_S, \tag{4.33}$$

for all 4 switches T_5 , T_6 , T_7 , and T_8 ; the forward voltage drops due to the MOSFETs' body diodes are neglected.

Initially, T_5 and T_8 are in the on-state and T_6 and T_7 in the off-state. At $t = t_{1A}$, T_5 is turned off and $v_{DS,T6}$ quickly drops until the body diode starts to conduct at $t = t_{1B}$. However, sufficiently large currents and a small time interval $t_{1A} < t < t_{1B}$ are assumed in order to estimate the worst possible current drop in \tilde{i}_{L2} , i.e. the time interval $t_{1A} < t < t_{1B}$ shown in Figure 4.24 (a) is neglected.

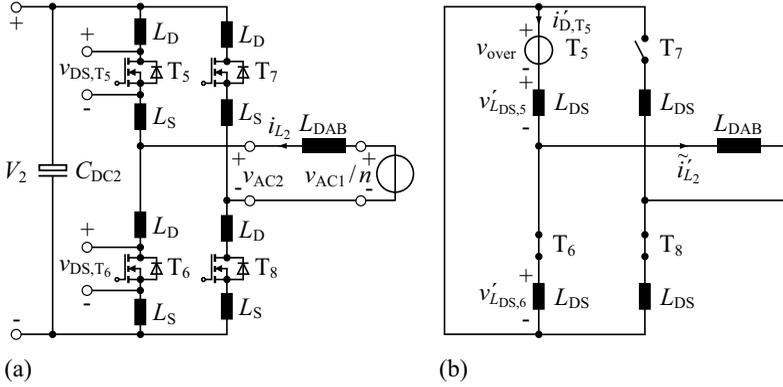


Figure 4.25: (a) Inductively loaded full bridge (LV side) with parasitic inductances L_D and L_S ; (b) equivalent circuit of the LV full bridge used to exclusively investigate the implication of v_{over} on the inductor current \tilde{i}_{L2} .

During $t_{1B} < t < t_{1C}$, the excess voltage $v_{over}(t) > 0$ is superimposed on $v_{DS,T5}$,

$$v_{DS,T5} = V_2 + v_{over}(t). \quad (4.34)$$

Consequently, $v_{over}(t) = v_{DS,T5}(t) - V_2$ is partly applied to the parasitic lead inductances of T5 [Figure 4.25 (b)]:

$$v'_{L_{DS,5}} = v'_{L_{D,5}} + v'_{L_{S,5}} = -\frac{L_{DS}}{L_{total}} v_{over} \quad \text{with} \quad (4.35)$$

$$L_{total} = L_{DS} + L_{DS} || (L_{DAB} + L_{DS}) \quad (4.36)$$

($'$ denotes currents and voltages that are generated due to v_{over}). Furthermore, v_{over} causes a voltage drop across the lead inductors of T6:

$$v'_{L_{DS,6}} = v'_{L_{D,6}} + v'_{L_{S,6}} = -\left(1 - \frac{L_{DS}}{L_{total}}\right) v_{over}. \quad (4.37)$$

The voltage $v'_{L_{DS,5}}$, applied to L_S and L_D , causes the current $i'_{D,T5}$ to decrease according to:

$$i'_{D,T5}(t) = i'_{D,T5}(t_{1B}) - \frac{1}{L_{DS}} \frac{L_{DS}}{L_{total}} \int_{t_{1B}}^t v_{over}(t_{int}) dt_{int}, \quad t_{1B} \leq t \leq t_{1C}. \quad (4.38)$$

With the condition $i'_{D,T_5}(t_{1C}) = 0$, the integrated overvoltage becomes:

$$\int_{t_{1B}}^{t_{1C}} v_{\text{over}}(t_{\text{int}}) dt_{\text{int}} = i'_{D,T_5}(t_{1B}) L_{\text{total}} = i'_{D,T_5}(t_{1B}) \frac{L_{\text{DS}} \cdot (2L_{\text{DAB}} + 3L_{\text{DS}})}{L_{\text{DAB}} + 2L_{\text{DS}}}. \quad (4.39)$$

With (4.37), the inductor current,

$$\tilde{i}'_{L_2}(t_{1C}) = \tilde{i}'_{L_2}(t_{1B}) - \frac{1}{L_{\text{DAB}} + L_{\text{DS}}} \cdot \left(1 - \frac{L_{\text{DS}}}{L_{\text{total}}}\right) \int_{t_{1B}}^{t_{1C}} v_{\text{over}}(t_{\text{int}}) dt_{\text{int}}, \quad (4.40)$$

is derived at $t = t_{1C}$. Thus, the inductor current drops by

$$\Delta \tilde{i}'_{L_2} = \tilde{i}'_{L_2}(t_{1C}) - \tilde{i}'_{L_2}(t_{1B}) = -\frac{L_{\text{DS}}}{L_{\text{DAB}} + 2L_{\text{DS}}} \tilde{i}'_{L_2}(t_{1B}) = -\frac{L_{\text{DS}}}{L/n^2} \tilde{i}'_{L_2}(t_{1B}) \quad (4.41)$$

[using (4.39), $i_{D,T_5}(t_{1B}) = \tilde{i}'_{L_2}(t_{1B})$, and $L/n^2 = L_{\text{DAB}} + 2L_{\text{DS}}$], independent of v_{over} . Moreover, according to (4.40), an arbitrary waveform $v_{\text{over}}(t)$ that satisfies (4.39) can be used to accurately calculate $\Delta \tilde{i}'_{L_2}$. The employed numerical solver (Section 4.6.1) superimposes a rectangular voltage with the constant magnitude $V_{\text{over}} = 10.2 \text{ V}$ and the variable duration $t_{1C} - t_{1B}$,

$$t_{1C} - t_{1B} = \begin{cases} 179 \text{ ps/A} \cdot I_{S2,\text{sw}} & \text{if } I_{S2,\text{sw}} > 0, \\ 0 & \text{if } I_{S2,\text{sw}} < 0, \end{cases} \quad (4.42)$$

on $v_{\text{AC}2}(t)$ after a single switching process on the LV side (Figure 4.24, Figure 4.28).

Switching Time Delays

The total time delays between the initiation of a switching process and the actual change of the respective drain-to-source voltage are measured with the LV counterpart of the measurement setup depicted in Figure 4.18.

The measured switching time delays predominantly depend on the switching current $I_{S2,\text{sw}}$; the minimal time delay, $T_{S2,d,\text{min}} \approx 220 \text{ ns}$, is achieved for maximal positive current (i.e. $I_{S2,\text{sw}} = 500 \text{ A}$ in Figure 4.26); maximal time delay, $T_{S2,d,\text{max}} \approx 560 \text{ ns}$, occurs for hard switching operation with maximal negative current (i.e. $I_{S2,\text{sw}} = -500 \text{ A}$ in Figure 4.26). In the range $0 \text{ A} < I_{S2,\text{sw}} < 50 \text{ A}$, the relation between $T_{S2,d}$ and $I_{S2,\text{sw}}$ is highly non-linear: for low current levels, the time to charge the drain-to-source capacitances of the MOSFETs increases (cf. Section 4.3.2).

Measurements with different voltages V_2 within the specified voltage range, $10 \text{ V} \leq V_2 \leq 16 \text{ V}$, show slightly different time delays (i.e. the time delay varies

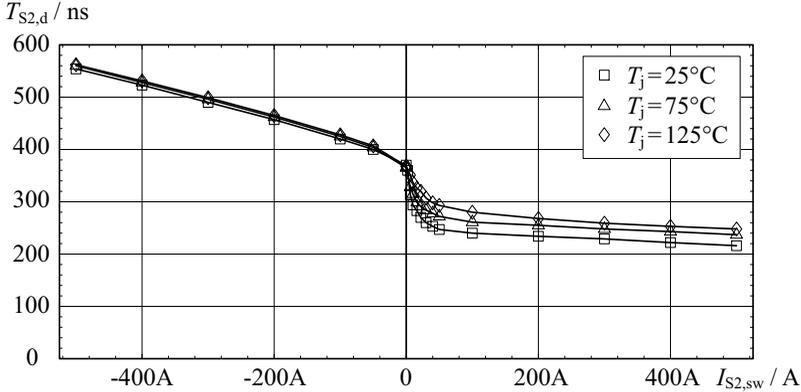


Figure 4.26: Measured LV side switching time delays with respect to the switching current $I_{S2,sw}$ and with constant supply voltage, $V_1 = 12\text{ V}$, and different junction temperatures T_j .

within $\pm 20\text{ ns}$); however, compared to the dependence on $I_{S2,sw}$, the influence of V_2 is considered to be negligible. Increased semiconductor temperatures cause the time delays to increase slightly, i.e. if the junction temperature rises from $T_j = 25^\circ\text{C}$ to $T_j = 125^\circ\text{C}$, the time delay in the soft switching range, $I_{S2,sw} > 0$, increases by $\approx 30\text{ ns}$; in the hard switching range, the time delay increases by $\approx 10\text{ ns}$ (Figure 4.26).

4.3.4 Gate Driver Losses

The gate driver circuits handle the charging and discharging processes of the parasitic gate-to-source and gate-to-drain capacitances of the MOSFETs in order to turn the MOSFETs on or off. The employed gate drivers simply use series resistances to charge or discharge the effective input capacitances of the MOSFETs. With this circuit, the related power dissipation can be calculated using the total gate charge Q_G of the MOSFET (datasheet value), the steady-state gate-to-source voltage V_{GS} during turn-on, and the switching frequency [107]. The HV side auxiliary power supply thus provides the resulting total gate driver power $P_{S1,gate}$,

$$P_{S1,gate} = 4 Q_{G,1} V_{GS,1} f_s, \quad (4.43)$$

for all 4 HV MOSFETs. Similarly, the LV side auxiliary power supply provides the total gate driver power $P_{S2, \text{gate}}$,

$$P_{S2, \text{gate}} = 32 Q_{G,2} V_{GS,2} f_s, \quad (4.44)$$

for all 32 LV MOSFETs. Thus, $P_{1, \text{aux}}$ already includes $P_{S1, \text{gate}}$ and $P_{2, \text{aux}}$ includes $P_{S2, \text{gate}}$.

4.4 Core Losses

For the given converter, the losses predicted with (4.10) and (4.14) are considered accurate enough, since the core losses are found to account for less than 10% of the total losses (at rated output power). However, for different specifications, core losses may become more important and thus a more advanced method, e.g. the modified Steinmetz equation [108], finite element analysis or the use of measurement results [109], may be required.

4.5 Accurate Input and Output Power Calculation

According to Section 4.1.3, all quantities required to calculate the efficiency (e.g. RMS current values) are determined at a certain input power P_{in} . However, the port power levels calculated with the electric DAB model [e.g. (3.111) for the DAB converter model with conduction losses and magnetizing inductance] are inaccurate, since the losses considered within the DAB model are different to the accurately calculated losses. Consequently, the calculated efficiency is inaccurately mapped to the considered input and output power levels.

A reference power level P_{ref} is introduced in order to achieve a more accurate calculation of the actual input and output power levels. P_{ref} is calculated based on the HV side DAB power obtained with the electric DAB model, $P_1 = V_1 \cdot I_1$, and the HV side conduction losses,⁷

$$P_{\text{ref}} = P_1 - R_1 \cdot I_1^2. \quad (4.45)$$

The more precise values of the HV port power, $P_{1, \text{prec}}$, and the LV port power, $P_{2, \text{prec}}$, are then obtained with

$$P_{1, \text{prec}} = P_{\text{ref}} + P_{1, \text{aux}} + P_{S1, \text{cond}} + P_{S1, \text{sw}} + P_{L_{\text{HV}}, \text{cond}} + P_{L_{\text{HV}}, \text{core}} + P_{\text{tr}1, \text{cond}} + P_{\text{tr}, \text{cond}}/2 \quad \text{and} \quad (4.46)$$

$$P_{2, \text{prec}} = P_{\text{ref}} - (P_{\text{tr}, \text{core}}/2 + P_{\text{tr}2, \text{cond}} + P_{\text{PCB}, \text{a}, \text{cond}} + P_{S2, \text{cond}} + P_{S2, \text{sw}} + P_{\text{PCB}, \text{b}, \text{cond}} + P_{2, \text{aux}}), \quad (4.47)$$

⁷ P_{ref} could as well be calculated using $P_2 = V_2 I_2$. However, overvoltage switching transients are regarded on the LV side and therefore P_2 partly contains switching losses; it is thus more intuitive to use P_1 for the presented calculation.

whereas evenly shared transformer core losses between LV side and HV side are assumed. The expressions (4.45), (4.46), and (4.47) are independent of the direction of power transfer, however, negative values result for P_{ref} , $P_{1,\text{prec}}$, and $P_{2,\text{prec}}$ if power is transferred from the LV port to the HV port.

4.6 Calculated and Measured Efficiencies, Phase Shift Modulation

4.6.1 Numerical Efficiency Calculation

A numerical solver calculates the transformer currents $i_{L_1}(t)$ and $i_{L_2}(t)$ in steady-state operation using piecewise constant voltages $v_{\text{AC1}}(t)$ and $v_{\text{AC2}}(t)$, which may change several times during a switching period and which repeat with changed sign after one half-cycle. By way of an examples, Figure 4.27 (a) illustrates $v_{\text{AC1}}(t)$ and $v_{\text{AC2}}(t)$ for $V_1 = 240$ V, $V_2 = 16$ V, $D_1 = 0.45$, $D_2 = 0.4$, and $\varphi = 60^\circ$.

The employed numerical solver algorithm applies v_{AC1} and v_{AC2} to the most complete electric DAB model discussed in Section 3.3 (Figure 3.31) in order to calculate the waveforms $i_{L_1}(t)$ and $i_{L_2}(t)$ [Figure 4.27 (b)].⁸ Furthermore, current dependent overvoltage spikes due to switching processes on the LV side (Section 4.3.3) are added to v_{AC2} to consider their impacts on the currents i_{L_1} and i_{L_2} (Figure 4.28; an iterative loop within the solver algorithm determines the actual duration of the overvoltage spikes).

With the proposed method, excellent matching to measured current waveforms is achieved (Figure 4.29). The RMS currents, harmonic current components, instantaneous current values, and input and output power levels obtained from $i_{L_1}(t)$ and $i_{L_2}(t)$ [cf. (3.111) and (3.117), Section 3.3], are then applied to the methods discussed in this Chapter in order to determine the converter losses.

4.6.2 Comparison to Measured Efficiency Values

With increasing level of detail, the calculated efficiency becomes more and more accurate (Figure 4.2): Table 4.2 compares the predicted losses P_t to the measured losses $P_{t,\text{meas}}$ (the absolute differences in Table 4.2 are equal to $|P_t - P_{t,\text{meas}}|$, the relative differences are calculated with $|P_t - P_{t,\text{meas}}|/P_{t,\text{meas}}$). In particular, the accurate consideration of the conduction losses – including high frequency effects – and the accurate consideration of the switching losses result in a major improvement and reduces the relative error from 44.0% to 6.3%

⁸The current waveform calculation employs (3.106)–(3.110), (3.114)–(3.116), and (3.67).

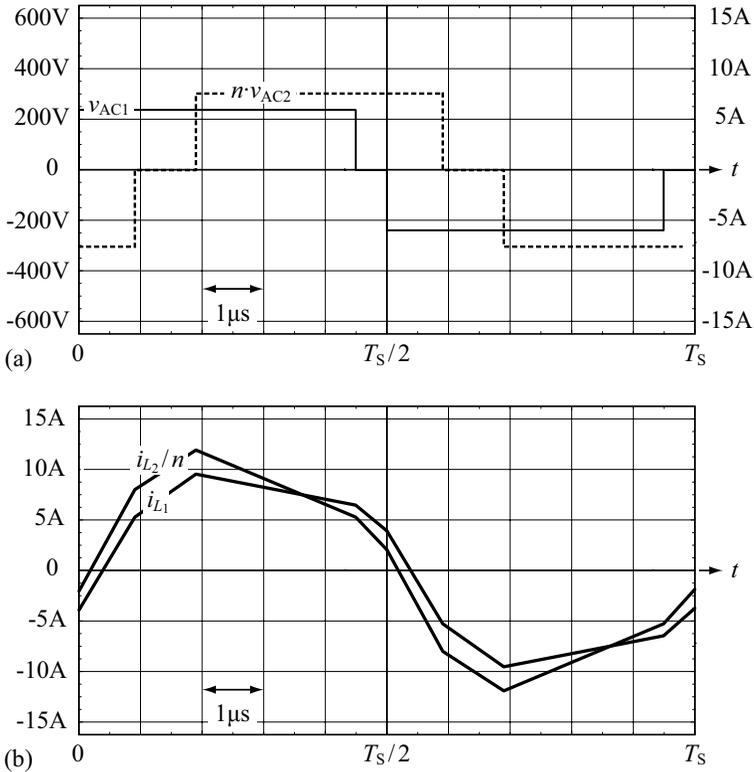


Figure 4.27: (a) Considered voltage waveforms and (b) calculated current waveforms after the first run of the numerical solver using $V_1 = 240\text{ V}$, $V_2 = 16\text{ V}$, $D_1 = 0.45$, $D_2 = 0.4$, $\varphi = 60^\circ$, $n = 19$, $L_1 + n^2 L_2 = 26.7\ \mu\text{H}$, $R_1 + n^2 R_2 = 0.76\ \Omega$ and a low magnetizing inductance of $L_M = 100\ \mu\text{H}$ (to emphasize the effect of the magnetizing current); during the first run, over-voltage spikes due to LV side switching are not considered.

in average. Additional little improvement to 6.0% average error is achieved with the correct consideration of input and output power levels according to Section 4.5.

In Figure 4.30, measured efficiencies are compared to calculated efficiencies for different operating points. Very good agreement between the results obtained from the theoretical model and the experimental values is observed.

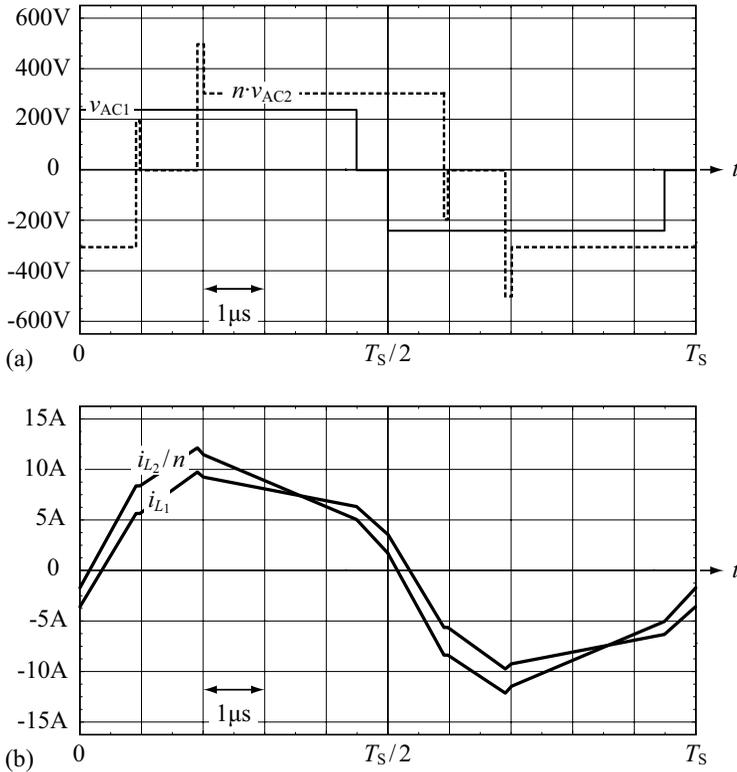


Figure 4.28: (a) The final voltage waveforms and (b) the final current waveforms calculated with the numerical solver algorithm include overvoltage switching spikes according to Section 4.3.3; the illustrated waveforms are calculated using the same parameters used to obtain Figure 4.27.

Moreover, Figure 4.30 illustrates the strong dependence of the efficiency values on the operating point. Interestingly, these efficiency values also depend on the direction of power transfer (e.g. for $V_1 = 240$ V and $V_2 = 11$ V), even though the DAB topology shows a symmetric structure. The main reason for this difference is the transformer current reduction due to LV side switching according to (4.41). For power being transferred to the LV port (mode A), this current reduction occurs at the beginning of the main energy transfer interval (interval II in Figure 4.29), which consequently reduces the amount of transferred power. Thus, the phase angle $\varphi = \varphi_A$ must be increased in order

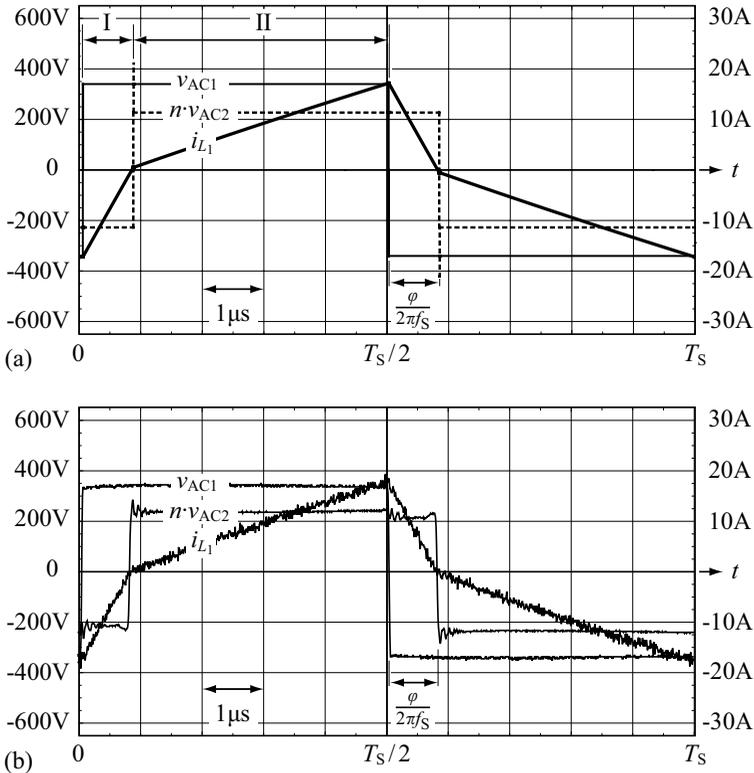


Figure 4.29: (a) Calculated and (b) measured voltage and current waveforms for phase shift modulation, $V_1 = 340$ V, $V_2 = 12$ V, $P_2 = 2$ kW, and power being transferred from the HV port to the LV port; $n = 19$, $L = 26.7 \mu\text{H}$. At this operating point, the instantaneous switch currents during a switching process of the LV side are close to zero and therefore, the overvoltage switching spikes contained in the calculation of $v_{AC2}(t)$ (Section 4.3.3) are almost negligible.

to obtain the required output power $P_{2,A,\text{prec}}$. For power being transferred to the HV port (mode B), the current reduction due to LV side switching occurs at the end of the main energy transfer interval. Hence, a lower phase angle $|\varphi_B| < |\varphi_A|$ is required for the same output power level $|P_{1,B,\text{prec}}| = P_{2,A,\text{prec}}$ which results in less circulating currents and lower switching losses.

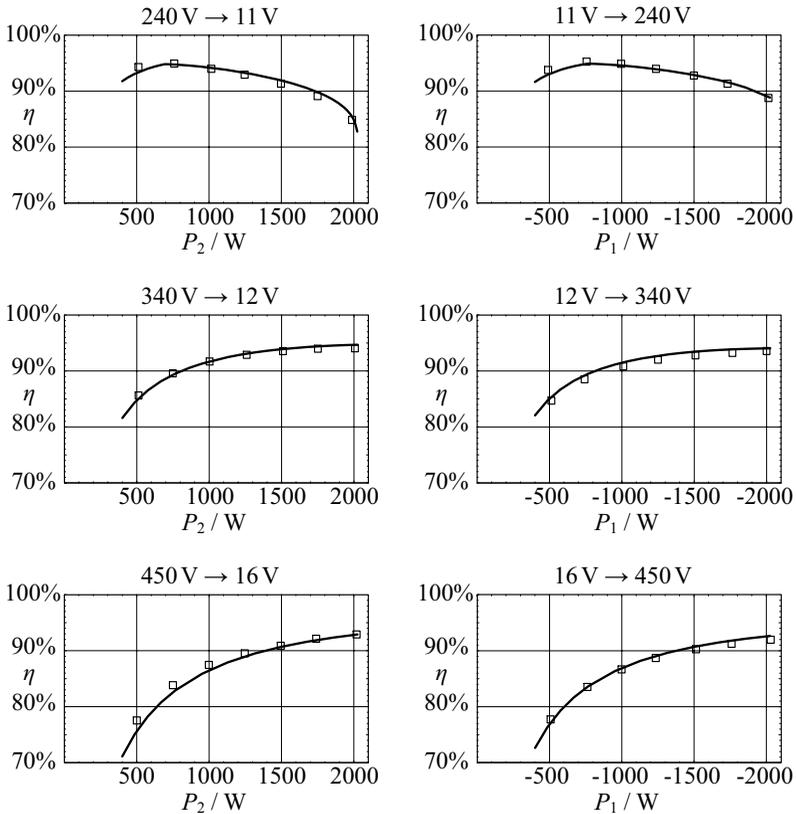


Figure 4.30: Predicted efficiencies (solid lines) and measured efficiencies (\square) for different operating conditions; the efficiencies are calculated with the improved DAB loss model which includes all methods discussed in this Chapter.

The presented loss model facilitates the prediction of the power loss distribution in the converter. In Figure 4.31 the losses for nominal operation are presented for the PCB, the low and high voltage side MOSFETs, the transformer, the inductor, and the auxiliary power supplies that provide the gate driver power. The LV MOSFETs dissipate 31 W, for the HV MOSFETs, total losses of 24 W occur, and the transformer has 22 W of losses.

However, the presented loss model does not include the effect of the temperature rise on the efficiency. Thus, besides the discussed electric model, a

thermal converter model, which contains accurate information on the temperature dependency of the losses, would be required in order to calculate the expected component temperatures [104,105].

For nominal operation of the DAB, high efficiency of more than 90% is achieved. The efficiency decreases for operating points that diverge significantly from the nominal operating point (Figure 4.30). The main reasons for the additional power loss arise from the conduction losses due to circulating transformer currents and increased switching losses on the LV side. A considerable improvement of the converter performance is achieved with optimized modulation methods where circulating transformer currents and switching losses are reduced, which is addressed in Chapter 5.

The development of the loss model has shown that the critical parts of the converter are the resistive losses on the LV side as well as switching losses. The losses on the LV side are considerably higher than on the HV side, even though the LV side contains eight switches in parallel and occupies twice the volume of the high voltage side.

Therefore, the following issues must be considered carefully in the design of a low voltage and high current converter to achieve high efficiency:

- Circulating transformer currents should be as small as possible.
- The impact of high frequency skin and proximity effects must be considered (transformer and PCB).
- LV side switching should occur at low currents.

	<i>Maximum relative difference</i>	<i>Maximum absolute difference</i>	<i>Average relative difference</i>	<i>Average absolute difference</i>
Simple Model	56.4%	135 W	44.0%	56.3 W
Accurate conduction losses	46.1%	67 W	31.1%	39.8 W
Accurate conduction and switching losses	17.4%	47 W	6.3%	8.1 W
Full model (Figure 4.30)	17.1%	16 W	6.0%	7.1 W

Table 4.2: Differences between calculated and measured losses.

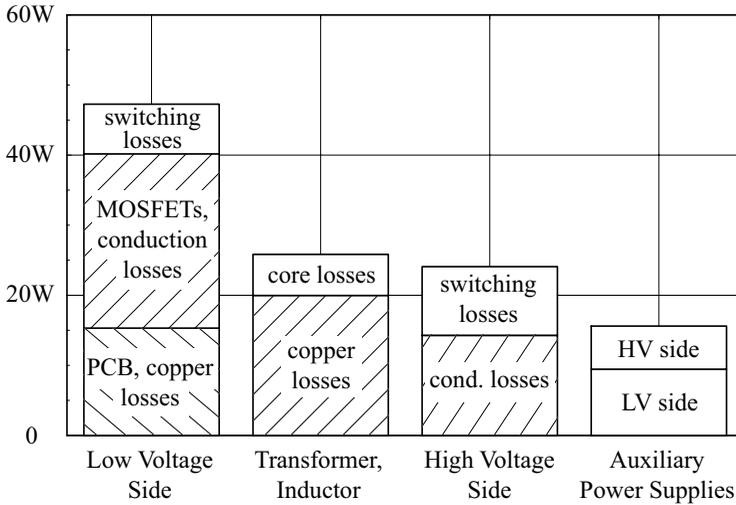


Figure 4.31: Calculated distribution of the power losses for operation at $V_1 = 340$ V, $V_2 = 12$ V, and $P_2 = 2$ kW.

One important aspect is the layout of the LV side PCB in order to achieve good current distribution in the PCB and between the parallel connected MOSFETs (cf. Appendix A.2.3). On the LV side, the transformer winding termination needs to be designed carefully due to high frequency losses (Appendix A.2.4). A model with calculated resistance and switching loss values can be used in a first step to design the system and can be refined with measurement results from a prototype.

4.7 Conclusion

An accurate power loss model for a bidirectional DC-DC converter with a high current/low voltage port is developed. It shows that switching losses and the LV side conduction losses are most critical for the design of the converter. Calculated results are compared to measurements obtained from a 2kW experimental system in order to verify the loss model. Based on this model the expected converter efficiency as well as the distribution of the power losses in the converter are calculated. This in-depth knowledge facilitates the development of efficiency optimized modulation schemes (Section 5.2) and enables the efficiency optimized converter design presented in Appendix A.2.

Even though, the discussion's focus is on a high current DAB, the general nature of the presented methods enables an accurate prediction of the power losses of other DC-DC converter topologies operated at high switching frequencies; the presented approach is particularly suitable for power converters that exhibit large current ripples. The method could thus as well be applied to automotive power converters with high power density [88] or resonant DC-DC converters with a high current port (Appendix A.4).

Chapter 5

Advanced DAB Modulation Schemes

According to Chapter 3, high transformer and switch RMS currents result if the DAB converter employs the conventional phase shift modulation. Alternative modulation schemes, e.g. the triangular and trapezoidal current mode modulation schemes (Section 3.1.3, Section 3.1.3, [97]) and the modulation schemes with minimum transformer RMS current (Section 3.1.3), cause lower RMS currents and thus, lower converter losses are expected.

The DAB converter, however, not only generates conduction losses: depending on the actual operating point (given V_1 , V_2 , and P_{out}), switching losses may contribute a considerable percentage of the total losses (Chapter 4).

In the present chapter, in Section 5.1, a suitable extension of the triangular and trapezoidal current mode modulation schemes is discussed (Section 5.1.1) and applied to the DAB loss model (Section 5.1.2). The resulting modulation schemes are further improved in Section 5.2 based on the findings obtained from a thorough optimization of the DAB modulation method with respect to the total converter losses.

5.1 Extended Triangular and Trapezoidal Current Mode Modulation

Figure 5.1 depicts the converter efficiencies calculated for different modulation schemes, different operating voltages, and different power levels P_2 . Obviously, compared to phase shift modulation, a major improvement is achieved with the triangular and trapezoidal current mode modulation schemes [Figures 5.1 (c) and (d)].¹ With these modulation schemes, however,

¹The efficiency calculation employed to obtain the results depicted in Figure 5.1 considers the effect of the linear interpolation, used by the DSP, to determine the actual

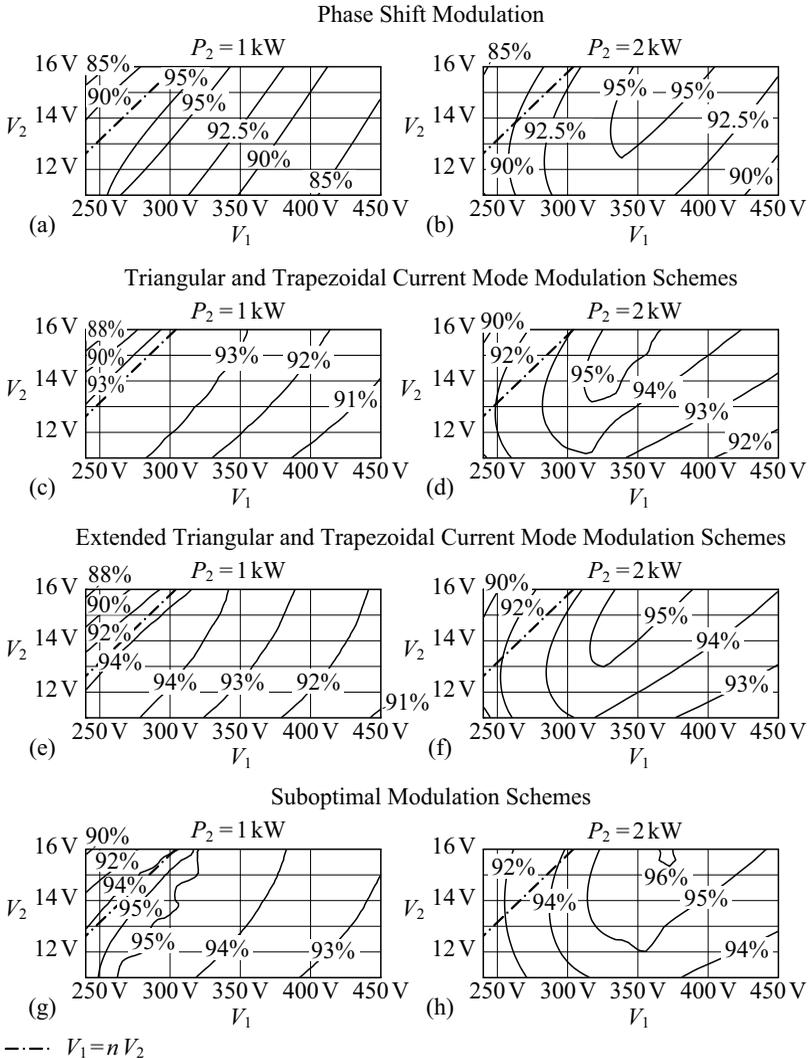


Figure 5.1: Comparison of the efficiencies calculated for different modulation schemes and different power levels P_2 ; (a) and (b) phase shift modulation ($n = 19$, $L = 26.7 \mu\text{H}$); (c) and (d) triangular and trapezoidal current mode modulation schemes according to [97] ($n = 19$, $L = 18.7 \mu\text{H}$); (e) and (f) extended triangular and trapezoidal current mode modulation schemes (Section 5.1; $n = 19$, $L = 18.7 \mu\text{H}$); (g) and (h) suboptimal modulation schemes (Section 5.2.2; $n = 19$, $L = 26.7 \mu\text{H}$). The calculation considers the effect of the linear interpolation used by the DSP to determine the actual modulation parameters (Appendix E.2). The efficiency is calculated for $T_j = 25^\circ\text{C}$ (cf. Chapter 4).

hard switching processes at zero transformer current occur, which cause high switching losses on the HV side (cf. Section 4.3.2, Figure 4.14). The extended triangular and trapezoidal current mode modulation schemes discussed in this Section operate the HV side full bridge with ZVS and thus, further efficiency improvements are achieved [Figures 5.1 (e) and (f)]. Finally, with the suboptimal modulation schemes discussed in Section 5.2.2, converter efficiencies close to the optimum efficiencies are achieved [Figures 5.1 (g) and (h), Figure 5.28].

5.1.1 Working Principle

According to Section 3.1.3, the triangular and trapezoidal current mode modulation schemes employ 3 different operating modes of the DAB:

- *Mode a*: triangular current mode, $V_1 > nV_2 \wedge 0 < |P| \leq P_{\Delta,a,\max}$
- *Mode b*: triangular current mode, $V_1 < nV_2 \wedge 0 < |P| \leq P_{\Delta,b,\max}$
- *Mode c*: trapezoidal current mode,
 $(V_1 > nV_2 \wedge P_{\Delta,a,\max} < |P| \leq P_{\Delta,\max}) \vee$
 $(V_1 < nV_2 \wedge P_{\Delta,b,\max} < |P| \leq P_{\Delta,\max})$

Within the subsequent sections, the 3 operating modes are separately improved with respect to converter efficiency; the resulting modulation schemes are termed extended triangular and trapezoidal current mode modulation schemes. Due to the implemented changes, however, the transition conditions change:

- *Mode a*: extended triangular current mode,
 $V_{2,\text{lim}} > V_2 \wedge 0 < |P| \leq P_{\Delta,a,\max}$
- *Mode b*: extended triangular current mode,
 $V_{2,\text{lim}} < V_2 \wedge 0 < |P| \leq P_{\Delta,b,\max}$
- *Mode c*: extended trapezoidal current mode,
 $(V_{2,\text{lim}} > V_2 \wedge P_{\Delta,a,\max} < |P| \leq P_{\Delta,\max}) \vee$
 $(V_{2,\text{lim}} < V_2 \wedge P_{\Delta,b,\max} < |P| \leq P_{\Delta,\max})$

Thus, besides different values for $P_{\Delta,a,\max}$, $P_{\Delta,b,\max}$, and $P_{\Delta,\max}$, the new variable $V_{2,\text{lim}}$ is introduced [cf. (5.7) and Figure 5.24].

Since this Section focuses on the working principles of the employed extended triangular and trapezoidal current mode modulation schemes, the lossless electric DAB model is used to generate all equations and Figures. Accordingly, equal power levels occur for port 1 and port 2, i.e. $P_1 = P_2 = P$.

modulation parameters (Appendix E.2). This causes the irregular characteristics of the depicted contour lines.

Again, positive power values denote a power transfer from port 1 to port 2 (HV to LV) and negative power values denote a power transfer from port 2 to port 1 [cf. (3.14)].

Triangular Current Mode Modulation Revisited

Mode a, $V_{2,\text{lim}} > V_2$. The unmodified triangular current mode modulation scheme generates transformer currents according to the currents depicted in Figure 3.7 and Figure 3.8, i.e. the LV side full bridge solely switches at zero transformer current causing low switching losses (cf. Section 4.3.3); once per half period, the HV side full bridge switches zero transformer current, too, which causes high switching losses (Section 4.3.2).

With respect to low total switching losses, the modulation scheme needs to be modified, such that the LV side full bridge continues to switch at zero current and the HV side full bridge is operated with ZVS. The required modification to the modulation scheme introduces circulating transformer currents (Figure 5.2), needed to achieve ZVS on the HV side (for the given hardware prototype, the reduced switching losses more than outweigh the slightly increased conduction losses, cf. Section 5.2.1, Figure 5.17).

With this modified triangular modulation scheme, the maximum achieved power is far below the maximum possible power of the DAB [cf. (3.27), Section 3.1.3]. However, different to the original triangular current mode modulation, no direct transition to a high power modulation scheme (e.g. trapezoidal current mode modulation) exists; the transition between low and high power operation rather includes an intermediate modulation scheme (Figure 5.3) which considerably increases the complexity of the modulator.

Figure 5.4 depicts a different extension of the triangular current mode modulation scheme which also enables the actual hardware prototype to achieve a high converter efficiency (i.e. considerably higher than the efficiency achieved with the unmodified triangular current mode modulation scheme). The modulation scheme shown in Figure 5.4 furthermore facilitates a seamless transition to high power modulation schemes (e.g. the extended trapezoidal current mode modulation scheme discussed below, cf. Figure 5.6). There, a certain transformer current remains during the freewheeling time interval, $t_3 < t < T_S/2$, which enables ZVS of the HV side full bridge at $t = T_S/2$; at $t = t_1$, the LV side full bridge switches at zero transformer current is achieved at $t = t_1$. The implemented modification, however, increases the transformer RMS current and causes the LV side full bridge to perform hard switching processes at $t = t_3$ and $t = t_7$. Still, with this extended triangular current mode modulation, increased converter efficiency is achieved (compared to the original triangular current mode modulation), since the full bridge on the

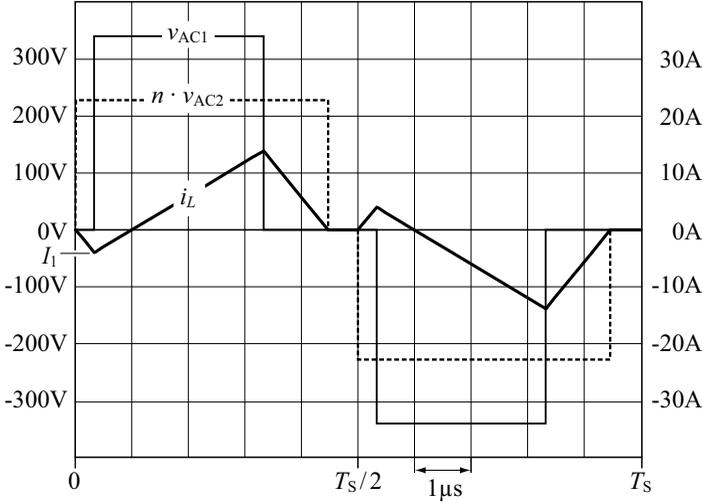


Figure 5.2: Modified triangular current mode modulation which enables HV side ZVS and LV side switching at zero transformer current; $V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$, $P = 1\text{ kW}$, $n = 19$, $L = 18.7\text{ }\mu\text{H}$, and $f_s = 100\text{ kHz}$.

LV side causes comparably low switching losses when operated with hard switching (Figure 4.22).

Based on the lossless electric DAB model, the required duty cycles and the required phase shift angle are determined with:

$$D_1 = \frac{1}{\pi} \frac{nV_2}{V_1 - nV_2} |\varphi| + \frac{2f_s L (-I_0)}{V_1}, \tag{5.1}$$

$$D_2 = \frac{1}{\pi} \frac{V_1}{V_1 - nV_2} |\varphi|, \tag{5.2}$$

$$\varphi = \frac{\pi f_s L I_0}{nV_1 V_2} \left[V_1 - nV_2 - \sqrt{V_1 (V_1 - nV_2) \left(1 + \frac{|P|}{f_s L I_0^2} \right)} \right] \text{sgn}(P) \tag{5.3}$$

$$\forall V_2 < V_{2,\text{lim}} \wedge P_{\Delta,a,\text{min}} < |P| \leq P_{\Delta,a,\text{max}} \tag{5.4}$$

(with given operating voltages V_1 and V_2 , the DAB power level P , and the current $I_0 = i_L(0)$ required to achieve ZVS on the HV side).

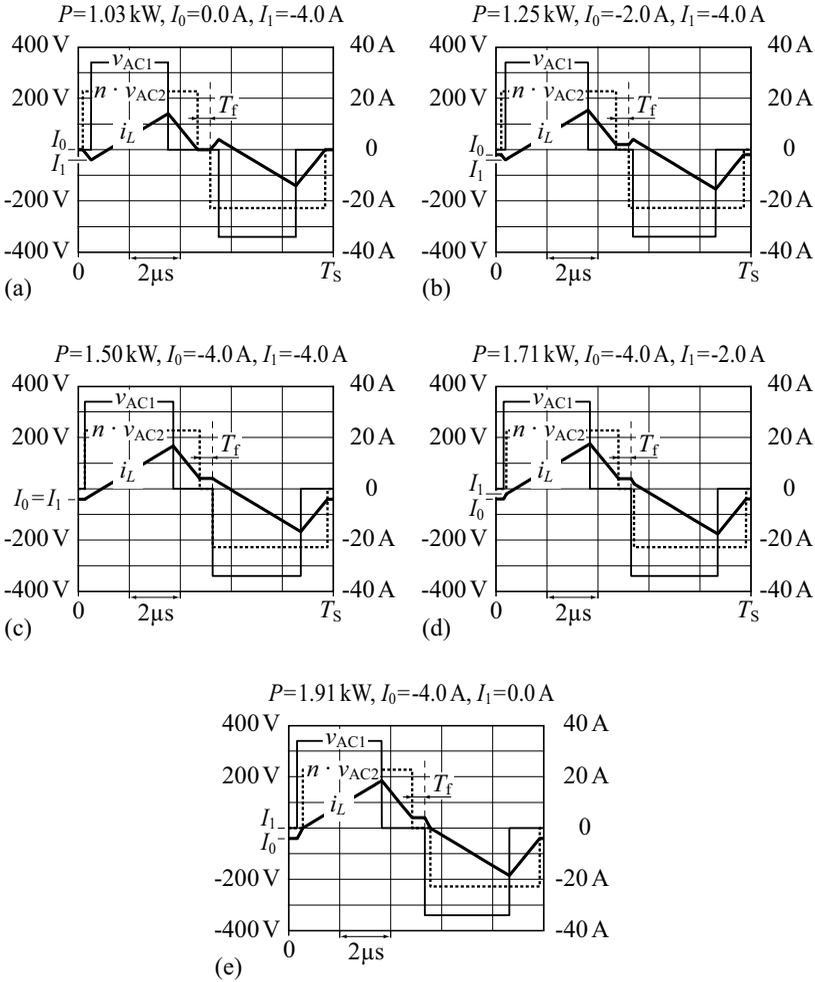


Figure 5.3: Sequence of DAB operating modes required to transit from low power levels (modified triangular current mode modulation scheme, Figure 5.2) to high power levels (extended trapezoidal current mode modulation scheme, Figure 5.6): (a) maximum power achieved with the operating mode depicted in Figure 5.2 and with $T_f = 500$ ns; (b), (c), and (d) continuously increasing DAB power levels, achieved with the extended triangular current mode modulation depicted in Figure 5.4; (e) continuous transition to the extended trapezoidal current mode modulation (Figure 5.6); $V_1 = 340$ V, $V_2 = 12$ V, $n = 19$, $L = 18.7$ μ H, and $f_s = 100$ kHz; a minimum freewheeling time of $T_f = 500$ ns is selected in order to obtain a clear illustration.

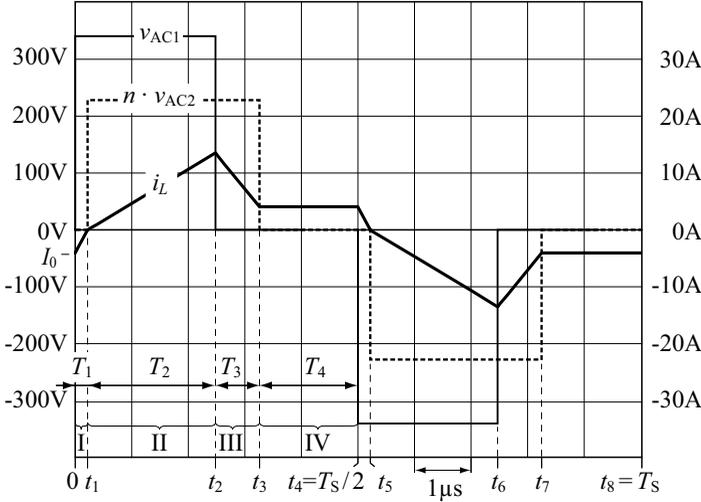


Figure 5.4: Extended triangular current mode modulation scheme (*mode a*), which enables ZVS on the HV side and allows for a direct transition to the extended trapezoidal current mode modulation scheme; $V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$, $P = 1\text{ kW}$, $n = 19$, $L = 18.7\text{ }\mu\text{H}$, and $f_s = 100\text{ kHz}$.

The operating range is limited according to:

$$P_{\Delta,a,\min} = \frac{nV_2}{V_1 - nV_2} f_s L I_0^2, \quad (5.5)$$

$$P_{\Delta,a,\max} = \frac{(nV_2)^2 (V_1 - nV_2)}{4f_s L V_1} \left[4f_s L (1 - 2f_s T_f) (-I_0) \frac{V_1 - nV_2}{nV_1 V_2} + (1 - 2f_s T_f)^2 - 4(f_s L)^2 I_0^2 \frac{3V_1^2 - 3nV_1 V_2 + (nV_2)^2}{V_1^3 nV_2 - (nV_1 V_2)^2} \right], \quad (5.6)$$

$$nV_{2,\lim} = V_1 + \frac{1}{\frac{1}{V_1} + \frac{T_f}{L(-I_0)} - \frac{1}{2f_s(-I_0)L}} \quad (5.7)$$

(T_f denotes the minimum length of the freewheeling time interval, cf. Figure 5.3 (e), [97]).

Mode b, $V_{2,\lim} < V_2$. For triangular current mode modulation with $V_{2,\lim} < V_2$, the HV side full bridge solely switches at zero transformer current and the LV side full bridge alternately switches at zero current, i.e. $I_{S2,sw} = 0$, and at $I_{S2,sw} > 0$ (Figure 3.10 and Figure 3.11; cf. Table 4.1 regarding $I_{S2,sw}$).

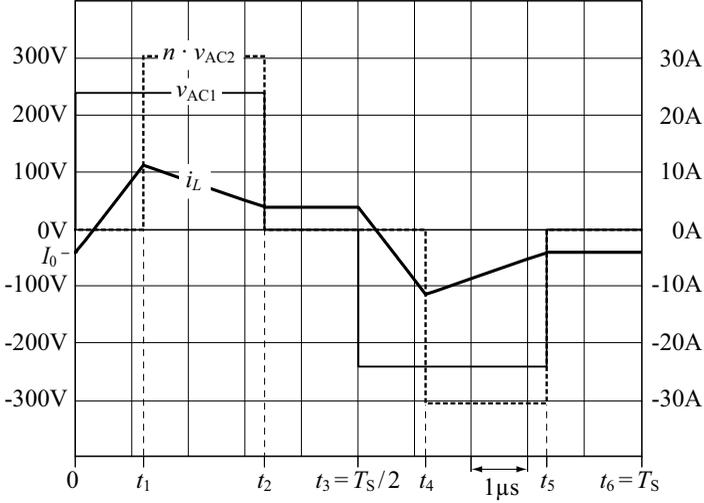


Figure 5.5: Extended triangular current mode modulation scheme (*mode b*), which enables ZVS on the HV side for $V_{2,\text{lim}} < V_2$; $V_1 = 240\text{ V}$, $V_2 = 16\text{ V}$, $P = 1\text{ kW}$, $n = 19$, $L = 18.7\text{ }\mu\text{H}$, and $f_s = 100\text{ kHz}$.

Similar to *mode a*, a reduction of the switching losses on the HV side (i.e. ZVS operation) is achieved with the extended triangular current mode modulation scheme (*mode b*) depicted in Figure 5.5: the freewheeling current during $t_2 < t < T_S/2$ enables ZVS operation on the HV side, however, increases the transformer RMS current and causes hard switching processes on the LV side at $t = t_2$ and at $t = t_5$.

For a given operating point (given V_1 , V_2 , and P), the required duty cycles and the phase shift angle are:

$$D_1 = \frac{1}{\pi} \frac{nV_2}{nV_2 - V_1} |\varphi| - \frac{2f_s L (-I_0)}{nV_2 - V_1}, \quad (5.8)$$

$$D_2 = \frac{1}{\pi} \frac{V_1}{nV_2 - V_1} |\varphi| - \frac{2f_s L (-I_0)}{nV_2 - V_1}, \quad (5.9)$$

$$\varphi = \frac{\pi f_s L (-I_0)}{V_1} \left[1 + \sqrt{1 + \frac{nV_2 - V_1}{nV_2} \frac{|P|}{f_s L I_0^2}} \right] \text{sgn}(P) \quad (5.10)$$

$$\forall (V_2 < V_{2,\text{lim}} \wedge |P| \leq P_{\Delta,\text{a,min}}) \vee (V_2 \geq V_{2,\text{lim}} \wedge |P| \leq P_{\Delta,\text{b,max}}) \quad (5.11)$$

[using the lossless electric DAB model, the current $I_0 = i_L(0)$ required to achieve ZVS, and (5.7)]. The useful range of the above equations is limited

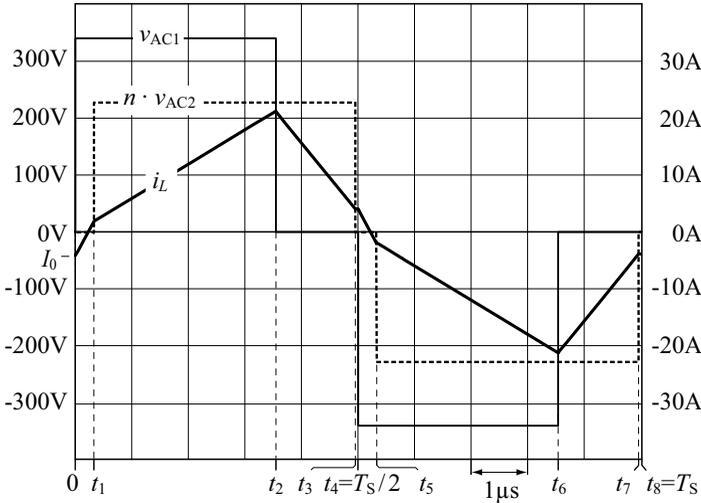


Figure 5.6: Extended trapezoidal current mode modulation scheme, which enables HV side ZVS and high power operation of the DAB; $V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$, $P = 2.5\text{ kW}$, $n = 19$, $L = 18.7\text{ }\mu\text{H}$, and $f_s = 100\text{ kHz}$.

with (5.5) and

$$P_{\Delta, b, \max} = 4f_s L I_0^2 \frac{V_1}{nV_2} \left[V_1 \frac{1 - 2f_s T_f}{4f_s L (-I_0)} - 1 \right] \left[(nV_2 - V_1) \frac{1 - 2f_s T_f}{4f_s L (-I_0)} + 1 \right]. \tag{5.12}$$

Extended Trapezoidal Current Mode Modulation

The trapezoidal current mode modulation scheme (Figure 3.12, and Figure 3.13) requires the HV side full bridge to alternately switch at $I_{S1,sw} = 0$ (hard switching process) and at $I_{S1,sw} > 0$ (ZVS). Similarly, the LV side full bridge alternately switches at $I_{S2,sw} = 0$ and at $I_{S2,sw} > 0$.

In order to avoid hard switching processes on the HV side, the current $I_0 = i_L(0)$ is shifted accordingly, which, however, causes the transformer RMS current to increase and introduces hard switching processes on the LV side at $t = t_3$ and at $t = t_7$ (Figure 5.6). (Again, a minimum freewheeling time $T_f = T_s/2 - t_3$ may be used to avoid overlapping of the transformer voltages v_{AC1} and v_{AC2} at $t = kT_s/2$, $k \in \mathbb{Z}$, caused by different time delays of the employed semiconductor; cf. Section 4.3.2 and Section 4.3.3.)

Based on the lossless electric DAB model, the modulation parameters of the extended trapezoidal current mode modulation scheme (*mode c*) for a given operating point (V_1 , V_2 , and P) are calculated with:

$$D_1 = \frac{nV_2(1 - 2f_s T_f) + 2f_s L(-I_0)}{V_1 + nV_2} - \frac{nV_2}{\pi(V_1 + nV_2)} |\varphi|, \quad (5.13)$$

$$D_2 = \frac{V_1(1 - 2f_s T_f) - 2f_s L(-I_0)}{V_1 + nV_2} - \frac{V_1}{\pi(V_1 + nV_2)} |\varphi|, \quad (5.14)$$

$$\varphi = \frac{\pi}{V_1^2 + nV_1V_2 + (nV_2)^2} \left[-f_s T_f (V_1^2 + (nV_2)^2) + \frac{V_1^2 - 2f_s L(-I_0)(V_1 - nV_2) + (nV_2)^2 - (V_1 + nV_2)\sqrt{f}}{2} \right] \text{sgn}(P) \quad (5.15)$$

$$\forall (V_2 < V_{2,\text{lim}} \wedge P_{\Delta,\text{a,max}} < |P| \leq P_{\Delta,\text{max}}) \vee (V_2 \geq V_{2,\text{lim}} \wedge P_{\Delta,\text{b,max}} < |P| \leq P_{\Delta,\text{max}}), \quad (5.16)$$

using (5.6), (5.7), (5.12), and

$$\begin{aligned} f &= nV_1V_2 + 4f_s L(-I_0)[V_1 - nV_2 - 3f_s L(-I_0)] \\ &\quad - 4f_s L|P| \frac{V_1^2 + nV_1V_2 + (nV_2)^2}{nV_1V_2} \\ &\quad + 4f_s T_f [2f_s L(-I_0)(nV_2 - V_1) + nV_1V_2(f_s T_f - 1)]. \end{aligned} \quad (5.17)$$

The maximum possible power is limited according to:

$$P_{\Delta,\text{max}} = \frac{nV_1V_2}{4f_s L[V_1^2 + nV_1V_2 + (nV_2)^2]} [4f_s L(1 - 2f_s T_f)(-I_0)(V_1 - nV_2) - 12(f_s L)^2 I_0^2 + nV_1V_2(1 - 2f_s T_f)^2]. \quad (5.18)$$

Summary of the Extended Triangular and Trapezoidal Current Mode Modulation Schemes

Very low power operation. At DAB power levels close to zero, the operation using the *mode b* extended triangular current mode modulation is always possible [Figures 5.7 (a) and (b)].²

²According to Figures 5.7 (a) and (b) almost a trapezoidal current i_L results at very low power operation, due to the current I_0 , which is required to achieve ZVS.

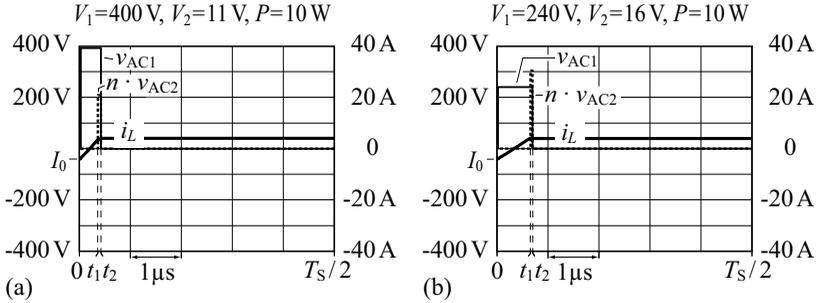


Figure 5.7: Extended triangular current mode modulation (*mode b*) at very low power levels: (a) $V_1 = 400 \text{ V}$, $V_2 = 11 \text{ V}$, $P = 10 \text{ W}$ and (b) $V_1 = 240 \text{ V}$, $V_2 = 16 \text{ V}$, $P = 10 \text{ W}$; $I_0 = -4 \text{ A}$, $n = 19$, $L = 18.7 \mu\text{H}$, and $f_S = 100 \text{ kHz}$. Only the first half-cycle is shown; the waveforms repeat with opposite sign during the second half-cycle. The inductor current i_L is almost trapezoidal at very low power levels, due to the current I_0 , which is required to achieve ZVS.

Low and medium power operation. With increasing power levels, the current I_1 depicted in Figure 5.8 (a) decreases and becomes zero at $|P| = P_{\Delta a, \min}$ [Figure 5.8 (b)]; simultaneously, t_2 increases and becomes equal to $T_S/2 - T_f$ at $|P| = P_{\Delta b, \max}$. For $V_2 = V_{2, \text{lim}}$, the power limits $P_{\Delta a, \min}$, $P_{\Delta a, \max}$, and $P_{\Delta b, \max}$ are all equal, i.e. the useful range of *mode a* becomes zero. Consequently, *mode a* applies for $V_2 < V_{2, \text{lim}}$ and $P_{\Delta a, \min} < |P| < P_{\Delta a, \max}$ [Figure 5.9 (a)] and *mode b* applies for $V_2 \geq V_{2, \text{lim}}$ and $|P| < P_{\Delta b, \max}$ [Figure 5.9 (b)].

High power operation. For DAB power levels exceeding $P_{\Delta a, \max}$ or $P_{\Delta b, \max}$ (for $V_2 < V_{2, \text{lim}}$ or $V_2 \geq V_{2, \text{lim}}$, respectively), the trapezoidal current mode modulation scheme (*mode c*) is employed.

Selection of I_0

With the employed HV MOSFETS (CoolMOS SPW47N60CFD) and the selected dead time used to avoid a shoot-through in the half bridge ($T_{\text{deadtime}} = 200 \text{ ns}$), I_0 could be set to $\approx -2 \text{ A}$, based on the switching losses depicted in Figure 4.15. However, different to the switching loss measurement, the current in the actual DAB may considerably change during the dead time interval and thus, $I_0 < -2 \text{ A}$ is required to obtain ZVS (cf. Section 4.3.2).

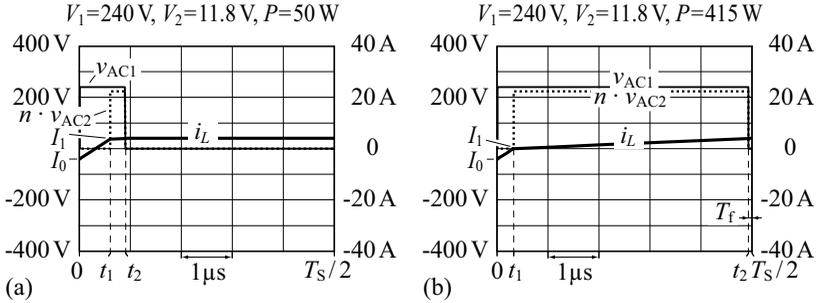


Figure 5.8: Extended triangular current mode (*mode b*) modulation at low power levels: (a) $V_1 = 240\text{ V}$, $V_2 = V_{2,\text{lim}} = 11.8\text{ V}$, $P = 50\text{ W} < P_{\Delta b,\text{max}}$ and (b) $V_1 = 240\text{ V}$, $V_2 = V_{2,\text{lim}} = 11.8\text{ V}$, $P = P_{\Delta b,\text{max}} = 415\text{ W}$; $I_0 = -4\text{ A}$, $n = 19$, $L = 18.7\text{ }\mu\text{H}$, and $f_S = 100\text{ kHz}$. For $V_2 = V_{2,\text{lim}}$ and $P = P_{\Delta b,\text{max}}$, t_2 becomes equal to $T_S/2 - T_f$ and $I_1 = i_L(t_1)$ becomes zero. Only the first half-cycle is shown; the waveforms repeat with opposite sign during the second half-cycle.

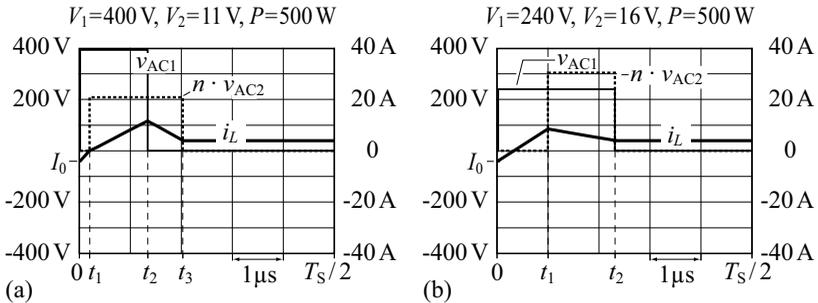


Figure 5.9: Extended triangular current mode modulation at medium power levels: (a) *mode a*, $V_1 = 400\text{ V}$, $V_2 = 11\text{ V}$, $P = 500\text{ W}$ and (b) *mode b*, $V_1 = 240\text{ V}$, $V_2 = 16\text{ V}$, $P = 500\text{ W}$; $I_0 = -4\text{ A}$, $n = 19$, $L = 18.7\text{ }\mu\text{H}$, and $f_S = 100\text{ kHz}$. Only the first half-cycle is shown; the waveforms repeat with opposite sign during the second half-cycle.

The measurement setup depicted in Figure 5.10 (a) is used to determine reasonable values for I_0 . During $t_{0b} < t < t_{1a}$, the full bridge circuit applies

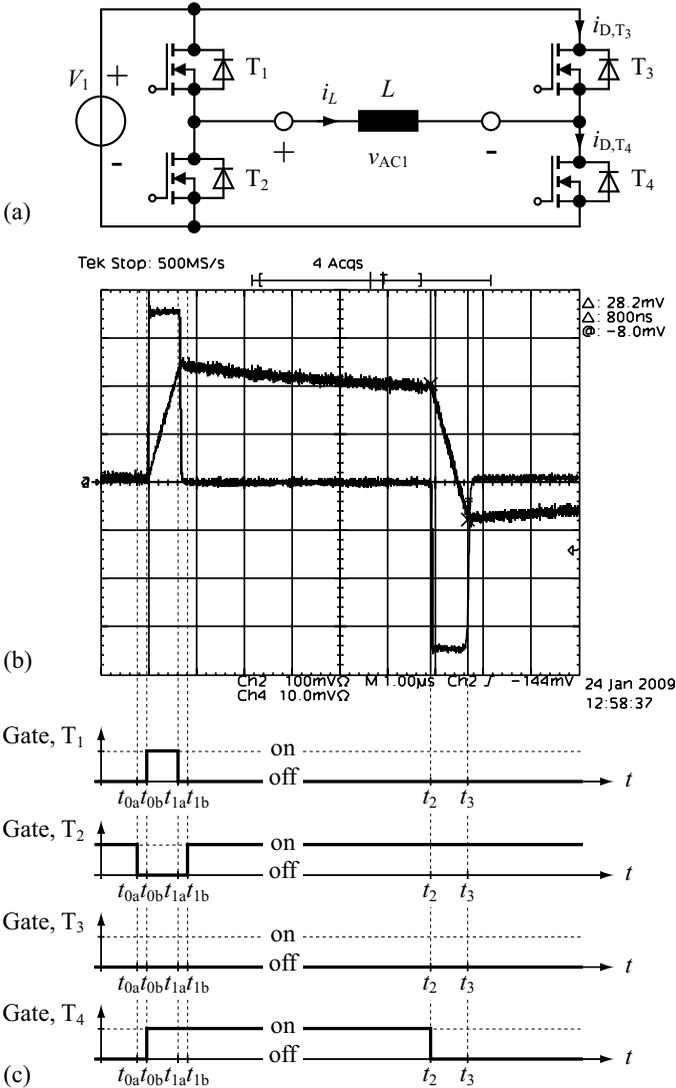


Figure 5.10: (a) Full bridge measurement setup used to obtain reasonable values for I_0 ; (b) measured waveforms $v_{AC1}(t)$ and $i_L(t)$ for $V_1 = 350\text{ V}$, $i_L(t_2) = 10\text{ A}$, $L = 20\text{ }\mu\text{H}$, and $T_j = 25^\circ\text{C}$: with the selected MOSFETs (SPW47N60CFD), $I_0 = i_L(t_3) \approx -4\text{ A}$ occurs; (c) gate signals required to obtain the depicted voltage waveform $v_{AC1}(t)$.

positive voltage to the inductor L in order to increase i_L . The subsequent freewheeling time interval ($t_{1a} < t < t_2$) is used to accurately adjust $i_L(t_2)$, since the inductor current slightly decreases due to resistive losses. At $t = t_2$, T_4 turns off and the body diode of T_3 conducts during $t_2 < t < t_3$ with $i_{D,T_3}(t) = -i_L(t)$. Consequently, negative voltage, $v_{AC1}(t) = -V_1$, is applied to L , which causes the inductor current to drop quickly. At $t = t_3$, the diode reverse recovery charge is removed, the drain-to-source capacitances of T_3 and T_4 are charged or discharged, and thus, $v_{AC1}(t)$ changes from $-V_1$ to zero.

The value of the peak reverse current determines the actual value of I_0 [i.e. $I_0 = i_L(t_3)$]; I_0 depends on the supply voltage V_1 , the current slope di_L/dt , the initial diode current $i_L(t_2)$, and the junction temperature T_j (Figure 5.11). Similar to the switching loss measurements, the polynomial function

$$I_0(di_L/dt, V_1, i_L(t_2), T_j) = a + \begin{matrix} b_1 di_L/dt + \\ c_1 V_1 di_L/dt + \\ c_4 V_1 i_L(t_2) + \end{matrix} \begin{matrix} b_2 V_1 + \\ c_2 i_L(t_2) di_L/dt + \\ c_5 V_1 T_j + \end{matrix} \begin{matrix} b_3 i_L(t_2) + \\ c_3 T_j di_L/dt + \\ c_6 T_j i_L(t_2) \end{matrix} + b_4 T_j + \quad (5.19)$$

with the constant coefficient a , 4 linear terms with the coefficients b_1, b_2, b_3 , and b_4 , and 6 product terms (coefficients $c_1 \dots c_6$), is fitted to the measurement data by means of least mean square optimization. The minimum of the average over all absolute values of the relative error,

$$e_{\text{avg}} = \frac{1}{m} \sum_{i=1}^m |e_i|, \quad e_i = \frac{I_{0,\text{calc},i} - I_{0,\text{meas},i}}{I_{0,\text{meas},i}}, \quad (5.20)$$

($m = 99$ denotes the total number of measurements; $I_{0,\text{meas},i}$ and $I_{0,\text{calc},i}$ denote the i -th measured and calculated values of I_0 , respectively), $\min(e_{\text{avg}}) \approx 2.5\%$, is obtained for

$$\begin{aligned} a &= -269 \text{ mA}, \\ b_1 &= 132 \text{ ns}, & b_2 &= -5.09 \text{ mA/V}, & b_3 &= 79.8 \text{ mA/A}, & b_4 &= 0, \\ c_1 &= -119 \text{ ps/V}, & c_2 &= 5.08 \text{ ns/A}, & c_3 &= 222 \text{ ps/K}, \\ c_4 &= 0, & c_5 &= 7.72 \text{ } \mu\text{A}/(\text{VK}), & c_6 &= -1.39 \cdot 10^{-3} \text{ K}^{-1}. \end{aligned} \quad (5.21)$$

With $di_L/dt = -V_1/L$ and for constant L, T_j , and $i_L(t_2)$, the relation between V_1 and I_0 becomes almost linear (Figure 5.12), e.g. for $L = 18.7 \text{ } \mu\text{H}$, $T_j = 125^\circ\text{C}$, and $i_L(t_2) = 2 \text{ A}$,

$$I_0(V_1)|_{L=18.7 \text{ } \mu\text{H}} = -1.19 \text{ A} - 8.82 \text{ mA/V} \cdot V_1 \quad (5.22)$$

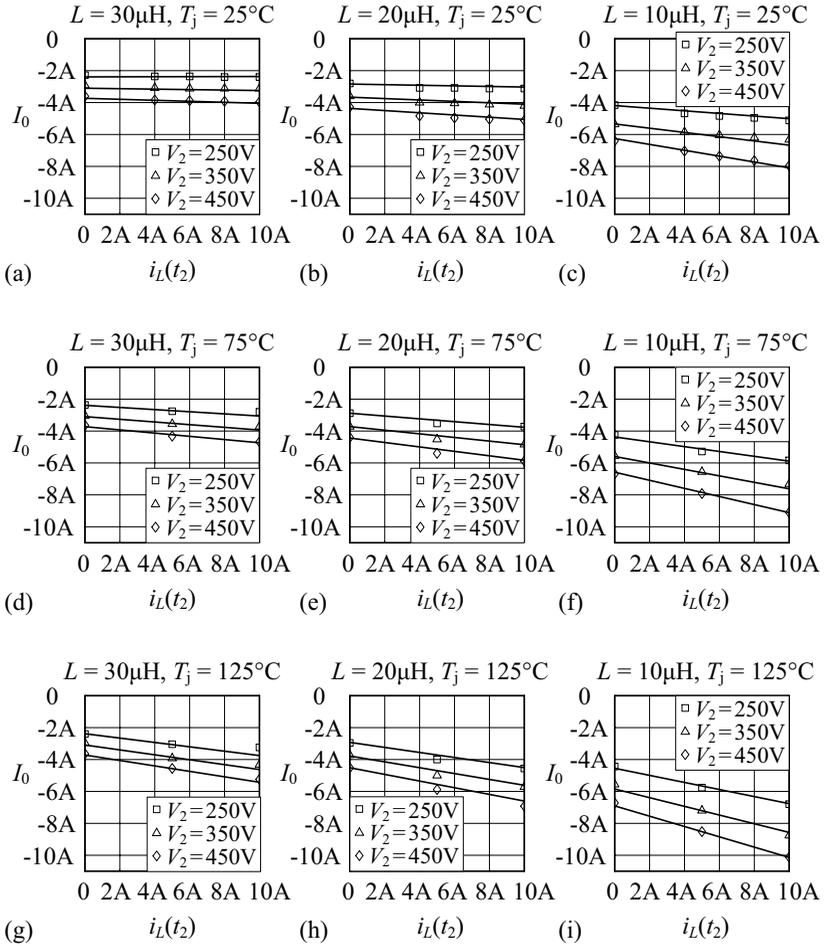


Figure 5.11: Measured peak reverse currents $i_L(t_3)$ for different supply voltages V_1 , different inductances L and different junction temperatures T_j ; the measured values are obtained from the full bridge circuit depicted in Figure 5.10 with CoolMOS SPW47N60CFD MOSFETs being employed. The solid lines are calculated with (5.19).

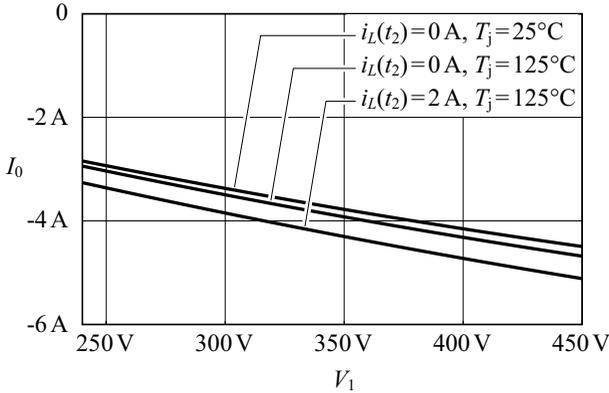


Figure 5.12: Evaluated polynomial function (5.19) using $di_L/dt = -V_1/L$, $L = 18.7 \mu\text{H}$, and different values for $i_L(t_2)$ and T_j : for constant L , $i_L(t_2)$, and T_j an almost linear relation between V_1 and I_0 results.

results;³ for $L = 26.7 \mu\text{H}$, $T_j = 125^\circ\text{C}$, and $i_L(t_2) = 2 \text{ A}$, $I_0(V_1)$ is approximately given with

$$I_0(V_1)|_{L=26.7 \mu\text{H}} = -0.97 \text{ A} - 7.41 \text{ mA/V} \cdot V_1. \quad (5.23)$$

5.1.2 Application of the DAB Loss Model

According to Chapter 4, the lossless DAB model (Figure 3.2) is insufficient to accurately predict the actual DAB output power P_{out} [cf. (3.71)]. Consequently, the equations to calculate the DAB control parameters D_1 , D_2 , and φ for a given output power presented in Section 5.1.1 (based on the lossless DAB model) cause the DAB hardware prototype to inaccurately set P_{out} and I_0 .

More precise values for D_1 , D_2 , and φ are achieved with the numerical solver discussed in Section 4.6.1. On-line parameter calculation, however, is not feasible due to the limited DSP processing power. Therefore, in a more

³The actually required value of $|I_0|$ may be lower due to a lower $|di_L/dt|$ at the switching instant (i.e. for power being transferred from the HV port to the LV port, cf. Figure 5.4 and Figure 5.5); however, for the opposite power transfer direction and once per half-cycle, a switching process similar to the process at $t = t_3$, depicted in Figure 5.10, occurs. Thus, in order to cover the worst case, I_0 is selected according to (5.19) by setting $di_L/dt = -V_1/L$.

practical approach, the DSP stores the control parameters D_1 , D_2 , and φ , precalculated for dedicated output power levels P_{out} and voltages V_1 and V_2 , in three-dimensional tables and employs a fast linear interpolation algorithm to compute the actually required control parameters (Appendix E.2).

The off-line calculation of the control parameters considers the 3 different operating modes of the DAB (i.e. 2 triangular current modes and 1 trapezoidal current mode), separately.

Mode a, triangular current mode (cf. Figure 5.4). In order to reduce the computational effort, the time $T_{I_0} = t_1 - 0$, required to enable ZVS, is approximated with

$$T_{I_0} = \frac{L |I_0|}{V_1} \quad (5.24)$$

and thus,

$$D_1 = D_2 - \frac{|\varphi|}{\pi} + 2T_{I_0} f_s \quad (5.25)$$

applies (cf. Figure 5.4 and Figure 3.3). A numerical search algorithm seeks for suitable values D_2 and φ that meet the requirements

$$P_{\text{out}}(D_1, D_2, \varphi) = P_{\text{out,d}}, \quad (5.26)$$

$$I_0(D_1, D_2, \varphi) = I_{0,d} \quad (5.27)$$

$$\forall V_2 < V_{2,\text{lim}} \wedge |P_{\text{out},\Delta,a,\text{min}}| < |P_{\text{out}}| \leq |P_{\text{out},\Delta,a,\text{max}}| \quad (5.28)$$

in order to achieve the designated output power $P_{\text{out,d}}$ and the designated freewheeling current $I_{0,d}$.⁴

The numerical solver as well computes $P_{\text{out},\Delta,a,\text{min}}$ and $P_{\text{out},\Delta,a,\text{max}}$: for $P_{\text{out},\Delta,a,\text{min}}$, $D_1 - D_2 = T_{I_0} f_s$ applies; thus, using (5.25),

$$\begin{aligned} [I_0(D_1, D_2, \varphi) = I_{0,d} \wedge D_1 = D_2 + T_{I_0} f_s \wedge \varphi = \pi T_{I_0} f_s \text{sgn}(P_{\text{out,d}})] \\ \Leftrightarrow P_{\text{out}}(D_1, D_2, \varphi) = P_{\text{out},\Delta,a,\text{min}}, \text{ search variable: } D_2, \end{aligned} \quad (5.29)$$

needs to be solved with respect to $P_{\text{out},\Delta,a,\text{min}}$. At $P_{\text{out}} = P_{\text{out},\Delta,a,\text{max}}$,

$$\begin{aligned} [I_0(D_1, D_2, \varphi) = I_{0,d} \wedge D_1 = D_2 - \frac{|\varphi|}{\pi} + 2T_{I_0} f_s \wedge D_2 = \frac{1}{2} - (T_{I_0} + T_{\text{f}}) f_s] \\ \Leftrightarrow P_{\text{out}}(D_1, D_2, \varphi) = P_{\text{out},\Delta,a,\text{max}}, \text{ search variable: } \varphi, \end{aligned} \quad (5.30)$$

applies.

The calculation of $V_{2,\text{lim}}$ is discussed in the next paragraph, since $V_2 = V_{2,\text{lim}}$ causes the DAB to operate exactly at the border between *mode a* and *mode b*.

⁴Different to Section 5.1.1, the values of the limiting power levels $P_{\text{out},\Delta,a,\text{min}}$, $P_{\text{out},\Delta,a,\text{max}}$, $P_{\text{out},\Delta,b,\text{max}}$, and $P_{\text{out},\Delta,\text{max}}$ now depend on the direction of power transfer.

Mode b, triangular current mode (cf. Figure 5.5). With (5.24),

$$D_2 = D_1 - \frac{|\varphi|}{\pi} \quad (5.31)$$

results; a numerical search algorithm determines the appropriate values for D_1 and φ that satisfy (5.26) and (5.27) within

$$(V_2 < V_{2,\text{lim}} \wedge |P_{\text{out}}| \leq |P_{\text{out},\Delta,\text{a},\text{min}}|) \vee (V_2 \geq V_{2,\text{lim}} \wedge |P_{\text{out}}| \leq |P_{\text{out},\Delta,\text{b},\text{max}}|). \quad (5.32)$$

The maximum allowable power $P_{\text{out},\Delta,\text{b},\text{max}}$ is obtained from

$$\begin{aligned} \left[I_0(D_1, D_2, \varphi) = I_{0,\text{d}} \wedge D_1 = \frac{1}{2} - T_{\text{f}} f_{\text{S}} \wedge D_2 = D_1 - \frac{|\varphi|}{\pi} \right] \\ \Leftrightarrow P_{\text{out}}(D_1, D_2, \varphi) = P_{\text{out},\Delta,\text{b},\text{max}}, \text{ search variable: } \varphi. \end{aligned} \quad (5.33)$$

A slightly more complex procedure is needed to obtain $V_{2,\text{lim}}$: unlike (5.7), $V_{2,\text{lim}}$ now as well depends on the actual value of $P_{\text{out},\text{d}}$, due to resistive losses and due to the magnetizing current. First, $P_{\text{out},\Delta,\text{V}2\text{lim},\text{max}} = P_{\text{out},\Delta,\text{b},\text{max}}(V_2 = V_{2,\text{lim}})$ is calculated; there (5.29), (5.30), and (5.33) are simultaneously valid (cf. Section 5.1.1) and with (5.24) and constant V_1 , a constant phase shift angle and constant duty cycles result. The numerical solver hence needs to vary V_2 in order to determine $P_{\text{out},\Delta,\text{V}2\text{lim},\text{max}}$ and the corresponding $V_{2,\text{lim}}(P_{\text{out},\Delta,\text{V}2\text{lim},\text{max}})$ in compliance with

$$\begin{aligned} \left[I_0(D_1, D_2, \varphi, V_2) = I_{0,\text{d}} \wedge \right. \\ \left. D_1 = \frac{1}{2} - T_{\text{f}} f_{\text{S}} \wedge D_2 = \frac{1}{2} - (T_{I_0} + T_{\text{f}}) f_{\text{S}} \wedge \varphi = \pi T_{I_0} f_{\text{S}} \text{sgn}(P_{\text{out},\text{d}}) \right] \\ \Leftrightarrow \left[V_2 = V_{2,\text{lim}}(P_{\text{out},\Delta,\text{V}2\text{lim},\text{max}}) \wedge P_{\text{out}}(D_1, D_2, \varphi, V_2) = P_{\text{out},\Delta,\text{V}2\text{lim},\text{max}} \right], \\ \text{search variable: } V_2. \end{aligned} \quad (5.34)$$

For $|P_{\text{out},\text{d}}| \geq |P_{\text{out},\Delta,\text{V}2\text{lim},\text{max}}|$, (5.34) already determines the correct $V_{2,\text{lim}}$. For $|P_{\text{out},\text{d}}| < |P_{\text{out},\Delta,\text{V}2\text{lim},\text{max}}|$ and with (5.24) and (5.31),

$$\begin{aligned} \left[P_{\text{out}}(D_1, D_2, \varphi, V_2) = P_{\text{out},\text{d}} \wedge I_0(D_1, D_2, \varphi, V_2) = I_{0,\text{d}} \wedge \right. \\ \left. D_2 = D_1 - \frac{|\varphi|}{\pi} \wedge \varphi = \pi T_{I_0} f_{\text{S}} \text{sgn}(P_{\text{out},\text{d}}) \right] \\ \Leftrightarrow V_2 = V_{2,\text{lim}}(P_{\text{out},\text{d}}) \quad \forall \quad |P_{\text{out},\text{d}}| < |P_{\text{out},\Delta,\text{V}2\text{lim},\text{max}}| \\ \text{(search variables: } D_1, V_2) \end{aligned} \quad (5.35)$$

applies, which is used to compute $V_{2,\text{lim}}(P_{\text{out},\text{d}})$.

Mode c, trapezoidal current mode (cf. Figure 5.6). The trapezoidal current mode modulation scheme employs

$$D_1 + D_2 = 1 - \frac{|\varphi|}{\pi} - 2T_{\text{f}}f_{\text{S}} \quad (5.36)$$

$$\forall \left(V_2 < V_{2,\text{lim}} \wedge |P_{\text{out},\Delta,\text{a,max}}| < |P| \leq |P_{\text{out},\Delta,\text{max}}| \vee \right. \\ \left. (V_2 \geq V_{2,\text{lim}} \wedge |P_{\text{out},\Delta,\text{b,max}}| < |P| \leq |P_{\text{out},\Delta,\text{max}}|) \right), \quad (5.37)$$

whereas the maximum possible output power, $|P_{\text{out},\Delta,\text{max}}|$, is obtained using a numerical maximum search. For practical reasons, the sum $D_1 + D_2$ and the weighting factor a ,

$$D_{12} = D_1 + D_2, \quad (5.38)$$

$$a = \frac{D_1}{D_{12}}, \quad (5.39)$$

are used instead of D_1 and D_2 . With (5.36) and (5.38), the numerical solver adjusts φ and a in order to meet (5.26) and (5.27).

5.1.3 Measurement Results

In Figure 5.13, the waveforms of $v_{\text{AC1}}(t)$, $v_{\text{AC2}}(t)$, and $i_{\text{L1}}(t)$, calculated with the numerical solver outlined in Section 4.6.1, are compared to the measured waveforms at $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, and $P_2 = 2 \text{ kW}$ (extended triangular current mode modulation). The very good matching of calculated and measured waveforms [in particular regarding the current $i_{\text{L1}}(t)$] is essential with respect to an accurate prediction of the expected converter efficiency.

The converter efficiencies achieved for the DAB converter designed in Appendix A.2 (i.e. $n = 16$ and $L = 15.5 \mu\text{H}$) and with the extended triangular and trapezoidal current mode modulation schemes are depicted in Figure 5.14 (measured at $T_{\text{j}} \approx 25^\circ\text{C}$, cf. Chapter 4): compared to phase shift modulation (Figure 4.30), increased converter efficiencies are achieved for most operating points, in particular at power levels considerably below the rated power of 2 kW.

5.2 Minimum Loss Modulation

The extended triangular and trapezoidal current mode modulation schemes, developed in Section 5.1, facilitate a considerably more efficient converter operation than phase shift modulation (for most operating points, in particular at low power levels). The extended triangular and trapezoidal current mode modulation schemes, however, are developed based on the findings discussed in Section 4 rather than on an extensive efficiency optimization; in retrospect

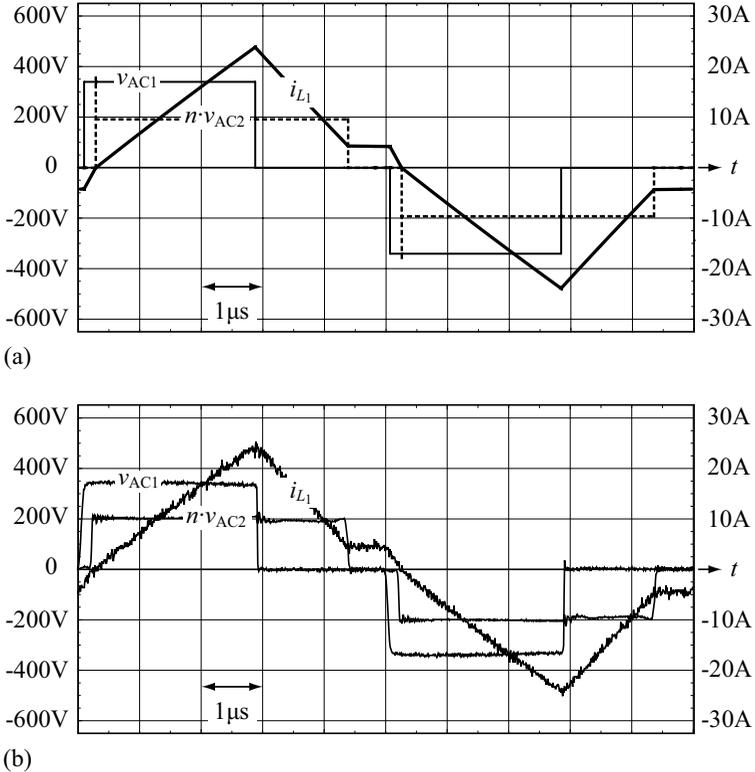


Figure 5.13: (a) Calculated (cf. Section 4.6.1) and (b) measured voltage and current waveforms obtained with the extended triangular and trapezoidal current mode modulation schemes for $V_1 = 340$ V, $V_2 = 12$ V, and $P_2 = 2$ kW; for all measurements, the efficiency optimized DAB design with $n = 16$ and $L = 15.5$ μ H is employed (cf. Appendix A.2).

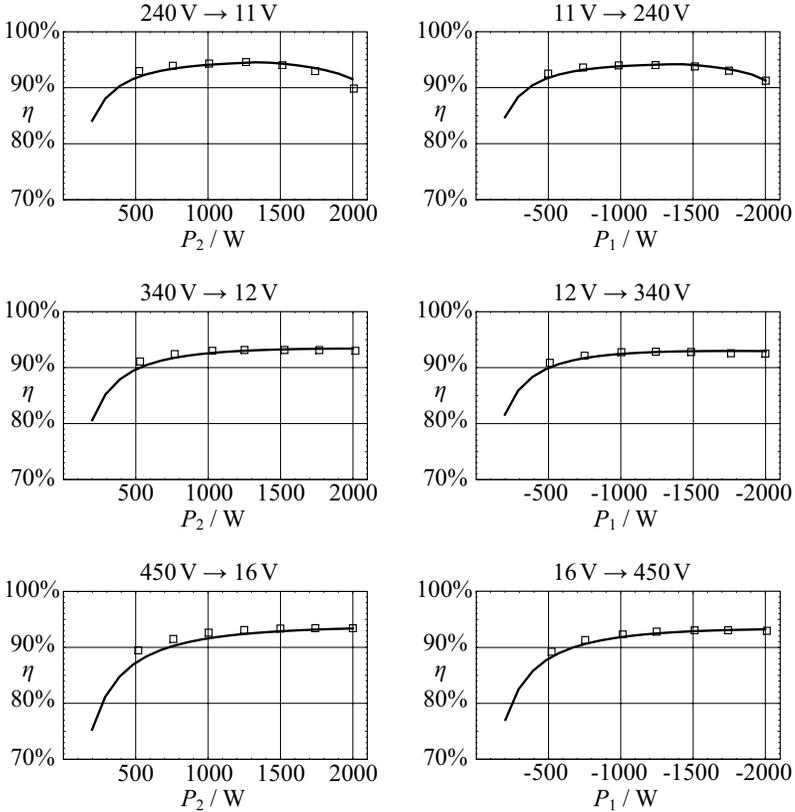


Figure 5.14: Predicted efficiencies (solid lines) and measured efficiencies (\square) obtained with the extended triangular and trapezoidal current mode modulation schemes ($T_f = 50 \text{ ns}$) and for different operating conditions; the efficiencies are calculated with the full DAB loss model discussed in Section 4; for all measurements, the efficiency optimized DAB design with $n = 16$ and $L = 15.5 \mu\text{H}$ is employed (cf. Appendix A.2); the efficiency is measured according to Chapter 4, i.e. $T_j \approx 25^\circ\text{C}$.

on the findings presented in Chapter 3 it is conceivable that more effective DAB modulation schemes exist.

For a particular operating point (i.e. given V_1 , V_2 , and P_{out}), the optimal DAB converter parameters φ , D_1 , and D_2 (with respect to maximum efficiency) are calculated according to the optimization procedure discussed in Section 3.1.3 using the numerical solver discussed in Section 4.6.1. The result of this optimization procedure reveals, that the optimal operation of the DAB within the specified operation ranges (V_1 , V_2 , and P_{out}) requires fundamental mode transitions, which cause steps in the control parameters (φ , D_1 , and D_2) and consequently increases the controller complexity.⁵ However, with a minor decrease of the DAB efficiency being tolerated, especially at low output power, suboptimal modulation schemes with continuous control parameter functions are feasible, and still, converter operation close to maximum efficiency is achieved.

5.2.1 Numerical Efficiency Optimization

In order to determine a modulation strategy with respect to maximum converter efficiency, 100 particular operating points (Table 5.1) are optimized using the numerical solver and the loss model discussed in Section 4. The presented discussion summarizes the obtained results based on 12 representative operating points:

- $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, $P_{\text{out}} = \pm 200 \text{ W}$ (Figure 5.17),
- $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, $P_{\text{out}} = \pm 1 \text{ kW}$ (Figure 5.15),
- $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, $P_{\text{out}} = \pm 2 \text{ kW}$ (Figure 5.16),
- $V_1 = 240 \text{ V}$, $V_2 = 11 \text{ V}$, $P_{\text{out}} = \pm 2 \text{ kW}$ (Figure 5.19),
- $V_1 = 240 \text{ V}$, $V_2 = 16 \text{ V}$, $P_{\text{out}} = 200 \text{ W}$ [Figure 5.20 (a)],
- $V_1 = 240 \text{ V}$, $V_2 = 16 \text{ V}$, $P_{\text{out}} = 1 \text{ kW}$ [Figure 5.20 (b)],
- $V_1 = 240 \text{ V}$, $V_2 = 16 \text{ V}$, $P_{\text{out}} = \pm 2 \text{ kW}$ (Figure 5.21).

⁵Due to the discontinuities in the control parameter functions, the inductor currents, the switching currents, the transformer magnetization, and the DAB efficiency change discontinuously, as well. The mentioned mode transitions thus need to be carefully considered in order to achieve a stable DAB operation.

Optimal DAB operation at $V_1 = 340\text{ V}$ and $V_2 = 12\text{ V}$

If the DAB is operated with maximum efficiency at $V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$, and $P_{\text{out}} = \pm 1\text{ kW}$, a DAB inductor current waveform $i_{L_1}(t)$ similar to the inductor current achieved with the extended triangular current mode modulation scheme results (Figure 5.15); merely, the LV side switch current at $t = t_1$ in Figure 5.15 (a) is equal to

$$I_{S2,\text{sw,opt}} \approx 20\text{ A} \quad (5.40)$$

giving minimum switching losses (Figure 4.22).

The DAB exceeds the power limit of the triangular current mode modulation at rated output power, $P_{\text{out}} = \pm 2\text{ kW}$ (Figure 5.16), however, the obtained optimal modulation strategy is different to the trapezoidal current mode modulation, but rather similar to the optimal transition mode modulation presented in Section 3.1.3. For $P_{\text{out}} = \pm 2\text{ kW}$, the optimization algorithm employs $D_2 = 0.5$ and adjusts D_1 and φ in order to simultaneously obtain the required output power, low conduction losses on the LV side, and low switching losses on the LV side (i.e. minimum LV side inductor RMS currents are achieved, taking $I_{S2,\text{sw,opt}} \approx 20\text{ A}$ into account).

At low output power levels, the most efficient modulation method (Figure 5.17) is similar to the method illustrated in Figure 5.2, due to low switching and conduction losses: compared to the extended triangular current mode modulation, only a small inductor current circulates during the

	V_1	V_2	P_{out}
1	340 V	12 V	$\pm 200\text{ W}$, $\pm 500\text{ W}$, $\pm 1\text{ kW}$, $\pm 1.5\text{ kW}$, $\pm 2\text{ kW}$
2	240 V	11 V	$\pm 200\text{ W}$, $\pm 500\text{ W}$, $\pm 1\text{ kW}$, $\pm 1.5\text{ kW}$, $\pm 2\text{ kW}$
3	240 V	13.5 V	$\pm 200\text{ W}$, $\pm 500\text{ W}$, $\pm 1\text{ kW}$, $\pm 1.5\text{ kW}$, $\pm 2\text{ kW}$
4	240 V	16 V	$\pm 200\text{ W}$, $\pm 500\text{ W}$, $\pm 1\text{ kW}$, $\pm 1.5\text{ kW}$, $\pm 2\text{ kW}$
5	345 V	11 V	$\pm 200\text{ W}$, $\pm 500\text{ W}$, $\pm 1\text{ kW}$, $\pm 1.5\text{ kW}$, $\pm 2\text{ kW}$
6	345 V	13.5 V	$\pm 200\text{ W}$, $\pm 500\text{ W}$, $\pm 1\text{ kW}$, $\pm 1.5\text{ kW}$, $\pm 2\text{ kW}$
7	345 V	16 V	$\pm 200\text{ W}$, $\pm 500\text{ W}$, $\pm 1\text{ kW}$, $\pm 1.5\text{ kW}$, $\pm 2\text{ kW}$
8	450 V	11 V	$\pm 200\text{ W}$, $\pm 500\text{ W}$, $\pm 1\text{ kW}$, $\pm 1.5\text{ kW}$, $\pm 2\text{ kW}$
9	450 V	13.5 V	$\pm 200\text{ W}$, $\pm 500\text{ W}$, $\pm 1\text{ kW}$, $\pm 1.5\text{ kW}$, $\pm 2\text{ kW}$
10	450 V	16 V	$\pm 200\text{ W}$, $\pm 500\text{ W}$, $\pm 1\text{ kW}$, $\pm 1.5\text{ kW}$, $\pm 2\text{ kW}$

Table 5.1: For these 100 operating points, the optimal control parameters D_1 , D_2 , and φ are calculated with respect to maximum efficiency; the results are given in Table 5.2.

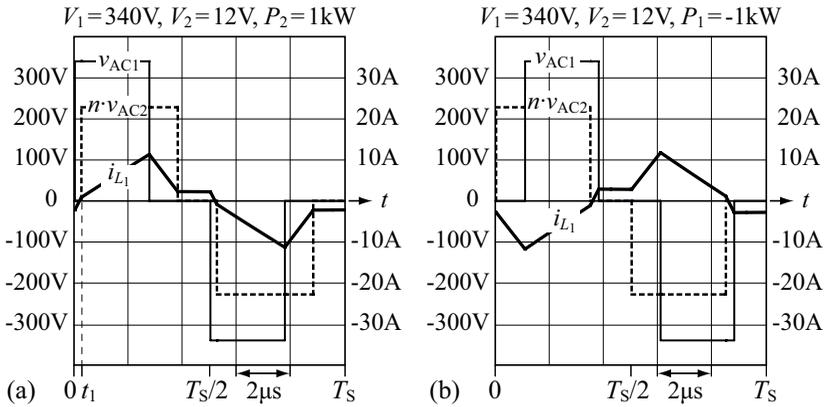


Figure 5.15: Calculated waveforms $v_{AC1}(t)$, $v_{AC2}(t)$, and $i_{L1}(t)$ for maximum efficiency at (a) $P_{\text{out}} = P_2 = 1\text{kW}$, and (b) $P_{\text{out}} = P_1 = -1\text{kW}$; $V_1 = 340\text{V}$, $V_2 = 12\text{V}$, $n = 19$, $L = 26.7\mu\text{H}$, and $f_s = 100\text{kHz}$; due to the large magnetizing inductance ($L_M = 2.7\text{mH}$), $i_{L1} \approx i_{L2}/n$ applies.

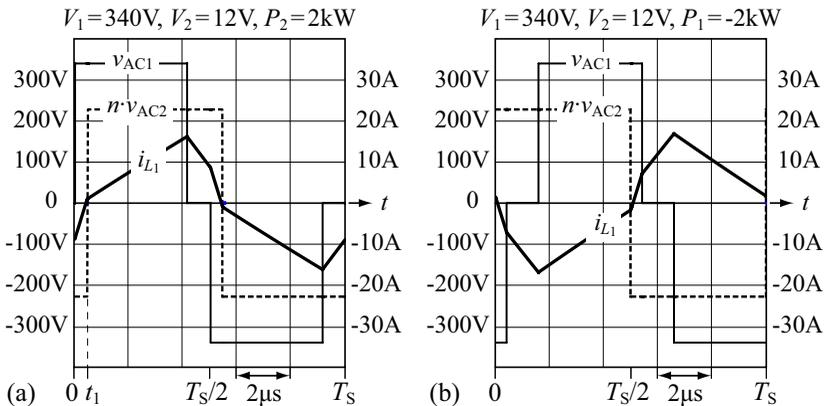


Figure 5.16: Calculated waveforms $v_{AC1}(t)$, $v_{AC2}(t)$, and $i_{L1}(t)$ for maximum efficiency at (a) $P_{\text{out}} = 2\text{kW}$, and (b) $P_{\text{out}} = -2\text{kW}$; $V_1 = 340\text{V}$, $V_2 = 12\text{V}$, $n = 19$, $L = 26.7\mu\text{H}$, $L_M = 2.7\text{mH}$, and $f_s = 100\text{kHz}$.

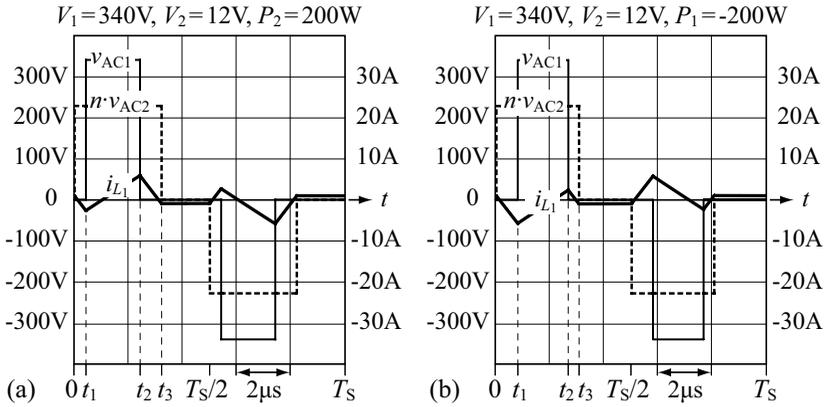


Figure 5.17: Calculated waveforms $v_{AC1}(t)$, $v_{AC2}(t)$, and $i_{L1}(t)$ for maximum efficiency at (a) $P_{\text{out}} = 200\text{ W}$, and (b) $P_{\text{out}} = -200\text{ W}$; $V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$, $n = 19$, $L = 26.7\ \mu\text{H}$, $L_M = 2.7\ \text{mH}$, and $f_S = 100\ \text{kHz}$.

freewheeling time interval $[t_3 < t < T_S/2]$ in Figures 5.17 (a) and (b)] and the LV side full bridge switches with $I_{S2,sw,opt}$. With this modulation scheme, however, discontinuous control parameters D_1 , D_2 , and φ result [Figure 5.18 (a) for P_{out} between 800 W and 900 W], which presents difficulties to the practical implementation (e.g. a particular sequence of different modulation schemes needs to be implemented in order to avoid the depicted discontinuities, cf. Figure 5.3). Therefore, at low power levels, the extended triangular current modulation scheme depicted in Figure 5.15 is preferred.

Optimal DAB operation at $V_1 = 240\text{ V}$, $V_2 = 11\text{ V}$, and $P_{\text{out}} = \pm 2\text{ kW}$

At $V_1 = 240\text{ V}$, $V_2 = 11\text{ V}$, and $P_{\text{out}} = \pm 2\text{ kW}$, the DAB operates close to its maximum possible power [cf. Table 1.4 and (3.15)]. There, according to the optimization procedure discussed in Section 3.1.3, phase shift modulation is employed to achieve minimum inductor RMS currents. The actual efficiency optimization based on the DAB loss model (Section 4), however, identifies $D_1 = 0.5$ and $D_2 < 0.5$ to yield most efficient converter operation at very high power levels (Figure 5.19), due to a reduction of the LV side switching losses.

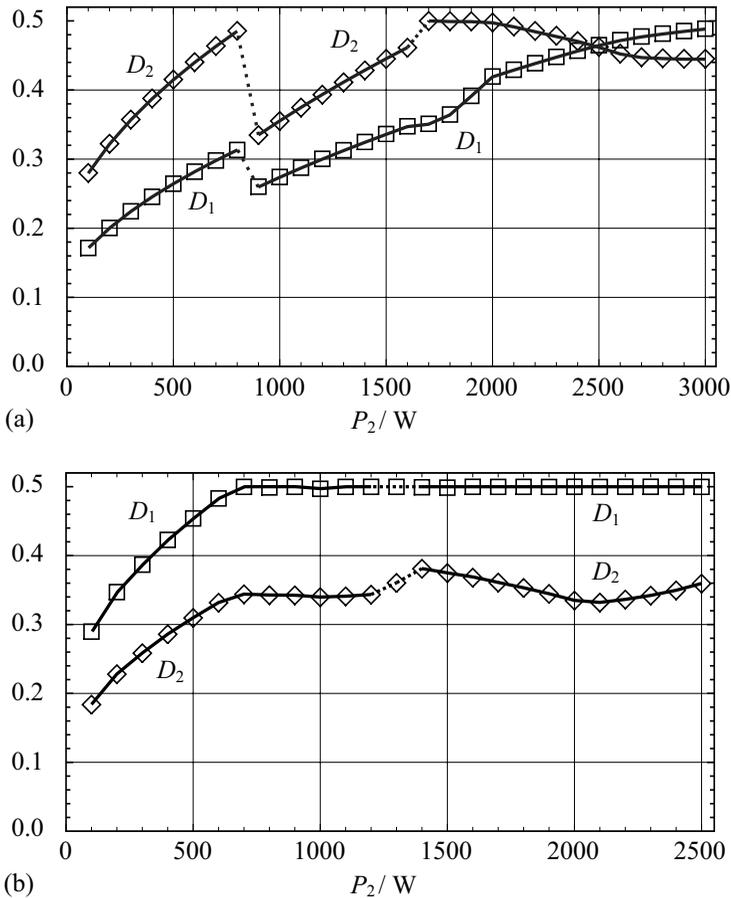


Figure 5.18: (a) Duty cycles D_1 and D_2 required in order to achieve maximum converter efficiency for $V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$, and power being transferred from the HV port to the LV port: for P_{out} between 800 W and 900 W, a large step occurs [a second step of D_2 occurs between 1.6 kW and 1.7 kW, which is, however, covered using linear interpolation, cf. (5.50)]; (b) D_1 and D_2 for maximum converter efficiency, $V_1 = 240\text{ V}$, $V_2 = 16\text{ V}$, power being transferred to the LV port: for P_{out} between 1.2 kW and 1.4 kW, $D_2(P_{\text{out}})$ changes considerably. Employed DAB: $n = 19$, $L = 26.7\text{ }\mu\text{H}$.

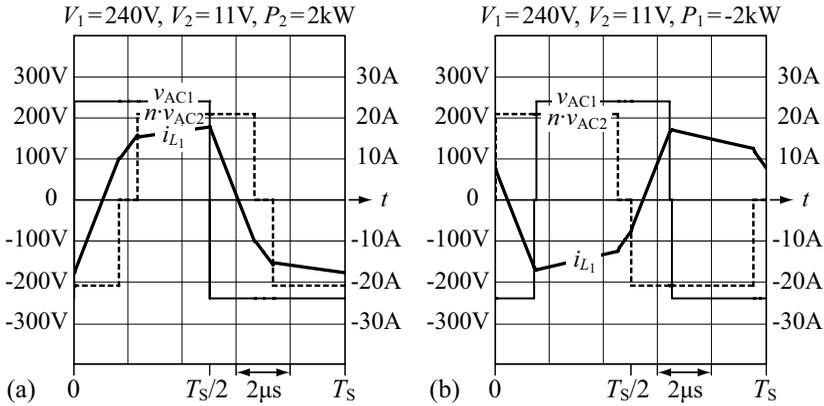


Figure 5.19: Calculated waveforms $v_{AC1}(t)$, $v_{AC2}(t)$, and $i_{L1}(t)$ for maximum efficiency at (a) $P_{out} = 2\text{ kW}$, and (b) $P_{out} = -2\text{ kW}$; $V_1 = 240\text{ V}$, $V_2 = 11\text{ V}$, $n = 19$, $L = 26.7\text{ }\mu\text{H}$, $L_M = 2.7\text{ mH}$, and $f_s = 100\text{ kHz}$.

Optimal DAB operation at $V_1 = 240\text{ V}$ and $V_2 = 16\text{ V}$

At $V_1 = 240\text{ V}$, $V_2 = 16\text{ V}$, and $P_{out} = 200\text{ W}$ or $P_{out} = 1\text{ kW}$ (Figure 5.20), the optimization algorithm suggests the DAB operation mode 1b [Figure 3.15 (i)] to be used, since minimum switching losses are achieved, there. However, similar to the DAB operation at $V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$, and $P_{out} = 200\text{ W}$, difficulties arise with respect to the practical realization and the complexity required to calculate the modulation parameters increases [e.g. for P_{out} between 1.2 kW and 1.4 kW in Figure 5.18 (b)]. Since the efficiency achieved with the extended triangular current mode modulation (mode b, Section 5.1.1, Figure 5.5) is close to the maximum achievable efficiency [cf. Figure 5.28 (b) for $P_{out} < 1.2\text{ kW}$], the less complex extended triangular current mode modulation is preferred over the modulation method suggested by the numerical optimization algorithm.

The DAB exceeds the maximum possible output power of the extended triangular current mode modulation (mode b) at $V_1 = 240\text{ V}$, $V_2 = 16\text{ V}$, and $P_{out} = \pm 2\text{ kW}$. There, $D_1 = 0.5$ and $D_2 < 0.5$ result for maximum efficiency (low conduction losses and low switching losses are achieved, cf. optimal DAB operation at $V_1 = 240\text{ V}$, $V_2 = 11\text{ V}$, and $P_{out} = \pm 2\text{ kW}$).

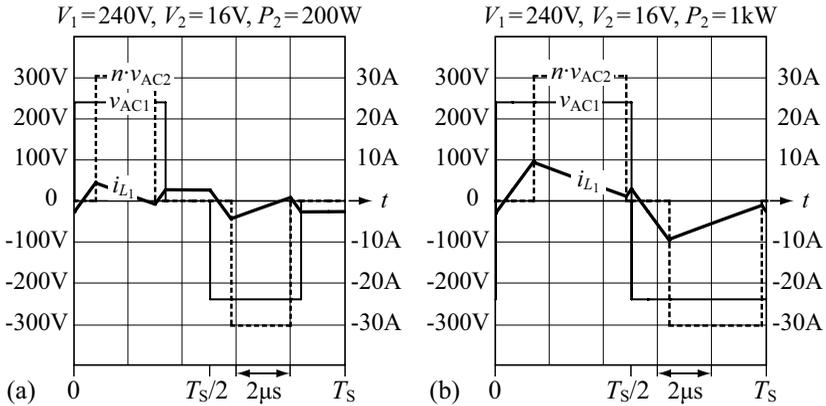


Figure 5.20: Calculated waveforms $v_{AC1}(t)$, $v_{AC2}(t)$, and $i_{L1}(t)$ for maximum efficiency at (a) $P_{\text{out}} = 200\text{ W}$, and (b) $P_{\text{out}} = 1\text{ kW}$; $V_1 = 240\text{ V}$, $V_2 = 16\text{ V}$, $n = 19$, $L = 26.7\text{ }\mu\text{H}$, $L_M = 2.7\text{ mH}$, and $f_S = 100\text{ kHz}$.

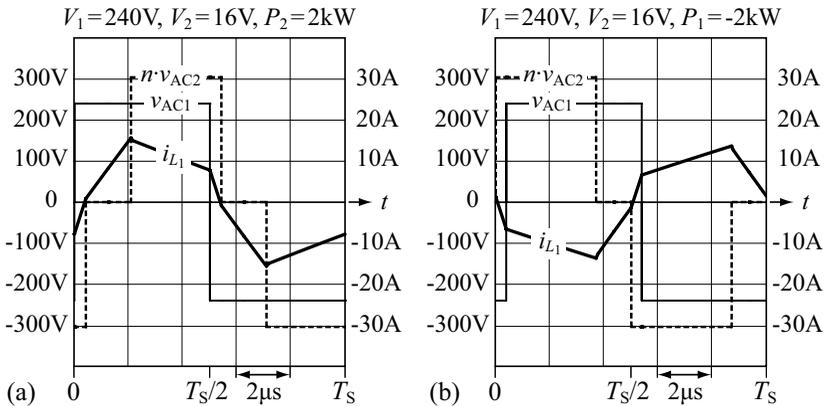


Figure 5.21: Calculated waveforms $v_{AC1}(t)$, $v_{AC2}(t)$, and $i_{L1}(t)$ for maximum efficiency at (a) $P_{\text{out}} = 2\text{ kW}$, and (b) $P_{\text{out}} = -2\text{ kW}$; $V_1 = 240\text{ V}$, $V_2 = 16\text{ V}$, $n = 19$, $L = 26.7\text{ }\mu\text{H}$, $L_M = 2.7\text{ mH}$, and $f_S = 100\text{ kHz}$.

5.2.2 Suboptimal Modulation Schemes

The discussions presented in Section 5.2.1 enable the development of suboptimal modulation schemes, which facilitate the DAB to be operated close to its maximum efficiency.

The proposed modulation schemes try to minimize the impact of the most important DAB loss mechanisms:

- conduction losses,
- HV side switching losses (ZVS is required), and
- LV side switching losses [during switching, large currents should be avoided; switching processes with $I_{S2,sw} = I_{S2,sw,opt}$, cf. (5.40), generate minimum switching losses].

Suboptimal DAB Operation at Low Power Levels

According to Section 5.2.1, the extended triangular current mode modulation scheme is employed at low output power levels. The results of the optimization procedure discussed in Section 5.2.1 suggest to select the value of the circulating current, I_0 , as small as possible to achieve low conduction losses and ZVS on the HV side; I_0 is therefore selected according to (5.23). The results of the optimization further suggest to employ LV side ZVS with $I_{S2,sw,opt}$, since lowest losses occur, there. Thus, a modified value is used for T_{I_0} [cf. (5.24)],

$$T_{I_0} = \frac{L(|I_0| + \frac{20\text{A}}{n})}{V_1} \quad (5.41)$$

(on the assumption of negligible magnetizing currents and negligible losses during $0 < t < T_{I_0}$).

The applicable power range of the extended triangular current mode modulation is given with (5.28) and (5.32):

$$(|P_{out}| \leq |P_{out,\Delta,a,max}| \wedge V_2 < V_{2,lim}) \vee (|P_{out}| \leq |P_{out,\Delta,b,max}| \wedge V_2 \geq V_{2,lim}). \quad (5.42)$$

Suboptimal DAB Operation at High Power Levels

For power levels exceeding the limits given with (5.42), the modulation modes 3b or 7b (depending on the direction of power transfer) are employed [cf. Figures 3.15 (k) and (l)].⁶ Thus, the minimum freewheeling time T_f ,

⁶The presented explanation confines to a power transfer direction from the HV port to the LV port.

needed to obtain $P_{\text{out},\Delta,a,\text{max}}$ and $P_{\text{out},\Delta,b,\text{max}}$, is set to zero in order to facilitate a seamless transition between the extended triangular current mode modulation schemes and the suboptimal high power modulation schemes based on modulation modes 3b or 7b. The proposed high power modulation schemes furthermore require the calculations of D_1 , D_2 , and φ to be considered separately for $V_2 \geq V_{2,\text{lim}}$ and $V_2 < V_{2,\text{lim}}$.

$V_2 \geq V_{2,\text{lim}}$ (**Figure 5.22**). At $P_{\text{out}} = P_{\text{out},\Delta,b,\text{max}}$ and with $T_f = 0$, the duty cycles $D_1 = 0.5$ and $D_2 < 0.5$ result [Figure 5.22 (a)]; furthermore, hard switching occurs on the LV side at $t = t_1 = 0$ with $i_{L_2,\text{sw},\Delta,b,\text{max}} = i_{L_2}(0) < 0$. With increasing output power D_2 and φ increase, and the current $i_{L_2}(t_1)$ becomes equal to $I_{S_2,\text{sw,opt}}$ at $P_{\text{out}} = P_{\text{out,opt,b,min}}$ [Figure 5.22 (b)]:

$$\begin{aligned} [i_{L_1}(D_1, D_2, \varphi, t = 0) = I_{0,d} \wedge i_{L_2}(D_1, D_2, \varphi, t = t_1) = I_{S_2,\text{sw,opt}} \wedge D_1 = 0.5] \\ \Leftrightarrow P_{\text{out}}(D_1, D_2, \varphi) = P_{\text{out,opt,b,min}}, \text{ search variables: } D_2, \varphi. \end{aligned} \quad (5.43)$$

For $|P_{\text{out},\Delta,b,\text{max}}| < |P_{\text{out}}| \leq |P_{\text{out,opt,b,min}}|$, a numerical search algorithm seeks for suitable values of D_2 and φ (D_1 remains equal to 0.5) in order to satisfy

$$\begin{aligned} P_{\text{out}}(D_1 = 0.5, D_2, \varphi) &= P_{\text{out,d}}, \\ i_{L_2}(D_1 = 0.5, D_2, \varphi, t = t_1) &= I_{S_2,\text{sw,d}} \\ \forall V_2 \geq V_{2,\text{lim}} \wedge |P_{\text{out},\Delta,b,\text{max}}| < |P_{\text{out}}| &\leq |P_{\text{out,opt,b,min}}| \end{aligned} \quad (5.44)$$

employing a linear transition for the LV side current $i_{L_2}(t_1)$,

$$\begin{aligned} I_{S_2,\text{sw,d}} &= I_{S_2,\text{sw},\Delta,b,\text{max}} + (I_{S_2,\text{sw,opt}} - I_{S_2,\text{sw},\Delta,b,\text{max}}) \cdot \\ &\quad \frac{P_{\text{out,d}} - P_{\text{out},\Delta,b,\text{max}}}{P_{\text{out,opt,b,min}} - P_{\text{out},\Delta,b,\text{max}}}. \end{aligned} \quad (5.45)$$

The maximum achievable output power, $P_{\text{out,max}}$, is approximately determined using phase shift modulation and a numerical maximum search:

$$(D_1 = 0.5 \wedge D_2 = 0.5) \Leftrightarrow P_{\text{out,max}} \approx \max[P_{\text{out}}(D_1, D_2, \varphi)], \text{ search var.: } \varphi. \quad (5.46)$$

For output power levels between $P_{\text{out,opt,b,min}}$ and $P_{\text{out,max}}$, $D_1 = 0.5$ remains and D_2 and φ are adjusted in order to obtain the required output power and maximum efficiency, provided that the LV side switching current $i_{S_2}(t_1) = i_{L_2}(t_1)$ remains greater or equal than $I_{S_2,\text{sw,opt}}$ [Figure 5.22 (c)], i.e. a numerical search algorithm seeks for D_2 and φ in order to satisfy:

$$\begin{aligned} P_{\text{out}}(D_1, D_2, \varphi) &= P_{\text{out,d}}, \\ \eta(D_1, D_2, \varphi) &= \max[\eta(D_1, D_2, \varphi)], \\ i_{L_2}(D_1, D_2, \varphi, t = t_1) &> I_{S_2,\text{sw,opt}} \\ \forall V_2 \geq V_{2,\text{lim}} \wedge |P_{\text{out,opt,b,min}}| < |P_{\text{out}}| &\leq |P_{\text{out,max}}|. \end{aligned} \quad (5.47)$$

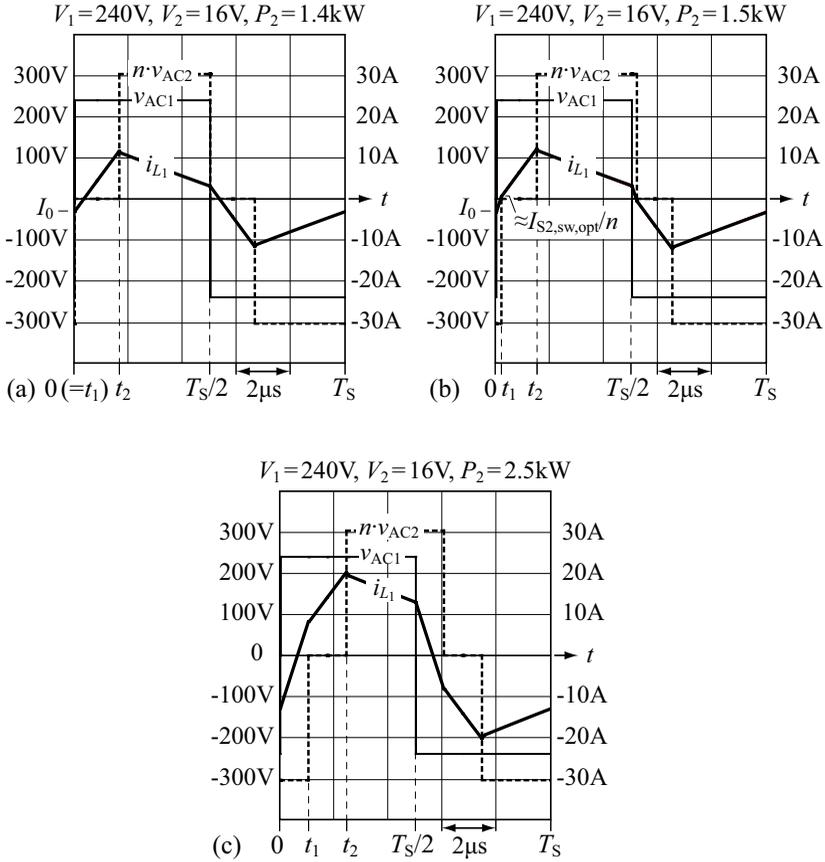


Figure 5.22: Calculated waveforms $v_{AC1}(t)$, $v_{AC2}(t)$, and $i_{L1}(t)$ for $V_1 = 240\text{ V}$ and $V_2 = 16\text{ V}$, using the suboptimal modulation schemes: (a) $P_{\text{out}} = 1.4\text{ kW}$, (b) $P_{\text{out}} = 1.5\text{ kW}$, and (c) $P_{\text{out}} = 2.5\text{ kW}$; $n = 19$, $L = 26.7\text{ }\mu\text{H}$, $L_M = 2.7\text{ mH}$ (thus, $i_{L1} \approx i_{L2}/n$ applies), and $f_s = 100\text{ kHz}$; Figures (a) and (b) depict the limits of the respective operating modes: (a) $P_{\text{out}} = P_{\text{out},\Delta,b,\text{max}}$; (b) $P_{\text{out}} = P_{\text{out,opt,b,min}}$.

$V_2 < V_{2,\text{lim}}$ (**Figure 5.23**). At $P_{\text{out}} = P_{\text{out},\Delta,\text{a,max}}$, $D_1 < 0.5$ and $D_2 < 0.5$ result (due to the time interval $0 < t < T_{I_0}$, required to generate the freewheeling current I_0). Moreover, hard switching occurs on the LV side, e.g. at $t = 0$, with $I_{\text{S2,sw},\Delta,\text{a,max}} = i_{L_2}(0) < 0$ [Figure 5.23 (a)]. If $|P_{\text{out}}|$ exceeds $|P_{\text{out},\Delta,\text{a,max}}|$, the conditions $D_2 = 0.5$, $i_{L_1}(0) \geq I_{0,\text{d}}$, and $i_{L_2}(t_1) = I_{\text{S2,sw,opt}}$ need to be satisfied in order to achieve low conduction losses and low switching losses; the respective minimum power level $P_{\text{out,opt,a,min}}$ is thus determined using

$$\begin{aligned} [i_{L_1}(D_1, D_2, \varphi, t = 0) = I_{0,\text{d}} \wedge i_{L_2}(D_1, D_2, \varphi, t = t_1) = I_{\text{S2,sw,opt}} \wedge D_2 = 0.5] \\ \Leftrightarrow P_{\text{out}}(D_1, D_2, \varphi) = P_{\text{out,opt,a,min}}, \text{ search variables: } D_1, \varphi. \end{aligned} \quad (5.48)$$

The resulting voltage and current waveforms for $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, and $P_{\text{out}} = P_{\text{out,opt,a,min}}$ are depicted in Figure 5.23 (b). For output power levels between $P_{\text{out},\Delta,\text{a,max}}$ and $P_{\text{out,opt,a,min}}$, the modulation parameters D_1 , D_2 , and φ are calculated using

$$\begin{aligned} P_{\text{out}}(D_1, D_2, \varphi) &= P_{\text{out,d}}, \\ i_{L_1}(D_1, D_2, \varphi, t = 0) &= I_0, \\ i_{L_2}(D_1, D_2, \varphi, t = t_1) &= I_{\text{S2,sw,d}} \\ \forall V_2 < V_{2,\text{lim}} \wedge |P_{\text{out},\Delta,\text{a,max}}| < |P_{\text{out}}| &\leq |P_{\text{out,opt,a,min}}|. \end{aligned} \quad (5.49)$$

For the LV side current $i_{L_2}(t_1)$, a linear transition is employed:

$$\begin{aligned} I_{\text{S2,sw,d}} &= I_{\text{S2,sw},\Delta,\text{a,max}} + (I_{\text{S2,sw,opt}} - I_{\text{S2,sw},\Delta,\text{a,max}}) \cdot \\ &\quad \frac{P_{\text{out,d}} - P_{\text{out},\Delta,\text{a,max}}}{P_{\text{out,opt,a,min}} - P_{\text{out},\Delta,\text{a,max}}}. \end{aligned} \quad (5.50)$$

With increasing output power, $D_2 = 0.5$ is kept constant and D_1 and φ are calculated in order to satisfy

$$\begin{aligned} P_{\text{out}}(D_1, D_2, \varphi) &= P_{\text{out,d}}, \\ i_{L_2}(D_1, D_2, \varphi, t = t_1) &= I_{\text{S2,sw,opt}} \\ \forall V_2 < V_{2,\text{lim}} \wedge |P_{\text{out,opt,a,min}}| < |P_{\text{out}}| &\leq |P_{\text{out,opt,a,hi}}|. \end{aligned} \quad (5.51)$$

At $|P_{\text{out}}| = |P_{\text{out,opt,a,hi}}|$, D_1 is equal to 0.5 [Figure 5.23 (c)]:

$$\begin{aligned} [i_{L_2}(D_1, D_2, \varphi, t = t_1) = I_{\text{S2,sw,opt}} \wedge D_1 = 0.5 \wedge D_2 = 0.5] \\ \Leftrightarrow P_{\text{out}}(D_1, D_2, \varphi) = P_{\text{out,opt,a,hi}}, \text{ search variable: } \varphi. \end{aligned} \quad (5.52)$$

If the required output power level exceeds $P_{\text{out,opt,a,hi}}$, $D_2 < 0.5$ is employed in order to reduce the LV side switching losses [Figure 5.23 (d)]. With

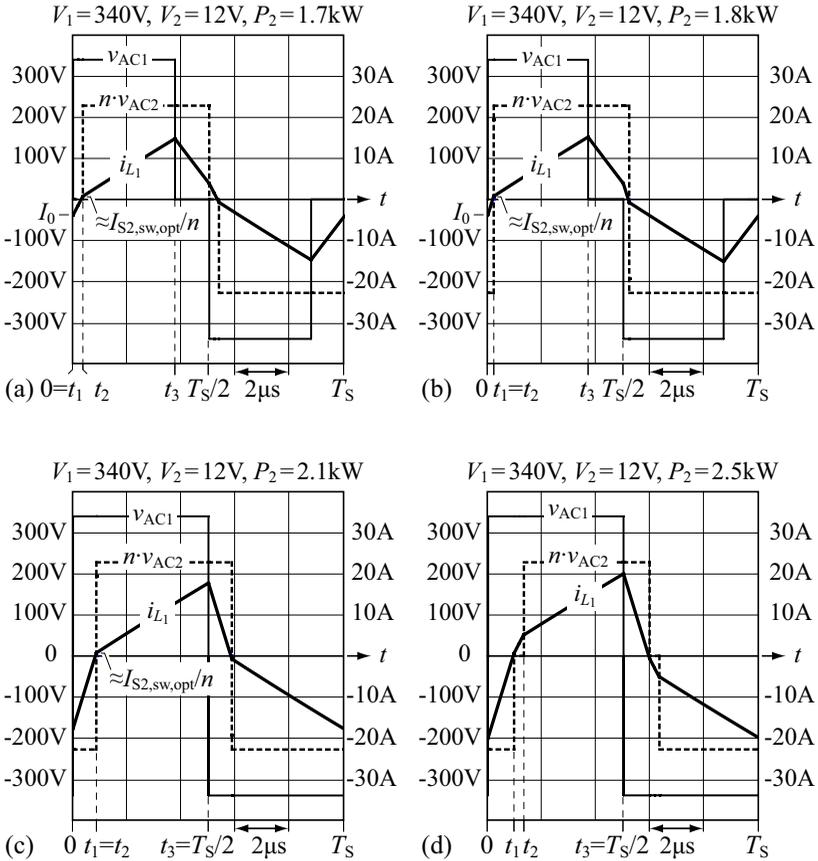


Figure 5.23: Calculated waveforms $v_{AC1}(t)$, $v_{AC2}(t)$, and $i_{L1}(t)$ for DAB operation at $V_1 = 340\text{ V}$ and $V_2 = 12\text{ V}$, using the suboptimal modulation scheme: (a) $P_{out} = 1.7\text{ kW}$, (b) $P_{out} = 1.8\text{ kW}$, (c) $P_{out} = 2.1\text{ kW}$, and (d) $P_{out} = 2.5\text{ kW}$; $n = 19$, $L = 26.7\text{ }\mu\text{H}$, $L_M = 2.7\text{ mH}$ (thus, $i_{L1} \approx i_{L2}/n$ applies), and $f_s = 100\text{ kHz}$; Figures (a), (b), and (c) depict the limits of the respective operating modes: (a) $P_{out} = P_{out,\Delta,a,max}$; (b) $P_{out} = P_{out,opt,a,min}$; (c) $P_{out} = P_{out,opt,a,hi}$.

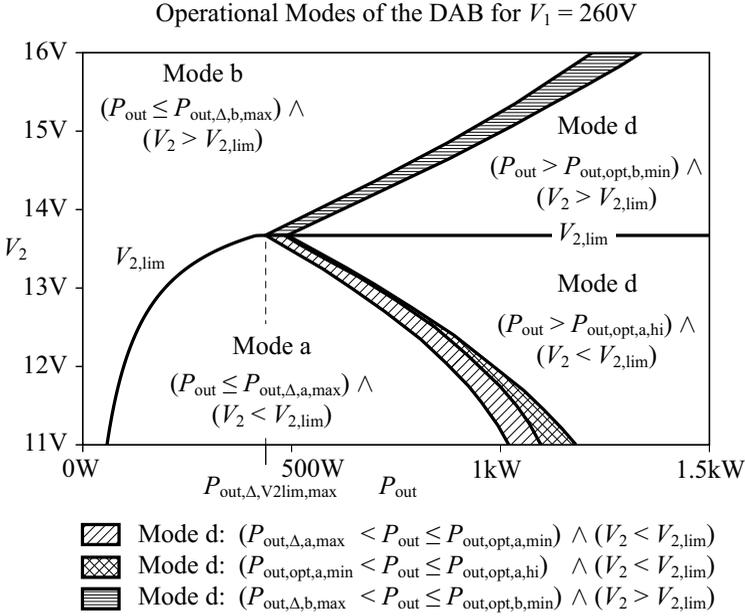


Figure 5.24: DAB operating modes for $V_1 = 260\text{V}$, different voltages V_2 , different output power levels P_{out} , $n = 19$, and $L = 26.7\ \mu\text{H}$; *mode d* denotes the voltage sequences 3b or 7b [depending on the direction of power transfer; Figures 3.15 (k) and (l)]; *mode c* would denote the trapezoidal current mode modulation and is not used for the suboptimal current mode modulation.

decreasing D_2 , however, the inductor RMS currents I_{L_1} and I_{L_2} increase. Thus, D_2 and φ are determined with respect to maximum total efficiency:

$$\begin{aligned}
 P_{\text{out}}(D_1 = 0.5, D_2, \varphi) &= P_{\text{out,d}}, \\
 \eta(D_1 = 0.5, D_2, \varphi) &= \max[\eta(D_1 = 0.5, D_2, \varphi)], \\
 i_{L_2}(D_1 = 0.5, D_2, \varphi, t = t_1) &> I_{S2,\text{sw,opt}} \\
 \forall V_2 < V_{2,\text{lim}} \wedge |P_{\text{out,opt,a,hi}}| < |P_{\text{out}}| \leq |P_{\text{out,max}}|. & \quad (5.53)
 \end{aligned}$$

Summary on the Suboptimal Modulation Schemes

Figure 5.24 presents an overview over the different operating modes employed for the suboptimal modulation schemes detailed in this Section ($V_1 = 260\text{V}$, $11\text{V} \leq V_2 \leq 16\text{V}$, $0 \leq P_{\text{out}} \leq 1.5\text{kW}$).

At low power levels (i.e. $|P_{\text{out}}| < P_{\text{out},\Delta,a,\text{max}}$ or $|P_{\text{out}}| < P_{\text{out},\Delta,b,\text{max}}$) the extended triangular current mode modulation schemes are employed (either *mode a* for $V_2 < V_{2,\text{lim}}$ or *mode b* for $V_2 > V_{2,\text{lim}}$). At high power levels, the voltage sequences 3b or 7b [depending on the direction of power transfer; cf. Figures 3.15 (k) and (l)], denoted with *mode d* in Figure 5.24, are used. The maximum power achieved with the extended triangular current mode modulation schemes, however, is slightly smaller than the minimum power achieved with the high power modulation schemes (i.e. $|P_{\text{out,opt,a,min}}|$ or $|P_{\text{out,opt,b,min}}|$, depending on $V_2/V_{2,\text{lim}}$) and therefore, the missing power levels are covered using *mode d* converter operation and linearly interpolated modulation parameters. Furthermore, for $V_2 < V_{2,\text{lim}}$, the cases $|P_{\text{out,opt,a,min}}| < |P_{\text{out}}| \leq |P_{\text{out,opt,a,hi}}|$ and $|P_{\text{out}}| > |P_{\text{out,opt,a,hi}}|$ are treated separately in order to achieve a reduction of the switching losses on the LV side.

5.2.3 Results

In order to compare the improvement achieved with the extended triangular and trapezoidal current mode modulation schemes and the suboptimal modulation schemes, the average efficiencies, calculated over the operating points listed in Table 5.1, are depicted in Figure 5.25 (the calculated efficiency values are given in Table 5.2). Furthermore, the losses calculated at the edges of the specified voltage operating range are depicted in Figure 5.26 for different output power levels and power being transferred to the LV port.

With respect to the specified voltage and power ranges (Table 1.4), phase shift modulation obviously results in the lowest average efficiency. A significant improvement is achieved with the extended triangular and trapezoidal current mode modulation being employed; there, the calculated average efficiency [Figure 5.25 (d)] increases from 83.5% to 89.0%. For most operating points, further efficiency improvements are achieved with the suboptimal modulation schemes (Section 5.2.2) and the optimal modulation schemes (Section 5.2.1): the respective average efficiencies increase to $\bar{\eta} = 90.3\%$ and $\bar{\eta} = 91.6\%$ [Figure 5.25 (d)]. However, for $V_1 = 240 \text{ V}$, $V_2 = 11 \text{ V}$, and $P_{\text{out}} = 2 \text{ kW}$, a power dissipation of $P_t = 253 \text{ W}$ is calculated for the extended trapezoidal current mode modulation scheme whereas $P_t = 291 \text{ W}$ results with the suboptimal modulation scheme [cf. Figure 5.25 (c) and Figure 5.26 (a)]. The reason for this result is the reduced inductance required to achieve 2 kW output power for the extended trapezoidal current mode modulation ($L = 18.7 \mu\text{H}$). Thus, at a given operating point, fixed duty cycles D_1 and D_2 , and $L = 18.7 \mu\text{H}$, the employed phase shift angle φ is less than the phase shift angle required for $L = 26.7 \mu\text{H}$. Consequently, at high power levels, a decrease of the transformer RMS currents may be achieved by reducing the inductance values: with $L = 18.7 \mu\text{H}$, $V_1 = 240 \text{ V}$, $V_2 = 11 \text{ V}$, $P_{\text{out}} = 2 \text{ kW}$, and the suboptimal modulation schemes being employed, the total losses de-

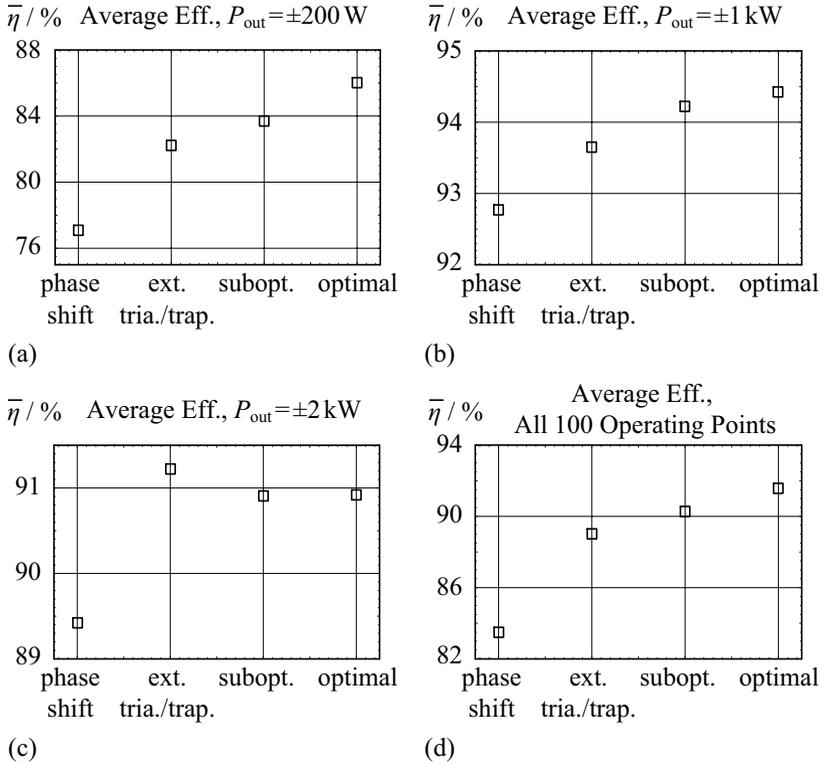


Figure 5.25: Calculated mean efficiencies for the different modulation schemes [phase shift modulation, extended triangular and trapezoidal current mode modulation (Section 5.1), suboptimal modulation (Section 5.2.2), and optimal modulation (Section 5.2.1)], averaged over all regarded voltages V_1 and V_2 (cf. Table 5.2) and different output power levels: (a) $P_{\text{out}} = \pm 200 \text{ W}$, (b) $P_{\text{out}} = \pm 1 \text{ kW}$, (c) $P_{\text{out}} = \pm 2 \text{ kW}$, (d) average efficiency regarding all 100 operating points given in Table 5.2; $n = 19$, $L_M = 2.7 \text{ mH}$, and $f_S = 100 \text{ kHz}$; $L = 26.7 \mu\text{H}$ applies for Figures (a), (c), and (d); $L = 18.7 \mu\text{H}$ applies for Figure (b).

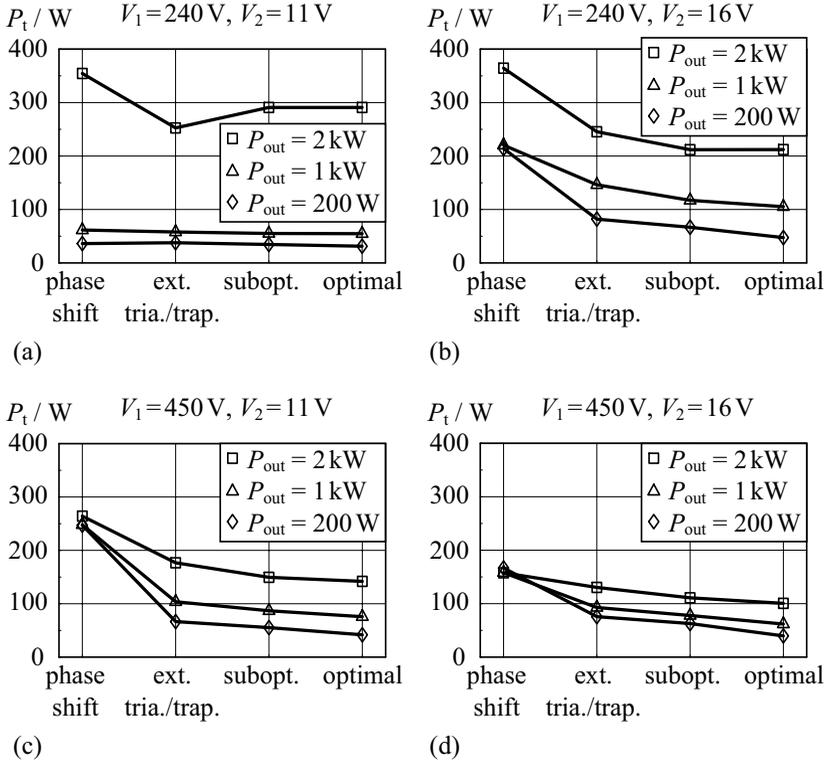


Figure 5.26: Calculated total converter losses for the different modulation schemes [phase shift modulation, extended triangular and trapezoidal current mode modulation (Section 5.1), suboptimal modulation (Section 5.2.2), and optimal modulation (Section 5.2.1)], power being transferred to the LV port, and different operating points: (a) $V_1 = 240 \text{ V}, V_2 = 11 \text{ V}$, (b) $V_1 = 240 \text{ V}, V_2 = 16 \text{ V}$, (c) $V_1 = 450 \text{ V}, V_2 = 11 \text{ V}$, (d) $V_1 = 450 \text{ V}, V_2 = 16 \text{ V}$; $n = 19$, $L_M = 2.7 \text{ mH}$, and $f_S = 100 \text{ kHz}$; $L = 26.7 \mu\text{H}$ applies for phase shift modulation, suboptimal modulation, and optimal modulation; $L = 18.7 \mu\text{H}$ is required for the extended triangular and trapezoidal current mode modulation.

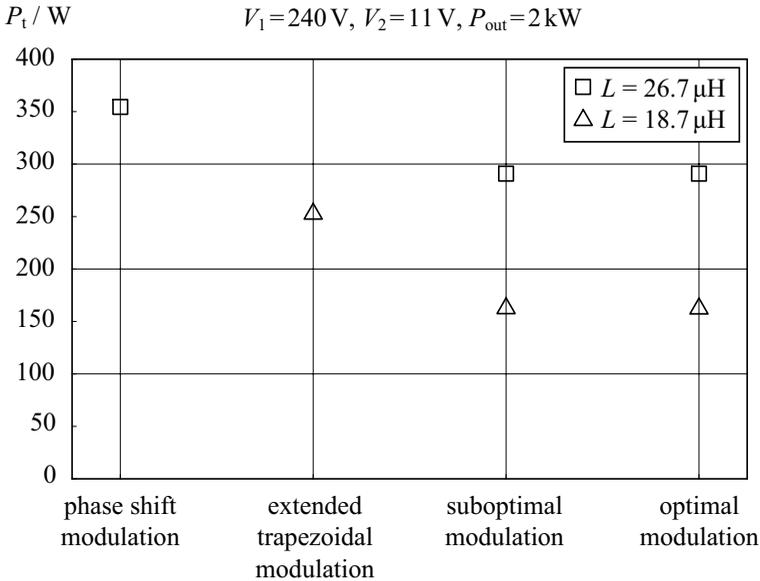


Figure 5.27: Efficiencies obtained with $V_1 = 240 \text{ V}$, $V_2 = 11 \text{ V}$, $P_{\text{out}} = 2 \text{ kW}$, $n = 19$, and $f_S = 100 \text{ kHz}$ for different modulation schemes and different inductance values: at high power levels and low DC voltages V_1 and V_2 , the losses decrease with decreasing L , due to a reduction of the transformer RMS currents.

crease from 291 W to 162 W (Figure 5.27). A reduction of L , however, causes a reduced average efficiency at low and medium power levels if the DAB converter is operated within wide input and output voltage ranges.⁷ Therefore, L is designed with respect to maximum average efficiency (Appendix A.1).

In Figure 5.28, the efficiency achieved with the suboptimal modulation scheme is compared to the maximum achievable efficiency and the efficiency achieved with phase shift modulation. Moreover, two different operating voltages are considered in Figure 5.28: $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$ [Figure 5.28 (a)] and $V_1 = 240 \text{ V}$, $V_2 = 16 \text{ V}$ [Figure 5.28 (b)]. For $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, and phase shift modulation, high efficiency is only achieved for $P_{\text{out}} > 2 \text{ kW}$. In contrast, with the suboptimal modulation schemes (detailed in Section 5.2.2),

⁷Consider, for example, phase shift modulation at zero output power (i.e. Figure 3.4 with $T_\varphi = 0$). There, the inductor current changes according to the second equation given in (3.11) and therefore, the inductor RMS current is proportional to $|V_1 - nV_2|/L$.

the DAB converter operates close to the maximum achievable efficiency. Due to the use of the extended triangular current mode modulation at low and medium power levels the efficiency is approximately 1% to 2% below the maximum possible efficiency for $P_{\text{out}} < 1000 \text{ W}$ and less than 1% below the maximum achievable efficiency for $P_{\text{out}} > 1000 \text{ W}$ [Figure 5.28 (a)].

With the calculation procedure outlined in Section 4.6.1, employed to accurately predict the converter efficiency for the different operating points, good matching between calculated and measured waveforms is achieved (Figure 5.29). Thus, the calculated current RMS values (required to calculate the conduction and copper losses) and the instantaneous current values (needed to calculate the switching losses) are close to the values obtained with the DAB hardware prototype.

The converter efficiency is measured for the suboptimal modulation schemes and different operating points in order to verify the calculated results (for these measurements the optimized DAB designed in Appendix A.2 with $n = 16$ and $L = 22.4 \mu\text{H}$ is employed; the efficiency measurement is conducted at room temperature according to Chapter 4). Figure 5.30 illustrates the result; the \square -symbols indicate measured values and solid lines denote the calculated efficiencies. The depicted results show good matching between calculated and measured results; accordingly, the employed loss model (Chapter 4) and the numerical calculation outlined in Section 4.6.1 are adequate for determining the suboptimal modulation schemes. Finally, the efficiencies calculated within the input and output voltage ranges specified in Table 1.4 are depicted in Figure 5.31 for the optimized DAB with $n = 16$ and $L = 22.4 \mu\text{H}$ and for different output power levels (cf. Figure 5.1).

5.2.4 Conclusion

With the presented modulation schemes, converter operation close to maximum converter efficiency is achieved:

- the extended triangular and trapezoidal current mode modulation schemes facilitate a comparably simple and intuitive method to obtain the modulation parameters D_1 , D_2 , and φ ; however, the achieved average converter efficiency [cf. (A.1)] is slightly less than the average efficiency achieved with the suboptimal modulation schemes (Appendix A.2);
- the suboptimal modulation schemes achieve a converter efficiency close to the maximum converter efficiency (Figure 5.28), though, compared to the extended trapezoidal current mode modulation scheme, the calculation of D_1 and D_2 is considerably more complex.

The key achievements with these modulation schemes are:

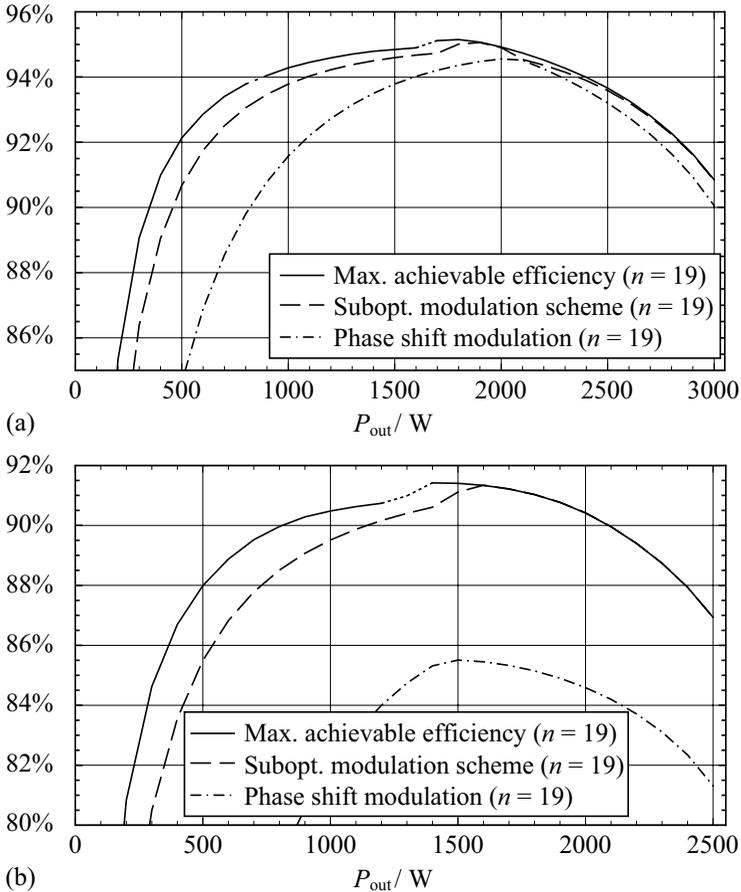
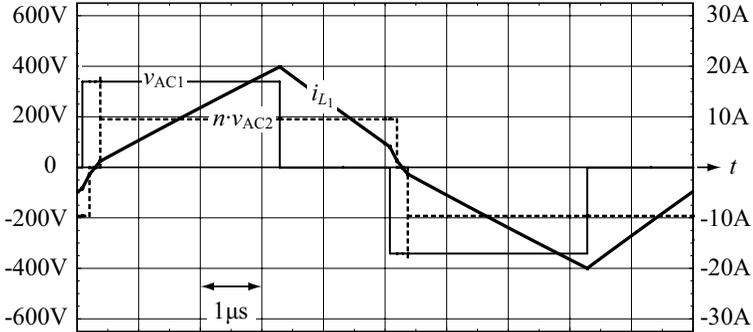
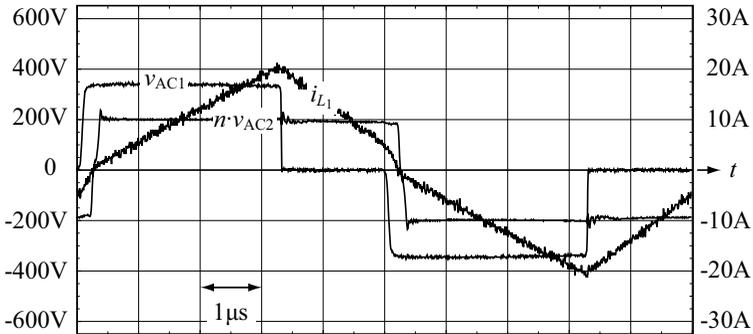


Figure 5.28: Efficiencies calculated for different modulation schemes and two different operating points: (a) $V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$ and (b) $V_1 = 240\text{ V}$, $V_2 = 16\text{ V}$; the solid line denotes the maximum achievable efficiency calculated according to Section 5.2.1, the dashed line denotes the efficiency achieved with the suboptimal modulation schemes (Section 5.2.2) and the line with alternating dashes and dots marks the efficiency obtained with phase shift modulation. With the optimized modulation scheme, highly efficient converter operation, close to maximum efficiency, is achieved ($n = 19$, $L = 26.7\text{ }\mu\text{H}$, $T_j = 25^\circ\text{C}$).



(a)



(b)

Figure 5.29: (a) Calculated and (b) measured voltage and current waveforms obtained with the suboptimal modulation schemes for $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, and $P_2 = 2 \text{ kW}$; for all measurements, the efficiency optimized DAB design with $n = 16$ and $L = 22.4 \mu\text{H}$ is employed (cf. Appendix A.2); at the nominal operating point, the instantaneous switch current during switching of the LV side switches is close to zero and therefore, the overvoltage switching spikes contained in the calculation of $v_{AC2}(t)$ (Section 4.3.3) are almost negligible.

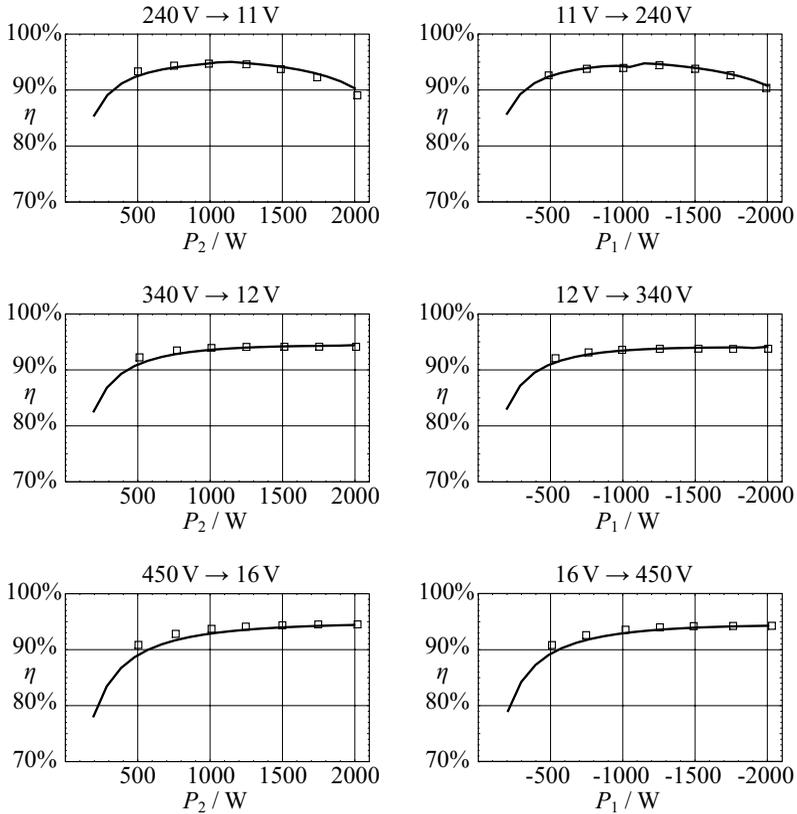


Figure 5.30: Predicted efficiencies (solid lines) and measured efficiencies (\square) obtained with the suboptimal modulation schemes and for different operating conditions; the efficiencies are calculated with the full DAB loss model discussed in Section 4; for all measurements, the efficiency optimized DAB design with $n = 16$ and $L = 22.4 \mu\text{H}$ is employed (cf. Appendix A.2).

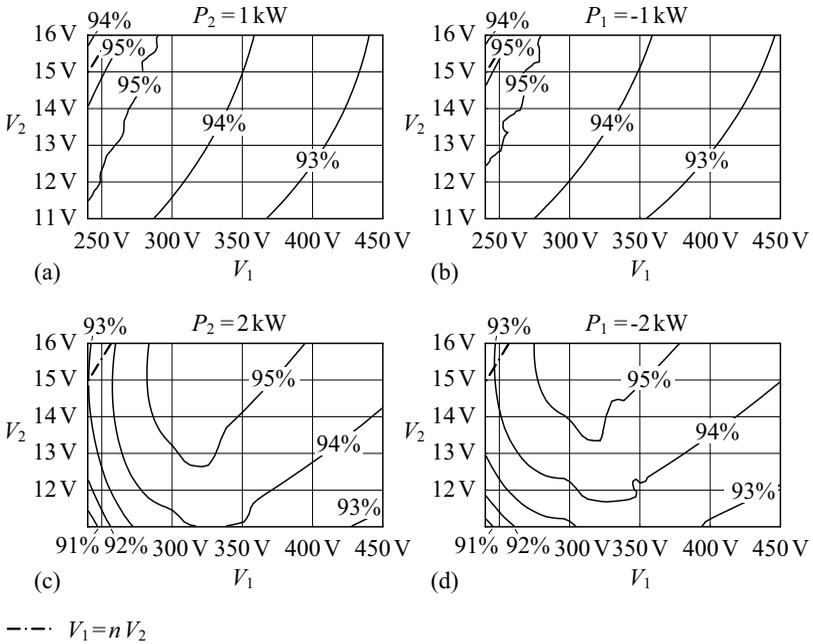
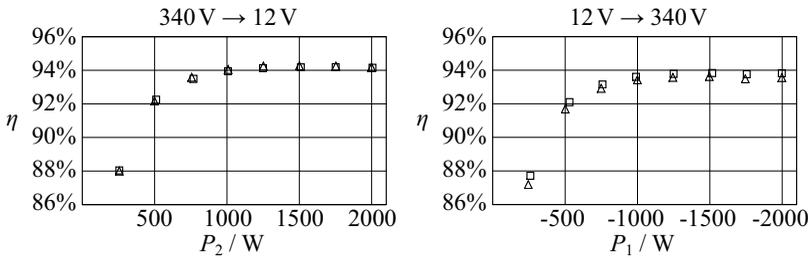


Figure 5.31: Efficiencies predicted for the optimized DAB with $n = 16$ and $L = 22.4 \mu\text{H}$ within the input and output voltage ranges specified in Table 1.4, different output power levels, and different directions of power transfer (cf. Appendix A.2): (a) LV \leftarrow LV, $P_{\text{out}} = 1 \text{ kW}$; (a) HV \leftarrow LV, $P_{\text{out}} = 1 \text{ kW}$; (a) LV \leftarrow HV, $|P_{\text{out}}| = 1 \text{ kW}$; (c) HV \leftarrow LV, $P_{\text{out}} = 2 \text{ kW}$; (d) LV \leftarrow HV, $|P_{\text{out}}| = 2 \text{ kW}$. The efficiency calculation considers the effect of the linear interpolation used by the DSP to determine the actual modulation parameters (Appendix E.2); this causes the irregular characteristics of the depicted contour lines.

1. low transformer RMS currents (low conduction and copper losses);
2. ZVS on the HV side;
3. switch currents close to zero (if possible) on the LV side (low switching losses on the LV side).

With the use of these modulation schemes, efficiency improvements are achieved without changing (and in particular extending) the DAB hardware (except for the selection of n and L according to Section A.2). Further efficiency improvements may be achieved by reducing the magnetizing inductance L_M : the resulting circulating transformer currents extend the ZVS range [50] and thus, a reduction of the HV side switching losses can be achieved, while the RMS transformer on the LV side can be reduced. An according investigation, however, confirms that this modification is only effective at medium power levels; at high power levels ZVS is naturally achieved with $L_M \rightarrow \infty$ (thus, a reduced magnetizing inductance causes the conduction losses to increase) and at low power levels the voltage-time-area applied to L_M is insufficient to obtain the current level required for ZVS. For the presented converter, it was tried to achieve a high efficiency without the use of additional hardware components; if additional power components can be employed, a multitude of different hardware extensions, used to achieve ZVS for the full operating range at arbitrary currents $i_L(t_{\text{sw}})$, are discussed in literature (e.g. resonant pole circuits [110,111], auxiliary resonant pole circuits [85,112,113], and ZVS-FB converters using a modified HF transformer with center tapping [82,83]).

Furthermore, the employed loss model is evaluated at room temperature ($T = T_j = 25^\circ\text{C}$) and therefore, the presented calculations and measurements do not consider the impact of increased component temperatures (cf. Chapter 4). However, comparably low losses result with the suboptimal modulation schemes and thus, the efficiencies obtained during continuous converter operation are similar to the efficiencies obtained for a limited run time of 30 seconds (Figure 5.32).



- \square Short-time operation (30 s per measurement)
- \triangle Continuous operation (> 1 h continuous run, > 10 min. per measurement)

Figure 5.32: Comparison of different efficiency measurements: the \square -symbols denote the efficiencies measured after a short operating time of 30 seconds (i.e. $T_j \approx 25^\circ\text{C}$, cf. Chapter 4) and the \triangle -symbols denote the efficiencies measured during continuous converter operation (at room temperature); $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, suboptimal modulation schemes; (a) power transfer from the HV port to the LV port; (b) opposite power transfer (LV → HV). Due to the effective water cooler and the comparably low losses obtained with the suboptimal modulation schemes, similar efficiencies are obtained for a short operating time and for continuous operation.

P_{out}	Phase shift modulation $L = 26.7 \mu\text{H}$			Extended triangular and trapezoidal current mode modulation $L = 18.7 \mu\text{H}$			Suboptimal modulation $L = 26.7 \mu\text{H}$			Optimal modulation $L = 26.7 \mu\text{H}$		
	$P_{\text{h,PS}}$	η_{PS}	$P_{\text{h,TT}}$	η_{TT}	$\Delta\eta_{\text{TT}}$	$P_{\text{h,subopt}}$	η_{subopt}	$\Delta\eta_{\text{subopt}}$	$P_{\text{h,opt}}$	η_{opt}	$\Delta\eta_{\text{opt}}$	
	$V_1 = 340 \text{ V}, V_2 = 12 \text{ V}$											
200 W	92 W	68.4%	54 W	78.9%	10.4%	46 W	81.4%	12.9%	34 W	85.3%	16.9%	
-200 W	88 W	69.5%	49 W	80.3%	10.8%	43 W	82.1%	12.6%	34 W	85.6%	16.1%	
500 W	91 W	84.6%	60 W	89.3%	4.6%	51 W	90.7%	6.0%	43 W	92.1%	7.5%	
-500 W	89 W	84.9%	57 W	89.7%	4.8%	50 W	90.8%	5.9%	43 W	92.1%	7.2%	
1 kW	92 W	91.6%	77 W	92.9%	1.3%	66 W	93.8%	2.2%	61 W	94.3%	2.7%	
-1 kW	95 W	91.4%	78 W	92.8%	1.4%	68 W	93.7%	2.3%	63 W	94.0%	2.7%	
1.5 kW	99 W	93.8%	99 W	93.8%	0.0%	86 W	94.6%	0.8%	82 W	94.8%	1.1%	
-1.5 kW	107 W	93.3%	104 W	93.5%	0.2%	90 W	94.3%	1.0%	88 W	94.5%	1.2%	
2 kW	115 W	94.6%	125 W	94.1%	-0.3%	107 W	94.9%	0.3%	107 W	94.9%	0.4%	
-2 kW	130 W	93.9%	136 W	93.6%	-0.1%	116 W	94.5%	0.6%	116 W	94.5%	0.6%	
	$V_1 = 240 \text{ V}, V_2 = 11 \text{ V}$											
200 W	36 W	84.7%	38 W	84.1%	-0.5%	35 W	85.3%	0.6%	31 W	86.5%	1.8%	
-200 W	36 W	84.7%	37 W	84.5%	-0.1%	34 W	85.6%	0.8%	32 W	86.1%	1.4%	
500 W	36 W	93.2%	41 W	92.4%	-0.8%	38 W	92.9%	-0.2%	35 W	93.4%	0.2%	
-500 W	37 W	93.0%	42 W	92.3%	-0.6%	38 W	92.9%	-0.1%	37 W	93.1%	0.1%	
1 kW	62 W	94.2%	58 W	94.5%	0.3%	55 W	94.8%	0.6%	55 W	94.8%	0.6%	
-1 kW	58 W	94.5%	57 W	94.6%	0.0%	55 W	94.8%	0.3%	54 W	94.9%	0.4%	
1.5 kW	133 W	91.9%	106 W	93.4%	1.5%	109 W	93.2%	1.3%	109 W	93.2%	1.3%	
-1.5 kW	116 W	92.8%	100 W	93.7%	0.9%	104 W	93.5%	0.7%	103 W	93.6%	0.7%	
2 kW	354 W	84.9%	253 W	88.8%	3.8%	291 W	87.3%	2.4%	291 W	87.3%	2.4%	
-2 kW	247 W	89.0%	211 W	90.5%	1.4%	231 W	89.6%	0.6%	231 W	89.7%	0.6%	

Table 5.2: Calculated losses and efficiencies for different operating points and for phase shift modulation, extended triangular and trapezoidal current mode modulation (Section 5.1), optimized modulation (Section 5.2.2), and optimal modulation (Section 5.2.1); $n = 19$, $L_M = 2.7 \text{ mH}$, and $f_S = 100 \text{ kHz}$; $L = 26.7 \mu\text{H}$ applies for phase shift modulation, optimized modulation, and optimal modulation; $L = 18.7 \mu\text{H}$ is required for the extended triangular and trapezoidal current mode modulation.

P_{out}	Phase shift modulation $L = 26.7 \mu\text{H}$		Extended triangular and trapezoidal current mode modulation $L = 18.7 \mu\text{H}$		Suboptimal modulation $L = 26.7 \mu\text{H}$		Optimal modulation $L = 26.7 \mu\text{H}$				
	$P_{\text{t,PS}}$	η_{PS}	$P_{\text{t,TT}}$	η_{TT}	$\Delta\eta_{\text{TT}}$	$P_{\text{t,subopt}}$	η_{subopt}	$\Delta\eta_{\text{subopt}}$	$P_{\text{t,opt}}$	η_{opt}	$\Delta\eta_{\text{opt}}$
	$V_1 = 240 \text{ V}, V_2 = 13.5 \text{ V}$										
200 W	79 W	71.7%	63 W	76.1%	4.4%	52 W	79.4%	7.7%	36 W	84.7%	13.1%
-200 W	98 W	67.1%	53 W	79.4%	12.4%	46 W	81.2%	14.1%	35 W	85.1%	18.1%
500 W	75 W	87.0%	71 W	87.5%	0.5%	59 W	89.4%	2.4%	48 W	91.3%	4.2%
-500 W	92 W	84.5%	60 W	89.3%	4.8%	53 W	90.4%	5.9%	45 W	91.7%	7.2%
1 kW	99 W	91.0%	89 W	91.9%	0.9%	69 W	93.5%	2.6%	69 W	93.5%	2.6%
-1 kW	82 W	92.4%	75 W	93.0%	0.6%	63 W	94.1%	1.7%	63 W	94.1%	1.7%
1.5 kW	168 W	89.9%	128 W	92.2%	2.2%	114 W	92.9%	3.0%	114 W	92.9%	3.0%
-1.5 kW	133 W	91.9%	109 W	93.2%	1.4%	101 W	93.7%	1.8%	101 W	93.7%	1.8%
2 kW	293 W	87.2%	205 W	90.7%	3.5%	209 W	90.5%	3.3%	209 W	90.5%	3.3%
-2 kW	215 W	90.3%	169 W	92.2%	1.9%	174 W	92.0%	1.7%	174 W	92.0%	1.7%
	$V_1 = 240 \text{ V}, V_2 = 16 \text{ V}$										
200 W	214 W	48.3%	82 W	70.9%	22.6%	67 W	75.0%	26.7%	47 W	80.8%	32.5%
-200 W	238 W	45.6%	68 W	74.7%	29.1%	59 W	77.2%	31.5%	45 W	81.7%	36.0%
500 W	212 W	70.2%	105 W	82.6%	12.4%	85 W	85.5%	15.3%	68 W	88.0%	17.8%
-500 W	232 W	68.3%	89 W	84.9%	16.6%	76 W	86.8%	18.5%	63 W	88.8%	20.5%
1 kW	220 W	81.9%	146 W	87.2%	5.3%	117 W	89.5%	7.6%	105 W	90.5%	8.5%
-1 kW	224 W	81.7%	124 W	89.0%	7.3%	105 W	90.5%	8.8%	94 W	91.4%	9.7%
1.5 kW	254 W	85.5%	191 W	88.7%	3.2%	146 W	91.1%	5.6%	141 W	91.4%	5.9%
-1.5 kW	227 W	86.8%	160 W	90.4%	3.5%	134 W	91.8%	4.9%	131 W	92.0%	5.1%
2 kW	364 W	84.6%	245 W	89.1%	4.5%	212 W	90.4%	5.8%	212 W	90.4%	5.8%
-2 kW	264 W	88.3%	200 W	90.9%	2.6%	178 W	91.8%	3.5%	178 W	91.8%	3.5%

Table 5.2 cont.: Calculated losses and efficiencies for different operating points and for phase shift modulation, extended triangular and trapezoidal current mode modulation (Section 5.1), optimized modulation (Section 5.2.2), and optimal modulation (Section 5.2.1)); $n = 19$, $L_M = 2.7 \text{ mH}$, and $f_S = 100 \text{ kHz}$; $L = 26.7 \mu\text{H}$ applies for phase shift modulation, optimized modulation, and optimal modulation; $L = 18.7 \mu\text{H}$ is required for the extended triangular and trapezoidal current mode modulation.

P_{out}	Phase shift modulation $L = 26.7 \mu\text{H}$		Extended triangular and trapezoidal current mode modulation $L = 18.7 \mu\text{H}$				Suboptimal modulation $L = 26.7 \mu\text{H}$				Optimal modulation $L = 26.7 \mu\text{H}$			
	$P_{\text{t,PS}}$	η_{PS}	$P_{\text{t,TT}}$	η_{TT}	$\Delta\eta_{\text{TT}}$	$P_{\text{t,subopt}}$	η_{subopt}	$\Delta\eta_{\text{subopt}}$	$P_{\text{t,opt}}$	η_{opt}	$\Delta\eta_{\text{opt}}$			
	$V_1 = 345 \text{ V}, V_2 = 11 \text{ V}$													
200 W	107 W	65.0%	53 W	79.0%	13.9%	45 W	81.5%	16.5%	34 W	85.4%	20.3%			
-200 W	103 W	66.0%	49 W	80.4%	14.4%	43 W	82.2%	16.2%	34 W	85.5%	19.4%			
500 W	107 W	82.4%	61 W	89.1%	6.6%	52 W	90.5%	8.1%	44 W	91.9%	9.5%			
-500 W	105 W	82.7%	59 W	89.4%	6.8%	52 W	90.6%	8.0%	44 W	91.9%	9.2%			
1 kW	109 W	90.2%	82 W	92.4%	2.2%	71 W	93.4%	3.2%	65 W	93.9%	3.7%			
-1 kW	113 W	89.9%	84 W	92.3%	2.4%	72 W	93.3%	3.4%	68 W	93.6%	3.8%			
1.5 kW	118 W	92.7%	109 W	93.2%	0.5%	94 W	94.1%	1.4%	90 W	94.4%	1.7%			
-1.5 kW	128 W	92.1%	115 W	92.9%	0.7%	99 W	93.8%	1.7%	97 W	94.0%	1.8%			
2 kW	137 W	93.6%	140 W	93.5%	-0.0%	120 W	94.3%	0.8%	120 W	94.4%	0.8%			
-2 kW	156 W	92.8%	153 W	92.9%	0.1%	132 W	93.8%	1.0%	132 W	93.8%	1.0%			
	$V_1 = 345 \text{ V}, V_2 = 13.5 \text{ V}$													
200 W	82 W	70.9%	56 W	78.2%	7.2%	48 W	80.7%	9.8%	35 W	84.9%	14.0%			
-200 W	78 W	72.0%	51 W	79.8%	7.7%	45 W	81.6%	9.6%	34 W	85.4%	13.4%			
500 W	80 W	86.3%	60 W	89.3%	3.0%	52 W	90.6%	4.3%	43 W	92.1%	5.9%			
-500 W	78 W	86.6%	57 W	89.7%	3.2%	50 W	90.8%	4.3%	42 W	92.3%	5.7%			
1 kW	79 W	92.7%	73 W	93.2%	0.5%	63 W	94.1%	1.4%	57 W	94.6%	1.9%			
-1 kW	81 W	92.5%	73 W	93.2%	0.7%	64 W	94.0%	1.5%	61 W	94.3%	1.8%			
1.5 kW	84 W	94.7%	90 W	94.3%	-0.3%	78 W	95.0%	0.3%	74 W	95.3%	0.6%			
-1.5 kW	90 W	94.3%	94 W	94.1%	-0.1%	82 W	94.8%	0.5%	79 W	95.0%	0.6%			
2 kW	97 W	95.4%	110 W	94.8%	-0.5%	97 W	95.4%	0.0%	94 W	95.5%	0.2%			
-2 kW	106 W	95.0%	119 W	94.4%	-0.5%	100 W	95.3%	0.3%	99 W	95.3%	0.3%			

Table 5.2 cont.: Calculated losses and efficiencies for different operating points and for phase shift modulation, extended triangular and trapezoidal current mode modulation (Section 5.1), optimized modulation (Section 5.2.2), and optimal modulation (Section 5.2.1)); $n = 19$, $L_M = 2.7 \text{ mH}$, and $f_S = 100 \text{ kHz}$; $L = 26.7 \mu\text{H}$ applies for phase shift modulation, optimized modulation, and optimal modulation; $L = 18.7 \mu\text{H}$ is required for the extended triangular and trapezoidal current mode modulation.

P_{out}	Phase shift modulation $L = 26.7 \mu\text{H}$		Extended triangular and trapezoidal current mode modulation $L = 18.7 \mu\text{H}$				Suboptimal modulation $L = 26.7 \mu\text{H}$				Optimal modulation $L = 26.7 \mu\text{H}$			
	$P_{\text{k,PS}}$	η_{PS}	$P_{\text{k,TT}}$	η_{TT}	$\Delta\eta_{\text{TT}}$	$P_{\text{k,subopt}}$	η_{subopt}	$\Delta\eta_{\text{subopt}}$	$P_{\text{k,opt}}$	η_{opt}	$\Delta\eta_{\text{opt}}$			
	$V_1 = 345 \text{ V}, V_2 = 16 \text{ V}$													
200 W	60 W	76.8%	73 W	73.3%	-3.4%	59 W	77.3%	0.5%	40 W	83.3%	6.5%			
-200 W	59 W	77.3%	53 W	79.1%	1.7%	48 W	80.7%	3.4%	38 W	83.9%	6.6%			
500 W	57 W	89.8%	59 W	89.4%	-0.3%	52 W	90.6%	0.8%	44 W	92.0%	2.2%			
-500 W	57 W	89.8%	57 W	89.8%	0.0%	51 W	90.8%	1.0%	46 W	91.5%	1.7%			
1 kW	54 W	94.9%	66 W	93.8%	-1.0%	59 W	94.4%	-0.3%	53 W	95.0%	0.1%			
-1 kW	57 W	94.6%	66 W	93.8%	-0.7%	59 W	94.4%	-0.1%	56 W	94.7%	0.1%			
1.5 kW	66 W	95.8%	75 W	95.2%	-0.4%	63 W	96.0%	0.2%	62 W	96.0%	0.3%			
-1.5 kW	64 W	95.9%	79 W	95.0%	-0.8%	63 W	96.0%	0.0%	62 W	96.0%	0.1%			
2 kW	107 W	94.9%	100 W	95.2%	0.3%	91 W	95.6%	0.7%	91 W	95.7%	0.7%			
-2 kW	99 W	95.3%	98 W	95.3%	0.0%	90 W	95.7%	0.4%	89 W	95.7%	0.5%			
	$V_1 = 450 \text{ V}, V_2 = 11 \text{ V}$													
200 W	247 W	44.7%	67 W	75.0%	30.3%	55 W	78.4%	33.6%	42 W	82.7%	38.0%			
-200 W	237 W	45.7%	60 W	77.0%	31.3%	52 W	79.3%	33.6%	39 W	83.7%	37.9%			
500 W	247 W	67.0%	77 W	86.6%	19.6%	64 W	88.6%	21.6%	50 W	90.9%	23.9%			
-500 W	241 W	67.5%	73 W	87.3%	19.8%	62 W	88.9%	21.4%	51 W	90.8%	23.3%			
1 kW	248 W	80.1%	104 W	90.6%	10.5%	87 W	92.0%	11.9%	76 W	93.0%	12.8%			
-1 kW	249 W	80.0%	103 W	90.7%	10.6%	88 W	91.9%	11.9%	78 W	92.7%	12.7%			
1.5 kW	253 W	85.6%	138 W	91.6%	6.0%	116 W	92.8%	7.3%	107 W	93.3%	7.8%			
-1.5 kW	263 W	85.1%	142 W	91.4%	6.3%	120 W	92.6%	7.5%	114 W	93.0%	7.9%			
2 kW	264 W	88.3%	177 W	91.9%	3.5%	150 W	93.0%	4.7%	142 W	93.4%	5.0%			
-2 kW	285 W	87.5%	187 W	91.4%	3.9%	158 W	92.7%	5.1%	154 W	92.8%	5.3%			

Table 5.2 cont.: Calculated losses and efficiencies for different operating points and for phase shift modulation, extended triangular and trapezoidal current mode modulation (Section 5.1), optimized modulation (Section 5.2.2), and optimal modulation (Section 5.2.1)); $n = 19$, $L_M = 2.7 \text{ mH}$, and $f_S = 100 \text{ kHz}$; $L = 26.7 \mu\text{H}$ applies for phase shift modulation, optimized modulation, and optimal modulation; $L = 18.7 \mu\text{H}$ is required for the extended triangular and trapezoidal current mode modulation.

P_{out}	Phase shift modulation $L = 26.7 \mu\text{H}$		Extended triangular and trapezoidal current mode modulation $L = 18.7 \mu\text{H}$				Suboptimal modulation $L = 26.7 \mu\text{H}$				Optimal modulation $L = 26.7 \mu\text{H}$			
	$P_{\text{k,PS}}$	η_{PS}	$P_{\text{k,TT}}$	η_{TT}	$\Delta\eta_{\text{TT}}$	$P_{\text{k,subopt}}$	η_{subopt}	$\Delta\eta_{\text{subopt}}$	$P_{\text{k,opt}}$	η_{opt}	$\Delta\eta_{\text{opt}}$	$P_{\text{k,opt}}$	η_{opt}	$\Delta\eta_{\text{opt}}$
	$V_1 = 450 \text{ V}, V_2 = 13.5 \text{ V}$													
200 W	204 W	49.4%	71 W	73.9%	24.5%	59 W	77.3%	27.9%	39 W	83.7%	34.3%	39 W	83.7%	34.3%
-200 W	191 W	51.2%	62 W	76.2%	25.0%	55 W	78.5%	27.3%	39 W	83.8%	32.6%	39 W	83.8%	32.6%
500 W	202 W	71.2%	78 W	86.5%	15.3%	65 W	88.5%	17.3%	48 W	91.2%	20.0%	48 W	91.2%	20.0%
-500 W	192 W	72.3%	72 W	87.5%	15.2%	62 W	89.0%	16.7%	48 W	91.3%	19.0%	48 W	91.3%	19.0%
1 kW	200 W	83.3%	97 W	91.2%	7.9%	81 W	92.5%	9.2%	67 W	93.7%	10.4%	67 W	93.7%	10.4%
-1 kW	196 W	83.6%	94 W	91.4%	7.8%	80 W	92.6%	8.9%	69 W	93.6%	10.0%	69 W	93.6%	10.0%
1.5 kW	201 W	88.2%	121 W	92.5%	4.4%	102 W	93.6%	5.5%	91 W	94.3%	6.1%	91 W	94.3%	6.1%
-1.5 kW	204 W	88.0%	122 W	92.5%	4.4%	104 W	93.5%	5.5%	94 W	94.1%	6.0%	94 W	94.1%	6.0%
2 kW	206 W	90.6%	149 W	93.0%	2.4%	127 W	94.0%	3.4%	118 W	94.4%	3.8%	118 W	94.4%	3.8%
-2 kW	217 W	90.2%	156 W	92.8%	2.6%	132 W	93.8%	3.6%	128 W	94.0%	3.8%	128 W	94.0%	3.8%
	$V_1 = 450 \text{ V}, V_2 = 16 \text{ V}$													
200 W	167 W	54.5%	76 W	72.5%	18.0%	63 W	76.1%	21.6%	40 W	83.5%	28.9%	40 W	83.5%	28.9%
-200 W	153 W	56.7%	66 W	75.1%	18.5%	58 W	77.5%	20.8%	39 W	83.7%	27.1%	39 W	83.7%	27.1%
500 W	163 W	75.5%	80 W	86.2%	10.8%	67 W	88.2%	12.8%	47 W	91.4%	16.0%	47 W	91.4%	16.0%
-500 W	152 W	76.7%	73 W	87.3%	10.6%	63 W	88.8%	12.1%	46 W	91.5%	14.8%	46 W	91.5%	14.8%
1 kW	158 W	86.4%	93 W	91.5%	5.1%	78 W	92.8%	6.4%	62 W	94.2%	7.8%	62 W	94.2%	7.8%
-1 kW	153 W	86.8%	89 W	91.9%	5.1%	76 W	92.9%	6.1%	63 W	94.1%	7.3%	63 W	94.1%	7.3%
1.5 kW	156 W	90.6%	110 W	93.2%	2.6%	93 W	94.2%	3.6%	80 W	94.9%	4.4%	80 W	94.9%	4.4%
-1.5 kW	156 W	90.6%	109 W	93.2%	2.6%	94 W	94.1%	3.6%	82 W	94.8%	4.3%	82 W	94.8%	4.3%
2 kW	158 W	92.7%	130 W	93.9%	1.2%	111 W	94.7%	2.1%	101 W	95.2%	2.5%	101 W	95.2%	2.5%
-2 kW	164 W	92.4%	134 W	93.7%	1.3%	115 W	94.6%	2.2%	108 W	94.9%	2.5%	108 W	94.9%	2.5%

Table 5.2 cont.: Calculated losses and efficiencies for different operating points and for phase shift modulation, extended triangular and trapezoidal current mode modulation (Section 5.1), optimized modulation (Section 5.2.2), and optimal modulation (Section 5.2.1)); $n = 19$, $L_M = 2.7 \text{ mH}$, and $f_S = 100 \text{ kHz}$; $L = 26.7 \mu\text{H}$ applies for phase shift modulation, optimized modulation, and optimal modulation; $L = 18.7 \mu\text{H}$ is required for the extended triangular and trapezoidal current mode modulation.

Chapter 6

Dynamic DAB Model and Control

In order for the presented converter to operate at a designated power level and a desired direction of power transfer, a two loop control structure is employed: the inner control loop adjusts the required current (e.g. on the high voltage side) and the superimposed voltage control loop regulates the respective output voltage.¹ Thus, in order to enable the controller design, the small-signal model of the DAB converter needs to be determined.

First small-signal models of switching power converters have been calculated with averaged switched circuits [114]. There, a converter circuit diagram results, which partly consists of the original circuit (except for switches and diodes) and additional current sources or voltage sources or both that model the low frequency system dynamics. It thus presents the small-signal system dynamics in a comprehensible way to the engineer. However, its construction requires circuit arrangements and is thus not accomplished in a straightforward way; with the introduction of state space averaging [115], the automated derivation of small-signal transfer functions has been achieved. Both methods employ the local average values of all independent system properties (e.g. inductor currents, capacitor voltages) and all input and output variables (e.g. actuating variable, output current), calculated over one switching period T_S in order to determine the desired transfer functions. A precise small-signal and continuous-time transfer function approximation is thus achieved for frequencies well below $1/T_S$ [114,116] and well below the filter cut-off frequencies (negligible current and voltage ripples are assumed). These two methods presumably compute wrong transfer functions for the given DAB power converter

¹For power being transferred from the high voltage DC bus to the 14 V DC bus, V_2 becomes the output voltage (cf. Figure 6.1). Hence, the voltage control loop may become very sensitive due to the high electric storage capability of the 12 V battery and the voltage control loop may be replaced by a voltage inspection and battery charging algorithm and / or battery charging current control.

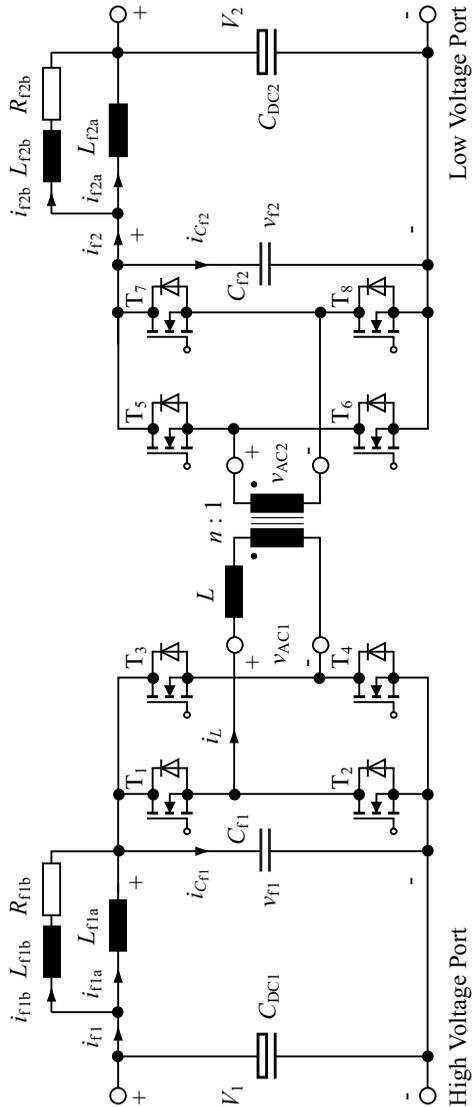


Figure 6.1: Dual active bridge (DAB) converter with EMI filters connected to the high voltage (HV) and to the low voltage (LV) ports.

(Figure 6.1), since the assumption of negligible current ripple is not satisfied for the transformer and inductor current i_L . A very accurate, but discrete-time, small-signal model is obtained with the discrete modeling of switching regulators [117] which solely assumes a “small” input signal excitation around a steady-state value in order to reduce the nonlinear (exact) large signal model to a linear small-signal model.

Today, many applications still employ continuous-time regulators, e.g. low power and low cost converters that are used for standard applications and where integrated regulators are available. There, the discrete-time nature of the transfer function obtained with [117] is considered disadvantageous and thus, numerous extensions to the discrete-time modeling approach have been developed in order to achieve a highly accurate continuous-time small-signal converter model, for instance the so-called sampled data modeling [118]. For many high power converters, though, digital signal processors (DSPs) are increasingly employed, mainly because today a high computational performance is available at a comparably low cost. Advantages of a digital implementation are a considerably higher flexibility compared to analog electronics, a high EMI immunity, and the enhanced possibility of process and fault monitoring using an external interface or a network connection. Therefore, a digital control platform is employed for the control of the presented DAB and thus, the discrete-time transfer function obtained with discrete modeling could readily be used for the controller design. However, [117] only focuses on simple DC–DC converters (e.g. boost converter) operated with PWM modulation. An extension to resonant power converters including modulator constraints is presented in [119] and a straight forward summary on the construction of a discrete-time small-signal model for arbitrary resonant converters is discussed in [120]. Merely the time lag that arises due to software and A/D converter delay times is not considered in [120] and could be included using the procedure discussed in [121].

In this Chapter, an exact discrete-time DAB model including input and output filter dynamics is developed and verified with results obtained from an experimental system. Moreover, a flexible control structure, which allows for optimized modulation and control algorithms, is proposed and detailed. The effect of time delays, mainly due to software processing time, is identified to be crucial with respect to a sufficiently large phase margin. The obtained results facilitate a significantly simplified construction of the DAB control-to-output transfer function, which can be universally employed to design the digital controllers.

In Section 6.1, the small-signal model for the DAB is derived; the employed control loop is discussed in Section 6.2; and in Section 6.3, the design of the digital current and voltage controllers is detailed. The calculated results are verified with measured results in Sections 6.2 and 6.3.

6.1 Small-Signal Model

The proposed control structure, depicted in Figure 6.2, mainly consists of digital signal processing blocks: the voltage controller ($G_{C,V}$), the current controller ($G_{C,I}$), and the digital filters ($\mathbf{H}_{\text{filter}}$, H_{avg}) are fully implemented in a DSP; software and A/D converter time delays ($\mathbf{G}_{\text{Td,DSP}}$, $\mathbf{G}_{\text{Td,FPGA}}$, $\mathbf{G}_{\text{Td,meas}}$) are due to the digital implementation. Besides, the modulator function ($\mathbf{G}_{\text{mod,PS}}$ or $\mathbf{G}_{\text{mod,alt}}$) is realized in the DSP and determines the required timing values for the DAB [e.g. $T_\varphi = \varphi/(2\pi f_S)$ for phase shift modulation based on (3.13)] with respect to the desired controller set value $I_{1,\text{mod}}$ and the selected modulation scheme. Variations of these timing values dynamically alter the transferred power of the DAB power stage. The resulting changes of the filter currents $i_{f1}(t)$, $i_{f2}(t)$ and the filter voltages $v_{f1}(t)$, $v_{f2}(t)$ (cf. Figure 6.1) are obtained from the DAB small-signal model \mathbf{G}_{PE} (the voltages V_1 and V_2 remain approximately constant during one switching period T_S , since very large filter capacitors C_{DC1} and C_{DC2} are considered).

The full control diagram (Figure 6.2) indicates two transfer functions, that need to be determined in order to further investigate the control loop: the control-to-output transfer function \mathbf{G}_{PE} of the DAB and the transfer function of the modulator.

6.1.1 DAB Power Stage, Phase Shift Modulation

Phase shift modulation is the most simple as well as the most common modulation method for the DAB. Therefore, the small-signal transfer function is first derived for this basic modulation scheme.

The small-signal calculation method outlined in [120] regards a single half-cycle (e.g. $0 < t \leq T_S/2$ in Figure 3.4) and separately considers the time intervals between two switching events (time intervals I and II in Figure 3.4). Within these time intervals, the time domain expressions for all system state variables (i.e. all time varying inductor currents and capacitor voltages) are required in order to determine their sensitivity on input signal variations. With the employed method, the state variables at the end of a half-cycle are compared to the state variables at the beginning of the corresponding half-cycle. This allows for the formulation of the control-to-output transfer function in discrete-time domain.

Prior to the derivation of the transfer function, system inputs and outputs must be defined. Clearly, the timing parameter T_φ is an input to the dynamic system. Additionally, the voltages V_1 and V_2 may be considered as inputs, too. The proposed system outputs are the filter current $i_{f1}(t) = i_{f1a}(t) + i_{f1b}(t)$ and the filter voltages $v_{f1}(t)$, $n v_{f2}(t)$. Further, it is reasonable to collect the

system state variables in a state vector \vec{x} :

$$\vec{x} = (i_L \quad i_{f1a} \quad i_{f1b} \quad i_{f2a}/n \quad i_{f2b}/n \quad v_{f1} \quad n v_{f2})^T. \quad (6.1)$$

In a next step, the time domain expressions for the system state variables need to be derived. These may change at each switching instant indicated in Figure 3.4. For the sake of clarity the time domain expressions during each time interval i are combined to one single function

$$\begin{aligned} \vec{f}_{\text{PS},i}(\vec{x}_{i-1}, \Delta t_i) = & \begin{bmatrix} i_{L,i}(\vec{x}_{i-1}, \Delta t_i) \\ i_{f1a,i}(\vec{x}_{i-1}, \Delta t_i) & i_{f1b,i}(\vec{x}_{i-1}, \Delta t_i) \\ i_{f2a,i}(\vec{x}_{i-1}, \Delta t_i)/n & i_{f2b,i}(\vec{x}_{i-1}, \Delta t_i)/n \\ v_{f1,i}(\vec{x}_{i-1}, \Delta t_i) & n v_{f2,i}(\vec{x}_{i-1}, \Delta t_i) \end{bmatrix}^T. \end{aligned} \quad (6.2)$$

In (6.2), Δt_i denotes the time within the considered time interval (i.e. Δt_i is zero at the beginning of the i -th time interval) and \vec{x}_{i-1} contains the initial values, so $\vec{f}_{\text{PS},i}(\vec{x}_{i-1}, 0) = \vec{x}_{i-1}$; the index ‘‘PS’’ denotes the phase shift modulation, the index i specifies the considered time interval. The analysis considers two different time intervals for phase shift modulation (Figure 3.4),²

$$\text{Interval I } (i = 1): \quad 0 < t \leq T_\varphi \quad \rightarrow \quad \Delta t_1 = t, \quad (6.3)$$

$$\text{Interval II } (i = 2): \quad T_\varphi < t \leq T_S/2 \quad \rightarrow \quad \Delta t_2 = t - T_\varphi. \quad (6.4)$$

In steady-state operation, the system state vector $\vec{x}_{\text{st}}(t)$ (index ‘‘st’’ denotes steady-state) repeats cyclically every switching period. The steady-state values of $\vec{x}_{\text{st}}(t)$ are obtained from

$$\vec{x}_{\text{st}} \left(t + \frac{T_S}{2} \right) = \begin{bmatrix} -1 & \mathbf{0} \\ \mathbf{0} & \mathbf{I} \end{bmatrix} \cdot \vec{x}_{\text{st}}(t) = \mathbf{R} \cdot \vec{x}_{\text{st}}(t), \quad (6.5)$$

since the DAB inductor current $i_L(t)$ changes its sign every half-cycle in steady-state [120], whereas the signs of the filter inductor currents and capacitor voltages remain the same after one half-cycle. In order to solve for $\vec{x}_{\text{st}}(t)$ in (6.5), the time domain expressions for $\vec{x}(t + T_S/2)$ are required as a function of $\vec{x}(t)$. The derivation of these expressions is described based on the switching sequence shown in Figure 3.4 and starts with the unknown values in $\vec{x}(t = 0)$. With (6.2), (6.3), and $i = 1$, the general expression for $\vec{x}(t)$ at $t = T_\varphi$ is equal to

$$\vec{x}(T_\varphi) = \vec{f}_{\text{PS},1}(\vec{x}_0, T_\varphi) \quad \text{with} \quad \vec{x}_0 = \vec{x}(0). \quad (6.6)$$

²The derivation of the time domain expressions in $\vec{f}_{\text{PS},i}(\vec{x}_{i-1}, \Delta t_i)$ is associated with a considerable calculation effort and is preferably carried out with a mathematical software tool that allows for symbolic evaluation (e.g. Mathematica, Maple).

At $t = T_\varphi$ the switches T_6, T_7 are turned off, T_5, T_8 are turned on, and time interval II starts. Since capacitor voltages as well as inductor currents cannot change instantaneously, the initial conditions of time interval II are equal to the final state variable values of time interval I, $\vec{x}_1 = \vec{x}(T_\varphi)$. With the time domain expressions for all state variables during time interval II the state vector at the end of the half-cycle (cf. Figure 3.4) becomes

$$\vec{x}(T_S/2) = \vec{f}_{\text{PS},2}(\vec{x}_1, T_S/2 - T_\varphi) = \vec{f}_{\text{PS},2}\left[\vec{f}_{\text{PS},1}(\vec{x}_0, T_\varphi), T_S/2 - T_\varphi\right]. \quad (6.7)$$

The steady-state values are then obtained from the equation system (6.5) with (6.7), $\vec{x}_{\text{st}}(t) = \vec{x}(t)$, and $t = 0$.

Besides for the calculation of the steady-state, (6.7) forms the basis for the derivation of the discrete-time small-signal model with sampling time

$$T_{\text{DAB}} = T_S/2 = 5 \mu\text{s}. \quad (6.8)$$

The proposed model considers small-signal deviations, $\hat{\vec{x}}(t)$, of the system state variables $\vec{x}(t)$ from the steady-state $\vec{x}_{\text{st}}(t)$,

$$\hat{\vec{x}}(t) = \vec{x}(t) - \vec{x}_{\text{st}}(t) \quad (6.9)$$

(the symbol “ $\hat{\cdot}$ ” denotes small-signal variables), by reason of three different kinds of excitations:

- variations of the state variables due to prior excitations of input variables: $\hat{\vec{x}}_0 = \hat{\vec{x}}(0) = \vec{x}(0) - \vec{x}_{\text{st}}(0)$,
- HV and LV voltage changes: $\hat{\vec{v}}_{\text{g},0} = [\hat{V}_1(0) \ n \hat{V}_2(0)]^T$,
- excitation of the control input: $\hat{c}_{\text{PS},0} = \hat{T}_\varphi(0)$.

It is important to note, that the proposed discrete-time model considers an excitation of any of these variables exactly at the beginning of the half-cycle and calculates the respective values of the system state variables at the end of the half-cycle (Figure 6.3). Consequently, all changes of the input variables $\hat{\vec{v}}_{\text{g}}(t)$ and $\hat{c}_{\text{PS}}(t)$ that occur for $0 < t \leq T_{\text{DAB}}$ are not at all considered in $\hat{\vec{x}}(T_{\text{DAB}})$. This limitation only regards transfer functions with continuous-time input signals such as $V_1(t), V_2(t)$. It does not affect the control-to-output transfer function in a digitally controlled system, provided that the digital controller is synchronized to the power electronics, i.e. $T_\varphi(t)$ changes exactly at $t = k \cdot T_{\text{DAB}}, k \in \mathbb{N}_0$.

The small-signal deviations $\hat{\vec{x}}(T_{\text{DAB}})$ at the end of the half-cycle are then obtained from a linear approximation [120],

$$\hat{\vec{x}}(T_{\text{DAB}}) \approx \mathbf{A} \cdot \hat{\vec{x}}_0 + \mathbf{B}_{\text{PS}} \cdot \hat{c}_{\text{PS},0} + \mathbf{C} \cdot \hat{\vec{v}}_{\text{g},0}, \quad (6.10)$$

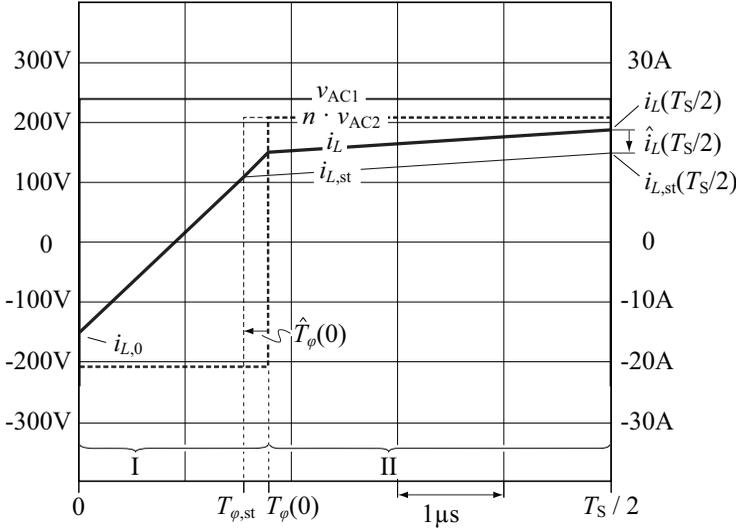


Figure 6.3: Reaction of the DAB to a phase shift excitation $\hat{T}_\varphi(0)$ (thick lines): at the end of the half-cycle, $t = T_S/2$, the inductor current deviation $\hat{i}_L(T_S/2)$ results. The thin lines depict steady-state operation according to Figure 3.4 (index “st” denotes steady-state). The digital control electronics determines $T_\varphi(0)$ at $t = 0$, which is applied during $0 < t < T_S/2$.

whereas the three terms $\mathbf{A} \cdot \hat{x}_0$, $\mathbf{B}_{\text{PS}} \cdot \hat{c}_{\text{PS},0}$, and $\mathbf{C} \cdot \hat{v}_{g,0}$ express the small-signal deviations of the state variables at $t = T_{\text{DAB}}$ as a result of excitations in \hat{x}_0 , $\hat{c}_{\text{PS},0}$, and $\hat{v}_{g,0}$, respectively. The expressions for \mathbf{A} , \mathbf{B}_{PS} , and \mathbf{C} are given in Appendix F.1.1.

Expression (6.10) allows for the derivation of the required small-signal transfer functions: according to [120] and Appendix F.1.2, the z-domain control-to-output transfer functions are calculated with

$$\mathbf{G}_{\text{PE,PS}} = \begin{bmatrix} G_{\text{PE,PS},I_{f1}} \\ G_{\text{PE,PS},V_{f1}} \\ G_{\text{PE,PS},V_{f2}} \end{bmatrix} = \mathbf{E}^T \cdot (z_{\text{DAB}}\mathbf{I} - \mathbf{Q}\mathbf{R}\mathbf{A}\mathbf{Q})^{-1} \cdot \mathbf{Q}\mathbf{R}\mathbf{B}_{\text{PS}}, \quad (6.11)$$

$$\mathbf{Q} = \begin{bmatrix} \text{sgn}(i_{L,0}) & \mathbf{0} \\ \mathbf{0} & \mathbf{I} \end{bmatrix}, \quad \mathbf{R} = \begin{bmatrix} -1 & \mathbf{0} \\ \mathbf{0} & \mathbf{I} \end{bmatrix}, \quad (6.12)$$

and $z_{\text{DAB}} = e^{sT_{\text{DAB}}}$. In order to collect the three control-to-output transfer functions with the output variables $I_{f1}(z_{\text{DAB}})$, $V_{f1}(z_{\text{DAB}})$, and $nV_{f2}(z_{\text{DAB}})$ in

one matrix $\mathbf{G}_{\text{PE,PS}}$,

$$\mathbf{G}_{\text{PE,PS}} = \begin{bmatrix} I_{\text{fla}}(z_{\text{DAB}}) + I_{\text{flb}}(z_{\text{DAB}}) & V_{\text{fl}}(z_{\text{DAB}}) & n V_{\text{f2}}(z_{\text{DAB}}) \\ T_{\varphi}(z_{\text{DAB}}) & T_{\varphi}(z_{\text{DAB}}) & T_{\varphi}(z_{\text{DAB}}) \end{bmatrix}^T, \quad (6.13)$$

the matrix \mathbf{E}^T in (6.11) becomes

$$\mathbf{E}^T = \begin{bmatrix} 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}. \quad (6.14)$$

The small-signal transfer functions in (6.11) have been verified for various operating points with results from a circuit simulator (e.g. the control-to-output transfer function $G_{\text{PE,PS},I_{\text{fl}}}$ in Figure 6.4). Simulated and calculated results show very good agreement for all investigated operating points.

6.1.2 DAB Power Stage, Alternative Modulation Schemes

If the DAB converter is operated with phase shift modulation within wide voltage ranges, its efficiency drops considerably for certain operating points (i.e. for $V_1/V_2 \ll n$ or $V_1/V_2 \gg n$). The average DAB converter efficiency substantially increases with the use of alternative modulation schemes (the index “alt” denotes all variables regarding alternative modulation schemes, cf. Chapter 3 and Chapter 5).

The derivations of the small-signal transfer functions for phase shift modulation and the alternative modulation schemes are very similar. However, phase shift modulation requires only one control input T_{φ} whereas three control inputs T_1 , T_2 , and T_3 are needed for the alternative modulation schemes.

Figure 5.4 depicts typical voltage and current waveforms for the DAB with the extended triangular current mode modulation. Again, one single half-cycle is segmented into the time intervals where no switching occurs:

$$\begin{aligned} \text{Interval I } (i = 1): & \quad 0 < t \leq T_1 & \rightarrow \Delta t_1 = t, \\ \text{Interval II } (i = 2): & \quad T_1 < t \leq T_1 + T_2 & \rightarrow \Delta t_2 = t - T_1, \\ \text{Interval III } (i = 3): & \quad T_1 + T_2 < t \leq T_1 + T_2 + T_3 \\ & \quad \rightarrow \Delta t_3 = t - (T_1 + T_2), \\ \text{Interval IV } (i = 4): & \quad T_1 + T_2 + T_3 < t \leq T_{\text{S}}/2 \\ & \quad \rightarrow \Delta t_4 = t - (T_1 + T_2 + T_3). \end{aligned}$$

This, together with (6.1) and the time domain expressions for all state variables within time interval i , $\vec{f}_{\text{alt},i}(\vec{x}_{i-1}, \Delta t_i)$ [cf. (6.2)], facilitates the derivation of the system state values at the end of the half-cycle (Figure 5.4),

$$\vec{x}(T_{\text{S}}/2) = \vec{f}_{\text{alt},4}(\vec{f}_{\text{alt},3}\{\vec{f}_{\text{alt},2}[\vec{f}_{\text{alt},1}(\vec{x}_0, T_1), T_2], T_3\}, T_4), \quad (6.15)$$

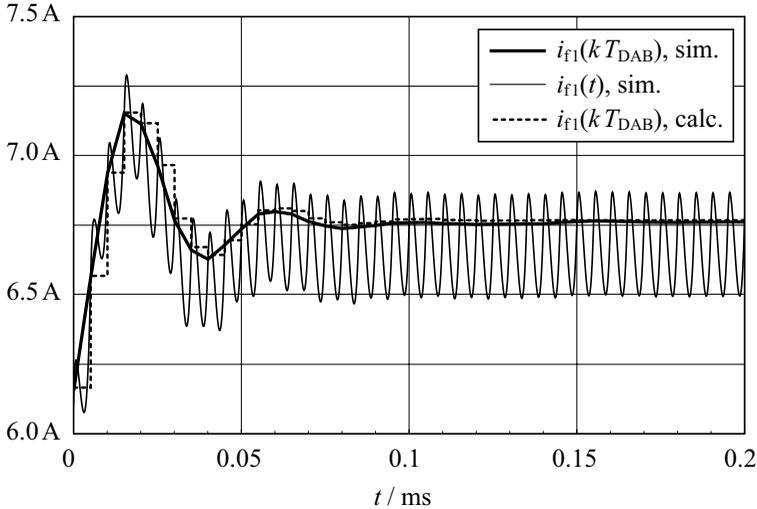


Figure 6.4: Simulated step response (solid lines) and calculated step response (dashed line) of $i_{f1}(t)$ for phase shift modulation, a time step, \hat{T}_φ , of 100 ns, nominal operating point, and power being transferred from the HV to the LV port. The circuit simulator generates a continuous-time waveform $i_{f1}(t)$ which is sampled after every half-cycle, $t = k \cdot T_{DAB}$, in order to facilitate the comparison to the step response obtained from the discrete-time small-signal transfer function $G_{PE,PS,I_{f1}}$. The solid line forms a linear connection of the sampled values of the simulated waveform $i_{f1}(t)$ to facilitate the comparison with the calculated values $i_{f1}(kT_{DAB})$ (dashed line). This solid line is thus different from the local average of $i_{f1}(t)$.

whereas $T_4 = T_S/2 - (T_1 + T_2 + T_3)$.

The solution to the equation system formed with (6.5) and (6.15) determines the steady-state values for $\vec{x}_{st}(t) = \vec{x}(t)$ at $t = 0$.

Equation (6.15) as well denotes the starting point for the small-signal transfer function derivation. In contrast to the phase shift modulation, the control input variable is now vector valued,

$$\hat{\vec{c}}_{alt,0} = [\hat{T}_1(0) \quad \hat{T}_2(0) \quad \hat{T}_3(0)]^T; \quad (6.16)$$

the small-signal vectors $\hat{\vec{x}}_0$ and $\hat{\vec{v}}_{g,0}$ remain unchanged. Consequently, the system states at the end of the half-cycle can be approximately calculated

with

$$\hat{x}(T_{\text{DAB}}) \approx \mathbf{A} \cdot \hat{x}_0 + \mathbf{B}_{\text{alt}} \cdot \hat{c}_{\text{alt},0} + \mathbf{C} \cdot \hat{v}_{g,0}. \quad (6.17)$$

(\mathbf{A} , \mathbf{B}_{alt} , and \mathbf{C} are derived in Appendix F.1.1). The control-to-output transfer functions are collected in the matrix

$$\mathbf{G}_{3 \times 3}^{\text{PE,alt}} = \begin{bmatrix} \vec{G}_{\text{PE,alt},1} & \vec{G}_{\text{PE,alt},2} & \vec{G}_{\text{PE,alt},3} \end{bmatrix}, \quad (6.18)$$

$$\vec{G}_{\text{PE,alt},i} = \begin{bmatrix} I_{\text{fla}}(z_{\text{DAB}}) + I_{\text{flb}}(z_{\text{DAB}}) & V_{\text{fl}}(z_{\text{DAB}}) & nV_{\text{f2}}(z_{\text{DAB}}) \\ T_i(z_{\text{DAB}}) & T_i(z_{\text{DAB}}) & T_i(z_{\text{DAB}}) \end{bmatrix}^{\text{T}},$$

($i = 1, 2, 3$) which is derived based on (6.17) with (6.12) and (6.14),

$$\mathbf{G}_{3 \times 3}^{\text{PE,alt}} = \mathbf{E}^{\text{T}} \cdot (z_{\text{DAB}}\mathbf{I} - \mathbf{QRAQ})^{-1} \cdot \mathbf{QRB}_{\text{alt}}. \quad (6.19)$$

The small-signal transfer functions in (6.18) have been verified with a circuit simulator. Very good agreement between simulation and calculation has been obtained for all investigated operating points [e.g. for nominal operation in Figure 6.5 and Figure 6.6 which show the step responses of the control-to-output transfer functions $G_{\text{PE,alt},1,I_{\text{fl}}}$ for the extended triangular current mode modulation and the suboptimal modulation, respectively, with input $T_1(z_{\text{DAB}})$ and output $I_{\text{fl}}(z_{\text{DAB}})$].

6.1.3 Modulator

The modulator calculates the control variables depending on the applied modulation scheme, the set current $i_{1,\text{mod}}$, and the measured values \bar{v}_{fl} and $n\bar{v}_{\text{f2}}$, obtained from v_{fl} and nv_{f2} . The modulator function for phase shift modulation,

$$c_{\text{PS}} = T_{\varphi} = f_{\text{mod,PS}}[i_{1,\text{mod}}(kT), \bar{v}_{\text{fl}}(kT), n\bar{v}_{\text{f2}}(kT)], \quad (6.20)$$

can be derived from (3.13) for a lossless DAB [the sampling time T is defined with (6.24), $k \in \mathbb{Z}$, and variables with lowercase letters denote time domain functions, e.g. $i_{1,\text{mod}}(kT)$ is equal to the sum of the steady-state DC component $I_{1,\text{mod,st}}$ and the small-signal disturbance $\mathcal{Z}^{-1}\{I_{1,\text{mod}}(z)\}$: $i_{1,\text{mod}}(kT) = I_{1,\text{mod,st}} + \mathcal{Z}^{-1}\{I_{1,\text{mod}}(z)\}$]. The expressions for the alternative modulation schemes,

$$\vec{c}_{\text{alt}} = (T_1 \ T_2 \ T_3)^{\text{T}} = \vec{f}_{\text{mod,alt}}[i_{1,\text{mod}}(kT), \bar{v}_{\text{fl}}(kT), n\bar{v}_{\text{f2}}(kT)] \quad (6.21)$$

are rather complicated, hence their evaluation in the DSP is avoided. Instead, precalculated values stored in DSP memory tables are used together with the fast linear interpolation algorithm presented in Appendix E.2. Since the

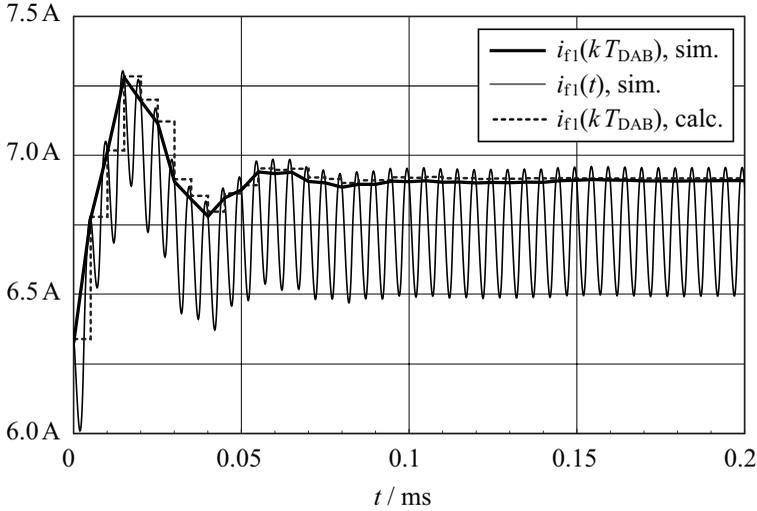


Figure 6.5: Simulated step response (solid lines) and calculated step response (dashed line) of $i_{f1}(t)$ for the extended triangular current mode modulation if a time step $\hat{T}_1 = 100 \text{ ns} \cdot \sigma(t)$ is applied and $\hat{T}_2 = \hat{T}_3 = 0$, at nominal operation, and for power being transferred from the HV to the LV port. The continuous-time waveform $i_{f1}(t)$ is again sampled after every half-cycle in order to facilitate the comparison to the step response obtained from the discrete-time small-signal model. The solid line forms a linear connection of the sampled values of the simulated waveform $i_{f1}(t)$ to facilitate the comparison with the calculated values $i_{f1}(kT_{\text{DAB}})$ (dashed line). This solid line is thus different from the local average of $i_{f1}(t)$.

modulator function is static, the small-signal transfer function is simply determined with the respective derivatives at the operating point. Thus, the transfer functions for phase shift modulation are

$$\mathbf{G}_{1 \times 3}^{\text{mod,PS}} = \begin{bmatrix} \frac{\partial f_{\text{mod,PS}}}{\partial i_{1,\text{mod}}} & \frac{\partial f_{\text{mod,PS}}}{\partial \bar{v}_{f1}} & \frac{\partial f_{\text{mod,PS}}}{\partial (n \bar{v}_{f2})} \end{bmatrix}, \quad (6.22)$$

and for the alternative modulation schemes

$$\mathbf{G}_{3 \times 3}^{\text{mod,alt}} = \begin{bmatrix} \frac{\partial \vec{f}_{\text{mod,alt}}}{\partial i_{1,\text{mod}}} & \frac{\partial \vec{f}_{\text{mod,alt}}}{\partial \bar{v}_{f1}} & \frac{\partial \vec{f}_{\text{mod,alt}}}{\partial (n \bar{v}_{f2})} \end{bmatrix}. \quad (6.23)$$

$\mathbf{G}_{\text{mod,PS}}$ and $\mathbf{G}_{\text{mod,alt}}$ are evaluated at the operating point with the steady-state values of $i_{1,\text{mod}}$, \bar{v}_{f1} , and \bar{v}_{f2} .

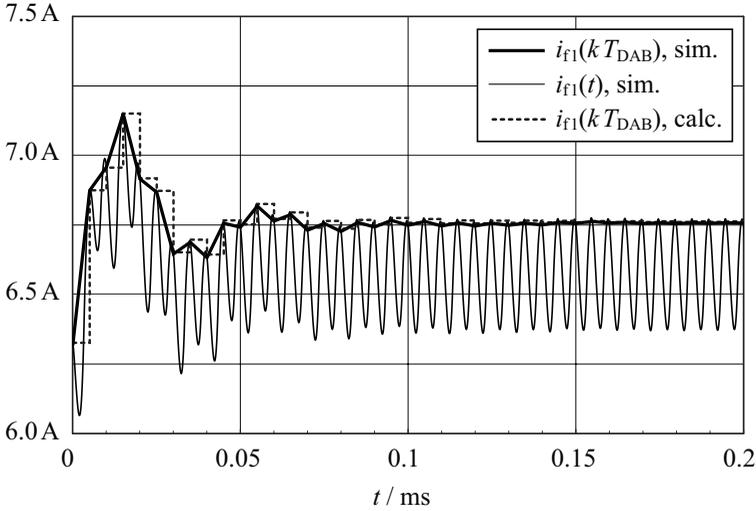


Figure 6.6: Simulated step response (solid lines) and calculated step response (dashed line) of $i_{f1}(t)$ for the suboptimal modulation if a time step $\hat{T}_1 = 100 \text{ ns} \cdot \sigma(t)$ is applied and $\hat{T}_2 = \hat{T}_3 = 0$, at nominal operation, and for power being transferred from the HV to the LV port. The continuous-time waveform $i_{f1}(t)$ is again sampled after every half-cycle in order to facilitate the comparison to the step response obtained from the discrete-time small-signal model. The solid line forms a linear connection of the sampled values of the simulated waveform $i_{f1}(t)$ to facilitate the comparison with the calculated values $i_{f1}(kT_{DAB})$ (dashed line). This solid line is thus different from the local average of $i_{f1}(t)$.

6.2 DAB Digital Control Loop

In the given laboratory setup, the average DAB output voltage is controlled (e.g. \overline{V}_{f2} in Figure 6.2 for power transfer from HV to LV). The proposed control loop consists of an inner loop with a PI-controller $G_{C,I}$ that controls $\overline{I}_{f1}(z)$ and an outer loop with another PI-controller $G_{C,V}$, which controls the output voltage. Depending on the power transfer direction, the average output voltage can be either $\overline{V}_{f2}(z)$ for power transfer from the HV port to the LV port or $\overline{V}_{f1}(z)$ for the opposite direction.

According to Figure 6.2, the current controller $G_{C,I}$ outputs $I_{1,\text{mod}}(z)$ and connects to the modulator \mathbf{G}_{mod} . The modulator then calculates the DAB timing parameters in order to achieve the required power transfer. Since the current controller solely operates on the difference between $\overline{I}_{f1}(z)$ and $I_{1,\text{ref}}(z)$,

G_{DAB} is a single input, single output transfer function with set current input $I_{1,\text{mod}}(z)$ and HV side current output $\bar{I}_{\text{fl}}(z)$. However, there is internal feedback in the transfer function G_{DAB} , since $\bar{V}_{\text{fl}}(z)$ and $n\bar{V}_{\text{f2}}(z)$ are required for the modulator; this must be considered in order to determine G_{DAB} .

Except for the DAB small-signal transfer function matrix \mathbf{G}_{PE} (equal to $\mathbf{G}_{\text{PE,PS}}$ or $\mathbf{G}_{\text{PE,alt}}$), all transfer functions in Figure 6.2 are part of the digital system and either reside in the DSP or in the FPGA. Relatively simple z-domain transfer functions result for the modulator \mathbf{G}_{mod} (Section 6.1.3), the time delays $\mathbf{G}_{\text{Td,DSP}}$, $\mathbf{G}_{\text{Td,FPGA}}$, and $\mathbf{G}_{\text{Td,meas}}$, the moving average filters $\mathbf{H}_{\text{filter}}$ and H_{avg} as well as for the controllers $G_{\text{C,V}}$ and $G_{\text{C,I}}$. This section focuses on these transfer functions in order to complete the derivation of G_{DAB} . The obtained transfer function is finally compared to a transfer function based on a simplified DAB model that allows for a significantly reduced calculation effort.

6.2.1 System Sampling Rate

The small-signal model of the power stage results in a z-domain transfer function with sampling time T_{DAB} [cf. (6.8)]. Due to the required DSP calculation time, the DAB timing parameters are only updated every $10T_{\text{DAB}}$, therefore the DSP sampling time is

$$T = 10T_{\text{DAB}} = 50 \mu\text{s}, \quad z = e^{sT}. \quad (6.24)$$

Hence, all transfer functions with faster update rate, such as \mathbf{G}_{PE} and voltage and current measurements (Figure 6.2), need to be resampled (e.g. with the method outlined in Appendix F.2).

6.2.2 Time Delays

The implemented software acquires three measurements during one calculation period T in order to achieve higher noise immunity. The resulting time delay in $\mathbf{G}_{\text{Td,meas}}$ is $10T_{\text{DAB}}$ for the first measurement, $8T_{\text{DAB}}$ for the second and $6T_{\text{DAB}}$ for the third measurement. The FPGA ($\mathbf{G}_{\text{Td,FPGA}}$) causes an additional time delay of $2T_{\text{DAB}}$ in order to apply the new timing values to the power electronics. FPGA and measurement time delays sum up to a total time delay of $12T_{\text{DAB}}$ for the first measurement, and $10T_{\text{DAB}}$ and $8T_{\text{DAB}}$ for the two subsequent measurements. The DSP calculates the average of the three measured values and

$$\mathbf{G}_{\text{PE,measure}}(z_{\text{DAB}}) = \frac{z_{\text{DAB}}^{-12} + z_{\text{DAB}}^{-10} + z_{\text{DAB}}^{-8}}{3} \cdot \mathbf{G}_{\text{PE}}(z_{\text{DAB}}) \quad (6.25)$$

results for that part of G_{DAB} which is updated with the higher sampling rate T_{DAB} (Figure 6.2). The sampling rate of this transfer function finally needs

to be converted to the system sampling rate T (cf. Appendix F.2),

$$\mathbf{G}_{\text{PE,measure}}(z_{\text{DAB}}) \xrightarrow{\text{resample}} \mathbf{G}_{\text{r,PE,measure}}(z). \quad (6.26)$$

The DSP causes another time delay of T in order to carry out all calculations, therefore

$$G_{\text{Td,DSP,PS}}(z) = z^{-1}, \quad (6.27)$$

$$\mathbf{G}_{\text{Td,DSP,alt}}(z) = \text{diag}(z^{-1}, z^{-1}, z^{-1}), \quad (6.28)$$

for phase shift or alternative modulation, respectively.

6.2.3 Moving Average Filters

The z-domain transfer function of the implemented N -th order moving average filter,

$$H_{\text{avg}}(z) = \frac{1}{N} \sum_{i=0}^{N-1} z^{-i}, \quad (6.29)$$

calculates the average over N previously measured values $x(0)$, $x(T) \dots x[(N-1) \cdot T]$; the present software implementation uses $N = 5$. The moving average filter is applied to $I_{\text{fl}}(z)$, $V_{\text{fl}}(z)$, and $nV_{\text{f2}}(z)$. The filter regarding I_{fl} is included in G_{DAB} (Section 6.2.4), and the feedback transfer function $\mathbf{H}_{\text{filter}}$ contains the remaining two filter functions,

$$\mathbf{H}_{\text{filter}}(z) = \text{diag}(H_{\text{avg}}, H_{\text{avg}}). \quad (6.30)$$

6.2.4 DAB Control Plant G_{DAB}

The transfer function G_{DAB} is calculated according to Appendix F.3,

$$G_{\text{DAB}} = \bar{I}_{\text{fl}}/I_{1,\text{mod}} = H_{\text{avg}} [G_{00} + \mathbf{G}_{0\text{r}}\mathbf{H}(\mathbf{I} - \mathbf{G}_{\text{sr}}\mathbf{H})^{-1}\mathbf{G}_{\text{s0}}], \quad (6.31)$$

with G_{00} , $\mathbf{G}_{0\text{r}}$, \mathbf{G}_{sr} , and \mathbf{G}_{s0} summarized in the matrix \mathbf{G} ,

$$\mathbf{G} = \begin{bmatrix} G_{00} & \mathbf{G}_{0\text{r}} \\ \mathbf{G}_{\text{s0}} & \mathbf{G}_{\text{sr}} \end{bmatrix} \quad (6.32)$$

[cf. (F.13) in Appendix F.3]. According to Figure F.1 and Figure 6.2, \mathbf{G} and \mathbf{H} become

$$\begin{aligned} \mathbf{G} &= \mathbf{G}_{\text{r,PE,measure,PS}} \cdot G_{\text{Td,DSP,PS}} \cdot \mathbf{G}_{\text{mod,PS}}, \\ \mathbf{H} &= \mathbf{H}_{\text{filter}} \end{aligned} \quad (6.33)$$

for phase shift modulation and

$$\begin{aligned} \mathbf{G} &= \mathbf{G}_{\text{r,PE,measure,alt}} \cdot G_{\text{Td,DSP,alt}} \cdot \mathbf{G}_{\text{mod,alt}}, \\ \mathbf{H} &= \mathbf{H}_{\text{filter}} \end{aligned} \quad (6.34)$$

if the alternative modulation is employed.

6.2.5 Experimental Verification

The control-to-output transfer function $I_{f1}/I_{1,\text{mod}}$ (cf. Figure 6.2) is measured using a sinusoidal current sequence superimposed on the steady-state modulator current value $I_{1,\text{mod,st}}$ (Figure 6.7 and Figure 6.8). The proposed measurement sequence consists of three different time intervals (Figure 6.7):

- *Time interval I* is used to settle the desired converter operating point. Therefore, controlled converter operation is needed during time interval I.
- At the beginning of *time interval II*, the steady-state value $I_{1,\text{mod,st}}$ is stored in the DSP and thereafter, current and voltage controllers are turned off. Hence, the converter is operated in open loop during time interval II. The stored value $I_{1,\text{mod,st}}$ and a superimposed sinusoidal time series $\mathcal{Z}^{-1}\{I_{1,\text{mod}}(z)\}$, calculated in the DSP, with a given amplitude and the desired excitation frequency are used to generate a sinusoidal current excitation around the steady-state operating point. The DSP measures the current i_{f1} which results in the time series $\bar{I}_{f1,\text{st}} + \mathcal{Z}^{-1}\{I_{f1}(z)\}$. During time interval II, however, the DSP discards the measured current values in order to eliminate transient effects.
- During *time interval III*, the DSP continues to generate the DC shifted sinusoidal time series (Figure 6.7 and Figure 6.8) and stores the generated modulator current values $I_{1,\text{mod,st}} + \mathcal{Z}^{-1}\{I_{1,\text{mod}}(z)\}$ and the measured current values $\bar{I}_{f1,\text{st}} + \mathcal{Z}^{-1}\{I_{f1}(z)\}$ in an on-chip table; the measurement sequence completes after time interval III has elapsed. In a post processing pass, the tabulated current values are refined with a FIR filter in order to suppress noise and to accurately obtain gain and phase of the control-to-output transfer function at the employed excitation frequency. The outlined procedure is repeated for each data point depicted in Figure 6.9, Figure 6.10, and Figure 6.11.

The results obtained for phase shift modulation (Figure 6.9), and for the extended triangular current mode modulation scheme (Figure 6.10) show a good matching between calculated and measured transfer functions. A noticeable difference between measured and calculated gain response is observed for the suboptimal modulation scheme (Figure 6.11). This error is attributed to the instantaneous inductor currents $i_L(t_1)$ and $i_L(t_2)$ being close to zero [cf. Figures 5.23 (a) and (b) and Figure 5.29]: there, the characteristics of the delay of the LV switches is highly non-linear (Figure 4.26). For all depicted results and for frequencies below 7 kHz, a maximum gain difference of less than ± 1.5 dB is achieved; the phase differences are smaller than $\pm 10^\circ$.

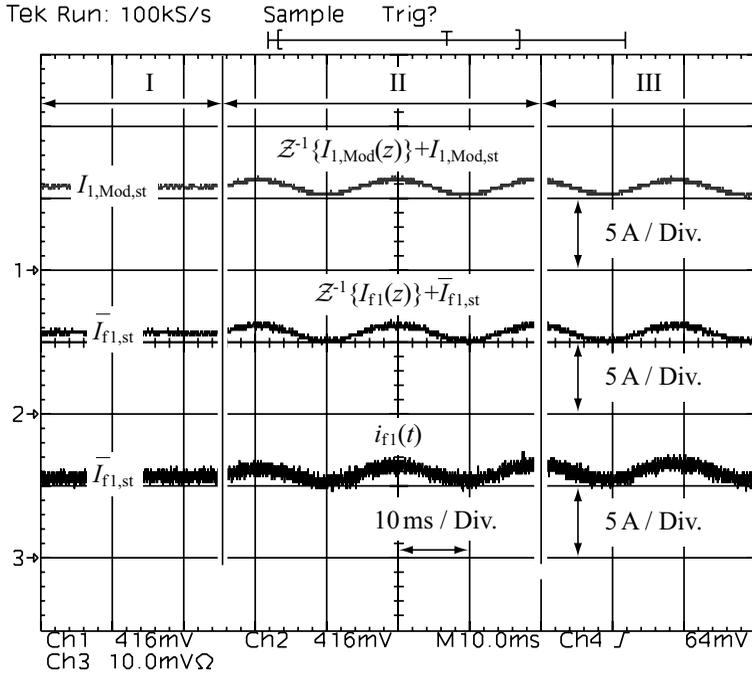


Figure 6.7: Current waveforms for the proposed measurement of the control-to-output transfer functions: during time interval I, the converter settles the desired operating point, time interval II is used to avoid transient effects, and during time interval III gain and phase are measured (cf. Figure 6.8). The converter is voltage and current controlled during time interval I and is operated in open loop during time intervals II and III with a sinusoidal waveform $\mathcal{Z}^{-1}\{I_{1,mod}(z)\}$ being superimposed on $I_{1,mod,st}$. The depicted example employs an excitation amplitude of 500 mA at a frequency of 51 Hz and has been measured on a previous setup of the DAB with $L = 31 \mu\text{H}$ and $n = 24$; $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, $P_2 = 2 \text{ kW}$, phase shift modulation. The waveform $i_{f1}(t)$ is measured with an analog current probe in order to allow for a comparison between digital and analog signals. Time interval III is not fully depicted; its duration is equal to 50 ms.

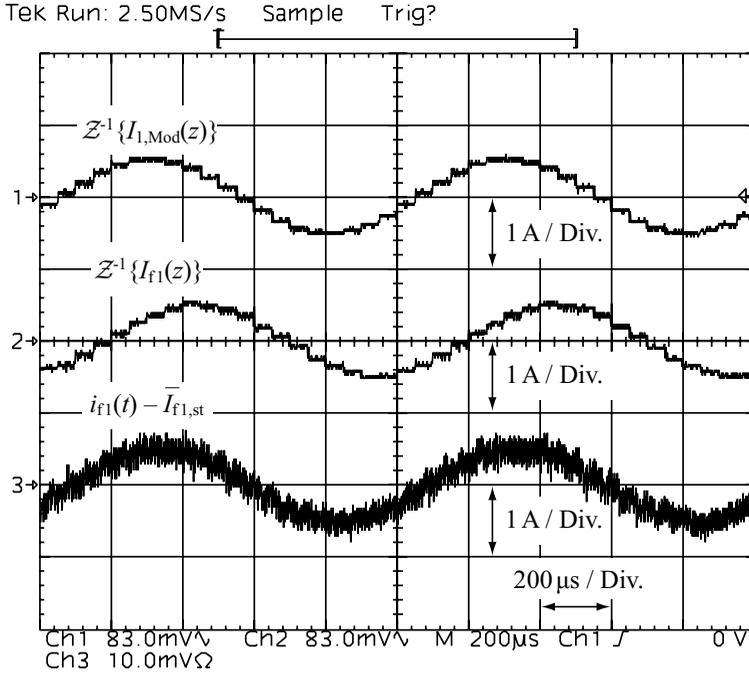


Figure 6.8: Measurement method employed to determine the DAB transfer function: during time interval III (cf. Figure 6.7), amplitude and phase of the generated sinusoidal time series $\mathcal{Z}^{-1}\{I_{1,mod}(z)\}$ are compared to amplitude and phase of the measured time series $\mathcal{Z}^{-1}\{I_{f1}(z)\}$ in order to obtain gain and phase shift for one frequency of the control-to-output transfer function (for this, only AC components are regarded – the DC components $I_{1,mod,st}$ and $\bar{I}_{f1,st}$ are not considered). The depicted example employs an excitation amplitude of 500 mA at a frequency of 1 kHz and nominal converter operation. The waveform $i_{f1}(t)$ is measured with an analog current probe in order to allow for a comparison between digital and analog signals.

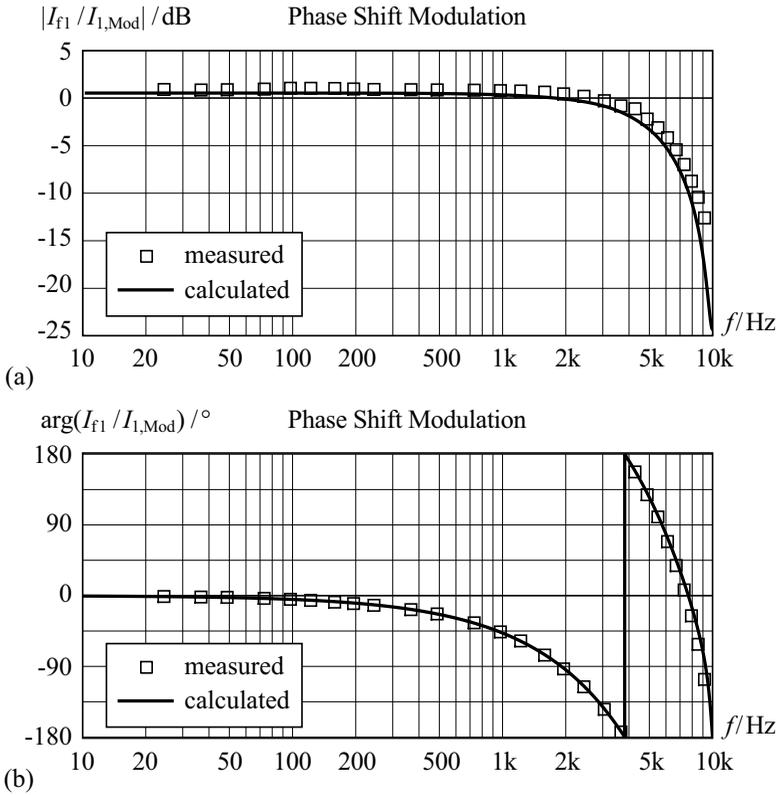


Figure 6.9: Calculated and measured DAB frequency response for phase shift operation [(a) gain and (b) phase]; the Nyquist frequency $1/(2T) = 10 \text{ kHz}$ limits the maximum possible frequency; the solid line denotes the calculated frequency response and the boxes mark the measured values. The DAB is operated with $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, and with a reduced output power $P_2 = 1.5 \text{ kW}$ [at $P_2 = 2 \text{ kW}$, the inductor current $i_L(T_\varphi)$ is approximately zero (Figure 3.4) and, consequently, the time delays of the LV side switches become highly dependent on the actual current $i_L(T_\varphi)$ (Figure 4.26); even though, these time delays are considered in the employed modulator function, a reduced gain has been measured for phase shift modulation at $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, and $P_2 = 2 \text{ kW}$; the effect of these time delays is detailed in [122]].

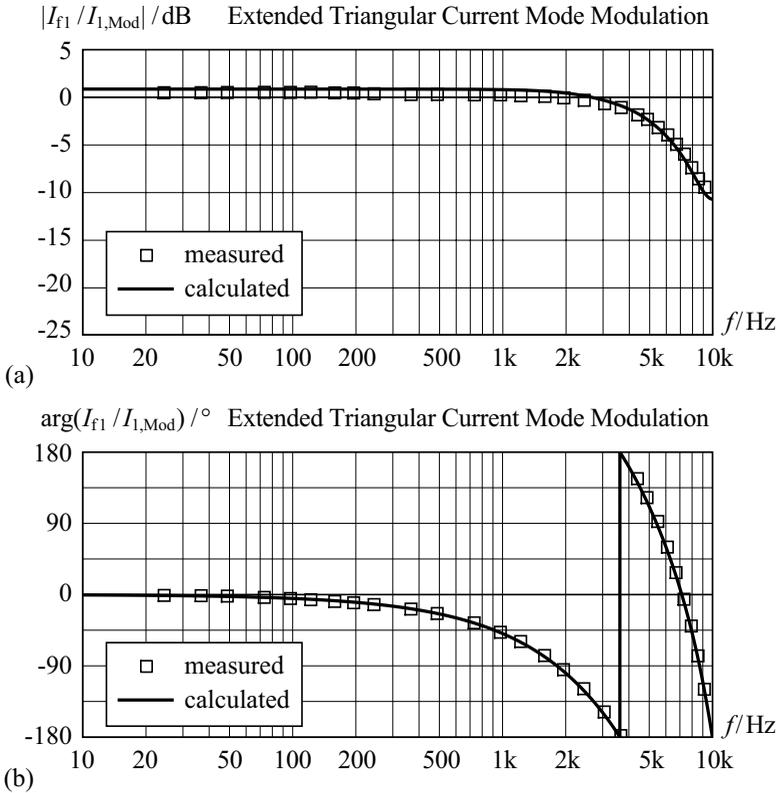


Figure 6.10: Calculated and measured DAB frequency response for the extended triangular current mode modulation [(a) gain and (b) phase]; the Nyquist frequency $1/(2T) = 10 \text{ kHz}$ limits the maximum possible frequency; the solid line denotes the calculated frequency response and the boxes mark the measured values. The DAB is operated with $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, and with 2 kW output power at the LV port.

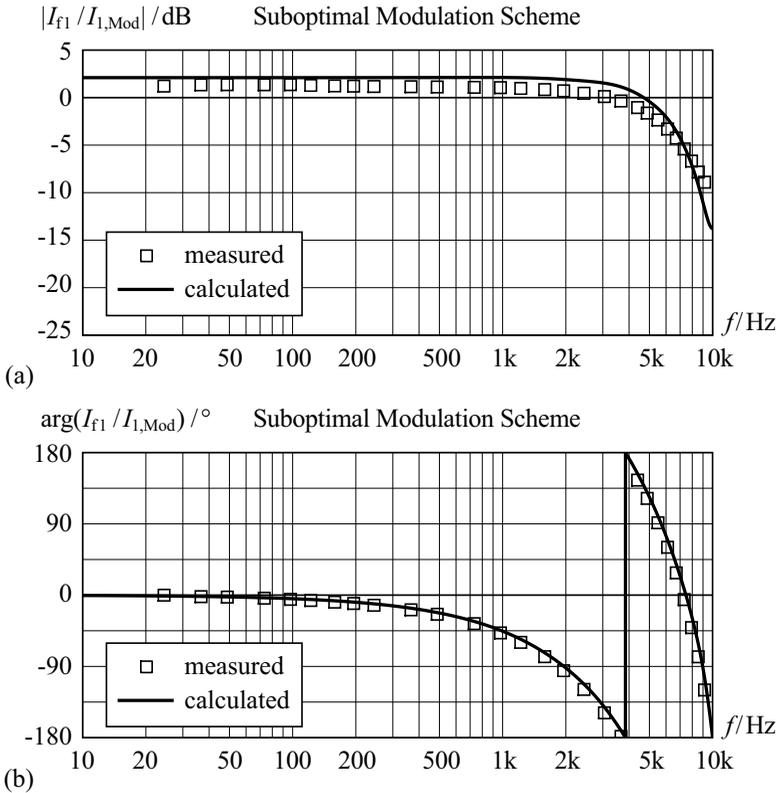


Figure 6.11: Calculated and measured DAB frequency response [(a) gain and (b) phase] for the suboptimal modulation scheme depicted in Figures 5.29; the Nyquist frequency $1/(2T) = 10 \text{ kHz}$ limits the maximum possible frequency; the solid line denotes the calculated frequency response and the boxes mark the measured values. The DAB is operated with $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, and with 2 kW output power at the LV port.

The error between measured and calculated frequency response is attributed to instantaneous inductor currents $i_L(t_1)$ and $i_L(t_2)$ close to zero [cf. Figures 5.23 (a) and (b) and Figure 5.29]. There, the characteristics of the delay of the LV switches is highly non-linear (Figure 4.26). Still, for frequencies below 8 kHz, the maximum absolute gain error is less than 1.5 dB and the relative gain error is less than 20%.

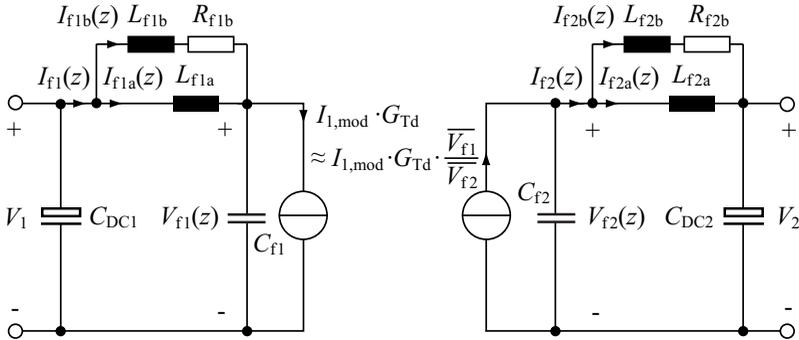


Figure 6.12: Simplified circuit of the DAB: the two current sources replace the switches, the inductor L , and the transformer. For a lossless DAB, the accurate current for the source on the right hand side would be equal to $\mathcal{Z}\{i_{1,\text{mod}}(kT) \cdot v_{f1}(kT)/v_{f2}(kT)\} \cdot G_{\text{Td}}$ which is approximately equal to $I_{1,\text{mod}}(z) \cdot G_{\text{Td}} \cdot \bar{V}_{f1}/\bar{V}_{f2}$. On the assumption of a constant transfer ratio $\bar{V}_{f1}/\bar{V}_{f2}$, the simplified circuit can be analyzed by means of Laplace- or Z-transform.

6.2.6 Derivation of a Simplified G_{DAB}

In the presented system, all time constants of the EMI filters are significantly smaller than the time delay caused by the digital controller. The question may now arise, whether a simple DAB converter model which neglects the couplings between the input filter, the output filter, and the DAB power stage itself would be sufficiently accurate in order to design current and voltage controllers. For steady-state operation, the employed modulator functions $\mathbf{G}_{\text{mod,PS}}$ or $\mathbf{G}_{\text{mod,alt}}$ already generate almost correct timing parameters, i.e. $I_{f1} \approx I_{1,\text{mod}}$ and $I_{f2} \approx I_{1,\text{mod}} \cdot \bar{V}_{f1}/\bar{V}_{f2}$. Additionally, the total time delay G_{Td} (DSP, FPGA, and measurement) needs to be regarded according to (6.25), (6.27), and (6.28). Thus, the DAB converter in Figure 6.1 may be replaced with the two current sources depicted in Figure 6.12 (cf. [96]).

In Figure 6.13, the frequency response of G_{DAB} (phase shift modulation, nominal operation) is compared to the frequency response of the simplified transfer function $G_{\text{DAB,simp}}$ derived from the circuit depicted in Figure 6.12. The frequency response obtained from the simplified model differs only slightly from the accurate model which is mainly due to the linearization achieved with the modulator table (regarding the gain response) and due to the digital controller's time delays (regarding the phase response).

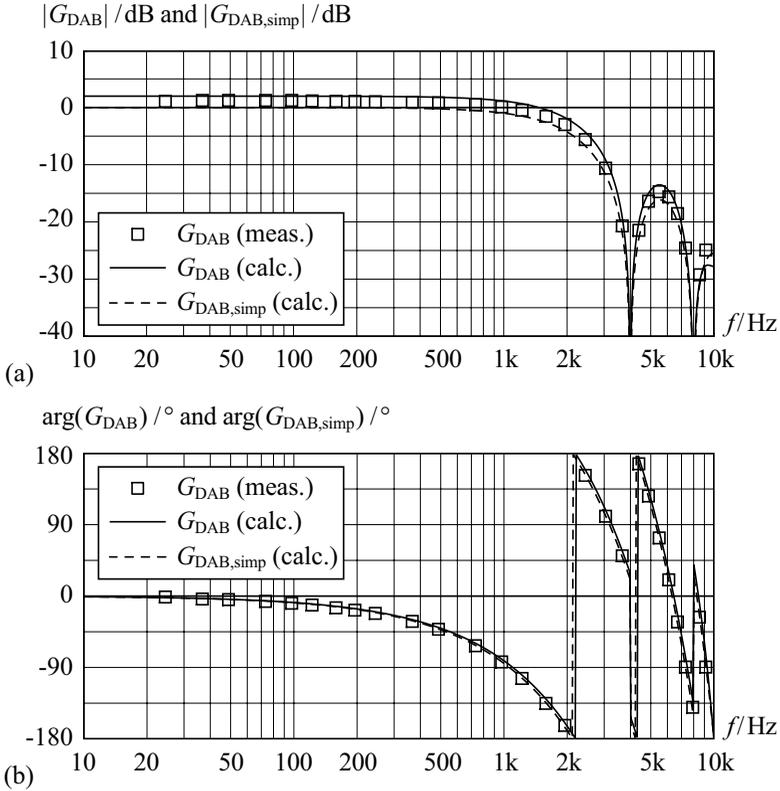


Figure 6.13: Frequency response of the detailed transfer function G_{DAB} (solid lines) and the simplified transfer function $G_{DAB,simp}$ (dashed lines); (a) gain and (b) phase diagrams for $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, $P_2 = 2 \text{ kW}$, suboptimal modulation; the boxes mark measured values.

6.3 Current and Voltage Controllers

Due to the large capacitance values of C_{DC1} and C_{DC2} , constant input and output voltages V_1 and V_2 are assumed for the design of the current controller. Furthermore, according to the considerations discussed in Section 6.2.6, the transfer function G_{DAB} is regarded to be independent of the actual operating point.

The proposed current controller (Figure 6.2) is a discrete-time PI con-

troller,³

$$G_{C,I} = K_{p,I} \frac{z - (1 - T/T_{i,I})}{z - 1} \quad (6.35)$$

with gain $K_{p,I}$ and cut-off frequency $\omega_{i,I} = 1/T_{i,I}$. Consequently, the open loop transfer function

$$F_{o,I} = G_{C,I} \cdot G_{DAB} \quad (6.36)$$

results. Due to the low pass behavior of G_{DAB} , the following design method is proposed in order to achieve a high bandwidth of the closed current loop transfer function:

1. Calculation of the controller cut-off frequency such that $|G_{DAB}|$ at $\omega_{i,I}$ is 3 dB lower than the DC gain, i.e. $|G_{DAB}(z_{i,I})| = |G_{DAB}(e^{j \cdot 0})|/\sqrt{2}$ with $z_{i,I} = e^{j\omega_{i,I}T}$.
2. The controller gain $K_{p,I}$ is determined in order to achieve a given phase margin Φ_R . First, the z-Parameter z_{Φ_R} where the open loop phase is equal to $-180^\circ + \Phi_R$ needs to be determined: $\arg(F_{o,I}(z_{\Phi_R})/K_{p,I}) = -180^\circ + \Phi_R$. With this, the controller gain $K_{p,I} = |1/F_{o,I}(z_{\Phi_R})|$ can be calculated.

With $\Phi_R = 60^\circ$, the controller parameters $K_{p,I} = 0.29$ and $T_{i,I} = 93 \mu\text{s}$ result for the given system setup. The calculated and the measured step response of the closed current control loop are depicted in Figure 6.14. Since the measured current signals are superimposed by noise, the average of 128 singular current step responses is shown; calculated and measured results match closely. The proposed current controller achieves the rise time $t_r \approx 250 \mu\text{s} = 5T$ and the delay time $t_d \approx 200 \mu\text{s} = 4T$ with a percentage overshoot of approximately 7% ($\Delta I_{f1,p} \approx 70 \text{ mA}$, $\hat{I}_{1,\text{ref}} = 1 \text{ A}$). For the given application, a rise time of less than $500 \mu\text{s}$ and a delay time of less than $500 \mu\text{s}$ are required, which has been achieved with the given controller design. If a faster response is required, the DSP time delays should be reduced (optimized algorithm, faster DSP), instead of using a smaller phase margin, to obtain an adequate control performance (fast response and small overshoot), since the time delays caused by the digital controller account for the main part of the presented converter's phase lag.

The direction of power transfer determines the voltage that needs to be controlled: this is V_1 for power transfer from the LV to the HV port, and V_2 for the opposite direction. However, V_1 and V_2 are not measured in the given system, only v_{f1} and v_{f2} are (Figure 6.1). Therefore, according to the direction of power transfer, either \bar{V}_{f1} or \bar{V}_{f2} is controlled and $V_1 \approx \bar{V}_{f1}$ as

³The transfer function of the digital PI controller is obtained from its continuous-time counterpart [123].

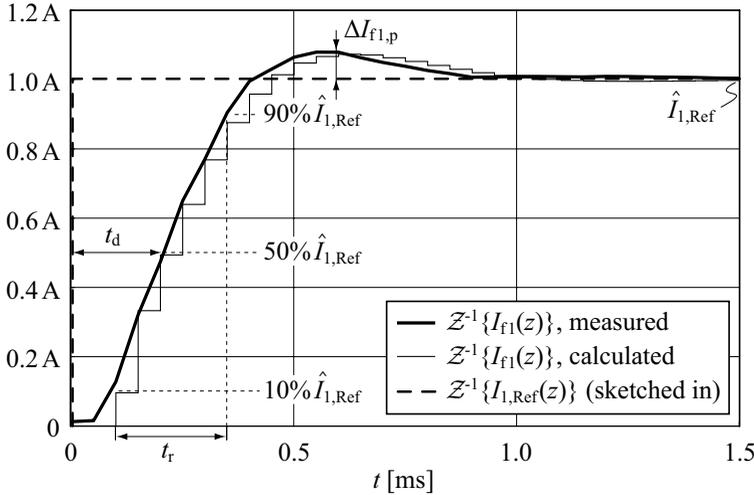


Figure 6.14: Measured and calculated unity step response of the closed current control loop; a rise time t_r of approximately $250 \mu\text{s}$ and a delay time t_d of approximately $200 \mu\text{s}$ are achieved.

well as $V_2 \approx \bar{V}_{f2}$ is assumed. For the voltage controller, again a PI controller with the transfer function

$$G_{C,V} = K_{P,V} \frac{z - (1 - T/T_{i,V})}{z - 1} \tag{6.37}$$

is employed. For power being transferred from the LV to the HV port, the controlled current I_{f1} flows into the output capacitor C_{DC1} and the load. The plant transfer function for the voltage controller ($\bar{V}_{f1}/I_{1,\text{ref}}$, cf. Figure 6.2) therefore consists of the closed current loop transfer function, the filter impedances L_{f1a} , L_{f1b} , R_{f1b} , and C_{DC1} (Figure 6.12) and the load connected to the HV port. If the direction of power transfer changes (HV to LV), then the current I_{f2} , which is not measured in the given system, flows into C_{DC2} and into the load connected to the LV port. However, I_{f2} can be approximated with $I_{f1} \cdot \bar{V}_{f1}/\bar{V}_{f2}$ for control purposes, since losses are rather low and the capacitance C_{DC2} is comparably large. The transfer function of the closed current loop again exhibits low-pass characteristics but the output capacitor adds an integration stage to the plant. For this type of plant, the symmetric optimum design method [124] is selected in order to design the voltage controller (in the case of a resistive load, the no-load operation is the worst case for the voltage controller design). A phase margin of $\Phi_R = 75^\circ$ leads to $K_{P,V} = 79.5 \text{ A/V}$ and $T_{i,I} = 24.7 \text{ ms}$.

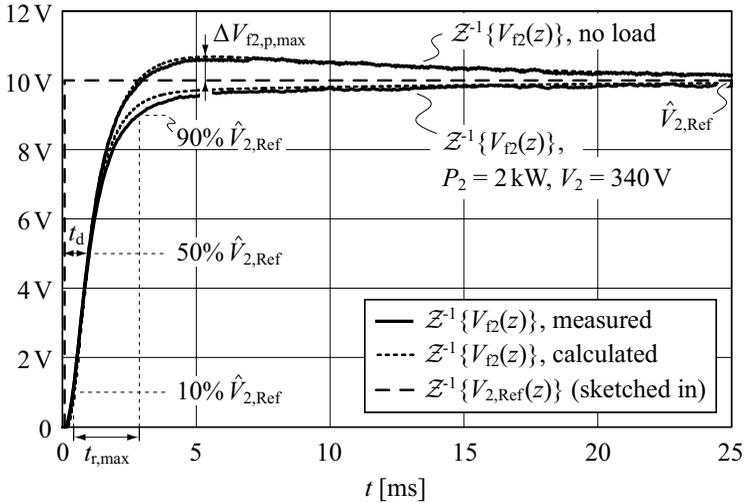


Figure 6.15: Step response of the closed voltage control loop for no-load operation and for 2 kW output power at 12 V output voltage; the input voltage is 340 V and the output voltage step amplitude is 250 mV.

In Figure 6.15, the measured and the calculated step responses of the voltage controlled system are shown for no load and for a load resistance of $72 \text{ m}\Omega = (12 \text{ V})^2 / 2 \text{ kW}$; again a good matching between measured and calculated results is achieved.

The proposed voltage controller achieves the rise time $t_r \approx 6.5 \text{ ms} = 130T$ and the delay time $t_d \approx 1.8 \text{ ms} = 36T$ with a maximum percentage overshoot of approximately 7% at no-load operation ($\Delta V_{f1,p,\max} \approx 18 \text{ mV}$, $\hat{V}_{1,\text{ref}} = 250 \text{ mV}$).

6.4 Conclusion

To develop an accurate small-signal model for a DAB converter, a precise knowledge of the modulation method is required and the EMI filters need to be included in order to consider their interactions with the DAB. However, simplified converter models may be used in order to facilitate a less laborious controller design, since the time delay of a digitally controlled system causes a significant phase lag, which is considerably larger than the power converter's phase lag.

In this Chapter, the small-signal models for the DAB including EMI filter are derived for different modulation schemes. Further, the structure of the digital control system (including the most relevant algorithms), a simplified DAB model and the controller design are detailed. The resulting control-to-output transfer functions are verified using measurements (obtained from an experimental setup) and a good matching between measured and calculated results is shown. Besides, in this Chapter, a measurement method to obtain the control-to-output transfer functions is proposed; this method may even be applied automatically in order to enable the autonomous calibration of the current and voltage controllers.

Chapter 7

Two-Stage Converter Realizations

7.1 Motivation, Investigated Converter Topologies

According to the results obtained in Chapter 3 and Chapter 5, the DAB converter efficiency considerably depends on the employed input and output voltages (cf. Figure 5.1). With the given DAB hardware prototype, the highest efficiency is achieved for V_1/V_2 close to the transformer turns ratio n . Thus, in order to effectively utilize the DAB converter, an additional DC–DC converter (without galvanic isolation) can be used to provide the required ratio V_1/V_2 . In order to limit the total system complexity, a simple buck-or-boost converter forms the additional converter stage (Figure 7.1: buck conversion

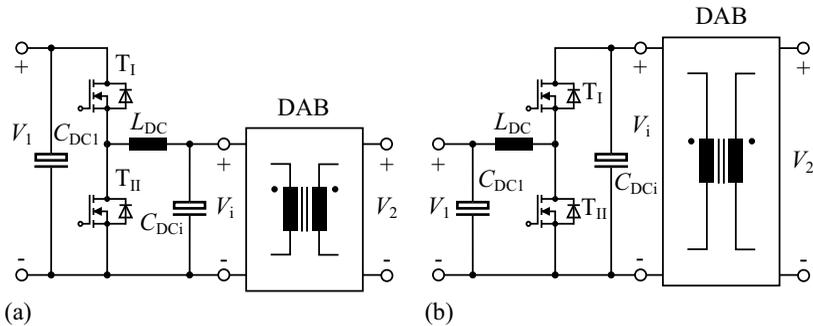


Figure 7.1: Investigated two-stage circuits: DAB converter and a HV side buck-or-boost converter (without galvanic isolation); (a) $V_i < V_1$, (b) $V_i > V_1$.

in one direction of power transfer, boost conversion for the opposite power transfer direction).

According to Chapter 2, 4 different circuit arrangements are possible. However, the presented investigation is limited to the two arrangements depicted in Figure 7.1; there, the additional DC–DC converter is placed on the HV side. With the additional DC–DC converter being placed on the HV side, considerably lower total losses are expected compared to an additional LV side DC–DC converter [Figures 2.22 (c) and (d); Section 2.2.2].

The topology shown in Figure 7.1 (a) proposes a DC link voltage $V_i < V_1$;¹ consequently, the HV side peak voltages of the DAB decrease and the respective HV side currents increase (switch currents, transformer current, and inductor current on the HV side of the DAB). For $V_i < V_1$, two different situations are investigated: constant $V_i = 225 \text{ V}$ (on the assumption of a maximum duty cycle of the buck-or-boost converter of

$$D_{b,\max} = D_{\text{buck},\max} = 1 - D_{\text{boost},\min} = 0.95, \quad (7.1)$$

cf. Appendix A.8) and variable V_i , $225 \text{ V} \cdot 11 \text{ V}/16 \text{ V} \approx 150 \text{ V} \leq V_i \leq 225 \text{ V}$. With constant V_i , the additional DC–DC converter generates lower losses and with variable V_i , the DAB is expected to operate at a higher efficiency.

The second investigated topology [Figure 7.1 (b)] employs $V_i > V_1$ to achieve lower currents on the HV side of the DAB. Again, constant and variable V_i are considered (Table 7.1). However, regarding a variable DC link voltage V_i , the exclusive DAB operation close to V_i/V_2 requires $475 \text{ V} \leq V_i \leq 475 \text{ V} \cdot 16 \text{ V}/11 \text{ V} \approx 700 \text{ V}$, which exceeds the drain-to-source breakdown voltage $V_{(\text{BR})\text{DSS}}$ of the employed MOSFETs ($V_{(\text{BR})\text{DSS}} = 600 \text{ V}$). In order to maintain the MOSFETs with $V_{(\text{BR})\text{DSS}} = 600 \text{ V}$,² the variable voltage range is reduced to $475 \text{ V} \cdot 11 \text{ V}/16 \text{ V} \approx 325 \text{ V} \leq V_i \leq 475 \text{ V}$. This selection enables highly efficient operation of the DAB for $V_1/D_{b,\max} < nV_2$ and prevents low DAB converter efficiency which would occur for $V_i/V_2 < n$ (e.g. $V_1 = 240 \text{ V}$ and $V_2 = 16 \text{ V}$ in Figure 5.1). Table 7.1 summarizes the voltage ranges employed for V_i .

7.2 Buck-or-Boost Converter Loss Model

In order to achieve a highly efficient and compact design of the additionally required buck-or-boost converter, the circuit depicted in Figure 7.2 is employed. There, the high side switch is composed of 3 power semiconductors: the MOSFET T_{I} , the Schottky diode $D_{\text{I},\text{s}}$, and the silicon-carbide diode D_{I} . Similarly, the low side switch is composed of the MOSFET T_{II} , the Schottky

¹The index “i” originates from intermediate link voltage [79].

²For $V_{(\text{BR})\text{DSS}} = 600 \text{ V}$, optimized MOSFETs with very low on-state resistances are available (Section D.1.2).

No.	Circuit Arrangement	Voltage Range Employed for V_i
1	Figure 7.1 (a), constant V_i	$V_i = 225 \text{ V}$
2	Figure 7.1 (a), variable V_i	$V_i = 225 \text{ V} \cdot \frac{V_2}{16 \text{ V}}$ $\Rightarrow 150 \text{ V} \leq V_i \leq 225 \text{ V}$
3	Figure 7.1 (b), constant V_i	$V_i = 475 \text{ V}$
4	Figure 7.1 (b), variable V_i	$V_i = \max\left(\frac{V_1}{D_{b,\max}}, 475 \text{ V} \cdot \frac{V_2}{16 \text{ V}}\right)$ $\Rightarrow 325 \text{ V} \leq V_i \leq 475 \text{ V}$

Table 7.1: Two-stage converters (Figure 7.1): investigated DC link voltage ranges.

diode $D_{II,s}$, and the silicon-carbide diode D_{II} (the silicon-carbide diodes eliminate reverse recovery effects and the Schottky diodes prevent the internal body diodes of the MOSFETs to conduct). With the proposed switches, low switching losses are achieved on the expense of increased conduction losses. Due to the use of MOSFETs and silicon-carbide diodes, a high switching frequency f_s of 100 kHz is selected in order to achieve both, low converter volume and low converter losses [125].

Depending on the employed mode of operation (i.e. buck or boost operation), either T_I , $D_{I,s}$, and D_{II} or T_{II} , $D_{II,s}$, and D_I are operated; thus, the resulting converter efficiency depends on the actual operating mode.

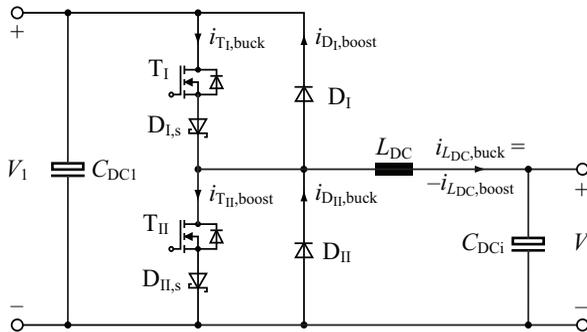


Figure 7.2: Circuit diagram of the employed buck-or-boost converter [annotation with respect to Figure 7.1 (a)].

7.2.1 Buck Operation

The average and the RMS values of the currents through T_I , $D_{I,s}$, D_{II} , and L_{DC} are required in order to calculate the converter losses. Since very low losses are expected for the considered buck-or-boost converter, the lossless converter model is considered to accurately predict these currents. Moreover, constant voltages V_I and V_i are considered.

The discussed model is used in the subsequent Section 7.3 to predict the expected converter efficiencies at medium and high output power (i.e. $P_{out} = 1$ kW and $P_{out} = 2$ kW). There, the buck-or-boost converters designed in Appendix A.8 are operated in continuous conduction mode (CCM, [116]); thus, in order to simplify the outlined analysis, only CCM operation is considered.

Figure 7.3 depicts the employed converter model, typical voltage and current waveforms for ($V_I = 340$ V, $V_i = 225$ V, and $P_{out} = 2$ kW), and the relative turn on time of T_I , i.e. the duty cycle D_{buck} .

Based on the above assumptions, the duty cycle D_{buck} is equal to

$$D_{buck} = \frac{V_i}{V_I} \quad (7.2)$$

during steady-state converter operation. The average inductor current is

$$\bar{I}_{L_{DC},buck} = \frac{P_{out,buck}}{V_i}, \quad (7.3)$$

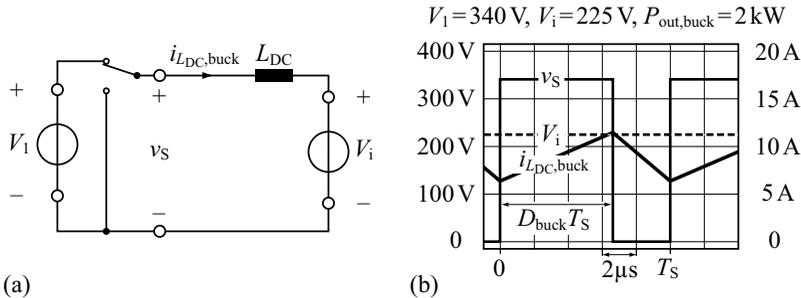


Figure 7.3: (a) Equivalent circuit diagram employed to calculate the currents through T_I , $D_{I,s}$, D_{II} , and L_{DC} during buck operation; (b) typical voltage and current waveforms during buck operation ($V_I = 340$ V, $V_i = 225$ V, $P_{out,buck} = 2$ kW, $L_{DC} = 150$ μ H, $f_s = 100$ kHz).

the peak-to-peak value of the inductor current ripple is

$$\Delta I_{L_{DC},\text{buck}} = \frac{V_i(1 - D_{\text{buck}})}{L_{DC}f_S}, \quad (7.4)$$

and the inductor RMS current is

$$I_{L_{DC},\text{buck}} = \sqrt{\bar{I}_{L_{DC},\text{buck}}^2 + \frac{\Delta I_{L_{DC},\text{buck}}^2}{12}}. \quad (7.5)$$

Consequently, the average switch current $\bar{I}_{T_{I},\text{buck}}$ and the switch RMS current $I_{T_{I},\text{buck}}$ are:

$$\bar{I}_{T_{I},\text{buck}} = D_{\text{buck}}\bar{I}_{L_{DC},\text{buck}}, \quad (7.6)$$

$$I_{T_{I},\text{buck}} = \sqrt{D_{\text{buck}}}\bar{I}_{L_{DC},\text{buck}}. \quad (7.7)$$

The current through the diode D_{II} causes the current stresses:

$$\bar{I}_{D_{II},\text{buck}} = (1 - D_{\text{buck}})\bar{I}_{L_{DC},\text{buck}}, \quad (7.8)$$

$$I_{D_{II},\text{buck}} = \sqrt{1 - D_{\text{buck}}}\bar{I}_{L_{DC},\text{buck}} \quad (7.9)$$

($\bar{I}_{D_{II},\text{buck}}$: average diode current; $I_{D_{II},\text{buck}}$: diode RMS current).

The discussed expressions are valid for the circuit depicted in Figure 7.1 (a); V_1 and V_i need to be interchanged in order to determine the currents of the buck-or-boost converter shown in Figure 7.1 (b).

7.2.2 Boost Operation

On the assumptions given in Section 7.2.1 (lossless buck-or-boost converter, constant voltages V_1 and V_i , CCM operation), $P_{\text{out},\text{buck}} = P_{\text{out},\text{boost}}$ applies; moreover, the relative turn-on time of T_{II} , D_{boost} , is equal to

$$D_{\text{boost}} = 1 - \frac{V_i}{V_1} = 1 - D_{\text{buck}} \quad (7.10)$$

during steady-state operation (Figure 7.4).

The inductor current for boost operation is thus equal to the inductor current for buck operation, i.e.:

$$\bar{I}_{L_{DC},\text{boost}} = \bar{I}_{L_{DC},\text{buck}}, \quad (7.11)$$

$$\Delta I_{L_{DC},\text{boost}} = \Delta I_{L_{DC},\text{buck}}, \quad (7.12)$$

$$I_{L_{DC},\text{boost}} = I_{L_{DC},\text{buck}}. \quad (7.13)$$

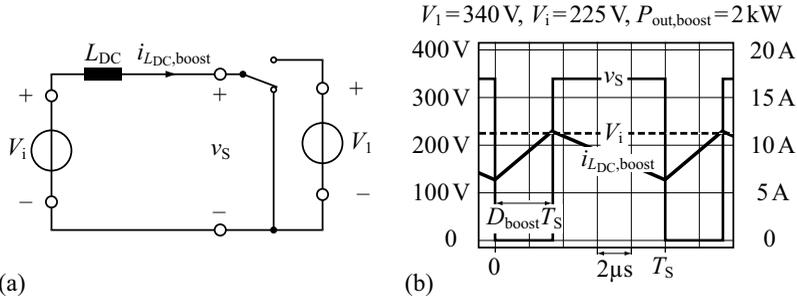


Figure 7.4: (a) Equivalent circuit diagram employed to calculate the currents through T_I , $D_{I,s}$, D_{II} , and L_{DC} during boost operation; (b) typical voltage and current waveforms during boost operation ($V_1 = 340\text{ V}$, $V_i = 225\text{ V}$, $P_{\text{out,boost}} = 2\text{ kW}$, $L_{DC} = 150\text{ }\mu\text{H}$, $f_S = 100\text{ kHz}$).

During boost operation, the switch and diode currents are:

$$\bar{I}_{T_{II},\text{boost}} = D_{\text{boost}} \bar{I}_{L_{DC},\text{boost}}, \quad (7.14)$$

$$I_{T_{II},\text{boost}} = \sqrt{D_{\text{boost}}} I_{L_{DC},\text{boost}}, \quad (7.15)$$

$$\bar{I}_{D_{I},\text{boost}} = (1 - D_{\text{boost}}) \bar{I}_{L_{DC},\text{boost}}, \quad (7.16)$$

$$I_{D_{I},\text{boost}} = \sqrt{1 - D_{\text{boost}}} I_{L_{DC},\text{boost}} \quad (7.17)$$

($\bar{I}_{T_{II},\text{boost}}$, $I_{T_{II},\text{boost}}$: average value and RMS value of $i_{T_{II},\text{boost}}(t)$, respectively; $\bar{I}_{D_{I},\text{boost}}$, $I_{D_{I},\text{boost}}$: average value and RMS value of $i_{D_{I},\text{boost}}(t)$, respectively).

The expressions discussed in Section 7.2.1 and Section 7.2.2 are valid for the circuit depicted in Figure 7.1 (a); in order to determine the currents of the buck-or-boost converter in Figure 7.1 (b), V_1 and V_i need to be interchanged.

7.2.3 Conduction Losses, Copper Losses, Dielectric Losses

Buck Operation

During buck operation, T_I , $D_{I,s}$, and D_{II} cause conduction losses:

$$P_{\text{cond},T_I,\text{buck}} = R_{T_I} I_{T_I,\text{buck}}^2, \quad (7.18)$$

$$P_{\text{cond},D_{I,s},\text{buck}} = V_{D_{I,s}} \bar{I}_{T_I,\text{buck}} + R_{D_{I,s}} I_{T_I,\text{buck}}^2, \quad (7.19)$$

$$P_{\text{cond},D_{II},\text{buck}} = V_{D_{II}} \bar{I}_{D_{II},\text{buck}} + R_{D_{II}} I_{D_{II},\text{buck}}^2. \quad (7.20)$$

The MOSFET's on-state resistance R_{T_I} , the diodes' forward voltage drops $V_{D_{I,s}}$, $V_{D_{II}}$ and the diodes' bulk resistances $R_{D_{I,s}}$, $R_{D_{II}}$ are given in Table 7.2.

Variable	Value	Description
CoolMOS SPW47N60C3:		
$R_{T_I}, R_{T_{II}}$	70 m Ω	on-state resistances of T_I and T_{II}
DSS25-0025B		
$V_{D_{I,s}}, V_{D_{II,s}}$	0.3 V	cut-in voltage of $D_{I,s}$ and $D_{II,s}$
$R_{D_{I,s}}, R_{D_{II,s}}$	8.6 m Ω	diode series resistances of $D_{I,s}$ and $D_{II,s}$
SDT12S60		
$V_{D_I}, V_{D_{II}}$	1.0 V	cut-in voltage of D_I and D_{II}
$R_{D_I}, R_{D_{II}}$	43 m Ω	diode series resistances of D_I and D_{II}
$L_{DC} = 150 \mu\text{H}$ [employed in Figure 7.1 (a); cf. Figure A.49]:		
$R_{L_{DC,DC}}$	26 m Ω	inductor's DC resistance
$R_{L_{DC,AC}}$	290 m Ω	inductor's AC resistance at 100 kHz
$L_{DC} = 200 \mu\text{H}$ [employed in Figure 7.1 (b); cf. Figure A.50]:		
$R_{L_{DC,DC}}$	45 m Ω	inductor's DC resistance
$R_{L_{DC,AC}}$	390 m Ω	inductor's AC resistance at 100 kHz
Electrolytic capacitors used for C_{DCi} [cf. Figure A.51]:		
$R_{C_{DCi}}$	250 m Ω	total equivalent series resistance (100 kHz)

Table 7.2: Converter parameters used to predict the conduction losses of the buck-or-boost converter at room temperature ($T_j = 25^\circ\text{C}$; cf. Chapter 4).

The copper losses in the DC inductor are approximately calculated with

$$P_{\text{cond},L_{DC},\text{buck}} = R_{L_{DC,DC}} \overline{I_{L_{DC},\text{buck}}}^2 + R_{L_{DC,AC}} \frac{\Delta I_{L_{DC},\text{buck}}^2}{12} \quad (7.21)$$

($R_{L_{DC,DC}}$ is the inductor's DC resistance and $R_{L_{DC,AC}}$ is the AC resistance of the inductor at $f = 100 \text{ kHz}$).

The losses generated in C_{DC1} are neglected, since film capacitors are employed. For C_{DCi} , however, electrolytic capacitors are used (cf. Figure A.51) with a measured total equivalent series resistance of 250 m Ω at 100 kHz. The respective losses are:

$$P_{\text{ESR},C_{DCi},\text{buck}} = R_{C_{DCi}} \frac{\Delta I_{L_{DC},\text{buck}}^2}{12}. \quad (7.22)$$

Boost Operation

During boost operation, T_{II} , $D_{II,s}$, and D_I cause conduction losses:

$$P_{\text{cond},T_{II},\text{boost}} = R_{T_{II}} I_{T_{II},\text{boost}}^2, \quad (7.23)$$

$$P_{\text{cond},D_{II,s},\text{boost}} = V_{D_{II,s}} \bar{I}_{T_{II},\text{boost}} + R_{D_{II,s}} I_{T_{II},\text{boost}}^2, \quad (7.24)$$

$$P_{\text{cond},D_I,\text{boost}} = V_{D_I} \bar{I}_{D_I,\text{boost}} + R_{D_I} I_{D_I,\text{boost}}^2. \quad (7.25)$$

The MOSFET's on-state resistance and the diodes' forward voltage drops and bulk resistances are given in Table 7.2.

The copper losses in the DC inductor are approximately calculated with

$$P_{\text{cond},L_{DC},\text{boost}} = R_{L_{DC},DC} \bar{I}_{L_{DC},\text{boost}}^2 + R_{L_{DC},AC} \frac{\Delta I_{L_{DC},\text{boost}}^2}{12}. \quad (7.26)$$

The losses in C_{DCi} are:

$$P_{\text{ESR},C_{DCi},\text{boost}} = R_{C_{DCi}} \frac{\Delta I_{L_{DC},\text{boost}}^2}{12}. \quad (7.27)$$

7.2.4 Switching Losses

Buck Operation

During buck operation, T_I is actively switched and T_{II} remains in the off-state. The switching losses of T_I comprise of the turn-on losses and the turn-off losses of this MOSFET; the switching losses of the Schottky diode $D_{I,s}$ and the silicon-carbide diode D_{II} are neglected. According to the discussions given in Section 4.3.2, the MOSFET's effective output capacitance enables ZVS and thus, very low turn-off losses result. Accordingly, the turn-off losses of the buck-or-boost converter are neglected.

In contrast, during turn-on, the involved MOSFET actively charges or discharges the parasitic capacitances depicted in Figure 7.5, which causes turn-on losses. The equivalent circuit used to calculate the turn-on losses (Figure 7.5) contains:

- the effective output capacitances of the employed MOSFETs [$C_{DS,T_I}(v_{T_I})$, $C_{DS,T_{II}}(v_{T_{II}})$; Figure 7.6 (a)],
- the junction capacitances of the silicon-carbide diodes [$C_{D_I}(v_{D_I})$, $C_{D_{II}}(v_{D_{II}})$; Figure 7.6 (b)],
- the backside to heat sink capacitances of the MOSFETs and the diodes (Table 7.3), and

- the winding capacitance of L_{DC} , C_{LDC} , estimated using the measured impedances depicted in Figures A.49 and A.50. For $L_{DC} = 150 \mu\text{H}$, a parallel resonant frequency of $f_{0,p} = 2.9 \text{ MHz}$ is measured and thus, $C_{LDC} = 20 \text{ pF}$ results; for $L_{DC} = 200 \mu\text{H}$, parallel resonance occurs for 3.5 MHz and C_{LDC} is approximately equal to 11 pF .

The heat sink is left on floating potential (not connected to ground) and thus, the backside to heat sink capacitances are connected in star between the nodes ①, ②, ③, and ④ [depicted in Figure 7.7 (a)]:

- $C_{Y1} = C_{TO220} + C_{TO247}$,
- $C_{Y2} = 2C_{TO220} + C_{TO247}$,
- $C_{Y3} = C_{TO220}$.

The outlined method used to predict the turn-on losses further considers a very simple MOSFET model: each MOSFET is replaced by the series con-

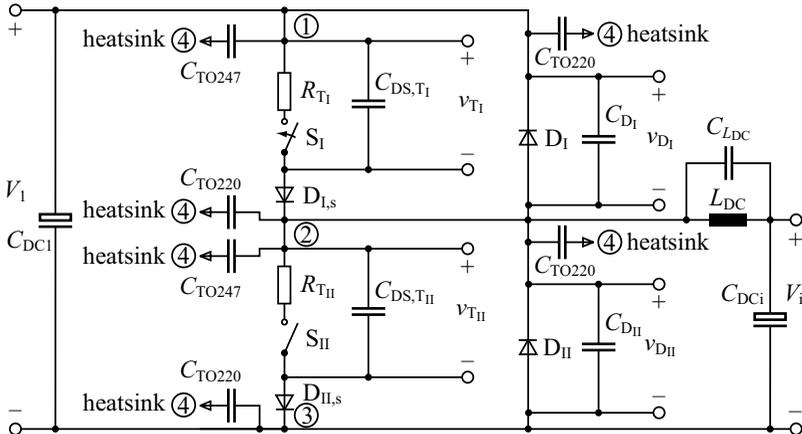


Figure 7.5: Parasitic capacitors considered to predict the turn-on losses of T_I : C_{DS,T_I} and $C_{DS,T_{II}}$ denote the output capacitances of the MOSFETs [Figure 7.6 (a)], C_{D_I} , and $C_{D_{II}}$ are the silicon-carbide diodes’ junction capacitances [Figure 7.6 (b)], C_{TO220} denotes the capacitance of a single TO-220 package (capacitances between the diodes’ cathodes and the heat sink), and C_{TO247} is the capacitance of a TO-247 package (capacitances between the MOSFETs’ drain connections and the heat sink).

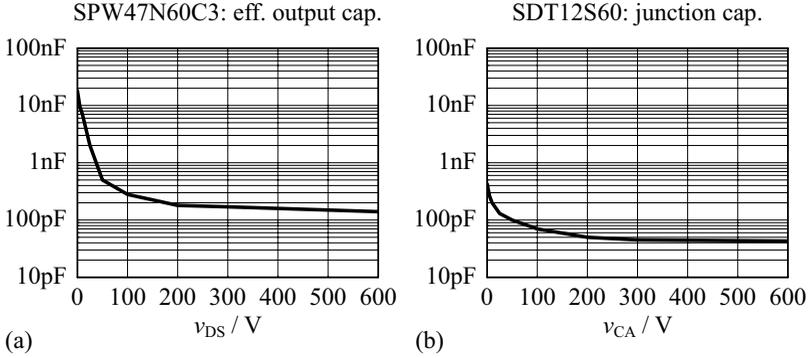


Figure 7.6: (a) Effective output capacitance (i.e. drain-to-source capacitance) of the employed MOSFET (CoolMOS, SPW47N60C3; obtained from [153]); (b) junction capacitance of the employed silicon-carbide diode (SDT12S60; obtained from [153]).

nection of an ideal switch and its on-state resistance (the body diodes of the MOSFETs never conduct and are thus not included).

Turning on S_I starts the charging or discharging of all the capacitors shown in Figure 7.5 via R_{T_I} . During the turn-on process, the diodes $D_{I,s}$ and $D_{II,s}$ conduct and the diodes D_I and D_{II} block. Therefore, the circuit shown in Figure 7.5 can be replaced by the simplified circuit depicted in Figure 7.7 (b). During the duration of the turn-on process, constant inductor current $I_{L_{DC}}$ is assumed and the voltage drops across $D_{I,s}$ and $D_{II,s}$ are neglected.

In order to determine C_I and C_{II} , the star connection of C_{Y1} , C_{Y2} , and C_{Y2} needs to be transformed to a delta circuit:

- $C_{D12} = (C_{TO220} + C_{TO247})/2$,
- $C_{D23} = C_{TO220}/2$,
- $C_{D13} = C_{TO220} (C_{TO220} + C_{TO247}) / [2 (2 C_{TO220} + C_{TO247})]$

[cf. Figure 7.7 (a)]. The resulting capacitances C_I and C_{II} [Figure 7.7 (b)] comprise of:

- $C_I = C_{DS,T_I} + C_{D_I} + C_{D12}$,
- $C_{II} = C_{DS,T_{II}} + C_{D_{II}} + C_{D23} + C_{L_{DC}}$ (on the assumption $C_{L_{DC}} \ll C_{D_{Ci}}$).

Variable	Value	Description
<i>KOOL-PADS K200 (thermally conductive and electr. insulating foil):</i>		
λ_{iso}	$1.30 \frac{\text{W}}{\text{mK}}$	thermal conductivity
$\epsilon_{\text{r,iso}}$	2.5	relative permittivity (measured at 1 kHz)
d_{iso}	0.2 mm	thickness (typical)
$V_{\text{iso,br}}$	1000 VRMS	breakdown voltage at 50 Hz
<i>TO-220:</i>		
A_{TO220}	13.5 mm × 10 mm	considered capacitor surface
C_{TO220}	15 pF	backside to heat sink capacitance
<i>TO-247:</i>		
A_{TO247}	20.9 mm × 15.9 mm	considered capacitor surface
C_{TO247}	37 pF	backside to heat sink capacitance

Table 7.3: Parasitic capacitances formed by the diodes’ backsides and the heat sink and the MOSFETs’ backsides and the heat sink (cf. Figure 7.5). Between the backsides of the power semiconductors and the heat sink, a thermally conductive and electrically insulating foil (KOOL-PADS K200) is used.

The energy $E_{\text{on},T_{\text{I}},\text{buck}}$, dissipated in $R_{T_{\text{I}}}$ during discharging or charging C_{I} and C_{II} , is used as an estimate of the turn-on losses. $E_{\text{on},T_{\text{I}},\text{buck}}$ can be obtained with an energy balance calculation:

$$E_{\text{stored,final}} + E_{\text{dissipated}} = E_{\text{stored,initial}} + E_{\text{delivered}}, \tag{7.28}$$

where $E_{\text{stored,initial}}$ denotes the energy stored in C_{I} and C_{II} at the beginning of the turn-on switching operation, $E_{\text{stored,final}}$ is the energy stored in C_{I} and C_{II} at the end of the switching operation, $E_{\text{delivered}}$ denotes the energy delivered by the source V_{I} , and $E_{\text{dissipated}}$ is the energy dissipated during turn-on. According to [127] the energy $E_C(V)$, which is stored in a non-linear capacitor $C(v)$ at a capacitor voltage V , is obtained from:

$$E_C(V) = \int_0^V v C(v) dv = \frac{1}{2} C_{\text{E,eq}}(V) V^2, \tag{7.29}$$

where $C_{\text{E,eq}}(V)$ denotes the energy equivalent capacitance value at a given capacitor voltage [Figure 7.8 (a) depicts the energy equivalent output capacitance of the SPW47N60C3 CoolMOS]. Since $C(v)$ is a differential capacitance,

$$C(v) = \frac{dq}{dv}, \tag{7.30}$$

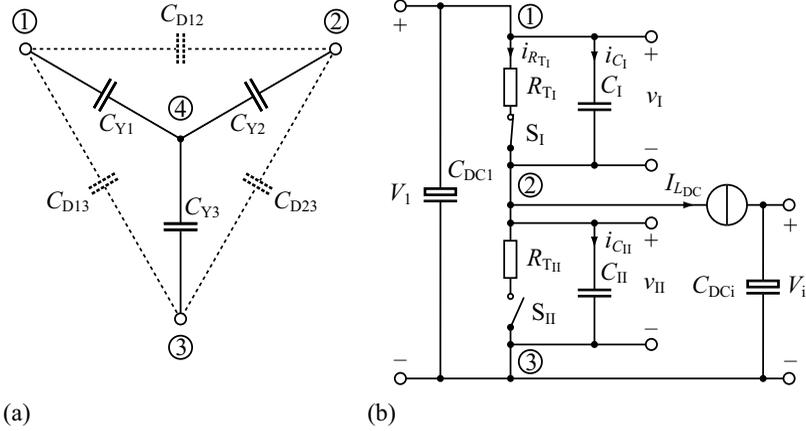


Figure 7.7: (a) Star connection of the parasitic backside to heat sink capacitances of the MOSFETs and the diodes (dashed lines: delta connection obtained with the wye-delta transformation). (b) simplified circuit employed to estimate the turn-on losses (buck operation). The electric capacitance of the heat sink with respect to earth is neglected; the presented calculation and the equivalent circuit need to be modified if a considerably high capacitance with respect to earth is present, e.g. by using the star to polygon transformation given in [126].

the charge $Q_C(V)$, which is stored in $C(v)$ at a capacitor voltage V , is given with [107]:

$$Q_C(V) = \int_0^V C(v)dv = C_{Q,eq}(V)V; \quad (7.31)$$

$C_{Q,eq}(V)$ represents the charge equivalent capacitance value at a given capacitor voltage [Figure 7.8 (b)]. The particular energies used in (7.28) can be expressed with (7.29) and (7.31):

- $E_{\text{stored,initial}} = C_{I,E,eq}(V_1)V_1^2/2$, since C_I is charged to V_1 and C_{II} is fully discharged at the beginning of the turn-on switching operation of S_I ;
- $E_{\text{stored,final}} = C_{II,E,eq}(V_1)V_1^2/2$, since C_I is fully discharged and C_{II} is charged to V_1 at the end of the turn-on switching operation of S_I ;
- $E_{\text{delivered}} = V_1 \Delta Q = V_1 C_{II,Q,eq}(V_1)V_1 = V_1^2 C_{II,Q,eq}(V_1)$, since the source V_1 delivers the charge stored in C_{II} after the switching operation has completed (the charge of C_I is dissipated in R_{T_I});

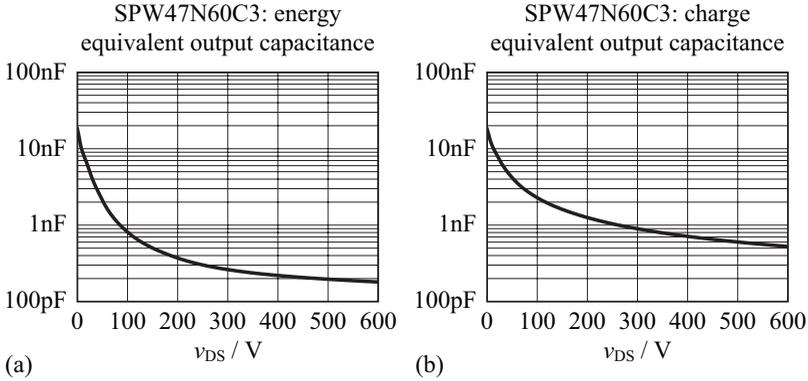


Figure 7.8: (a) Energy equivalent output capacitance of the SPW47N60C3 CoolMOS calculated with (7.29); (b) charge equivalent output capacitance of the SPW47N60C3 CoolMOS calculated with (7.31). The effective output capacitance of the SPW47N60C3 CoolMOS (Figure 7.6 (a)) is substituted for $C(v)$ used in (7.29) and (7.31).

- $E_{\text{dissipated}} = E_{\text{on},T_{\text{I}},\text{buck}}$.

Thus, the result for $E_{\text{on},T_{\text{I}},\text{buck}}$ is:

$$E_{\text{on},T_{\text{I}},\text{buck}} = \frac{1}{2}C_{\text{I,E,eq}}(V_1)V_1^2 - \frac{1}{2}C_{\text{II,E,eq}}(V_1)V_1^2 + V_1^2C_{\text{II,Q,eq}}(V_1). \quad (7.32)$$

The turn-on losses are finally calculated using:

$$P_{\text{on},T_{\text{I}},\text{buck}} = f_S E_{\text{on},T_{\text{I}},\text{buck}}. \quad (7.33)$$

The energy and charge equivalent capacitances calculated for $C_{\text{I}}(V_1)$ and $C_{\text{II}}(V_1)$ are shown in Figure 7.9.

Boost Operation

During boost operation, T_{II} is actively switched and T_{I} remains in the off-state. Again, the turn-off losses of T_{II} are neglected and the turn-on losses are estimated according to the discussion given in the Section above. However, since the direction of $I_{L_{\text{DC}}}$ reverses [cf. Figure 7.7 (b)], C_{I} and C_{II} need to be interchanged in order to calculate the turn-on losses $P_{\text{on},T_{\text{II}},\text{boost}}$:

$$E_{\text{on},T_{\text{II}},\text{boost}} = \frac{1}{2}C_{\text{II,E,eq}}(V_1)V_1^2 - \frac{1}{2}C_{\text{I,E,eq}}(V_1)V_1^2 + V_1^2C_{\text{I,Q,eq}}(V_1), \quad (7.34)$$

$$P_{\text{on},T_{\text{II}},\text{boost}} = f_S E_{\text{on},T_{\text{II}},\text{boost}}. \quad (7.35)$$

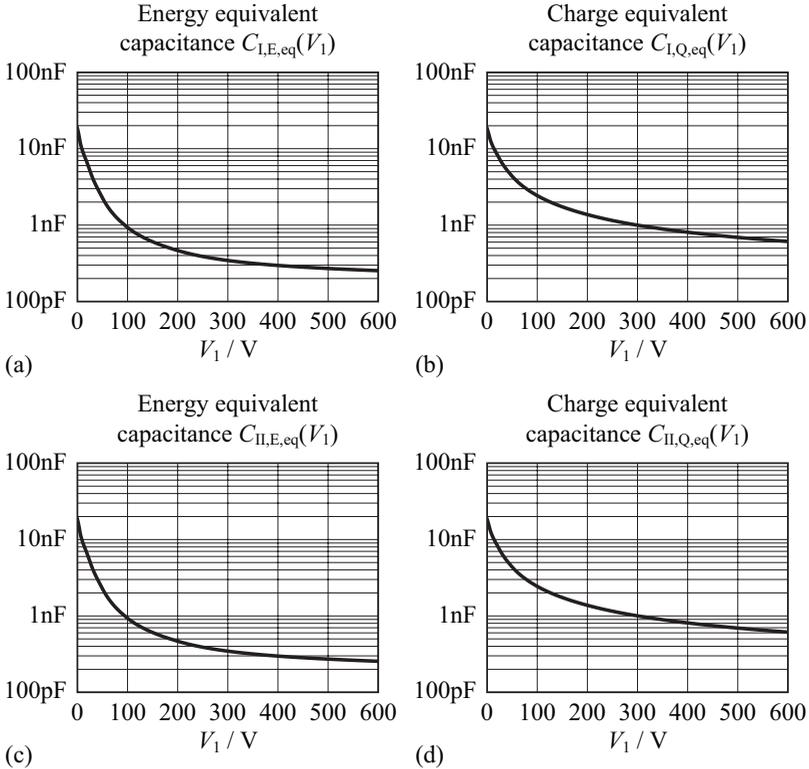


Figure 7.9: (a) Energy equivalent capacitance values calculated for $C_I(v)$; (b) charge equivalent capacitance values calculated for $C_I(v)$; (c) energy equivalent capacitance values calculated for $C_{II}(v)$; (d) charge equivalent capacitance values calculated for $C_{II}(v)$. $C_I(v)$ and $C_{II}(v)$ of the investigated buck-boost converter are nearly equal.

7.2.5 Core Losses

The core losses of the DC inductor L_{DC} are calculated with the Steinmetz equation,

$$P_{\text{core},L_{DC}} = dpf(H_{L_{DC},DC}) \cdot V_{\text{core},L_{DC}} \cdot k \cdot f_S^\alpha \cdot B_{L_{DC},AC,\text{peak}}^\beta; \quad (7.36)$$

the displacement factor $dpf(H_{L_{DC},DC})$ considers the increase of the core losses due to the DC inductor current $\bar{I}_{L_{DC},\text{buck}}$ or $\bar{I}_{L_{DC},\text{boost}}$

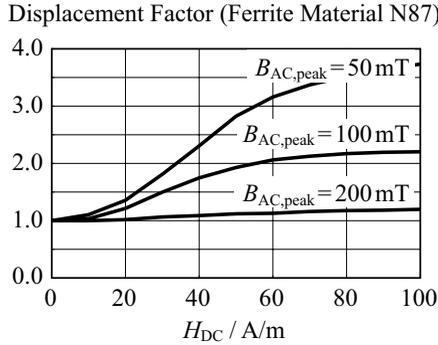


Figure 7.10: Relative increase of the core losses by reason of a DC biased inductor core (ferrite material N87); H_{DC} denotes the DC component of the magnetic field in the inductor core, $B_{AC,peak}$ is the amplitude of the AC component of the flux density (from [128]; measured at a core temperature of 100°C and at a frequency of 100 kHz).

[(7.3), (7.11); Figure 7.10, [128]]. The actual value of $d_{pf}(H_{L_{DC},DC})$ is obtained based on the data given in Figure 2 in [128] and linear approximation.³ The DC component of the magnetic field in the ferrite core is:

$$H_{L_{DC},DC} \approx \frac{L_{DC} \bar{I}_{L_{DC}}}{\mu_0 \mu_r, L_{DC} N_{L_{DC}} A_{core, L_{DC}}} \tag{7.37}$$

and the amplitude of the AC component of the magnetic flux density is:

$$B_{L_{DC},AC,peak} = \frac{L_{DC} \Delta I_{L_{DC}} / 2}{N_{L_{DC}} A_{core, L_{DC}}}. \tag{7.38}$$

Table 7.4 summarizes the remaining parameters used in (7.36), (7.37), and (7.38).

7.2.6 Gate Driver Losses

With the employed power MOSFETs (SPW47N60C3), at rated output power ($P_{out} = 2\text{ kW}$), $V_1 = 340\text{ V}$, $V_i = 225\text{ V}$, buck operation (only T_1 is actively

³In [128] the displacement factor depicted in Figure 7.10 is measured for the ferrite material N87 at 100 kHz and for a core temperature T_{core} of 100°C. The presented converter model, however, considers a core temperature of 25°C. Still, with the data given in [128] being directly adopted for a core temperature of $T_{core} = 25^\circ\text{C}$, acceptable total losses are calculated (cf. Figure 7.11). However, if a more accurate calculation of the core losses is required, new measurements have to be conducted at $T_{core} = 25^\circ\text{C}$.

<i>Variable</i>	<i>Value</i>	<i>Description</i>
<i>Currents:</i>		
$\bar{I}_{L_{DC}}$	$\bar{I}_{L_{DC},\text{buck}}$ (buck operation) $\bar{I}_{L_{DC},\text{boost}}$ (boost operation)	average inductor current
$\Delta I_{L_{DC}}$	$\Delta I_{L_{DC},\text{buck}}$ (buck operation) $\Delta I_{L_{DC},\text{boost}}$ (boost operation)	peak-to-peak current value
<i>Inductor parameters:</i>		
$A_{\text{core},L_{DC}}$	519 mm^2 ($L_{DC} = 150 \mu\text{H}$)	core cross section area
$A_{\text{core},L_{DC}}$	310 mm^2 ($L_{DC} = 200 \mu\text{H}$)	
$V_{\text{core},L_{DC}}$	36.2 cm^3 ($L_{DC} = 150 \mu\text{H}$)	total core volume
$V_{\text{core},L_{DC}}$	20.8 cm^3 ($L_{DC} = 200 \mu\text{H}$)	
$N_{L_{DC}}$	16 ($L_{DC} = 150 \mu\text{H}$)	employed number of turns
$N_{L_{DC}}$	24 ($L_{DC} = 200 \mu\text{H}$)	
<i>Core material parameters (ferrite, N87):</i>		
μ_r, L_{DC}	2200	relative initial permeability
k	14.1	Steinmetz-parameters for a core temperature of 25°C, obtained from data sheet values, App. C.
α	1.275	
β	2.416	

Table 7.4: Additional data used to calculate the core losses of L_{DC} .

switched), and 100 kHz switching frequency, an input current of the high side gate driver of $\approx 40 \text{ mA}$ is measured at a supply voltage of 12 V. On the assumption of an efficiency of 75% of the isolated DC–DC converter, used to supply the high side gate driver, and an efficiency of 75% of the auxiliary power supply, needed to provide the supply voltages for the converter electronics (5 V, 12 V) from one of the DC voltages (e.g. V_1), the gate driver’s power demand is

$$P_{\text{gate,buck}} = 12 \text{ V} \cdot 40 \text{ mA} / (0.75 \cdot 0.75) = 0.85 \text{ W}. \quad (7.39)$$

During boost operation, only T_{II} is actively switched, and the measured input current of the respective gate driver is again $\approx 40 \text{ mA}$ at 12 V. For the low side gate driver, the 12 V DC voltage provided from the auxiliary power supply is directly used to supply the gate driver. On the assumption of a power supply

efficiency of 75%, the gate driver's power demand is

$$P_{\text{gate,boost}} = 12 \text{ V} \cdot 40 \text{ mA} / 0.75 = 0.64 \text{ W}. \quad (7.40)$$

7.2.7 Total Buck-or-Boost Converter Losses

Buck Operation

During buck operation, the proposed loss model considers the total losses according to:

$$\begin{aligned} P_{\text{t,buck}} = & P_{\text{cond,TI,buck}} + P_{\text{on,TI,buck}} + P_{\text{cond,DIs,buck}} + P_{\text{cond,DII,buck}} \\ & + P_{\text{cond,LDC,buck}} + P_{\text{ESR,CDCi,buck}} + P_{\text{gate,buck}}. \end{aligned} \quad (7.41)$$

Boost Operation

During boost operation, the total losses are:

$$\begin{aligned} P_{\text{t,boost}} = & P_{\text{cond,TII,boost}} + P_{\text{on,TII,boost}} + P_{\text{cond,DII,s,boost}} + P_{\text{cond,DII,boost}} \\ & + P_{\text{cond,LDC,boost}} + P_{\text{ESR,CDCi,boost}} + P_{\text{gate,boost}}. \end{aligned} \quad (7.42)$$

7.2.8 Results

In Figure 7.11 the measured losses of the buck-or-boost converter prototype, designed in Appendix A.8, are compared to the losses calculated with (7.41) [Figure 7.11 (a)] or (7.42) [Figure 7.11 (b)]. There, the nominal input voltage, $V_1 = 340 \text{ V}$, and the DC link voltage $V_l = 225 \text{ V}$ are used [according to the converter setup depicted in Figure 7.1 (a); cf. Table 7.1]. Similar to the DAB, the influence of raised component temperatures is not included (cf. Chapter 4); the losses are calculated for component and junction temperatures of 25°C (in Figure 7.11, the \square -symbols denote the efficiencies measured after a short run time of 30 seconds and the \triangle -symbols denote the efficiencies measured at continuous converter operation).

With the simple converter model discussed in this Chapter, acceptable matching between measured and calculated losses is achieved. The accuracy achieved with the discussed buck-or-boost converter model is considered to be sufficient, if buck-or-boost converter and DAB are connected in series (Figure 7.1) since the DAB converter losses are considerably larger than the buck-or-boost converter losses.⁴

⁴The model improvements discussed in Chapter 4, in particular the accurate consideration of conduction losses and the use of measured switching losses, could be applied to the buck-or-boost converter if a better matching between measured and calculated losses would be needed.

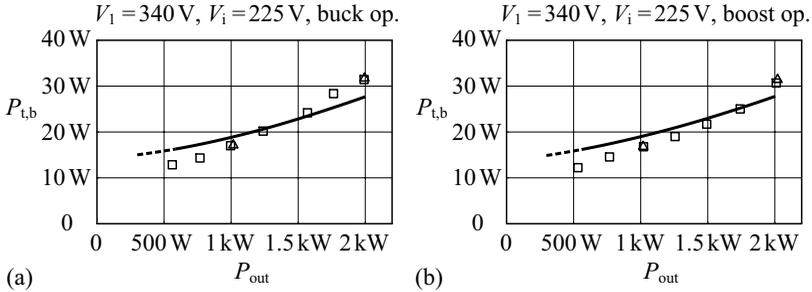


Figure 7.11: Measured and calculated buck-or-boost converter losses for (a) buck operation and (b) boost operation; $V_1 = 340$ V, $V_i = 225$ V [Figure 7.1 (a)], $L_{DC} = 150$ μ H, $f_S = 100$ kHz, and $T = 25^\circ$ C. The solid line denotes the calculated losses (CCM operation), the rectangles mark the measured losses for a short run time of 30 seconds (cf. Chapter 4) and the \triangle -symbols mark the losses measured at continuous operation (≈ 10 minutes). The dashed line denotes discontinuous conduction mode (DCM) operation; there, the calculations are not valid.

7.3 Two-Stage Converters – Efficiencies

The efficiency calculations for the converters depicted in Figure 7.1 employ the DAB converter model detailed in Chapter 4 and the buck-or-boost converter model discussed in Section 7.2, whereas the power transfer direction determines the input and output power levels of the converters:

- HV \rightarrow LV: the DAB input power is equal to the output power of the buck-or-boost converter, $P_{in,DAB} = P_{out,b}$ [Figure 7.12 (a)],
- LV \rightarrow HV: the input power of the buck-or-boost converter is equal to the DAB output power, $P_{in,b} = P_{out,DAB}$ [Figure 7.12 (b)].

The DAB is operated with the optimized modulation scheme discussed in Section 5.2.2 in order to achieve maximum efficiency. Moreover, for each of the 4 circuit variants listed in Table 7.1, the DAB is separately designed according to Appendix A.2 using the voltage ranges specified in Table 1.4 and Table 7.1. The resulting DAB converter parameters n and L for maximum average efficiency $\bar{\eta}$ [calculated with (A.1), (A.2), (A.3), and (A.4)] of the two-stage converters are listed in Table 7.5. Besides, the value of the DC inductor L_{DC} depends on the circuit arrangement [i.e. buck/boost in Figure 7.1 (a) or boost/buck in Figure 7.1 (b); cf. Appendix A.8 and Table 7.5].

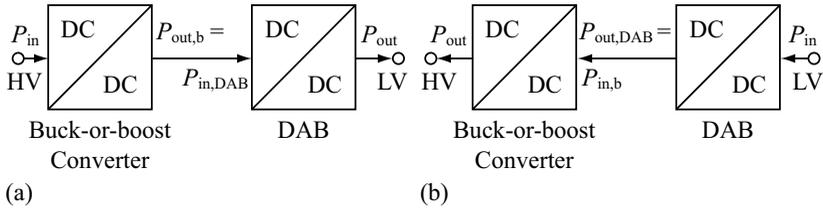


Figure 7.12: The calculation of the total converter efficiency employs the loss models of the buck-or-boost converter (Section 7.2) and of the DAB converter (Chapter 4). The considered input and output power levels depend on the direction of power transfer: (a) power transfer from the HV to the LV port, (b) power transfer from the LV to the HV port.

Figure 7.13 and Figure 7.14 depict the calculated total converter efficiencies for power being transferred from the HV port to the LV port, $P_{out}(= P_{out,DAB}) = 1\text{ kW}$ and $P_{out} = 2\text{ kW}$, and the 4 circuit variants listed in Table 7.1:

- Figure 7.13 (a), (b): $V_i = 225\text{ V}$,
- Figure 7.13 (c), (d): $V_i = 225\text{ V} \cdot \frac{V_2}{16\text{ V}}$, i.e. $150\text{ V} \leq V_i \leq 225\text{ V}$,
- Figure 7.14 (a), (b): $V_i = 475\text{ V}$,
- Figure 7.14 (c), (d): $V_i = \max\left(\frac{V_1}{D_{b,max}}, 475\text{ V} \cdot \frac{V_2}{16\text{ V}}\right)$, i.e. $325\text{ V} \leq V_i \leq 475\text{ V}$.

7.3.1 Efficiencies for $V_i \leq 225\text{ V}$ [Figure 7.1 (a)]

The converter setup depicted in Figure 7.1 (a) achieves highest efficiencies at low HV port voltages, i.e. for V_1 close to 240 V (Figure 7.13). Moreover, regarding the operation with $P_{out} = 2\text{ kW}$ [Figures 7.13 (b) and (d)], the use of a constant DC link voltage, $V_i = 225\text{ V}$, facilitates higher converter efficiencies than the operation with a variable DC link voltage, $150\text{ V} \leq V_i \leq 225\text{ V}$: with decreasing DC link voltages, the MOSFET currents and the diode currents of the buck-or-boost converter increase, which causes the conduction losses to increase and the efficiency to decrease. Consequently, the average efficiency achieved with constant DC link voltage ($\bar{\eta} = 93.0\%$) is higher than the average efficiency achieved with variable DC link voltage ($\bar{\eta} = 92.7\%$, Table 7.5).

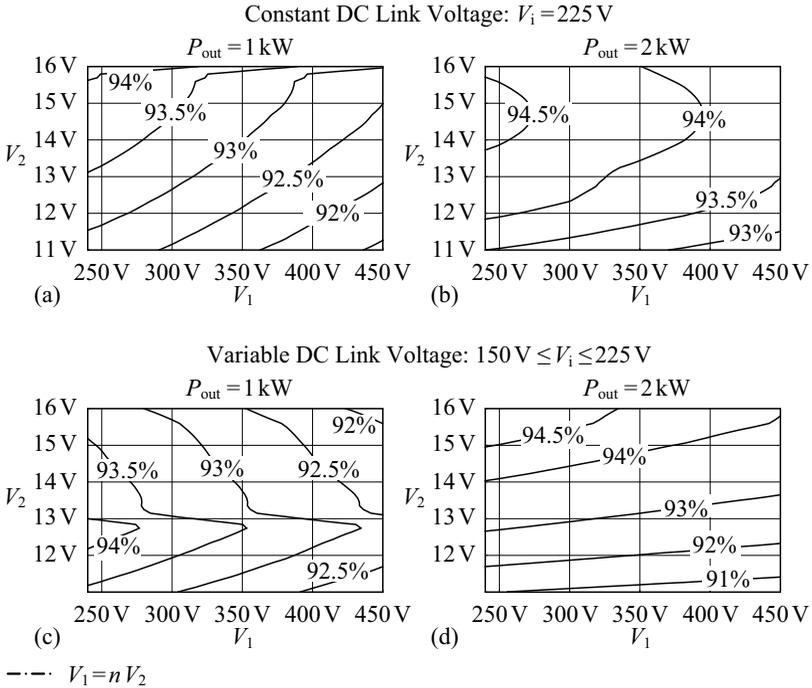


Figure 7.13: Efficiencies achieved with the two-stage circuit variants 1 and 2 listed in Table 7.1 [Figure 7.1 (a)], $P_{\text{out}} = 1\text{ kW}$ or $P_{\text{out}} = 2\text{ kW}$, and power being transferred from the HV port to the LV port: (a), (b) constant $V_i = 225\text{ V}$; (c), (d) variable $150\text{ V} \leq V_i \leq 225\text{ V}$. The efficiency calculation considers the effect of the linear interpolation used by the DSP to determine the actual modulation parameters (Appendix E.2), which causes the irregular efficiency characteristics of the depicted contour lines. Moreover, the irregular efficiency characteristics at $V_2 \approx 16\text{ V}$ in Figure (a) and at $V_2 \approx 13\text{ V}$ in Figure (c) are caused by the suboptimal modulation scheme: at these port voltages V_2 , P_{out} migrates from values less than $P_{\text{out},\Delta,a,\text{max}}$ (extended triangular current mode modulation, i.e. the efficiency is slightly below the maximum achievable efficiency) to values greater than $P_{\text{out},\Delta,a,\text{max}}$ [operation with almost maximum achievable efficiency, cf. Section 5.2.2 and Figure 5.28 (a)].

<i>Circuit No.:</i>	1	2	3	4
<i>DC-Link Voltage or DC-Link Voltage Range (according to Table 7.1):</i>				
V_i	225 V	150 ... 225 V	475 V	325 ... 475 V
<i>Design Results for the DAB:</i>				
L	11.0 μH	6.1 μH	50.0 μH	36.1 μH
n	13	13	28	26
<i>Design Results for the Buck-or-Boost Converter:</i>				
L_{DC}	150 μH	150 μH	200 μH	200 μH
<i>Calculated Total Average Converter Efficiencies (Appendix A.1)</i>				
$\bar{\eta}$	93.0%	92.7%	92.7%	92.8%

Table 7.5: Design summary for the two-stage converters depicted in Figure 7.1 and characterized in Table 7.1.

7.3.2 Efficiencies for $V_i \geq 325$ V [Figure 7.1 (b)]

With the converter setup depicted in Figure 7.1 (b) and constant DC link voltage ($V_i = 475$ V), the highest efficiencies are achieved for high HV port voltages (V_1 close to 450 V). At $P_{\text{out}} = 2$ kW, high converter efficiency is achieved within the defined input and output voltage ranges [Figure 7.14 (b)], due to the reduced MOSFET currents in the HV side full bridge of the DAB. At $P_{\text{out}} = 1$ kW, however, reduced efficiencies result [Figure 7.14 (a)], since the turn-on losses of the MOSFET T_{II} increase with increasing DC link voltage V_i (Section 7.2.4).

With variable DC link voltage and rated output power, $P_{\text{out}} = 2$ kW, highest efficiency is obtained for a high DC voltage V_2 [i.e. close to 16 V, Figure 7.14 (d)]; the obtained efficiency decreases with a reduced DC voltage V_2 close to 11 V, due to increasing currents in the buck-or-boost converter and in the HV side full bridge of the DAB. At $P_{\text{out}} = 1$ kW, however, the average efficiency achieved with a variable DC link voltage V_i [Figure 7.14 (c)] is higher than the average efficiency obtained with a constant V_i [Figure 7.14 (a)], since the turn-on losses of T_{II} and the conduction losses due to the circulating transformer currents decrease with decreasing DC link voltage V_i . Besides, according to Figures 7.14 (a) and (c), the characteristics of the efficiencies achieved with constant $V_i = V_2/D_{\text{b,max}}$ is clearly different to the efficiency characteristics achieved with variable V_i .

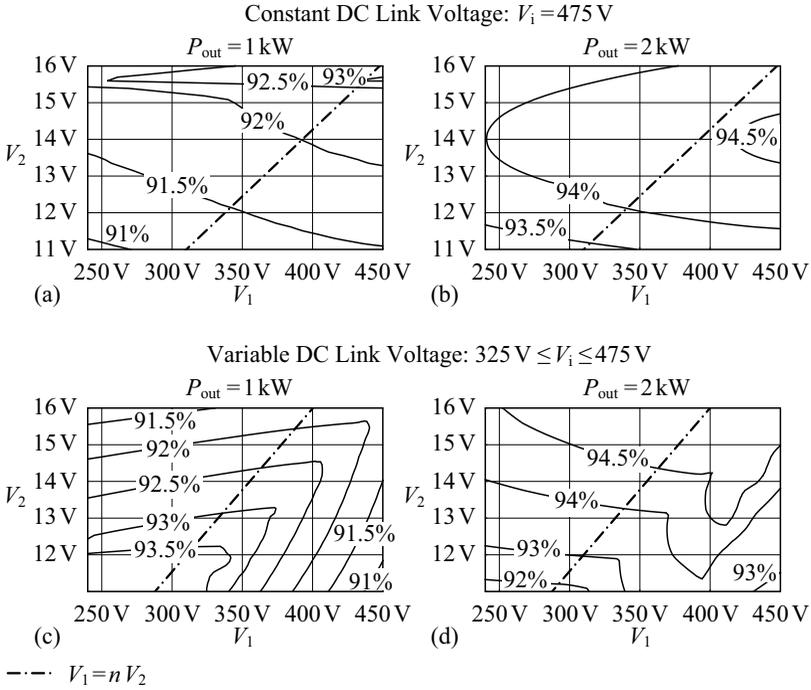


Figure 7.14: Efficiencies achieved with the two-stage circuit variants 3 and 4 listed in Table 7.1 [Figure 7.1 (b)], $P_{\text{out}} = 1\text{ kW}$ or $P_{\text{out}} = 2\text{ kW}$, and power being transferred from the HV port to the LV port: (a), (b) constant $V_i = 475\text{ V}$; (c), (d) variable $325\text{ V} \leq V_i \leq 475\text{ V}$. Irregular characteristics of the contour lines are due to the reasons given in the caption of Figure 7.13.

The average efficiencies achieved with $V_i \geq 325\text{ V}$ ($\bar{\eta} = 92.7\%$ or $\bar{\eta} = 92.8\%$, Table 7.5) are slightly below the average efficiency achieved with $V_i = 225\text{ V}$ ($\bar{\eta} = 93.0\%$). Thus, out of the converter configurations depicted in Figure 7.1 and detailed in Table 7.1, the converter setup with a constant DC link voltage of 225 V [Figure 7.1 (a)] is preferred.

7.4 Conclusion

In this Chapter, 4 different bidirectional, two-stage DC–DC converter configurations are investigated. The aim of the presented analysis is to determine the two-stage DC–DC converter with the highest average efficiency (calcu-

lated according to Appendix A.1).

The two-stage converters considered in Figure 7.1 consist of an optimized DAB converter, which provides galvanic isolation and facilitates highly efficient, bidirectional power transfer between an LV port and a HV DC link port, and a highly efficient buck-or-boost converter (Figure 7.2). Moreover, constant and variable DC link voltages are investigated (Table 7.1).

In order to facilitate the calculation of the total converter efficiency, a loss model is developed for the buck-or-boost converter. The loss model is validated using measurement results obtained from an actual hardware prototype.

At rated output power, $P_{\text{out}} = 2 \text{ kW}$, and within the specified input and output voltage ranges (Table 1.4), the distribution of the efficiencies obtained for the two-stage solutions 1 and 3 (constant DC link voltage, cf. Table 7.1) is more balanced than the efficiency distribution achieved for a single-stage DAB converter (Figure 5.31). However, the calculated average efficiencies ($92.7\% \leq \bar{\eta} \leq 93.0\%$) are below the average efficiency values calculated for the single-stage DAB (93.5%). This, together with the more complex hardware setup required, renders the proposed two-stage solutions less attractive than the single-stage DAB.

Chapter 8

Conclusions and Outlook

In the presented work, a bidirectional DC–DC converter with a low voltage/high current port, specified in Table 1.4, is investigated. Based on an evaluation of 6 different suitable single-stage converter topologies, the DAB converter is judged to be most promising with respect to a high achievable converter efficiency and a high achievable power density (Chapter 2.3). Accordingly, the DAB converter is investigated in detail; the results obtained for the DAB converter are summarized in the following list.

- In Chapter 3, the working principle of the DAB converter is explained based on different simplified converter models. This includes the lossless converter model (Figure 3.2), which facilitates basic analytical investigations on the DAB converter. In this context, in Section 3.1.3, closed-form analytical expressions for the modulation parameters D_1 , D_2 , and φ of an optimal modulation scheme, optimized with respect to minimum inductor RMS current, are derived. Moreover, two different refinements of the electric DAB converter model are presented: Section 3.2 investigates the impact of the conduction losses on the transformer currents and on the power transfer characteristics; Section 3.3 discusses a simplified method to consider the magnetizing current in the transformer currents.
- Chapter 4 presents a detailed loss model of the DAB converter, used to calculate the losses in the most relevant converter components, i.e. the semiconductor switches (conduction and switching losses), the transformer (winding and core losses), and the inductor (copper and core losses). The efficiencies calculated with this loss model are verified using experimental results: for phase shift modulation, an average relative error of the calculated losses of 6.0% is achieved (Table 4.2). The de-

tailed loss model of the DAB converter is needed in order to develop the efficiency optimized modulation schemes presented in Chapter 5.

- Chapter 5 details a systematic investigation of efficiency improvements achievable for the given DAB converter, obtained with the use of optimized modulation schemes. Finally, with the suboptimal modulation schemes discussed in Section 5.2.2, converter operation close to its maximum possible efficiency is achieved (Figure 5.28). However, in order to calculate modulation parameters D_1 , D_2 , and φ suitable for the experimental setup, the detailed converter loss model discussed in Chapter 4 is used. Due to the high complexity of this model, no closed-form expressions can be given for D_1 , D_2 , and φ ; the modulation parameters are calculated with the equation systems given in Section 5.2.2, using a multidimensional numerical solver.

The most critical loss mechanisms of the given DAB converter, identified in Section 5, are:

- conduction losses,
- HV side switching losses (ZVS is required), and
- LV side switching losses (large currents should be avoided during switching).

The calculated results are verified using experimental data.

- In Chapter 6, a small-signal model of the DAB and a dynamic model of the complete converter system (including the digital control platform) are derived. The calculated results are verified using experimental data; good matching between measured and calculated results is achieved. Moreover, Section 6.2.6 illustrates an effective method to derive a simplified transfer function of a given DAB converter. According to the obtained results, the time delays caused by the digital control platform mainly limit the dynamic properties of the given DAB converter. The achieved step response of the current control loop is depicted in Figure 6.14: the proposed current controller achieves a rise time $t_r \approx 250 \mu\text{s}$ and a delay time $t_d \approx 200 \mu\text{s}$ with a percentage overshoot of approximately 7%.

Chapter 7 considers 4 different circuit variants of the series connection of a DAB converter and a buck-or-boost converter (without galvanic isolation) in order to quantify possible efficiency improvements obtained with a two-stage solution. Consequently, a loss model of the buck-or-boost converter is developed to facilitate the calculation of the efficiency of the two-stage converter. However, the calculated average efficiency of the two-stage converters is less

than the average efficiency calculated for the single-stage DAB converter (two-stage converter variants: $\bar{\eta} \leq 93.0\%$, single-stage DAB converter: $\bar{\eta} = 93.5\%$; $\bar{\eta}$ is calculated according to Appendix A.1; the DAB converters employ the suboptimal modulation schemes discussed in Section 5.2.2). Thus, in average, the additional losses of the buck-or-boost converter cannot outweigh the efficiency improvements achieved with the DAB converter.

8.1 Concluding Remarks Regarding Suitable Bidirectional DC–DC Converter Topologies

With the given DAB converter, the optimized modulation schemes, and the design procedure presented in Appendix A.2, high converter efficiency is achieved for a constant switching frequency, within wide voltage ranges ($240\text{ V} \leq V_1 \leq 450\text{ V}$ and $11\text{ V} \leq V_2 \leq 16\text{ V}$), and within a wide power range (Figure 5.31). However, the construction of the LV side full bridge is challenging with respect to low conduction losses and low switching losses; furthermore, the LV side DC capacitor C_{DC2} is subject to large RMS currents and the calculation of applicable modulation parameters (D_1 , D_2 , and φ) is considerably complex. These difficulties can be avoided with the full bridge converter topologies with one or more DC inductors on the LV side (Section 2.2.1): the DC inductors reduce the RMS current through the DC capacitor C_{DC2} and with the modulation schemes discussed in Appendix A.5, the switches of the LV side full bridge do not actively turn off current. However, due to the large volume of the filter inductors L_{DC2} or L_{DC2a} and L_{DC2b} , the achievable power density is considered to be less than the power density that can be achieved with the DAB converter (following [39]). Furthermore, with the modulation schemes presented in Appendix A.5, the resulting efficiency depends on the direction of power transfer, i.e. the efficiency for power being transferred from the HV port to the LV port is higher than for power being transferred in the opposite direction.

Among the full bridge converter topologies with one or more DC inductors on the LV side, the current doubler circuit features the lowest transformer currents (advantageous with respect to low losses on the connecting paths between the LV port of the HF transformer and the switches) whereas the push-pull converter only requires a single DC inductor. With respect to the voltage range specified for V_2 , $11\text{ V} \leq V_2 \leq 16\text{ V}$, and the power rating of 2 kW, the current doubler (Figure 2.13) and the push-pull converter (Figure 2.14) will both outperform the LV side full bridge with DC inductor (Figure 2.12), due to the available semiconductor switches (Appendix D.2).

According to the specifications given in Table 1.4, a constant switching frequency f_S is required. However, if a variable switching frequency would be permitted, f_S could be used to modify the transferred power (besides D_1 , D_2 ,

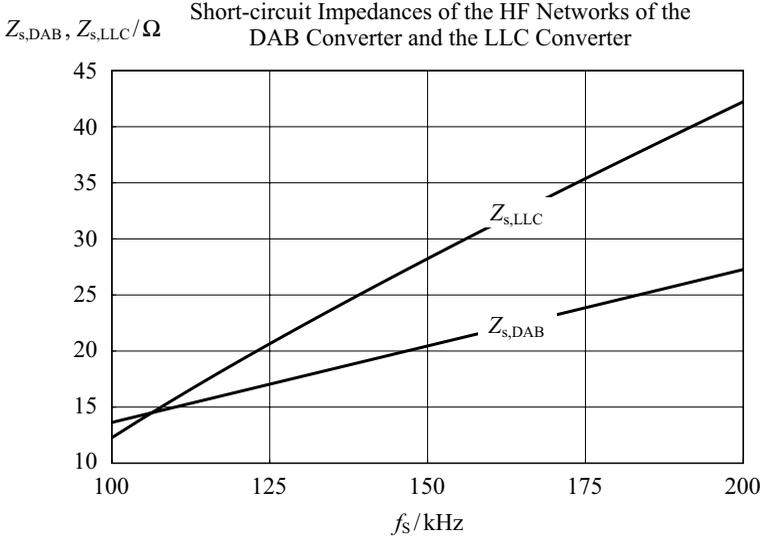


Figure 8.1: Short-circuit impedances of the HF networks of the DAB and the LLC converters; $|Z_{s,DAB}|$ considers $L = 21.7 \mu H$ (determined in case of optimal modulation parameters being used, cf. Appendix A.2.1); $|Z_{s,LLC}|$ considers $L = 38.3 \mu H$ and $C = 135 \text{ nF}$ (optimal modulation parameters, cf. Appendix A.4.4).

and φ). The absolute value of the short-circuit impedance of the HF network of the LLC converter,

$$|Z_{s,LLC}(\omega)| = \frac{1 - \omega^2 LC}{\omega C}, \quad (8.1)$$

varies more than the short-circuit impedance of the HF network of the DAB converter (Figure 8.1),

$$|Z_{s,DAB}(\omega)| = \omega L, \quad (8.2)$$

if two different frequencies ω_1 and ω_2 and operation above resonance of the LLC converter are regarded:

$$|Z_{s,DAB}(\omega_2)/Z_{s,DAB}(\omega_1)| < |Z_{s,LLC}(\omega_2)/Z_{s,LLC}(\omega_1)| \quad \forall (\omega_1 > \frac{1}{\sqrt{LC}}) \vee (\omega_2 > \omega_1). \quad (8.3)$$

According to (3.13), $|\underline{Z}_{s,\text{DAB}}(\omega)|$ limits the maximum output power of the DAB converter and according to (16) in [129], $|\underline{Z}_{s,\text{LLC}}(\omega)|$ limits the maximum possible output power of the LLC converter.¹ Thus, for the LLC converter, a given increase of the switching frequency results in a larger reduction of the maximum output power than for the DAB converter (this is particularly true if the LLC converter is operated close to the resonance frequency of $Z_{s,\text{LLC}}$). Figure 8.1 depicts the short-circuit impedances $|\underline{Z}_{s,\text{DAB}}(\omega)|$ and $|\underline{Z}_{s,\text{LLC}}(\omega)|$ for the DAB converter with $L = 21.7 \mu\text{H}$ (Appendix A.2.1) and for the LLC converter with $L = 38.3 \mu\text{H}$ and $C = 135 \text{ nF}$ (Appendix A.4.4): for $\omega_1 = 2\pi \cdot 100 \cdot 10^3 \text{ s}^{-1}$ and $\omega_2 = 2\pi \cdot 200 \cdot 10^3 \text{ s}^{-1}$, $|\underline{Z}_{s,\text{DAB}}(\omega_2)/\underline{Z}_{s,\text{DAB}}(\omega_1)| = 2.0$ and $|\underline{Z}_{s,\text{LLC}}(\omega_2)/\underline{Z}_{s,\text{LLC}}(\omega_1)| = 3.44$ result, i.e. due to the increased switching frequency, the maximum output power of the DAB converter reduces by a factor of 2.0 and the maximum output power of the LLC converter reduces by a factor of 3.44. Thus, with variable switching frequency, a more effective operation of the LLC converter can be achieved than of the DAB converter; consequently, the achievable efficiency is higher for the LLC converter than for the DAB converter [130].

8.2 Concluding Remarks Regarding Suitable Unidirectional DC–DC Converters (HV → LV)

If solely unidirectional power transfer capability is required, the output switches of the DAB topology (T_5 , T_6 , T_7 , and T_8) could be replaced by diodes in order to reduce the number of gate drivers (phase shifted DC–DC converter, [54]); the modulation schemes discussed in [131] could be used to control the output power (at low power levels, the employed modulation scheme is similar to the triangular current mode modulation scheme presented in Section 3.1.3). However, the RMS currents in the transformer, in the switches, and in the DC capacitors are larger than those of the DAB converter. With the output switches of the DAB converter being replaced by diodes, the achievable power density is less than the power density that can be achieved with the DAB converter [54].

If a variable switching frequency is permitted, a resonant LLC or LCC converter requires a lower variation of the switching frequency than the DAB converter in order to achieve the same change of the output power (Section 8.1). Thus, with variable switching frequency, a higher power density may be achieved for a resonant converter, than for the DAB.

A reduced RMS current through $C_{\text{DC}2}$ is achieved with a DC–DC converter with output inductor. With respect to the specification given in Table 1.4,

¹The parallel inductor L_M , not considered in [129], only causes an increase of the reactive power provided by $v_{\text{AC}2}$ and does not affect the transferred power.

the current doubler converter or the push-pull converter are most promising (cf. Section 8.1 and Appendix D). Due to the volume of the employed DC inductor, however, the achievable power density decreases [39, 132].

8.3 Concluding Remarks Regarding Suitable Unidirectional DC–DC Converters (LV → HV)

If power is solely transferred to the HV port, again a DAB converter or a phase shifted DC–DC converter [54, 131] could be used, whereas a higher power density can be achieved with the DAB converter [54]. Even higher power density may be achieved with a resonant LLC or LCC converter, if a variable switching frequency is permitted.

Again, difficulties due to large capacitor RMS currents occur on the LV side. However, different to Section 8.2, a large capacitor current through C_{DC2} results, if a converter topology with one or more DC inductors on the output side (i.e. on the HV side) is selected. A reduction of the respective capacitor current can be achieved with a topology with one or more DC inductors on the input side. According to the specification given in Table 1.4, either a current doubler converter or a push-pull converter, operated in reverse direction, are considered to be most suitable. Reliable converter operation is either achieved with the modulation scheme presented in Appendix A.5, with a passive snubber, or an active clamping circuit [57, 133, 134, 135].²

8.4 Outlook

Future research on the investigated DAB DC–DC converter may be related to the DAB converter modelling and optimization, the DAB converter hardware, or the dynamic behavior of the DAB converter. Besides, the suitability of the DAB converter as a bidirectional AC–DC converter could be investigated, including a comparison to existing bidirectional AC–DC converters (for AC–DC operation, the AC side full bridge of the DAB needs to be equipped with 4-quadrant switches to allow for the operation with positive and negative voltages at the AC port).

8.4.1 DAB Converter Modelling and Optimization

The loss model presented in Chapter 4 neglects the impact of raised component temperatures on the losses. Thus, in a future step, the discussed

²The modulation scheme presented in Appendix A.5 requires semiconductor switches on the HV side. With a passive snubber or an active clamping circuit, the semiconductor switches on the HV side (i.e. T_1 , T_2 , T_3 , and T_4 in Figure A.38) can be replaced by diodes.

model needs to be extended with a coupled electro-thermal converter model, which allows to cover the effect of raised component temperatures on the efficiency [104, 105].

Future investigation may as well consider a complete converter optimization with respect to maximum power density and /or maximum efficiency, using the suboptimal modulation schemes developed in Section 5.2.2 and the design procedure discussed in Appendix A.2 (i.e. calculation of n and L). Therefore, volume models of all converter components and thermal models of the converter, the HF transformer, the HF inductor L , and the DC capacitor C_{DC2} need to be developed besides the loss model detailed in Chapter 4. In this context, the optimization of the LV side full bridge with respect to low volume needs to be necessarily addressed, since the volume of the currently realized LV side full bridge is large [volume of the LV side full bridge including gate driver circuits and DC filter capacitor: $9.0 \text{ cm} \cdot 9.2 \text{ cm} \cdot 5.3 \text{ cm} = 439 \text{ cm}^3$, volume of the HV side full bridge including gate driver circuits and DC filter capacitor: $9.0 \text{ cm} \cdot 7.5 \text{ cm} \cdot 2.5 \text{ cm} = 169 \text{ cm}^3$]. In doing so, low HF resistances of the PCB, a low HF resistance of the transformer contacts, and low parasitic inductances in series to the semiconductor switches need to be maintained in order to achieve low conduction losses (Section 4.2 and Appendix A.2.3) and low switching losses [cf. (4.7) and Section 4.3.3].

The presented investigation only considers a single DAB converter module. A reduction of the currents in a single converter module would be achieved if multiple modules were used. Moreover, the interleaved operation of multiple converter modules enables a considerable reduction of the DC capacitor currents [136]. Thus, future research may detail the effect of the use of multiple converter modules on the total converter efficiency and /or power density. Furthermore, new possibilities due to the use of multiple converter modules arise and could be analyzed (e.g. at low power operation increased efficiency can be achieved by turning off single modules [137]).

Future research may also address the detailed calculation of the HF losses on the PCB. According to Appendix A.2.3 the switching operations cause spectral components of the currents in the PCB tracks which depend on the position on the PCB: the fundamental frequency component is mainly present at the transformer connection whereas a large DC current and increased harmonic components are observed at the connecting pads of the MOSFETs. Therefore, the accurate calculation of the HF losses on the PCB needs to consider this effect caused by the switching operations.

Furthermore, continuative refinements of the electric DAB model could be investigated, e.g. the impact of non-constant DC voltages V_1 and V_2 on the transformer currents i_{AC1} and i_{AC2} could be considered. One possible solution would be the use of an electric circuit simulator, however, it is difficult to reliably calculate the steady state currents and voltages of the simulated

circuit. Moreover, the calculation time needed for an electric circuit simulation is considerably larger than the calculation time needed to evaluate the simplified model presented in Chapter 3.

8.4.2 Possible Improvements of the DAB Converter Hardware

In future, different steps could be undertaken to improve the hardware prototype designed in Appendix A.2. Suggestions for potential hardware improvements are listed below.

- An evaluation of different transformer concepts could be carried out, e.g. the suitability of different transformer cores with respect to the high current operation and a comparison of the efficiencies and/or power densities achievable with different transformer cores (e.g. planar cores, E-cores) may be analyzed. Furthermore, the impact of the integration of the DAB converter inductance L into the HF transformer on the achievable converter efficiency and/or power density could be investigated.
- The impact of component tolerances on the converter's efficiency and on the reliable converter operation may be analyzed.
- The expected life cycle of the low voltage DC capacitor C_{DC2} needs to be investigated, since C_{DC2} is subject to large RMS currents. Moreover, possible consequences of a device failure need to be considered.
- The design procedure of the EMI filters may be accomplished with respect to a certain optimum, e.g. maximum power density.

8.4.3 Future Research on the Dynamic Behavior of the DAB

The small-signal model derived in Chapter 6 considers constant port voltages V_1 and V_2 and therefore neglects the impact of power components and converters that are connected to the DAB on the dynamic converter behavior. Future investigations may consider this effect, e.g. according to [116]. The implications of component tolerances and timing inaccuracies [e.g. due to a limited time resolution of the gate signals (time resolution of the employed gate signal generation unit is 10 ns) and/or due to strongly non-linear time delays of the MOSFETs] on the dynamic converter behavior form further possibilities regarding future research on the DAB.

Appendices

Appendix A

Converter Design

A.1 Aim of the Converter Design

The objectives of the presented converter design are (in the order of the considered priorities):

1. converter efficiency $> 90\%$ at the nominal operating point ($V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, $P_{\text{out}} = \pm 2 \text{ kW}$),
2. converter efficiency $> 90\%$ within reasonable input and output voltage ranges and reasonable power ranges,
3. low converter volume.

The selectable converter parameters (i.e. n and L for the DAB) are thus calculated in order to guarantee $\eta > 90\%$ at $V_1 = 340 \text{ V}$, $V_2 = 12 \text{ V}$, and $P_{\text{out}} = \pm 2 \text{ kW}$. Furthermore, if possible (e.g. for the DAB), the design process maximizes the average efficiency $\bar{\eta}_{\text{design}}$,

$$\bar{\eta}_{\text{design}} = \frac{1}{36} \sum_{i=1}^3 \sum_{j=1}^3 \sum_{k=1}^4 \left(\eta \Big|_{V_1 = \vec{V}_{1,i}, V_2 = \vec{V}_{2,j}, P_{\text{out}} = \vec{P}_{\text{out},k}} \right), \quad (\text{A.1})$$

that considers 36 different operating points using

$$\vec{V}_1 = (240 \text{ V} \quad 340 \text{ V} \quad 450 \text{ V})^T, \quad (\text{A.2})$$

$$\vec{V}_2 = (11 \text{ V} \quad 12 \text{ V} \quad 16 \text{ V})^T, \quad (\text{A.3})$$

$$\vec{P}_{\text{out}} = (-2 \text{ kW} \quad -1 \text{ kW} \quad 1 \text{ kW} \quad 2 \text{ kW})^T. \quad (\text{A.4})$$

Equation (A.4) is defined in order to consider the operation at different output power levels (rated power and half of the rated power) in either direction of

power transfer. Moreover, with (A.2) and (A.3), the operation with different combinations of DC port voltages V_1 and V_2 is considered in order to evaluate the predicted efficiency at:¹

- the nominal operating point ($V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$),
- the edges of the specified voltage ranges,
- nominal HV port voltage and minimum or maximum LV port voltage ($V_1 = 340\text{ V}$, $V_2 = 11\text{ V}$ and $V_1 = 340\text{ V}$, $V_2 = 16\text{ V}$), and
- nominal LV port voltage and minimum or maximum HV port voltage ($V_1 = 240\text{ V}$, $V_2 = 12\text{ V}$ and $V_1 = 450\text{ V}$, $V_2 = 12\text{ V}$).

Finally, the employed converter components are arranged in a way that a low converter volume is achieved.

A.2 Design of the DAB

The design of the DAB is an iterative process: in a first step, approximate values of the component stress values (i.e. maximum blocking voltages, maximum RMS currents, maximum magnetic flux densities) are calculated with the lossless DAB converter model (Section 3.1). The obtained results enable a first selection of the employed DAB converter components (e.g. semiconductor switches, transformer core). With the lossless converter model, however, an inaccurate efficiency results and thus, the presented DAB loss model (Chapter 4) is used in a second step in order to improve the calculated stress values; thereafter, the DAB converter design is accordingly refined. Due to the changed DAB converter design, however, the parameters employed in the DAB loss model change; thus, the design procedure needs to be repeated until the specified requirements are met.

In order to avoid iterations in the presented documentation, the final DAB loss model is employed in Appendix A.2.1 to determine the DAB converter parameters n and L . Based on the calculated component stress values, the DAB converter components are designed:

- HV side semiconductor switches (Appendix A.2.2),
- LV side semiconductor switches (Appendix A.2.3),
- HF transformer (Appendix A.2.4),

¹If a different evaluation criteria is specified, then (A.1) (A.2), (A.3), and (A.4) need to be modified accordingly; consequently, different values for n and L may result. The converter design procedures discussed in the subsequent sections, however, remain the same.

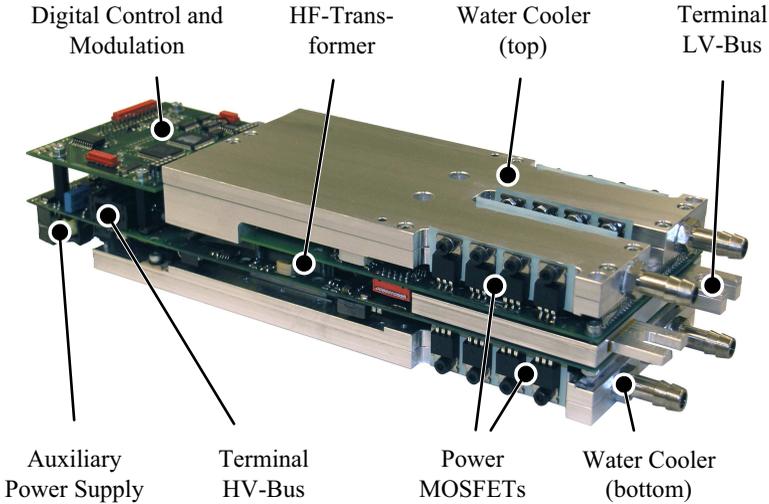


Figure A.1: Picture of the 2kW DAB converter prototype (273 mm × 90 mm × 53 mm).

- DAB converter inductor L (Appendix A.2.5),
- EMI filters (Appendix A.2.6).

Figure A.1 shows a picture of the final DAB hardware prototype: it contains the 2 full bridges (HV side and LV side), the HF transformer, the digital control platforms (DSP: TMS320F2808, FPGA: LCMXO2280), the auxiliary power supplies (HV side and LV side; only the HF transformer of the HV side auxiliary power supply – a flyback converter – is visible in Figure A.1), and 2 water coolers on the top and on the bottom side of the converter.

A.2.1 Calculation of n and L

With the full electric DAB converter model (Section 3.3) and the loss model discussed in Chapter 4 an accurate prediction of the converter efficiency is feasible and thus, the converter parameters n and L can be calculated with respect to maximum average efficiency, $\max(\bar{\eta}_{\text{design}})$, [cf. (A.1)].

Extending the DAB Loss Model for $n \neq 19$

The existing loss model is established for $n = 19$ and is not readily applicable for $n \neq 19$. Still, for $n \neq 19$, most components of the discussed DAB loss model remain unchanged (i.e. conduction losses, switching losses, transformer core losses, and copper losses of the PCB).

Since the predominant part of the converter inductance L is placed on the HV side (cf. Appendix A.2.5), the voltage v_{AC2} , generated by the LV side full bridge, mainly excites the transformer core and generates the peak flux density $B_{tr,peak}$. Therefore, the LV side winding of the HF transformer remains independent of n (i.e. $N_2 = 1$; R_{tr2} remains constant) and the HV winding is adapted: $N_1 = n N_2 = n$. In order to enable a simple calculation of R_{tr1} a constant cross section surface of the HV winding, A_{HV} , and a constant average length of a single turn, l_{single} , are assumed. Thus, R_{tr1} is scaled according to

$$R_{tr1}(N_1) = f_{AC} \rho_{Cu} \frac{N_1 l_{single}}{A_{HV}/N_1} = N_1^2 f_{AC} \rho_{Cu} \frac{l_{single}}{A_{HV}} = N_1^2 \frac{R_{tr1}(19)}{19^2} \quad (A.5)$$

(the implication of N_1 on the AC resistance factor $f_{AC} > 1$ is neglected; cf. Appendix A.2.4).

The parameters L_{HV} , $R_{L_{HV}}$, $V_{L_{HV},core}$, and $N_{L_{HV}}$, used to calculate the inductor conduction and core losses (Section 4.1.2), change with varying n and L . Consequently, separate inductor designs are required for each combination of n and L (Appendix A.9).

Results for n and L

In order to reduce the required calculation time, the DAB converter is designed for a discrete number of turns ratios n_i and inductances L_j (Figure A.2, Figure A.3, Figure A.4):

$$\begin{aligned} \vec{n} &= (11 \ 12 \ 13 \ 14 \ 15 \ 16 \ \dots \ 23 \ 24)^T, \\ \vec{L} &= L_{\max}(n) \cdot (1.0 \ 0.975 \ 0.95 \ 0.925 \ 0.90 \ \dots \ 0.525 \ 0.5)^T. \end{aligned} \quad (A.6)$$

With phase shift modulation, maximum average efficiency, $\max(\bar{\eta}_{\text{design,PS}}) = 89.5\%$, is achieved for $n = 19$ and $L = 26.7 \mu\text{H}$ (Figure A.2). There, the maximum inductor RMS currents are: $I_{L_1} = 15.6 \text{ A}$ and $I_{L_2} = 294 \text{ A}$. On the LV side, capacitor RMS currents of up to 244 A occur (Table A.1).

The achievable maximum average efficiency considerably increases with the extended triangular and trapezoidal current mode modulation schemes being employed (Figure A.3, Section 5.1): for $n = 16$ and $L = 15.5 \mu\text{H}$, $\max(\bar{\eta}_{\text{design,TT}}) = 92.6\%$ is obtained. Compared to phase shift modulation,

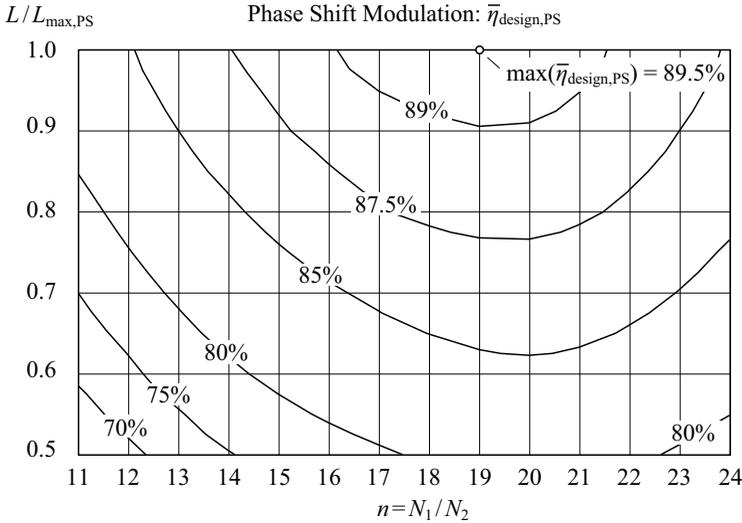


Figure A.2: Average DAB efficiency $\bar{\eta}_{\text{design,PS}}$, calculated with the DAB loss model (Chapter 4), obtained for phase shift modulation and different n and L . L_{max} denotes the maximum possible DAB inductance which allows for the specified output power within the specified voltage ranges. Its value depends on the turns ratio n ; for $n = 19$, $L_{\text{max}} = 26.7 \mu\text{H}$ is calculated.

reduced maximum inductor RMS currents and reduced capacitor RMS currents are achieved, as well (Table A.1). Moreover, the HV side full bridge operates with ZVS within the complete specified operating range.²

The suboptimal modulation schemes (Section 5.2.2) allow for an even higher average efficiency of 93.5% for $n = 16$ and $L = 22.4 \mu\text{H}$ (Figure A.4) and enable a further reduction of the maximum inductor RMS currents (HV side: 15.1 A, LV side: 240 A) and a reduction of the maximum capacitor RMS currents on the LV side (138 A; cf. Table A.1). Again, ZVS operation of the HV side full bridge is achieved within the complete specified operating range.

With optimal modulation parameters (Section 5.2.1) $\max(\bar{\eta}_{\text{design,opt}}) = 93.7\%$ is achieved for $n = 17$ and $L = 21.7 \mu\text{H}$ (Figure A.5). The design with optimal modulation parameters considers a reduced number of turns

²With phase shift modulation, hard switching occurs on the HV side for certain operating points [50], e.g. for $V_1 = 240 \text{ V}$, $V_2 = 16 \text{ V}$, $P_{\text{out}} = 200 \text{ W}$, $n = 19$, $L = 26.7 \mu\text{H}$, and $f_S = 100 \text{ kHz}$.

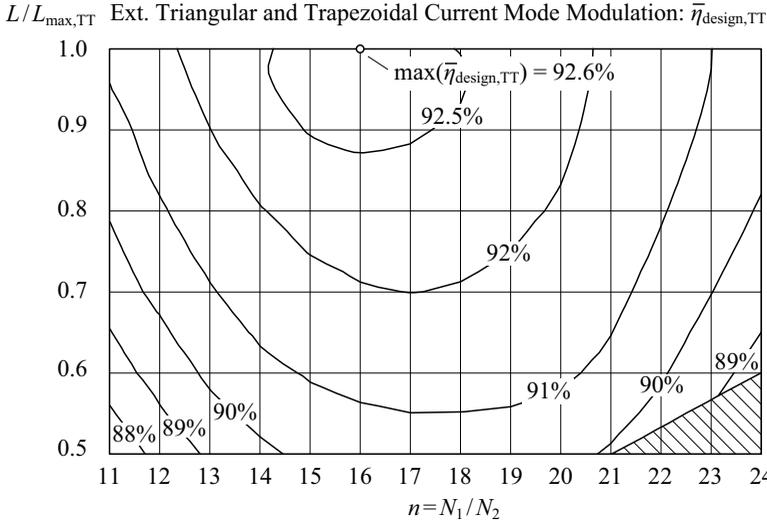


Figure A.3: Average DAB efficiency $\bar{\eta}_{\text{design},TT}$, calculated with the DAB loss model (Chapter 4), obtained for the extended triangular and trapezoidal current mode modulation schemes and different n and L ; L_{\max} denotes the maximum possible DAB inductance which allows for the specified output power within the specified voltage ranges. For $n = 16$, $L_{\max} = 15.5 \mu\text{H}$ is calculated.

ratios and inductance values in order to further reduce the calculation effort:

$$\vec{n} = (14 \ 15 \ 16 \ 17 \ 18 \ 19 \ 20 \ 21 \ 22 \ 23 \ 24)^T, \quad (\text{A.7})$$

$$\vec{L} = L_{\max}(n) \cdot (0.975 \ 0.95 \ 0.925 \ 0.90 \ \dots \ 0.775 \ 0.75)^T.$$

The result depicted in Figure A.5 justifies the step sizes selected for \vec{n} and \vec{L} : around the maximum average efficiency of 93.7% a single step change causes $\bar{\eta}_{\text{design,opt}}$ to change by less than 0.1% [around the maximum, the maximum largest change (0.081%) occurs between $n = 17$ and $n = 18$ in Figure A.5 (a)].

A.2.2 HV Side Full Bridge

On the HV side, a full bridge with a maximum supply voltage of 450 V (Table 1.4) and with a maximum output RMS current of 15.9 A (cf. Table A.1) is needed. In order to enable a high switching frequency and

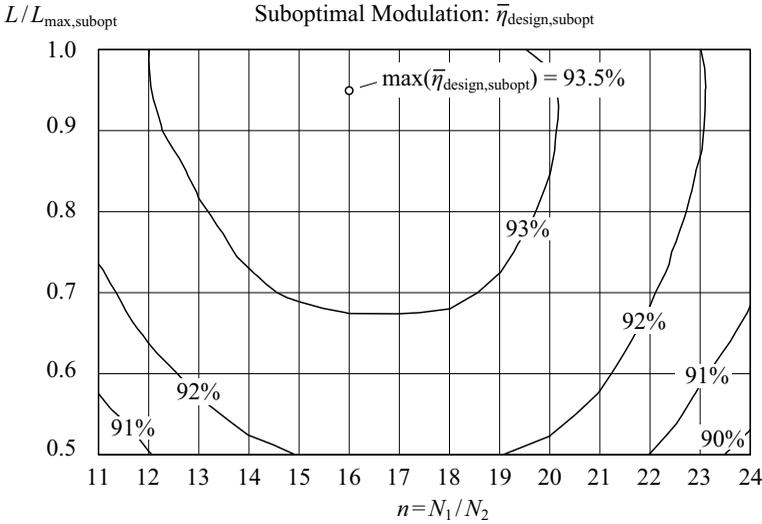


Figure A.4: Average DAB efficiency $\bar{\eta}_{\text{design,subopt}}$, calculated with the DAB loss model (Chapter 4), obtained for the suboptimal modulation schemes and different n and L ; L_{max} denotes the maximum possible DAB inductance which allows for the specified output power within the specified voltage ranges; for $n = 16$, $L_{\text{max}} = 23.6 \mu\text{H}$ is calculated.

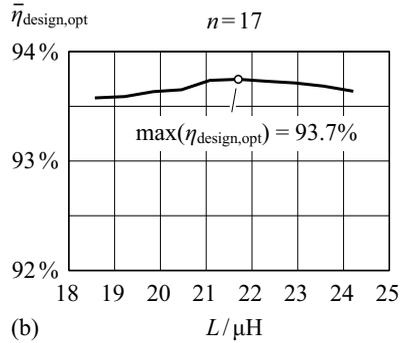
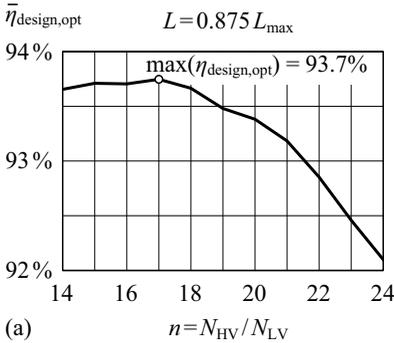


Figure A.5: Average DAB efficiency $\bar{\eta}_{\text{design,opt}}$, calculated with the DAB loss model (Chapter 4), obtained for efficiency optimal modulation parameters D_1 and D_2 and for different n and L ; maximum average converter efficiency of 93.7% is achieved for $n = 17$ and $L = 21.7 \mu\text{H}$.

<i>Property</i>	<i>Phase Shift Mod.</i>	<i>Extended Triang./Trap. Mod.</i>	<i>Suboptimal Mod.</i>	<i>Optimal Mod.</i>
$\max(\bar{\eta}_{\text{design}})$	89.5%	92.6%	93.5%	93.7%
L	26.7 μH	15.5 μH	22.4 μH	21.7 μH
n	19	16	16	17
$\max(V_{\text{DS},1,\text{peak}})$	450 V			
$\max(V_{\text{DS},2,\text{peak}})$	16 V			
$\max(I_{L_1,\text{peak}})$	29.0 A	29.1 A	24.9 A	23.9 A
$\max(I_{L_2,\text{peak}})$	550 A	467 A	399 A	407 A
$\max(I_{L_1})$	15.6 A _{RMS}	15.9 A _{RMS}	15.1 A _{RMS}	13.6 A _{RMS}
$\max(I_{L_2})$	294 A _{RMS}	253 A _{RMS}	240 A _{RMS}	231 A _{RMS}
$\max(I_{C_{f1}})$	14.9 A _{RMS}	8.4 A _{RMS}	12.1 A _{RMS}	9.2 A _{RMS}
$\max(I_{C_{f2}})$	244 A _{RMS}	153 A _{RMS}	138 A _{RMS}	125 A _{RMS}
$\max(B_{\text{tr},\text{peak}})$	142 mT	126 mT	129 mT	130 mT

Table A.1: DAB inductances, transformer turns ratios, and DAB stress values calculated for the different modulation schemes; n and L are selected with respect to maximum $\bar{\eta}_{\text{design}}$ [cf. (A.1)].

simultaneously achieve low losses, the SPW47N60CFD (CoolMOS) has been selected due to its low on-state resistance [cf. (4.5)], fast switching, and the enhanced and robust body diode. With its non-linear characteristic of the parasitic drain-to-source capacitance the proposed device is well suited for converters operating with ZVS.

A.2.3 LV Side Full Bridge

The construction of the LV side full bridge is considerably more challenging than the construction of the HV side full bridge, due to the high RMS values and the high frequency (100 kHz, Table 1.4) of the full bridge output currents.

The DAB hardware prototype therefore employs 2 full bridges which are operated in parallel [Figure A.6 (a)], such that the current rating of a single full bridge is cut into half and thus, a converter realization using printed circuit boards becomes feasible.

In order to achieve good current distribution at high frequencies, the component arrangement depicted in Figure A.7 is employed (considering 4 MOSFETs per switch on a single LV full bridge, cf. “Selecting the LV MOSFETs” on p. 289). There, the low side MOSFETs (T_6 , T_8) are placed on the inside and the high side MOSFETs (T_5 , T_7) on the outside. This arrangement splits the full bridge up into 2 circuits and introduces a second instance of parallelization. The 2 output tracks of the bridge and the solder pads connecting to the transformer are in layers on top of each other in order to achieve a low inductive conduction path to the transformer and a low resistive transformer contact. The current flow paths related to the different switching states of the LV side full bridge are shown in Figure A.8, Figure A.9, Figure A.10, and Figure A.11. Two layers of the PCB are used for the output tracks of the full bridge and one layer forms the minus connection of the LV port. The remaining layer of the PCB (layer 1), however, is needed for the wiring of the gate driver circuits. Therefore, the bus bar used for the plus connection of the LV port (Figure A.7) is used as a fifth layer and forms a solid plane below the PCB.

FEM simulation has been used to determine the current distribution among the MOSFETs for the different switching states of the LV side full bridge shown in Figure A.6 (b). For this purpose a sinusoidal current with a frequency of $f = f_s = 100 \text{ kHz}$ has been employed. The obtained simulation results give a first insight into the current distribution on the PCB, however, the impact of the switching operations on the current distribution is not accounted for: Figure A.12 shows a typical current waveform of the DAB and the related spectrum of the transformer current; Figure A.13 and Figure A.14 show the respective currents in T_5 and T_7 including the related spectra. Obviously, a distinct fundamental frequency component occurs for the transformer current, whereas a DC component and considerably large harmonic components result for the switch currents. Thus, due to the switching operations, different spectra of the PCB currents occur (depending on the position on the PCB), which is not accounted for in the presented approach. Still, the results obtained from the FEM simulations allow for an estimation of the expected current distributions among the MOSFETs, since a distinct fundamental frequency component results due to the fact that each MOSFET conducts for one half-cycle in steady-state operation.

Figure A.15 (a) shows the FEM simulation results of the RMS current distribution for a current with an RMS value of 100 A in the output conductor of the half bridge leg formed by T_5 and T_6 with the switches T_5 and T_8

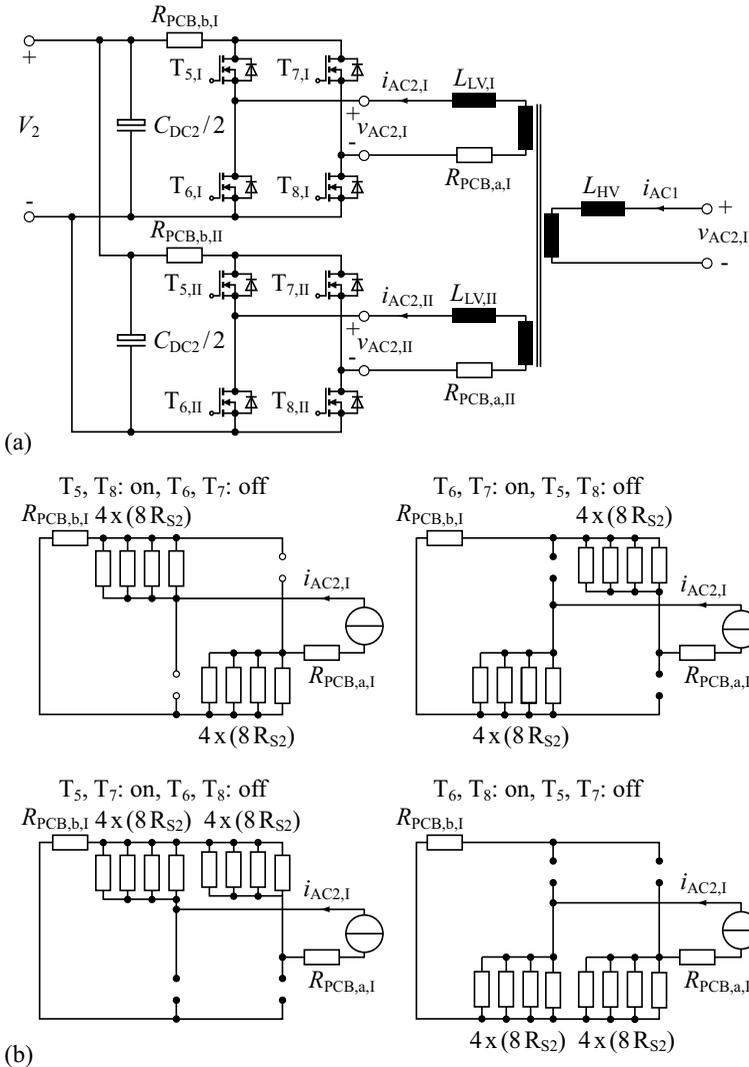


Figure A.6: (a) The final converter prototype employs two full bridges on the LV side, which are operated in parallel; (b) equivalent circuits for the different switching states of a single LV side full bridge, used to determine the current distributions given in Table A.2 using FEM simulations (for high frequency excitations the DC capacitor can be replaced by a shorting bar).

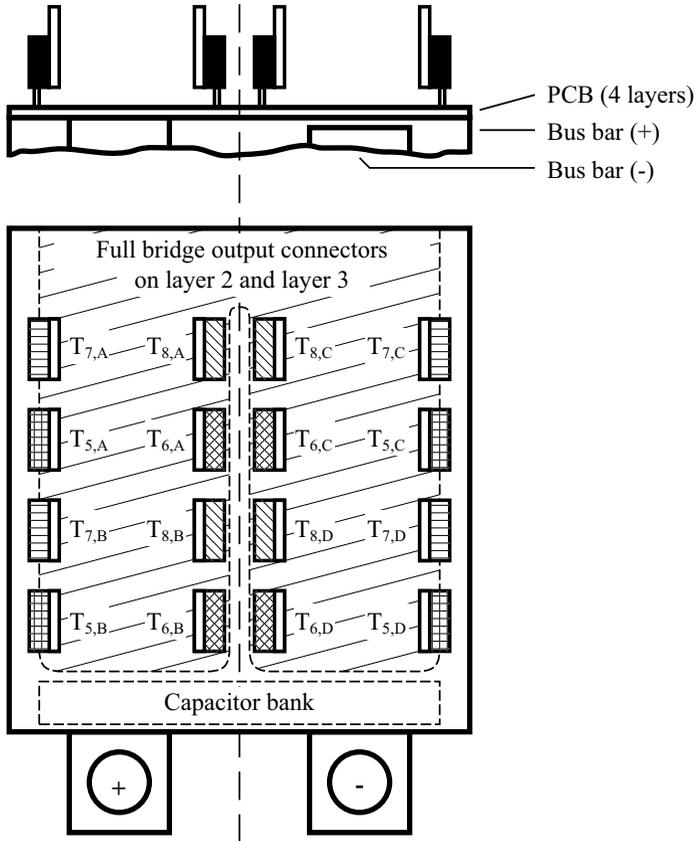


Figure A.7: Proposed arrangement of the power electronic components of a single LV full bridge employing 4 MOSFETs per switch.

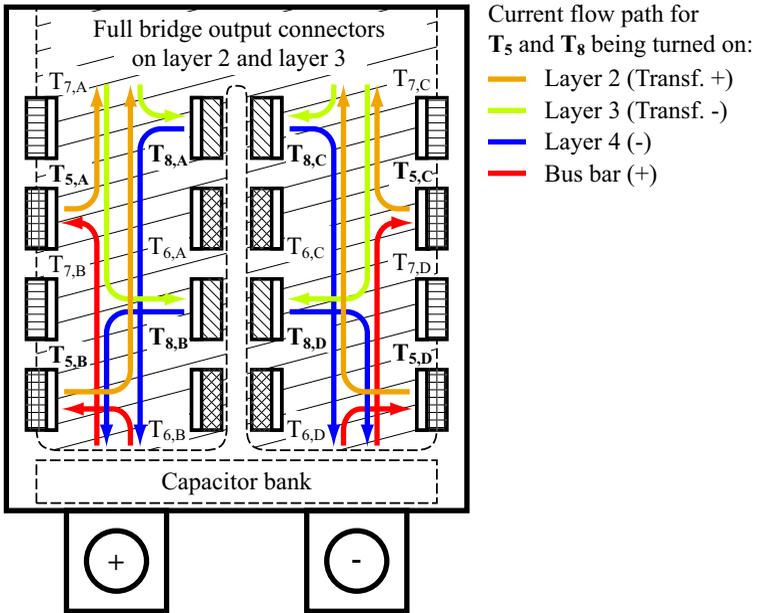


Figure A.8: Current paths in the LV full bridge if T_5 and T_8 are turned on and T_6 and T_7 are turned off.

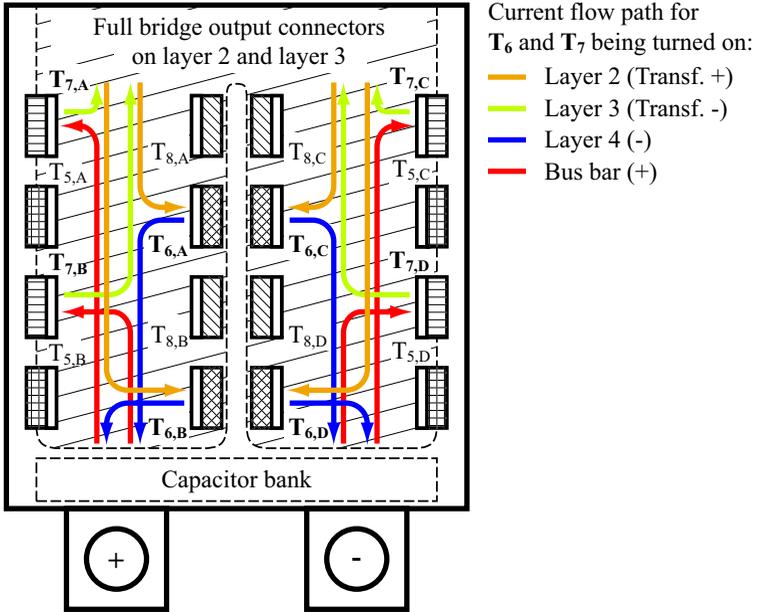


Figure A.9: Current paths in the LV full bridge if T_6 and T_7 are turned on and T_5 and T_8 are turned off.

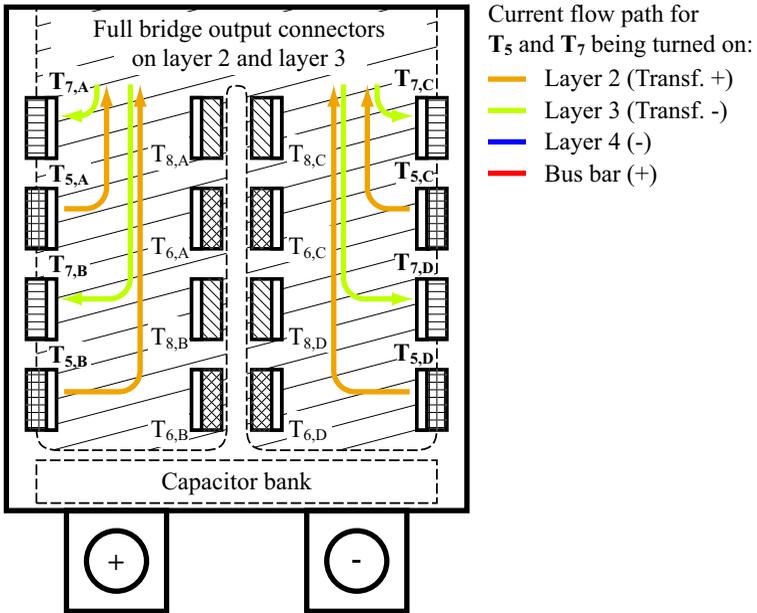


Figure A.10: Current paths in the LV full bridge if T_5 and T_7 are turned on and T_6 and T_8 are turned off.

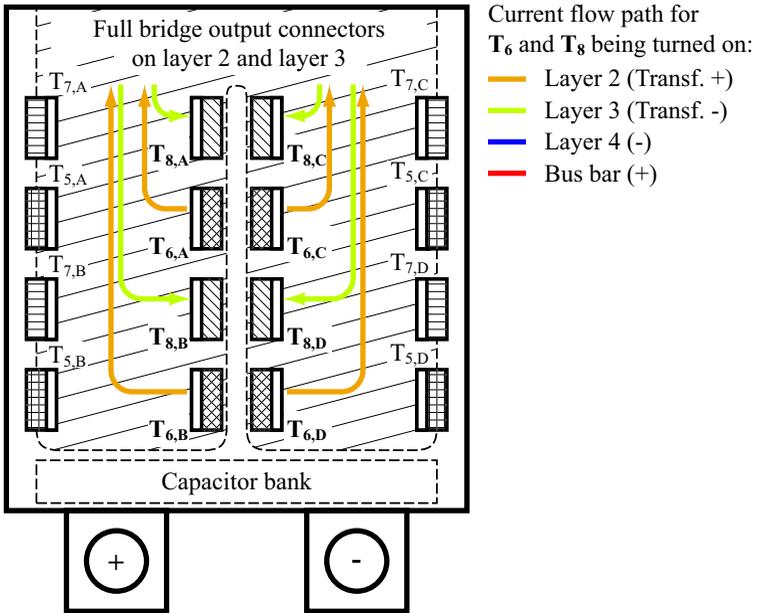


Figure A.11: Current paths in the LV full bridge if T_6 and T_8 are turned on and T_5 and T_7 are turned off.

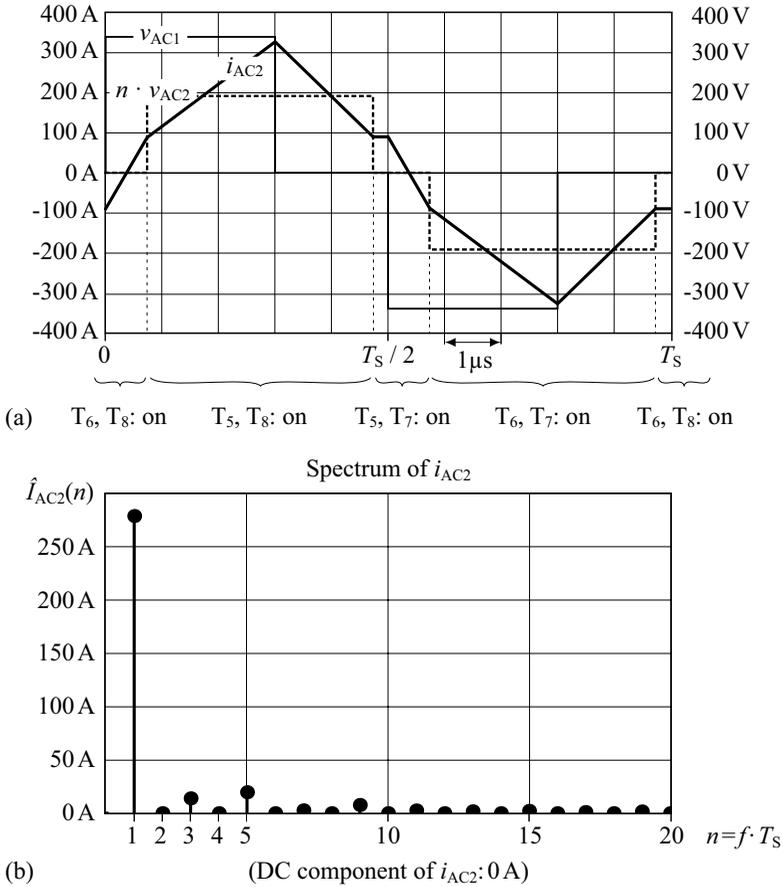


Figure A.12: (a) Current waveform $i_{AC2}(t)$ in the LV side transformer winding of the DAB, calculated for $V_1 = 340$ V, $V_2 = 12$ V, $P_2 = 2$ kW, $D_1 = 0.3$, $D_2 = 0.4$, $L = 22.4$ μ H, and $f_s = 100$ kHz; (b) frequency spectrum calculated for $i_{AC2}(t)$.

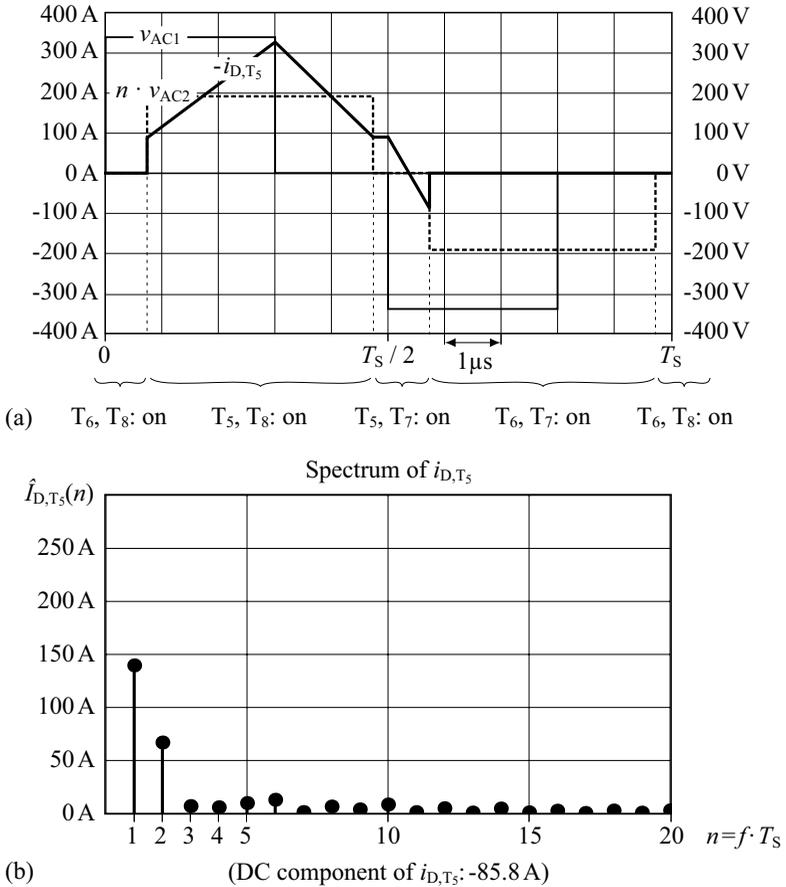


Figure A.13: (a) Waveform of the current through T_5 , calculated for $V_1 = 340$ V, $V_2 = 12$ V, $P_2 = 2$ kW, $D_1 = 0.3$, $D_2 = 0.4$, $L = 22.4$ μ H, and $f_S = 100$ kHz; (b) frequency spectrum calculated for $i_{D,T_5}(t)$.

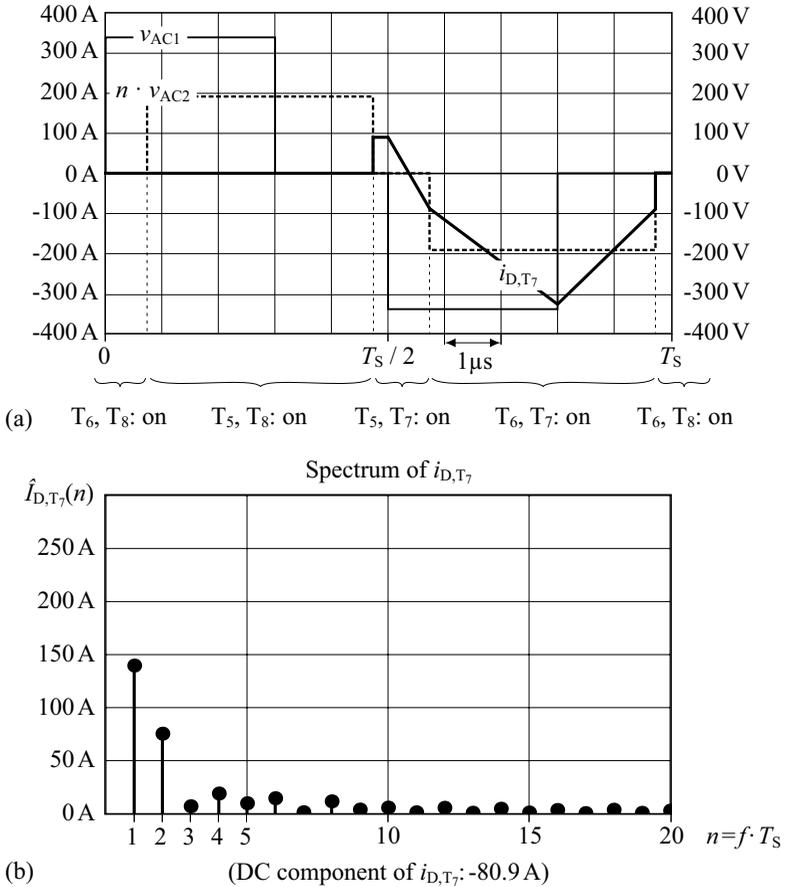


Figure A.14: (a) Waveform of the current through T_7 , calculated for $V_1 = 340$ V, $V_2 = 12$ V, $P_2 = 2$ kW, $D_1 = 0.3$, $D_2 = 0.4$, $L = 22.4$ μ H, and $f_s = 100$ kHz; (b) frequency spectrum calculated for $i_{D,T_7}(t)$.

Results for closed switches T_5 , T_8 and open switches T_6 , T_7 :							
$I_{T_{5,A}}$	$I_{T_{5,B}}$	$I_{T_{5,C}}$	$I_{T_{5,D}}$	$I_{T_{8,A}}$	$I_{T_{8,B}}$	$I_{T_{8,C}}$	$I_{T_{8,C}}$
25.8 A	24.3 A	25.8 A	24.3 A	24.9 A	25.1 A	24.9 A	25.1 A
(+3.0%)	(-3.0%)	(+3.0%)	(-3.0%)	(-0.3%)	(+0.3%)	(-0.3%)	(+0.3%)
Results for closed switches T_6 , T_7 and open switches T_5 , T_8 :							
$I_{T_{6,A}}$	$I_{T_{6,B}}$	$I_{T_{6,C}}$	$I_{T_{6,D}}$	$I_{T_{7,A}}$	$I_{T_{7,B}}$	$I_{T_{7,C}}$	$I_{T_{7,D}}$
26.1 A	24.0 A	26.1 A	24.0 A	24.5 A	25.6 A	24.5 A	25.6 A
(+4.2%)	(-4.2%)	(+4.3%)	(-4.2%)	(-2.2%)	(+2.2%)	(-2.3%)	(+2.3%)
Results for closed switches T_5 , T_7 and open switches T_6 , T_8 :							
$I_{T_{5,A}}$	$I_{T_{5,B}}$	$I_{T_{5,C}}$	$I_{T_{5,D}}$	$I_{T_{7,A}}$	$I_{T_{7,B}}$	$I_{T_{7,C}}$	$I_{T_{7,D}}$
26.3 A	23.7 A	26.3 A	23.7 A	25.1 A	24.9 A	25.1 A	24.9 A
(+5.3%)	(-5.3%)	(+5.3%)	(-5.3%)	(+0.5%)	(-0.5%)	(+0.5%)	(-0.5%)
Results for closed switches T_6 , T_8 and open switches T_5 , T_7 :							
$I_{T_{6,A}}$	$I_{T_{6,B}}$	$I_{T_{6,C}}$	$I_{T_{6,D}}$	$I_{T_{8,A}}$	$I_{T_{8,B}}$	$I_{T_{8,C}}$	$I_{T_{8,C}}$
26.3 A	23.7 A	26.3 A	23.7 A	25.2 A	24.8 A	25.2 A	24.8 A
(+5.3%)	(-5.3%)	(+5.3%)	(-5.3%)	(+0.8%)	(-0.8%)	(+0.8%)	(-0.8%)

Table A.2: MOSFET currents obtained from a FEM simulation of a single LV side full bridge PCB; the percentage values in parentheses denote the respective relative current deviation from the average value. For the presented results, the 4 different situations shown in Figure A.6 (b) are considered. The simulation is carried out with a RMS current of 100 A and $f = 100$ kHz.

being closed and T_6 and T_7 being open. With the proposed PCB layout, a good current distribution among the MOSFETs is achieved: according to Table A.2, the current deviation from the average current value is less than $\pm 6\%$. Furthermore, the transformer termination needs to be designed carefully: for an RMS current of 100 A and with the side-by-side arrangement depicted in Figure A.15 (b), a large hot spot with exceedingly high current densities of more than 100 A/mm^2 (RMS value) occurs. A considerably better current distribution is achieved at the transformer terminations if the respective solder pads are arranged on top of each other [Figure A.15 (a)].

Due to the high current stress, a 4 layer PCB with $200 \mu\text{m}$ copper on each layer is employed to obtain low resistive losses. The copper resistances of one

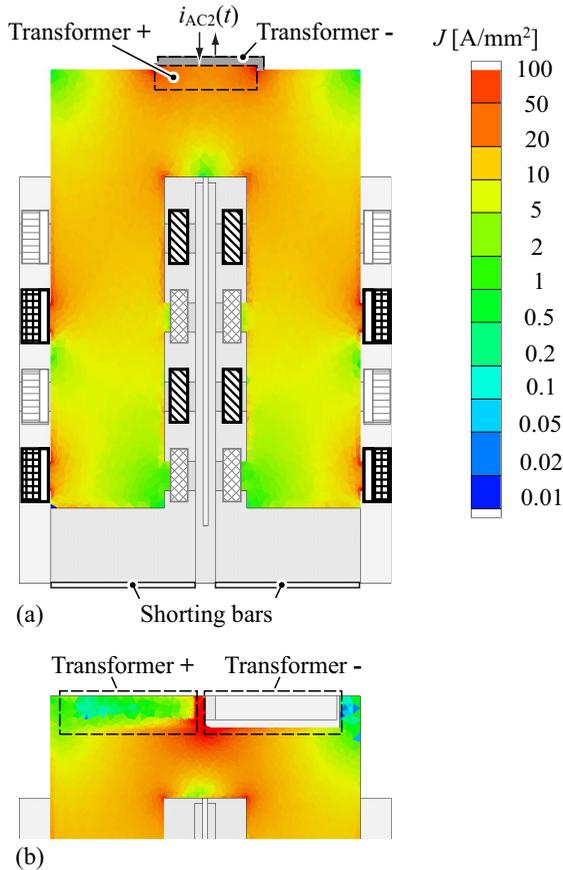


Figure A.15: (a) FEM simulation of the current distribution on a single LV full bridge using an AC RMS current of 100 A with a frequency of 100 kHz (the depicted current densities are RMS values); switches T_5 and T_8 conduct, switches T_6 and T_7 are off [cf. Figure A.6 (b) and Figure A.7]; in (a) the transformer terminations are arranged on top of each other; (b) simulated current distribution at the transformer terminations with a side-by-side arrangement of the respective solder pads: there, a large hot spot with current densities of more than 100 A/mm² occurs.

PCB is measured with an impedance analyzer (cf. Section 4.2 and Figure 4.3):

$$\begin{aligned} 2R_{\text{PCB,a}}(f = 100 \text{ kHz}) &= 520 \mu\Omega, \\ 2R_{\text{PCB,b}}(f = 0) &= 240 \mu\Omega, \\ 2R_{\text{PCB,b}}(f = 200 \text{ kHz}) &= 580 \mu\Omega. \end{aligned} \tag{A.8}$$

Two full bridges are operated in parallel on the LV side. Therefore, the effective resistance values $R_{\text{PCB,a}}$ and $R_{\text{PCB,b}}$ are half of the resistance values given above and the values depicted in Figure 4.3 are half of the resistance values measured for a single PCB.

Large currents also occur in the full bridge filter capacitor C_{f2} , therefore ceramic capacitors have been selected as they are superior to film capacitors with respect to energy density and to electrolytic capacitors with respect to ripple currents [138]. The DC capacitor C_{f2} is formed by the parallel connection of 96 ceramic capacitors, each with a value of $10 \mu\text{F}$, and this keeps the peak-to-peak voltage ripple below $\approx 600 \text{ mV}$. In the case of ideal current distribution, a maximum RMS ripple current of 2.5 A flows through each capacitor which causes less than 25 mW per capacitor (calculated with a dissipation factor of 5%) and is well below the specified maximum RMS value of 6 A [154].

Selecting the LV MOSFETs

On the LV side, the maximum blocking voltage of each switch is 16 V ; however, due to overvoltage spikes during switching (cf. Section 4.3.3), MOSFETs with a rated voltage of 40 V are selected. For the LV side full bridge, the MOSFET IRF2804 is selected due to its low on-state resistance of $2.2 \text{ m}\Omega$. Moreover, each switch on the single LV side full bridge is composed of a certain number of MOSFETs connected in parallel in order to achieve low conduction losses and low switching losses. In order to achieve a symmetric arrangement of the MOSFETs according to Figure A.7, a multiple of 4 MOSFETs needs to be employed. The number of required MOSFETs per switch, N_{IRF2804} , is determined based on the efficiency calculated for different values for N_{IRF2804} . This calculation employs the loss model discussed in Chapter 4 and considers the scaling laws listed below:

- the MOSFET currents are reciprocally proportional to the number of employed MOSFETs;
- the switching losses for a given number of MOSFETs per switch are evaluated based on the measured switching losses (Section 4.3.3) and

scaled according to

$$E_{S2,sw,scaled}(I_{S2,sw}, N_{IRF2804}) = \frac{N_{IRF2804}}{8} E_{S2,sw} \left(\frac{8}{N_{IRF2804}} I_{S2,sw} \right); \quad (\text{A.9})$$

- the leakage inductance of each LV switch (T_5 , T_6 , T_7 , and T_8 in Figure 3.1) is reciprocally proportional to the number of employed MOSFETs per switch; consequently, the durations of the overvoltage spikes discussed in Section 4.3.3 are reciprocally proportional to the number of employed MOSFETs;
- the gate driver power demand scales proportional to the number of employed MOSFETs (Section 4.3.4).

In Figure A.16 and Figure A.17, the efficiencies calculated for $N_{IRF2804} = 4$ and $N_{IRF2804} = 8$ and different MOSFET junction temperatures, T_j , are depicted (for the HV side MOSFETs and for the LV side MOSFETs the same junction temperatures are assumed: $T_{j,HV} = T_{j,LV} = T_j$), whereas optimal transformer and inductor designs are used (i.e. n and L are adapted depending on $N_{IRF2804}$ and T_j). At elevated temperatures, the conduction losses of the MOSFETs increase considerably. Accordingly, with $N_{IRF2804} = 4$ and $T_j = 125^\circ\text{C}$, the efficiency calculated at low port voltages and at rated output power drops below 84% [Figure A.17 (b)]. Thus, $N_{IRF2804} = 8$ is selected in order to maintain a high efficiency of more than 90% at elevated temperatures (e.g. at $T_j = 125^\circ\text{C}$) and within a wide operating range.

A.2.4 Transformer

A planar core (E 58: 58 mm \times 38 mm \times 11 mm)³ is employed for the power transformer, mainly because of its advantageous properties with respect to high power density and excellent electromagnetic and thermal characteristics [105]. Its height (21 mm) is significantly lower than the total height of the converter (50 mm) what leaves space for a surrounding heat sink. For the selected ferrite core (material 3F3) a maximum peak flux density of 142 mT is calculated for phase shift modulation (Table A.1). The large safety margin between 142 mT and the saturation level of more than 300 mT has been selected to achieve low core losses and to prevent transformer saturation, since no DC coupling capacitors are implemented. DC coupling capacitors would show a significant volume, especially on the low voltage side due to the high current ratings.

³Since the ELP 58 core (which was initially considered) was not available, the E 58 core was used, instead. However, the dimensions of the ELP 58 and the E 58 cores are nearly identical, cf. [155, 156].

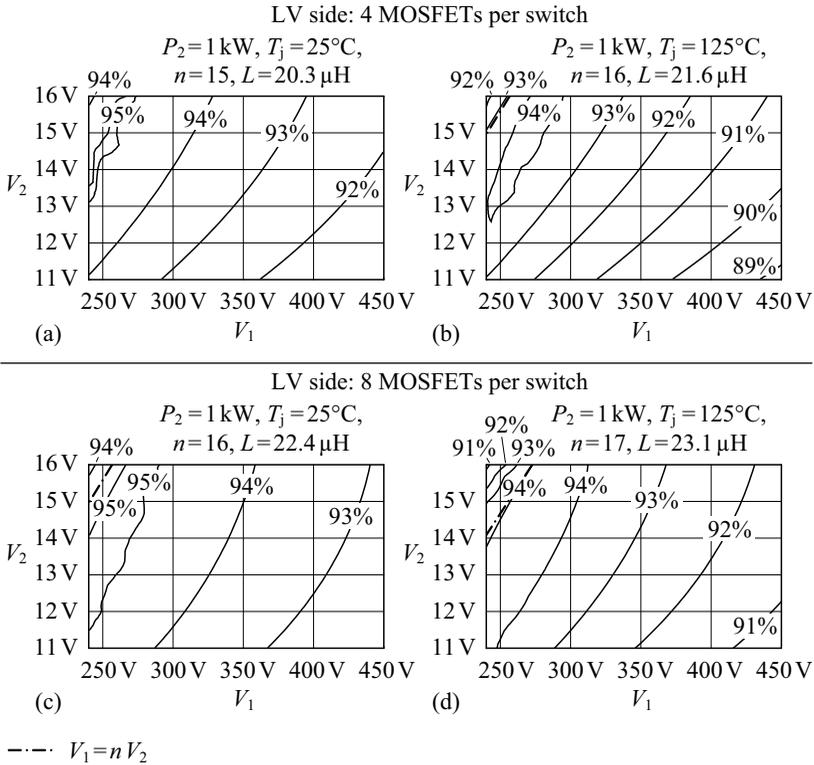


Figure A.16: Calculated efficiencies for an output power of 1 kW, a power transfer from the HV port to the LV port, different junction temperatures T_j (equal T_j is assumed for all MOSFETs), and for different numbers of parallel MOSFETs used per switch on the LV side: (a) $N_{\text{IRF2804}} = 4, T_j = 25^\circ\text{C}$, (b) $N_{\text{IRF2804}} = 4, T_j = 125^\circ\text{C}$, (c) $N_{\text{IRF2804}} = 8, T_j = 25^\circ\text{C}$, (d) $N_{\text{IRF2804}} = 8, T_j = 125^\circ\text{C}$; n and L of each configuration are optimized with respect to maximum average efficiency.

Typically, flat and wide windings are used in planar core transformers to achieve a low AC resistance. Hence, a considerably large parasitic coupling capacitance results between the primary side (HV side) and the secondary side (LV side) of the HF transformer if the transformer comprises of a large number of interleaved HV and LV windings that are placed on top of each other. In order to achieve a small coupling capacitance and a low AC resis-

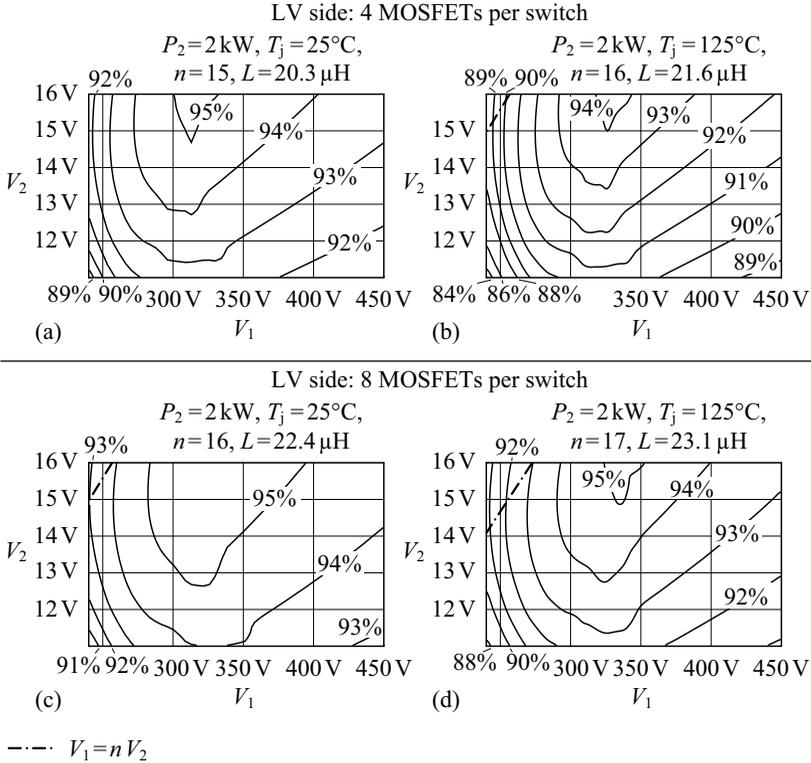


Figure A.17: Calculated efficiencies for an output power of 2 kW, a power transfer from the HV port to the LV port, different junction temperatures T_j (equal T_j is assumed for all MOSFETs), and for different numbers of parallel MOSFETs used per switch on the LV side: (a) $N_{\text{IRF2804}} = 4$, $T_j = 25^\circ\text{C}$, (b) $N_{\text{IRF2804}} = 4$, $T_j = 125^\circ\text{C}$, (c) $N_{\text{IRF2804}} = 8$, $T_j = 25^\circ\text{C}$, (d) $N_{\text{IRF2804}} = 8$, $T_j = 125^\circ\text{C}$; n and L of each configuration are optimized with respect to maximum average efficiency.

tance, litz wire windings and an interleaved winding arrangement with a low number of alternating winding layers are employed: the HV winding with either 16 or 19 turns is placed in the middle and 2 single turn LV windings, which are operated in parallel, are placed above and below the HV winding (Figure A.18). Table A.3 lists the geometric dimensions of the HF transformer core and Table A.4 lists the employed litz wires, which are optimized accord-

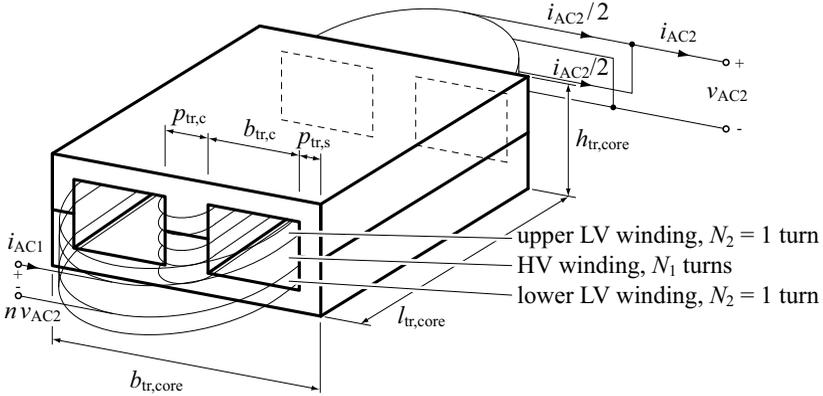


Figure A.18: Planar HF transformer employed for the DAB. The transformer contains 2 windings on the LV side, one above and one below the HV winding, which are operated in parallel. The HV winding is placed in the middle.

ing to [139] in order to achieve a minimum high frequency resistance [140,141].

On the LV side, the winding terminations need to be designed with care in order to avoid high HF losses. The winding terminations depicted in Figure A.19 (a) (i.e. side-by-side arrangements of the wire ends) cause an in-

<i>Property</i>	<i>Value</i>	<i>Description</i>
$b_{tr,core}$	58.4 mm	core width
$h_{tr,core}$	21.1 mm	core height
$l_{tr,core}$	38.1 mm	core depth
$p_{tr,c}$	8.1 mm	width of the inner core leg
$b_{tr,c}$	21.5 mm	width of the window area
$p_{tr,s}$	3.7 mm	width of each outer core leg

Table A.3: Dimensions of the HF transformer core ELP 58 (according to Figure A.18, [155]).

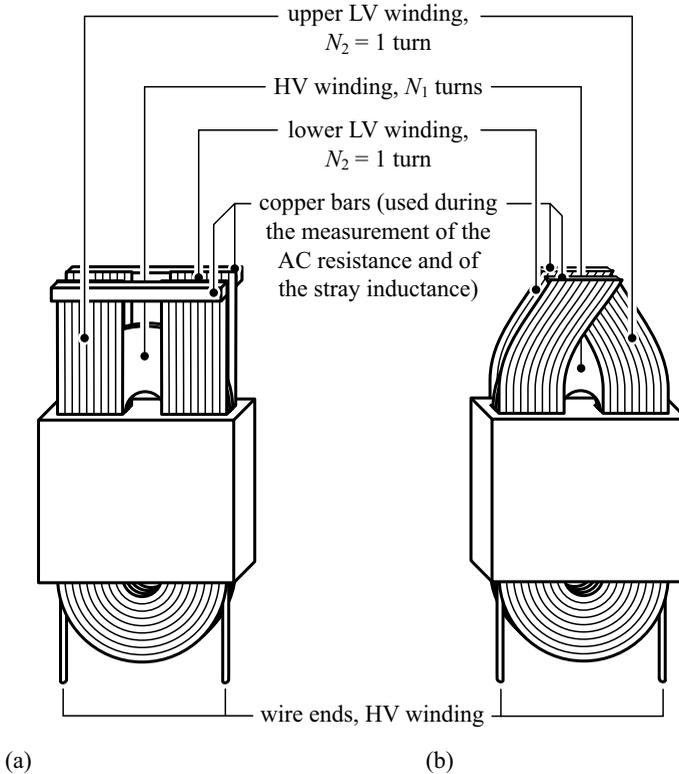


Figure A.19: (a) Side-by-side arrangement of the LV side transformer winding termination; (b) LV side winding ends being placed on top of each other (the HF transformer employs 2 windings on the LV side, which are operated in parallel). The shown copper bars are used to short circuit the LV port of the transformer in order to enable the measurement of the stray inductance and the AC resistance of the winding; the copper bars are removed once the measurement is done. According to the measurement results depicted in Figure A.20, the total AC resistance, $R_{tr1} + n^2 R_{tr2}$, achieved with arrangement (b) is 26% less than the AC resistance achieved with (a).

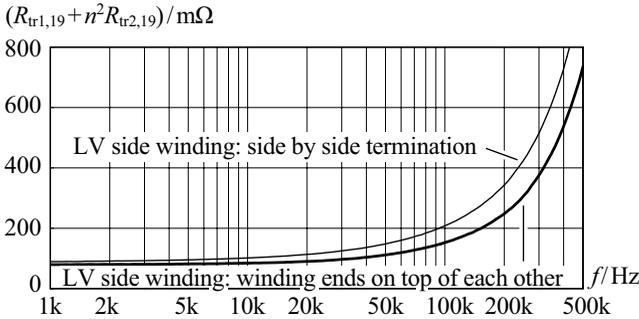


Figure A.20: Measured HV side referred AC resistance, $R_{tr1,19} + n^2 R_{tr2,19}$, of the HF transformer with $n = 19$ and the 2 winding terminations depicted in Figure A.19 (using the transformer model depicted in Figure 3.29). At $f = 100$ kHz, a total AC resistance of either 208 mΩ (side-by-side arrangement) or 153 mΩ (winding ends on top of each other) is measured. The measurement is accomplished using the Agilent 4294A Precision Impedance Analyzer. At $f = 100$ kHz, the accuracies of the Impedance Analyzer are $\pm 3.8\%$ for $R_{tr1,19} + n^2 R_{tr2,19} = 208$ mΩ and $\pm 4.1\%$ for $R_{tr1,19} + n^2 R_{tr2,19} = 153$ mΩ (calculated according to [152]).

crease of the total stray inductance [142] and generate additional HF losses (cf. Appendix A.2.3). Figure A.20 depicts the measured HV side referred copper resistance of the HF transformer with $n = 19$, using the side-by-side arrangements shown in Figure A.19 (a) and 2 shorting bars being soldered to the wire ends of the 2 transformer windings on the LV side: at $f = 100$ kHz, a total AC resistance of 208 mΩ results.

<i>Winding</i>	<i>Employed Litz Wire</i>
LV windings	9 parallel connected litz wires: 245 strands, single strand copper diameter: 0.1 mm
HV winding, $n = 16$	parallel connected litz wires: 245×0.1 mm and 120×0.071 mm
HV winding, $n = 19$	245×0.1 mm

Table A.4: Litz wires employed for the HF transformer windings.

The HF resistances of the transformer terminations clearly decrease if the winding terminations are placed on top of each other [Figure A.19 (b), Figure A.20]: the total HV side referred copper resistance is now 153 m Ω (at $f = 100$ kHz), i.e. 26% less than the AC resistance measured for the side-by-side arrangement.

Furthermore, for the transformer with $n = 19$, a total HV side referred stray inductance of 7.9 μ H, a magnetizing inductance of 2.7 mH and a parasitic coupling capacitance of 65 pF between HV side and LV side are measured at 100 kHz (Figure A.21 and Figure A.22). For $n = 16$ and $f = 100$ kHz, the measured total HV side referred copper resistance is 110 m Ω , the total stray inductance is 5.0 μ H, the magnetizing inductance is 1.9 mH, and the coupling capacitance between HV side and LV side is 69 pF (Figure A.23 and Figure A.24).

The measurement results presented in Figure A.21 and Figure A.23 depict the total stray inductances $L_{\text{tr}1} + n^2 L_{\text{tr}2}$ and the total AC resistances $R_{\text{tr}1} + n^2 R_{\text{tr}2}$. For the employed transformer model (Figure 3.29 in Section 3.3), however, distinct values are required for $L_{\text{tr}1}$, $L_{\text{tr}2}$, $R_{\text{tr}1}$, and $R_{\text{tr}2}$.

The inductances $L_{\text{tr}1}$ and $L_{\text{tr}2}$ are determined from the measurement results (Figure A.21 and Figure A.23) at $f = 100$ kHz and based on the assumption that the magnetic energy stored in the transformer stray inductance is equally shared by the LV side winding and the HV side winding, i.e. $L_{\text{tr}1} \approx n^2 L_{\text{tr}2}$. The respective results for $L_{\text{tr}1}$ and $L_{\text{tr}2}$ are listed in Table A.9.

The resistances $R_{\text{tr}1}$ and $R_{\text{tr}2}$ are determined from the measurement results, too; there, however, the AC resistance $R_{\text{tr}1}$ is calculated according to Appendix A.9.4; $R_{\text{tr}2}$ is then obtained from (A.17). Due to the essentially different characteristics of the magnetic field lines inside the conductors for the part of the winding which is surrounded by the transformer core and for the transformer's end turns, the calculation of $R_{\text{tr}1}$ distinguishes between these 2 parts.

For the winding portion which is surrounded by the transformer core, the respective AC resistance of the i -th turn, $R_{\text{tr}1,\text{inside},i}$, is calculated according to Appendix A.9.4 and [38]:

$$R_{\text{tr}1,\text{inside},i} = R_{\text{tr}1,\text{inside},\text{DC}} \cdot \left(F_{\text{R}} + \frac{4G_{\text{R}}n_{\text{strands}}^2}{\pi d_{\text{tl}}^2} \underbrace{\int_0^{d_{\text{tl}}/2} \int_0^{2\pi} |\vec{H}_i(r, \varphi)|^2 r d\varphi dr}_{\substack{\text{obtained from FEM simulation,} \\ \text{Table A.5 and Table A.6}}} \right) \quad (\text{A.10})$$

[$R_{\text{tr}1,\text{inside},\text{DC}}$ is calculated with (A.12); d_{tl} denotes the total diameter of

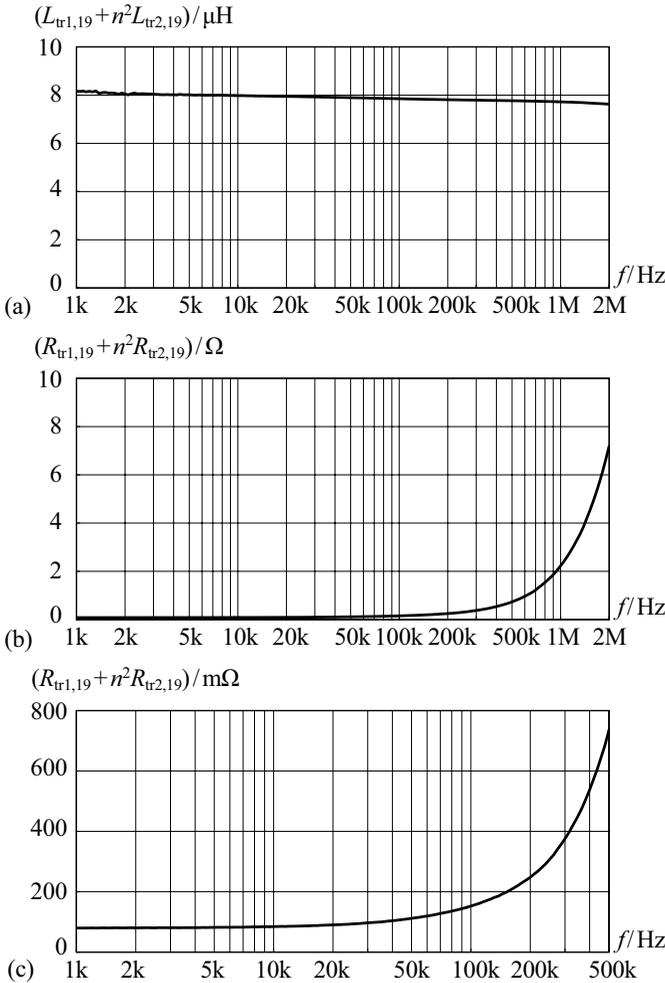


Figure A.21: (a) Measured HV side referred total stray inductance of the HF transformer with $n = 19$ (cf. Figure 3.29); (b) and (c) measured HV side referred AC resistance. In order to obtain the depicted measurement results, the LV winding of the transformer is shorted and thus, the implication of the transformer magnetizing inductance (2.7 mH at 100 kHz) on $L_{tr2,19}$ and $R_{tr2,19}$ is neglected. The measurement is accomplished using the Agilent 4294A Precision Impedance Analyzer. At $f = 100$ kHz, the accuracies of the Impedance Analyzer are $\pm 0.13\%$ for $L_{tr1,19} + n^2 L_{tr2,19}$ and $\pm 4.1\%$ for $R_{tr1,19} + n^2 R_{tr2,19}$ (calculated according to [152]).

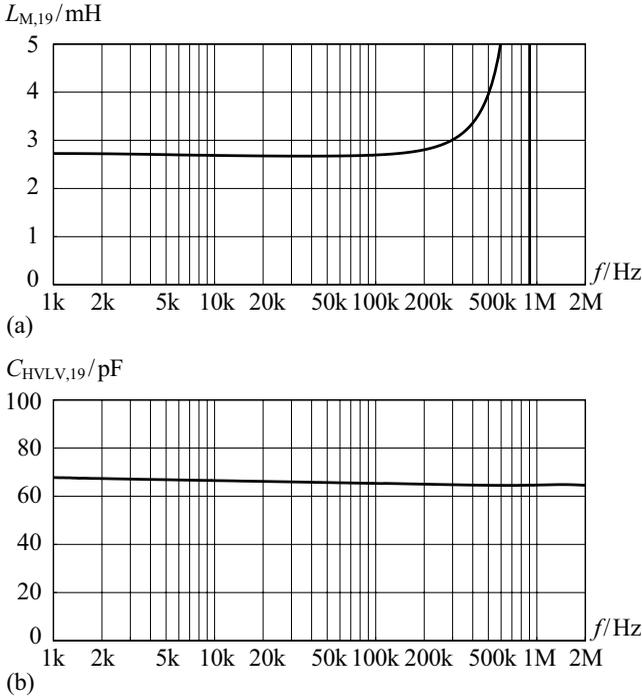


Figure A.22: (a) Measured magnetizing inductance, $L_{M,19}$ of the HF transformer with $n = 19$; at $f = 900$ kHz a parallel resonance occurs ($L_{M,19} = 2.7 \mu\text{H}$ in parallel to a capacitance of 11.6 pF); (b) coupling capacitance between the HV side and the LV side of the HF transformer for $n = 19$. The measurement is accomplished using the Agilent 4294A Precision Impedance Analyzer. At $f = 100$ kHz, the accuracies of the Impedance Analyzer are $\pm 0.1\%$ for $L_{M,19}$ and $\pm 0.1\%$ for $C_{HVLV,19}$ (calculated according to [152]).

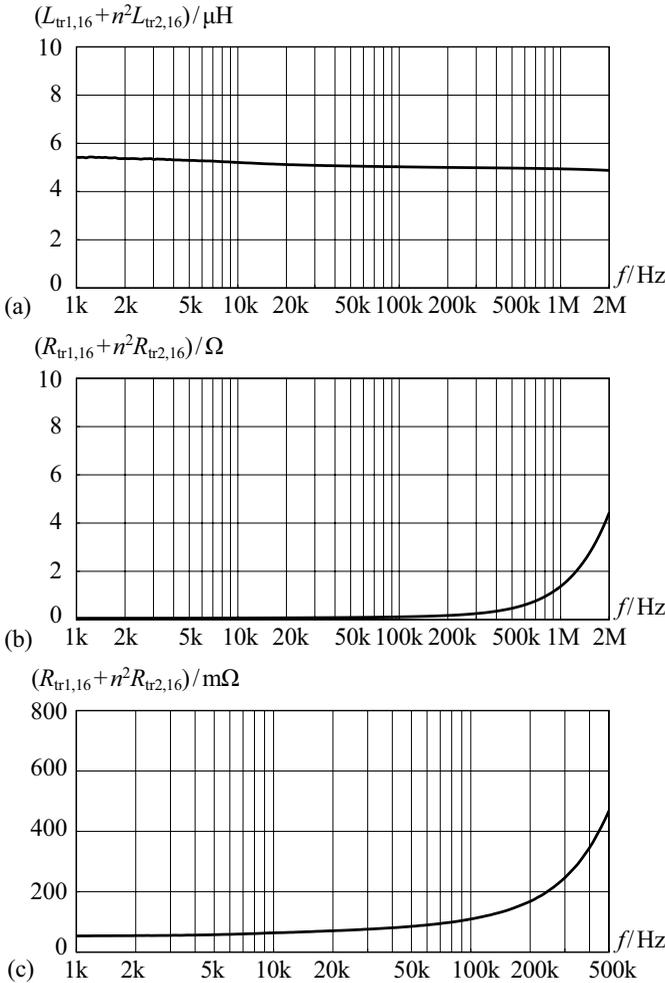


Figure A.23: (a) Measured HV side referred total stray inductance of the HF transformer with $n = 16$ (cf. Figure 3.29); (b) and (c) measured HV side referred AC resistance. In order to obtain the depicted measurement results in (a), (b), and (c), the LV winding of the transformer is shorted and thus, the implication of the transformer magnetizing inductance (1.9 mH at 100 kHz) on $L_{tr2,16}$ and $R_{tr2,16}$ is neglected. The measurement is accomplished using the Agilent 4294A Precision Impedance Analyzer. At $f = 100$ kHz, the accuracies of the Impedance Analyzer are $\pm 0.15\%$ for $L_{tr1,16} + n^2 L_{tr2,16}$ and $\pm 4.4\%$ for $R_{tr1,16} + n^2 R_{tr2,16}$ (calculated according to [152]).

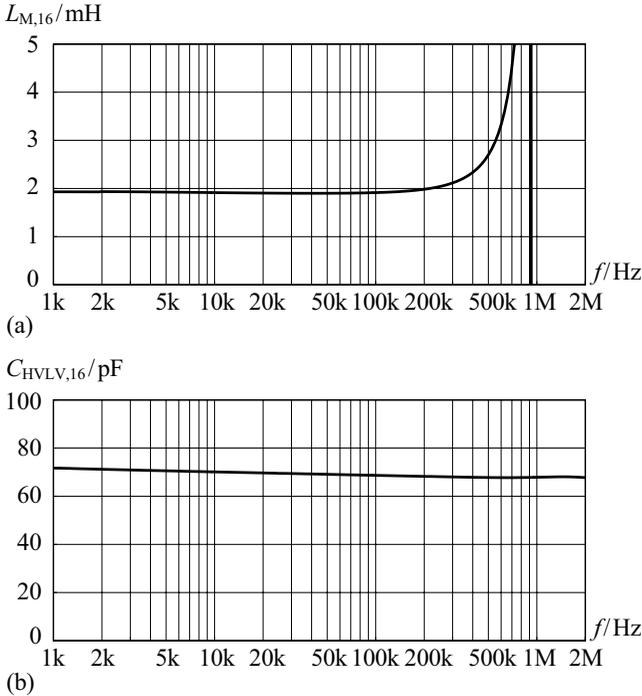


Figure A.24: (a) Measured magnetizing inductance, $L_{M,16}$ of the HF transformer with $n = 16$; at $f = 920$ kHz a parallel resonance occurs ($L_{M,19} = 1.9 \mu\text{H}$ in parallel to a capacitance of 15.8 pF); (b) coupling capacitance between the HV side and the LV side of the HF transformer for $n = 16$. The measurement is accomplished using the Agilent 4294A Precision Impedance Analyzer. At $f = 100$ kHz, the accuracies of the Impedance Analyzer are $\pm 0.1\%$ for $L_{M,16}$ and $\pm 0.1\%$ for $C_{HVLV,16}$ (calculated according to [152]).

the litz wire, calculated with (A.178); n_{strands} denotes the number of single strands]. FEM simulation is used to calculate $\int_0^{d_{t1}/2} \int_0^{2\pi} |\vec{H}_i(r, \varphi)|^2 r d\varphi dr$ (Table A.5, Table A.6).

The AC resistance of the i -th turn of the end turns is also calculated using FEM simulation results [Figure A.25 (a)]:

$$R_{\text{tr1, outside}, i} = R_{\text{tr1, outside}, \text{DC}, i} \cdot \left(F_{\text{R}} + \frac{4G_{\text{R}}n_{\text{strands}}^2}{\pi d_{t1}^2} \underbrace{\int_0^{d_{t1}/2} \int_0^{2\pi} |\vec{H}_i(r, \varphi)|^2 r d\varphi dr}_{\substack{\text{obtained from FEM simulation,} \\ \text{Table A.7 and Table A.8}}} \right) \quad (\text{A.11})$$

[$R_{\text{tr1, outside}, \text{DC}, i}$ is calculated with (A.13)]. The additional resistance increase due to the winding termination is neglected on the HV side.

With the DC resistances of the employed litz wires,

$$R_{\text{tr1, inside}, \text{DC}} = \frac{4 l_{\text{tr1, inside}}}{\sigma_{\text{Cu}} n_{\text{strands}} \pi d_{\text{c}}^2}, \quad (\text{A.12})$$

$$R_{\text{tr1, outside}, \text{DC}, i} = \frac{4 l_{\text{tr1, outside}, i}}{\sigma_{\text{Cu}} n_{\text{strands}} \pi d_{\text{c}}^2}, \quad (\text{A.13})$$

the particular wire lengths (cf. Figure A.18, Table A.7, Table A.8),

$$l_{\text{tr1, inside}} = 2l_{\text{tr, core}} = 2 \cdot 38.1 \text{ mm} = 76.2 \text{ mm}, \quad (\text{A.14})$$

$$l_{\text{tr1, outside}} = d_{\text{tr1}, i} \cdot \pi, \quad (\text{A.15})$$

and the equations (A.10) and (A.11), the total AC resistance R_{tr1} can be calculated:⁴

$$R_{\text{tr1}} = \sum_{i=1}^{N_1} (R_{\text{tr1, inside}, i} + R_{\text{tr1, outside}, i}). \quad (\text{A.16})$$

The remaining winding resistance is attributed to the LV side:

$$R_{\text{tr2}} = \frac{1}{n^2} \left(\underbrace{(R_{\text{tr1}} + n^2 R_{\text{tr2}})}_{\substack{\text{measured value,} \\ \text{e.g. from Figure A.21}}} - R_{\text{tr1}} \right). \quad (\text{A.17})$$

⁴In order to simplify the calculations, the 2 litz wires employed for the HF transformer with $n = 16$ are combined to a single litz wire with a single strand copper diameter of 0.1 mm. The number of strands is adjusted such that the total copper cross section area remains the same, i.e. $n_{\text{strands}} = 305$.

$n = 19, d_{t1} = 2.3 \text{ mm}$					
<i>Conductor Number:</i>	1	2	3	4	5
$\int_0^{d_{t1}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	37.8 A ²	16.1 A ²	12.7 A ²	52.2 A ²	50.6 A ²
<i>Conductor Number:</i>	6	7	8	9	10
$\int_0^{d_{t1}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	15.2 A ²	14.5 A ²	54.2 A ²	52.3 A ²	15.8 A ²
<i>Conductor Number:</i>	11	12	13	14	15
$\int_0^{d_{t1}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	15.2 A ²	55.2 A ²	51.7 A ²	17.3 A ²	15.3 A ²
<i>Conductor Number:</i>	16	17	18	19	
$\int_0^{d_{t1}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	57.1 A ²	43.8 A ²	24.7 A ²	13.8 A ²	

Table A.5: FEM simulator results for $\int_0^{d_{t1}/2} \int_0^{2\pi} |\vec{H}_i(r, \varphi)|^2 r d\varphi dr$ obtained for the winding portion inside the core [i -th turn of the HF transformer with $n = 19$, cf. Figure A.25 (b)].

$n = 16, d_{t1} = 2.6 \text{ mm}$					
<i>Conductor Number:</i>	1	2	3	4	5
$\int_0^{d_{t1}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	32.7 A ²	32.7 A ²	37.1 A ²	37.1 A ²	38.2 A ²
<i>Conductor Number:</i>	6	7	8	9	10
$\int_0^{d_{t1}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	38.2 A ²	38.5 A ²	38.5 A ²	38.5 A ²	38.5 A ²
<i>Conductor Number:</i>	11	12	13	14	15
$\int_0^{d_{t1}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	38.2 A ²	38.2 A ²	37.1 A ²	37.1 A ²	32.7 A ²
<i>Conductor Number:</i>	16				
$\int_0^{d_{t1}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	32.7 A ²				

Table A.6: FEM simulator results for $\int_0^{d_{t1}/2} \int_0^{2\pi} |\vec{H}_i(r, \varphi)|^2 r d\varphi dr$ obtained for the winding portion inside the core [i -th turn of the HF transformer with $n = 16$, cf. Figure A.25 (b)].

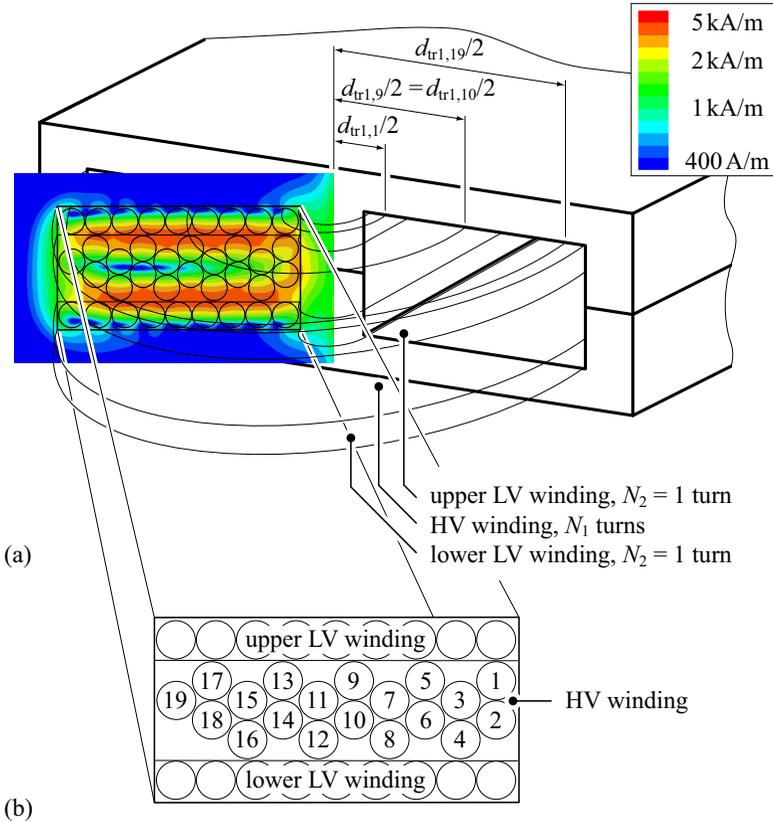


Figure A.25: (a) FEM simulation of the magnetic field (RMS value) generated by the transformer end turns ($N_1 = 19$, $N_2 = 1$). For the depicted field plot, $I_{AC1} = 10.5$ A, $I_{AC2} = 200$ A, and $f = 100$ kHz are selected. This Figure also shows the 4 radiuses $d_{tr1,1/2}$, $d_{tr1,9/2}$, $d_{tr1,10/2}$, and $d_{tr1,19/2}$ of the first, the ninth, the tenth, and the 19th end turn to illustrate the calculation of $d_{tr1,i}$; $d_{tr1,i}$ is needed to calculate the DC resistances $R_{tr1,outside,DC,i}$ [cf. (A.13) and (A.15)]. (b) Numbering used for the turns of the HV winding.

Table A.9 lists the component values of the equivalent transformer circuit depicted in Figure 3.29 (however, in order to improve the model accuracy, the transformer stray inductance determined for the fully assembled converter setup is used to obtain L_{tr1} and L_{tr2} , cf. Appendix A.2.5 and Table A.10).

$n = 19, d_{tl} = 2.3 \text{ mm}$					
<i>Conductor Number:</i>	1	2	3	4	5
$\int_0^{d_{ii}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	45.7 A ²	43.8 A ²	26.4 A ²	51.6 A ²	51.0 A ²
$d_{tr1,i}$	11.2 mm	11.2 mm	15.4 mm	15.4 mm	19.5 mm
<i>Conductor Number:</i>	6	7	8	9	10
$\int_0^{d_{ii}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	21.1 A ²	17.9 A ²	51.7 A ²	50.2 A ²	16.3 A ²
$d_{tr1,i}$	19.5 mm	23.7 mm	23.7 mm	27.9 mm	27.9 mm
<i>Conductor Number:</i>	11	12	13	14	15
$\int_0^{d_{ii}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	14.5 A ²	50.5 A ²	47.1 A ²	14.2 A ²	11.9 A ²
$d_{tr1,i}$	32.1 mm	32.1 mm	36.2 mm	36.2 mm	40.4 mm
<i>Conductor Number:</i>	16	17	18	19	
$\int_0^{d_{ii}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	47.4 A ²	36.2 A ²	18.3 A ²	14.2 A ²	
$d_{tr1,i}$	40.4 mm	44.6 mm	44.6 mm	48.7 mm	

Table A.7: FEM simulator results for $\int_0^{d_{ii}/2} \int_0^{2\pi} |\vec{H}_i(r, \varphi)|^2 r d\varphi dr$ and the respective diameters $d_{tr1,i}$ obtained for the i -th winding of the end turns of the HF transformer with $n = 19$.

A.2.5 Inductor

The converter inductor L can be placed in series to the LV side and/or the HV side of the HF transformer without affecting the converter functionality. For the given converter specifications it is easier to place the inductor on the HV side due to the lower current rating, despite the larger inductance value required.

Since the transformer stray inductances (L_{tr1} , L_{tr2}) and the LV side stray inductances of MOSFETs and PCB (L_{LV}) contribute to L , reduced additional inductance values L_{HV} are needed for the DAB, depending on the employed modulation scheme. The total stray inductance, $L_{\sigma} = L_{tr1} + n^2(L_{tr2} + L_{LV})$, is measured on the final DAB hardware prototype in order to correctly determine the additionally required inductance L_{HV} . Therefore, the HV side transformer winding is shorted and the LV side full bridge generates rectan-

$n = 16, d_{tl} = 2.6 \text{ mm}$					
Conductor Number:	1	2	3	4	5
$\int_0^{d_{ti}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	42.6 A^2	42.6 A^2	39.4 A^2	39.4 A^2	38.5 A^2
$d_{tr1,i}$	11.5 mm	11.5 mm	16.8 mm	16.8 mm	22.1 mm
Conductor Number:	6	7	8	9	10
$\int_0^{d_{ti}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	38.5 A^2	37.8 A^2	37.8 A^2	36.9 A^2	36.9 A^2
$d_{tr1,i}$	22.1 mm	27.4 mm	27.4 mm	6 mm	32.6 mm
Conductor Number:	11	12	13	14	15
$\int_0^{d_{ti}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	35.4 A^2	35.4 A^2	31.7 A^2	31.7 A^2	24.0 A^2
$d_{tr1,i}$	37.9 mm	37.9 mm	43.2 mm	43.2 mm	48.5 mm
Conductor Number:	16				
$\int_0^{d_{ti}/2} \int_0^{2\pi} \vec{H}_i(r, \varphi) ^2 r d\varphi dr$	24.0 A^2				
$d_{tr1,i}$	48.5 mm				

Table A.8: FEM simulator results for $\int_0^{d_{ti}/2} \int_0^{2\pi} |\vec{H}_i(r, \varphi)|^2 r d\varphi dr$ and the respective diameters $d_{tr1,i}$ obtained for the i -th winding of the end turns of the HF transformer with $n = 16$.

n	L_{tr1}	L_{tr2}	L_M	R_{tr1}	R_{tr2}	R_M
16	2.1 μH	8.0 nH	1.9 mH	27 m Ω	83 $\mu\Omega$	∞
19	3.3 μH	9.1 nH	2.7 mH	39 m Ω	114 $\mu\Omega$	∞

Table A.9: Parasitic transformer component values ($f = f_S = 100 \text{ kHz}$) employed for the detailed DAB converter model (Section 3.3: Figure 3.29, Figure 3.30). The resistance values R_{tr1} and R_{tr2} are calculated with (A.16) and (A.17), the stray inductances are obtained from Table A.10 and on the assumption $L_{tr1} = n^2 L_{tr2}$, and L_M is measured (Figure A.22 and Figure A.24).

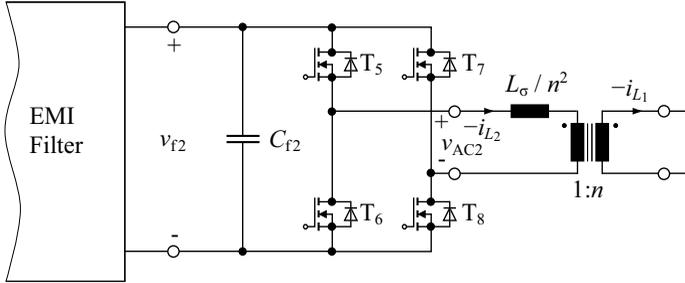


Figure A.26: Measurement setup used to determine the stray inductance L_σ : the LV side full bridge generates a rectangular voltage v_{AC2} with a duty cycle D_2 according to Figure 3.3, which causes a linear change of the currents i_{L_2} and i_{L_1} ; the inductance L_σ is determined according to (A.18).

gular voltage pulses (Figure A.26), which excite linearly changing inductor currents i_{L_1} and i_{L_2} . On the assumption of a negligible transformer magnetizing current, i.e. $i_{L_1} \approx i_{L_2}/n$, L_σ is calculated with the measured input voltage v_{f2} of the full bridge and the measured current slope $di_{L_1}/dt \approx \Delta i_{L_1}/\Delta t$ (Figure A.27):

$$L_\sigma = L_{tr1} + n^2(L_{tr2} + L_{LV}) \approx \frac{n v_{f2}}{|\Delta i_{L_1}/\Delta t|}. \quad (\text{A.18})$$

Moreover, with the average LV side transformer voltage, \overline{V}_{AC2} , being measured (e.g. according to Figure A.27: in order to eliminate the effect of the resistive voltage drop, the average is evaluated over the time interval $t_1 < t < t_3$, which is symmetrical around the time of the zero crossing of the inductor current, t_2), the stray inductances of the transformer ($L_{tr1} + n^2 L_{tr2}$) and of the PCB ($n^2 L_{LV}$) can be determined separately:

$$L_{tr1} + n^2 L_{tr2} \approx \frac{n \overline{V}_{AC2}}{|\Delta i_{L_1}/\Delta t|}, \quad (\text{A.19})$$

$$n^2 L_{LV} \approx \frac{n(v_{f2} - \overline{V}_{AC2})}{|\Delta i_{L_1}/\Delta t|}. \quad (\text{A.20})$$

Table A.10 summarizes the results obtained for $n = 16$ and $n = 19$ and lists the respective inductance values required for L_{HV} . Compared to the stray inductances measured for the stand-alone transformers (Figures A.23 and A.21), considerably smaller inductance values result; this effect is addressed to the high impedance transfer ratio, e.g. for $n = 19$ the impedance

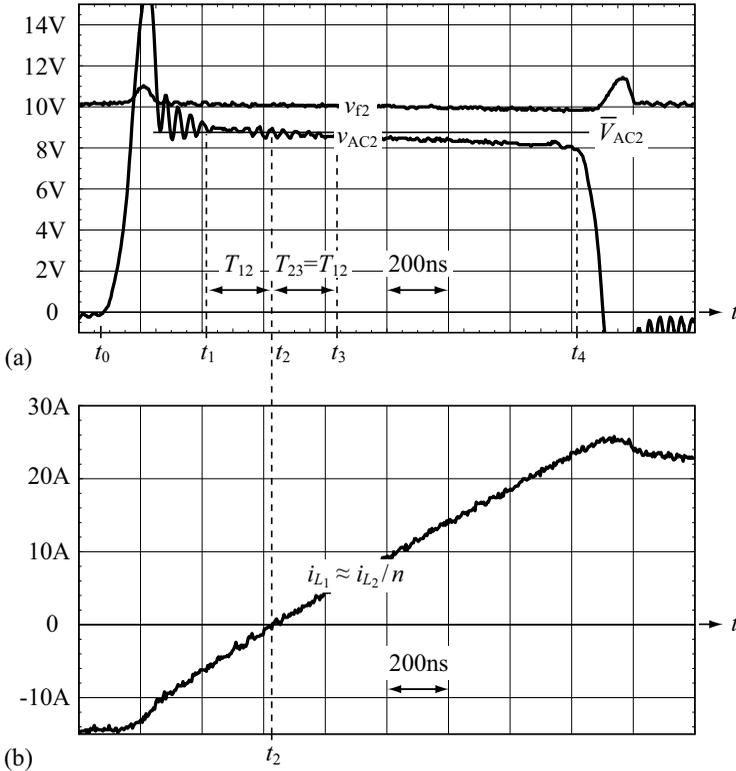


Figure A.27: (a) Measured voltages v_{f2} and v_{AC2} ; at $t = t_0$ the LV side full bridge changes its output voltage from $v_{AC2} = 0$ to $v_{AC2} = V_2$, i.e. T_6 is turned off, T_5 is turned on, and T_8 remains in its on-state; at $t = t_4$ the LV side full bridge changes its output voltage from $v_{AC2} = V_2$ to $v_{AC2} = 0$, i.e. T_8 is turned off, T_7 is turned on, and T_5 remains in its on-state; v_{AC2} decreases due to resistive losses in the semiconductors and in the PCB; moreover, the overvoltage on v_{AC2} (generated due to the effects detailed in Section 4.3.3) causes the dip in the waveform of v_{f2} ; (b) measured current $-i_{L1}$ in the HV side shorting bar for $n = 19$ and an input voltage of $v_{f2} = 10$ V.

transfer ratio is $n^2 = 361$, which makes the measured stray inductance very sensitive on the impedance of the shorting bar connected to the LV transformer terminations.

L	n	$ \Delta i_{L1}/\Delta t $ ($v_{f2} = 10\text{ V}$)	\bar{V}_{AC2}	$L_{tr1} + n^2 L_{tr2}$	$n^2 L_{LV}$	Remaining L_{HV}
15.5 μH	16	33.3 A/ μs	8.45 V	4.1 μH	0.7 μH	10.7 μH
22.4 μH	16	33.3 A/ μs	8.45 V	4.1 μH	0.7 μH	17.6 μH
26.7 μH	19	24.2 A/ μs	8.46 V	6.6 μH	1.2 μH	18.9 μH

Table A.10: Measured stray inductances of the transformer and the PCB; employed inductance values L_{HV} .

L_{HV}	Employed Cores	Employed Litz Wires	N_{LHV}	l_g
10.7 μH	4×E 32/6/20, 4×PLT 32/20/3, material: 3F3	parallel connected litz wires: $2 \times (200 \times 0.071\text{ mm})$	5	2.41 mm
17.6 μH	5×E 32/6/20, 5×PLT 32/20/3, material: 3F3	parallel connected litz wires: $2 \times (200 \times 0.071\text{ mm})$	5	1.67 mm
18.9 μH	6×E 32/6/20, 6×PLT 32/20/3, material: 3F3	parallel connected litz wires: $2 \times (200 \times 0.071\text{ mm})$	5	1.93 mm

Table A.11: Design data of the inductors placed in series to the transformer (HV side) in order to obtain the total DAB converter inductance calculated for the different modulation schemes; the inductors are designed according to Appendix A.9.

The required inductors are designed according to Appendix A.9 using ferrite cores and litz wire windings; Table A.11 summarizes the key parameters of the employed inductors.

A.2.6 EMI Filters

Employed EMI Filters

The DC filter capacitors which are directly connected to the DAB (i.e. C_{f1} and C_{f2} in Figure 6.1) are exposed to high RMS currents (Table A.1). Therefore, and due to DC voltages of up to 450 V, metalized polypropylene film capacitors are selected for C_{f1} (470 nF / 630 VDC, 7 connected in parallel).

The low voltage capacitor C_{f2} is subject to very high RMS currents; moreover, a very low parasitic inductance (< 1 nH) is required. Thus, 96 ceramic capacitors ($10 \mu\text{F} / 25 \text{V} / \text{X7R}$) are connected in parallel (Appendix A.2.3).

Both filter capacitors C_{f1} and C_{f2} are selected with respect to the capacitor RMS current; accordingly, the implemented capacitance values are small. In order to reduce the resulting DC port voltage ripples, the EMI filters depicted in Figure 6.1 are employed: the filter inductors L_{f1a} , L_{f1b} , L_{f2a} , and L_{f2b} suppress conducted EMI, the resistors R_{f1b} and R_{f2b} are providing a proper damping of the filters, and the DC capacitors C_{DC1} and C_{DC2} provide constant port voltages V_1 and V_2 . For C_{DC1} and C_{DC2} electrolytic capacitors are selected, since the RMS current stresses are very low in steady-state operation.

In order to simplify the design of the EMI filters, sinusoidal AC components of the inductor currents with a frequency of twice the switching frequency, $\hat{i}_{f1}(t) = \hat{I}_{f1,\text{peak}} \sin(4\pi f_s t)$ and $\hat{i}_{f2}(t) = \hat{I}_{f2,\text{peak}} \sin(4\pi f_s t)$, are considered and the maximum peak values of these AC components are set to:

- $\hat{I}_{f1,\text{peak,max}} = 500 \text{ mA}$,
- $\hat{I}_{f2,\text{peak,max}} = 10 \text{ A}$.

In a more comprehensive approach, the EMI filters could be designed with respect to a certain optimum, e.g. maximum power density.

HV Filter Design

For the design of L_{f1a} , L_{f1b} , R_{f1b} , and C_{DC1} , the HV side full bridge is replaced by the current source $i_{\text{FBI}}(t)$ [Figure A.28 (a), cf. Section 6.2.6]. On the assumption $C_{\text{DC1}} \gg C_{f1}$, the capacitor C_{DC1} can be replaced by a constant voltage source. Accordingly, the employed equivalent circuit of the EMI filter disregards C_{DC1} since the filter design solely considers AC signals [Figure A.28 (b)]. Moreover, the design only considers the fundamental component of the filter currents and voltages, i.e. $f = 2f_s$; the AC component $\hat{i}_{\text{FBI}}(t)$ is approximated with:

$$\hat{i}_{\text{FBI}}(t) \approx \sqrt{2} \hat{I}_{\text{FBI,RMS}} \cdot \sin(4\pi f_s t). \quad (\text{A.21})$$

Besides the main filter inductor L_{f1a} (L_{f1a} carries the converter DC current), the components L_{f1b} and R_{f1b} , depicted in Figure A.28 (b), form a damping network. The design of this filter structure closely follows [116]. There, the ratio

$$n_{L_{f1}} = L_{f1b} / L_{f1a} \quad (\text{A.22})$$

sets the filter damping. However, the filter attenuation decreases with increasing damping. According to [116], $n_{L_{f1}} = 0.5$ gives a good compromise

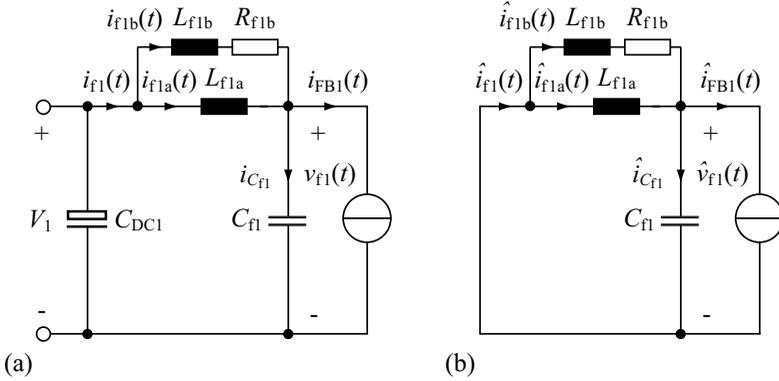


Figure A.28: (a) EMI filter employed on the HV side; the HV side full bridge is replaced by a current source (cf. Section 6.2.6); (b) equivalent AC circuit of the EMI filter used to calculate L_{f1} ; due to $C_{DC1} \gg C_{f1}$, the capacitor C_{DC1} can be replaced by a short circuit.

between filter degradation and the achievable damping. The filter resistance R_{f1b} is selected with respect to the optimal Q factor, $Q_{opt,fl}$ [116],

$$Q_{opt,fl} = \sqrt{\frac{n_{L_{f1}}(3 + 4n_{L_{f1}})(1 + 2n_{L_{f1}})}{2(1 + 4n_{L_{f1}})}}, \quad (\text{A.23})$$

$$R_{f1b} = Q_{opt,fl} Z_{0,fl}, \quad (\text{A.24})$$

using

$$Z_{0,fl} = \sqrt{\frac{L_{f1a}}{C_{f1}}}. \quad (\text{A.25})$$

With the specified peak current $\hat{I}_{f1,peak,max}$ and the maximum AC component of the input current on the HV side ($\hat{I}_{FB1,RMS,max} = 14.9$ A for phase shift modulation), the expression of the filter damping, given with

$$\begin{aligned} d(\omega = 4\pi f_S) &= \left| \frac{1 + j\omega \frac{L_{f1a} + L_{f1b}}{R_{f1b}}}{1 - \omega^2 L_{f1a} C_{f1} + j\omega \frac{L_{f1a} + L_{f1b}}{R_{f1b}} [1 - \omega^2 (L_{f1a} || L_{f1b}) C_{f1}]} \right| = \\ &= \frac{\hat{I}_{FB1,RMS,max}}{\hat{I}_{f1,peak,max}/\sqrt{2}} = 32.5 \text{ dB}, \quad (\text{A.26}) \end{aligned}$$

is solved with respect to L_{f1a} , L_{f1b} , and R_{f1b} at $\omega = 4\pi f_S$.

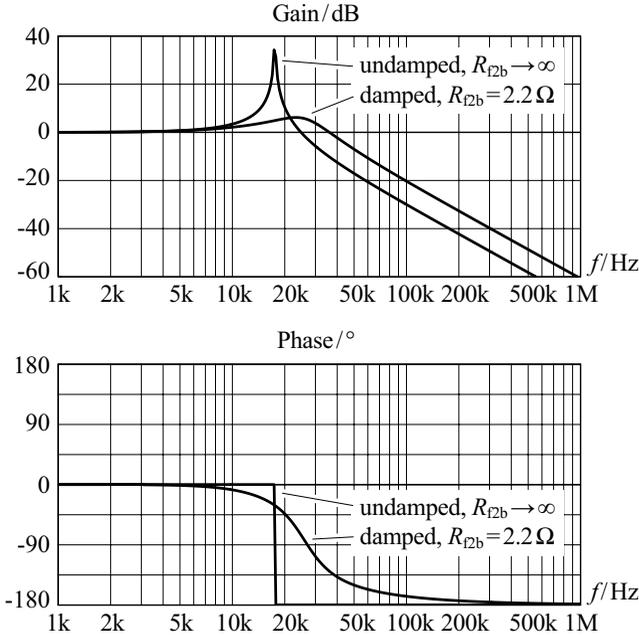


Figure A.29: Bode plot of the HV EMI filter transfer function, $G_{f1} = \hat{I}_{FB1,RMS}/\hat{I}_{f1,RMS}$, with and without filter damping; $C_{f1} = 3.3 \mu\text{F}$, $L_{f1a} = 25 \mu\text{H}$, $L_{f1b} = 12.5 \mu\text{H}$, $R_{f1b} = 2.5 \Omega$. With the proposed damping network, the maximum gain is 6.2 dB at $f = 23 \text{ kHz}$ and the filter attenuation at $f = 200 \text{ kHz}$ decreases from 42.2 dB to 32.5 dB.

For $C_{f1} = 7 \cdot 470 \text{ nF} = 3.3 \mu\text{F}$, the specified attenuation and optimal damping are achieved for:

- $L_{f1a} = 25 \mu\text{H}$,
- $L_{f1b} = 12.5 \mu\text{H}$,
- $R_{f1b} = 2.5 \Omega$.

The Bode plots of the respective filter transfer functions, $G_{f1} = \hat{I}_{FB1,RMS}/\hat{I}_{f1,RMS}$, with and without damping are shown in Figure A.30.

The DC capacitor C_{DC1} is designed with respect to the output impedance of the connected hardware in order to achieve a stable converter operation [116]

and with respect to the required electric energy storage capabilities; for the given DAB converter, $C_{DC1} = 220 \mu\text{F}$ is selected.

LV Filter Design

On the HV side and on the LV side, the same filter structures are employed. Therefore, the LV filter design method is identical to the method discussed above for the HV filter. For $C_{f2} = 96 \cdot 10 \mu\text{F} = 960 \mu\text{F}$, the specified attenuation and optimal damping are achieved for:

- $L_{f2a} = 70 \text{ nH}$,
- $L_{f2b} = 35 \text{ nH}$,
- $R_{f2b} = 8 \text{ m}\Omega$.

The Bode plots of the respective filter transfer functions, $G_{f2} = \hat{I}_{\text{FB2,RMS}}/\hat{I}_{\text{f2,RMS}}$, with and without damping are shown in Figure A.30.

For C_{DC2} a very large capacitance of 200 mF is employed in order to decouple the LV port of the DAB and the LV DC supply, since the impedance of the connecting cable to the LV supply considerably influences the control-to-output transfer function, derived in Section 6, if a smaller capacitance (e.g. $C_{DC2} = 20 \text{ mF}$) is used.

A.3 Three-Phase DAB Design

This Section summarizes the principle of operation and the design equations employed for the three-phase DAB. A more detailed discussion on this power converter and the derivations of the presented equations are given in [49, 54].

A.3.1 Principle of Operation

The three-phase DAB converter consists of 6 half bridge circuits and 3 HF transformers [Figure A.31 (a)]. During steady-state operation, the HV side half bridges are operated with a respective phase shift of $\pi/3$ [equal to a time shift of $T_S/6$, Figure A.31 (c)]. Moreover, each HF transformer connects a HV side half bridge to a LV side half bridge. According to Figures A.31 (b) and (c) [there, $T_\varphi = \varphi T_S/(2\pi)$ applies], equal phase shifts φ between the output voltages of the respective half bridges on the HV side and on the LV side are used to achieve the required power transfer between the DC ports of the power converter.

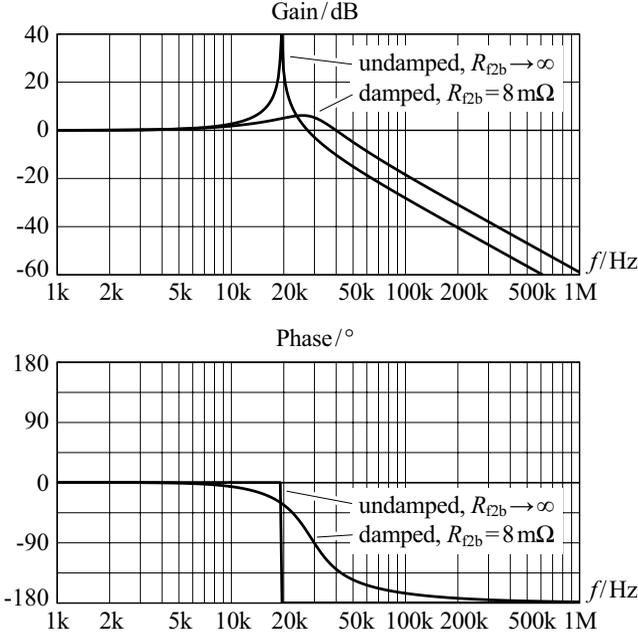


Figure A.30: Bode plot of the LV side EMI filter transfer function, $G_{f2} = \hat{I}_{FB2,RMS}/\hat{I}_{f2,RMS}$, with and without filter damping; $C_{f2} = 960 \mu\text{F}$, $L_{f2a} = 70 \text{ nH}$, $L_{f2b} = 35 \text{ nH}$, $R_{f2b} = 8 \text{ m}\Omega$. With the proposed damping network, the maximum gain is 6.2 dB at $f = 26 \text{ kHz}$ and the filter attenuation at $f = 200 \text{ kHz}$ decreases from 40.4 dB to 30.8 dB.

A.3.2 Lossless Electric Converter Model

In order to simplify the design process, the lossless electric model of the three-phase DAB converter is employed (cf. Section 3.1, [54]).

The phase shift, φ , required to achieve a certain power transfer, is:

$$\varphi = \begin{cases} \frac{2\pi - 2\pi\sqrt{1 - \frac{9f_S L|P|}{nV_1 V_2}}}{3} \text{sgn}(P) & \forall |P| \leq \frac{nV_1 V_2}{12f_S L} \\ \frac{3\pi - \pi\sqrt{7 - \frac{72f_S L|P|}{nV_1 V_2}}}{6} \text{sgn}(P) & \forall \frac{nV_1 V_2}{12f_S L} < |P| \leq P_{\max} \end{cases} \quad (\text{A.27})$$

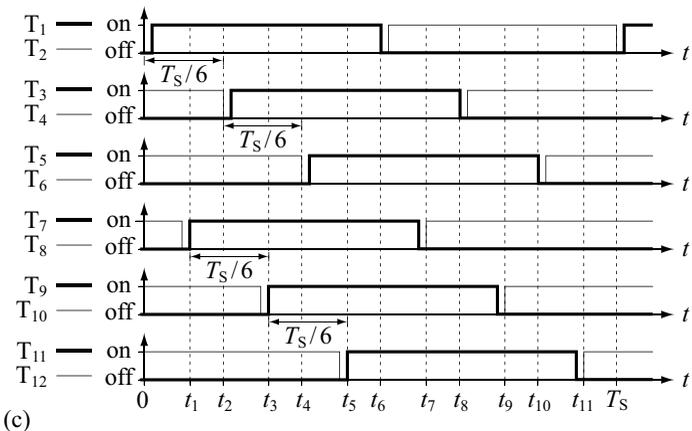
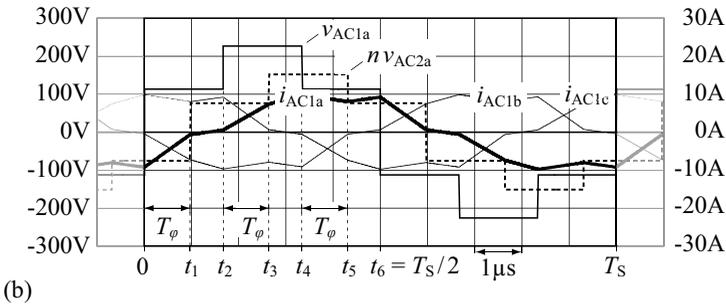
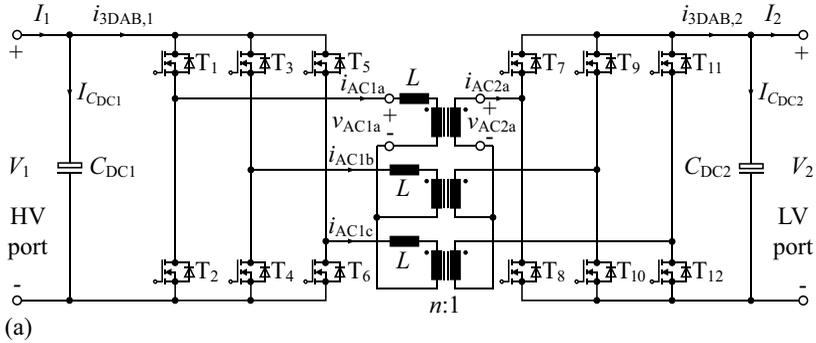


Figure A.31: (a) Three-phase DAB converter topology according to [49,54]; (b) voltage waveforms $v_{AC1}(t)$ and $v_{AC2}(t)$ and current waveforms $i_{AC1a}(t)$, $i_{AC1b}(t)$, and $i_{AC1c}(t)$ for $V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$, $P_2 = 2\text{ kW}$ (power transfer direction: HV \rightarrow LV), $n = 19$, $L = 21.4\text{ }\mu\text{H}$, and $f_s = 100\text{ kHz}$; (c) respective gate signals inclusive dead time intervals. At the particular operating point, soft switching is achieved on the HV side. On the LV side, hard switching transitions occur (cf. Section 4.3.2 and Section 4.3.3).

using:

$$P_{\max} = \frac{7nV_1V_2}{72f_sL} \quad (\text{A.28})$$

(maximum power occurs for $\varphi = \pm\pi/2$; for the lossless model, $P = P_1 = P_2$ applies).

Similar to the single-phase DAB, the conduction losses $P_{S1,\text{cond}}$ (HV side switches) and $P_{S2,\text{cond}}$ (LV side switches), the copper losses $P_{\text{tr}1,\text{cond}}$, $P_{\text{tr}2,\text{cond}}$ (HF transformer), and $P_{L_{\text{HV}},\text{cond}}$ (HF inductor), and the AC losses on the LV side of the PCB are calculated using the transformer RMS currents I_{AC1a} , I_{AC1b} , and I_{AC1c} ,

$$P_{S1,\text{cond}} = (I_{AC1a}^2 + I_{AC1b}^2 + I_{AC1c}^2) R_{3\text{DAB},S1}, \quad (\text{A.29})$$

$$P_{S2,\text{cond}} = n^2 (I_{AC1a}^2 + I_{AC1b}^2 + I_{AC1c}^2) R_{3\text{DAB},S2}, \quad (\text{A.30})$$

$$P_{L_{\text{HV}},\text{cond}} = (I_{AC1a}^2 + I_{AC1b}^2 + I_{AC1c}^2) R_{3\text{DAB},L_{\text{HV}}}, \quad (\text{A.31})$$

$$P_{\text{tr}1,\text{cond}} = (I_{AC1a}^2 + I_{AC1b}^2 + I_{AC1c}^2) R_{3\text{DAB},\text{tr}1}, \quad (\text{A.32})$$

$$P_{\text{tr}2,\text{cond}} = n^2 (I_{AC1a}^2 + I_{AC1b}^2 + I_{AC1c}^2) R_{3\text{DAB},\text{tr}2}, \quad (\text{A.33})$$

$$P_{\text{PCB},a,\text{cond}} = n^2 (I_{AC1a}^2 + I_{AC1b}^2 + I_{AC1c}^2) R_{3\text{DAB},\text{PCB},a}; \quad (\text{A.34})$$

the respective resistance values are obtained at the switching frequency, $f_s = 100$ kHz. In steady-state operation, the transformer RMS currents I_{AC1a} , I_{AC1b} , and I_{AC1c} are all equal, i.e. $I_{3\text{DAB},L} = I_{AC1a} = I_{AC1b} = I_{AC1c}$, and are calculated with:

$$I_{3\text{DAB},L} = \begin{cases} \frac{\sqrt{-9nV_1V_2|\varphi|^3 + 18\pi nV_1V_2|\varphi|^2 + \frac{5}{3}\pi^3(V_1 - nV_2)^2}}{18\pi^{3/2}f_sL} \vee |\varphi| \leq \frac{\pi}{3}, \\ \frac{\sqrt{nV_1V_2}}{18\pi^{3/2}f_sL} \cdot \left[-18|\varphi|^3 + 27\pi|\varphi|^2 - 3\pi^2|\varphi| + \frac{\pi^3}{3} \frac{5V_1^2 - 9nV_1V_2 + 5(nV_2)^2}{nV_1V_2} \right]^{\frac{1}{2}} \vee \frac{\pi}{3} < |\varphi| \leq \frac{\pi}{2}. \end{cases} \quad (\text{A.35})$$

The calculation of the switching losses $P_{S1,\text{sw}}$ (HV side) and $P_{S2,\text{sw}}$ (LV side) requires the instantaneous currents at the switching instants:

$$P_{S1,\text{sw}} = 6 f_s E_{3\text{DAB},S1,\text{sw}}(I_{3\text{DAB},S1,\text{sw}}), \quad (\text{A.36})$$

$$P_{S2,\text{sw}} = 6 f_s E_{3\text{DAB},S2,\text{sw}}(I_{3\text{DAB},S2,\text{sw}}) \quad (\text{A.37})$$

with:

$$I_{3\text{DAB},\text{S1},\text{sw}} = \begin{cases} \frac{2\pi(V_1 - nV_2) + 3nV_2|\varphi|}{18\pi f_S L} & \forall |\varphi| \leq \frac{\pi}{3}, \\ \frac{2\pi(V_1 - \frac{3nV_2}{2}) + 6nV_2|\varphi|}{18\pi f_S L} & \forall \frac{\pi}{3} < |\varphi| \leq \frac{\pi}{2}, \end{cases} \quad (\text{A.38})$$

$$I_{3\text{DAB},\text{S2},\text{sw}} = \begin{cases} n \frac{2\pi(nV_2 - V_1) + 3V_1|\varphi|}{18\pi f_S L} & \forall |\varphi| \leq \frac{\pi}{3}, \\ n \frac{2\pi(nV_2 - \frac{3V_1}{2}) + 6V_1|\varphi|}{18\pi f_S L} & \forall \frac{\pi}{3} < |\varphi| \leq \frac{\pi}{2}. \end{cases} \quad (\text{A.39})$$

The transformer core loss calculation employs the Steinmetz equation (4.10) and thus, the peak flux density inside the transformer core, $B_{3\text{DAB},\text{tr},\text{peak}}$ is required. According to Appendix A.2.5, the HF inductor is placed on the HV side, so

$$B_{3\text{DAB},\text{tr},\text{peak}} = \frac{V_2}{9f_S N_2 A_{3\text{DAB},\text{tr},\text{core}}} \quad (\text{A.40})$$

results (N_2 denotes the number of turns on the LV side and $A_{3\text{DAB},\text{tr},\text{core}}$ is the core cross section employed for a single HF transformer of the three-phase DAB). The total core losses are:

$$P_{3\text{DAB},\text{tr},\text{core}} \approx 3V_{3\text{DAB},\text{tr},\text{core}} k f_S^\alpha B_{3\text{DAB},\text{tr},\text{peak}}^\beta \quad (\text{A.41})$$

(i.e. 3 HF transformers; $V_{3\text{DAB},\text{tr},\text{core}}$ denotes the core volume of a single transformer). The Steinmetz parameters k , α , and β are given in Appendix C (Table C.2, Figure C.4).

The inductors' core losses $P_{3\text{DAB},L_{\text{HV}},\text{core}}$ are calculated according to (4.14) and (4.15), using the peak inductor currents $I_{3\text{DAB},L,\text{peak}} = I_{\text{AC1a},\text{peak}} = I_{\text{AC1b},\text{peak}} = I_{\text{AC1c},\text{peak}}$. The peak inductor currents are approximately calculated with

$$I_{3\text{DAB},L,\text{peak}} \approx \sqrt{2} \cdot I_{3\text{DAB},L}, \quad (\text{A.42})$$

since the waveforms of the transformer currents are close to a sinusoidal waveform [Figure A.31 (b)].

In order to calculate the RMS currents through the DC capacitors C_{DC1} and C_{DC2} , the RMS values of the input current $i_{3\text{DAB},1}$ and of the output

current $i_{3\text{DAB},2}$ [cf. Figure A.31 (a)] need to know:

$$I_{3\text{DAB},1} = \begin{cases} \frac{1}{18\pi^{3/2}f_S L} \left[-9nV_2(2V_1 + 3nV_2)|\varphi|^3 + \right. \\ \qquad \qquad \qquad \left. 9\pi nV_2(V_1 + 3nV_2)|\varphi|^2 + \frac{\pi^3}{3}(V_1 - nV_2)^2 \right]^{\frac{1}{2}} \\ \qquad \qquad \qquad \forall |\varphi| \leq \frac{\pi}{3}, \\ \\ \frac{1}{18\pi^{3/2}f_S L} \left[-36nV_1V_2|\varphi|^3 + 27\pi(2V_1 - nV_2)nV_2|\varphi|^2 + \right. \\ \qquad \qquad \qquad \left. 3\pi^2nV_2(9nV_2 - 8V_1)|\varphi| + \frac{\pi^3}{3}(V_1^2 + 9nV_1V_2 - 11(nV_2)^2) \right]^{\frac{1}{2}} \\ \qquad \qquad \qquad \forall \frac{\pi}{3} < |\varphi| \leq \frac{\pi}{2}, \end{cases} \quad (\text{A.43})$$

$$I_{3\text{DAB},2} = \begin{cases} \frac{n}{18\pi^{3/2}f_S L} \left[-9V_1(3V_1 + 2nV_2)|\varphi|^3 + \right. \\ \qquad \qquad \qquad \left. 9\pi V_1(3V_1 + nV_2)|\varphi|^2 + \frac{\pi^3}{3}(V_1 - nV_2)^2 \right]^{\frac{1}{2}} \\ \qquad \qquad \qquad \forall |\varphi| \leq \frac{\pi}{3}, \\ \\ \frac{n}{18\pi^{3/2}f_S L} \left[-36nV_1V_2|\varphi|^3 - 27\pi V_1(V_1 - 2nV_2)|\varphi|^2 + \right. \\ \qquad \qquad \qquad \left. 3\pi^2V_1(9V_1 - 8nV_2)|\varphi| + \frac{\pi^3}{3}(-11V_1^2 + 9nV_1V_2 + (nV_2)^2) \right]^{\frac{1}{2}} \\ \qquad \qquad \qquad \forall \frac{\pi}{3} < |\varphi| \leq \frac{\pi}{2}. \end{cases} \quad (\text{A.44})$$

With known DC port currents $I_1 = P/V_1$ and $I_2 = P/V_2$, the capacitor RMS currents $I_{3\text{DAB},C_{\text{DC}1}}$ and $I_{3\text{DAB},C_{\text{DC}2}}$ result:

$$I_{3\text{DAB},C_{\text{DC}1}} = \sqrt{I_{3\text{DAB},1}^2 - I_1^2}, \quad (\text{A.45})$$

$$I_{3\text{DAB},C_{\text{DC}2}} = \sqrt{I_{3\text{DAB},2}^2 - I_2^2}. \quad (\text{A.46})$$

The second part of the losses generated by the PCB (connection between the DC capacitors $C_{\text{DC}2}$ and the half bridges) is calculated according to (4.24) using (A.44) and $I_2 = P/V_2$:

$$P_{\text{PCB},b,\text{cond}} = I_2^2 R_{3\text{DAB},\text{PCB},b}(f=0) + I_{3\text{DAB},C_{\text{DC}2}}^2 R_{3\text{DAB},\text{PCB},b}(f=6f_S). \quad (\text{A.47})$$

For the single-phase DAB and for the three-phase DAB, the same semiconductor chip areas are considered and, consequently, the same gate driver power demand is assumed. Therefore, the power demands of the auxiliary power supplies remain equal to (4.16).

A.3.3 Model Parameterization

The three-phase DAB converter model is parameterized using data from the single-phase DAB detailed in Chapter 4 and Appendix A.2.

Resistance Values

The single-phase DAB employs 2 half bridge circuits on the HV side and 2 half bridge circuits on the LV side. In contrast, the three-phase DAB uses 3 half bridge circuits on either side. With respect to a constant semiconductor chip area, the employed on-state resistances of the switches are scaled according to:

$$R_{3\text{DAB},S1} = \frac{3}{2}R_{S1} = 105 \text{ m}\Omega, \quad (\text{A.48})$$

$$R_{3\text{DAB},S2} = \frac{3}{2}R_{S2} = 0.52 \text{ m}\Omega \quad (\text{A.49})$$

$$(\text{A.50})$$

[on the assumption of a junction temperature of $T_j = 25^\circ\text{C}$; cf. (4.5), and (4.6); in order to include increased losses due to HF effects on the LV side, the MOSFET channel resistance $R_{\text{DS(on)},\text{IRF2804}}(f = 100 \text{ kHz}) \approx 280 \text{ m}\Omega$ is considered, cf. Figure 4.4].

In order to achieve low HF losses, 3 parallel copper planes are needed on the LV side to provide an electric connection between each HF transformer and the HF port of the respective half bridge (similar to Figure A.7, cf. Appendix A.2.3). Thus, compared to the single-phase DAB, one additional copper layer is required on the LV side of the PCB of the three-phase DAB. Provided that the PCB geometry remains unmodified and that the PCB again employs copper layers with a thickness of $200 \mu\text{m}$ [cf. Section 4.1, (A.8)], then the following resistances apply:

$$R_{3\text{DAB,PCB,a}}(f = 100 \text{ kHz}) = \frac{1}{2}R_{\text{PCB,a}}(f = 100 \text{ kHz}) = 130 \mu\Omega, \quad (\text{A.51})$$

$$R_{3\text{DAB,PCB,b}}(f = 0) = R_{\text{PCB,b}}(f = 0) = 120 \mu\Omega, \quad (\text{A.52})$$

$$R_{3\text{DAB,PCB,b}}(f = 600 \text{ kHz}) = R_{\text{PCB,b}}(f = 600 \text{ kHz}) = 530 \mu\Omega \quad (\text{A.53})$$

[for the single-phase DAB, $R_{\text{PCB,a}}$ considers the resistance of the transformer feed line and the respective return line; therefore the factor 1/2 is needed in (A.51)].

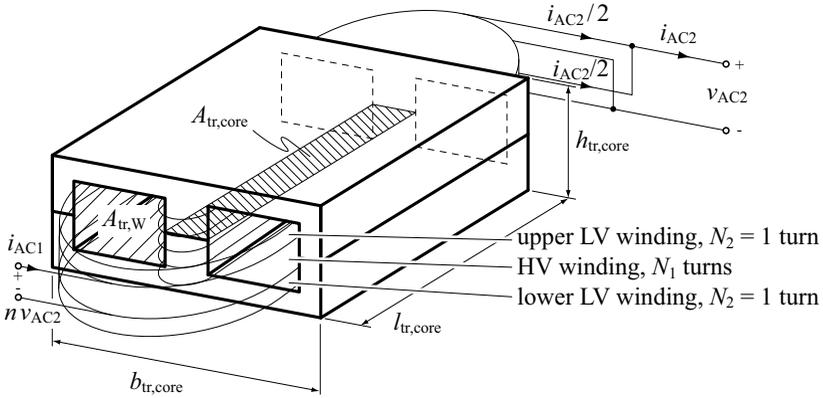


Figure A.32: Planar transformer employed for the single-phase DAB; in order to improve the efficiency, 2 windings are operated in parallel on the LV side. The depicted setup is used to estimate the expected resistance values $R_{3DAB,tr1}$ and $R_{3DAB,tr2}$ for the three-phase DAB.

The calculations of the expected transformer resistance values $R_{3DAB,tr1}$ and $R_{3DAB,tr2}$ are based on the transformer setup depicted in Figure A.32 and on the product of $A_{tr,W}$ (winding window area) and $A_{tr,core}$ (core cross section area).

Provided that the HF inductor L solely resides on the HV side and that the peak magnetic flux densities in the transformer cores of the single-phase DAB ($B_{DAB,tr,peak}$) and the three-phase DAB ($B_{3DAB,tr,peak}$) are equal, the ratio of the core cross sections employed for the three-phase DAB and for the single-phase DAB, $A_{3DAB,tr,core}/A_{DAB,tr,core}$, is

$$\left. \begin{aligned} B_{DAB,tr,peak} &= \frac{V_2}{4f_S N_2 A_{DAB,tr,core}} \\ B_{3DAB,tr,peak} &= \frac{V_2}{9f_S N_2 A_{3DAB,tr,core}} \end{aligned} \right\} \text{for } B_{DAB,tr,peak} = B_{3DAB,tr,peak} \Rightarrow$$

$$\Rightarrow \frac{A_{3DAB,tr,core}}{A_{DAB,tr,core}} = \frac{4}{9}. \quad (\text{A.54})$$

According to [92] and in anticipation of the VA ratings presented in Section 2.2.1 ($S_{DAB,tr} = 4.6 \text{ kVA}$ and $S_{3DAB,tr} = 4.2 \text{ kVA}$, whereas $S_{3DAB,tr}$ denotes the total VA rating of all 3 transformers of the three-phase DAB), the winding window of a single transformer of the three-phase DAB, $A_{3DAB,tr,W}$

can be calculated according to:

$$\frac{S_{3\text{DAB,tr}}/3}{S_{\text{DAB,tr}}} = \frac{A_{3\text{DAB,tr,core}} A_{3\text{DAB,tr,W}}}{A_{\text{DAB,tr,core}} A_{\text{DAB,tr,W}}} \Rightarrow \frac{A_{3\text{DAB,tr,W}}}{A_{\text{DAB,tr,W}}} = \frac{A_{\text{DAB,tr,core}}}{A_{3\text{DAB,tr,core}}} \frac{S_{3\text{DAB,tr}}/3}{S_{\text{DAB,tr}}} \approx 0.68. \quad (\text{A.55})$$

Furthermore, on the assumption of the core length, $l_{\text{tr,core}}$, being proportional to $\sqrt{A_{\text{tr,core}}}$ (cf. Figure A.32) and with the core length of the transformer used for the single-phase DAB, $l_{\text{DAB,tr,core}} = 38.1$ mm, the core length of a single transformer of the three-phase DAB, $l_{3\text{DAB,tr,core}}$, can be estimated:

$$l_{3\text{DAB,tr,core}} = l_{\text{DAB,tr,core}} \sqrt{\frac{A_{3\text{DAB,tr,core}}}{A_{\text{DAB,tr,core}}}} = \frac{2}{3} \cdot 38.1 \text{ mm} = 25.4 \text{ mm}. \quad (\text{A.56})$$

Besides $l_{3\text{DAB,tr,core}}$, the length of a single turn, $l_{3\text{DAB,tr,s}}$, needed in (A.59) and (A.60), additionally includes the average length of the end turns, $\bar{l}_{3\text{DAB,tr,e}}$. With the dimensions of the ferrite core used for the DAB (ELP 58: $p_c = 8.1$ mm, $b_c = 21.5$ mm, Figure A.52), $\bar{l}_{3\text{DAB,tr,e}}$ becomes

$$\bar{l}_{3\text{DAB,tr,e}} = \pi \left(p_c \sqrt{\frac{A_{3\text{DAB,tr,core}}}{A_{\text{DAB,tr,core}}}} + b_c \sqrt{\frac{A_{3\text{DAB,tr,W}}}{A_{\text{DAB,tr,W}}}} \right) = 23.2 \text{ mm}. \quad (\text{A.57})$$

With this, the ratio $l_{3\text{DAB,tr,s}}/l_{\text{DAB,tr,s}}$ can be determined ($l_{\text{DAB,tr,s}}$ denotes the length of a single turn of the windings used for the HF transformer of the single-phase DAB):

$$\frac{l_{3\text{DAB,tr,s}}}{l_{\text{DAB,tr,s}}} = \frac{2l_{3\text{DAB,tr,core}} + \bar{l}_{3\text{DAB,tr,e}}}{2l_{\text{DAB,tr,core}} + \bar{l}_{\text{DAB,tr,e}}} = \frac{2 \cdot 25.4 \text{ mm} + 72.9 \text{ mm}}{2 \cdot 38.1 \text{ mm} + 93.0 \text{ mm}} = 0.731. \quad (\text{A.58})$$

Finally, with the data given in Table A.9 and (A.55) and (A.58), the transformer resistances $R_{3\text{DAB,tr1}}$ and $R_{3\text{DAB,tr2}}$ can be calculated:

$$R_{3\text{DAB,tr1}} = \rho \frac{N_1 l_{3\text{DAB,tr,s}}}{k A_{3\text{DAB,tr,W}}/(2N_1)} = \rho \frac{0.731 N_1 l_{\text{DAB,tr,s}}}{0.68 k A_{\text{DAB,tr,W}}/(2N_1)} \\ = 1.07 R_{\text{DAB,tr1}} \approx n^2 \cdot 0.12 \text{ m}\Omega, \quad (\text{A.59})$$

$$R_{3\text{DAB,tr2}} = 1.07 R_{\text{DAB,tr2}} \approx 0.34 \text{ m}\Omega \quad (\text{A.60})$$

(winding temperature: 25°C).

Depending on the actual converter parameters n and L , separate HF inductors L_{HV} are designed (Appendix A.2), according to the inductor design procedure outlined in Appendix A.9. Subsequently, the respective conduction and core losses are calculated according to (A.31) and (4.14).

The dielectric losses generated by the DC capacitors C_{DC1} and C_{DC2} are very small and therefore neglected.

Switching Losses

The switching losses are calculated using the results discussed in Sections 4.3.2 and 4.3.3. In order to facilitate a meaningful comparison of the single-phase DAB and the three-phase DAB, the particular loss energies $E_{S1,sw}$ and $E_{S2,sw}$ are scaled with respect to a constant semiconductor chip area.

In case of a constant current density in the semiconductor chip, the switching losses increase with increasing chip area (on the assumption of a homogeneous distribution of the switching losses across the chip surface):

$$E_{3DAB,S1,sw}(A_{S1}J_{3DAB,S1,sw}) = aE_{S1,sw}(A_{S1}J_{3DAB,S1,sw}), \quad (\text{A.61})$$

$$E_{3DAB,S2,sw}(A_{S2}J_{3DAB,S2,sw}) = aE_{S2,sw}(A_{S2}J_{3DAB,S2,sw}) \quad (\text{A.62})$$

(a denotes the relative chip size, i.e. the ratio of the chip size used for each switch of the three-phase DAB to the chip size used for the respective switch of the single-phase DAB; A_{S1} and A_{S2} denote the chip areas of the switches on the HV side and on the LV side, respectively). However, with constant currents $I_{3DAB,S1,sw}$ and $I_{3DAB,S2,sw}$ and with increasing chip areas, the current densities $J_{3DAB,S1,sw}$ and $J_{3DAB,S2,sw}$ decrease. Thus, the switching loss energies are calculated according to:

$$E_{3DAB,S1,sw}(I_{3DAB,S1,sw}) = aE_{S1,sw} \left(\frac{1}{a} I_{3DAB,S1,sw} \right), \quad (\text{A.63})$$

$$E_{3DAB,S2,sw}(I_{3DAB,S2,sw}) = aE_{S2,sw} \left(\frac{1}{a} I_{3DAB,S2,sw} \right), \quad (\text{A.64})$$

$$a = \frac{2}{3}. \quad (\text{A.65})$$

With $a = 2/3$, equal semiconductor chip areas are used for the switches of the three-phase DAB and for the switches of the single-phase DAB.

Transformer Core Volume

The core volume of a single transformer of the three-phase DAB, $V_{3DAB,tr,core}$, required to calculate the transformer core losses, is equal to the total transformer volume (except for the volume of the end turns) minus the volume of the winding window:

$$V_{3DAB,tr,core} = b_{3DAB,tr,core} h_{3DAB,tr,core} l_{3DAB,tr,core} - 2A_{3DAB,tr,W} l_{3DAB,tr,core}. \quad (\text{A.66})$$

Provided that the respective widths and heights of $A_{3DAB,tr,W}$ and $A_{3DAB,tr,core}$ scale proportional to $\sqrt{A_{3DAB,tr,W}}$ and $\sqrt{A_{3DAB,tr,core}}$, the ex-

pected transformer height and width can be determined with:

$$h_{3\text{DAB,tr,core}} = 13 \text{ mm} \sqrt{\frac{A_{3\text{DAB,tr,W}}}{A_{\text{DAB,tr,W}}}} + 8.1 \text{ mm} \sqrt{\frac{A_{3\text{DAB,tr,core}}}{A_{\text{DAB,tr,core}}}} = 16.2 \text{ mm}, \quad (\text{A.67})$$

$$b_{3\text{DAB,tr,core}} = 43 \text{ mm} \sqrt{\frac{A_{3\text{DAB,tr,W}}}{A_{\text{DAB,tr,W}}}} + 15.4 \text{ mm} \sqrt{\frac{A_{3\text{DAB,tr,core}}}{A_{\text{DAB,tr,core}}}} = 45.8 \text{ mm} \quad (\text{A.68})$$

(using the dimensions of the ELP 58 core [155]). Thus, the estimated core volume of one transformer of the three-phase DAB is:

$$V_{3\text{DAB,tr,core}} = 9.12 \text{ cm}^3. \quad (\text{A.69})$$

A.3.4 Design Results

The three-phase DAB converter is designed with respect to maximum average efficiency, according to Appendix A.1. For $n = 20$ and $L = 22.2 \mu\text{H}$ the maximum average efficiency $\bar{\eta}_{\text{design}} = 90.9\%$ results. Table A.12 summarizes the expected converter currents and voltages.

A.4 LLC Converter Design

A.4.1 Analytical Model of the LLC Converter

Lossless Electric Converter Model

With the investigations on the LLC converter being confined to the continuous conduction mode (CCM), the analytical converter model (Figure A.33) becomes very similar to the analytical model of the DAB: again, the full bridge circuits are replaced by voltage sources and all LV side quantities are referred to the HV side. Thus, the LLC converter [Figure A.33 (a)] can be replaced by the circuit shown in Figure A.33 (b), with the high frequency AC part being composed of a series resonant circuit (inductor L and capacitor C) and the additional inductance L_M . In contrast to the DAB, second order differential equations need to be considered regarding the inductor current i_L and the capacitor voltage v_C . With the inductor current $i_{L,i-1}$ and the capacitor voltage $v_{C,i-1}$ at the beginning of the i -th time interval ($t = t_{i-1}$),

$$i_{L,i-1} = i_L(t_{i-1}), \quad v_{C,i-1} = v_C(t_{i-1}), \quad (\text{A.70})$$

collected in the vector

$$\vec{x}_{i-1} = (i_{L,i-1} \quad v_{C,i-1})^T, \quad (\text{A.71})$$

<i>Property</i>	<i>Value</i>	<i>Description</i>
<i>Maximum Average Efficiency:</i>		
$\bar{\eta}_{\text{design}}$	90.9%	maximum average converter efficiency calculated with (A.1), (A.2), (A.3), and (A.4)
<i>HV Side Switches $T_1, T_2, T_3, T_4, T_5, T_6$ ($i = 1 \dots 6$):</i>		
$\max(V_{3\text{DAB,DS},T_i,\text{peak}})$	450 V	maximum HV switch voltages
$\max(I_{3\text{DAB,D},T_i,\text{peak}})$	14.2 A	max. instantaneous HV switch current
$\max(I_{3\text{DAB,D},T_i})$	6.4 A	maximum HV switch RMS current
<i>LV Side Switches $T_7, T_8, T_9, T_{10}, T_{11}, T_{12}$ ($i = 7 \dots 12$):</i>		
$\max(V_{3\text{DAB,DS},T_i,\text{peak}})$	16 V	maximum LV switch voltages
$\max(I_{3\text{DAB,D},T_i,\text{peak}})$	285 A	max. instantaneous LV switch current
$\max(I_{3\text{DAB,D},T_i})$	129 A	maximum LV switch RMS currents
<i>Transformer:</i>		
n	20	turns ratio
$\max(I_{3\text{DAB,L}})$	9.1 A	HV windings, max. RMS curr.
$\max(n I_{3\text{DAB,L}})$	182 A	LV windings, max. RMS curr.
$\max(B_{3\text{DAB,tr,core,peak}})$	129 mT	peak transformer flux densities
<i>HF Inductors L:</i>		
L	22.2 μH	inductance values
$\max(I_{3\text{DAB,L,peak}})$	14.2 A	max. instantaneous inductor current
$\max(I_{3\text{DAB,L}})$	9.1 A	maximum inductor RMS current
<i>HV Side DC Capacitor C_{DC1}:</i>		
$\max(I_{3\text{DAB},C_{\text{DC1}}})$	4.1 A	maximum capacitor RMS current
<i>LV Side DC Capacitor C_{DC2}:</i>		
$\max(I_{3\text{DAB},C_{\text{DC2}}})$	66 A	maximum capacitor RMS current

Table A.12: Design summary for the three-phase DAB converter.

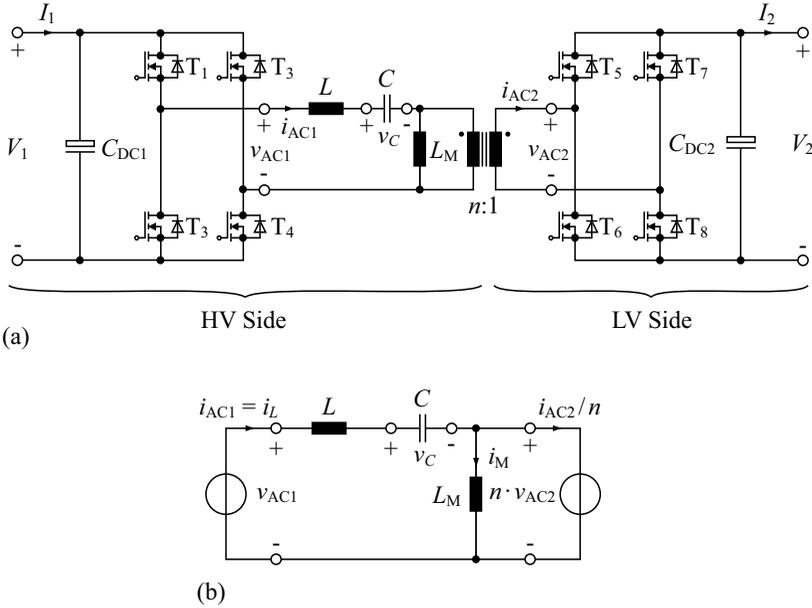


Figure A.33: (a) Power stage of the considered LLC converter; (b) lossless electric model of the LLC converter, provided that the converter is operated in continuous conduction mode (CCM).

and on the assumption of constant voltage being applied to L and C during the i -th time interval (defined in order to be consistent with the definitions used in Chapter 6),

$$v_{R,i-1} = v_{AC1}(t_{(i-1)+}) - n v_{AC2}(t_{(i-1)+}), \quad (\text{A.72})$$

the respective time domain solutions for $i_{L,i}$ and $v_{C,i}$ at the end of the regarded time interval with the duration T_i are:

$$i_{L,i} = i_L(\vec{x}_{i-1}, T_i) = i_{L,i-1} \cos(\omega_0 T_i) + \frac{v_{R,i-1} - v_{C,i-1}}{Z_0} \sin(\omega_0 T_i), \quad (\text{A.73})$$

$$v_{C,i} = v_C(\vec{x}_{i-1}, T_i) = Z_0 i_{L,i-1} \sin(\omega_0 T_{i-1}) + v_{R,i-1} - (v_{R,i-1} - v_{C,i-1}) \cos(\omega_0 T_i), \quad (\text{A.74})$$

$$\omega_0 = \frac{1}{\sqrt{LC}}, \quad Z_0 = \sqrt{\frac{L}{C}}. \quad (\text{A.75})$$

The voltage nv_{AC2} generates the current i_M through L_M [Figure A.33 (b)] and therefore $i_M(t)$ can be calculated separately using the solution of a first order differential equation.

Improved Converter Model

In order to increase the accuracy of the calculated inductor current waveform $i_L(t)$, conduction losses need to be considered (cf. Section 3.2). The final LLC converter model further includes the improved transformer model depicted in Figure A.34 (cf. Appendix A.2.4 and Table A.9) and LV side stray inductances (Table A.10). The resulting LLC converter model is shown in Figure A.35 (a).

The HF AC circuit of the LLC converter model depicted in Figure A.35 (a) is of 4th-order and thus, the expressions for $i_{L_1}(t)$ and $i_{L_2}(t)$ become very involved. Similar to the DAB, the wye-delta transformation is employed in order to reduce the calculation effort [Figure A.35 (b); cf. Section 3.3].

The expressions for \underline{Z}_{12} , \underline{Z}_{13} , and \underline{Z}_{23} ,

$$\underline{Z}_{12} = R_1 + n^2 R_2 + s \cdot (L_1 + n^2 L_2) + \frac{1}{sC} + \frac{n^2 (R_1 + sL_1 + \frac{1}{sC}) \cdot (R_2 + sL_2)}{R_M || (sL_M)}, \quad (A.76)$$

$$\underline{Z}_{13} = R_1 + sL_1 + \frac{1}{sC} + [R_M || (sL_M)] \cdot \left[1 + \frac{R_1 + sL_1 + \frac{1}{sC}}{n^2(R_2 + sL_2)} \right], \quad (A.77)$$

$$\underline{Z}_{23} = n^2(R_2 + sL_2) + [R_M || (sL_M)] \cdot \left[1 + \frac{n^2(R_2 + sL_2)}{R_1 + sL_1 + \frac{1}{sC}} \right], \quad (A.78)$$

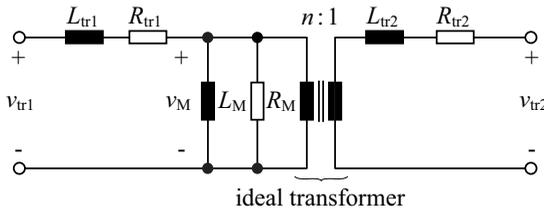


Figure A.34: Transformer model employed for the improved electric model of the LLC converter.

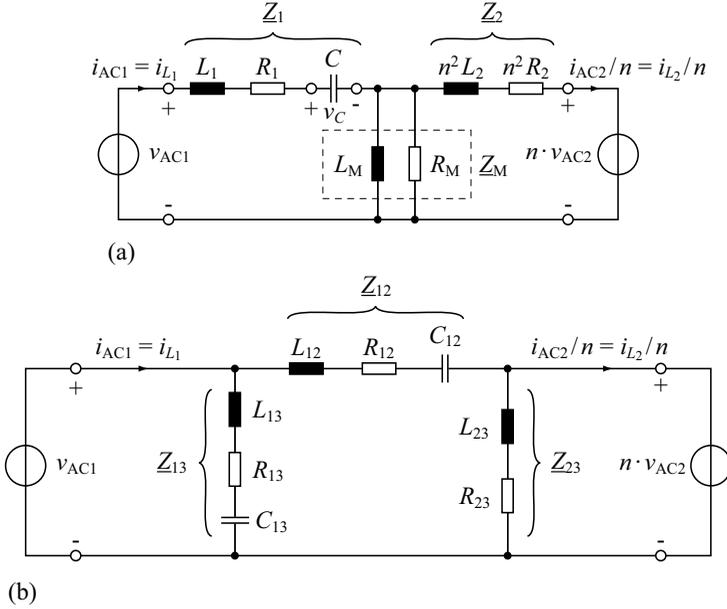


Figure A.35: (a) Improved electric model of the LLC converter; (b) the wye-delta transformation is employed to simplify the calculations.

contain higher order components and need to be simplified. On the assumptions

$$R_1 \ll s L_1 + \frac{1}{sC}, \quad R_2 \ll s L_2, \quad R_M \gg s L_M \quad (\text{A.79})$$

[cf. (3.102)], Z_{12} and Z_{13} become:

$$\begin{aligned} Z_{12} &\approx R_1 + n^2 R_2 + s \cdot \left(L_1 + n^2 L_2 + \frac{n^2 L_1 L_2}{L_M} \right) + \frac{1}{sC} \left(1 + \frac{n^2 L_2}{L_M} \right) \\ &= R_{12} + s L_{12} + \frac{1}{s C_{12}}, \quad (\text{A.80}) \end{aligned}$$

$$\begin{aligned} Z_{13} &\approx \left(R_1 + s L_1 + \frac{1}{sC} \right) \left(1 + \frac{L_M}{n^2 L_2} \right) + s L_M \\ &= R_{13} + s L_{13} + \frac{1}{s C_{13}}, \quad (\text{A.81}) \end{aligned}$$

i.e. equal to the impedances of 2 separate series resonant circuits. For the simplification of the remaining impedance \underline{Z}_{23} , the assumption $s^2 L_1 C \gg 1$ is additionally required, i.e. converter operation above resonance. With this, \underline{Z}_{23} reduces to the impedance of an inductor and a resistor connected in series,

$$\underline{Z}_{23} \approx n^2 (R_2 + s L_2) \left(1 + \frac{L_M}{L_1} \right) + s L_M = R_{23} + s L_{23}, \quad (\text{A.82})$$

and thus, $i_{L_{23}}$ can be calculated using (3.60).

The expressions for the inductor current and the capacitor voltage of \underline{Z}_{12} are:

$$i_{L_{12}}(\vec{x}_{12,i-1}, t) = e^{-\frac{d_{12} \omega_{0,12}}{2} t} \left\{ i_{L_{12},i-1} \cos(\omega_{r,12} t) + \left[\frac{v_{R,i-1} - v_{C_{12},i-1}}{Z_{0,12}} - \frac{d_{12}}{2} i_{L_{12},i-1} \right] \frac{\omega_{0,12}}{\omega_{r,12}} \sin(\omega_{r,12} t) \right\} \quad (\text{A.83})$$

$$v_{C_{12}}(\vec{x}_{12,i-1}, t) = v_{R,i-1} + e^{-\frac{d_{12} \omega_{0,12}}{2} t} \left\{ (v_{C_{12},i-1} - v_{R,i-1}) \cos(\omega_{r,12} t) + \left[Z_{0,12} i_{L_{12},i-1} + \frac{d_{12}}{2} (v_{C_{12},i-1} - v_{R,i-1}) \right] \frac{\omega_{0,12}}{\omega_{r,12}} \sin(\omega_{r,12} t) \right\}, \quad (\text{A.84})$$

$$\vec{x}_{12,i-1} = (i_{L_{12},i-1} \quad v_{C_{12},i-1})^T, \quad (\text{A.85})$$

$$\omega_{0,12} = \frac{1}{\sqrt{L_{12} C_{12}}}, \quad Z_{0,12} = \sqrt{\frac{L_{12}}{C_{12}}}, \quad (\text{A.86})$$

$$Q_{12} = \frac{Z_{0,12}}{R_{12}}, \quad d_{12} = \frac{1}{Q_{12}}, \quad \omega_{r,12} = \frac{\omega_{0,12} \sqrt{4 - d_{12}^2}}{2}. \quad (\text{A.87})$$

The expressions regarding the inductor current and the capacitor voltage of \underline{Z}_{13} are similar to (A.83) and (A.84), however, besides the respective component values, $v_{R,i-1}$ needs to be replaced by $v_{AC1,i-1} = v_{AC1}(t_{(i-1)+})$. The currents $i_{L_1}(t)$ and $i_{L_2}(t)$ are finally calculated with (3.106).

The converter power levels P_1 and P_2 are calculated with (3.111) and the conduction losses are calculated based on the RMS currents I_{L_1} and I_{L_2} [cf. (3.117) and Chapter 4].

Steady-State Inductor Current and Capacitor Voltage

In order to determine the optimal converter parameters n , L , C , and L_M with respect to maximum average converter efficiency (Appendix A.1), the numerical solver algorithm discussed in Section 4.6.1 is used to predict the expected total losses of the LLC converter. The employed algorithm calculates the different stress values (RMS currents, RMS voltages, peak currents, peak voltages, and peak flux densities) for the converter components. It assumes steady-state converter operation, CCM, and constant AC voltages $v_{AC1}(t)$ and $v_{AC2}(t)$ during the considered time intervals.

The numerical solver requires the initial steady-state values of all inductor currents and all capacitor voltages of the employed simplified resonant tank [Figure A.35 (b)] to be known at one particular point in time (e.g. at $t = 0$) in order to calculate the converter stress values [i.e. to evaluate (3.60), (A.83), and (A.84) and the expressions derived therefrom, e.g. the expressions for the RMS transformer currents; cf. Section 3.2.1]. For \underline{Z}_{23} , the initial value $i_{L_{23}}(0)$ is calculated with (3.67). Considerably more complex expressions result for the initial inductor currents and the initial capacitor voltages of the series resonant circuits represented by \underline{Z}_{12} and \underline{Z}_{13} . The respective expressions are derived for $i_{L_{12}}(0)$ and $v_{C_{12}}(0)$ in the following paragraph; (A.92) summarizes the result for \underline{Z}_{12} .

Each half-cycle is assumed to consist of m different time intervals (i.e. m time intervals with constant voltages v_R applied to \underline{Z}_{12} and constant voltages v_{AC1} applied to \underline{Z}_{13}). For \underline{Z}_{12} , the inductor currents and the capacitor voltages at the end of each time interval are calculated with:

$$\begin{pmatrix} i_{L_{12},i} \\ v_{C_{12},i} \end{pmatrix} = \mathbf{A}_{12,i} \cdot \begin{pmatrix} i_{L_{12},i-1} \\ v_{C_{12},i-1} \end{pmatrix} + \vec{b}_{12,i} \cdot v_{R,i-1}, \quad 1 \leq i \leq m, \quad (i, m) \in \mathbb{N}; \quad (\text{A.88})$$

$\mathbf{A}_{12,i}$ and $\vec{b}_{12,i}$ are obtained from (A.83) and (A.84).

The final current and voltage values after one half period with $m (\geq 2)$ different time intervals are:

$$\begin{pmatrix} i_{L_{12},m} \\ v_{C_{12},m} \end{pmatrix} = \mathbf{A}_{p,12,m,1} \cdot \begin{pmatrix} i_{L_{12},0} \\ v_{C_{12},0} \end{pmatrix} + \left(\sum_{i=1}^{m-1} \mathbf{A}_{p,12,m,i+1} \cdot \vec{b}_{12,i} \cdot v_{R,i-1} \right) + \vec{b}_{12,m} \cdot v_{R,m-1}, \quad (\text{A.89})$$

with

$$\mathbf{A}_{p,12,j,i} = \mathbf{A}_{12,j} \cdot \mathbf{A}_{12,j-1} \cdot \mathbf{A}_{12,j-2} \cdots \mathbf{A}_{12,i+1} \cdot \mathbf{A}_{12,i}. \quad (\text{A.90})$$

The steady-state solution for $i_{L_{12},0}$ and $v_{C_{12},0}$ is then obtained from

$$\begin{pmatrix} i_{L_{12},m} \\ v_{C_{12},m} \end{pmatrix} = \begin{pmatrix} -i_{L_{12},0} \\ -v_{C_{12},0} \end{pmatrix} \quad (\text{A.91})$$

and calculated with

$$\begin{pmatrix} i_{L_{12},0} \\ v_{C_{12},0} \end{pmatrix} = (-\mathbf{I} - \mathbf{A}_{p,12,m,1})^{-1} \cdot \left[\left(\sum_{i=1}^{m-1} \mathbf{A}_{p,12,m,i+1} \cdot \vec{b}_{12,i} \cdot v_{R,i-1} \right) + \vec{b}_{12,m} \cdot v_{R,m-1} \right]. \quad (\text{A.92})$$

For the initial inductor current and the initial capacitor voltage regarding the impedance \underline{Z}_{13} an expression similar to (A.92) results, however, $v_{R,i}$, $A_{p,12,j,i}$, and $\vec{b}_{12,i}$ need to be replaced by $v_{AC1,i}$, $A_{p,13,j,i}$, and $\vec{b}_{13,i}$.

A.4.2 HF Capacitor

Compared to the DAB converter, the resonant tank of the LLC converter additionally contains the HF capacitor C , which carries the HV side transformer RMS current I_{L_1} . In order to achieve low losses, film capacitors with a typical dissipation factor $\tan \delta$ of

$$\tan \delta \approx 1.5 \cdot 10^{-3} \quad (\text{A.93})$$

are used [157]. The corresponding ESR of the capacitor is:

$$R_C = \frac{\tan \delta}{2\pi f C}. \quad (\text{A.94})$$

A.4.3 Design Results, Phase Shift Modulation

The LLC and the DAB converter topologies are almost identical, except for the impedance network employed in the HF path. Thus, the modulation methods investigated for the DAB can also be applied to the LLC converter. However, different transformer currents $i_{L_1}(t)$ and $i_{L_2}(t)$ result and, consequently, a different converter efficiency is obtained.

Compared to the DAB, the design of the LLC converter requires the 4 converter parameters n , L_1 , C , and L_M to be varied⁵ in order to determine the best configuration regarding maximum $\bar{\eta}_{\text{design}}$ [Figure A.35 (a)]. The LLC converter is operated above resonance to achieve low switching losses [35] and thus, it is more convenient to consider Z_0 and ω_0 instead of L_1 and C to design the LLC converter:

$$Z_0 \approx \sqrt{\frac{L_1 + n^2 L_2}{C}}, \quad \omega_0 \approx \frac{1}{\sqrt{(L_1 + n^2 L_2)C}}. \quad (\text{A.95})$$

⁵ L_2 only considers parasitic inductances and remains approximately constant.

The design algorithm searches for the maximum average efficiency within a discrete number of turns ratios n_i , characteristic impedances $\vec{Z}_{0,j}$, resonance frequencies $\omega_{0,k}$ and magnetizing inductances $L_{M,i}$.⁶

$$\begin{aligned}\vec{n} &= (14 \ 15 \ 16 \ 17 \ 18 \ 19 \ 20 \ 21 \ 22 \ 23 \ 24)^T, \\ \vec{Z}_0 &= Z_{0,\max}(n, \omega_0, L_M) \cdot (0.975 \ 0.95 \ 0.925 \ 0.90 \ 0.875 \ 0.85)^T, \\ \vec{\omega}_0 &= 2\pi f_S \cdot (0.95 \ 0.9 \ 0.85 \ 0.8 \ 0.7 \ 0.6 \ 0.4 \ 0.2 \ 0.1)^T, \\ \vec{L}_M &= (1600 \ \mu\text{H} \ 800 \ \mu\text{H} \ 400 \ \mu\text{H} \ 200 \ \mu\text{H} \ 100 \ \mu\text{H})^T.\end{aligned}\tag{A.96}$$

With phase shift modulation (cf. Section 3.1.1), the maximum average efficiency, $\bar{\eta}_{\text{design}} = 90.0\%$, is achieved for:

- $n = 20$,
- $L_1 + n^2 L_2 = 55.4 \ \mu\text{H}$ ($\approx L$),
- $C = 93.3 \ \text{nF}$ ($\omega_0 = 2\pi \cdot 70 \cdot 10^3 \ \text{s}^{-1}$, $Z_0 = 0.975 Z_{\max} = 24.4 \ \Omega$),
- $L_M = 1.6 \ \text{mH}$ (Figure A.36).

The result depicted in Figure A.36 justifies the step sizes selected for \vec{n} , \vec{Z}_0 , $\vec{\omega}_0$, and \vec{L}_m : around the maximum average efficiency of 90.0% a single step change causes $\bar{\eta}_{\text{design,PS}}$ to change by less than 0.2% [around the maximum, the largest change (0.17%) occurs between $\omega_0 = 2\pi \cdot 70 \cdot 10^3 \ \text{s}^{-1}$ and $\omega_0 = 2\pi \cdot 80 \cdot 10^3 \ \text{s}^{-1}$ in Figure A.36 (c)].

The average efficiency achieved for the LLC converter is better than the average efficiency achieved for the DAB converter if phase shift modulation is employed (DAB: $\bar{\eta}_{\text{design,PS}} = 89.5\%$, Section A.2.1). It is, however, significantly below the average efficiency of the DAB if optimal modulation parameters are employed (DAB: $\bar{\eta}_{\text{design,opt}} = 93.7\%$).

A.4.4 Design Results, Optimal Modulation

With optimal duty ratios D_1 and D_2 (with respect to minimal losses, Section 5.2.1), the maximum average efficiency of 93.9% is achieved for:

- $n = 17$,
- $L_1 + n^2 L_2 = 38.3 \ \mu\text{H}$ ($\approx L$),

⁶The design considers $Z_0 \leq 0.975 \cdot Z_{0,\max}$ instead of $Z_0 \leq 1.0 \cdot Z_{0,\max}$ in order to maintain a certain margin to the theoretically calculated maximum characteristic impedance $Z_{0,\max}$.

<i>Property</i>	<i>Value</i>	<i>Description</i>
<i>Maximum Average Efficiency:</i>		
$\bar{\eta}_{\text{design}}$	90.0%	maximum average converter efficiency calculated with (A.1), (A.2), (A.3), and (A.4)
<i>HV Side Switches T_1, T_2, T_3, T_4 ($i = 1 \dots 4$):</i>		
$\max(V_{D_S, T_i, \text{peak}})$	450 V	maximum HV switch voltages
$\max(I_{D, T_i, \text{peak}})$	23.2 A	max. instantaneous HV switch current
$\max(I_{D, T_i})$	10.0 A	maximum HV switch RMS current
<i>LV Side Switches T_5, T_6, T_7, T_8 ($i = 5 \dots 8$):</i>		
$\max(V_{D_S, T_i, \text{peak}})$	16 V	maximum LV switch voltages
$\max(I_{D, T_i, \text{peak}})$	465 A	max. instantaneous LV switch current
$\max(I_{D, T_i})$	203 A	maximum LV switch RMS currents
<i>Transformer:</i>		
n	20	turns ratio
L_M	1.6 mH	magn. ind. value (HV side referred)
$\max(I_{AC1})$	14.2 A	HV windings, max. RMS curr.
$\max(I_{AC2})$	287 A	LV windings, max. RMS curr.
$\max(B_{\text{tr, core, peak}})$	138 mT	peak transformer flux densities
<i>HF Inductor L:</i>		
L	55.4 μH	inductance value
$\max(I_{L, \text{peak}})$	23.2 A	max. instantaneous inductor current
$\max(I_L)$	14.2 A	maximum inductor RMS current
<i>HF Capacitor C:</i>		
C	93.3 nF	capacitance value
$\max(V_{C, \text{peak}})$	342 V	max. instantaneous capacitor voltage
$\max(I_C)$	14.2 A	maximum capacitor RMS current
<i>HV Side DC Capacitor C_{DC1}:</i>		
$\max(I_{C_{DC1}})$	11.4 A	maximum capacitor RMS current
<i>LV Side DC Capacitor C_{DC2}:</i>		
$\max(I_{C_{DC2}})$	271 A	maximum capacitor RMS current

Table A.13: Design summary for the LLC converter operated with phase shift modulation.

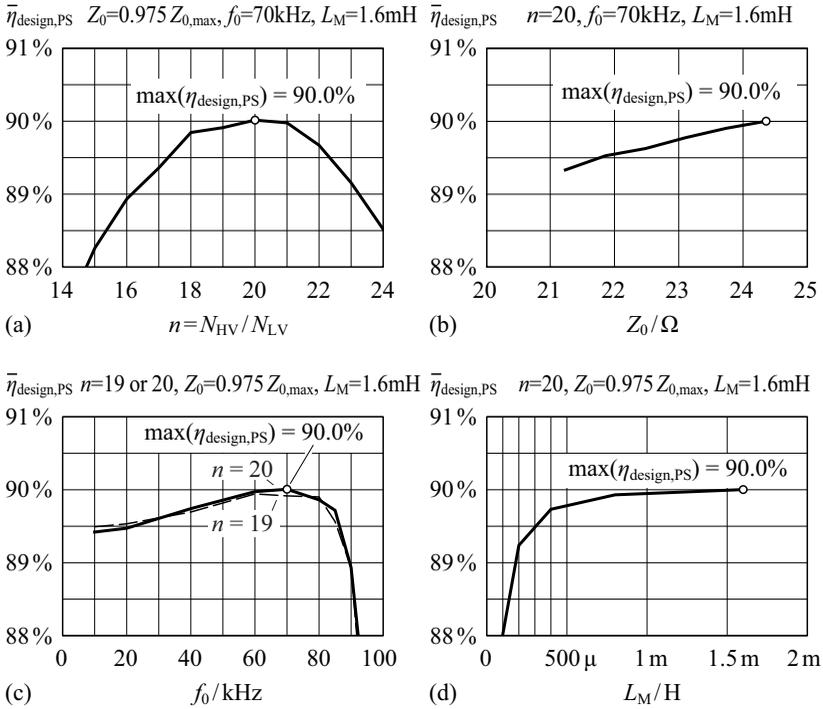


Figure A.36: Average efficiency, $\bar{\eta}_{\text{design,PS}}$, calculated for the LLC converter if phase shift modulation is employed; the maximum average converter efficiency is 90.0% for $n = 20$, $Z_0 = 0.975 Z_{\text{max}} = 24.4 \Omega$, $\omega_0 = 70 \cdot 10^3 \text{ s}^{-1}$, and $L_M = 400 \mu\text{H}$.

- $C = 135 \text{ nF}$ ($\omega_0 = 2\pi \cdot 70 \cdot 10^3 \text{ s}^{-1}$, $Z_0 = 0.775 Z_{\text{max}} = 16.9 \Omega$),
- $L_M = 400 \mu\text{H}$ (Figure A.37).

The calculation employs discrete values for n , ω_0 , and L_M according to (A.96). However, a higher number of considered impedance values is needed to find the maximum average converter efficiency:

$$\vec{Z}_0 = Z_{0,\text{max}}(n, \omega_0, L_M) \cdot (0.975 \quad 0.95 \quad 0.925 \quad 0.90 \quad \dots \quad 0.525 \quad 0.5)^T. \tag{A.97}$$

The result depicted in Figure A.37 justifies the step sizes selected for \vec{n} , \vec{Z}_0 , $\vec{\omega}_0$, and \vec{L}_m : around the maximum average efficiency of 93.9% a single step

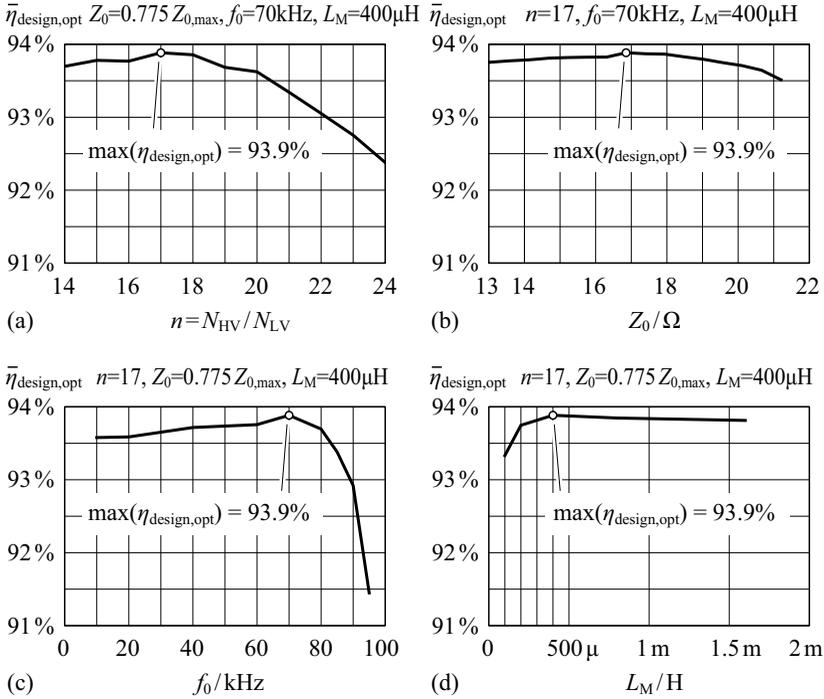


Figure A.37: Average efficiency $\bar{\eta}_{\text{design,opt}}$ of the LLC converter, obtained for efficiency optimal modulation parameters D_1 and D_2 and for different n , Z_0 , ω_0 , and L_M ; maximum average converter efficiency is 93.9% for $n = 17$, $\omega_0 = 70 \cdot 10^3 \text{ s}^{-1}$, $Z_0 = 0.775 Z_{\text{max}} = 16.9 \Omega$, and $L_M = 400 \mu\text{H}$.

change causes $\bar{\eta}_{\text{design,PS}}$ to change by less than 0.2% [around the maximum, the largest change (0.19%) occurs between $\omega_0 = 2\pi \cdot 70 \cdot 10^3 \text{ s}^{-1}$ and $\omega_0 = 2\pi \cdot 80 \cdot 10^3 \text{ s}^{-1}$ in Figure A.37 (c)].

Compared to the DAB converter, only little improvement is achieved: for the DAB, a maximum average efficiency of 93.7% is calculated if optimal modulation parameters are employed; with the suboptimal modulation schemes still $\bar{\eta}_{\text{design}} = 93.5\%$ is achieved for the DAB (Section A.2). Thus, the increased complexity of the LLC converter, the increased inductance required for L and the additionally required capacitor C render the LLC converter less attractive than the DAB converter.

<i>Property</i>	<i>Value</i>	<i>Description</i>
<i>Maximum Average Efficiency:</i>		
$\bar{\eta}_{\text{design}}$	93.9%	maximum average converter efficiency calculated with (A.1), (A.2), (A.3), and (A.4)
<i>HV Side Switches</i> T_1, T_2, T_3, T_4 ($i = 1 \dots 4$):		
$\max(V_{D_{S,T_i,\text{peak}}})$	450 V	maximum HV switch voltages
$\max(I_{D,T_i,\text{peak}})$	22.2 A	max. instantaneous HV switch current
$\max(I_{D,T_i})$	9.8 A	maximum HV switch RMS current
<i>LV Side Switches</i> T_5, T_6, T_7, T_8 ($i = 5 \dots 8$):		
$\max(V_{D_{S,T_i,\text{peak}}})$	16 V	maximum LV switch voltages
$\max(I_{D,T_i,\text{peak}})$	377 A	max. instantaneous LV switch current
$\max(I_{D,T_i})$	164 A	maximum LV switch RMS currents
<i>Transformer:</i>		
n	17	turns ratio
L_M	400 μH	magn. ind. value (HV side referred)
$\max(I_{AC1})$	13.8 A	HV windings, max. RMS curr.
$\max(I_{AC2})$	231 A	LV windings, max. RMS curr.
$\max(B_{\text{tr,core,peak}})$	131 mT	peak transformer flux densities
<i>HF Inductor</i> L :		
L	38.4 μH	inductance value
$\max(I_{L,\text{peak}})$	22.2 A	max. instantaneous inductor current
$\max(I_L)$	13.8 A	maximum inductor RMS current
<i>HF Capacitor</i> C :		
C	135 nF	capacitance value
$\max(V_{C,\text{peak}})$	230 V	max. instantaneous capacitor voltage
$\max(I_C)$	13.8 A	maximum capacitor RMS current
<i>HV Side DC Capacitor</i> C_{DC1} :		
$\max(I_{C_{DC1}})$	9.3 A	maximum capacitor RMS current
<i>LV Side DC Capacitor</i> C_{DC2} :		
$\max(I_{C_{DC2}})$	122 A	maximum capacitor RMS current

Table A.14: Design summary for the LLC converter operated with optimal duty ratios D_1 and D_2 (with respect to minimum converter losses, cf. Section 5.2.1).

A.5 Full Bridge Converter Design

A.5.1 Mode of Operation

Figure A.38 depicts the bidirectional and isolated full bridge converter with a voltage sourced full bridge on the HV side (using the DC capacitor C_{DC1}) and a current sourced full bridge on the LV side (using the DC inductor L_{DC2}) [135]. The circuit structure of the full bridge converter is not symmetric (as opposed to the DAB) and thus, depending on the actual direction of power transfer, 2 different modulation schemes are employed.

- HV \rightarrow LV (*forward mode*, Figure A.39): the HV side full bridge applies the AC voltage v_{AC1} to the series connection of the inductance L and the primary side winding of the HF transformer. The LV side full bridge rectifies the secondary side transformer voltage v_{AC2} and the second order filter, formed by the DC inductor L_{DC2} and the DC capacitor C_{DC2} , filters the rectified transformer voltage.
- LV \rightarrow HV (*reverse mode*, Figure A.40): the LV side full bridge alternately forces the secondary side transformer current i_{AC2} to become equal to either $+i_{L_{DC2}}$ or $-i_{L_{DC2}}$. The HV side full bridge rectifies the primary side transformer current i_{AC1} and the DC capacitor C_{DC1} provides filtering of the output voltage V_1 .

In particular the HF inductance L , needed to achieve soft switching for the MOSFETs T_1, T_2, T_3 , and T_4 [143], causes a major difficulty during the reverse mode of operation: then, the LV full bridge repeatedly connects L_{DC2} in series to L which causes voltage spikes on v_{AC2} and large losses. Therefore,

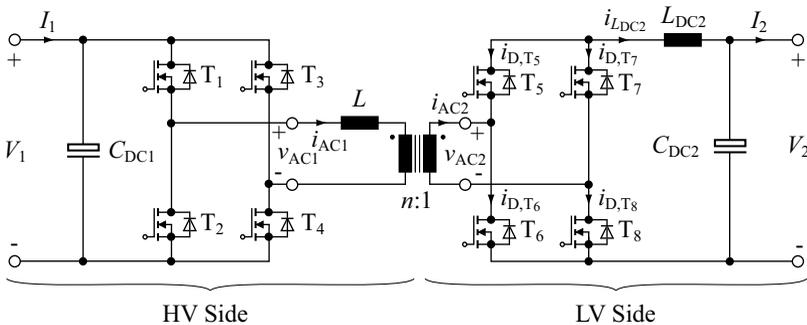


Figure A.38: Bidirectional full bridge converter with LV side DC inductor.

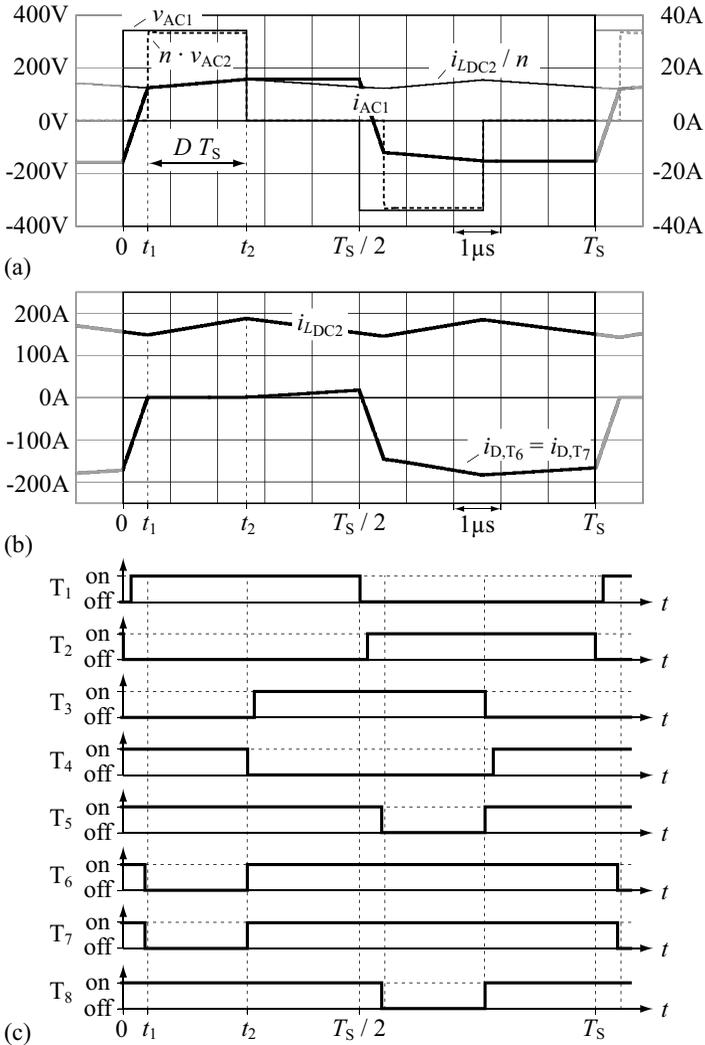


Figure A.39: (a) Simulated voltage and current waveforms of the full bridge converter; (b) simulated currents through the DC inductor L_{DC2} and through the LV switches T_6 and T_7 [the currents through T_5 and T_8 are given with $i_{D,T_5}(t) = i_{D,T_8}(t) = i_{D,T_6}(t - T_S/2)$]; (c) employed gate signals on the assumption of zero turn-on time delays and zero turn-off time delays; $V_1 = 340$ V, $V_2 = 12$ V, $P_2 = 2$ kW, $f_S = 100$ kHz.

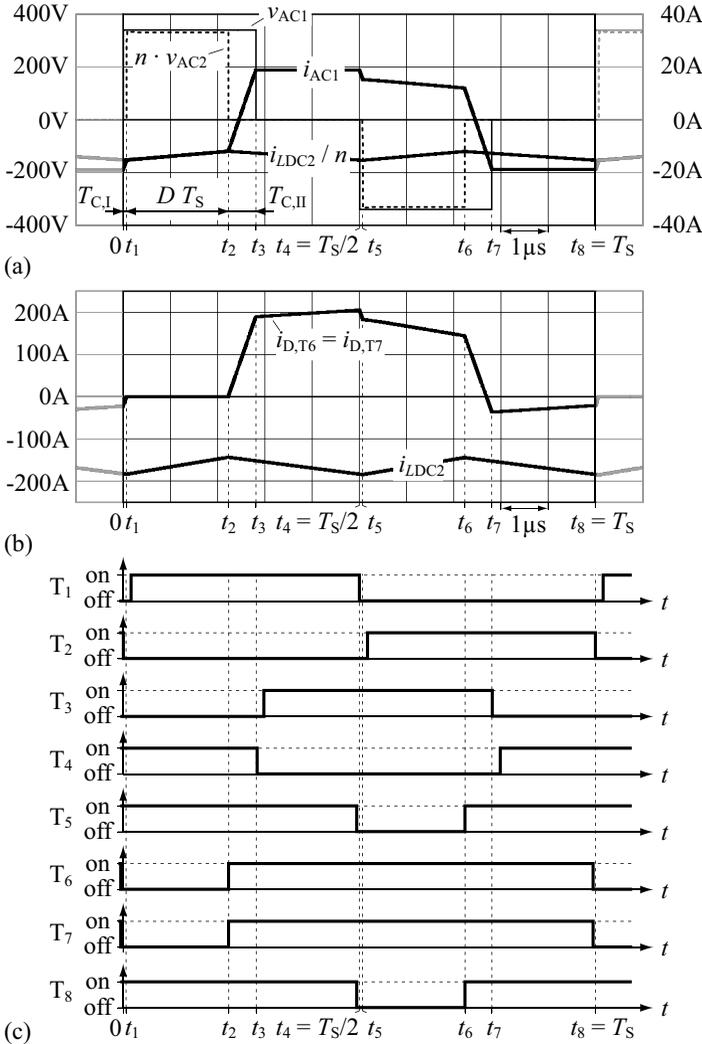


Figure A.40: (a) Simulated voltage and current waveforms of the full bridge converter; (b) simulated currents through the DC inductor L_{DC2} and through the LV switches T_6 and T_7 [the currents through T_5 and T_8 are given with $i_{D,T_5}(t) = i_{D,T_8}(t) = i_{D,T_6}(t - T_S/2)$]; (c) employed gate signals on the assumption of zero turn-on time delays and zero turn-off time delays; $V_1 = 340$ V, $V_2 = 12$ V, $P_1 = -2$ kW, $f_S = 100$ kHz.

snubber circuits are typically used to achieve high converter efficiency [135]; in this Section, however, a special modulation scheme is proposed in order to avoid additional circuitry.

Power Transfer from the HV Port to the LV Port (Forward Mode)

Figure A.39 shows typical current and voltage waveforms of the full bridge converter if power is transferred to the LV port ($V_1 = 340\text{ V}$, $V_2 = 12\text{ V}$, $P_2 = 2\text{ kW}$). At $t = 0$, the HV full bridge switches from $v_{AC1} \approx 0$ to $v_{AC1} \approx V_1$. During $0 < t < t_1$ the current i_{AC1} rises until it reaches the primary side referred DC inductor current $i_{L_{DC2}}(t)/n$ at $t = t_1$. During the subsequent time interval, $t_1 < t < t_2$, the LV full bridge applies $v_{AC2} \approx V_2$ while $v_{AC1} \approx V_1$ remains and the converter transfers power from the HV side to the LV side. Consequently, the relative duration of the active power transfer time interval, T_{rel} , is:

$$T_{\text{rel}} = \frac{t_2 - t_1}{T_S/2}. \quad (\text{A.98})$$

The respective duty cycle, defined according to Figure A.39, is thus:

$$D = \frac{T_{\text{rel}}}{2} = \frac{t_2 - t_1}{T_S}. \quad (\text{A.99})$$

The remaining time interval of the regarded half-cycle, $t_2 < t < T_S/2$, is the freewheeling time interval and is used to adjust V_2 and to control the actual output power. During the second half-cycle, $T_S/2 < t < T_S$, the transformer voltages and the transformer currents repeat with negative sign.

In summary, during the converter operation in forward mode, each half-cycle consists of 3 different time intervals:

1. $0 < t < t_1$: current commutation time interval used to reverse the current in the HF inductance L ,
2. $t_1 < t < t_2$: active power transfer; similar to a buck converter, the current through the DC inductor L_{DC2} increases,
3. $t_2 < t < T_S/2$: freewheeling time interval.

Power Transfer from the LV Port to the HV Port (Reverse Mode)

During reverse mode of operation, at $t = 0$, the HV full bridge applies $v_{AC1} \approx V_1$. Moreover, the transformer current $i_{AC1}(0)$ needs to be more negative than the current through the DC inductor at $t = 0$, i.e. $i_{AC1}(0) < i_{L_{DC2}}(0)/n$, in order to achieve low switching losses (Figure A.40). Thus, the absolute value of the transformer current, $|i_{AC1}(t)|$, decreases during $0 < t < t_1$ until it

becomes equal to $|i_{L_{DC2}}(t)/n|$ at $t = t_1$. Since the switches T_6 and T_7 are turned off at $t = 0$ (i.e. diode operation), the body diodes of T_6 and T_7 stop to conduct at $t = t_1$ (provided that the MOSFETs' body diodes are ideal). During $t_1 < t < t_2$, the current through L remains equal to the primary side referred DC inductor current,⁷ $i_{AC1}(t) = i_{L_{DC2}}(t)/n$, and the converter transfers power from the LV port to the HV port. At $t = t_2$, the switches T_6 and T_7 are turned on and the LV full bridge generates $v_{AC2} \approx 0$. The subsequent time interval, $t_2 < t < t_3$, is the current commutation interval which is used to prepare the transformer current for the beginning of the next half-cycle. The freewheeling time interval ($t_3 < t < T_S/2$) is finally used to adjust V_1 and to control the output power of the converter. Again, the transformer voltages and the transformer currents repeat with negative sign during the second half-cycle ($T_S/2 < t < T_S$).

The duration of the time interval of active power transfer defines the duty cycle:

$$D = \frac{t_2 - t_1}{T_S}. \quad (\text{A.100})$$

In summary, during reverse mode of operation, each half-cycle consists of 4 different time intervals:

1. $0 < t < t_1$: current commutation time interval used to achieve $i_{AC1}(t_1) = i_{L_{DC2}}(t_1)/n$,
2. $t_1 < t < t_2$: active power transfer similar to a boost converter,
3. $t_2 < t < t_3$: current commutation time interval used to reverse the current through the HF inductance L ,
4. $t_3 < t < T_S/2$: freewheeling time interval.

A.5.2 Converter Design

According to Figure A.40, the semiconductor and transformer current stresses are higher for reverse mode of operation. Therefore, the converter is designed for power being transferred from the LV port to the HV port. Table A.16 summarizes the design results.

Assumptions and Definitions

In order to simplify the calculations, the impact of conduction and copper losses on the transformer currents i_{AC1} and i_{AC2} is neglected. Consequently,

⁷On the assumption of a negligible transformer magnetizing current.

constant transformer currents are considered during the freewheeling time intervals (e.g. $t_3 < t < T_S/2$). Moreover, during the freewheeling time intervals, the switch currents slightly change (Figure A.40), due to the current ripple on $i_{L_{DC2}}$:

$$i_{D,T_5}(t) = i_{D,T_8}(t) = \frac{i_{AC2}(t) - i_{L_{DC2}}(t)}{2} \approx \frac{i_{AC2}(t) - I_2}{2} \quad \forall t_3 < t < T_S/2, \quad (\text{A.101})$$

$$i_{D,T_6}(t) = i_{D,T_7}(t) = \frac{-i_{AC2}(t) - i_{L_{DC2}}(t)}{2} \approx \frac{-i_{AC2}(t) - I_2}{2} \quad \forall t_3 < t < T_S/2. \quad (\text{A.102})$$

At rated power, the change of the switch currents during the freewheeling interval is comparably small [cf. (A.104)] and thus, its impact on the RMS values of the switch currents is neglected, i.e. the approximations given in (A.101) and (A.102) are used to design the full bridge converter.

Throughout the design, three important current values are needed (defined with respect to Figure A.40):

$$\begin{aligned} I_{L_{DC2},0} &= i_{AC2}(0), \\ I_{L_{DC2},1} &= i_{AC2}(t_1), \\ I_{L_{DC2},2} &= i_{AC2}(t_2). \end{aligned} \quad (\text{A.103})$$

Moreover, the magnetizing current of the transformer is neglected, i.e. $i_{AC1} = i_{AC2}/n$ is considered.

At rated output power, the maximum peak-to-peak value of the current ripple on $i_{L_{DC2}}(t)$ is assumed to be equal or less than 40% of the output current [116],

$$\Delta I_{L_{DC2},\max} = I_{L_{DC2},2} - I_{L_{DC2},1} \leq 40\% |I_2| \quad \forall P_1 = -2.22 \text{ kW}, \quad (\text{A.104})$$

and thus, the currents $I_{L_{DC2},1}$ and $I_{L_{DC2},2}$ are calculated according to:

$$\begin{aligned} I_{L_{DC2},1} &= I_2 - \frac{\Delta I_{L_{DC2}}}{2}, \\ I_{L_{DC2},2} &= I_2 + \frac{\Delta I_{L_{DC2}}}{2}. \end{aligned} \quad (\text{A.105})$$

For the current $I_{L_{DC2},0}$, a value of

$$I_{L_{DC2},0} = 1.2 \cdot I_{L_{DC2},1} \quad (\text{A.106})$$

is assumed in order to ensure low switching losses on the LV side.

The commutation times $T_{C,I}$ and $T_{C,II}$, depicted in Figure A.40, are given with:

$$T_{C,I} = \frac{L}{V_1} \left(\frac{|I_{L_{DC2,0}}| - |I_{L_{DC2,1}}|}{n} \right), \quad (\text{A.107})$$

$$T_{C,II} = \frac{L}{V_1} \left(\frac{|I_{L_{DC2,0}}| + |I_{L_{DC2,2}}|}{n} \right). \quad (\text{A.108})$$

The duration $T_{C,I} + T_{C,II}$ is specified for the maximum voltage $V_2 = V_{2,\max} = 16 \text{ V}$ and for the minimum voltage $V_1 = V_{1,\min} = 240 \text{ V}$ [there, maximum duty cycle occurs, cf. (A.111)]:⁸

$$T_{C,\max} = (T_{C,I} + T_{C,II})_{\max} \Big|_{V_1=V_{1,\min}, V_2=V_{2,\max}} = 7.5\% T_S. \quad (\text{A.109})$$

For the freewheeling time interval, a minimum duration of $2.5\% T_S$ is used:

$$T_{\text{free},\min} = T_S/2 - t_3 \leq 2.5\% T_S. \quad (\text{A.110})$$

The full bridge converter is designed for an assumed converter efficiency of 90%. Table A.15 summarizes all the assumptions needed to carry out the converter design.

Transformer Turns Ratio

In steady-state operation, the duty cycle defined in Figure A.40 is equal to:

$$D = \frac{nV_2}{2V_1} \quad (\text{A.111})$$

(on the assumptions of a lossless converter and constant DC voltages V_1 and V_2). Thus, the maximum duty cycle occurs for $V_1 = V_{1,\min} = 240 \text{ V}$ and $V_2 = V_{2,\max} = 16 \text{ V}$; there, (A.111) represents an upper limit to the transformer turns ratio n . Furthermore, the commutation times $T_{C,I}$ and $T_{C,II}$ and the minimum freewheeling time $T_{\text{free},\min}$ need to be included into the calculation of n , since $T_{C,I}$, $T_{C,II}$, and $T_{\text{free},\min}$ reduce the maximum duration of the active power transfer time interval (e.g. $t_1 < t < t_2$ in Figure A.40):

$$D_{\max} = 0.5 - f_S \cdot (T_{C,I} + T_{C,II} + T_{\text{free},\min}). \quad (\text{A.112})$$

The transformer turns ratio results from (A.111) and (A.112):

$$n = \left[\frac{V_1}{V_2} \cdot [1 - 2f_S \cdot (T_{C,I} + T_{C,II} + T_{\text{free},\min})] \right] \Big|_{V_1=V_{1,\min}, V_2=V_{2,\max}} = 12. \quad (\text{A.113})$$

⁸For $V_1 = V_{1,\min}$ and $V_2 = V_{2,\max}$, the maximum duty cycle results. With decreasing values V_2 (and constant $V_1 = V_{1,\min}$), the duty cycle decreases [cf. (A.111)], while $T_{C,I}$ and $T_{C,II}$ increase (due to the increasing port current I_2). Within the specified voltage ranges (Table 1.4), however, the maximum value of $(D/f_S) + T_{C,I} + T_{C,II}$ occurs for $V_1 = V_{1,\min}$ and $V_2 = V_{2,\max}$. On the assumptions given in Table A.15, $(D/f_S) + T_{C,I} + T_{C,II} = T_S/2$ would occur for $V_2 \approx 3 \text{ V}$ (provided that $V_1 = V_{1,\min}$).

<i>Property</i>	<i>Assumption</i>	<i>Description</i>
η_{est}	90%	estimated converter efficiency
$\Delta I_{L_{\text{DC}2},\text{max}}$	40% $ I_2 $ ($P_1 = -2 \text{ kW} / \eta_{\text{est}}$ $\approx -2.22 \text{ kW}$)	maximum peak-to-peak value of the current ripple on $i_{L_{\text{DC}2}}(t)$
$I_{L_{\text{DC}2},0}$	$1.2 \cdot I_{L_{\text{DC}2},1}$	inductor current at $t = 0$, used to achieve low switching losses on the LV side
$T_{\text{C},\text{max}}$	7.5% T_S	duration of $T_{\text{I},\text{C}} + T_{\text{II},\text{C}}$ at $V_1 = 240 \text{ V}$ and $V_2 = 16 \text{ V}$
$T_{\text{free},\text{min}}$	2.5% T_S	minimum duration of the freewheeling time interval

Table A.15: Assumptions used to design the full bridge converter.

DC Inductor $L_{\text{DC}2}$

The specified maximum peak-to-peak value of the current ripple, $\Delta I_{L_{\text{DC}2},\text{max}}$, represents a lower boundary to the inductance value of $L_{\text{DC}2}$, whereas $\Delta I_{L_{\text{DC}2}}$ is equal to

$$\Delta I_{L_{\text{DC}2}} = \left(\frac{V_1}{n} - V_2 \right) \frac{D}{f_S L_{\text{DC}2}} \leq 40\% \frac{|P_1|}{V_2}. \quad (\text{A.114})$$

Thus, the inductance value of $L_{\text{DC}2}$ is determined with:

$$L_{\text{DC}2} = \min \left[\left(\frac{V_1}{n} - V_2 \right) \frac{D}{40\% \frac{|P_1|}{V_2} f_S} \right] \left| \begin{array}{l} V_{1,\text{min}} \leq V_1 \leq V_{1,\text{max}}, \\ V_{2,\text{min}} \leq V_2 \leq V_{2,\text{max}}, \\ P_1 = -2.22 \text{ kW} \end{array} \right. = 0.83 \mu\text{H}. \quad (\text{A.115})$$

The peak current through $L_{\text{DC}2}$ is obtained from

$$\min(i_{L_{\text{DC}2}}) = \min \left(\frac{P_1}{V_2} - \frac{\Delta I_{L_{\text{DC}2}}}{2} \right) = -226 \text{ A} \quad (\text{A.116})$$

in reverse mode of operation [accordingly, $\max(i_{L_{\text{DC}2}}) = 226 \text{ A}$ applies in forward mode]. The respective maximum RMS current is

$$\max(I_{L_{\text{DC}2}}) = \max \left[\sqrt{\left(\frac{P_1}{V_2} \right)^2 + \left(\frac{\Delta I_{L_{\text{DC}2}}}{2\sqrt{3}} \right)^2} \right] = 202 \text{ A}. \quad (\text{A.117})$$

HF Inductance L

The HF inductance L is calculated with (A.107), (A.108), and with the specified maximum commutation time $T_{C,\max}$:

$$L = \frac{T_{C,\max}}{[(T_{C,I} + T_{C,II})/L] \Big|_{V_1=V_{1,\min}, V_2=V_{2,\max}, P_1=-2.22 \text{ kW}}} = 6.4 \mu\text{H}. \quad (\text{A.118})$$

The maximum peak inductor current, $\max(I_{L,\text{peak}})$, is determined for $P_1 = -2.22 \text{ kW}$ within the specified input and output voltage ranges:

$$\max(I_{L,\text{peak}}) = \max\left(\frac{|I_{L_{\text{DC}2,0}}|}{n}\right) = 22.6 \text{ A}. \quad (\text{A.119})$$

Transformer Currents

The primary side transformer RMS current is obtained from:

$$I_{\text{AC}1} = \left\{ \frac{2f_s}{n^2} \left[\frac{T_{C,I}}{3} (I_{L_{\text{DC}2,0}}^2 + I_{L_{\text{DC}2,0}} I_{L_{\text{DC}2,1}} + I_{L_{\text{DC}2,1}}^2) + \frac{D}{3f_s} (I_{L_{\text{DC}2,1}}^2 + I_{L_{\text{DC}2,1}} I_{L_{\text{DC}2,2}} + I_{L_{\text{DC}2,2}}^2) + \frac{T_{C,II}}{3} (I_{L_{\text{DC}2,0}}^2 - I_{L_{\text{DC}2,0}} I_{L_{\text{DC}2,2}} + I_{L_{\text{DC}2,2}}^2) + \frac{0.5 - D - f_s (T_{C,I} + T_{C,II})}{f_s} I_{L_{\text{DC}2,0}}^2 \right] \right\}^{\frac{1}{2}}. \quad (\text{A.120})$$

The maximum values of the primary and secondary side transformer RMS currents are:

$$\begin{aligned} \max(I_{\text{AC}1}) &= 20.0 \text{ A}, \\ \max(I_{\text{AC}2}) &= n \max(I_{\text{AC}1}) = 241 \text{ A}. \end{aligned} \quad (\text{A.121})$$

Transformer Peak Flux Density

The peak flux density in the transformer core is:

$$B_{\text{tr,core,peak}} = \frac{V_1}{N_1} \frac{D}{2f_s A_{\text{tr,core}}} \quad (\text{A.122})$$

(on the assumption of a homogeneously distributed magnetic flux inside the transformer core; stray flux is neglected).

HV Side Switch Currents and Voltages

On the HV side, the peak switch voltages are equal to the maximum port voltage,

$$V_{DS,T_1,\text{peak,max}} = V_{DS,T_2,\text{peak,max}} = V_{DS,T_3,\text{peak,max}} = V_{DS,T_4,\text{peak,max}} = 450 \text{ V.} \quad (\text{A.123})$$

The maximum switch RMS currents are calculated according to (4.1),

$$I_{D,T_1,\text{max}} = I_{D,T_2,\text{max}} = I_{D,T_3,\text{max}} = I_{D,T_4,\text{max}} = \frac{\max(I_{AC1})}{\sqrt{2}} = 14.2 \text{ A,} \quad (\text{A.124})$$

and the peak switch currents are equal to $\max(I_{L,\text{peak}}) = 22.6 \text{ A}$ [cf. (A.119)].

LV Side Switch Currents and Voltages

On the assumption of negligible overvoltage spikes, the peak switch voltages applied to the LV side switches are obtained from:

$$V_{DS,T_5,\text{peak,max}} = V_{DS,T_6,\text{peak,max}} = V_{DS,T_7,\text{peak,max}} = V_{DS,T_8,\text{peak,max}} = \frac{450 \text{ V}}{n} = 37.5 \text{ V.} \quad (\text{A.125})$$

The calculation of the switch RMS currents requires 4 interim current values (cf. Figure A.40),

$$I_{D,T_{LV},1} = -I_{L_{DC2},0} + \frac{I_{L_{DC2},0} - P_1/V_2}{2} [\approx i_{D,T_6}(t_3) \approx i_{D,T_6}(T_S/2)], \quad (\text{A.126})$$

$$I_{D,T_{LV},2} = i_{D,T_6}(t_5) = -I_{L_{DC2},1}, \quad (\text{A.127})$$

$$I_{D,T_{LV},3} = i_{D,T_6}(t_6) = -I_{L_{DC2},2}, \quad (\text{A.128})$$

$$I_{D,T_{LV},4} = \frac{I_{L_{DC2},0} - P_1/V_2}{2} [\approx i_{D,T_6}(t_7) \approx i_{D,T_6}(T_S)]; \quad (\text{A.129})$$

the switch RMS currents are:

$$\begin{aligned}
 I_{D,T_{LV}} = I_{D,T_5} = I_{D,T_6} = I_{D,T_7} = I_{D,T_8} = \\
 \left\{ f_S \left[\frac{T_{C,II}}{3} (I_{D,T_{LV},1}^2 + I_{D,T_{LV},3}^2 + I_{D,T_{LV},3} I_{D,T_{LV},4} + I_{D,T_{LV},4}^2) + \right. \right. \\
 \left. \frac{0.5 - D - f_S (T_{C,I} + T_{C,II})}{f_S} (I_{D,T_{LV},1}^2 + I_{D,T_{LV},4}^2) + \right. \\
 \left. \frac{T_{C,I}}{3} (I_{D,T_{LV},1}^2 + I_{D,T_{LV},1} I_{D,T_{LV},2} + I_{D,T_{LV},2}^2 + I_{D,T_{LV},2}^2 + I_{D,T_{LV},4}^2) + \right. \\
 \left. \left. \frac{D}{3f_S} (I_{D,T_{LV},2}^2 + I_{D,T_{LV},2} I_{D,T_{LV},3} + I_{D,T_{LV},3}^2) \right] \right\}^{\frac{1}{2}}. \quad (A.130)
 \end{aligned}$$

Within the specified input and output voltage ranges and for $P_1 = -2.22$ kW, the maximum switch RMS currents are:

$$I_{D,T_{LV},\max} = \max(I_{D,T_{LV}}) = 157 \text{ A}. \quad (A.131)$$

HV Side Capacitor AC Current

On the assumption of a constant HV port current I_1 , the RMS value of the current through C_{DC1} is:

$$\begin{aligned}
 I_{C_{DC1}} = \left\{ \frac{2f_S}{n^2} \left[\frac{T_{C,I}}{3} (I_{L_{DC2},0}^2 + I_{L_{DC2},0} I_{L_{DC2},1} + I_{L_{DC2},1}^2) + \right. \right. \\
 \left. \frac{D}{3f_S} (I_{L_{DC2},1}^2 + I_{L_{DC2},1} I_{L_{DC2},2} + I_{L_{DC2},2}^2) + \right. \\
 \left. \left. \frac{T_{C,II}}{3} (I_{L_{DC2},0}^2 - I_{L_{DC2},0} I_{L_{DC2},2} + I_{L_{DC2},2}^2) \right] - \left(\frac{P_1}{V_1} \right)^2 \right\}^{\frac{1}{2}}. \quad (A.132)
 \end{aligned}$$

For $V_1 = 240$ V, $V_2 = 11$ V, and $P_1 = -2.22$ kW the maximum capacitor current occurs:

$$I_{C_{DC1},\max} = 10.1 \text{ A}. \quad (A.133)$$

LV Side Capacitor AC Current

On the assumption of a constant LV port current I_2 the RMS value of the current through C_{DC2} is:

$$I_{C_{DC2}} = \frac{\Delta I_{L_{DC2}}}{2\sqrt{3}}; \quad (A.134)$$

the maximum value of $I_{C_{DC2}}$ is:

$$I_{C_{DC2},\max} = 16 \text{ A.} \quad (\text{A.135})$$

Table A.16 summarizes the design results.

A.6 Current Doubler Converter Design

A.6.1 Mode of Operation

Figure A.41 depicts the bidirectional and isolated current doubler topology [144]. Similar to the bidirectional full bridge converter, the actually employed modulation scheme depends on the direction of power transfer.

- HV \rightarrow LV (*forward mode*, Figure A.42): the HV side full bridge applies the AC voltage v_{AC1} to the series connection of the inductance L and the HF transformer. The diodes on the LV side (operated using synchronous rectification) rectify the secondary side transformer voltage v_{AC2} . Finally, the output filter, formed with the DC inductors L_{DC2a} and L_{DC2b} and the DC capacitor C_{DC2} , filters the rectified transformer voltage.
- LV \rightarrow HV (*reverse mode*, Figure A.43): the LV side switches alternately force the secondary side transformer current i_{AC2} to become equal to either $+i_{L_{DC2a}}$ or $-i_{L_{DC2b}}$. The HV side full bridge rectifies the primary side transformer current i_{AC1} and the DC capacitor C_{DC1} provides filtering of the output voltage V_1 .

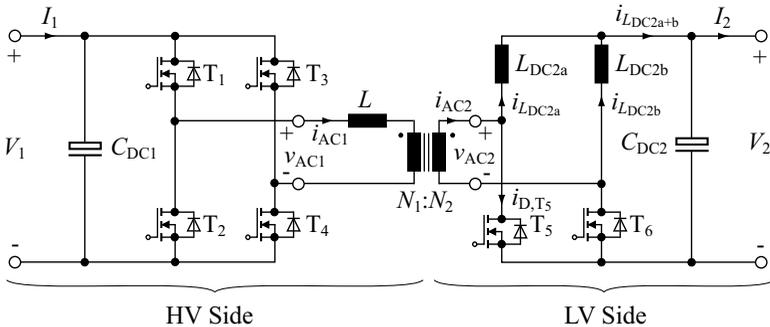


Figure A.41: Bidirectional current doubler topology with LV side DC inductors.

<i>Property</i>	<i>Value</i>	<i>Description</i>
<i>HV Side Switches</i> T ₁ , T ₂ , T ₃ , T ₄ :		
max ($V_{DS,T_{HV,peak}}$)	450 V	maximum HV switch voltages
max ($I_{D,T_{HV,peak}}$)	22.6 A	max. HV switch curr. (instantaneous value)
max ($I_{D,T_{HV}}$)	14.2 A	maximum HV switch currents (RMS value)
<i>LV Side Switches</i> T ₅ , T ₆ , T ₇ , T ₈ :		
max ($V_{DS,T_{LV,peak}}$)	37.5 V	maximum LV switch voltages
max ($I_{D,T_{LV,peak}}$)	236 A	max. LV switch curr. (instantaneous value)
max ($I_{D,T_{LV}}$)	157 A	maximum LV switch currents (RMS value)
<i>Transformer:</i>		
n	12	turns ratio
max (I_{AC1})	10.0 A	HV transformer winding, max. RMS current
max (I_{AC2})	241 A	LV transformer winding, max. RMS current
max ($B_{tr,core,peak}$)	130 mT	for $N_1 = 12$, $N_2 = 1$, and $A_{tr,core} = 308 \text{ mm}^2$ (ELP 58 core, cf. Section A.2.4)
<i>DC Inductor</i> L_{DC2} :		
L_{DC2}	0.83 μH	inductance value
max ($I_{L_{DC2,peak}}$)	226 A	maximum instantaneous inductor current
max ($I_{L_{DC2}}$)	202 A	maximum inductor RMS current
<i>HF Inductor</i> L :		
L	6.4 μH	inductance value
max ($I_{L_{DC2,peak}}$)	22.6 A	maximum instantaneous inductor current
max ($I_{L_{DC2}}$)	20.0 A	maximum inductor RMS current
<i>HV Side DC Capacitor</i> C_{DC1} :		
max ($I_{C_{DC1}}$)	10.1 A	maximum capacitor RMS current
<i>LV Side DC Capacitor</i> C_{DC2} :		
max ($I_{C_{DC2}}$)	16 A	maximum capacitor RMS current

Table A.16: Design summary for the bidirectional full bridge converter.

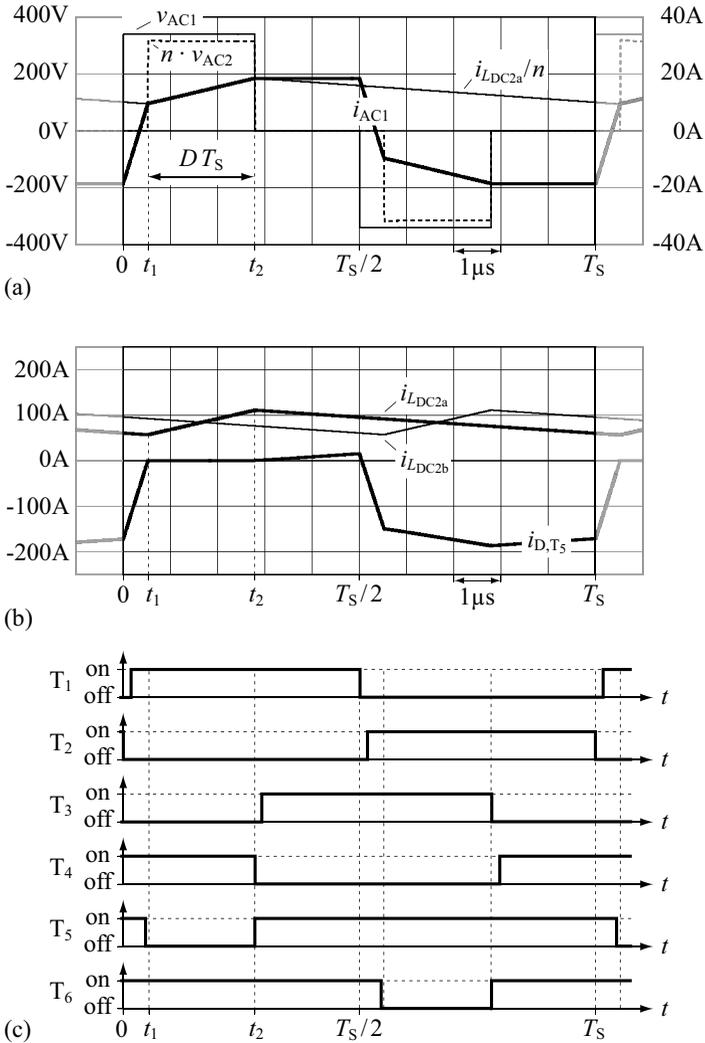


Figure A.42: (a) Simulated voltage and current waveforms of the bidirectional current doubler DC–DC converter; (b) simulated currents through the DC inductors L_{DC2a} and L_{DC2b} and through the LV switch T_5 [the current through T_6 is given with $i_{D,T_6}(t) = i_{D,T_5}(t - T_S/2)$]; (c) employed gate signals for the assumption of zero turn-on time delays and zero turn-off time delays; $V_1 = 340$ V, $V_2 = 12$ V, $P_2 = 2$ kW, $f_S = 100$ kHz.

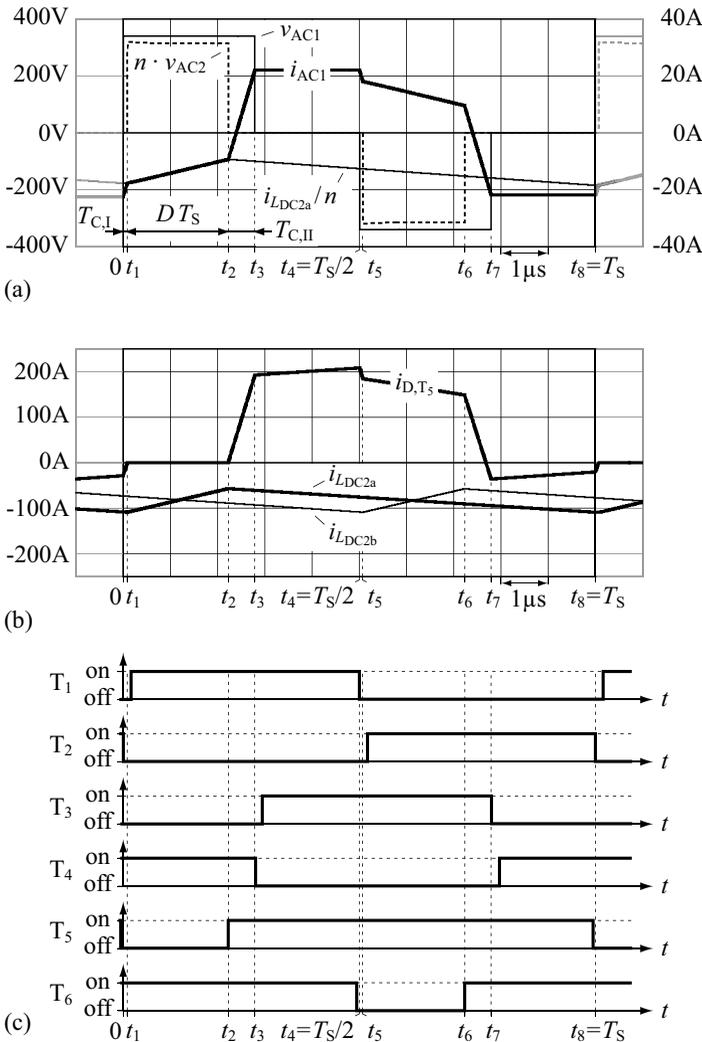


Figure A.43: (a) Simulated voltage and current waveforms of the bidirectional current doubler DC–DC converter; (b) simulated currents through the DC inductors L_{DC2a} and L_{DC2b} and through the LV switch T_5 [the current through T_6 is given with $i_{D,T_6}(t) = i_{D,T_5}(t - T_S/2)$]; (c) employed gate signals on the assumption of zero turn-on time delays and zero turn-off time delays; $V_1 = 340$ V, $V_2 = 12$ V, $P_1 = -2$ kW, $f_s = 100$ kHz.

The employed modulation schemes are identical to the modulation schemes used for the bidirectional full bridge converter (Appendix A.5.1).

A.6.2 Converter Design

According to Figure A.43, the semiconductor and transformer current stresses are higher for reverse mode of operation. Therefore, the converter is designed for power being transferred from the LV port to the HV port. Table A.18 summarizes the design results.

Assumptions and Definitions

In order to simplify the calculations, the impact of conduction and copper losses on the transformer currents i_{AC1} and i_{AC2} is neglected. Consequently, constant transformer currents are considered during the freewheeling time intervals (e.g. $t_3 < t < T_S/2$).

Throughout the design, three important current values are needed (defined with respect to Figure A.43):

$$\begin{aligned} I_{L_{DC2a},0} &= i_{AC1}(0), \\ I_{L_{DC2a},1} &= i_{AC1}(t_1), \\ I_{L_{DC2a},2} &= i_{AC1}(t_2). \end{aligned} \quad (\text{A.136})$$

Moreover, the magnetizing current of the transformer is neglected, i.e. $i_{AC1} = i_{AC2}/n$ is considered.

The peak-to-peak value of the current ripple on $i_{L_{DC2a}}(t)$ [and on $i_{L_{DC2b}}(t)$] is equal to

$$\Delta I_{L_{DC2a}} = \Delta I_{L_{DC2b}} = I_{L_{DC2a},2} - I_{L_{DC2a},1} \quad (\text{A.137})$$

and thus, the currents $I_{L_{DC2a},1}$ and $I_{L_{DC2a},2}$ are calculated according to:

$$\begin{aligned} I_{L_{DC2a},1} &= \frac{I_2}{2} - \frac{\Delta I_{L_{DC2a}}}{2}, \\ I_{L_{DC2a},2} &= \frac{I_2}{2} + \frac{\Delta I_{L_{DC2a}}}{2}. \end{aligned} \quad (\text{A.138})$$

At rated output power, the maximum peak-to-peak value of the current ripple on $i_{L_{DC2a}}(t) + i_{L_{DC2b}}(t)$ is assumed to be equal or less than 40% of the output current,

$$\begin{aligned} \Delta I_{L_{DC2a+b},\max} &= \max [i_{L_{DC2a}}(t) + i_{L_{DC2b}}(t)] - \min [i_{L_{DC2a}}(t) + i_{L_{DC2b}}(t)] \\ &\leq 40\% |I_2| \quad \forall P_1 = -2.22 \text{ kW}. \end{aligned} \quad (\text{A.139})$$

For the current $I_{L_{DC2a},0}$, a value of

$$I_{L_{DC2a},0} = 1.2 \cdot I_{L_{DC2a},1} \quad (\text{A.140})$$

is assumed in order to ensure low switching losses on the LV side.

The commutation times $T_{C,I}$ and $T_{C,II}$ depicted in Figure A.43 are given with:

$$T_{C,I} = \frac{L}{V_1} \left(\frac{|I_{L_{DC2a},0}| - |I_{L_{DC2a},1}|}{n} \right), \quad (\text{A.141})$$

$$T_{C,II} = \frac{L}{V_1} \left(\frac{|I_{L_{DC2a},0}| + |I_{L_{DC2a},2}|}{n} \right). \quad (\text{A.142})$$

The duration $T_{C,I} + T_{C,II}$ is specified for the maximum voltage $V_2 = V_{2,\max} = 16 \text{ V}$ and the minimum voltage $V_1 = V_{1,\min} = 240 \text{ V}$ [there, the maximum duty cycle occurs, cf. (A.145) and Appendix A.5.2]:

$$T_{C,\max} = (T_{C,I} + T_{C,II})_{\max} \Big|_{V_1=V_{1,\min}, V_2=V_{2,\max}} = 7.5\% T_S. \quad (\text{A.143})$$

For the freewheeling time interval, a minimum duration of $2.5\% T_S$ is used:

$$T_{\text{free},\min} = T_S/2 - t_3 \leq 2.5\% T_S. \quad (\text{A.144})$$

The bidirectional current doubler DC–DC converter is designed for an assumed converter efficiency of 90%. Table A.17 summarizes all the assumptions needed to carry out the converter design.

Transformer Turns Ratio

In steady-state operation, the duty cycle defined in Figure A.43 is equal to:

$$D = \frac{nV_2}{V_1} \quad (\text{A.145})$$

(on the assumptions of a lossless converter and constant DC voltages V_1 and V_2). Thus, the maximum duty cycle occurs for $V_1 = V_{1,\min} = 240 \text{ V}$ and $V_2 = V_{2,\max} = 16 \text{ V}$; there, (A.145) represents an upper limit to the transformer turns ratio n . Furthermore, the commutation times $T_{C,I}$ and $T_{C,II}$ and the minimum freewheeling time $T_{\text{free},\min}$ need to be included into the calculation of n , since $T_{C,I}$, $T_{C,II}$, and $T_{\text{free},\min}$ reduce the maximum duration of the active power transfer time interval (e.g. $t_1 < t < t_2$ in Figure A.43):

$$D_{\max} = 0.5 - f_S \cdot (T_{C,I} + T_{C,II} + T_{\text{free},\min}). \quad (\text{A.146})$$

The transformer turns ratio results from (A.145) and (A.146):

$$n = \left[\frac{V_1}{2V_2} \cdot [1 - 2f_S \cdot (T_{C,I} + T_{C,II} + T_{\text{free},\min})] \right] \Big|_{V_1=V_{1,\min}, V_2=V_{2,\max}} = 6. \quad (\text{A.147})$$

<i>Property</i>	<i>Assumption</i>	<i>Description</i>
η_{est}	90%	estimated converter efficiency
$\Delta I_{L_{\text{DC}2\text{a}+\text{b}},\text{max}}$	40% $ I_2 $ ($P_1 = -2 \text{ kW} / \eta_{\text{est}}$ $\approx -2.22 \text{ kW}$)	maximum peak-to-peak value of the current ripple on $i_{L_{\text{DC}2\text{a}}}(t) + i_{L_{\text{DC}2\text{b}}}(t)$
$I_{L_{\text{DC}2\text{a}},0}$	$1.2 \cdot I_{L_{\text{DC}2\text{a}},1}$	ind. current at $t = 0$, used to achieve low switching losses on the LV side
$T_{\text{C},\text{max}}$	7.5% T_{S}	duration of $T_{\text{I,C}} + T_{\text{II,C}}$ at $V_1 = 240 \text{ V}$ and $V_2 = 16 \text{ V}$
$T_{\text{free},\text{min}}$	2.5% T_{S}	minimum duration of the freewheeling time interval

Table A.17: Assumptions used to design the bidirectional current doubler DC–DC converter.

DC Inductor $L_{\text{DC}2}$

The specified maximum peak-to-peak value of the current ripple, $\Delta I_{L_{\text{DC}2\text{a}+\text{b}},\text{max}}$, represents a lower boundary to the inductance values of $L_{\text{DC}2\text{a}}$ and $L_{\text{DC}2\text{b}}$, whereas $\Delta I_{L_{\text{DC}2\text{a}+\text{b}}}$ is equal to

$$\Delta I_{L_{\text{DC}2\text{a}+\text{b}}} = \left(\frac{V_1}{n} - V_2 \right) \frac{D}{f_{\text{S}} L_{\text{DC}2\text{a}}} - V_2 \frac{D}{f_{\text{S}} L_{\text{DC}2\text{b}}} \leq 40\% \frac{|P_1|}{V_2}. \quad (\text{A.148})$$

Provided that $L_{\text{DC}2\text{a}} = L_{\text{DC}2\text{b}}$ applies, the inductance value of $L_{\text{DC}2\text{a}}$ can be determined using:

$$L_{\text{DC}2\text{a}} = \min \left[\left(\frac{V_1}{n} - 2V_2 \right) \frac{D}{40\% \frac{|P_1|}{V_2} f_{\text{S}}} \right] \left| \begin{array}{l} V_{1,\text{min}} \leq V_1 \leq V_{1,\text{max}}, \\ V_{2,\text{min}} \leq V_2 \leq V_{2,\text{max}}, \\ P_1 = -2.22 \text{ kW} \end{array} \right. = 1.7 \mu\text{H}. \quad (\text{A.149})$$

The peak currents through $L_{\text{DC}2\text{a}}$ and $L_{\text{DC}2\text{b}}$ are obtained from

$$\min(i_{L_{\text{DC}2\text{a}}}) = \min(i_{L_{\text{DC}2\text{b}}}) = \min \left(\frac{P_1}{V_2} - \frac{\Delta I_{L_{\text{DC}2\text{a}}}}{2} \right) = -129 \text{ A} \quad (\text{A.150})$$

in reverse mode of operation [accordingly, $\max(i_{L_{\text{DC}2\text{a}}}) = \max(i_{L_{\text{DC}2\text{b}}}) =$

129 A applies in forward mode]. The respective maximum RMS current is

$$\max(I_{L_{\text{DC}2a}}) = \max(I_{L_{\text{DC}2b}}) = \max \left[\sqrt{\left(\frac{P_1}{2V_2}\right)^2 + \left(\frac{\Delta I_{L_{\text{DC}2a}}}{2\sqrt{3}}\right)^2} \right] = 102 \text{ A.} \quad (\text{A.151})$$

HF Inductance L , Transformer Currents

The calculation of the HF inductance L and of the transformer RMS currents is identical to the calculation presented in Appendix A.5.2. The results are:

$$L = 6.1 \text{ } \mu\text{H,} \quad (\text{A.152})$$

$$\max(I_{L,\text{peak}}) = 25.9 \text{ A,} \quad (\text{A.153})$$

$$\max(I_{\text{AC}1}) = 22.5 \text{ A,} \quad (\text{A.154})$$

$$\max(I_{\text{AC}2}) = n \max(I_{\text{AC}1}) = 135 \text{ A.} \quad (\text{A.155})$$

Transformer Peak Flux Density

The peak flux density in the transformer core is calculated with (A.122).

HV Side Switch Currents and Voltages

On the HV side, the peak switch voltages are equal to the maximum port voltage,

$$V_{\text{DS},\text{T}1,\text{peak,max}} = V_{\text{DS},\text{T}2,\text{peak,max}} = V_{\text{DS},\text{T}3,\text{peak,max}} = V_{\text{DS},\text{T}4,\text{peak,max}} = 450 \text{ V.} \quad (\text{A.156})$$

The maximum switch RMS currents are calculated according to (4.1),

$$I_{\text{D},\text{T}1,\text{max}} = I_{\text{D},\text{T}2,\text{max}} = I_{\text{D},\text{T}3,\text{max}} = I_{\text{D},\text{T}4,\text{max}} = \frac{\max(I_{\text{AC}1})}{\sqrt{2}} = 15.9 \text{ A,} \quad (\text{A.157})$$

and the peak switch currents are [cf. (A.153)]:

$$I_{\text{D},\text{T}1,\text{peak,max}} = I_{\text{D},\text{T}2,\text{peak,max}} = I_{\text{D},\text{T}3,\text{peak,max}} = I_{\text{D},\text{T}4,\text{peak,max}} = \max(I_{L,\text{peak}}) = 25.9 \text{ A.} \quad (\text{A.158})$$

LV Side Switch Currents and Voltages

On the assumption of negligible overvoltage spikes, the peak switch voltages applied to the LV side switches are obtained from:

$$V_{\text{DS},\text{T}5,\text{peak,max}} = V_{\text{DS},\text{T}6,\text{peak,max}} = \frac{450 \text{ V}}{n} = 75 \text{ V.} \quad (\text{A.159})$$

The calculation of the switch RMS currents requires 6 interim current values (cf. Figure A.40),

$$I_{D,T_{LV},1} = i_{D,T_5}(t_3) = -I_{L_{DC2a},0} - I_{L_{DC2a},2} + \frac{V_2}{L_{DC2a}} T_{C,II}, \quad (A.160)$$

$$I_{D,T_{LV},2} = i_{D,T_5}(t_4) = -I_{L_{DC2a},0} - I_{L_{DC2a},2} + \frac{V_2}{L_{DC2a}} \frac{1 - 2D - 2f_S T_{C,I}}{2f_S}, \quad (A.161)$$

$$I_{D,T_{LV},3} = i_{D,T_5}(t_5) = -2I_{L_{DC2a},1} - \frac{V_2}{L_{DC2a}} \frac{1}{2f_S}, \quad (A.162)$$

$$I_{D,T_{LV},4} = i_{D,T_5}(t_6) = -I_{L_{DC2a},2} - I_{L_{DC2a},1} - \frac{V_2}{L_{DC2a}} \frac{1 - 2D}{2f_S}, \quad (A.163)$$

$$I_{D,T_{LV},5} = i_{D,T_5}(t_7) = I_{L_{DC2a},0} - I_{L_{DC2a},1} - \frac{V_2}{L_{DC2a}} \frac{D + f_S T_{C,I}}{f_S}, \quad (A.164)$$

$$I_{D,T_{LV},6} = i_{D,T_5}(t_8) = I_{L_{DC2a},0} - I_{L_{DC2a},1} - \frac{V_2}{L_{DC2a}} T_{C,I}; \quad (A.165)$$

the switch RMS currents are:

$$\begin{aligned} I_{D,T_{LV}} = I_{D,T_5} = I_{D,T_6} = & \\ & \left\{ f_S \left[\frac{T_{C,II}}{3} (I_{D,T_{LV},1}^2 + I_{D,T_{LV},4}^2 + I_{D,T_{LV},4} I_{D,T_{LV},5} + I_{D,T_{LV},5}^2) + \right. \right. \\ & \frac{0.5 - D - f_S (T_{C,I} + T_{C,II})}{3 f_S} (I_{D,T_{LV},1}^2 + I_{D,T_{LV},1} I_{D,T_{LV},2} + I_{D,T_{LV},2}^2 + \\ & I_{D,T_{LV},5}^2 + I_{D,T_{LV},5} I_{D,T_{LV},6} + I_{D,T_{LV},6}^2) + \\ & \left. \frac{T_{C,I}}{3} (I_{D,T_{LV},2}^2 + I_{D,T_{LV},2} I_{D,T_{LV},3} + I_{D,T_{LV},3}^2 + I_{D,T_{LV},3}^2 + I_{D,T_{LV},6}^2) + \right. \\ & \left. \left. \frac{D}{3 f_S} (I_{D,T_{LV},3}^2 + I_{D,T_{LV},3} I_{D,T_{LV},4} + I_{D,T_{LV},4}^2) \right] \right\}^{\frac{1}{2}}. \quad (A.166) \end{aligned}$$

Within the specified input and output voltage ranges and for $P_1 = -2.22$ kW, the maximum switch RMS currents are:

$$I_{D,T_{LV},\max} = \max(I_{D,T_{LV}}) = 159 \text{ A}. \quad (A.167)$$

HV Side and LV Side Capacitor AC Currents

The calculation of the capacitor AC currents is identical to the calculation presented in Appendix A.5.2 [solely, in (A.134), $\Delta I_{L_{DC2}}$ needs to be replaced by $\Delta I_{L_{DC2a+b}}$]. The results are:

$$I_{C_{DC1},\max} = 10.7 \text{ A}, \quad (A.168)$$

$$I_{C_{DC2},\max} = 16 \text{ A}. \quad (A.169)$$

<i>Property</i>	<i>Value</i>	<i>Description</i>
<i>HV Side Switches</i> T_1, T_2, T_3, T_4 :		
$\max(V_{DS,T_{HV,peak}})$	450 V	maximum HV switch voltages
$\max(I_{D,T_{HV,peak}})$	25.9 A	max. HV switch curr. (instantaneous value)
$\max(I_{D,T_{HV}})$	15.9 A	maximum HV switch currents (RMS value)
<i>LV Side Switches</i> T_5, T_6 :		
$\max(V_{DS,T_{LV,peak}})$	75 V	maximum LV switch voltages
$\max(I_{D,T_{LV,peak}})$	251 A	max. LV switch curr. (instantaneous value)
$\max(I_{D,T_{LV}})$	159 A	maximum LV switch currents (RMS value)
<i>Transformer:</i>		
n	6	turns ratio
$\max(I_{AC1})$	22.5 A	HV transformer winding, max. RMS current
$\max(I_{AC2})$	135 A	LV transformer winding, max. RMS current
$\max(B_{tr,core,peak})$	130 mT	for $N_1 = 12$, $N_2 = 2$, and $A_{tr,core} = 308 \text{ mm}^2$ (ELP 58 core, cf. Section A.2.4)
<i>DC Inductor</i> L_{DC2} :		
L_{DC2}	1.7 μH	inductance value
$\max(I_{L_{DC2,peak}})$	129 A	maximum instantaneous inductor current
$\max(I_{L_{DC2}})$	102 A	maximum inductor RMS current
<i>HF Inductor</i> L :		
L	6.1 μH	inductance value
$\max(I_{L_{DC2,peak}})$	25.9 A	maximum instantaneous inductor current
$\max(I_{L_{DC2}})$	22.5 A	maximum inductor RMS current
<i>HV Side DC Capacitor</i> C_{DC1} :		
$\max(I_{C_{DC1}})$	10.7 A	maximum capacitor RMS current
<i>LV Side DC Capacitor</i> C_{DC2} :		
$\max(I_{C_{DC2}})$	16 A	maximum capacitor RMS current

Table A.18: Design summary for the bidirectional current doubler topology.

A.7 Push-Pull Converter Design

A.7.1 Mode of Operation

Figure A.44 depicts the bidirectional and isolated push-pull converter. Again, the actually employed modulation scheme depends on the direction of power transfer (cf. Appendix A.5.1):

- HV \rightarrow LV (*forward mode*, Figure A.45): the HV side full bridge applies the AC voltage v_{AC1} to the series connection of the inductance L and the HF transformer. The diodes on the LV side (operated using synchronous rectification) rectify the secondary side transformer voltage $v_{AC2a} - v_{AC2b}$ and the output filter formed with the DC inductor L_{DC2} and the DC capacitor C_{DC2} filters the rectified transformer voltage.
- LV \rightarrow HV (*reverse mode*, Figure A.46): the LV side switches alternately force one of the secondary side transformer currents to become equal to $i_{L_{DC2}}$ (i.e. either $i_{AC2a} = i_{L_{DC2}}$ or $i_{AC2b} = i_{L_{DC2}}$). The HV side full bridge rectifies the primary side transformer current i_{AC1} and the DC capacitor C_{DC1} provides filtering of the output voltage V_1 .

The employed modulation schemes are identical to the modulation schemes used for the bidirectional full bridge converter (detailed in Appendix A.5.1).

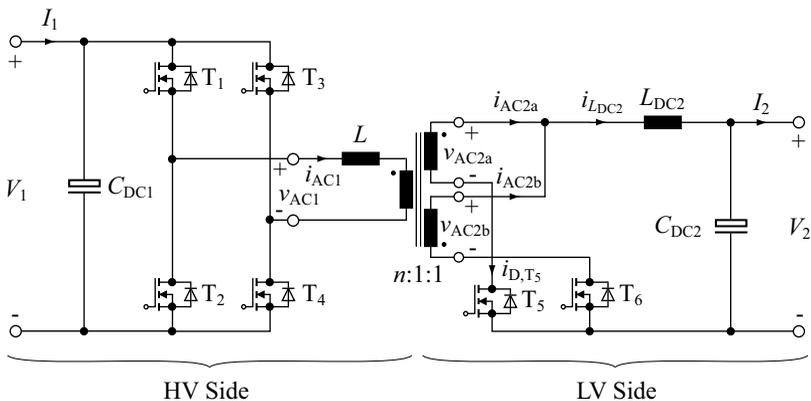


Figure A.44: Bidirectional push-pull converter with LV side DC inductor.

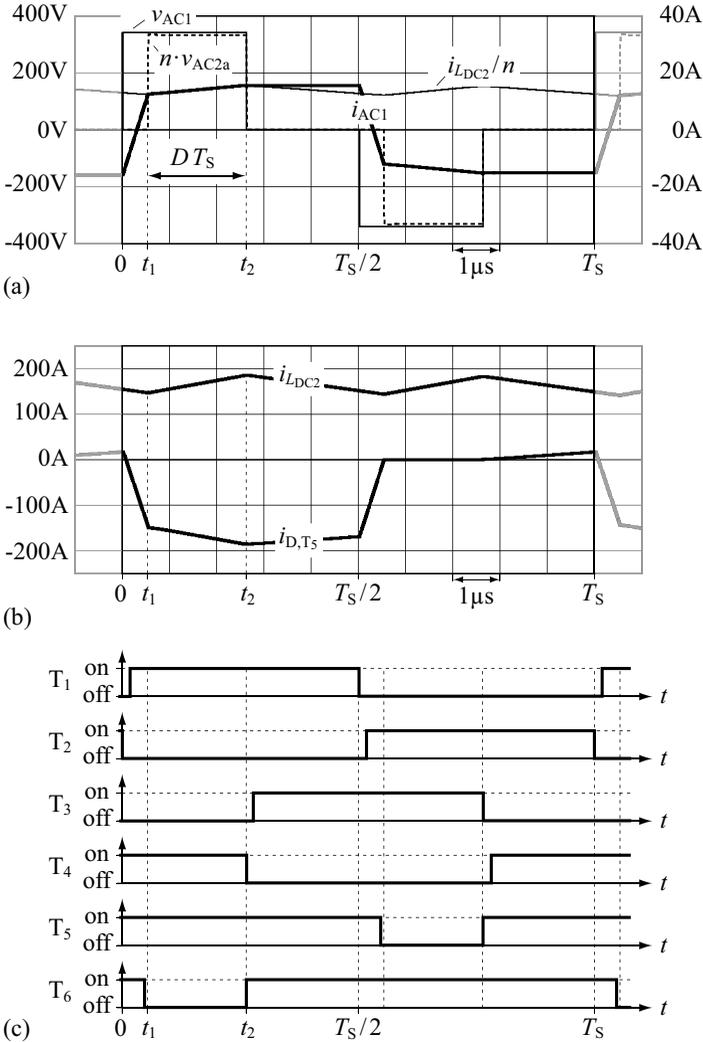


Figure A.45: (a) Simulated voltage and current waveforms of the bidirectional push-pull converter; (b) simulated currents through the DC inductor L_{DC2} and through the LV switch T_5 [the current through T_6 is given with $i_{D,T_6}(t) = i_{D,T_5}(t - T_s/2)$]; (c) employed gate signals on the assumption of zero turn-on time delays and zero turn-off time delays; $V_1 = 340$ V, $V_2 = 12$ V, $P_2 = 2$ kW, $f_s = 100$ kHz.

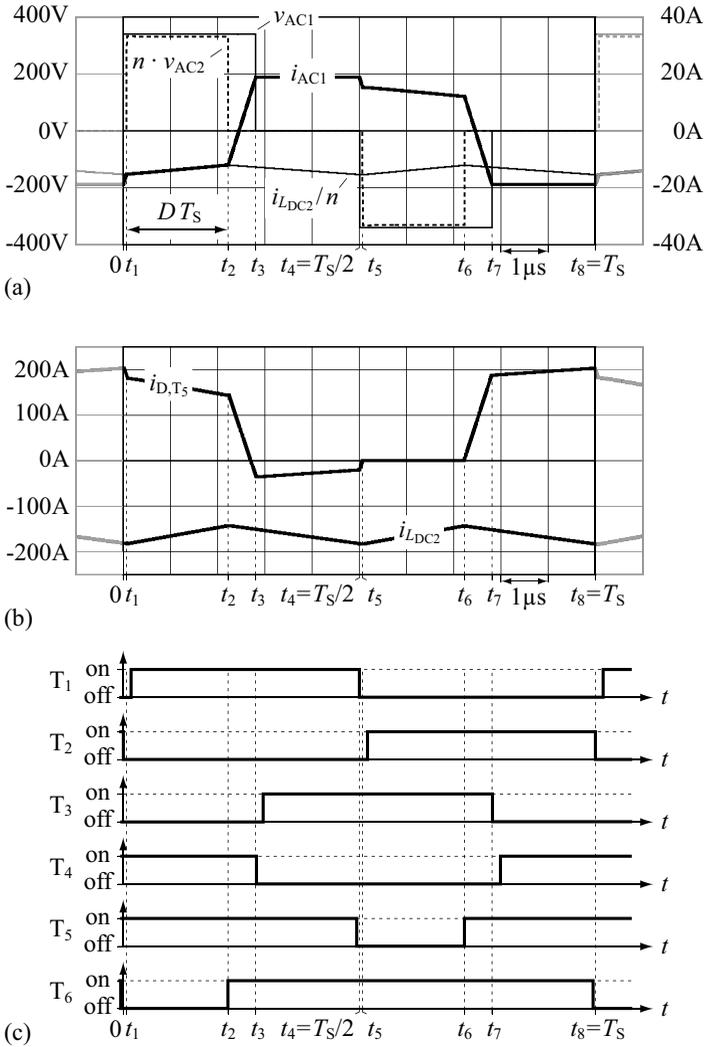


Figure A.46: (a) Simulated voltage and current waveforms of the bidirectional push-pull converter; (b) simulated currents through the DC inductor L_{DC2} and through the LV switch T_5 [the current through T_6 is given with $i_{D,T_6}(t) = i_{D,T_5}(t - T_S/2)$]; (c) employed gate signals on the assumption of zero turn-on time delays and zero turn-off time delays; $V_1 = 340$ V, $V_2 = 12$ V, $P_1 = -2$ kW, $f_s = 100$ kHz.

A.7.2 Converter Design

The design of the push-pull converter is almost identical to the design of the full bridge converter detailed in Appendix A.5.2 except for 2 differences:

1. The transformer of the push-pull converter employs 2 windings on the LV side (however, the turns ratio n is the same as for the full bridge converter).
2. The maximum voltage applied to the switches T_5 and T_6 of the push-pull converter is (approximately) twice the maximum voltage applied to the LV side switches of the full bridge converter.

Table A.19 summarizes the design results obtained for the push-pull converter.

<i>Property</i>	<i>Value</i>	<i>Description</i>
<i>HV Side Switches</i> T_1, T_2, T_3, T_4 :		
$\max(V_{DS,T_{HV,peak}})$	450 V	maximum HV switch voltages
$\max(I_{D,T_{HV,peak}})$	22.6 A	max. HV switch curr. (instantaneous value)
$\max(I_{D,T_{HV}})$	14.2 A	maximum HV switch currents (RMS value)
<i>LV Side Switches</i> T_5, T_6 :		
$\max(V_{DS,T_{LV,peak}})$	75 V	maximum LV switch voltages
$\max(I_{D,T_{LV,peak}})$	236 A	max. LV switch curr. (instantaneous value)
$\max(I_{D,T_{LV}})$	157 A	maximum LV switch currents (RMS value)
<i>Transformer:</i>		
n	12	turns ratio
$\max(I_{AC1})$	20.0 A	HV transformer winding, max. RMS current
$\max(I_{AC2a})$	157 A	LV transformer winding 1, max. RMS curr.
$\max(I_{AC2b})$	157 A	LV transformer winding 2, max. RMS curr.
$\max(B_{tr,core,peak})$	130 mT	for $N_1 = 12, N_2 = 1$, and $A_{tr,core} = 308 \text{ mm}^2$ (ELP 58 core, cf. Section A.2.4)
<i>DC Inductor</i> L_{DC2} :		
L_{DC2}	0.83 μH	inductance value
$\max(I_{L_{DC2,peak}})$	226 A	maximum instantaneous inductor current
$\max(I_{L_{DC2}})$	202 A	maximum inductor RMS current
<i>HF Inductor</i> L :		
L	6.4 μH	inductance value
$\max(I_{L_{DC2,peak}})$	22.6 A	maximum instantaneous inductor current
$\max(I_{L_{DC2}})$	20.0 A	maximum inductor RMS current
<i>HV Side DC Capacitor</i> C_{DC1} :		
$\max(I_{C_{DC1}})$	10.1 A	maximum capacitor RMS current
<i>LV Side DC Capacitor</i> C_{DC2} :		
$\max(I_{C_{DC2}})$	16 A	maximum capacitor RMS current

Table A.19: Design summary for the bidirectional push-pull converter.

A.8 Design of the Bidirectional Buck-or-Boost Converter

A.8.1 Assumptions and Specifications

In order to simplify the design of the bidirectional buck-or-boost converter used in Chapter 7 (Figure A.47), the maximum peak-to-peak value $\Delta I_{L_{DC}}$ of the inductor current $i_{L_{DC}}(t) = -i_{L_{DC}}(t)$ is specified. Typically, $\Delta I_{L_{DC}} \approx 20\% \dots 40\% \bar{I}_{L_{DC}}$ [cf. (7.3)] is selected at rated load to limit the increase of the RMS value of the inductor current [116]. A larger current ripple decreases the inductor volume (provided that the converter operates in the continuous conduction mode), however, the inductor RMS current and – in particular – the current through the DC capacitor C_{DCi} increase. The relative increase of the inductor RMS current $I_{L_{DC,rel}}$ with respect to the relative current ripple $\Delta I_{L_{DC,rel}} = \Delta I_{L_{DC}} / \bar{I}_{L_{DC}}$ is given with:

$$I_{L_{DC,rel}} = \sqrt{1 + \frac{\Delta I_{L_{DC,rel}}^2}{12}}; \tag{A.170}$$

Figure A.48 (a) depicts the relative increase. Obviously, values below 40% cause the RMS inductor current to increase by less than 0.7%. In order to achieve a low inductor core volume, a higher maximum value of the relative peak-to-peak current ripple of 80% is selected (Table A.20). Still, the relative increase of the inductor RMS current is low, $I_{L_{DC,rel}} < 2.7\%$. Furthermore, the RMS current through the DC capacitor C_{DCi} increases linearly with increasing

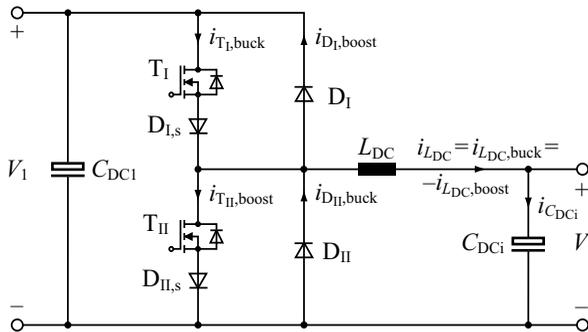


Figure A.47: Bidirectional buck-or-boost converter employed for the two-stage converters discussed in Chapter 7.

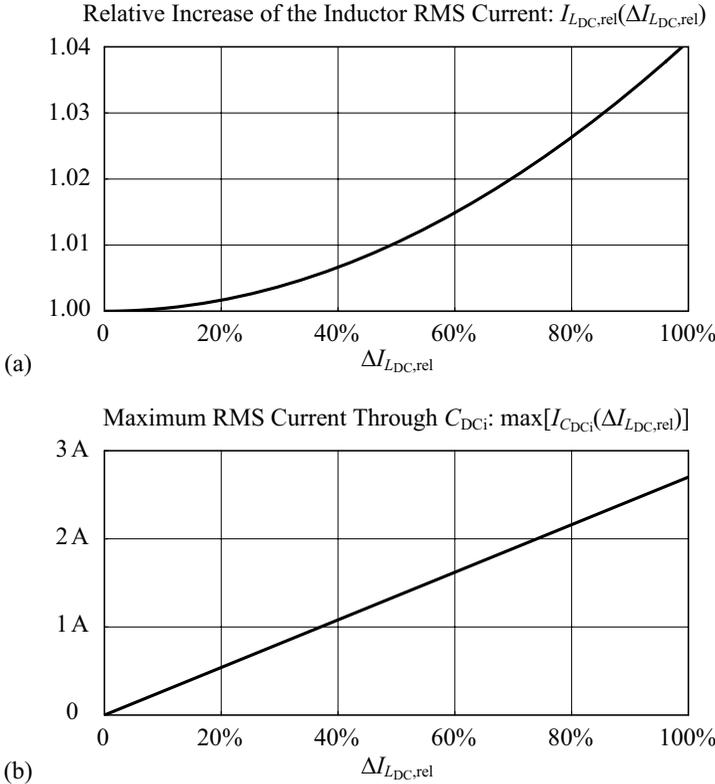


Figure A.48: (a) Relative increase of the RMS current through the DC inductor L_{DC} , $I_{L_{DC},rel} = I_{L_{DC}}/\bar{I}_{L_{DC}}$ due to an increase of the relative current ripple $\Delta I_{L_{DC},rel} = \Delta I_{L_{DC}}/\bar{I}_{L_{DC}}$; (b) calculated maximum RMS current through the DC capacitor C_{DCi} , plotted against $\Delta I_{L_{DC},rel}$.

$I_{L_{DC},rel}$ [Figure A.48 (b)].⁹ With the selected limit, $\Delta I_{L_{DC},rel} \leq 80\%$, the maximum capacitor RMS current results: $I_{C_{DCi}} \approx 2.2$ A.

In order to facilitate the practical realization of the bidirectional buck-or-boost converter, the applicable duty cycles are limited to $0 \leq D_{buck} \leq 95\%$ during buck operation and $5\% \leq D_{boost} \leq 95\%$ during boost operation.

⁹For the calculation of the maximum capacitor RMS current depicted in Figure A.48 (b), the converter inductance L_{DC} is first calculated according to (A.171) and subsequently, $\max(I_{C_{DCi}})$ is determined.

<i>Property</i>	<i>Assumption</i>	<i>Description</i>
η_{est}	95%	estimated converter efficiency
$D_{buck,min}$	0	min. duty cycle, buck operation
$D_{buck,max}$	95%	max. duty cycle, buck operation
$D_{boost,min}$	5%	min. duty cycle, boost operation
$D_{boost,max}$	95%	max. duty cycle, boost operation
$\max(\Delta I_{L_{DC}})$	$\leq 80\% \bar{I}_{L_{DC}} $	maximum peak-to-peak value of the current ripple on $i_{L_{DC}}(t)$
f_s	100 kHz	switching frequency

Table A.20: Assumptions and specifications used to design the bidirectional buck-or-boost converter (in addition to the HV side voltage range specified in Table 1.4).

Furthermore, a switching frequency, f_s , of 100 kHz is specified in order to achieve both, low converter volume and low converter losses.¹⁰ The bidirectional buck-or-boost converter is designed for an assumed converter efficiency of 95%. Table A.20 summarizes the specifications and assumptions needed (in addition to the HV side voltage range specified in Table 1.4) to carry out the converter design.

A.8.2 Calculation of L_{DC}

With the specifications given in Table 1.4 and in Table A.20 and with the analytical results presented in Section 7.2, the DC inductors can be calculated. For the configurations 1 and 2 (i.e. $V_1 > V_i$, Table 7.1) the inductance value $L_{DC} = 150 \mu\text{H}$,

$$L_{DC} \geq \max \left[\frac{V_i^2(V_1 - V_i)}{f_s V_1 I_{L_{DC},rel} P / \eta_{est}} \right] \left| \begin{array}{l} V_{1,min} \leq V_1 \leq V_{1,max} \\ V_{i,min} \leq V_i \leq V_{i,max} \\ P = 2.1 \text{ kW} \end{array} \right. \approx 150 \mu\text{H}, \tag{A.171}$$

¹⁰The employed silicon-carbide diodes facilitate low switching losses; cf. Figure 7.11 and [125].

results and for the configurations 3 and 4 ($V_1 < V_i$) L_{DC} is:

$$L_{DC} \geq \max \left[\frac{V_1^2 (V_i - V_1)}{f_S V_i I_{L_{DC,rel}} P / \eta_{est}} \right] \left| \begin{array}{l} V_{1,min} \leq V_1 \leq V_{1,max} \\ V_{i,min} \leq V_i \leq V_{i,max} \\ P = 2.1 \text{ kW} \end{array} \right. \approx 200 \mu\text{H}. \quad (\text{A.172})$$

With the expressions given in Section 7.2, the peak inductor currents and the inductor RMS currents can be calculated:

$$L = 150 \mu\text{H} : \max(I_{L_{DC,peak}}) = \max \left(\bar{I}_{L_{DC}} + \frac{\Delta I_{L_{DC}}}{2} \right) = 17.0 \text{ A}, \quad (\text{A.173})$$

$$L = 200 \mu\text{H} : \max(I_{L_{DC,peak}}) = \max \left(\bar{I}_{L_{DC}} + \frac{\Delta I_{L_{DC}}}{2} \right) = 11.7 \text{ A}, \quad (\text{A.174})$$

$$L = 150 \mu\text{H} : \max(I_{L_{DC}}) = 13.7 \text{ A}, \quad (\text{A.175})$$

$$L = 200 \mu\text{H} : \max(I_{L_{DC}}) = 8.9 \text{ A}. \quad (\text{A.176})$$

A.8.3 Design Summary

Semiconductor Switches and Diodes

According to the voltage and current ratings calculated for the semiconductor switches and diodes (Section 7.2 and Table A.21), appropriate MOSFETs and diodes are selected:

- T_I, T_{II} : CoolMOS SPW47N60C3 (max. drain-to-source voltage: 600 V, max. drain current at $T_j = 25^\circ\text{C}$: 47 A; obtained from [153])
- D_I, D_{II} : Silicon-carbide Diodes SDT12S60 (max. blocking voltage: 600 V, max. diode current at $T_j = 25^\circ\text{C}$: 23 A; obtained from [153])
- $D_{I,s}, D_{II,s}$: Schottky Diodes DSS25-0025B (max. blocking voltage: 25 V, max. diode current at $T_j = 25^\circ\text{C}$: 35 A; obtained from [158])

DC Inductor 1: $L_{DC} = 150 \mu\text{H}$, $\max(I_{L_{DC,peak}}) = 17.0 \text{ A}$.

The design of the DC inductors is very close to the inductor design presented in Appendix A.9, however, multilayer windings are used to effectively utilize the available winding window. For the inductor design, a peak flux density of $B_{L_{DC,peak,max}} = 310 \text{ mT}$ and a maximum RMS current density of $J_{L_{DC,max}} = 7 \text{ A/mm}^2$ are assumed.¹¹ Furthermore, a litz wire with a single strand copper

¹¹With respect to the employed ferrite material, a rather large value of the flux density can be used; compared to a HF transformer, the ferrite core of the DC inductor is not subject to a full reversal of the flux at the rate of the switching frequency and thus, low core losses result (cf. Section 7.2.5).

Property	Value	Description
<i>Semiconductor Switches T_I, T_{II} (CoolMOS SPW47N60C3):</i>		
$\max(V_{DS,T_{I,II,peak}})$	475 V	maximum switch voltages
$\max(I_{T_I,peak})$	17.0 A	max. instantaneous switch current, T_I
$\max(I_{T_{II,peak}})$	17.0 A	max. instantaneous switch current, T_{II}
$\max(I_{T_I})$	11.0 A	maximum switch RMS current, T_I
$\max(I_{T_{II}})$	11.1 A	maximum switch RMS current, T_{II}
<i>Silicon-carbide Diodes D_I, D_{II} (SDT12S60):</i>		
$\max(V_{CA,D_{I,II,peak}})$	475 V	maximum blocking voltages
$\max(I_{D_I,peak})$	17.0 A	max. instantaneous diode current, D_I
$\max(I_{D_{II,peak}})$	17.0 A	max. instantaneous diode current, D_{II}
$\max(\bar{I}_{D_I})$	8.8 A	maximum average diode current, D_I
$\max(\bar{I}_{D_{II}})$	8.9 A	maximum average diode current, D_{II}
$\max(I_{D_I})$	11.0 A	maximum diode RMS current, D_I
$\max(I_{D_{II}})$	11.1 A	maximum diode RMS current, D_{II}
<i>Series Diodes $D_{I,s}, D_{II,s}$ (DSS25-0025B):</i>		
$\max(V_{CA,D_{I,II,s,peak}})$	< 10 V	maximum blocking voltages
$\max(I_{D_{I,s,peak}})$	17.0 A	max. instantaneous diode current, $D_{I,s}$
$\max(I_{D_{II,s,peak}})$	17.0 A	max. instantaneous diode current, $D_{II,s}$
$\max(\bar{I}_{D_{I,s}})$	8.8 A	maximum average diode current, $D_{I,s}$
$\max(\bar{I}_{D_{II,s}})$	8.9 A	maximum average diode current, $D_{II,s}$
$\max(I_{D_{I,s}})$	11.0 A	maximum diode RMS current, $D_{I,s}$
$\max(I_{D_{II,s}})$	11.1 A	maximum diode RMS current, $D_{II,s}$
<i>DC Inductor 1, $L_{DC} = 150 \mu\text{H}$ (config. 1 and 2, i.e. $V_1 > V_i$; Table 7.1):</i>		
L_{DC}	150 μH	inductance value
$\max(I_{L_{DC,peak}})$	17.0 A	maximum instantaneous inductor current
$\max(I_{L_{DC}})$	13.7 A	maximum inductor RMS current
<i>DC Inductor 2, $L_{DC} = 200 \mu\text{H}$ (config. 3 and 4, i.e. $V_1 < V_i$; Table 7.1):</i>		
L_{DC}	200 μH	inductance value
$\max(I_{L_{DC,peak}})$	11.7 A	maximum instantaneous inductor current
$\max(I_{L_{DC}})$	8.9 A	maximum inductor RMS current
<i>DC Capacitor C_{DC1}:</i>		
C_{DC1}	3 μF	type of capacitor: 2 film capacitors
$\max(I_{C_{DC1}})$	6.9 A	maximum capacitor RMS current
<i>DC Capacitor C_{DCi}:</i>		
C_{DCi}	47 μF	type of capacitor: 4 electrolytic capacitors
$\max(I_{C_{DC2}})$	2.2 A	maximum capacitor RMS current

Table A.21: Design summary for the bidirectional buck-or-boost converter.

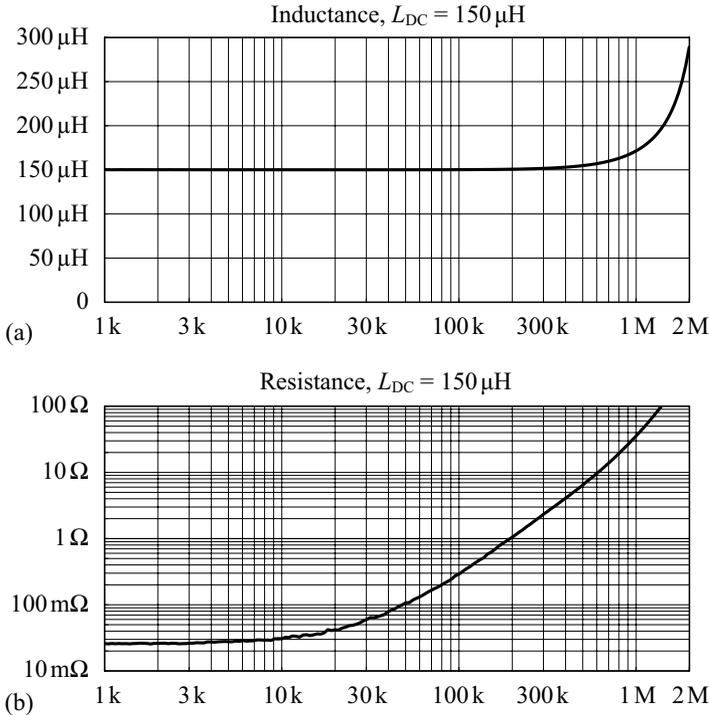


Figure A.49: Inductance and series resistance of the converter inductor $L_{DC} = 150 \mu\text{H}$, measured with the Agilent 4294A Precision Impedance Analyzer: (a) series inductance, (b) series resistance; at $f = 100 \text{ kHz}$, an AC resistance of approximately $290 \text{ m}\Omega$ is measured (according to [152] the relative error of the resistance measurement is $\pm 24\%$ at $f = 100 \text{ kHz}$). At $f = f_{L_{DC},\text{res}} = 2.9 \text{ MHz}$ a parallel resonance occurs; the effective capacitance in parallel to L_{DC} is 20 pF .

diameter of 0.2 mm is selected and a realization with one of the planar cores ELP 32, ELP 38, ELP 43, ELP 58, and ELP 64 is considered.

The design algorithm suggests the planar ferrite core ELP 64 (material N87) to be used with respect to minimum inductor volume. The following list summarizes the inductor design results.

- Total air gap length: 1.51 mm

- Number of turns: 16
- Employed litz wire: 65×0.2 mm.

Figure A.49 depicts the measured inductance and the measured resistance of this DC inductor, plotted against the measurement frequency.

DC Inductor 2: $L_{\text{DC}} = 200 \mu\text{H}$, $\max(I_{L_{\text{DC}},\text{peak}}) = 11.7$ A.

The second inductor is again designed according to Appendix A.9 (except for the employed multilayer winding) and employs a planar ferrite core. The selected peak flux density and the maximum RMS current density are: $B_{L_{\text{DC}},\text{peak},\text{max}} = 310$ mT, $J_{L_{\text{DC}},\text{max}} = 7$ A/mm².

Minimum inductor volume is achieved with the ELP 58 ferrite core; since the ELP 58 core was not available, an E 58 core was used, instead (the dimensions of the ELP 58 and the E 58 cores are nearly identical, cf. [155, 156]; employed ferrite material: 3F3).

- Total air gap length: 1.62 mm
- Number of turns: 24
- Employed litz wire: 50×0.2 mm.

Figure A.50 depicts the measured inductance and the measured resistance of this DC inductor, plotted against the measurement frequency.

DC Capacitors

Due to the large value of the maximum RMS current through $C_{\text{DC}1}$ [$\max(I_{C_{\text{DC}1}}) = 6.9$ A], 2 film capacitors, each with a capacitance of $1.5 \mu\text{F}$ and a rated DC voltage of 630 V, are connected in parallel to form $C_{\text{DC}1}$. A considerably lower RMS current rating is required for $C_{\text{DC}i}$ [$\max(I_{C_{\text{DC}i}}) = 2.2$ A]; there, 4 electrolytic capacitors, each with a capacitance of $47 \mu\text{F}$ and a rated voltage of 250 V, are forming the DC capacitor with a total capacitance of $47 \mu\text{F}$ and a rated voltage of 500 V. Figure A.51 depicts the impedance of $C_{\text{DC}i}$, measured with the Agilent 4294A Precision Impedance Analyzer.

A.9 HF Inductor Design

The additional HF inductor employed for the DAB (L_{HV} in Figure 3.30) consists of a ferrite core, 3 air gaps, and a litz wire winding in order to achieve a compact inductor design and a low AC resistance $R_{L_{\text{HV}}}$ [Figure A.52 (a)]. The

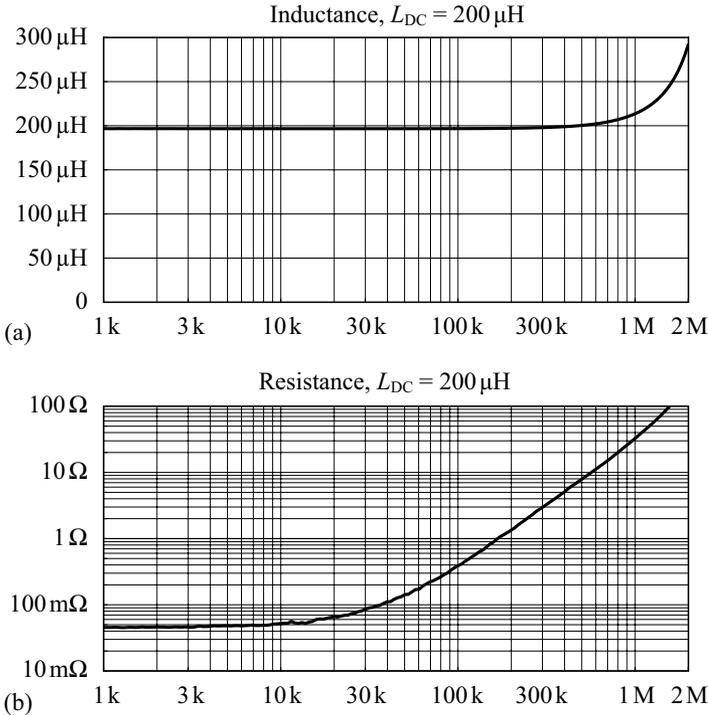


Figure A.50: Inductance and series resistance of the converter inductor $L_{DC} = 200 \mu\text{H}$, measured with the Agilent 4294A Precision Impedance Analyzer: (a) series inductance, (b) series resistance; at $f = 100 \text{ kHz}$, an AC resistance of approximately $390 \text{ m}\Omega$ is measured (according to [152] the relative error of the resistance measurement is $\pm 24\%$ at $f = 100 \text{ kHz}$). At $f = f_{L_{DC}, \text{res}} = 3.5 \text{ MHz}$ a parallel resonance occurs; the effective capacitance in parallel to L_{DC} is 10.3 pF .

proposed design procedure (Appendix A.9.1), required for the design of the DAB (Appendix A.2) is thus confined to inductors with a litz wire winding and a magnetic core. Apart from that, the design procedure is flexible regarding the geometric properties of the employed core. For the DAB hardware prototype, however, there is space for 2 inductors, each made of 3 stacked planar ELP 32 cores (Table A.22). Therefore, the design of L_{HV} is carried

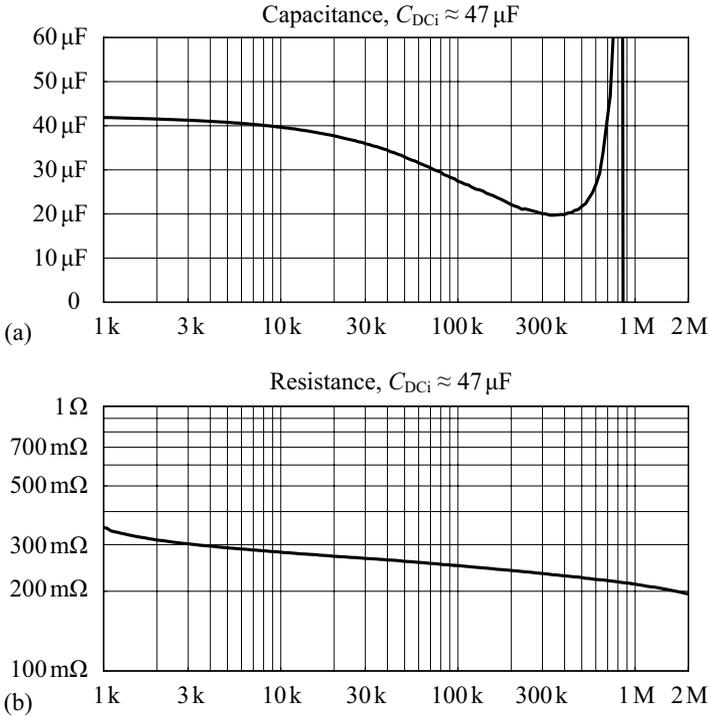


Figure A.51: Capacitance and series resistance of the electrolytic DC capacitor $L_{DCi} \approx 47 \mu\text{F}$, measured with the Agilent 4294A Precision Impedance Analyzer: (a) series capacitance, (b) series resistance; at $f = 100 \text{ kHz}$, an AC resistance of approximately $250 \text{ m}\Omega$ is measured (according to [152] the relative error of the resistance measurement is $\pm 1.1\%$ at $f = 100 \text{ kHz}$). For $f > 10 \text{ kHz}$ the capacitance value drops considerably; at $f_{C_{DCi},res} = 850 \text{ kHz}$ the series resonance frequency, which is due to the parasitic equivalent series inductance, occurs.

out with these ELP 32 cores (ferrite material: 3F3).¹²

¹²Since the ELP 32 core was not available, an E 32 core was used, instead (the dimensions of the ELP 32 and the E 32 cores are nearly identical, cf. [155, 156]).

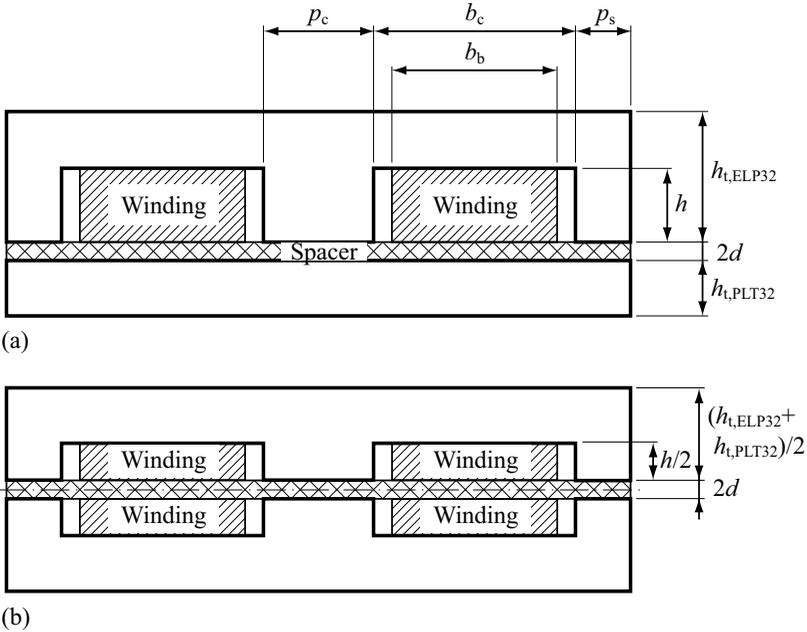


Figure A.52: (a) Cross-sectional drawing of the employed planar HF inductor, composed of an E-core / I-core combination; (b) modified position of the inductor air gap considered in Appendix A.9.3 to calculate the fringing coefficients; dimensioning according to Table A.22.

A.9.1 Design Procedure

The proposed design procedure, outlined in Figure A.53, starts with a single turn, $N_{LHV} = 1$, and a single core, $N_{cores} = 1$, and increases the number of stacked cores in order to keep the peak flux density, calculated with (4.15), below the specified maximum value: $B_{LHV,peak} < B_{LHV,peak,max}$. Thereafter, the optimal winding arrangement with respect to minimum AC resistance (Appendix A.9.2) is calculated in order to determine the resulting maximum current density, J_{RMS} , and subsequently the number of turns is increased until the maximum current density exceeds the specified maximum value: $J_{RMS} > J_{RMS,max}$. The proposed design procedure finally returns the inductor design with the highest number of turns, N_{LHV} , and the lowest number of cores, N_{cores} , which fulfills the conditions $B_{LHV,peak} < B_{LHV,peak,max}$ and $J_{RMS} \leq J_{RMS,max}$. It further returns the optimal winding arrangement with

<i>Property</i>	<i>Value</i>	<i>Description</i>
ELP 32		
b_t	31.8 mm	core width
b_c	9.5 mm	breadth of the window area
b_b	7.5 mm	breadth of the window area used for the winding (1 mm space on either side)
h	3.2 mm	height of the window area
$h_{t,ELP32}$	6.4 mm	total core height
q_c	20.3 mm	core depth
p_c	6.4 mm	width of the inner core leg
p_s	3.2 mm	width of each outer core leg
PLT 32		
b_t	31.8 mm	core width
$h_{t,PLT32}$	3.2 mm	core height
q_c	20.3 mm	core depth
Combination ELP 32 / PLT 32		
l_m	35.9 mm	average length of the magnetic path
A_c	130 mm ²	core cross section

Table A.22: Geometric properties of the planar ELP 32 core and the PLT 32 plate (from [155]).

respect to minimum AC resistance: for the given copper diameter of a single strand, d_c , the optimal number of strands, $n_{strands}$, and the optimal number of parallel wires in horizontal direction, $n_{parallel,h}$, and vertical direction, $n_{parallel,v}$, (cf. Figure A.54) are given. In a final step, the required inductor air gap (Appendix A.9.3) and the expected AC resistance (Appendix A.9.4) are calculated; the total inductor core cross-sectional area, $A_{L_{HV},core}$, is equal to:

$$A_{L_{HV},core} = N_{cores} A_c. \tag{A.177}$$

A.9.2 Winding Configuration, Optimal Litz Wire Calculation

Based on the given number of turns $N_{L_{HV}}$ and the geometric properties of the winding area, this subroutine identifies the best possible choice of litz wires, i.e. the number of litz wire strands and the number of parallel wires [either in

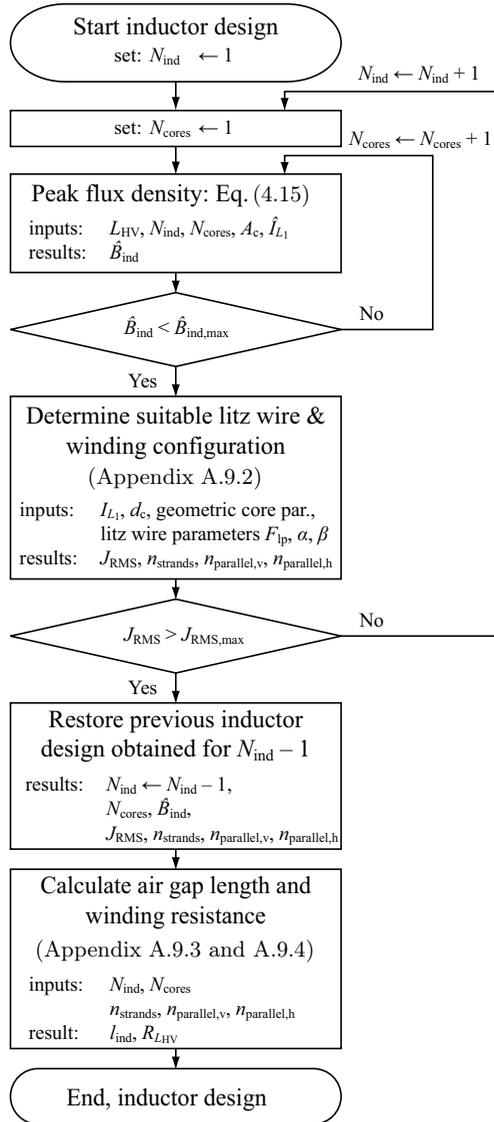


Figure A.53: Inductor design flowchart: the proposed procedure uses the constraints $B_{L_{HV},peak} < B_{L_{HV},peak,max}$ and $J_{RMS} \leq J_{RMS,max}$ to search for the optimal number of turns $N_{L_{HV}}$ and the optimal number of stacked cores N_{cores} , in order to achieve a most effective core utilization.

horizontal direction, Figure A.54 (a), or vertical direction, Figure A.54 (b)]¹³ in order to obtain the constrained minimum for J_{RMS} .

The procedure therefore requires the outer diameter of the litz wire (including the covering with thread), d_{tl} , to be known as a function of the single strand copper diameter, d_c , and the number of strands, n_{strands} . A suitable approximation is discussed in [139]:

$$d_{\text{tl}} = \alpha_{\text{litz}} d_c^{\beta_{\text{litz}}} d_{\text{ref}}^{1-\beta_{\text{litz}}} \left(\frac{F_{1\text{p}}}{n_{\text{strands}}} \right)^{-\frac{1}{2}}, \quad (\text{A.178})$$

$$\alpha_{\text{litz}} = 1.16, \quad (\text{A.179})$$

$$\beta_{\text{litz}} = 0.915, \quad (\text{A.180})$$

$$F_{1\text{p}} = 0.6, \quad (\text{A.181})$$

$$d_{\text{ref}} = 0.079 \text{ mm}. \quad (\text{A.182})$$

The coefficients α_{litz} and β_{litz} are obtained from manufacturers data [159] using least mean square approximation; the selected litz packing factor $F_{1\text{p}}$ and the reference diameter d_{ref} are adopted from [139].

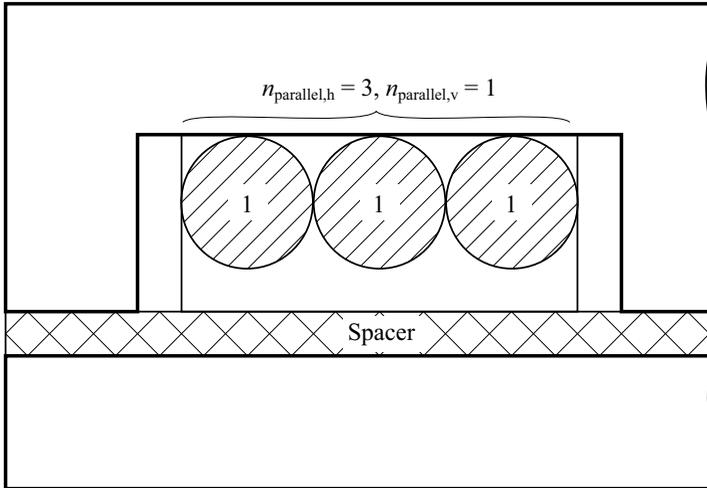
A.9.3 Inductor Air Gap Length

Compared to the core dimensions (Table A.22), the total air gap length, l_g , of the employed inductors is relatively large ($l_g > 1 \text{ mm}$) and thus, the calculation based on the well-known equation $L_{\text{HV}} = N_{L_{\text{HV}}}^2 \mu_0 A_{L_{\text{HV,core}}} / l_g$ predicts a considerably wrong air gap length.

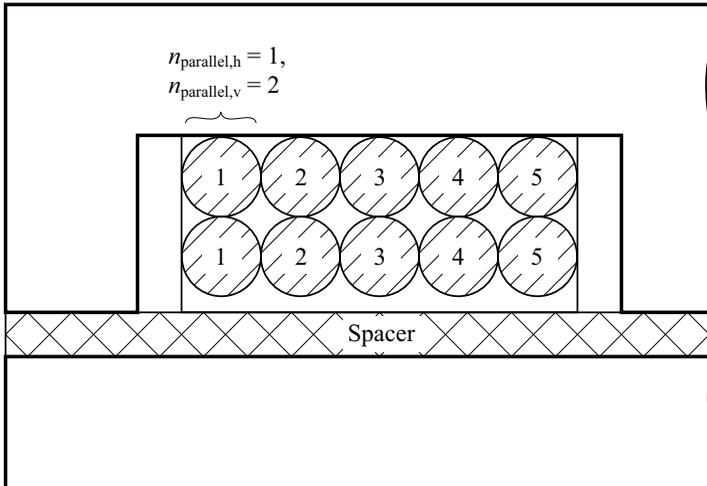
A more advanced approach employs the reluctance model depicted in Figure A.55 and the fringing coefficients F_1 , F_2 , and F_3 given in [145] in order to determine the air gap reluctances $\mathcal{R}_{\text{g,mid}}$ and $\mathcal{R}_{\text{g,side}}$. For the fringing coefficients given in [145], however, 2 E-cores are considered instead of the E-core / I-core combination depicted in Figure A.52 (a). Still, good results are obtained for the inductance value if the inductor air gap is considered in the middle of the inductor, according to Figure A.52 (b).

With the arrangement depicted in Figure A.52 (b), the fringing coefficients F_1 , F_2 , and F_3 become [145]:

¹³The employed method only considers $(n_{\text{parallel,h}} > 1 \wedge n_{\text{parallel,v}} = 1) \vee (n_{\text{parallel,h}} = 1 \wedge n_{\text{parallel,v}} > 1)$ to avoid a large number of parallel wires.



(a)



(b)

Figure A.54: Considered winding configurations for round litz wire (the numbers inside the wire denote the turn number the wire belongs to); (a) $N_{L_{\text{HV}}} = 1$: in order to utilize the winding area the best possible way, 3 wires are placed in parallel ($n_{\text{parallel,h}} = 3, n_{\text{parallel,v}} = 1$); (b) $N_{L_{\text{HV}}} = 5$: best possible utilization of the winding area is achieved with 2 parallel litz wires ($n_{\text{parallel,h}} = 1, n_{\text{parallel,v}} = 2$).

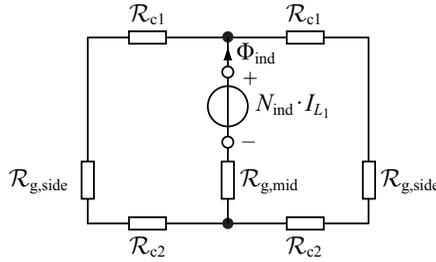


Figure A.55: Reluctance model of the HF inductor: \mathcal{R}_{c1} and \mathcal{R}_{c2} denote the reluctances of the core, $\mathcal{R}_{g,mid}$ is the reluctance of the middle air gap, and $\mathcal{R}_{g,side}$ denote the reluctances of the outer air gaps.

$$F_1 = \frac{2}{\pi} \ln \left(\frac{\frac{1}{b_c} + \frac{1}{d}}{\frac{1}{b_c} + \frac{1}{h/2}} \right) + \frac{h/2 - 0.26d - 0.5b_c}{3b_c(h/2)^2} (h/2 - d)^2 + \frac{b_c}{3h/2}, \quad (\text{A.183})$$

$$F_2 = \frac{2}{\pi} \ln \left[\left(\frac{0.44[(h/2)^2 + b_c^2] - 0.218dh/2 + 0.67b_cd}{d^2} + \right. \right. \quad (\text{A.184})$$

$$\left. \frac{0.33b_ch/2 + 0.7825d^2}{d^2} \right)^{\frac{1}{2}}, \quad (\text{A.185})$$

$$F_3 = \frac{1}{\pi} \operatorname{arccosh} \left\{ 3.395 \left[\frac{(h_{t,ELP32} + h_{t,PLT32})/2}{d} \right]^2 + \right. \quad (\text{A.186})$$

$$\left. 0.15 \frac{(h_{t,ELP32} + h_{t,PLT32})/2}{d} + 1.1155 \right\}$$

(using the parameters listed in Table A.22 and $d = l_g/4$). With these fringing coefficients, an increased effective air gap area is considered for the calculation of $\mathcal{R}_{g,mid}$ and $\mathcal{R}_{g,side}$:

$$\mathcal{R}_{g,mid} = \frac{1}{\mu_0} \frac{2d}{AL_{HV,core} + 2 \cdot F_1 \cdot dq_c N_{cores} + 2 \cdot F_2 \cdot dp_c}, \quad (\text{A.187})$$

$$\mathcal{R}_{g,side} = \frac{1}{\mu_0} \frac{2d}{AL_{HV,core}/2 + (F_1 + F_3)dq_c N_{cores} + 2 \cdot F_3 \cdot dp_s}. \quad (\text{A.188})$$

The reluctances of the left core leg and of the right core leg are equal to:

$$\mathcal{R}_{c1} + \mathcal{R}_{c2} = \frac{1}{\mu_0 \mu_r} \frac{l_m}{AL_{HV,core}/2}. \quad (\text{A.189})$$

The total reluctance, \mathcal{R}_{LHV} , becomes:

$$\mathcal{R}_{LHV} = \mathcal{R}_{g,mid} + \frac{1}{2} (\mathcal{R}_{g,side} + \mathcal{R}_{c1} + \mathcal{R}_{c2}) \quad (\text{A.190})$$

and the result for the inductance is:

$$L_{\text{HV}}(d = l_{\text{g}}/4) = \frac{N_{\text{LHV}}^2}{\mathcal{R}_{L_{\text{HV}}}}. \quad (\text{A.191})$$

Finally, a numerical solver is used to solve for the air gap length l_{g} , required to obtain a given inductance L_{HV} .

A.9.4 Inductor AC Resistance

The DC resistance of a litz wire with n_{strands} strands, single strand copper diameter d_{c} , and length l_{litz} is equal to:

$$R_{\text{DC,litz}} = \frac{4 l_{\text{litz}}}{\sigma_{\text{Cu}} n_{\text{strands}} \pi d_{\text{c}}^2}; \quad (\text{A.192})$$

σ_{Cu} denotes the conductivity of copper [146, 147],

$$\sigma_{\text{Cu}} \approx \frac{56.2 \cdot 10^6 (\Omega\text{m})^{-1}}{1 + 3.9 \cdot 10^{-3} (\text{°C})^{-1} \cdot \Delta T - 0.6 \cdot 10^{-6} (\text{°C})^{-2} \cdot \Delta T^2}, \quad (\text{A.193})$$

$$\Delta T = T_{\text{Cu}} - 20\text{°C}. \quad (\text{A.194})$$

The increase of the wire resistance due to the skin effect at the excitation frequency f is determined with [38, 148]:¹⁴

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma_{\text{Cu}} f}}, \quad (\text{A.195})$$

$$\xi = \frac{d_{\text{c}}}{\sqrt{2} \cdot \delta}, \quad (\text{A.196})$$

$$F_{\text{R}} = \frac{\sqrt{2} \cdot \xi}{4} \left[\frac{\text{Ber}_0(\xi) \text{Bei}_1(\xi) - \text{Ber}_0(\xi) \text{Ber}_1(\xi)}{\text{Ber}_1(\xi)^2 + \text{Bei}_1(\xi)^2} - \frac{\text{Bei}_0(\xi) \text{Ber}_1(\xi) + \text{Bei}_0(\xi) \text{Bei}_1(\xi)}{\text{Ber}_1(\xi)^2 + \text{Bei}_1(\xi)^2} \right], \quad (\text{A.197})$$

$$R_{\text{AC,litz,skin}} = F_{\text{R}} \cdot R_{\text{DC,litz}} \quad (\text{A.198})$$

and the increase due to the proximity effect by reason of the currents in the surrounding conductors and an external magnetic field \vec{H}_{ext} (RMS value)

¹⁴ $\text{Ber}_n(\xi)$ and $\text{Bei}_n(\xi)$ are the n^{th} order Kelvin functions obtained from the n^{th} order Bessel function $J_n(\zeta)$: $\text{Ber}_n(\xi) = \text{Re}[J_n(\xi e^{i \cdot 3\pi/4})]$ and $\text{Bei}_n(\xi) = \text{Im}[J_n(\xi e^{i \cdot 3\pi/4})]$; δ denotes the skin depth.

is [38, 148]:

$$G_R = -\frac{\sqrt{2} \cdot \xi \pi^2 d_c^2}{2} \left[\frac{\text{Ber}_2(\xi)\text{Ber}_1(\xi) + \text{Ber}_2(\xi)\text{Bei}_1(\xi)}{\text{Ber}_0(\xi)^2 + \text{Bei}_0(\xi)^2} + \frac{\text{Bei}_2(\xi)\text{Bei}_1(\xi) - \text{Bei}_2(\xi)\text{Ber}_1(\xi)}{\text{Ber}_0(\xi)^2 + \text{Bei}_0(\xi)^2} \right], \quad (\text{A.199})$$

$$P_{\text{AC,litz,prox}} = \frac{4}{\pi d_{t1}^2} G_R n_{\text{strands}}^2 R_{\text{DC}} \int_0^{d_{t1}/2} \int_0^{2\pi} |\vec{H}(r, \varphi)|^2 r d\varphi dr, \quad (\text{A.200})$$

$$\vec{H}(r, \varphi) = \frac{2Ir}{\pi d_{t1}^2} (-\sin\varphi \vec{e}_x + \cos\varphi \vec{e}_y) + \vec{H}_{\text{ext}}(r, \varphi), \quad (\text{A.201})$$

$$R_{\text{AC,litz,prox}} = \frac{P_{\text{AC,litz,prox}}}{I_{L_1}^2}; \quad (\text{A.202})$$

[each strand is assumed to carry current with the same RMS value I/n_{strands} ; moreover, in (A.201), the conductor current I is oriented along the positive z-axis].

The challenge in the calculation of the AC resistance is to correctly determine the external magnetic field $\vec{H}_{\text{ext}}(r, \varphi)$ (in particular close to the air gap, where high field densities considerably deteriorate the HF properties of the inductor). Different possibilities to approximate $H_{\text{ext}}(r, \varphi)$ include the Schwarz-Christoffel transformation [38], field approximations [149], or FEM simulation. The Schwarz-Christoffel transformation results in a rather complex mathematical problem and the field approximation given in [149] fails due to the large air gaps of the employed inductors. Thus, FEM simulation is used to determine $\vec{H}(r, \varphi)$ for a sample inductor with $L_{\text{HV}} = 15 \mu\text{H}$, a peak current of 30 A and an RMS current of 15 A (the specifications used for the sample inductor, Table A.23, are close to the specifications of the inductors required for the DAB, cf. Table A.1). The sample inductor incorporates a space of 1 mm (approximately equal to $l_g/2$) between the winding and the sides of the inductor core [Figure A.52: $(b_c - b_b)/2 = 1 \text{ mm}$] in order to avoid excessive magnetic fields inside the winding; the winding employs 2 parallel litz wires in order to effectively utilize the remaining winding area.

Figure A.56 depicts the simulated magnetic field strength (RMS values) by reason of an RMS current of 15 A: close to the air gap, the magnetic field reaches values of up to 35 kA/m; moreover, the lower row of conductors (1a ... 5a) is exposed to considerably higher magnetic fields than the upper row (1b ... 5b). Numerical integration confirms the higher values

of $\int_0^{d_{t1}/2} \int_0^{2\pi} |\vec{H}(r, \varphi)|^2 r d\varphi dr$ for the lower conductor row (Table A.24). Consequently, different AC resistances result for the 2 parallel conductors, which causes a considerable increase of the inductor HF losses (between $f = 5 \text{ kHz}$

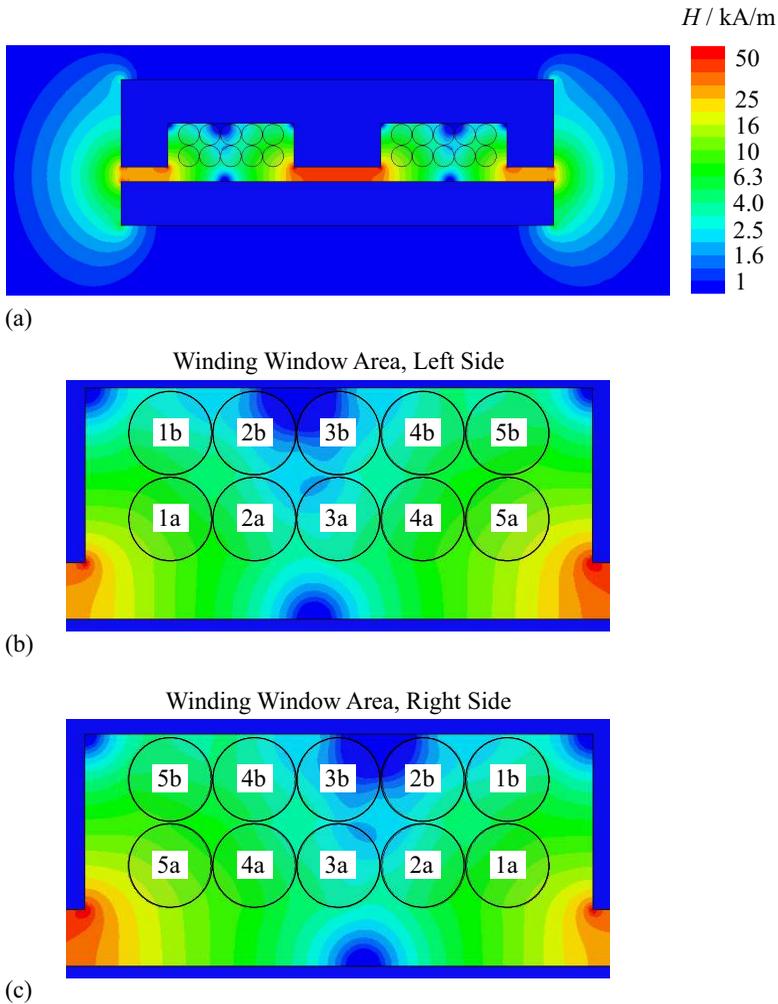


Figure A.56: Cross-sectional plot of the magnetic fields (RMS values) in the sample inductor, $L = 15 \mu\text{H}$, Table A.23, by reason of an RMS current of 15 A (FEM simulation, $f = 100 \text{ kHz}$); the winding is optimized according to Appendix A.9.2: $n_{\text{parallel,h}} = 1$, $n_{\text{parallel,v}} = 2$ [cf. Figure A.54 (b)]; the circles indicate the litz wires]; (a) full inductor cross-sectional view: close to the air gap, the magnetic field reaches values of up to 35 kA/m; (b) and (c) magnified winding window areas [to the left and to the right of the middle leg shown in (a), respectively]: the numbers inside the litz wires denote the turn number the conductor belongs to; “a” and “b” are used to distinguish between the 2 parallel wires.

Specifications:		
<i>Property</i>	<i>Value</i>	<i>Description</i>
L	15 μH	inductance
I_{peak}	30 A	maximum peak current
I	15 A	maximum RMS current
$B_{\text{peak,max}}$	150 mT	maximum peak flux density excitation of the ferrite core
J_{max}	10 A/mm ²	maximum RMS current density
Inductor Design Properties:		
<i>Property</i>	<i>Value</i>	<i>Description</i>
l_{g}	2.06 mm	total air gap length
$N_{L_{\text{HV}}}$	5	number of turns
$N_{\text{parallel,h}}$	1	number of horizontally arranged parallel conductors
$N_{\text{parallel,v}}$	2	number of vertically arranged parallel conductors
N_{cores}	5	number of employed cores (ELP 32 / PLT 32 combinations)
$l_{\text{wdg,core}}$	5 · 203 mm	litz wire length inside the core
$l_{\text{wdg,end turns}}$	5 · 49 mm	litz wire length due to the end turns
d_{c}	0.071 mm	litz wire, single strand copper diameter
n_{strands}	200	litz wire, number of strands

Table A.23: Specifications and properties of the sample inductor used to verify the calculations discussed in Appendix A.9.

and $f = 500 \text{ kHz}$ in Figure A.57). The slightly modified winding configuration depicted in Figure A.58 cancels this effect: there, the 2 parallel litz wires are twisted by 180° on one side in order to achieve an equal increase of the AC resistance for both litz wires. The measured AC resistance thus decreases from 33 m Ω to 22 m Ω (at $f = 100 \text{ kHz}$ in Figure A.59).

The evaluation of $\int_0^{d_{\text{el}}/2} \int_0^{2\pi} |\vec{H}(r, \varphi)|^2 r d\varphi dr$ enables the calculation of the winding’s AC resistance for different litz wires (Table A.25), whereas the AC resistance of the end turns is calculated on the assumption $\vec{H}_{\text{ext}}(r, \varphi) = \vec{0}$. Thus, in a final step, the optimal litz wire with respect to minimum AC re-

<i>Conductor Number</i>	1a	1b	2a	2b
$\int_0^{d_{tl}/2} \int_0^{2\pi} \vec{H}(r, \varphi) ^2 r d\varphi dr$	135.9 A ²	28.7 A ²	32.9 A ²	9.3 A ²

<i>Conductor Number</i>	3a	3b	4a	4b
$\int_0^{d_{tl}/2} \int_0^{2\pi} \vec{H}(r, \varphi) ^2 r d\varphi dr$	18.5 A ²	6.5 A ²	71.5 A ²	29.1 A ²

<i>Conductor Number</i>	5a	5b
$\int_0^{d_{tl}/2} \int_0^{2\pi} \vec{H}(r, \varphi) ^2 r d\varphi dr$	236.7 A ²	53.6 A ²

Table A.24: FEM simulator results for $\int_0^{d_{tl}/2} \int_0^{2\pi} |\vec{H}(r, \varphi)|^2 r d\varphi dr$ with respect to the different conductors depicted in Figure A.56; the outer conductor diameter used in the simulation is $d_{tl} = 1.51$ mm.

sistance is to be determined: with an increasing single strand copper diameter d_c , the effective copper area increases and the DC resistance decreases; however, with increasing d_c , the impact of high frequency effects increases, too (Table A.25). With the given data (Tables A.22, A.23, and A.24), minimum AC resistance is achieved with single strand copper diameters of either 0.071 mm or 0.1 mm. For the inductor winding, $d_c = 0.071$ mm and $n_{\text{strands}} = 200$ is selected due to the availability of the respective litz wire.¹⁵

For $d_c = 0.071$ mm, the difference between DC and AC winding resistances is rather small (14.5 mΩ vs. 15.2 mΩ; cf. Table A.25) and the impact of this difference on the total converter losses is negligible. Therefore, the presented calculation of the AC resistance is used to determine the appropriate single strand diameter $d_c = 0.071$ mm of the litz wire and the DC resistance, calculated for $d_c = 0.071$ mm, is used to approximately determine the resistance $R_{L_{\text{HV}}}$ used to calculate the inductor copper losses.

¹⁵The difference between the measured AC resistance of 22 mΩ and the calculated AC resistance of 15 mΩ is addressed to the precision of the Agilent 4294A Precision Impedance Analyzer: at $f = 100$ kHz, the accuracy of the resistance measurement is $\pm 42\%$, since the phase angle of the inductor's impedance is close to 90° (calculated according to [152]). Moreover, the measured total series resistance includes (small-signal) core losses, as well.

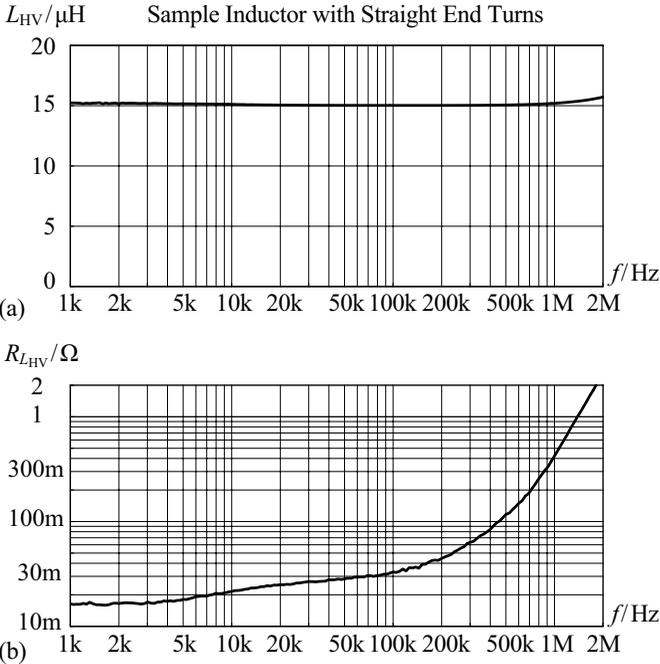


Figure A.57: Inductance and series resistance of the sample inductor (Table A.23) with straight end turns, measured with the Agilent 4294A Precision Impedance Analyzer: at $f = 100$ kHz, the accuracy of the resistance measurement is $\pm 30\%$, since the phase angle of the total impedance is very close to 90° (calculated according to [152]). Still, a considerable increase of R_{LHV} can be observed for $f > 5$ kHz due to different AC losses in each of the 2 parallel wires (cf. Table A.24).

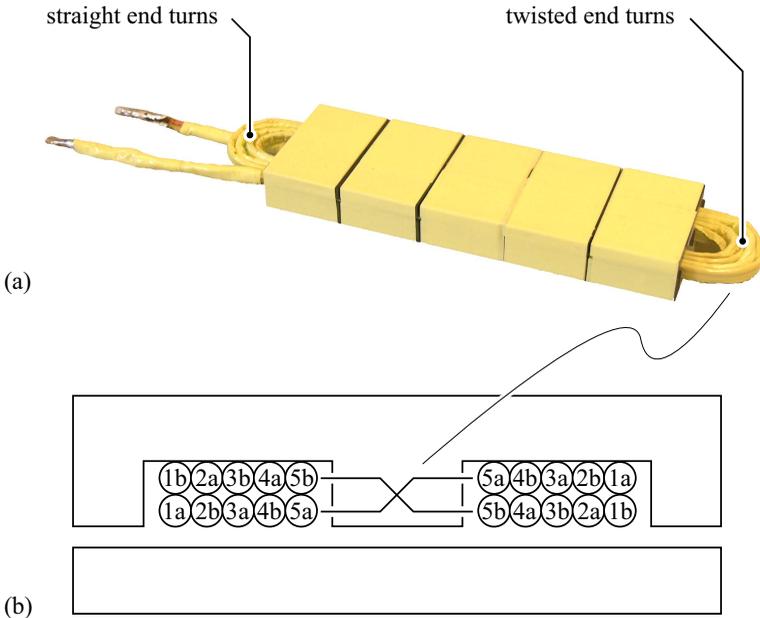


Figure A.58: (a) Picture of the sample inductor (Table A.23) with the modified winding configuration; an insulating tape holds the 2 parallel litz wires together. The picture shows the employed end turns: on the right side, the end turns are twisted by 180° in order to decrease the AC resistance of the inductor. (b) Cross-sectional drawing of the inductor to illustrate the resulting arrangement of the litz wires (cf. Figure A.56).

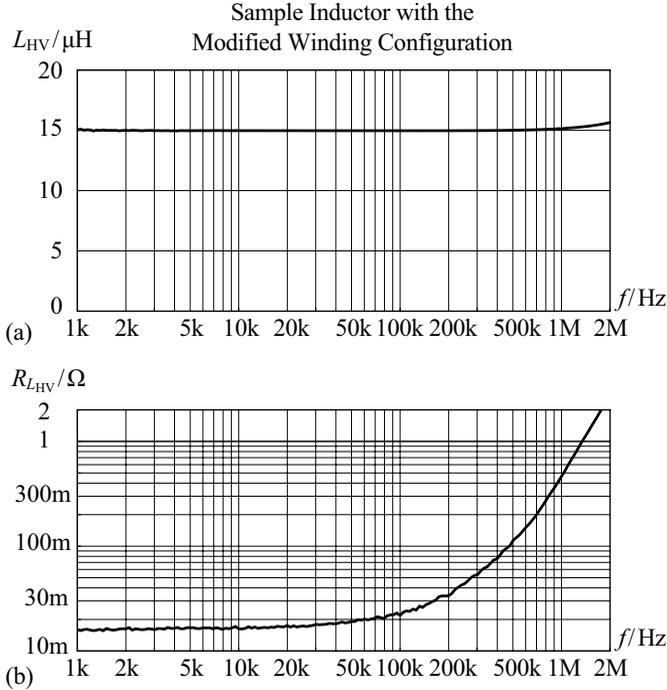


Figure A.59: Inductance and series resistance of the sample inductor (Table A.23) with twisted end turns on one side, according to Figure A.58, measured with the Agilent 4294A Precision Impedance Analyzer: at $f = 100\text{ kHz}$, the accuracy of the resistance measurement is $\pm 42\%$, since the phase angle of the total impedance is very close to 90° (calculated according to [152]). Still, compared to Figure A.57, a reduced AC resistance is observed for $5\text{ kHz} < f < 500\text{ kHz}$.

d_c	n_{strands}	d_{tl}	DC resistance R_{DC}	AC resistance R_{AC}
0.03 mm	964	1.51 mm	16.8 m Ω	16.9 m Ω
0.04 mm	569	1.51 mm	16.0 m Ω	16.2 m Ω
0.05 mm	378	1.51 mm	15.4 m Ω	15.7 m Ω
0.071 mm	200	1.51 mm	14.5 m Ω	15.2 m Ω
0.1 mm	106	1.51 mm	13.8 m Ω	15.2 m Ω
0.2 mm	29	1.49 mm	12.6 m Ω	19.1 m Ω
0.355 mm	10	1.48 mm	11.6 m Ω	33.1 m Ω

Table A.25: Number of strands, n_{strands} , and outer litz wire diameter, d_{tl} , calculated with the algorithm discussed in Appendix A.9.2. The DC resistance increases with decreasing values of the single strand copper diameter d_c due to a decrease of the effective copper area [i.e. $\beta_{\text{litz}} < 1$ in (A.178)]; the ratio $R_{\text{AC}}/R_{\text{DC}}$ increases with increasing d_c due to increasing AC losses (evaluated at $f = 100$ kHz). Regarding the shown numerical precision, minimum AC resistance is achieved with $d_c = 0.071$ mm and with $d_c = 0.1$ mm.

Appendix B

Converter Comparison: Calculation of the VA ratings

B.1 Semiconductor Switches

Following [116], the VA rating of each semiconductor switch is expressed with

$$S_{\text{switch}} = \max(V_{\text{switch,peak}}) \cdot \max(I_{\text{switch}}) \quad (\text{B.1})$$

using the maximum voltage applied to the switch, $\max(V_{\text{switch,peak}})$, and the maximum RMS current through the switch, $\max(I_{\text{switch}})$.

B.2 Transformer

The VA rating of a single-phase transformer with m windings (i.e. $m = 2$ for the transformer used for the DAB, Figure 2.10), operated with sinusoidal voltages and currents, is calculated with

$$S_{\text{tr}} = \frac{1}{2} \sum_{i=1}^m \hat{V}_{\text{tri}} \cdot \hat{I}_{\text{tri}}, \quad (\text{B.2})$$

whereas \hat{V}_{tri} denotes the RMS voltage applied to the i -th winding and \hat{I}_{tri} denotes the RMS current through the i -th winding [92]. In order to consider the increased component stress due to the wide operating range, (B.2) is

modified accordingly:¹

$$S_{\text{tr}} = \frac{1}{2} \sum_{i=1}^m \max(\hat{V}_{\text{tri}}) \cdot \max(\hat{I}_{\text{tri}}); \quad (\text{B.3})$$

there, $\max(\hat{V}_{\text{tri}})$ and $\max(\hat{I}_{\text{tri}})$ denote the maximum RMS values of the voltages and currents applied to the i -th winding, which are calculated within the operating ranges defined in Table 1.4.

However, none of the DC–DC converters discussed in Section 2.2 employs purely sinusoidal voltages and currents; accordingly the modified expression

$$S_{\text{tr}} = \frac{1}{2} \sum_{i=1}^m \max(V_{\text{tri,eq}}) \cdot \max(I_{\text{tri,eq}}) \quad (\text{B.4})$$

with

$$\begin{aligned} \frac{V_{\text{tri,eq}}}{\hat{V}_{\text{tri}}} &= \frac{\max\left(\int_0^{T_s} v_{\text{tri}}(t) dt\right) - \min\left(\int_0^{T_s} v_{\text{tri}}(t) dt\right)}{\max\left(\int_0^{T_s} \hat{v}_{\text{tri}}(t) dt\right) - \min\left(\int_0^{T_s} \hat{v}_{\text{tri}}(t) dt\right)} = \\ &= \frac{\max\left(\int_0^{T_s} v_{\text{tri}}(t) dt\right) - \min\left(\int_0^{T_s} v_{\text{tri}}(t) dt\right)}{\frac{\sqrt{2}}{\pi f_s} \hat{V}_{\text{tri}}} = \end{aligned} \quad (\text{B.5})$$

$$= \frac{\pi D}{\sqrt{2}} \frac{V_1}{\hat{V}_{\text{tri}}} \quad (\text{for rectangular voltages according to Figure 3.3}), \quad (\text{B.6})$$

$$I_{\text{tri,eq}} = \hat{I}_{\text{tri}}, \quad (\text{B.7})$$

is used instead of (B.3). There, the currents $I_{\text{tri,eq}}$ and the voltages $V_{\text{tri,eq}}$ are selected with respect to the resulting losses (on the assumptions of negligible high frequency effects and negligible stray and magnetizing inductances). Consequently, the employed current RMS values remain unchanged. The voltages $V_{\text{tri,eq}}$, however, are adjusted such that the peak magnetic flux density caused by $v_{\text{tri}}(t)$ becomes equal to the peak magnetic flux density caused by the sinusoidal voltage $\hat{v}_{\text{tri}}(t)$ [92].

B.3 AC and DC Inductors

Similar to (B.3), the VA rating of an AC inductor can be defined:

$$S_{\text{ind}} = \max(\hat{V}) \cdot \max(\hat{I}) \quad (\text{B.8})$$

¹On the assumptions of a limited value of the current density J_{max} in the winding and a limited value of the magnetic flux density $B_{\text{peak,max}}$ in the core, i.e. no thermal limitations apply.

$[\max(\hat{V})]$ denotes the maximum RMS voltage applied to the inductor and $[\max(\hat{I})]$ denotes the maximum RMS value of the AC component of the inductor current, calculated within the operating ranges defined in Table 1.4]. However, none of the DC–DC converters discussed in Section 2.2 employs purely sinusoidal inductor voltages and currents, and the modified expression

$$S_{\text{ind}} = \max(V_{\text{eq}}) \cdot \max(I_{\text{eq}}) \tag{B.9}$$

with

$$\begin{aligned} \frac{V_{\text{eq}}}{\hat{V}} &= \frac{\max\left(\int_0^{T_s} v(t) dt\right) - \min\left(\int_0^{T_s} v(t) dt\right)}{\max\left(\int_0^{T_s} \hat{v}(t) dt\right) - \min\left(\int_0^{T_s} \hat{v}(t) dt\right)} = \\ &= \frac{\max\left(\int_0^{T_s} v(t) dt\right) - \min\left(\int_0^{T_s} v(t) dt\right)}{\frac{\sqrt{2}}{\pi f_s} \hat{V}}, \end{aligned} \tag{B.10}$$

$$\frac{I_{\text{eq}}}{\hat{I}} = 1 \tag{B.11}$$

is used instead of (B.8), cf. Appendix B.2.

For DC inductors,² the VA rating defined with (B.8) is of no relevance: with increasing inductance L and unchanged inductor voltage $v(t)$, the RMS value of the AC component of the inductor current, \hat{I} , decreases and converges to 0 for $L \rightarrow \infty$. It is thus more meaningful to specify the peak magnetic energy $W_{\text{mag,peak}}$ stored in the DC inductor, since the inductor volume increases with increasing $W_{\text{mag,peak}}$ (Appendix B.3.1).

B.3.1 Theoretical Relation between $W_{\text{mag,peak}}$ and Inductor Volume V_L

The inductance L of an inductor with a magnetic core and an air gap (Figure B.1) is approximately:

$$L \approx \mu_0 N^2 \frac{A_{\text{Fe}}}{l}. \tag{B.12}$$

On the assumption of a maximum allowable peak current density $J_{\text{peak,max}}$ inside the winding window A_W and with a filling factor k_W

$$k_W A_W = \frac{N I_{\text{peak,max}}}{J_{\text{peak,max}}} \tag{B.13}$$

²For a DC inductor, the DC component of the inductor current is predominant.

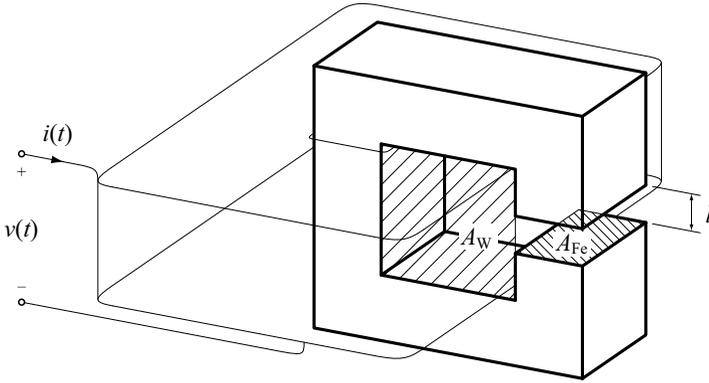


Figure B.1: Principle setup of an inductor with magnetic core and air gap.

applies and thus, the maximum allowable peak value of the winding current is:

$$I_{\text{peak,max}} = \frac{k A_W J_{\text{peak,max}}}{N}. \quad (\text{B.14})$$

The permissible peak flux density $B_{\text{peak,max}}$ defines a second requirement:

$$B_{\text{peak,max}} = \mu_0 \frac{N I_{\text{peak,max}}}{l}. \quad (\text{B.15})$$

With this, the stored magnetic energy is proportional to the product $A_{\text{Fe}} \cdot A_W$,

$$\begin{aligned} W_{\text{mag,peak}} &= \frac{1}{2} L I_{\text{peak,max}}^2 \stackrel{(\text{B.12})}{=} \frac{1}{2} N \cdot \underbrace{\left(\mu_0 N \frac{I_{\text{peak,max}}}{l} \right)}_{= B_{\text{peak,max}}, \text{ cf. (B.15)}} A_{\text{Fe}} I_{\text{peak,max}} = \\ &\stackrel{(\text{B.14})}{=} \frac{B_{\text{peak,max}} A_{\text{Fe}} A_W k J_{\text{peak,max}}}{2}. \quad (\text{B.16}) \end{aligned}$$

Provided that $B_{\text{peak,max}}$, k , and $J_{\text{peak,max}}$ are constant, $W_{\text{mag,peak}} \propto A_{\text{Fe}} A_W$

applies. With the scaling laws given in [92],

$$\frac{A_{\text{Fe}}}{A_{\text{Fe}}^*} = \left(\frac{Lin}{Lin^*} \right)^2 \quad (\text{B.17})$$

$$\frac{A_{\text{W}}}{A_{\text{W}}^*} = \left(\frac{Lin}{Lin^*} \right)^2 \quad (\text{B.18})$$

$$\frac{V_{\text{L}}}{V_{\text{L}}^*} = \left(\frac{Lin}{Lin^*} \right)^3 \quad (\text{B.19})$$

(Lin denotes a linear reference dimension, quantities without * denote the reference design values, and quantities with * denote all values obtained from the scaled design), the expression for $V_{\text{L}}/V_{\text{L}}^*$ can be rewritten [92]:

$$\frac{V_{\text{L}}}{V_{\text{L}}^*} = \left(\frac{W_{\text{mag,peak}}}{W_{\text{mag,peak}}^*} \right)^{\frac{3}{4}}. \quad (\text{B.20})$$

Thus,

$$\frac{w_{\text{mag,peak}}}{w_{\text{mag,peak}}^*} = \frac{W_{\text{mag,peak}}/V_{\text{L}}}{W_{\text{mag,peak}}^*/V_{\text{L}}^*} = \left(\frac{V_{\text{L}}}{V_{\text{L}}^*} \right)^{\gamma}, \quad \gamma = 1/3, \quad (\text{B.21})$$

results, i.e. the energy density of an inductor increases with increasing volume (the presented calculation, however, neglects thermal aspects; in case of a thermally limited design γ decreases [92]).

B.4 AC and DC Capacitors

Similar to the AC inductor, a VA rating can be defined for an AC capacitor with a given capacitance C :

$$S_{\text{cap}} = \max(\hat{V}) \cdot \max(\hat{I}) = \max(\hat{V} \cdot \hat{I}) = \frac{\max(\hat{I}^2)}{B_C}, \quad B_C = 2\pi f_s C. \quad (\text{B.22})$$

The VA rating is meaningless for DC capacitors and the peak electric energy storage capability $W_{\text{el,peak}}$ and the peak RMS capacitor current $\max(\hat{I})$ are used, instead:

- $W_{\text{el,peak}}$ is a figure for the expected capacitor volume (cf. Appendix B.4.1),
- depending on the capacitor technology (e.g. electrolytic capacitors, ceramic capacitors, film capacitors), $\max(\hat{I})$ may have a considerable impact on the required number of capacitors [138].

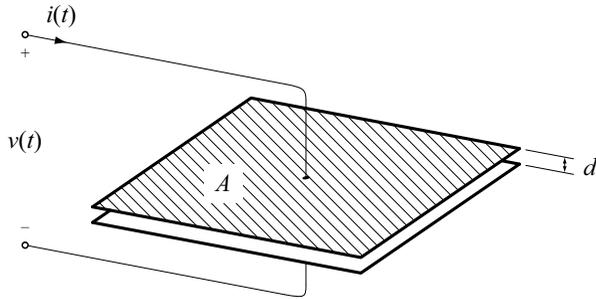


Figure B.2: Principle setup of a parallel-plate capacitor.

B.4.1 Theoretical Relation between $W_{\text{el,peak}}$ and Capacitor Volume V_C

The capacitance C of the parallel-plate capacitor depicted in Figure B.2 is given with:

$$C = \epsilon_0 \epsilon_r \frac{A}{d}; \quad (\text{B.23})$$

a dielectric material with $\epsilon = \epsilon_0 \epsilon_r$ fills the space between the two metal plates (provided that fringing effects are negligible). The respective capacitor volume is equal to:

$$V_C = A \cdot d. \quad (\text{B.24})$$

On the assumption of a maximum permissible peak value of the electric field strength $E_{\text{peak,max}}$ inside the dielectric material, the minimum distance d_{min} between the plates is:

$$d_{\text{min}} = \frac{V_{\text{peak,max}}}{E_{\text{peak,max}}} \quad (\text{B.25})$$

and the maximum allowable voltage is:

$$V_{\text{peak,max}} = d_{\text{min}} E_{\text{peak,max}}. \quad (\text{B.26})$$

With $d \rightarrow d_{\min}$ the energy stored in the parallel-plate capacitor becomes:

$$\begin{aligned} W_{\text{el,peak}} &= \frac{1}{2} C V_{\text{peak,max}}^2 = \frac{1}{2} \epsilon_0 \epsilon_r \frac{A}{d_{\min}} (d_{\min} E_{\text{peak,max}})^2 = \\ &= \frac{1}{2} \epsilon_0 \epsilon_r \underbrace{A d_{\min}}_{=V_{C,\min}} E_{\text{peak,max}}^2. \quad (\text{B.27}) \end{aligned}$$

Thus, in theory, the volume of a parallel-plate capacitor is proportional to the stored electric energy, $W_{\text{el}} \propto V_{C,\min}$.³

³According to (B.27), the capacitor volume should be directly proportional to C and $V_{\text{peak,max}}^2$, i.e. $V_C \propto C$ for constant $V_{\text{peak,max}}$ and $V_C \propto V_{\text{peak,max}}^2$ for constant C . Data sheet values confirm $V_C \propto C$; however, with increasing peak voltage $V_{\text{peak,max}}$, the capacitor volume rather increases according to $V_C \propto V_{\text{peak,max}}^\gamma$ with $1 < \gamma < 2$ (γ needs to be extracted from data sheet values for the selected type of capacitor).

Appendix C

Extracting the Steinmetz Coefficients

According to Chapter 4, the Steinmetz equation is used to estimate the core losses P_{core} of the transformer and the inductor:

$$P_{\text{core}} \approx V_{\text{core}} k f^\alpha B_{\text{peak}}^\beta \quad (\text{C.1})$$

(V_{core} denotes the respective core volume, B_{peak} is the respective peak flux density, and f is the excitation frequency). The Steinmetz coefficients k , α , and β are obtained from data sheet values using a least mean square (LMS) approximation. In order to obtain a polynomial function suitable for the LMS approximation, the natural logarithm is first applied to (C.1),

$$\ln(p_{\text{core}}) = \ln(P_{\text{core}}/V_{\text{core}}) = \ln(k) + \alpha \ln(f) + \beta \ln(B_{\text{peak}}) \quad (\text{C.2})$$

(p_{core} denotes the core loss density), and the LMS approximation is accomplished with respect to $\ln(k)$, α , and β . The employed input data $p_{\text{core}}(f, B_{\text{peak}})$ and the calculated Steinmetz coefficients are given in Table C.1 for the N87 ferrite [160] and in Table C.2 for the 3F3 ferrite [161].

In Figure C.1 and Figure C.2 the input data listed in Table C.1 is compared to the values calculated with (C.1). For $T_{\text{core}} = 25^\circ\text{C}$ the maximum relative error due to the Steinmetz approximation (C.1) is 21% and the average relative error is 9.3%; for $T_{\text{core}} = 100^\circ\text{C}$ the maximum relative error is 30% and the average relative error is 11%. Figure C.3 compares the input data listed in Table C.2 to the values calculated with (C.1); the resulting maximum relative error is 19% and the average relative error is 8.8%.

In [161] the core losses of the 3F3 ferrite material are comprehensively characterized for $T_{\text{core}} = 100^\circ\text{C}$. Since the DAB converter model presented in Chapter 4 is parameterized for $T_{\text{core}} = 25^\circ\text{C}$, the Steinmetz parameters listed in Table C.2 need to be modified. According to Table C.1, all 3 Steinmetz

f	B_{peak}	p_{core}	k	α	β
Ferrite material: N87, core temperature: $T_{\text{core}} = 25^\circ\text{C}$ [160]					
50 kHz	50 mT	11 kW/m ³	14.1	1.27	2.42
50 kHz	100 mT	67 kW/m ³			
50 kHz	200 mT	285 kW/m ³			
100 kHz	25 mT	4.1 kW/m ³			
100 kHz	50 mT	67 kW/m ³			
100 kHz	100 mT	128 kW/m ³			
100 kHz	200 mT	650 kW/m ³			
200 kHz	25 mT	9.9 kW/m ³			
200 kHz	50 mT	50 kW/m ³			
200 kHz	100 mT	320 kW/m ³			
200 kHz	200 mT	1.4 MW/m ³			
300 kHz	25 mT	19 kW/m ³			
300 kHz	50 mT	100 kW/m ³			
300 kHz	100 mT	627 kW/m ³			
300 kHz	200 mT	3.1 MW/m ³			
Ferrite material: N87, core temperature: $T_{\text{core}} = 100^\circ\text{C}$ [160]					
50 kHz	50 mT	2.4 kW/m ³	0.0786	1.72	2.74
50 kHz	100 mT	17 kW/m ³			
50 kHz	200 mT	141 kW/m ³			
50 kHz	300 mT	426 kW/m ³			
100 kHz	25 mT	1.2 kW/m ³			
100 kHz	50 mT	7.8 kW/m ³			
100 kHz	100 mT	51 kW/m ³			
100 kHz	200 mT	393 kW/m ³			
200 kHz	25 mT	6.2 kW/m ³			
200 kHz	50 mT	30 kW/m ³			
200 kHz	100 mT	175 kW/m ³			
200 kHz	200 mT	1.2 MW/m ³			

Table C.1: Core loss densities of the N87 ferrite material for different excitation frequencies and different peak flux densities (from [160]); the Steinmetz parameters are obtained with a least mean square approximation.

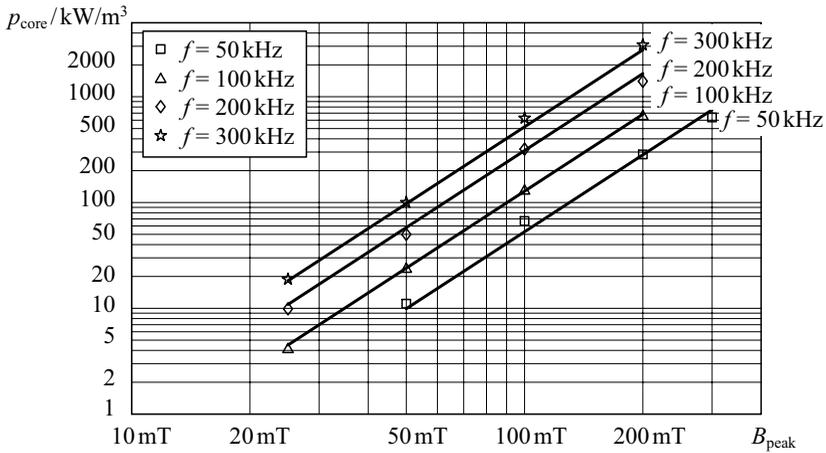


Figure C.1: Comparison of the core loss densities calculated with (C.1) (solid lines) to the core loss densities obtained from the data sheet [160]; ferrite material: N87, core temperature: 25°C .

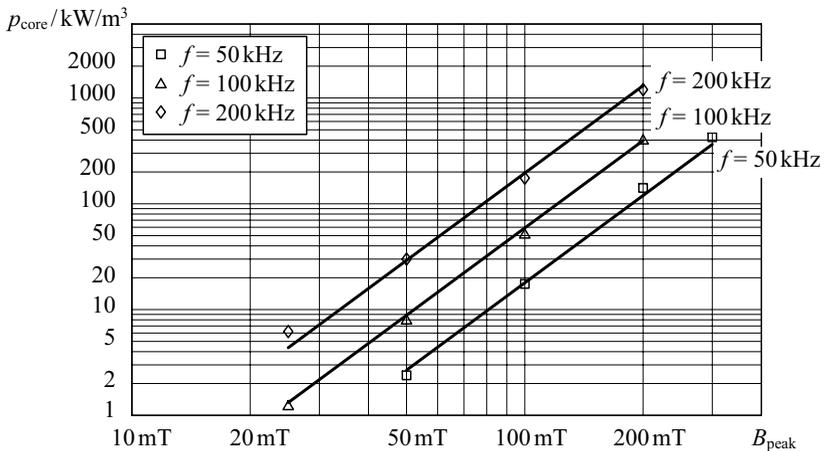


Figure C.2: Comparison of the core loss densities calculated with (C.1) (solid lines) to the core loss densities obtained from the data sheet [160]; ferrite material: N87, core temperature: 100°C .

f	B_{peak}	p_{core}	k	α	β
Ferrite material: 3F3, core temperature: $T_{\text{core}} = 100^\circ\text{C}$ [161]					
25 kHz	100 mT	12.5 kW/m ³	6.79	1.34	2.63
25 kHz	200 mT	85 kW/m ³			
25 kHz	300 mT	220 kW/m ³			
100 kHz	60 mT	17 kW/m ³			
100 kHz	70 mT	27 kW/m ³			
100 kHz	100 mT	70 kW/m ³			
100 kHz	200 mT	480 kW/m ³			
200 kHz	40 mT	20 kW/m ³			
200 kHz	70 mT	88 kW/m ³			
200 kHz	100 mT	215 kW/m ³			
200 kHz	200 mT	1.15 MW/m ³			

Table C.2: Core loss densities of the 3F3 ferrite material for different excitation frequencies and different peak flux densities (from [161]); the Steinmetz parameters are obtained with a least mean square approximation.

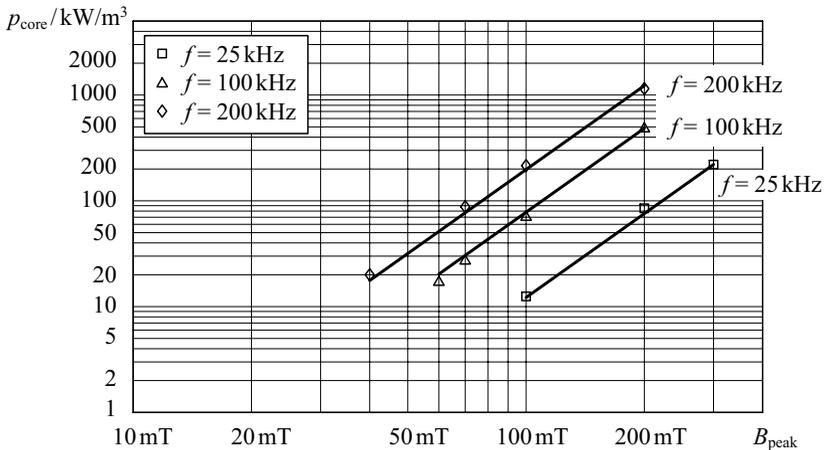


Figure C.3: Comparison of the core loss densities calculated with (C.1) (solid lines) to the core loss densities obtained from the data sheet [161]; ferrite material: 3F3, core temperature: 100°C .

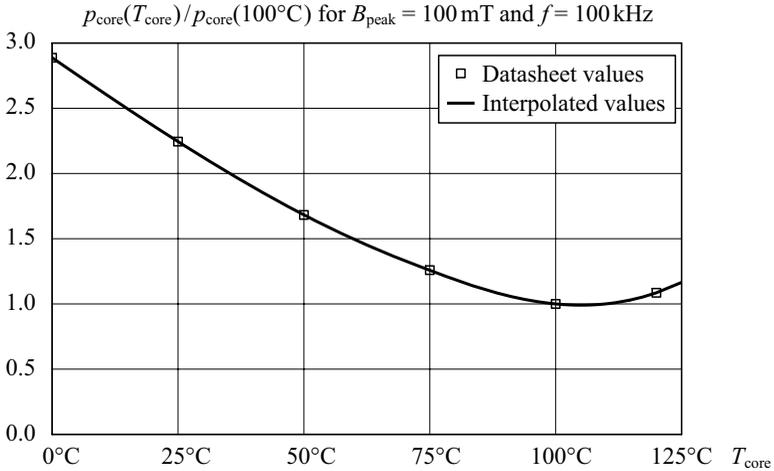


Figure C.4: Relative temperature dependency of the core losses (ferrite: 3F3) for an excitation frequency of 100 kHz and for a peak flux density of 100 mT [161].

parameters are expected to change due to the change of the core temperature; however, in [161], the temperature dependency of the core losses is only specified for selected combinations of B_{peak} and f (e.g. for $B_{\text{peak}} = 100 \text{ mT}$ and $f = 100 \text{ kHz}$ in Figure C.4), which is insufficient to calculate k , α , and β . For the DAB converter, the switching frequency is 100 kHz and the peak magnetic flux densities in the transformer core and in the inductor core are typically close to 100 mT. Thus, solely the Steinmetz parameter k is scaled according to the function depicted in Figure C.4 and α and β remain unmodified. This approximation is considered accurate enough for the given DAB converter, since, at rated output power, the total core losses (inductor and transformer) are found to account for less than 10% of the total losses. If more accurate Steinmetz parameters are required, the core losses first need to be measured and, subsequently, k , α , and β are obtained from a least mean square optimization using (C.2).

Appendix D

Evaluation of Power MOSFETs

The decisions on the power semiconductors used for the DAB are mainly based on the maximum blocking voltages and the maximum switch RMS currents calculated in Appendix A.2. On the LV side, MOSFETs are most suitable due to low voltage and high current ratings [162]. On the HV side, either IGBTs or MOSFETs could be used: at high currents, IGBTs offer lower on-state losses than MOSFETs, however, the turn-off losses of IGBTs are considerably higher than the turn-off losses of MOSFETs. Regarding the peak switch currents of up to 24 A during turn-off,¹ the high switching frequency of 100 kHz (Table 1.4), and the required voltage and current ratings of the semiconductor switches, MOSFETs are found to be superior to IGBTs; therefore, the HV side full bridge also employs MOSFETs.

D.1 HV Side

D.1.1 Selection of the MOSFETs used for the DAB Converter

The HV side full bridge of the DAB converter requires MOSFETs with a maximum blocking voltage of 450 V. Considering a safety margin of 30%, the drain-source breakdown voltage of the selected MOSFET, $V_{(BR)DSS}$, should be at least 585 V. The maximum switch RMS current is 11 A for phase shift modulation [Table A.1 and (4.18)].

With the alternative modulation schemes, detailed in Section 5, hard switching operation does not occur during steady-state operation of the DAB. During transient operation, however, sporadic hard switching processes may occur. Therefore, acceptable reverse recovery characteristics of the MOSFETs' body diodes is required in order to ensure reliable converter operation.

¹Efficiency optimal operation of the DAB, Table A.1.

Considering the MOSFETs listed in Table D.1, three devices are most suitable: IXFH36N60P (IXYS), SPW47N60CFD (Infineon), and STW77N65M5 (ST Microelectronics). Amongst these MOSFETs, the STW77N65M5 facilitates minimum conduction losses (≈ 3.6 W per MOSFET at $I_D = 11$ A and $T_j = 25^\circ\text{C}$; typ. $R_{DS,on} = 30$ m Ω); however, the reverse recovery charge of the body diode is comparably large (Table D.2). Conversely, the IXFH36N60P contains a body diode with a low reverse recovery charge but the device generates high conduction losses. The SPW47N60CFD presents a trade-off; its low on-state resistance (typ. 70 m Ω at $I_D = 29$ A, $V_{GS} = 10$ V, and $T_j = 25^\circ\text{C}$) allows for comparably low conduction losses (≈ 8.5 W per MOSFET at $I_D = 11$ A and $T_j = 25^\circ\text{C}$) and the low reverse recovery charge ensures reliable converter operation.

D.1.2 Drain-Source Breakdown Voltages and On-State Resistances

On the HV side, all single-stage topologies regarded in Appendix A require semiconductor switches with a rated voltage of 450 V. However, for the two-stage topologies discussed in Chapter 7, semiconductors with a different voltage rating may be considered. Therefore, in Table D.1, a selection of MOSFETs with different drain-source breakdown voltages is presented. In order to allow for a comparison, all considered MOSFETs employ the TO-247 package. Moreover, each table entry gives the device with the maximum available continuous drain current amongst all devices available in the TO-247 package for a certain type series.

Most commonly, the vertical MOSFET structure is used to realize power MOSFETs in order to achieve both: a low on-state resistance and a high blocking voltage capability. According to [150], the on-state resistance of the device is almost identical to the resistance of the epitaxial layer, $R_{DS,on} \approx R_{epi}$, for high blocking voltages. The relative resistance of the epitaxial layer, $A_{chip} \cdot R_{epi}$, scales according to:

$$A_{chip} \cdot R_{epi} \propto V_{(BR)DSS}^{\frac{5}{2}} \quad (\text{D.1})$$

(A_{chip} is the surface of the semiconductor) [150]. With increasing breakdown voltage the relative resistance $A_{chip} \cdot R_{epi}$ increases by more than $V_{(BR)DSS}^2$. Thus, a MOSFET with a higher breakdown voltage requires a larger chip area in order to maintain a given current carrying capability for a given maximum junction temperature.

The so-called super-junction devices facilitate a more effective utilization of the available chip surface. There, the relative resistance of the epitaxial layer scales according to [150]:

$$A_{chip} \cdot R_{epi} \propto V_{(BR)DSS}^{\frac{7}{6}} \quad (\text{D.2})$$

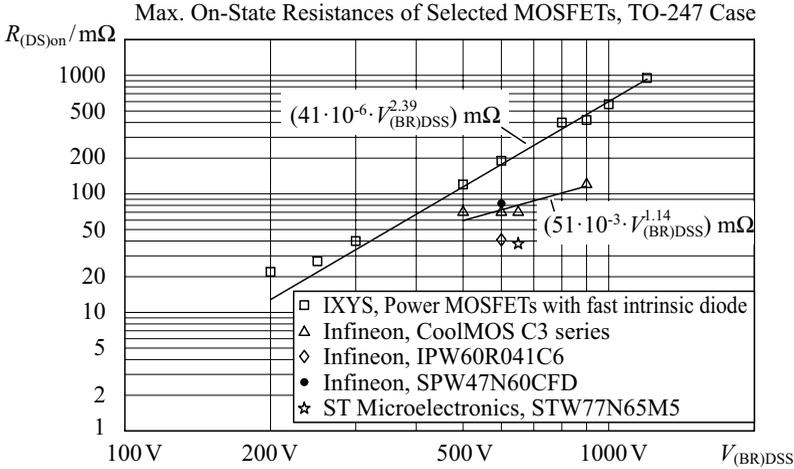


Figure D.1: On-state resistances of selected MOSFETs in the TO-247 package with drain-source breakdown voltages $V_{(BR)DSS}$ between 200 V and 1200 V.

Thus, the chip area required to maintain a given current carrying capability (for a given maximum junction temperature) becomes smaller if the breakdown voltage increases.

Figure D.1 depicts the on-state resistances of the MOSFETs listed in Table D.1 at $T_j = 25^\circ\text{C}$. For $V_{(BR)DSS} > 300$ V, the on-state resistances of the IXYS power MOSFETs increase approximately proportional to $V_{(BR)DSS}^{2.39}$. Conversely, the on-state resistances of the super-junction CoolMOS MOSFETs scale approximately proportional to $V_{(BR)DSS}^{1.14}$.²

Except for the CoolMOS with $V_{(BR)DSS} = 900$ V, IPW90R120C3, highly optimized MOSFETs are only available for $V_{(BR)DSS}$ close to 600 V. Besides, the IPW90R120C3 is not considered to be used for the DAB due to the large reverse recovery charge of the body diode (Table D.2).

²Provided that all the listed power MOSFETs employ the same chip areas, the relations between $R_{DS,on}$ and $V_{(BR)DSS}$, given in Figure D.1, directly apply to $A_{chip} \cdot R_{epi}$. Thus, a vertical MOSFET structure seems to be employed for the IXYS MOSFETs; the CoolMOS MOSFETs employ the super-junction technology.

<i>Manufacturer's part designation</i>	<i>Drain-source breakdown voltage</i> $V_{(BR)DSS}$	<i>Continuous drain current</i> I_D (case temp.: 25°C)	<i>Max. on-state resistance</i> $R_{DS,on}$ ($V_{GS} = 10$ V, $T_j = 25^\circ\text{C}$)
IXYS, Power MOSFETs with fast intrinsic diode, TO-247 package			
IXFH120N20P	200 V	120 A	22 m Ω ($I_D = 60$ A)
IXFH100N25P	250 V	100 A	27 m Ω ($I_D = 50$ A)
IXFH88N30P	300 V	88 A	40 m Ω ($I_D = 44$ A)
IXFH52N50P2	500 V	52 A	120 m Ω ($I_D = 26$ A)
IXFH36N60P	600 V	36 A	190 m Ω ($I_D = 18$ A)
IXFH24N80P	800 V	24 A	400 m Ω ($I_D = 12$ A)
IXFH24N90P	900 V	24 A	420 m Ω ($I_D = 12$ A)
IXFH20N100P	1000 V	20 A	570 m Ω ($I_D = 10$ A)
IXFH16N120P	1200 V	16 A	950 m Ω ($I_D = 8$ A)
CoolMOS, C3 series, TO-247 package			
SPW52N50C3	500 V	52 A	70 m Ω ($I_D = 30$ A)
SPW47N60C3	600 V	47 A	70 m Ω ($I_D = 30$ A)
SPW47N65C3	650 V	47 A	70 m Ω ($I_D = 30$ A)
IPW90R120C3	900 V	36 A	120 m Ω ($I_D = 26$ A)
Selected miscellaneous power MOSFETs, TO-247 package			
IPW60R041C6	600 V	77.5 A	41 m Ω ($I_D = 44.4$ A)
SPW47N60CFD	600 V	46 A	83 m Ω ($I_D = 29$ A)
STW77N65M5	650 V	69 A	38 m Ω ($I_D = 34.5$ A)

Table D.1: Drain-source breakdown voltages $V_{(BR)DSS}$, continuous drain currents I_D , and maximum on-state resistances $R_{DS,on}$ of the power MOSFETs used for the survey depicted in Figure D.1 (data sheet information obtained from [153, 158, 163]). All listed MOSFETs employ the TO-247 package. Moreover, amongst all devices available in the TO-247 package for a certain type series, each table entry gives the device with the maximum available continuous drain current.

Manufacturer's part designation	$V_{(\text{BR})\text{DSS}}$	Body diode: reverse recovery charge Q_{rr} , peak reverse recovery current I_{rrm}		
		Q_{rr}	I_{rrm}	Measurement conditions (besides $-di_{\text{D}}/dt = 100 \text{ A}/\mu\text{s}$, $T_{\text{j}} = 25^{\circ}\text{C}$)
IXYS, Power MOSFETs with fast intrinsic diode, TO-247 package				
IXFH120N20P	200 V	0.4 μC	6 A	$I_{\text{D}} = -25 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$
IXFH100N25P	250 V	0.6 μC	10 A	$I_{\text{D}} = -25 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$
IXFH88N30P	300 V	0.6 μC	—	$I_{\text{D}} = -25 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$
IXFH52N50P2	500 V	1.3 μC	14 A	$I_{\text{D}} = -26 \text{ A}$, $V_{\text{DS}} = 85 \text{ V}$
IXFH36N60P	600 V	0.8 μC	6 A	$I_{\text{D}} = -25 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$
IXFH24N80P	800 V	0.8 μC	6 A	$I_{\text{D}} = -25 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$
IXFH24N90P	900 V	1.1 μC	11 A	$I_{\text{D}} = -12 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$
IXFH20N100P	1000 V	0.9 μC	9 A	$I_{\text{D}} = -10 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$
IXFH16N120P	1200 V	0.75 μC	7.5 A	$I_{\text{D}} = -8 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$
Infineon, CoolMOS, C3 series, TO-247 package				
SPW52N50C3	500 V	20 μC	70 A	$I_{\text{D}} = -52 \text{ A}$, $V_{\text{DS}} = 380 \text{ V}$
SPW47N60C3	600 V	23 μC	73 A	$I_{\text{D}} = -47 \text{ A}$, $V_{\text{DS}} = 350 \text{ V}$
SPW47N65C3	650 V	19 μC	56 A	$I_{\text{D}} = -47 \text{ A}$, $V_{\text{DS}} = 480 \text{ V}$
IPW90R120C3	900 V	30 μC	65 A	$I_{\text{D}} = -26 \text{ A}$, $V_{\text{DS}} = 400 \text{ V}$
Selected miscellaneous power MOSFETs, TO-247 package				
IPW60R041C6	600 V	32 μC	62 A	$I_{\text{D}} = -44.4 \text{ A}$, $V_{\text{DS}} = 400 \text{ V}$
SPW47N60CFD	600 V	2 μC	18 A	$I_{\text{D}} = -46 \text{ A}$, $V_{\text{DS}} = 480 \text{ V}$
STW77N65M5	650 V	12 μC	46 A	$I_{\text{D}} = -34.5 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$

Table D.2: Reverse recovery characteristics of the body diodes of the power MOSFETs listed in Table D.1 (data sheet information obtained from [153, 158, 163]).

D.2 LV Side

At the time the LV side full bridge of the DAB was designed, the IRF2804 MOSFET offered the lowest on-state resistance in the TO-220 package (max. $R_{DS,on} = 2.3 \text{ m}\Omega$ at $T_j = 25^\circ\text{C}$) for a drain-source breakdown voltage of 40 V (for the DAB, the selection of the LV MOSFETs is detailed in Appendix A.2 on page 289).³ Meanwhile, suitable MOSFETs with an on-state resistance below $2.3 \text{ m}\Omega$ are available (Table D.3), which could be used instead of the IRF2804.

D.2.1 Drain-Source Breakdown Voltages and On-State Resistances

Some of the topologies designed in Appendix A require switches with blocking voltages different to 16 V.

- The bidirectional full bridge converter with LV side DC inductor (Appendix A.5) requires switches with a maximum blocking voltage of 37.5 V on the LV side.
- The LV side switches of the bidirectional current doubler (Appendix A.6) and of the bidirectional push pull converter (Appendix A.7) are exposed to a maximum blocking voltage of 75 V (on the assumption of negligible voltage spikes).

Table D.3 and Figure D.2 present suitable MOSFETs (TO-220 package) for this low voltage and high current application. For drain-source breakdown voltages between 100 V and 200 V, the on-state resistance of the selected devices are approximately proportional to $V_{(BR)DSS}^2$ (Figure D.2). However, for $V_{(BR)DSS} < 100 \text{ V}$, the on-state resistances are considerably higher than the on-state resistances predicted with the least mean square approximations. Thus, for $V_{(BR)DSS} < 100 \text{ V}$, MOSFETs with a higher breakdown voltage are capable of a higher VA rating, which is demonstrated below.

According to Table D.3, a new converter design may consider the MOSFETs listed below.

- DAB converter: IPP015N04N with $R_{DS,on} = 1.5 \text{ m}\Omega$;
- full bridge converter: IPP023NE7N3 with $R_{DS,on} = 2.3 \text{ m}\Omega$ (due to possible overvoltage spikes, a drain-source breakdown voltage of at least $1.5 \cdot 37.5 \text{ V} = 56 \text{ V}$ is considered);

³At the time the LV side full bridge of the DAB was designed, only surface-mounted MOSFETs offered a higher power density (in particular the IRF2804S-7P with a maximum on-state resistance of $1.6 \text{ m}\Omega$ at $T_j = 25^\circ\text{C}$). However, compared to through-hole components, it is considerably more difficult to attach surface-mounted devices to a heat sink and therefore, through-hole components are preferred.

- current doubler, push pull converter: IPP041N12N3 with $R_{DS,on} = 4.1 \text{ m}\Omega$ (due to possible overvoltage spikes, a drain-source breakdown voltage of at least $1.5 \cdot 75 \text{ V} = 113 \text{ V}$ is considered).

With the selected MOSFETs, the following conduction losses are calculated for the different converter topologies ($T_j = 25^\circ\text{C}$ is assumed).

- DAB converter: the maximum switch RMS current is 163 A [suboptimal modulation scheme, Table A.1 and (4.25)]; with 4 switches, the total conduction losses are:

$$P_{S2,cond} = 4 \cdot (163 \text{ A})^2 \cdot 1.5 \text{ m}\Omega = 159 \text{ W}. \quad (\text{D.3})$$

- Full bridge converter: the maximum switch RMS current is 157 A and with 4 switches, the total conduction losses are:

$$P_{S2,cond} = 4 \cdot (157 \text{ A})^2 \cdot 2.3 \text{ m}\Omega = 227 \text{ W}. \quad (\text{D.4})$$

- Current doubler: each switch operates 2 MOSFETs in parallel in order to allow for a comparison with the DAB and with the full bridge converter; the maximum switch RMS current is 159 A. Thus, the total conduction losses are:

$$P_{S2,cond} = 2 \cdot 2 \cdot (79.5 \text{ A})^2 \cdot 4.1 \text{ m}\Omega = 104 \text{ W}. \quad (\text{D.5})$$

- Push pull converter: each switch operates 2 MOSFETs in parallel in order to allow for a comparison with the DAB and with the full bridge converter. The maximum switch RMS current is 157 A and the total conduction losses are:

$$P_{S2,cond} = 2 \cdot 2 \cdot (78.5 \text{ A})^2 \cdot 4.1 \text{ m}\Omega = 101 \text{ W}. \quad (\text{D.6})$$

Thus, lowest conduction losses result with the push pull converter, even though the VA rating of the respective switches is higher than for the DAB (push pull converter: 23.5 kVA, DAB: 10.5 VA).

<i>Manufacturer's part designation</i>	<i>Drain-source breakdown voltage</i> $V_{(\text{BR})\text{DSS}}$	<i>Continuous drain current</i> I_{D} (case temp.: 25°C)	<i>Max. on-state resistance</i> $R_{\text{DS,on}}$ ($V_{\text{GS}} = 10 \text{ V}$, $T_{\text{j}} = 25^\circ\text{C}$)
International Rectifier, HEXFET, TO-220 package			
AUIRF1324	24 V	195 A	1.5 m Ω ($I_{\text{D}} = 195 \text{ A}$)
IRLB3034PBF	40 V	195 A	1.7 m Ω ($I_{\text{D}} = 195 \text{ A}$)
IRLB3036PBF	60 V	195 A	2.4 m Ω ($I_{\text{D}} = 165 \text{ A}$)
IRFB3077GPBF	75 V	120 A	3.3 m Ω ($I_{\text{D}} = 75 \text{ A}$)
IRFL4030PBF	100 V	180 A	4.3 m Ω ($I_{\text{D}} = 110 \text{ A}$)
IRFB4115GPBF	150 V	104 A	11 m Ω ($I_{\text{D}} = 62 \text{ A}$)
IRFB4127PBF	200 V	76 A	20 m Ω ($I_{\text{D}} = 44 \text{ A}$)
IRFB4332PBF	250 V	60 A	33 m Ω ($I_{\text{D}} = 35 \text{ A}$)
Infineon, OptiMOS, TO-220 package			
IPP015N04N	40 V	120 A	1.5 m Ω ($I_{\text{D}} = 100 \text{ A}$)
IPP023NE7N3	75 V	120 A	2.3 m Ω ($I_{\text{D}} = 100 \text{ A}$)
IPP028N08N3	80 V	100 A	2.8 m Ω ($I_{\text{D}} = 100 \text{ A}$)
IPP030N10N3	100 V	100 A	3.0 m Ω ($I_{\text{D}} = 100 \text{ A}$)
IPP041N12N3	120 V	120 A	4.1 m Ω ($I_{\text{D}} = 100 \text{ A}$)
IPP075N15N3	150 V	100 A	7.5 m Ω ($I_{\text{D}} = 100 \text{ A}$)
IPP110N20N3	200 V	88 A	11 m Ω ($I_{\text{D}} = 88 \text{ A}$)
IPP200N25N3	250 V	64 A	20 m Ω ($I_{\text{D}} = 64 \text{ A}$)

Table D.3: Drain-source breakdown voltages $V_{(\text{BR})\text{DSS}}$, continuous drain currents I_{D} , and maximum on-state resistances $R_{\text{DS,on}}$ of the power MOSFETs used for the survey depicted in Figure D.2 (data sheet information obtained from [153,164]). All listed MOSFETs employ the TO-220 package. Moreover, amongst all devices available in the TO-220 package for a certain type series, each table entry gives the device with the maximum available continuous drain current.

Manufacturer's part designation	$V_{(\text{BR})\text{DSS}}$	Body diode: reverse recovery charge Q_{rr} , peak reverse recovery current I_{rrm}		
		Q_{rr}	I_{rrm}	Measurement conditions (besides $-di_{\text{D}}/dt = 100 \text{ A}/\mu\text{s}$, $T_{\text{j}} = 25^{\circ}\text{C}$)
International Rectifier, HEXFET, TO-220 package				
AUIRF1324	24 V	160 nC	7.7 A	$I_{\text{D}} = -195 \text{ A}$, $V_{\text{DS}} = 20 \text{ V}$
IRLB3034PBF	40 V	39 nC	1.7 A	$I_{\text{D}} = -195 \text{ A}$, $V_{\text{DS}} = 34 \text{ V}$
IRLB3036PBF	60 V	310 nC	4.4 A	$I_{\text{D}} = -165 \text{ A}$, $V_{\text{DS}} = 51 \text{ V}$
IRFB3077GPBF	75 V	89 nC	2.5 A	$I_{\text{D}} = -75 \text{ A}$, $V_{\text{DS}} = 64 \text{ V}$
IRLB4030PBF	100 V	88 nC	3.3 A	$I_{\text{D}} = -110 \text{ A}$, $V_{\text{DS}} = 85 \text{ V}$
IRFB4115GPBF	150 V	300 nC	6.5 A	$I_{\text{D}} = -62 \text{ A}$, $V_{\text{DS}} = 130 \text{ V}$
IRFB4127PBF	200 V	458 nC	8.3 A	$I_{\text{D}} = -44 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$
IRFB4332PBF	250 V	820 nC	—	$I_{\text{D}} = -35 \text{ A}$, $V_{\text{DS}} = 50 \text{ V}$
Infineon, OptiMOS, TO-220 package				
IPP015N04N	40 V	141 nC	—	$I_{\text{D}} = -120 \text{ A}$, $V_{\text{DS}} = 15 \text{ V}$
IPP023NE7N3	75 V	129 nC	—	$I_{\text{D}} = -120 \text{ A}$, $V_{\text{DS}} = 37.5 \text{ V}$
IPP028N08N3	80 V	317 nC	—	$I_{\text{D}} = -100 \text{ A}$, $V_{\text{DS}} = 40 \text{ V}$
IPP030N10N3	100 V	232 nC	—	$I_{\text{D}} = -100 \text{ A}$, $V_{\text{DS}} = 50 \text{ V}$
IPP041N12N3	120 V	356 nC	—	$I_{\text{D}} = -120 \text{ A}$, $V_{\text{DS}} = 60 \text{ V}$
IPP075N15N3	150 V	478 nC	—	$I_{\text{D}} = -100 \text{ A}$, $V_{\text{DS}} = 75 \text{ V}$
IPP110N20N3	200 V	640 nC	—	$I_{\text{D}} = -88 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$
IPP200N25N3	250 V	780 nC	—	$I_{\text{D}} = -64 \text{ A}$, $V_{\text{DS}} = 100 \text{ V}$

Table D.4: Reverse recovery characteristics of the body diodes of the power MOSFETs listed in Table D.3 (data sheet information obtained from [153, 164]).

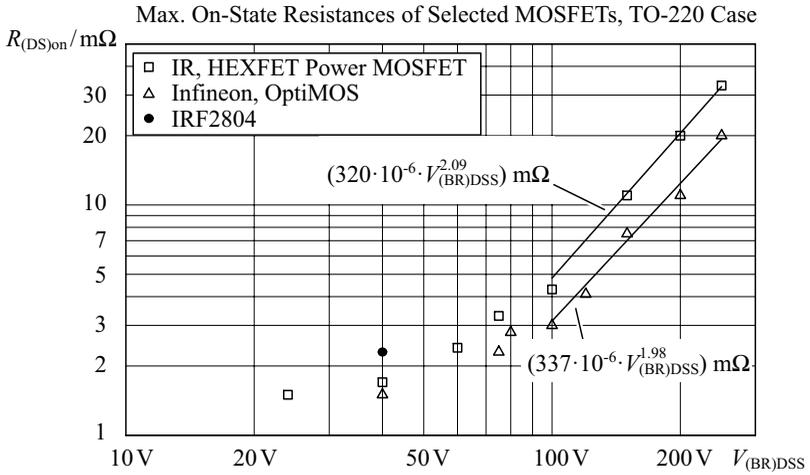


Figure D.2: On-state resistances of selected MOSFETs in the TO-220 package with drain-source breakdown voltages $V_{(BR)DSS}$ between 24 V and 250 V.

Appendix E

Practical Implementation

E.1 Digital Control: Concept

A digital signal processor (DSP) controls the converter currents and voltages according to the block diagram depicted in Figure 6.2. The DSP runs the PI controllers, interfaces to current and voltage measurement peripherals (A/D converters), monitors overcurrent and overvoltage conditions in order to ensure safe converter operation, and communicates with a control PC which is used to start and stop the bidirectional DC-DC converter and to adjust the output voltage. The DSP as well calculates the different timing parameters, i.e. the phase shift time $\varphi/(2\pi f_s)$, the HV side duty cycle duration D_1/f_s , and the LV side duty cycle duration D_2/f_s (cf. Section E.2), and interfaces to a programmable logic device (field programmable gate array, FPGA) that generates the dedicated gate signals (Section E.3).

The employed DSP is a TMS320F2808 (Texas Instruments) operated with a clock frequency of 100 MHz; the software is implemented in the computer language C. For the FPGA, the device LCMXO2280, Lattice Semiconductor, operated with a clock frequency of 100 MHz, is employed; the hardware description language VHDL is used to program the FPGA.

E.2 On-Line Calculation of the Modulation Parameters

Except for phase shift modulation, elaborate numerical calculations are required in order to determine the 3 timing parameters φ , D_1 , and D_2 depending on the operating point defined with V_1 , V_2 , and P_{out} (Section 5). With the given computational power of the DSP, on-line parameter calculation is not feasible. In order to still run the discussed extended modulation methods, the respective timing parameters are calculated off-line for a set of basic values

and stored in a table on the DSP. The controller software then uses linear interpolation to approximately determine the actual timing parameters.

Each timing parameter depends on the current operating point, characterized by V_1 , V_2 , and P_{out} : $\varphi(V_1, V_2, P_{\text{out}})$, $D_1(V_1, V_2, P_{\text{out}})$, and $D_2(V_1, V_2, P_{\text{out}})$. Consequently, a 3-D table is required for every timing parameter to store the basic values; an appropriate algorithm then interpolates the function values between the basic values.

In order to develop the 3-D interpolation algorithm, a simplified 2-D version is first discussed based on a table with x - and y -axis and is then extended to 3-D. For the sake of clarity, the input values to the underlying 2-D function $f(x, y)$ are confined to $0 \leq x \leq 1$ and $0 \leq y \leq 1$ with four surrounding basic values $f(0, 0)$, $f(0, 1)$, $f(1, 0)$, and $f(1, 1)$, obtained from the 2-D table. The interpolated function values at $x = 0$ and $x = 1$ are calculated using linear expressions,

$$\begin{aligned} f_i(0, y) &= f(0, 0) + [f(0, 1) - f(0, 0)] \cdot y, \\ f_i(1, y) &= f(1, 0) + [f(1, 1) - f(1, 0)] \cdot y. \end{aligned}$$

The obtained values $f_i(0, y)$ and $f_i(1, y)$ are then used to calculate the interpolated function value $f_i(x, y)$,

$$f_i(x, y) = f_i(0, y) + [f_i(1, y) - f_i(0, y)] \cdot x. \quad (\text{E.1})$$

This method is extended to a 3-D function $f(x, y, z)$ with $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$ and 8 surrounding table values $f(0, 0, 0) \dots f(1, 1, 1)$ in a straight forward manner:

$$\begin{aligned} f_i(0, 0, z) &= f(0, 0, 0) + [f(0, 0, 1) - f(0, 0, 0)] \cdot z, \\ f_i(0, 1, z) &= f(0, 1, 0) + [f(0, 1, 1) - f(0, 1, 0)] \cdot z, \\ f_i(1, 0, z) &= f(1, 0, 0) + [f(1, 0, 1) - f(1, 0, 0)] \cdot z, \\ f_i(1, 1, z) &= f(1, 1, 0) + [f(1, 1, 1) - f(1, 1, 0)] \cdot z, \\ \\ f_i(0, y, z) &= f_i(0, 0, z) + [f_i(0, 1, z) - f_i(0, 0, z)] \cdot y, \\ f_i(1, y, z) &= f_i(1, 0, z) + [f_i(1, 1, z) - f_i(1, 0, z)] \cdot y, \\ \\ f_i(x, y, z) &= f_i(0, y, z) + [f_i(1, y, z) - f_i(0, y, z)] \cdot x. \end{aligned} \quad (\text{E.2})$$

The calculation of $f_i(x, y, z)$ requires a total of 7 multiplications and 14 additions or subtractions.

The current implementation uses 16 basic values $V_{1,k}$ and $V_{2,l}$,

$$V_{1,k} = V_{1,\min} + k \frac{V_{1,\max} - V_{1,\min}}{15}, \quad k \in \mathbb{N}_0 \wedge 0 \leq k \leq 15, \quad (\text{E.3})$$

$$V_{2,l} = V_{2,\min} + l \frac{V_{2,\max} - V_{2,\min}}{15}, \quad l \in \mathbb{N}_0 \wedge 0 \leq l \leq 15, \quad (\text{E.4})$$

and 32 values $P_{\text{out},m}$:

$$P_{\text{out},m} = -P_{\text{out,max}} + m \frac{2P_{\text{out,max}}}{31}, \quad m \in \mathbb{N}_0 \wedge 0 \leq m \leq 31. \quad (\text{E.5})$$

In total, the tables for D_1 , D_2 , and φ require $3 \cdot 16^2 \cdot 32 = 24576$ memory cells; this fits into the on-chip FLASH of the TMS320F2808.

Depending on the operating point, the actual converter output power may deviate from the set output power by reason of the linear interpolation. The maximum output power errors occur approximately in the middle between 8 adjacent basic values, i.e.

$$V_{1,e,k} = \frac{V_{1,k} + V_{1,k+1}}{2}, \quad k \in \mathbb{N}_0 \wedge 0 \leq k < 15, \quad (\text{E.6})$$

$$V_{2,e,l} = \frac{V_{2,l} + V_{2,l+1}}{2}, \quad l \in \mathbb{N}_0 \wedge 0 \leq l < 15, \quad \text{and} \quad (\text{E.7})$$

$$P_{\text{out},e,m} = \frac{P_{\text{out},e,m} + P_{\text{out},e,m+1}}{2}, \quad m \in \mathbb{N}_0 \wedge 0 \leq m < 31, \quad (\text{E.8})$$

is considered in order to calculate the absolute and relative errors:

$$e_{\text{P}}(V_{1,e,k}, V_{2,e,l}, P_{\text{out},e,m}) = P_{\text{out}} - P_{\text{out},i}(V_{1,e,k}, V_{2,e,l}, P_{\text{out},e,m}), \quad (\text{E.9})$$

$$e_{\text{P,r}}(V_{1,e,k}, V_{2,e,l}, P_{\text{out},e,m}) = \frac{e_{\text{P}}(V_{1,e,k}, V_{2,e,l}, P_{\text{out},e,m})}{P_{\text{out}}} \quad (\text{E.10})$$

($P_{\text{out},i}$ denotes the output power calculated with the interpolated duty cycles and the interpolated phase shift angle). Table E.1 summarizes the errors calculated for the different modulation schemes. The maximum absolute error of 107 W occurs for phase shift modulation; with the extended triangular and trapezoidal current mode modulation, a maximum relative error of 15% occurs. In order to eliminate the error due to the linear interpolation, the current controller discussed in Section 6.3 is required.

E.3 Flexible Gate Signal Generation Unit

The voltage sequences required for the different modulation schemes demand for a highly flexible gate signal generation unit. The gate signal generation is therefore performed with finite state machines (FSMs) being executed in the FPGA; this approach allows for very high flexibility regarding the generation of different gate signal pulse patterns.

The gate signal generation unit consists of 6 different state machines: the master FSM (Figure E.1) and its supporting subsidiary FSM (Figure E.2) control 4 subordinate FSMs which in turn generate the gate signals (Figure E.3). Let us assume, that the state “POS1” of the master FSM becomes active with the configured direction of power transfer being “HV→LV”.

Phase shift modulation:			
$\max e_P $	$\overline{ e_P }$	$\max e_{P,r} $	$\overline{ e_{P,r} }$
107 W	4.7 W	5.7%	0.32%
Extended triangular and trapezoidal current mode modulation:			
51 W	4.7 W	15%	0.77%
Suboptimal modulation scheme:			
58 W	6.2 W	6.0%	0.83%

Table E.1: Output power error by reason of the linear interpolation: $\overline{|e_P|}$ and $\overline{|e_{P,r}|}$ denote the average absolute and relative errors. The error values are calculated according to (E.9) and (E.10), whereas the calculation of the relative error excludes zero output power.

The FPGA thus resets the half-cycle counter (required in order to detect the end of the half-cycle), updates the FSM timing parameters, and generates an external DSP interrupt to synchronize the DSP controllers to the FPGA. It further sets the switch signal events $S_{1,2}$ to 1 which triggers the half bridge FSM assigned to T_1 and T_2 (Figure E.3 with $i = 1$ and $j = 2$). At the time the half-cycle counter reaches T_1 , the master FSM state changes to “POS2”, triggers the half bridge FSM assigned to T_5 and T_6 , and resets an independent counter used to control the subsidiary FSM. In order to avoid an erroneous switching sequence, a flag indicating the current half-cycle, `HC1_active_flag`, is set (Figure E.1). As soon as the half-cycle counter reaches T_2 , the half bridge FSM assigned to T_3 and T_4 is triggered. The master state machine starts with the second half-cycle, as soon as the half-cycle counter elapses.

The use of the independent subsidiary state machine enables the time between the events $S_{5,6}$ and $S_{7,8}$ (which is equivalent to the duration D_2/f_S) to range from 0 to $T_S/2$ —on the assumption of a power transfer direction from the HV port to the LV port. With the extension to both power transfer directions, as shown in Figures E.1 and E.2, the proposed architecture allows to reproduce all required voltage sequences discussed in Chapters 3 and 5.

The use of independent FSMs for each half bridge finally allows the switching events $S_{i,j}$ to be delayed individually in order to compensate for the switching time delays discussed in Sections 4.3.2 and 4.3.3.

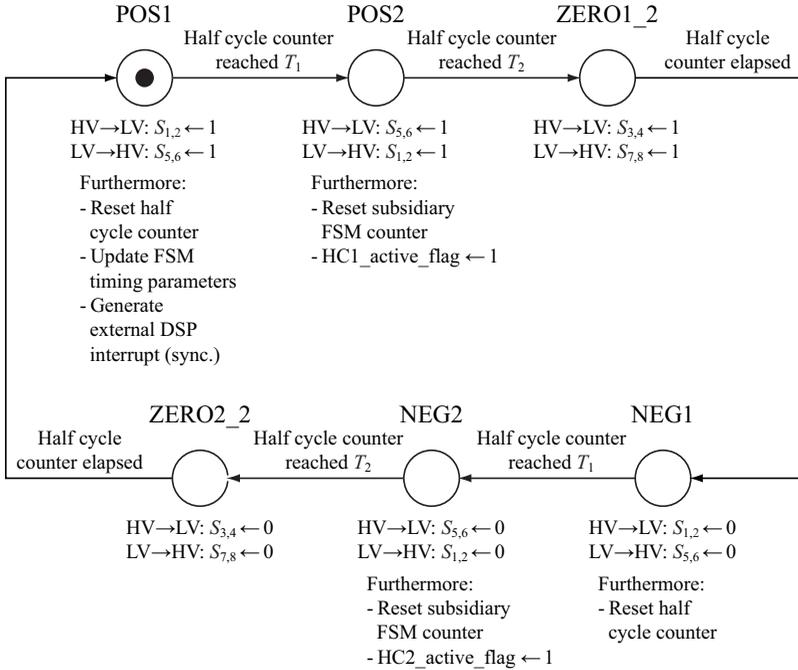


Figure E.1: Master state machine: employed for the DAB to control 3 out of 4 half bridge state machines (cf. Figure E.3). The 4th half bridge is controlled with the additional state machine depicted in Figure E.2, since those particular switching commands may occur after the half-cycle has elapsed (cf. Figure 4.29 and Figure 5.29). It is important to note, that the assignments related to each state are only performed at the instant when the FSM enters the respective state.

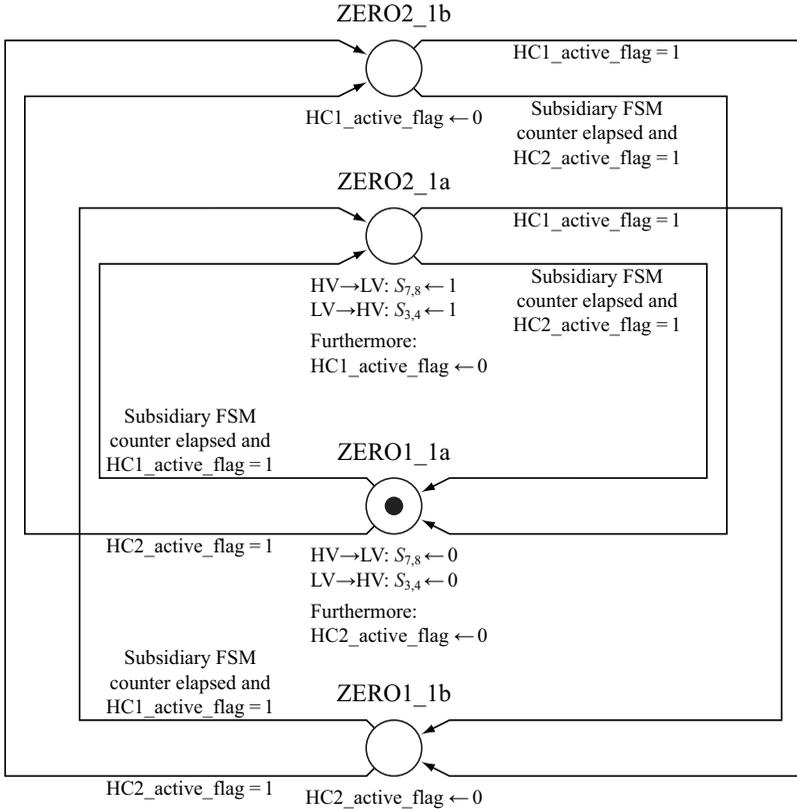


Figure E.2: Subsidiary part of the master state machine depicted in Figure E.1; controls the state machine of the 4th half bridge ($HV \rightarrow LV$: T_7, T_8 ; $LV \rightarrow HV$: T_3, T_4). This additional state machine is required, since the switching action of the 4th half bridge may occur after the half-cycle in the master state machine has elapsed. Therefore, the control of the 4th half bridge needs to be decoupled from the master state machine (cf. Figure 4.29 and Figure 5.29). The state machine uses the variables $HC1_active_flag$ and $HC2_active_flag$ to prevent failure modes during unsteady converter operation. It is important to note, that the assignments related to each state are only performed at the instant when the FSM enters the respective state.

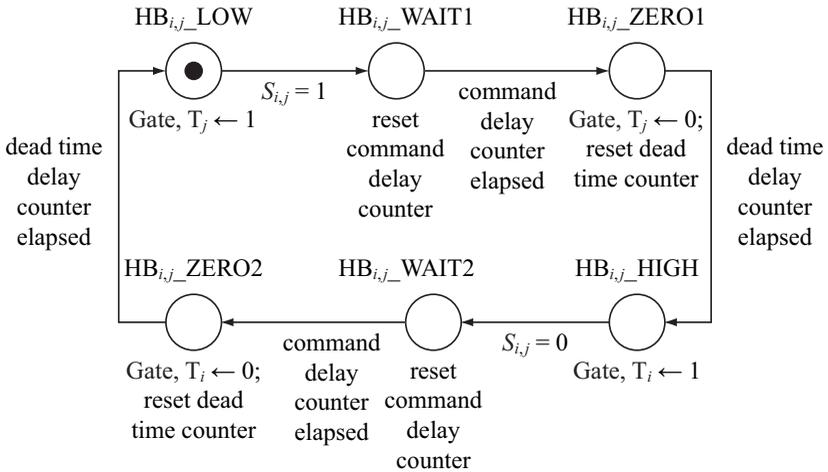


Figure E.3: State machine $HB_{i,j}$ employed to generate the gate signals of a single half bridge (inclusive command delay and dead time interval generation). The indices i and j denote the indices of the MOSFET’s reference designators given in the respective circuit diagrams (e.g. Figure 2.10 for the DAB). In case of the DAB, the FPGA runs four of these state machines, i.e. $HB_{1,2}$, $HB_{3,4}$, $HB_{5,6}$, and $HB_{7,8}$, simultaneously. It is important to note, that the assignments related to each state are only performed at the instant when the FSM enters the respective state.

Appendix F

Supplement to the Small-Signal Model of the DAB

F.1 Small-Signal Model

F.1.1 Matrix Expressions (from [120])

The state space matrix \mathbf{A} for phase shift modulation (6.10) contains the derivatives of all system state variables at the end of the half-cycle, $\vec{x}(t = T_{\text{DAB}})$, with respect to the state variables at the beginning of the half-cycle, $\vec{x}(t = 0)$,

$$\mathbf{A} = \lim_{t \rightarrow T_{\text{DAB}}} \begin{bmatrix} \frac{\partial i_L}{\partial i_{L,0}} & \frac{\partial i_L}{\partial i_{f1a,0}} & \frac{\partial i_L}{\partial i_{f1b,0}} & \frac{\partial i_L}{\partial (i_{f2a,0}/n)} & \frac{\partial i_L}{\partial (i_{f2b,0}/n)} & \frac{\partial i_L}{\partial v_{f1,0}} & \frac{\partial i_L}{\partial (nv_{f2,0})} \\ \frac{\partial i_{f1a}}{\partial i_{L,0}} & \frac{\partial i_{f1a}}{\partial i_{f1a,0}} & \frac{\partial i_{f1a}}{\partial i_{f1b,0}} & \frac{\partial i_{f1a}}{\partial (i_{f2a,0}/n)} & \frac{\partial i_{f1a}}{\partial (i_{f2b,0}/n)} & \frac{\partial i_{f1a}}{\partial v_{f1,0}} & \frac{\partial i_{f1a}}{\partial (nv_{f2,0})} \\ \frac{\partial i_{f1b}}{\partial i_{L,0}} & \frac{\partial i_{f1b}}{\partial i_{f1a,0}} & \frac{\partial i_{f1b}}{\partial i_{f1b,0}} & \frac{\partial i_{f1b}}{\partial (i_{f2a,0}/n)} & \frac{\partial i_{f1b}}{\partial (i_{f2b,0}/n)} & \frac{\partial i_{f1b}}{\partial v_{f1,0}} & \frac{\partial i_{f1b}}{\partial (nv_{f2,0})} \\ \frac{\partial (i_{f2a}/n)}{\partial i_{L,0}} & \frac{\partial (i_{f2a}/n)}{\partial i_{f1a,0}} & \frac{\partial (i_{f2a}/n)}{\partial i_{f1b,0}} & \frac{\partial (i_{f2a}/n)}{\partial (i_{f2a,0}/n)} & \frac{\partial (i_{f2a}/n)}{\partial (i_{f2b,0}/n)} & \frac{\partial (i_{f2a}/n)}{\partial v_{f1,0}} & \frac{\partial (i_{f2a}/n)}{\partial (nv_{f2,0})} \\ \frac{\partial (i_{f2b}/n)}{\partial i_{L,0}} & \frac{\partial (i_{f2b}/n)}{\partial i_{f1a,0}} & \frac{\partial (i_{f2b}/n)}{\partial i_{f1b,0}} & \frac{\partial (i_{f2b}/n)}{\partial (i_{f2a,0}/n)} & \frac{\partial (i_{f2b}/n)}{\partial (i_{f2b,0}/n)} & \frac{\partial (i_{f2b}/n)}{\partial v_{f1,0}} & \frac{\partial (i_{f2b}/n)}{\partial (nv_{f2,0})} \\ \frac{\partial v_{f1}}{\partial i_{L,0}} & \frac{\partial v_{f1}}{\partial i_{f1a,0}} & \frac{\partial v_{f1}}{\partial i_{f1b,0}} & \frac{\partial v_{f1}}{\partial (i_{f2a,0}/n)} & \frac{\partial v_{f1}}{\partial (i_{f2b,0}/n)} & \frac{\partial v_{f1}}{\partial v_{f1,0}} & \frac{\partial v_{f1}}{\partial (nv_{f2,0})} \\ \frac{\partial (nv_{f2})}{\partial i_{L,0}} & \frac{\partial (nv_{f2})}{\partial i_{f1a,0}} & \frac{\partial (nv_{f2})}{\partial i_{f1b,0}} & \frac{\partial (nv_{f2})}{\partial (i_{f2a,0}/n)} & \frac{\partial (nv_{f2})}{\partial (i_{f2b,0}/n)} & \frac{\partial (nv_{f2})}{\partial v_{f1,0}} & \frac{\partial (nv_{f2})}{\partial (nv_{f2,0})} \end{bmatrix}, \quad (\text{F.1})$$

and is evaluated at the steady-state operating point $\vec{x}_{\text{st}}(0)$. \mathbf{B}_{PS} and \mathbf{C} contain the derivatives of $\vec{x}(t = T_{\text{DAB}})$ with respect to the input variables,

$$\mathbf{B}_{\text{PS}} = \lim_{t \rightarrow T_{\text{DAB}}} \begin{bmatrix} \frac{\partial i_L}{\partial T_{\varphi,0}} \\ \frac{\partial i_{f1a}}{\partial T_{\varphi,0}} \\ \frac{\partial i_{f1b}}{\partial T_{\varphi,0}} \\ \frac{\partial(i_{f2a}/n)}{\partial T_{\varphi,0}} \\ \frac{\partial(i_{f2b}/n)}{\partial T_{\varphi,0}} \\ \frac{\partial v_{f1}}{\partial T_{\varphi,0}} \\ \frac{\partial(nv_{f2})}{\partial T_{\varphi,0}} \end{bmatrix} \quad \text{and} \quad \mathbf{C} = \lim_{t \rightarrow T_{\text{DAB}}} \begin{bmatrix} \frac{\partial i_L}{\partial V_{1,0}} & \frac{\partial i_L}{\partial(nV_{2,0})} \\ \frac{\partial i_{f1a}}{\partial V_{1,0}} & \frac{\partial i_{f1a}}{\partial(nV_{2,0})} \\ \frac{\partial i_{f1b}}{\partial V_{1,0}} & \frac{\partial i_{f1b}}{\partial(nV_{2,0})} \\ \frac{\partial(i_{f2a}/n)}{\partial V_{1,0}} & \frac{\partial(i_{f2a}/n)}{\partial(nV_{2,0})} \\ \frac{\partial(i_{f2b}/n)}{\partial V_{1,0}} & \frac{\partial(i_{f2b}/n)}{\partial(nV_{2,0})} \\ \frac{\partial v_{f1}}{\partial V_{1,0}} & \frac{\partial v_{f1}}{\partial(nV_{2,0})} \\ \frac{\partial(nv_{f2})}{\partial V_{1,0}} & \frac{\partial(nv_{f2})}{\partial(nV_{2,0})} \end{bmatrix}. \quad (\text{F.2})$$

For the alternative modulation (6.17), \mathbf{A} and \mathbf{C} are again derived according to (F.1) and (F.2), only \mathbf{B}_{PS} changes to \mathbf{B}_{alt} ,

$$\mathbf{B}_{\text{alt}} = \lim_{t \rightarrow T_{\text{DAB}}} \begin{bmatrix} \frac{\partial i_L}{\partial T_{1,0}} & \frac{\partial i_L}{\partial T_{2,0}} & \frac{\partial i_L}{\partial T_{3,0}} \\ \frac{\partial i_{f1a}}{\partial T_{1,0}} & \frac{\partial i_{f1a}}{\partial T_{2,0}} & \frac{\partial i_{f1a}}{\partial T_{3,0}} \\ \frac{\partial i_{f1b}}{\partial T_{1,0}} & \frac{\partial i_{f1b}}{\partial T_{2,0}} & \frac{\partial i_{f1b}}{\partial T_{3,0}} \\ \frac{\partial(i_{f2a}/n)}{\partial T_{1,0}} & \frac{\partial(i_{f2a}/n)}{\partial T_{2,0}} & \frac{\partial(i_{f2a}/n)}{\partial T_{3,0}} \\ \frac{\partial(i_{f2b}/n)}{\partial T_{1,0}} & \frac{\partial(i_{f2b}/n)}{\partial T_{2,0}} & \frac{\partial(i_{f2b}/n)}{\partial T_{3,0}} \\ \frac{\partial v_{f1}}{\partial T_{1,0}} & \frac{\partial v_{f1}}{\partial T_{2,0}} & \frac{\partial v_{f1}}{\partial T_{3,0}} \\ \frac{\partial(nv_{f2})}{\partial T_{1,0}} & \frac{\partial(nv_{f2})}{\partial T_{2,0}} & \frac{\partial(nv_{f2})}{\partial T_{3,0}} \end{bmatrix}. \quad (\text{F.3})$$

\mathbf{B}_{PS} , \mathbf{B}_{alt} , and \mathbf{C} are again evaluated at the steady-state operating point $\vec{x}_{\text{st}}(0)$.

F.1.2 Small-Signal Transfer Function

The z-domain control to output transfer function is derived with equations (71) and (74) in [120],

$$\mathbf{G} = \mathbf{E}^T \cdot [z_{\text{DAB}}\mathbf{I} - \mathbf{Q}(k)\mathbf{R}\mathbf{P}(k)\mathbf{A}\mathbf{P}(k)\mathbf{Q}(k)]^{-1} \cdot \mathbf{Q}(k)\mathbf{R}\mathbf{P}(k)\mathbf{B}_{\text{PS}}, \quad (\text{F.4})$$

with \mathbf{R} being defined in (6.12) in Chapter 6, an integer number k , and

$$\mathbf{P}_{7 \times 7}(k) = \begin{bmatrix} (-1)^k & \mathbf{0}_{1 \times 6} \\ \mathbf{0}_{6 \times 1} & \mathbf{I}_{6 \times 6} \end{bmatrix}, \quad \mathbf{Q}_{7 \times 7}(k) = \begin{bmatrix} (-1)^k \cdot \text{sgn}(i_{L,0}) & \mathbf{0}_{1 \times 6} \\ \mathbf{0}_{6 \times 1} & \mathbf{I}_{6 \times 6} \end{bmatrix}. \quad (\text{F.5})$$

The products $\mathbf{P}(k)\mathbf{Q}(k)$ and $\mathbf{Q}(k)\mathbf{R}\mathbf{P}(k)$ are equal to

$$\begin{aligned} \mathbf{Q}(k)\mathbf{R}\mathbf{P}(k) &= \begin{bmatrix} -\text{sgn}(i_{L,0}) & \mathbf{0} \\ \mathbf{0} & \mathbf{I} \end{bmatrix} = \mathbf{Q}(0)\mathbf{R}, \\ \mathbf{P}(k)\mathbf{Q}(k) &= \begin{bmatrix} \text{sgn}(i_{L,0}) & \mathbf{0} \\ \mathbf{0} & \mathbf{I} \end{bmatrix} = \mathbf{Q}(0) \text{ for } k \in \mathbb{Z}, \end{aligned} \tag{F.6}$$

and thus independent on k which allows for the simplified representation (6.11), (6.12).

F.2 Sampling Rate Reduction

For a given discrete time system with sampling rate T , step response function $h(kT)$, $k \in \mathbb{N}_0$, and corresponding z -domain transfer function $G(z)$, the transfer function $G_r(z)$ with increased sampling time $T_r = N \cdot T$, $N \in \mathbb{N}$ and similar step response function $h_r(kT_r) = h(kNT)$, is derived.

The original z -domain transfer function

$$G(z) = \frac{a(z)}{b(z)} \tag{F.7}$$

contains two polynomials $a(z)$ and $b(z)$ with constant and real coefficients and $\deg[a(z)] < \deg[b(z)]$.

Based on the relation between the i -th pole $p_{s,i}$ of a continuous time transfer function and the i -th pole $p_{z,i}$ of the corresponding discrete time transfer function [151],

$$p_{z,i} = e^{p_{s,i}T}, \tag{F.8}$$

the i -th pole $p_{rz,i}$ of $G_r(z)$ can be expressed as

$$p_{rz,i} = e^{p_{s,i}T_r} = e^{p_{s,i}NT} = p_{z,i}^N. \tag{F.9}$$

The method discussed in [151] then represents a simple way to obtain the numerator $a_r(z)$ of $G_r(z)$ based on the step response $h_r(kT_r)$ of the corresponding time domain function which is equal to the step response of the already known function $h(kNT)$ for $k_N = N \cdot k$ (this can be achieved with the Matlab command `d2d` as well).

F.3 Derivation of G_{DAB}

For the sake of clarity, the derivation of G_{DAB} is based on a simplified single-input, single-output system with input X_{in} and output Y_{out} in **Figure F.1**.

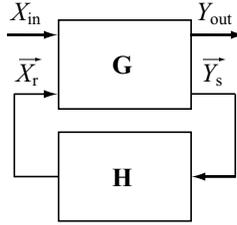


Figure F.1: Single-input, single-output system with internal feedback used to derive G_{DAB} .

It contains the multiple-input, multiple-output transfer function $\mathbf{G}(z)$ in the forward path and $\mathbf{H}(z)$ in the feedback path. Vector \vec{X} denotes the input of $\mathbf{G}(z)$,

$$\vec{X} = \begin{pmatrix} X_{in} & \vec{X}_r^T \end{pmatrix}^T, \quad \vec{X}_r \in \mathbb{C}^n, \quad (\text{F.10})$$

with the system input value X_{in} and internal system values in \vec{X}_r . The output of $\mathbf{G}(z)$,

$$\vec{Y} = \mathbf{G} \cdot \vec{X} = \begin{pmatrix} Y_{out} & \vec{Y}_s^T \end{pmatrix}^T, \quad \vec{Y}_s \in \mathbb{C}^m, \quad (\text{F.11})$$

contains Y_{out} and another set of internal system values \vec{Y}_s that denote the inputs to $\mathbf{H}(z)$. The output of $\mathbf{H}(z)$ is then equal to \vec{X}_r ,

$$\vec{X}_r = \underset{n \times m}{\mathbf{H}} \cdot \vec{Y}_s, \quad (\text{F.12})$$

in order to close the feedback loop. The transfer function matrix \mathbf{G} is split according to

$$\mathbf{G} = \begin{bmatrix} G_{00} & \mathbf{G}_{0r} \\ \mathbf{G}_{s0} & \mathbf{G}_{sr} \end{bmatrix}. \quad (\text{F.13})$$

$1 \times n$
 $m \times 1$ $m \times n$

With (F.10), (F.11), (F.12), and (F.13) the system output value Y_{out} and the vector \vec{Y}_s become

$$Y_{out} = G_{00}X_{in} + \mathbf{G}_{0r}\vec{X}_r = G_{00}X_{in} + \mathbf{G}_{0r}\mathbf{H}\vec{Y}_s \quad (\text{F.14})$$

$$\vec{Y}_s = \mathbf{G}_{s0}X_{in} + \mathbf{G}_{sr}\vec{X}_r = \mathbf{G}_{s0}X_{in} + \mathbf{G}_{sr}\mathbf{H}\vec{Y}_s \quad (\text{F.15})$$

and thus

$$\vec{Y}_s = (\mathbf{I} - \mathbf{G}_{sr}\mathbf{H})^{-1} \mathbf{G}_{s0}X_{in}. \quad (\text{F.16})$$

Based on (F.14) and (F.16) the system transfer function G_{DAB} results:

$$G_{DAB} = Y_{out}/X_{in} = G_{00} + \mathbf{G}_{0r}\mathbf{H}(\mathbf{I} - \mathbf{G}_{sr}\mathbf{H})^{-1} \mathbf{G}_{s0}. \quad (\text{F.17})$$

Glossary

Commonly Used Abbreviations

HV	High Voltage
LV	Low Voltage
HF	High Frequency
ZVS	Zero Voltage Switching
DAB	Dual Active Bridge
SRC	Series Resonant Converter
PRC	Parallel Resonant Converter
SPRC	Series-Parallel Resonant Converter
LLC	Series-Parallel Resonant Converter: the resonant network consists of two inductors (L and L_M) and one capacitor C (cf. Figures 2.17 and 2.18)
LCC	Series-Parallel Resonant Converter: the resonant network consists of one inductor L and two capacitors (C and C_P ; cf. Figures 2.16 and 2.19).

Commonly Used Designators of Physical Properties

<i>Designator</i>	<i>Description</i>
f_S	switching frequency
T_S	switching period, $T_S = 1/f_S$
n	transformer turns ratio
L	series inductance of the DAB and LLC converter inductor

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<i>Designator</i>	<i>Description</i>
C	series capacitance of the LLC converter capacitor
L_M	transformer magnetizing inductance
R	resistor in series to L ; R models the converter conduction losses.
C_{DC1}	HV side DC capacitor
L_{f1a}	main filter inductor, HV side
R_{f1a}	resistor in series to L_{f1a} ; R_{f1a} models the inductor's conduction losses
L_{f1b}	HV side filter inductor, damping circuit
R_{f1b}	HV side filter, damping resistor
C_{f1}	HV side filter capacitor
C_{DC2}	LV side DC capacitor
L_{f2a}	main filter inductor, LV side
R_{f2a}	resistor in series to L_{f2a} ; R_{f2a} models the inductor's conduction losses
L_{f2b}	LV side filter inductor, damping circuit
R_{f2b}	LV side filter, damping resistor
C_{f2}	LV side filter capacitor
V_1	HV port voltage
V_2	LV port voltage
$V_{1,\min}$	minimal HV port voltage (within the specified range)
$V_{1,\max}$	maximal HV port voltage (within the specified range)
$V_{2,\min}$	minimal LV port voltage (within the specified range)
$V_{2,\max}$	maximal LV port voltage (within the specified range)
p_1	instantaneous HV port power (> 0 for power transfer from the HV port to the LV port)
p_2	instantaneous LV port power (> 0 for power transfer from the HV port to the LV port)
v_{AC1}	instantaneous bridge voltage, HV side
v_{AC2}	instantaneous bridge voltage, LV side
v_R	instantaneous voltage applied to the HF networks of the DAB and the LLC converters, $v_R = v_{AC1} - n v_{AC2}$
i_L	instantaneous inductor current, HV side (used by the DAB models without magnetizing inductance)

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<i>Designator</i>	<i>Description</i>
$\tilde{i}_L = -i_L$	negative instantaneous inductor current, HV side (used by the DAB models without magnetizing inductance), used in Section 4.3.3
i_{L1}	instantaneous inductor current, HV side (used by the DAB model with magnetizing inductance)
i_{L2}	instantaneous inductor current, LV side (used by the DAB model with magnetizing inductance)
v_{f1}	instantaneous voltage applied to C_{f1}
v_{f2}	instantaneous voltage applied to C_{f2}
i_{f1}	sum of the instantaneous currents through L_{f1a} and L_{f1b}
i_{f2}	sum of the instantaneous currents through L_{f2a} and L_{f2b}
P_1	average HV port power obtained from the electric DAB model (> 0 for power transfer from the HV port to the LV port)
P_2	average LV port power obtained from the electric DAB model (> 0 for power transfer from the HV port to the LV port)
V_{AC1}	RMS bridge voltage, HV side
V_{AC2}	RMS bridge voltage, LV side
I_L	RMS value of the HV side inductor and transformer current (magnetizing inductance neglected)
I_{L1}	RMS values of the inductor and transformer currents on the HV side (magnetizing inductance considered)
I_{L2}	RMS values of the inductor and transformer currents on the LV side (magnetizing inductance considered)
V_{f1}	RMS value of the DAB filter capacitor voltage, HV side
V_{f2}	RMS value of the DAB filter capacitor voltage, LV side
I_{f1}	RMS value of the DAB filter inductor current, HV side
I_{f2}	RMS value of the DAB filter inductor current, LV side
$P_{\text{prec},1}$	precise HV port power obtained from the accurate DAB loss model (> 0 for power transfer from the HV port to the LV port)
$P_{\text{prec},2}$	precise LV port power obtained from the accurate DAB loss model (> 0 for power transfer from the HV port to the LV port)

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<i>Designator</i>	<i>Description</i>
P_t	total losses ($P_t = P_{\text{prec},1} - P_{\text{prec},2}$)
P_{cond}	total conduction and copper losses
$P_{\text{tr,cond}}$	transformer copper losses
$P_{L_{\text{HV,cond}}}$	inductor copper losses
$P_{1,\text{cond}}$	total conduction losses of the HV side of the converter (including the HV transformer winding)
$P_{2,\text{cond}}$	total conduction losses of the LV side of the converter (including the LV transformer winding)
$P_{S1,\text{cond}}$	conduction losses, all HV switches
$P_{S2,\text{cond}}$	conduction losses, all LV switches
$P_{\text{tr1,cond}}$	conduction losses, HV transformer winding
$P_{\text{tr2,cond}}$	conduction losses, LV transformer winding
$P_{S1,\text{sw}}$	total switching losses, HV side
$P_{S2,\text{sw}}$	total switching losses, LV side
$P_{S1,\text{gate}}$	gate driver losses, HV side
$P_{S2,\text{gate}}$	gate driver losses, LV side
$P_{\text{tr,core}}$	transformer core losses
$P_{1,\text{aux}}$	power demand of the HV side auxiliary power supply
$P_{2,\text{aux}}$	power demand of the LV side auxiliary power supply
$V_{\text{GS},1}$	gate driver voltage, HV side
$V_{\text{GS},2}$	gate driver voltage, LV side
$Q_{\text{G},1}$	gate charge of a single MOSFET, HV side
$Q_{\text{G},2}$	gate charge of a single MOSFET, LV side
v_{DS,T_x}	drain-to-source voltage applied to the switch T_x
R_{S1}	MOSFETs' on-state resistances, HV side
R_{S2}	MOSFETs' on-state resistances, LV side
$R_{L_{\text{HV}}}$	copper resistance of the DAB inductor, HV side
R_{tr1}	copper resistance of the HV side transformer winding
R_{tr2}	copper resistance of the LV side transformer winding
$R_{\text{PCB,a}}$	LV side PCB resistance, HF path
$R_{\text{PCB,b}}$	LV side PCB resistance between LV side full bridge and the (ceramic) DC capacitor

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<i>Designator</i>	<i>Description</i>
$V_{\text{tr,core}}$	transformer core volume
$V_{L_{\text{HV,core}}}$	inductor core volume
i	index counter
\bar{x}	average value of placeholder x
\hat{x}	small-signal value of placeholder x

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