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Ultra-High Efficiency Isolated/Non-Isolated Three-Phase Multi-Level PWM Converters

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presented by

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Nere gurasoentzat,
e per la mia fidanzata.

For my parents,
and my fiancée.

Ikasten ez duena ari da ahazten
Esaera Zaharra

He who is not learning is forgetting
Old Basque Saying

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Mila esker. Thank you.

Abstract

With an increasing need to reduce greenhouse gases on a global scale, new solutions are constantly being developed such that people can continue with their current standard of living, albeit in an environmentally sustainable fashion. However, to lure people into changing their habits and adopting new technologies, these new solutions have to be both technically and economically competitive. Such a challenge occurs for example in houses and buildings, where the standard household consumes the electricity mix provided by the local electric utility, and its members drive an internal combustion engine vehicle. But with recent advancements in technology, it is possible to live in a sustainable house or building that generates electricity from a photovoltaic panel system (e.g., installed on the roof), has a battery storage that balances the electricity demand throughout the day, and has a DC charger in the garage that can recharge electric vehicle batteries. Underpinning all of these technologies, there is a solid state power conversion taking place by means of power electronic systems.

The main goal of this thesis is to explore efficiency boundaries of such power electronic systems, by finding solutions that improve the state-of-the-art performance without compromising the size and weight of the converters. With this aim in mind, multi-level converters that make use of a series-connection of lower-voltage devices, have been identified as a suitable solution. Three are the main advantages of such converters: they offer a multi-level output voltage waveform, they benefit from an interleaving of gate signals that leads to a multiplication of the switching frequency at the output voltage node, and they make use of lower voltage devices which feature better performance than their higher voltage counterparts.

Therefore, the fundamental properties of semiconductor devices in hard-switching bridge-legs are revisited and scaling laws of the on-state resistance and output capacitance of switches are obtained with respect to the blocking voltage. By optimizing conduction and switching losses with respect to the die area, a revised device figure-of-merit is proposed, that can directly quantify the minimal bridge-leg semiconductor losses. In a next step, the same concept is applied to multi-level bridge-legs, where the possibility of defining a novel extended figure-of-merit is seized, a powerful tool that allows to calculate the maximum achievable efficiency of bridge-legs across a different number of levels, power ratings, and switching frequencies. The utility of this extended figure-of-merit is then finally validated with a case study on a 10 kW three-phase photovoltaic inverter, where the performance difference between two- and three-level bridge-leg configurations is evaluated.

In order to perform a comprehensive comparative evaluation of multi-level bridge-legs, in a next step the volume and losses of the passive components are included in the analysis, to assess which topology and number of levels reaches the imposed 99.5 % efficiency target in the most compact realization for a three-phase 10 kW photovoltaic inverter. This analysis yields that a seven-level hybrid active neutral point clamped (HANPC) converter is the best solution.

Therefore, in a next step a seven-level HANPC 10 kW three-phase all-Silicon inverter is realized, featuring a 99.35 % peak efficiency, and a volumetric power density of 3.4 kW/dm^3 (55.9 W/in^3) and a gravimetric power density of 3.2 kW/kg, furthermore also fulfilling CISPR Class A EMI requirements. A Pareto analysis shows that with the next generation Silicon devices the 99.5 % efficiency target can be met, and that with commercially available GaN devices, 99.6 % efficiency could be reached, both within the same volume.

In a further step, a holistic approach is taken to analyze two-stage AC/DC + DC/DC systems, where a novel synergetic control is proposed for a typical EV fast charging architecture that comprises a three-phase Vienna rectifier followed by two series connected isolated DC/DC modules. This synergetic control method allows to have sinusoidal grid currents by only switching one out of the three phases of the front-end converter, thanks to having the DC/DC modules control the DC-link voltage to the maximum line-to-line phase voltage shape. Moreover, the DC/DC modules guarantee an equal splitting of the DC-link voltage to the series connected DC-link capacitors, enabling the use of state-of-the-art 600 V GaN devices. If necessary, the front-end rectifier stage can also be used to boost the DC-link voltage, thus reducing the input-output voltage range of the DC/DC converters. The correct operation of this control strategy, which can readily be retrofitted into existing systems to save over two thirds of the rectifier switch losses, is then verified by means of circuit simulations.

Further considerations concerning semiconductor physics, semiconductor losses, and bridge-leg configurations are given in the Appendix, where it is worth highlighting that a seven-level 2.2 kW flying capacitor inverter prototype with a power density of 15.8 kW/dm^3 and a peak efficiency of 99.03 % is realized to justify that seven-levels are required for ultra-high efficiency three-phase 800 V DC-link voltage systems.

Finally, considering the contributions of this work, a new state-of-the-art efficiency vs. power density boundary is established in the conclusion, and future research directions are identified, particularly for investigations

concerning a further volume reduction of multi-level converters and their application to variable speed drives.

Kurzfassung

Angesichts der zunehmenden Notwendigkeit, Treibhausgase weltweit zu reduzieren, müssen insbesondere für die Energieversorgung und Mobilität neue Konzepte entwickelt werden, welche es der Menschheit erlauben den derzeitigen Lebensstandard auf umweltverträgliche Weise zu halten. Um die Gesellschaft dazu zu bewegen, Gewohnheiten zu ändern und neue Technologien einzuführen, müssen diese sowohl technisch als auch wirtschaftlich wettbewerbsfähig sein. Unter Nutzung des technologischen Fortschritts ist es möglich, erneuerbare Energien zu gewinnen und temporär zu speichern und auf abgasarme Formen der Mobilität zu wechseln. Grundlage all dieser Technologien ist die elektronische Konversion elektrischer Spannungen und Ströme und die elektronische Steuerung elektrischer Leistungsflüsse mittels leistungselektronischer Systeme.

Das Hauptziel dieser Arbeit ist es, die Effizienzgrenzen leistungselektronischer Systeme zu ermitteln und neue Konzepte zu finden, welche die Effizienzen derzeitiger Konverter verbessern ohne die Baugrösse oder das Gewicht zu erhöhen. Durch die Analysen werden Multi-Level-Wandler, welche eine Reihenschaltung von Niederspannungsschaltern verwenden, als geeignete Lösung identifiziert. Multi-Level-Konverter weisen drei Hauptvorteile auf: Sie bieten eine mehrstufige Ausgangsspannungsform, sie profitieren von der Möglichkeit einer zeitlichen Versetzung der Gatesignale der Einzelschalter, die zu einer Multiplikation der Schaltfrequenz am Ausgang eines Brückenzweiges führt, und sie verwenden Schalter mit niedrigem Sperrspannungsbedarf die insgesamt zu geringeren Leit- und Schaltverlusten als Komponenten mit höherer Sperrspannungsfestigkeit führen.

Daher werden in einem ersten Schritt die grundlegenden Eigenschaften von Halbleiterbauelementen in hart schaltenden Brückenzweigen analysiert und die Abhängigkeit des Einschaltwiderstands und der parasitären Ausgangskapazität von der Sperrspannung ermittelt. Auf Basis einer Minimierung der Summe aus Leit- und Schaltverlusten wird eine neue Kennzahl für Zweipunkt-Brückenzweige vorgeschlagen, welche die minimal erreichbaren Halbleiterverluste quantifiziert. In einem nächsten Schritt wird das Konzept auf Flying-Capacitor-Multilevel-Brückenzweige erweitert und eine neue Kennzahl definiert, welche es erlaubt, die maximal erreichbare Effizienz für eine beliebige Anzahl von Leveln, eine definierte Ausgangsleistung und eine gegebene Schaltfrequenz zu berechnen. Die praktische Einsetzbarkeit dieser Gütezahl wird schließlich an einem 10 kW Dreiphasen-Photovoltaik-Wechselrichter validiert, und die Effizienzdifferenz zwischen zwei- und dreistufigen Brückenzweigkonfigurationen bewertet.

Um eine umfassende vergleichende Bewertung von mehrstufigen Brückenzweigen durchzuführen, werden in einem nächsten Schritt das Volumen und die Verluste der passiven Komponenten in die Analyse einbezogen. Dies erlaubt es zu klären, mit welcher Topologie und welcher Anzahl an Spannungsleveln ein Effizienzziel von 99.5 % bei gleichzeitig kompaktester Realierung des oben erwähnten 10 kW PV-Wechselrichters erreicht werden kann. Die Analyse zeigt, dass ein siebenstufiger Hybrid-Wandler (Hybrid Active Neutral Point Clamped-HANPC-Converter) die beste Lösung darstellt.

Daher wird in einem nächsten Schritt ein dreistufiger HANPC 10 kW Dreiphasen-Wechselrichter mit Silizium-Leistungs-MOSFETs, einem Spitzenwirkungsgrad von 99.35 %, einer volumetrischen Leistungsdichte von 3.4 kW/dm^3 (55.9 W/in^3) und einer gravimetrischen Leistungsdichte von 3.2 kW/kg realisiert, welcher auch die EMI-Anforderungen gemäss CISPR 11, Klasse A, erfüllt. Eine Pareto-Analyse zeigt, dass unter Beibehaltung des Konverterbauvolumens mit Siliziumschaltern der nächsten Generation das Effizienzziel von 99.5 % erreicht werden kann und dass mit neuesten GaN-Leistungshalbleiterelementen ein Wirkungsgrad von 99.6 % möglich ist.

In einem weiteren Schritt wird ein neuer synergetischer Ansatz zur Regelung dreiphasiger Gleichrichterstufen mit nachgeschaltetem potentialgetrenntem DC/DC-Konverter vorgeschlagen, welcher z.B. in Schnellladestationen für Elektroautos Einsatz finden kann. Der Gleichrichterteil wird dabei als Vienna Rectifier realisiert und der DC/DC-Konverter in zwei Module, jeweils an einer der beiden Ausgangsspannungshälften liegend, aufgespalten. Die synergetische Regelung ermöglicht es, sinusförmige Netzströme zu erreichen, indem nur jeweils eine der drei Phasen der Gleichrichterstufe hochfrequent getaktet wird. Dabei regeln die DC/DC-Module die Zwischenkreisspannung derart, dass auch in den beiden nicht getakteten Phasen eine sinusförmige Stromaufnahme resultiert. Darüber hinaus garantieren die DC/DC-Module eine gleiche Aufteilung der Zwischenkreisspannung auf die in Reihe geschalteten Zwischenkreiskondensatoren und ermöglichen somit den Einsatz modernster 600 V GaN-Bauelemente trotz 800 V Zwischenkreisspannung. Bei Bedarf kann die Gleichrichterstufe auch zur Erhöhung der Zwischenkreisspannung verwendet werden, wodurch der Eingangsspannungsbereich der DC/DC-Wandler verringert wird bzw. bei gegebenem Spannungsübersetzungbereich ein höherer Ausgangsspannungsbereich realisiert werden kann. Der korrekte Betrieb der Regelstrategie, die in bestehenden Systemen problemlos nachgerüstet werden kann und mit der mehr als zwei Drittel der Schalterverluste der Gleichrichterstufe eingespart werden können, wird abschliessend mittels Schaltungssimulation überprüft.

Weitere Überlegungen zu den parasitären Eigenschaften elektronischer Leistungsschalter, zu Mehr-Level-Brückenzweigen und zur Effizienzmessung sind in Anhängen aufgeführt. Hervorzuheben ist hier ein 2.2 kW Demonstrator eines Sieben-Level-Brückenzweiges mit einer Leistungsdichte von 15.8 kW/dm³ und einem maximalen Wirkungsgrad von 99.03 %, der bestätigt, dass für 800 V DC-Zwischenkreisspannung und Wirkungsgrade von 99+ % mindestens sieben Level erforderlich sind.

In Zusammenfassung der Beiträge der Arbeit wird abschliessend unter Berücksichtigung des neuesten Standes der Technik der in Abhängigkeit der Leistungsdichte maximal erreichbare Wirkungsgrad ermittelt. Weiters werden zukünftige Forschungsrichtungen identifiziert, insbesondere hinsichtlich einer weiteren Volumenreduzierung durch Mehrpunkt-Wandler und deren Anwendung für Frequenzumrichter drehzahlvariabler Antriebe.

Abbreviations

1D	One-Dimensional
2D	Two-Dimensional
3D	Three-Dimensional
3-Φ	Three-Phase
AC	Alternating Current
ANPC	Active Neutral Point Clamped
CAD	Computer Aided Design
CI	Coupled Inductor
CM	Common-Mode
CCM	Continuous Conduction Mode
CSPI	Cooling System Performance Index
DC	Direct Current
DM	Differential-Mode
DPT	Double Pulse Test
DUT	Device-Under-Test
EMI	Electromagnetic Interference
EV	Electric Vehicle
FET	Field-Effect Transistor
FC	Flying Capacitor
FCC	Flying Capacitor Converter
FOM	Figure of Merit
GaN	Gallium Nitride
HANPC	Hybrid Active Neutral Point Clamped
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
ICEV	Internal Combustion Engine Vehicle
IGBT	Insulated Gate Bipolar Transistor
LCOE	Levelized Cost of Energy
ML	Multi-Level
MLCC	Multi-Layer Ceramic Capacitor
MOSFET	Metal-Oxide-Semiconductor FET
MPPT	Maximum Power Point Tracker
PCB	Printed Circuit Board
PFC	Power Factor Correction
PV	Photovoltaic
PWM	Pulse-Width Modulation
Q2L	Quasi-2-Level

RMS	Root-Mean-Square
SJ	Super-Junction
Si	Silicon
SiC	Silicon Carbide
TCM	Triangular Current Mode
TCO	Total Cost of Ownership
VR	Vienna Rectifier
VSD	Variable-Speed Drive
WBG	Wide-Bandgap
xL	x-Level (with $x \in 2,3,4\ldots$)
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Contents

1 Introduction

It is beyond reasonable doubt that human activities have caused around 1 ℃ of global warming since preindustrial times [1]. The Intergovernmental Panel on Climate Change (IPCC), the United Nations (UN) body that is responsible for the science behind climate change, estimated in 2018 that global warming will reach 1.5 ℃ between 2030 and 2052, provided the current temperature growth rate. However, with data taken from [1], it is reported in [2] that in the "business-as-usual" scenario, the temperature growth by 2050 will be above 2 ℃, and that in order to limit this growth to 1.5 ℃, the global greenhouse gas (GHG) emissions have to be reduced by more than two-thirds. A clear path forward, hence, is to either reduce the energy demand, or, if an energy demand reduction is not possible, to at least make use of renewable energy sources (as indicated in the Seventh Sustainable Development Goal of the UN [3]).

Two key technologies that help limit the greenhouse gas emissions without jeopardizing socioeconomic development and human well-being are:

(a) Photovoltaic Energy

Taking Germany's 2019 data as example, photovoltaic (PV) energy covered 8.2% of gross electricity demand, providing temporarily on sunny days over 50% of the electric power supply [4]. PV installations feature an energy pay back time of between 1 and 1.5 years, depending mainly on the latitude (or, more precisely, the irradiation intensity) of the location at which a system is installed, which over a lifespan of 20-25 years, means it produces ≈20 times the energy that was needed to manufacture the PV installation [5]. With a rapidly growing market, averaging 35% cumulative PV installation year-on-year growth between 2010 and 2019 [5], and with the fastest decreasing levelized cost of

energy (LCOE) among renewable energies (-77% cost reduction from 2010 until 2018, compared to the second best performer, onshore wind energy, which reduced its LCOE by 35%), it has in 2020 reached the same price per energy unit ($/kWh) than on-shore wind energy, already making both cheaper than the most cost effective fossil fuels [6, 7] (although for a comprehensive comparison, the costs of a temporary energy storage would also have to be considered). In such a competitive electricity supply market, one of the main challenges is to further reduce the LCOE [8], for which both a reduction of initial cost and an increase in system efficiency are required [9], specially also considering that temporary storage (e.g., a battery pack) has to be provided for covering the fluctuation in the PV supply.

(b) Electric Vehicles

Heavily fostered by increasing government regulation aiming to limit the GHG emissions of internal combustion engine vehicles (ICEV), together with ambitious transport electrification goals and public subsidies, EV sales have grown fivefold since 2015, accounting in 2019 for 2.5 % of total new private vehicle sales worldwide [10, 11]. In Europe, moreover, in 2019 7.5 % of newly sold vehicles were EVs, featuring a year-on-year growth of 44 %, rendering it the fastest growing EV market worldwide. However, EVs still account for only 1 % of the global car stock in 2019 [11], as there are many challenges to overcome. From a user perspective, customers fear "range anxiety" and lack of charging stations [10], and from a technical standpoint, the two largest challenges relate to batteries (such as lifetime degradation, energy density and charge rate limitations, etc.), and charging infrastructure (initial cost, charging station size, standardization, grid integration, etc.) [12, 13].

A combination of PV energy and EVs is analyzed in [15], where a case study shows the equivalent GHG emissions of both an ICEV and an EV over driven distance (cf., **Fig. 1.1**). Assuming an EV with a battery pack of 35 kWh, in the range of e.g., a BMW i3, and a mixed mileage between city and countryside, the break-even point for a business-as-usual energy mix would be at around 60,000 km, whereas if the energy would be purely coming from a PV source, the break-even distance would be below 40,000 km. Including the equivalent GHG emission of the PV manufacturing, installation and maintenance, it can be seen that over a 200,000 km driven lifetime with an EV of such characteristics, the equivalent CO_2 emissions can be reduced by 57 %. With this reduction in carbon footprint, the two-thirds GHG reduction

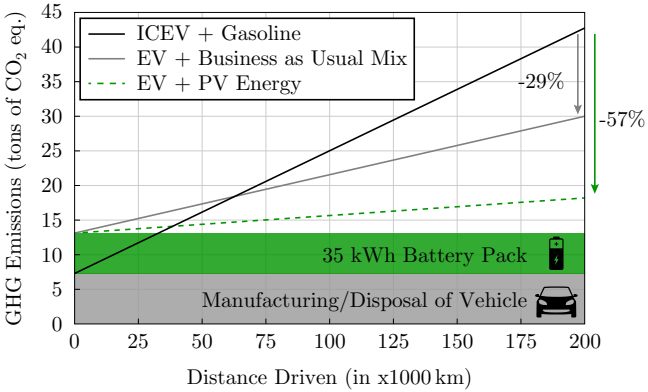

Fig. 1.1: Greenhouse gas emissions in CO_2 equivalent of a gasoline powered ICE vehicle and an EV. The assumed consumption data for the gasoline powered vehicle is 5.9 l/100 km, and for the EV is 16 kWh/100 km. Electricity mix is taken from [14], and the figure is reproduced from [15].

requirement predicted in [2] to limit the average global temperature rise by 2050 to 1.5 ℃ is nearly reached, accepting that the calculations are already within the prognosis error margin.

Frameworks which offer such a combined solution have recently been made commercially available, enabled by visionary companies such as *Tesla, Inc.*, that already offer turnkey solutions that integrate PV + EV, and optionally, even batteries, for use at e.g., households and offices. The architecture of such a system is shown in **Fig. 1.2**, with an exemplary component selection presented in **Table 1.1**. Such systems inevitably require several power electronics conversion interfaces for which, although solutions already exist, there is still a large margin of improvement. Thankfully, the power electronics research field is very active and new solutions that continuously improve the state-of-the-art are being proposed. It is in this context, therefore, that this thesis aims to contribute by proposing novel concepts and bringing the field forward in several key aspects and overcoming challenges concerning these power electronics conversion stages.

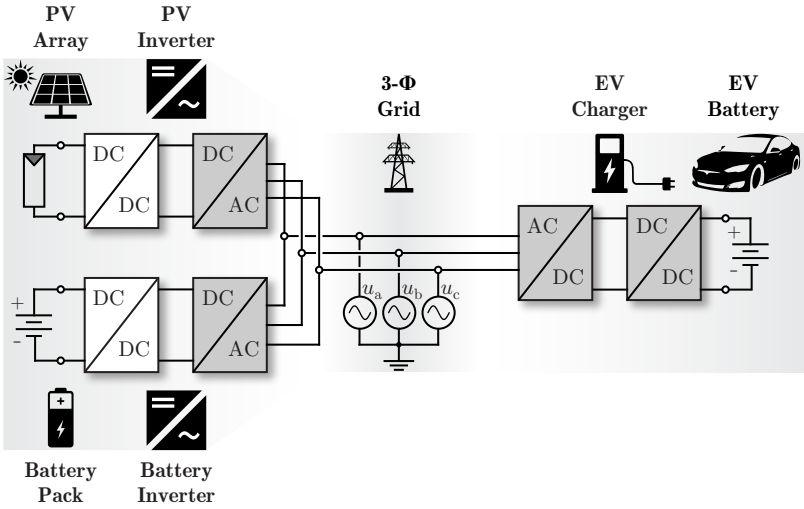

Fig. 1.2: Integrated PV + EV solutions that can be used for, e.g., households, where the energy generated by the PV installation can charge the EV, be fed into the grid, or, optionally, charge a battery pack for later use. Although an AC-connected system is shown here, a DC-connected system would also be possible and would allow to reduce the number of conversion stages. Note, that the conversion stages shaded in grey are the main focus of this thesis.

Tab. 1.1: Example selection of key components for e.g., households, according to a power system architecture as shown in **Fig. 1.2**. Data taken from [16].

Object	Model	Power	Energy Stor.	Approx. Price
PV Panels	Tesla Solar Roof	10 kW	-	≈ 31,100…43,500 $
EV	Tesla Model 3	211-340 kW	54…75 kWh	≈ 37,900…54,900 $
Battery Pack	Tesla Powerwall	5 kW 7 kW_{pk}	13.5 kWh	≈ 9,000 $

1.1 Challenges

In order to make the solution of **Fig. 1.2** accessible to a wider range of the average population, it is clear that the total cost of ownership (TCO), which includes the purchase price plus the operation cost, has to reduce (**Table 1.1** shows that a rough initial investment of ≈100,000 $ is required for the integral solution). The power electronics field can tackle this issue by addressing several challenges, two out of which are the main focus of this thesis:

- **Ultra-High Efficiency**

  Achieving ultra-high efficiency is advantageous from many perspectives. Firstly, by outputting more power for a given input power, higher efficiency systems reduce the operation cost, which if optimized from a total cost of ownership point of view, can lead to systems above 99 % efficiency being the best solution (for instance, [9] shows how for a 8 kW three-phase data center rectifier, for a lifetime of 15 years 99.2 % efficient converters would be cost optimal). Secondly, for EV fast chargers increasing efficiency can reduce charging times, which is one of the largest present-day challenges [12]. Finally, ultra-high-efficiency designs allow to reduce the cooling effort, to such an extent, that as shown in this work, it can even be omitted. This, besides a reduction in volume, weight, and potentially cost, increases also the reliability of converters, by avoiding any mechanically moving parts.

- **Low-Volume Realization**

  Besides the more obvious advantage of compact realization, volume can be taken as a de facto substitute for cost. Acknowledging that publicly available component pricing is not representative of large-scale purchases, it is difficult for academic researchers to perform a cost optimization which corresponds to a meaningful representation of the industry and/or field. Hence, a volume optimization, which is perfectly tangible and quantifiable, serves as a proxy for cost, given that there is a clear positive correlation between both (e.g., the smaller the core volume and/or weight is, the cheaper it is).

Finally, it is worth noting that another large challenge is the light-weight realization of such converters. Gravimetric power density can be the main challenge if the power converter systems are placed, e.g., inside vehicles or aircraft [17, 18]. Although system weight is not the main focus of the research work of this thesis, it does have be taken into consideration when designing

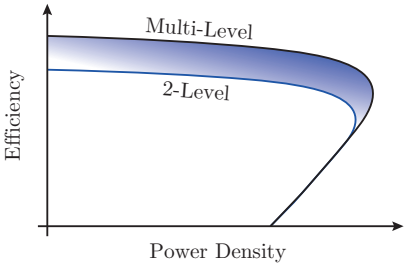

Fig. 1.3: Representative Pareto front curves that highlight the trade-off between efficiency and power density for a 2-level (2L) and a multi-level (ML) converter approach.

PV inverters in the kW range, since the overall weight of the system is typically limited such that a single person is allowed to handle the equipment, for instance, at the time of installation (e.g., these values are limited to 25 kg in Switzerland [19], and recommended to remain below 23 kg in the United States [20]).

1.2 Aims and Contributions

The two power electronic system challenges that are the focus of this thesis can readily be represented in a performance space, as the one shown in **Fig. 1.3**, from which then the Pareto front optimal designs can be identified [21]. Given the clear trade-off between both, this thesis focuses on identifying and proposing solutions that extend the Pareto front of power electronics converters towards ultra-high efficiency, while still achieving a compact system realization. The structure of this work is represented in **Fig. 1.4**, and the aims and contributions are described in the following:

- **Component Level**

  In a first step, semiconductor devices and their losses are analyzed, since these are typically the main loss contributors in converters. This is done in **Chapter 2**, where after introducing a device Figure-of-Merit (D-FOM) that characterizes the losses of a 2L bridge-leg (half-bridge), the properties of ML converters are analyzed, yielding a clear performance improvement potential. This leads to the opportunity of defining an extended Figure-of-Merit (X-FOM), which can directly be used to quantify and assess the benefits of ML topologies.

- **Bridge-Leg / Topology Level**

  Having identified the potential of ML converters, the next step in **Chapter 3** is to discretize the analysis to specific converter topologies with the goal of identifying the most suitable bridge-leg configuration for a 99.5 % efficient realization of a three-phase PV inverter in the 10 kW range. After a comprehensive topology evaluation which includes the volume and losses of the EMI filter components, a hybrid ML topology which was originally proposed for medium voltage drives is identified as the best candidate for reaching the ultra-high-efficiency target while still featuring a compact realization.

- **Full System / Converter Level**

  The realization of an all-Silicon (all-Si) 7-level (7L) hybrid neutral point clamped converter featuring a 99.35 % peak efficiency and a power density of 3.4 kW/dm³ (55.9 W/in³) is presented in **Chapter 4**. It is shown that replacing the 200 V Si semiconductors in the flying capacitor (FC) stage with commercially available 200 V Gallium Nitride (GaN) semiconductors would allow to reach over 99.5 % efficiency.

- **Synergetic Control / Function Integration**

  As a last step, a holistic approach is taken in **Chapter 5** considering the interaction of two-stage conversion processes consisting of cascaded AC/DC and DC/DC converters. For this, a Vienna rectifier front-end followed by two series-connected DC/DC modules is analyzed, whereby using a synergetic control strategy, only one out of the three phases must be switched at a time while still guaranteeing sinusoidal currents at the AC grid interface. Consequently, a saving of more than two thirds of the switching transitions is obtained, at a ≈ 10 % increase in diode losses.

1.3 Ultra-High-Efficiency DC/AC Converter State-of-the-Art

To identify where the current boundaries of ultra-high efficiency are, two subsets of systems are analyzed: commercial systems and research and/or academic systems.

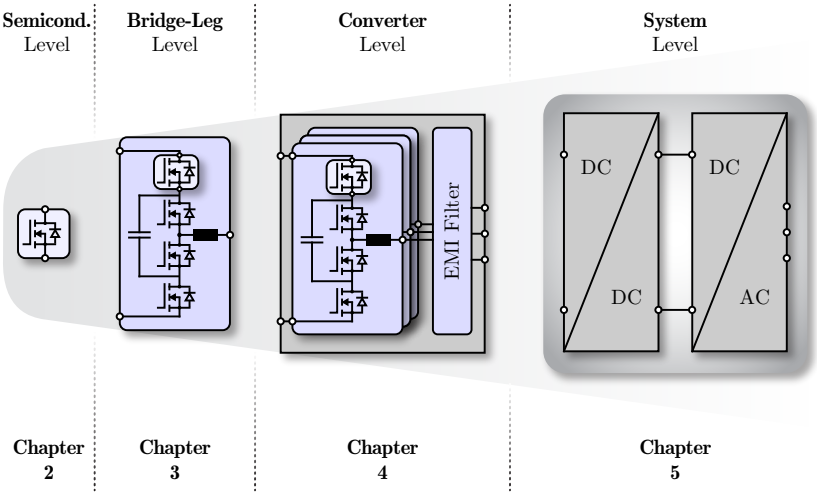

Fig. 1.4: Structural representation of the thesis, where different concepts that enable ultra-high-efficiency and highly-compact solutions are analyzed and proposed for an increasing range of power electronics abstraction levels.

The three-phase PV inverters of the five companies with the largest market share in 2019 in terms of installed MWs [22] that offer systems in the 10 kW power range are given in **Table 1.2**. Note that these systems also include the DC/DC converter stage with the integrated maximum power point tracker (MPPT). The standard PV inverter features a peak efficiency above 98.0 %, with the two largest suppliers manufacturing inverters peaking at 98.6 % and featuring a weighted European Efficiency of above 98.0 % [23].

In order to understand how much further the research field of power electronics is compared to industry, a handful of the best performing converters and/or bridge-legs realized with an *LC* filter (i.e., bridge-legs with only a switching stage and no filtering are not considered) are summarized in **Table 1.3**. Here, all the examples have been chosen such that the DC-link voltages are larger than the peak line-to-line voltage of a 400 V_{rms} three-phase system, i.e., 565 V, such that they could be used as a bridge-leg of a three-phase PV (buck-type) inverter, and the rated power is limited to converters between 1 kW and 25 kW to allow for meaningful comparisons. To the knowledge of the author, there is no converter that falls into the 99+ % category, where the best performing bridge-leg features a peak efficiency of 98.9 %. Finally, it is

Tab. 1.2: Main characteristics of commercially available three-phase PV inverters of the largest PV inverter suppliers worldwide, which include an integrated DC/DC converter for MPPT.

Supplier	Power	$U_{ac,rms,ph}$	$U_{dc,max}$	Peak Eff.	Eur. Eff.	Weight
Huawei [24]	8 kW	230 V	950 V	98.6 %	98.0 %	17 kg
Sungrow [25]	10 kW	230 V	1000 V	98.6 %	98.1 %	24 kg
SMA [26]	10 kW	230 V	800 V	98.3 %	98.0 %	20.5 kg
Fimer [27]	10 kW	230 V	750 V	97.8 %	97.1 %	41 kg
SolarEdge [28]	10 kW	230 V	<900 V	98.0 %	97.6 %	18.9 kg

Tab. 1.3: Main characteristics of a selection highest efficiency DC/AC bridge-legs and converters from literature that have a DC-link voltage larger than the three-phase peak to peak line voltage 400 V_{rms} (U_{dc}>565 V) and feature at least one *LC* filter stage.

Author	Power	$U_{ac,rms,ph}$	U_{dc}	Peak Eff.	Vol. Density	Grav. Density
Barth *et al.*, [30]	3 kW	250 V	800 V	98.4 %	-	12.4 $\frac{kW}{kg}$
Pallo *et al.*, [31]	13.5 kW	380 V	1000 V	98.6 %	17.4 $\frac{kW}{dm^3}$	26.7 $\frac{kW}{kg}$
Modeer *et al.*, [17]	10 kW	380 V	1000 V	98.6 %	31.25 $\frac{kW}{dm^3}$	17 $\frac{kW}{kg}$
Deboy *et al.*, [32]	17 kW	230 V	950 V	98.8 %	-	-
He *et al.*, [33]	20 kW	277 V	600 V	98.85 %	4.0 $\frac{kW}{dm^3}$	-
Huang *et al.*, [34]	25 kW	220 V	800 V	98.9 %	7.72 $\frac{kW}{dm^3}$	-

worth to explicitly mention, that in [29] a 60 kW Silicon Carbide (SiC) based three-phase PV inverter is presented featuring an outstanding 99.2 % efficiency and a power density of 1.64 kW/dm³. This system, however, presents a filterless design that is meant to be directly interfaced with the grid, and hence, essentially only provides a measure for the semiconductor efficiency.

Concerning EV chargers, a survey done in [12] finds that all of the commercial state-of-the-art DC fast chargers (with a combined rating between 50 kW and 350 kW) have an efficiency between 91 % and 95 %, and all weigh more than 165 kg. Finally, it is noteworthy that most of the fast chargers are

built in modular designs [12, 13], where, e.g., for the Tesla Supercharger 12 modules are connected in parallel to supply a power of 135 kW.

1.4 List of Contributions

The most significant contributions of this thesis developed in the scope of related projects are collected in the following in reverse-chronological order.

1.4.1 Journal Papers

[J8] **J. Azurza Anderson**, G. Zulauf, P. Papamanolis, S. Hobi, S. Mirić, J. W. Kolar, "Three levels are not enough: Scaling laws for multi-level converters in AC/DC applications," *IEEE Transactions in Power Electronics*, vol. 36, no. 4, pp. 3967–3986, 2021.

[J7] **J. Azurza Anderson**, G. Zulauf, J. W. Kolar, G. Deboy, "New figure-of-merit combining semiconductor and multi-level converter properties," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322–338, 2020.

[J6] M. Guacci, **J. Azurza Anderson**, K. Pally, D. Bortis, J. W. Kolar, M. Kasper, J. Sanchez, and G. Deboy, "Experimental characterization of Silicon and Gallium Nitride 200 V power semiconductors for modular/multi-level converters using advanced measurement techniques," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2238–2254, 2020.

[J5] **J. Azurza Anderson**, E. J. Hanak, L. Schrittwieser, M. Guacci, J. W. Kolar, and G. Deboy, "All-Silicon 99.35 % efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 1, pp. 50–61, 2019.

Furthermore, during the course of this PhD thesis, the author had the pleasure to also contribute to the following journal papers:

[J4] M. Haider, **J. Azurza Anderson**, S. Mirić, N. Nain, G. Zulauf, J. W. Kolar, D. Xu, G. Deboy, "Novel ZVS S-TCM modulation of three-phase AC/DC converters," in *IEEE Open Journal of Power Electronics*, vol. 1, pp. 529–543, 2020.

[J3] M. Haider, **J. Azurza Anderson**, N. Nain, G. Zulauf, J. W. Kolar, D. Xu, G. Deboy, "Analytical calculation of the residual ZVS losses of TCM-operated single-phase PFC rectifiers," in *IEEE Open Journal of Power Electronics* (Early Access).

[J2] M. Antivachis, **J. Azurza Anderson**, D. Bortis, J. W. Kolar, "Analysis of a synergetically controlled two-stage three-phase DC/AC buck-boost converter," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 1, pp. 34–51, 2020.

[J1] **J. Azurza Anderson**, C. Gammeter, L. Schrittwieser, J. W. Kolar, "Accurate calorimetric switching loss measurement for 900V 10mΩ SiC MOSFETs," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 5240–5250, 2017.

1.4.2 Conference Papers

[C6] J. W. Kolar, **J. Azurza Anderson**, S. Mirić, M. Haider, M. Guacci, M. Antivachis, G. Zulauf, D. Menzi, P. Niklaus, J. Miniböck, P. Papamanolis, G. Rohner, N. Nain, D. Cittanti, D. Bortis, "Application of WBG power devices in future 3-phase variable speed drive inverter systems - How to handle a double-edged sword," in *IEEE Proc. of the International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2020.

[C5] **J. Azurza Anderson**, M. Haider, D. Bortis, J. W. Kolar, M. Kasper, G. Deboy, "New synergetic control of a 20kW isolated Vienna rectifier front-end EV battery charger," in *IEEE Proc. of the Workshop on Control and Modeling for Power Electronics (COMPEL)*, Toronto, Canada, 2019.

[C4] **J. Azurza Anderson**, E. J. Hanak, L. Schrittwieser, J. W. Kolar, G. Deboy, "Towards a 99.5% efficient all-Silicon three-phase seven-level hybrid active neutral point clamped inverter," in *IEEE Proc. of the International Power Electronics and Application Conference and Exposition (PEAC)*, Shenzhen, China, 2018.

Best Presenter at the Session Award

[C3] **J. Azurza Anderson**, M. Leibl, L. Schrittwieser, J. W. Kolar, "Multi-level topology evaluation for ultra-efficient three-phase inverters," in *IEEE Proc. of the International Telecommunications Energy Conference (INTELEC)*, Broadbeach, Australia, 2017.

Additionally, I have also contributed to the following conference papers:

[C2] Y. Li, **J. Azurza Anderson**, D. Bortis, J. W. Kolar, "Control and protection of a synergetically controlled two-stage boost-buck PFC rectifier system under irregular grid conditions," in *IEEE Proc. of the International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Nanjing, China, 2020.

[C1] P. Niklaus, **J. Azurza Anderson**, D. Bortis, J. W. Kolar, "Ultra-high bandwidth GaN-based class-D power amplifier for testing of three-phase mains interfaces for renewable energy systems," in *IEEE Proc. of the International Conference on Renewable Energy Research and Applications (ICRERA)*, Brasov, Romania, 2019.

Best Paper Award

1.4.3 Patents

[P3] **J. Azurza Anderson**, M. Haider, S. Mirić, J. W. Kolar, "Power conversion method and power converter," Patent Application, 2020.

[P2] D. Menzi, M. Zhang, **J. Azurza Anderson**, J. W. Kolar, "Multi-level bidirectional electrical AC/DC converter," Patent Application, 2020.

[P1] D. Bortis, J. W. Kolar, **J. Azurza Anderson**, "Control method for 3-phase isolated converter systems," Patent Application, 2019.

1.4.4 Workshops, Tutorials, Keynotes, etc.

[W8] **J. Azurza Anderson**, Y. Li and J. W. Kolar, "Record breaking concepts in power electronics: Multi-level power conversion and synergetic control," *Presentation at Technology Talks of Infineon Technologies Austria AG*, Villach, Austria, 2020.

[W7] J. W. Kolar, **J. Azurza Anderson**, M. Guacci, M. Antivachis, D. Bortis, "Advanced 3-phase SiC/GaN PWM inverter & rectifier systems," *Presentation at the Centre for Power Electronics Annual Conference*, Loughborough, UK, 2019.

[W6] D. Bortis, J. W. Kolar, M. Antivachis, **J. Azurza Anderson**, M. Guacci, D. Menzi, "Advanced three-phase PFC-rectifiers," *Presentation at the*

ECPE Cluster-Seminar "Power Factor Correction (PFC)" und "Active Frontend" Schaltungen, Bauelemente, Regelung (in German), Augsburg, Germany, 2019.

[W5] **J. Azurza Anderson**, M. Guacci, D. Neumayr, and J. W. Kolar, "Evaluation of a hybrid multi-level flying capacitor bridge-leg topology for beyond 99 % power conversion efficiency," *Presentation at the Huawei Workshop on Highly Efficient Single Phase Power Converters in the Low Voltage Grid Connected Application*, Nuremberg, Germany, 2019.

[W4] D. Neumayr, J. W. Kolar, D. Bortis, M. Guacci, and **J. Azurza Anderson**, "Google little-box reloaded - Advances in ultra-compact GaN based single-phase DC/AC power conversion," *Tutorial at the International Wide-Bandgap Power Electronics Applications Workshop (SCAPE)*, Stockholm, Sweden, 2019.

[W3] J. W. Kolar, D. Neumayr, D. Bortis, M. Guacci, and **J. Azurza Anderson**, "Google little-box reloaded," *Keynote Presentation at the 10th International Conference on Integrated Power Electronics (CIPS)*, Stuttgart, Germany, 2018.

[W2] D. Neumayr, D. Bortis, M. Guacci, **J. Azurza Anderson**, and J. W. Kolar, "Google little-box reloaded," *Presentation at the STS (Spezial Transformatoren Stockach) Annual Seminar*, Ludwigshafen, Germany, 2018.

[W1] M. Guacci, D. Neumayr, D. Rothmund, **J. Azurza Anderson**, D. Bortis, and J. W. Kolar, "Accurate calorimetric switching loss measurement of ultra-fast power semiconductors," *Presentation at the ECPE Workshop "EMC in Power Electronics: From Harmonics to MHz - Design for EMC and Fast Switching"*, Berlin, Germany, 2017.

2

New Figure-of-Merit Combining Semiconductor and Multi-Level Converter Properties

This chapter summarizes the most relevant results of the research on a new Figure-of-Merit characterization of multi-level converters also published in:

- **J. Azurza Anderson**, G. Zulauf, J. W. Kolar, G. Deboy, "New figure-of-merit combining semiconductor and multi-level converter properties," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322–338, Aug. 2020.

Motivation

Multi-level bridge-legs offer a clear performance benefit in terms of power semiconductor losses and filter size and/or loss reduction. However, lacking a simple metric to quantify these benefits, a new Figure-of-Merit that allows to map the switching device properties into multi-level converter performance is proposed.

Executive Summary

Figures-of-Merit (FOMs) are widely-used to compare power semiconductor materials and devices and to motivate research and development of new technology nodes. These material- and device-specific FOMs, however, fail to directly translate into quantifiable performance in a specific power electronics application. Here, device performance is combined with specific bridge-leg topologies to propose the extended FOM, or X-FOM, a Figure-of-Merit that quantifies bridge-leg performance in ML topologies and supports the quantitative comparison and optimization of topologies and power devices. To arrive at the proposed X-FOM, the fundamental scaling laws of the on-state resistance and output capacitance of power semiconductors are revisited to first propose a revised device-level semiconductor Figure-of-Merit (D-FOM). The D-FOM is then generalized to a ML topology with an arbitrary number of levels, output power, and input voltage, resulting in the X-FOM that quantitatively compares hard-switched semiconductor stage losses and filter stage requirements across different bridge-leg structures and numbers of levels, identifies the maximum achievable efficiency of the semiconductor stage, and determines the loss-optimal combination of semiconductor die area and switching frequency. To validate the new X-FOM and showcase its utility, a case study on candidate bridge-leg structures for a three-phase 10 kW PV inverter is performed, with the X-FOM showing that *(a)* the minimum hard-switching losses are an accurate approximation to predict the theoretically maximum achievable efficiency and relative performance between bridge-legs and *(b)* the 3-level (3L) bridge-leg outperforms the 2L configuration, despite utilizing a SiC MOSFET with a lower D-FOM than in the 2L case.

2.1 Introduction

FOMs are ubiquitous and powerful, and are used widely to compare candidate power semiconductor materials and realized devices. Material-based Figures-of-Merit (M-FOMs) compare the material properties that are critical to device operation, including critical electric field, electron mobility, and/or the thermal conductivity [35–39], and have driven the research, development, and recent commercialization of wide-bandgap (WBG) power semiconductors like GaN and SiC. When a given M-FOM is combined with a particular device structure, manufacturing process, and packaging technique (see **Fig. 2.1a**), higher-level device parameters – such as on-state resistance (R_{on}), equivalent output capacitance (C_{oss}), and gate charge (Q_g) – can be compared across power semiconductors as die area-independent device Figures-of-Merit, or D-FOMs [38–45], which are often used to compare technology generations and commercial devices across technology, manufacturer, and breakdown voltage in both academia and industry [46]. None of the proposed FOMs, however, translates directly to the performance of a power semiconductor bridge-leg in a particular power electronics application, a literature gap that

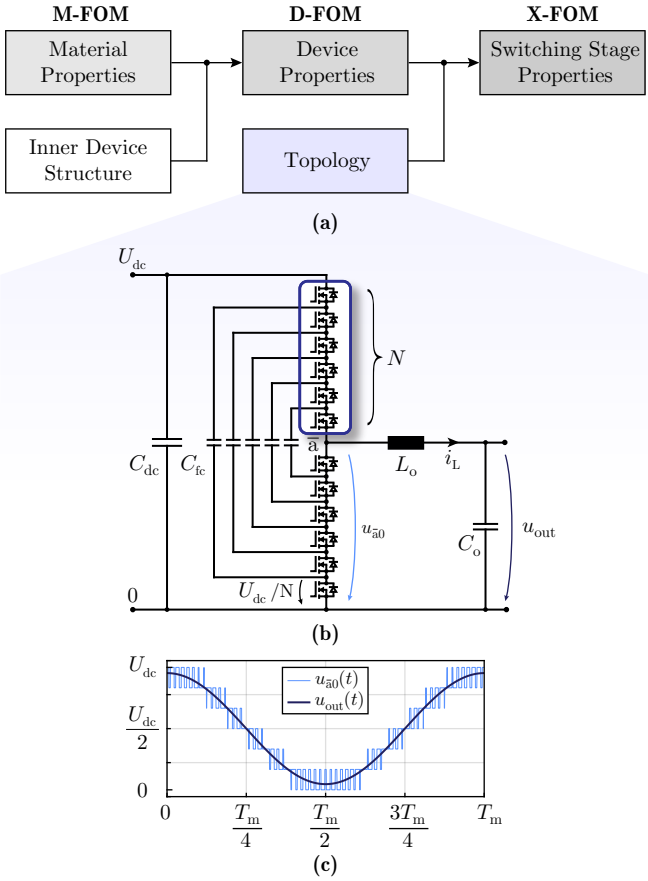

Fig. 2.1: (a) Comparison of FOMs, with the combination of material properties (M-FOM) and device structure leading to a device Figure-of-Merit (D-FOM), and the combination of device properties and topology leading to the application-specific Figure-of-Merit proposed here, the extended FOM, X-FOM. **(b)** ML bridge-leg with $N+1$ levels, with $2N$ devices per bridge-leg, each device withstanding U_{dc}/N, and **(c)**, ML voltage waveform applied to the output filter inductor L_o.

leaves designers unable to compare the *combination* of devices and topologies to optimize bridge-leg performance in a particular application.

To address this shortcoming, modern power semiconductor device properties are combined with the increasingly-adopted ML bridge-leg configuration

(**Fig. 2.1b**) to propose an *extended FOM* (X-FOM) that compares the performance of ML bridge-legs across input voltage, power device selection, number of levels, switching frequency, and a host of other parameters to quantitatively compare performance among different configurations and predict the optimal bridge-leg efficiency. Compared to a conventional 2L bridge-leg, ML converters (**Fig. 2.1b**) can utilize power semiconductors with lower voltage ratings for lower on-resistance [47], demonstrate increased power density [48, 49] and efficiency [29, 50]. In flying capacitor converters (FCC [51]), in particular, the filter size can also be reduced as more levels are added due to the lower volt-seconds applied to the output inductor [52] (**Fig. 2.1c**). Despite the demonstrated promise of these ML converters, though, there does not exist a straightforward method to optimally select the power semiconductor alongside the correct number of levels in a ML topology. Here, the fundamental understanding of the advantages of using a ML power semiconductor stage is developed – a quantification summarized in the proposed X-FOM.

First, the voltage scaling laws of on-state resistance and output capacitance across power semiconductor technologies are revisited (**Section 2.2**) to arrive at a device-level Figure-of-Merit, or D-FOM, for a hard-switching bridge-leg that considers the theoretical *minimum* hard-switching losses in the semiconductor devices (**Section 2.3**). This improved D-FOM explicitly defines the maximum achievable efficiency of a bridge-leg with application-specific conditions. With these minimum losses defined, then the loss calculation and die area optimization are generalized to an arbitrary number of levels in a ML bridge-leg (see **Fig. 2.2**) to arrive at the proposed extended FOM, or X-FOM (**Section 2.4**), which is a direct and straightforward comparison between various combinations of bridge-leg structure and power semiconductor selection. The new X-FOM is applied to a three-phase 10 kW PV inverter in a case study (**Section 2.5**) to validate the minimum loss approximation and illustrate the utility of this new Figure-of-Merit. With this X-FOM verified as an accurate predictor of the maximum achievable efficiency for a given bridge-leg, it is seen that the X-FOM can be used directly to compare and motivate both device and topological improvements, finally bringing device considerations to the end power electronics application. **Section 2.6** summarizes the main findings and, in light of this new X-FOM, highlights promising research directions on both power devices and topologies.

Fig. 2.2: Relationship between the **(a)** device Figure-of-Merit, D-FOM, which depends only on semiconductor properties, and **(b)**, the extended Figure-of-Merit, X-FOM, which combines the properties of both the semiconductor and converter structure, including the DC-link voltage U_{dc}, the RMS output current of the bridge-leg, and the switching frequency. The developed mapping between the D-FOM and X-FOM assumes a semiconductor die area that is optimized to minimize the hard-switched semiconductor losses (sum of conduction and switching losses) of the bridge-leg.

2.2 Semiconductor Device Voltage Scalings

To compare across topologies, first the foundation of understanding how semiconductor performance scales when a high-voltage switch is replaced with lower-voltage counterparts must be layed (e.g., when increasing the number of levels in a ML configuration, where each semiconductor must block U_{dc}/N, U_{dc} being the DC-link voltage and N the number of levels minus one, cf., **Fig. 2.1b**). In this section, this voltage scaling is considered in the context of the two dominant power semiconductor loss mechanisms: conduction losses and switching losses.

2.2.1 Conduction Losses

A first step towards calculating the maximum efficiency of a converter is to only consider the conduction losses of the power semiconductors. For the topology depicted in **Fig. 2.1b**, the conduction losses are given by

$$P_{cond} = R_{eq} I_{rms}^2, \tag{2.1}$$

where R_{eq} is the total on-state resistance of the simultaneously-conducting devices of the bridge-leg (i.e. NR_{on}, where there are $2N$ devices per bridge-leg and R_{on} is the on-state resistance of one switch), and I_{rms} is the RMS current through the inductor L_o. I_{rms} is given by the power and voltage specifications of the application, and assuming L_o is selected for a relatively small current ripple, conduction losses can only be decreased by reducing R_{eq}. This assumption is not reliant on the particular selection of L_o – even if the ripple RMS current ($I_{rms,HF}$) is, e.g., 10 % of the fundamental RMS (cf., **Fig. 2.4a**), the conduction losses change by only 1 % ($I_{rms}^2 + I_{rms,HF}^2 = I_{rms}^2 + (0.1 I_{rms})^2 = 1.01 I_{rms}$).

To analyze the conduction loss difference between a single high-voltage device and several series-connected lower-voltage devices (**Fig. 2.1b)**, first the voltage dependence of the on-state resistance, R_{on}, as a function of the blocking voltage of a device, U_B, must be considered. The on-state resistance can be written as the area-specific on-resistance (R'_{on}), and further rewritten with a technology-specific constant (k_R) and voltage-scaling exponential coefficient (α_R), as:

$$R_{on}(U_B) = \frac{R'_{on}(U_B)}{A_{die}} = \frac{k_R U_B^{\alpha_R}}{A_{die}} \approx \frac{k_R U_B^2}{A_{die}}, \tag{2.2}$$

where A_{die} is the die area. For vertical devices, and only considering a very basic model, i.e., the resistance contributed by a one-dimensional (1D)

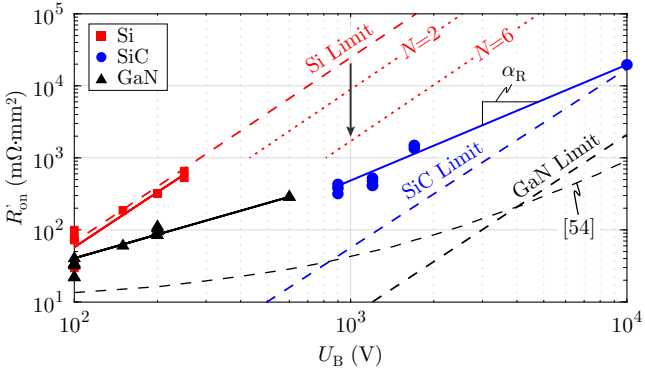

Fig. 2.3: Specific on-state resistance R'_{on} at 25 °C junction temperature (T_j) for a selection of commercial power semiconductors. The Si, SiC and GaN theoretical limits from [53–55] are shown (dashed) together with the power function fits ($k_R \cdot U_B^{\alpha_R}$) given in **Table 2.1**. The Si scaling with increased number of series-connected devices ($N = 2$ and $N = 6$) toward ML converters use a constant (individual) die area scaling.

Tab. 2.1: Scaling factors α_R and k_R for R'_{on}. k_R is given such that R'_{on} is in mΩ·mm² and is fit at $T_j = 25$ °C.

	Si	SiC	GaN
k_R	$4.8 \cdot 10^{-4}$	$7.2 \cdot 10^{-3}$	0.26
α_R	2.5	1.6	1.1

ideal drift region, α_R is theoretically equal to 2, as derived in **Appendix A** and given widely (e.g., in [38]).

This approximation for α_R is given as a first step to facilitate an understanding of the scaling laws, and, in the following, the assumption of $\alpha_R \approx 2$ for applicable device technologies for hard-switched converters, i.e., Si MOSFETs, SiC MOSFETs, and GaN-on-Si HEMTs, will be examined. **Fig. 2.3** shows a survey of commercially available state-of-the-art devices and **Table 2.1** gives the empirically-fit exponential coefficients and constants for each technology.

For Si MOSFETs, the empirical fitting agrees with the theoretical $R'_{on} \propto U_B^{2.5}$ scaling found when considering the dependence of electric field on doping concentration [53]. For SiC MOSFETs and GaN-on-Si HEMTs, the voltage scaling terms are less than the $\alpha_R \approx 2$ predicted by the simple model (see **Appendix A** for a discussion of the root causes of the respective voltage

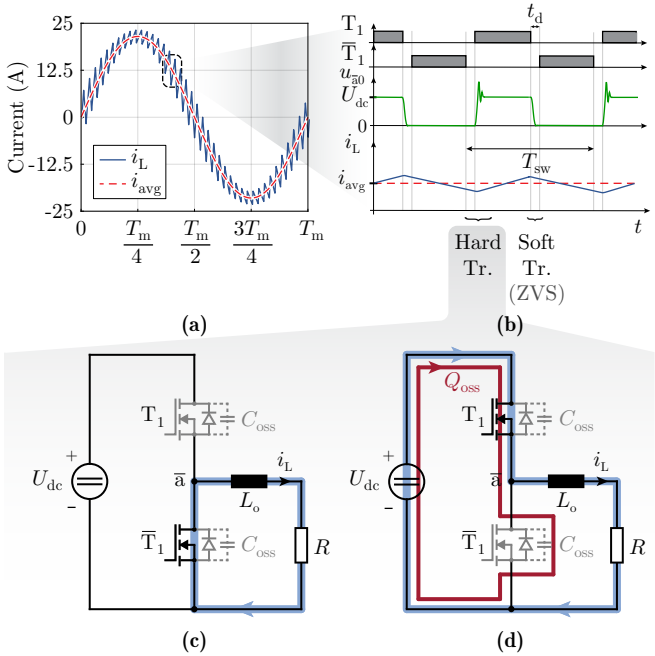

Fig. 2.4: (a) Continuous conduction mode (CCM) simulated waveforms, where i_L is the inductor current and i_{avg} is the filtered output current. **(b)** Detailed transition waveforms for a switching period (T_{sw}), where t_d denotes the deadtime. **(c)** Start of the hard-switched transition, and **(d)**, end of the hard-switched transition. During the switch transition, C_{dc} (modelled as a voltage source) supplies a charge of Q_{oss} at voltage U_{dc}, and this supplied energy equals the dissipated energy of $Q_{oss}U_{dc}$ [57].

scalings) but agree with previously-derived empirical fits of α_R [56]. These technology-specific scaling factors have far-reaching impacts on the desirability and design of ML topologies, as they define the reduction in individual R_{on} with lower blocking voltage. With the voltage scaling of specific on-resistance – and therefore conduction losses – well-defined, the process is repeated to determine the dependence of switching losses on device blocking voltage.

Triangular Current Mode

One common application where it is sufficient to only evaluate the R_{on} scaling is in Triangular Current Mode (TCM) operation [58–60], which in contrast to

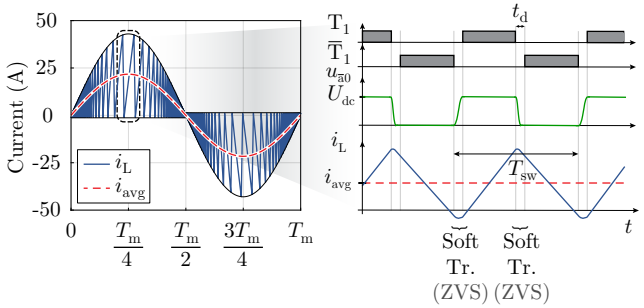

Fig. 2.5: (a) TCM operation, **(b)** with two soft-switching transitions per switching period. Relative to CCM, TCM has higher RMS currents ($2/\sqrt{3}$ higher, leading to 33 % higher conduction losses) but eliminates hard-switching.

CCM that features one hard-switching and one soft-switching transition per switching period (cf., **Fig. 2.4a,b**), features two soft-switching transitions per switching period (cf., **Fig. 2.5a,b**), but at a cost of an increased RMS current.

At frequencies in the hundreds of kHz range, where TCM may be preferred [58–60], it can safely be assumed that any soft-switching losses are negligible compared to the conduction losses [61–65], and analyze the increase in RMS current in the bridge-leg under TCM operation. The relation between the RMS current of TCM and CCM is given by:

$$I_{\text{rms,tcm}} = \frac{2}{\sqrt{3}} I_{\text{rms,ccm}} \,, \tag{2.3}$$

which leads to

$$P_{\text{cond,tcm}} = \frac{4}{3} P_{\text{cond,ccm}}. \tag{2.4}$$

Hence, at a cost of 33 % higher conduction losses, then, switching losses can be de facto eliminated and the R_{on} scaling laws are sufficient for a complete analysis.

2.2.2 Switching Losses

To accurately model the minimum hard-switching losses, first a single hard-switching transition in a bridge-leg is reexamined to find the correct linear-equivalent capacitance model and losses from hard-switching. To derive these scaling laws, it is noted again that the $V - I$ overlap period is assumed to be

small and therefore only capacitive switching losses occur, an assumption that is later relaxed when this model is compared to experimentally-measured switching losses. Nonetheless, this assumption is reasonable with the operating conditions considered here for hard-switched high-efficiency applications, where switched currents are typically much lower than rated currents [50, 66], and fast switching transitions are desired as well as enabled by WBG devices.

These capacitive losses, which occur under zero-load-current switching (ZCS), represent the minimum hard-switching losses, the desired quantity to assess the maximum achievable efficiency with the various bridge-leg configurations. A single hard-switching transition is shown in **Fig. 2.4c,d**, where the parasitic output capacitor (C_{oss}) of T_1 starts charged to U_{dc} in the initial state (**Fig. 2.4c**, $\overline{\mathrm{T}}_1$ conducting) and the transition ends with T_1 conducting and the C_{oss} of $\overline{\mathrm{T}}_1$ charged to U_{dc} (**Fig. 2.4d**) by the supply. The two switches are assumed identical and the inductor current remains constant during the switching transition. The minimum hard-switching energy dissipated per cycle (E_{sw}, assuming that there is one hard-switched and one soft-switched transition per period) is given as [57]:

$$E_{\mathrm{sw}} = Q_{\mathrm{oss}}(U_{\mathrm{dc}})U_{\mathrm{dc}} = C_{\mathrm{oss,Q}}(U_{\mathrm{dc}})U_{\mathrm{dc}}^2 \tag{2.5}$$

where $C_{\mathrm{oss,Q}}(U_{\mathrm{dc}})$ is the voltage-dependent charge-equivalent output capacitance [57, 67]. The losses in **(2.5)** are equal to the ZCS losses, and are the minimum hard-switching losses where the $V-I$ overlap losses [56] don't exist due to zero load current. These minimum losses match very precisely with the measurements presented in **Section 2.5** and with results reported in prior literature [64, 65]. Note however, that if there zero load current is present during the whole switching period, then two zero-load-current transitions occur per switching period, leading to double the losses presented in Eq. **(2.5)**.

Therefore, as a first step, the hard-switching losses are written as:

$$P_{\mathrm{sw}} = Q_{\mathrm{oss}}(U_{\mathrm{dc}})U_{\mathrm{dc}}f_{\mathrm{sw}} = C_{\mathrm{oss,Q}}(U_{\mathrm{dc}})U_{\mathrm{dc}}^2 f_{\mathrm{sw}}, \tag{2.6}$$

where f_{sw} is the switching frequency and $C_{\mathrm{oss,Q}}(U_{\mathrm{dc}})$ is the charge-equivalent output capacitance evaluated at U_{dc}.

Similarly to the derivation for the relationship between R_{on} and the blocking voltage of the device, U_{B}, a voltage-scaling for $C_{\mathrm{oss,Q}}$ is desired. This charge-equivalent capacitance can be written as the area-specific charge-equivalent capacitance ($C'_{\mathrm{oss,Q}}$), and further rewritten with a technology-specific constant (k_{C}) and voltage-scaling factor (α_{C}) for this capacitance, as:

$$C_{\mathrm{oss,Q}}\left(U_{\mathrm{B}}\right) = C'_{\mathrm{oss,Q}}(U_{\mathrm{B}})A_{\mathrm{die}} = k_{\mathrm{C}}U_{\mathrm{B}}^{\alpha_{\mathrm{C}}}A_{\mathrm{die}} \approx k_{\mathrm{C}}U_{\mathrm{B}}^{-1}A_{\mathrm{die}}. \tag{2.7}$$

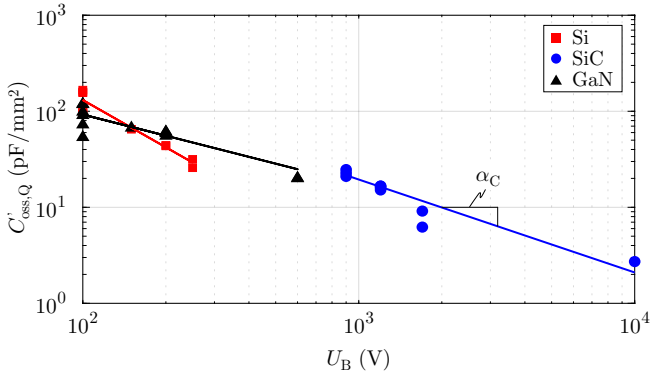

Fig. 2.6: Specific charge-equivalent output capacitance $C'_{\mathrm{oss,Q}}$ for a selection of commercially-available power devices. The power function fits ($k_{\mathrm{C}} \cdot U_{\mathrm{B}}^{\alpha_{\mathrm{C}}}$) are given in **Table 2.2**.

Tab. 2.2: Scaling factors α_{C} and k_{C} for $C'_{\mathrm{oss,Q}}$. k_{C} is given such that $C'_{\mathrm{oss,Q}}$ is in pF/mm^2.

	Si	SiC	GaN
k_{C}	$2.4 \cdot 10^5$	$1.6 \cdot 10^4$	$2.7 \cdot 10^3$
α_{C}	-1.6	-1.0	-0.7

For vertical devices, and only considering the one-dimensional (1D) ideal drift region, $\alpha_{\mathrm{C}} = -1$, as derived in **Appendix A**. This capacitance scaling is typically not considered in deriving voltage-scaling laws for semiconductors, but, as it is shown in the following sections, is critical in determining a voltage-specific X-FOM for any type of hard-switched converter. This α_{C} approximation is again used to develop an intuition of the scaling laws before finding technology-specific α_{C} values for candidate devices.

To relate the assumption of $\alpha_{\mathrm{C}} \approx -1$ to the actual device characteristics, commercially-available devices are surveyed again, this time for their respective $C'_{\mathrm{oss,Q}}$ values across blocking voltage, U_{B}. This survey is shown in **Fig. 2.6** with fittings in **Table 2.2**, where it is found that, for all candidate technologies, the approximation of $\alpha_{\mathrm{C}} \approx -1$ is relatively close to the empirical fittings. Si has the largest voltage-dependence of the available technologies,

with $\alpha_C = -1.6$, and GaN has the flattest $C'_{oss,Q}$ characteristic with voltage at $\alpha_C = -0.7$.

With a reduction in device voltage rating, then – for example, when moving from a 2L to a ML configuration – the on-resistance decreases (**Fig. 2.3**), reducing the conduction losses, but the output capacitance increases (**Fig. 2.6**), resulting in larger switching losses. The existing of an optimal semiconductor area to trade-off switching losses and conduction losses is well-known; observing these counteracting scaling laws with N, however, the existence of an optimal *total* semiconductor die area for a given number of levels is recognized. In the next section, the optimal die area and minimum semiconductor losses for a 2L bridge-leg are derived before subsequently generalizing these findings to a ML configuration in **Section 2.4**.

2.3 Minimal Power Semiconductor Losses for Two-Level Bridge-Legs

For a 2L bridge-leg (like in **Fig. 2.1b** with $N = 1$) with a DC input voltage U_{dc}, a filter inductor output current I_{rms}, and a switching frequency $f_{sw}|_{2L}$, the losses in the bridge-leg can be calculated as [44, 68]:

$$P_{semi} = I_{rms}^2 \frac{R'_{on}(U_{dc})}{A_{die}} + C'_{oss,Q}(U_{dc})\, U_{dc}^2\, f_{sw}|_{2L}\, A_{die}, \tag{2.8}$$

where it is observed that an increase of die area (A_{die}) reduces conduction losses but increases the switching losses, as shown in **Fig. 2.7**. Naturally, this leads to a loss-minimizing $\left(\frac{dP_{semi}}{dA_{die}} = 0\right)$, optimal total bridge-leg semiconductor area of:

$$A_{die,opt,tot}\big|_{2L} = 2\frac{I_{rms}}{U_{dc}}\sqrt{\frac{R'_{on}(U_{dc})}{C'_{oss,Q}(U_{dc})\, f_{sw}|_{2L}}} \tag{2.9}$$

and the minimized semiconductor losses in the 2L bridge-leg of:

$$P_{semi,min}\big|_{2L} = 2 I_{rms} U_{dc} \sqrt{f_{sw}|_{2L}\, R'_{on}(U_{dc})\, C'_{oss,Q}(U_{dc})}, \tag{2.10}$$

both of which are shown under normalized conditions in **Fig. 2.7**. Before introducing scaling to these loss-optimized conditions with the number of levels and/or individual device blocking voltage, some observations from this simple derivation merit discussion.

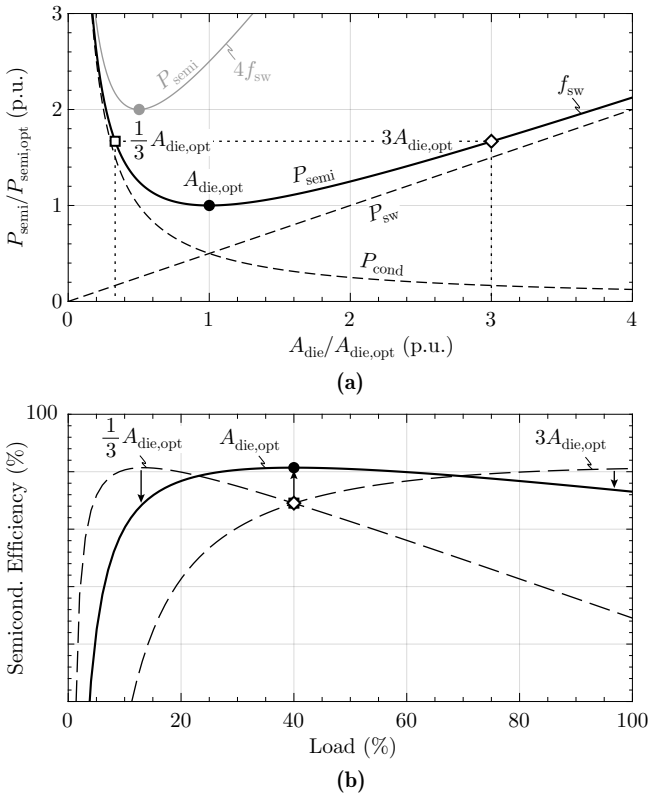

Fig. 2.7: 2L loss-minimized optimal semiconductor die area and minimum bridge-leg losses (considering only semiconductor losses). **(a)** Variation of optimal bridge-leg losses and optimal die area, from Eqs. **(2.9)** and **(2.10)**. At higher switching frequencies, a smaller die area is preferred to reduce switching losses. The optimal area curve is relatively flat, which is convenient for selecting commercially-available power devices, with a 3× deviation in either direction from the optimum only increasing losses by 67 %. **(b)** Variation of optimal bridge-leg efficiency with load depending on the selected die area. For light-load optimization, a smaller area is preferred to limit the fixed switching losses. At heavy loads, an increased die area improves efficiency by reducing conduction losses.

- *Effect of* f_{sw} *on* $P_{\text{semi,min}}$: $P_{\text{semi,min}}$ depends on $\sqrt{f_{\text{sw}}}$. Hence, if the desired f_{sw} is increased fourfold, the optimal losses will double and the optimal die area will be halved, as seen in **Fig. 2.7a**.

- *Effect of A_{die} on $P_{\text{semi,min}}$*: $P_{\text{semi,min}}$ features a rather flat curve as a function of A_{die} around $A_{\text{die,opt}}$, as seen in **Fig. 2.7a**. If, e.g., the selected die area is $A_{\text{die}} = 2 \times A_{\text{die,opt}}$, the bridge-leg losses only increase by 25 %. With a 3× larger A_{die} than $A_{\text{die,opt}}$, losses increase by 67 %.

- *Effect of A_{die} selection on part-load efficiency*: The die area can be further selected to optimize efficiency at different load values since I_{rms} is included in Eqs. **(2.9)** and **(2.10)**. In **Fig. 2.7b**, for example, a semiconductor stage that has been initially optimized for operation at 40 % of full load is considered. If the designer prefers higher light-load efficiency, a smaller die area will reduce switching losses and improve this metric. For optimization at heavier loads, a larger die area that reduces conduction losses is preferred.

- *Optimal number of parallel devices from $A_{die,opt}$*: The loss-optimal number of parallel *devices* rather than the loss-optimal device *area* can be simply derived from **(2.9)** by substituting the absolute values (R_{on}, $C_{\text{oss,Q}}$) for the specific values (R'_{on}, $C'_{\text{oss,Q}}$) with Eqs. **(2.2)** and **(2.7)**. Hence, similarly to Eq. **(2.8)**, the minimum power losses in a bridge-leg can be written as:

$$P_{\text{semi}} = I_{\text{rms}}^2 \frac{R_{\text{on}}}{N_{\text{par}}} + N_{\text{par}} C_{\text{oss,Q}}\left(U_{\text{dc}}\right) U_{\text{dc}}^2 \, f_{\text{sw}}\big|_{\text{2L}}, \tag{2.11}$$

  leading to a loss-optimal number of parallel devices,

$$N_{\text{par,opt}}\big|_{\text{2L}} = 2 \frac{I_{\text{rms}}}{U_{\text{dc}}} \sqrt{\frac{R_{\text{on}}}{C_{\text{oss,Q}}\left(U_{\text{dc}}\right) \, f_{\text{sw}}\big|_{\text{2L}}}}. \tag{2.12}$$

  With the die area typically not publicly-available, this substitution allows the designer to select the optimal device number from only absolute, datasheet-provided values.

Lastly, it is identified that the minimum achievable losses of the bridge-leg are influenced through $R'_{\text{on}} C'_{\text{oss,Q}}$ in **(2.10)**. For a given blocking voltage requirement, a "better" semiconductor would lower R'_{on} and/or $C'_{\text{oss,Q}}$, and the opportunity to define a device-level Figure-of-Merit arises:

$$D\text{-}FOM(U_{\text{B}}) = \frac{1}{\sqrt{R'_{\text{on}}\left(U_{\text{B}}\right) C'_{\text{oss,Q}}\left(U_{\text{B}}\right)}}. \tag{2.13}$$

This D-FOM does not require knowledge of the die area of the device, as $R'_{\text{on}}C'_{\text{oss,Q}} = R_{\text{on}}C_{\text{oss,Q}}$, and the D-FOM for a given semiconductor therefore can be determined from non-proprietary datasheet parameters. Similar device FOMs that depend on R'_{on} and the differential C'_{oss} [40] and energy-equivalent output capacitance $C'_{\text{oss,E}}$ [44, 69, 70] have been reported, but the $C'_{\text{oss,Q}}$ dependency proposed here is the correct metric to determine the *minimum* hard-switching losses of a half-bridge. Finally, **(2.10)** can be rewritten compactly as:

$$P_{\text{semi,min}}\big|_{\text{2L}} = \frac{2I_{\text{rms}}U_{\text{dc}}\sqrt{f_{\text{sw}}|_{\text{2L}}}}{D\text{-}FOM|_{\text{2L}}}. \tag{2.14}$$

2.3.1 D-FOM of Commercial Devices

With the introduction of the D-FOM and its influence on the losses, the D-FOM of commercial semiconductors are numerically compared in **Fig. 2.8**.

Now, to understand the influence of the blocking voltage requirement on the D-FOM, and therefore, on the optimal area and minimum bridge-leg losses, a voltage-scaling parameter $\alpha_{\text{D-FOM}}$ is defined (from the R'_{on} and $C'_{\text{oss,Q}}$ power function fits with respect to the blocking voltage U_{B} **(2.2)** and **(2.7)**):

$$\alpha_{\text{D-FOM}} = -\frac{(\alpha_{\text{R}} + \alpha_{\text{C}})}{2} \approx -0.5. \tag{2.15}$$

Using $\alpha_{\text{D-FOM}}$, the D-FOM can be rewritten as:

$$\begin{aligned} D\text{-}FOM(U_{\text{B}}) &= \frac{1}{\sqrt{R'_{\text{on}}\left(U_{\text{B}}\right) C'_{\text{oss,Q}}\left(U_{\text{B}}\right)}} = \frac{1}{\sqrt{k_{\text{R}}k_{\text{C}}}}\frac{1}{U_{\text{B}}^{-\alpha_{\text{D-FOM}}}} \\ &\approx \frac{1}{\sqrt{k_{\text{R}}k_{\text{C}}}}\frac{1}{\sqrt{U_{\text{B}}}} \end{aligned} \tag{2.16}$$

The technology-specific voltage scaling factors $\alpha_{\text{D-FOM}}$ are given in **Table 2.3**. These factors describe the scaling of performance of different semiconductor technologies as a function of blocking voltage, where the higher the absolute value of $\alpha_{\text{D-FOM}}$, the higher the D-FOM gain of reducing the blocking voltage of the switches, as shown in **Fig. 2.8**. For every material, the power factor of on-state resistance voltage dependence is larger than the output capacitance factor (compare **Table 2.1** to **Table 2.2**), resulting in higher D-FOMs for lower blocking voltages in the same device class. For

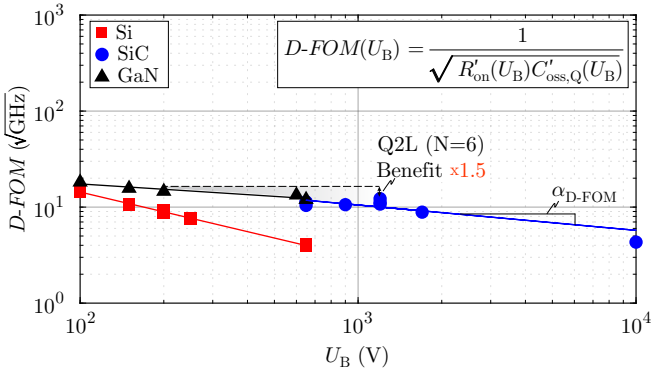

Fig. 2.8: The device Figure-of-Merit *D-FOM* for a survey of commercially available power semiconductors plotted over their blocking voltage, where the $C_{oss,Q}$ is calculated for two-thirds of the rated voltage, and the R_{on} is the typical value at 25 °C. For the Quasi 2-Level (Q2L) operation of bridge-legs, refer to **Appx. B**.

Tab. 2.3: Scaling factors $\alpha_{D\text{-}FOM}$ for D-FOMs for commercially available power semiconductors.

	Si	SiC	GaN
$\alpha_{D\text{-}FOM}$	-0.5	-0.3	-0.2

instance, Si devices, with $\alpha_{D\text{-}FOM} = -0.5$, feature a larger benefit of reducing the blocking voltage of each device than SiC or GaN devices, which feature $\alpha_{D\text{-}FOM} = -0.3$ and $\alpha_{D\text{-}FOM} = -0.2$, respectively.

Using the voltage-scaling approximations, **(2.10)** can instead be rewritten as:

$$P_{semi,min}\big|_{2L} \approx 2I_{rms}U_{dc}\sqrt{U_B}\sqrt{f_{sw}|_{2L}}\sqrt{k_R k_C}\,. \tag{2.17}$$

It can be seen that a reduction of semiconductor blocking voltage (U_B) would straightforwardly result in a higher semiconductor D-FOM and therefore lower losses in a 2L bridge-leg (cf., Eq. **(2.17)**). However, U_{dc} is typically specified for a given application – not a degree of freedom – so alternative bridge-leg topologies are required to utilize the improved D-FOM of lower-voltage devices for a given U_{dc}. This motivates the exploration of ML converters, where it will be quantified how and if the superior properties of

lower-voltage semiconductors, as indicated in Eqs. **(2.16)** and **(2.17)**, together with the topology change, can achieve higher performance.

2.4 Multi-Level Bridge-Leg Generalization

When replacing a 2L bridge-leg with a ML configuration, the following characteristics are obtained:

- A series connection of N devices, where each device must block U_{dc}/N,
- An increase of the effective switching frequency at the output node ($\overline{\mathrm{a}}$ in **Fig. 2.1b**): for an $(N+1)$-level ML converter, the effective switching frequency at the output node is

$$f_{\mathrm{eff}} = N\, f_{\mathrm{sw}}|_{\mathrm{ML}}\ , \tag{2.18}$$

  where $f_{\mathrm{sw}}|_{\mathrm{ML}}$ is the switching frequency of the individual devices.
- Smaller voltage steps at the output node $\overline{\mathrm{a}}$: as shown in **Fig. 2.1b**, there is a ML $(N+1)$ output voltage waveform, reducing the voltage steps across the filter inductor in a switch cycle to only U_{dc}/N.

Note again that the ML is a generalization of a 2L case, where for the 2L case, $N = 1$.

To directly compare the ML bridge-leg to a 2L counterpart, the volt-seconds applied to the inductor are constrained to be constant (this constraint is later relaxed in **Section 2.5.2**). By fixing the volt-seconds applied to the inductor, the current ripple term, $L_{\mathrm{o}}\Delta i_{\mathrm{L}}$ is also fixed between the 2L and ML topologies. In the 2L case, the (worst-case) voltage-time product is:

$$L_{\mathrm{o}}\Delta i_{\mathrm{L}} = \frac{U_{\mathrm{dc}}}{4\, f_{\mathrm{sw}}|_{\mathrm{2L}}}\ , \tag{2.19}$$

where Δi_{L} is the peak-to-peak current ripple. For the two advantages of the ML topology given above, however, the ripple in the ML case is reduced by:

$$L_{\mathrm{o}}\Delta i_{\mathrm{L}} = \frac{\left(\frac{U_{\mathrm{dc}}}{N}\right)}{4\left(N\, f_{\mathrm{sw}}|_{\mathrm{ML}}\right)} = \frac{U_{\mathrm{dc}}}{4N^2\, f_{\mathrm{sw}}|_{\mathrm{ML}}} \Rightarrow L_{\mathrm{o}}\Delta i_{\mathrm{L}} \propto \frac{1}{N^2}, \tag{2.20}$$

where $f_{\mathrm{sw}}|_{\mathrm{ML}}$ is the switching frequency of a single device in the ML bridge-leg (and not the effective switching frequency f_{eff}). Therefore, for the same $L_{\mathrm{o}}\Delta i_{\mathrm{L}}$, the switching frequency in the ML topology can be reduced by N^2 as:

$$f_{\mathrm{sw}}|_{\mathrm{ML}} = \frac{f_{\mathrm{sw}}|_{\mathrm{2L}}}{N^2}. \tag{2.21}$$

For the general case, the bridge-leg losses in the ML topology are:

$$P_{\mathrm{semi}} = NI_{\mathrm{rms}}^2 \frac{R'_{\mathrm{on}}\left(U_{\mathrm{dc}}/N\right)}{A_{\mathrm{die}}} + NC'_{\mathrm{oss,Q}}\left(U_{\mathrm{dc}}/N\right)\left(\frac{U_{\mathrm{dc}}}{N}\right)^2 f_{\mathrm{sw}}|_{\mathrm{ML}}\, A_{\mathrm{die}}\,, \tag{2.22}$$

where the modeling of the switching losses for a ML bridge-leg is discussed in detail in **Appendix C**. When the switching frequency reduction is considered for a fair bridge-leg comparison, the loss-minimized semiconductor losses become:

$$P_{\mathrm{semi,min}}\big|_{\mathrm{ML}} = \frac{2I_{\mathrm{rms}}U_{\mathrm{dc}}\sqrt{f_{\mathrm{sw}}|_{\mathrm{ML}}}}{D\text{-}FOM\left(\frac{U_{\mathrm{dc}}}{N}\right)} = \underbrace{\frac{2I_{\mathrm{rms}}U_{\mathrm{dc}}\sqrt{f_{\mathrm{sw}}|_{\mathrm{2L}}}}{N\cdot D\text{-}FOM\left(\frac{U_{\mathrm{dc}}}{N}\right)}}_{X-FOM(U_{\mathrm{dc}},N)}, \tag{2.23}$$

where the final step of this equation substitutes **(2.21)** and therefore applies the assumption that a constant volt-second product is applied to the filter inductor. This loss-minimized bridge-leg total semiconductor area is:

$$\begin{aligned} A_{\mathrm{die,opt,tot}}\big|_{\mathrm{ML}} &= 2\frac{N^2 I_{\mathrm{rms}}}{U_{\mathrm{dc}}}\sqrt{\frac{R'_{\mathrm{on}}\left(U_{\mathrm{dc}}/N\right)}{C'_{\mathrm{oss,Q}}\left(U_{\mathrm{dc}}/N\right)\, f_{\mathrm{sw}}|_{\mathrm{ML}}}} \\ &\approx N^{1.5}\, A_{\mathrm{die,opt,tot}}\big|_{\mathrm{2L}}\,, \end{aligned} \tag{2.24}$$

and the approximations of **(2.2)** and **(2.7)**, and the constant volt-second assumption are applied to reach the final equation. Keeping these same assumptions, and following the same process as in the previous derivations, it is found:

$$P_{\mathrm{semi,min}}\big|_{\mathrm{ML}} \approx \frac{P_{\mathrm{semi,min}}\big|_{\mathrm{2L}}}{N^{1.5}} \tag{2.25}$$

and for the ML converter Figure-of-Merit:

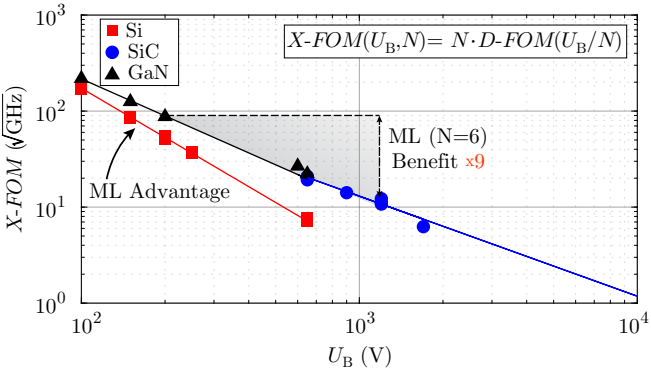

Fig. 2.9: The extended Figure-of-Merit *X-FOM* for ML bridge-legs for the same device survey and operating conditions as **Fig. 2.8**. The *X-FOM* values are normalized around the 1200 V devices, which serve as a benchmark for 2L bridge-legs operating with $U_{\mathrm{dc}} = 800\,\mathrm{V}$.

$$\begin{aligned} X\text{-}FOM(U_{\mathrm{dc}}, N) &= N \cdot D\text{-}FOM\left(\frac{U_{\mathrm{dc}}}{N}\right) \\ &= \frac{N}{\sqrt{R'_{\mathrm{on}}\left(\frac{U_{\mathrm{dc}}}{N}\right) C'_{\mathrm{oss,Q}}\left(\frac{U_{\mathrm{dc}}}{N}\right)}} \\ &= N^{(1-\alpha_{\text{D-FOM}})} \cdot D\text{-}FOM(U_{\mathrm{dc}}) \\ &\approx N^{1.5} \cdot D\text{-}FOM\,(U_{\mathrm{dc}})\ . \end{aligned} \tag{2.26}$$

Relative to the 2L benchmark, and using the same output filter and applied volt-seconds, the ML topology enables a loss reduction of $N^{1.5}$ at the cost of $N^{1.5}$ larger die area. Note, that Eqs. **(2.22)-(2.26)** are also valid for the 2L case ($N = 1$), recalling that the ML derivation in this section is the generalization of the 2L bridge-leg.

2.4.1 X-FOM of Commercial Devices

With the Figures-of-Merit for ML bridge-leg configurations defined, commercial semiconductors can numerically be compared for an example application and the broader implications of the D-FOM and X-FOM can be considered.

For a tangible comparison, the case of a grid-interfaced PV inverter is taken, assuming $U_{dc} = 800\,V$ bus voltage and, to include a reasonable voltage margin, a device voltage rating of 1200 V for a 2L base case scenario.

In **Fig. 2.9**, the improvement when moving from a 2L with 1200 V SiC MOSFETs to the 7L case with 200 V GaN HEMTs is highlighted, where the X-FOM improves by a factor of $N^{1-\alpha_{\text{D-FOM}}} = N^{1.2} \approx 9$ for the 7L configuration, as shown in **Fig. 2.9**, and the semiconductor bridge-leg losses will decrease by the same factor for a fixed voltage-time product applied to the inductor. This massive reduction in semiconductor losses may enable the designer to eliminate a forced cooling system (fan and heatsink) and realize other system improvements [50, 71]. Recognizing, however, that improvements in power density may also be desired, the assumption of a fixed $L_o \Delta i_L$ is relaxed in the following section to explore the X-FOM-predicted system-level benefits of the ML topology.

2.5 Case Study & Experimental Verification

To this point, an extended FOM, X-FOM, has been defined, which can be applied to ML bridge-legs to determine the performance of the switching stage. Using the X-FOM, it has been identified that ML topologies can lead to higher performance, both because of the higher D-FOM of lower voltage devices and the switching frequency multiplication with smaller voltage steps that results from the nature of ML structures. To highlight the powerful topology analysis provided by the X-FOM, and how this can be translated into a quantifiable increase in performance, a case study is presented, analyzed, and validated with experimental results.

2.5.1 Case Study Definition

The analyzed system consists of the inverter stage of a grid-connected three-phase PV inverter, like the one highlighted in **Fig. 2.10a**. The key nominal characteristics are a rated power of 10 kW, a DC-link voltage of 800 V, and an RMS grid interface voltage of 400 V_{rms} (line-to-line).

In this context, two different bridge-leg configurations are considered for each of the three phases:

- 2L bridge-legs featuring 1200 V semiconductor technology (**Fig. 2.10b**), and,

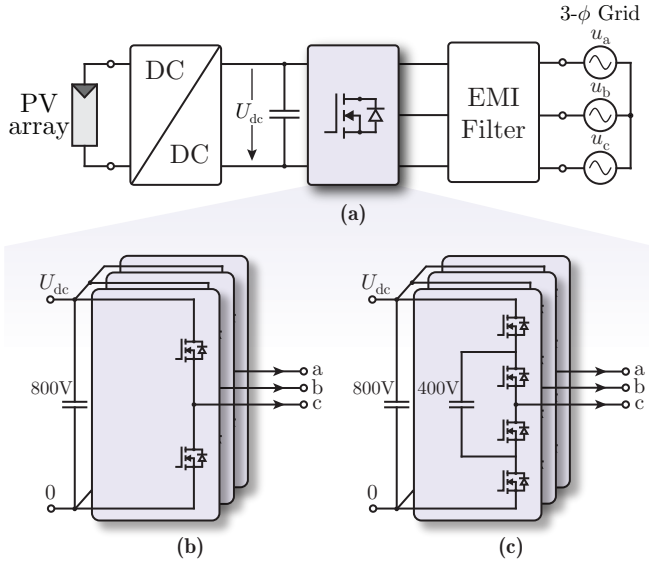

Fig. 2.10: (a) Example use case for the efficiency-optimized bridge-legs considered here, shaded in blue, which are part of the DC-AC conversion stage in a three-phase, grid-connected photovoltaic (PV) array with an 800 V DC-link (U_{dc}) and a 400 V_{rms} line-to-line grid voltage. **(b)** 2L bridge-leg configuration that can use 1200 V-rated switches, and **(c)** 3L FCC bridge-leg configuration that can feature switches rated for 600-650 V.

- 3L FCC bridge-legs featuring 600-650 V semiconductor technology (**Fig. 2.10c**).

A state-of-the-art commercially-available SiC MOSFET is selected for the implementation of each of these configurations, respectively:

- 1200 V 32 mΩ SiC device, and,
- 650 V 27 mΩ SiC device.

The key characteristics of these switches are shown in **Table 2.4**. As **Fig. 2.8** shows, 650 V GaN HEMTs have a similar D-FOM to the selected 650 V SiC MOSFET, but for a direct comparison on an X-FOM basis, two devices from the same technology class are preferred – i.e., without commercial 1200 V GaN HEMTs available, 650 V SiC MOSFETs are chosen for the comparison instead of a GaN HEMT. However, with the similar D-FOM (cf., **Fig. 2.8**),

Tab. 2.4: Nominal characteristics of the two selected devices. All values are given for 25 °C and for the switched voltage U_{sw}.

Num. Levels	Tech.	U_{rated}	Manuf.	Part Number	U_{sw}	R_{on}	$C_{oss,Q}$	Q_{oss}	$Q_{oss}U_{sw}$	*D-FOM*	*X-FOM*
2-Level	SiC	1200 V	*Wolfspeed*	C3M0032120K/D	800 V	32 mΩ	249 pF	199 nC	160 uJ	10.7 $\sqrt{\text{GHz}}$	10.7 $\sqrt{\text{GHz}}$
3-Level (ML)	SiC	650 V	*Infineon*	IMZA65R027M1H	400 V	27 mΩ	367 pF	147 nC	59 uJ	9.5 $\sqrt{\text{GHz}}$	19.0 $\sqrt{\text{GHz}}$

many of the conclusions drawn will be directly transferable to 600/650 V GaN HEMTs.

For the following analysis, a balanced three-phase grid is assumed, where each one of the three phases processes, on average, the same power. Therefore, without loss of generality, the analysis can focus on only one of the phases and/or bridge-legs, under the premise that it processes one third of the rated power (3.3 kW).

2.5.2 Using the X-FOM to Trade-Off Semiconductor Efficiency and Power Density

Until now,the case where $L_o \Delta i_L$ is held constant across different numbers of levels has been explored, and the aim has been to minimize the semiconductor stage losses. By relaxing this constraint, however, a second degree of freedom can be introduced to the converter design space that leverages the advantages of ML topologies.

To explore this design space [72], Eq. **(2.23)** that describes the minimum (conduction + switching) semiconductor losses $P_{\text{semi,min}}$ can be rewritten with **(2.19)** and **(2.21)** as a function of the voltage-time product $L_o \Delta i_L$:

$$P_{\text{semi,min}}\big|_{\text{ML}} = \frac{I_{\text{rms}} U_{\text{dc}}^{1.5}}{\sqrt{L \Delta i_L} \cdot X\text{-}FOM(U_{\text{dc}}, N)}. \tag{2.27}$$

With this loss-minimized equation that now includes the filter stress as $L_o \Delta i_L$, the potential performance gains of the bridge-leg and the filter stress in turn can be analyzed.

P_{semi} Reduction

With the same filter and same filter inductor stresses $L_o \Delta i_L$ for the 3L and 2L case, the difference between the minimum achievable losses of a system with the *same voltage-time product* ($L_o \Delta i_L$) is:

$$\frac{P_{\text{semi,min,3L}}}{P_{\text{semi,min,2L}}} = \frac{X\text{-}FOM_{\text{2L}}}{X\text{-}FOM_{\text{3L}}} = 0.56 \tag{2.28}$$

The vertical arrow in **Fig. 2.11a** represents this improvement – an increase in X-FOM (cf., **Table 2.4**) directly translates into a 44 % reduction in the minimum achievable semiconductor losses.

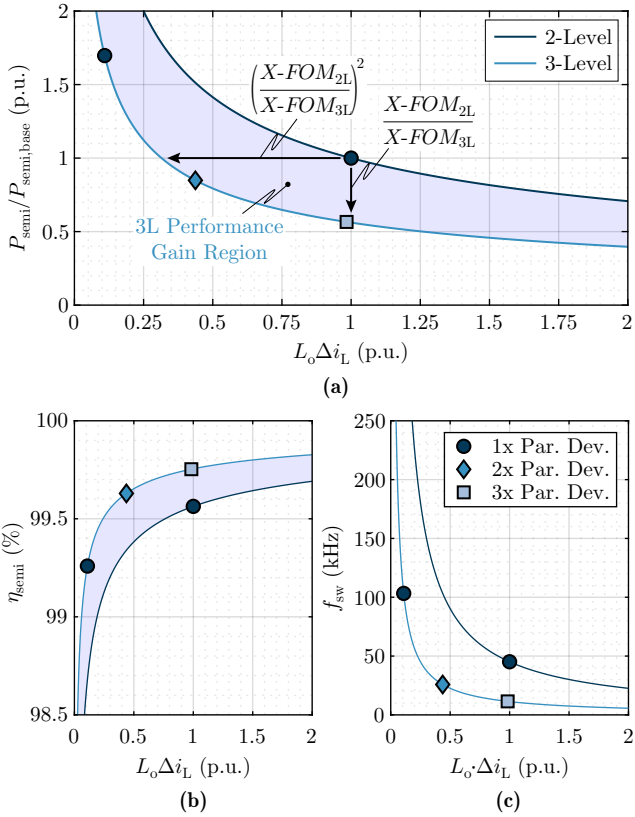

Fig. 2.11: Axes and tradeoffs of performance gains from increasing the X-FOM from a 2L to a 3L FCC bridge-leg: **(a)** semiconductor (conduction + switching) losses normalized to the 2L case, **(b)** semiconductor-stage efficiency, and switching frequency **(c)** vs. $L_o\Delta i_L$. The X-FOM values are taken from **Table 2.4**, and all values are calculated for rated power (3.3 kW) assuming a junction temperature of 75 °C. The ● represents that one single device (of the 1200 V 32 mΩ SiC device for the 2L case and of the 650 V 27 mΩ SiC device for the 3L case) is the optimum for that operating point, the ♦ represents that two paralleled devices (twice the die area) are optimal, and the ■ represents that three paralleled devices are optimal for the respective operating point.

Filter $L_o\Delta i_L$ Reduction

On the other hand, the bridge-leg losses could be held constant and it can be sought to miniaturize the filter by taking advantage of the $L_o\Delta i_L$ reduction [52].

In this case, the ratio of $L_o \Delta i_L$ between converter topologies and/or device technologies is given by the square of the inverse of the X-FOM:

$$\frac{(L_o \Delta i_L)_{3L}}{(L_o \Delta i_L)_{2L}} = \left(\frac{X\text{-}FOM_{2L}}{X\text{-}FOM_{3L}} \right)^2 = 0.32 \tag{2.29}$$

In **Fig. 2.11a**, this is represented by the arrow pointing to the left, where the voltage-time product is reduced by 68 % for the improvement in X-FOM between the considered 2L and 3L bridge-legs. For the same current ripple, then, the inductance can be reduced, or vice-versa, or some combination of both. The consequences of reducing $L_o \Delta i_L$ are comprehensively shown in [52], where, with fixed semiconductor losses among 2L, 3L and 7L bridge-legs, the passive component volume decreases by 65 % (3L) and 89 % (7L) relative to the 2L bridge-leg.

Combined P_{semi} and $L_o \Delta i_L$ Performance Gain

Finally, the shaded areas in **Fig. 2.11** focus on this combined improvement design space. In the highlighted "Performance Gain Region", the designer can use the knob of switching frequency to select any combination of bridge-leg improvement and filter size and/or efficiency improvement. Although the D-FOM is lower for the 3L case than for the 2L case (9.5 $\sqrt{\text{GHz}}$ vs. 10.7 $\sqrt{\text{GHz}}$, respectively, cf., **Table 2.4**), it features a nearly 2× higher X-FOM, explaining the resulting "Performance Gain Region" in **Fig. 2.11**. These significant gains in semiconductor losses and filter stress are entirely driven by the topology advantage – the 3L bridge-leg device has a slightly *worse* D-FOM than the SiC MOSFET for the 2L design, and therefore does not benefit from the typical gains of moving to lower-voltage devices (cf., **Fig. 2.8**).

It is reiterated here that the performance gain region is valid for the case in which the optimal die area (or number of parallel devices) is always chosen. However, since only discrete devices are available from power semiconductor manufacturers, **Fig. 2.11** also shows where one, two, and three parallel 650 V 27 mΩ SiC devices (resulting in an equivalent R_{on} of 27 mΩ, 13.5 mΩ and 9 mΩ, respectively) are the optimal choice vs. the benchmark case of one single 1200 V 32 mΩ device for the 2L bridge-leg.

For the benchmark 2L bridge-leg, one single 1200 V 32 mΩ device is the optimal choice at f_{sw} = 46 kHz. For the 3L bridge-leg, one single 650 V 27 mΩ device is optimal at f_{sw} = 103 kHz, two parallel devices are optimal at f_{sw} = 26 kHz, and three parallel devices are optimal at f_{sw} = 11 kHz, as seen in **Fig. 2.11c** (the relationship between f_{sw} and $L_o \Delta i_L$ is given in Eq. **(2.20)**). If the

goal is to minimize the filter stresses, the 3L design should be realized with one single 650 V 27 mΩ device switching at f_{sw} = 103 kHz. If the goal is instead to halve the semiconductor losses while maintaining a similar or identical filter, then the design should be realized with three parallel-connected 650 V 27 mΩ devices switching at f_{sw} = 11 kHz. (Note that here it is always referred to the individual device switching frequency (f_{sw}), and not the effective switching frequency (f_{eff}), cf., Eq. **(2.18)**.)

Finally, the X-FOM can be used to identify the maximum achievable efficiency of the semiconductor stage of a hard-switched bridge-leg, shown in **Fig. 2.11b** at the rated power. The efficiency of the bridge-leg, considering only the semiconductor losses, is calculated as:

$$\eta_{semi} = \frac{P_{in} - P_{semi}}{P_{in}} = 1 - \frac{P_{semi}}{P_{in}}\,, \tag{2.30}$$

where P_{in} is the input power.

2.5.3 Adding Measured Switching Losses to the X-FOM Theory

Thus far, with both the D-FOM and the X-FOM, only the conduction losses and the capacitive hard-switching losses have been accounted for, which are the minimum losses that can occur in a hard-switched bridge-leg ($E_{sw,min} = U_{sw}Q_{oss}$) [44]. As a final step towards validating the efficacy of the X-FOM concept in predicting the performance of different bridge-leg structures, the measured switching losses instead of the minimum theoretical hard-switching losses are now included.

To obtain accurate switching loss data, the calorimetric switching loss measurement method presented and validated in [65, 73, 74] is used. In this method, the switches are mechanically attached and thermally coupled to a brass block. By measuring the time required to increase the brass block temperature by a given amount (e.g., ΔT = 10 °C), and by subtracting the conduction losses (R_{on} of the devices under test is measured with varying temperature during the calibration), the semiconductor switching losses can be extracted.

The measured losses for the 1200 V 32 mΩ SiC devices in both 3-pin and 4-pin TO-247 packages are presented in **Fig. 2.12a**, and the measured hard-switching losses for the 650 V 27 mΩ SiC device in a 4-pin TO-247 package are presented in **Fig. 2.12b**, for an average junction temperature of 129.5 °C (±10 °C) and 91.5 °C (±10 °C), respectively (to guarantee the accuracy of the

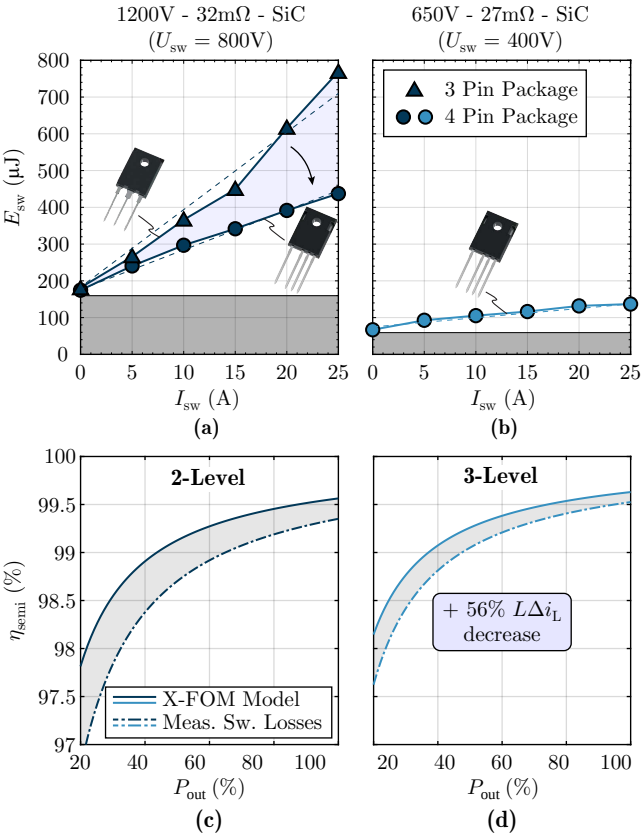

Fig. 2.12: (a-b) Measured switching losses (hard + soft transition) of the 1200 V and 650 V devices, respectively, given in **Table 2.4**. In **(a-b)**, the area shaded in grey represents the share of switching losses accounted for in the X-FOM calculations, i.e., the minimum hard-switching losses of $Q_{oss}U_{sw}$, and the dashed lines show the linearization of the switching losses (cf., Eq. **(2.31)** and **Table 2.5**). In **(c)** and **(d)** the bridge-leg semiconductor efficiency is shown for the X-FOM model **(2.23)** and with the measured switching losses for the 2L and 3L bridge-leg cases in 4-pin packages, respectively. The 2L bridge-leg uses one parallel device ((●) in **Fig. 2.11**) and the 3L case uses two parallel devices per switch ((⧫) in **Fig. 2.11**).

switching loss measurements by ensuring that the switching losses are always larger than the conduction losses [64], for the 1200 V devices, a larger brass

block is needed [73] and correspondingly higher losses have to be generated leading to a slightly higher junction temperature). The employed gate drivers are the 1EDI60I12AF from *Infineon*, and all of the measurements were taken with 0 Ω (both turn-on and turn-off) external gate resistances. Since 4-pin devices feature a Kelvin source connection, the current dependence of the switching losses is drastically reduced relative to the 3-pin devices that don't feature a dedicated Kelvin source contact [75]. This can be clearly seen in **Fig. 2.12a**, where for the same MOSFET the 3-pin device shows (for example, at 25 A) 64 % higher losses than the 4-pin device. Therefore, the measurements on the 4-pin package are used for the losses of the 1200 V device, and the switching loss reduction from a 3-pin to a 4-pin package is revisited at the end of this section.

Nevertheless, the switching losses in **Fig. 2.12a-b** still feature a current dependent term, which can be modelled with a first order polynomial (linear) curve [9]:

$$E_{\mathrm{sw}}(I_{\mathrm{sw}}) = k_{\mathrm{sw,o}} + k_{\mathrm{sw,1}} I_{\mathrm{sw}} \ . \tag{2.31}$$

The first term, $k_{\mathrm{sw,o}}$, is current-independent (but die area-dependent) and is described by Eq. **(2.5)** as $k_{\mathrm{sw,o}} = C_{\mathrm{oss,Q}}(U_{\mathrm{dc}})U_{\mathrm{dc}}^2$. The second term, $k_{\mathrm{sw,1}}$, describes the linear dependence of switching losses on the current ($V - I$ overlap losses), can be empirically measured, and depends on different factors that limit the switching speed such as the turn-on gate resistance, gate voltages, and gate loop inductance (including the common source inductance, the effect of which can be reduced if the device features a Kelvin connection, cf., **Fig. 2.12a-b** and **Table 2.5**), as well as on the reverse recovery charge of the (parasitic) body diodes [76, 77]. Assuming that the current splits equally among N_{par} paralleled devices and considering Eq. **(2.31)**, then the switching

Tab. 2.5: First order polynomial coefficients for devices in **Fig. 2.12a-b** resulting from a polynomial fit according to Eq. **(2.31)**.

	1200 V - 32 mΩ		650 V - 27 mΩ
	3-pin	4-pin	4-pin
$k_{\mathrm{sw,o}}$ [µJ]	180.0	176.6	76.4
$k_{\mathrm{sw,1}}$ [µJ/A]	21.0	10.9	2.7

losses are:

$$E_{\mathrm{sw}}(I_{\mathrm{sw}}, N_{\mathrm{par}}) = N_{\mathrm{par}} \left(k_{\mathrm{sw,o}} + k_{\mathrm{sw,1}} \frac{I_{\mathrm{sw}}}{N_{\mathrm{par}}} \right) = N_{\mathrm{par}} k_{\mathrm{sw,o}} + k_{\mathrm{sw,1}} I_{\mathrm{sw}} \,, \tag{2.32}$$

where $N_{\mathrm{par}} = A_{\mathrm{die}}/A_{\mathrm{die,base}}$, with $A_{\mathrm{die,base}}$ as the benchmark die area for which $k_{\mathrm{sw,o}}$ and $k_{\mathrm{sw,1}}$ have been parameterized. It is seen that the linear term of the equation does (ideally) not depend on the die area or number of parallel-connected devices. In other words, one can switch, for example, one device with 25 A or two devices with 12.5 A each, the latter with larger constant (capacitive) losses but equal current-dependent losses. Note that a linear fit is also adequate for GaN devices, as shown e.g., in [78] for 600 V devices and in [65] for 200 V devices, as well as e.g., for 200 V Si devices [65]. Hence, when writing the semiconductor losses as in Eq. **(2.8)** and deriving the optimal die area $\left(\frac{\mathrm{d}P_{\mathrm{semi}}}{\mathrm{d}A_{\mathrm{die}}} = 0 \right)$, the linear part of the switching losses has no effect on the optimal die area, but it does influence the absolute value of the losses, which will be larger when the current dependence of the switching losses is included.

This is highlighted in **Fig. 2.12c-d**, where the calculated semiconductor efficiency over output load of a 2L bridge-leg with *one* parallel device is shown in comparison to a 3L bridge-leg with *two* parallel devices (as detailed in **Fig. 2.11** and **Table 2.4**). In both cases, the predicted peak semiconductor efficiency at rated load matches those shown in **Fig. 2.11b**, where the 2L bridge-leg should reach 99.56 % and the 3L bridge-leg 99.63 %. When the measured switching losses are added, the peak efficiency is reduced to 99.35 % and 99.53 %, respectively, leading to a 0.21 % and 0.10 % deviation between the X-FOM model and the actual losses. This difference arises because the X-FOM only includes the minimum hard-switching losses, providing a minimum boundary for the losses (and identifying the maximum bridge-leg performance). The linear switching loss term only provides a loss offset that shifts the efficiency curve downwards (**Fig. 2.12c-d**) but, does not influence the optimal die area selection. Finally, note that the larger deviation in the 2L efficiency curves in **Fig. 2.12c-d** originates from the linear switching loss term, which is larger in the 1200 V devices than in the 650 V devices (**Fig. 2.12a-b**).

In the end, even with the measured switching losses, the 3L structure achieves both a 0.18 % semiconductor efficiency increase (a 27 % decrease in loss fraction) and a 56 % $L_{\mathrm{o}}\Delta i_{\mathrm{L}}$ decrease, which, according to [52], would reduce the inductor volume by approximately the corresponding fraction.

In this case study, the X-FOM identified the performance improvement for the PV inverter semiconductor stage when moving from a 2L bridge-leg to a 3L bridge-leg. By using the X-FOM approach, the relative gains that are expected in terms of semiconductor losses and filter stress can be calculated, the maximum achievable efficiency of the semiconductor stage is identified for both cases, and the optimal combinations of switching frequency and number of parallel devices are obtained. Although additional losses that occur surrounding the bridge-leg losses in a full converter system (e.g., magnetics, flying capacitors (FCs), clamping diodes) are not directly considered, with the X-FOM an advantage in terms of the switching losses, the filter stress, or a combination of both by moving from a 2L to a 3L bridge-leg structure is clearly identified. Finally, by including the switching loss measurements, the X-FOM-predicted performance gain of the 3L bridge-leg (relative to the 2L structure) is validated, where it is confirmed that there is no region in the switching loss and filter stress performance space where the 2L outperforms the 3L structure (even when using devices with a higher D-FOM for the 2L bridge-leg).

2.5.4 Future Challenges of WBG Devices

One of the largest challenges identified with the X-FOM – setting aside technology specific issues like the reverse recovery charge for Si and SiC MOSFETs [79] and dynamic R_{on} for GaN HEMTs [80] – is the need for the development of advanced semiconductor packaging solutions. From **Fig. 2.12a** it becomes clear that the efficiency difference between the X-FOM-predicted efficiency and the real efficiency can be reduced by simply adding a Kelvin connection [75]. As semiconductor technology has improved (and especially with the faster switching speed provided by WBG devices [81, 82]), better device packages with reduced parasitics that increase switching performance and reduce overvoltages [76, 77, 83] have become available (e.g., devices with planar bond wires [84] or direct PCB connection [85, 86] for SiC devices and surface-mounted devices for GaN HEMTs [87]). With the integration of the gate driver circuitry, as shown in **Fig. 2.13**, into both lower-voltage (< 200 V) [88,89] and higher-voltage semiconductors (> 600 V) [90,91] (which leads to lower parasitic inductances L_g and L_s, higher power density, reduced component count, lower system complexity, and lower cost [92, 93]), there is the potential to further reduce current-related switching losses. With these developments, the X-FOM approach becomes an increasingly valuable tool to

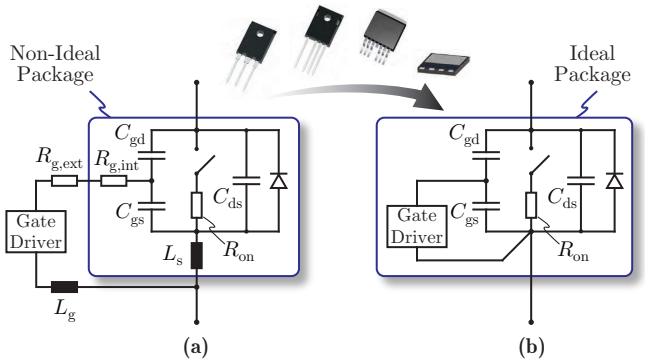

Fig. 2.13: (a) Gate driver, power semiconductor package and model of a voltage-controlled switch with the main parasitics that influence the switching transients, and **(b)** the idealization of the gate driver and semiconductor packaging that reduce the inevitable parasitic elements. L_g is the gate driver loop inductance, $R_{g,ext}$ the external gate resistance, $R_{g,int}$ the internal MOSFET gate resistance and L_s the common gate-source inductance.

quantify both the relative and absolute performance of a certain combination of semiconductor and topology.

2.6 Summary

By applying fundamental principles to model the conduction and switching losses of hard-switched semiconductor bridge-legs, a device Figure-of-Merit, D-FOM, is derived and extended to the X-FOM. While the D-FOM only refers to the performance of an individual semiconductor device, the X-FOM quantitatively compares the performance of individual devices of all voltage ratings across a number of topologies, with a particular focus on ML structures here. The X-FOM is a simple-yet-powerful metric to evaluate the performance of the semiconductor stage of a system. It identifies, among others,

- the performance gain that can be obtained either in semiconductor stage losses and/or in the filter design requirements,
- the maximum efficiency that can be achieved by the semiconductor stage by selecting the loss-optimal die area for each frequency, and

- the loss-optimal die area (or number of parallel devices) for each switching frequency.

Furthermore, the X-FOM reveals the underlying enablers behind the higher efficiency and/or reduced filter size of ML converters, and provides a simple tool to quantify these two parameters. This is shown by applying the X-FOM to a case study where the semiconductor stage performance of a three-phase PV inverter is analyzed, in which it is shown that the 3L bridge-leg offers superior performance to its 2L counterpart on both power semiconductor loss and filter stress – despite using fundamentally lower-performance devices. This is further validated by adding measured switching loss data to the X-FOM theory and analysis.

Finally, the X-FOM also identifies the remaining performance gap between the losses of *ideally*-packaged power semiconductors and *real* commercial ones. This reaffirms the X-FOM as a valid performance metric for future power electronics converters, where devices with switching losses close to the theoretical minimum are expected to become increasingly available.

3

Multi-Level Topology Evaluation for Ultra-Efficient Three-Phase Inverters

This chapter summarizes the most relevant findings concerning the comparative evaluation of multi-level converter topologies targeting the realization of compact ultra-efficient three-phase PV inverter systems also published in:

- **J. Azurza Anderson**, M. Leibl, L. Schrittwieser, J. W. Kolar, "Multi-level topology evaluation for ultra-efficient three-phase inverters," in *IEEE Proc. of the International Telecommunications Energy Conference (INTELEC)*, Broadbeach, Australia, 2017.

Motivation

With the semiconductor scaling laws defined for multi-level converters, this chapter evaluates different topologies across several numbers of levels in order to identify the concept which offers the most compact realization of a three-phase PV inverter targeting 99.5 % efficiency.

Executive Summary

ML topologies reduce the requirements on inductors and filters, while at the same time allowing to reduce the semiconductor losses. However, given the large number of possible topologies and numbers of levels, it is still unclear what combination of both is the best option to achieve ultra-high efficiency while maintaining a reasonable power density. For this purpose, an extensive quantitative evaluation of different topologies is carried out to determine the required volume for a targeted 99.5 % efficiency of a 10 kW three-phase inverter. This includes the EMI filter stage, where contrary to the conventional common-mode (CM) noise AC-side filtering, an alternative CM filter placement on the DC-side is proposed to save losses. With an evaluation of ML topologies, it is shown that even if a high number of levels can reduce the size of the magnetic components by an order of magnitude, the volume and losses of the capacitive components required to create the ML voltage output have to be considered. The performance of topologies ranging from 2L to 7L bridge-legs are quantitatively evaluated, and detailed conceptual 3D CAD designs of the 3L T-type and 7L Hybrid Active Neutral Point Clamped (HANPC) converters are presented to validate the initial results, achieving a relatively high power density of 2.2 kW/dm³ and 2.7 kW/dm³ respectively.

3.1 Introduction

In the previous chapter, semiconductor properties were analyzed together with ML bridge-leg structures, allowing for a fundamental understanding of the main performance benefits of switching from conventional 2L approaches to ML converters. However, this analysis excluded the influence of what can be considered *hidden* filter elements, i.e., the FCs, in the overall volume and losses. Regarding the FCs, particular attention has to be given not only to the volume of the capacitors themselves, but also to the impact that they have in the converter design, by e.g., influencing the size and layout of the PCB. Therefore, it is still unclear whether the ML performance gain predicted by the X-FOM finally translates to a more compact design of an ultra-high efficiency three-phase PV inverter compared to a 2L approach.

In order to find out which topology and number of levels (cf., **Fig. 3.1**) is the most suitable for achieving the 99.5 % efficiency target, the topic of this chapter is to quantitatively analyze and compare, on the one hand, conventional 2L and 3L topologies, where the interleaving of 2L bridge legs is also considered (which achieves a 3L characteristic), and on the other hand, the ML approaches of the FCC and a hybrid topology that merges an active neutral point clamped stage with an FC stage, named hereafter Hybrid Active Neutral Point Clamped

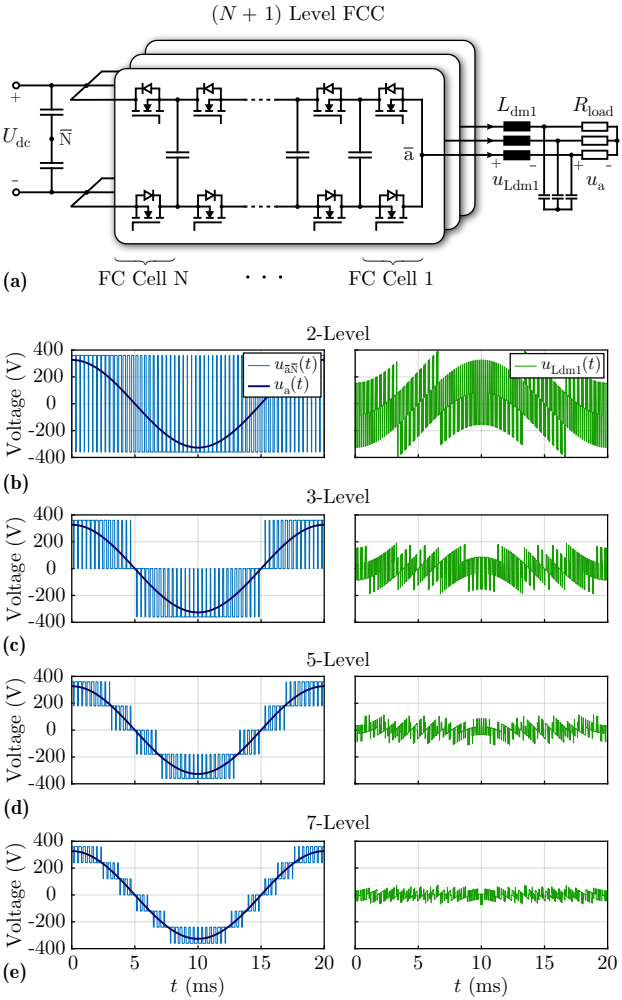

Fig. 3.1: (a) A three-phase (N+1) level FCC, with N FC stages. **(b-e)** FCC output node voltage referenced to the DC-link midpoint $u_{\overline{aN}}(t)$ and the filtered output voltage $u_a(t)$ (left), and the first stage differential-mode (DM) inductor voltage (right) considering a CM filter or a floating neutral point of the load. Note, that for a clear representation, the switching frequency is chosen for each case such that the effective frequency of the voltage waveform applied to the inductor is only 3 kHz.

Tab. 3.1: Three-phase system specifications.

Efficiency Target	99.5 %
P_{nominal}	10 kW
$P_{\text{rated,max}}$	12.5 kW
$U_{\text{dc,nominal}}$	720 V
$U_{\text{ac,ll,rms}}$	400 V_{rms}
f_{mains}	50 Hz
EMI Filter Requirement	Class A

(HANPC) converter [94]. In **Section 3.2** the evaluated topologies to reach the given efficiency target are introduced, followed by **Section 3.3**, where the framework and results of the topology comparison are shown. Then, detailed 3D CAD models of the 3L T-type converter and the 7L-HANPC converter with the corresponding loss and volume distributions are presented in **Section 3.4** to validate these preliminary calculations. Finally, in **Section 3.5** the main results of the chapter are summarized.

3.2 Evaluated Topologies

The considered topologies for the comparative evaluation to achieve the efficiency target of 99.5 % for a 10 kW three-phase PV inverter are presented in **Fig. 3.2**, and will be discussed in detail. The full system specifications for the comparative evaluation are given in **Table 3.1**.

3.2.1 Two- and Three-Level Bridge-Legs

2L and 3L bridge-legs are the conventional solutions for three-phase converters [95–97]. In this context, the following converters are chosen for comparison:

(a) *2L bridge-leg* (shown in **Fig. 3.2a**): requires semiconductors in the 1200 V range in order to block the full DC-link voltage.

(b) *2L 2×interleaved bridge-legs* (shown in **Fig. 3.2b**): offers a 3L output voltage $u_{\overline{aN}}(t)$ at twice the switching frequency of the individual 2L bridges by inserting an additional magnetic component, i.e. a coupling inductor (CI) [98–100].

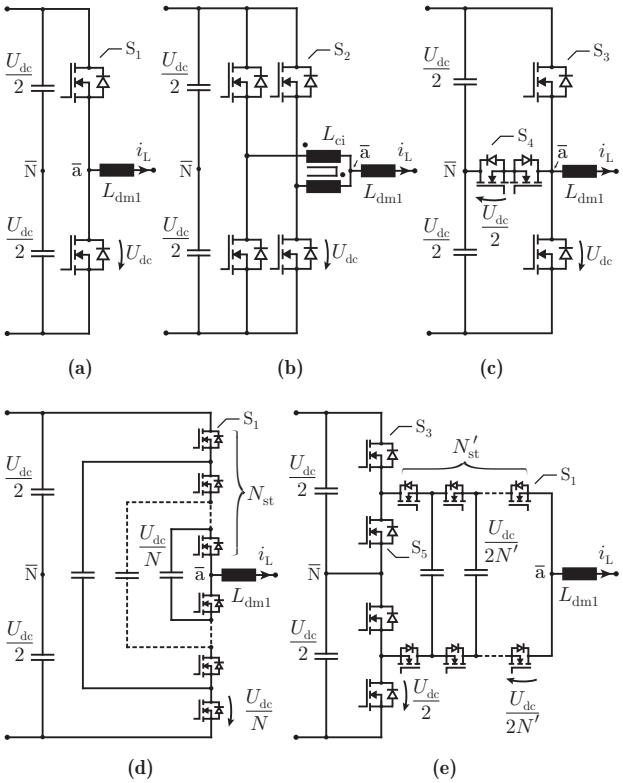

Fig. 3.2: Bridge-leg topologies considered in the evaluation, shown for a single phase. **(a)** 2L converter, **(b)** 2L interleaved converter with a CI, **(c)** 3L T-type converter, **(d)** $(N+1)$-level FCC and **(e)** $(2N'+1)$-level HANPC converter.

(c) *3L T-type bridge-leg* (shown in **Fig. 3.2c** [101]): the third level is achieved by inserting two additional switches connected to the midpoint, which advantageously only have to block (and consequently, switch) half of the DC-link voltage. However, T-type bridge-legs do not offer any switching frequency multiplication, unlike FCCs.

Note, that for the 3L bridge-leg implementation, active neutral point clamped (ANPC) converters would also be possible, but due to the increased component count and proven performance of the T-type topology [101, 102], they were not included in the comparison at hand.

3.2.2 ML Bridge-Legs

To assess the potential of ML converters for high-efficiency applications, two topologies are selected: the FCC and the HANPC bridge-legs (cf., **Fig. 3.2(d,e)**), respectively.

(d) *FCC* (shown in **Fig. 3.2d** [51]): as a main feature all of the switches are rated to block the same voltage, namely $\frac{U_{\mathrm{dc}}}{N}$, where N is the number of series-connected switches, and $N+1$ is the number of levels. The FCCs achieve a ML output voltage waveform and an effective switching frequency multiplication by series connecting capacitors, as opposed to the bridge-leg interleaving approach in **(b)**, where the same is achieved with magnetic components.

(e) *HANPC converter* (shown in **Fig. 3.2e**): is realized with a combination of an ANPC front-end with semiconductor devices that block $\frac{U_{\mathrm{dc}}}{2}$ and are switched at mains frequency (50/60Hz), followed by a FC stage comprised of switches that have to be rated for $\frac{U_{\mathrm{dc}}}{N}$. Since the switching frequency of the ANPC devices is typically two-or-more orders of magnitude lower than the operating frequency of the switches of the FC stage, the switching losses of the ANPC stage can safely be neglected, and the stage can be realized therefore with a large die area to reduce conduction losses.

Both of these bridge-legs are expandable to a higher number of levels, by adding additional FC stages. In the comparative evaluation at hand, the FCC is considered for 3L, 5L and 7L, whereas the HANPC converter is considered for 5L and 7L. The choice of the levels is taken in accordance to the semiconductor availability, since for instance the lack of competitive MOSFETs in the 350-400 V range directly rules out a 4L solution for the FCC. Finally, note that although a combination of ML and bridge-interleaving in not considered in this work, this analysis has been performed in e.g., [78], with the goal of achieving an ultra-high bandwidth (>100 kHz) power amplifier in the kW power range.

3.3 Topology Comparison Methodology and Results

In this section, the models used to quantify the losses and the volume of the converter will be discussed.

3.3.1 Semiconductor Loss Modeling

The semiconductor loss modeling follows the principles presented in **Chapter 2**, where according to the high efficiency target, paralleling switches has to be considered in order to find the loss-optimal die area of the semiconductors. With the target of achieving an ultra-efficient converter, which typically leads to semiconductor stage designs switching at low frequencies with large die areas or a large number of parallel switches (cf., **Fig. 2.11**) [9, 66] where the majority of switching losses arise from the capacitive hard-switching loss component (cf., **Fig. 2.12**), the switching losses of a switch pair that receives complimentary gate signals or of a FC cell (cf., **Fig. 3.1a**) are modeled as:

$$\begin{aligned} P_{\mathrm{sw}} &= N_{\mathrm{par}} f_{\mathrm{sw}} Q_{\mathrm{oss}}(U_{\mathrm{n}}) U_{\mathrm{n}} + f_{\mathrm{sw}} Q_{\mathrm{rr}}(I_{\mathrm{sw,avg}}) U_{\mathrm{n}} \\ &= N_{\mathrm{par}} f_{\mathrm{sw}} C_{\mathrm{oss,Q}}(U_{\mathrm{n}}) U_{\mathrm{n}}^2 + f_{\mathrm{sw}} Q_{\mathrm{rr}}(I_{\mathrm{sw,avg}}) U_{\mathrm{n}} \,, \end{aligned} \tag{3.1}$$

where N_{par} is the number of switches in parallel, f_{sw} is the switching frequency of each device, U_{n} is the switched voltage, $Q_{\mathrm{oss}}(U_{\mathrm{n}})$ is the voltage dependent output capacitance charge of the switch, $C_{\mathrm{oss,Q}}(U_{\mathrm{n}})$ is voltage dependent charge equivalent output capacitance of the switch, Q_{rr} the reverse recovery charge, and $I_{\mathrm{sw,avg}}$ the average switched current.

The reverse recovery losses are in a first step considered to be linear with the switched current and independent of the number of devices in parallel or the die area (for more details, see **Appendix D**).

The conduction losses of each switch are modeled as

$$P_{\mathrm{cond}} = I_{\mathrm{rms}}^2 R_{\mathrm{on}} / N_{\mathrm{par}} \,, \tag{3.2}$$

with the RMS current of the switch I_{rms} and the switch on-state resistance R_{on} . The RMS currents of all the switches considered in this evaluation (cf., **Fig. 3.2**) are found in **Table 3.2**,

3.3.2 EMI Filter Stage Design

For the comparative topology evaluation, a splitting of the EMI filtering into discrete DM and CM stages is considered (**Fig. 3.3**) [103], although this is then reevaluated in **Chapter 4**.

The first constraint that has to be fulfilled when defining the inductance and capacitance values of the EMI filter stages is the compliance with the CISPR 11 Class A standard (**Table 3.1**). This yields a minimum attenuation (Att) required to fulfill the quasi-peak and average limits, which typically

Tab. 3.2: The RMS currents for the different switches in **Fig. 3.2**, where the duty cycle is $d(t) = M \cdot \sin(\omega t) + M_3 \cdot \sin(3\omega t)$; M is the modulation index, M_3 is the amplitude of the superimposed third harmonic injection and $I_{\mathrm{ac,pk}}$ is the peak output current.

$I_{\mathrm{rms,S1}} = \frac{I_{\mathrm{ac,pk}}}{2}$
$I_{\mathrm{rms,S2}} = \frac{I_{\mathrm{ac,pk}}}{4}$
$I_{\mathrm{rms,S3}} = \frac{I_{\mathrm{ac,pk}}}{\sqrt{2}} \sqrt{\frac{4M}{3\pi} - \frac{4M_3}{15\pi}}$
$I_{\mathrm{rms,S4}} = I_{\mathrm{ac,pk}} \sqrt{\frac{1}{2} - \frac{4M}{3\pi} + \frac{4M_3}{15\pi}}$
$I_{\mathrm{rms,S5}} = \frac{I_{\mathrm{ac,pk}}}{\sqrt{2}} \sqrt{\frac{1}{2} - \frac{4M}{3\pi} + \frac{4M_3}{15\pi}}$

coincides with the first switching frequency harmonic above 150 kHz [44]. At the outset, the same values of the filter components for all the filter stages will be considered in order to achieve maximum attenuation ($L_{\mathrm{dm},k} = L_{dm}$ and $C_{\mathrm{dm},k} = C_{dm}$ for DM components and $L_{\mathrm{cm},k} = L_{cm}$ and $C_{\mathrm{cm},k} = C_{cm}$ for CM components) [104, 105]. In this case, the asymptotic attenuation provided by an N_{f} stage filter is given by $Att = (\omega T_{\mathrm{c}})^{(2N_{\mathrm{f}})}$, where $T_{\mathrm{c}} = \sqrt{LC}$ is the filter time constant of the individual stage. Additionally, a margin of 10 dBµV is included to consider tolerances of the components.

The second constraint that the EMI filter has to fulfill is to have resonance frequencies which are sufficiently separated from the (effective) switching frequency and its harmonics. For this, the filter cut-off frequency is chosen to be at maximum one fourth of the (effective) switching frequency, for which a minimum filter time constant remains, $T_{\mathrm{c,min}} = 4/(2\pi f_{\mathrm{eff}})$, where f_{eff} is the effective switching frequency. If the value of T_{c} obtained from the EMI compliance requirement is smaller than $T_{\mathrm{c,min}}$ (allowing, in theory, for a smaller filter realization should only the filter attenuation requirement be satisfied), then the filter time constant is set to $T_{\mathrm{c}} = T_{\mathrm{c,min}}$. For the topology comparison, the same filter time constant T_{c} is considered for all filter stages.

To determine the number of filter stages, the volume of capacitors and inductors are considered to be proportional to the stored energy, and hence, $\sum L$ and $\sum C$ should be minimized [104]. For filter stages limited by the cut-off

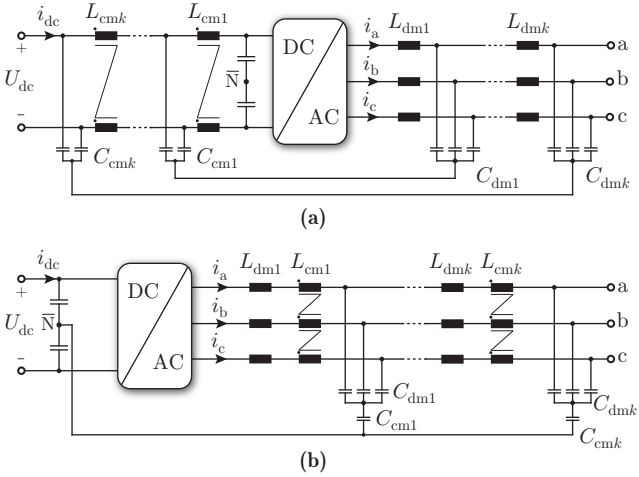

Fig. 3.3: (a) DC-side CM filtering, with capacitive feedback from the star-point of the DM capacitors to the positive and negative rail of the DC-link, and **(b)** AC-side CM filtering with capacitive feedback to the DC-link midpoint.

frequency ($T_{c,min}$), a minimum number of filter stages is desired for minimum volume, and hence, the number of filter stages N_f is determined by selecting the lowest number of filter stages that fulfill the required attenuation.

For the design of the DM filter, since the reactive power Q that a converter should process is limited (here $Q_{max} = 5\% P_{nominal}$ is considered), the total maximum DM capacitance value per phase is given by

$$C_{dm,tot,max} = \frac{Q_{max}}{2\pi f_{mains} U_{ac,ll,rms}^2}, \tag{3.3}$$

which yields then a minimum DM inductance value $L_{dm,min}$ for a given T_c. The output inductor L_{dm1} is then optimized for minimizing losses, with the constraint of achieving $L_{dm,min}$. For the inductor optimization, nanocrystalline cut-cores with helical windings are used, since they offer low core losses and high filling factor, and have been found suitable for applications with low current ripple [9, 66, 106].

DC-Side Common-Mode Noise Filtering

Seeking to save losses, the CM chokes can be placed on the DC-side (cf., **Fig. 3.3a**) instead of the AC-side (cf., **Fig. 3.3b**). Although the magnetic core losses for both configurations are equal (since the applied CM voltage generated by the converter is the same), the winding losses can be substantially reduced. By defining the modulation index as $M = \frac{U_{\mathrm{ac,pk}}}{U_{\mathrm{dc}}/2}$, where $U_{\mathrm{ac,pk}}$ is the peak output phase voltage (325 V), the relationship between the DC input current I_{dc} and the output RMS phase current $I_{\mathrm{ac,rms}}$ is given by

$$I_{\mathrm{dc}} = \frac{3M}{2\sqrt{2}} I_{\mathrm{ac,rms}}. \tag{3.4}$$

(the DC current i_{dc} is assumed approximately constant, $i_{\mathrm{dc}} \approx I_{\mathrm{dc}}$, as filter capacitors are placed at the input of the switching stage). For the same CM choke core size, where the total copper conductor cross section and average turn length are assumed to be the same for both a DC- and AC-side CM choke placement, the ratio of the low-frequency winding losses is

$$\frac{P_{\mathrm{w,dc}}}{P_{\mathrm{w,ac}}} = \frac{M^2}{2}\,, \tag{3.5}$$

which for the nominal operating point of the converter ($M = 0.904$) yields a minimum winding loss saving of 60 %. Additionally, the eddy current and proximity losses are negligible for the DC-side choke placement, since in steady-state balanced operation the only high-frequency current flowing through the windings is the CM current, which is in the order of tens or low-hundreds of milliamperes. However, if the CM choke is placed on the AC-side, it is subject to the same current ripple as the DM inductors L_{dm}, which in the case of, e.g., the first stage filter, can be considerable, leading to additional high frequency winding losses. For the design of the CM filter, the CM choke is also optimized for minimum losses. Finally, C_{cm} is adapted to satisfy the required attenuation for the CM noise.

3.3.3 Flying and DC-Link Capacitors

There are two additional sets of capacitors that have to be dimensioned. For the FCs, the minimum capacitance is defined by

$$C_{\mathrm{fc,min}} \geq \frac{I_{\mathrm{ac,pk}}}{N_{\mathrm{cell}}\, f_{\mathrm{sw}}\, \Delta U_{\mathrm{fc,max}}}\,, \tag{3.6}$$

where $N_{\text{cell}} = N$ for the FCC bridge-legs and $N_{\text{cell}} = N'$ for the HANPC bridge-legs, and $\Delta U_{\text{fc,max}}$ is the peak-to-peak switching frequency maximum voltage ripple of the FCs. For this work, $\Delta U_{\text{fc,max}}$ is set to a maximum of 5 V, which ensures a maximum switching frequency over-voltage on the switches of only 10 V during steady-state operation, which is low enough also for switches in the 200-250 V range that are operating in the vicinity of two thirds of their rated blocking voltage. Since the switching frequency imposed by the efficiency target is low, the required capacitance values are relatively large (tens of µF), and therefore, film capacitors are considered to be the most adequate option for the FCs. A detailed discussion on the suitability of ceramic capacitors for the realization of the FCs of ultra-high efficiency converters can be found in **Section 4.3** and **Appx. F**, but from a practical and cost point of view, finally only film capacitors are considered for the evaluation.

For the case of the DC-link capacitors, only the capacitance needed to filter the switching frequency ripple current is taken into account in the comparison. The minimum capacitance of the DC-link is determined by

$$C_{\text{dc,min}} \geq \frac{I_{\text{dc}}}{2 f_{\text{sw}} \Delta U_{\text{dc,max}}} \tag{3.7}$$

which is also limited for the comparison to $\Delta U_{\text{dc,max}} = 5\,\text{V}$. This limitation does not cover the low frequency (150 Hz) voltage ripple in the midpoint of the DC-link for the 3L T-type and the HANPC topologies, as this can be balanced by superimposing a third harmonic component to the modulation [105]. Neither is any additional capacitance for potential grid unbalances or single-phase operation considered.

3.3.4 Cooling and PCB Volume

To model the volume of the heat sink, a conservative cooling system performance index (CSPI) of $3\,\text{W/(K·dm}^3\text{)}$ is assumed [21]. For highly efficient systems, low CPSI values are obtained, firstly due to the large semiconductor area that has to be attached to the heat sinks (cf., **Fig. 3.5**), and secondly, because the selected fans are low power consumption fans, in the <1 W range. This CSPI value is additionally in accordance to the realized designs presented in **Fig. 3.5**. The maximum thermal resistance of the cooling system is set by the maximum temperature that the heat sink is allowed to reach. Taking 30 °C as the ambient temperature and 75 °C as the maximum allowable heat sink temperature (to limit MOSFET conduction losses) leads to the maximum

Tab. 3.3: Semiconductor devices used for the topology evaluation.

U_{rated}	Model	R_{on} (typ., 25 °C)	Technology
1200 V	C2M0025120D	25 mΩ	SiC
650 V	SCT3022AL	22 mΩ	SiC
250 V	IPB200N25N3	17.5 mΩ	Si
200 V	EPC2034	7 mΩ	GaN

thermal resistance from the heat sink to the air to be between 2.2 K/W for the 2L interleaved converter (with the lowest semiconductor losses) and 1.4 K/W for the 7L-HANPC converter (that has the maximum semiconductor losses). This finally yields the minimum volume of the cooling system to be between 0.15 dm^3 and 0.24 dm^3, which is assumed to be proportionally distributed over the semiconductor area for the volume computation of the comparison. When considering the boxed volume of converters, the volume of the PCB with all components on it (e.g., control board, current sensors and connectors) is taken into account, for which the footprint of the main power components is modeled and a 15 mm height offset is included for calculating the PCB volume.

3.3.5 Auxiliary Losses

Part of the total converter loss budget, which is 50 W for the 99.5 % efficiency target at 10 kW, has to be reserved for additional power losses in the converter (P_{others}). These loss components include controllers, gate driver losses, PCB conduction and connector losses, etc., and all of these are estimated to be around 12 W [9,66]. Hence, in order to account for these losses in the topology evaluation, $P_{\text{others}} = 12.5\,\text{W}$ (25 % of the loss budget) are reserved for this purpose.

3.3.6 Comparison of Results

The results of the topology evaluation, with all of the converters designed to achieve a target efficiency of 99.5 % are presented in **Fig. 3.4**, where the total estimated minimum volume of the converters is shown together with the optimal loss distribution. The considered switches are given in **Table 3.3**, and the number of paralleled devices, switching frequencies and the number of filter stages is presented in **Table 3.4**.

Tab. 3.4: Number of switches of each voltage rating used in parallel, the switching frequency f_{sw}, the effective switching frequency for the first stage EMI filter inductors $f_{sw,eff}$, and the number of filter stages to comply with CISPR 11 Class A regulations.

	2L	2L-INT	3L-T-type	3L-FCC	5L-HANPC	5L-FCC	7L-HANPC	7L-FCC
N_{sw} 1200 V	2	2	2	-	-	-	-	-
N_{sw} 650 V	-	-	2	3	2 (S_3) & 1 (S_5)	-	2 (S_3) & 1 (S_5)	-
N_{sw} 250 V	-	-	-	-	4	5	-	-
N_{sw} 200 V	-	-	-	-	-	-	2	3
f_{sw}	17.2 kHz	14.5 kHz	30.4 kHz	15.2 kHz	14.2 kHz	9.5 kHz	54.9 kHz	34.4 kHz
$f_{sw,eff}$	17.2 kHz	29.0 kHz	30.4 kHz	30.4 kHz	28.4 kHz	37.9 kHz	164.7 kHz	206.7 kHz
# Filter Stages	2	2	2	2	2	2	3	3
Semicond. Technology	SiC	SiC	SiC	SiC	SiC & Si	Si	SiC & GaN	GaN

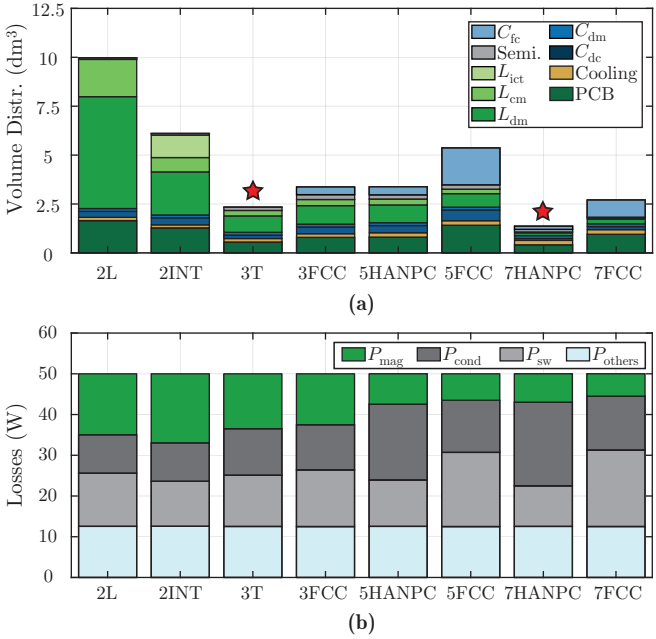

Fig. 3.4: (a) Total volume distribution and **(b)** optimal power loss distribution for each topology resulting in a minimum converter volume. The number of switches, switching frequency, number of EMI filter stages and semiconductor technology of each converter is shown in **Table 3.4**.

For the 2L topology, the 2L voltage output and the low switching frequency lead to large inductor requirement. However, to understand the volume difference of the 2L conveter with respect to the rest of the converters, the scaling law between the power losses and the volume of an inductor have to be analyzed [44]. For a certain inductance value L, current ripple Δi_{L}, magnetic core cross section A_{core}, and number of turns N_{t}, the flux density ripple is given by

$$\Delta B = \frac{L\Delta i_{\mathrm{L}}}{N_{\mathrm{t}} A_{\mathrm{core}}} \propto \frac{U_{\mathrm{L}}}{f_{\mathrm{sw}} A_{\mathrm{core}}} \propto \frac{1}{A_{\mathrm{core}}} \propto \frac{1}{l^2} \tag{3.8}$$

where l is the linear dimension. If this is then used for the Steinmetz equation, the core losses are

$$P_{\mathrm{core}} \propto V_{\mathrm{core}} \Delta B^{\beta} f_{\mathrm{sw}}^{\alpha} \propto \frac{l^3}{l^{2\beta}} \propto \Big|_{\beta=2} \frac{1}{l}\,, \tag{3.9}$$

with V_{core} the volume of the magnetic core and α and β the Steinmetz paremeters. For the winding losses, neglecting the high frequency effects,

$$P_{\mathrm{w}} = I_{\mathrm{L,rms}}^2 R_{\mathrm{w}} \propto I_{\mathrm{L,rms}}^2 \frac{l}{\kappa A_{\mathrm{w}}} \propto \frac{l}{l^2} \propto \frac{1}{l} \tag{3.10}$$

with $I_{\mathrm{L,rms}}$ the RMS current of the inductor, R_{w} the resistance of the windings, A_{w} the cross section of the conductor, and κ the conductivity. Hence, it is seen that in a very rough approximation the losses of an inductor are inversely proportional to its linear dimension. This is further confirmed in the analysis done in [72], where it is shown that for sinusoidal currents and $\beta = 2$ an optimization for minimum power losses results in,

$$P_{\mathrm{L}} \propto V_{\mathrm{L}}^{-\frac{1}{3}} \propto \frac{1}{l}\,, \tag{3.11}$$

where V_{L} is the inductor volume. This means, that unless the output inductor L_{dm1} is limited by saturation (which in this comparison is not the case for the 2L and 3L topologies), to cut the inductor losses in half an $\approx 8\times$ larger volume is needed. Hence, since the 2L converter exhibits the largest inductor requirement, Eq. **(3.11)** penalizes it the most, leading its total volume to be substantially larger than, e.g., for the 3L converters.

In the case of the 2L interleaved converter, the CIs reduce the requirement on the first EMI filter stage by providing a 3L voltage output and higher effective switching frequency, however, the losses of the CIs have to be

included into the available loss budget for the magnetics. For these 2L bridge-leg converters, discontinuous PWM (DPWM) or 2/3-PWM was considered [107, 108], which is a modulation scheme that only switches two out of three phases-legs at any point in time and leads to over a third of switching loss savings [108].

The 3L T-type converter offers better performance than the 2L bridge-leg variants, since it provides a third output voltage level without inserting more passive energy storage components in the system, leading to a reduced size of the filter inductors compared to the 2L bridge-leg variants, and without the need of inserting bulky film capacitors, as is the case for all of the FC-based topologies. This can be observed when comparing the 3L T-type to the 3L FCC, where the volume of the magnetics is similar, but the total volume difference is due to the additional FCs that are needed to create the 3L voltage output.

For the 5L converters, the volume of the FCs is large due to the low switching frequencies. The fact that the capacitance requirement for all FC voltage levels is the same and that higher voltage capacitors have larger volumes penalizes the 5L FCC, given that it needs FCs at 540 V, 360 V and 180 V, whereas the 5L HANPC converter only needs FCs at 180 V.

The 7L converters offer a comparably higher switching frequency of each stage due to the high-performing low-voltage GaN semiconductors, and yield the highest effective switching frequency on the first filter stage ($\approx$ 4x higher than the 5L converters). This reduces the volume of the magnetics drastically, however, for the 7L FCC the volume of the capacitors is large, with five FC stages distributed equally between 600 V and 120 V.

In case the efficiency constraint would be relaxed from 99.5 % to 99.0 %, the 2L converter would be the one that gains most in performance, reducing its volume fivefold, compared to a threefold volume reduction of the 2L interleaved converter and a twofold reduction of the 3L and 5L converters.

Finally, if the voltage ripple constraint of the FCs, $\Delta U_{\mathrm{fc,max}}$, would be relaxed from 5 V to 10 V, which would mean a worst-case 20 V steady-state overvoltage on a FC switching stage, the volume of the FCs could be reduced by up to 50 %.

3.4 Detailed Design of the Selected Topologies

The analysis done in **Section 3.3** serves the purpose of identifying the best performing topologies for the efficiency target at hand. In order to have a better understanding of the achievable power density, the converters have to be designed in more detail. Having identified the 3L T-type and the 7L-HANPC

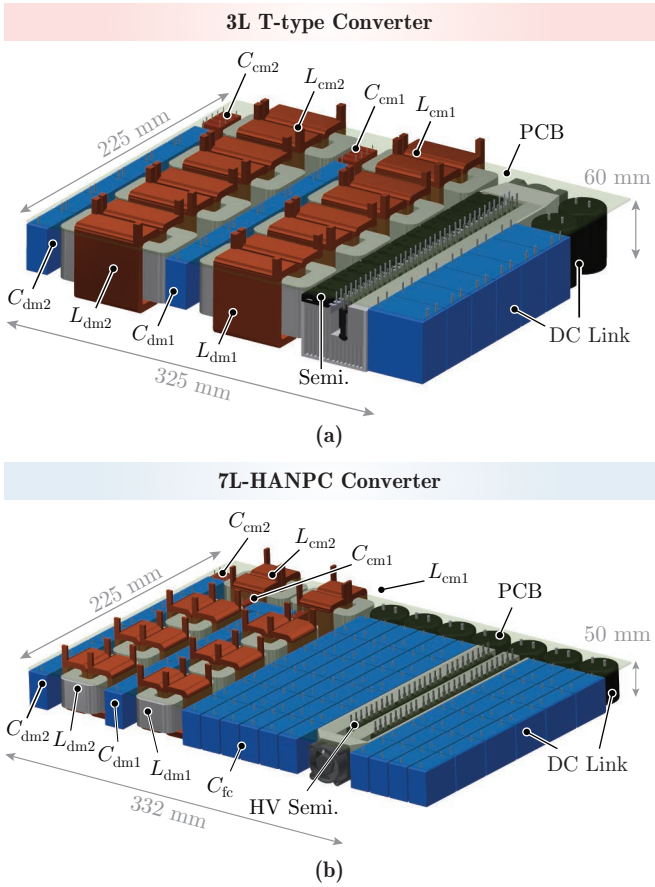

Fig. 3.5: 3D CAD illustrations of **(a)** the 3L T-type converter and **(b)** the 7L-HANPC converter.

converters as suitable candidates, in a next step both of them are modeled with 3D CAD software, and presented in **Fig. 3.5**. The relevant component values of both designs can be found in **Table 3.5**.

The first step to design the converters is to account for additional switching losses, since the switching loss model presented in **Section 3.3.1** only considers the minimum and unavoidable switching losses. Due to the channel of the semiconductor not closing infinitely fast, there are additional $V - I$

Tab. 3.5: Final parameters of the topologies shown in **Fig. 3.5**.

	3L T-type	7L-HANPC
f_{sw}	20 kHz	20 kHz
$f_{sw,eff}$	20 kHz	60 kHz
L_{dm}	166.3 µH Nanocrystalline Core: F3CC0040 3 Distr. Airgaps in L_{dm1}	30.8 µH Nanocrystalline Core: F3CC06.3 1 Airgap in L_{dm1}
C_{dm}	6.6 µF	4.4 µF
C_{fc}	-	60 µF
C_{dc}	60 µF	60 µF

overlap switching losses that will occur, and a sufficient margin of 60 % has been added to the minimum losses (cf., **Section 2.5**). Since the switching frequency is reduced by considering additional switching losses, for the 7L-HANPC a third low-voltage MOSFET is introduced in parallel to reduce the conduction losses. Since both topologies have bridge-legs with a DC-link midpoint connection, a 150 Hz ripple occurs on the DC-link midpoint voltage. Although this voltage ripple can be eliminated by employing third harmonic modulation ($M_3 \neq 0$) [105], further capacitance can be added to the DC-link, for which aluminum-electrolyte capacitors are placed in the available space of the DC current path of the converters, parallel to the foil capacitors and with a small inductance in series (bridged by a damping resistor) to avoid uncontrolled resonances between the capacitor stages. Note, that in the 7L-HANPC converter, the low voltage switches are placed on the PCB area above the FCs.

The loss distributions presented in **Fig. 3.6a** for the final designs are in close accordance to the ones obtained from the topology comparison. Both of the designs have a 15-16 % (7.5 W) of loss margin left for the PCB tracks and connectors among others. Due to the additional considered switching losses, for a 20 kHz operation of the 7L-HANPC converter a two-stage EMI filter is superior to the three-stage filter resulting from the topology comparison (**Table 3.4**). In addition, for the 7L-HANPC converter the losses occurring in the foil capacitors cannot be neglected, as they account for up to 5 % of the loss budget.

From the power density perspective, the 7L-HANPC converter is superior to the 3L T-type converter (2.7 kW/dm^3 vs. 2.2 kW/dm^3), however, the relative

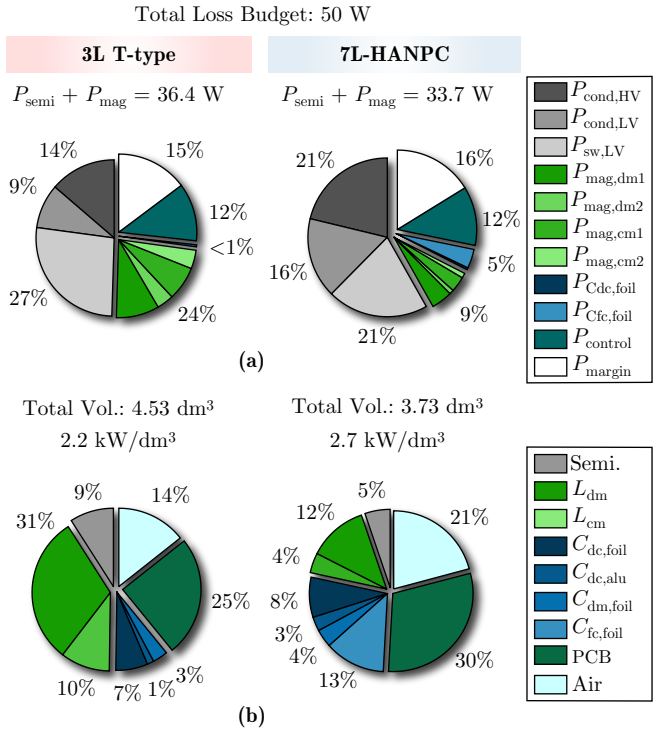

Fig. 3.6: (a) Loss distribution and **(b)** volume distribution of the 3L T-type converter (left) and 7L-HANPC converter (right).

volume difference between both converters decreases from 70 % that result from the theoretical comparison to only 21 % in the 3D CAD design. This results mainly from the difference between the direct summation of the boxed volumes of individual components and the final 3D design of the converter. For the volume calculation, it is also assumed here that a space with a height of 15 mm above the PCB is required to accommodate the control board, the measurement devices, the auxiliary power circuitry and the connectors amongst others.

3.5 Summary

In this chapter, a quantitative ML topology evaluation is conducted to identify the most suitable three-phase inverter topologies to achieve a 99.5 % efficiency target. The low switching frequency imposed by the efficiency target leads to large passive (magnetic and capacitive) components. On the one hand, for the 2L bridge-leg based converters, the size of the magnetics is very large due to a very tight loss budget, EMI and filter cut-off frequency requirements and the scaling laws of the switching stage output inductors (8x larger volume needed to halve the losses). On the other hand, creating a ML voltage output waveform comes at a cost of large volumes of the FCs. Hence, the two topologies that are offering the best power densities were designed in more detail, and the difference in power density from a conventional 3L T-type converter (2.2 kW/dm^3) and a 7L-HANPC converter (2.7 kW/dm^3) was identified to be approximately 20 % for the same efficiency. Therefore, it can be concluded that the 7L-HANPC can be built in a more compact fashion than the 3L T-type converter for the same efficiency target, which motivates the next chapter, where the topology is analyzed in detail and then finally realized.

4

All-Silicon 99.35 % Efficient Three-Phase Seven-Level Hybrid Neutral Point Clamped / Flying Capacitor Inverter

This chapter summarizes the most relevant findings in the context of designing, building and experimentally analyzing an ultra-efficient three-phase PV inverter system also published in:

- **J. Azurza Anderson**, E. J. Hanak, L. Schrittwieser, M. Guacci, J. W. Kolar, and G. Deboy, "All-Silicon 99.35 % efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 1, pp. 50–61, 2019.

Motivation

The promise that multi-level converter concepts enable an ultra-efficient yet compact realization has to be experimentally validated. In this chapter, a 7L three-phase hybrid-topology PV inverter that achieves 99.35 % peak efficiency with an all-Si passively-cooled realization is presented, and it is shown that achieving the 99.5 % efficiency target with GaN power semiconductors and next-generation Si devices is feasible.

Executive Summary

With the increasing use of photovoltaic systems, a large demand for efficient, power-dense and lightweight grid-interface inverters is arising. Accordingly, new concepts like ML converters, which are able to reduce the converter losses while still keeping a low construction volume, have to be investigated. The hybrid 7L topology introduced in the previous chapter is analyzed here in depth. This topology comprises an active neutral point clamped stage, followed by a FC stage. Compared to a pure FCC, the combination of these two stages allows to save more than half of the capacitor volume, while still having the same requirement for the output filter stage, and hence, the same output filter volume. Moreover, the topology employs low-voltage devices and ensures low conduction and switching losses, resulting in a higher efficiency. The principle of operation of the system is briefly reviewed, and based on a detailed component modeling, an efficiency vs. power density optimization is carried out, for which switching loss measurements of state-of-the-art 200 V semiconductors are performed. From the optimization, a high-efficiency design is selected and the practical hardware realization is discussed. The simulation and optimization results are then verified by realizing an all-Si 99.35 % efficient three-phase 7L system, featuring a volumetric power density of 3.4 kW/dm^3 (55.9 W/in^3), a gravimetric power density of 3.2 kW/kg, and fulfilling CISPR Class A EMI requirements. Finally, it is shown that, an all-Si realization with next generation Si switches can achieve 99.5 % efficiency with the same hardware, and 99.6 % with commercial state-of-the-art GaN switches.

4.1 Introduction

As PV energy generation provides a continuously increasing share to the net electricity supply [4, 109], there is a clear demand for power electronics with high efficiency, high power density, low weight and low costs [21, 44, 110, 111]. For PV systems with high capacity factors, which are in operation for many hours a day, a high energy conversion efficiency is of major importance [112]. With the goal of exploring the efficiency limits, this chapter presents an ultra-efficient ML three-phase inverter solution designed for a typical PV installation, as conceptually shown in **Fig. 4.1,** targeting a peak efficiency of 99.5 % for a nominal power of 10 kW.

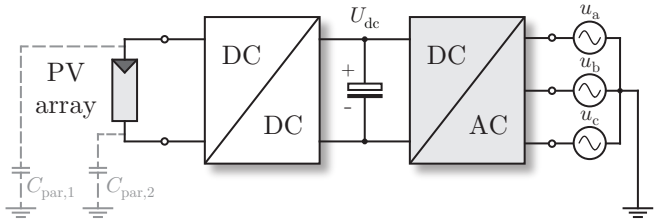

Fig. 4.1: System overview for transformerless transfer of PV power into the low-voltage three-phase grid (400 V_{rms}, line-to-line). The PV array is typically followed by a DC/DC converter for MPPT and a three-phase PWM inverter (highlighted), which is the focus of this chapter.

When aiming for ultra-high-efficiency converters, the trade-off with respect to losses and volume between active (power semiconductors) and passive (magnetic and capacitive) components has to be evaluated in detail. As three-phase converters are typically hard-switched, an optimum between conduction and switching losses that favors large die areas and low switching frequencies exists [72]. However, low switching frequencies lead to bulky magnetic components. This contradiction can be solved by the use of ML topologies like the FCC, illustrated in **Fig. 4.2a** for the case of seven levels. ML converters reduce the inductance requirement of the AC-side inductors for a given current ripple amplitude quadratically with respect to the number of levels, due to the ML output voltage characteristic and due to the increase of the effective switching frequency, leading to smaller and more efficient magnetic components [113, 114]. Additionally, ML converters take advantage of low-voltage power MOSFETs, featuring a higher hard-switching FOM compared to high-voltage power semiconductors [56]. To achieve a ML output voltage characteristic with an FCC, capacitors carrying an integer multiple of the lowest cell voltage are alternatingly connected to the output during operation. However, the capacitance requirement of the FCs, driven by the need to constrain the switching frequency voltage ripple across them, is directly proportional to the load current (and hence, output power) and inversely proportional to the switching frequency [113]. Accordingly, ultra-high power densities can be achieved at the expense of an efficiency reduction, by using high switching frequencies (in the hundreds of kHz range) that favor the utilization of multi-layer ceramic capacitors (MLCC) with high energy density [17, 49, 115]. However, as already mentioned, ultra-efficient hard-switching converters designed for high power ratings are typically operated

at low switching frequencies (low tens of kHz) [9, 66]. These low switching frequencies lead to higher capacitance requirements of the FCs, giving a clear incentive to research alternatives to the FCC approach, which should still offer ML voltage characteristics but with a smaller capacitance demand. A topology that allows to reduce by more than half the number of capacitors is presented in [94, 116], where a hybrid approach between the ANPC converter and the FCC is proposed (cf., **Fig. 4.2b**), hereafter referred to as the HANPC converter. This topology, besides reducing the number of capacitors, enables a further volume saving, as only the capacitors with the lowest voltages remain. This is advantageous, since the higher the voltage rating of the capacitors, the lower the capacitance density, and hence, more capacitors have to be arranged in parallel and/or series, as can be seen e.g., for the case of a 13L FCC in [30]. These characteristics of the HANPC converter outperform the FCC in terms of achieving higher power densities for ultra-efficient converters, in particular for three-phase inverters in the 10 kW range targeting 99.5 % efficiency, as shown in the comprehensive ML topology evaluation done in **Chapter 3**.

Therefore, this chapter focuses on the optimization and hardware realization of an all-Si ultra-efficient passively-cooled 12.5 kW three-phase 7L-HANPC inverter, and finally experimentally verifies a peak efficiency of 99.35 % and a power density of 3.4 kW/dm^3 (55.9 W/in^3) [117]. Firstly, the principle of operation of the HANPC converter is explained in detail in **Section 4.2**. In **Section 4.3** a design optimization is presented for the specifications given in **Table 3.1**. The hardware design and the measurement results are presented in **Section 4.4**, and finally the paper is concluded in **Section 4.5**. Additionally, a detailed comparison of the accuracy of electric and calorimetric efficiency measurement methods is done in the **Appendix E**.

4.2 Principle of Operation of the HANPC Converter

As the HANPC topology so far has only been employed in medium-voltage high-power applications [94,118], a brief review of the principle of operation is provided in the following. Each bridge-leg of the HANPC inverter, illustrated in **Fig. 4.2b** for seven levels, consists of two cascaded stages: the ANPC stage connected to the DC input voltage and the FC stage finally generating the AC output voltage. The ANPC stage switches ($S_{1...4}$) connect the points I and II for positive output voltages $u_i > 0$ to the positive DC-link voltage rail

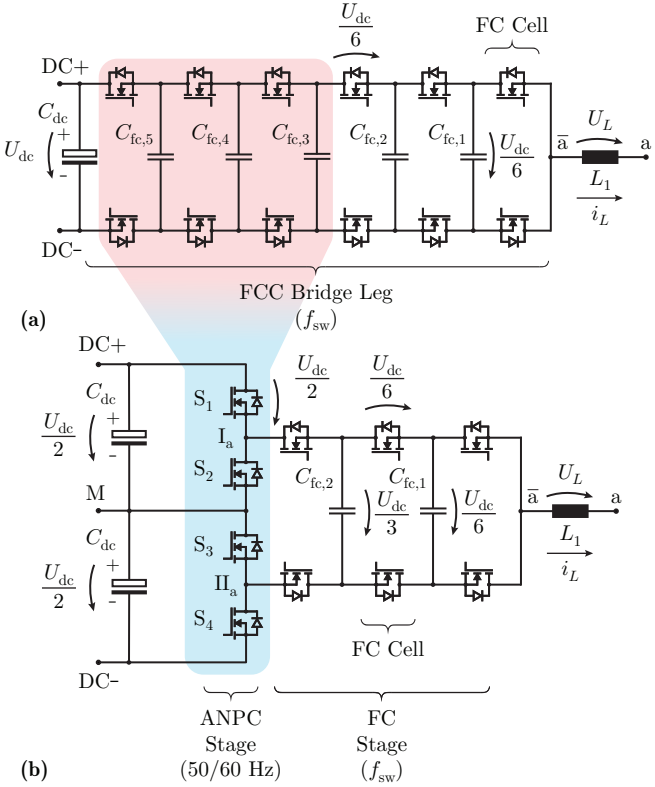

Fig. 4.2: (a) Circuit schematic of a 7L-FCC bridge-leg, which is purely composed of low-voltage semiconductors operated at switching frequency and **(b)** the 7L-HANPC bridge-leg structure, i.e., a hybrid approach composed of an ANPC stage with semiconductors switching at 50/60 Hz, and a FC stage, with semiconductors operating at switching frequency; both arrangements are shown for phase a of the three-phase (phases a, b, c) inverter topology.

(DC+) and the DC-link midpoint M respectively, and to M and the negative DC-link voltage rail (DC-) for $u_i < 0$, as shown in **Fig. 4.3**. This results in grid frequency operated ANPC stage switches that have to be rated to withstand $U_{dc}/2$. Following, there is a FC stage (for the case of a 7L-HANPC it is a 4L FC stage, as shown in **Fig. 4.2b**), whose semiconductors are operated at switching frequency using phase shifted PWM, and have to be rated for $U_{dc}/6$.

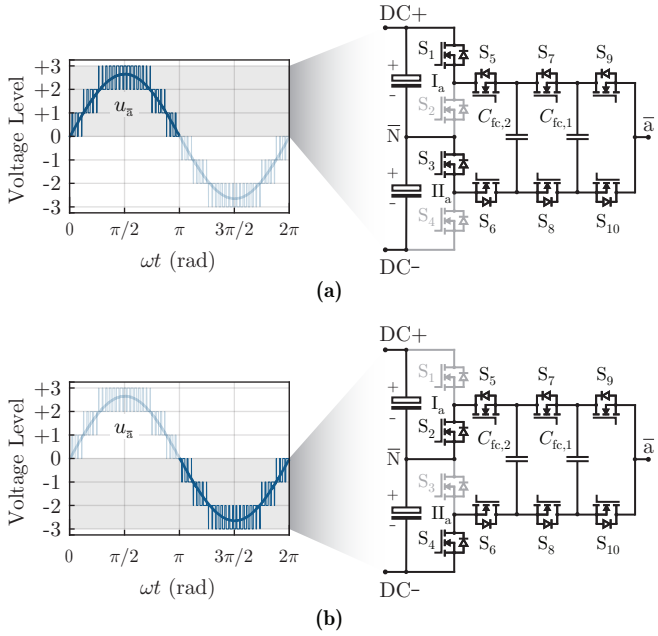

Fig. 4.3: Conduction states of the ANPC stage for **(a)** positive and **(b)** negative output voltages, shown for a bridge-leg of the 7L-HANPC. The ANPC stage switches ($S_{1...4}$) are connecting the subsequent FC stage ($S_{5...10}$) to the upper or lower half of the DC-link depending on the sign of the output voltage, while the FC stage is continuously switching at switching frequency. It has to be noted that the 0 output voltage level can be created with the FC stage clamped to either the high- or low-side of the DC-link.

The fundamental difference between the HANPC converter and the FCC structure is that by actively clamping the FC stage to either the high-side or the low-side of the DC-link, the same number of levels can be obtained with a HANPC converter compared to a FCC. For the HANPC converter, the number of levels is given by

$$N_{\text{lev,HANPC}} = 2 \cdot N_{\text{cell}} + 1\,, \tag{4.1}$$

where N_{cell} is the number of FC cells, whereas for the FCC bridge-leg the number of levels is

$$N_{\text{lev,FCC}} = N_{\text{cell}} + 1\,. \tag{4.2}$$

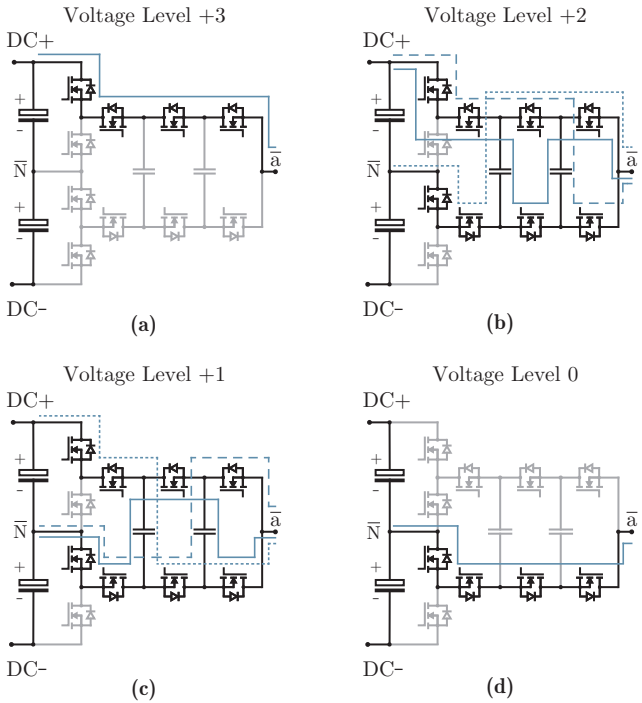

Fig. 4.4: Conduction states of a 7L-HANPC bridge-leg for **(a-c)** the positive output voltage levels and **(d)** zero output voltage. For output voltage levels +3 and 0, the FCs are shorted by the high- and low-side FC stage switches respectively, and for levels +2 and +1, there are three redundant switching states [119]. By ensuring equal conduction times of the three switching states, done by phase-shifted PWM, the FCs are naturally balanced, as shown in **Fig. 4.5**.

From Eqs. **(4.1)** and **(4.2)** it can be seen that the HANPC converter needs half the FC cells compared to the FCC to generate the same number of levels. For the case shown in **Fig. 4.2**, both the FCC and HANPC converter produce a 7L voltage output, but for the FCC the number of cells is $N_{\text{cell}} = 6$, and for the HANPC converter only $N_{\text{cell}} = 3$ is implemented. This is further illustrated in **Fig. 4.3**, where it can be seen that the +3…0 output voltage levels are created by connecting the FC stage to the upper half of the DC-link (cf., **Fig. 4.4**), whereas the output voltage levels 0… − 3 are created by connecting the FC stage to the lower DC-link half. Hence, the ANPC stage acts as a selector

switch, where the 0 output voltage level can be created in both ANPC stage configurations.

The effective switching frequency applied to the AC-side inductor and/or filter stage, which affects the filter design, losses and volume, is

$$f_{\mathrm{sw,eff}} = N_{\mathrm{cell}} \cdot f_{\mathrm{sw}} \,, \tag{4.3}$$

with f_{sw} being the switching frequency of the individual stages. The difference in N_{cell} between both topologies, however, has a minor effect on the effective switching frequency as will be made visible by the following qualitative analysis: if it is assumed that there is a certain loss budget allocation for the power semiconductors of the converter, and that for optimizing semiconductor losses the die areas of the switches are chosen such that the conduction losses and hard-switching losses are similar (cf., **Section 2.8**), then the FCC can be designed to have approximately equal conduction losses and switching losses. To adapt the design to the HANPC converter, following **Fig. 4.2**, if the conduction losses of half the FC cells of the FCC stage are chosen to be the same as the conduction losses of the ANPC stage switches (which are switching at line frequency and hence have negligible switching losses), then the available budget for the switching losses of the FC stage of the HANPC converter is equal to that of the six cells of the FCC. Therefore, the last three HANPC FC cells can switch at twice the switching frequency of their pure FCC counterpart switches, hence imposing the same effective switching frequency on the filter stage. Following the same argumentation, the dimensioning of the capacitance of the FCs, which depends on the maximum conduction time,

$$t_{\mathrm{fc,max}} = \frac{1}{N_{\mathrm{cell}} f_{\mathrm{sw}}} \,, \tag{4.4}$$

shown in **Fig. 4.5**, remains similar for the FCC and the HANPC converter [49, 113, 120], since the product of $N_{\mathrm{FC,cell}}$ and f_{sw} remains similar. Hence, the dimensioning of the FCs follows

$$C_{\mathrm{fc,min}} = \frac{t_{\mathrm{fc,max}} I_{\mathrm{ac,pk}}}{\Delta U_{\mathrm{fc,max}}} \,, \tag{4.5}$$

where $I_{\mathrm{ac,pk}}$ is the peak AC current, and $\Delta U_{\mathrm{fc,max}}$ the maximum allowed peak-to-peak FC voltage ripple. This is illustrated in detail in **Fig. 4.5**, where a two-cell and three-cell FC stage are shown for the duty cycle at which $t_{\mathrm{fc,max}}$ respectively occurs. For the case of a two-cell FC stage, $t_{\mathrm{fc,max}}$ occurs for a duty cycle of 0.5, while in the case of a three-cell FC stage, $t_{\mathrm{fc,max}}$ occurs at

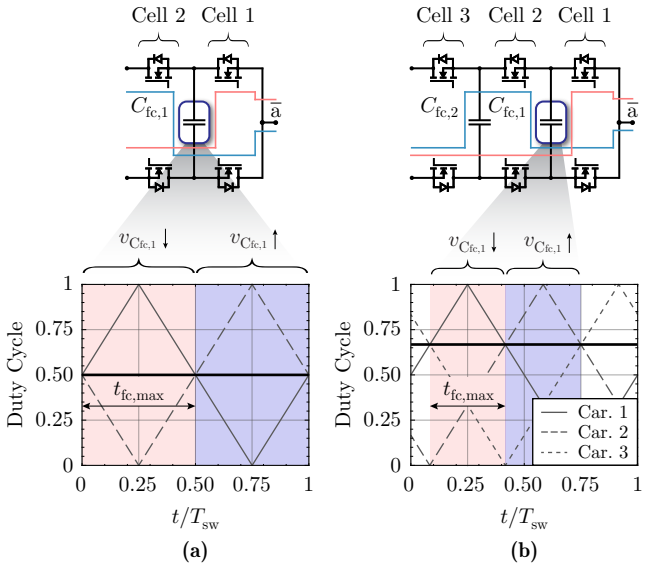

Fig. 4.5: Conduction states that charge (blue) and discharge (red) $C_{\mathrm{fc},1}$ for **(a)** a two-cell and **(b)** a three-cell FC stage. Additionally, the duty cycle that leads to the longest FC conduction time $t_{\mathrm{fc,max}}$ is shown, where it is seen that $t_{\mathrm{fc,max}}$ is inversely proportional to the number of levels. Due to phase-shifted PWM, the FC charge and discharge times remain equal for a whole switching period T_{sw}.

0.66 or a duty cycle of 0.33. Hence, to have a conservative approach on the FC dimensioning (cf., Eq. **(4.5)**), it is considered that the peak output current $I_{\mathrm{ac,pk}}$ occurs for the duty cycles that result in $t_{\mathrm{fc,max}}$. By phase shifting the carriers by $2\pi/N_{\mathrm{cell}}$, natural balancing of the FCs occurs regardless of the number of levels, as shown in **Fig. 4.5** for $C_{\mathrm{fc},1}$. Therefore, no measurement of the FC voltages is required to operate this converter. Further analysis of the modulation and switching states of the HANPC converter can be found in [94, 118, 119], a variant of the 7L-HANPC is presented and discussed in [121], the natural balancing of FC voltages by phase-shifted PWM is covered in [122–124], and the behavior of flyinig capacitor converters under critical operating conditions such as start-ups and shut-downs is discussed in [125].

The main waveforms of the 7L-HANPC inverter are shown in **Fig. 4.6** for an output EMI filter structure with the star-point of the filter capacitors connected to the DC-link midpoint as illustrated in **Fig. 4.9**. The seven

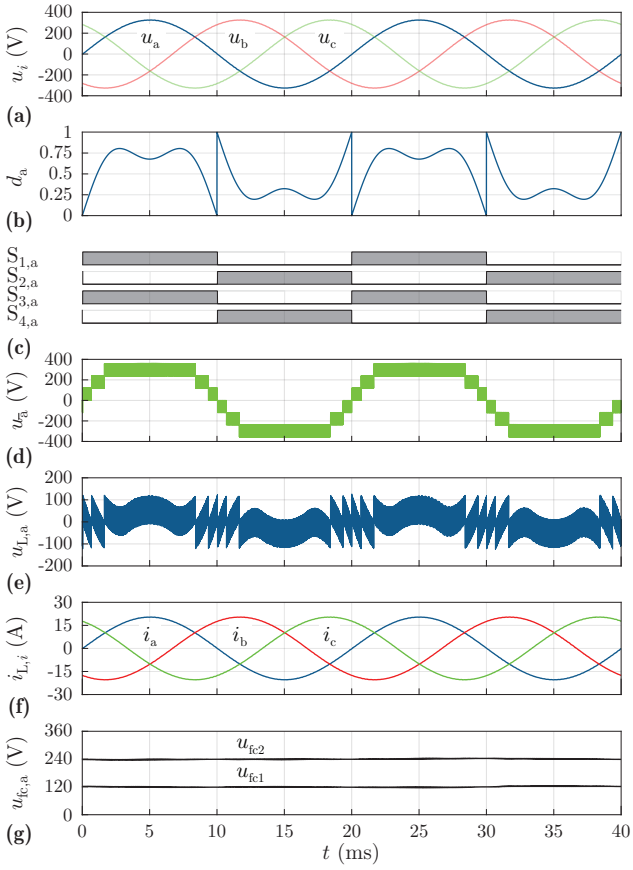

Fig. 4.6: Main waveforms of the 7L-HANPC inverter (cf., **Fig. 4.2(b)** and **Fig. 4.9**) operating with a DC-voltage of 720 V and an output power of 10 kW: **(a)** mains phase voltages, **(b)** duty cycle for phase a (d_a), **(c)** gate signals for the ANPC stage switches of phase a, **(d)** ML voltage output of node $\bar{a}$ (cf., **Fig. 4.2(b)**) referenced to the DC-link midpoint and **(e)** filter inductor (L) voltage waveform of phase a, **(f)** grid phase currents, and **(g)** FC voltages of phase a. Note that a third harmonic component is superimposed in the modulation to reduce the low-frequency component of the DC-link midpoint current, as seen for d_a, with an amplitude of one fourth of the phase output voltage.

output voltage levels together with the voltage applied to L_1 are shown for phase *a*, as well as the grid phase currents and the FC voltages, which are naturally balanced using phase shifted PWM. Finally, it has to be mentioned that, as for all NPC converters (as well as for the T-type converter), a certain difference of the voltages of the upper and lower DC-link half arises due to the midpoint current i_{mid} which has a dominant third harmonic component (cf., **Fig. 4.9**) [105, 119, 126, 127]. However, this voltage difference can be reduced by either superimposing a third harmonic (zero sequence) to the modulation in such a way that the amplitude of the low-frequency part of i_{mid} is minimized ($i_{\text{mid}}(t) \approx 0$), or by increasing the capacitance of the DC-link capacitors.

4.3 Design Optimization

To evaluate the most suitable component selection for the final hardware demonstrator, a comprehensive optimization of the 7L-HANPC inverter is performed, following the flowchart presented in **Fig. 4.7**. The optimization routine is conducted according to the converter dimensioning guidelines presented in **Chapter 3**, where for the FC stage, four different types of switches are considered, switching in a frequency range between 10 kHz and 40 kHz:

- two commercial 200 V Si *OptiMOS 3* devices (*Infineon*),
- a prototype of a *next generation* 200 V Si device (*Infineon*), for which data and samples have been provided by the manufacturer [65], and,
- the GaN power semiconductors of type *EPC2047* (*EPC Co.*).

For the ANPC stage, however, the following two options are considered:

- 600 V *CoolMOS CFD7* switches (*Infineon*), and,
- a series-connection of the same low-voltage switches as used in the FC stage [71, 128]. This series-connection of the low-voltage switches shown in **Fig. 4.10** would lead to the advantage of having the same semiconductors employed in the whole system, as is done in [128]. Its circuit schematic is similar to an FCC, but operated in a 2L configuration by adding balancing resistors (R_{b}) that ensure equal voltage balancing during steady-state, and capacitors (C_{f}) of low capacitance that ensure equal voltage balancing during the switching transients.

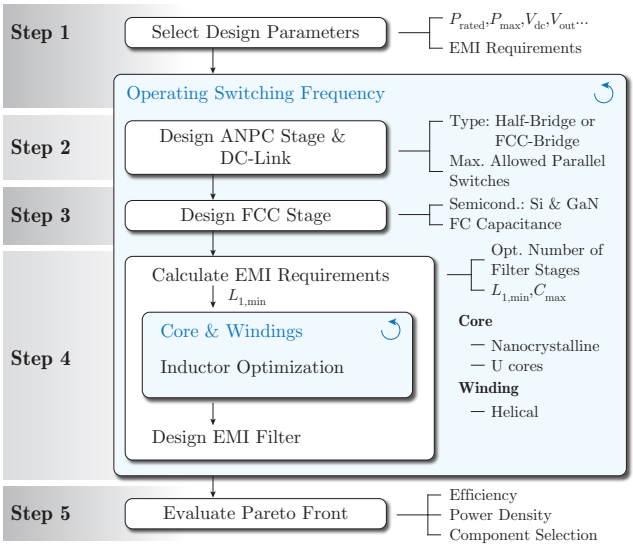

Fig. 4.7: 7L-HANPC converter optimization flowchart used to determine the Pareto front lines shown in **Fig. 4.10**.

Since the semiconductors, and in particular the FC stage switches, are the largest power loss contributors of the converter (cf., **Fig. 4.11a**), it is essential to have accurate switching loss data in order to obtain reasonable and realistic results in the converter optimization. For this reason, the two lowest R_{on} devices of GaN and Si available at the time (the 11.1 mΩ 200 V Si switches of *Infineon* and the 10 mΩ 200 V GaN switches from *EPC Co.*) were experimentally characterized, and the complete results can be found in [65]. Most importantly for this work, the switching losses of both devices were measured, and the results are summarized in **Fig. 4.8**.

Given that the ML output voltage waveform enables a large reduction of the size and losses of the magnetic components, it was observed that for the topology at hand a sufficiently compact filter can be obtained by implementing a combined DM + CM filter instead of separating the noise filtering into discrete DM and CM filters, which would inevitably lead an increased magnetic component count. Hence, without the need to turn to a separate CM filter on the DC side in order to save losses and/or volume as presented in **Section 3.3.2**, to comply with the CISPR 11 Class A standard [130] on the AC-side a N_f-stage *L-C* EMI filter structure is considered in the

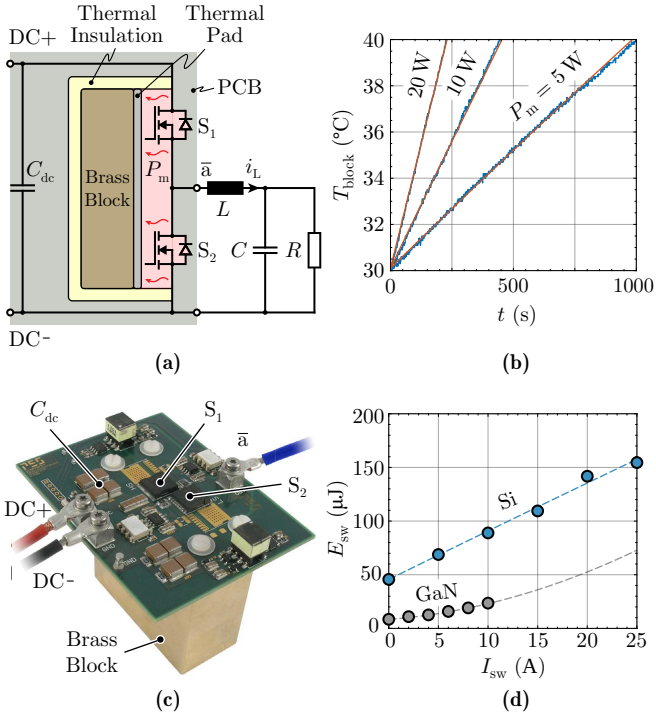

Fig. 4.8: Switching loss measurements of the lowest-R_{on}-in-class low-voltage (200 V) Si (11.1 mΩ *IPT111N20NFD* from *Infineon*) and GaN (10 mΩ *EPC2047* from *EPC Co.*) power semiconductors. The switching loss measurements are taken with **(a)** a calorimetric setup based on [73,74,129], where the switching losses are determined by fitting the measured temperature rise curve from 30 °C to 40 °C to a calibrated *R-C* thermal model; **(b)** mapping of the power losses to the temperature rise curve for the case of the Si switches; **(c)** switching loss measurement setup for the Si switches, and **(d)** measured hard-switching loss data at a DC-link voltage of 120 V (addition of the soft- and hard-switched transition losses of a half-bridge that occur during one switching period) for both devices (markers) together with a second order fit (dashed line). A full experimental characterization of both devices is presented in [65].

optimization routine ($N_f \in \{1,2,3\}$), which simultaneously attenuates DM and CM noise [103] as the filter stages are referenced to the DC midpoint (cf., **Fig. 4.9**).

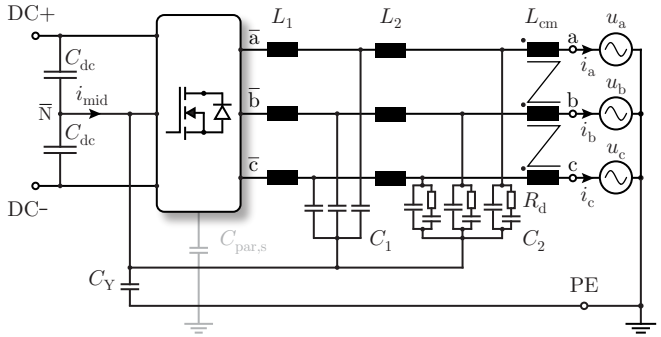

Fig. 4.9: EMI filter structure of the final prototype, with two *L-C* filter stages simultaneously attenuating DM and CM components of the output voltages of the inverter bridge-legs (with reference to the DC voltage midpoint) and a CM choke placed before the grid connection terminals.

The filter design space is restricted by two factors: firstly, it should comply with the Class A EMI limits by a minimum attenuation margin of 10 dBµV, and secondly, the resonance frequency of the filter should be lower than one fourth of the effective switching frequency of the converter, to avoid unwanted excitation of the filter circuit (cf., **Section 3.3.2**). For the filter inductor L_1, modeled and optimized according to [105], nanocrystalline cores with helical windings are used in order to reduce the losses [9,66], whereas for the further stage inductors (L_2, cf., **Fig. 4.9**) commercially available inductors are considered.

Given the efficiency barriers obtained for different semiconductor technologies (indicated with the Pareto curves in **Fig. 4.10**), for the final design the all-Si approach shown with a star is chosen, since the calculated efficiency difference between the commercially available Si devices and GaN devices is only 0.25 % for the same power density; with the introduction of *next generation* Si devices, this difference is expected to be reduced to 0.15 %, achieving then the 99.5% efficiency target. Regarding the ANPC stage configuration, the optimization results shown in **Fig. 4.10** suggest that using 600 V switches for the ANPC stage (solid line Pareto front) offers superior performance both in terms of efficiency and power density compared to the series-connected 200 V device variant (dashed line Pareto front). This is due to the lower R_{on} of the 600 V switches compared to three 200 V switches connected in series, and the need to passively balance the voltage of the 200 V switches by means

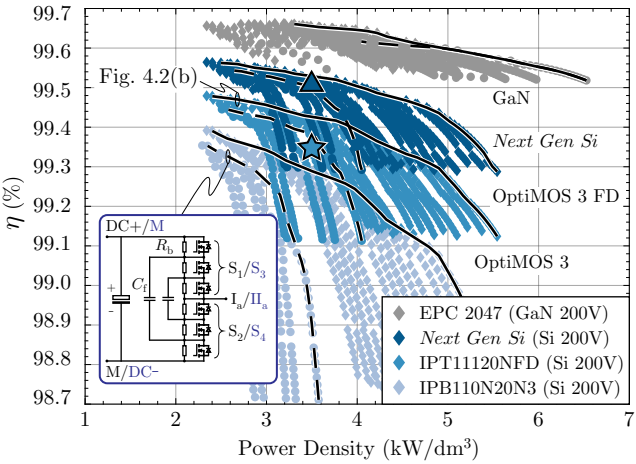

Fig. 4.10: Pareto optimization results for the different considered semiconductor devices and realizations of the ANPC stages. Results for the ANPC stage with 31 mΩ 600 V *CoolMOS CFD7* devices (*Infineon*) are shown with rhombi and continuous black Pareto lines, and the results for the series-connection of the same low-voltage MOSFETs of the ANPC stage [71] are shown with circles and dashed black Pareto lines. The efficiency is calculated at the operating point of 10 kW of the three-phase system, where the hardware prototype presented in this paper is represented by a star (four parallel devices for each switch of the ANPC stage), and the achievable performance with *next generation* 200 V Si switches (estimation resulting from an extrapolation of recent FOM improvement) is shown by a triangle.

of balancing resistors R_b, shown in **Fig. 4.10.** (Note, however, that with the new modulation scheme presented in [131] the balancing of series-connected switches in a quasi-X-level configuration can be solved.) Since low switching frequencies yield designs with a high efficiency but a large volume, and high switching frequencies yield compact but more lossy designs (cf., **Fig. 4.10**), the design that is finally chosen for the hardware demonstrator reserves place for up to six parallel-connected 31 mΩ *CoolMOS CFD7* devices for the ANPC stage, and two parallel 11.1 mΩ *IPT111N20NFD* devices switching at 16 kHz, resulting in an effective switching frequency of 48 kHz for the filter stage. It has to be noted that for the case of the 600 V switches, the more switches connected in parallel, the lower the losses (negligible switching losses at grid frequency), however, at the price of increased cost and volume. It is for this reason that, in this optimization, a limit of six paralleled switches is

considered for the ANPC switches for both ANPC stage configurations. The loss distribution of the selected design for the realized hardware demonstrator is shown in **Fig. 4.11a** for a power of 10 kW, where it can be observed that the semiconductors account for 66 % of the total converter losses, out of which 84 % are caused by the FC switches. The resulting contribution of the magnetic components to the loss and volume distributions is in the range of 10…15 %, since with the relatively high output effective frequency and the ML output voltage waveform, only a small voltage-time area is applied to the inductors.

The final filter structure comprises two *L-C* filter stages, whose star point is connected to the midpoint of the DC-link to provide a return path for the CM current, as shown in **Fig. 4.9**. To mitigate the effects of the unavoidable parasitic capacitance from the switching stage $C_{\mathrm{par,s}}$ to ground, an additional CM-choke is placed before the grid connection terminals and a Y-rated capacitor C_{Y} is connected between earth (PE) and the DC-link midpoint. Finally, *R-C* damping is provided in the second filter stage with damping resistors R_{d} similar to [66], in order to avoid larger damping losses that would arise due to the switching voltage ripple if damping would be installed in the first stage. A list of the main power components used in the hardware prototype and their part numbers can be found in **Table 4.1**.

The volume distribution of the hardware is given in **Fig. 4.11(b)**, where it can be seen that the capacitors are the main volume contributors. The FC capacitance is dimensioned by the minimum capacitance requirement that is obtained by imposing a maximum switching frequency ripple of the FC voltage (see Eq. **(4.5)**), limited here to $\Delta U_{\mathrm{fc,max}} = 5\,\mathrm{V}$. Given the low switching frequency and high output current, the capacitance requirement is large, i.e., 107 µF for capacitors which operate at nominal voltages of 120 V and 240 V. Hence, film capacitors are chosen instead of MLCCs, to avoid the need of having to parallel-connect ≈ 200 capacitors per FC, which would also lead to approximately a × 15 price increase of the capacitors. However, for converters with a lower power rating (and lower load currents) and higher switching frequencies, MLCCs are more suitable, since a higher volumetric energy density can be achieved (cf., **Appendix F** and [30, 48, 49, 125]).

Tab. 4.1: Main components of the final design. The EMI filter component values are given per phase.

Component	Value	Part Number
ANPC Stage Switches	31.0 mΩ	4 paralleled Infineon CoolMOS CFD7 600 V IPW60R031CFD7
FC Stage Switches	11.1 mΩ	2 paralleled Infineon OptiMOS 3 FD 200 V IPT111N20NFD
Gate Driver		10 A Infineon 1EDI60N12AF
L_1	113.3 µH	22 turns, core: F3CC0008 2 mm × 5 mm wire
C_1	2.2 µF	Epcos TDK B32923H3225
L_2	15 µH	Wuerth Elek. 7443641500
C_2	13.2 µF	Epcos TDK B32924D3335
L_{cm}	400 µH (at 100 kHz)	4 turns, 2.5 mm wire Vacuumschmelze 2 x T60006-L2030-W358
C_{dc}	240 µF	Epcos TDK B32776G4406
C_{fc}	120 µF	Epcos TDK B32776G4406
C_Y	40 nF	Epcos TDK B32022A3103
R_d	1.65 Ω	pulse withstanding, through hole

4.4 Hardware Implementation and Measurement Results

To validate the presented calculations and the suitability of the 7L-HANPC topology for ultra-high efficiency applications, the hardware implementation of the 7L-HANPC and the main measurement results will be presented in the following.

The first step to build the 7L-HANPC inverter is to design an optimal bridge-leg layout, especially because switching losses cause a significant

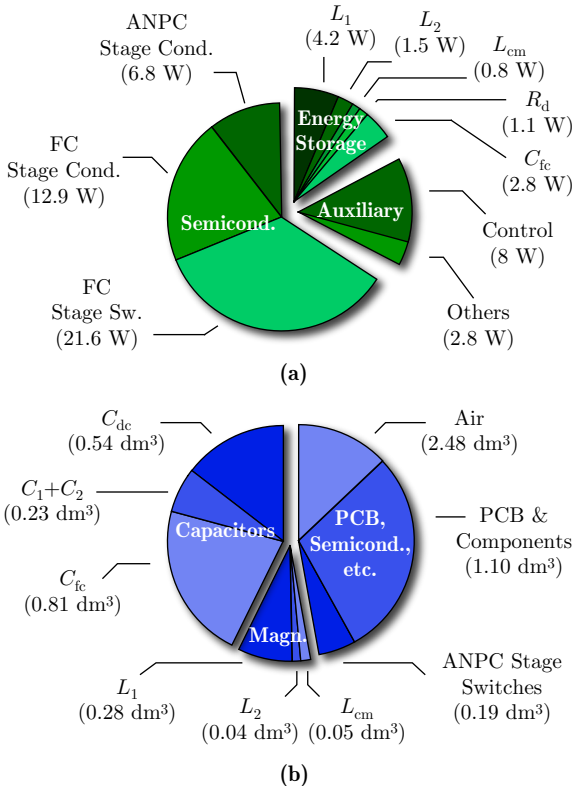

Fig. 4.11: (a) Loss and **(b)** volume distribution of the realized hardware (cf., **Fig. 4.13**), where the loss breakdown is shown for operation at 10 kW.

part of the overall losses and depend to a large extent on layout parasitics [76]. The implemented layout and its schematic arrangement are shown in **Fig. 4.12,** where particular care has to be taken for the FC stage layout. Since there are three FC cells per bridge-leg, there are three switching frequency commutation loops that require attention in the layout, namely L_{c1}, L_{c2} and L_{c3}, out of which L_{c3} is the most critical for two reasons: firstly, the commutation path of L_{c3} always closes through either the upper side or the lower side DC-link capacitor, for which layout symmetry has to be maximized such that L_{c3} is equal for both cases, as seen in **Fig. 4.12**; secondly, given that the high-side and low-side (partial) DC-link voltages are not always equal in value due to

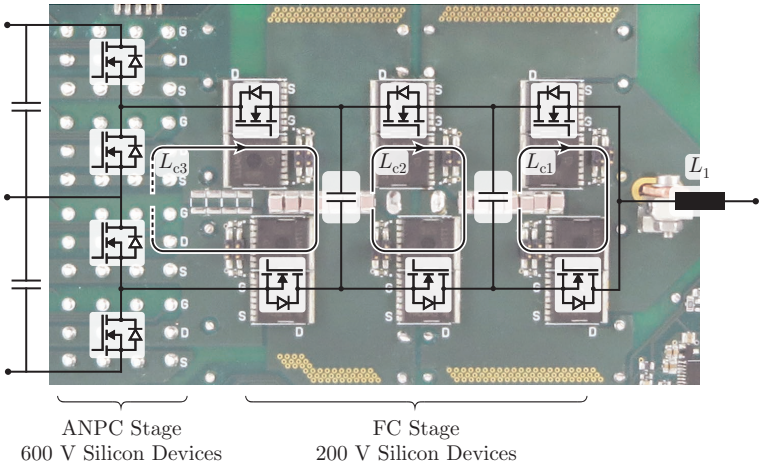

Fig. 4.12: Realization of the hardware layout of a three-phase 7L-HANPC inverter bridge-leg, where the FCs (film-type) are placed underneath the PCB, and ceramic capacitors are placed on top to improve the switching behavior of the MOSFETs. The commutation loop introduced by the connection of the FC stage to the HANPC stage L_{c3} is the most critical.

the nature of the topology, care has to be taken if commutation capacitors are placed between the ANPC stage and FC stage switches. Since two capacitors of unequal voltage, i.e., the respective DC-link capacitor and the commutation capacitor, which has previously been connected to the opposite half DC-link capacitor, would be connected in parallel, current spikes and ringing would occur when commutating the ANPC stage switches. Note that although space is provided to place ceramic capacitors between the ANPC and FC stages, these capacitors were not finally placed in the setup (cf., **Fig. 4.12**). However, L_{c1} and L_{c2} can easily be optimized by placing ceramic (commutation) capacitors in parallel to the (film-type) FCs to reduce the size of the commutation loop (cf., **Fig. 4.12**), keeping the maximum overvoltage of the FC stage switches below 30 V. All the gate drivers are placed on separate PCBs, which on the one hand has the advantage of keeping the power PCB free from the gate driver circuitry for an optimized layout, but on the other hand has the disadvantage of increasing the gate loop inductance. This inductance is minimized by using low-profile board-to-board connectors (*Samtec TMM* and *CLT* types)

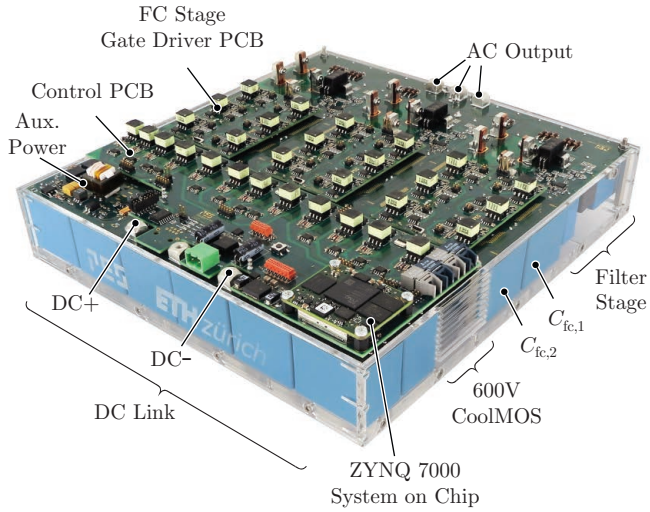

Fig. 4.13: Hardware prototype of the 12.5 kW three-phase 7L-HANPC inverter, measuring 256 mm × 269 mm × 53 mm (10.1 in × 10.6 in × 2.1 in). The final volumetric power density is 3.4 kW/dm³ (55.9 W/in³), and the gravimetric power density is 3.2 kW/kg (1.5 kW/lb).

that result in a distance between the PCBs of only 2.77 mm (0.11 in). Each switch gate drive has its own isolated power supply, for which dedicated transformers are used to obtain isolated gate voltages of 15 V and -5 V.

4.4.1 Hardware Implementation

The 12.5 kW hardware demonstrator shown in **Fig. 4.13**, features a volumetric power density of 3.4 kW/dm³ (55.9 W/in³) and a gravimetric power density of 3.2 kW/kg. It has to be noted that, for the presented measurements, four power MOSFETs were connected in parallel for implementing each switch of the ANPC stage, however, space was provided in the layout to accommodate a total of six parallel switches.

Given the high efficiency nature of the converter, there is no need for active cooling, and hence, neither fans nor heat sinks are required, thus minimizing the implementation effort and increasing the overall reliability of the system. This is particularly true for the converter at hand, where the semiconductor losses are distributed among many switches: the estimated

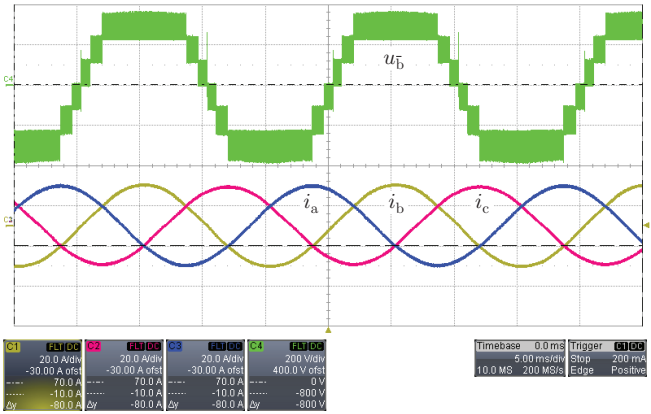

Fig. 4.14: Measurements of the 7L output voltage of a bridge-leg of the 7L-HANPC inverter shown in **Fig. 4.13** (200 V/div, referenced to the DC-link midpoint, 5 ms/div) and the three phase mains currents (20 A/div) during operation at 10 kW. The experimental waveforms are in accordance with the simulation results shown in **Fig. 4.6.**

losses of a single ANPC stage switch, housed in a TO-247 three-lead package, are of 0.14 W on average, whereas the losses for an individual SMD FC stage switch are 0.96 W. Experimental measurements yield that at thermal steady-state during operation at 10 kW and an ambient temperature of 40 °C, the 600 V switches housed in a though-hole TO-247 package have a case temperature of 64.8 °C, and that the 200 V switches housed in a HSOF SMD package have a case temperature of 69.3 °C, resulting in a case-to-ambient thermal resistance of 175 °C/W and 36 °C/W, and junction temperature of 64.9 °C and 69.7 °C respectively.

4.4.2 Experimental Waveforms

The main measured waveforms taken with a resistive load (i.e., operating the system in inverter mode) are presented in **Fig. 4.14** for 10 kW operation, where the unfiltered 7L phase voltage measured at the output node $\bar{b}$ with respect to the DC-link midpoint and the three phase currents are shown. The voltage spikes that can be seen during the voltage zero crossings are due to the unequal switching times of the ANPC stage and FC stage switches, and last only for some few tens of nanoseconds not affecting the overall system performance. The DC-link voltage midpoint is controlled by superimposing

a third harmonic to the sinusoidal modulation of one fourth of the output voltage amplitude (cf., **Fig. 4.6**), achieving a low maximum instantaneous voltage deviation between the upper half and the lower half of the DC-link of 8.9 V during nominal operation. The FC voltages are naturally balanced by phase shifted PWM [122] at their nominal voltages, i.e., at average values of $U_{\mathrm{fc},2}$ =240.5 V and $U_{\mathrm{fc},1}$ =120.9 V for the operating point of **Fig. 4.14**.

4.4.3 Efficiency Measurements

The efficiency of the three-phase 7L-HANPC inverter is measured both calorimetrically, with the calorimeter presented in [44], and electrically, with a *Yokogawa WT3000* precision power analyzer. The efficiency measurement results of both methods are reported in **Fig. 4.15**, together with the calculated efficiency at U_{dc} = 720 V. A peak efficiency of 99.35 % is achieved for U_{dc} = 650 V, and 99.30 % for U_{dc} = 720 V, where all the converter losses are considered, including those of the EMI filter stage and the auxiliary power. The fitted European weighted efficiency is 99.10 %, whereas the California Energy Commission (CEC) weighted efficiency is 99.20 % [23]. Since electrical power measurements with precision power analyzers have a large efficiency

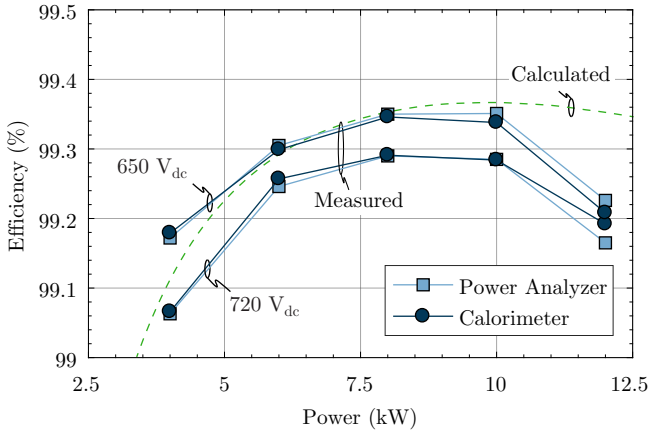

Fig. 4.15: Measured efficiency of the hardware demonstrator (cf., **Fig. 4.13**) reaching peak values of 99.35 % for U_{dc} = 650 V and 99.30 % for U_{dc} = 720 V, and calculated efficiency characteristic for U_{dc} = 720 V. All efficiency measurements are taken at a controlled ambient temperature of 40 °C.

error band ($\Delta\eta$ = ±0.38 % at 10 kW, leading to the uncertainty of the efficiency measurement to be between η = 98.92…99.68 %, cf., **Appendix E**), also calorimetric measurements were performed in order to accurately determine the overall efficiency. The calorimetric approach measures the power losses with a relative error smaller than 1 % for the whole range where measurements were taken [44], leading to an efficiency accuracy of $\Delta\eta$ = ±0.0065 %. The efficiency measurement points presented in **Fig. 4.15** are taken with the converter at thermal steady-state inside the inner chamber of the calorimeter, which is controlled to have an ambient temperature of 40 °C, resulting in 2 to 3 hours of continuous operation for each efficiency measurement point. However, it has to be noted that the electric and the calorimetric loss measurements match very well, as also shown in [66], from which it can be concluded that the actual accuracy of the power analyzer is substantially higher than specified in the datasheet. An in-depth comparison of the electric and calorimetric measurement methods is provided in the **Appendix E**.

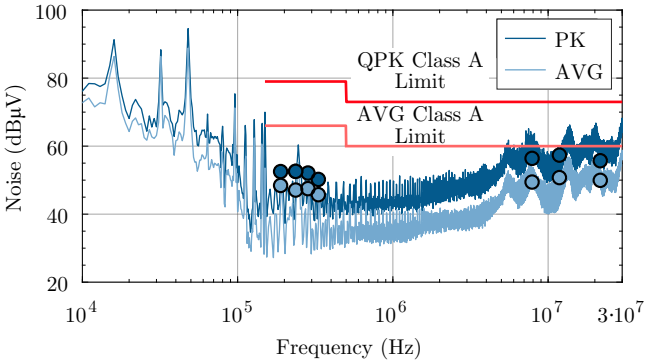

Fig. 4.16: Conducted EMI noise emission spectrum of the hardware demonstrator presented in **Fig. 4.13**, where the CISPR 11 peak and average detectors are used with a 1 kHz step, 200 Hz bandwidth, and 50 ms measurement time for frequencies <150 kHz and a 4 kHz step, 9 kHz bandwidth, and 10 ms measurement time for frequencies ≥150 kHz. Selected peaks (markers) have been measured with quasi-peak and average detectors for a measurement time of 1 s.

4.4.4 Conducted EMI Measurements

The results of the conducted EMI emissions measurement are presented in **Fig. 4.16**, for the frequency range between 10 kHz and 30 MHz. Two different scans are shown, the first one with the peak and average detector for a measurement time of 50 ms for frequencies <150 kHz, and 10 ms measurement time for frequencies ≥150 kHz, and a second one, with the quasi-peak and average detector at selected frequencies for a measurement time of 1 s (see the rounded markers in **Fig. 4.16**). It has to be noted, that for the effective switching frequency (48 kHz) resulting from the converter optimization described in **Section 4.3**, the filter dimensioning is limited by the need of sufficiently separating the filter resonance frequency and the effective switching frequency, in order to not excite any filter resonance, and not by the EMI filtering requirements. This can be seen in **Fig. 4.16**, since for the first harmonic above 150 kHz, the attenuation margin is well above the 10 dBµV for which the EMI filter design space was restricted in the optimization.

4.5 Summary

In this chapter, a 99.35 % efficient 3.4 kW/dm³ (55.9 W/in³) all-Si 7L three-phase inverter is presented, setting a new benchmark for ultra-high efficient and power-dense converters. A topological alternative to the conventional FCC is employed, which has the advantage of halving the amount of FC cells by making use of a DC-link midpoint connection, and an ANPC stage front-end that uses switches rated for half the DC-link voltage and is switching at grid frequency. Substantial volume savings are obtained by halving the number of FC cells, particularly for the case of low switching frequencies, since the capacitance requirement to guarantee a certain voltage ripple of the FCs is inversely proportional to the switching frequency, which is limited for ultra-efficient converters. Additionally, no active cooling is required given the high efficiency of the system and the fact that the losses are spread among many switches and/or power components, reducing the design effort and increasing reliability.

With recently available 18 mΩ 600 V *CoolMOS CFD7* power MOSFETs (*Infineon*), which have a lower on-state resistance compared to the 31 mΩ switches used in this work, the efficiency and/or volume could be further improved, as the switching losses are negligible at grid frequency. Furthermore, a comprehensive optimization shows that it is feasible to reach the boundary of 99.5 % efficiency with *next generation* 200 V Si devices (engineering samples

on which preliminary measurements were taken in [65]), and 99.6 % with state-of-the-art GaN devices.

Finally, in order to gain a fundamental insight as to why three-phase 800 V_{dc} systems that interface 230 V_{rms} phase voltages require ML approaches to achieve ultra-high efficiency, whereas single-phase 400 V_{dc} systems that generate the same 230 V_{rms} phase voltage achieve e.g., 99.1 % efficiency with simple 2L approaches [132], an in-depth analysis is done in **Appendix F**.

5

New Synergetic Control of a 20 kW Isolated VIENNA Rectifier Front-End EV Battery Charger

This chapter summarizes the most relevant findings concerning a new coordinated control of two-stage three-phase EV charger systems also published in:

- **J. Azurza Anderson**, M. Haider, D. Bortis, J. W. Kolar, M. Kasper, G. Deboy, "New synergetic control of a 20 kW isolated VIENNA rectifier front-end EV battery charger," in *IEEE Proc. of the Workshop on Control and Modeling for Power Electronics (COMPEL)*, Toronto, Canada, 2019.

Motivation

Three-phase EV chargers in the tens of kW range are typically built in a two-stage architecture, i.e., an AC/DC stage followed by a DC/DC stage, where both operate decoupled from each other. Employing the same two-stage solution, a novel synergetic control method is presented, whereby with coupling the control of both phases a large loss saving potential is identified.

Executive Summary

EV chargers with output power levels in the range of tens of kW are typically employing a front-end three-phase boost-type PFC rectifier stage for sinusoidal input current and DC-link voltage control, and a series-connected isolated DC/DC converter controlling the actual output/charging current or voltage. This chapter explores a new synergetic control of both converter stages, which utilizes the DC/DC converter also for varying the DC-link voltage with six times the mains frequency, such that the currents of two mains phases are shaped sinusoidally. Accordingly, two bridge-legs of the rectifier stage can remain clamped in 60 °-wide intervals of the mains cycle and the pulse width modulation (PWM) can be restricted to the phase carrying the lowest current, i.e., only one of the three bridge-legs is operated with PWM, designated as 1/3-PWM. Furthermore, the DC-link voltage that is switched by the operating rectifier phase is kept to the minimum and the system features high efficiency and low EMI, but still maintains boost capability, i.e., the option of conventional PWM of all three rectifier bridge-legs (thus denominated as 3/3-PWM), which is advantageous in case a wide input or output voltage range is still provided. The new control concept is derived starting from a conventional approach with constant DC-link voltage, and is verified by simulations for a three-level Vienna Rectifier (VR) front-end and two cascaded DC/DC modules supplied from the halves of the symmetrically partitioned DC-link voltage. First, the operating behavior of the system utilizing the proposed control is described analytically. Next, the performance improvement achievable with the proposed control scheme is comparatively evaluated for a 20 kW system designed for operation in a wide mains voltage range (260-530 V_{rms} line-to-line) and an extremely wide DC output / battery voltage range (150-750 V_{dc}), according to EV charging equipment supplier requirements of the State Grid Corp. of China. Finally, simulation results are presented which validate the operating principle of the proposed modulation and control scheme.

5.1 Introduction

High-power EV battery chargers are supplied from the three-phase mains (e.g., 400 V_{rms} or 480 V_{rms} line-to-line) and are typically built using a boost-type PFC rectifier input stage ensuring sinusoidal mains current control and delivering a constant DC-link voltage 650-800 V_{dc} to a series-connected isolated DC/DC converter stage, which finally generates the required output voltage and/or battery charging current. In this way the operation and control of both converter stages is largely decoupled and both stages can be commissioned separately.

A well-known and widely used realization of the aforementioned concept is depicted in **Fig. 5.1** [133]. The system employs a 3L VR input stage, which

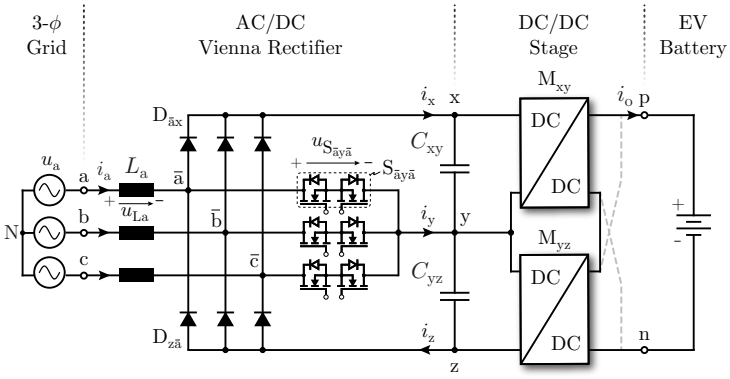

Fig. 5.1: Circuit diagram of a typical three-phase/level PFC rectifier mains interface (Vienna Rectifier) with an isolated DC/DC output stage, comprising individual converter modules, which can either be connected in series- or parallel-configuration at the output. Optionally, an additional active series/parallel rearrangement of the DC/DC converter modules can be implemented to optimally adapt the conversion ratio between DC-link and output voltage, i.e., limiting the requirements on voltage and current capabilities of the DC/DC converter modules.

features low magnetics volume and provides a symmetrically partitioned (constant) DC-link voltage (cf., **Fig. 5.3**), such that the DC/DC converter stage can be split into two cascaded converter modules M_{xy} and M_{yz}. This approach allows to benefit from 600 V semiconductor and converter technologies known, e.g., from high-power datacenter power supply modules. Furthermore, a series/parallel rearrangement of the outputs of M_{xy} and M_{yz} could be used to cover the extremely wide output voltage range required for future EV chargers (150-750 V_{dc}, cf., **Fig. 5.2** [134]).

However, considering that the voltage control function is implemented twice, i.e., for the output of the PFC rectifier stage and for the output of the DC/DC converter supplying the charging current, the question arises if a synergy of the control of both stages could be found, which would allow to reduce the overall realization effort and costs.

An according approach, which limits the functionality of the input stage to pure rectifier and/or mains frequency commutated three-phase unfolder operation and generates two cascaded time varying DC-link voltages which are supplying two cascaded DC/DC converters responsible for input current shaping and output voltage control, has been analyzed in [135, 136] (based on [137–139]). Characteristic waveforms are shown in **Fig. 5.4**. However, the

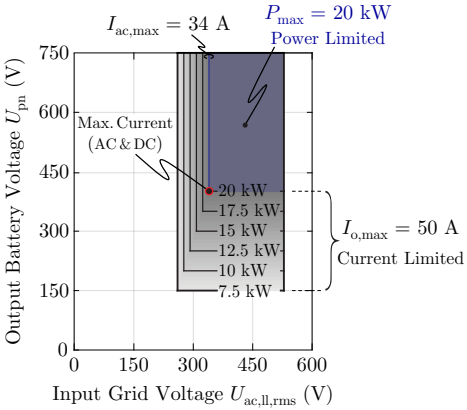

Fig. 5.2: Wide-input and wide-output voltage range specification for the 20 kW EV charger at hand, where for a nominal line-to-line voltage of $U_{ac,ll,rms}$ = 400 V, the converter has to be able to provide full output current (I_o = 50 A) for output DC voltages below U_{pn} = 400 V, and thereafter has to be capable of delivering full power (P_o = 20 kW) until reaching the maximum output DC voltage U_{pn} = 750 V.

cascaded voltages u_{xy} and u_{yz} are widely varying and differing, which results in relatively high voltage stresses on the DC/DC converter and unfolder power semiconductors. E.g., for a 480 V_{rms} + 10 % line-to-line three-phase mains the maximum blocking voltage reaches $\frac{\sqrt{3}}{2} \cdot \hat{U}_{ac,ll}$ = 647 V, i.e., 600 V semiconductors cannot be employed any more. Furthermore, the boost functionality of the rectifier stage is not any more available, as the boost inductors at the input side are omitted for this concept [135, 136]. Accordingly, DC/DC converter modules with extremely wide voltage transfer ratio range are required, which results in overdesign and impairs efficiency and power density. Furthermore, each DC/DC converter module has to be designed to temporarily operate at full power, and a limited input current quality has to be accepted, as no direct mains current control is performed.

Therefore, this chapter proposes an alternative concept of synergetic control of the rectifier and DC/DC converter stage, where the basic power circuit structure of **Fig. 5.1** is fully kept, and cascaded DC-link voltages of equal value are generated. Furthermore, the current control of one mains phase, i.e., of the phase carrying the lowest current is maintained by pulse width modulation (PWM) of the corresponding bridge-leg within 60 °-intervals around the current zero crossings [108, 134, 140–146]. The currents of the two other

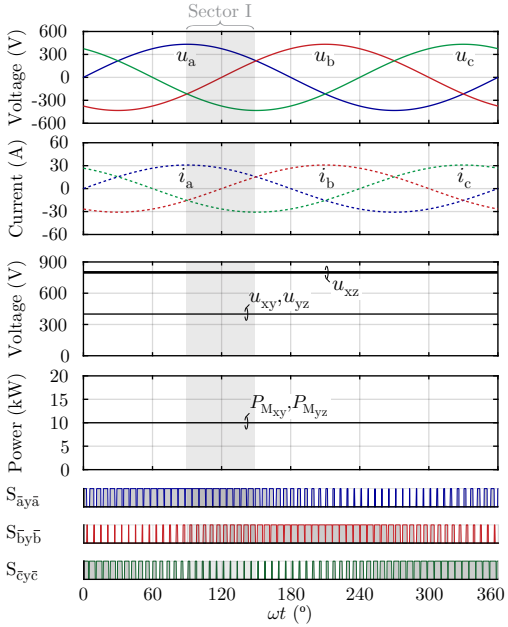

Fig. 5.3: Characteristic waveforms of the three-phase/level PFC rectifier and isolated DC/DC output stage (cf., **Fig. 5.1**) presented for the highest specified input voltage ($U_{ac,ll,max}$ = 530 V) and operation at 20 kW for a conventional control and modulation scheme of boosting the input mains voltage to a DC-link voltage of 800 V, by pulse width modulating all three rectifier stage bridge-legs (3/3-PWM) and subsequent decoupled equal-power operation of the DC/DC modules.

phases, which are clamped to the positive and negative DC bus through the rectifier diodes (the associated bidirectional switches remain in the off-state), are controlled by the DC/DC converter modules M_{xy} and M_{yz} resulting in a six-pulse (six times mains frequency) DC-link voltage shape (cf., **Fig. 5.5**). Consequently, this synergetic control scheme is designated as 1/3-PWM, since only one bridge-leg of the three-phase VR front-end is pulse width modulated. In addition, the DC/DC converter modules are ensuring an equal splitting of the total DC-link voltage such that the maximum voltage on the semiconductors (for a 480 V_{rms} + 10 % mains) is only $0.5 \cdot \hat{U}_{ac,ll}$ = 374 V, allowing the use of 600 V semiconductor technology which can be implemented by an anti-series configuration of two discrete switches, or by recently introduced monolithic bidirectional GaN HEMTs [147, 148].

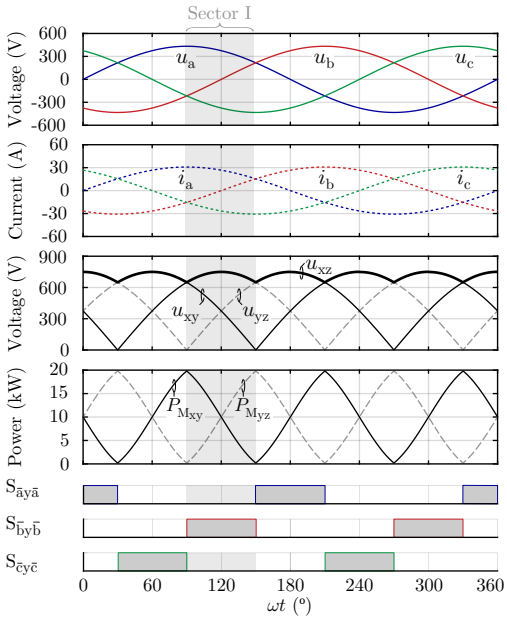

Fig. 5.4: Characteristic waveforms of the three-phase/level PFC rectifier and isolated DC/DC output stage (cf., **Fig. 5.1**) presented for the highest specified input voltage ($U_{ac,ll,max}$ = 530 V) and operation at 20 kW for the control and modulation scheme presented in [135–137, 139] where the three-phase/level front-end is operated as a three-phase unfolder and the isolated DC/DC modules are controlled to behave as current sources generating piecewise sinusoidal currents that are defining the mains current.

As the boost inductors remain on the AC-side, the above-described mode of operation, which directly connects always the highest AC-side line-to-line voltage (and/or sum of the two lower value line-to-line voltages) in 60 °-wide intervals to the DC-link, can also be changed into a partial-boost mode or a full-boost mode, where all three rectifier bridge-legs are operated with PWM, thus denominated as 3/3-PWM, in case a high output voltage needs to be generated or a low mains voltage is present. This allows to reduce the voltage conversion ratio requirement of the DC/DC converter modules and/or results in higher efficiency and power density. Further details of the operation of the system, which is denominated as *SynC-VR-i* (*Synergetically Controlled*

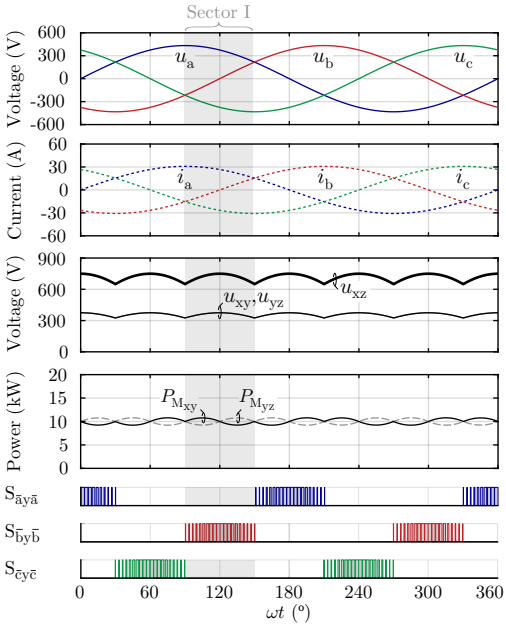

Fig. 5.5: Characteristic waveforms of the three-phase/level PFC rectifier and isolated DC/DC output stage (cf., **Fig. 5.1**) presented for the highest specified input voltage ($U_{ac,ll,max}$ = 530 V) and operation at 20 kW for the proposed synergetic control scheme that combines 1/3-PWM (pulse width modulation of one of the phases [134, 140, 142–145]) with six-pulse control of the DC-link voltages through the DC/DC modules, ensuring sinusoidal input currents and equal voltage sharing of the DC-link capacitors, besides a controlled DC output voltage.

Vienna Rectifier with *i*solated DC/DC converter output stage), are given in the following Sections.

The chapter is organized as follows: **Section 5.2** discusses the operation principle of the SynC-VR-i, and **Section 5.3** describes the corresponding control structure. **Section 5.4** shows simulation results of the new control method proving its correct functionality, while **Section 5.5** presents an analytic and quantitative comparison of the semiconductor stresses. Finally, the main conclusions are presented in **Section 5.6**.

5.2 Operation Principle of the SynC-VR-i

Due to the three-line supply of the three-phase PFC rectifier stage (cf., **Fig. 5.1**), it is sufficient to independently control only two phase currents, e.g., i_a and i_c for the following considerations, as the third current (e.g., i_b) is directly defined by KCL (Kirschoff's Current Law), i.e., $i_b = -(i_a + i_c)$. For controlling two phase currents two degrees of freedom are required, i.e., two line-to-line voltages of the rectifier stage, $u_{\overline{ab}}$ and $u_{\overline{bc}}$, have to be generated accordingly at any point in time, as this, together with the given mains voltage (u_{ab} and u_{bc}) and the KCL, fully determines the voltages u_{L_a}, u_{L_b} and u_{L_c} applied across the input inductors L_a, L_b and L_c, which finally determine the input currents.

Given that the mains frequency components of the inductor voltages u_{L_a}, u_{L_b} and u_{L_c} are small (operation at high switching frequency resulting in a low inductance value), the local average values $\overline{u}_{\overline{a}}$, $\overline{u}_{\overline{b}}$ and $\overline{u}_{\overline{c}}$ of $u_{\overline{a}}$, $u_{\overline{b}}$ and $u_{\overline{c}}$, are almost equal to the grid voltages u_a, u_b and u_c. Consequently, assuming input currents which are in phase with the mains phase voltages, the conduction state of the diode bridge-legs of phases *a* and *c* only depends on the sign of the actual mains phase voltages u_a and u_c. Therefore, considering, e.g., *Sector I* in **Fig. 5.5**, the upper diode of phase *a*, showing the most positive phase voltage (u_a) and the lower diode of phase *c*, showing the most negative phase voltage (u_c), are always conducting. Accordingly, the total DC-link voltage $u_{xz} = \overline{u}_{\overline{ab}} + \overline{u}_{\overline{bc}}$ always follows the largest line-to-line voltage, i.e., $u_{xz} = \overline{u}_{\overline{ac}} \approx u_{ac}$, and exhibits a six-pulse shape as shown in **Fig. 5.5**.

All in all, the DC-link voltage u_{xz} (= $u_{\overline{ac}}$ in *Sector I*) has to be adjusted with respect to the actual maximum line-to-line voltage u_{ac}. For the proposed synergetic control method, the DC-link voltage is controlled by properly defining the power consumption of the subsequent DC/DC converter modules M_{xy} and M_{yz}.

However, only controlling the DC-link voltage would mean that only in the most positive and most negative phase equal currents with opposite signs would be flowing and, the current in phase *b* (*Sector I*) would be zero, i.e., no sinusoidal set of three phase currents would result. Hence, a current has to be impressed in the middle phase, which in each sector is proportional to the middle phase voltage, in order to obtain three sinusoidal phase currents. As shown in **Fig. 5.7**, this current always equals the minimum absolute phase current, which is symmetric around zero, and features a quasi triangular shape for PFC operation, i.e., within one 60 °-wide voltage sector the current is positive for 30 ° and negative for the other 30 °. Depending on the momentary voltage sector, this current can be controlled by always pulse

width modulating the bidirectional switch $S_{\bar{a}y\bar{a}}$, $S_{\bar{b}y\bar{b}}$ or $S_{\bar{c}y\bar{c}}$ corresponding to the middle phase voltage, i.e., $S_{\bar{b}y\bar{b}}$ for *Sector I*.

During the turn-on phase of the pulse width modulated bidirectional switch, the switch node of the corresponding rectifier stage bridge-leg is directly connected to the DC-link midpoint y, regardless of the current direction in the middle phase. However, during the turn-off phase, the resulting bridge-leg voltage actually depends on the current direction, hence the possible voltage levels of the bridge-leg of the middle phase, $u_{\bar{b}}$ for *Sector I*, are limited by the current direction in the inductor L_b. For $i_b > 0$, the switch node $\bar{b}$ can only be actively connected to the DC-link midpoint by closing $S_{\bar{b}y\bar{b}}$, and when $S_{\bar{b}y\bar{b}}$ is opened, the current commutates to the upper diode $D_{\bar{b}x}$. Consequently, since $\bar{c}$ is connected to the negative DC-link rail z, the voltage $u_{\overline{bc}}$ equals $u_{xz}/2$ when $S_{\bar{b}y\bar{b}}$ is closed and u_{xz} when $S_{\bar{b}y\bar{b}}$ is open, assuming that the DC-link voltage is equally split, i.e., $u_{xy} = u_{yz} = u_{xz}/2$. Accordingly, since the duty cycle of $S_{\bar{b}y\bar{b}}$ is limited between 0 and 1, the local average of the line-to-line voltage $u_{\overline{bc}}$ that can be generated for positive i_b is constrained between $u_{xz}/2$ ($= u_{\overline{ac}}/2$) and u_{xz} ($= u_{\overline{ac}}$). Hence, in order to be able to control the phase current in the middle phase (i_b) to a positive value, the local average of the line-to-line voltage u_{bc} must be larger or equal to $u_{\overline{ac}}/2$.

In analogy, for negative currents in phase b in *Sector I*, $\bar{b}$ can either be actively connected to the DC-link midpoint, or assumes the voltage of the negative rail z of the DC-link through the diode $D_{z\bar{b}}$. Given again the limitation of the duty cycle of $S_{\bar{b}y\bar{b}}$ between 0 and 1, the local average of the line-to-line voltage $u_{\overline{bc}}$ that can be generated for negative currents in this case is constrained between $u_{xz}/2$ ($= u_{\overline{ac}}/2$) and 0, and hence, the local average of u_{bc} must be smaller or equal than $u_{\overline{ac}}/2$. Consequently, for the described modulation scheme, the control is limited to pure PFC rectifier operation where u_{bc} actually equals $u_{\overline{ac}}/2$.

Based on these considerations, now the duty cycle of $S_{\bar{b}y\bar{b}}$ can be easily calculated for steady-state operation, which means that within one switching period in average effectively no voltage is applied to the inductors, i.e., $u_{bc} \approx u_{\overline{bc}}$ for *Sector I*. Assuming a local averaging, the voltage $u_{\overline{bc}}$ can be written for positive currents i_b as $u_{\overline{bc}} = d_{S_{\bar{b}y\bar{b}}} \cdot u_{xz}/2 + (1 - d_{S_{\bar{b}y\bar{b}}}) \cdot u_{xz}$, while for negative currents it is just given as $u_{\overline{bc}} = d_{S_{\bar{b}y\bar{b}}} \cdot u_{xz}/2$. Furthermore, considering that in *Sector I* the DC-link voltage u_{xz} equals the line-to-line voltage u_{ac}, yields that the duty cycles of $S_{\bar{b}y\bar{b}}$ are

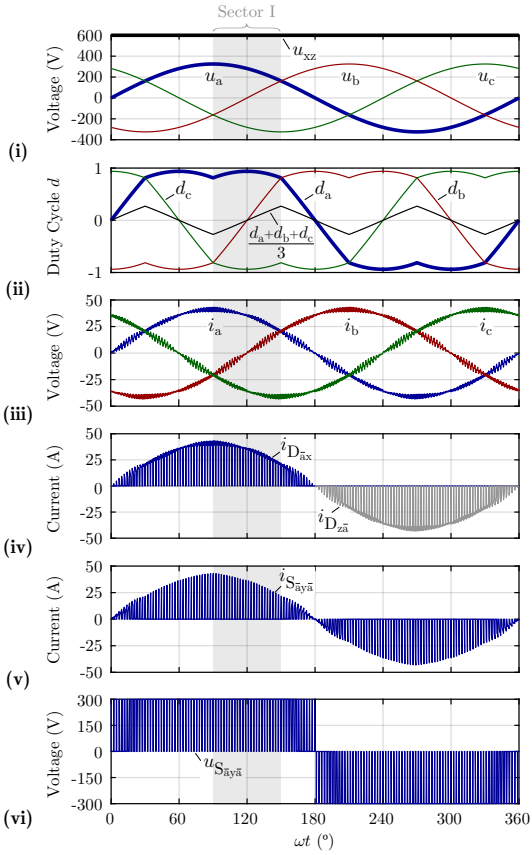

Fig. 5.6: Characteristic waveforms for full-boost mode with 3/3-PWM, where all three bridge-legs are pulse width modulated. From top to bottom: **(i)** input grid voltages u_i for $i = \{a,b,c\}$ together with the DC-link voltage u_{xz}, **(ii)** phase-leg duty cycles d_i and common-mode (zero sequence) duty cycle (where $d_i = 1$ implies that the diode $D_{\bar{i}x}$ is clamping the phase-leg to the positive rail x of the DC-link, and $d_i = -1$ implies that the diode $D_{z\bar{i}}$ is clamping the phase-leg i to the negative rail z of the DC-link), **(iii)** mains (input) phase currents $i_{\{a,b,c\}}$, **(iv)** currents of the VR diodes for phase a, $i_{D\bar{a}x}$ and $i_{Dz\bar{a}}$, **(v)** current through the switch $S_{\bar{a}y\bar{a}}$, and **(vi)** voltage $u_{S_{\bar{a}y\bar{a}}}$ across the switch $S_{\bar{a}y\bar{a}}$. For illustration purpose, the waveforms are calculated for a low switching frequency of 7.5 kHz and an input inductance of $L_{\{a,b,c\}} = 700\,\mu H$.

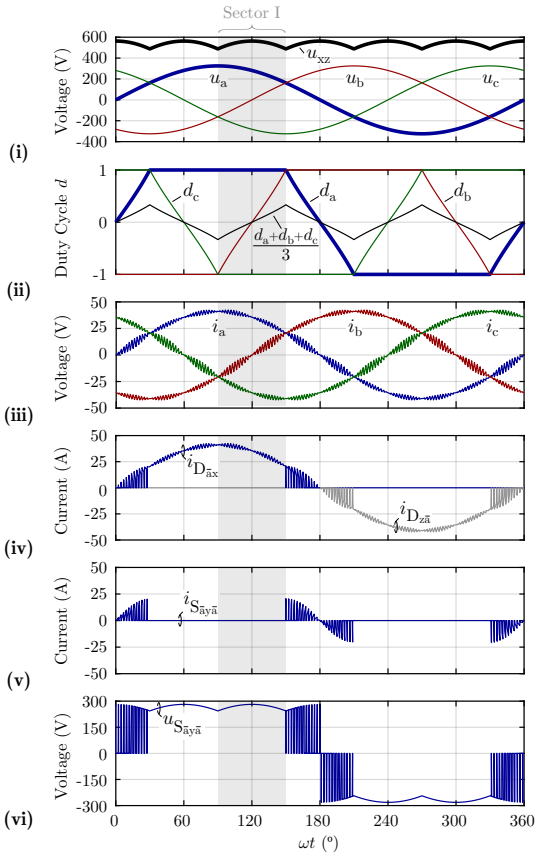

Fig. 5.7: Characteristic waveforms for 1/3-PWM operation. From top to bottom: **(i)** input grid voltages u_i for $i = \{a,b,c\}$ together with the DC-link voltage u_{xz}, **(ii)** phase-leg duty cycles d_i and common-mode (zero sequence) duty cycle (where $d_i = 1$ implies that the diode $D_{\bar{i}x}$ is clamping the phase-leg to the positive rail x of the DC-link, and $d_i = -1$ implies that the diode $D_{z\bar{i}}$ is clamping the phase-leg i to the negative rail z of the DC-link), **(iii)** mains (input) phase currents $i_{\{a,b,c\}}$, **(iv)** currents of the VR diodes for phase a, $i_{D\bar{a}x}$ and $i_{Dz\bar{a}}$, **(v)** current through the switch $S_{\bar{a}y\bar{a}}$, and **(vi)** voltage $u_{S_{\bar{a}y\bar{a}}}$ across the switch $S_{\bar{a}y\bar{a}}$. For illustration purpose, the waveforms are calculated for a low switching frequency of 7.5 kHz and an input inductance of $L_{\{a,b,c\}} = 700\,\mu H$.

$$\begin{cases} d_{S_{\overline{byb}}} = 2 \cdot \dfrac{u_{\overline{bc}}}{u_{\overline{ac}}} & \text{for} \quad i_b < 0 \\ d_{S_{\overline{byb}}} = 2 \cdot \left(1 - \dfrac{u_{\overline{bc}}}{u_{\overline{ac}}}\right) & \text{for} \quad i_b > 0\,. \end{cases} \tag{5.1}$$

In a next step, the low frequency current component that flows through the bidirectional switches to the DC-link midpoint i_y can be determined by multiplying the phase current in the middle phase (i_b) with the duty cycle of the bidirectional switches, e.g., $i_y = d_{S_{\overline{byb}}} \cdot i_b$ in the case of *Sector I*. Since the duty cycle is always smaller than one, and the current in the middle phase is already low, the product of these two values leads to an even smaller current i_y, especially since when i_b is maximum, the duty cycle $d_{S_{\overline{byb}}}$ is zero (cf., **Fig. 5.7**). This current i_y multiplied by half the DC-link voltage actually determines the power mismatch drawn by the two series-connected DC/DC modules, which due to the small value of i_y, is very low (a maximum of ±800 W occurs for each converter module for 20 kW operation). Therefore both DC/DC converter modules are processing half the power ±8 % and can be designed accordingly, as opposed to [135, 136], where the DC/DC converter modules have to alternatingly process the full output power.

5.3 Control Strategy of the SynC-VR-i

A detailed schematic of the cascaded control consisting of three essential functional blocks is shown in **Fig. 5.8**. The first main block is the output current controller, which shows the lowest bandwidth of all controllers, and sets the output current reference I_o^*. By measuring the output voltage U_{pn}, the required power to be drawn from the mains is calculated. From this, the converter's input conductance G^* is determined, which together with the measured input voltages defines the reference phase currents that are compared with the measured phase currents. The input current control errors are then fed to the input current controller, which outputs the needed voltages across the input inductors, $u_{L_a}^*$, $u_{L_b}^*$ and $u_{L_c}^*$ (note that these are locally averaged values), and together with the mains phase voltages sets a reference for each AC terminal voltage $u_{\overline{a}}^*$, $u_{\overline{b}}^*$ and $u_{\overline{c}}^*$ of the rectifier stage. Based on these reference values, on the one hand, the actual voltage sector, and on the other hand, the line-to-line voltages in between the rectifier bridge AC terminals, $u_{\overline{ab}}^*$, $u_{\overline{bc}}^*$ and $u_{\overline{ca}}^*$, are derived in order to calculate the duty cycles of the bidirectional switches (cf., Eq. **(5.1)**). In addition, the maximum line-

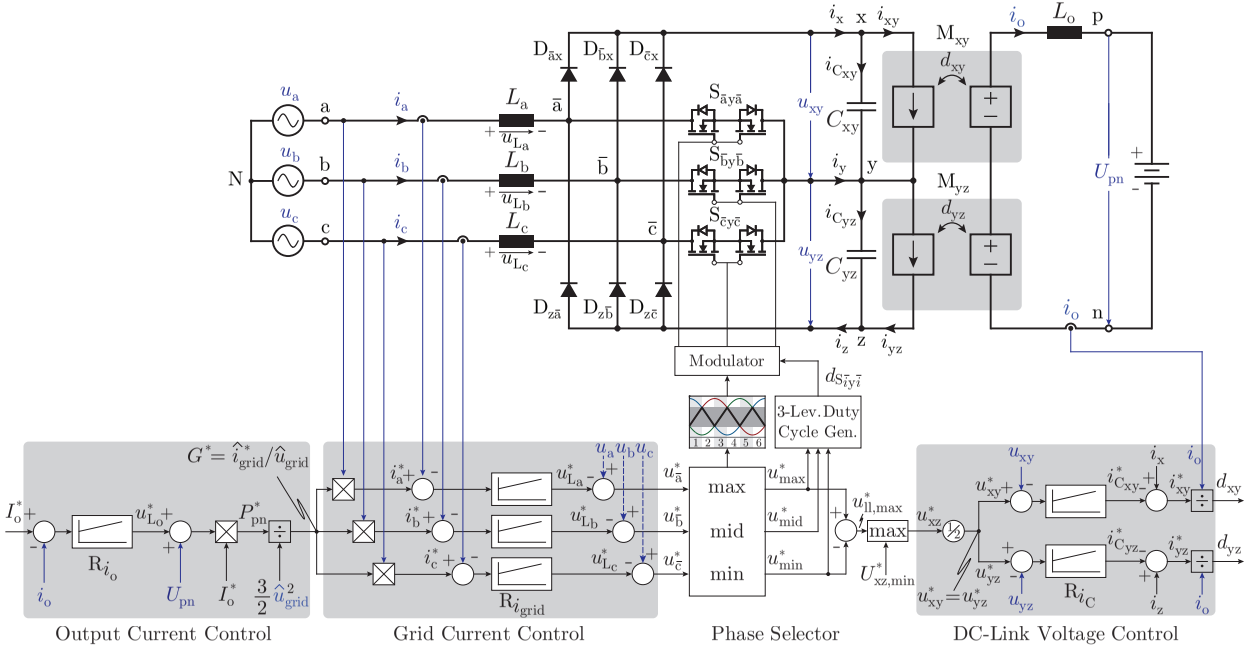

Fig. 5.8: Cascaded battery/output current control structure of the SynC-VR-i, where measurement values are displayed in blue, and the isolated DC/DC converter modules are replaced by equivalent dependent current and voltage sources. Note that the voltage transfer ratio of the DC/DC converter modules is considered to be 1:1 for simplicity.

to-line voltage, $u^*_{\mathrm{ll,max}} = u^*_{\mathrm{max}} - u^*_{\mathrm{min}}$, directly determines the DC-link voltage reference for 1/3-PWM operation. This reference voltage, however, first has to be compared with the minimum DC-link voltage setpoint $U^*_{\mathrm{xz,min}}$, which has to be larger than the required output voltage of the DC/DC converter stage, $U_{\mathrm{pn}} + u^*_{\mathrm{L_o}}$, in order to be able to control the load current I_{o}, and can be arbitrarily increased in order to utilize the DC/DC converter modules in a more favorable operating point concerning overall system efficiency.

As long as this voltage setpoint is below the actual maximum of the line-to-line voltage, i.e., $U^*_{\mathrm{xz,min}} < u^*_{\mathrm{ll,max}}$, the VR front-end can be operated with 1/3-PWM; on the other hand, if $U^*_{\mathrm{xz,min}} > u^*_{\mathrm{ll,max}}$, the VR front-end has to boost the input voltages to $U^*_{\mathrm{xz,min}}$ by switching all three bridge-legs, i.e., 3/3-PWM operation. Consequently, the DC-link voltage reference value u^*_{xz} provided to the DC-link voltage controller always equals the maximum of two references, $U^*_{\mathrm{xz,min}}$ and $u^*_{\mathrm{ll,max}}$. This voltage is then multiplied with 1/2 and serves as reference value for the two DC-link capacitor voltage controllers, which finally control the transferred power of each DC/DC converter module. Hence, the two DC-link voltage controllers translate the DC-link voltage control error into a charging/discharging current $i_{\mathrm{C_{xy}}}$ and $i_{\mathrm{C_{yz}}}$ of the DC-link capacitors C_{xy} and C_{yz} in order to track the DC-link voltage reference. Finally, the currents $i_{\mathrm{C_{xy}}}$ and $i_{\mathrm{C_{yz}}}$, where optionally the load state, i.e., i_{x} and i_{z} can be fed forward, are divided by the measured output current i_{o}, resulting in the duty cycles d_{xy} and d_{yz} of the two DC/DC converter modules.

5.4 Simulation Results

The presented operation principle and proposed synergetic control strategy are verified with a closed-loop circuit simulation. The waveforms of the converter operating at 20 kW output power and $U_{\mathrm{ac,ll,rms}} = 400$ V input voltage are shown in **Fig. 5.9** for an output voltage of $U_{\mathrm{pn}} = 400$ V and a controlled output current of $i_{\mathrm{o}} = 50$ A. Starting with 1/3-PWM operating mode, the minimum DC-link voltage setpoint $U^*_{\mathrm{xz,min}}$ is gradually increased until 600 V, which means that the controller has to transition from 1/3-PWM operation to partial-boost mode, and finally to full-boost mode, i.e., 3/3-PWM operation.

- **1/3-PWM Mode**
  As already mentioned, as long as the DC-link voltage setpoint $U^*_{\mathrm{xz,min}}$ is lower than the minimum of the six-pulse reference voltage $u^*_{\mathrm{ll,max}}$, the VR front-end is operated in 1/3-PWM mode. The cascaded controller structure is able to draw sinusoidal currents from the grid by always

only switching the phase carrying the lowest current and by controlling the remaining two currents through proper shaping of the DC-link voltage $u_{xz}(= u_{xy} + u_{yz})$, where $u_{xy} = u_{yz}$ is always kept.

- **Partial-Boost Mode**
  As soon as the DC-link voltage setpoint $U^*_{xz,min}$ increases to a value between the minimum and maximum of the six-pulse reference voltage $u^*_{ll,max}$, the VR front-end operates in partial-boost mode, which means that there are intervals where the DC-link voltage reference u^*_{xz} is either defined by $u^*_{ll,max}$ or by the minimum DC-link voltage setpoint $U^*_{xz,min}$. Consequently, within one sixth of a mains period, the controller has to alternate between 1/3-PWM and 3/3-PWM operation.

- **Full-Boost Mode**
  When the DC-link voltage setpoint $U^*_{xz,min}$ is higher than the maximum of the six-pulse reference voltage $u^*_{ll,max}$, the VR front-end has to continuously operate in boost mode, where all three phase-legs are pulse width modulated (3/3-PWM).

It should be noted that for all above mentioned operating modes, the controller is able to symmetrically partition the total DC-link voltage, i.e., to ensure $u_{xy} = u_{yz}$ for the two DC/DC converter modules, and hence the blocking voltage requirement defined by half the DC-link voltage is not exceeded for the midpoint connected switches, which enables the use of 600 V semiconductor technology.

For sake of completeness, it has to be mentioned, that there is a possibility to modulate the VR front-end in such a way that the midpoint current i_y is minimized during partial-boost and full-boost mode, as shown in **Fig. 5.10** for the same operating conditions as considered for **Fig. 5.9**. This is actually explained for full-boost mode in [105, 126, 149], leading to a reduction of the power mismatch of the DC/DC converter modules.

Furthermore, besides minimizing the midpoint current, there is a certain voltage range in partial-boost and full-boost mode, where the transition from 1/3-PWM to 3/3-PWM can be smoothed out by only pulse width modulating two of the three rectifier stage phases, i.e., by 2/3-PWM operation as shown in **Fig. 5.10**. The optimal implementation of this improved transition between the three modulation schemes 1/3-PWM, 2/3-PWM, and 3/3-PWM is subject to further research, which also considers the optimal use of 2/3-PWM for other types of midpoint-connected converters, including all possible VR configurations [150], the HANPC [50], or the Stacked Multicell Converter (SMC) [151].

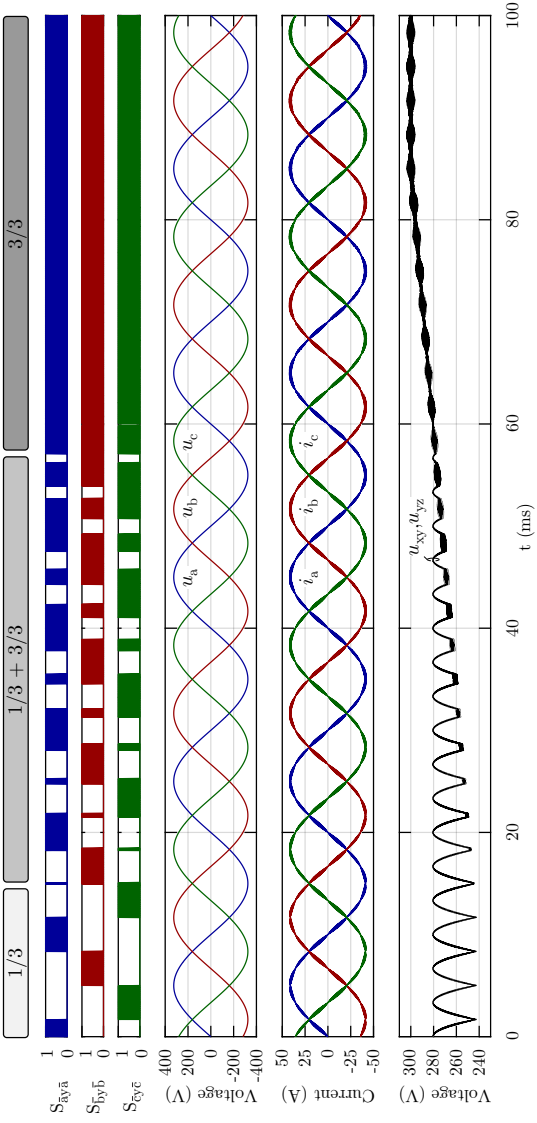

Fig. 5.9: Simulation waveforms of the SynC-VR-i, for a transition between 1/3-PWM and full-boost mode with intermediate (1/3 + 3/3)-PWM operation: **(i)** modulation strategy and gate signals, **(ii)** grid (AC input) voltages $u_{\{a,b,c\}}$, **(iii)** input phase currents $i_{\{a,b,c\}}$, **(iv)** DC-link voltages, where $u_{xy} = u_{yz}$ is ensured at all times. For **(v-vii)** see next page. Simulation parameters are: f_{sw} = 100 kHz, $L_{\{a,b,c\}}$ = 100 µH, $C_{xy} = C_{yz}$ = 10 µF, and L_0 = 100 µH.

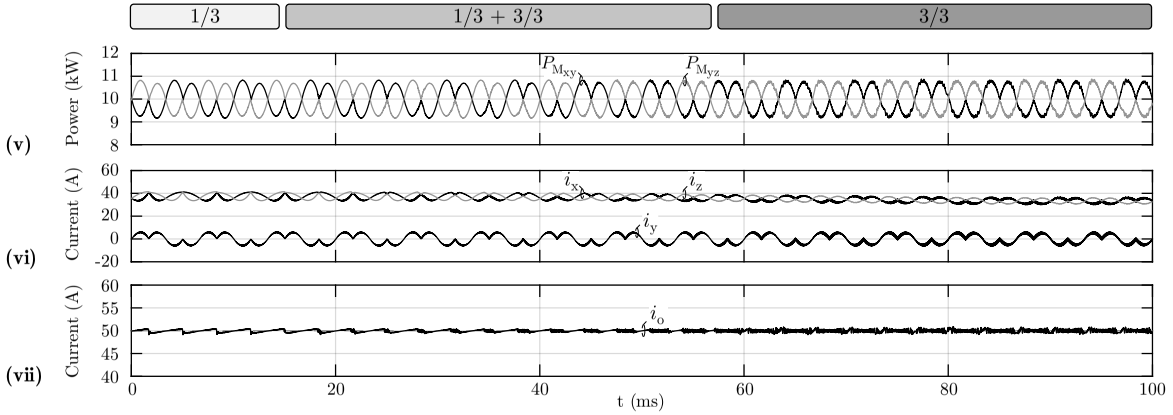

Fig.: 5.9 (cont'd): Simulation waveforms of the SynC-VR-i, for a transition between 1/3-PWM and full-boost mode with intermediate (1/3 + 3/3)-PWM operation: For **(i-iv)** see previous page. **(v)** Currents of the positive (i_x), mid (i_y) and negative (i_z) DC-link rail (filtered with a first-order low-pass filter with a corner frequency of 5 kHz in order to extract the local average values), **(vi)** power transferred by the two isolated DC/DC converter modules $P_{M_{xy}}$ and $P_{M_{yz}}$, and **(vii)** battery charging, i.e., output current i_o closely adhering to the set reference value $I_o^* = 50$ A. Simulation parameters are: $f_{sw} = 100$ kHz, $L_{\{a,b,c\}} = 100$ µH, $C_{xy} = C_{yz} = 10$ µF, and $L_o = 100$ µH.

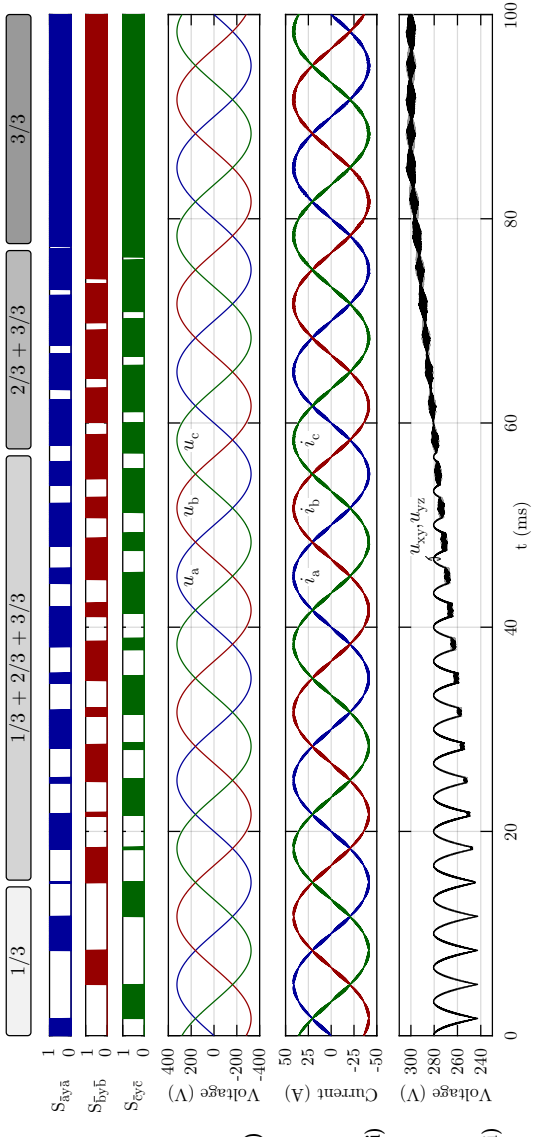

Fig. 5.10: Simulation waveforms of the SynC-VR-i, for the same transition as in **Fig. 5.9** with intermediate (1/3 + 2/3 + 3/3)-PWM and (2/3 + 3/3)-PWM operation: **(i)** modulation strategy and gate signals, **(ii)** grid (AC input) voltages $u_{[a,b,c]}$, **(iii)** input phase currents $i_{[a,b,c]}$, **(iv)** DC-link voltages, where $u_{xy} = u_{yz}$ is ensured at all times. For **(v-vii)** see next page. Simulation parameters are: f_{sw} = 100 kHz, $L_{[a,b,c]}$ = 100 µH, $C_{xy} = C_{yz}$ = 10 µF, and L_o = 100 µH.

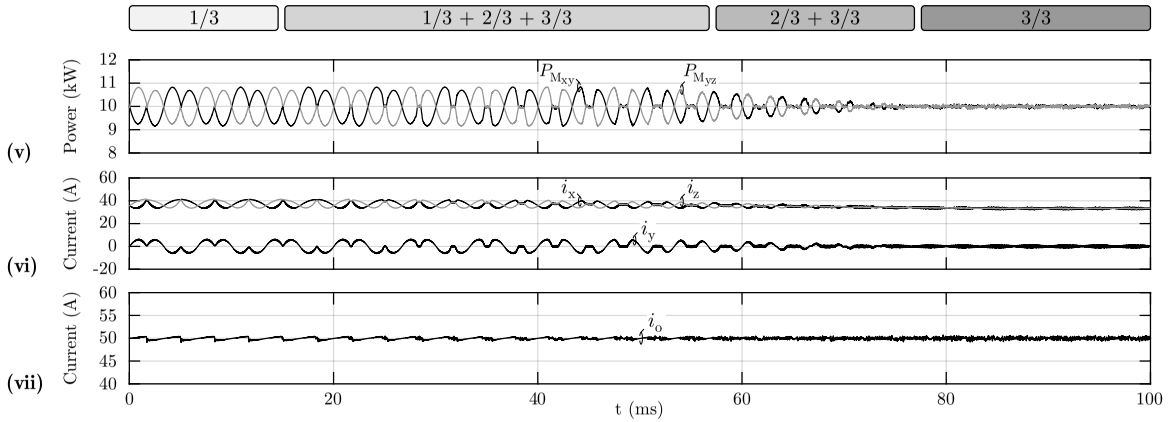

Fig.: 5.10 (cont'd): Simulation waveforms of the SynC-VR-i, for the same transition as in **Fig. 5.9** with intermediate (1/3 + 2/3 + 3/3)-PWM and (2/3 + 3/3)-PWM operation: For **(i-iv)** see previous page. **(v)** Currents of the positive (i_x), mid (i_y) and negative (i_z) DC-link rail (filtered with a first-order low-pass filter with a corner frequency of 5 kHz in order to extract the local average values), **(vi)** power transferred by the two isolated DC/DC converter modules $P_{M_{xy}}$ and $P_{M_{yz}}$, and **(vii)** battery charging, i.e., output current i_o closely adhering to the set reference value $I_o^* = 50$ A. Simulation parameters are: $f_{sw} = 100$ kHz, $L_{\{a,b,c\}} = 100$ µH, $C_{xy} = C_{yz} = 10$ µF, and $L_o = 100$ µH.

5.5 Semiconductor Stress Analysis

In order to quantify the performance gain achieved by the 1/3-PWM for the VR front-end at hand in terms of semiconductor losses, the switching and conduction losses of the semiconductors are analytically derived and compared for both the 3/3-PWM and 1/3-PWM operation.

Switching Losses

To model the switching losses, the following two assumptions are made. Firstly, the input currents $i_{\{a,b,c\}}$ are assumed purely sinusoidal, i.e., the switching frequency current ripple of the input currents is considered to be small, such that only hard-switching transitions are occurring at turn-on of a power transistor. And secondly, a linear dependency of the hard-switching losses on the switched current is considered. This last assumption is a valid first step approximation, particularly for WBG devices, as shown in [152] for 650 V GaN devices and in [64] for 900 V SiC devices. Therefore, the switching losses are modeled as

$$E_{\mathrm{sw}}(t) = k_{\mathrm{sw,o}} + k_{\mathrm{sw,1}} \cdot i(t)\,, \tag{5.2}$$

where $k_{\mathrm{sw,o}}$ is the current independent switching loss component (which is equal to the switching losses occurring in one zero-load-current transition) and $k_{\mathrm{sw,1}}$ characterizes the linear dependency of the switching losses on the switched current $i(t)$. By averaging the switching losses $E_{\mathrm{sw}}(t)$ over a fundamental grid period, the following expressions for the switching losses are obtained:

$$P_{\mathrm{sw,3/3}} = \left(k_{\mathrm{sw,o}} + k_{\mathrm{sw,1}} \cdot I_{\mathrm{avg}}\right) f_{\mathrm{sw}} \tag{5.3}$$

$$P_{\mathrm{sw,1/3}} = \underbrace{\left(\frac{k_{\mathrm{sw,o}}}{3}\right)}_{-66\,\%} + \underbrace{\left(1 - \frac{\sqrt{3}}{2}\right) k_{\mathrm{sw,1}} \cdot I_{\mathrm{avg}}}_{-86\,\%} f_{\mathrm{sw}}\,; \tag{5.4}$$

$P_{\mathrm{sw,3/3}}$ and $P_{\mathrm{sw,1/3}}$ are the switching losses for 3/3-PWM and 1/3-PWM operation, f_{sw} denominates the switching frequency, and I_{avg} is the average value of the rectified sinusoidal input current $i_{\{a,b,c\}}$, resulting as $I_{\mathrm{avg}} = \frac{2 \cdot \hat{I}}{\pi}$, with $\hat{I}$ being the peak value of $i_{\{a,b,c\}}$.

In addition to a 66 % saving of current independent switching losses, and a 86 % saving of linearly current dependent losses, it has to be noted that in

practice some further switching loss savings will occur due to the dependency of the switching losses on the switched voltage (e.g., $k_{sw,o}$ actually is proportional to u_{xy}^2 and u_{yz}^2 [57]). For the sake of clarity, the voltage dependency of the switching losses has been omitted in this analysis, but still more than two-thirds of the switching losses of the front-end VR are saved.

Conduction Losses

In the following, the RMS currents of the switches, and the RMS and average (AVG) currents of the diodes of the VR front-end are derived for the the 3/3-PWM and 1/3-PWM schemes, in order to quantitatively compare the conduction loss difference between both modulation schemes.

- *Switch RMS Current:*

$$I_{S,rms,3/3} = \frac{\hat{I}}{\sqrt{\pi}} \sqrt{\frac{\pi}{2} + \frac{5\sqrt{3} - 16M - 8}{12}}\,, \tag{5.5}$$

$$I_{S,rms,1/3} = \frac{\hat{I}}{\sqrt{\pi}} \sqrt{\frac{\pi}{6} + 2\sqrt{3} \ln\left(\frac{\sqrt{3}}{2}\right)}\,. \tag{5.6}$$

- *Diode RMS Current:*

$$I_{D,rms,3/3} = \frac{\hat{I}}{\sqrt{\pi}} \sqrt{\left(\frac{1}{3} - \frac{3\sqrt{3}}{16}\right)(2M+1) + \frac{18M-1}{16\sqrt{3}}}\,, \tag{5.7}$$

$$I_{D,rms,1/3} = \frac{\hat{I}}{\sqrt{\pi}} \sqrt{\frac{\pi}{6} + \frac{\sqrt{3}}{8} \ln\left(\frac{256}{81}\right)}\,. \tag{5.8}$$

- *Diode AVG Current:*

$$I_{D,avg,3/3} = \hat{I}\frac{M}{\sqrt{4}}\,, \tag{5.9}$$

$$I_{D,avg,1/3} = \hat{I}\frac{\sqrt{3}\ln(3)}{2\pi}\,. \tag{5.10}$$

Tab. 5.1: Simulated and calculated semiconductor currents. 3/3-PWM case is for u_{xz} = 600 V, cf., **Figs. 5.6** and **5.7**.

		3/3-PWM		1/3-PWM		Difference
		Sim.	Theor.	Sim.	Theor.	
Switch	rms	10.15 A	9.85 A	3.71 A	3.68 A	-63.4 %
Diode	rms	19.28 A	19.28 A	20.40 A	20.33 A	+5.5 %
	avg	11.08 A	11.10 A	12.44 A	12.41 A	+12.3 %

All currents are given in dependency of the modulation index M, which is defined as

$$M = \frac{u_{ac,pk}}{(u_{xz}/2)}\,, \tag{5.11}$$

where $u_{ac,pk}$ is the peak value of the grid (input) phase voltages $u_{\{a,b,c\}}$.

A quantitative comparison of the current stresses of 3/3-PWM vs. 1/3-PWM operation is shown in **Table 5.1**, where for the 3/3-PWM mode a DC-link voltage of u_{xz} = 600 V is chosen, as also considered for the representation in **Fig. 5.6**. The main advantage of 1/3-PWM operation regarding conduction losses is that the switches of the VR front-end only conduct the current in two 60 °-wide intervals, which are moreover centered around the zero crossing of the current. This translates into a very large reduction of the RMS current stress on the switches (63.4 %), leading to 86.7 % lower conduction losses of the switches, at the cost of a small RMS and average current increase in the diodes, +5.5 % and +12.3 % respectively (cf., **Fig. 5.7(iv-v)**).

Remark: If the VR front-end would always be operated with 1/3-PWM without transitioning into partial-boost or full-boost mode, a smaller die area (or number of parallel switches) could be selected for realizing the switches $S_{\bar{i}y\bar{i}}$ without large influence on the losses, since conduction losses would increase for a smaller die area, but the capacitive hard-switching losses due to the parasitic output capacitance of the switches (C_{oss}) would reduce inversely proportional to the die area [18], finally enabling a more cost effective realization of the EV-charger VR front-end for a similar performance.

5.6 Summary

In this chapter, a novel synergetic control scheme of a three-phase/level PFC rectifier and a series-connected isolated DC/DC stage for high power EV

chargers is introduced. By only always pulse width modulating the phase with the smallest current (1/3-PWM), and by shaping the DC-link voltage close to the six-pulse maximum line-to-line grid voltage, a sinusoidal current consumption of all phases can be ensured, while the switching losses of the PFC stage can be reduced by more than two thirds for the given example, and the conduction losses even decrease by around 86 %. Furthermore, by symmetrically partitioning the total DC-link voltage, 600 V semiconductor technology can be used throughout the whole converter, further decreasing the losses by allowing the use of latest GaN devices. Finally, it has been shown that the converter can seamlessly transition from 1/3-PWM to partial-boost and full-boost operation mode, i.e., 2/3-PWM or 3/3-PWM operation, thus obtaining a widely controllable DC-link voltage value which reduces the output voltage range requirement of the DC/DC converter modules.

6 Conclusion and Outlook

In the quest to reduce the carbon footprint on earth, people will have to actively change their habits, be it by self-initiative, or motivated by progressive government policies. And motivated by this need to transition towards sustainable habits, a revolution to what is considered the average household has started. Future households will feature PV installations, most probably also energy storage in shape of a battery to balance the energy consumption, and the house owners will be (car-)sharing an EV. In this path towards sustainable development, power electronics is a key enabler, that although not making it often to global headlines, is a crucial technology that allows to convert energy using static systems employing solid state devices.

This thesis contributes in several levels of power electronics abstraction, starting from analyzing the fundamentals of modern power semiconductor devices, then evaluating different converter topologies that enable ultra-high efficiency, building a three-phase 99.35 % efficient 10 kW PV inverter, and finally proposing a novel synergetic control that can be retrofitted into existing fast EV chargers.

In the following, the main findings for each abstraction layer will be summarized, and the outlook and future research will be discussed.

6.1 Component Level

Summary

A fundamental approach to analyze semiconductors and their performance in hard-switching bridge-legs is taken in **Chapter 2**, where in a first step the conduction and switching losses of modern power switches are analyzed. After defining a quantitatively-meaningful device figure-of-merit, D-FOM,

that can be used to calculate the minimum losses of a a 2L bridge-leg, the scaling laws of these devices are analyzed with respect to voltage. This then leads to the definition of a new extended figure-of-merit, X-FOM, that by optimizing the die area for each switching frequency, allows to calculate the maximum achievable performance of low-voltage switches in ML configurations for different numbers of levels, power ratings and switching frequencies. This enables, then, to quantitatively map device properties into ML bridge-leg properties. In this context, two metrics of improvement are identified: semiconductor losses, and applied voltage-time area to the filter inductor, both of which enable more efficient and/or more compact converter realizations. Finally, a numerical example is provided, where the utility of the proposed figure-of-merit is conveyed by analyzing a 10 kW three-phase PV inverter, which shows that a 3L bridge-leg configuration clearly outperforms a 2L counterpart in both aforementioned metrics.

Discussion, Outlook and Future Research

With the proposed X-FOM, ML bridge-leg performance boundaries can be calculated. However, these are theoretical limits, since in reality, due to finite switching speeds, an unavoidable V-I overlap exists during hard-switching transients. The main culprits for these limited switching speeds are the parasitic elements of the devices, which can either be intrinsic to the nature of the switch (e.g., MOSFET gate capacitances, that although reduced considerably with WBG, will never disappear), and others that are created by external factors, such as the packaging or PCB routing. It is shown how moving from a 3-pin to a 4-pin SiC device, the switching performance is increased dramatically for higher load currents, by simply making a Kelvin source connection that eliminates the influence of the changing load current on the inner gate-source voltage. Hence, by only improving the packaging, a significant improvement in switching speed can be obtained (cf., **Fig. 2.12**), allowing to switch up to, e.g., 127 V/ns for 650 V GaN devices featuring advanced embedded packages [153, 154], and close-to-ideal minimal losses can be obtained.

However, if the close-to-ideal-switch would be made possible with future WBG devices, this would translate into very high $\mathrm{d}u/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ values, which pose several challenges, both for EMI and for variable speed motor drive (VSD) systems. Firstly, fast transients result in resonances due to parasitic components of the filter elements, that could complicate EMI compliance [155], and secondly, high $\mathrm{d}u/\mathrm{d}t$ stresses pose challenges for the motors, such as

insulation aging, common-mode bearing currents and overvoltages due to reflections on long motor cables [156]. Hence, research has to be done on how to handle this "double-edged sword" of WBG devices [157]. It is precisely also here, that due to the typically larger parasitic capacitances of lower-voltage devices, these achieve lower $\mathrm{d}u/\mathrm{d}t$ values (see, e.g., the 200 V GaN devices in [17], where 200 V GaN devices achieve ≈20V/ns with a highly-optimized power commutation loop, where there is hardly any room for improvement left, compared to the 127 V/ns for 650V GaN devices in [153]) while still substantially reducing the filter size. Hence, ML converters are not only suitable for high-efficiency power-dense solutions, but also for EMI-sensitive and variable speed drive applications, where fast switching transients are a potential issue.

6.2 Bridge-Leg Level

Summary

In **Chapter 3**, a comparative ML topology evaluation is performed with the goal of finding the most compact solution that achieves 99.5 % efficiency for a three-phase 10 kW inverter. With the properties of ML bridge-legs already highlighted, a range of different topologies and numbers of levels are selected for the evaluation. This fulfills the goal of analyzing and understanding the advantages and disadvantages of different topologies for ultra-high efficiency applications. After a preliminary optimization, a pre-selection of two topologies is done: a 3L T-type and a 7L hybrid active neutral point clamped converter. These two are then analyzed in more detail, and 3D-CAD models are built to validate that the calculations are correct. With this it is finally concluded that the 7L HANPC topology is the best suited solution to achieve the target efficiency in a power-dense realization, and is therefore realized in **Chapter 4**.

Discussion, Outlook and Future Research

The insight gained with this quantitative evaluation is very important, because although there is a clear advantage in volume when going towards a high level count, there are also considerable trade-offs (cf., **Fig. 3.4**) that are invisible to the X-FOM. Whereas 2L converters are ruled out due to the large magnetics required to filter low switching frequencies, the T-type converter performed better than 3L and 5L FCCs, since the balance between generating a third

level with a midpoint connection instead of using FCs was more favorable concerning the system volume. Another very interesting outcome is that the hybrid approach is very advantageous, specially since it can create a ML output with the same number of levels as a standard FCC with less than half of the FCs. However, whereas this is an advantage for the target three-phase 99.5 % efficiency 10 kW converter, it might not always be the case. The HANPC converter requires also switches that block a higher voltage, which increases the bill-of-materials part count (especially, if it also requires a different gate driver circuitry), and also concentrates the switching losses in a lower number of devices - which for ultra-high efficiency applications is not an issue, but for applications seeking extreme power density like in the Google Little Box Challenge, it might be a drawback as the device cooling might become critical. A further disadvantage of the HANPC, although not relevant for the application considered in this thesis, is that it can't be used for DC/DC conversion without an external DC-link voltage balancer (e.g., the one in [158]), as a certain finite current would be drawn from the DC-link midpoint connection, thus fully charging and discharging the upper and lower capacitors, respectively, depending on the duty cycle and power flow direction.

This analysis shows also, that the FCs can be thought of as "hidden filter" elements. FCC topologies clearly reduce the size of the magnetic filter components, but this comes at a cost of including FCs, that at least in this work, have not been considered as filter elements per se. Optimizations, like the one performed in this chapter or the Pareto analysis done in the following one, arrive at an optimal balance between FCs and filter elements, but without really providing a fundamental understanding to the trade-offs and the sensitivity of parameters. And perhaps future work should indeed consider FCs as part of the filter realization effort as in [52], and not just take the ML waveform as a given for the conventional filter volume optimization.

In order to handle the extensive analysis covering many different bridge-leg topologies, the number of considered topologies was limited. However, with the knowledge that 7L seem to be optimal for systems with DC-links in the range of 800 V (mainly also because there are no competitive switches in the 300 V range that would make it worth to reevaluate 5L systems), other ML topologies, many of which can for instance be found in ML topology review papers [112, 159–162], could be researched, not only for high-efficiency solutions but also power-dense or lightweight solutions, providing a missing comprehensive view to the field.

Finally, the proposed DC-link side CM filtering, although very promising, still has to be demonstrated in hardware. The loss saving potential is clear, but it poses risks concerning EMI compliance, as the DC-link is jumping with respect to ground (or any stable potential), a fact which might also pose challenges with the referencing of the control and measurement signals, specially if referenced to the jumping DC-link potential.

6.3 Converter Level

Summary

After describing the operation principle of the HANPC converter, in **Chapter 4** a Pareto front optimal 99.35 % efficient all-Si three-phase 12.5 kW 7L inverter is realized, featuring 3.4 kW/dm^3 and 3.2 kW/kg. Moreover, the realized system also fulfills CISPR Class A EMI requirements, and features no active cooling system, which increases the reliability given that no maintenance-prone fans are required. The Pareto front analysis shows that with the upcoming generation of 200 V Si devices, of which the first engineering samples are already available [65], the ultimate 99.5 % efficiency target would be reached. Moreover, with commercially available GaN devices, it is predicted that on the same hardware design and with the same switching frequency, an efficiency of 99.6 % is achievable.

Discussion, Outlook and Future Research

The main reason why this hardware was built with Si devices, and not GaN devices, is that this hardware implementation is meant for rather shorter than longer term industry application. As a matter of fact, the industry partner of this project has, based on the positive outcome of this research, engineered a 4 kW 400 V DC-link single-phase all-Si 5L HANPC inverter peaking at 99.1 % efficiency, as it is shown in the recently published application note [128]. Besides an immense satisfaction for having had such a strong influence (as the idea originates from this work), this means that there is a genuine interest in industry for ML solutions. However, it is also true, that if more companies were to adopt a ML solution to increase the performance of their product portfolio, they would do this with the knowledge that this entails a larger degree of complexity. Hence, considering that commercializing ML converters is a challenge, doing so at the same time with state-of-the-art GaN devices might be two too-large steps to take at once.

In view of the volume of the presented hardware demonstrator, nearly one quarter of the volume of the 7L HANPC hardware demonstrator is occupied by the FCs, which in this work were realized with film capacitors. Hence, it should be thought as to how this volume can be reduced. Firstly, one could replace the Si switches with GaN switches, and switch at higher frequencies, thus reducing the capacitance requirement for the FCs. Secondly, MLCC could be used to save approximately two thirds of the volume (see **Section F.2** of the Appendix), but depending on the capacitance and voltage rating requirements, they might not be practical for assembly (series-parallel stacking MLCC is very tedious), reliability would be too low (since they are very brittle components that are very susceptible to mechanical vibrations and shocks, and because there is a difference of thermal expansion coefficients between the MLCC and the PCB materials which potentially causes the MLCCs to crack), and because the price compared to film capacitors is an order of magnitude higher (around ×15 higher price for the same capacitance). And finally, an option would be to allow a larger ripple in the capacitors. Provided that the blocking voltage of the switches would not be a problem when defining the allowable FC voltage ripple, it remains unclear what the limit to the allowable ripple is, and if this ripple can be increased, say from 5 % of the switch blocking voltage to 20 %. Although this would allow to shrink the FC volume by a factor four, it could also complicate the EMI filter design, as the harmonics of the (actual, and not the effective) switching frequency could appear in the output voltage spectrum and potentially require more filtering than if the voltage ripple of the FCs would be limited.

Concerning further reducing the losses, most of the improvement potential comes from improving the switches. However, other than the switches, one loss factor that is improvable is the digital control. For this work, a System on Chip (SoC) module with a Xilinx Zynq XC7Z020 was integrated into the hardware, which consumes around 3-3.5 W. Switching at 16 kHz, there is no need for fast computing of control algorithms, and hence, a low-power microprocessor that would consume power in the range of some hundreds of mW would be a good alternative to save further losses.

An advantage, however, of having 200 V Si switches is, that as a cost of performance they switch slower, i.e., they switch with a $\mathrm{d}u/\mathrm{d}t$ of only 5 V/ns [65]. This means, that for motor drives where the $\mathrm{d}u/\mathrm{d}t$ should be limited to values approximately below 10 V/ns [156], this directive is complied with these switches without any further effort, so no additional filtering would in theory be needed.

However, to make ML converters more attractive for industry adoption, advancements in the semiconductor industry are required. In the very recent years, half-bridge gate drivers are becoming popular, as they reduce the component count substantially. These half-bridge gate drivers can equally be used in FCC converters for two adjacent switches, since their outputs don't necessarily need to be complimentary. A next step in this direction is to integrate the gate driver into the switch, and this is what for instance *Texas Instruments* has developed with their 600 V 50 mΩ device, where they integrated the gate driver into the device and achieve $\mathrm{d}u/\mathrm{d}t > 100\,\mathrm{V/ns}$ [90]. And a final step, which would be the ultimate FCC enabler for industrial applications, is something similar to what *Texas Instruments* has developed with their 80 V switches [88], where they offer a half-bridge with an integrated half-bridge gate driver.

At this point, a natural question that arises is, if it is really necessary to use so many levels to achieve ultra-high efficiency, when, for instance, a single-phase $230\,\mathrm{V_{rms}}$ 2L rectifier can achieve e.g., 99.1 % efficiency, like in the PFC data center rectifier presented in [132], where a totem-pole structure with a bridge-leg with 600 V GaN devices switching at 65 kHz is used in combination with a line-frequency unfolder bridge-leg with Silicon Superjunction (Si SJ) devices. This is investigated in detail in **Appendix F**, where a clear performance difference is observed between systems that generate $230\,\mathrm{V_{rms}}$ with a 400 V DC-link and those that generate it with a 800 V DC-link. In this analysis, it is shown that *3-levels are not enough* for a 800 V DC-link bridge-leg to regain the performance loss of a 400 V DC-link counterpart, even though 600 V devices can be used in both cases. This is confirmed by building a 400 V benchmark 2L 2.2 kW inverter bridge-leg featuring 99.2 % peak efficiency and 18.0 $\mathrm{kW/dm^3}$ power density, and a 3L 800 V counterpart reaching 98.8 % efficiency and a power density of 9.1 $\mathrm{kW/dm^3}$, the latter suffering both an efficiency and power density penalty. After using the X-FOM, 7L are identified as the minimum amount of levels required to regain the efficiency loss, and a Pareto front optimization is performed to confirm this. In a final step, a 2.2kW 800 V DC-link 7L GaN-based FCC inverter bridge-leg is built, achieving a peak 99.03 % efficiency in 15.8 $\mathrm{kW/dm^3}$. This means, that in order to achieve ultra-high efficiency, two possible paths are identified: either using ML circuit topologies, or, operating with a reduced DC-link voltage. Two examples of how to reduce the DC-link voltage requirement for grid-connected and motor drive applications are given in **Section F.6** of **Appendix F**.

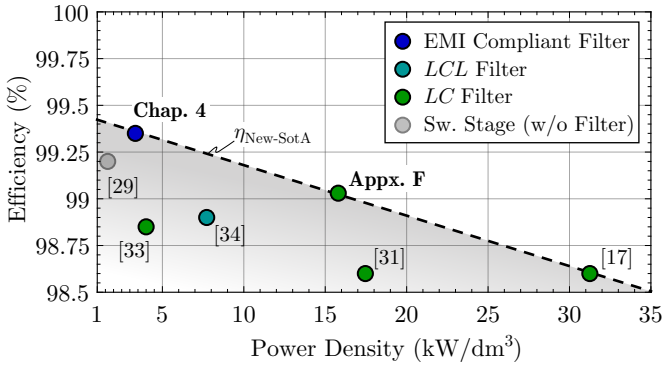

Fig. 6.1: Overview of the systems in **Table 1.3** and in addition the two systems presented in this work. A linear trendline of the new state-of-the-art is shown ($\eta_{\text{New-SotA}}$), where a clear trade-off between efficiency and power density of realized converters can be observed.

Finally, **Fig. 6.1** shows the performance of the two systems built in this work in comparison to the state of the art systems of **Table 1.3**. If a linear trendline is extracted from the best performing converters, then this yields:

$$\eta_{\text{New-SotA}}\,[\%] = 99.45 - 0.027\rho\left[\frac{\text{kW}}{\text{dm}^3}\right] , \tag{6.1}$$

where $\eta_{\text{New-SotA}}$ is the new state-of-the-art efficiency in percentage and ρ is the power density in kW/dm³ (trendline is valid in the 1 kW/dm³ to 35 kW/dm³ range, cf., **Fig. 6.1**). This yields a very meaningful conclusion, since at the end of the day, it can be seen that in order to gain ≈0.75 % efficiency (or, taking the examples of [17] and **Chapter 4**, to halve the converter losses) a power density reduction of factor 10 would have to be accepted.

6.4 System Level

Summary

Typical EV chargers are built in a modular fashion, where several modules of a smaller rating are paralleled to create a fast DC charger. These modules are usually built with an AC/DC front-end, and an isolated DC/DC stage, that besides providing galvanic isolation also regulates the output voltage.

In **Chapter 5** a holistic approach is taken to such a state-of-the-art architecture [133], where a synergetic control is proposed for a Vienna AC/DC rectifier stage which is followed by to two series-connected DC/DC modules. By having the two stacked DC/DC modules control the DC-link voltage to the maximum line-to-line voltage while ensuring an equal DC-link voltage partitioning to the upper and lower DC-link capacitors, it is possible to pulse width modulate always only one out of the three rectifier bridge-legs while still drawing sinusoidal currents from the mains, hence, leading to the 1/3-PWM while still using 600 V GaN switches. This allows a saving of approximately two thirds of the losses in the switches (because both switching and conduction losses are reduced), for a slight ≈10 % increase in the diode losses. Additionally, it is shown that the same topology can seamlessly transition into boost-mode, thus finally reducing the output voltage range variation that the DC/DC converters need to provide, enabling a more efficient realization of the EV charger.

Discussion, Outlook and Future Research

First of all, it is important to note that the proposed synergetic solution enabling the 1/3-PWM can be applied to any AC/DC + DC/DC or DC/DC + DC/AC system, i.e., it can also be used for inverter systems for variable speed motor drives, and this has very recently been experimentally validated in [108, 146, 163]. Hence, three-phase PV and battery inverters, if preceded by a DC/DC converter could also profit from this solution, enabling an additional increase in efficiency.

However, the 1/3-PWM for rectifiers still has to be demonstrated in hardware. This is a topic of current research, where a 10 kW SynC-VR-i demonstrator is currently being commissioned and will provide hardware verification of the proposed synergetic control.

Irregular grid conditions, i.e., grid overvoltages, unbalanced grid voltages, harmonic distortions, etc. can be an issue for 1/3-PWM modulated converters, given that there is no voltage margin in the DC-link to control such irregularities. A recent paper [164] analyzes these faulty grid situations and how a 1/3-PWM modulated grid-connected converter could deal with them. Simulations showed, that indeed, by using appropriate protection elements in the front-end (e.g., surge protection devices and bypass diodes), and by means of slight control structure changes, all of the grid irregularities specified in the corresponding standards can be fulfilled. A next step, would be to

also validate the simulations by demonstrating this in a working hardware prototype.

Furthermore, having proposed a front-end rectifier that now can also be used in a wider DC-link voltage range, the right choice of the DC/DC module topology is needed. It is in this context, that recently an additional novel hybrid quantum series resonant DC/DC converter is proposed in [165], that essentially operates in the same way as a series resonant converter, but instead of regulating the output voltage by changing the switching frequency, it always operates at a constant frequency and regulates the output voltage by skipping power pulses (i.e., using free-wheeling states on the primary or secondary side). Hence, without there being a priori a clear answer to which is the best DC/DC topology for the 1/3-PWM front-end, a comprehensive analysis and optimization is required to shed light on this.

By using 2/3-PWM in the transition from 1/3-PWM to the boost-mode with 3/3-PWM, not only can the losses be reduced in the front-end, but the midpoint balancing is also done by the rectifier stage, leading to an equal power splitting of the DC/DC modules. This is done by injecting a third-harmonic component in the phase voltage modulation process that minimizes the midpoint currents generated by the Vienna rectifier (and all the converters which feature a DC-link midpoint connection in the topology, like for instance the HANPC converters). Using the 2/3-PWM is typically not an option for such three-phase converters, because it injects a finite local average current into the DC-link midpoint (which increases with decreasing modulation index), that creates a large DC-link midpoint ripple with three times mains frequency. However, as in this architecture there are two subsequent series-connected DC/DC converter modules, these modules could be controlled a way that the midpoint current is not entering the DC-link capacitors and creating a voltage ripple any more, but is covered by a power mismatch of the DC/DC modules, like in **Fig. 5.9**. Hence, if a larger instantaneous power mismatch between the DC/DC modules would be allowed (which although on average the same power is processed, would certainly require an overdimensioning of the DC/DC modules), the front-end Vienna rectifier could always be operated either in 1/3-PWM or in 2/3-PWM, which could be considered particularly for high modulation indexes. Hence, it has to be analyzed and quantified if operating the Vienna rectifier during the boost-mode always in 2/3-PWM instead of in 3/3-PWM is beneficial or detrimental for the system as a whole.

Appendices

A

Semiconductor Physics-Based Derivation of the Proposed Device Figure-of-Merit

To understand the fundamental dependencies of the specific on-state resistance R'_{on} and specific charge equivalent capacitance $C'_{oss,Q}$ on the blocking voltage, a physics-based derivation of these characteristics is presented in the following for a vertical MOSFET device (**Fig. A.1a**), where a 1D approximation of an ideal drift region is assumed [55]. This basic derivation should only serve as a theoretical framework to understand fundamental physical semiconductor dependencies. For a detailed semiconductor physics analysis of WBG devices, please refer to [55].

A.1 Conduction Losses: R'_{on}

For the R'_{on} derivation, only the resistance of the n^- drift region is considered, since the resistance of this region dominates the R'_{on} for vertical MOSFETs with blocking voltages above 50 V [166]. Further, the traditional assumption of unipolar carrier conduction is made.

The blocking voltage U_B of a vertical MOSFET that maximally utilizes its electric field such that the critical field E_c is reached at the breakdown voltage (cf., **Fig. A.1b**) is given by:

$$U_B = \frac{E_c W}{2}\,, \tag{A.1}$$

from which the required width of the drift region W is:

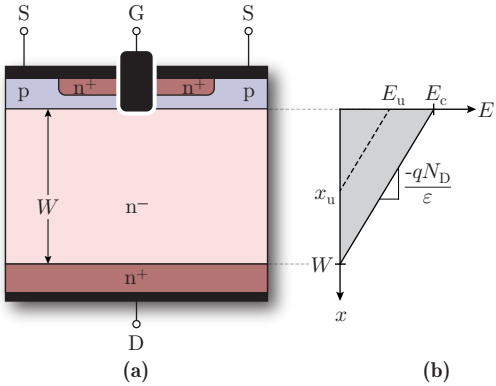

Fig. A.1: (a) Vertical n-type MOSFET structure and **(b)** electrical field distribution in the drift region. **(a)** and **(b)** are considered for the derivation of the theoretical dependency of R'_{on} and $C'_{oss,Q}$ on the blocking voltage to complement the empirical study performed in this work.

$$W = \frac{2U_B}{E_c} \,. \tag{A.2}$$

Assuming an optimally-doped drift region, the doping concentration N_D is:

$$qN_D = \frac{\varepsilon E_c}{W} = \frac{\varepsilon E_c^2}{2U_B} \,, \tag{A.3}$$

where q is the elementary charge, and ε the permittivity. With the on-state resistance

$$R_{on} = \frac{W}{\sigma A} = \frac{W}{qN_D \mu A} \,, \tag{A.4}$$

where σ is the conductivity, μ the donor carrier mobility and A the semiconductor area, the specific (area-related) on-state resistance can be calculated with Eqs. **(A.2)** and **(A.3)** as:

$$R'_{on} = R_{on}A = \frac{4U_B^2}{\mu\varepsilon E_c^3} \propto U_B^2 \,. \tag{A.5}$$

Therefore, the theoretical limit for vertical devices shows a dependency $R'_{on} \propto U_B^2$. It is widely documented in literature, though, that the empirical

Si dependence on blocking voltage for vertical devices is $R'_{\mathrm{on}} \propto U_{\mathrm{B}}^{2.5}$ (mainly due to the dependency of E_{c} on N_{D}, where lowering N_{D}, which is required for blocking higher voltages, cf., Eq. **(A.3)**, also leads to a reduction in E_{c}) [56, 166, 167] and coincides with the device survey performed in **Section 2.2**. Both Si and SiC devices are variations of vertical structures, and although the device structure may vary, for instance, by including field plates to shape the electric field profile [168], this derivation yields a valid insight for both of these technology classes.

For lateral GaN-on-Si HEMTs, the ideal on-resistance, only considering the drift region (valid for high breakdown voltages), is [54, 169]:

$$R'_{\mathrm{on}} = \frac{L_{\mathrm{drift}}^2}{q\mu Q_{\mathrm{s}}}, \tag{A.6}$$

where L_{drift} is the drift region length and Q_{s} is the 2-D electron gas (2DEG) charge-sheet density. Assuming a constant electric field in the drift region, the drift length is $L_{\mathrm{drift}} = U_{\mathrm{B}}/E_{\mathrm{c}}$, and the $R'_{\mathrm{on}} \propto U_{\mathrm{B}}^2$ theoretical dependency is found again. At lower voltages, the channel resistance dominates – which is not voltage-dependent – and R'_{on} has a less pronounced dependency on U_{B} ($R'_{\mathrm{on}} \propto U_{\mathrm{B}}^{1.1}$ is found in the empirical survey in **Section 2.3)**. These two regions of U_{B} dependence are shown in **Fig. 2.3** and are discussed in [54].

A.2 Switching Losses: $C'_{\mathrm{oss,Q}}$

Similar to the derivation of R'_{on}, a basic physical derivation for the specific charge equivalent capacitance across the depletion region of vertical devices $C'_{\mathrm{oss,Q}}$ is presented here.

The definition of the specific (differential) capacitance is:

$$C'_{\mathrm{oss}}(u) = \frac{\mathrm{d}Q'_{\mathrm{oss}}(u)}{\mathrm{d}u}, \tag{A.7}$$

where u is the voltage across the depletion region and Q'_{oss} is the specific charge in the depletion region. In a first step, Q'_{oss} can be written as a function of the extension of the depletion region x_{u}, as

$$Q'_{\mathrm{oss}}(x_{\mathrm{u}}) = x_{\mathrm{u}} q N_{\mathrm{D}} \,. \tag{A.8}$$

With the assumption of an optimally-doped drift region,

$$\frac{E_{\mathrm{u}}}{x_{\mathrm{u}}} = \frac{E_{\mathrm{c}}}{W} = \frac{qN_{\mathrm{D}}}{\varepsilon} \,, \tag{A.9}$$

and with the electric field as a function of applied voltage u, E_u, given by (cf., **Fig. A.1b**)

$$E_\mathrm{u} = \frac{2u}{x_\mathrm{u}} \,, \tag{A.10}$$

the relationship between u and x_u can be found as a function of W and U_B by taking Eq. **(A.10)** and **(A.9)**:

$$u = \frac{x_\mathrm{u}^2}{W^2} U_\mathrm{B} \,. \tag{A.11}$$

With this, the Q'_oss can be written as

$$Q'_\mathrm{oss}(u) = WqN_\mathrm{D}\sqrt{\frac{u}{U_\mathrm{B}}} = \varepsilon E_\mathrm{c}\sqrt{\frac{u}{U_\mathrm{B}}} \,, \tag{A.12}$$

and by deriving Q'_oss with respect to u,

$$\frac{\mathrm{d}Q'_\mathrm{oss}(u)}{\mathrm{d}u} = \frac{\varepsilon E_\mathrm{c}}{2}\frac{1}{\sqrt{U_\mathrm{B}}\sqrt{u}} \tag{A.13}$$

finally yields C'_oss (cf., Eq. **(A.7)**) [40]:

$$C'_\mathrm{oss}(u) = \frac{\varepsilon E_\mathrm{c}}{2}\frac{1}{\sqrt{U_\mathrm{B}}\sqrt{u}} \,. \tag{A.14}$$

Now that the specific differential capacitance across the depletion region $C'_\mathrm{oss}(u)$ has been modelled, the (absolute) charge-equivalent specific capacitance $C'_\mathrm{oss,Q}(u)$ can be analytically obtained. For this, the charge stored in the depletion region has to be calculated. This is done as a function of the voltage utilization of the device β (defined as $u = \beta U_\mathrm{B}$, where $0 \leq \beta \leq 1$):

$$Q'_\mathrm{oss}(\beta) = \int_0^{\beta U_\mathrm{B}} C'_\mathrm{oss}(u)\mathrm{d}u = \varepsilon E_\mathrm{c}\sqrt{\beta} \,. \tag{A.15}$$

The charge Q'_oss stored in the depletion region is independent of the blocking voltage U_B, and only depends on E_c (and not W). This is because for a given E_c, to block a higher voltage U_B, the depletion region W is enlarged (see Eq. **(A.1)**), but to stay below the critical field E_c the charge density N_D must be reduced, leading to a U_B-independent charge in the drift region (see **Fig. A.1b** and Eq. **(A.3)**). Note, however, that for devices that feature two-dimiensional (2D) p-n junctions (e.g., field plate or superjunction concepts [56, 65, 168]) instead of 1D p-n junctions, additional Q'_oss charge to the one modelled in

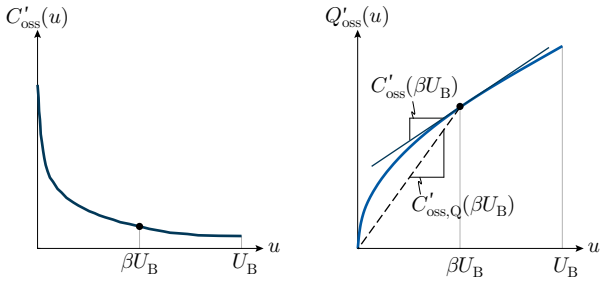

Fig. A.2: Exemplary **(a)** (differential) output capacitance C'_{oss} and **(b)** output charge as a function of u, where the distinction between C'_{oss} and absolute charge-equivalent capacitance $C'_{\mathrm{oss,Q}}$ evaluated at $u = \beta U_{\mathrm{B}}$ is shown.

Eq. **(A.15)** is introduced in the device (due to the 2D nature of the p-n junction) as a trade-off to reduce the R'_{on}.

With the charge defined, the (absolute) charge-equivalent specific capacitance is calculated as

$$C'_{\mathrm{oss,Q}}(\beta) = \frac{Q'_{\mathrm{oss}}(\beta)}{\beta U_{\mathrm{B}}} = \frac{\varepsilon E_{\mathrm{c}}}{\sqrt{\beta} U_{\mathrm{B}}} \,. \tag{A.16}$$

For $\beta = 1$, i.e., a full voltage rating utilization of the device,

$$C'_{\mathrm{oss,Q}} = \frac{\varepsilon E_{\mathrm{c}}}{U_{\mathrm{B}}} \propto \frac{1}{U_{\mathrm{B}}} \tag{A.17}$$

where it can be seen that $C'_{\mathrm{oss,Q}}$ is inversely proportional to the blocking voltage U_{B} for vertical devices. Finally, it is noted that using Eqs. **(A.1)** and **(??)** in Eq. **(A.17)**, it can be found that:

$$C'_{\mathrm{oss,Q}}(u) = 2C'_{\mathrm{oss}}(u) \,, \tag{A.18}$$

yielding that the (absolute) charge-equivalent capacitance is twice the value of the (differential) capacitance across the junction for any given voltage, which is in fair agreement with real semiconductor devices (see **Table A.1**).

A.3 Device Figure-of-Merit

With the previous derivations, the D-FOM obtained in **Section 2.3** can be expressed as a function of the permittivity ε and the resistivity (ρ) or the

Tab. A.1: Capacitance and energy values for a survey of Si/SiC/GaN MOSFETs with different blocking voltage ratings. All of the capacitance, charge, and energy values are evaluated at $u = U_{\mathrm{sw}}$.

Device		Capacitance			$E_{\mathrm{sw,min}}$		
Model	$U_{\mathrm{sw}}(V)$	$C_{\mathrm{oss,Q}}$ (pF)	C_{oss} (pF)	$C_{\mathrm{oss,Q}}/C_{\mathrm{oss}}$	$Q_{\mathrm{oss}}U_{\mathrm{sw}}$ (µJ)	E_{oss} (µJ)	$Q_{\mathrm{oss}}U_{\mathrm{sw}}/E_{\mathrm{oss}}$
1200 V SiC	800	250	131	1.9	159.7	53.1	3.0
650 V SiC	400	482	292	1.7	77.3	27.9	2.8
600 V GaN	400	102	71	1.4	16.4	6.4	2.6
200 V GaN	133	523	365	1.4	9.2	3.7	2.5
200 V Si	133	1336	370	3.6	23.6	5.4	4.4

conductivity (σ):

$$D\text{-}FOM = \frac{1}{\sqrt{R'_{\text{on}} C'_{\text{oss,Q}}}} = \sqrt{\frac{1}{2\varepsilon\rho}} = \sqrt{\frac{\sigma}{2\varepsilon}} \,. \tag{A.19}$$

Alternatively, using the R'_{on} and $C'_{\text{oss,Q}}$ as a function of physical properties of the materials (see Eqs. **(A.5)** and **(A.17)**), the D-FOM can also be defined as:

$$D\text{-}FOM = \frac{1}{\sqrt{R'_{\text{on}} C'_{\text{oss,Q}}}} = \frac{E_{\text{c}}}{2} \frac{\sqrt{\mu}}{\sqrt{U_{\text{B}}}} \propto \frac{1}{\sqrt{U_{\text{B}}}} \,, \tag{A.20}$$

where it is seen that the D-FOM is inversely proportional to the square root of U_{B}. This dependency of the D-FOM on $\frac{1}{\sqrt{U_{\text{B}}}}$ proves to be the case for Si devices, however for the SiC and GaN cases, the dependency is slightly lower, with $\frac{1}{U_{\text{B}}^{0.3}}$ and $\frac{1}{U_{\text{B}}^{0.2}}$, respectively (cf., **Fig. 2.8** and **Table 2.3**).

A.4 Zero-Load-Current Switching - Minimum Hard-Switching Losses

Refs. [57,68] and **Fig. 2.4** show that the minimum hard-switching losses occur while switching zero current and arise due to the capacitive switching losses (see **Fig. 2.4**) for bridge-legs that only employ switch-switch pairs (and not diode-switch pairs). These are defined as $E_{\text{sw,min}} = Q_{\text{oss}}(U_{\text{B}})U_{\text{B}}$, assuming that the switched voltage is the blocking voltage.

However, to get an understanding of how these losses relate to the energy stored in the output capacitance of the device (typically referred to as E_{oss} in the datasheets, a convention that is kept here), Eq. **(A.14)** can be taken to obtain the energy stored in the capacitance:

$$E_{\text{oss}}(U_{\text{B}}) = \int_0^{U_{\text{B}}} C_{\text{oss}}(u) u \, \mathrm{d}u = \frac{1}{3} \varepsilon E_{\text{c}} U_{\text{B}} \tag{A.21}$$

whereas from Eq. **(A.15)** with $\beta = 1$,

$$Q_{\text{oss}}(U_{\text{B}})U_{\text{B}} = \varepsilon E_{\text{c}} U_{\text{B}} \tag{A.22}$$

Hence, the minimum hard-switching losses occurring while switching zero current switch-switch pairs are:

$$E_{\mathrm{sw,min}} = Q_{\mathrm{oss}}(U_{\mathrm{B}})U_{\mathrm{B}} = 3E_{\mathrm{oss}}(U_{\mathrm{B}})\,, \tag{A.23}$$

concluding that the minimum hard-switching losses for switch-switch pairs are approximately three times larger than the E_{oss}, closely matching the energy values given in **Table A.1** for real semiconductor devices.

B

Quasi Two-Level Bridge-Leg

The first step towards using lower-voltage devices when starting from a 2L bridge-leg is to replace a single higher voltage device with a series connection of N devices that each must block U_{dc}/N, which is shown in **Fig. B.1a**. This "Quasi 2-Level" (Q2L) configuration switches all of the high-side or low-side devices simultaneously (no gate signal interleaving), resulting in the same 2L output voltage waveform shown in **Fig. B.1b**. In this case, the FCs shown in the background of **Fig. B.1a** can be used (with substantially reduced capacitance compared to the ML operation) to symmetrically partition the blocking voltage [71, 131].

To maintain the same filter structure and stresses as in the benchmark 2L topology (by ensuring $f_{\mathrm{sw}}|_{\mathrm{Q2L}} = f_{\mathrm{sw}}|_{\mathrm{2L}}$), rewriting Eq. **(2.8)** the minimum semiconductor losses are:

$$P_{\mathrm{semi,min}}\Big|_{\mathrm{Q2L}} = \frac{2 I_{\mathrm{rms}} U_{\mathrm{dc}} \sqrt{f_{\mathrm{sw}}|_{\mathrm{2L}}}}{\textit{D-FOM}\left(\frac{U_{\mathrm{dc}}}{N}\right)}\,, \tag{B.1}$$

which occur when using the optimal bridge-leg semiconductor area of:

$$A_{\mathrm{die,opt,tot}}\Big|_{\mathrm{Q2L}} = 2\frac{N^2 I_{\mathrm{rms}}}{U_{\mathrm{dc}}}\sqrt{\frac{R'_{\mathrm{on}}}{C'_{\mathrm{oss,Q}}\left(U_{\mathrm{dc}}/N\right)\, f_{\mathrm{sw}}|_{\mathrm{2L}}}} \approx \tag{B.2}$$

$$\approx \sqrt{N}\; A_{\mathrm{die,opt,tot}}\Big|_{\mathrm{2L}}\,.$$

With Eqs. **(2.2)** and **(2.7)**, it is found that the optimum die area $A_{\mathrm{die,opt,tot}}$ of a Q2L bridge-leg is $\sqrt{N}\times$ larger than for a 2L bridge-leg.

Comparing Eqs. **(2.14)** and **(B.1)**, it can be seen the losses in the Q2L arrangement are only lowered by the ratio of $\textit{D-FOM}\left(\frac{U_{\mathrm{dc}}}{N}\right)$ to $\textit{D-FOM}\left(U_{\mathrm{dc}}\right)$,

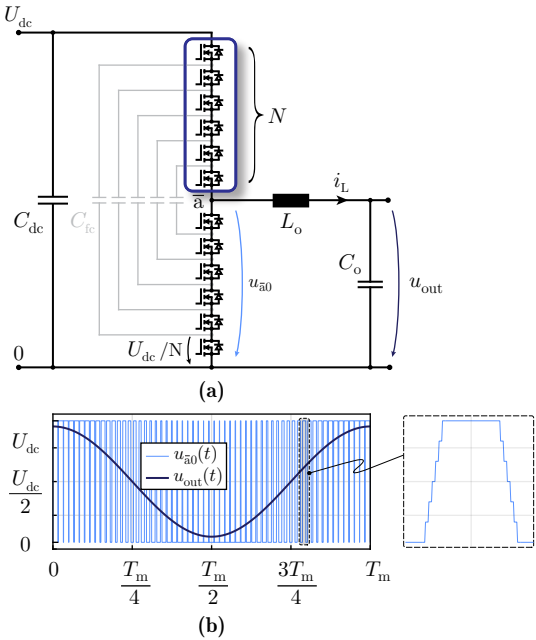

Fig. B.1: (a) Quasi Two-Level ("Q2L") bridge-leg configuration, with $2N$ devices per bridge-leg, featuring **(b)** a 2L waveform with staircase shaped transitions [131]. Each power device must withstand U_{dc}/N, and small capacitors may be added to ensure equal voltage balancing during switching transients [71].

i.e., there is no topological advantage (switching frequency multiplication) beyond the improved D-FOM of lower voltage devices (as there is for ML structures, as discussed in **Section 2.4**). Hence, for the quasi same output voltage waveform (i.e., same filter stress), the bridge-leg semiconductor losses are reduced by a factor $\approx \sqrt{N}$:

$$P_{\text{semi,min}}\big|_{\text{Q2L}} \approx \frac{P_{\text{semi,min}}\big|_{\text{2L}}}{\sqrt{N}}, \tag{B.3}$$

at the cost of an $\approx \sqrt{N}$ factor increase in die area. The X-FOM for the Q2L topology is, then:

$$X\text{-}FOM|_{\text{Q2L}} = D\text{-}FOM\left(\frac{U_{dc}}{N}\right) \approx \sqrt{N} \cdot D\text{-}FOM|_{\text{2L}} \ . \tag{B.4}$$

C

Switching Losses in Multi-Level Bridge-Leg Semiconductors

In **Section 2.2.2**, the minimum (capacitive) hard-switching losses were analyzed for a 2L bridge-leg. This analysis is extended to a ML FC arrangement in the following. For the sake of clarity, initially a 3L bridge-leg is considered and later generalized to an $(N+1)$-level structure.

Fig. C.1a,b revisit the conduction states for the middle (2^{nd}) and the uppermost (3^{rd}) level of a 3L bridge-leg: state ① outputs U_{dc} at the node $\overline{\text{a}}$ (with reference to the negative DC bus), whereas state ② and ③ are generating $u_{\overline{\text{a}}} = \frac{U_{\text{dc}}}{2}$. Assuming a positive inductor current i_{L}, state ② discharges and ③ charges the FC C_{fc}.

For positive i_{L}, the switching transitions from state ② → ① and ③ → ① are hard-switched transitions, and ① → ② and ① → ③ are soft-switched transitions (the opposite holds for negative i_{L}).

To analyze the minimum (capacitive) hard-switching losses, the ② → ① hard-switched transition, which occurs once every switching period T_{sw} for the switch pair T_1 and $\overline{\text{T}}_1$, is shown in **Fig. C.1c**.

A charge Q_{oss} is delivered by the input voltage source, resulting in a charging of the C_{oss} of $\overline{\text{T}}_1$ to $u_{\overline{\text{T}}_1} = \frac{U_{\text{dc}}}{2}$, and a (slight) charging of C_{fc}. Considering C_{fc} as a temporary lossless voltage source with voltage $\frac{U_{\text{dc}}}{2}$, and performing an energy balance of the switching transition [57], this results in a dissipated energy of

$$E_{\text{dissipated}} = Q_{\text{oss}} \frac{U_{\text{dc}}}{2} = Q_{\text{oss}} U_{\text{sw}}. \tag{C.1}$$

This equation holds for $(N+1)$-level bridge-legs, where $U_{\text{sw}} = \frac{1}{N} U_{\text{dc}}$, and Q_{oss} is the output capacitance charge evaluated at U_{sw}.

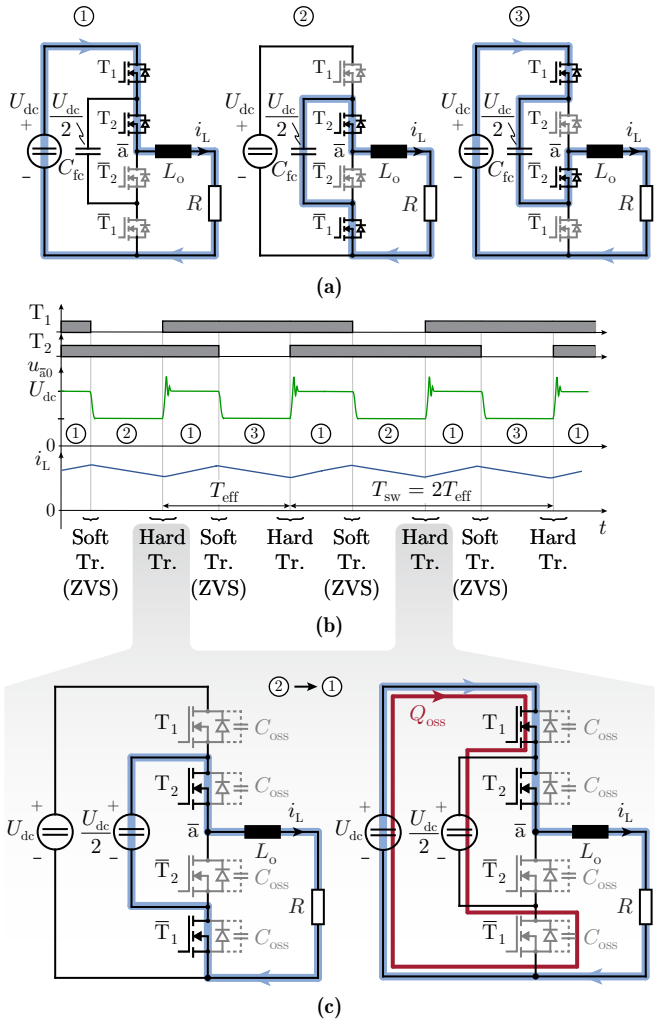

Fig. C.1: (a) Conduction states for the middle (2^{nd}) and the uppermost (3^{rd}) level of a 3L FCC bridge-leg, shown for positive i_{L}. **(b)** Characteristic waveforms of the 3L bridge-leg: T_1 and T_2 gate signals ($\overline{\text{T}}_1$ and $\overline{\text{T}}_2$ feature the opposite gate signals, respectively), the output voltage node voltage $u_{\bar{\text{a}}0}$ and the output current i_{L}. **(c)** Hard-switched transition of the 3L bridge-leg, where the load current commutates from $\overline{\text{T}}_1$ to T_1. C_{fc} is considered to be a lossless voltage source with voltage $\frac{U_{\text{dc}}}{2}$ during the switching instant.

D

Further Experimental Data on Switching Characteristics

Although GaN HEMT devices do not have any reverse recovery charge Q_{rr} [56], SiC, and especially Si devices, present a reverse recovery effect caused by their intrinsic body diodes. To analyze the behavior of the reverse recovery, extensive measurements of the Q_{rr} were carried out at different temperatures and voltages for 1200 V 25 mΩ and 80 mΩ SiC MOSFETs from *Wolfspeed* (C2M0025120D and C2M0080120D). The Q_{rr} is obtained from a double pulse test (DPT) setup [57], by integrating the drain-source current waveform from the moment it crosses the zero-current line, and subtracting the Q_{oss} charge that simultaneously flows to charge the output capacitance of the device, as shown in **Fig. D.1**.

A summary of the obtained results is shown in **Fig. D.2**, where it can be seen that the Q_{rr} data fits a first order function as described in **Section 3.3.1**. In literature, both a linear and a square root dependency of the drain current to the reverse recovery charge can be found [79, 166, 170, 171]. However, Q_{rr} can, in a first approximation, be modeled with a linear current dependency to improve the minimum switching loss model (cf., **Fig. D.2**). No noteworthy die area dependency was observed between the 25 mΩ and 80 mΩ SiC MOSFETs, where the difference in die areas is of ≈ x3. Note that besides the temperature and current dependency of the Q_{rr}, there are other influencing factors such as dead time and $\mathrm{d}i/\mathrm{d}t$ [170, 172–174], which are not further analyzed in this work.

Furthermore, the Q_{oss} was measured for different temperature values in **Fig. D.3** for both the specified 1200 V 25 mΩ and 80 mΩ SiC MOSFETs, where it is again shown that the measured and datasheet-extracted Q_{oss} values match for these MOSFETs. As expected, the Q_{oss} is not temperature

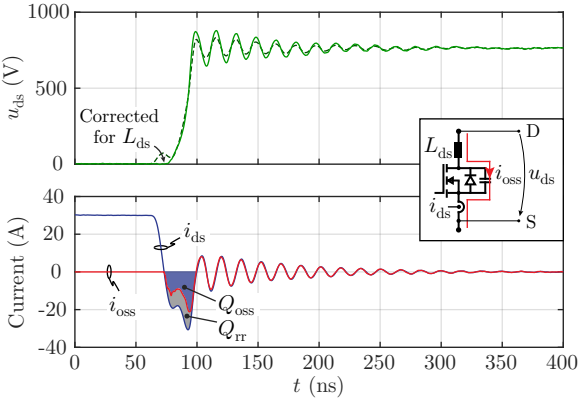

Fig. D.1: Measured drain-source voltage u_{ds} (dashed line) and calculated actual u_{ds} considering the voltage drop across the parasitic inductance L_{ds} (continuous line), and measured drain-source current i_{ds} together with the recreated output capacitance current i_{oss} (bottom). A charge distinction between Q_{oss} and Q_{rr} is done, showing that both occur simultaneously. Data is taken from a measured switching transient of a C2M0025120D SiC MOSFET.

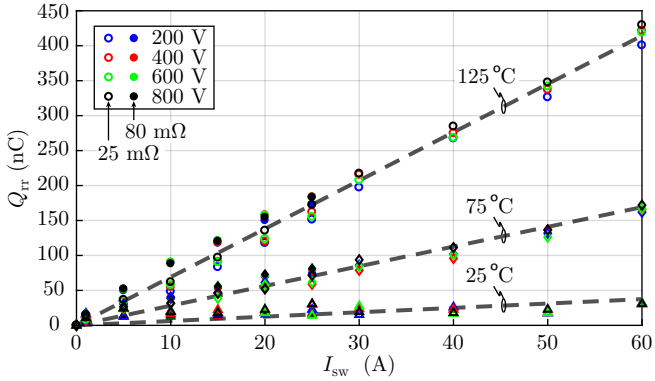

Fig. D.2: Measured Q_{rr} for the 1200 V 25 mΩ (C2M0025120D) and 80 mΩ (C2M0080120D) SiC MOSFET from *Wolfspeed*. The linearization of the Q_{rr} with respect to the switched current I_{sw} is shown with dashed lines for 25 °C, 75 °C and 125 °C. The average di/dt is 1430 A/µs and the dead time is 200 ns.

dependent, meaning that a temperature increase does not incur additional capacitive switching losses, at least for the analyzed devices.

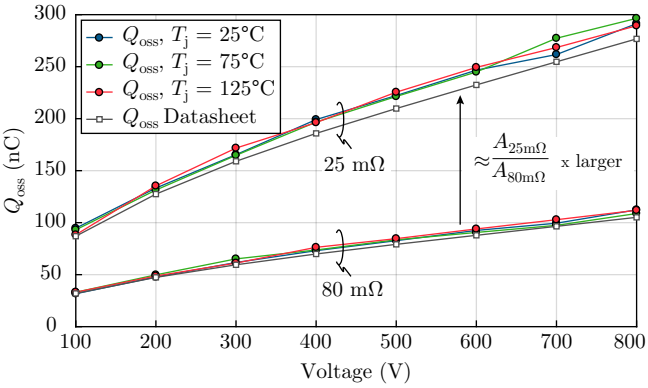

Fig. D.3: Datasheet-extracted and measured output capacitance charge Q_{oss} data at different junction temperatures for 1200 V 25 mΩ and 80 mΩ SiC MOSFETs from *Wolfspeed* (C2M0025120D and C2M0080120D).

For older generations of Si MOSFETs, since $Q_{rr} \gg Q_{oss}$, the manufacturer provided values typically include Q_{oss} within Q_{rr} [77, 172]. However, with SiC and the new generations of Si MOSFETs, both Q_{rr} and Q_{oss} are of the same order of magnitude (cf., **Fig. D.2** and **Fig. D.3**) and have to be correspondingly separated. **Fig. D.1** indicates that the reverse recovery phase of the internal body diode of the MOSFETs occurs at the same time the parasitic output capacitance C_{oss} is being charged (and hence the voltage across the device is rising). As shown in **Fig. D.1**, after correcting the measured drain-source voltage u_{ds} of the MOSFET for the parasitic inductance voltage drop through data post-processing, the current charging the output capacitance i_{oss} is recreated by use of the $C_{oss}(u)$ data. Note that for this case L_{ds} = 15 nH, which is mostly due to the leads and bond wires of the TO-247 package and the low-inductive current shunt.

Hence, it can be concluded that for state-of-the-art power MOSFETs, where Q_{rr} and Q_{oss} can be of similar values, a clear distinction between Q_{rr} and Q_{oss} is necessary, particularly when using Q_{rr}. If the Q_{rr} charge is calculated by integrating the i_{ds} measurement over time, as in **Fig. D.1**, it is important to subtract the Q_{oss} charge from it, such that if e.g., Eq. **(3.1)** is used to calculate the switching losses, the Q_{oss} is not accounted for twice.

E

Accurate Efficiency Measurements: Electric vs. Calorimetric Methods

For power converters in the low- and mid-ninety percent efficiency range, the efficiency can be directly determined using a power analyzer. However, for ultra-efficient converters, particularly for those in the 99+ % efficiency range [9, 44, 66, 175], accurately determining the efficiency characteristic requires additional calorimetric loss measurements. In the following, both the electric and calorimetric efficiency measurement methods are described, followed by a discussion and comparison between them.

E.1 Electric Efficiency Measurement

The first approach to determine efficiency is to measure the input and output powers, P_{out} and P_{in} respectively, using a precision power analyzer:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \,. \tag{E.1}$$

However, since P_{out} and P_{in} are large values in comparison to the power losses, a small error in the measurement of both power values can lead to a large deviation in the measured efficiency, and therefore has to be considered accordingly [44, 175]. Assuming that P_{out} and P_{in} are measured with an error ΔP_{out} and ΔP_{in}, respectively, the worst-case absolute error of the efficiency measurement $\Delta\eta$ can be calculated as

$$\eta + \Delta\eta = \frac{P_{\text{out}} + \Delta P_{\text{out}}}{P_{\text{in}} - \Delta P_{\text{in}}} \,, \tag{E.2}$$

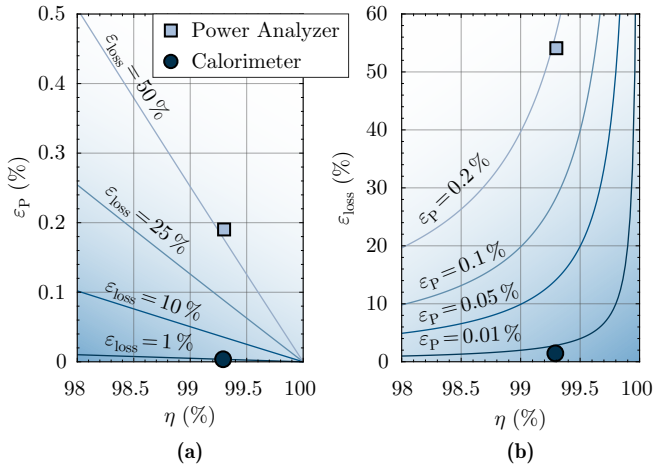

Fig. E.1: (a) Graphical representation of the relative power loss calculation error $\varepsilon_{\text{loss}}$ as a function of the relative power measurement error ε_{p} and efficiency η, and **(b)** vice versa. The accuracy of the performed efficiency measurements with the *Yokogawa WT3000* precision power analyzer (■) and the calorimeter (●) [44] is shown for a processed power of 10 kW.

whereby using the relative measurement errors, $\varepsilon_{\text{Pout}} = \frac{\Delta P_{\text{out}}}{P_{\text{out}}}$ and $\varepsilon_{\text{Pin}} = \frac{\Delta P_{\text{in}}}{P_{\text{in}}}$, then $\Delta\eta$ is given by

$$\Delta\eta = \eta \frac{(\varepsilon_{\text{Pout}} + \varepsilon_{\text{Pin}})}{(1 - \varepsilon_{\text{Pin}})} \,. \tag{E.3}$$

If the output and input power measurement show the same error, ε_{P}, the error of the efficiency measurement can be approximated as

$$\Delta\eta \approx \varepsilon_{\text{Pout}} + \varepsilon_{\text{Pin}} \approx 2\varepsilon_{\text{P}} \,. \tag{E.4}$$

For the case at hand, the *Yokogawa WT3000* precision power analyzer was used to electrically measure the efficiency. To determine the efficiency measurement error, errors are specified for both the DC and the AC power measurement as follows: firstly, an error depending on the power reading, ε_{Y}, and secondly, an error depending on the power range X in which the measurement has been taken, ε_{X}. With these two errors, the power measurement errors for the DC side input ε_{Pdc} and the three-phase AC power output ε_{Pac} can be calculated as

Tab. E.1: Calorimeter accuracy specifications [44].

P_{loss}	Error ($\varepsilon_{\text{loss}}$)
<10 W	<± 3.5 %
<100 W	<± 1 %
<200 W	<± 0.5 %

$$\varepsilon_{\text{Pdc}} = \varepsilon_{\text{Y,dc}} + \frac{X_{\text{Pdc}}}{P_{\text{DC}}} \varepsilon_{\text{X,dc}} \tag{E.5}$$

$$\varepsilon_{\text{Pac}} = 3 \left(\varepsilon_{\text{Y,ac}} + \frac{X_{\text{Pac}}}{P_{\text{AC},1\phi}} \varepsilon_{\text{X,ac}} \right) , \tag{E.6}$$

where P_{DC} is the power taken from the DC-side, and $P_{\text{AC},1\phi}$ is the power of one the three phases (under balanced load conditions, all three phases process the same power).

For an efficiency measurement at 10 kW, Eq. **(E.5)** yields $\varepsilon_{\text{Pdc}} = \pm\, 0.25\,\%$ and Eq. **(E.6)** $\varepsilon_{\text{Pac}} = \pm\, 0.13\,\%$, leading to a large error of the efficiency measurement of $\Delta\eta = \pm\, 0.38\,\%$.

E.2 Calorimetric Efficiency Measurement

For ultra-high efficiency converters, a second approach that leads to more accurate efficiency measurements is used, i.e. a calorimetric measurement, which by directly measuring the power losses P_{loss}, allows to calculate the efficiency as

$$\eta = 1 - \frac{P_{\text{loss}}}{P_{\text{in}}} . \tag{E.7}$$

An error in the loss measurement leads to an absolute error in the efficiency of only

$$\Delta\eta = \frac{\Delta P_{\text{loss}}}{P_{\text{in}}} = (1 - \eta)\, \varepsilon_{\text{loss}} , \tag{E.8}$$

where $\varepsilon_{\text{loss}}$ is the relative error in the power loss measurement.

The employed calorimeter is presented in [44], and determines the power losses by measuring the coolant volume flow $\dot{V}$ and the coolant temperature difference between the input and output of the calorimeter ΔT, with

$$P_{\text{loss}} = c_{\text{p}} \rho \dot{V} \Delta T \,, \tag{E.9}$$

where c_{p} is the specific heat capacity of the coolant, and ρ is the mass density [176]. The main advantage of calorimetric measurement method is that the power losses can be measured independent from the power processed by the converter, and its accuracy therefore only depends on the error with which P_{loss} can be measured. In this case, since the accuracy of both $\dot{V}$ and ΔT profit from higher measured values, which occur when measuring higher values of P_{loss}, the accuracy of the employed calorimeter increases for higher measured power losses, as shown in **Table E.1**. Finally, it has to be noted that the accuracy of the calorimetric measurements benefit further from calibration, which is performed before taking measurements on a device under test.

E.3 Accuracy Comparison of Electric and Calorimetric Efficiency Measurements

A general comparison between both measurement methods can be done by finding a relation between ε_{P} and $\varepsilon_{\text{loss}}$, which with Eqs. **(E.3)** and **(E.8)** yields:

$$\varepsilon_{\text{loss}} = \frac{\eta \left(\varepsilon_{\text{Pout}} + \varepsilon_{\text{Pin}} \right)}{\left(1 - \varepsilon_{\text{Pin}}\right) \left(1 - \eta\right)} \approx \frac{2\varepsilon_{\text{P}}}{\left(1 - \eta\right)} \,. \tag{E.10}$$

The relation between ε_{P} and $\varepsilon_{\text{loss}}$ can be seen in **Fig. E.1**, where additionally the errors for the efficiency measurement for the converter at hand for 10 kW operation are shown for both the electric measurement with the precision power analyzer and the calorimeter. It is seen that for the electric efficiency measurement, the relative error in the power loss determination is above 50 %. Accordingly, in order to achieve the same performance as with the calorimeter ($\varepsilon_{\text{loss}} = 1\,\%$), the accuracy when measuring the input and output power would have to be 0.003 %, which is not possible with state-of-the-art precision power analyzers.

Finally, the difference of the efficiency calculation confidence interval for both measurement methods is shown in **Fig. E.2** for the presented converter. It can be seen that for operation at two different power levels (2 kW and 10 kW), the uncertainty in the calorimetric efficiency measurement is much smaller than with an electric measurement.

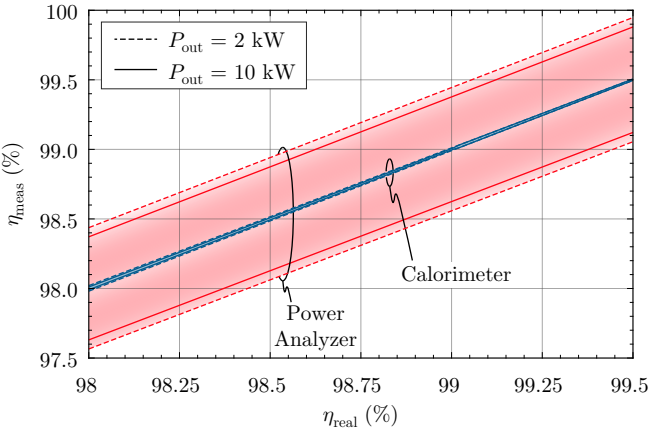

Fig. E.2: Confidence interval for the measured efficiency (η_{meas}) vs. the real efficiency (η_{real}) for the presented inverter, where $\eta_{\text{meas}} = \eta_{\text{real}} \pm \Delta\eta$. Both electric (*Yokogawa WT3000* precision power analyzer) and calorimetric [44] efficiency measurements are shown for 2 kW and 10 kW of processed power.

F

Three Levels Are Not Enough for Ultra-High-Efficiency Three-Phase Systems

This Appendix summarizes the most relevant findings concerning the comparative evaluation of 800 V_{dc} vs. 400 V_{dc} AC/DC converter systems also published in:

- **J. Azurza Anderson**, G. Zulauf, P. Papamanolis, S. Hobi, S. Mirić, J. W. Kolar, "Three levels are not enough: Scaling laws for multi-level converters in AC/DC applications," *IEEE Transactions in Power Electronics*, vol. 36, no. 4, pp. 3967–3986, 2021.

Motivation

The reason why 99+ % efficiency for 230 V_{rms} systems can be achieved with a conventional totem-pole 2L topology with unfolder bridge-leg for single-phase 400 V_{dc} DC-link systems, whereas for the same efficiency, 800 V_{dc} DC-link systems require complex multi-level solutions is explained in this Appendix.

Executive Summary

Single-phase inverters and rectifiers in 230 V_{rms} applications, with a DC-side voltage of 400 V_{dc}, achieve ultra-high efficiency with a simple 2L topology. These single-phase designs typically utilize a line-frequency unfolder stage, which has very low losses and essentially doubles the peak-to-peak voltage that can be generated on the AC-side for a given DC-link voltage. For certain applications, however, such as higher-power grid-connected photovoltaic inverters, electric vehicle chargers and machine drives, three-phase converters are needed. Due to the three-phase characteristic of the system, unfolders cannot be similarly used, leading to a higher minimum DC-link voltage determined by the three-phase line-to-line voltage amplitude, which is typically set to 800 V_{dc} for 230 V_{rms} phase voltage systems. Previous demonstrations indicate that significantly more levels – and the associated higher cost and complexity – are required for ultra-high-efficiency three-phase converters relative to their single-phase counterparts. In this Appendix, it is sought to determine the fundamental reason for the performance difference between three-phase, 800 V_{dc} DC-link and single-phase, 400 V_{dc} converters. First, a 2.2 kW AC/DC hardware demonstrator is built to confirm the necessity of higher-complexity converters, showing a simultaneous reduction in efficiency and power density between a 2L, 400 V_{dc} benchmark (99.2 % peak efficiency at 18.0 kW/dm³) and a 3L, 800 V_{dc} AC/DC converter phase-leg (98.8 %, 9.1 kW/dm³). Scaling laws indicate that 6 or more levels would be required for an 800 V_{dc}, three-phase AC/DC converter to meet or exceed the bridge-leg efficiency of a 2L 400 V_{dc} GaN benchmark for a fixed output filter with commercially-available Si or GaN power semiconductors. After performing a comprehensive Pareto optimization, it is found that at least 7L are necessary to recover the efficiency of the 2L, 400 V_{dc} benchmark, and this theory is validated with a 7L, 800 V_{dc}, 2.2 kW hardware prototype with a power density of 15.8 kW/dm³ and a peak efficiency of 99.03 %. Finally, two practical solutions that make use of the benefits of unfolder bridges familiar in single-phase systems are identified for three-phase systems.

F.1 Introduction

Ultra-efficient and power-dense AC/DC and DC/AC power converters are critical for a broad range of emerging applications, from renewable energy converters [177] to more-electric aircraft motor drives [17] to PFC rectifiers [44, 58]. Single-phase inverters and rectifiers, such as the bridgeless totem-pole PFC rectifier shown in **Fig. F.1a**, typically include an unfolder bridge-leg to provide a return path for the current, that operates at line-frequency (50 Hz – 60 Hz) and can therefore be designed for very low conduction losses [59]. This unfolder essentially doubles the "effective" output voltage from the DC-link voltage, U_{dc}, to $2U_{dc}$ without increasing the semiconductor or capacitor

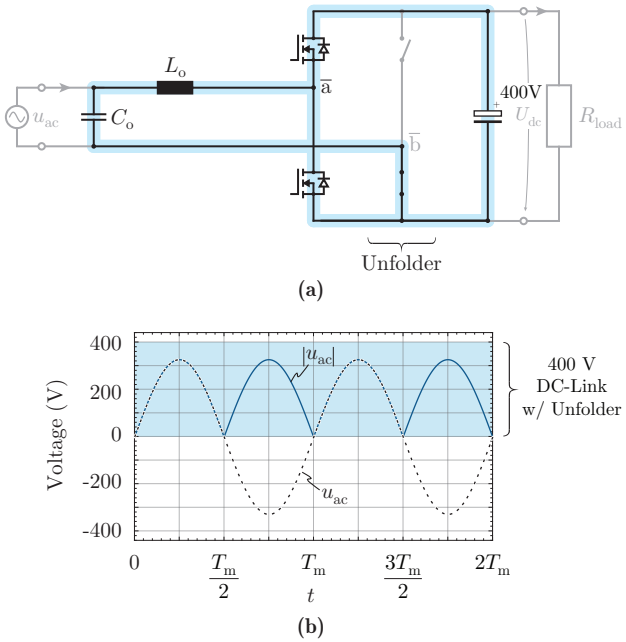

Fig. F.1: (a) Single-phase, 2L, totem-pole, PFC rectifier, with a high-frequency bridge-leg (highlighted) and a line-frequency unfolder (which is typically implemented with Si SJ-MOSFETs and is only conceptually indicated) used to generate a bipolar output. Output capacitance must be sized to provide power pulsation buffering. **(b)** Typical voltage waveforms (for two line periods T_m) of a 230 V_{rms} single-phase PFC rectifier like in **(a)**, where the continuous line represents the rectified sinusoidal voltage $|\, u_{ac} \,|$ and the dashed line represents the single-phase grid voltage u_{ac}. The unfolder permits operation with a 400 V_{dc} to 450 V_{dc} DC-link for a 230 V_{rms} phase voltage.

voltage stresses, allowing single-phase designs for 230 V_{rms} – 240 V_{rms} lines to operate with DC-link voltages near 400 V_{dc} – 450 V_{dc} (with around 20 % voltage margin), as shown in **Fig. F.1b**.

These single-phase systems, however, are limited by 16 A_{rms} feeds to 3.7 kW, and by the less-common 32 A_{rms} outlets to 7.4 kW [178]. Therefore, for applications that require higher power ratings such as residential PV inverters, EV chargers and machine drives, a three-phase 230 V_{rms} – 240 V_{rms} (line-to-neutral) interface is required, where oftentimes the power that each one of the three phases processes is similar to that of single-phase systems [156,

178, 179]. In contrast to single-phase systems, however, three-phase inverters and rectifiers (**Fig. F.2a**) cannot straightforwardly utilize a similar unfolding technique, given that the current that is generated in one of the phases is returned through the other two phases. Accordingly, in these systems, the DC-link voltage must be doubled to near 720 V_{dc} – 800 V_{dc} [61], as shown in **Fig. F.2b**, as the AC voltage is generated against the DC-link midpoint. For the same AC power and phase voltage, then, three-phase systems will have lower DC current but at the penalty of doubled voltage stresses on the key components, as the high-frequency bridge-leg must generate both the positive- and negative-polarity AC cycles.

For 400 V_{dc} DC-link voltage single-phase systems (used, for example, in data center power supply modules or solar inverters), a literature review finds that a simple "2L" half-bridge (**Fig. F.3a**) can deliver efficiencies above 99 % [58, 59,180] and as high as 99.1 % [132]. Designs with more levels and/or interleaved stages – a preferred approach in the Google Little Box Challenge [60] – achieve higher power densities through filter size reduction [17, 44, 49, 181–184], but these higher-complexity designs generally do not improve upon the efficiency of a 2L design.

Ultra-high-efficiency three-phase 800 V_{dc} DC-link voltage inverters and rectifiers shown in literature, however, feature much higher complexities. In [185], a 5L E-type converter reaches a peak efficiency of 98.3 %. Similarly, in Ref. [30], 13 levels are used to achieve 98.3 % peak efficiency with low-voltage GaN devices. Ref. [29] utilizes a 5L T-type inverter with 1200 V SiC devices for 99.2 % peak AC/DC semiconductor efficiency at 720 V_{dc} input voltage, and an all-Si, 7L design in [50] (**Chapter 4**) peaks at 99.3 % efficiency at the same 720 V_{dc} input voltage.

The interest naturally arises, then, to assess the fundamental reason behind the performance difference between simple 2L single-phase systems, which can operate with 400 V_{dc} DC-links due to the (nearly lossless [58, 60]) unfolder stage, and three-phase systems, where the required DC-link voltage is near 800 V_{dc} and most of the ultra-high-efficiency converters presented in literature feature a more complex ML structure, see **Table 1.3**. Hence, the goal of this analysis is to assess if 3Ls are "enough" for an 800 V_{dc} DC-link voltage system to recover the performance of a 400 V_{dc} DC-link voltage system, or if this can only be achieved by using a higher number of levels. For this, the following comparison is centered on ML converters, and in particular on the FCC topology (**Fig. F.2a**) [49, 51, 186], which is capable of generating DC outputs and is gaining interest in both single- and three-phase systems to achieve ultra-high-efficiency and/or power density. Although compared

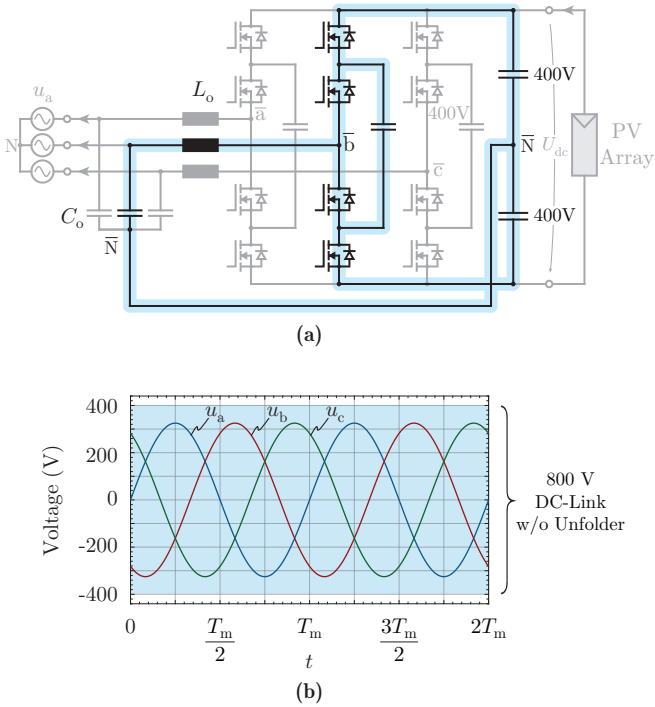

Fig. F.2: (a) Three-phase grid-tied FC inverter with 3L, shown for a solar photovoltaic (PV) application, with one of the three high-frequency bridge-legs highlighted. With a 3L configuration, identical semiconductors with > 400 V voltage ratings can be used in **(a)** as in **Fig. F.1a**. The DC-link capacitor does not need to provide power pulsation buffering due to the overall constant power flow of three-phase systems. **(b)** Typical voltage waveforms of a 230 V_{rms} line-to-neutral three-phase PFC rectifier like in **(a)**, where the three-phase grid voltages u_a, u_b and u_c are shown. For the three-phase system case, a 720 V_{dc} – 800 V_{dc} DC-link is required to generate the 230 V_{rms} phase voltages.

to a conventional half-bridge (**Fig. F.1a**), ML converters (a) increase the effective frequency (f_{eff}) at the filter for a given switching frequency (f_{sw}), (b) apply smaller voltage steps to the filter inductor, and (c) enable the use of lower-voltage power semiconductors, increasing the numbers of levels of converter designs to improve efficiency may carry, for particular applications, penalties in power density, cost, and/or reliability and maintenance [61, 187].

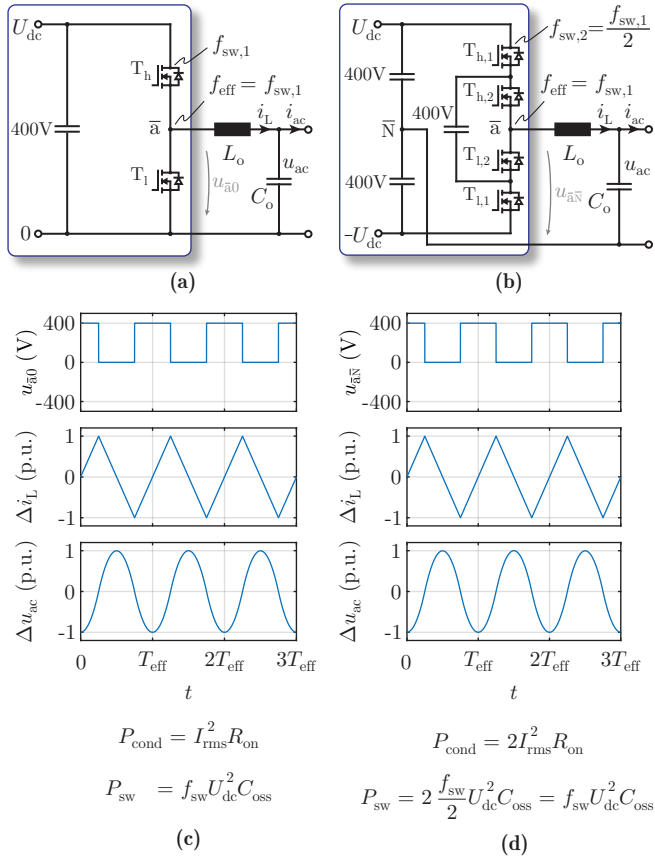

Fig. F.3: Comparison of power circuits and key waveforms between 400 V_{dc} DC-link, 2L and 800 V_{dc} DC-link, 3L FCC designs. **(a)** 2L, 400 V_{dc} DC-link converter circuit, with the line-frequency unfolder in **Fig. F.1a** removed to highlight the high-frequency bridge-leg comparison. **(b)** 3L, 800 V_{dc} DC-link FCC circuit, with the switching frequency (f_{sw}) halved to keep the same effective switching frequency at the bridge-leg output terminal, inductor current ripple, and capacitor voltage ripple. **(c)** Key normalized waveforms and semiconductor losses for the 2L, 400 V_{dc} benchmark. **(d)** Key normalized waveforms and semiconductor losses for the 3L, 800 V_{dc} design, referenced to the DC-link midpoint $\overline{N}$. With the same power devices, conduction losses double and capacitive switching losses remain the same when moving to the 800 V_{dc} DC-link in three-phase converters.

Therefore, to more deeply analyze the performance difference between the single-phase 400 V_{dc} DC-link voltage and the three-phase 800 V_{dc} DC-link voltage cases presented in **Fig. F.1a** and **Fig. F.2a**, the individual bridge-legs shown in **Fig. F.3a-b** are analyzed, respectively. When moving from a 400 V_{dc} DC-link to an 800 V_{dc} DC-link for a three-phase system, as a first step towards a ML approach, a third level to mitigate the component stress increase and reuse the same power switches and output filter (**Fig. F.3b**) [97] can be added. With f_{sw} halved and all other components kept the same, the output filter waveforms (f_{eff} and current ripple magnitude, Δi_L, and voltage ripple magnitude, Δu_{ac}) are identical (**Figs. F.3c-d**), and therefore the filter losses and performance do not change (assuming the filter capacitor star point is connected to the DC-link midpoint [188], as shown in **Fig. F.3b**). Output current now flows through two devices instead of one, doubling the conduction losses, and the hard-switching losses are kept constant (since the switched current is the same in both cases across all switching cycles). Due to the 2× higher conduction losses and additional components, the 800 V_{dc}, 3L design must have lower efficiency and lower power density than a 400 V_{dc}, 2L bridge-leg. With the chip area re-optimized (and increased) for the 3L design, the increase in losses is slightly smaller than the increase in this case of identical switches, but the 400 V_{dc}, 2L bridge-leg will still outperform the 800 V_{dc}, 3L design. In this analysis, and for the remainder of the Appendix, the losses in any unfolder stages are ignored. This approximation is valid because the unfolder stages switch at line frequency, hundreds or thousands of times slower than the bridge-leg semiconductors, and therefore incur negligible switching losses. Without switching losses as a trade-off, the die area of the unfolder power semiconductors can be increased to nearly eliminate conduction losses and therefore any unfolder-stage cooling requirements. A more detailed justification of neglecting the unfolder stage losses is included in **Section F.2** and [60].

While this simple analysis, **Fig. F.3** shows that 3Ls are clearly not enough for ultra-high-efficiency at 800 V_{dc}, the number of levels for a given efficiency target is not known from existing literature. Ref. [52] aims to keep the semiconductor losses constant and optimize the output filter, and general design criteria for ML converters are included in [51, 186, 189, 190]. Here, after determining with the semiconductor scaling laws given in **Chapter 2** that 7Ls would be enough for an 800 V_{dc} system to regain the efficiency of a 400 V_{dc} 2L system, this prediction is finally validated with a hardware prototype.

In **Section F.2**, 2L, 400 V_{dc} and 3L, 800 V_{dc} AC/DC converters are built and characterized to verify the intuition that 3Ls are indeed "not enough,"

motivating the remainder of the Appendix. After determining with semiconductor scaling laws that at least 7Ls are necessary in **Section F.3**, an efficiency versus power density Pareto optimization is performed in **Section F.4** to ascertain this prediction, determining the design of a Pareto-optimized 7L, 800 V_{dc} inverter which is built and characterized in **Section F.5**, to validate that the theorized 7Ls are "enough" to regain the efficiency of the 2L, 400 V_{dc} benchmark. **Section F.6** highlights paths forward for ultra-high-efficiency three-phase inverters and rectifiers through a system-wide lens.

F.2 Hardware Validation: 3 Levels are Not Enough

To validate the intuition that 3Ls are indeed not enough for an 800 V_{dc} DC-link bridge-leg to recover the efficiency (or power density) of a 2L, 400 V_{dc} benchmark, a loss-optimized 2.2 kW AC/DC converter shown in **Fig. F.4c** is constructed, which can be used for the 3L 800 V_{dc} (**Fig. F.4b**) as well as for the 2L 400 V_{dc} analysis (cf., **Fig. F.4a**, operation limited to cyclic repetition of the positive half-cycle of an actual single-phase PFC rectifier system). The design details are shown in **Table F.1**. These inverters utilize 35 mΩ, 600 V GaN-on-Si HEMTs and film capacitors. Note that using for the converter in **Fig. F.4c** the MLCC utilized in **Section F.5**, the volume of the FCs could be decreased by approximately a factor of 3 at a ×10…15 higher cost, but would not change the key bridge-leg comparison. The 3L design operates with half the switching frequency (f_{sw} = 35 kHz) of the 2L design (f_{sw} = 70 kHz, selected to be similar to previous literature and existing commercial designs, e.g., [132]), keeping in **Fig. F.4** identical output filter waveforms as described in **Fig. F.3**.

The measured AC/DC efficiencies for each design are reported in **Fig. F.5a**, and, as expected, the 3L, 800 V_{dc} design has both lower efficiency and, because of the extra semiconductor stage for the 3L characteristic and the FCs, lower power density (see **Table F.1**). Efficiencies are measured with the *Yokogawa WT3000* precision power analyzer, which is shown in **Appendix E** to have excellent agreement with calorimetric techniques in this efficiency and output power range. The peak efficiency for the 2L, 400 V_{dc} inverter is 99.2 %, and the peak efficiency for the 3L, 800 V_{dc} inverter is 98.8 %. Both efficiencies are relatively flat from 40 % to 120 % load. The power pulsation buffer capacitors and unfolder stage necessary for single-phase conversion are both excluded from the efficiency measurements and reported power densities, as the goal

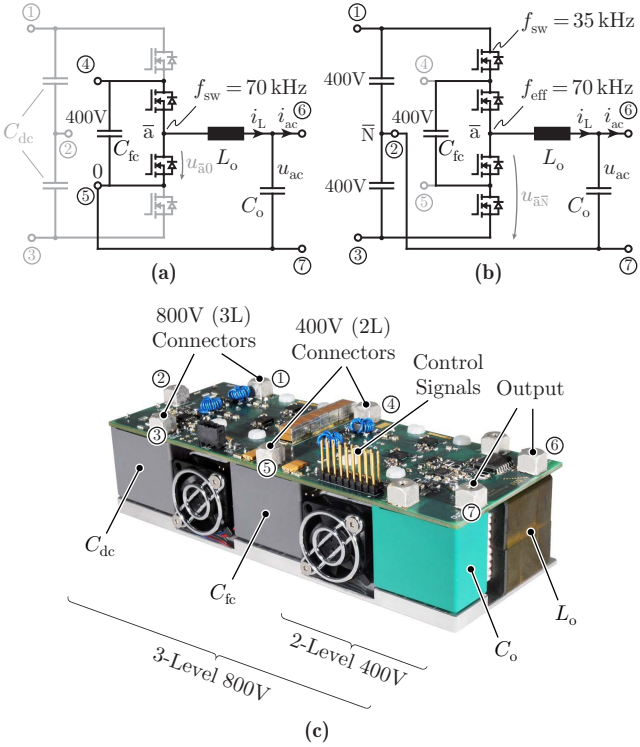

Fig. F.4: (a) 2L 400 V_{dc} and **(b)** 3L 800 V_{dc} hardware connection schematics of the **(c)** loss-optimized 2.2 kW AC/DC inverter used for experimental 2L, 400 V_{dc} and 3L, 800 V_{dc} comparison (cf., **Fig. F.3**). 2L inverter operates at f_{sw} = 70 kHz and 3L inverter operates at f_{sw} = 35 kHz to maintain the same f_{eff}. 2L size is 61 mm × 59 mm × 34 mm (18.0 kW/dm^3), and 3L size is 121 mm × 59 mm × 34 mm (9.1 kW/dm^3).

of this study is to compare the bridge-legs in single-phase and three-phase systems.

The exclusion of the unfolder can be justified considering two aspects: losses and costs. A typical single-phase 400 V_{dc} power supply features a high switching frequency bridge-leg realized with GaN devices, and a low-frequency (mains frequency) unfolder bridge-leg implemented with Si SJ devices to save costs [132]. Taking as example for the unfolder realization the lowest R_{on} class Si SJ-devices available in the market (34 mΩ devices at a junction temperature of T_j = 125 °C [191, 192]), the losses would be around 3.8 W, incurring a 0.19 % efficiency penalty at 2.0 kW, cf., **Fig. F.5a**. To analyze

Tab. F.1: Components, key values, and performance metrics for the constructed AC/DC inverters of **Figs. F.5** and **F.6**. Component labels reference **Fig. F.3**.

Parameter	400 V_{dc}, 2L	800 V_{dc}, 3L
U_{dc}	400 V_{dc}	800 V_{dc}
f_{sw}	70 kHz	35 kHz
P_o	2.2 kW	
Power semicond.	35 mΩ 600 V IGOT60R035D1, *Infineon*	
Gate driver	1EDF5673K, *Infineon*	
Filter inductor, L_o	58 µH N87 3x stacked E32x16x9 Litz Wire 630x71 µm, 16 turns	
Filter capacitor, C_o	4.7 µF (film) F861FR475M310ZLH0J	
Flying capacitors	–	4x10 µF (film) C4AEGBU5100A1YJ
Fan	1x ⌀25 mm, 0.6 W	2x ⌀25 mm, 0.6 W
Heatsink	1x (25 × 28 × 42) mm^3	2x (25 × 28 × 42) mm^3
Power density	18.0 kW/dm^3	9.1 kW/dm^3
Peak efficiency	99.2 %	98.8 %

the cost of the unfolder bridge-leg, an electrical conductance related cost can be defined as

$$\sigma_G = \frac{\frac{Cost}{A_{die}}}{\frac{G_{on}}{A_{die}}} = \frac{Cost}{G_{on}} \left[\frac{\$}{m\Omega^{-1}}\right] = Cost \cdot R_{on} \left[\$ \cdot m\Omega\right] , \tag{F.1}$$

where $G_{on} = R_{on}^{-1}$ is the electrical on-state conductance in $[m\Omega^{-1}]$, A_{die} is the die area of a given device, and die area proportional costs are assumed. Taking the aforementioned 34 mΩ (at $T_j = 125\,°C$) Si SJ-devices [191], $\sigma_{G,Si\,SJ} = 439\ \$ \cdot m\Omega$, whereas the 110 mΩ (at $T_j = 125\,°C$) GaN devices [193] feature $\sigma_{G,GaN} = 1694\ \$ \cdot m\Omega$, indicating for the current state-of-the-art a factor ×3.9 cost advantage of the Si SJ-technology (cost data obtained from [192] for a MOQ of 1000 pcs.).

The key measured waveforms are shown in **Fig. F.6**, where the naturally balanced FC [124] in the 3L design and identical output waveforms in each design, ignoring the unipolar current in the 2L design due to the excluded unfolder stage, are highlighted.

The measured efficiency difference between the designs can be compared to that predicted by the simple, intuitive model of **Fig. F.3**, and the predicted loss breakdown for each design is shown in **Fig. F.5b-c**. Total losses of 15.5 W are measured in the 2L design at 2 kW of output power, a deviation of only

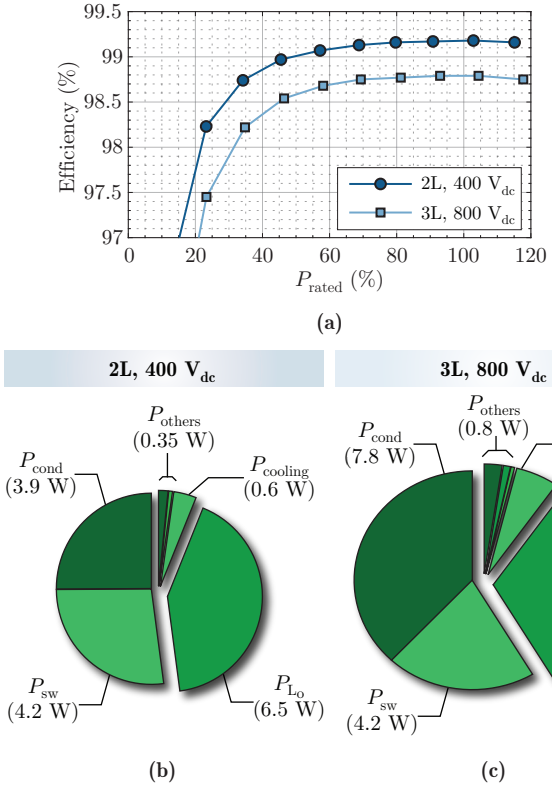

Fig. F.5: **(a)** Measured AC/DC efficiency for the 2L, 400 V_{dc} and 3L, 800 V_{dc} inverters from 20 % – 100 % load. Efficiency measurements include fan and gate drive power and exclude losses in power pulsation buffer capacitors to emphasize the bridge-leg comparison between single- and three-phase systems. Peak efficiency for the 2L, 400 V_{dc} inverter is 99.2 % at 2.25 kW. Peak efficiency for the 3L, 800 V_{dc} inverter is 98.8 % at 2.25 kW. Expected loss breakdown at 90 % load (2 kW) for the **(b)** 2L, 400 V_{dc} inverter (predicted losses: 15.5 W, measured losses: 16.6 W) and the **(c)** 3L, 800 V_{dc} inverter (predicted losses: 20.5 W, measured losses: 24.2 W). P_{others} includes gate driver, output capacitor (C_{o}), and FC losses. P_{cooling} is fan power consumption. The 3L, 800 V_{dc} conduction losses are 2× higher than the 2L conduction losses, and the switching losses are identical.

1.1 W from the predicted losses. In the 3L design, the measured losses (24.2 W)

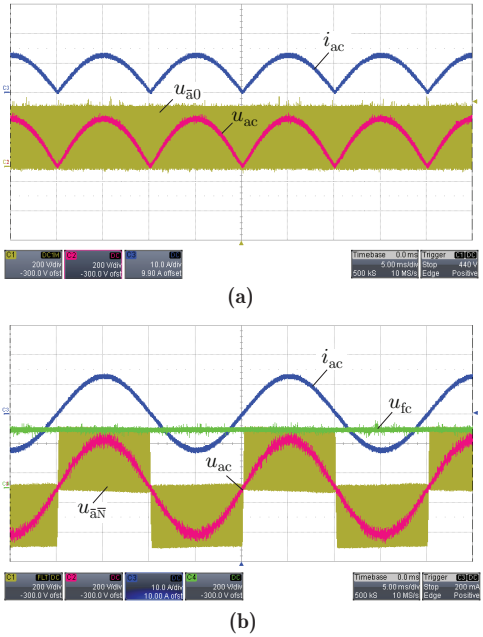

Fig. F.6: **(a)** Key measured waveforms at 90 % load (2 kW) for the 2L, 400 V_{dc} inverter. **(b)** Key measured waveforms at 90 % load (2 kW) for the 3L, 800 V_{dc} inverter. Labels are referenced to **Fig. F.3**. The output waveforms are identical with the exception of an unfolder for the 2L inverter. Without a bipolar output, one switch in the 2L design will hard-switch more often than its bridge-leg counterpart, while in the 3L design, the hard- and soft-switching periods will be symmetric. This asymmetry has a negligible effect on device heating and, therefore, also a negligible effect on measured efficiency.

are 3.7 W higher than the modeled losses, an efficiency error of 0.19 %. These additional losses are partially attributed to the increased parasitic capacitance that arises by having the FCs and the switch pair closest to the switch node $u_{\bar{a}0}$ ($T_{h,2}$, $T_{l,2}$ in **Fig. F.3b**) jumping in potential with respect ground. This parasitic capacitance was measured to be 70 pF, which besides increasing the hard-switching losses, extends the partial (or incomplete) soft-switching regime to higher currents [57], and degrades the efficiency across the line cycle.

This hardware demonstration, at its core, validates the intuition that 3Ls are "not enough" for inverters and rectifiers in three-phase, 800 V_{dc} DC-link

Tab. F.2: Blocking voltage scaling factors for R'_{on} and C'_{Q}. Data obtained from **Figs. 2.3** and **2.6**.

	R'_{on}	C'_{Q}	α_R	α_C
Si	300 mΩ mm^2 @ 200 V	40 pF/mm^2 @ 200 V	2.5	-1.6
SiC	300 mΩ mm^2 @ 900 V	20 pF/mm^2 @ 900 V	1.6	-1.0
GaN	300 mΩ mm^2 @ 650 V	20 pF/mm^2 @ 650 V	1.1	-0.7

applications to match the performance of single-phase bridge-legs in 400 V_{dc} DC-link applications. With a fixed output filter, the 3L bridge-leg efficiency will always be less than the 2L, 400 V_{dc} design due to the increased conduction losses. With the motivating intuition validated, the defining question of this Appendix is: how many levels are enough for an 800 V_{dc} DC-link bridge-leg to recover the efficiency of a 400 V_{dc}, 2L benchmark?

F.3 Determination of the Minimum Number of Levels

In order to determine how many levels are enough (not yet considering power density), the scaling laws presented in **Chapter 2** are revisited. In particular, Eq. **(2.22)** can be rewritten with

$$R'_{on}\left(\frac{U_{dc}}{N}\right) = \frac{R'_{on}(U_{dc})}{N^{\alpha_R}} \tag{F.2}$$

$$C'_{Q}\left(\frac{U_{dc}}{N}\right) = \frac{C'_{Q}(U_{dc})}{N^{\alpha_C}}, \tag{F.3}$$

yielding

$$P_{semi} = \frac{2I_{rms,ac}U_{dc}}{N^{(\alpha_R+\alpha_C)/2}}\sqrt{R'_{on}(U_{dc})C'_{Q}(U_{dc})f_{sw}}\,. \tag{F.4}$$

The condition that only arbitrary semiconductor voltage ratings can be used based on commercially-available devices is applied, allowing a maximum voltage utilization of 2/3. At the time of writing, GaN-on-Si HEMTs are commercially-available at ratings of [100, 120, 150, 200, 600/650, 900] V, where lower-voltage devices that cannot be used at the maximum number of considered levels (10) with an 800 V_{dc} DC-link are ignored. SiC MOSFETs are

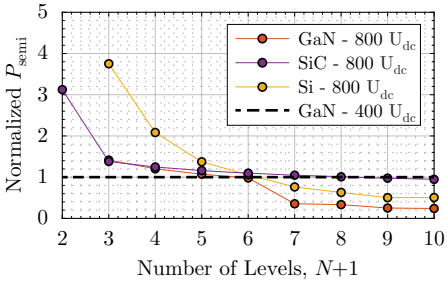

Fig. F.7: Normalized semiconductor power dissipation for chip area-optimized FCC with a given power rating, fixed peak Δi_L and a fixed output filter, using commercially-available device voltage ratings (compared to a 2L, 400 V_{dc} DC-link GaN benchmark). GaN refers to GaN-on-Si HEMTs and Si/SiC refers to Si/SiC MOSFETs, respectively. With commercially-available device voltage ratings, this analysis indicates that, with an 800 V_{dc} DC-link, only a ML converter with more than 6L will approach the semiconductor efficiency of the 2L, 400 V_{dc} DC-link GaN benchmark, which is shown with a dashed line.

not commercially-available below 650 V, and Si MOSFETs are available at a broad range of voltages. Replacing in Eq. **(F.4)** the semiconductor dependent coefficients with the values given in **Table F.2**, the relative semiconductor efficiency with a fixed Δi_L and fixed output filter (cf., **Section 2.5.2**) is obtained and shown in **Fig. F.7**. The results indicate that 6L or 7L are necessary to recover the benchmark 400 V_{dc} efficiency at 800 V_{dc} . The 6L, 800 V_{dc} GaN design has approximately the same modelled semiconductor losses as the benchmark, and once other unavoidable losses are included (e.g., gate driver and FC losses), it is predicted that 7 or more levels will be required to reach the efficiency of the benchmark. At 7L, it can be transitioned from 600 V to 200 V GaN devices, accounting for the dramatic improvement in efficiency when stepping from 6L to 7L. Because SiC MOSFETs are not available at voltage ratings below 650 V, SiC-based bridge-legs do not materially lower their losses with level counts higher than 3. In summary, then, a high level count (much higher than the academia- and industry-standard of 3) is necessary for a three-phase bridge-leg to meet or exceed the efficiency of a single-phase bridge-leg with the same output filter.

With the focus on ultra-high-efficiency, however, thus far the power density improvements for the filter stage with increasing f_{eff} have been ignored, and the optimal f_{sw} to balance efficiency and power density have not been considered. More tangibly, with the 70 kHz operating frequency of the 2L,

400 V_{dc} benchmark, the 7L design with the assumptions of **Fig. F.7** would operate with a switching frequency of only 3.9 kHz, an unrealistically low selection that would sacrifice available gains in power density. At this stage, specificity is introduced to find optimized designs, with the ultimate goal of finding the required number of levels and associated power density sacrifices necessary to recover the efficiency of a 2L, 400 V_{dc} DC-link benchmark for an 800 V_{dc} DC-link.

F.4 Pareto Optimization

A full efficiency vs. power density optimization is required, such that the trade-off between filter size and bridge-leg efficiency with switching frequency is included, where for the 800 V_{dc} DC-link case, 3L and the 7L bridge-legs are chosen for the comparison. In the previous section, the analysis only examines *relative* bridge-leg efficiencies with a fixed output filter; here, the full bridge-leg is optimized, i.e., the semiconductors, the cooling system, the L_oC_o-filter, and the FCs, if applicable, for each evaluated design to find *absolute* power density and inverter efficiency across switching frequency. The electrolytic DC buffer capacitor for power pulsation, any additional EMI filter outside of L_oC_o, and unfolder stages are excluded to equitably compare single- and three-phase systems, aiming for a fundamental understanding of the underlying difference between 400 V_{dc} and 800 V_{dc} DC-link voltage systems. The exclusion of these components is revisited in **Section F.6**, and it is proceeded here with the bridge-leg focus.

The Pareto front is generated for three bridge-leg configurations:

- the 2L, 400 V_{dc} base case
- a 3L, 800 V_{dc} design with identical filter stresses (f_{eff}, Δi_L, and Δu_{ac}) as the 2L, 400 V_{dc} base case, and
- a 7L, 800 V_{dc} design

The selected power rating of the bridge-leg is 2.2 kW, which is similar to the 99.1 % data center power supply presented in [132] and derived from the motivation of this Appendix: to ascertain why single-phase systems with a 400 V_{dc} DC-link voltage in the 2.2 kW – 3.3 kW power range (like [132]) outperform three-phase systems with a 800 V_{dc} DC-link voltage power rating of 6.6 kW – 10 kW like the one presented in **Chapter 4**, even though each of

the three phases processes the same power, AC voltage, and AC current as the single-phase system.

Commercially-available GaN HEMT devices are selected for the semiconductor stage, where voltage ratings are used with a maximum applied voltage of 2/3 of the rating (i.e. 200 V GaN HEMTs may be used up to 133 V). For the 2L 400 V_{dc} and 3L 800 V_{dc} bridge-legs, the 600 V GaN HEMT device suite of *Infineon* [194] are considered for the optimization, and for the 7L 800 V_{dc} bridge-leg, the 200 V EPC 2034C GaN HEMT devices from *EPC Co.* are used. For a comprehensive and accurate Pareto front optimization, switching losses including the $V - I$ overlap [56] improve the accuracy over including only the capacitive switching losses ($Q_{oss}U_{dc}$). For this purpose, calorimetrically-measured switching losses are employed for the Pareto optimization routine. The switching losses for the 600 V, 70 mΩ GaN devices from *Infineon* (IGOT60R070D1) are taken from [78], and the switching losses from [65] for the 200 V, EPC 2047 7 mΩ GaN devices of *EPC Co.* are scaled proportionally by Q_{oss} to model the 200 V, 6 mΩ EPC 2034C GaN devices that are used in this work. To model the dynamic on-state resistance of the GaN devices, data is taken from [80]. Paralleled devices are allowed to support the optimized selection of semiconductor area.

For the cooling system of the 2L, 400 V_{dc} and 3L, 800 V_{dc} designs, an extruded fin-fan heat sink is assumed with a CSPI of 20 W/(K·L) (this value is measured from the hardware demonstrator used for the measurements shown in **Section F.2**) and a temperature difference between heat sink and ambient of 20 °C. With the low losses of the 7L topology and the fact that the losses are distributed among several switches (which additionally reduces the overall junction-to-PCB thermal resistance due to the heat spreading effect [195]), the 7L converter can be designed with natural convection. For example: if 10.9 W of total semiconductor losses (the case for the built hardware in **Fig. F.11b**) are distributed among 24 semiconductor devices with a junction-to-ambient thermal resistance of 45 K/W [196], the temperature rise is only 20.5 °C. Contrarily, natural convection would not be possible for the 2L, 400 V_{dc} and 3L, 800 V_{dc} designs – at a measured 4 W of losses per device (**Fig. F.5b** at 2 kW output power), the measured case temperature with natural convection would exceed 150 °C. The on-state resistance dependence of the semiconductors on the junction temperature is taken into account, and the maximum junction temperature of all semiconductor models is limited to 130 °C. Fan and gate driver power and size are included in the optimization.

To design the output filter, the filter design space [197] is constrained in such a way that the output voltage ripple is guaranteed to be below 1% of the

peak output voltage amplitude that occurs at a modulation index of $M = 0.81$, and the maximum reactive power consumption of the L_o C_o-filter is limited to 3 %. The inductor modelling for L_o follows the guidelines presented in [114]. The considered core material is N87 ferrite featuring E, ELP, and ETD core geometries of different sizes, and the considered wire types are round and litz wires.

The FC dimensioning follows the guidelines presented in [49], where the capacitance value of the FCs is chosen to limit the voltage ripple of the FCs to 5 % of the blocking voltage of each switch (400 V for the 3L case, and 133 V for the 7L case). For the FCs, X6S ceramic capacitors of the C5750X6S series of *TDK* are chosen. Although the Ceralink capacitor family from *TDK* feature lower losses than the selected X6S capacitors [198], these losses are negligible (in the tens of mW) and the X6S capacitors are selected for the 2× increase in capacitance density and 3× decrease in price relative to the Ceralink capacitors.

For C_o, C0G type ceramic capacitors are preferred to the X6S type. Although C0G capacitors feature a lower capacitance density than the X6S type devices, the DC voltage bias has no effect on their capacitance, i.e., they don't have a capacitance derating, and they can safely be assumed to be lossless, which is not the case for X6S capacitors with a large-signal 50 Hz excitation [199–201].

Finally, the volume is calculated as the summed boxed volume of each component with a 30 % overhead for air and PCB height. Each of the considered designs evaluated for a base switching frequency of f_{sw} in the range of 20 kHz – 140 kHz [44, 132] and for an inductor peak-to-peak ripple ratio r in the range of 2 % and 200 %, where $r = \Delta i_{L,pp,max}/I_{ac,pk}$, with $\Delta i_{L,pp,max}$ as the maximum peak-to-peak inductor current ripple.

The Pareto fronts for the evaluated designs are shown in **Fig. F.8**. The trade-off between power density and efficiency for ultra-high-efficiency FCC can now be clearly understood in the full design space, with a few takeaways that merit highlighting:

- Relative to the 2L, 400 V_{dc} DC-link benchmark, a 3L 800 V_{dc} design that sought to maintain the same efficiency (say, 99.1 %) will incur a 7× penalty in power density. Our previous analysis showed that the same efficiency cannot be achieved with a fixed filter, so efficiency can only be held constant through a large reduction in f_{sw} and the filter inductor will grow in size and value accordingly. The 3L design must further add volume for the FCs and the additional switching stage.

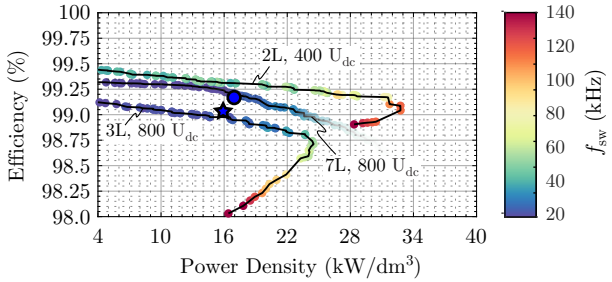

Fig. F.8: Pareto fronts for efficiency vs. power density for 2.2 kW AC/DC inverters with different level counts and input voltages. All fronts are shown for commercially-available GaN HEMTs. Gate driver and fan losses are included, and the volume is calculated as the summed component boxed volume with a 30 % overhead for air and PCB height. Power densities and efficiencies exclude the power pulsation buffer capacitors and unfolder stages for a direct comparison between bridge-legs. The '●' is the selected design for the hardware demonstrator in **Section F.5**, and the '★' indicates measured efficiency and power density. Note, that for higher power densities, either a forced cooling system, or, a certain overhead space that would allow for a sufficient natural convection air flow generation above the switches would have to be considered for the 7L case.

- Relative to the 2L, 400 V_{dc} DC-link benchmark, a 3L 800 V_{dc} design that sought to maintain the same power density (e.g., 12 kW/dm³) will feature around 50 % higher losses. A fixed power density must increase f_{eff} to counterbalance the power density reduction from adding FCs and having to cool more switches, so the real increase in losses with a fixed power density is even larger than the fixed output filter analysis found in the preceding section.

- For an 800 V_{dc} DC-link, 7Ls nearly recover the efficiency of the 400 V_{dc}, 2L benchmark, but with a power density reduction. Our previous analysis only considered efficiency; with power density included, the large volume penalty of the large PCB area determined by the switch cells and the FCs is seen more clearly. In **Section F.5**, this Pareto-optimized 7L design that is predicted to meet the efficiency of the 400 V_{dc}, 2L benchmark is built and characterized.

- 7L inverters achieve a higher overall efficiency and power density than the 3L inverter at the same DC input voltage. The main reason for this is that the 7L bridge-leg does not require active cooling because

of the lower semiconductor losses and larger chip area to spread these losses. Since the 3L design needs active cooling, the power density is also limited by the amount of heat that has to be extracted from the switches – as f_{sw} starts to increase, the decrease in magnetics size outweighs the cooling system size increase, but, at a certain f_{sw}, this balance tips and increasing f_{sw} brings only a small benefit in inductor size but a large penalty in cooling system size due to the increased switching losses.

F.5 Hardware Validation: 7 Levels are (Nearly) Enough

To confirm the Pareto optimization finding that a 7L, 800 V_{dc} DC-link bridge-leg can (nearly) recuperate the efficiency of the 2L, 400 V_{dc} benchmark, a 7L-FCC bridge-leg hardware prototype is constructed (cf., **Fig. F.9**) with the component details in **Table F.3**. The measured 7L characteristic waveforms are shown in **Fig. F.10**, where the ML output waveform is a result of naturally balanced FCs [49, 50, 124].

The design of the hardware follows the switch cell design principle first used in medium voltage drives [186] and then adopted and optimized for lower voltage applications [30, 49, 202], where FC switch cells (cf., **Fig. F.9a-b**) are implemented such that two adjacent switch pairs are housed in each individual cell. To enable high efficiency, each switch utilizes two paralleled

Tab. F.3: Components, key values, and performance metrics for the 7L inverter of **Fig. F.9b-c**. Component labels reference **Fig. F.9a**.

Parameter	**800 V_{dc}, 7L**
U_{dc}	800 V_{dc}
f_{sw}	30 kHz (eff. 180 kHz)
P_o	2.2 kW
Power semicond.	6 mΩ 200 V EPC 2034C, *EPC Co.*
Gate driver	2EDF7275K, *Infineon*
Filter inductor, L_o	28 µH N87 2x stacked ELP 32x6x20 Litz Wire 630x71 µm, 6 turns
Flying capacitors	12.2 µF (C5750X6S2W225K250KA)
Filter capacitor, C_o	2.0 µF (C5750C0G2J104J280KC)
Power density	15.8 kW/dm³
Peak efficiency	99.03 %

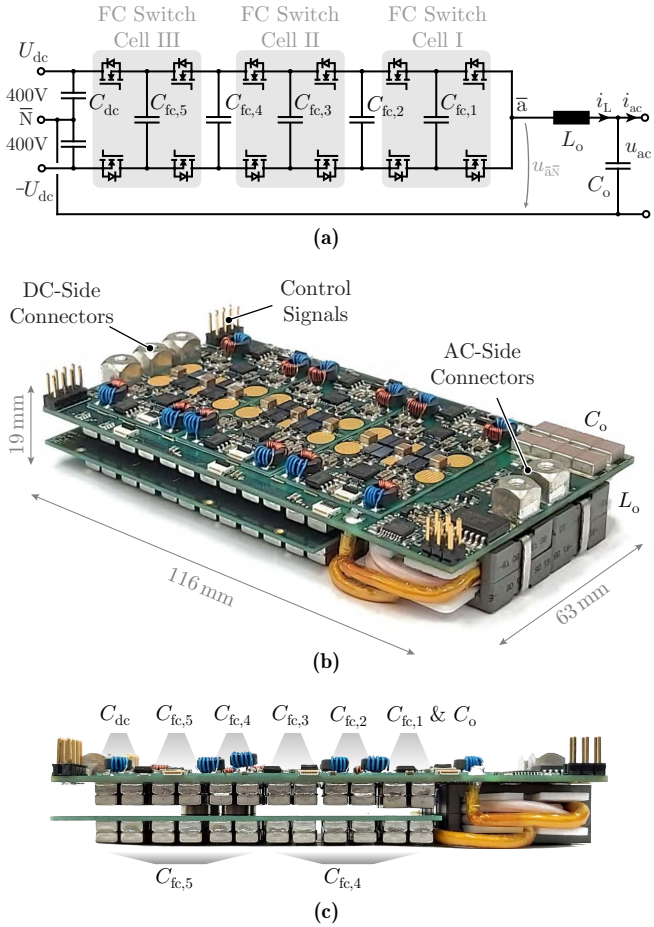

Fig. F.9: **(a)** 7L-FCC bridge-leg circuit schematic. **(b)** Hardware implementation of the 7L-FCC bridge-leg, featuring a boxed volume of 116 mm × 63 mm × 19 mm. **(c)** Side-view of the implemented hardware with a detailed annotation of the capacitor placement.

EPC 2034C GaN devices from *EPC Co.* Because of the high efficiency and the increased switch count and area, a heatsink-less design can be realized that relies solely on passive convective cooling. Each pair of adjacent switches is driven with the 2EDF7275K gate driver from *Infineon.*

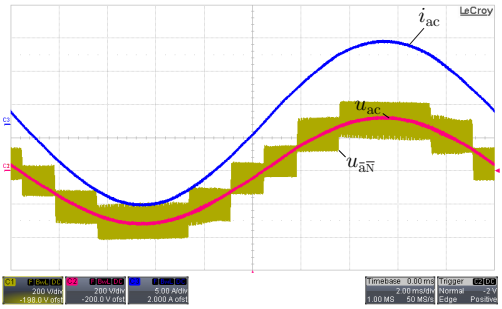

Fig. F.10: Key measured waveforms at 2 kW for the 7L, 800 V_{dc} inverter, where labels are referenced to **Fig. F.9(a)**.

To limit the voltage ripple across each FC to less than 5 % of the blocking voltage of the switches, an *effective* capacitance of 12 µF is required for each FC. These capacitors are implemented with the C5750X6S ceramic capacitor series by *TDK*, which are rated for 450 V and feature a nominal capacitance of 2.2 µF at zero DC bias voltage. Since the capacitance of these X6S capacitors decreases with DC bias voltage – reducing up to 20 % of the nominal capacitance value at 400 V_{dc} for a capacitance of only 0.44 µF – a different number of capacitors has to be placed for each one of the five FCs $C_{fc,i}$. For $C_{fc,4}$ (DC bias: 533 V) and $C_{fc,5}$ (DC bias: 666 V), the situation is aggravated by the 450 V capacitor rating, which requires a series-connection of multiple capacitors and an additional parallel resistive divider to ensure a continuously-balanced voltage across the capacitors [203]. This leads to a large mismatch in the number of capacitors between, for example, $C_{fc,1}$, which requires at least 11 discrete capacitors to achieve 12 µF at 133 V DC bias voltage, and $C_{fc,5}$ which requires at least 99 discrete capacitors to feature 12 µF at 666 V DC bias voltage. The resistive divider is implemented with 1.6 MΩ resistors, leading to total losses of 1.3 W, cf., **Fig. F.11b**. To accommodate all of these capacitors in a power-dense configuration, a second PCB is connected to the main PCB through screw connectors that allow the series and/or parallel connection of additional capacitors, as shown in **Fig. F.9c**.

The efficiency measurements (measured with the *Yokogawa WT3000* precision power analyzer) and calculated loss breakdown are shown in **Fig. F.11**. The efficiency of the 7L, 800 V_{dc} DC-link design is higher than the 3L, 800 V_{dc} DC-link design and reaches the efficiency of the 2L, 400 V_{dc} baseline case, particularly near around 40 % of rated load. The flattening of the efficiency curve

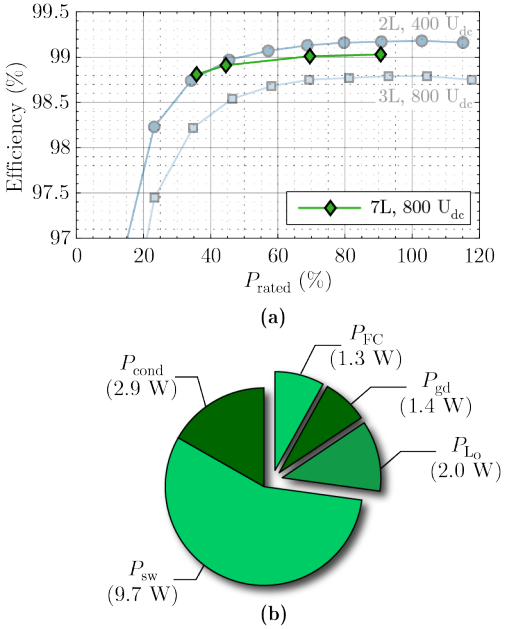

Fig. F.11: (a) Measured AC/DC efficiency for the 7L, 800 V_{dc} inverter. Efficiency measurements include gate drive power and exclude losses in power pulsation buffer capacitors. Peak efficiency for the inverter is 99.03 %. **(b)** Expected loss breakdown at 2.0 kW (predicted losses: 17.3 W, measured losses: 19.4 W).

of the 7L prototype for higher loads can be attributed to two reasons: firstly, since the semiconductor losses increase at higher load (higher conduction and switching losses), the junction temperature increases more relative to the 2L and 3L designs that feature forced-air cooling, and conduction losses further increase due to the positive temperature coefficient of the GaN on-state resistance. Secondly, in order to limit the switching transient overshoot across the semiconductors to ≈ 10 % (150 V maximum at a nominal switched voltage of 133 V), the gate resistance is increased to 30 Ω per device. Unless the power stage design is further optimized (as in [17], where power semiconductors are soldered on both sides of the PCB to reduce the commutation loop inductance and therefore the transient overshoot, the only way of reducing these overvoltages is to increase the turn-on gate resistance to slow the switching transient speed). The slow transition, though, increases switching losses

(more tangibly, [17] shows that increasing the gate resistance from 10 Ω to 30 Ω for the EPC2034 devices more than halves the du/dt of the switch transition). In sum, 99.03 % peak efficiency is measured in the hardware prototype, close to the predicted 99.15 % peak efficiency of the Pareto-optimized design and with the degradation explained by the two drivers above (with some additional contributions from unmodelled losses, e.g., conduction losses in PCB traces and additional parasitic capacitance at the switch nodes).

Despite this flat efficiency curve, the 7L, 800 V_{dc} DC-link inverter matches the efficiency of the 2L, 400 V_{dc} baseline. Increasing the number of levels of a bridge-leg enables higher efficiency, recovering the loss penalty associated with increasing the DC-link voltage from 400 V_{dc} to 800 V_{dc} for the same AC output voltage. Confirming the analysis, it is shown that a minimum of 7Ls is required for a three-phase bridge-leg to meet the efficiency of a single-phase bridge-leg, which benefits immensely from an unfolder (see **Fig. F.1b**). In the final section of this Appendix, the ramifications of this crucial finding on three-phase grid and motor drive applications are discussed, and different system architectures that can halve the DC-link voltage, enabling higher efficiency, are proposed.

F.6 Summary and Discussion

Through the scaling laws and hardware demonstrations in this Appendix, it is shown that 3Ls are indeed "not enough" for high-efficiency AC/DC and DC/AC converters in three-phase applications featuring an 800 V_{dc} DC-link voltage to recover the performance of a single-phase converter that, thanks to an unfolder bridge-leg, can feature a 400 V_{dc} DC-link voltage to generate the same 230 V_{rms} to 240 V_{rms} AC voltage. Our hardware demonstrators validate this prediction, with the 800 V_{dc} DC-link, 3L FCC inverter featuring 50 % higher measured losses and 2× lower power density than the 400 V_{dc} DC-link, 2L design. With idealized power semiconductors and with currently-available device voltage ratings, a minimum of 6Ls is required to recover the efficiency of a 2L, single-phase design at the 800 V_{dc} DC-links required for three-phase conversion. With a complete Pareto optimization, it is found that a 7L, 800 V_{dc} DC-link inverter will nearly reach the efficiency of the 400 V_{dc} DC-link, 2L benchmark at full load, and this theory is validated with a 7L, 2.2 kW hardware prototype with a power density of 15.8 kW/dm^3 and a peak efficiency of 99.03 % that reaches the same partial load efficiency as the 2L, 400 V_{dc} benchmark, however, at a slightly lower power density.

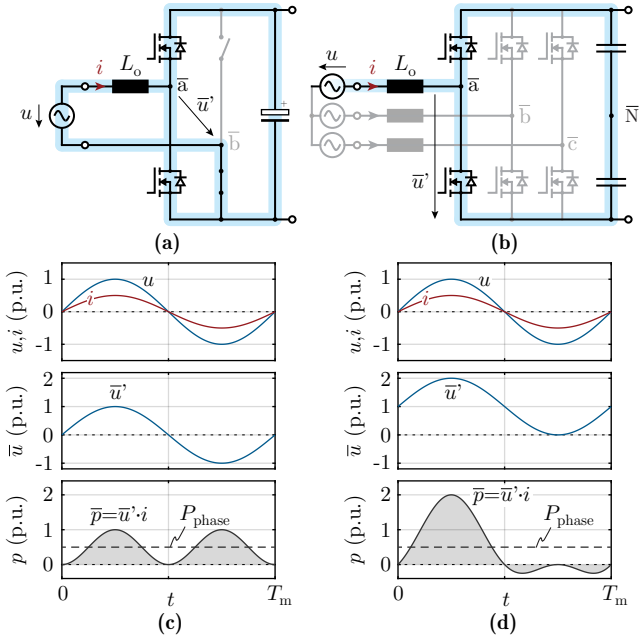

Fig. F.12: Instantaneous power flow considerations for a **(a)** single-phase 2L PFC rectifier, with the conduction path highlighted for $u > 0$ (the return path of the current via the unfolder bridge-leg, which is typically implemented with Si SJ-MOSFETs is only conceptually indicated), and a **(b)** three-phase 2L PFC rectifier, with the conduction path of one of the three high-frequency bridge-legs highlighted (phase current returns through the other two phases). **(c-d)** Typical input phase voltage, current and power waveforms for a single mains period (T_m) shown per unit (p.u.), for the converters in **(a-b)**, respectively. For the same input voltage u and global average phase power P_phase, the power $\overline{p}$ processed by a bridge-leg of the three-phase system shows twice the maximum instantaneous peak power value of the single-phase system and even includes intervals of (slightly) negative instantaneous power.

The increase in DC-link voltage between single-phase and three-phase systems can be fundamentally attributed to the unavailability of a line-frequency unfolder in three-phase systems. In single-phase systems, these unfolders essentially double the AC voltage generation capability without increasing voltage stresses or power semiconductor losses [60], allowing the use of low-voltage semiconductors at low overall complexity. The fundamental advantage of a line-frequency unfolder is also immediately understandable by

comparing the instantaneous power flow $\overline{p}$ (averaged over a switching cycle) which is processed by a bridge-leg for a single-phase and a three-phase PFC rectifier system (cf., **Figs. F.12a-b**). Characteristic waveforms for same global (related to a mains period) average power P_{phase} are depicted in **Figs. F.12c-d**. The three-phase system shows a heavily uneven distribution of $\overline{p}$ over the mains period which reaches twice the maximum value of the single-phase converter. Moreover, for the three-phase system in **Fig. F.12b**, the processed power is (slightly) negative for negative phase voltages $u < 0$, i.e., the DC-link is instantaneously sourcing power back to the grid for the considered phase (although the sum of the instantaneous powers of the three individual phases for a balanced three-phase system is constant at any point in time) [204], an issue which is also known from single-phase class-D amplifier circuits that feature a half-bridge instead of a full-bridge power circuit structure [205].

It follows directly, then, that three-phase applications should seek to, where possible, replicate the reduced-voltage benefit of single-phase designs, and two use cases that may accomplish this goal are briefly discussed. These two sample cases that are identified utilize the same unfolder concept used in single-phase systems and extend it to systems which require a three-phase solution, thereby halving the DC-link voltage requirement and leading to a performance increase of the three-phase semiconductor stage.

Three-phase grid-connected converters

Three-phase grid-connected converters often include an isolated DC/DC stage for safety and/or large voltage ratio conversion, as shown in **Fig. F.13a**. The AC/DC conversion stage can be implemented as a monolithic three-phase converter (like the one shown in **Fig. F.1b**), where the DC-link capacitor is small due to the constant three-phase power (cf., **Fig. F.2b**) but the DC-link voltage must be high, with the associated penalties that are detailed in this Appendix. In this application, unfolder-like three-phase techniques that can reduce the semiconductor blocking voltage requirements are especially valuable, including input voltage selectors [9, 206] or novel modulation schemes [134, 141, 142]. Alternatively, the single-phase bridge-leg benefits can be recovered by adopting a phase-modular approach (**Fig. F.13b**), where each of the three phases has a separate, isolated powertrain connected in parallel at the DC output [150, 207]. The DC-link capacitance requirement of the AC/DC stage is increased substantially, as each phase block must include power pulsation energy storage, but each AC/DC stage can be implemented with the low complexity and ultra-high-efficiency 2L configuration of **Fig. F.1a**. In

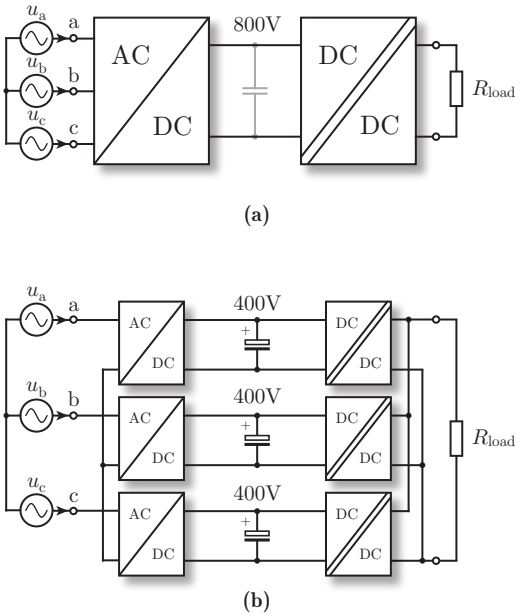

Fig. F.13: Three-phase grid-connected converter block diagrams with an isolated DC/DC stage to provide galvanic isolation for safety and/or large voltage conversion ratios. **(a)** Monolithic three-phase conversion stage, with a single three-phase converter and isolated DC/DC converter. In this case, the AC/DC bridge-legs must be rated for the full 800 V_{dc} DC-link (cf., **Fig. F.2b**) but the output power is constant, reducing the DC-link capacitor size. The AC/DC converter may include an unfolder-like structure for three-phase capabilities, such as an input voltage selector [9, 206]. **(b)** Phase-modular three-phase system, where each phase has a single-phase AC/DC stage (cf., **Fig. F.1a**) and an isolated DC/DC converter [150]. In this architecture, the AC/DC bridge-legs can operate with low complexity and ultra-high-efficiency due to the low DC-link voltage, but the DC-link capacitor must be sized for power pulsation buffering (cf., **Fig. F.1b**).

this configuration, the summation of the phase power (shown in **Fig. F.2b**) is performed by the parallel electric connection at the combined DC-link. High-efficiency monolithic (**Fig. F.13a**) configurations (e.g., used for 10 kW EV chargers) typically feature a 3L (for example, a Vienna configuration) rectifier, where a midpoint DC-link connection is used to series-connect two DC/DC modules [133] (also, see **Chapter 5**). This enables the use of

600/650 V-rated semiconductors in the DC/DC stage of the monolithic approach, where each DC/DC module processes half of the input power (5 kW). Similarly, the DC/DC stage of the phase-modular (**Fig. F.13b**) approach can be realized with 600/650 V-rated semiconductors, given the reduction to a 400 V_{dc} DC-link, and requires the power rating of each module to be 3.3 kW, or one-third of the rated power. Hence, assuming the DC/DC modules for both the monolithic and phase-modular approaches can be realized with similar efficiencies (the only difference being a minor difference in power rating), one can safely conclude that the main efficiency difference lies in the front-end AC/DC stage.

Three-phase motor drive systems

As seen in (**Fig. F.14a**), three-phase motor drives require a higher DC-link voltage than a "phase-modular" counterpart (**Fig. F.14b**). If the virtual star-point formed at the capacitor connection is not connected to the DC-link midpoint, as shown in **Fig. F.14a**, discontinuous PWM schemes could improve semiconductor losses and change the optimal area [208]; however, these considerations are kept outside the scope of this work to maintain the focus on the bridge-leg comparison. The advantages of moving to a single-phase architecture, then, can be realized with an open-winding configuration, with an unfolder for each stage placed at the winding terminal opposite the high-frequency bridge [156, 209, 210]. In motor drives, the summation of the individual phase powers is performed in the rotor, and the DC-link capacitor does not need to provide power pulsation capability. In this case, the only penalty for the higher-efficiency bridge-leg is the addition of three motor terminals, but with the accelerating adoption of integrated motor drives, these additional connections will decrease in importance.

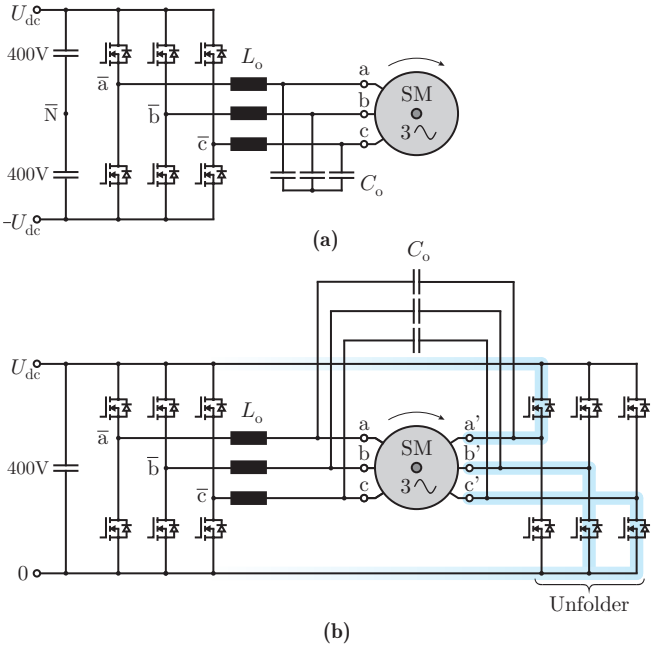

Fig. F.14: Three-phase motor drive inverter systems. **(a)** Conventional three-phase motor drive system, where the motor windings are terminated in a star or delta configuration. The three-phase drive must operate with a high DC-link voltage because the winding terminations cannot be individually accessed, decreasing the bridge-leg efficiency. **(b)** Open-winding motor configuration, with both terminals on the individual windings accessible. The individual unfolder stages (highlighted) reduce the required DC-link voltage by a factor of ≈ 2 (as shown in **Figs. F.1** and **F.2**), improving the efficiency of the bridge-legs [156, 209, 210].

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