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Conceptualization and Multi-Objective Analysis of Multi-Cell Solid-State Transformers

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For my parents,
Susanne and Edy

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Abstract

Increasing the share of renewable energy sources in the total energy production as well as improving the energy efficiency in general are important goals ranking high on political agendas, and are aiming at a reduction of greenhouse gas emissions and a sustainable usage of limited resources. Solid-state transformers (SSTs), which are galvanically isolated power electronic conversion interfaces between a medium-voltage (MV) system and a low-voltage (LV) system, whereby the isolation transformer is operated in the medium-frequency (MF) range, can contribute to achieving these goals in two different ways: SSTs are envisioned for replacing conventional low-frequency (LF) transformers (LFTs) in applications such as traction, where weight and volume savings as well as efficiency improvements can be achieved, or, utilizing the controllability inherent to power electronic systems, in smart distribution grids in order to address, e. g., the challenges arising from an increased amount of renewable energy sources connected at lower voltage levels.

There are five main classes of modern SST topologies: matrix-type AC-AC topologies, isolated back end (IBE) topologies, isolated front end (IFE) topologies, topologies based on the modular multilevel converter (M2LC), and single-cell topologies based on novel silicon carbide (SiC) power devices with very high blocking voltages. However, because of the limited blocking voltage capability of readily available power semiconductors, typically multi-cell converter structures are employed to cope with high voltages.

Therefore, considering the cascaded AC-DC input stage of a typical multi-cell IBE SST, i. e., a generic cascaded H-bridge converter structure, a comprehensive analysis and a multi-objective optimization of the optimum number of cascaded converter cells (or equivalently, the optimum blocking voltage of the employed silicon (Si) power semiconductors) is provided, which is based on physics-inspired, empirical models of the dependencies of Si power semiconductors' loss-relevant parameters on the rated blocking voltage and current. For a 1 MVA system connected to the 10 kV grid, designs based on 1200 V or 1700 V devices (corresponding to 15 or 11 cascaded full-bridge cells per phase stack, respectively) are identified as providing the most suitable trade-offs between efficiency (above 99 %) and power density (about 5 $\mathrm{kW/dm^3}$). Significant efficiency and power density gains can be realized by replacing Si IGBTs with LV SiC devices in multi-cell systems, whereas single-cell designs based on high-voltage SiC devices suffer from the high dv/dt and di/dt values required to limit switching losses.

Furthermore, the reliability of multi-cell SST systems is analyzed, and it is shown that cell redundancy, which is facilitated by the modular nature of

multi-cell systems, is a mighty concept to improve reliability. Considering similar costs of the redundancy, the reliability of designs based on many converter cells can be comparable to that of designs using only few cascaded cells (based on devices with higher blocking voltages).

In such cascaded cells topologies, the cells' DC buses (or, in case of IFE topologies, |AC| buses) on floating potentials are connected to a common LV DC bus (or LV |AC| bus) by means of isolated DC-DC (or |AC|-|AC|) converters featuring an MF transformer (MFT), thereby forming an input-series output-parallel (ISOP) arrangement. The series resonant converter (SRC) operated in the half-cycle discontinuous conduction mode (HC-DCM) is a very suitable realization option for these conversion stages, because it provides a fixed voltage transfer ratio in open-loop operation. Therefore, this thesis provides a comprehensive analysis of the HC-DCM SRC. First, a dynamic equivalent model for the terminal behavior of the converter is generically derived, and then experimentally verified for the special case of small (with respect to the series resonant capacitor) DC link capacitors. Considering a 1 MVA example IBE SST system interfacing a 10 kV MV grid to a 800 V DC bus (and optionally to the 400 V LV AC grid), this model facilitates an optimized choice of the cascaded converter cells' DC capacitors with respect to minimum volume and losses. Furthermore, an experimentally verified model of the switching losses occurring in Si IGBTs under zero-current switching (ZCS) and/or zero-voltage switching (ZVS) conditions found in this type of converter enables an efficiency versus power density $\eta\rho$-Pareto optimization of the example SST's converter cells' 52.5 kW isolation stages that connect a 2.2 kV DC to a 800 V DC bus. The results indicate that an efficiency above 99 % can be achieved with high power densities of more than $4\,\mathrm{kW/dm^3}$ and comparatively low switching frequencies in the range of 7 kHz…9 kHz.

The switching actions of the cascaded cells' AC-DC input stages in such multi-cell IBE SSTs causes the other cells in the stack to change their potential with respect to ground at high dv/dt values, giving rise to significant common-mode ground currents. A comprehensive analytic model describing this phenomenon is derived. This facilitates the evaluation of different mitigation strategies, whereby the placement of common-mode chokes at each cells' AC terminals is found to be an effective solution.

In contrast to the IBE approach, the IFE approach has not received much attention in literature so far. Therefore, a detailed derivation and analysis of this concept is provided using the example of a 25 kW single-phase all-SiC SST system acting as an interface between a 6.6 kV MV grid and a 400 V LV DC bus, e. g., in auxiliary power supply applications in volume and/or weight

restricted environments. In an IFE SST, an ISOP configuration of HC-DCM SRC isolation stages (operating as |AC|-|AC| converters) is used to directly interface the MV AC grid, whereas the shaping of the grid current (to achieve unity power factor) and the regulation of the output DC voltage is carried out by a non-isolated |AC|-DC boost converter stage on the LV side. This reduces the complexity of the system, especially on the MV side (no measurements required, only small resonant capacitors on floating potential).

Whereas the magnetizing current of the MFT can be used to realize ZVS independent of the load in case the HC-DCM SRC is operated between two DC sources, i. e., as a DC-DC converter in an IBE system, this is more complicated in an IFE system, where the converter operates as |AC|-|AC| converter, because the available magnetizing current as well as the voltage to be switched and hence the non-linear parasitic capacitances of the power semiconductors vary over the grid period. A detailed analysis of the ZVS behavior under these conditions is given, and it is shown how an optimized combination of a magnetizing inductance and an interlock time can be chosen such as to either achieve lowest losses or a wide ZVS range over the grid period in order to reduce electromagnetic interference (EMI) generated by (partially) hard-switched transitions. In order to realize both of these desirable characteristics simultaneously, it is proposed to vary the interlock time over the grid period. The considerations include component tolerances among the converter cells' resonant tanks, and are verified using a detailed simulation model that includes non-linear MOSFET capacitances.

Eventually, a generic comparison based on analytic expressions for the main component stresses of the IFE and the IBE concept reveals that for the same specifications, the IFE approach requires fewer cascaded cells and less individual switches, but a larger total SiC chip area. The overall volume (and hence material consumption) of the transformers is similar. The generic comparative evaluation is complemented by a case study considering the aforementioned ratings, which indicates that the IFE approach shows a lower full-load efficiency but a higher part-load efficiency due to lower switching and transformer core losses. Furthermore, the IFE approach does not suffer from the common-mode ground current issues discussed above, because the floating parts of the cascaded cells change their potential with respect to ground only comparatively slowly.

Finally, the applicability of SST technology in different application areas is evaluated. Regarding a quantitative study comparing the aforementioned 1 MVA IBE-based AC-AC SST with an equally rated conventional LF distribution transformer, which revelas higher losses and significantly higher costs of

the SST solution, and regarding also the availability of alternative technologies to provide required controllability to the distribution grid, e. g., by means of complementing LFTs by robust, mechanical on-load tap-changers, the feasibility of SST applications in the AC distribution grid seems questionable. However, it is also found that AC-DC applications, e. g., the application of an SST as interface between the distribution grid and a local DC microgrid, might be more attractive. In pure DC-DC applications, e. g., in future DC collecting grids for large PV power plants or wind farms, there is no alternative to SST technology in case galvanic separation and/or high voltage transfer ratios are required. The highest potential for SSTs is identified in environments where space and/or weight is limited, such as in traction vehicles, future ships with on-board MV AC or MV DC distribution grids, subsea applications, or even future all-electric aircraft, because there the main benefit of SST technology—higher gravimetric and volumetric power densities, and, compared with an LFT designed to be small and light (which implies higher utilization of the active materials and hence increased losses) also a higher efficiency, are truly unique.

Kurzfassung

Sowohl eine Erhöhung des Anteils der erneuerbaren Energiequellen an der gesamten Energieproduktion als auch allgemein Verbesserungen bei der Energieeffizienz sind wichtige Ziele, die weit oben auf vielen politischen Agenden stehen, und die auf eine Reduktion der Treibhausgasemissionen und auf eine nachhaltige Nutzung beschränkter Ressourcen abzielen. Solid-State-Transformatoren (SSTs) sind galvanisch isolierte leistungselektronische Konversionseinheiten zwischen einem Mittelspannungs- und einem Niederspannungssystem, wobei der eigentliche Isolationstransformator bei Mittelfrequenz (MF) betrieben wird, und können auf zwei Arten zu diesen Zielen beitragen: SSTs werden als möglicher Ersatz für Niederfrequenztransformatoren gesehen, beispielsweise in Traktionsanwendungen, wo Gewichts- und Volumeneinsparungen und auch eine verbesserte Effizienz erreicht werden können, oder, unter Verwendung der inhärenten Regelbarkeit von leistungselektronischen Systemen, auch in smarten Verteilnetzen, zum Beispiel um die sich aus dem vermehrten Anschluss von eneuerbaren Energiequellen an niederen Spannungsebenen ergebenden Herausforderungen zu meistern.

Es gibt fünf Hauptklassen von modernen SST-Topologien: Auf dem Matrixkonverter basierende AC-AC-Topologien, Topologien mit Isolations-Backend (isolated back end, IBE), Topologien mit Isolations-Frontend (isolated front end, IFE), auf dem Modularen Multilevelkonverter (M2LC) basierende Topologien, und Einzellen-Topologien, die durch neue Siliziumkarbid-Halbleiter (silicon carbide, SiC) mit sehr hohen Sperrspannungen ermöglicht werden. Trotzdem werden aufgrund der limitierten Sperrspannungen von gut verfügbaren Leistungshalbleitern typischerweise Konverterstrukturen mit mehreren Zellen eingesetzt, um hohe Spannungen beherrschen zu können.

Deshalb wird in dieser Arbeit unter Betrachtung der kaskadierten AC-DC Eingangsstufe eines typischen Multizellen-IBE-SSTs, also einem generischen kaskadierten H-Brücken-Wechselrichter, eine umfassende Analyse und Mehrkriterienoptimierung der Anzahl kaskadierter Konverterzellen (oder äquivalent dazu der Sperrspannung der eingesetzten Siliziumhalbleiter) durchgeführt, basierend auf von der Physik inspirierten empirischen Modellen für die Abhängigkeiten der verlustrelevanten Parameter von Siliziumleistungshalbleitern von Nennsperrspannung und Nennstrom. Für ein an das 10 kV-Netz angeschlossenes 1 MVA-System bieten Lösungen, die auf 1200 V- oder 1700 V-Halbleitern basieren (oder entsprechend 15 beziehungsweise 11 kaskadierten Vollbrückenzellen pro Phasenstack) gute Kompromisse zwischen Effizienz (über 99 %) und Leistungsdichte (ca. 5 $\mathrm{kW/dm^3}$). Wenn die Silizium-IGBTs in solchen Multizellensystemen durch Niederspannungs-SiC-

Halbleiter ersetzt werden, können signifikante Verbesserungen der Effizienz und der Leistungsdichte erzielt werden, wohingegen Einzellendesigns, die auf Hochspannungs-SiC-Halbleitern basieren, ungünstig hohe dv/dt- und di/dt-Werte aufweisen müssten, um die Schaltverluste in Grenzen zu halten.

Des Weiteren wird die Zuverlässigkeit von Multizellen-SST-Systemen analysiert, wobei gezeigt wird, dass Zellen-Redundanz, welche durch die Modularität von Multizellensystemen einfach realisierbar ist, ein mächtiges Konzept zur Verbesserung der Zuverlässigkeit darstellt. Werden ähnliche Kosten für die Redundanz zu Grunde gelegt, so kann die Zuverlässigkeit von Designs, die auf vielen Konverterzellen basieren, vergleichbar mit jener von Designs sein, die nur wenige kaskadierte Zellen (und dementsprechend Leistungshalbleiter mit höheren Sperrspannungen) verwenden.

In solchen Multizellentopologien liegen die Gleichspannungszwischenkreise (oder, im Falle von IFE-Topologien, die |AC|-Zwischenkreise) der einzelnen Zellen auf massefreien Potentialen und sind via isolierter DC-DC-Konverter, die jeweils einen Mittelfrequenztransformator enthalten, mit einem gemeinsamen DC-Zwischenkreis (oder einem |AC|-Zwischenkreis) auf der Niederspannungsseite verbunden, d. h., die Zellen sind auf der Eingangsseite in Serie und auf der Ausgangsseite parallel verschaltet (input-series, output-parallel, ISOP). Der Serieresonanzkonverter (series resonant converter, SRC), der in einem Modus mit diskontinuierlichem Strom in jeder Halbperiode (half-cycle discontinous-conduction-mode, HC-DCM) betrieben wird, ist eine äusserst geeignete Realisierungsvariante für diese Konversionsstufen, weil er ein fixes Spannungsübersetzungsverhältnis aufweist, ohne dass dafür eine Regelung notwendig ist. Deshalb beinhaltet die vorliegende Arbeit eine umfassende Analyse des HC-DCM SRCs. Zuerst wird ein dynamisches Modell für das Klemmenverhalten des Konverters auf generische Art und Weise hergeleitet und danach für den Spezialfall von bezüglich des Serienresonanzkondensators verhältnismässig kleinen Zwischenkreiskondensatoren experimentell verifiziert. Dieses dynamische Modell ermöglicht eine im Hinblick auf minimales Volumen und minimale Verluste optimale Wahl der Gleichspannungszwischenkreiskondensatoren der kaskadierten Konverterzellen in einem beispielhaft betrachteten 1 MVA-IBE-SST, der als Schnittstelle zwischen einem 10 kV-Wechselspannungsnetz und einen 800 V-Gleichspannungszwischenkreis (und optional einem 400 V-Wechselspannungsnetz) arbeitet. Ausserdem wird ein zunächst experimentell verifiziertes Modell für die Schaltverluste, die in Silizium-IGBTs unter den im HC-DCM SRC vorliegenden Bedingungen für stromloses bzw. spannungsloses Schalten (zero-current switching, ZCS; zero-voltage switching, ZVS), entste-

hen dazu verwendet, eine Effizienz und Leistungsdichte berücksichtigende Pareto-Optimierung der 52.5 kW-Isolationsstufen durchzuführen, welche in den kaskadierten Zellen des oben erwähnten Beispiel-SSTs zwischen einem 2.2 kV-Gleichspannungszwischenkreis und einem 800 V-Gleichspannungszwischenkreis betrieben werden. Die Resultate zeigen, dass Effizienzen über 99 % bei hohen Leistungsdichten von mehr als 4 kW/dm^3 und verhältnismässig tiefen Schaltfrequenzen im Bereich von 7 kHz…9 kHz erreicht werden können.

Die Schalthandlungen der AC-DC Eingangsstufen der kaskadierten Zellen in solchen Multizellen-IBE-SSTs führen dazu, dass die anderen Zellen im Phasenstack ihr Potential in Bezug zur Erde mit hohen dv/dt-Werten ändern, was wiederum zu signifikanten Gleichtakterdströmen führt. Es wird ein umfassendes analytisches Modell zur Beschreibung dieses Phänomens hergeleitet. Dies erlaubt dann die Evaluation von verschiedenen Unterdrückungsmassnahmen, wobei die Anordnung von Gleitaktdrosseln an den AC-Anschlüssen der einzelnen Zellen als effektive Lösung identifiziert wird.

Im Gegensatz zum IBE-Ansatz hat das IFE-Konzept bis jetzt nicht viel Aufmerksamkeit in der Literatur erfahren. Deshalb umfasst diese Arbeit eine detaillierte Herleitung und Analyse dieses Konzepts am Beispiel eines einphasigen, komplett auf SiC-Halbleitern basierenden 25 kW-SST-Systems, das als Schnittstelle zwischen einem 6.6 kV-Mittelspannungsnetz und einem Niederspannungsanschluss mit 400 V Gleichspannung eingesetzt werden kann; zum Beispiel als Hilfsstromversorgung in Applikationsumgebungen mit Volumen- und/oder Gewichtsbeschränkungen. In einem IFE-SST wird eine ISOP-Konfiguration von als HC-DCM SRC ausgeführten Isolationsstufen, die als |AC|-|AC|-Konverter arbeiten, direkt ans Mittelspannungsnetz angeschlossen, wohingegen die Formung des Netzstromes (um einen Leistungsfaktor nahe eins zu erreichen) sowie die Regelung der Ausgangsgleichspannung mittels eines nichtisolierten |AC|-DC Hochsetzstellers auf der Niederspannungsseite erreicht wird. Dies reduziert die Komplexität des Systems, insbesondere auf der Mittelspannungsseite (keine Messungen, nur kleine Resonanzkondensatoren auf massefreien Potentialen).

Wird der HC-DCM SRC zwischen zwei Gleichspannungsquellen betrieben, zum Beispiel als DC-DC-Konverter in einem IBE-SST, kann der Magnetisierungsstrom des Mittelfrequenztransformators dazu verwendet werden, unabhängig von der Last spannungsloses Schalten der Leistungshalbleiter zu erreichen. Dies ist jedoch komplizierter beim Betrieb als |AC|-|AC|-Konverter in einem IFE-System, weil dann der für das stromlose Schalten zur Verfügung stehende Magnetisierungsstrom und auch die zu schaltende Spannung

und damit die nichtlinearen parasitären Kapazitäten der Leistungshalbleiter über die Netzperiode variieren. Es wird eine detaillierte Analyse des spannungslosen Schaltens unter diesen Bedingungen präsentiert, und es wird gezeigt, wie eine optimierte Kombination einer Magnetisierungsinduktivität und einer Totzeit beim Schalten der Brückenzweige gewählt werden kann, sodass entweder minimale Verluste oder aber spannungsloses Schalten in einem möglichst grossen Bereich der Netzperiode, um elektromagnetische Interferenzen, die beim (partiellen) harten Schalten entstehen können zu vermindern, erreicht werden. Es wird vorgeschlagen, die Totzeit über die Netzperiode zu variieren, um vorteilhaft beide Charakteristiken gleichzeitig zu realisieren. Die durchgeführten Betrachtungen berücksichtigen Toleranzen der Elemente der Resonanzkreise in den einzelnen kaskadierten Zellen, und werden dann anhand eines detaillierten Simulationsmodells, das auch die nichtlineare Kapazitäten der SiC-MOSFETs enthält, verifiziert.

Schliesslich zeigt ein generischer Vergleich zwischen dem IBE- und dem IFE-Konezpt auf Basis von analytischen Ausdrücken für die Belastungen der Hauptkomponenten, dass bei gleichen Spezifikationen der IFE-Ansatz weniger kaskadierte Zellen und weniger individuelle Schalter, aber eine grössere totale SiC-Chipfläche benötigt. Das Gesamtvolumen (und damit auch der Materialaufwand) für die Transformatoren ist für beide Konzepte vergleichbar. Die generische komparative Evaluation wird mit einer Fallstudie ergänzt, welche die oben erwähnten Spezifikationen berücksichtigt. Es zeigt sich, dass der IFE-Ansatz eine tiefere Volllasteffizienz, dafür aber aufgrund von tieferen Schalt- und Transformatorkernverlusten eine höhere Teillasteffizienz aufweist. Ausserdem treten die oben beschriebenen Probleme mit Gleichtakterdströmen beim IFE-System nicht auf, da die massefreien Teile der kaskadierten Zellen ihre Potentiale gegenüber Erde nur langsam ändern.

Schlussendlich wird die Anwendbarkeit der SST-Technologie in verschiedenen Szenarien evaluiert. Ein quantitativer Vergleich zwischen dem oben erwähnten AC-AC 1 MVA-IBE-SST und einem konventionellen Verteiltransformator gleicher Leistung ergibt höhere Verluste und signifikant höhere Kosten für die SST-Lösung. Dies, und auch die Verfügbarkeit von alternativer Technologie zur Bereitstellung von tatsächlich benötigter Regelbarkeit im Verteilnetz, zum Beispiel regelbarer Ortsnetztransformatoren mit robusten, mechanischen Laststufenschaltern, machen die Sinnhaftigkeit eines Einsatzes von SSTs im Verteilnetz zumindest fraglich. Andererseits zeigt die Analyse, dass AC-DC-Anwendungen, zum Beispiel als Schnittstelle zwischen einem Verteilnetz und einem lokalen Gleichspannungs-Microgrid, attraktiv sein könnten. In reinen DC-DC-Anwendungen, zum Beispiel in zukünftigen Gleichspannungs-

Sammelnetzen in grossen Photovoltaik- oder Windkraftwerken, gibt es keine Alternative zur SST-Technologie, wenn Isolation und/oder hohe Spannungsübersetzungsverhältnise benötigt werden. Das grösste Potential für SSTs wird für Anwendungen in Umgebungen mit Platz- und/oder Gewichtsbeschränkungen identifiziert, wie zum Beispiel in Schienenfahrzeugen, zukünftigen Schiffen mit Mittelspannungsbordnetzen (AC oder DC), Unterwasseranwendungen, oder sogar zukünftigen vollelektrischen Flugzeugen, weil dort die SST-Technologie aufgrund der höheren gravimetrischen und volumetrischen Leistungsdichte, und der im Vergleich zu einem auf kleine Baugrösse und geringes Gewicht optimierten Niederfrequenztransformator (der aufgrund der dazu notwendigen höheren Ausnutzung der aktiven Materialien relativ hohe Verluste aufweist) höheren Effizienz tatsächlich einzigartig ist.

Abbreviations

AC	Alternating Current
ARU	Active Rectification Unit
*a*IFE	Autonomous Isolation Front End
CSPI	Cooling System Performance Index
DAB	Dual Active Bridge
DC	Direct Current
CAPEX	Capital Expenditure
CHB	Cascaded H-Bridge
CMC	Common-Mode Choke
CNB	Cascaded NPC-Bridge
DCM	Discontinuous Conduction Mode
EMI	Electromagnetic Interference
EMU	Electric Multiple Unit
GDU	Gate Drive Unit
GTO	Gate Turn-Off Thyristor
HC-DCM	Half-Cycle Discontinuous Conduction Mode
HF	High Frequency
HV	High Voltage
IBE	Isolated Back End
IFE	Isolated Front End
IGBT	Insulated-Gate Bipolar Transistor
ISOP	Input-Series, Output-Parallel
LF	Low Frequency
LFT	Low-Frequency Transformer
LV	Low Voltage
M2LC	Modular Multilevel Converter
MF	Medium Frequency
MFT	Medium-Frequency Transformer
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MV	Medium Voltage
NPC	Neutral Point Clamped
OPEX	Operational Expenditure
PET	Power Electronic Transformer
PETT	Power Electronic Traction Transformer
PFC	Power Factor Correction
PV	Photovoltaic
PWM	Pulse-Width Modulation

RMS	Root Mean Square
S^3T	Swiss SST
Si	Silicon
SiC	Silicon Carbide
SPSS	Solid-State Power Substation
SRC	Series Resonant Converter
SST	Solid-State Transformer
TCM	Triangular Current Mode
TCO	Total Cost of Ownership
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Contents

1 Introduction

Ever since the Club of Rome published the book *The Limits to Growth* in 1972 [1], the public awareness for the limitation of global resources, be it fossil fuels, clean air and water, or others, and for environmental concerns in general, has been increasing steadily. This awareness and also the notion of responsibility to future generations have put the promotion of renewable energy sources and the improvement of energy efficiency in a top position on many political agendas. For example, the *Europe 2020* strategy [2] of the European Union defines targets in different areas that are to be achieved by the year 2020. Regarding production and usage of energy, greenhouse gas emissions should be cut by 20 %…30 % compared to the levels of 1990. To support this, the energy efficiency should be increased by 20 %, and the share of renewable energy in the total gross energy consumption should be boosted to 20 %; a target that seems within reach with 16 % achieved already in 2014 (cf. **Fig. 1.1a**). As can be seen from **Fig. 1.1b**, an increase of renewable energy production facilitates a reduction of energy produced from fossil, and to a lesser extent also from nuclear, fuels.

The production of electrical energy from renewable sources contributes significantly to an overall increase of their share in the total energy production (cf. **Fig. 1.1a**). However, in a traditional power grid, the power is generated in large, central power plants and is then distributed through a transmission and distribution network, where typically the voltage levels decrease in the direction of the power flow and with increasing granularity of the distribution network, i. e., loads are typically connected either to the medium-voltage (MV) distribution grid if they have a high power demand, or to the low-voltage (LV) distribution grid in case of residential loads.

Whereas it is possible to continuously generate bulk power on a large scale with large hydro power plants, other important renewable energy sources,

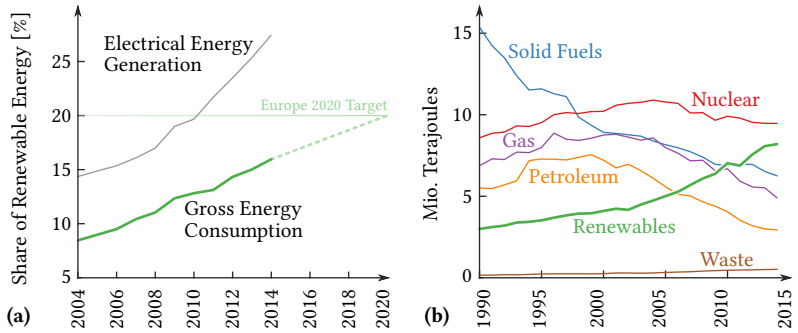


Fig. 1.1: (a) Share of renewables in total energy consumption and electrical energy generation in the EU28 countries (data from [3]). **(b)** Primary energy production in the EU28 countries (data from [4]).

such as wind and solar power, do not lend themselves to be harvested in large, central power plants as easily, and furthermore their availability depends on the weather and hence shows stochastic fluctuations. Both of these aspects create new challenges for the electrical distribution grid: The dispersed nature of such renewable resources often requires connection to the distribution grid in remote locations and correspondingly on low voltage levels—a trend known as "Distributed Generation" [5–7]. This can cause a reversal of the power flow direction in the distribution grid in situations where the locally generated power exceeds the locally consumed power, e. g., due to a high availability of solar energy at noon on a sunny summer day. In the context of distributed generation, also local networks connecting several distributed generation resources with local loads, so-called "microgrids" or "nanogrids", which could be either based on conventional alternating current (AC) connections or in future also on direct current (DC) networks, are discussed in literature [6, 8].

To enhance the distribution grids with the adaptability and controllability required to cope with the challenges outlined above and to ensure high power quality [9], power electronics will play an increasingly important role in an emerging "smart grid", e. g., as devices for flexible AC transmission systems (FACTS) or as interfaces to renewable energy sources such as photovoltaics (PV), etc.

Instead of only complementing the power grid with additional power electronic devices, so-called *Solid-State Transformers* (SSTs) are discussed as replacements for conventional distribution transformers since around the turn of the millennium [9–16]. In addition to isolation and voltage scaling,

such power electronic interfaces between MV and LV levels could provide desirable features such as, e. g., an LV DC bus to interface renewables or local DC microgrids, the ability to control power flows or to provide reactive power, etc.

Note that whereas in this thesis always the term "SST" will be used, the concept is referred to also with other designations in literature, e. g.:

- *Electronic Transformer* [17]
- *Solid-State Transformer, SST* [18]
- *Intelligent Universal Transformer* [14]
- *Energy Control Center, ECC* [8]
- *Energy Router* [16]
- *Power Electronic (Traction) Transformer, PE(T)T* [19].

The last denomination includes the word "traction", highlighting that SSTs are also envisioned for future traction applications. The goals for energy efficiency mentioned above apply also to rail traffic, especially considering that transport by rail is competing with road transportation, which is generally perceived as a main contributor to greenhouse gas emissions and environmental pollution, and hence a shift from the road to the rail is desirable. Whereas a locomotive requires a certain weight in order to achieve sufficient traction, especially in passenger trains there is a trend towards distributed propulsion. So-called electric multiple unit (EMU) concepts are employed [20, 21] in order to increase the useful load, i. e., the available space for passengers and/or freight, which is economically beneficial [22]. Such an increase of the useful load can for example be achieved with low-floor vehicles, where (part of) the traction equipment is mounted on the vehicle roof, which, however, limits the allowable volume and weight [23, 24]. As another example, in case of high-speed trains which could be an environmentally sustainable alternative to domestic flights, the available traction power must be increased to facilitate higher velocities, however, the maximum permissible axle loading limits the weight of the traction equipment, which implies that an increase of the gravimetric power density is required, and again the volumetric power density should be maximized in the interest of a high useful load and passenger comfort [21, 22, 24, 25]. An SST allows to operate the MV/LV transformer, which is required in traction applications to step down the catenary voltage

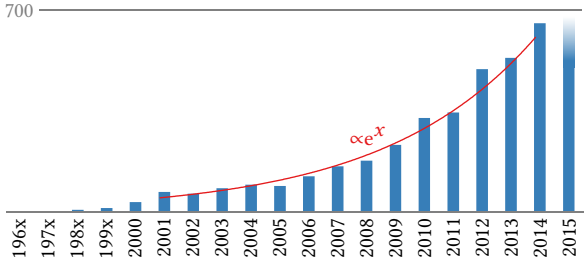


Fig. 1.2: Evolution of the number of SST-related publications *per year*. Numbers are obtained from searching Google Scholar with the query *("solid-state transformer") or ("electronic transformer") or ("intelligent universal transformer") or ("power electronic transformer") or ("power electronics transformer").*

to a level that is suitable for traction drives, by transformers operated with a higher frequency, and hence to reduce volume and weight [19, 24, 26–31].

Fig. 1.2 illustrates that thus there is a high interest in SST technology for various applications in a (future) smart distribution grid, in traction applications, and also in other emerging applications that require an interface between an MV and an LV system, as will be discussed in the next sections in more detail.

1.1 Defining Characteristics of an SST

Solid-state transformer technology has undergone a quick development during the past two decades, and a high number of different topologies, systems, and applications have been—and are being—proposed and analyzed. Various projects [14–16, 32, 33] have been or currently are dedicated to developing SST technology as a key building block of future smart distribution grids, where SSTs could facilitate the integration of renewable energy sources or energy storage systems with either AC or DC interfaces, such as PV, into the grid, or where they could control power routing and facilitate energy management in local microgrids [9–13]. On the other hand, SSTs are also considered for applications where volume and weight restrictions apply, as is the case, e. g., in traction applications. There, SSTs allow to simultaneously improve power density and efficiency compared to conventional solutions based on low-frequency (LF) transformers (LFTs), which has attracted the interest of different manufacturers of traction equipment [19, 24, 26–31].

In the following, based on [34], first the key characteristics of today's SSTs

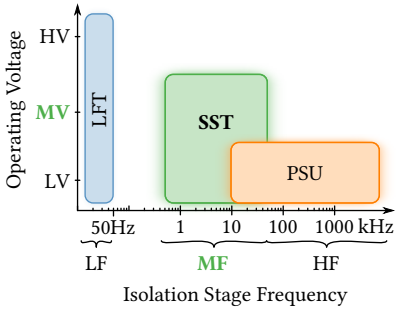


Fig. 1.3: Key characteristics that set an SST apart from a low-frequency transformer (LFT) and from a conventional power supply unit (PSU).

are identified, and it is then shown that the five main modern SST topologies (and hence almost all contemporary SST topologies, which are variations thereof) realize these characteristics by employing the same few key concepts in various combinations (Section 1.2 and Section 1.3). The origins of these key concepts, however, can be traced back to the 1960s.

To understand *why* the same few key concepts are employed in most contemporary SSTs, first the defining characteristics of an SST must be established. Considering, e. g., the aforementioned literature on SSTs, the common key characteristics can be identified as

- connection to MV (in contrast to other isolated power electronic converters that operate with an LV input),
- potential separation by means of medium-frequency (MF) transformers (MFTs),
- controllability (as opposed to conventional LFTs).

Fig. 1.3 illustrates these key characteristics of an SST.

First, an SST interfaces to MV levels, be it AC or DC, at least with one input or output, which is a consequence of the high power levels involved with typical applications, such as traction or smart distribution grids. Thus, any SST needs to handle the connection of power electronics to MV by some means.

Second, increasing the operating frequency of a transformer allows to reduce its volume and weight without increasing the winding current density, J_{rms}, and/or the maximum core flux density, $\hat{B}_{\mathrm{max}}$, (and hence degrading the

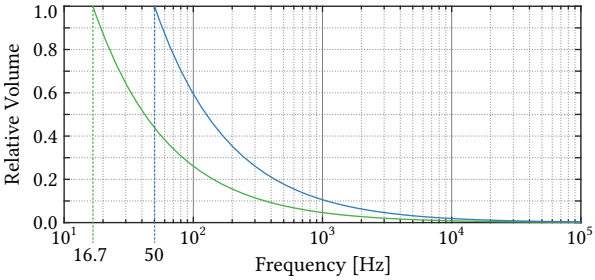


Fig. 1.4: Scaling of transformer volume with frequency (for constant power and given k_W, J_{rms} and $\hat{B}_{max}$) according to (1.1); for two initial operating frequencies (related to 100 % volume) of 16.7 Hz and 50 Hz, respectively.

efficiency), as can be seen from the area product, i. e., the product of the core cross section area, A_{core}, and the winding window area, A_{wdg}, which defines the dependency of the physical size and/or volume of a transformer on the power to be transferred (cf., e. g., [35]),

$$A_{core}A_{wdg} = \frac{\sqrt{2}}{\pi} \cdot \frac{P}{k_W J_{rms} \hat{B}_{max} f} \quad \Rightarrow \quad V \propto (A_{core}A_{wdg})^{\frac{3}{4}} \propto \frac{1}{f^{3/4}}, \qquad (1.1)$$

where f denotes the transformer operating frequency and k_W is the winding window filling factor. **Fig. 1.4** illustrates this dependency of the transformer volume on the operating frequency. This is especially relevant in applications where space and weight are limited, as is, e. g., the case in traction applications (cf. **Fig. 1.5a**). Thus, early efforts to increase the operating frequency of a locomotive's main transformer above the low grid frequency (which can be as low as $16^2/_3$ Hz in several European national traction grids) by means of power converters, and to hence reduce its volume and weight, date back to 1978 [36]. Recent trends in traction systems such as, e. g., distributed propulsion, low-floor vehicles with the traction equipment mounted on the roof, and high-speed trains where a higher power processing capability must be provided while maintaining the same maximum axle weight limit lead to tighter volume and weight constraints [23, 24], which renders MF isolation even more attractive for these applications. In contrast, whereas in grid applications usually weight and volume constraints do not apply, the additional features an SST could provide to a future smart grid, such as harmonic filtering, etc., do require high control dynamics and hence high switching frequencies, too. Thus, independent of its application area, a typical SST employs power elec-

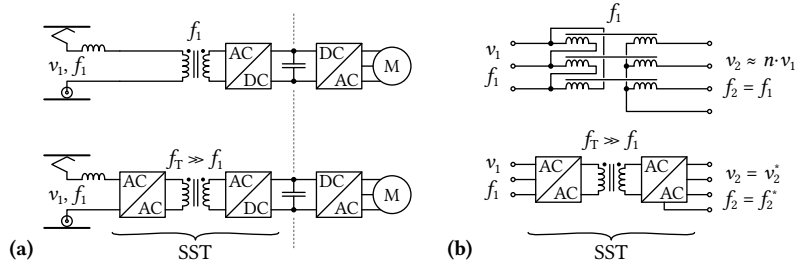


Fig. 1.5: Replacement of an LFT by an SST in **(a)** a traction application in order to comply with weight and space constraints, and **(b)** in a distribution grid application, which is motivated by increased functionality such as, e. g., output voltage control or reactive power compensation. Note that v_1 is in the MV range, f_T is in the MF range, and f_2^* includes also the possibility of a DC output ($f_2^* = 0\,\text{Hz}$).

tronic interfaces and an isolation stage that features a transformer operated in the MF range, i. e., several 100 Hz to several kHz.

Third, in contrast to a conventional transformer, an SST features controllability, i. e., it allows to control its input and/or output voltages and currents (and typically the output frequency) as well as the power flows, and it can protect loads from power system disturbances or the power system from load disturbances, etc. This, and especially also the possibility to interface renewable energy sources such as PV and/or energy storage systems directly to an internal DC bus available in many SST topologies, are further important arguments for the application of SSTs in future smart grids (cf. **Fig. 1.5b**), which has first been proposed around the turn of the millennium [9–13].

1.2 Origins of the Key Concepts Employed in Modern SSTs

With the key characteristics of an SST defined, next the key concepts (and their origins) that are employed to realize these key characteristics can be given a closer look. The two basic variants of isolated converters that allow to use high-frequency (HF) or MF transformers to provide galvanic separation have been proposed by McMurray in 1968 [37,38], as "converter circuits having a high frequency link". **Fig. 1.6a** shows the basic, non-resonant concept [37], where an input AC voltage is chopped by four-quadrant turn-off switches (13 and 15), implemented as anti-parallel connections of transistors with series

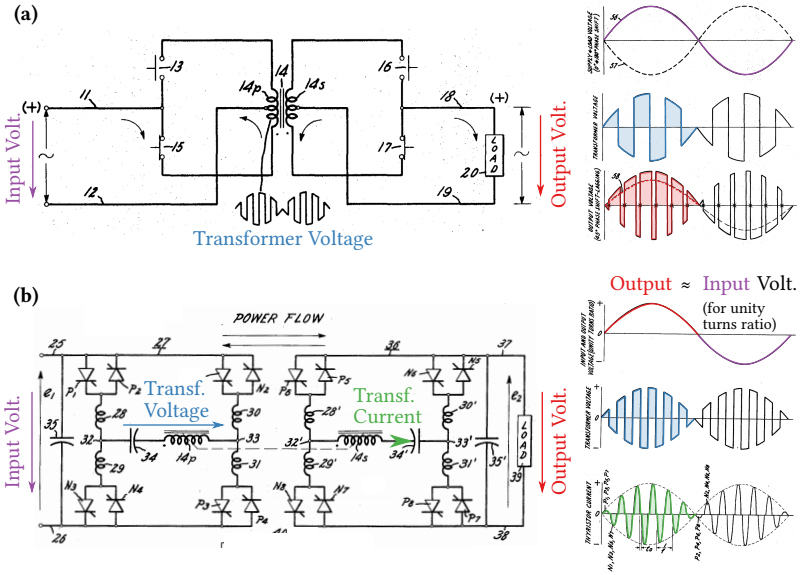


Fig. 1.6: (a) Non-resonant AC-AC power converter with a HF link as proposed in 1968 by McMurray [37], with key converter waveforms illustrating the output voltage regulation by delaying the firing of the secondary side bridge; and **(b)** resonant variant (also shown in an AC-AC configuration) employing the half-cycle discontinuous conduction mode (HC-DCM), also taken from a patent filed by McMurray in 1968 [38] (colors added by the author).

diodes, or, alternatively, as anti-parallel connections of reverse-blocking gate turn-off thyristors (GTOs), in order to generate a HF voltage that is applied to the transformer. The output voltage can be regulated by phase shifting the switching instants of the secondary side rectifier's four-quadrant turn-off switches (16 and 17) with respect to the primary side switches—the system can thus be seen as a (direct) matrix-type electronic AC-AC transformer with voltage regulation capability and HF isolation.

In the 70s, typically thyristor switching devices were employed instead of power transistors, especially for higher power levels. In order to facilitate the commutation of these thyristors, a shaping of the transformer current into sinusoidal pulses with a natural zero-crossing by means of adding a series resonant capacitor as shown in **Fig. 1.6b** was additionally proposed by McMurray, also in 1968 [17, 38] (and, almost simultaneously, in a similar

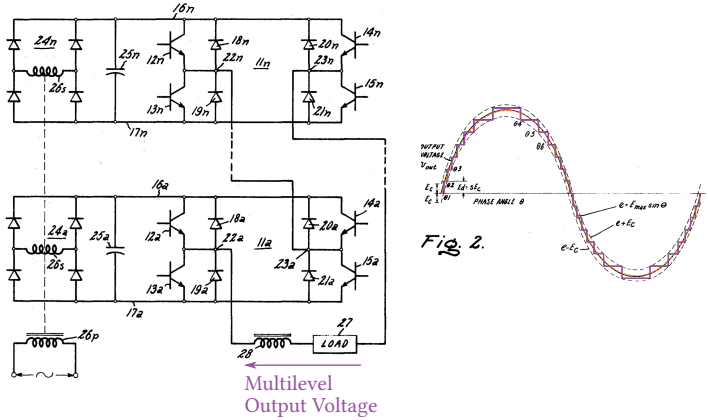


Fig. 1.7: "Fast response stepped-wave switching power converter circuit" patented in 1971 by McMurray [40] (colors added by the author).

fashion by Schwarz [39]). Today, this type of resonant converter is known as "half-cycle discontinuous conduction mode series resonant converter" (HC-DCM SRC), due to the discontinuous shape of the transformer current pulses. The HC-DCM SRC features the very interesting property of maintaining a constant ratio between its input and output DC (or, in case bidirectional switches are employed as in **Fig. 1.6b**, also LF AC) voltages without requiring control and (largely) independent of the transferred power (cf. Section 3.2). Therefore, it acts as an AC-AC or DC-DC transformer with a fixed voltage transfer ratio defined by the turns ratio of the MFT. Furthermore, in contrast to the non-resonant concept, the HC-DCM SRC allows for soft-switching of the power semiconductors, thereby reducing the switching losses and improving the converter efficiency (cf. Section 3.3). Therefore, even though today's semiconductors do not need a zero crossing of the current to turn off as did McMurray's thyristors, the simplicity of the HC-DCM SRC's autonomous operation as an isolation stage and the ability to achieve load-independent soft-switching renders it highly advantageous for many modern SST topologies.

Whereas the converter circuits shown in **Fig. 1.6** are suitable to increase the operating frequency of the isolation transformer, they cannot be connected directly to MV, i. e., several kV to several 10 kV, because the blocking voltage ratings of readily available power semiconductors are limited to a few kV. Therefore, either series connection of semiconductors or multilevel converter topologies must be employed, where the latter offer significant

benefits in terms of reduced filtering effort due to a multilevel output voltage. The use of neutral-point clamped (NPC) converters (1981, [41]) is feasible up to typically five levels, but not arbitrarily scalable to higher voltages. Flying capacitor converters (1992, [42]) can be realized with more voltage levels and hence can support higher voltages, however, also without providing a modular system structure. Therefore, most contemporary SSTs employ a cascade configuration of several converter *cells*. Such a topology is shown in **Fig. 1.7**, which is an excerpt from a patent filed in 1969—also by McMurray—describing a "fast response stepped-wave switching power converter" for driving a sonar transducer [40]. Even though the focus then was not on high voltage levels but on fast transient response, the structure shown in **Fig. 1.7** corresponds to the cascaded H-bridges (CHB) topology as it is employed in one form or the other in most of today's multi-cell SSTs: Each converter cell features an isolated DC interface and a DC-AC conversion stage. The cells are connected in series at their AC terminals and in parallel at their (isolated) DC terminals, thereby forming an input-series output-parallel (ISOP) structure. Today, the supply of a cells' isolated DC bus is typically realized by a (bidirectional) isolated DC-DC converter instead of an unidirectional diode rectifier as shown in the figure. Note, however, that already McMurray mentioned the possibility of using a HF transformer to supply the cells in order to reduce the system's size and weight. It should also be noted that ISOP structures typically feature a beneficial self-balancing mechanism that ensures the balancing of the floating capacitor voltages, essentially because all cells are connected in parallel to the same LV output [43].

1.3 The Five Classes of Modern SST Topologies

Up to today, a myriad of SST topologies has been proposed by both, academia and industry (cf., e. g., [44–47] for a more comprehensive overview). However, most of these are variations of five main modern SST topologies that can be derived as combinations of the key concepts described above, as will be discussed in the following. Note that those topologies that are discussed here on the example of an AC-DC configuration can of course also be realized with an AC output voltage, i. e., as AC-AC converters, by adding an additional inverter stage on the LV side.

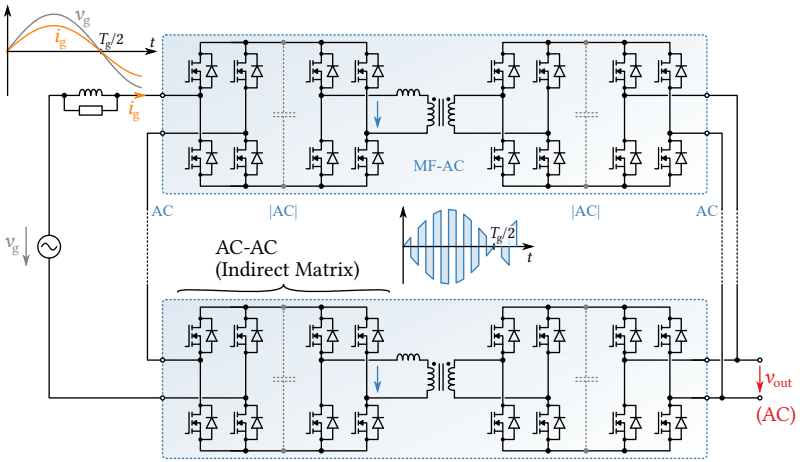


Fig. 1.8: Typical modern matrix-type AC-AC SST topology, which consists of an ISOP arrangement of AC-AC isolation stages as shown in **Fig. 1.6** (resonant or non-resonant variants are possible); an industrial prototype employing this topology is shown in **Fig. 1.10a**.

1.3.1 Matrix-Type SSTs

In applications where a direct AC-AC conversion with MF isolation is required, e. g., for reducing the overall weight and volume of the isolation transformer, but no adaption of the output frequency or any other more advanced controllability that would rely on an intermediate DC bus, an ISOP arrangement of McMurray's AC-AC isolation stages (cf. **Fig. 1.6**) can be used in order to interface to MV systems. Instead of employing a direct matrix-converter approach with bidirectional switches as in the original McMurray patent, it is also possible to first place a folding/unfolding stage to convert the AC voltage into a rectified, i. e., |AC|, voltage, which can then be further processed. This concept has its origin in the field of power supplies and dates back to 1979 [48]. If the further processing is simply a chopping of the |AC| voltage to operate an isolation transformer at a higher frequency, the SST topology shown in **Fig. 1.8** is obtained, where the conversion stages are of the indirect matrix-converter type. This modern (indirect) matrix-type AC-AC SST toppology has recently been patented by GE in 2008 [49], and later a 1 MVA single-phase prototype system has been realized (cf. **Fig. 1.10a**). This "solid-state power substation" (SPSS) prototype employs an ISOP configuration of

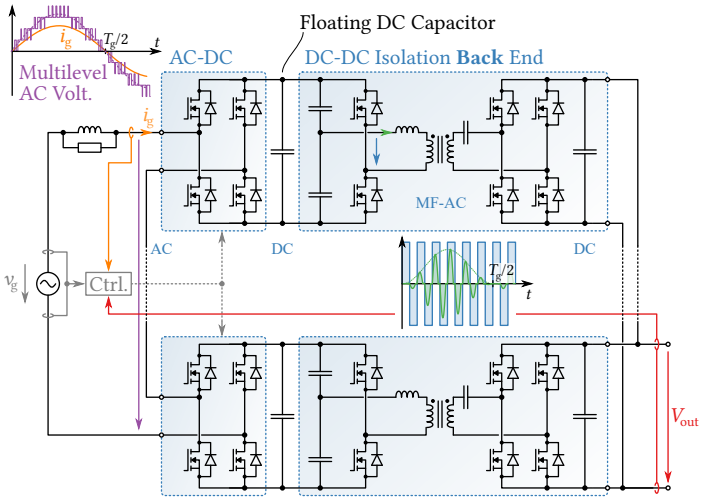
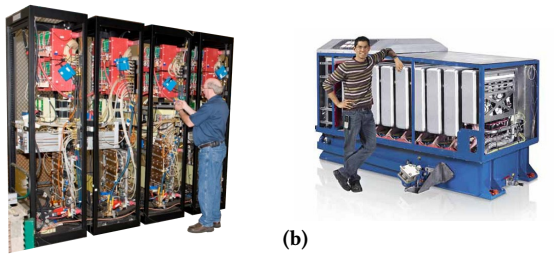


Fig. 1.9: Typical modern Isolated Back End (IBE) topology, realizing a multilevel AC input voltage by means of cascaded H-bridges (cf. **Fig. 1.7**) and employing a resonant DC-DC isolation stage (cf. **Fig. 1.6b**); an industrial prototype is shown in **Fig. 1.10b**.

four cells based on 10 kV silicon carbide (SiC) devices to interface a 13.8 kV grid, which allows for an MFT operating frequency of 20 kHz and an overall AC-AC conversion efficiency of 97 %, and a claimed reduction of the weight by 75 % and of the size by 50 % compared to conventional LFTs [50, 51], even if this is not easily visible from published material. Note that the planned full three-phase system would connect three single-phase systems in a delta configuration on the MV side and in a star configuration on the LV side [52].

1.3.2 Isolated Back End SSTs

If, in contrast, a DC output and/or a higher degree of controllability is required, McMurray's "stepped-wave converter" (cf. **Fig. 1.7**) can be combined with HC-DCM SRC (cf. **Fig. 1.6b**) DC-DC isolation stages supplying the cascaded cells' floating DC buses in order to obtain the topology shown in **Fig. 1.9**. This SST topology, which is likely the most common of the basic modern SST topologies, has actually been patented already in 1996 [26, 27]. Because the controlled AC-DC stages that generate the multilevel output voltage and that are used to control the grid current are located on the MV side of the isolation barrier, this kind of SST topology can be referred to as an



(a) **(b)**

Fig. 1.10: Examples of industrial realizations of SST systems: **(a)** GE's all-SiC 1 MVA single-phase "solid-state power substation" (SPSS) prototype featuring a matrix-type AC-AC topology as shown in **Fig. 1.8** (photo from [51]), and **(b)** ABB's single-phase 1.2 MVA AC-DC "power electronic traction transformer" (PETT) employing an IBE topology as shown in **Fig. 1.9** (photo from [53]).

Isolated Back End (IBE) system [54]. Since the initial patent has been filed at the end of the 1990s, the IBE topology has gained interest from different companies [19,28,30,31], recently resulting in ABB mounting a fully functional SST prototype on a shunting locomotive that has been field-tested on the Swiss railroad (cf. **Fig. 1.10b**). This 1.2 MW single-phase "power electronic traction transformer" (PETT) connects to the 15 kV, $16^2/_3$ Hz Swiss traction grid using an ISOP configuration of nine cascaded converter cells (one of which being redundant) based on 6.5 kV silicon (Si) IGBTs on the input AC side, operating the MFTs with 1.8 kHz and realizing a high overall AC-DC conversion efficiency of 96 % and an improved power to weight ratio of up to 0.75 kVA/kg compared to a standard LFT realization ($\leq$ 0.35 kVA/kg) [19].

Chapter 4 of this thesis provides detailed analyses of several aspects of an IBE SST system.

1.3.3 Isolated Front End SSTs

Another option to arrange the isolation and the controlling stage, which is a third key concept, has been proposed by Weiss already in 1985 for a traction application [55]: As shown in **Fig. 1.11**, the output voltage of a folding stage, i. e., the rectified grid voltage, is directly chopped by a thyristor inverter to operate the isolation transformer with a voltage of higher frequency, which is similar to McMurray's approach (cf. **Fig. 1.7a**). However, the pulsating LV-side DC bus is then interfaced by an additional controlling stage, which, back in the 1980s, Weiss realized as boost converter based on forced-commutated thyristors. This boost converter is controlled to draw a current that is pro-

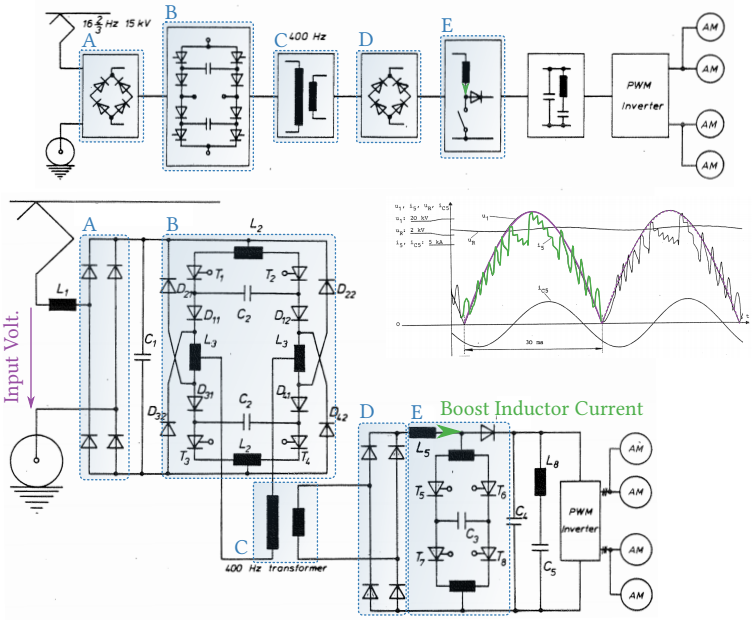


Fig. 1.11: Topology to "eliminate the 16⅔ Hz main transformer on electrical traction vehicles" as proposed by Weiss in 1985 [55], where the control stage (boost converter, E) is placed on the secondary side of the MF isolation stage (B-C-D), resulting in an isolated front end (IFE) approach. The figure is from [55], and colors have been added by the author.

portional to the (rectified) transformer voltage, which in turn is proportional to the rectified input voltage on the primary side. Doing so realizes unity power factor operation on the grid side and provides a DC voltage at the boost converter's output. Since, in contrast to the IBE approach, the controlling and input current shaping stage is placed on the LV side of the isolation barrier, i. e., after the isolation stage, this approach can be referred to as an *Isolated Front End* (IFE) system.

Recently, this concept has been combined with the cascading of converter cells to obtain SST topologies for traction [56] or multi-purpose applications [57]. However, as the original topology from Weiss, these systems feature hard-switched matrix-type isolation stages as shown in **Fig. 1.7a**. In contrast, Han et al. [58, 59] employed the resonant (and hence soft-switched) version of McMurray's "high-frequency link" isolation stage (cf. **Fig. 1.7b**), thereby

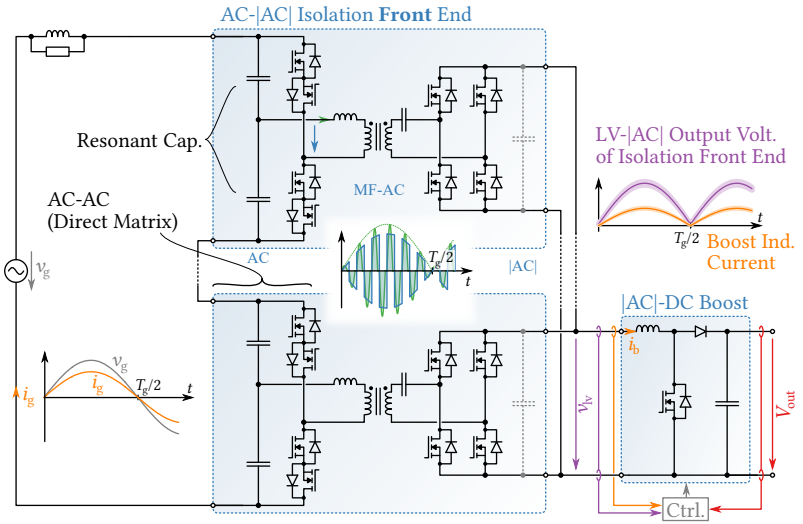


Fig. 1.12: Typical modern IFE topology (cf. **Fig. 1.11**), using also cascaded converter cells and a resonant AC-|AC| isolation stage (cf. also **Fig. 1.6b**).

realizing an IFE topology similar to, but slightly more complicated than the one shown in **Fig. 1.12** [54, 60]. Here, the HC-DCM SRC isolation stage operates as an AC-|AC| converter (which is similar to the AC-AC operating mode shown in McMurray's 1968 patent (cf. **Fig. 1.6b**)). This is in contrast to the IBE approach, where it operates as a DC-DC converter and therefore large DC capacitors on the cascaded cells' MV sides, i. e., on floating potential, are required. In the IFE topology, the capacitors of the isolation stage are only small commutation or resonant capacitors, i. e., there is no significant energy storage in the isolation stage. Hence, the power flow defined by the controlled boost converter on the LV side is directly translated to the MV grid side, allowing for unity power factor operation without requiring MV side measurements, thereby reducing the overall system complexity (note, however, that operation with power factors differing from unity is possible but results in disturbances in the grid current [54]).

Currently, the Power Electronic Systems Laboratory of ETH Zurich is working on an all-SiC realization of an IFE-based SST [54, 60]—the Swiss SST (S^3T)—in the scope of a research program funded by the Swiss government aiming at the promotion of renewable energy and the implementation of smart grid concepts [32]. Therefore, **Chapter 5** of this thesis details on the

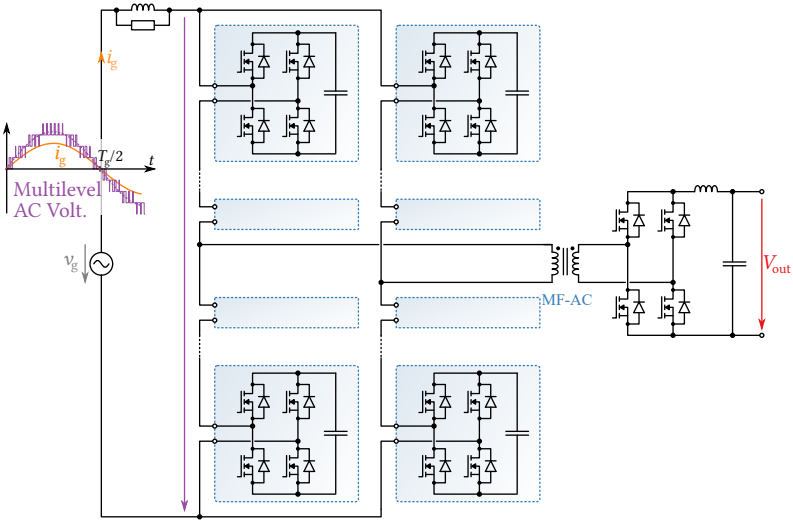


Fig. 1.13: Modular multilevel converter (M2LC) based SST topology [61]. There is only a single transformer, i. e., the modularity is limited to the power electronics.

S^{3}T and **Chapter 6** provides a comparative evaluation of the IFE and the IBE concepts.

1.3.4 Modular Multilevel SSTs

Considering the cascaded cells arrangement shown in **Fig. 1.7**, the topology could be simplified if the individual cells would not need a DC supply. Such a structure has been basically shown in 1981 [62], however, only about 20 years later, in 2002, Marquardt et al. have proposed a full converter including a control method that does not require individual DC supplies for the cells: the Modular Multilevel Converter (M2LC) [63, 64]. A year later, the first SST topology based on a single-phase M2LC and a single MFT (cf. **Fig. 1.13**) has been proposed for a traction application [61, 65]. In contrast to the fully modular topologies discussed so far and shown in **Fig. 1.8**, **Fig. 1.9**, and **Fig. 1.12**, here only the power electronics is modular, whereas there is only a single MFT. The effort in terms of power semiconductors is comparatively high, but on the other hand the single transformer might facilitate the implementation of the isolation system.

1.3.5 Single-Cell Approach

Finally, recent advances in SiC power semiconductor technology provide power semiconductors, e. g., SiC MOSFETs, with significantly higher blocking voltages than available Si devices. These could enable the use of single-cell converter topologies such as, e. g., a standard two-level converter, or more advanced approaches such as the NPC converter mentioned earlier, for interfacing at least lower MV levels. Whereas with these approaches, which are pursued, e. g., by the Future Renewable Electric Energy Delivery and Management (FREEDM) project employing 15 kV SiC devices in an NPC configuration to interface a 13.8 kV MV grid [16], the cascading of converter cells might not be necessary anymore, still an MF isolation stage is employed. The isolation stage is realized either as a HC-DCM SRC, or, offering a higher degree of controllability but also complexity, which, however, is less critical in single-cell systems, as a dual active bridge (DAB) converter, which has been patented 25 years ago by DeDoncker et al. in 1989 [66].

1.3.6 Discussion

The five main SST topologies discussed above, and hence almost all modern SST topologies, have evolved from combinations, and possibly adaptions, of only very few key concepts, whose origins can be traced back to the late 1960s. Interestingly, a common characteristic of four of the five main SST topologies is that they feature a modular structure, i. e., that they employ multiple converter cells, which allows to achieve high reliability by means of adding redundant cells. High reliability is a key requirement of applications where SSTs may replace conventional transformers in the future, such as, e. g., traction and distribution grid applications, future MV DC grids in marine [67, 68], naval [69], and subsea applications [70], and possibly even future aircraft employing distributed propulsion concepts [71]. Furthermore, a modular approach is scalable, in theory to arbitrary voltage levels, and also benefits from economies of scale. Therefore, it can be expected that even with the availability of high-voltage (HV) SiC devices, multi-cell SST topologies and hence, in addition to the MF isolation, also the concept of cascading converter cells will continue to be an integral part of modern SST topologies.

1.4 Aims and Contributions of the Thesis

Considering Section 1.3.6, the aim of this thesis is to contribute to the understanding of key aspects of multi-cell SST technology by providing detailed multi-objective analyses of two main multi-cell SST concepts, the IBE and the IFE approaches. Specifically, the contributions of this thesis to the body of knowledge of SST technology are listed in the following:

- The thesis first presents a comprehensive analysis and multi-objective optimization of the number of cascaded cells (or equivalently, of the semiconductor blocking voltages) employed in an IGBT-based generic multi-cell AC-DC converter.
- In the same context, a generic reliability analysis of multi-cell systems is presented, where advanced concepts such as cell redundancy are included.
- A detailed analysis of the SRC operated in the HC-DCM, which is employed as an isolation stage in IBE- and IFE-based SSTs, is provided. The generic derivation of a dynamic equivalent circuit that accurately models the converter's terminal behavior is described and experimentally verified for the special case of small DC link capacitors. The resulting dynamic equivalent circuit/model facilitates an optimized design of the converter for applications in an IBE or an IFE SST.
- Additionally, an experimentally verified model of IGBT switching losses under zero-current switching (ZCS) or zero-voltage switching (ZVS) conditions is discussed, which enables a comprehensive efficiency versus power density Pareto optimization of the HC-DCM SRC.
- An in-depth analysis of common-mode ground currents, which are observed in cascaded cells converter systems (such as in the AC-DC stages of IBE SSTs) due to the switching actions of the individual cells, and of corresponding mitigation means is provided.
- In order to evaluate the feasibility of an IBE SST in a grid application, a detailed multi-objective comparison (losses, volume, weight, and cost) between such a 1 MVA, 10 kV/400 V SST system and a conventional LF distribution transformer is given.
- A detailed derivation and analysis of a multi-cell IFE topology, which has not yet received much attention in literature, is provided.

- The ZVS behavior of the isolation stage (a HC-DCM SRC) of the IFE SST topology is analyzed in detail, and a variable interlock time that allows to extend the ZVS range is proposed.
- Based on an IFE SST topology variant that is simplified slightly compared to concepts described in literature, a comparative evaluation of all-SiC realizations of an IFE and an IBE SST for MVAC-LVDC power supply applications is provided.
- Finally, a discussion of the applicability of SST technology to various existing and potential future applications is provided, and those applications and environments where SSTs may prove suitable and beneficial are identified.

1.5 Outline of the Thesis

According to the goals and contributions mentioned above, the content of the thesis is divided into six chapters.

Chapter 1 serves as a generic introduction to the SST concept, the motivation for its development and its application, and provides also an overview on the origins of concepts that are key to SSTs. Furthermore, the five main classes of contemporary SST topologies are identified.

Chapter 2 provides a comprehensive analysis and multi-objective optimization of the number of cascaded converter cells of a generic IGBT-based multi-cell AC-DC converter, including also an analysis of reliability aspects of multi-cell systems.

The SRC operated in the HC-DCM is an integral part of many multi-cell SST topologies, where it serves as isolation stage to interface the cascaded converter cells' floating DC buses to a common LV bus. **Chapter 3** discusses the HC-DCM SRC's operating principle and presents a generic derivation of a dynamic equivalent model for the converter's terminal behavior, which is then experimentally verified. Furthermore, a model for loss mechanisms of IGBTs operating under ZCS/ZVS conditions found in this type of converter is experimentally verified, which enables then an efficiency versus power density Pareto optimization of the converter.

Chapter 4 focuses on IBE SST systems and their application in future grid applications. First, the design of the HC-DCM SRC for application in an IBE SST is discussed on the basis of the dynamic equivalent model mentioned above. Also, common-mode ground currents that can be critical in such multi-cell converter systems are analyzed and mitigation means are discussed.

Finally, a comparison of a 1 MVA 10 kV/400 V IBE SST system with an equally rated conventional distribution transformer is carried out.

Focusing more on applications as MVAC-LVDC power supplies, especially in weight and/or volume limited environments, **Chapter 5** provides an in-depth analysis of a 25 kW, 6.6 kV/400 V DC, all-SiC IFE SST system, whereby first a detailed explanation of the topology and the operating principle is given. Then, a detailed analysis of the IFE isolation stage's ZVS behavior and a corresponding optimization of the magnetizing inductance of the isolation transformer and the interlock time is given, whereby a time-dependent variation of the latter is proposed in order to maximize the ZVS range within a period of the grid voltage without increasing converter losses.

Chapter 6 contains a generic comparison of the above mentioned IFE SST and an equally rated IBE SST, which allows to identify the strengths and weaknesses of both concepts, and to evaluate the suitability for certain applications.

Partly based on findings of the other chapters, **Chapter 7** provides a more generic discussion of the applicability of SST technology in grid applications, in environments where volume and weight restrictions apply, or in DC-DC applications. Limitations and potentials of the technology are evaluated considering these different application scenarios, and possible future application areas are outlined.

Finally, the thesis concludes with **Chapter 8**, where the main contributions and findings of the thesis are summarized. In addition, an outlook on possible future research is provided.

1.6 List of Publications

Various parts of the research presented in this thesis have already been published or will be published in international scientific journals, conference proceedings, tutorials, or are being protected by patents. The publications and patents created as part of this PhD thesis, or also in the scope of other projects, are listed below.

Journal Papers

- J. E. Huber, J. Böhler, D. Rothmund, and J. W. Kolar, "A 25kW all-SiC isolated front end 6.6kV/400V AC-DC solid-state transformer," *CPSS Trans. Power Electron. and Appl.*, under review.

- J. E. Huber and J. W. Kolar, "Applicability of solid-state transformers in today's and future distribution grids," *IEEE Trans. Smart Grid*, under review.
- J. E. Huber and J. W. Kolar, "Modular multilevel converter circulating current control using a single active filter module per phase," *IEEJ Trans. Electrical and Electronic Engineering*, under review.
- J. E. Huber, J. W. Kolar, and G. Pammer, "Hybrid inverter concept for extreme bandwidth high-power AC source," *IET Electronics Letters*, May 2017 (early access). DOI: 10.1049/EL.2017.1064
- J. E. Huber, J. Miniböck, and J. W. Kolar, "Generic derivation of dynamic model for half-cycle DCM series resonant converters," *IEEE Trans. Power Electron.*, May 2017 (early access). DOI: 10.1109/TPEL.2017.2703300
- J. E. Huber and J. W. Kolar, "Optimum number of cascaded cells for high-power medium-voltage AC-DC converters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 213–232, Mar. 2017. DOI: 10.1109/JESTPE.2016.2605702
- J. E. Huber and J. W. Kolar, "The origins of key concepts employed in modern solid-state transformers", *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 19–28, Sep. 2016. DOI: 10.1109/MIE.2016.2588878

Conference Papers

- J. E. Huber, D. Rothmund, L. Wang, and J. W. Kolar, "Full-ZVS modulation for all-SiC ISOP-type isolated front end (IFE) solid-state transformer," in *Proc. IEEE Energy Conversion Congr. and Expo. (ECCE USA)*, Milwaukee, WI, USA, Sep. 2016. DOI: 10.1109/ECCE.2016.7855128
- J. E. Huber, D. Rothmund, and J. W. Kolar, "Comparative evaluation of isolated front end and isolated back end multi-cell SSTs," in *Proc. 8th Int. Power Electron. and Motion Contr. Conf. (IPEMC/ECCE Asia)*, Hefei, China, May 2016. DOI: 10.1109/IPEMC.2016.7512863
  Best Paper Award (2nd Price).
- J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio DC/DC converter cells for phase-modular solid-state transformers," in *Proc. IEEE Energy Conversion Congr. and Expo. (ECCE USA)*, Montréal, QC, Canada, Sep. 2015. DOI: 10.1109/ECCE.2015.7310368

- J. E. Huber and J. W. Kolar, "Volume/weight/cost comparison of 1 MVA 10 kV/400 V solid-state against a conventional low-frequency distribution transformer," in *Proc. IEEE Energy Conversion Congr. and Expo. (ECCE USA)*, Pittsburgh, PA, USA, Sep. 2014. DOI: 10.1109/ECCE.2014.6954023

- J. E. Huber and J. W. Kolar, "Common-mode currents in multi-cell solid-state transformers," in *Proc. Int. Power Electronics Conf. (IPEC/ECCE Asia)*, Hiroshima, Japan, May 2014. DOI: 10.1109/IPEC.2014.6869674

- J. E. Huber and J. W. Kolar, "Optimum number of cascaded cells for high-power medium-voltage multilevel converters," in *Proc. IEEE Energy Conversion Congr. and Expo. (ECCE USA)*, Denver, CO, USA, Sep. 2013. DOI: 10.1109/ECCE.2013.6646723

- J. E. Huber, G. Ortiz, F. Krismer, N. Widmer, and J. W. Kolar, "η-ρ Pareto optimization of bidirectional half-cycle discontinuous-conduction-mode series-resonant DC/DC converter with fixed voltage transfer ratio," in *Proc. 28th Applied Power Electronics Conf. (APEC)*, Long Beach, CA, USA, Mar. 2013. DOI: 10.1109/APEC.2013.6520484

- J. E. Huber and A. Korn, "Optimized pulse pattern modulation for modular multilevel converter high-speed drive," in *Proc. 15th Int. Power Electron. and Motion Control Conf. (EPE-PEMC)*, Novi Sad, Serbia, Sep. 2012. DOI: 10.1109/EPEPEMC.2012.6397383

Tutorials

- J. W. Kolar and J. E. Huber, "Fundamentals and application-oriented evaluation of solid-state transformer concepts," Tutorial at the *Southern Power Electron. Conf. (SPEC)*, Auckland, New Zealand, Dec. 2016.

- J. W. Kolar and J. E. Huber, "Solid-state transformers: Key design challenges, applicability, and future concepts," Tutorial at the *8th Int. Power Electron. and Motion Contr. Conf. (IPEMC/ECCE Asia)*, Hefei, China, May 2016.

- J. W. Kolar and J. E. Huber, "Solid-state transformers: Key design challenges, applicability, and future concepts," Tutorial at the *31st Applied Power Electronics Conf. (APEC)*, Long Beach, CA, USA, Mar. 2016.

- J. W. Kolar and J. E. Huber, "Solid-state transformers in future traction and smart grids," Tutorial at the *Int. Power Conv. and Intelligent Motion Conf. (PCIM Europe),* Nuremberg, Germany, May 2015.

Workshops

- J. E. Huber and J. W. Kolar, "Derivation and comparative analysis of multi-cell isolated front end and isolated back end SSTs," presented at the *ECPE Workshop "Smart Transformers for Traction and Future Grid Applications",* Zurich, Switzerland, Feb. 2016.
- J. E. Huber and J. W. Kolar, "Interfacing of medium voltage and low voltage power systems using solid-state transformers," presented at the *EADS Workshop "High Voltage Propulsion Network for Electro/Hybrid Aircraft",* Ottobrunn, Germany, Mar. 2016.

Patents

- J. W. Kolar and J. E. Huber, "Modularer Multilevel-Stromrichter", Swiss Patent Application, Filed Apr. 26, 2017.
- J. W. Kolar, J. E. Huber, F. Krismer, D. Neumayr, and P. Papamanolis, "Wechselrichter", Austrian Patent Application A 50231/2017, Filed Mar. 22, 2017.
- J. W. Kolar and J. E. Huber, "Konverter zur potentialgetrennten Übertragung elektrischer Energie," Swiss Patent Application, Filed Jan. 12, 2016.
- J. W. Kolar, P. Cortes and J. E. Huber, "Verfahren zur Regelung einer Sternpunktspannung eines elektronischen Leistungswandlers," Swiss Patent Application, Filed Sep. 09, 2013.

Further Scientific Contributions

- J. Miniböck, J. E. Huber, and J. W. Kolar, "Three-phase buck-boost PFC rectifier with common-mode free output voltage and low semiconductor blocking voltage stress," *IEEJ Trans. Electrical and Electronic Engineering*, under review.
- G. Ortiz, M. Leibl, J. E. Huber, and J. W. Kolar, "Design and experimental testing of a resonant DC-DC converter for solid-state transformers,"

IEEE Trans. Power Electron., vol. 32, no. 10, pp. 7534–7542, Oct. 2017. DOI: 10.1109/TPEL.2016.2637827

- D. Rothmund, D. Bortis, J. E. Huber, D. Biadene, and J. W. Kolar, "10kV SiC-based bidirectional soft-switching single-phase AC/DC converter for medium-voltage solid-state transformers," in *Proc. 8th Int. Symp. on Power Electron. for Distributed Generation Systems (PEDG)*, Florianópolis, Brazil, Apr. 2017.

- T. Guillod, J. E. Huber, G. Ortiz, A. De, C. Franck, and J. W. Kolar, "Characterization of the voltage and electric field stresses in multi-cell solid-state transformers," in *Proc. IEEE Energy Conversion Congr. and Expo. (ECCE USA)*, Pittsburgh, PA, USA, Sep. 2014. DOI: 10.1109/ECCE.2014.6954048

- D. Rothmund, J. E. Huber, and J. W. Kolar, "Operating behavior and design of the half-cycle discontinuous-conduction-mode series-resonant-converter with small DC link capacitors," in *Proc. 14th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Salt Lake City, USA, Jun. 2013. DOI: 10.1109/COMPEL.2013.6626447

- P. Cortes, J. E. Huber, M. Silva, and J. W. Kolar, "New modulation and control scheme for phase-modular isolated matrix-type three-phase AC/DC converter," in *Proc. 39th Annu. IEEE Industrial Electronics Society Conf. (IECON)*, Vienna, Austria, Nov. 2013. DOI: 10.1109/IECON.2013.6699928

2 Optimum Number of Cascaded Converter Cells

For power electronic systems, such as SSTs, to interface MV grids, usually cascaded cells converters need to be employed, whereby either few cells featuring power semiconductors with high blocking voltage capability or a larger number of cells using LV semiconductors can be used. As shown in this section, which is based on [72], physics-inspired empirical models of the dependency of IGBT power modules' loss-relevant characteristics on the blocking voltage enable an analytic optimization of the efficiency of a CHB (AC-DC) converter, which is complemented by a full efficiency versus power density $\eta\rho$-Pareto optimization. For a 10 kV grid, 1200 V or 1700 V are identified as optimum blocking voltages resulting in a suitable trade-off between efficiency and power density. Significant efficiency and power density gains can be realized by replacing Si IGBTs by LV SiC devices in multi-cell systems, whereas single-cell designs based on HV SiC devices suffer from the high dv/dt and di/dt values required to limit switching losses. Reliability is analyzed considering redundancy, showing that the reliability of designs based on lower blocking voltages can be comparable to that of designs using higher blocking voltages and hence fewer cells, if similar effort concerning additionally installed power capability is considered.

2.1 Introduction

In order to interface, e. g., a 10 kV MV grid, either series connections of power semiconductors or multilevel converters have to be employed [9]. The latter avoid issues with voltage sharing among individual switches and can generate

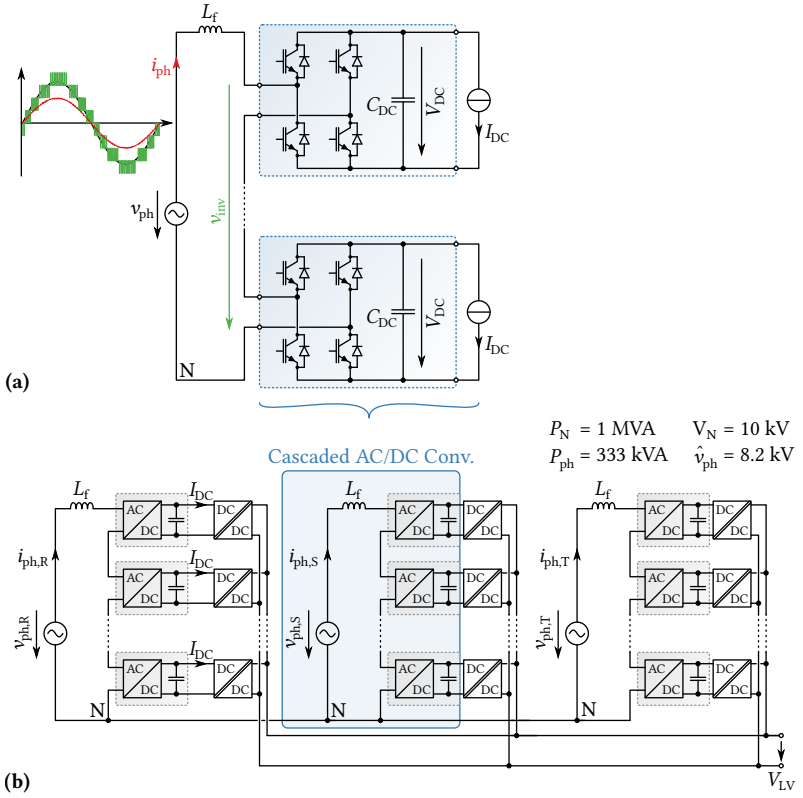


Fig. 2.1: (a) Single-phase CHB converter structure with the DC-side supply/loads modeled as DC current sources (as considered throughout the chapter), including key waveforms, and **(b)** exemplary application of this CHB structure in a three-phase AC-DC SST.

multilevel output voltage waveforms with improved harmonic performance and hence reduced filtering requirements compared to a conventional two-level approach [73]. Therefore, single-cell three-level diode-clamped [41] and capacitor-clamped topologies [42] have found widespread application in the MV drives industry, however, these concepts cannot be scaled to higher voltage levels easily without resorting again to a direct series connection of power semiconductors, because even though topology variants with more than three voltage levels are possible, such configurations increase the system

complexity yet do not provide modularity.

Paralleling [74] or series connecting [75] converter *cells* instead of the power semiconductors is a well-known alternative approach. A typical example using a series connection of converter cells is the CHB topology (cf. **Fig. 2.1a**), which has been patented already in the 1970s [40]. In theory, this modular approach can cope with any grid voltage by increasing the number of cascaded cells. As an aside, instead of cascading H-bridges, cells featuring two NPC legs could be employed, creating a cascaded NPC-bridge converter (CNB) [76] as is used in the *MEGAlink* SST (cf. **Chapter 4**). Since the cells' potentials with respect to ground change constantly due to the switching operations of the other cells in the stack, the DC-side supply or the DC-side load of each cell requires a galvanic isolation (notable exceptions being the modular multilevel converter [63, 64], or battery storage applications [77]). Realizing these isolation stages by means of isolated DC-DC converters featuring an MFT, and connecting then the LV DC outputs of all these DC-DC converters in parallel to a common LV DC bus, i. e., employing an ISOP configuration, results in a typical multi-cell MVAC-LVDC SST topology [19, 26, 30, 78], which is shown in **Fig. 2.1b** in a three-phase configuration. Note that only one phase stack would be required in a single-phase traction application.

Cascading of converter cells is thus a feasible approach to interface power electronic systems such as SSTs to the MV grid. Considering recent advances in HV SiC power semiconductor technology which have resulted in 4H-SiC IGBTs with blocking voltages of 15 kV and beyond [79, 80], SSTs based on 10 kV [81] or 15 kV [82] devices and conventional single-cell two-level or three-level converter topologies could be alternatively considered. However, only LV SiC power modules with blocking voltages up to 1700 V are currently available as products, cf. e. g., [83–85]. Therefore, especially in heavy-duty industrial applications, Si IGBT power modules will prevail in the foreseeable future and might be gradually complemented by LV SiC solutions. In either case, the blocking voltages of industrially available semiconductor modules are limited to several kV (e. g., to 6.5 kV for silicon IGBTs). Furthermore, only about 50 % to 60 % of the devices' rated blocking voltage can be utilized in an application in order to limit the susceptibility to cosmic-ray induced failures [86, 87].

Thus, a cascaded cells system can be realized using few cells employing, e. g., 6.5 kV IGBTs, but also using many cells based on, e. g., 600 V IGBTs. This section comprehensively discusses the trade-offs which have to be considered for the selection of the number of cells in order to identify the optimum num-

ber of cascaded cells for a given grid voltage (or, equivalently, the optimum semiconductor blocking voltage), considering efficiency, power density, and also reliability aspects.

Initial analyses of the trade-offs affected by the number of cascaded cells have been addressed in [88] for IGBTs with 3.3 kV blocking voltage and higher, and in [77], where due to the employed low switching loss modulation scheme basically only conduction losses have been considered. Therefore, first an analytic loss analysis based on physics-inspired models of IGBT parameters' dependencies on the blocking voltage, covering the full range from 600 V to 6.5 kV, is introduced in Section 2.2. Subsequently, a full efficiency versus power density $\eta\rho$-Pareto analysis [89] is performed in Section 2.3, where also modern LV-SiC power modules are considered. Finally, fundamental reliability aspects of multi-cell systems are discussed in Section 2.4.

2.2 Basic Considerations on the Optimum Number of Cascaded Converter Cells

In the following, a single CHB phase stack as shown in **Fig. 2.1a** will be considered. In order to obtain generic results that are applicable to cascaded cells converters in general, the cascaded cells' DC side sources or loads are modeled as DC current sources. Depending on the application, these might represent isolated DC-DC converters (SSTs) or passive diode rectifiers fed by a grid-frequency multi-winding transformer (drive systems); in case of a STATCOM application, or for an M2LC, no current sources would be present. In addition to the variable number of cascaded converter cells that can generate an output voltage waveform with multiple levels, a filter inductor, L_f, is required to limit the current harmonics injected into the grid.

Fig. 2.2 gives an overview of the trade-offs affected by the number of cascaded converter cells. If the number of cells is high, the required semiconductor blocking voltage is low. By using pulse-width modulation (PWM) with phase-shifted carriers [90, 91] and many cascaded cells, the number of voltage levels and the effective switching frequency seen by the filter inductor are increased and hence the required switching frequency per cell and the filtering effort, i. e., L_f, can be reduced. However, the conduction losses increase because the phase current passes through more (bipolar) power semiconductors in series, i. e., the total voltage drop increases. Also, reliability concerns might arise if the number of cells is high. On the other hand, using only few cascaded cells employing devices with higher blocking voltages

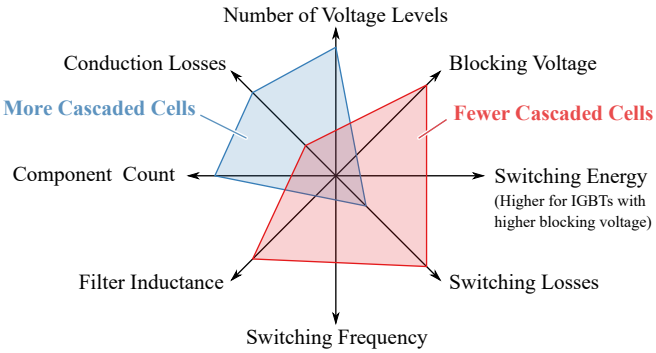


Fig. 2.2: Overview of the trade-offs that are affected by the number of cascaded converter cells.

reduces the number of available voltage levels, which requires either a larger filter, L_f, and/or higher switching frequencies to keep the harmonic content of the grid current within limits. However, since the switching energies of IGBTs increase with blocking voltage, high switching losses are generated if high switching frequencies are needed. Therefore, designs based on devices with higher blocking voltages are dominated by switching losses, whereas designs based on lower blocking voltages are dominated by conduction losses. This trade-off regarding semiconductor losses will be analyzed in detail in the following.

2.2.1 Blocking Voltage Scaling of IGBT and Diode Characteristics

In order to investigate how the device blocking voltage affects the trade-off between conduction and switching losses, the scaling of the relevant parameters of IGBTs and diodes with blocking voltage and rated current needs to be investigated and approximated, which is done in the following by fitting physics-inspired models to empirical data of modern IGBT modules (Infineon IGBT3/IGBT4 types featuring a trench/field-stop design, considering the data for a junction temperature of $T_j = 125\,°C$). The raw data, the corresponding fits, and resulting model parameters can be found in the next Section 2.2.2. These models allow to estimate the conduction and switching loss characteristics of a *virtual* power module with arbitrary rated blocking voltage, V_B, and rated current, I_N.

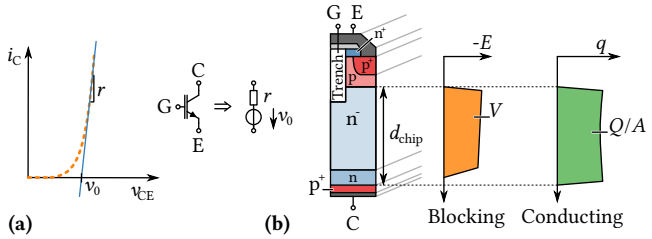


Fig. 2.3: (a) Approximation of an IGBT (or diode) forward characteristic by v_0 and r, and **(b)** schematic cross section (not to scale) of a trench/field-stop IGBT with qualitative drift region field distribution in the blocking state and qualitative charge carrier concentration in the conducting state [92]. The integral of the electric field corresponds to the applied reverse voltage, and the integral of the charge carrier density along d_{chip} gives the stored charge per chip area.

Conduction Losses

Generally, the v_{CE} versus i_C (or, for diodes, v_F versus i_F) characteristic of bipolar power semiconductors can be approximated by a linear model $v_{CE}(i_C) = v_{CE,0} + r \cdot i_C$ as shown in **Fig. 2.3a** ($v_{CE,0} = v_0$). The total forward voltage drop at rated current, $v_{CE}(I_N)$, thus consists of the two parts, $v_{CE,0}$ and $v_{CE,r} = r \cdot I_N$. From semiconductor physics [93] it is expected that the total forward voltage drop at rated current and hence $v_{CE,0}$ and $v_{CE,r}$ scale with the blocking voltage roughly as

$$v_{CE,0}(V_B) = A_{v0} \cdot \log(B_{v0} \cdot V_B + C_{v0}) \text{ and} \tag{2.1}$$

$$v_{CE,r}(V_B) = r \cdot I_N = A_r \cdot \log(B_r \cdot V_B), \tag{2.2}$$

implying

$$r(V_B, I_N) = \frac{1}{I_N} \cdot A_r \cdot \log(B_r \cdot V_B). \tag{2.3}$$

These functions can be fitted (parameters A_{v0}, B_{v0}, C_{v0}, A_r, and B_r) with good accuracy to empirical data as is shown in Section 2.2.2. Note that r is inversely proportional to the rated current (chip area) for a given blocking voltage. This can be explained considering that the maximum loss density in a chip is limited, corresponding to a maximum permissible current density at rated current [94]. Therefore, the chip area in a module must be $A_{chip} \propto I_N$ and hence $r \propto 1/A_{chip} \propto 1/I_N$.

Switching Losses

In order to express the dependency of switching losses on the blocking voltage with low complexity, the switching energies of a given device are approximated to scale linearly with the switched current and also with the applied DC voltage, i. e., the blocking voltage utilization, $u = V_{DC}/V_B$. Then, the switching losses of a specific device can be expressed by a normalized switching energy, $K_{sw} = E_{sw}(I_N)/I_N$ for $u = 0.5$ (as typically specified in datasheets) and with $[K_{sw}] = \text{mJ/A}$. The switching energy of a certain transition can then be calculated from K_{sw} as

$$E_{sw} = K_{sw} \cdot i_{sw} \cdot \frac{u}{0.5} \quad \text{with} \quad [E_{sw}] = \text{mJ}, \tag{2.4}$$

where u denotes the actual application's blocking voltage utilization which might be different from $u = 0.5$ for which K_{sw} is specified. Note that three individual values of K exist for turn-off, turn-on and diode recovery losses, i. e., K_{off}, K_{on} and K_{rec}.

Fig. 2.3b shows a schematic cross section of a modern field-stop IGBT with a trench-gate structure together with the field distribution across the n^- drift region in the blocking state and the charge carrier density distribution across the n^- drift region in the conducting state. Switching energies of bipolar power semiconductors are roughly proportional to this stored charge that needs to be removed during the turn-off process, and to the reapplied voltage, i. e., $E_{sw} \propto Q \cdot u \cdot V_B$ [95]. Assuming an approximately rectangular field profile in the blocking state, the chip thickness, d_{chip}, is proportional to the blocking voltage, i. e., $d_{chip} \propto V_B$. Assuming further an approximately rectangular charge density profile in the conduction state, the stored charge per chip area is proportional to the chip thickness i. e., $Q/A_{chip} \propto d_{chip} \propto V_B$. Hence, since the chip area is proportional to the rated current, the normalized switching energies are expected to scale with the square of the blocking voltage, i. e., $K_{sw} \propto V_B^2$. These considerations inspire the following models for the scaling of normalized turn-off, turn-on and diode recovery losses with the rated blocking voltage:

$$K_{off}(V_B) = A_{off}V_B^2 + B_{off}V_B + C_{off}, \tag{2.5}$$

$$K_{on}(V_B) = A_{on}V_B^2 + B_{on}V_B + C_{on}, \tag{2.6}$$

$$K_{rec}(V_B) = A_{rec}V_B^2 + B_{rec}V_B + C_{rec}. \tag{2.7}$$

Note that the approximated normalized switching energies are modeled without a dependency on the current rating, i. e., the chip area, which is in accor-

dance with findings from [96]. Again, Section 2.2.2 provides the fit results and model parameters (A_i, B_i, C_i with i = off, on, rec).

Thermal Resistance

The thermal resistance from junction to heat sink, $R_{th,jh}$, (in datasheets specified per device, i. e., per individual IGBT or diode) is expected to be roughly inversely proportional to the chip area, while other factors such as the package, etc. also have an influence. The chip area, in turn, is proportional to the current rating, but depends also on the blocking voltage because $v_{CE}(I_N)$ and hence also the allowable maximum current density for a given loss density limit shows this dependency (cf. Section 2.2.2). Therefore, and to account for the observed increase of package size with rated blocking voltage, the thermal resistances are modeled as

$$R_{th,jh}(V_B, I_N) = A_{Rth} \cdot (V_B \cdot I_N)^{-B_{Rth}}, \tag{2.8}$$

which fits the empirical data well, as is shown in Section 2.2.2.

2.2.2 Empirical Modeling of Power Modules

This subsection presents parameters of analytical approximations used to model the IGBT and diode characteristics concerning the dependencies on the rated blocking voltage, V_B, and the rated current, I_N, and provides some additional remarks. The empirical data (for $T_j = 125\,°C$) has been obtained from datasheets of modern Infineon IGBT3/IGBT4 trench/field-stop IGBT modules with a wide range of blocking voltage and nominal current ratings. The number of modules considered per blocking voltage has been considered in the fits in order to assign the same weight to each blocking voltage.

Conduction Losses

Fig. 2.4a shows the voltage drop at nominal current, $v_{CE}(I_N)$, and its two components, $v_{CE,v0}$ and $v_{CE,r}$ (cf. **Fig. 2.3a**), as functions of the blocking voltage, and the fitted curves according to (2.1) and (2.2); **Fig. 2.4b** shows the same data for diodes (note that the dependencies on the blocking voltage for IGBTs and diodes are quite similar). The resulting model parameters can be found in **Tbl. 2.1** and **Tbl. 2.2**, respectively. To further verify the model, **Fig. 2.4c** shows typical on-state voltages at rated current, i. e., $v_{CE}(I_N)$, for IGBTs with different blocking voltages as published in [94] (note that these values are for IGBT modules from *another* manufacturer). The $v_{CE}(I_N)$

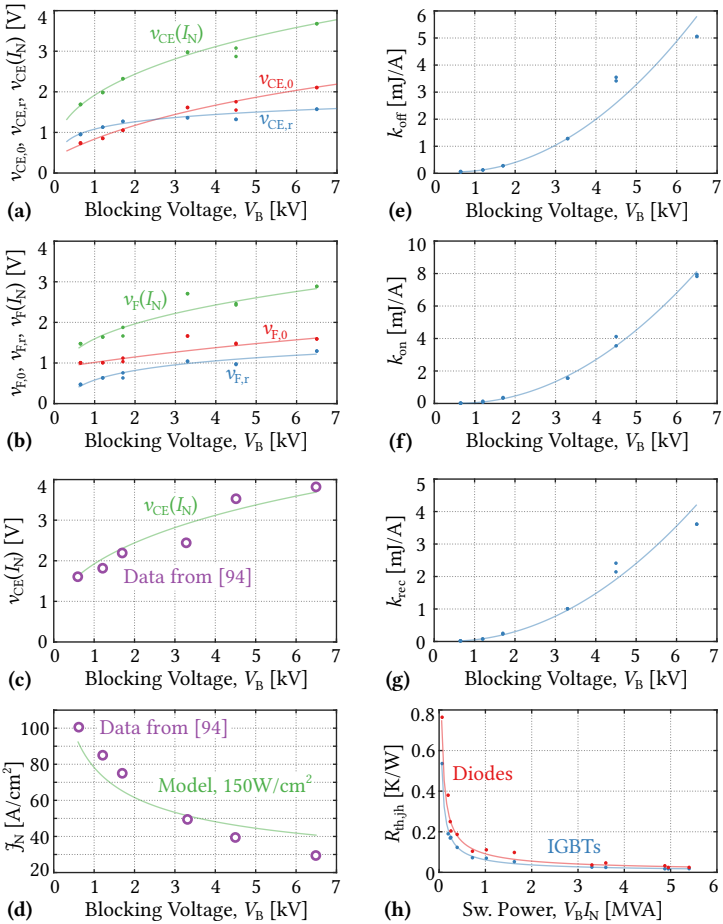


Fig. 2.4: Datasheet values for the loss-relevant IGBT and diode parameters and fitted analytical approximations for **(a)** IGBT conduction losses, **(b)** diode conduction losses, **(e)** normalized turn-off losses, **(f)** normalized turn-on losses, **(g)** normalized diode recovery losses, and **(f)** thermal resistances from junction to heat sink; **(c)** compares the conduction loss model with typical data for the forward voltage at rated current from [94], and **(d)** does the same for the corresponding nominal current densities.

Tbl. 2.1: Parameters of IGBT model (based on the SI unit system, units omitted for better legibility).

$v_{\mathrm{CE,v0}}(V_\mathrm{B})$	A_v0	=	1.3862
	B_v0	=	$5.0353 \cdot 10^{-4}$
	C_v0	=	1.3244
$v_{\mathrm{CE,r}}(V_\mathrm{B})$	A_r	=	0.2605
	B_r	=	0.0635
$K_\mathrm{off}(V_\mathrm{B})$	A_off	=	$1.6097 \cdot 10^{-7}$
	B_off	=	$-1.6897 \cdot 10^{-4}$
	C_off	=	0.0992
$K_\mathrm{on}(V_\mathrm{B})$	A_off	=	$2.3481 \cdot 10^{-7}$
	B_off	=	$-2.9117 \cdot 10^{-4}$
	C_off	=	0.1066
$R_{\mathrm{th,jh}}(V_\mathrm{B}, I_\mathrm{N})$	A_Rth	=	1866.7
	B_Rth	=	0.7468

characteristic obtained from the model in (2.1) and (2.2) using the parameters given in **Tbl. 2.1** shows good agreement also with these values, indicating that the objective of modeling the characteristics of a "typical" IGBT is achieved.

As mentioned earlier, the datasheet current ratings are typically chosen such that the loss density in the IGBT chips of a module at rated current, i. e., $v_\mathrm{CE}(I_\mathrm{N}) \cdot J_\mathrm{N} = v_\mathrm{CE}(I_\mathrm{N}) \cdot I_\mathrm{N}/A_\mathrm{chip}$, does not exceed a limit of about $100\,\mathrm{W/cm^2}$ to $150\,\mathrm{W/cm^2}$, resulting in a decrease of the nominal current density, J_N, with increasing blocking voltage, as is illustrated again by data taken from [94] in **Fig. 2.4d**. This means that a module with higher blocking voltage rating has a larger chip area for the same rated current. Taking the $v_\mathrm{CE}(I_\mathrm{N})$ characteristic from the fitted model and assuming a loss density limit of $150\,\mathrm{W/cm^2}$ to calculate $J_\mathrm{N}(V_\mathrm{B})$, again good agreement with the data from [94] can be observed. The deviations indicate that for lower blocking voltages higher loss densities might be permissible in practical module designs, whereas for higher blocking voltages lower loss densities must be used, which can be attributed to differences in the packaging technologies [94]. Note also that the effective silicon area would in addition also include the chip edge passivations, further increasing the chip areas for higher blocking voltages.

Tbl. 2.2: Parameters of diode model (based on the SI unit system, units omitted for better legibility).

$v_{\mathrm{F,v0}}(V_{\mathrm{B}})$	A_{v0}	=	1.2316
	B_{v0}	=	$2.5990 \cdot 10^{-4}$
	C_{v0}	=	2.0201
$v_{\mathrm{F,r}}(V_{\mathrm{B}})$	A_{r}	=	0.3410
	B_{r}	=	0.0055
$K_{\mathrm{rec}}(V_{\mathrm{B}})$	A_{rec}	=	$1.1240 \cdot 10^{-7}$
	B_{rec}	=	$-8.6844 \cdot 10^{-5}$
	C_{rec}	=	0.0267
$R_{\mathrm{th,jh}}(V_{\mathrm{B}}, I_{\mathrm{N}})$	A_{Rth}	=	2014.2
	B_{Rth}	=	0.7240

Switching Losses

Fig. 2.4e, **f** and **g** show the normalized switching energies as functions of the blocking voltage and the corresponding approximations and/or model characteristics. Since, in contrast to the conduction loss case, the raw data obtained from the datasheets spans about two orders of magnitudes, it is important to find the model parameters by considering normalized residuals, i. e., by minimizing the function

$$R = \sum_{\mathrm{i}=1}^{N_{\mathrm{devices}}} \left(\frac{K_{\mathrm{sw}}(V_{\mathrm{B,i}}) - K_{\mathrm{sw,i}}}{K_{\mathrm{sw,i}}} \right)^2 , \tag{2.9}$$

with $K_{\mathrm{sw}}(V_{\mathrm{B}})$ as in (2.5), (2.6) or (2.7), respectively. This ensures similar *relative* errors between the model and the data points, and explains why the fit curves in **Fig. 2.4e**, **f** and **g** seem to be very accurate for lower blocking voltages and less accurate for higher blocking voltages.

As an aside, note that the 4.5 kV devices show lower $v_{\mathrm{CE}}(I_{\mathrm{N}})$ and higher K_{sw} than expected. The reason for this is that the available devices in this voltage class are optimized more towards low conduction losses, which is achieved by increasing the high-level lifetime of the charge carriers, resulting in an increase of the switching energies [93].

Thermal Resistances

Finally, **Fig. 2.4h** shows the thermal resistances of IGBTs and diodes versus the rated switching power, i. e., $V_B \cdot I_N$, and the corresponding fits, which are obtained in the same way as those for the switching losses.

2.2.3 Analytic Derivation of the Optimum Blocking Voltage

The models for semiconductor parameters as functions of the blocking voltage and current rating derived in the previous subsections facilitate the calculation of conduction and switching losses of a cascaded cells converter system according to **Fig. 2.1a** with an arbitrary cell number, which will be discussed in the following. Unity power factor operation and a power flow from AC to DC (i. e., rectifier mode) is assumed without loss of generality.

System Quantities

The required total DC voltage of a phase stack (i. e., the sum of the cell's DC voltages) is given by

$$V_{DC,total} = \frac{\hat{v}_{ph}}{M_N} = \sqrt{\frac{2}{3}} \frac{V_N}{M_N}, \tag{2.10}$$

where $M_N = \hat{v}_{ph}/V_{DC,total}$ denotes the nominal modulation index and V_N is the nominal grid voltage (line-to-line). This total DC link voltage is split among the cascaded converter cells. With V_B denoting the blocking voltage of the power semiconductors used and with u being the blocking voltage utilization, the DC voltage of a single cell is given by $V_{DC} = u \cdot V_B$ and hence the required number of cascaded cells follows directly as

$$n_{cell} = \frac{V_{DC,total}}{u \cdot V_B}. \tag{2.11}$$

This equation illustrates the equivalence of looking at the optimum number of cascaded converter cell and at the optimum semiconductor blocking voltage. Note that in actual implementations of course only a discrete number of cells could be used, i. e., $n_{cell,actual} = \lceil n_{cell} \rceil$.

The amplitude of the phase current, $\hat{i}_{ph}$, can be calculated as

$$\hat{i}_{ph} = \sqrt{2} \cdot \frac{P_{ph}}{V_N/\sqrt{3}}, \tag{2.12}$$

and its RMS value and the rectified average value follow then directly as

$$\tilde{i}_{\mathrm{ph}} = \frac{1}{\sqrt{2}}\hat{i}_{\mathrm{ph}} \quad \text{and} \quad \bar{i}_{\mathrm{ph}} = \frac{2}{\pi}\hat{i}_{\mathrm{ph}}. \tag{2.13}$$

Conduction Losses

The current flowing into one of the cascaded converter cells equals the phase current and flows through two power semiconductors per cell at any instant in time. Assuming here in a first step that the conduction loss characteristics of IGBTs and diodes are the same, the total conduction losses of a phase stack based on power semiconductors with a certain blocking voltage, V_{B}, and a certain rated current, I_{N}, can be calculated as

$$P_{\mathrm{cond}}(V_{\mathrm{B}}, I_{\mathrm{N}}) = 2n_{\mathrm{cell}} \cdot \left(v_{\mathrm{CE},0}(V_{\mathrm{B}}) \cdot \bar{i}_{\mathrm{ph}} + r(V_{\mathrm{B}}, I_{\mathrm{N}}) \cdot \tilde{i}_{\mathrm{ph}}^2 \right), \tag{2.14}$$

where n_{cell} has been given in (2.11). Note that $n_{\mathrm{cell}} \propto 1/V_{\mathrm{B}}$ and hence, since the reduction of the forward voltage drop with the blocking voltage is not very pronounced (cf. Section 2.2.2), high conduction losses must be expected for designs based on lower blocking voltages.

Required Switching Frequency

The required switching frequency (per cell) depends strongly on the number of cascaded converter cells. Let l_{f} denote the filter inductance in per unit, whereby

$$Z_{\mathrm{B}} = \frac{V_{\mathrm{N}}^2}{P_{\mathrm{N}}} = \frac{\tilde{v}_{\mathrm{ph}}^2}{P_{\mathrm{ph}}} = \frac{(V_{\mathrm{N}}/\sqrt{3})^2}{P_{\mathrm{N}}/3} \quad \text{and} \quad L_{\mathrm{B}} = \frac{Z_{\mathrm{B}}}{2\pi f_{\mathrm{g}}} \tag{2.15}$$

are the reference impedance and inductance, respectively. Let further $\delta i_{\mathrm{pp}} = \Delta i_{\mathrm{pp}}/\hat{i}_{\mathrm{ph}}$ denote the allowable maximum relative peak-to-peak ripple of the phase-current. Then, since for a single two-level H-bridge inverter operated with unipolar PWM, where the output frequency of the full-bridge is already twice the device switching frequency, i. e., $f_{\mathrm{s,eff}} = 2 \cdot f_{\mathrm{s}}$, due to interleaved operation of the two bridge legs, the maximum current ripple during a half-period of the grid current occurs when the modulation index is $M = 1/2$. Thus, the required switching frequency for a given maximum peak-to-peak current ripple can be calculated as

$$f_{\mathrm{s,2L}} = \frac{V_{\mathrm{DC,total}}}{8 \cdot L_{\mathrm{f}} \cdot \Delta i_{\mathrm{pp}}} = \frac{V_{\mathrm{DC,total}}}{8 \cdot l_{\mathrm{f}} L_{\mathrm{B}} \cdot \delta i_{\mathrm{pp}} \hat{i}_{\mathrm{ph}}}. \tag{2.16}$$

If more than one cell is connected in series and if phase-shifted PWM [90, 91] is used, the magnitude of the steps in the output voltage (cf. **Fig. 2.1a**) is reduced to $V_{\mathrm{DC,total}}/n_{\mathrm{cell}}$, and the effective switching frequency seen by the filter inductor is increased by a factor of n_{cell} (i. e., to $f_{\mathrm{s,eff}} = 2 \cdot n_{\mathrm{cell}} \cdot f_{\mathrm{s}}$). Therefore, solving

$$\Delta i_{\mathrm{pp}} = \frac{V_{\mathrm{DC,total}}}{8 \cdot L_{\mathrm{f}} \cdot f_{\mathrm{s,2L}}} \stackrel{!}{=} \frac{V_{\mathrm{DC,total}}/n_{\mathrm{cell}}}{8 \cdot L_{\mathrm{f}} \cdot n_{\mathrm{cell}} f_{\mathrm{s}}} \tag{2.17}$$

reveals that the switching frequency *per bridge leg*, f_{s}, that is required to achieve the same current ripple in the same filter inductor is reduced according to

$$f_{\mathrm{s}} = \frac{1}{n_{\mathrm{cell}}^2} \cdot f_{\mathrm{s,2L}}, \tag{2.18}$$

i. e., it decreases with the number of cascaded converter cells *squared*, which is in accordance with the findings reported in [97].

Switching Losses

Each bridge leg in a cell is operated at a fixed switching frequency, f_{s} from above. For normal PWM operation where the ratio between switching frequency and fundamental frequency is quite high, and since a linear dependency between switched current and resulting switching energies is assumed (cf. (2.4)), e. g., the turn-off losses during half a grid period can be estimated based on the bridge leg's average current, $\bar{i}_{\mathrm{ph}}$, as

$$P_{\mathrm{off,leg}}(V_{\mathrm{B}}) = K_{\mathrm{off}}(V_{\mathrm{B}}) \cdot \frac{1}{1000} \cdot \bar{i}_{\mathrm{ph}} \cdot \frac{u}{0.5} \cdot f_{\mathrm{s}}, \tag{2.19}$$

where the factor 1/1000 is required to compensate for the mJ/A unit of K_{off}. Each of the three switching energies is dissipated once per bridge leg during one switching cycle (although not in the same device). The overall switching losses of a phase stack based on power semiconductors with a certain blocking voltage, V_{B}, can thus be calculated from

$$P_{\mathrm{sw}}(V_{\mathrm{B}}) = 2n_{\mathrm{cell}} \cdot \left(K_{\mathrm{sw}}(V_{\mathrm{B}}) \cdot \frac{1}{1000} \cdot \bar{i}_{\mathrm{ph}} \cdot \frac{u}{0.5} \cdot f_{\mathrm{s}} \right), \tag{2.20}$$

with $K_{\mathrm{sw}}(V_{\mathrm{B}}) = K_{\mathrm{off}}(V_{\mathrm{B}}) + K_{\mathrm{on}}(V_{\mathrm{B}}) + K_{\mathrm{rec}}(V_{\mathrm{B}})$ and with f_{s} given in (2.18). Inserting some of the relationships discussed earlier, $P_{\mathrm{sw}}(V_{\mathrm{B}}) \propto V_{\mathrm{B}}^3$ is found, indicating high switching losses for designs employing semiconductors with high blocking voltages.

Optimum Blocking Voltage

The above derivations, especially (2.14) and (2.20), allow to calculate conduction and switching losses and hence the total semiconductor losses of a CHB system as shown in **Fig. 2.1a**, employing IGBT modules with arbitrary blocking voltage ratings. Considering now an example system with a grid voltage of $V_N = 10\,\text{kV}$ (line-to-line), a nominal (three-phase) power of $P_N = 1\,\text{MVA}$ and hence a nominal power of $P_{ph} = 333\,\text{kVA}$ for the phase stack, the blocking voltage utilization is chosen as $u = 0.55$, and the nominal modulation index as $M_N = 0.8$. The filter inductance is set to $l_f = 10\,\%$, and the allowable relative peak-to-peak current ripple to $\delta i_{pp} = 1\,\%$, since the filter inductor current corresponds to the grid current, and therefore strict limits on its harmonic content apply, e. g., IEEE 519 [98].

In order to establish a fair comparison, the total silicon area should be the same for all considered designs. Thus, aiming for a high overall efficiency of above 99 %, for a reference blocking voltage, e. g., for $V_{B,ref} = 1700\,\text{V}$, the target for the relative semiconductor losses is set to $2/3\,\%$ in order to account for additional losses, e. g., in the filter inductor. Solving

$$\frac{P_{cond}(V_{B,ref}, I_N) + P_{sw}(V_{B,ref})}{P_N/3} \stackrel{!}{=} \frac{2}{3} \cdot 0.01 \tag{2.21}$$

for I_N with $V_{B,ref} = 1700\,\text{V}$ results in a required current rating of $I_{N,1700\,V} \approx 150\,\text{A}$. The rated current specified in datasheets is typically such that the nominal loss density in the IGBT chips of a module, i. e., $v_{CE}(I_N) \cdot J_N = v_{CE}(I_N) \cdot I_N / A_{chip}$, does not exceed a limit of, e. g., $150\,\text{W/cm}^2$, resulting in a decrease of the nominal current density, J_N, with increasing blocking voltage [94] (cf. also Section 2.2.2). Hence, the total silicon area used in a design based on these 1700 V/150 A devices is approximately

$$A_{Si,1700\,V} = n_{cell}(1700\,\text{V}) \cdot 8 \cdot \frac{I_{N,1700\,V}}{J_N(1700\,\text{V})}, \tag{2.22}$$

where the factor 8 comes from the fact that there are 4 IGBT/diode combinations per cell, each consisting of two devices (IGBT and diode, where, as stated before, equal characteristics are assumed here). In order to keep the total silicon area constant for all considered blocking voltages, the nominal currents of the devices considered for other blocking voltages can be found using (cf. **Fig. 2.5b**)

$$I_N(V_B) = I_{N,1700\,V} \cdot \frac{n_{cell}(1700\,\text{V})}{n_{cell}(V_B)} \cdot \frac{J_N(V_B)}{J_N(1700\,\text{V})}. \tag{2.23}$$

With I_N defined as a function of V_B such that in all cases the same *total* silicon area is used, the conduction and switching losses of designs based on different blocking voltages can be calculated using (2.14) and (2.20), respectively, which is shown in **Fig. 2.5a**. As expected, conduction losses dominate for designs based on IGBTs with lower blocking voltage ratings, whereas switching losses clearly dominate when devices with higher blocking voltages are employed, because, as a consequence of the lower number of cascaded cells, high switching frequencies are required in order to fulfill the current ripple specification, as can be seen from **Fig. 2.5d**, and because additionally the normalized switching energies increase with the blocking voltage. Therefore, an optimum blocking voltage resulting in lowest overall losses can be identified as (theoretically) 1710 V, where then 10.9 cells would be required. Note that the optimum is quite flat, and hence, considering common blocking voltages, either 1200 V or 1700 V devices should result in lowest overall losses.

The losses generated in the semiconductors must be removed by means of a cooling system, i. e., a heat sink. For each combination of V_B and I_N, the thermal resistance from junction to heat sink per IGBT can be approximated using (2.8). From that, the temperature, T_{hs}, which the heat sink would need to maintain in order to ensure that the devices operate at a junction temperature of $T_j = 125\,°C$, can be calculated as

$$T_{hs} = T_j - R_{th,jh}(V_B, I_N) \cdot \frac{P_{cond}(V_B, I_N) + P_{sw}(V_B)}{8 \cdot n_{cell}(V_B)}, \tag{2.24}$$

including a factor 8 again, since $R_{th,jh}$ is specified per device, i. e., per IGBT or per diode. As can be seen from **Fig. 2.5c**, designs that feature very low losses can tolerate very high heat sink temperatures. This means that a lower total chip area could be used from a loss dissipation point of view, however, while this would increase the thermal resistances from junction to heat sink, $R_{th,jh}$, and hence reduce the allowable heat sink temperature, it would also increase the losses, which is not feasible if an efficiency specification shall be met. In contrast, designs with higher losses require lower heat sink temperatures, implying a larger volume of the heat sink. Note that an increase of the silicon area for designs with higher blocking voltages would enable higher heat sink temperatures, i. e., smaller heat sinks, however, since the losses of these designs are dominated by switching losses, which do not depend on the nominal current (chip area), this measure would not improve the efficiency of these designs significantly. An increase of the total chip area would reduce thermal resistances of the devices and the conduction losses, i. e., slight efficiency improvements could be expected for designs based on

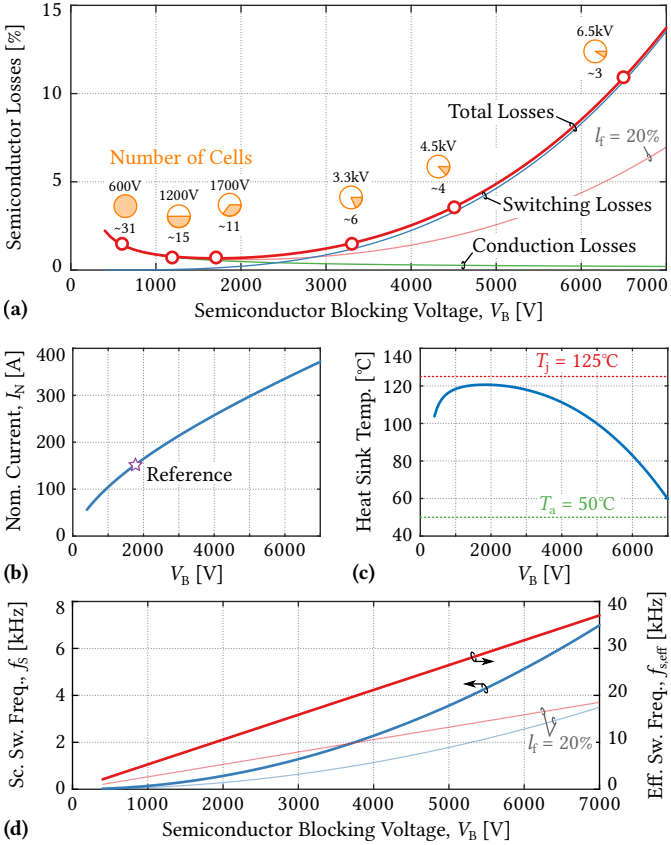


Fig. 2.5: (a) Normalized semiconductor losses as a function of the cells' blocking voltage in a 1 MVA CHB system interfacing a 10 kV grid. The total silicon area is kept constant for all designs, and the required number of cascaded cells is indicated for common IGBT blocking voltages. The main loss curves are for $l_f = 10\,\%$ and $\delta i_{pp} = 1\,\%$, and additionally the total losses for the case of an increased $l_f = 20\,\%$ is shown. **(b)** Nominal device currents for a constant total silicon area as a function of the blocking voltage. **(c)** Heat sink temperature that is required to dissipate the losses indicated in (a) with $T_j = 125\,°C$. **(d)** Required switching frequencies per semiconductor and resulting effective switching frequencies of the output multilevel voltage waveforms, $f_{s,eff} = 2 \cdot n_{cell} \cdot f_s$. Note that $f_{s,eff} \propto V_B$ because $f_{s,eff} \propto n_{cell} f_s \propto n_{cell} \cdot 1/n_{cell}^2 \propto 1/n_{cell} \propto V_B$, as described by (2.18) and (2.11).

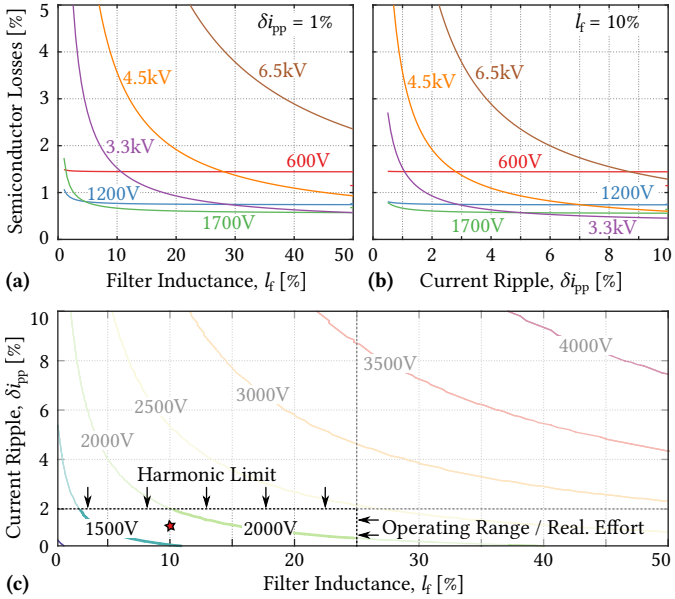


Fig. 2.6: Sensitivity of the semiconductor losses to variations of **(a)** the filter inductance, l_f, and **(b)** the allowable grid current ripple, δi_{pp}; **(c)** corresponding dependence of the optimum blocking voltage on these parameters, where the basic limitations of feasible values are indicated.

lower blocking voltages since these are dominated by conduction losses, and hence the optimum blocking voltage would be shifted to slightly lower values (cf. also **Fig. 2.7**). On the other hand, for designs based on higher blocking voltages only the cooling would be simplified, whereas the losses would not be reduced significantly.

Fig. 2.6a and **b** illustrate the sensitivity of the semiconductor losses on the relative filter inductance, l_f, and on the allowable relative current ripple, δi_{pp}. It can be seen that designs employing devices with lower blocking voltages do not benefit from an increase of either of these parameters, because the required switching frequencies are anyway low as a result of the high number of voltage levels (cf. also **Fig. 2.5d**), and hence these designs are dominated by conduction losses. If these are low, the switching frequencies could be increased, which would increase the semiconductor losses, but on the other hand allow to reduce the size of the filter inductor and potentially its losses, and hence

favorably affect the total system losses and/or volume. In contrast, designs based on devices with higher blocking voltages benefit from an increased filtering effort and/or current ripple, because lower switching frequencies can be used (cf. again **Fig. 2.5d**), thereby reducing the total semiconductor losses. Such an increase of the filter inductance or the current ripple corresponds to a shift of the optimum blocking voltage towards higher values, as can be seen in **Fig. 2.6c**. Note, however, that an increase of the current ripple is constrained by harmonic limits, and that an increase of the filter inductance is constrained by output voltage capability requirements, as will be discussed later, and also by the realization effort of the inductor, resulting in comparatively low values of the optimum blocking voltage.

Thus, changes of the filter inductance value affect the losses in the semiconductors (and hence the optimum blocking voltage) but also losses in the filter inductor itself, and, through the size of the required heat sinks and the size of the inductor, also the power density, ρ, of the system, which is another interesting performance characteristic in addition to the efficiency, η. Furthermore, a frequency-independent current ripple specification is a simplification only, since current harmonics are limited by standards such as IEEE 519 [98], which consider a variation of the limits with frequency. A detailed treatment of these aspects is beyond the possibilities of the simplified analytic analysis presented here, and will therefore be addressed comprehensively by means of an efficiency versus power density $\eta\rho$-Pareto optimization in Section 2.3.

2.2.4 Optimum Blocking Voltage for Other Grid Voltages

The above calculations can be repeated for grid voltages other than the 10 kV considered so far. The phase current is kept constant while the grid voltage (and hence the required number of cells, etc.) is varied, thereby scaling the system power proportionally to the grid voltage. The devices' current rating is kept constant, and therefore the same chip area is used for all designs at a given grid voltage. Also, the filter inductance value in per unit is kept constant, i. e., the actual inductor value, L_f, scales with the nominal power and the grid voltage.

Fig. 2.7 shows the optimum blocking voltage for a wide range of grid voltages, considering $l_\mathrm{f} = 10\,\%$ and $\delta i_\mathrm{pp} = 1\,\%$. Each of the common IGBT blocking voltages suits a certain range of grid voltages best. Note, however, that the optima are quite flat (cf. **Fig. 2.5**), and that a variation of l_f and/or δi_pp might shift these optima as indicated by **Fig. 2.6**. Furthermore, an increase of the total chip area, i. e., of $I_{\mathrm{N},1700\,\mathrm{V}}$ from above, lowers the optimum blocking

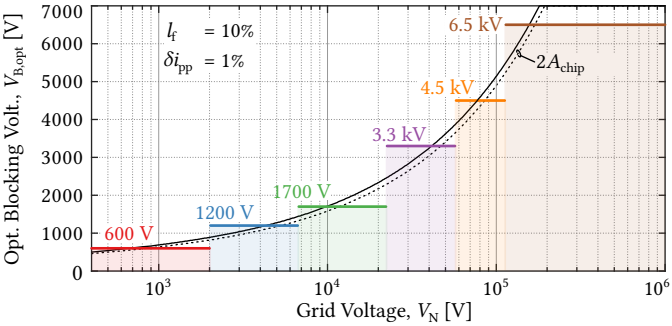


Fig. 2.7: Optimum blocking voltage as a function of the grid voltage (line-to-line); the theoretical curve is overlaid by bars indicating the most suitable IGBT voltage rating. The results consider $l_f = 10\,\%$ and $\delta i_{pp} = 1\,\%$. The optimum blocking voltage is slightly lowered if the available silicon chip area is doubled.

voltage for a given grid voltage, because the trade-off between conduction and switching losses is shifted in favor of conduction losses as discussed above, allowing to use more cascaded cells and hence lower blocking voltages for a given grid voltage.

2.2.5 The Silicon Multilevel Limits

For (unipolar) power semiconductor technology, diagrams showing the achievable specific on-state resistance versus the device blocking voltage on a log-log scale are used to indicate material and technology limits. By expressing the losses of a cascaded cells system as an equivalent normalized loss resistance,

$$r_{eq} = \frac{R_{eq}}{Z_B} = \frac{P_{cond} + P_{sw}}{\tilde{i}_{ph}^2} \cdot \frac{1}{Z_B}, \tag{2.25}$$

a similar diagram can be plotted in **Fig. 2.8**, showing the achievable r_{eq} for each blocking voltage as a function of the grid voltage. Note that the region where a certain blocking voltage provides the lowest r_{eq} coincides with the corresponding bar indicated in **Fig. 2.7**.

Here, in contrast to the initially mentioned semiconductor technology limit diagram, *two* different limits can be identified. Note that again l_f and δi_{pp} are fixed, and that the same total chip area is used for all designs at a given grid voltage. Then, there is a switching loss limit for low grid voltages, because for a given blocking voltage the number of required cells becomes

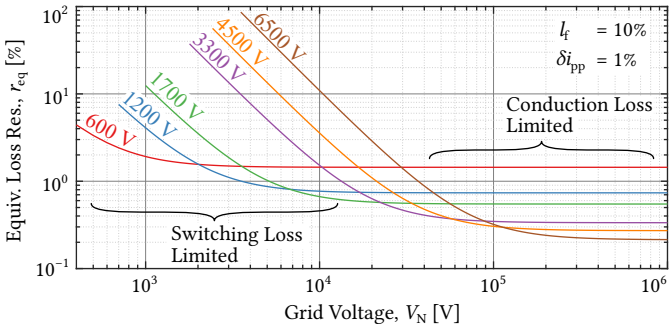


Fig. 2.8: Semiconductor losses expressed as an equivalent loss resistance, r_{eq}, for $l_f = 10\,\%$ and $\delta i_{pp} = 1\,\%$, showing the silicon multilevel limits, i. e., the switching loss limited region and the conduction loss limited region.

small and hence the required switching frequency increases. For a given filter inductance, the switching loss limit can be overcome by choosing a design with a *lower* blocking voltage and hence more cascaded cells that can operate at a lower switching frequency. On the other hand, there is a conduction loss limit when higher grid voltages are considered. Then, the number of cells is high and hence the required switching frequency and the switching losses are low. The conduction loss limit can thus be overcome by choosing a design with a *higher* blocking voltage and hence fewer cascaded cells. Note, however, that the conduction loss limit is a consequence of the voltage drop across the semiconductor junction of the bipolar power semiconductors considered here, i. e, $v_{CE,0}$. In case of unipolar devices such as MOSFETs, using more cells with a lower blocking voltage results in theory in lower conduction losses, also if the total chip area is kept constant [99], because the specific on-state resistance of MOSFETs scales roughly as $r_{on} \propto V_B^{2.5}$ [93].

2.3 $\eta\rho$-Pareto Optimization of the Number of Cascaded Converter Cells

As has been discussed in the previous section, the trade-off between switching and conduction losses is affected by the choice of the filter inductance, which is a passive component showing both, losses and, as a second characteristic, a considerable volume that affects the system's power density. Also, the cooling system required to maintain the semiconductor junction temperature at the

Tbl. 2.3: Number of cascaded cells and semiconductor blocking voltage utilization for $V_{\mathrm{DC,total}} = 10.3\,\mathrm{kV}$, and nominal currents, I_{N}, corresponding to a constant total chip area among the designs, where $I_{\mathrm{N},1700\,\mathrm{V}} = 150\,\mathrm{A}$ serves as reference.

V_{B}	n_{cell}	u	I_{N}	V_{B}	n_{cell}	u	I_{N}
600 V	29	0.592	81 A	3300 V	6	0.520	217 A
1200 V	15	0.572	124 A	4500 V	4	0.572	292 A
1700 V	11	0.551	150 A	6500 V	3	0.528	343 A

assumed $T_{\mathrm{j}} = 125\,^{\circ}\mathrm{C}$ contributes a volume that depends on the losses to be removed from the power modules. To include both of these dimensions, efficiency *and* power density, and their mutual coupling, into the determination of the optimum number of cascaded cells, a multi-objective efficiency versus power density $\eta\rho$-Pareto analysis of the CHB system shown in **Fig. 2.1a** is performed in the following.

2.3.1 System Modeling and Optimization Procedure

As indicated in **Fig. 2.1**, the grid voltage (line-to-line) of the considered example system is $V_{\mathrm{N}} = 10\,\mathrm{kV}$ and the nominal (three-phase) power is $P_{\mathrm{N}} = 1\,\mathrm{MVA}$. Note that due to the phase-modular nature of the three-phase configuration it is sufficient to confine the analysis to one phase stack with a nominal power of $P_{\mathrm{ph}} = 333\,\mathrm{kVA}$.

Blocking Voltage Utilization and Number of Cells

The analytic discussion before indicated that the optimum blocking voltage would be 1710 V, corresponding to 10.9 cascaded cells. However, in reality of course IGBT modules are only available with discrete blocking voltages, and only an integer number of cascaded cells can be used. Hence, if the blocking voltage utilization, u, was set to the equal value for all blocking voltages, the total DC link voltages would differ between the designs, and hence their output voltage capabilities would be different. Therefore, the total DC link voltage is set to be equal for all designs according to (2.10) with $M_{\mathrm{N}} = 0.8$, resulting in $V_{\mathrm{DC,total}} = 10.3\,\mathrm{kV}$. Then, the number of cascaded cells featuring devices with a certain blocking voltage is chosen such that the blocking voltage utilization lies within $u = 0.55 \pm 0.05$. **Tbl. 2.3** shows the resulting number of cascaded cells and utilizations for the considered blocking voltages.

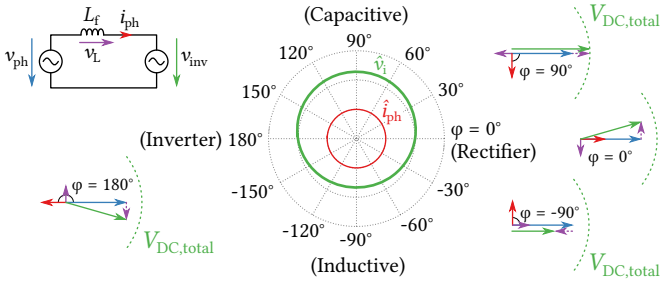


Fig. 2.9: Dependence of the required inverter output voltage amplitude, $\hat{v}_i = M \cdot V_{DC,total}$, on the phase angle between voltage and current, φ. The capacitive operating point ($\varphi = 90°$) limits the maximum feasible filter inductance, L_f, for a given total DC voltage.

Filter Inductance Value

Fig. 2.9 shows a fundamental frequency equivalent circuit of the phase stack, comprising the grid phase voltage, v_{ph}, the filter inductance, L_f, and the inverter voltage, v_{inv}, (i. e., the output voltage generated by the cascaded cells phase stack). Considering a constant phase current amplitude, the required inverter voltage amplitude varies with the power factor, i. e., with the phase angle between the phase voltage and the phase current, because of the voltage drop across the filter inductance, v_L. As can be seen in **Fig. 2.9**, the worst-case operating point, i. e., the highest inverter voltage amplitude requirement, occurs in the capacitive case ($\varphi = 90°$). Since the inverter voltage is limited by the total DC voltage, i. e., $\max(\hat{v}_{inv}) \leq M_{max} \cdot V_{DC,total}$, there is an upper limit for the filter inductance, L_f. If the capacitive operating point should be reachable at nominal current and $M_{max} = 1$, the filter inductance is constrained by

$$L_f \leq L_{f,max} = \frac{V_{DC,total} - \sqrt{2/3}V_N}{2\pi f_g \hat{i}_{ph}} \approx 26.1\,\%\,\text{pu}. \tag{2.26}$$

Filter Inductance Modeling

The losses and the volume of a filter inductor with a certain inductance, L_f, and stressed by a certain phase current, i_{ph}, are obtained from a local $\eta\rho$-Pareto optimization, which sweeps the dimensions of the inductor's core as well as the number of turns over wide ranges to obtain a large number of inductor designs.

For each of these inductor designs, winding losses are calculated for round solid copper wires, neglecting HF losses in the winding, which is a feasible approximation since the inductor current equals the grid current, where harmonics above 1 kHz are limited to below 1 % by IEEE 519 [98], i. e., the squares of the RMS current components at frequencies above 1 kHz are limited by $i^2_{\mathrm{rms}}(f > 1\,\mathrm{kHz}) < (0.01)^2 \cdot i^2_{\mathrm{rms}}(f_{\mathrm{g}}) = 0.0001 \cdot i^2_{\mathrm{rms}}(f_{\mathrm{g}})$. Therefore, even if the AC resistance at the harmonic frequencies would be a factor of 100 larger than at the fundamental (grid) frequency, the loss contribution of the current harmonics would be below $0.0001 \cdot i^2_{\mathrm{rms}}(f_{\mathrm{g}}) \cdot 100 \cdot R_{\mathrm{AC}}(f_{\mathrm{g}}) = 0.01 \cdot i^2_{\mathrm{rms}}(f_{\mathrm{g}}) \cdot R_{\mathrm{AC}}(f_{\mathrm{g}})$, i. e., only around 1 % of the losses at the grid frequency.

Core losses are calculated for laminated silicon steel cores (M165-35S material). HF core losses are considered using the iGSE approach [100], because the core losses of this type of material are quite sensitive to flux components at high-frequencies.

The thermal limit is observed by assuming a surface heat transfer coefficient of 15 W/(m²K) (typical value for natural convection in air [101]), an ambient temperature of 50 °C, and a maximum allowable surface temperature of 100 °C. Designs that generate losses that cannot be dissipated under these conditions are discarded. Also, all designs that cannot carry twice the rated current without saturation of the core are discarded in order to ensure that the inductor can contribute to current limiting during fault situations, e. g., overcurrent or grid overvoltage surges [102].

Finally, four designs from the resulting $\eta\rho$-Pareto front of the inductor are chosen: the most efficient one, the one with the highest power density, and two trade-off designs which are identified by allowing for a 25 % volume increase over the smallest design and then selecting the most efficient one within this volume range, or by allowing for a 25 % loss increase over the most efficient design and then selecting the smallest one within this efficiency range, resulting typically in designs close to the “knee” of the Pareto front.

Semiconductor Losses

The losses of the power semiconductors are calculated using either virtual devices for a certain V_{B} and I_{N} rating as discussed in the previous section, where I_{N} can again be chosen such that the total silicon area is equal for all designs, leading to the values shown in **Tbl. 2.3**. Alternatively, it is also possible to directly use datasheet conduction loss and switching loss characteristics of specific devices. Note that here, in contrast to the analytical approach described in the previous section, the losses of the IGBTs and diodes are calculated individually, i. e., separate loss models are used for IGBTs and diodes,

whereby the device currents of a specific converter cell can be obtained from the phase current and the modulation function.

Heat Sink Modeling

To remove these losses from the semiconductors and to ensure a junction temperature of $T_\mathrm{j} = 125\,°\mathrm{C}$, appropriate heat sinks are required. Considering a single heat sink per cell, the thermal resistances from junction to heat sink of the individual power devices, i. e., IGBTs and diodes, obtained from the models discussed in Section 2.2, $R_{\mathrm{th,jh,i}}$, together with the individual losses, $P_{\mathrm{loss,i}}$, allow to calculate the maximum allowable heat sink temperature as

$$T_{\mathrm{hs,max}} = \min_{\mathrm{i}}(T_\mathrm{j} - P_{\mathrm{loss,i}} \cdot R_{\mathrm{th,jh,i}}). \tag{2.27}$$

The Cooling System Performance Index (CSPI) [103], which characterizes the capability of certain cooling methods in terms of power dissipation capability per volume and temperature difference, i. e., $[CSPI] = \mathrm{W/(K\,dm^3)}$, is then used to estimate the volume of the heat sink according to

$$V_\mathrm{hs} = \frac{1}{CSPI \cdot R_{\mathrm{th,hs}}} \quad \text{with} \quad R_{\mathrm{th,hs}} = \frac{T_{\mathrm{hs,max}} - T_\mathrm{a}}{\sum_\mathrm{i} P_{\mathrm{loss,i}}}, \tag{2.28}$$

where T_a denotes the ambient temperature (50 °C). For a typical forced air cooling system, $CSPI = 10\,\mathrm{W/(K\,dm^3)}$, is assumed here [103]. If for a certain design the required $R_{\mathrm{th,hs}}$ becomes negative due to excessive losses, the design is discarded.

DC Link Capacitors

The DC link capacitances of the converter cells are chosen such as to result in a peak-to-peak voltage ripple of 10 %. This is mainly a ripple at twice the grid frequency, because the difference between the AC-side power that is $\propto \sin^2(2\pi f_\mathrm{g} t)$ and the DC-side power, which is constant, needs to be buffered. Note that therefore the total energy buffering capability of a phase stack at twice the grid frequency does not depend on the number of cells, while of course additional current components at the respective switching frequency might cause slight differences in the capacitance requirements for designs based on different blocking voltages. The capacitor current of a specific cell can be calculated from the phase current, the modulation function and the (constant) DC current, which leads directly to the required capacitance value for a given voltage ripple criterion.

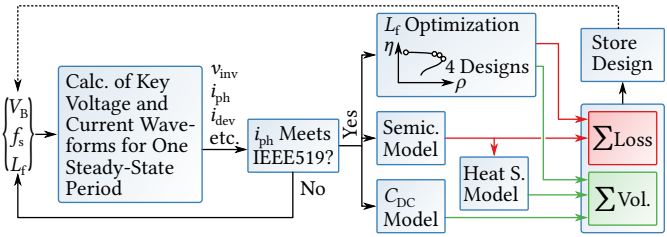


Fig. 2.10: Flowchart illustrating the optimization procedure used to calculate many design points allowing for the $\eta\rho$-Pareto fronts in **Fig. 2.11a** to be extracted. The component models and the overall optimization procedure are described in Section 2.3.1.

The capacitor volume is then estimated from the capacitance value and the DC voltage by assuming a constant volume per stored energy of 6.3 cm^3/J, which has been found by averaging datasheet values of polypropylene foil capacitors of various capacitance and voltage ratings (600 V to 1300 V), and from different manufacturers. This value corresponds to an energy density of 0.16 J/cm^3, which is in agreement with data reported in [104].

Optimization Procedure

Considering here again full-load operation in AC-DC rectifier mode with unity power factor, for each of the common IGBT blocking voltage values, V_B, the cell switching frequency, f_s, and the filter inductance, L_f, are swept over wide ranges (200 Hz...30 kHz and 1 µH...80 mH $< L_{f,max}$, respectively). As illustrated by **Fig. 2.10**, for each tuple $\{V_B, f_s, L_f\}$, the main converter waveforms can be numerically calculated for one steady-state period at full-load operation, whereby PWM with phase-shifted carriers [90, 91] is considered. The superposition of the switched AC output voltage waveforms of all converter cells yields together with the grid voltage and the filter inductor the output phase current. If a design's phase current spectrum does not comply with IEEE 519, the design is discarded. Else, the loss and volume contributions of the main components are calculated as described above, resulting in an efficiency, η, and a power density, ρ for each $\{V_B, f_s, L_f\}$. The power density is obtained from the sum of the main component volumes, and is then scaled with a factor $C_p = 0.7$ in order to account for spacing between components, etc., as suggested in [89].

Tbl. 2.4: Effective switching frequencies of the output voltage waveforms for different bridge leg switching frequencies, f_s (cf. **Fig. 2.11a**). Note that $f_s = 500\,\text{Hz}$ is not feasible for the 6.5 kV designs, because the filter inductance, L_f, is limited.

V_B	n_{cell}	I $f_s \approx 500\,\text{Hz}$	II $f_s \approx 1\,\text{kHz}$	III $f_s \approx 2\,\text{kHz}$
600 V	29	29 kHz	58 kHz	116 kHz
1200 V	15	15 kHz	30 kHz	60 kHz
1700 V	11	11 kHz	22 kHz	44 kHz
3300 V	6	6 kHz	12 kHz	24 kHz
4500 V	4	4 kHz	8 kHz	16 kHz
6500 V	3		6 kHz	12 kHz

2.3.2 Pareto Optimization Results and Discussion

Each $\{V_B, f_s, L_f\}$ combination can be plotted as a point in the $\eta\rho$-plane and these points can then be grouped by blocking voltages to obtain the Pareto fronts shown in **Fig. 2.11a**, where, as in the analytic calculations in the previous section, virtual semiconductors with rated currents, I_N, corresponding to equal total silicon areas for all designs have been considered to model the semiconductor losses. The current ratings are therefore obtained with (2.23), where the $v_{CE}(I_N)$ characteristics of IGBTs and a reference design employing 1700 V semiconductors with $I_{N,1700\,V} = 150$ A are considered. **Tbl. 2.3** shows the resulting current ratings for all blocking voltages.

All in all, the outcome of the Pareto optimization indicates that designs based on 1200 V or 1700 V devices offer the most suitable trade-off between efficiency and power density for the considered system, whereas designs based on devices with higher blocking voltages are not competitive. This confirms the results from the analytical considerations of the previous section.

The shape of the Pareto fronts can be explained as follows: Starting from very low power densities, an increase of the switching frequency allows to reduce the inductance and hence the size of the filter inductor while still meeting the current harmonic limits. As the switching frequency increases, so do the switching losses, causing the efficiency to decrease, which is much more pronounced for higher blocking voltages, because both, the required switching frequencies (lower number of cells) and the normalized switching energies are higher. For lower blocking voltages, the efficiency does not

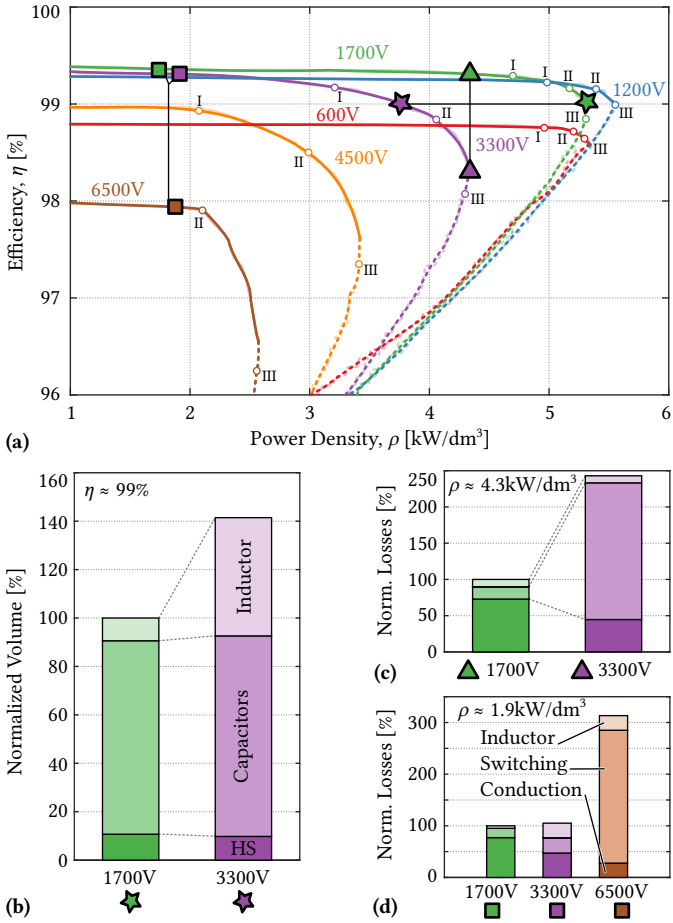


Fig. 2.11: (a) Results of the $\eta\rho$-Pareto optimization of a 1 MVA system (operating in AC-DC rectifier mode with unity power factor) connected to a 10 kV grid, based on virtual IGBT modules with current ratings, I_N, according to **Tbl. 2.3**, i. e., with equal total silicon areas for all designs. Approximate device switching frequencies are indicated by I → 500 Hz, II → 1 kHz, and III → 2 kHz; **Tbl. 2.4** shows the resulting effective switching frequencies of the multilevel output voltages. In addition, **(b)** shows the component volume distribution of two designs based on 1700 V and 3300 V IGBTs, respectively, which both feature the same efficiency of $\eta = 99\,\%$. Similarly, **(c)** shows the loss distribution of a 1700 V and a 3300 V design featuring the same power density (the maximum power density achievable with 3.3 kV IGBTs). Finally, **(d)** shows the loss distribution at a much lower power density, also including a 6.5 kV design.

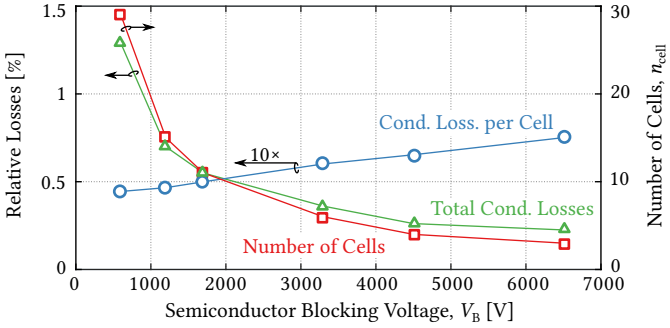


Fig. 2.12: Conduction losses per cell and total conduction losses, and number of cells used in the Pareto optimization as a function the blocking voltage. Note that the conduction losses per cell (blue curve) are multiplied by a factor of 10 for better visibility. Even though the losses per cell are increasing with the blocking voltage, the total conduction losses decrease because $n_{\text{cell}} \propto 1/V_{\text{B}}$.

decrease significantly over a wide range of power densities, because these designs are dominated by conduction losses, as can be seen from **Fig. 2.12**, which shows the dependency of the conduction losses on the blocking voltage: For lower blocking voltages the conduction losses *per cell* become lower, but only slightly because bipolar devices are considered, whereas the number of cells increases sharply. Thus, the total conduction losses increase for lower blocking voltages, e. g., to more than 1 % for 600 V designs, which is directly reflected by the Pareto front in **Fig. 2.11a**. Since these losses are independent of the switching frequency, an increase of the filter inductance and thus also the filter inductor size (and hence a decrease of the power density) does simply lead to current harmonics far below the IEEE 519 limits, but cannot significantly improve the system efficiency, which explains the flat shape of the Pareto fronts for designs based on lower blocking voltages. For all designs, the maximum power density point is reached when the decrease of the filter inductance with a further increase of the switching frequency is overcompensated by the increase of the heat sink volume that is required to dissipate the increasing (switching) losses.

To further illustrate these effects, **Fig. 2.11b** shows the volume distributions among the main components of a 1700 V design and a 3.3 kV design which both feature $\eta \approx 99\,\%$. As discussed above, the capacitor volume is similar, and due to the high efficiency the heat sink volume is rather small and almost equal in both designs. However, in order to achieve this high efficiency

with the 3.3 kV design, a very large filter inductor is required to allow a sufficient reduction of the switching frequency and hence the switching losses. This explains the lower power density of the design with higher blocking voltage devices at the same efficiency.

Additionally, **Fig. 2.11c** shows the loss distribution of a 1700 V design and a 3.3 kV design which both feature the same power density of $\rho \approx 4.3\,\mathrm{kW/dm^3}$, corresponding to the maximum power density achievable with designs based on 3.3 kV devices. Whereas the conduction losses are higher in the 1700 V design as discussed above, the switching losses of the 3.3 kV design are significantly higher as a consequence of the high switching frequency that is required to reduce the size of the filter inductor sufficiently. This explains the higher losses of the design with higher blocking voltage devices at the same power density.

Finally, **Fig. 2.11d** shows the loss distributions at a very low power density for a 1700 V, a 3.3 kV and a 6.5 kV design. The 1700 V and the 3.3 kV design achieve a similar efficiency, but by different means: whereas conduction losses dominate in the 1700 V design, the 3.3 kV design shows higher switching losses and higher losses in the filter inductor, which is again a consequence of the higher required switching frequency and/or the increased filtering effort to compensate for the lower number of cells. The 6.5 kV design shows much higher losses due to very high switching losses. Any option to improve the efficiency of designs based on 6.5 kV devices would therefore require higher filter inductance values, which would allow a reduction of the switching frequency. To do so, either the requirement that the capacitive operating point must be achievable at rated current could be relaxed, or, alternatively, the total DC link voltage, and hence the number of cells, could be increased.

Note that for grid-connected systems considerations regarding the protection against overvoltages, e. g., lightning strikes, and against overcurents might require a minimum value of the filter inductance, L_f, to limit fault currents [19, 102]. Such a lower bound on L_f would reduce the maximum achievable power densities, which would affect especially the designs based on low blocking voltages, because these can fulfill the current harmonic criteria with very low filter inductances due to the high number of levels and the high effective switching frequency, resulting in high power densities (cf. also **Fig. 2.11b**). On the other hand, even at lower power densities these designs still provide an efficiency benefit over designs with higher blocking voltages, as can be seen in **Fig. 2.11c**.

2.3.3 Silicon Carbide Power Semiconductors

Recent developments in SiC technology point in two directions: first, ever higher blocking voltages, exceeding those achievable with Si power semiconductors, are aimed for mainly in prototype devices (cf., e. g., [79, 80]), and second, LV SiC MOSFETs with very low on-state resistances have reached maturity and are available in standard power module packages (cf., e. g., [83–85]). HV SiC devices could allow to reduce the number of cells for a given line voltage or even enable single-cell solutions, and LV SiC devices applied in cascaded converter cells are expected to improve efficiency and power density over systems based on Si IGBTs. The following two subsections are discussing these aspects.

2.3.4 Low-Voltage SiC Power Modules

Significant improvements can be expected from replacing LV Si devices by their SiC counterparts in cascaded cells systems, as it is now possible to obtain suitable SiC power MOSFETs in standard 62 mm packages with very low on-resistances, e. g., 1200 V/13 mΩ [83], 1200 V/5 mΩ [84] or 1700 V/8 mΩ [85]. This motivates an application of the $\eta\rho$-Pareto optimization procedure described in Section 2.3 to designs based on such LV SiC power modules. To account for the higher allowable junction temperatures of SiC devices, $T_{\mathrm{j,SiC}} = 150\,^{\circ}\mathrm{C}$ is considered, and, since SiC devices can cope with higher blocking voltage utilizations [105, 106], $u_{\mathrm{SiC}} \approx 0.7$ is assumed. In addition, the switching frequency search range has been increased up to 100 kHz. The loss characteristics of the SiC semiconductors have been taken directly from the respective datasheets. Because the available SiC power modules are rated at roughly 200 A to 300 A, virtual IGBT modules with nominal currents of 150 A and also of 300 A have been considered for comparison purposes.

Fig. 2.13a shows the resulting Pareto fronts and compares them to the Pareto fronts of the best Si-based designs. It can be seen that both, efficiency and power density of cascaded cells systems can be significantly increased if Si IGBTs are replaced by LV SiC power modules. Considering the same power density, SiC designs show significantly lower losses (cf. **Fig. 2.13b**), which reduces the required heat sink volume. This, in turn, allows for a larger inductor and hence a lower switching frequency in the SiC designs, which, in combination with the superior switching properties, explains the very low switching losses of the SiC design. Note also, that the 1200 V SiC solution has a higher efficiency than the 1700 V SiC solution in the region of dominating conduction losses, which is to be expected for unipolar MOSFET devices,

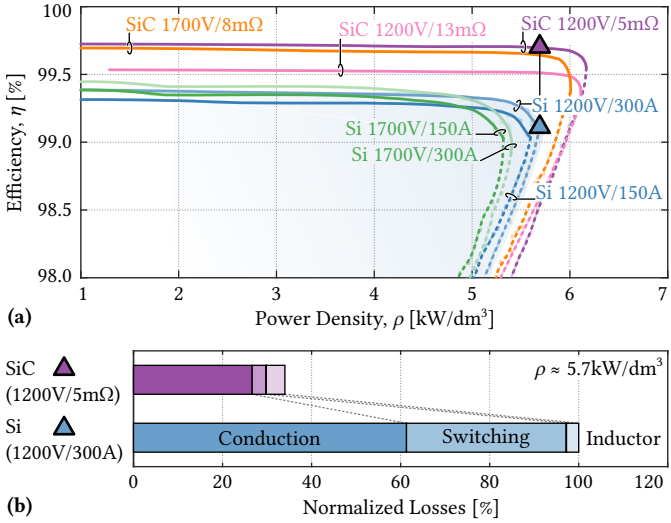


Fig. 2.13: (a) Comparison of Pareto fronts of designs based on Si IGBTs (cf. also **Fig. 2.11**) and SiC power MOSFET modules; **(b)** shows the the loss distribution of a SiC and a Si design featuring the same power density (the maximum power density achievable with Si designs).

where the specific on-state resistance scales roughly as $r_{on} \propto V_B^{2.5}$ [93]. On the other hand, the common-mode ground current issues observed in cascaded cells converter systems (cf. Section 4.2) worsen with increasing dv/dt values, which are typically higher with SiC than with Si devices. This needs to be considered during the converter design, or especially for retrofitting operations.

2.3.5 High-Voltage SiC Devices

The availability of SiC devices with blocking voltages of 15 kV and beyond would in theory allow to interface the 10 kV grid with a single two-level H-bridge converter, i. e., reducing n_{cell} to one. However, as discussed earlier, this is associated with a massive increase of the required switching frequency compared to a multi-cell solution. Therefore, the required switching characteristics which such devices would require in order to be competitive with multi-cell solutions are investigated in the following.

If a given total DC voltage, V_{DC}, is switched by, e. g., four cascaded con-

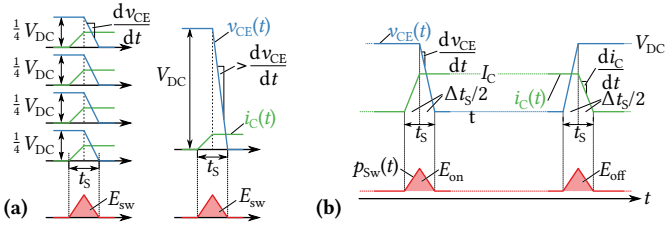


Fig. 2.14: (a) Increase of required dv/dt to obtain equal switching energies in a single-cell system as in a corresponding multi-cell system; **(b)** simplified modeling of turn-on and turn-off losses for the HV SiC devices.

verter cells, the total switching energy that results from the overlap of voltage and current for four switching transitions can be approximated as (cf. **Fig. 2.14a**)

$$E_{sw} = 4 \cdot \left(\frac{1}{4} V_{DC} \cdot I_C \cdot t_s \cdot \frac{1}{2} \right) = \frac{1}{2} \cdot V_{DC} \cdot I_C \cdot t_s, \tag{2.29}$$

where t_s denotes the duration of the switching transition. If the same total DC voltage should be switched by a single HV device such that the same switching energy results, the same switching time, t_s, is required. This, however, corresponds to an increase of the dv/dt by a factor of four (if, as here, the di/dt is assumed to be the same). Furthermore, the four transitions of the multi-cell system would not occur at the same time, but would be phase-shifted with respect ot each other, thereby increasing the effective switching frequency and reducing the magnitude of the voltage steps seen by the filter inductor as discussed earlier. If the single-cell design should provide the same switching *losses*, it therefore would need to achieve even shorter switching transitions and hence higher dv/dt (and di/dt) to compensate the high required switching frequency if the same filter inductor and the same current ripple limit would be considered as in the multi-cell case.

The switching characteristics of a HV SiC device are approximated in dependence of the total switching duration, t_s, as shown in **Fig. 2.14b**, where, taking the example of the turn-off transition, the voltage across the switch rises to the DC voltage, e. g., within $t_s/2$, and where the current decays from its nominal value to zero during the second half of t_s. Therefore, the involved switching characteristics are

$$\frac{di_C}{dt} = \frac{I_C}{t_s/2} \quad \text{and} \quad \frac{dv_{CE}}{dt} = \frac{V_{DC}}{t_s/2}. \tag{2.30}$$

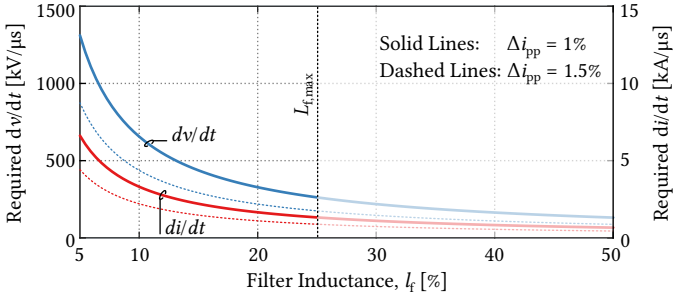


Fig. 2.15: Required dv/dt and di/dt (cf. **Fig. 2.14b**) to obtain relative switching losses of 0.5 % with a single-cell HV SiC solution as a function of the filter inductance and for two different current ripple limits. $L_{f,max}$ is the maximum allowable inductance value if the pure capacitive operating point must be achievable with rated current and $V_{DC,total} = 10.3\,kV$.

Assuming $E_{off} = E_{on} = E_{sw}$ as indicated in **Fig. 2.14b**, the total switching losses of the single-cell solution can be approximated as

$$P_{sw} = 4 f_{s,2L} \cdot E_{sw} = 4 f_{s,2L} \cdot \frac{1}{2} t_s \bar{i}_{ph} V_{DC}, \tag{2.31}$$

where the required switching frequency, $f_{s,2L}$, can be calculated with (2.16). Thus, by defining a switching loss budget of 0.5 %, the required switching characteristics in terms of t_s, and thus di/dt and dv/dt, can be calculated directly, whereby the results depend on the filter inductance and the inductor current ripple limit.

Fig. 2.15 shows that extreme dv/dt and di/dt values ranging up into the MV/µs range would be required—while 0.5 % switching losses corresponds already to a similar efficiency as can be achieved with Si multi-cell solutions, *including* also conduction and inductor losses (cf. **Fig. 2.11**). Note also, that for example a dv/dt of 1 MV/µs would result in common-mode current peak values of 10 A even for a very small common-mode capacitance of 10 pF, clearly indicating that the application of HV SiC power devices would pose significant challenges regarding electromagnetic interference (EMI) filtering, EMI immunity of control and driving circuits, and isolation stress. If, on the other hand, dv/dt values must be limited, the switching energies increase and hence the feasible switching frequencies for a given efficiency target decrease, which must be compensated by a higher filtering effort with an adverse impact on power density.

Although a two-level solution could be designed with very low complexity, especially considering a three-phase system, where also DC capacitance requirements could be reduced when compared to the three individual single-phase stacks, the above considerations clearly indicate that HV SiC technology, at least in the near future, will not supersede the need for cascading converter cells in MV and of course also in HV applications, at least in case a high power density is required.

2.4 Reliability Considerations

The considerations presented in the last sections indicate that designs featuring a comparably high number of cascaded cells achieve favorable performance. However, on the other hand high component counts are generally associated with reduced reliability. This notion is investigated in the following, whereby the calculations are based on a reliability textbook [107] to which the interested reader is referred for more detailed derivations.

2.4.1 Reliability Basics

The reliability of a component can be expressed by its *failure rate*, λ, with $[\lambda] = 1\,\text{FIT} = 1/10^{-9}\,\text{h}$, i. e., 1 FIT corresponds to statistically one failure per one billion hours of operation. In general, the failure rate is a function of time with the typical "bathtub" shape as shown in **Fig. 2.16a**: initially, the failure rate is high as a consequence of production quality fluctuations. These "early failures", however, should be filtered out by manufacturers' quality control measures. During the useful life of a component, the failure rate is approximately constant, which corresponds to a random distribution of failures, e. g. cosmic ray induced failures in power semiconductors. Towards the end of a component's life time, wear-out failures, e. g., bond-wire lift-off or solder delamination as a consequence of thermal cycling and material fatigue, cause the failure rate to increase again. Wear-out failures could be addressed by preventive maintenance measures. Thus, here only the useful life phase is considered, where $\lambda = const$. The failure rate λ_S of a system consisting of several components that all are required to work for the entire system to be operational can be calculated as the sum of the individual components' failure rates, which simplifies to $\lambda_\text{S} = k\lambda$ if k equal components are considered.

The *reliability function*, $R_\text{S}(t)$, expresses the probability that a system with k components (or, e. g., converter cells), each of which having a failure rate of

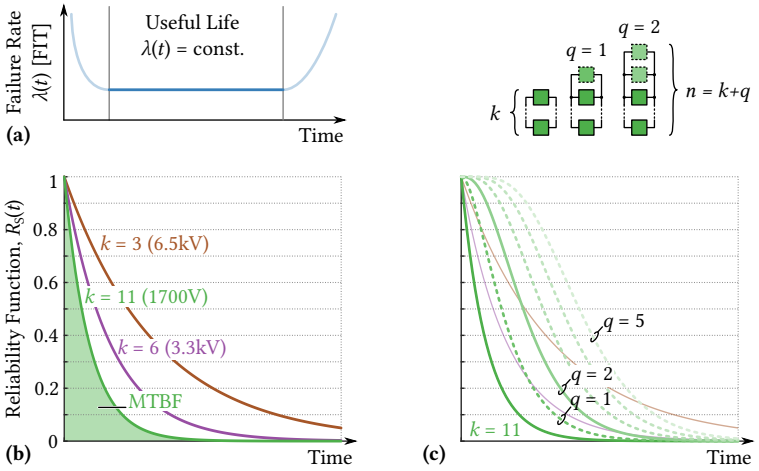


Fig. 2.16: (a) Typical evolution of a component's failure rate over time ("bathtub curve"); **(b)** reliability function in dependence of the number of elements (cascaded cells with equal failure rate per cell), where the system-level $MTBF_S$ is indicated as the area below the reliability function, and **(c)** improvement of the reliability by adding q redundant cells to the k cells strictly required for system operation.

λ, is still operational after t hours:

$$R_S(t) = e^{-k\lambda t}. \tag{2.32}$$

Fig. 2.16b shows the evolution of the reliability function over time for different k. Thus, considering a cascaded cells system with k being the number of cells, the probability that a system is still operational after a certain time decays with the number of cells. The area below the reliability function equals the *mean time between failures* of the system, $MTBF_S$[1], i. e.

$$MTBF_S = \int_0^\infty R_S(t)\,dt \overset{\lambda=\text{const.}}{=} \frac{1}{k\lambda}. \tag{2.33}$$

Because of the modular nature of cascaded cells converter systems, *redundancy* can be implemented by adding q additional cells to the k cells that are strictly required for the system to be operational (i. e., to provide enough

[1]The term $MTBF$ usually refers to systems that are repaired; else, the term $MTTF$ (mean time to failure) is used. However, since both cases are looked at here, only the term $MTBF$ is used to improve readability.

total DC voltage). Such a configuration features then a total of $n = k + q$ cells, and is called *k-out-of-n-redundant*, because it remains operational as long as k out of n cells are operational. Adding redundant cells to a system improves the reliability, as can be seen from **Fig. 2.16c**, and is therefore a mighty tool to alleviate the impact of a high component count on the system reliability, as has been discussed already in the 1990ies for the case of paralleled converter cells [108] and later also for series/parallel structures [109]. In the following, the concept is applied to the cascaded cells system discussed in this section, whereby also the cost of adding redundant converter cells is taken into account.

2.4.2 Reliability of Multi-Cell Systems with Redundancy

There are two different variants of how k-out-of-n redundancy can be implemented on the system level, i. e., with k and n referring to entire converter cells, each of which having a cumulative failure rate of λ_{cell}: standby redundancy and active redundancy with load sharing, which will be described in detail after an initial discussion of the cell failure rate, λ_{cell}.

A converter cell contains parts whose failure rates can be assumed to not depend on the blocking voltage, e. g., control electronics, and other components whose failure rates do depend on the blocking voltage. Especially the power semiconductors are falling in this category, since the required semiconductor chip area for the same rated current depends on the blocking voltage (cf. Section 2.2.2) and the failure rate, in turn, depends on the chip area [87]. Therefore, the cumulative failure rate of a cell is modeled to contain a constant part and a part that depends on the blocking voltage according to

$$\lambda_{\text{cell}}(V_{\text{B}}) = \lambda_{\text{B}} \cdot (a + b \cdot f(V_{\text{B}})) \quad \text{with} \quad a + b = 1, \tag{2.34}$$

where, to account for the dependency of the required chip area on the blocking voltage,

$$f(V_{\text{B}}) = \frac{v_{\text{CE}}(V_{\text{B}})}{v_{\text{CE}}(1700\,\text{V})}, \tag{2.35}$$

if the base fit rate, λ_{B}, and the parameters a and b are specified for a 1700 V design. Note that for reasons of simplicity this implies the same nominal currents for all modules.

To give an impression of the order of magnitude of a numerical value for λ_{B}, typical failure rates for one IGBT module are between 10 FIT and 100 FIT, depending on the operating conditions such as the blocking voltage utilization, and the altitude above sea level due to increased cosmic ray activity,

etc. [86,87]. Note that according to field experience information from industry, the failure rate of a combination of an IGBT module and its gate drive unit is dominated by the power module, not the gate drive unit. Considering entire converter cells, [110] reports 1000 FIT for a modular multilevel (M2LC) converter cell containing one 1700 V IGBT module, a DC link capacitor and control electronics. However, it must be highlighted that λ_B cancels out in the comparative results derived in the following and hence the actual value assumed for λ_B is not important.

Standby Redundancy

In this case, the q redundant cells are not active but simply in a ready state, which would allow them to immediately start taking over the power and voltage shares of a failing cell. Since in this reserve state the cells' stress level is significantly lower compared to that of cells in operation, the failure rate in the reserve state is assumed to be zero. Under these conditions, the $MTBF_S$ for the complete system (i. e., one phase stack) is given by

$$MTBF_S = \frac{n-k+1}{k\lambda_{cell}(V_B)}. \tag{2.36}$$

Since $n-k=q$ is the number of reserve cells, the $MTBF_S$ increases with the amount of reserve cells (cf. also **Fig. 2.16c**). However, adding additional cells to a system, i. e., additional power processing capability that is not utilized during normal operation, is associated with costs. Therefore, **Fig. 2.17** shows the normalized $MTBF_S$ versus the additionally installed power capability for systems based on different blocking voltages and hence different numbers of required cells, k. Note that $MTBF_S \propto 1/\lambda_{cell}(V_B) \propto 1/\lambda_B$ and that therefore λ_B cancels out when the $MTBF_S$ values are normalized—the results shown in **Fig. 2.17** do not depend on λ_B.

Consider the highlighted designs based on 1700 V and 3.3 kV devices, respectively. If about the same additionally installed power capability is considered, *two* additional cells can be added to the 1700 V design, whereas only *one* spare cell can be added to the 3.3 kV design—resulting in comparable $MTBF_S$ values for both configurations, even though the 1700 V design features almost twice as many converter cells.

To indicate the sensitivity on the distribution between constant and blocking-voltage dependent parts of the cells' failure rates, results for three different combinations of a and b are shown in **Fig. 2.17a** ($a=1, b=0$), **b** ($a=0.5, b=0.5$) and **c** ($a=0, b=1$). Although there is an impact, the general conclusion that with similar additionally installed power capability also

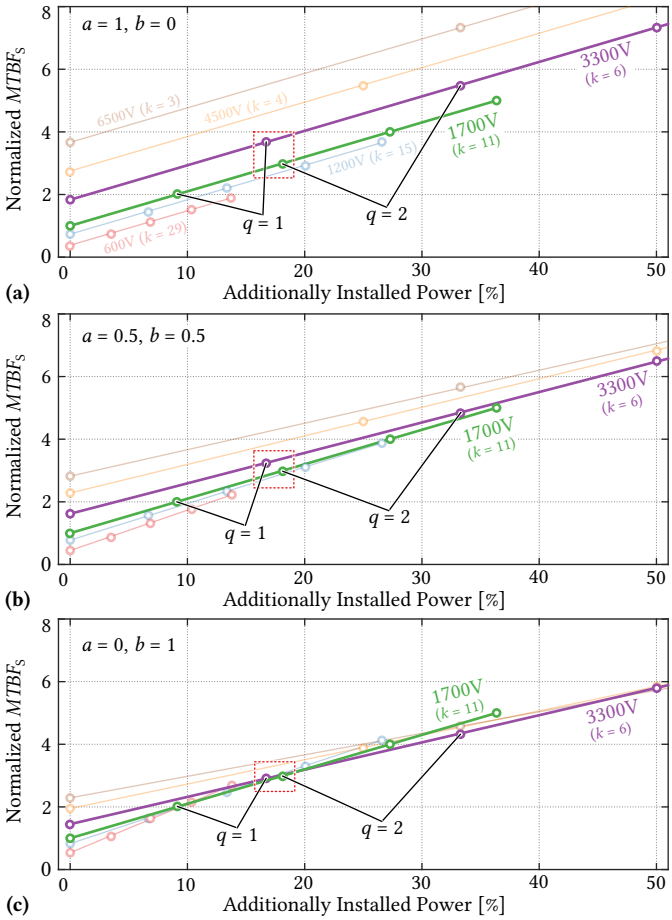


Fig. 2.17: Standby redundancy: $MTBF_S$ (normalized to the 1700 V design without redundancy) versus additionally installed power capability for different blocking voltages (and therefore different numbers of required cells, k). **(a)** considers a constant failure rate per cell ($a = 1, b = 0$), **(b)** a 1:1 distribution between a constant and a blocking-voltage dependent part of the cells' failure rates ($a = 0.5, b = 0.5$), and **(c)** only a blocking-voltage dependent part ($a = 0, b = 1$).

similar $MTBF_S$ values can be achieved, regardless of the actual number of cascaded cells, remains valid, especially considering that the case ($a = 1, b = 0$), i. e., no dependency of λ_{cell} on the blocking voltage, is rather optimistic, since it seems a reasonable assumption that a cell featuring higher blocking voltage devices and hence also a higher power rating typically would also show a higher complexity and hence a higher failure rate.

Active Redundancy with Load Sharing

Instead of keeping the reserve cells in a waiting state, they could also participate in the system operation, which would reduce the power processed per cell, and hence reduce the stress level of all cells, but on the other hand increase the number of cells experiencing this reduced stress. The failure rate of the reserve cells is thus not zero anymore, but equal to that of all the other cells. In addition, the failure rate of the cells depends on how many cells are still operational and share the total stress.

According to [111], the temperature-dependency of the semiconductors' failure rates can be expressed as

$$\lambda(T_j) = \lambda_{100\,°C} \cdot \pi_{T,i} \quad \text{with} \quad \pi_{T,i} = e^{3480\left(\frac{1}{373} - \frac{1}{T_{j,i}+273}\right)}. \tag{2.37}$$

Since this equation is valid for power semiconductors only, the case $a = 0$ and $b = 1$ is considered here, i. e., it is assumed that a cell's failure rate is dominated by the power module's failure rate, which depends on the blocking voltage as described above. Assuming further as an approximation that the total system losses were not affected by the number of cells involved in the power processing (for the same blocking voltage) and neglecting the semiconductor losses' dependency on the junction temperature, the losses that need to be dissipated by the power semiconductors of each converter cell depend only on the number of active cells. Let i denote the number of defective cells, i. e., $0 \leq i \leq n - k$ while the system is still operational. The junction temperature varies then according to

$$T_{j,i} = T_a + \frac{P_{loss,total}}{n - i} \cdot R_{th,cell}, \tag{2.38}$$

showing an increase with each defective cell, and a maximum, $T_{j,max}$, for $n - i = k$. With that, the equation can be made independent of $P_{loss,total}$ and $R_{th,cell}$,

$$T_{j,i} = (T_{j,max} - T_a) \cdot \frac{k}{n - i} + T_a. \tag{2.39}$$

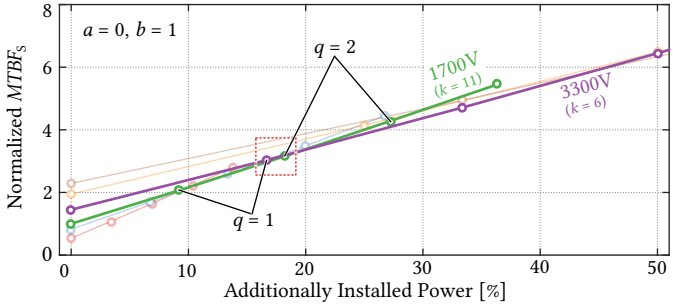


Fig. 2.18: Active redundancy: $MTBF_S$ (normalized to the 1700 V design without redundancy) versus additionally installed power capability, considering only a blocking-voltage dependent failure rate ($a = 0$, $b = 1$).

The system-level mean time between failures becomes then

$$MTBF_S = \sum_{i=0}^{n-k} \frac{1}{(n-i)\lambda_{cell}(V_B)\pi_{T,i}}, \tag{2.40}$$

which is again $\propto \lambda_B$. Therefore, the normalized results shown in **Fig. 2.18** do not depend on the base fit rate, λ_B, either. Comparing the results with those for standby redundancy and $a = 0$ and $b = 1$ in **Fig. 2.17c** reveals only minor differences. Therefore, other factors such as for example the feasibility of immediately bypassing a faulty cell and turning on a reserve cell or, most prominently, the non-optimal number of cascaded cells during the nominal operating state with active redundancy should be carefully taken into account regarding decisions on a redundancy concept.

Additional potential lies in the possibility of not only reducing the thermal stress due to a reduction of the processed power per cell, but also the voltage stress by reducing the cell's DC voltages as long as more cells than required are operational, since the failure rate of power semiconductors depends strongly on the blocking voltage utilization [86, 87]. However, whether this is possible or not depends on the realization of the cells' DC sources or loads. If, e. g., in an SST application (cf. **Fig. 2.1b**) DC-DC converters with a fixed voltage transfer ratio were used (cf. Section 4.1), the cells' DC voltages could not be changed if the LV DC bus voltage must maintain a certain value.

2.4.3 Reliability of Multi-Cell Systems with Redundancy and Repairability

In reality, a faulty cell in a system could be repaired as soon as possible. Depending on the implementation, this can even be possible as a hot-swap operation without service interruption on system level (cf., e. g., [112]). Repairability is an effective means of increasing the availability of systems with a high component count [113]. Again, based on derivations from [107], the $MTBF_S$ value of a repairable system can be calculated from the following relations, which hold for the assumptions of there being only a single repair crew, defective cells being repaired while the system remains operational, and no further failures at system down state (i. e., failures during the restoration time after the complete system has failed), as

$$\begin{aligned} MTBF_{S,0} &= \frac{1}{v_0} + MTBF_{S,1}, \\ MTBF_{S,i} &= \frac{1}{v_i + \mu}\left(1 + v_i MTBF_{S,i-1} + \mu MTBF_{S,i+1}\right), \\ &\qquad \text{for } i = 1, \ldots, n-k-1, \\ MTBF_{S,n-k} &= \frac{1}{v_{n-k} + \mu}\left(1 + \mu MTBF_{S,n-k-1}\right), \end{aligned} \tag{2.41}$$

where

$$v_i = k\lambda_{cell}(V_B) + (n-k-i)\lambda_{cell,reserve}, \tag{2.42}$$

and where μ denotes the repair rate and $\lambda_{cell,reserve}$ is the failure rate for cells in the reserve state. If $\lambda_{cell,reserve} = 0$ is considered (standby redundancy), the approximation

$$MTTF_{S,0} \approx \frac{\mu^{n-k}}{(k\lambda_{cell}(V_B))^{n-k+1}} \tag{2.43}$$

can be used, which illustrates directly that a higher failure rate, λ_{cell}, can be compensated by increasing the repair rate, μ, accordingly.

Note that here λ_B does not cancel out if again a normalization would be used due to the exponent in the denominator of (2.43), and therefore absolute values are given in **Fig. 2.19a**, which shows the $MTBF_S$ versus additionally installed power for the case of a repairable system with standby redundancy and a repair rate of $\mu = 1/(7 \cdot 24\,\mathrm{h})$, corresponding to a mean time to repair ($MTTR$) of one week. A base failure rate of $\lambda_B = 1000$ FIT is assumed (cf. [110]) and $a = 0.5$ and $b = 0.5$ are considered.

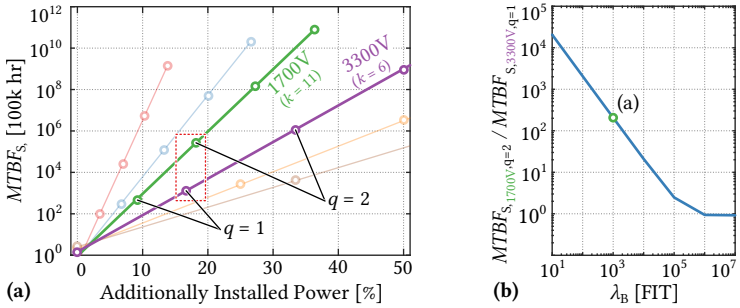


Fig. 2.19: (a) System-level (one phase stack) $MTBF_S$ versus additionally installed power capability considering a repairable system with standby redundancy ($\lambda_B = 1000$ FIT, $\mu = 1/(7 \cdot 24\,\text{h})$, $a = 0.5$, $b = 0.5$) and **(b)** impact of the base failure rate, λ_B, on the ratio between the $MTBF_S$ values of a 1700 V design with $q = 2$ and a 3300 V design with $q = 1$.

In contrast to the non-repairable cases, now the $MTBF_S$ value of the 1700 V design with two spare cells is significantly higher than that of a 3.3 kV design with one spare cell (again with about the same amount of additionally installed power capability). In the first case, after a first cell has failed, *two* more would have to fail before the repair of the first one is completed in order for the complete system to fail, whereas in the second case a single additional failure before completion of the repair leads to a system down state. Under the assumption of independent elements, the latter is much more likely, which corresponds to much lower $MTBF_S$ values. Changing a and b does not alter this conclusion significantly, whereas λ_B affects the ratio between the $MTBF_S$ values of the 1700 V design with two spare cells and the 3.3 kV design with one spare cell as shown in **Fig. 2.19b**. For typical failure rates, the 1700 V solution results in a significantly higher $MTBF_S$, and even for very high λ_B the ratio saturates close to unity.

All in all, the above discussion indicates that reliability considerations are not preventing the decision for designs with higher number of cascaded cells, especially as such designs can be superior regarding efficiency and power density as has been shown in Section 2.3. Furthermore, a modular system design using many cascaded cells allows to lower $MTTR$ figures and thus can help to improve the availability [113], for example by allowing for hot-swapping of defective converter cells against replacements stored on-site during full converter operation [112].

However, it should be kept in mind that with increasing number of re-

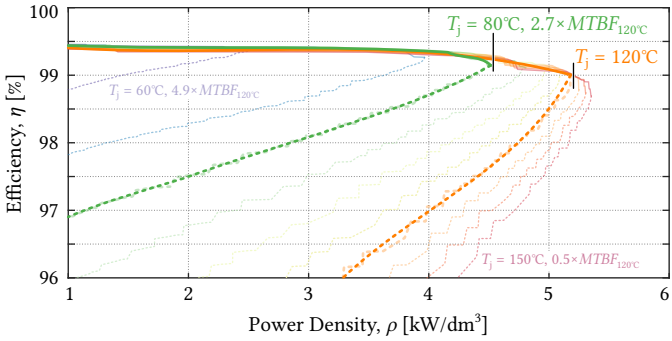


Fig. 2.20: Reliability versus power density trade-off for a design based on 1700 V/150 A IGBTs; no redundancy is considered.

dundant cells the other system components such as the control and communication system, etc., which might not be fully redundant, are effectively limiting reliability, as has been discussed in [110]. Such "reliability bottlenecks" must not be neglected when assessing the benefits of redundancy applied to multi-cell systems. Also, the limitations inherent to reliability figures such as the *MTBF* should be carefully considered during the design of an actual system, which is covered in, e. g., [114] using the example of high-power drive systems. A transition to a physics-based reliability design as proposed in [115] is advisable and in general reliability aspects need to be included in the design process of power electronic systems at an early stage. Approaches to reliability design based on reliability block diagrams and specialized software tools, such as described in, e. g., [116] for aircraft system architectures, could be applied to the design of complex converter systems in order to enable a comprehensive reliability assessment.

2.4.4 Reliability vs. Power Density

As an example of how reliability considerations could be included in the design of a converter system, in the following the trade-off between (semiconductor) reliability and achievable power density is described. It is well known and considered by relevant standards such as [117] and [111] that the reliability of power semiconductors depends on the blocking voltage utilization and the junction temperature, T_j. The latter offers the possibility to improve reliability by increasing the capability of the cooling system, e. g., the size of the heat sinks. According to [111], the semiconductor failure rate at $T_j = 100\,°C$ has to

be scaled by a factor, π_T, to account for different junction temperatures,

$$\lambda(T_j) = \lambda_{100\,°C}\pi_T \quad \text{with} \quad \pi_T = e^{3480\cdot\left(\frac{1}{373}-\frac{1}{T_j+273}\right)}, \tag{2.44}$$

i. e., as an example, $\lambda(T_j = 110\,°C) \approx 1.3 \cdot \lambda_{100\,°C}$. Using the same optimization routine as described in Section 2.3 and considering a real 1700 V/150 A IGBT module (with temperature-dependent loss characteristics from its datasheet [118]), but varying the allowable maximum junction temperature specifications, the $\eta\rho$-Pareto fronts shown in **Fig. 2.20** can be obtained. Each Pareto front is associated with a certain junction temperature, and hence with a certain correction factor, π_T, and a corresponding $MTBF_S$ value. No redundancy is considered here, and thus the value of $\lambda_{100\,°C}$ cancels out when normalizing the $MTBF_S$ values. By reducing the allowable junction temperature, e. g., from 120 °C to 80 °C, the $MTBF_S$ can be increased by a factor of 2.7, however, at the price of a larger heat sink and/or reduced maximum power density. Note also that the lower junction temperatures provide a slight efficiency benefit due to reduced semiconductor losses.

2.5 Summary

Cascaded cells converter systems such as the CHB topology are a very attractive solution to interface power electronic systems to MV applications. The choice of a number of cascaded cells, or, equivalently, of a semiconductor blocking voltage, affects trade-offs between system efficiency, power density, and also reliability aspects, which have been addressed comprehensively in this chapter.

By identifying simple, physics-inspired relationships between the loss-relevant characteristics of IGBT power modules and their blocking voltage and current ratings on the basis of empirical data (i. e., datasheet values), an analytic calculation of the optimum blocking voltage in terms of efficiency can be established, providing further insights on how the number of cells affects conduction and switching losses. The results indicate that 1200 V or 1700 V devices (i. e., 15 or 11 cells per phase stack, respectively) are most suitable for a 1 MVA system connected to a 10 kV grid. A full efficiency versus power density $\eta\rho$-Pareto optimization that includes also the loss and volume contributions of the grid filter inductance and the cooling system confirms that designs based on these blocking voltages offer the most suitable trade-off between efficiency and power density, whereby efficiencies above 99 % are possible at a power density of about 5 kW/dm^3 (considering a ratio of 0.7 between the

sum of the main component volumes and the actual overall boxed volume of the system) are achievable.

Since recent advances in SiC power semiconductor technology have produced devices with very high blocking voltages, it is shown that the switching characteristics that such devices would have to provide in order for a single two-level SiC inverter to be competitive with a Si multi-cell solution would involve extreme switching speeds, posing significant challenges regarding, e. g., EMI and isolation stress. In contrast, multi-cell designs employing LV SiC MOSFET power modules are found to yield significant improvements of both, efficiency and power density, compared to designs based on Si IGBTs. This is a result of the ohmic characteristic of the unipolar SiC devices, which allows to, in theory arbitrarily, reduce the conduction losses by increasing the chip area. Furthermore, the lower normalized switching energies of SiC devices allow for an increase of the switching frequencies and hence a further reduction of the filter inductor size, corresponding to higher power densities, at least if protection considerations do not set a lower bound for the filter inductance. It is therefore expected that even with a future emergence of high voltage SiC devices on an industrial scale, the most feasible options might not be single-cell systems, but *fewer*-cells systems featuring cells based on SiC power semiconductors with intermediate blocking voltages, e. g. 3.3 kV, which could offer a suitable trade-off between performance and complexity.

Furthermore, reliability concerns arising from the high number of components in multi-cell systems have been addressed by showing how the addition of redundant cells can improve the system reliability. If similar costs of the redundancy in terms of additionally installed power capability are considered, the resulting reliability of systems based on LV semiconductors and hence many cells is comparable to that of designs based on fewer cells with higher blocking voltages. Reliability considerations do therefore not a priori exclude solutions based on LV semiconductors and many cascaded cells, which have been identified before to offer suitable trade-offs between power density and efficiency.

Other aspects that could affect the choice of the number of cells comprise the complexity of the system, i. e., the signal electronics including the potentially required redundancy to fully benefit from increased reliability achieved by means of redundant converter cells, but also the construction complexity, especially if advanced features such as the capability to hot-swap converter cells are desired. Furthermore, economical considerations such as the trade-off between capital expenditure (CAPEX) and operating expenditure (OPEX), e. g., costs caused by energy losses but also by the effort for maintenance and

repair, etc., are important with respect to developing, selling, and servicing of industrial products. The comparatively flat optimum of the blocking voltage, and especially also the trade-off between efficiency and power density shown by the Pareto fronts leave room to include such advanced considerations in the selection of the number of converter cells for high-power MV converter systems, and hence to obtain suitable performance in multiple dimensions, i. e., not only concerning efficiency and power density, to satisfy specific customer requirements. Further considerations in this direction could be based on the analysis presented here.

3
HC-DCM SRC Isolation Stage

Cascaded multi-cell converter structures such as, e. g., IBE SSTs require an interface between the local DC buses of the cascaded converter cells and the common LV DC bus, which, since the cells' DC buses are on floating potential, must be isolated (cf. Section 1.3 and **Fig. 1.9**). Additionally, such isolated DC-DC converters can operate the transformer that provides the galvanic separation at an elevated frequency, i. e., MFTs can be employed, allowing for a corresponding reduction of volume and weight. To prevent a high switching frequency from degrading the converter efficiency, ZVS and/or, especially in case IGBTs are used, ZCS modulation schemes should be used.

Typically, two main realization options for high-power isolated DC-DC converter stages are considered for SST applications: The DAB converter that has been patented in 1989 by DeDoncker et al. [66], and the SRC operated in HC-DCM, which was first described by McMurray in 1969 [38]. A detailed comparison and analysis of the two concepts and their suitability for high-power SST applications has been presented in [119]. As an aside, the phase-shifted full-bridge converter [120] should be mentioned as third option, which was recently applied to LV multi-cell PFC rectifiers for telecom applications [121]. However, this converter requires an output inductor on the LV side, which would therefore carry high currents, and, more important, the topology is typically only unidirectional, which in general is not suitable for high-power SST applications.

In its standard form, the DAB converter consists of two power inverter bridges that are connected to the MV and the LV terminals of an isolation transformer, which features a certain stray inductance, L_σ. By suitable control of the two active bridges, the voltage applied to the stray inductance and hence the current flowing in it can be controlled. With the most basic modulation

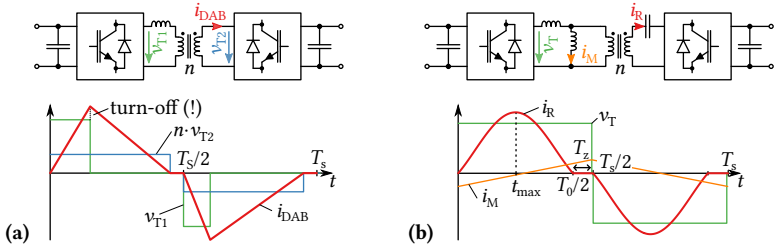


Fig. 3.1: (a) Basic operating principle of a DAB converter with triangular current mode [119, 123]; and **(b)** as HC-DCM SRC. Note that typically series capacitors need to be placed on both sides of the transformer in order to prevent saturation of the transformer core in case of a (small) DC bias of the bridge output voltage.

scheme, both bridges apply rectangular voltages with full duty ratio to the transformer, however, a phase-shift between the switching of the two bridges allows to control the current and hence the power flow in the converter. Furthermore, ZVS can be achieved within a certain operating range [66]. If additionally also the duty cycles of the two active bridges are varied, the increased number of degrees of freedom can be utilized to, e. g., optimize the RMS current in the transformer [122], or to achieve ZCS for the MV-side switches by means of a triangular transformer current [119, 123] as shown in in **Fig. 3.1a**. On the other hand, still the peak current must be turned-off by the LV-side switches.

By adding a capacitor in series to the stray inductance as shown in **Fig. 3.1b**, a resonant tank is formed. Thus, an excitation with a (rectangular) voltage by one of the converter bridges causes a (piecewise) sinusoidal current. From the large family of operating modes of resonant converters [124], especially the HC-DCM, which was initially described in [38], is of high interest for high-power applications, since it provides ZCS for all switching transitions (cf. **Fig. 3.1b**); it is also possible to achieve load-independent ZVS by utilizing the magnetizing current.

Another highly interesting feature of the HC-DCM SRC is the fact that it achieves a tight coupling of its input and its output voltage in open-loop operation. To do so, it is sufficient to switch the sourcing bridge with (almost) full duty ratio to apply a rectangular voltage to the transformer, while the sinking bridge can be operated passively as a diode rectifier. In contrast to the DAB converter, the HC-DCM SRC does not need comparatively complex control and modulation schemes, and it can inherently achieve ZVS/ZCS independent of the load. From another perspective, however, the HC-DCM

SRC *cannot* be controlled. However, note that in IBE as well as in IFE SST concepts (cf. **Chapter 1**) there is no strict need for the isolation stage to provide any control of the power flow, because this functionality can be taken over by the regulated converter stages that are either located on the MV side (IBE approach) or on the LV side (IFE approach) of the DC-DC (or, in case of the IFE concept, |AC|-|AC|) converter.

An autonomous "DC transformer" behavior of the DC-DC converter is thus sufficient, and, with respect to the complexity of larger multi-cell SST systems, even desirable. This is the reason, why almost all industrial SST projects, which employ typically IBE topologies, utilize HC-DCM SRC isolation stages [19,26–28,30,31,125–128]. Recently, the converter has also been proposed for a high-power DC-DC step-up application for MV DC collecting grids in offshore wind parks [129], and its application ranges even down to low-power applications such as point-of-load converters in datacenters, as for example described in [130].

Thus, the HC-DCM SRC is an important building block of both main SST topologies that are discussed in the scope of this thesis—IBE and IFE. This chapter first describes the operating principle of the HC-DCM SRC in detail (Section 3.1), derives then a dynamic model of the HC-DCM SRC, which is an important tool to analyze the dynamics of the converter's terminal behavior (Section 3.2), and finally provides an efficiency versus power density Pareto optimization of an IGBT-based HC-DCM SRC system for IBE-based SSTs, including the modeling of IGBT switching losses under ZCS/ZVS conditions (Section 3.3).

3.1 Operating Principle of the HC-DCM SRC

Following considerations described in [95, 131], this section discusses the steady-state converter waveforms, the calculation of key metrics such as peak and RMS currents, explains the "DC transformer" behavior and finally the influence of converter losses on the steady-state voltage transfer ratio of the HC-DCM SRC.

Fig. 3.2 shows a schematic representation of the HC-DCM SRC converter and key waveforms for one switching period. The AC-DC block and the DC-AC block symbolize converter bridges, which can either be realized as full-bridges or as half-bridges. The resonant tank consists of the transformer stray inductance, L_σ, and a dedicated resonant capacitor, C_r. Note that C_r could also be split between the two sides of the transformer, or it would be possible to implement the resonant capacitor as a capacitive bridge leg if a

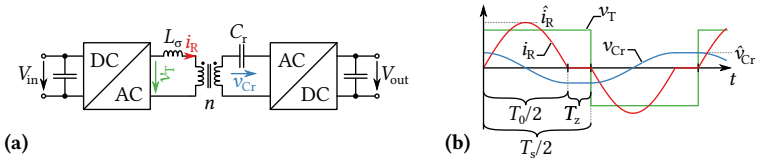


Fig. 3.2: Basic topology **(a)** and key waveforms **(b)** of the HC-DCM SRC.

half-bridge configuration is used.

For power transfer from the input to the output, only the input-side DC-AC converter is actively switching at a constant frequency, f_s, thereby generating a rectangular voltage, v_T, with (almost) full duty ratio. Considering a lossless case, ideal switches, and steady-state operation, the output voltage equals the input voltage (scaled by the transformer turns ratio), i. e., $V_{out} = V_{in}/n$. At the beginning of a new switching cycle, therefore only the voltage across the resonant capacitor, $\hat{v}_{Cr}$, excites the resonant tank and gives rise to a sinusoidal current pulse according to

$$i_R(t) = \frac{\hat{v}_{Cr}}{Z_0} \sin(\omega_0 t), \quad \text{where} \quad Z_0 = \sqrt{\frac{L_\sigma}{C_r}} \quad \text{and} \quad \omega_0 = \frac{1}{\sqrt{L_\sigma C_r}}. \tag{3.1}$$

Since the second bridge is operated as diode rectifier, the current cannot reverse its direction once it reaches zero at $t = T_0/2$, where $T_0 = 1/f_0$ and where f_0 denotes the natural resonant frequency, $f_0 = \omega_0/(2\pi)$. The positive semi-cycle of the transformer current can thus be described as

$$i_R(t) = \begin{cases} \hat{i}_R \sin(2\pi f_0 t) & 0 \le t < T_0/2 \\ 0 & T_0/2 \le t \le T_s/2 \end{cases}; \tag{3.2}$$

the negative semi-cycle follows from symmetry considerations. Since the resonant current pulse flows through the resonant capacitor, its voltage reaches $-\hat{v}_{Cr}$ at this point and then stays constant until the next switching cycle is initiated at $t = T_s/2$. Note that $f_s < f_0$, in order to account for the finite switching speed and the interlock delay time of a real system. In addition, the resulting zero current interval, T_z, between the end of the resonant half cycle and the switching transition (cf. **Fig. 3.2b**) can be utilized to reduce ZCS switching losses as will be discussed in Section 3.3.

As an aside, note that the shape of the current pulses deviates from a pure piecewise sinusoid if the ratio between the DC link capacitances and the

capacitance of the series resonant capacitor is less than about 10:1, and that then the calculation of the duration of a resonant half-cycle becomes more complicated, as is described in detail in [131, 132].

Currents for Full-Bridge Configuration

If the DC-AC converter on the input side is realized as full-bridge, the magnitude of the voltage applied to the transformer equals the input DC voltage, i. e., $\hat{v}_\mathrm{T} = V_\mathrm{in}$. Assuming a constant input voltage and piecewise sinusoidal currents, the transferred power becomes

$$P = \frac{2}{T_\mathrm{s}} \int_0^{\frac{T_0}{2}} V_\mathrm{in} \hat{i}_\mathrm{R} \sin(2\pi f_0 t)\, dt = \frac{2 V_\mathrm{in} \hat{i}_\mathrm{R} f_\mathrm{s}}{\pi f_0}, \tag{3.3}$$

and from that the peak and RMS currents of the resonant current follow as

$$\hat{i}_\mathrm{R} = \frac{\pi P}{2 V_\mathrm{in}} \cdot \frac{f_0}{f_\mathrm{s}} \quad \text{and} \quad \tilde{i}_\mathrm{R} = \frac{\sqrt{2}}{4} \cdot \frac{\pi P}{V_\mathrm{in}} \cdot \sqrt{\frac{f_0}{f_\mathrm{s}}}. \tag{3.4}$$

Currents for Half-Bridge Configuration

If, in contrast, the DC-AC converter on the input side is realized as a half-bridge, e. g., using an NPC bridge leg and a split DC link, only half of the input DC voltage is applied to the transformer, i. e., $\hat{v}_\mathrm{T} = V_\mathrm{in}/2$. Then, again assuming a constant input voltage, ideal symmetry of the split DC link capacitors, and piecewise sinusoidal currents, the transferred power becomes

$$P = \frac{2}{T_\mathrm{s}} \int_0^{\frac{T_0}{2}} \frac{V_\mathrm{in}}{2} \cdot \hat{i}_\mathrm{R} \sin(2\pi f_0 t)\, dt = \frac{V_\mathrm{in} \hat{i}_\mathrm{R} f_\mathrm{s}}{\pi f_0}, \tag{3.5}$$

and from that the peak and RMS currents of the resonant current follow as

$$\hat{i}_\mathrm{R} = \frac{\pi P}{V_\mathrm{in}} \cdot \frac{f_0}{f_\mathrm{s}} \quad \text{and} \quad \tilde{i}_\mathrm{R} = \frac{\sqrt{2}}{2} \cdot \frac{\pi P}{V_\mathrm{in}} \cdot \sqrt{\frac{f_0}{f_\mathrm{s}}}. \tag{3.6}$$

Note that in both cases the ratio between the resonant frequency and the switching frequency affects the peak and RMS values of the resonant current. Regarding conduction losses, $f_0 = f_\mathrm{s}$ would be the optimum choice; however, as will be discussed in Section 3.3, in case IGBTs are used, there is a trade-off between conduction and switching losses that has an optimum for $f_\mathrm{s} < f_0$. Also, considering component tolerances among cells in a multi-cell system, a certain margin between the resonant and the switching frequency must be admitted if DCM mode shall be ensured (cf. also Section 5.2).

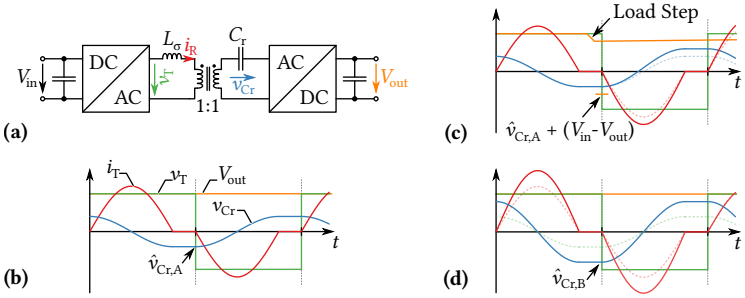


Fig. 3.3: (a) Basic topology of the HC-DCM SRC, **(b)** idealized waveforms for a steady state A, **(c)** disturbance of this steady state by a load step that causes a step in the output voltage, and **(d)** new steady state B corresponding to the increased power flow.

3.1.1 Idealized "DC Transformer" Behavior

As mentioned above, the HC-DCM SRC achieves a tight coupling between its input and output voltages, acting as a "DC Transformer". Considering for now still ideal components, i. e., neglecting losses, this behavior can be explained using **Fig. 3.3**. Starting from a certain steady state A with a given power flow through the converter and $V_{out} = V_{in}/n$ as shown in **Fig. 3.3b**, the initial condition of each resonant pulse is given by the peak resonant capacitor voltage, i. e., $\Delta V_{ex} = \hat{v}_{Cr,A}$ and hence $\hat{i}_R = \hat{v}_{Cr,A}/Z_0$.

If a step-change of the load current occurs, the output voltage will decay due to the finite output capacitance, as shown in **Fig. 3.3c**. However, then the temporary difference between the output and the input voltage will also contribute to the excitation voltage of the next resonant cycle, i. e., $\Delta V_{ex} = \hat{v}_{Cr,A} + (V_{in} - V_{out})$. Accordingly, the amplitude of this next resonant pulse will be higher, which corresponds to an increase of the power transfer through the converter (cf. (3.3)), i. e., the power flow is automatically adjusted to meet the higher load at the output such that finally a new steady state B with correspondingly higher power transfer is attained (cf. **Fig. 3.3b**). Section 3.2 provides an in-depth discussion of the involved dynamics, and details on the derivation of a passive equivalent circuit of the HC-DCM SRC that can be used to model the converter's dynamic terminal behavior.

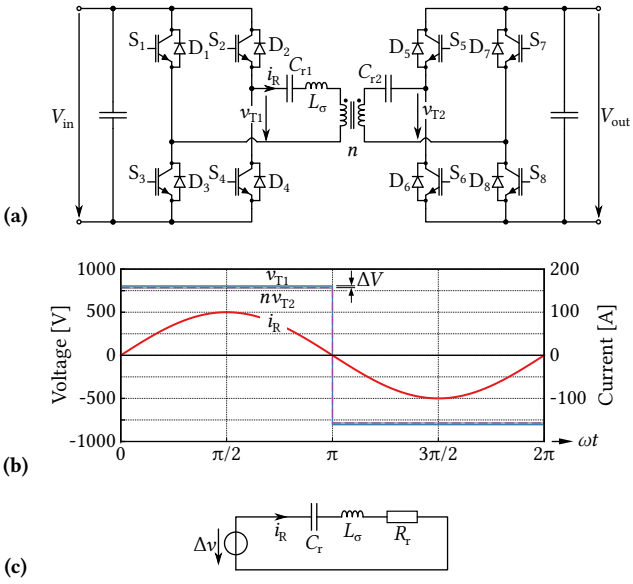


Fig. 3.4: (a) HC-DCM SRC topology; **(b)** simulated current and voltage waveforms for $L_\sigma = 16\,\mu\text{H}$, $C_\text{r} = 25\,\mu\text{F}$, $R_\text{r} = 130\,\text{m}\Omega$, $V_\text{in} = 800\,\text{V}$ and $P_\text{out} = 50\,\text{kW}$; **(c)** simplified and primary side referred converter model [133].

3.1.2 Effect of Losses on the Steady-State Output Voltage

A real converter system is, unfortunately, not lossless; current passing through power semiconductors causes voltage drops because of the junction voltage observed in bipolar devices such as IGBTs and diodes, and because of the on-state resistance of the devices. The same holds for current flowing through transformer windings and interconnections between components in general, where ohmic voltage drops and corresponding conduction losses appear. These voltage drops cause a (load-dependent) deviation of the output voltage from the input voltage, i. e., $V_\text{out} < V_\text{in}/n$. In this subsection, fundamental frequency analysis is applied in order to evaluate these effects on the HC-DCM SRC's steady-state voltage transfer ratio in more detail, whereby the considerations follow [95].

Ideally, the HC-DCM SRC (**Fig. 3.4a**) is operated such that the switching event occurs at the zero-crossing of the resonant tank current in order to achieve low switching losses. Thus, the sign of the resonant current, i_R,

determines the states of the switches:

$$\begin{aligned} i_\mathrm{R} > 0: &\ \mathrm{S}_1 \text{ and } \mathrm{S}_4 \text{ are turned on,} \\ i_\mathrm{R} < 0: &\ \mathrm{S}_2 \text{ and } \mathrm{S}_3 \text{ are turned on,} \end{aligned} \tag{3.7}$$

where the presented analysis confines to power transfer from input side to output side; operation for the opposite power flow direction yields similar results. As a consequence, a self-sustained oscillation close to the resonance frequency of the resonant tank,

$$f_0 = \frac{1}{2\pi\sqrt{L_\sigma C_\mathrm{r}}}, \tag{3.8}$$

is achieved (**Fig. 3.4b**), since a practical converter design features a comparably low ohmic voltage drop.

The resulting steady-state output voltage, V_out, is close to V_in/n, however, a small difference $V_\mathrm{in}/n - V_\mathrm{out}$ remains due to converter losses. In the following, an analytical model introduced in [133] will be used to determine the influence of the load power and the losses on this voltage difference, on which the model is based. It employs the simplified converter circuit depicted in **Fig. 3.4c**, which neglects all parasitic components of the transformer and refers all currents and voltages to the primary (input) side. There, R_r summarizes the resistive components of the circuit and $\Delta v(t)$ is the effective voltage applied to L_σ, C_r and R_r:

$$\begin{aligned} \Delta v(t) &= \left[V_\mathrm{in} - 2V_\mathrm{f,IGBT} - n(V_\mathrm{out} + 2V_\mathrm{f,diode}) \cdot \operatorname{sign}\left(i_\mathrm{R}(t)\right)\right] \\ &= \Delta V \cdot \operatorname{sign}\left(i_\mathrm{R}(t)\right) \end{aligned} \tag{3.9}$$

and

$$R_\mathrm{r} = R_\mathrm{L+C+tr} + 2(R_\mathrm{d,IGBT} + n^2 R_\mathrm{d,diode}), \tag{3.10}$$

where $R_\mathrm{L+C+tr}$ is the sum of the series resistances of L_σ, C_r and the transformer; $V_\mathrm{f,IGBT}$ and $V_\mathrm{f,diode}$ are the (approximately) constant forward voltage drops of IGBTs and diodes; and $R_\mathrm{d,IGBT}$ and $R_\mathrm{d,diode}$ are the IGBTs' and diodes' differential resistances.[1]

The steady-state operating point is calculated by means of fundamental frequency analysis [133], which features an accurate description of the processes in the resonant tank due to the reasons given below:

[1] Assuming identical diodes D_1...D_8 and identical IGBTs S_1...S_8.

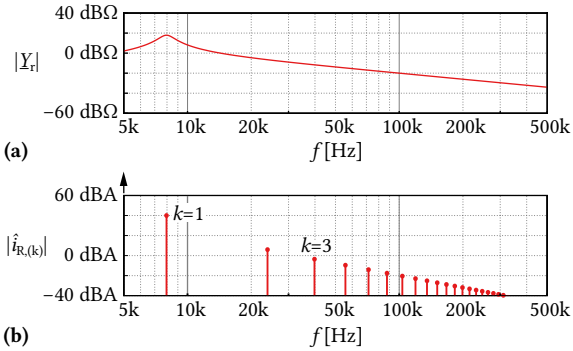


Fig. 3.5: (a) Admittance of the resonant tank ($L_\sigma = 16\,\mu\text{H}$, $C_\text{r} = 25\,\mu\text{F}$, $R_\text{r} = 130\,\text{m}\Omega$); **(b)** calculated spectrum of i_R: $\hat{i}_{\text{R},(1)}$ is 34 dB higher than $\hat{i}_{\text{R},(3)}$. The spectrum shown in **(b)** corresponds to the current depicted in **Fig. 3.4b**, which is almost sinusoidal.

1. The amplitude of each odd k-th harmonic component of the rectangular voltage $\Delta v(t)$, $\Delta\hat{v}_{(k)}$, is given with $\Delta\hat{v}_{(k)} = \Delta\hat{v}_{(1)}/k$. Thus, the impact of $\Delta\hat{v}_{(k)}$ on the waveform of i_R decreases with increasing k.

2. The frequency of the fundamental component of $\Delta v(t)$ is very close to f_0. The resonant tank represents a low pass filter for $f > f_0$ and effectively reduces harmonic current components with $k > 1$ (cf. **Fig. 3.5**).

Laplace transform is used to analyze the initial excitation of the resonant tank with

$$\Delta v_{(1)}(t) = \frac{4}{\pi}\Delta V \sin(\omega_0 t) \text{ where } \omega_0 = \frac{1}{\sqrt{L_\sigma C_\text{r}}}. \tag{3.11}$$

This yields the response shown in **Fig. 3.6**, which illustrates how steady-state operation is reached after a few oscillations. The steady-state operating point is calculated with conventional circuit theory,

$$\begin{aligned} \Delta\underline{v}_{(1)} &= \frac{4}{\pi}\Delta V e^{j\omega_0 t}, \quad \underline{i}_{\text{R},(1)} = \frac{\Delta\underline{v}_{(1)}}{R_\text{r}}, \\ \underline{v}_{\text{Cr},(1)} &= -jZ_0\underline{i}_{\text{R},(1)} \text{ with } Z_0 = \sqrt{\frac{L_\sigma}{C_\text{r}}}, \end{aligned} \tag{3.12}$$

and the resulting amplitudes of the capacitor voltage, v_Cr, and the inductor

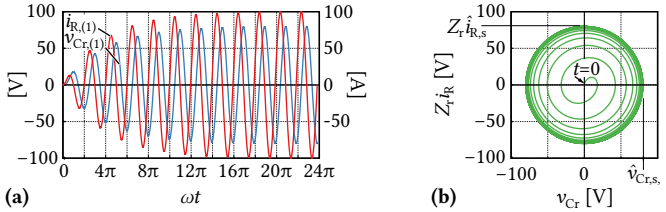


Fig. 3.6: (a) Response of the resonant tank of **Fig. 3.4c** to a sinusoidal excitation; **(b)** corresponding phase diagram.

current, i_R, are:

$$\hat{v}_{Cr,(1)} = \frac{4\Delta V}{\pi}\frac{Z_0}{R_r}, \quad \hat{i}_{r,(1)} = \frac{4\Delta V}{\pi}\frac{1}{R_r}. \tag{3.13}$$

The capacitor connected to the output side rectifier impresses a constant voltage, V_{out}, and thus the output power is proportional to the square of the average resonant tank current. Accordingly, (3.13) enables the calculation of ΔV as a function of the transferred power,

$$P_{out} = \left(\frac{2}{\pi}\hat{i}_{R,(1)}\right)^2 n^2 R_{load} = \left(\frac{8}{\pi^2}\frac{\Delta V}{R_r}\right)^2 n^2 R_{load}$$

$$\Rightarrow \Delta V(P_{out}) = R_r\frac{\pi^2}{8}\sqrt{\frac{P_{out}}{n^2 R_{load}}} = R_r\frac{\pi^2}{8}\frac{P_{out}}{nV_{out}}, \tag{3.14}$$

where $R_{load} = V_{out}^2/P_{out}$ has been used for the last step. From that, V_{out} can be obtained as

$$V_{out} = \frac{1}{n}\cdot\left[V_{in} - \Delta V(P_{out}) - 2V_{f,IGBT}\right] - 2V_{f,diode}, \tag{3.15}$$

and by substituting $\Delta V(P_{out})$ by (3.14), the relation between transferred power and resulting deviation from the ideal voltage transfer ratio can be found as

$$V_{out} = \frac{1}{2}V_0 + \frac{1}{2}\sqrt{V_0^2 - \frac{\pi^2}{2n^2}R_r P_{out}}, \tag{3.16}$$

where

$$V_0 = \frac{1}{n}V_{in} - 2\left(\frac{1}{n}V_{f,IGBT} + V_{f,diode}\right). \tag{3.17}$$

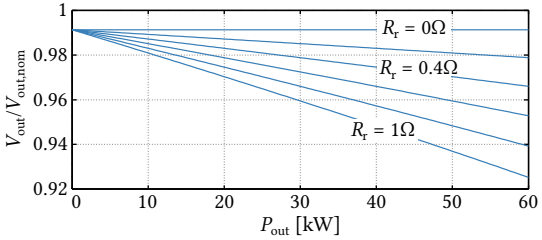


Fig. 3.7: Dependence of the LV-side output voltage on the transferred power and the resistor R_r.

This equation and its visualization in **Fig. 3.7** show clearly that the system losses, here considered only by the semiconductor voltage drops and the resistor R_r for reasons of clarity, cause a load-dependent variation of the input/output DC voltage ratio. Switching losses and core losses can be regarded as an increase of the effective load power. In order to achieve a tight coupling between input and output DC voltages that is (nearly) independent from the transferred power, it is thus mandatory to minimize the converter (conduction) losses.

Note also that the presence of series resistance causes a deviation of the resonant current pulses from the piecewise sinusoidal shape because the resistance damps the current oscillation, and hence affects the effective duration of a current half-cycle. However, this deviation is small for high-efficiency designs, as has been described in [131].

3.2 Dynamic Modeling of the HC-DCM SRC's Terminal Behavior

As has been discussed in Section 3.1.1, the HC-DCM SRC behaves as a "DC transformer" with respect to its input and output terminal voltages and currents. Essentially, the amplitude of the resonant current pulses is given by the exciting voltage steps, which are in steady state defined by the voltage difference of the two DC voltages (referred to the same side of the transformer). When a load increase creates a voltage sag in the load-side DC bus, the exciting voltage increases, leading to higher peak currents and hence to an increase of the power transfer through the converter. Thus, the power flow through the converter adjusts automatically such that the (transformed) DC voltages on either side stay equal (except for some deviation due to losses). Note that

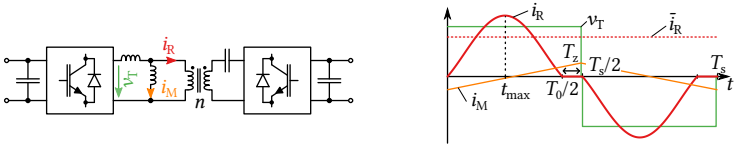


Fig. 3.8: Key waveforms of the HC-DCM SRC, where the local average value, $\bar{i}_R$, of the resonant current, i_R, is highlighted.

there is no control possibility; the converter acts as a "DC transformer" with a certain dynamic behavior, which leads to a number of consequences regarding the design and operation of SST converter cells based on the HC-DCM SRC.

In order to better understand these dynamic terminal behavior of the HC-DCM SRC, and also for facilitating the design of the DC link capacitors for an application as a DC-DC converter in a multi-cell SST system (cf. Section 4.1), a non-switching model that accurately mimics the converter's terminal behavior is beneficial.

A common approach to obtain such a model consists of averaging currents and voltages over a switching period (or half a switching period, for that matter), i. e., the current flowing in the model is the local average current, $\bar{i}_R$, of the real converter current, i_R (cf. **Fig. 3.8**). Such an equivalent circuit capturing the converter dynamics with respect to its terminal voltages and currents has been proposed already in 1990 [133, 134] (in German) for sinusoidal currents (cf. **Fig. 3.10a**), and was then refined later [126, 127] (both in German) (cf. **Fig. 3.9c**), considering piece-wise sinusoidal currents (cf. **Fig. 3.10b**).

In the following, based on [135], the equivalent circuit will be re-derived in a generic way using a power- and energy-based approach, which yields the known results for the two mentioned cases. In addition, here the validity is extended to the case of small DC link capacitors, where the current shape deviates from a purely sinusoidal shape [131], which is then verified with measurements of a full-scale IBE SST converter cell.

3.2.1 Dynamic Model Derivation

Generally, a given amount of power transfer through the converter is associated with certain losses and a certain amount of stored energy in the SRC's resonant tank (cf. **Fig. 3.9b**). In order to yield the same terminal behavior as the real converter, an equivalent model must correctly capture these two phenomena, i. e., losses and stored energy in the system as functions of the

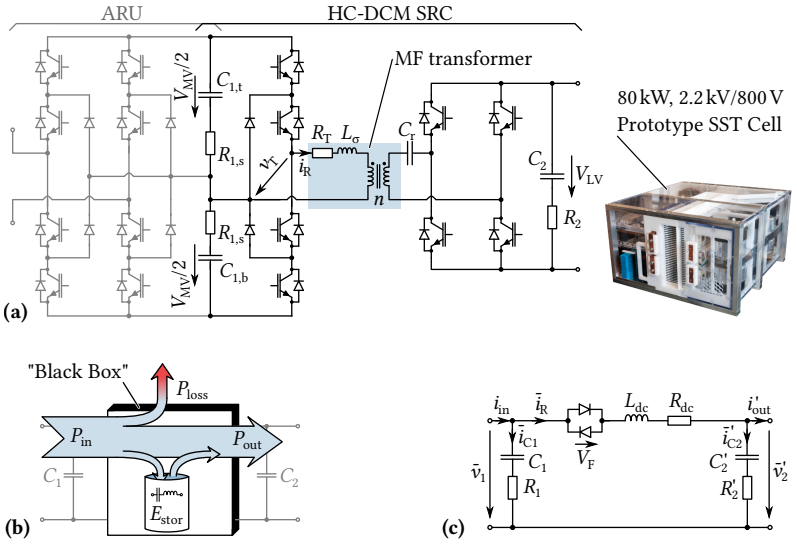


Fig. 3.9: (a) IBE SST cell power circuit consisting of an active rectification unit (ARU) and a HC-DCM SRC, and photo of realized prototype [136]; **(b)** energy- and loss-based modeling concept visualization; **(c)** resulting MV-referred dynamic equivalent circuit.

transferred power must be equal. In the following, this generic conditions are used to re-derive the dynamic equivalent circuit [126] shown in **Fig. 3.9c**, whereby all quantities are referred to the MV side of the considered example IBE SST converter cell topology shown in **Fig. 3.9a**.

Half-Bridge to Full-Bridge Transformation

In the considered example IBE SST converter cell, the MV-side topology is a half-bridge structure, whereas the LV-side topology is a full-bridge (cf. **Fig. 3.9a**). This combination yields a factor of two in the voltage gain, allowing for a lower turns-ratio of the MFT. To model this in the equivalent circuit, the following transformation is carried out,

$$\overline{v}_1 = V_{\mathrm{MV}}/2, \quad C_1 = 2C_{1,\mathrm{t}}, \quad \text{and } R_1 = 1/4 \cdot R_{1,\mathrm{t}}, \tag{3.18}$$

resulting in equal stored energy and losses in the MV DC link assembly.

Losses

The major share of the load-dependent losses occurs in the power semiconductors, which are modeled as a constant voltage drop, v_0, and a differential on-state resistance, r_{on}, as well as in the transformer windings, R_T.

Losses resulting from v_0 depend on the average current through the semiconductors. Since the local average current, $\bar{i}_R$, is flowing in the equivalent circuit (cf. **Fig. 3.9c**), these losses can be represented by anti-parallel diodes with an equivalent voltage drop, V_F, corresponding to the sum of the voltage drops of the semiconductors in the current path,

$$\bar{i}_R V_F \stackrel{!}{=} \bar{i}_R(2v_{0,1} + 2v'_{0,2}) \quad \Rightarrow \; V_F = 2v_{0,1} + 2v'_{0,2}, \tag{3.19}$$

where $v_{0,1}$ and $v_{0,2}$ denote the constant part of the voltage drops of the conducting semiconductors on either side of the transformer. Note that these values might change depending on the power flow direction (diode vs. IGBT).

On the other hand, losses resulting from the series resistances depend on the RMS current. Therefore, the equivalent resistance, R_{dc}, that only sees the average current, needs to be adapted,

$$\bar{i}_R^2 R_{dc} \stackrel{!}{=} \tilde{i}_R^2 R_{total} \quad \Rightarrow \; R_{dc} = \frac{\tilde{i}_R^2}{\bar{i}_R^2} R_{total} = \beta^2 R_{total}, \tag{3.20}$$

where R_{total} is the sum of all series resistances in the current path (R_T, r_{on} of conducting semiconductors, etc.).

Series resistances of the DC link capacitors can directly be inserted into the equivalent model; they retain their effect on the terminal currents, however, in reality they would also see the resonant current (i. e., its RMS value), not only its average value. To account for this, R_{dc} needs to be adapted [126]:

$$R_{dc} = \beta^2 R_{total} + (\beta^2 - 1)(R_1 + R'_2). \tag{3.21}$$

In the DCM operating mode, switching and core losses do not depend strongly on the transferred power, and therefore do not contribute to the converter dynamics. It would be possible to model them as shunt resistors in the equivalent circuit, though.

Stored Energy

The energy stored in the resonant tank, E_{stor}, (i. e., the sum of the energies stored in the stray inductance and in the resonant capacitor, respectively,

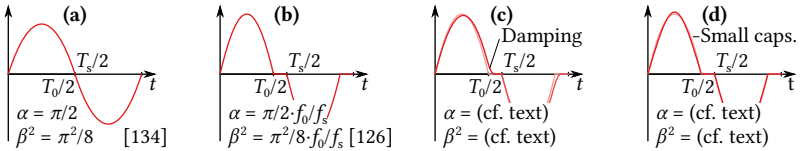


Fig. 3.10: SRC current shapes: **(a)** pure sinusoidal current; **(b)** piece-wise sinusoidal current; **(c)** effect of damping; **(d)** deviation caused by small DC capacitors.

which is constant during one switching period) depends on the transferred power,

$$E_{\text{stor}} = \frac{1}{2} L_\sigma \hat{i}_{\text{R}}^2. \tag{3.22}$$

Since the equivalent model is based on the average resonant current, an inductor, L_{dc}, is used to model the current-dependency of the stored energy,

$$\bar{i}_{\text{R}}^2 L_{\text{dc}} \stackrel{!}{=} \hat{i}_{\text{R}}^2 L_\sigma \quad \Rightarrow \; L_{\text{dc}} = \frac{\hat{i}_{\text{R}}^2}{\bar{i}_{\text{R}}^2} L_\sigma = \alpha^2 L_\sigma. \tag{3.23}$$

Summary

The elements of an equivalent circuit according to **Fig. 3.9c** can directly be calculated, for arbitrary waveform shapes, by means of the two ratios,

$$\alpha := \frac{\hat{i}_{\text{R}}}{\bar{i}_{\text{R}}} \quad \text{and} \quad \beta := \frac{\tilde{i}_{\text{R}}}{\bar{i}_{\text{R}}}. \tag{3.24}$$

Fig. 3.10a and **b** show the resulting values for the case of (piece-wise) sinusoidal current as derived earlier in [134] and [126], respectively. For the case of piece-wise sinusoidal current we have

$$\alpha = \frac{\pi}{2} \frac{f_0}{f_{\text{s}}} \quad \text{and} \quad \beta^2 = \frac{\pi^2}{8} \frac{f_0}{f_{\text{s}}}, \tag{3.25}$$

where f_{s} denotes the switching frequency and f_0 is the resonant frequency of the pulse, which is linked to the zero-current interval duration, T_{z}, as

$$f_0 = \frac{1}{2} \cdot \left(\frac{1}{2 f_{\text{s}}} - T_{\text{z}} \right)^{-1}. \tag{3.26}$$

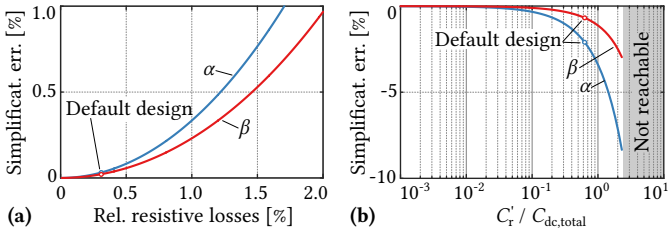


Fig. 3.11: Deviation of the simplified α and β (cf. **Fig. 3.10b**) from the correct calculation for **(a)** the influence of damping on the waveform (cf. **Fig. 3.10c**), and **(b)** for the case of small DC capacitors with $C_{\mathrm{dc,tot.}} := C_1 C_2' / (C_1 + C_2')$ (cf. **Fig. 3.10d**).

Damping Distortion

In reality, the series damping in the resonant circuit causes a deviation from the purely sinusoidal shape, as is indicated in **Fig. 3.10c**. While it is still possible to find an analytic expression for α and β, it is omitted here because **Fig. 3.11a** illustrates that the deviation from the idealized values remains below 0.5 % as long as RMS losses stay below 1 %, which is generally desired for reasons of system efficiency.

3.2.2 α and β for Small DC Link Capacitors

The current shape also deviates from a sinusoid if the DC link capacitors are chosen to be comparatively small with respect to the resonant capacitor, C_r, as illustrated in **Fig. 3.10d** [131]. **Fig. 3.11b** shows that the error introduced by not considering this effect can be quite high.

Starting from the normalized current shape in that case,

$$i_\mathrm{R}(t) = A \sin(\omega_0 t) + B(1 - \cos(\omega_0 t)), \tag{3.27}$$

where

$$\omega_0 = \sqrt{\frac{C_{1,\mathrm{t}} C_2' + C_{1,\mathrm{t}} C_\mathrm{r}' + C_2' C_\mathrm{r}'}{C_{1,\mathrm{t}} C_\mathrm{r}' C_2' L_\sigma}},$$

$$A = \frac{1}{\omega_0 L_\sigma} \left(\frac{1/2 \cdot T_\mathrm{s} + T_\mathrm{z}}{2 C_{1,\mathrm{t}}} + \frac{T_\mathrm{s}}{2 C_\mathrm{r}'} + \frac{T_\mathrm{z}}{C_2'} \right),$$

Tbl. 3.1: Main parameters of the *MEGAlink* IBE SST and the converter cell.

Rated SST power	1 MVA	LV DC voltage	800 V
Rated cell power	83.3 kW	Turns ratio, n	11 : 8
ARU sw. freq., $f_{\mathrm{s,i}}$	1 kHz	MV DC cap., $C_{1,\mathrm{t}}$	660 µF
SRC sw. freq., f_{s}	7.4 kHz	LV DC cap., C_2	140 µF
Zero-current interval, T_{z}	12.8 µs	Stray ind., L_σ	9 µH
MV DC voltage (per cell)	2.2 kV	Resonant cap., C_{r},	79 µF

and

$$B = \frac{2}{\omega_0^2 L_\sigma}\left(\frac{1}{C_2'} + \frac{1}{2C_{1,\mathrm{t}}}\right),$$

first the required resonant capacitor, C_{r}', for a desired T_{z} needs to be calculated by solving

$$\left(\frac{T_{\mathrm{s}}}{2} - T_{\mathrm{z}}\right) - \frac{2\pi - 2\arctan\left(A(C_{\mathrm{r}}')/B\right)}{\omega_0(C_{\mathrm{r}}')} \stackrel{!}{=} 0, \tag{3.28}$$

which is only possible numerically because both, A and ω_0, are functions of C_{r}'. For an in-detail discussion of the derivation of the current shape, etc., the reader is referred to [131]. Now that T_{z} and C_{r}' are matching, α and β can be found as

$$\alpha = \frac{\omega_0\left(A^2 + B^2 + B\sqrt{A^2+B^2}\right)}{2f_{\mathrm{S}}\sqrt{A^2+B^2}\,(BE + \pi B + 2A)}, \tag{3.29}$$

and

$$\beta^2 = \frac{\omega_0\left((A^2+3B^2)E + A^2\pi + 3B^2\pi + 6AB\right)}{4f_{\mathrm{S}}\,(BE + B\pi + 2A)^2}$$

with

$$E = \arctan\left(\frac{2AB}{A^2 - B^2}\right) \text{ and } A > B.$$

The expressions in (3.29) become equal to those in (3.25) for $C_{1,\mathrm{t}},\ C_2' \to \infty$.

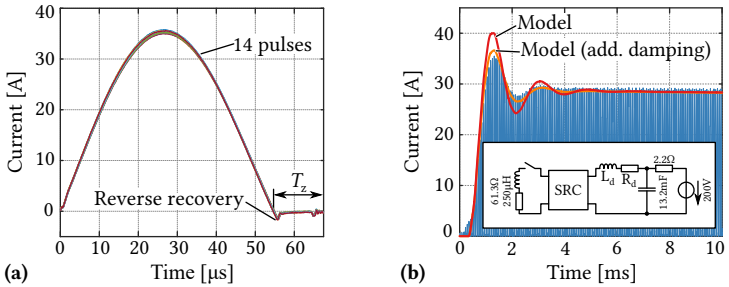


Fig. 3.12: (a) Measured resonant pulses used to determine α and β; **(b)** measured step response compared with results from the dynamic model.

Tbl. 3.2: Verification for small DC link capacitors ($C_{1,\mathrm{t}}$, $C_{1,\mathrm{b}}$ and C_2).

	Calc. (3.29)	Measured	Meas. w/o RR	Simpl. cal. (3.25)
α	1.971	1.991 (−1.7 %)	1.984 (−0.7 %)	1.938
β	1.240	1.248 (−0.6 %)	1.243 (−0.2 %)	1.234

3.2.3 Experimental Verification

Considering the prototype *MEGAlink* IBE SST converter cell (cf. **Chapter 4**) with the specifications detailed in **Tbl. 3.1** and the topology shown in **Fig. 3.9a**, the validity of the above derivation can be evaluated. Thus, **Fig. 3.12a** shows several measured current pulses plotted on top of each other. From each individual measurement, α and β are extracted and then averaged to improve accuracy. **Tbl. 3.2** shows the corresponding results, where the deviation of the calculated from the measured values is given in brackets.

The waveforms clearly show the effect of diode reverse recovery, which leads to a negative contribution to the local average value of the current pulse, which in turn needs to be compensated by a higher peak current for a given power transfer. Both effects increase the α of the measured waveform—setting the measured current to zero after its first zero crossing during post-processing results in α and β values that match even better with the calculation. In any case, values of α and β calculated assuming a piece-wise sinusoidal current, i. e., with (3.25), clearly deviate from the measurements, as was to be expected considering **Fig. 3.11b**.

Furthermore, **Fig. 3.12b** compares a measured step response of the SST cell prototype and the prediction obtained from a simulation of the equivalent

circuit in order to illustrate the model's capability of accurately describing the SRC converter's dynamic behavior. Note that the voltage and power levels are reduced compared to the nominal values in order to facilitate these measurements. The measurement circuit uses the switches of the converter cell's active rectification unit (ARU) to turn-on an *RL*-load, and a large capacitor on the LV DC side to exclude influences of the supplies' current limiter. L_d serves as a decoupling inductor to prevent a spreading of the SRC's switching harmonics (cf. Section 4.1), and R_d models its series resistance (specifically, an external coreless 17.9 µH inductor with a high $R_\mathrm{d} = 35\,\mathrm{m\Omega}$ is used). It can be noticed that the damping of the real system is higher than that of the model, which could be explained (cf. orange curve) by the presence of about 25 mΩ of additional series resistance in the LV DC side connections (cabling, contacts, etc.). Obviously, in a direct comparison of the equivalent circuit and a switched simulation model, where all component values are precisely known, almost perfect agreement can be achieved (cf. also **Fig. 4.3** and **Fig. 4.4b**).

3.2.4 Summary

The power flow through a HC-DCM SRC is not controllable. Instead, the HC-DCM SRC couples the two DC voltages with certain dynamics that can be described by means of a passive dynamic equivalent circuit. Therefore, a generic derivation of this equivalent circuit and an experimental verification for the special case of small DC link capacitors has been presented, and a good agreement of the model and the measurements has been found.

3.3 $\eta\rho$-Pareto Optimization of an IGBT-Based HC-DCM SRC

As has been discussed in the previous sections, the SRC operated in the HC-DCM is a very suitable option for the isolated DC-DC conversion stages that interface the floating DC buses of the cascaded converter cells in high-power SST systems to the common LV DC bus. Because typically semiconductor devices with high voltage blocking capability are required on the MV side, IGBTs are often considered. In order to operate these semiconductors in the MF range, ZCS modulation schemes are highly desirable and very often mandatory in order to reduce the switching losses sufficiently.

Earlier efforts focused on the ZCS behavior of power semiconductors

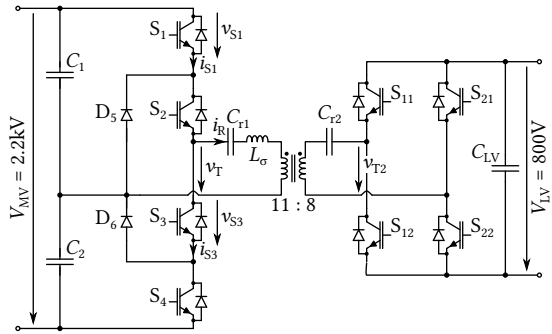


Fig. 3.13: HC-DCM SRC topology considered for the $\eta\rho$-Pareto analysis.

[125, 137, 138] and specifically the analysis presented in [139] for ZCS loss mechanisms in IGBTs allow to not only model conduction losses of the HC-DCM SRC as discussed so far, but also the residual switching losses caused by the stored-charge dynamics of bipolar power semiconductors such as IGBTs, which, e. g., affect an optimum choice of the f_0/f_s ratio. Such a comprehensive loss modeling provides a base to perform a full power density versus efficiency $\eta\rho$-Pareto optimization [89] of an IGBT-based HC-DCM SRC for high-power SST applications, which is described in the following based on [95].

3.3.1 MV-Side Bridge Topologies

For operation in the MV and MF range, IGBTs with 1.7 kV blocking voltage offer a feasible compromise between switching losses and the required number of semiconductors (cf. **Chapter 2**). The choice is further justified by cost considerations in comparison to IGBTs of higher blocking capability. Because the converter to be considered for the $\eta\rho$-Pareto optimization uses an MV-side DC link voltage of 2.2 kV (cf. specifications in **Tbl. 3.3**), three-level topologies must be considered for the MV side. In addition to the standard NPC topology shown in **Fig. 3.13** and used later in the Pareto optimization, **Fig. 3.14** shows two alternative realization options for the MV-side bridge. In both variants, additional capacitors are employed instead of clamping diodes.

Fig. 3.14a is a flying capacitor topology where capacitor C_3 is charged to half the DC link voltage and thus ensures voltage limitation for the switches [42]. The output current, i_R, flows through the flying capacitor during the freewheeling state. Since in the HC-DCM SRC the freewheeling interval is very short and only the magnetizing current is flowing during that time,

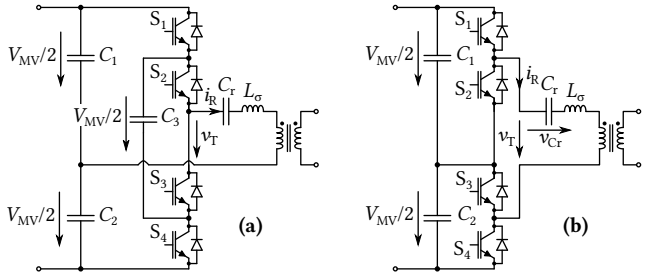


Fig. 3.14: Other realization options for the MV-side bridge that allow for using 1.7 kV IGBTs for $V_{\mathrm{MV}} = 2.2\,\mathrm{kV}$; **(a)** adds a flying capacitor while **(b)** uses a DC offset of $V_{\mathrm{MV}}/2$ on the resonant capacitor [140].

C_3 can be made small. By proper choice of the freewheeling states, natural balancing of its voltage can be achieved because of the dependence of the magnetizing current on the applied voltage. However, there is still a need to pre-charge that capacitor.

The third topology [140] is shown in **Fig. 3.14b**. Since the DC link midpoint is connected between S_2 and S_3, the switch voltage stress is limited to half the DC link voltage. The resonant capacitor, C_r, carries a DC offset of $V_{\mathrm{MV}}/2$, which enables again to apply three voltage levels to the transformer. However, C_r is subject to high DC voltage and simultaneously high current stress and/or AC voltage ripple, which is the main drawback of this topology.

Accordingly, all further considerations are for the NPC three-level topology depicted in **Fig. 3.13**. Performing an $\eta\rho$-Pareto optimization [89] for a converter is a suitable way of identifying designs that result in low overall losses and thus in a tight coupling of the DC voltages and on the other hand ensure a reasonably high power density. To do so, it is required to estimate the losses generated in the main components (semiconductors, transformer, resonant capacitors, DC link capacitors) as well as the component volumes for a given design. There exist a variety of models of these component losses, except for the switching losses under the conditions found in the HC-DCM SRC. Therefore, the modeling of the other components is only briefly discussed, whereas more room is dedicated to the semiconductor switching loss modeling. **Fig. 3.13** shows the converter topology considered for the Pareto optimization and **Tbl. 3.3** gives an overview on the system specifications, which are for an application of the converter in the *MEGAlink* IBE SST discussed later in **Chapter 4**.

Tbl. 3.3: Specifications of the HC-DCM SRC considered for the $\eta\rho$-Pareto optimization.

P	52.5 kW
Power flow direction	MV → LV
V_{MV}	2.2 kV
V_{LV}	800 V
Max. DC voltage ripple	0.5 %
Max. junction temp., T_{j}	125 °C
Ambient temperature, T_{a}	50 °C
Switching frequency range	5 kHz to 15 kHz
Transformer volume range	1 l to 30 l
Current zero interval duration	0 to $0.5\,T_{\mathrm{s}}/2$

3.3.2 Semiconductor Modeling

Even though the switching instants in the HC-DCM SRC are such that ZCS is obtained, significant switching losses are generated because of the dynamic behavior of the charge in the N-base layer of the IGBTs [139, 141]. A suitable model that allows estimation of the semiconductor losses under these conditions is presented in the following. In addition, the influence of the transformer magnetizing current on the switching losses is investigated and it is shown how the duration of the zero current interval can be used to reduce switching losses.

Stored Charge Behavior

This phenomenon has been analyzed in [141] and an analytical model for the stored charge, $Q(t)$, has been derived in [139] as

$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} + k_{\mathrm{s}} \cdot i_{\mathrm{s}}(t), \tag{3.30}$$

where τ and k_{s} are device parameters and $i_{\mathrm{s}}(t)$ is the current through the device. This model enables the calculation of the amount of charge, Q_{off}, that needs to be evacuated when the device is turned off, therefore providing information about the dissipated energy during the switching transient.

The model parameters τ and k_{s} are parameters of the semiconductors depending on the internal structure and/or design of the devices, which are

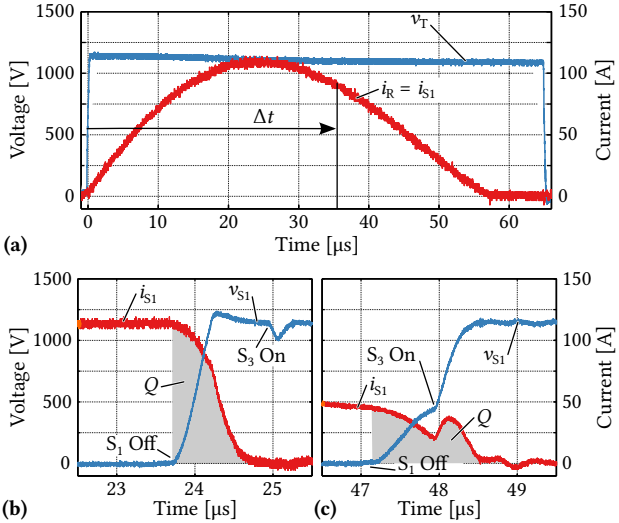


Fig. 3.15: (a) Positive current pulse where the current through S_1 equals the current i_R for $L_\sigma = 7.6\,\mu H$ and $C_r = 43\,\mu F$, resulting in $f_0 \approx 8.8\,kHz$. The turn-off time is defined by Δt and varied to measure the extracted charge at different points of the current waveform. Definition of the charge extracted from S_1 for **(b)** $\Delta t = 24\,\mu s$ and **(c)** $\Delta t = 48\,\mu s$.

generally not public, and therefore must be determined by curve fitting to experimental data as has been done in [139] for triangular current waveforms. The experiment is repeated here for the sinusoidal current of the HC-DCM SRC shown in **Fig. 3.15a** for the positive semi-cycle. The duration, Δt, of the applied voltage pulse is reduced in steps in order to measure the amount of charge extracted from S_1 at different points within the current waveform. **Fig. 3.15b** and **Fig. 3.15c** illustrate how this charge is measured during the turn-off switching transition of S_1.

Fig. 3.16 shows the measured charge, $Q_m(t)$, as well as the charge $Q(t)$ calculated with the the parameters k_s and τ obtained from fitting (3.30) to the measurement data (cf. **Tbl. 3.4** for parameter values). As can be seen, the model enables accurate prediction of the behavior of the stored charge in the IGBT.

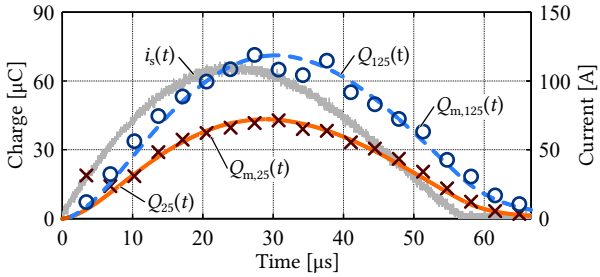


Fig. 3.16: Behavior of the stored charge for the IGBT Infineon FF150R17KE4 at T_j = 25 °C and T_j = 125 °C. $Q_{m,25}(t)$, $Q_{m,125}(t)$ are measurements and $Q_{25}(t)$, $Q_{125}(t)$ are obtained with (3.30) and k_s, τ as given in **Tbl. 3.4**.

Tbl. 3.4: Extracted parameters for the Infineon FF150R17KE4 IGBT.

Temperature T_j	τ	k_s
25 °C	4.45 µs	0.092
125 °C	6.04 µs	0.115

Switching Loss Reduction

When the switch current reaches zero, the charge carriers in the N-base layer recombine and thus the amount of stored charge in S_1 decays exponentially. During the subsequent transition from positive active state to freewheeling, first S_1 turns off, but since the current is already zero, v_{S1} stays low until the complementary switch S_3 turns on when the interlock delay time is over. If the turn-on of S_3, which ultimately forces v_{S1} to rise, occurs before the recombination process in S_1 is completed, the remaining charge in S_1 has to be evacuated through both of these switches and the resulting current spike generates turn-off losses in S_1 and turn-on losses in S_3, even though zero current switching is used (cf. **Fig. 3.18a**). However, there are several possibilities to reduce these switching losses as discussed in the following.

Zero Current Interval Duration During the time when the AC current is zero, the amount of stored charge decays because of recombination. Therefore, by increasing the duration of the zero-current interval, Q_{off} can effectively be

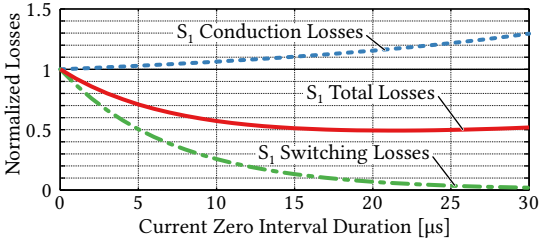


Fig. 3.17: Calculated influence of the zero current interval duration on the semiconductor losses for $f_s = 7.5\,\text{kHz}$ and $T_j = 125\,°\text{C}$. Note that the optimum is shifted to the left and upwards if other losses related to RMS current are included.

reduced [125,137]. However, from (3.4) it follows that $\hat{i}_R \propto f_0/f_s$ for $P = const.$, which clearly shows that a longer zero current interval (corresponding to higher f_0), while reducing switching losses, increases the peak current for the same amount of transferred power. This causes higher conduction losses in the semiconductors and also higher losses in passive components due to higher RMS current. However, as illustrated by **Fig. 3.17**, there is an optimum duration of the zero current interval resulting in lowest overall losses. The results in **Fig. 3.17** consider only semiconductor losses for the sake of clarity, while later in the $\eta\rho$-Pareto optimization all affected losses are included.

Magnetizing Current The magnetizing current, which is still flowing after the resonant current has already decayed to zero, helps to extract the charge from S_1 during the interlock delay time between the turn-off of S_1 and the turn-on of S_3 as described in [137, 138]. If the magnetizing current is high enough, ZVS turn-on for S_3 can be achieved. On the other hand, the turn-off losses in S_1 increase because the magnetizing current influences the charge profile and is switched off actively. **Fig. 3.18** shows the switching transitions for S_1 and S_3 for three different magnetizing current peak values. These results were obtained by connecting different external inductors in parallel to the MV transformer winding in order to emulate different magnetizing inductances [138]. **Fig. 3.19** shows the measured turn-off losses of S_1 and turn-on losses of S_3 for two different junction temperatures as a function of the peak magnetizing current. It can clearly be seen that there is an optimum regarding the overall switching losses, which occurs for the lowest magnetizing current peak value that is sufficient to achieve ZVS turn-on for S_3. The required peak magnetizing current can be estimated from $\hat{i}_M = Q_{off}/t_d$ under the assumption

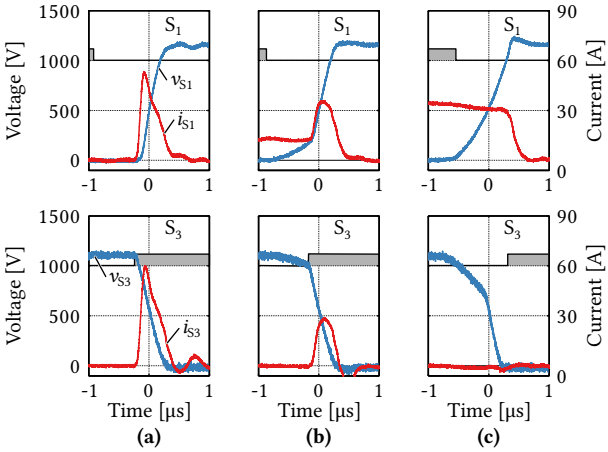


Fig. 3.18: The commutation process changes with increasing magnetizing current from **(a)** pure ZCS via **(b)** a mixed form to **(c)** soft-switching. The measurements were taken with a zero current interval of about 2 µs and an effective interlock time of about $t_d = 0.8\,\mu s$; the gate signals are indicated qualitatively.

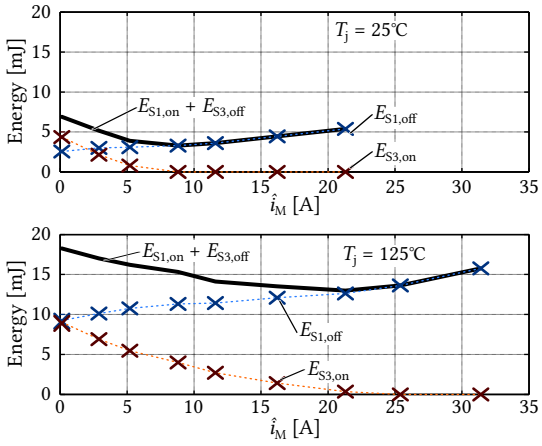


Fig. 3.19: Influence of the magnetizing current peak value, $\hat{i}_M$, on the turn-off losses in S_1 and the turn-on losses in the complementary switch S_3.

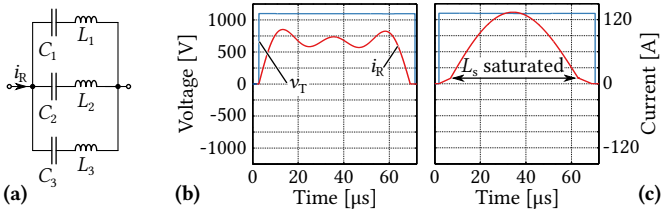


Fig. 3.20: (a) Extended resonant tank where branch 1 is tuned to $f_0 = 7.5\,\text{kHz}$, branch 2 to $3f_0$ and branch 3 to $5f_0$ and **(b)** resulting current waveform. **(c)** shows the current shape when a saturable inductor is connected in series to the normal LC resonant tank instead.

of constant magnetizing current during the interlock delay time t_d. Q_{off} is the remaining charge in S_1 at its turn-off instant.

To increase the accuracy, recombination of the charge according to (3.30) during t_d must be considered as well as the influence of a given magnetizing current peak value on the switch current waveform (hence on losses in all components carrying the magnetizing current) and the resulting charge profile in S_1, which has to be done in an iterative way. In the $\eta\rho$-Pareto optimization, the influence of the magnetizing current on the conduction losses and passive component losses is included.

Current Pulse Shaping The stored charge in the IGBT at a given point in time depends on the shape of the current up to that point. By shaping the current with an appropriate extension of the resonant tank, as, e. g., described in [142] and [143] for thyristor commutation circuits, the stored charge and/or the switching losses could be influenced, and/or shaping the current to a rectangular block with lower RMS value for a given power would allow to reduce RMS losses in the system. Such a current shape could be created by connecting several series resonant circuits in parallel as shown in **Fig. 3.20a**. As an example, let one resonant tank be tuned to f_0, the second to $3f_0$ and the third to $5f_0$. **Fig. 3.20b** shows the resulting shape of the resonant current. The RMS value is reduced to 93 % when compared with the RMS value of a pure sinusoidal current for the same transferred power. This corresponds to a reduction of all i^2-losses to 86.5 %.

In order to complete the picture, it has to be pointed out that it is not sufficient anymore to consider only the steady state forward characteristics when estimating conduction losses if the current shows a high di/dt at the

beginning of the pulse. Instead, the dynamic behavior of the IGBT (S_1) forward voltage after turn-on [141] would have to be considered.

Regarding the adverse effect of high di/dt at the beginning of the current pulse, another option of shaping the current consists of connecting a saturable inductor, L_s, in series to the standard LC resonant tank. This saturable inductor represents a high inductance for low currents, i. e., at the beginning and at the end of the pulse, and almost no inductance as soon as the current crosses the saturation threshold. **Fig. 3.20c** shows a resulting current waveform, which shows low di/dt at the beginning and at the end, where the latter is beneficial regarding Q_{off}, similar to an increase of the zero current interval duration.

Semiconductor Loss Modeling

The charge that would have to be removed for the current described by (3.2) can be calculated with (3.30). As indicated above, an iterative procedure is then used to determine the required magnetizing current to achieve ZVS turn-on for the complementary switch in order to obtain lowest overall switching losses. From that, Q_{off} of the turning-off switch can be determined and the turn-off energy can be estimated according to

$$E_{\text{off}} = \frac{1}{2} Q_{\text{off}} \frac{V_{\text{MV}}}{2}. \tag{3.31}$$

This approach is based on the assumption that the turn-off energy corresponds to the energy in a capacitance with charge Q_{off} at the blocking voltage of the device. **Fig. 3.21** illustrates that the assumption does agree well with measurements for pure ZCS (ca. $\Delta t \geq 55\,\mu\text{s}$) as well as for pure soft-switching (ca. $\Delta t \leq 40\,\mu\text{s}$). Especially for the mixed form (cf. **Fig. 3.18b**), future work will be required to unveil a more appropriate method of relating Q_{off} to the turn-off energy. However, all in all it becomes possible also with the models presented here to calculate semiconductor losses under ZCS conditions, which is a cornerstone of any comprehensive optimization of the HC-DCM SRC.

These losses occur four times (in all four MV-side switches) per switching period and consequently the switching losses are given by

$$P_{\text{off}} = 4 f_s E_{\text{off}}. \tag{3.32}$$

The switching losses of the diodes on the LV side are estimated accordingly. Conduction losses of both bridges are modeled following the procedure described in [144] using datasheet forward characteristics.

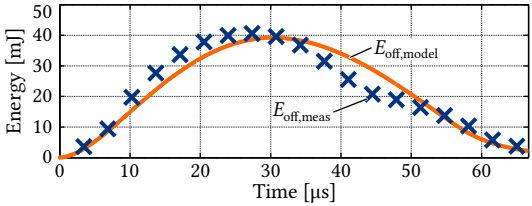


Fig. 3.21: Measurement and estimate of the turn-off losses in S_1 at $T_j = 125\,°C$. The Δt values used for the measurements are the same as in **Fig. 3.16**.

3.3.3 Modeling of Other Components

Heat Sinks

The losses generated in the semiconductors need to be removed in order to keep the maximum junction temperature below a certain value (typ. 125 °C). With the semiconductor loss estimates and datasheet values for the thermal resistances from junction to heat sink, the maximum allowable heat sink temperature can be calculated as

$$T_{hs,max} = T_{j,max} - (P_{switch} + P_{cond})R_{th,jh}. \tag{3.33}$$

Using the CSPI introduced in [103], it is possible to estimate the size of an air cooled heat sink for given power dissipation, ambient temperature and required maximum heat sink temperature as

$$V_{hs} = \frac{1}{CSPI \cdot R_{th,hs,max}}, \tag{3.34}$$

where $R_{th,hs,max} = (T_{hs,max} - T_a)/P_{loss}$. A CSPI value of $5\,W/(K\,dm^3)$ is used, which corresponds to a standard forced air cooled heat sink [103].

DC Link Capacitors

When constant DC input and output currents, $I_{MV} = P/V_{MV}$ and $I_{LV} = P/V_{LV}$, are assumed, the total current flowing through the DC link capacitors can directly be calculated using the total AC link current from (3.2), where the magnetizing current has to be added for the active bridge (i. e., the MV bridge in the case at hand). Integration of the current waveform gives the charge ripple and from that the capacitance needed to fulfill the voltage ripple requirement can be calculated. The capacitor volume is estimated assuming a

constant volume per capacitance for a given technology and voltage range, which is found to be 4.1 $\mathrm{cm^3/\mu F}$ from averaging the values for 1.3 kV film capacitors from different manufacturers. DC link capacitor losses are calculated from the RMS current and the ESR of the capacitors.

Transformer

The MFT is a core component of an isolated DC-DC converter. An existing optimization tool [145] was used to optimize transformers for a given boxed volume. This tool considers different core materials, winding arrangements, etc. For the transformer cooling, a heat transfer coefficient of $\alpha = 15\,\mathrm{W/m^2K}$ for free convection cooling is assumed [101] and designs that result in losses that could not be removed through the transformer surface for a maximum permissible surface temperature of 100 °C at 50 °C ambient temperature are dismissed.

Resonant Capacitors

The transformer stray inductance, L_σ, is one of the output parameters of the transformer optimization loop. Together with the desired resonance frequency, f_0, and neglecting the influence of the DC link capacitors, this defines the required series capacitance value as

$$C_\mathrm{r} = \frac{1}{4\pi^2 f_0^2 L_\sigma}. \tag{3.35}$$

Realization of C_r by capacitors of proper capacitance on both sides of the transformer as shown in **Fig. 3.13** is considered in order to prevent a DC magnetization of the transformer. The losses and the required volume are estimated in the same way as described above for the DC link capacitors.

3.3.4 $\eta\rho$-Pareto Optimization

The possibility of modeling the behavior of the stored charge in the IGBTs enables estimating switching losses also for the conditions found in the HC-DCM SRC. This is a requirement for performing a comprehensive $\eta\rho$-Pareto optimization [89] of the HC-DCM SRC, which is described in the following.

Using the modeling approach described above, a set of designs can be obtained by sweeping switching frequency, current zero interval duration and admissible transformer volume. The procedure is illustrated by **Fig. 3.22**. Each combination of these three parameters results in a specific design. The total

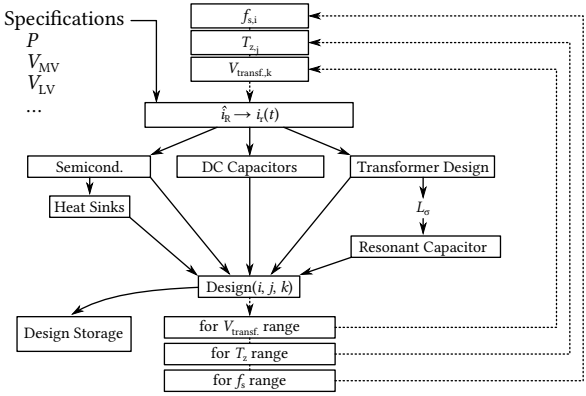


Fig. 3.22: Visualization of the procedure that calculates the design points used to find the Pareto front shown in **Fig. 3.23**.

losses of a design are given by the sum of individual component losses and the total component volume is given by the sum of the individual component volumes. In [89] it is suggested to account for form factor mismatches between components and inevitable empty spaces within a real converter with a coefficient $C_\mathrm{p} = 0.5 \ldots 0.7$ that relates the total volume, V_total, to the sum of component volumes, V_c, as $V_\mathrm{total} = V_\mathrm{c}/C_\mathrm{p}$. From the volume and the power loss, the efficiency $\eta = 1 - P_\mathrm{loss}/P$ and the power density $\rho = PC_\mathrm{p}/V_\mathrm{c}$ can be calculated directly.

Each design thus corresponds to a point in the $\eta\rho$-plane as shown in **Fig. 3.23**, where colors are used to indicate the designs' switching frequencies. An immediate conclusion from **Fig. 3.23** is that switching frequencies higher than about 10 kHz do not contribute anymore to volume reduction because the required heat sink size as a result of increasing switching losses does outweigh the reduction in size of passive components.

The achievable power density depends on the cooling concept. It would for example be possible to include a local optimization of a forced-air cooled heat sink into the overall optimization loop, which would result in a higher CSPI value and consequently shift the design points to the right, i. e., would increase the power density for a required efficiency. Also, considering a more advanced thermal management for the transformer (corresponding to an increase of α) would influence the specific position of the design points in the $\eta\rho$-plane.

It is in general also possible to calculate a Pareto front for a more specific

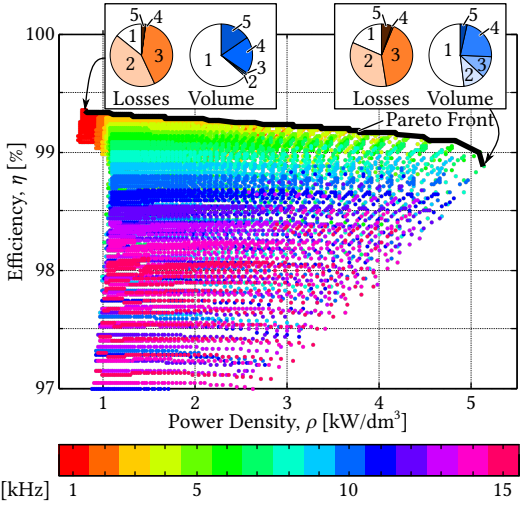


Fig. 3.23: Resulting designs in the $\eta\rho$-plane with $C_\mathrm{p} = 0.7$; the Pareto front is highlighted and relative loss and volume distribution for the two extreme points of the Pareto front are shown: 1) transformer, 2) LV semiconductors, 3) MV semiconductors, 4) DC links, 5) resonant capacitors.

design, where for example the arrangement of the components with respect to each other, various other constraints as well as additional variables such as costs could be considered. Furthermore, more detailed models for the individual components could be employed, however, at the cost of increased computation time. A Pareto optimization is thus a very suitable tool for investigating the performance limits of a given converter topology, operating mode and component technology [89] as well as for finding a feasible trade-off between efficiency, power density and possibly other performance indices when designing a specific system.

3.3.5 Summary

A detailed model for the behavior of the stored charge in the drift region of bipolar power semiconductors has been verified for the conditions found in the HC-DCM SRC. This allows for estimating the non-negligible switching losses under ZCS or quasi-ZCS conditions. Several methods to reduce these losses are evaluated, e. g., the use of the magnetizing current to achieve ZVS.

The switching loss model enables a comprehensive efficiency versus power density trade-off analysis resulting in the $\eta\rho$-Pareto front of the HC-DCM SRC. For a 52.5 kW converter interfacing a 2.2 kV DC bus to a 800 V DC bus by employing a NPC bridge based on 1700 V IGBTs on the MV side, an MV to LV efficiency of 99 % can be achieved at a power density of roughly 5 kW/dm^3. The corresponding switching frequency is comparably low (i. e., 7 kHz…9 kHz), and switching frequencies above 10 kHz are not suitable as a consequence of the switching losses.

4

IBE-Based Distribution SST: The MEGAlink

As has been discussed in **Chapter 1**, SSTs are envisioned for applications in the distribution grid, where, e. g., the possibility to control power flows or to provide an LV DC bus that could be used to connect renewables or to interface local DC micro grids, are considered as advantageous features. SST systems based on an IBE approach are most suitable for these kind of applications, because they can directly control the MV-side grid current, which facilitates accurate regulation of power flows, reactive power, etc., and provide an LV DC bus.

Fig. 4.1 shows a schematic representation of the *MEGAlink* SST, which is an IBE-based distribution SST serving as an example system for the considerations presented in this chapter. The *MEGAlink* interconnects a 10 kV MV grid to a 800 V LV DC bus, and optionally to the 400 V LV AC grid by means of additional LV inverters. The rated system power is 1 MVA—hence the term "*MEGAlink*".

This chapter covers several important aspects of the design of such an IBE-based SST system. First, Section 4.1 connects to the previous chapter and discusses the design of the HC-DCM SRC for applications in phase-modular SSTs. Section 4.2 presents a detailed analysis of the common-mode currents appearing in cascaded cells converter systems as a consequence of steep changes of the cells' potentials caused by the individual cells' switching actions. Finally, Section 4.3 provides a comparison of a 1000 kVA three-phase, LF distribution transformer (referred to as LFT only in the following) and the equally rated *MEGAlink* distribution SST, with respect to volume, weight, losses, and material costs.

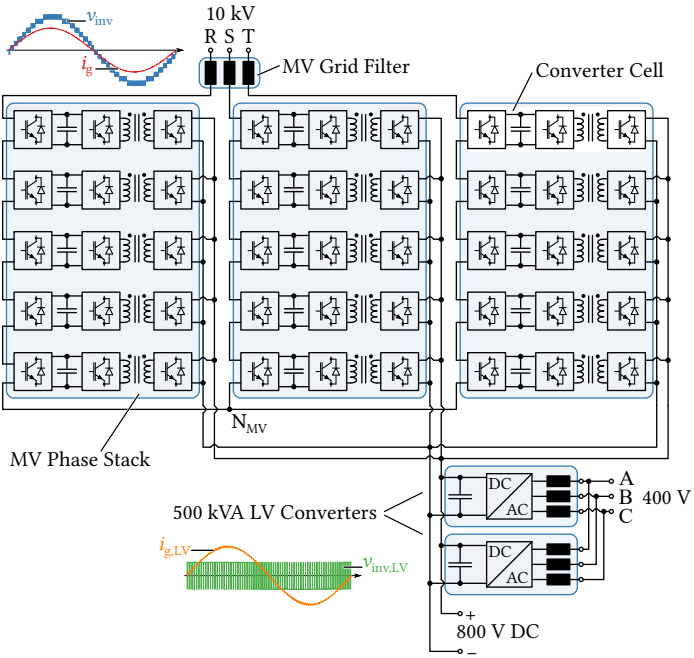


Fig. 4.1: Topology overview of the *MEGAlink* SST, including key voltage and current waveforms on the MV and LV grid sides, respectively.

4.1 The HC-DCM SRC in Phase-Modular SST Systems

While direct matrix-type AC-DC-AC converter structures have been discussed in literature (cf., e. g., [49]), the majority of all proposed SST concepts relies on a modular approach to handle high grid voltages on the MV side (cf. **Chapter 1**). Cascading several converter cells, each consisting of an ARU and a series connected isolated DC-DC converter with fixed voltage transfer ratio, allows to generate a filter-friendly multilevel output waveform; furthermore, using an ISOP configuration of the cells (cf. **Fig. 4.1**) contributes significantly to the overall voltage scaling between MV and LV side.

However, such designs are phase-modular on the MV side, meaning that they consist of three individual single-phase systems. Assuming the phase angle between grid voltage and current, φ, to be zero, neglecting the ARU

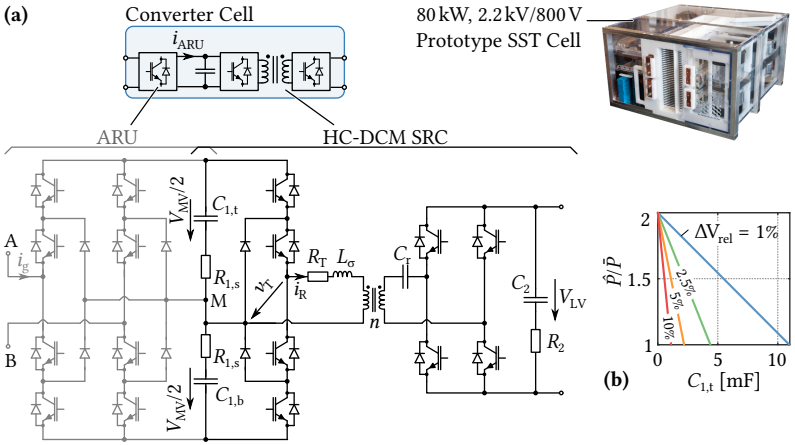


Fig. 4.2: (a) Topology of the converter cell of the considered IBE SST shown in **Fig. 4.1** and photo of realized prototype [136]; **(b)** trade-off between MV-side capacitance and ripple of the power processed by the DC-DC converter; ΔV_{rel} denotes the relative peak-to-peak MV DC voltage ripple ($C_{1,\mathrm{t}} = C_{1,\mathrm{b}}$).

switching, denoting the modulation index with M, and the MV DC link voltage with V_{MV}, the input power of one cell is given by

$$p(t) = 0.5\hat{i}_{\mathrm{g}} M V_{\mathrm{MV}} \cdot \left(1 - \cos(2\omega_{\mathrm{g}} t)\right) . \tag{4.1}$$

Accordingly, each cell processes a power fluctuating with twice the grid frequency. This single-phase power ripple at twice the grid frequency could be propagated through the cells' DC-DC converters to the LV side, where the instantaneous power contributions of the three MV phases ideally add up to a constant value. Doing so allows to reduce the capacitance on the cell's MV side as illustrated by **Fig. 4.2b**, but on the other hand increases the losses in the DC-DC converter due to increased RMS currents.

If the DC-DC converter is realized as a DAB, an arbitrary choice in the aforementioned trade-off can be made by suitable control of the power flow in the DC-DC converter. On the other hand, e. g., a triangular current modulation scheme of a DAB inevitably involves turning off the peak transformer current [119, 123], which causes high switching losses if heavy duty Si power devices are used, and hence is contrary to achieving a high efficiency.

The HC-DCM SRC can avoid these problems, and is generally an interesting solution for multi-cell systems, because of its autonomous operation

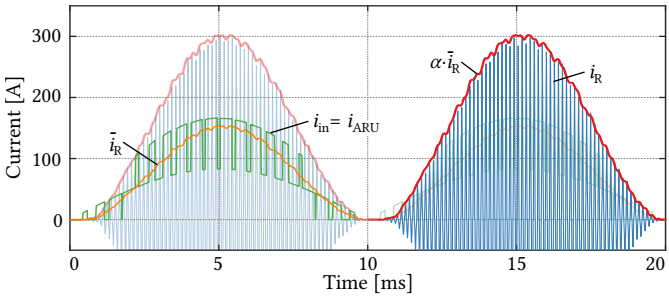


Fig. 4.3: Simulated waveforms of the circuits shown in **Fig. 3.9a** and **c** for pure active power transfer from the grid. i_{ARU} denotes the output current of the cell's ARU stage (cf. **Fig. 4.2a**), and $\alpha = \hat{i}_R/\bar{i}_R$ as dervied in Section 3.2.

(cf. Section 3.2). However, this converter does not offer any control possibilities; instead, it couples the two DC voltages through certain dynamics with fixed voltage transfer ratio. This leads to a propagation of the input side power fluctuations through the SRC to the common LV bus, which has certain consequences on the converter design.

Following [135], this section uses the dynamic model of the HC-DCM SRC that has been derived in Section 3.2 to discuss and optimize the choice of the input and output side DC capacitances of the DC-DC converter cell with respect to the placement of the converter's system level resonances, such as to obtain minimum volume and losses. Finally, aspects related to the design of a scaled demonstrator system featuring similar dynamic behavior as the full-scale system are addressed.

4.1.1 The HC-DCM SRC in Three-Phase IBE-SSTs

As described in Section 3.1 and Section 3.2, the HC-DCM SRC couples the MV and the LV DC link voltages tightly but passively with certain dynamics. There is no control possibility and the power transfer is mainly determined by the difference of the two DC voltages. As indicated above, the power contributions of the three MV phases ideally add up to a constant value at the common LV DC bus, which means that, assuming system-wide power balance and neglecting switching frequency components, this LV DC voltage is constant, whereas the MV-side voltage inevitably shows a ripple at twice the grid frequency for finite capacitances. Therefore, the full power ripple is transferred through each DC-DC converter cell (cf. **Fig. 4.3**), increasing the

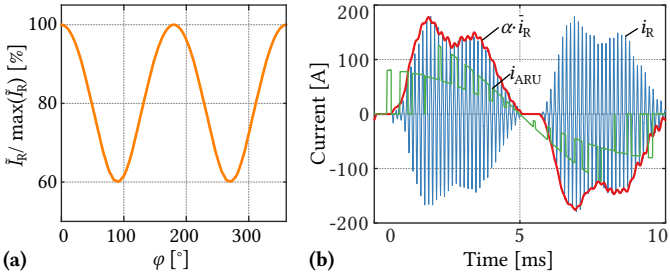


Fig. 4.4: (a) Relative $\tilde{I}_R$ for various grid current phase angles; **(b)** simulated example for $\varphi = 90°$ (note that $\alpha \bar{i}_R < 0$ corresponds to reversed power flow).

maximum peak transformer current, $\hat{I}_R$, by a factor of 2, and the RMS current (considering a whole grid period), $\tilde{I}_R$, by a factor of $\sqrt{3/2} = 1.225$ with respect to constant transmission of the average power.

An important aspect is the behavior in the case of reactive power compensation on the MV side: essentially, reactive power compensation is shifting instantaneous power between the MV phases, which, in a phase-modular SST, means through the DC-DC converters and via the LV-side DC link. **Fig. 4.4a** shows $\tilde{I}_R$ as a function of the grid current phase angle, φ, assuming a constant grid current amplitude. Even at $\varphi = \pm 90°$, $\tilde{I}_R$ still amounts to 60 % of its value for full active power transfer. The simulated waveforms from **Fig. 4.4b** illustrate that the power flow direction alternates with twice the grid frequency. On the other hand, there is no basic need to provide sufficient capacitance on the MV side to buffer the full power ripple (cf. **Fig. 4.2b**), thereby trading capacitor volume against losses. As an aside, note that the control unit needs to change the actively switched bridge (i. e., MV or LV side) of the DC-DC converter twice per grid period according to the power flow direction. To do so, the low-pass filtered DC voltages (to remove switching-frequency components), $V_{MV}/2$ and V'_{LV} (cf. **Fig. 4.2a**), are compared and the bridge with the higher voltage is actively switched.

In the following, three approaches to cope with and/or to mitigate the power ripple transmission through the HC-DCM SRC cells in phase-modular SSTs are discussed and compared.

Adapted Design

For the case of constant transfer of the average power, i. e., without any grid-frequency power fluctuation, the solid curves (index $_{...,A}$) in **Fig. 4.5a**

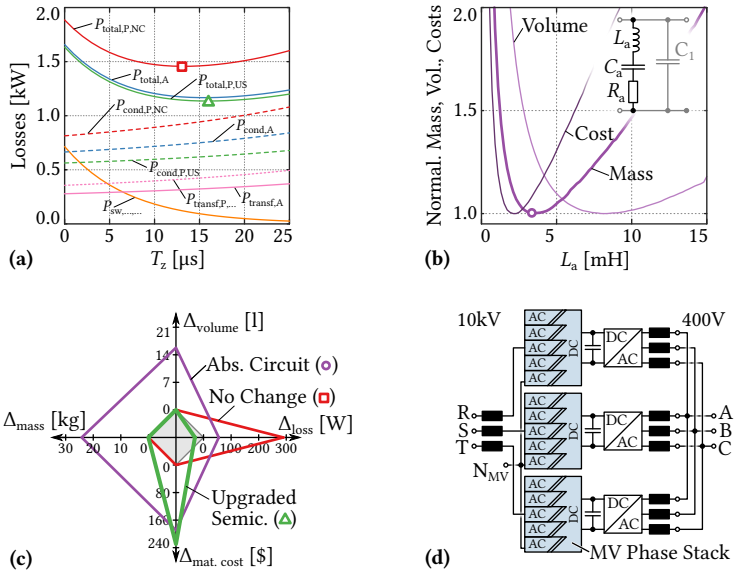


Fig. 4.5: (a) Converter losses for average and pulsating power transfer (cf. **Tbl. 3.1** for specifications). Index …,A denotes averaged power transfer, index …,P,NC denotes pulsating power transfer without changed power semiconductors, and index …,P,US denotes pulsating power transfer with upgraded power semiconductors. **(b)** Optimization of the absorption circuit. **(c)** Comparison of the two approaches on the basis of one converter cell; the symbols in parentheses refer to the respective designs in (a) and (b). **(d)** Overview schematic of a fully phase-modular SST system.

show the dependence of loss components in the SRC on the zero-current interval duration, T_z; the mentioned optimum is clearly visible. The switching losses arising in IGBTs even under ZCS conditions due to the stored charge dynamics are estimated using the stored charge model introduced in [139] and then verified for the HC-DCM SRC operating mode in Section 3.3. Conduction losses are modeled based on datasheet information for 150 A/1700 V Si IGBT modules on the MV side and 200 A/1200 A devices on the LV side. Transformer core losses are calculated, transformer winding losses are obtained using AC resistance measurements of a fully rated prototype transformer.

The dotted curves (index …,NC) indicate the corresponding losses for full propagation of the power fluctuation through the SRC. Whereas the switching losses do not change because they are proportional to the peak currents and

therefore average out to the same value over a grid period, RMS-related losses in the transformer winding and also in the power semiconductors increase considerably; note that the optimum T_z therefore becomes shorter.

Recalling that the peak current increases by a factor of 2 for pulsating power transfer, clearly the power semiconductor modules must be upgraded such that the peak currents remain below their ratings, i. e., in the case at hand an upgrade to 300 A/1700 V and 450 A/1200 A types is required. The dashed curves (index $_{\ldots,\mathrm{US}}$) in **Fig. 4.5a** show the resulting losses, which in case of upgrading are in total more or less the same as in the case of averaged power transfer, since the reduction of semiconductor conduction losses overcompensates the increased transformer copper losses. Of course, it would also be possible to additionally adapt the transformer design in order to accommodate more copper cross section for the windings, but it is not necessary in order to retain the initial efficiency.

Absorption Circuit

An option to achieve again averaged power transfer through the HC-DCM SRC consists of connecting an absorption circuit in parallel to the MV-side DC link of each cell, i. e., between the positive and the negative DC rail of the cell's MV side circuitry, as known from traction applications (cf. **Fig. 4.5b**). This resonant circuit can be tuned to twice the grid frequency, thus providing a shunt path for the corresponding power fluctuation. The elements L_a and C_a are related via $2\omega_\mathrm{g} = 1/\sqrt{L_\mathrm{a}C_\mathrm{a}}$, but their ratio can be varied to optimize different targets as is illustrated in the figure. Capacitor volume and mass are modeled assuming a constant energy density of 6.3 cm³/J (found from averaging datasheet values of film capacitors from different manufacturers). For each L_a value, an inductor is locally optimized by sweeping over a wide range of core and winding geometries, considering laminated steel cores and solid copper conductors, the minimum volume design for each inductance value is then used.

However, as can be seen from the comparison shown in **Fig. 4.5c**, where material costs are estimated using [146], the absorption circuit approach is not competitive and hence not considered further, since it contributes additional mass and volume (consider here also that the *MEGAlink* SST consists of 15 cells in total!), while not reducing costs nor losses when compared to simply upgrading the power semiconductors as described before.

Full Phase Modularity

The main reason for the complete transmission of the power ripple through the HC-DCM SRC is that the LV-side DC voltage is constant because of the three-phase power being constant, as has been pointed out earlier. By changing the overall SST structure to a fully phase-modular variant, as shown in **Fig. 4.5d** (note that then one of these phase assemblies corresponds to a traction application), the LV-side DC link voltages are not necessarily constant anymore, they can also vary at twice the MV grid frequency.

It can be shown that the amount of transferred power ripple then depends mainly on the ratio between the MV-side capacitance and the effective LV-side capacitance (which is a combination of the cell's own capacitance and the common inverter capacitance). While in the case of full phase-modularity there is thus at least the option to influence (not control!) the share of the power ripple propagated through the DC-DC converter, the approach suffers from other shortcomings: Besides the comparatively high price in terms of capacitance requirements to gain (limited) influence on power ripple propagation (three inverter stages), the main disadvantage is the more complicated and less efficient symmetrization of an asymmetric loading on the LV-side grid towards the MV grid because there is no common LV DC link.

Conclusion

All in all, the above considerations show that the transmission of the full single-phase power ripple through the DC/DC converter cannot be avoided in a feasible way when a HC-DCM SRC is employed in an IBE SST, but on the other hand can be handled without compromising the high efficiency, provided a simple upgrade of the power semiconductors is carried out.

4.1.2 Design Considerations

Thus, the HC-DCM SRC is well suited for application in the converter cells of phase-modular SSTs. In this section, some design aspects are explored based on the derived dynamic equivalent circuit (cf. Section 3.2).

Analysis Based on Transfer Functions

So far it is clear that the converter design must be able to handle transmission of the power ripple at twice the grid frequency, which has some implications on the proper choice of the DC link capacitors in addition to voltage ripple considerations alone. Starting from the dynamic equivalent circuit introduced

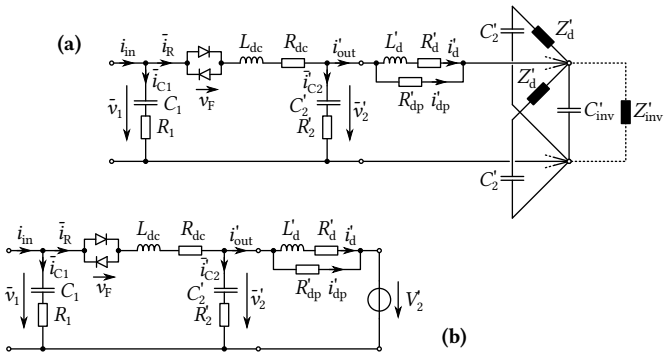


Fig. 4.6: Equivalent circuits of an SST cell, with **(a)** including a model of the LV-side DC bus assembly including the other converter cells, and **(b)** with simplification $C_{inv} \to \infty$. Z'_{inv} in (a) represents the input impedance of the LV-side DC-AC inverter, which is, however, not considered here.

in Section 3.2, **Fig. 4.6a** and **b** show extended versions that include additional parts of the overall SST, namely a decoupling inductor, L_d, a damping resistor, R_{dp}, the common LV inverter's DC link capacitor, C_{inv}, and the other converter cells' LV sides. The LV-side busbar assembly interconnecting the cells and the inverter stage inevitably features parasitic inductances, which can easily amount to several hundred nH, creating a parasitic resonance with the DC link capacitors. Providing a dedicated decoupling inductor in each cell prevents the propagation of HF currents across the busbar assembly and offers an additional degree of freedom to place the resonances of the converter dynamics such as not to coincide with, e. g., the switching frequency harmonics.

In essence, the HC-DCM SRC couples the two DC links through a multi-resonant network. The corresponding transfer functions can be calculated analytically, but the expressions become very complicated. Therefore, **Fig. 4.7** shows the magnitudes of the transfer functions $G_R = \underline{i}_R / i_{in}$, $G_{R,C\to\infty}$, and $G_{Out,A,C\to\infty} = i'_{out} / i_{in}$, the latter two assuming an infinite C_{inv} (cf. **Fig. 4.6b**). This assumption is required at $2f_g$ anyway as discussed earlier (no voltage ripple in the LV DC voltage at $2f_g$, i. e., "infinite capacitance", since the contributions of the three MV phases add up to zero), but does also not affect the HF region of the transfer functions, as can be seen from the figure; although the minor parasitic resonance caused by the presence of the other cells is then neglected.

Note that damping corresponds to losses; accordingly, the system reso-

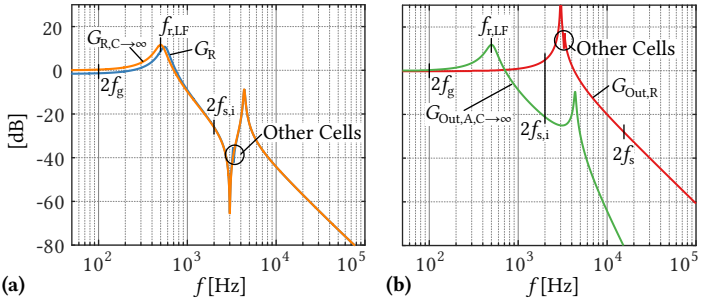


Fig. 4.7: Key transfer functions of the equivalent circuits shown in **Fig. 4.6**: $G_R = \tilde{i}_R/i_{in}$, $G_{R,C\to\infty} = G_R$ but considering $C_{inv} \to \infty$, and $G_{out,A,C\to\infty} = i'_{out}/i_{in}$ using the same approximation. $G_{out,R} = i'_{out}/i_R$, where i_R is the actual, i. e., switched, resonant current. The specifications used to generate the plots are given in **Tbl. 3.1**, from which $R_{dc} = 59.6\,\text{m}\Omega$ and $L_{dc} = 35\,\mu\text{H}$ follow. Furthermore, $L'_d = 20\,\mu\text{H}$ and $R'_d = 1\,\text{m}\Omega$ are considered. Note that the $R'_{dp} = 5\,\Omega$ damping is chosen very low in order to highlight the resonances caused by the other cells' DC link assemblies.

nances shown in **Fig. 4.7** are as lightly damped as possible in the interest of high efficiency, making it mandatory to carefully choose their locations in the frequency spectrum in order to prevent an excitation by harmonics of the processed currents. The input current to the DC-DC converter consists, apart from its DC component, of major AC components at $2f_g$, but resulting from the interleaved switching of the ARU stage's two bridge legs (cf. **Fig. 4.3**), also at $2f_{s,i}$, where $f_{s,i}$ is the switching frequency of one of the two bridge legs. To avoid excess current stress in the DC-DC converter, it is essential to place the LF resonance of G_R at $f_{r,LF}$, which is mainly given by C_1 and the sum of L_{dc} and L_d (cf. also **Fig. 4.8a**, and (4.2)), such that the gain is close to 0 dB at $2f_g$, and clearly negative at $2f_{s,i}$. It should be highlighted that this implies an upper limit for C_1 (or for $C_{1,t} = C_{1,b}$, respectively), unless it would be chosen large enough to move the resonance sufficiently below $2f_g$, which is not possible with realistic capacitor values. Note that L_d can be used as a second degree of freedom to place $f_{r,LF}$. Furthermore, the HF resonances of G_R and $G_{Out,A,C\to\infty}$, which depend mainly on L_d and C_2, should not coincide with the main ARU switching frequency component at $2f_{s,i}$.

In addition, **Fig. 4.7b** shows the transfer function $G_{Out,R} = i'_{out}/i_R$, which is valid for the actual (i. e., switched) resonant current, i_R, flowing into the LV-side DC bus after being rectified by the LV-side converter bridge (cf. **Fig. 4.2**). Its resonance must be significantly below twice the DC-DC converter

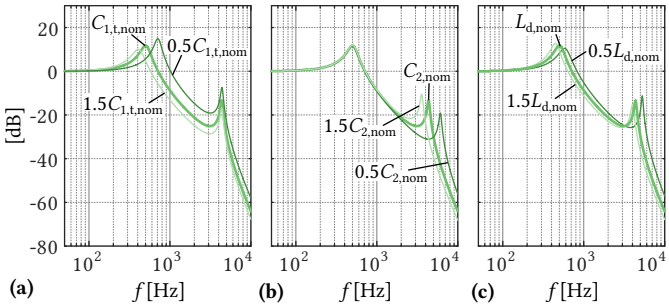


Fig. 4.8: Influence of the main parameters on the transfer function $G_{\mathrm{Out,A,C}\to\infty}$: **(a)** MV capacitor, $C_{1,\mathrm{t}}$; **(b)** LV capacitor, C_2; and **(c)** decoupling inductor, L_d.

switching frequency, $2f_\mathrm{s}$, which can be achieved by proper selection of L_d and C_2. Note that an adjustment of L_d affects also the LF resonance (whose location is quite critical as discussed above), whereas this is not the case when C_2 is adjusted to obtain a desired attenuation at $2f_\mathrm{s}$ (cf. **Fig. 4.8b** and **c**).

Design Optimization

Assuming a given transformer and given power semiconductors, R_dc and L_dc are fixed. In addition, it is assumed that for reasons of efficiency the resistors R_1, R_2, and R_d are comparatively small and not actively used as damping elements; specifically, they are set to 1 mΩ each for the optimization. Then, there are still four degrees of freedom left to influence the transfer function resonances, namely the two DC link capacitors, $C_{1,\mathrm{t}} = C_{1,\mathrm{b}}$ (or C_1) and C_2, the decoupling inductor, L_d, and also the damping resistor, R_dp. By sweeping those over wide ranges, a large number of designs based on specifications according to **Tbl. 3.1** is calculated by utilizing the transfer functions, each design featuring specific losses, voltage ripples, etc.

In **Fig. 4.9**, the increase of overall conduction losses (V_F, R_dc, R_d, R_dp, etc.) with respect to the best design is plotted for all combinations, where for each tuple $\{C_{1,\mathrm{t}}, C_2, L_\mathrm{d}\}$ the R_dp resulting in lowest losses has been considered. To establish lower limits for the capacitors, all designs that result in a relative DC voltage ripple of more than 7.5 % are grayed out. It can be seen that with small L_d values (1 µH) larger capacitors are required to achieve low losses, while very large L_d values (50 µH) are not interesting, too. However, for intermediate values there is a region (note that too large capacitances are also suboptimal, as expected from the transfer functions), within which designs with minimum

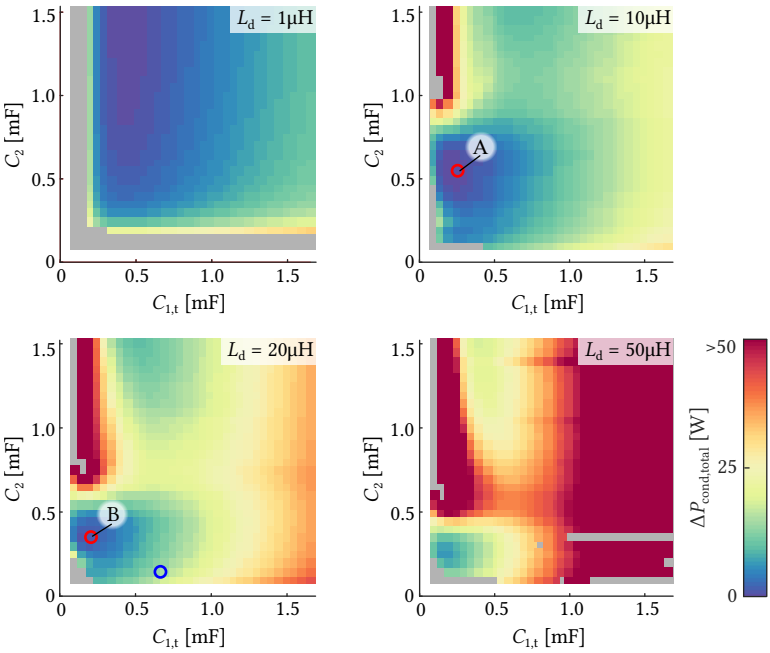


Fig. 4.9: Grid search result overview where the color encodes the overall conduction loss increase, $\Delta P_{\mathrm{cond,\,total}}$, with respect to the design with lowest losses.

losses can be found (cf. markings A and B, respectively).

Fig. 4.10 shows the corresponding losses vs. capacitance Pareto fronts for the four considered L_d values, which confirms that intermediate L_d values offer the best trade-off between capacitance requirements, which translate into volume, and losses. Considering the much lower capacitor values, B would be the recommended design, featuring the element values given in **Tbl. 4.1**. The total capacitor volume can roughly be halved with respect to the default design (cf. specifications in **Tbl. 3.1**) while the overall system losses can be reduced slightly, too.

Note, however, that the optimum is quite flat with respect to losses, e. g., the default design's (cf. **Tbl. 3.1**, blue circle in **Fig. 4.9**) conduction losses are less than 1.5 % higher than those of design B, although larger capacitors are used because of other system-level design considerations. On the other hand, even though the sensitivity to the parameters is low in the vicinity of the

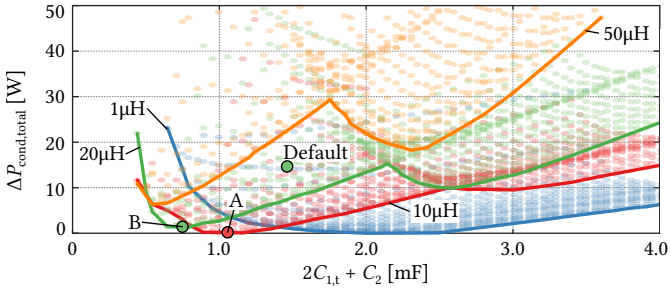


Fig. 4.10: Loss increase vs. capacitance Pareto fronts for four different L_d values with the two designs A and B from **Fig. 4.9** indicated.

Tbl. 4.1: Optimization results.

	$C_{1,\mathrm{t}} = C_{1,\mathrm{b}}$	C_2	L_d	Capacitor vol.
Default	660 µF	140 µF	20 µH	5.34 l
Optimized (B)	200 µF	350 µF	20 µH	2.24 l

optimum, **Fig. 4.9** clearly shows that there are parameter combinations that can lead to high losses because of badly placed resonances of the converter dynamics.

Finally, in order to illustrate the achievable performance, the power density of the built converter cell from **Fig. 4.2a** is roughly 1.5 kW/dm^3, including the ARU stage, isolated DC-DC converter (note that isolation considerations contribute significantly to the entire volume), air-cooling, all auxiliary systems, as well as structural parts. By reducing the capacitor volume as indicated in **Tbl. 4.1** it would be possible to improve the power density by adapting the mechanical design accordingly. The estimated full-load efficiency when transferring power (with single-phase power fluctuation) from the MV to the LV side is roughly 98.6 % for the DC-DC converter part, and roughly 98 % for the entire SST cell, i. e., including the ARU stage.

4.1.3 Scaled Demonstrator

In order to analyze control-related issues of the *MEGAlink* SST, a scaled demonstrator system featuring a full control system and the same power circuit structure as the real SST shown in **Fig. 4.1** and **Fig. 4.2a**, but scaled to

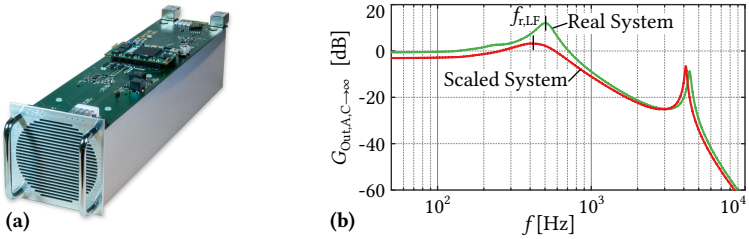


Fig. 4.11: (a) Scaled demonstrator SST cell providing a 100 V "MV" AC input (note that four cells will be cascaded to interface the 400 V grid) and an isolated 800 V LV DC output; **(b)** comparison of the main transfer function, $G_{\mathrm{Out,A,C}\to\infty}$, of the full-scale and the built scaled SST cell.

a lab-compatible power level (15 kVA, 400 V three-phase AC to 800 V DC to 400 V three-phase AC), has been developed (cf. **Fig. 4.11a**) [147].

In principle, the scaled system would show equal dynamics as the real system if all components were scaled such that the stored energy as well as the losses, both relative to the respective rated powers, would stay equal. While the first is easily achieved, usually a lower power system shows higher relative losses, which means higher damping. Since for low frequencies $G_{\mathrm{Out,A,C}\to\infty}$ can be approximated as

$$G^{\mathrm{simplified}}_{\mathrm{Out,A,C}\to\infty} \approx \frac{1}{C_1(L'_\mathrm{d} + L_\mathrm{dc})s^2 + C_1(R_\mathrm{dc} + R'_\mathrm{d})s + 1}, \tag{4.2}$$

which leads to a damping factor

$$\delta \approx \frac{R_\mathrm{dc} + R'_\mathrm{d}}{2(L_\mathrm{dc} + L'_\mathrm{d})}, \tag{4.3}$$

there is a degree of freedom to compensate the scaled system's higher relative resistance by means of increasing either L_σ or L_d. However, this also shifts the LF resonance, resulting in a trade-off between achieving similar resonance frequencies, $f_{\mathrm{r,LF}}$, or similar damping.

Fig. 4.11b shows the two transfer functions of the full-scale SST cell and the actually realized scaled version. In addition, **Fig. 4.12a** compares the measured step responses of the two systems, where it is clearly visible that the scaled system's response is somewhat slower and much better damped. Note that the temporary L_d used in the real system features a significantly higher R_d than what would be feasible during continuous full-power operation.

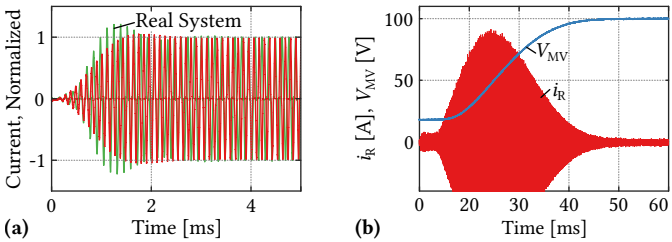


Fig. 4.12: (a) Comparison of the measured step responses of the real and the scaled system; **(b)** measurement of the scaled system's startup with an initially empty MV-side DC link.

Therefore, the measurement of the real system is better damped than the transfer function suggests. Nevertheless, the dynamics are matching quite well, allowing to use the scaled system to perform experiments that would be too expensive or cumbersome with a full-scale system.

As an application example, the startup process is looked at: if one DC link is charged while the other is not, the voltage excitation of the first resonant pulse would be high enough to excite destructive peak currents. Hence, one option to start the system is to start switching the HC-DCM SRC's active bridge before voltage is applied to any DC link, cf. e. g., [19, 126]. However, **Fig. 4.12b** shows measurements obtained from the scaled converter cell's startup with a charged LV DC link and an initially uncharged "MV" DC link. Here, the duty cycle of the switching LV bridge is ramped up very slowly from zero to about 50 % in steady-state, i. e., hard-switching transitions are used to crop the pulses at safe current levels. Thus it can be shown that HC-DCM SRC start-up with only one energized DC link is possible. Note, however, that this kind of duty-cycle control would not be feasible in steady-state operation due to the associated switching losses.

4.1.4 Summary

The HC-DCM SRC is a very suitable realization option for the isolated DC-DC converter with constant voltage transfer ratio that is required in the converter cells of phase-modular IBE SSTs, since it's ZCS/ZVS feature allows high efficiencies (cf. Section 3.3). However, the power flow through this type of converter is not controllable. Instead, the HC-DCM SRC couples the two DC voltages with certain dynamics that can be described by means of a passive dynamic equivalent circuit (cf. Section 3.2). The consequences of this dynamic

coupling, e. g., the propagation of the single-phase power fluctuation through the HC-DCM SRC, corresponding mitigation strategies, and design pitfalls resulting from the resonances of the converter dynamics have been discussed, and an optimization of the capacitance selection to result in small volume and low losses has been presented. If considered carefully during the design, the lack of controllability and the system dynamics of the HC-DCM SRC are not detrimental to its application in SST converter cells.

4.2 Common-Mode Currents in Multi-Cell IBE SSTs

Based on [148], this section presents a detailed analysis of the common-mode currents appearing in cascaded cells (AC-DC) converter systems as a consequence of steep changes of the cells' potentials caused by the individual cells' switching actions.

As has been discussed earlier, since the blocking voltage ratings of today's power semiconductors are limited, usually cascaded converter systems are used to interface the MV grid. The choice of the blocking voltage and hence the number of cascaded cells is an important design parameter. For the voltage and power ratings considered here (cf. **Tbl. 4.2**), it has been shown that systems based on LV power devices, i. e., 1700 V IGBTs, are Pareto-optimal regarding efficiency and power density (cf. **Chapter 2**).

Fig. 4.1 shows the *MEGAlink* multi-cell IBE SST system. In the following, only four (of the five) cascaded cells per phase are considered, because the fifth cell is a redundant cell that normally does not operate. **Fig. 4.2a** shows the power circuit of a single cell, consisting of a single-phase NPC ARU stage and a HC-DCM SRC isolation stage.

While there are many publications dealing with the reduction of common-mode voltages at the cascaded cells converter's output, which is important for, e. g., drive systems, by means of special modulation schemes [149–151], so far only a single paper discusses another common-mode-related phenomenon inherent to cascaded cells converter systems [152]: the potential of a cascaded cell's MV side with respect to ground cannot be fixed, instead it changes during every switching transition of any subjacent cell in the same phase stack. Each cell, however, has a certain capacitance to ground arising from, e. g., transformer windings, heatsinks, etc., that needs to be charged or discharged for the cell's midpoint potential to change, which gives rise to common-mode currents. Furthermore, it has been shown that severe oscillations between

Tbl. 4.2: Specifications of the multi-cell SST considered for the analysis of common-mode ground currents.

Rated power	1 MVA
MV grid voltage (line-line, RMS)	10 kV
LV grid voltage (line-line, RMS)	400 V
Cell ARU switching frequency (bridge leg)	1 kHz
Cell MV DC link voltage	2×1100 V
Cell LV DC link voltage	800 V

these parasitic ground capacitances and parasitic inductances of the cell interconnections can occur [152].

This section therefore provides a more detailed analysis of the phenomenon in Section 4.2.1 and Section 4.2.2, and discusses mitigation means in Section 4.2.3, where also comprehensive design guidelines for the most promising solution, i. e., common-mode chokes (CMCs) at each cell's AC terminals, are given.

4.2.1 Common-Mode Equivalent Circuit

In this and the next subsection, an analytical description of the common-mode currents arising in the cascaded cells converter is presented, where the analysis confines to a single phase without loss of generality, since the star point, N_{MV}, is assumed to be solidly grounded. To start, suitable equivalent circuits are derived.

Common-Mode Equivalent Circuit of a Converter Cell

A single converter cell's power circuit as shown in **Fig. 4.2a** can be simplified for common-mode analysis purposes, as for example suggested in [149]. To do so, the MV-side switches and DC link capacitors are replaced by stepped voltage sources with amplitude $V_{DC} = V_{MV}/2 = 1100$ V (corresponding to one half of the total MV-side DC link voltage), which results in the equivalent circuit shown in **Fig. 4.13a**. There, v_T and v_B for a certain cell are given by the switching state of that cell's ARU as

$$v_T = v_{AM} \qquad \text{and} \qquad v_B = -v_{BM}, \tag{4.4}$$

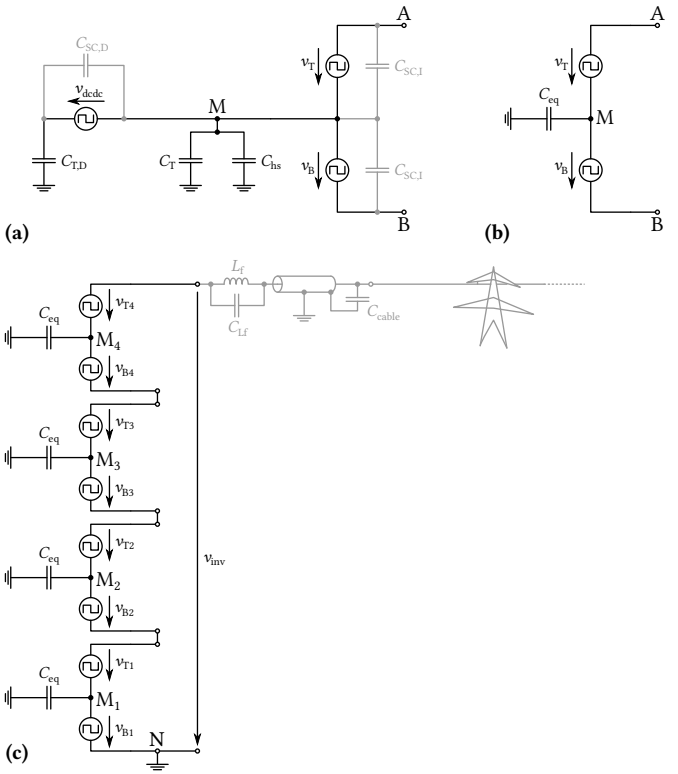


Fig. 4.13: (a) Common-mode equivalent circuit of a converter cell shown in **Fig. 4.2a**, including "local" common-mode effects and the DC-DC converter; **(b)** reduced version suitable for the analysis of "global" common-mode effects; and **(c)** corresponding common-mode equivalent circuit of a complete phase stack.

where A and B are the two AC terminals and where M denotes the DC bus midpoint as indicated in **Fig. 4.2a** and **Fig. 4.13a**. The grayed-out capacitances, $C_{sc,I}$ and $C_{sc,D}$, represent capacitances between semiconductor dies and the heatsink, which is connected to the MV-side midpoint, M. Any switching causes "local" common-mode currents through these capacitances. However, these currents flow only within a single cell and are not different from those present in any switching power converter. Therefore, these "local" common-mode currents are not considered further.

In contrast, any switching of the voltage source v_B, or of any other volt-

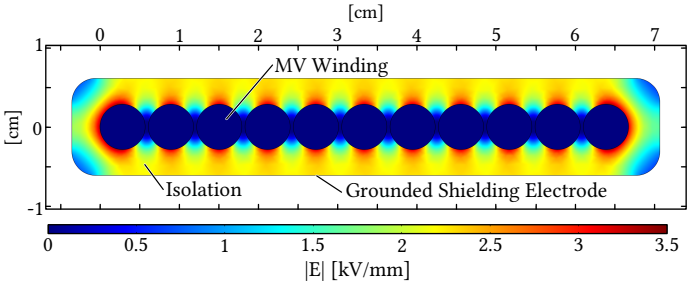


Fig. 4.14: Electrostatic FEM simulation of the transformer MV winding.

age source subjacent in the phase stack, will move the potential of the cell midpoint, M, with respect to ground. This will give rise to a current flow through the capacitance between the transformer's MV winding (note that one end of the MV winding is connected to the midpoint) and ground, C_T, as well as through C_hs, the capacitance between the cell structures on midpoint potential, such as the heatsink, and adjacent grounded parts such as cabinet walls. Additionally, also the switching of the DC-DC converter, represented by v_dcdc, causes common-mode currents through the capacitance between the transformer winding and ground, $C_\mathrm{T,D}$. However, these are independent of the cell's position in the phase stack and therefore not specific to cascaded cells systems; thus the DC-DC converter is not considered any further. Applying these simplifications yields the common-mode equivalent circuit of one converter cell as shown in **Fig. 4.13b**, where C_eq summarizes C_T and C_hs.

Due to the close geometric proximity of the MV winding on cell potential and grounded parts such as the core, which is mandatory to achieve good magnetic and thermal performance of the MFT, C_T can be assumed to dominate C_eq. Finite element simulation has been used to determine the parasitic capacitance of a transformer designed for the system under consideration. **Fig. 4.14** shows the corresponding electric field distribution, from which $C_\mathrm{eq} \approx C_\mathrm{T} = 650\,\mathrm{pF}$ is obtained.

Common-Mode Equivalent Circuit of a Phase Stack

Fig. 4.13c finally shows the common-mode equivalent circuit of a complete SST phase stack. The neutral point, N, is assumed to be solidly grounded, or at least directly connected to the aforementioned structures such as cabinet walls or transformer cores. In this second case, no direct ground connection

of the star point would be required, however, for safety reasons the voltage between N and ground would have to be kept small by suitable means.

Note that, in addition to C_{eq}, there is also a capacitive path to ground from the phase terminal via the parasitic capacitance of the filter inductor and the cable capacitance of a possibly connected MV cable. However, while these capacitances might be in the same order of magnitude as C_{eq} and need to be charged or discharged at every switching of any converter cell, the corresponding current spikes do not appear as common-mode current inside the converter structure, but only as a minor addition to the load current.

4.2.2 Analytical Description of Common-Mode Currents

The idealized equivalent circuit (not considering any parasitic inductances) depicted in **Fig. 4.13c** is now used to derive a basic analytic description of the common-mode currents flowing in the system.

The power semiconductors are impressing a high dv/dt during their switching transitions, $dv/dt = 15\,\mathrm{kV/\mu s}$ being a typical value for the IGBTs considered here. Assuming a constant dv/dt, the corresponding charging current for a cell's parasitic capacitance is given as

$$\hat{I}_{\mathrm{cm}} = C_{\mathrm{eq}} \frac{dv}{dt}. \tag{4.5}$$

A constant current with this magnitude flows until the capacitor is charged to the new voltage level. The current spike is therefore rectangular with magnitude $\hat{I}_{\mathrm{cm}}$ and a duration of

$$\Delta t = \frac{V_{\mathrm{DC}}}{\frac{dv}{dt}}, \tag{4.6}$$

where $V_{\mathrm{DC}} = 1100\,\mathrm{V}$, which is the voltage change resulting from any switching transition.

Consider now a cell at position k in the stack, where $1 \leq k \leq 4$ in the example system. If the voltage source $v_{\mathrm{B,k}}$ or the voltage source $v_{\mathrm{T,(k-1)}}$ is changing its voltage value as a result of corresponding switching actions, the midpoint potentials of cell k and of all cells at positions $l > k$ will change, requiring a current flow through their respective common-mode capacitances as described above.

Using PWM with phase-shifted carriers creates the desired multilevel output voltage waveform but implies that all cells are continuously switching with the same frequency, f_{s}. Thus, the higher a cell is positioned in the stack, the more common-mode current pulses it experiences per time.

RMS Common-Mode Current of Cell k

More precisely, every voltage source shown in **Fig. 4.13c** switches twice during a switching period, $T_\mathrm{s} = 1/f_\mathrm{s}$. Therefore, the midpoint of cell k experiences $2 \cdot (2k-1)$ potential changes during T_s. The RMS common-mode current flowing through the common-mode capacitance of cell k is thus given as

$$\begin{aligned}\tilde{i}_{\mathrm{cm,k}} &= \sqrt{\frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} i_{\mathrm{cm,k}}(t)^2 \, dt} = \sqrt{\frac{1}{T_\mathrm{s}} \sum_{\mathrm{j}=1}^{(4k-2)} \Delta t \hat{I}_\mathrm{cm}^2} \\ &= C_\mathrm{eq} \cdot \sqrt{f_\mathrm{s} V_\mathrm{DC} \frac{dv}{dt}} \cdot \sqrt{4k-2}. \end{aligned} \tag{4.7}$$

Note that therefore an effective capacitance for a cell at position k in the stack could be defined as

$$C^*_{\mathrm{eq,k}} = C_\mathrm{eq} \cdot \sqrt{4k-2}, \tag{4.8}$$

which is higher for cells at higher stack positions.

Total RMS Common-Mode Current

The common-mode currents of all cells flow back through the ground connection at node N in **Fig. 4.13c**. The magnitude of these current pulses depends on which cell, denoted by its position in the stack, k, is switching, namely $\hat{i}_{\mathrm{cm}\leftarrow\mathrm{k}} = (N-k+1) \cdot \hat{I}_\mathrm{cm}$. As mentioned above, there are two switching transitions of each voltage source in the equivalent circuit during one switching period. For $k > 1$, a switching transition of $v_{\mathrm{B,k}}$ has the same effect as one of $v_{\mathrm{T,(k-1)}}$, resulting in four corresponding current pulses per switching period. Thus, the total common-mode RMS current becomes

$$\begin{aligned}\tilde{i}_\mathrm{cm} &= \sqrt{f_\mathrm{s} V_\mathrm{DC} C_\mathrm{eq}^2 \frac{dv}{dt} \cdot \left(2N^2 + \sum_{\mathrm{k}=2}^{N} 4 \cdot (N-k+1)^2\right)} \\ &= C_\mathrm{eq} \cdot \sqrt{f_\mathrm{s} V_\mathrm{DC} \frac{dv}{dt} \cdot \left(\frac{4}{3}N^3 + \frac{2}{3}N\right)}. \end{aligned} \tag{4.9}$$

Verification

A complete simulation model of a single MV phase stack, featuring four cascaded cells including the DC-DC converter stages, has been implemented

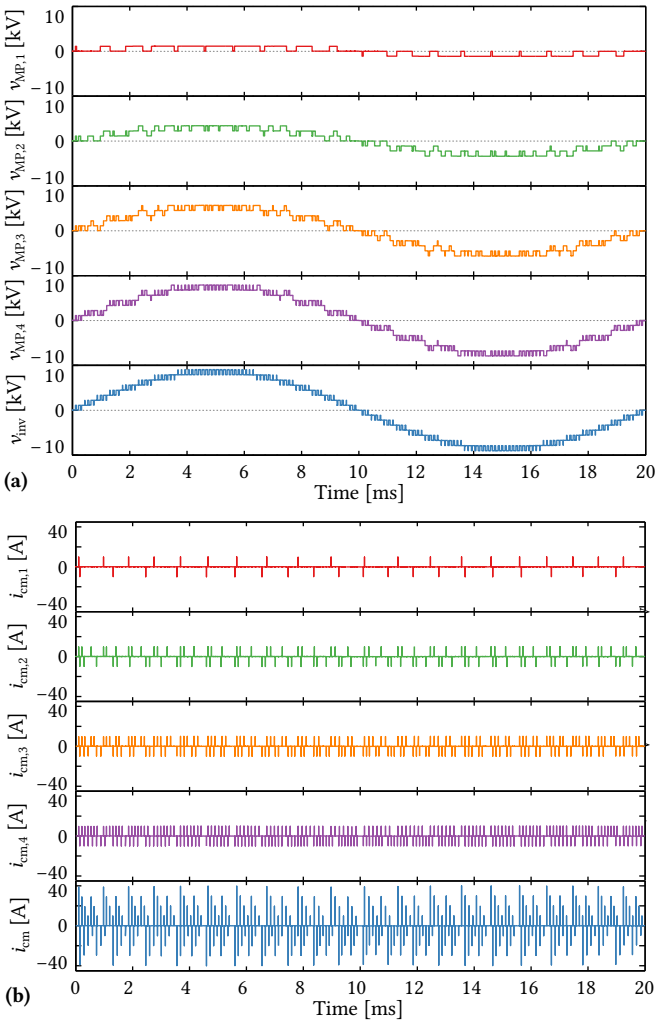


Fig. 4.15: Full-system simulation results for one SST phase considering $C_{eq} = 650\,\text{pF}$ and a dv/dt of $15\,\text{kV}/\mu\text{s}$. **(a)** shows the voltages between the cell midpoints and ground as well as the total phase stack output voltage, v_{inv}, and **(b)** shows the corresponding common-mode currents flowing through the cell's parastitic capacitances to ground, and also the total common-mode current, i_{cm}, flowing back through the node N.

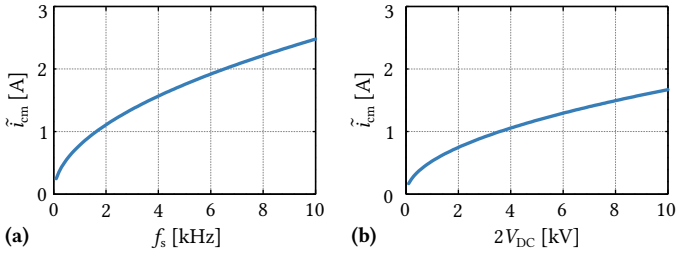


Fig. 4.16: (a) Dependence of the total RMS common-mode current, $\tilde{i}_{cm}$, on the cells' switching frequency, f_s, at $V_{DC} = 1.1\,kV$, and **(b)** on the cells' DC link voltage, V_{DC}, at $f_s = 1\,kHz$.

Tbl. 4.3: Calculated and simulated RMS common-mode currents.

	Calc. [mA]	Sim. [mA]	Error [%]
Cell 1	118.1	119.5	-1.17
Cell 2	204.5	206.7	-1.06
Cell 3	264.0	266.7	-1.01
Cell 4	312.4	315.6	-1.01
Total	783.2	790.9	-0.96

in GeckoCICRUITS [153] to verify the above calculations. Note that the fixed simulation time-step has to be chosen according to (4.6) in order to obtain a desired dv/dt. **Fig. 4.15a** shows the simulated cell midpoint voltages to ground and **Fig. 4.15b** shows the corresponding common-mode currents. The calculated and simulated RMS common-mode currents are listed in **Tbl. 4.3**, confirming the accuracy of the analytic calculations.

Parameter Influences

The validated analytic expressions allow to investigate the influence of certain system parameters on these common-mode currents. From (4.9) it can directly be seen that $\tilde{i}_{cm} \propto \sqrt{f_s}$ and $\tilde{i}_{cm} \propto \sqrt{V_{DC}}$, which is illustrated by **Fig. 4.16**. Note that if instead of a constant dv/dt a constant switching time for the voltage to rise from 0 V to V_{DC} would be considered, a linear dependency, $\tilde{i}_{cm} \propto V_{DC}$, would result.

Furthermore, there is a linear dependence on the parasitic capacitance, i. e., $\tilde{i}_{cm} \propto C_{eq}$ as shown in **Fig. 4.17**. There, also the fact that the RMS common-

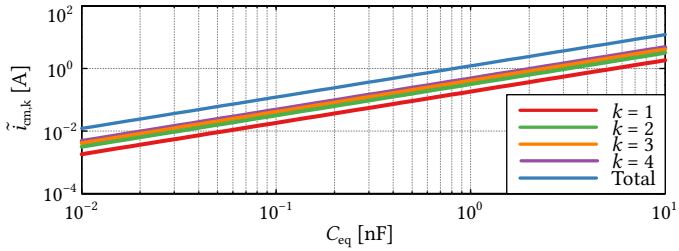


Fig. 4.17: Dependence of the individual cells' RMS common-mode currents, $\tilde{i}_{\mathrm{cm,k}}$, and of the total RMS common-mode current, $\tilde{i}_{\mathrm{cm}}$, on C_{eq}.

mode current increases with higher position of a cell in the stack, corresponding to increasing k, is clearly visible.

Influence of the Number of Cascaded Converter Cells

The choice of the optimum number of cascaded converter cells, $N = n_{\mathrm{cell}}$, for a given grid voltage level has been discussed in **Chapter 2**. It is thus interesting to assess the influence of N on the common-mode current stress in the system.

It has been shown that the following relations hold for a given output filter and constant output current ripple, i. e.,

$$V_{\mathrm{DC}} = V_{\mathrm{DC},0}\frac{N_0}{N} \quad \text{and} \quad f_{\mathrm{s}} = f_{\mathrm{s},0}\frac{N_0^2}{N^2}, \tag{4.10}$$

where $V_{\mathrm{DC},0}$, $f_{\mathrm{s},0}$ and N_0 are the parameters of a reference cascaded cells system. Coarsely approximated, the scaling behavior of the transformer stray capacitance is as follows: the cell power scales with $1/N$, but so does the cell DC voltage, resulting in the transformer current being independent of N, i. e., the required copper cross section remains constant and the same holds for the isolation distances, essentially leaving the cross section shown in **Fig. 4.14** unchanged, assuming an equivalent number of turns. Assuming further a constant switching frequency of the DC-DC stage, the required core area scales with $1/N$ since the applied voltage-time area does so. Consequently, the third dimension (e. g., the height) of the transformer scales with $1/N$, corresponding to an according reduction of the stray capacitance, i. e.,

$$C_{\mathrm{eq}} = C_{\mathrm{eq},0}\frac{N_0}{N}. \tag{4.11}$$

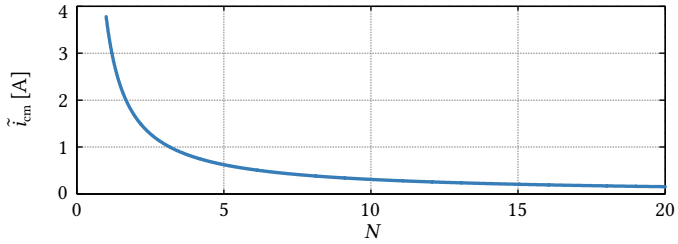


Fig. 4.18: Total RMS common-mode current, $\tilde{i}_{cm}$, as a function of the number of cascaded converter cells, N.

Inserting these dependencies in (4.9) yields

$$\tilde{i}_{cm}(N) = \sqrt{f_s \frac{N_0^2}{N^2} V_{DC} \frac{N_0}{N} C_{eq}^2 \frac{N_0^2}{N^2} \frac{dv}{dt} \cdot \left(\frac{4}{3} N^3 + \frac{2}{3} N \right)}, \tag{4.12}$$

which is plotted in **Fig. 4.18**. Even though the approximations are coarse and for example a scaling of the dv/dt with the switch voltage rating is not considered, the qualitative notion that an increasing number of cascaded cells results in lower total RMS common-mode current stress is very pronounced, since $\tilde{i}_{cm}(N) \propto \sqrt{N^3/N^5} \propto 1/N$.

Parasitic Inductances and Common-Mode Oscillations

So far, an idealized situation has been used to introduce the basic relations. However, additional parasitic elements, most prominentely series inductances of the interconnections of the cells, are present in a real system. **Fig. 4.19a** shows a common-mode equivalent circuit extended accordingly, where the series inductances are summarized as $L_{eq} = 100\,\text{nH}$. Severe oscillations between the parasitic common-mode capacitances and these series inductances have been described in [152]. Here, a more detailed theoretical analysis is presented.

Considering a single switching transition of the voltage source $v_{B,3}$ from $0\,\text{V}$ to V_{DC}, the circuit from **Fig. 4.19a** can be redrawn to obtain **Fig. 4.19b**, where for now $L_{cmc,L} = L_{cmc,G} = 0\,\text{H}$ is assumed (i. e., the case without any added CMCs is described). **Fig. 4.20** shows the Bode diagram of the transfer function

$$G_3(s) = \frac{I_{vB,3}(s)}{V_{B,3}(s)} = \frac{1}{Z_{T,3}(s)}, \tag{4.13}$$

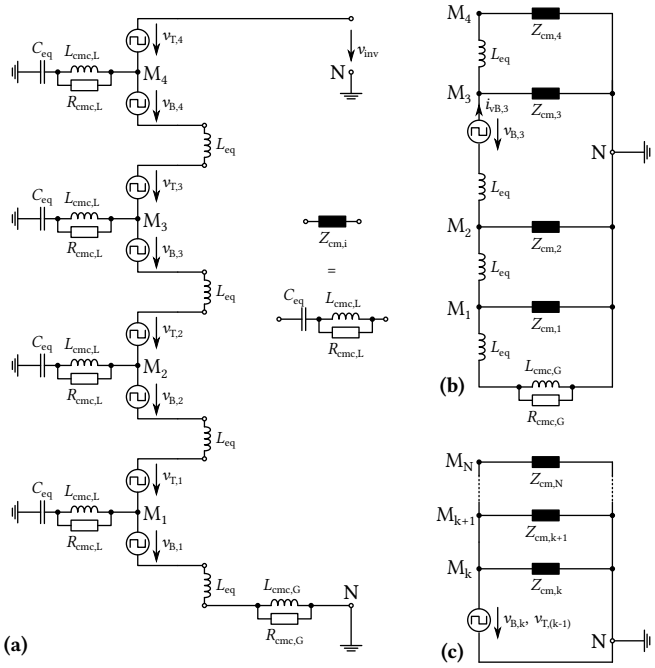


Fig. 4.19: (a) Common-mode equivalent circuit including parasitic inductances as well as local, i. e., per cell, common-mode chokes (CMCs), $L_{\mathrm{cmc,L}}$, and a global, i. e., per phase, CMC, $L_{\mathrm{cmc,G}}$. **(b)** Corresponding equivalent circuit for the case of a switching transition of the equivalent voltage source $v_{\mathrm{B,3}}$. **(c)** Simplified and generalized equivalent cicuit suitable for designing the local CMCs.

i. e., the transfer function from the voltage step to the resulting current flow through the switching voltage source, where $Z_{\mathrm{T,3}}(s)$ is the total impedance seen by the source in the circuit of **Fig. 4.19b**, including L_{eq}. As expected, severe resonances in the MHz-range are present. Although series resistances, e. g., semiconductor on-state resistances, etc., are not considered, these are required to be small from an efficiency point-of-view and therefore the provided damping is only minor.

4.2.3 Common-Mode Current Reduction Strategies

The analysis presented so far provides the basis to evaluate means for reducing the common-mode currents circulating in the system and to suppress the

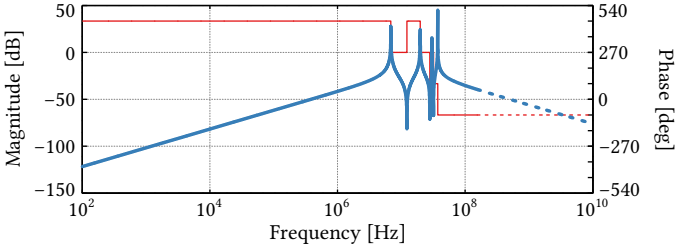


Fig. 4.20: Bode plot of the transfer function $G_3(s)$ (cf. **Fig. 4.19b**) for $C_{\mathrm{eq}} = 650\,\mu\mathrm{F}$ and $L_{\mathrm{eq}} = 100\,\mathrm{nH}$ and without any CMCs, i. e., $L_{\mathrm{cmc,G}} = L_{\mathrm{cmc,L}} = 0\,\mathrm{H}$.

severe common-mode oscillations indicated in **Fig. 4.20**.

Regarding the dependency of $\tilde{i}_{\mathrm{cm}}$ on the switching frequency, an obvious solution to mitigate common-mode currents would be to reduce the switching frequency, e. g., by using other modulation methods based on fundamental switching frequency at least for most of the cells [154]. However, such measures inevitably require increased passive filtering efforts to comply with harmonic standards.

Another approach would be to use dv/dt filters, as known from variable speed drive systems and described in, e. g., [155, 156], at the outputs of the individual converter cells. The downside of such filters is their differential-mode nature, which makes them potentially quite bulky.

Therefore, the most promising third option for reducing common-mode currents in the SST, common-mode choking, is investigated closer in the following.

Global CMC

A first approach could be to place a CMC at the output terminals of the complete phase stack. The global CMC increases the common-mode impedance at the stack output, i. e., suppresses common-mode currents flowing through the phase stack's output terminals, however, it does not prevent internal common-mode currents from flowing: Such a CMC, including a parallel damping resistor, appears in the common-mode equivalent circuit from **Fig. 4.19b** as $L_{\mathrm{cmc,G}}$ and $R_{\mathrm{cmc,G}}$. s **Fig. 4.21** shows the Bode plot of the accordingly adjusted transfer function $G_3(s)$. Even though the high global common-mode inductance creates a second, damped resonance at a much lower frequency, it does hardly affect some of the internal HF resonances occurring between the common-mode capacitances, C_{eq}, and the parasitic inductances, L_{eq}, *within*

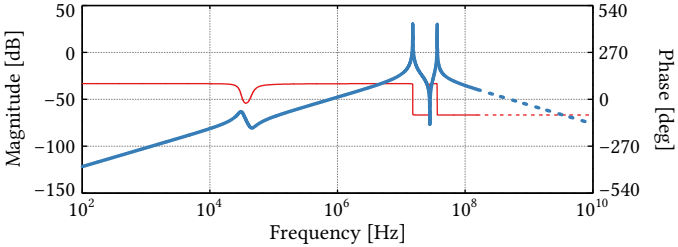


Fig. 4.21: Bode plot of the transfer function $G_3(s)$ for $L_{\mathrm{eq}} = 100\,\mathrm{nH}$, a global common-mode inductance of $L_{\mathrm{cmc,G}} = 10\,\mathrm{mH}$ and a parallel damping resistor of $R_{\mathrm{cmc,G}} = 10\,\mathrm{k\Omega}$.

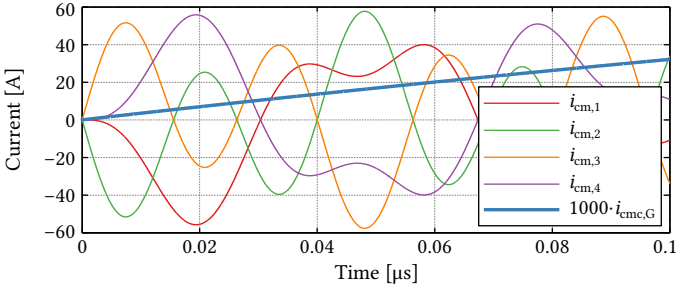


Fig. 4.22: Step responses of the common-mode currents, $i_{\mathrm{cm,k}}$, and the current in the global CMC, $i_{\mathrm{cmc,G}}$, for $L_{\mathrm{eq}} = 100\,\mathrm{nH}$, $L_{\mathrm{cmc,G}} = 10\,\mathrm{mH}$ and $R_{\mathrm{cmc,G}} = 10\,\mathrm{k\Omega}$.

the phase stack, which is in accordance with the findings reported in [152].

Similar to $G_3(s)$, transfer functions from the step voltage change to the common-mode currents flowing in the parasitic capacitances, C_{eq}, can be derived and **Fig. 4.22** shows the corresponding step responses. As expected, nearly undamped oscillations occur, where it should be noted that the initial current flow in the common-mode capacitances of the cells residing at lower stack positions than the switching voltage source is in the negative direction, i. e., discharging these capacitances, which results in an undesired lowering of these cells' midpoint potentials. This is a result of $L_{\mathrm{cmc,G}}$ very effectively suppressing the common-mode current flowing back through node N; the only other path for the required charging current inevitably involves the common-mode impedances of those cells initially not affected by the switching.

All in all, the above shows that common-mode choking at the phase stack terminals is not a feasible solution for mitigating common-mode current flows inside a multi-cell SST.

Local CMCs at Cell Inputs

Another option is to place "local" CMCs between the AC terminals of each individual cell, which appear as $L_{\mathrm{cmc,L}}$ and $R_{\mathrm{cmc,L}}$ in the equivalent circuit from **Fig. 4.19a**. This solution has been proposed in [152], but without consideration of the component design. Therefore, a detailed design guideline is provided in the following.

Design Equations The full transfer function, $G_3(s)$ given in (4.13), is a very complicated expression. However, since the parasitic inductances, L_{eq}, are much smaller than the common-mode inductances, $L_{\mathrm{cmc,L}}$, they can be neglected to reduce complexity and enable the derivation of straightforward design equations. In addition, no global CMC is present, which allows to reduce the equivalent circuit to that shown in **Fig. 4.19c**, where a generalized case is shown. With these simplifications, the simplified total impedance, $Z_{\mathrm{T,s,k}}$, seen by the switching source $v_{\mathrm{B,k}}$ (or, equivalently, $v_{\mathrm{T,(k-1)}}$), is given as

$$Z_{\mathrm{T,s,k}} = \frac{Z_{\mathrm{cm}}}{N-k+1}, \tag{4.14}$$

where

$$Z_{\mathrm{cm}} = \frac{1}{sC_{\mathrm{eq}}} + \frac{R_{\mathrm{cmc,L}} \cdot sL_{\mathrm{cmc,L}}}{R_{\mathrm{cmc,L}} + sL_{\mathrm{cmc,L}}}.$$

The simplified transfer function from the voltage step to the total common-mode current flowing through the voltage source is thus

$$\begin{aligned} G_{\mathrm{s,k}}(s) &= \frac{1}{Z_{\mathrm{T,s,k}}(s)} \\ &= \frac{(N-k+1)(s^2 C_{\mathrm{eq}} L_{\mathrm{cmc,L}} + sR_{\mathrm{cmc,L}} C_{\mathrm{eq}})}{s^2 C_{\mathrm{eq}} L_{\mathrm{cmc,L}} R_{\mathrm{cmc,L}} + sL_{\mathrm{cmc,L}} + R_{\mathrm{cmc,L}}}, \end{aligned} \tag{4.15}$$

which describes a second-order system.

With respect to reducing EMI, no oscillations are desired. On the other hand, while an overdamped response features a faster decay rate, this comes at the price of higher peak current values (and thus increased RMS current), since the total amount of charge that needs to be transferred is given by C_{eq} and the applied voltage step. Therefore, critical damping should be aimed at for an optimum design, which corresponds to the imaginary part of the poles of (4.15) being zero, i. e.,

$$L_{\mathrm{cmc,L}} = 4C_{\mathrm{eq}} R_{\mathrm{cmc,L}}^2. \tag{4.16}$$

Applying this condition to $G_{s,k}(s)$, the response to a voltage step of source $v_{B,k}$ (or $(v_{T,(k-1)})$ with magnitude V_{DC} can be calculated as

$$i_{cm,T,k}(t) = \frac{(N-k+1)V_{DC}}{4R_{cmc,L}^2 C_{eq}} \left(4C_{eq}R_{cmc,L} - t\right) e^{-\frac{t}{2C_{eq}R_{cmc,L}}}. \tag{4.17}$$

Note that the time integral of such a current pulse directly corresponds to the amount of charge required to increase the voltage of all affected, i. e., $(N-k+1)$, common-mode capacitances by V_{DC},

$$\int_0^\infty i_{cm,T,k}(t)dt = (N-k+1)\cdot C_{eq}V_{DC}. \tag{4.18}$$

The step response described by (4.17) features a time-constant

$$\tau = 2C_{eq}R_{cmc,L}, \tag{4.19}$$

and a peak value of

$$\hat{i}_{cm,T,k} = (N-k+1)\frac{V_{DC}}{R_{cmc,L}}. \tag{4.20}$$

Following the same procedure as in the idealized case (cf. (4.7) and (4.9)), the resulting RMS common-mode current flowing through node N can be calculated by replacing the rectangular current blocks with such of shape $i_{cm,T,k}(t)$. Defining

$$X(k) := \int_0^\infty i_{cm,T,k}^2(t)dt = \frac{5}{8}(N-k+1)^2\frac{C_{eq}V_{DC}^2}{R_{cmc,L}}, \tag{4.21}$$

the desired total RMS common-mode current becomes

$$\tilde{i}_{cm} = \sqrt{f_s \cdot \left[2X(1) + \sum_{k=2}^{N} 4X(k)\right]} = \sqrt{f_s \cdot \frac{5}{8}\frac{C_{eq}V_{DC}^2}{R_{cmc,L}} \cdot \left[\frac{4}{3}N^3 + \frac{2}{3}N\right]}. \tag{4.22}$$

Similarly, the RMS value of the common-mode current in cell l for $l \geq k$ is given by

$$\tilde{i}_{cm,l} = \sqrt{f_s \cdot (4l-2) \cdot \frac{5}{8}\frac{C_{eq}V_{DC}^2}{R_{cmc,L}}}. \tag{4.23}$$

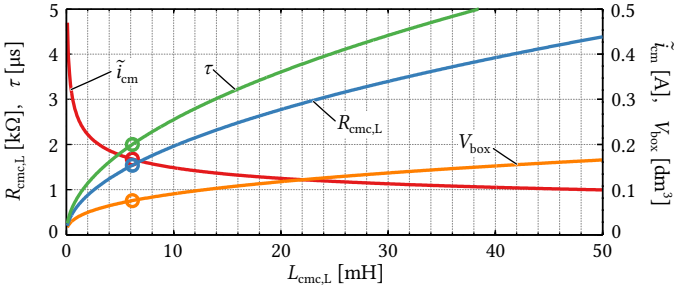


Fig. 4.23: Required damping resistor, $R_{\mathrm{cmc,L}}$, resulting time constant, τ, and RMS common-mode current, $\tilde{i}_{\mathrm{cm}}$, as functions of $L_{\mathrm{cmc,L}}$. The estimated boxed volume of the CMC, V_{box}, is also shown. The circles indicate the design selected for further evaluation (cf. text).

Using the current divider rule, the current flowing in $R_{\mathrm{cmc,L}}$ can be calculated as

$$\tilde{i}_{\mathrm{R,l}} = \sqrt{f_{\mathrm{s}} \cdot (4l-2)\frac{C_{\mathrm{eq}} V_{\mathrm{DC}}^2}{2R_{\mathrm{cmc,L}}}}. \tag{4.24}$$

Therefore, the power dissipated in the damping resistor becomes

$$P_{\mathrm{l,R}} = \tilde{i}_{\mathrm{l,R}}^2 \cdot R_{\mathrm{cmc,L}} = f_{\mathrm{s}} \cdot (2l-1) C_{\mathrm{eq}} V_{\mathrm{DC}}^2, \tag{4.25}$$

which is independent of the CMC and damping resistor, and amounts to negligible 5.5 W for $l = N = 4$ in the example system. The power dissipation in the CMC's series resistance, i. e., the windings, is anyway dominated by the differential-mode load current and will be addressed in the next section.

Example Design Eq. (4.22) serves together with (4.16) as design equation for the local CMCs and **Fig. 4.23** illustrates the design trade-offs. However, to choose a specific value of $L_{\mathrm{cmc,L}}$, an additional specification is required. In order for the common-mode current pulses to be short compared with the PWM pulses, the requirement $\tau \leq 0.2\,\% \cdot T_{\mathrm{s}} = 2\,\mu\mathrm{s}$ could be introduced. This results in $L_{\mathrm{cmc,L}} = 6.2\,\mathrm{mH}$, $R_{\mathrm{cmc,L}} = 1.539\,\mathrm{k\Omega}$ and $\tilde{i}_{\mathrm{cm}} = 167\,\mathrm{mA}$, as is indicated also in **Fig. 4.23**. Note that the RMS common-mode current is reduced by almost a factor of 5 when compared to the initial case (cf. **Tbl. 4.3**); a further reduction would come at the cost of very high $L_{\mathrm{cmc,L}}$ values.

Fig. 4.24 shows the Bode plot of $G_3(s)$, i. e., the full transfer function including L_{eq}, where the above values for $L_{\mathrm{cmc,L}}$ and $R_{\mathrm{cmc,L}}$ are used. The HF

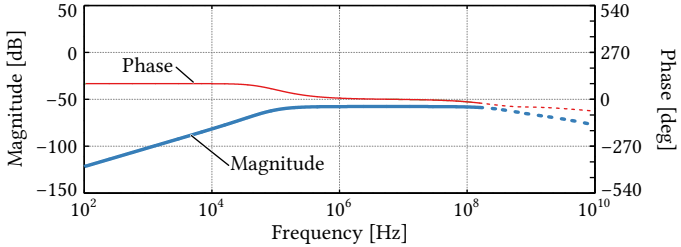


Fig. 4.24: Bode diagramm of $G_3(s)$ considering the designed local CMCs (cf. **Fig. 4.23**) and $L_{\text{eq}} = 100\,\text{nH}$.

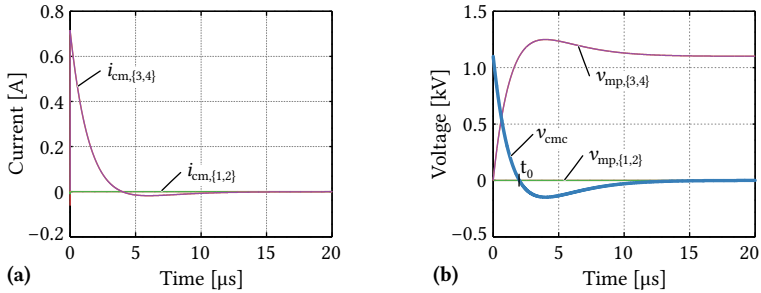


Fig. 4.25: Considering a step transition of $v_{\text{B},3}$, **(a)** shows the response of the common-mode currents and **(b)** shows the corresponding midpoint voltages, where also the voltage across a local CMC, v_{cmc}, is shown. Note that $L_{\text{eq}} = 100\,\text{nH}$ is considered in addition to the designed local CMCs.

resonances are successfully removed by the critically damped CMCs. This is also visible in **Fig. 4.25a** and **b**, where the corresponding responses of the common-mode currents and cell midpoint voltages to a step transition of the voltage source $v_{\text{B},3}$ are shown. Note that the peak value of $i_{\text{cm},\{3,4\}}$ follows from the voltage step (1100 V) and $R_{\text{cmc,L}} = 1.539\,\text{k}\Omega$.

Verification **Fig. 4.26** shows waveforms of the output voltage and total common-mode current (i. e., flowing through the ground connection at node N) obtained from a full-system simulation including the designed local CMCs. A massive reduction of the common-mode currents compared to those shown in **Fig. 4.15b** is obvious. **Tbl. 4.4** compares calculated and simulated RMS common-mode current values, which confirms the accuracy of the proposed analytic modeling, including the assumption $L_{\text{eq}} \approx 0$.

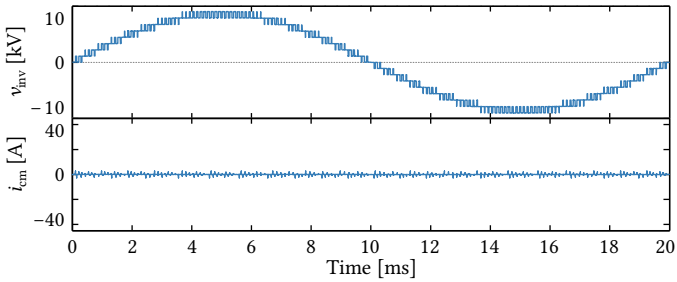


Fig. 4.26: Simulated phase stack output voltage, v_{inv}, and total common-mode current, i_{cm}, for the case of optimally damped local CMCs.

Tbl. 4.4: Calculated and simulated RMS common-mode currents with local CMCs.

	Calc. [mA]	Sim. [mA]	Error [%]
Cell 1	25.3	25.2	0.352
Cell 2	43.8	43.5	0.717
Cell 3	56.5	56.2	0.571
Cell 4	66.9	66.6	0.411
Total	167.7	166.7	0.615

CMC Design

With the required values of the local CMCs now being calculable, this section discusses the resulting size and losses of possible actual realizations. A key design parameter is the applied voltage-time integral, which follows from $v_{\mathrm{cmc}}(t)$ shown in **Fig. 4.25b** as

$$(vt) = \int_0^{t_0} v_{\mathrm{cmc}}(t)dt = \sqrt{L_{\mathrm{cmc,L}} C_{\mathrm{eq}}} V_{\mathrm{DC}} \mathrm{e}^{-1}, \tag{4.26}$$

where v_{cmc} is the difference between the applied voltage step and the voltage across the parasitic capacitance. Note that the simplified step response resulting from $G_{\mathrm{s,k}}(s)$ has been used to obtain this analytic result. However, the deviation from numeric integration of the full step response shown in **Fig. 4.25b** is only about 0.35 % for the values used here.

The two well-known inductor design equations become thus

$$\hat{B} = \frac{\sqrt{L_{\mathrm{cmc,L}} C_{\mathrm{eq}}} V_{\mathrm{DC}} \mathrm{e}^{-1}}{N A_{\mathrm{c}}} \quad \text{and} \quad J_{\mathrm{rms}} = \frac{2N\tilde{i}_{\mathrm{ph}}}{k_{\mathrm{w}} A_{\mathrm{w}}}, \tag{4.27}$$

where the factor 2 in the expression for J_{rms} accounts for the second CMC winding and where $\tilde{i}_{\mathrm{ph}}$ denotes the SST's MV RMS phase current. From these equations, the area product can be derived as

$$A_{\mathrm{c}} A_{\mathrm{w}} = \frac{2\sqrt{L_{\mathrm{cmc,L}} C_{\mathrm{eq}}} V_{\mathrm{DC}} \mathrm{e}^{-1} \tilde{i}_{\mathrm{ph}}}{\hat{B} k_{\mathrm{w}} J_{\mathrm{rms}}} \propto \sqrt{L_{\mathrm{cmc,L}}}. \tag{4.28}$$

Commonly, CMCs are realized using toroidal cores with an area product of (cf. **Fig. 4.27a**)

$$A_{\mathrm{c}} A_{\mathrm{w}} = (h \cdot (r_{\mathrm{a}} - r_{\mathrm{i}})) \cdot (\pi r_{\mathrm{i}}^2) = \pi s_{\mathrm{h}} s_{\mathrm{r}}^2 (1 - s_{\mathrm{r}}) \cdot r_{\mathrm{a}}^4, \tag{4.29}$$

where $s_{\mathrm{r}} = r_{\mathrm{i}}/r_{\mathrm{a}} = 0.7$ and $s_{\mathrm{h}} = h/r_{\mathrm{a}} = 0.7$, as found from averaging a range of suitable toroidal cores, are introduced to establish a dependency between the area product and the boxed volume of the resulting CMC. Neglecting the winding, the boxed volume of a toroidal coil is thus given by

$$V_{\mathrm{box}} = (2r_{\mathrm{a}})^2 \cdot h = (2r_{\mathrm{a}})^2 \cdot s_{\mathrm{h}} r_{\mathrm{a}}. \tag{4.30}$$

Solving (4.29) for r_{a} and inserting in (4.30) yields an estimate of the required CMC volume as a function of the area product,

$$V_{\mathrm{box}} = 4 s_{\mathrm{h}} \left(\frac{A_{\mathrm{c}} A_{\mathrm{w}}}{\pi s_{\mathrm{h}} s_{\mathrm{r}}^2 (1 - s_{\mathrm{r}})} \right)^{3/4}, \tag{4.31}$$

and substituting $A_{\mathrm{c}} A_{\mathrm{w}}$ with the expression from (4.28) leads to a direct dependence on the system parameters and the desired $L_{\mathrm{cmc,L}}$ value,

$$V_{\mathrm{box}} = 4 s_{\mathrm{h}} \left(\frac{2\sqrt{L_{\mathrm{cmc,L}} C_{\mathrm{eq}}} V_{\mathrm{DC}} \mathrm{e}^{-1} \tilde{i}_{\mathrm{ph}}}{\hat{B} k_{\mathrm{w}} J_{\mathrm{rms}} \pi s_{\mathrm{h}} s_{\mathrm{r}}^2 (1 - s_{\mathrm{r}})} \right)^{3/4} \propto L_{\mathrm{cmc,L}}^{3/8}. \tag{4.32}$$

Assuming $J_{\mathrm{rms}} = 5\,\mathrm{A/mm^2}$, $\hat{B} = 0.7\,\mathrm{T}$ for nanocrystalline core material such as Vitroperm [157], $k_{\mathrm{w}} = 0.1$ for a single-layer winding, and $\tilde{i}_{\mathrm{ph}} = 56.6\,\mathrm{A}$ corresponding to the phase current resulting from the specifications in **Tbl. 4.2**, yields the curve shown in **Fig. 4.23** and a volume estimate of $V_{\mathrm{box}} = 0.076\,\mathrm{dm^3}$ for the designed CMC with $L_{\mathrm{cmc,L}} = 6.2\,\mathrm{mH}$.

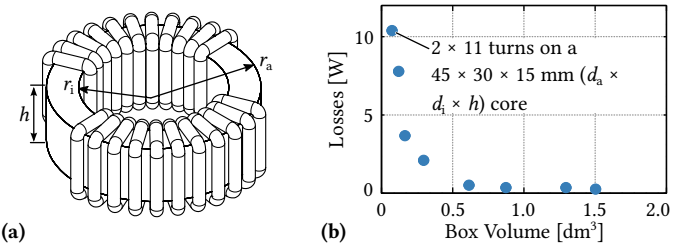


Fig. 4.27: (a) Geometric dimensions of the considered CMC and **(b)** thermally feasible CMC designs based on standard Vitroperm cores.

To back-up these approximations, a number of CMCs for $L_{\mathrm{cmc,L}} = 6.2\,\mathrm{mH}$ have been designed based on standard toroidal Vitroperm cores from VAC [157]. For each core geometry, the required number of turns to meet the above stated peak flux density has been calculated. Together with the requirement for a minimum spacing between the two windings (isolation requirements), the maximum possible wire diameter for single-layer windings and hence the losses caused by the load current can be calculated. Core losses are neglected due to the moderate peak flux density and the comparably low switching frequencies. Finally, the boxed volume is calculated taking into account also the windings. To account for thermal limitations, the box surface area, a heat transfer coefficient of $\alpha = 20\,\mathrm{W/(K \cdot m)}$ for natural convection, a maximum surface temperature of 100 °C and an ambient temperature of 50 °C are used to calculate the maximum allowable power dissipation, and any design exceeding this value is discarded.

Fig. 4.27 shows the resulting designs in a loss vs. volume plot, which confirms that a design with a volume of roughly $0.1\,\mathrm{dm}^3$ and about 10 W power dissipation is possible (cf. example design details in **Fig. 4.27**) and the estimate of the CMC volume based on $L_{\mathrm{cmc,L}}$ presented above gives acceptable results. Even though fifteen such CMCs are required for the complete three-phase SST, the additional volume and losses are negligible. Therefore, local CMCs designed as described above are a feasible means to suppress common-mode currents and associated resonant phenomena in cascaded cells converter systems.

4.2.4 Summary

Due to the high grid voltage levels, commonly multi-cell systems are employed in the MV interface of SSTs. Without proper countermeasures, the steeply

changing potentials within such cascaded cells converter systems give rise to high common-mode currents flowing through parasitic capacitances and potentially resonating with parasitic inductances. An analytic description of these effects as well as of the mitigation thereof by means of common-mode choking has been presented. In accordance with literature, placement of CMCs at the AC terminals of each individual converter cell has been identified as the most feasible solution and a detailed design guideline for such CMCs has been presented. Furthermore, the impact of the additional volume and losses has been shown to be negligible considering the overall SST system.

4.3 Volume/Weight/Cost Comparison of a Distribution SST Against a Conventional LFT

In today's distribution grids, conventional LFTs are ubiquitous at the interfaces between different voltage levels, where they provide voltage scaling and galvanic isolation. Because of the low operating frequency of 50 Hz or 60 Hz, LFTs are usually large and heavy devices. Their low complexity and passive nature is a benefit (high reliability) and a downside (no control possibilities) at the same time. The latter is increasingly limiting in the scope of recent developments such as the propagation of distributed generation systems on lower voltage levels and the Smart Grid paradigm in general, which implies a high degree of controllability of loads and also power flows. Controllability is an inherent feature of power electronic converter systems such as SSTs, which interface the grids on either side through power electronic converters and provide galvanic isolation by means of MFTs. Therefore, following [78], this section provides a comparison of a 1000 kVA three-phase distribution-type LFT and an equally rated IBE SST, with respect to volume, weight, losses, and material costs, where the corresponding data of the SST is partly based on characteristics of full-scale demonstrator of a cell of a 1 MVA SST (cf. **Fig. 4.1** and **Fig. 4.2a**).

4.3.1 Introduction

Commonly, reductions in size and weight are projected for changing from an LFT to an equally rated SST. However, whereas for traction systems a weight reduction of around 50 % at a 50 % higher price tag has been reported based on a 1.5 MVA prototype [24], literature provides only vague data for grid applications. In [14], a cost increase by a factor of ten is mentioned

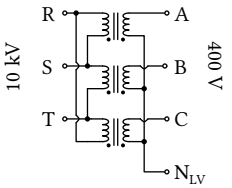


Fig. 4.28: Circuit schematic of a delta-wye connected LFT.

for grid-scale SSTs and small quantity production and [158] describes the optimization of a 150 kVA HF transformer for SSTs with respect to weight, volume and cost. A multi-dimensional comparison of cascaded converter designs with different numbers of levels for direct grid connection of wind turbines is described in [159], however, only power semiconductor costs are considered. Looking at lower power levels, [160] compares the cost of four different topologies suitable for a 50 kVA SST's MV-side converter and [161] provides a cost breakdown of a laboratory-scale prototype of an SST for wind energy applications and, as a side note, mentions an estimated cost reduction by a factor of five when moving from the laboratory prototype to series production. Recently, a single-phase, 13.8 kV/270 V SST based on SiC devices with 10 kV blocking voltage rating has been presented, apparently achieving a 75 % reduction in weight and a 40 % reduction in size compared with a conventional single-phase LFT [162]. However, for the time being, and probably also for several years to come, the industrial heavy-duty converter population is and likely will be dominated by proven and relatively low cost silicon technology.

Although, as has been tried to outline, research efforts in the SST area are diverse and exciting, no direct quantitative comparison of a fully rated three-phase AC-AC SST and a corresponding LFT has been reported so far. This section presents such a comparison of an exemplary 1000 kVA, 10 kV/400 V LFT, which is a typical unit rating found in European distribution systems, and an equally rated SST with respect to four key performance characteristics: weight, volume, material costs, and losses. The LV DC bus of the *MEGAlink* SST structure shown in **Fig. 4.1** could interface DC microgrids, e. g., in buildings, or also DC generators such as photovoltaics. Since such DC applications are becoming more and more important, scenarios where the LV-side output of the transformer involves 50 % or 100 % DC power are also considered in the comparison.

Material costs are estimated here by means of component cost models

for high-volume production as proposed in [146], i. e., it is important to highlight that all costs mentioned throughout this section comprise only material costs and hence are to be understood as lower bounds, not including labor costs, a certain share of development costs, profits, etc. In addition, this approach implies that only hardware costs are considered. In power systems engineering, however, usually a total cost of ownership (TCO) perspective is taken when evaluating the economical aspect of, e. g., equipment to reduce power quality issues [163], distribution system enhancement projects [164] or smart substations [165]. Therefore, this contribution should be viewed as a first step towards a comprehensive quantitative comparison of the costs of an SST and an LFT. The scope of the analysis presented here needs to be broadened in the future and the complete system consisting of the SST and the associated grid section should be taken into account whenever possible.

The section is structured as follows: Section 4.3.2 and Section 4.3.3 describe reference LFT data and the modeling of the SST, respectively, and Section 4.3.4 provides the results of the comparison between SST and LFT for different application scenarios as well as a discussion of these results.

4.3.2 LFT Performance Characteristics

Fig. 4.28 shows the basic circuit schematic of a three-phase LFT in delta-wye connection. The electrical part consists of two times three copper (or aluminum) windings and a magnetic core, which is usually made of low-loss silicon steel laminations. While dry-type solutions are available, distribution transformers with higher power ratings are typically immersed in oil to provide both, isolation and cooling.

Fig. 4.29 illustrates the largely linear dependency of weight and volume, respectively, on the rated power, based on data of a wide range of distribution transformers given in [166]. Usually, different transformer variants are available for a given power rating, which differ in their part load and full load efficiencies. This translates into different weights and sizes, since more or less active material, i. e., copper and silicon steel, is used. Consequently, a trade-off between purchase price and the cost of loss energy arising during the transformer's lifetime exists and an optimization can be performed, which is done within a TCO analysis.

Looking specifically at 1000 kVA units, datasheets of various manufacturers provide dimension, weight and loss information [166–168]. Averaging those values yields the volume and weight of a typical 1000 kVA LFT as 3.43 m^3 (4.48 yd^3) and 2590 kg (5710 lb), respectively, and an average full-load

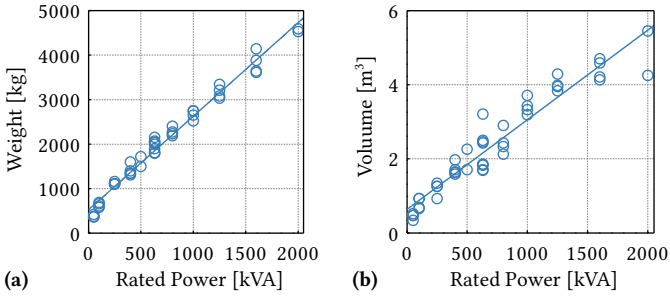


Fig. 4.29: Dependence of LFT weight **(a)** and volume **(b)** on the rated power; based on datasheet information from [166].

efficiency of 98.7 %. Note that the full-load efficiencies of the considered units vary between 98.5 % and 98.9 %, which is, however, not really relevant compared to the efficiency difference to an AC-AC SST, as will be discussed later.

The purchase price of a typical 1000 kVA distribution transformer is given as 16 kUSD in [169], and as 12 kEUR in [170], which corresponds to 16.2 kUSD (as of June 2014). Depending on the optimization target, as discussed above, prices may vary about ±35 % around this mean value. These numbers are also in agreement with pricing information obtained from a major European transformer manufacturer. According to [170], active material costs account for 50 % and overall material costs for 70 % of the transformer price. Thus, overall material costs of roughly 11.3 kUSD can be assumed for the exemplary 1000 kVA unit.

4.3.3 SST Performance Characteristics

While LFTs can be purchased off-the-shelf, no SST products do exist so far. Therefore, the four performance characteristics (weight, volume, material costs, and losses) of an exemplary SST realization are derived in this section, partly based on a hardware prototype of one converter cell [136] of a 1 MVA multi-cell SST (cf. **Fig. 4.1** and **Fig. 4.2a**).

Fig. 4.1 shows the basic schematic of the considered *MEGAlink* IBE SST circuit topology. The SST interfaces the MV grid through a cascaded cells converter system, where each of the cascaded converter cells (cf. **Fig. 4.2a**) features an isolated DC-DC converter, providing galvanic isolation by means of an MFT. **Fig. 4.30a** shows the MV converter's multilevel output voltage

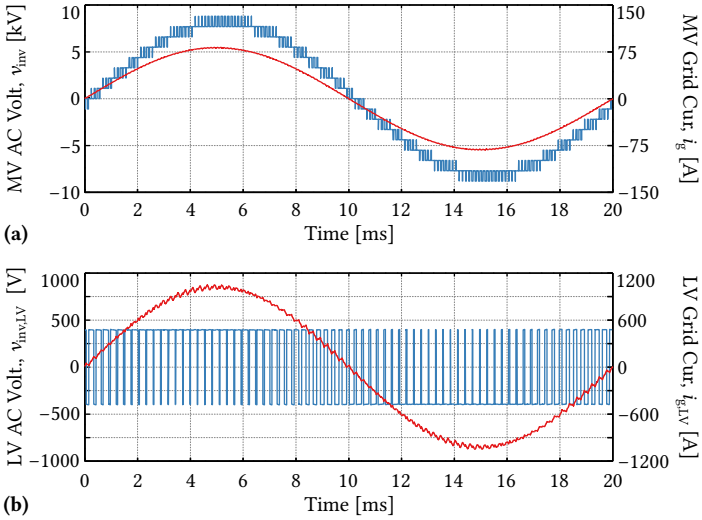


Fig. 4.30: (a) MV-side inverter voltage and resulting line current for **(a)** the cascaded 1000 kVA MV converter, and **(b)** corresponding LV-side waveforms for one of the 500 kVA LV converter units (cf. **Fig. 4.1**) for full-load active power operation.

and the resulting grid current at full-load operation.

On their LV side, all cells are connected to a common DC bus, which feeds two paralleled 500 kVA, three-phase inverters connected to the LV AC grid. Again, **Fig. 4.30b** shows the output voltage and the corresponding grid current for one of the two 500 kVA units.

The cascaded MV-side converter and the three-phase LV converter are discussed separately in the following two subsections, whereby, for the sake of brevity and clarity, the reader is referred to references for details on the models used.

MV-Side Cascaded Converter

Since today's Si power semiconductors are not available with blocking voltage ratings above 6.5 kV, cascading of converter cells becomes necessary when interfacing a 10 kV MV grid (cf. **Fig. 4.1**). In addition, cascading offers a multilevel output voltage waveform (cf. **Fig. 4.30a**), reducing filtering efforts, and provides modularity and redundancy. The converter considered here uses five cascaded cells (per MV phase) based on NPC bridge legs and 1700 V IGBTs

Tbl. 4.5: Main SST parameter and components overview.

MV filter indcutor, L_f	25 mH
Cell AC-DC stage devices	150 A/1700 V IGBTs
Cell AC-DC stage sw. freq.	1 kHz
Cell MV DC link voltage	2×1100 V
Cell MV DC link capacitors	2×750 µF, film
Cell DC/DC stage MV devices	150 A/1700 V IGBTs
Cell DC/DC stage sw. freq.	7 kHz
Cell DC/DC stage LV devices	200 A/1200 V IGBTs
Cell LV DC link voltage	800 V
Cell LV DC link capacitor	250 µF, film
LV inverter DC link capacitors	2×7 mF
LV inverter devices	1.2 kA/1200 V IGBTs
LV inverter sw. freq.	3.6 kHz
LV inverter boost inductor, L_b	345 µH

on their MV side, which have been found to offer a good trade-off between efficiency and power density for this voltage and power range (cf. **Chapter 2**). Note that one cell per phase stack serves only redundancy purposes and is not active during normal operation, i. e., it contributes to weight, volume and costs, but not to losses.

The power circuit of one converter cell is given in **Fig. 4.2a**, which shows also a photo of the corresponding fully rated 85 kW prototype, and **Tbl. 4.5** gives an overview on the main specifications. Each cell features a single-phase, five-level inverter/rectifier stage (three-level bridge legs), i. e., an ARU, and an isolated DC-DC converter, which is realized as a HC-DCM SRC (cf. **Chapter 3**). Its MFT is made of nanocrystalline core material and litz wire windings.

Based on the converter cell prototype, volume and weight of a single cell can directly be obtained. The costs of the main components are determined using cost models for high-volume production as presented in [146], however the cost model for the MFT has been adjusted by considering material costs only and adding a 50 % premium to account for the rather complicated, when compared to standard inductive components, isolation and cooling system.

The line filter inductors, L_f, are designed by means of thermally limited volume vs. loss Pareto optimization on the basis of laminated steel UI-cores

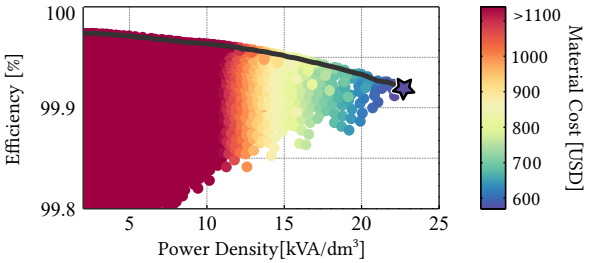


Fig. 4.31: Pareto optimization of the MV filter inductors with the chosen design highlighted.

and solid copper windings. The core dimensions are varied over a wide range to obtain a high number of designs, which can then be plotted in the efficiency/power density plane as done in **Fig. 4.31**, where the chosen design on the Pareto front is highlighted. Costs are again estimated using the material cost part of the inductor cost models given in [146].

Using datasheet characteristics for conduction and switching losses, the ARU efficiency has been calculated and together with the losses of the optimized filter inductors and an estimated DC-DC converter efficiency of 99 %, which is typically feasible with this kind of soft-switching DC-DC converters as discussed in **Chapter 3**, the overall MV-side (i. e., from three-phase MV AC to LV DC) converter efficiency is obtained as 98.2 %.

The volume of a converter cell is given by the prototype design and that of the filter inductor's bounding box follows from the optimization. The overall MV-side converter volume can therefore be obtained as the sum of fifteen times the cell volume and three times the inductor volume. In addition, a volume utilization factor of $u_\mathrm{V} = 0.75$ is assumed to account for empty spaces inevitably found in practical assemblies, i. e., the total volume is given as

$$V_\mathrm{total} = \frac{1}{u_\mathrm{V}} \sum_{\mathrm{i}=1}^{n} V_{\mathrm{component,i}}. \tag{4.33}$$

Of course, the SST's power electronics needs to be contained in cabinets. Therefore, **Fig. 4.32** shows the dependencies of cabinet weight and cost on the enclosed volume, i. e., V_total. Cabinet dimension and weight data is taken from a manufacturer's brochure [171], whereas price information is obtained from a large distributor. Thus, additional weight and cost contributions from the converter housing can be included in the corresponding estimates.

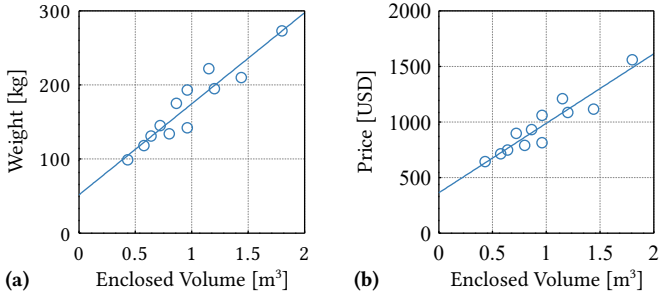


Fig. 4.32: Dependence of **(a)** cabinet weight and **(b)** price on the enclosed volume.

Tbl. 4.6: Performance characteristics overview (two 500 kVA units are considered for the LV side).

	SST MV	SST LV	SST	LFT
Efficiency [%]	98.3	98.0	96.3	98.7
Volume [m^3]	1.57	1.10	2.67	3.43
Weight [kg]	1270	1330	2600	2590
Material cost [kUSD]	34.1	18.6	52.7	11.4

The resulting performance characteristics for the SST's MV-side converter are summarized in **Tbl. 4.6**, while **Fig. 4.36a** and **Fig. 4.36d** present weight and cost breakdowns, respectively.

LV-Side Converter

As can be seen from the SST structure shown in **Fig. 4.1**, the LV-side three-phase inverter part is split into two parallel connected 500 kVA units for improving flexibility and providing high availability (continuation of operation at reduced power in case a unit should fail). **Fig. 4.33** shows the power circuit considered for the optimization of one of these 500 kVA units and **Tbl. 4.5** gives an overview on the main parameters resulting from the optimization described in the following.

The design of such standard three-phase systems is well documented in literature and analytic expressions for all semiconductor currents and, together with datasheet characteristics, device losses are available [172]. The DC link capacitor volume is modeled assuming a constant energy density of

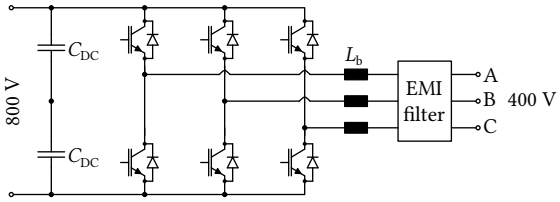


Fig. 4.33: Power circuit of the LV inverter stage.

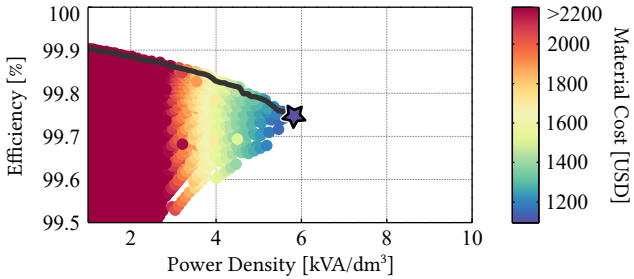


Fig. 4.34: Pareto optimization of the LV-side filter inductors with the chosen design highlighted. Due to the very high currents, the achievable power densities are significantly lower than in the MV case.

6.3 cm^3/J for film capacitors, which is based on datasheet averaging. Forced-air cooling is assumed and the corresponding heatsink volume is estimated using a CSPI [103] of 10 $W/K\,dm^3$ (0.164 $W/K\,in^3$), 50 °C ambient and 125 °C maximum junction temperature. The LV-side boost inductors, L_b, are optimized as described above for the MV-side filter inductors and the result is shown in **Fig. 4.34**. Thus, the overall weight and the overall volume—here employing a volume usage factor of $u_V = 0.25$ as a more conservative value for large, conventional power converters—of a given design can be estimated as well as costs can be modeled using [146] again.

To identify an optimum overall design, an efficiency vs. power density Pareto optimization is employed. For a given maximum peak-to-peak output current ripple specification of 10 %, the switching frequency is varied and the required boost inductance, L_b, adjusted accordingly [173]. The resulting designs can be plotted in the efficiency vs. power density plane as shown in **Fig. 4.35**, where the cost information is provided in the figure by the size of the circles. Three different optimization targets can be identified: maximum

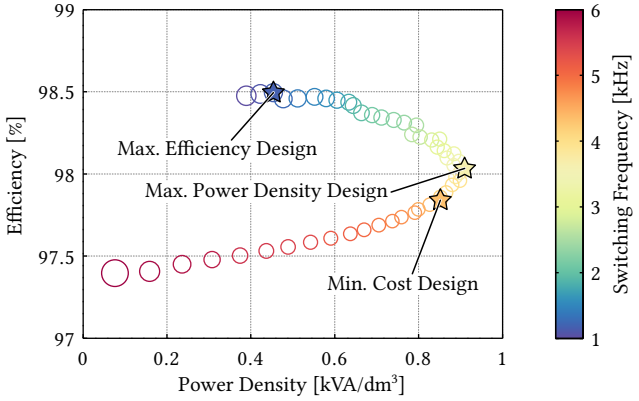


Fig. 4.35: Different design variants of a 500 kVA LV converter for 10 % peak-to-peak current ripple and different switching frequencies. The size of the circles indicates the designs' material costs.

efficiency, maximum power density and minimum cost; all of which are highlighted in the figure. The maximum power density design is considered for the comparison with the LFT, because it features still a comparatively high efficiency and its material costs are not significantly higher when compared with the minimum cost design. The related performance characteristics of the SST's LV-side converter can be found in **Tbl. 4.6**, and **Fig. 4.36b** and **Fig. 4.36e** show corresponding weight and loss breakdowns.

To support the results of this rather coarse modeling procedure, they are briefly compared with a 540 kVA active front end converter of a commercially available high-power drive system [174], i. e., a converter very similar to the one discussed here. First, this is a good opportunity to highlight again that the cost discussion here is limited to material cost estimates. The list price of the said active frontend converter is around 64 kUSD [175], which is almost seven times the material costs estimated here. Reasons for this difference are likely to be found in engineering and manufacturing costs, warehousing, amortizations, marketing and price policies, etc., which are hard to model. Regarding the other three performance characteristics, i. e., mass, efficiency, and volume, the calculated values for mass and volume of the 500 kVA LV unit are within ±10 % of the values reported for the said 540 kVA active front end converter, and the calculated losses are within ±15 %. These results indicate that despite neglecting many auxiliary components such as breakers, busbars,

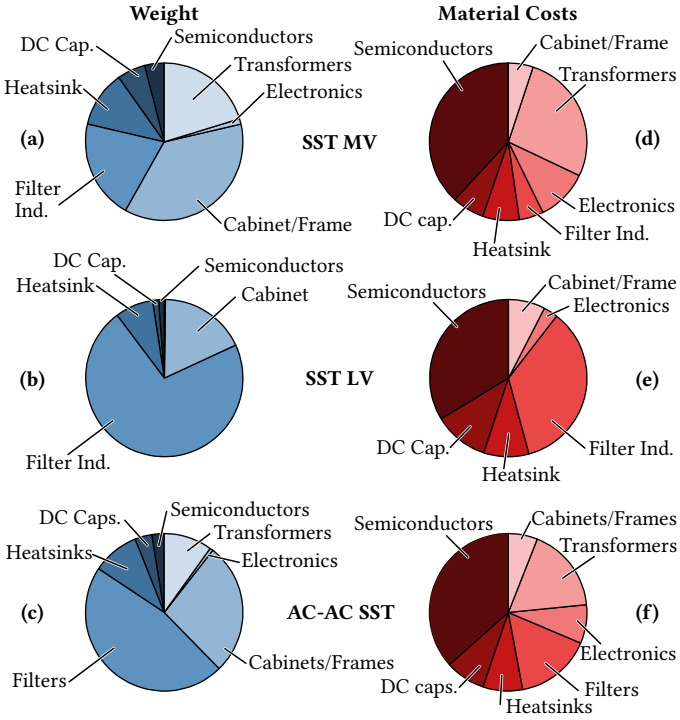


Fig. 4.36: Weight breakdowns of **(a)** the MV-side converter stage, **(b)** the LV-side converter stage, and **(c)** the complete AC-AC SST; material cost breakdowns of **(d)** the MV-side converter stage, **(e)** the LV-side converter stage, and **(f)** the complete AC-AC SST.

etc., still a fairly accurate estimate of these three performance characteristics can be obtained.

SST Weight and Cost Structure

Fig. 4.36 shows the weight and material cost structures of the MV-side converter stage, the LV-side converter stage, and, combining them, the overall 1000 kVA AC-AC SST. It is interesting to notice that still the LF magnetic components, i. e., the filter inductors, contribute a major share to weight and, especially in the case of the LV converter, where the phase currents are very high and consequently the required amount of copper conductor material is

high as well, also to material costs. Hence, these passive filter components are of particular interest for further cutting the cost and weight of SSTs. On the other hand, especially on the MV side, protection considerations might require a certain minimum value of the filter inductance [102], i. e., possibly eliminating the benefit of high switching frequencies and a high number of voltage levels.

However, on the LV side the required filter inductors could be reduced in volume by increasing the switching frequency, which is, however, not feasible with today's power semiconductors' high switching losses, as is illustrated in **Fig. 4.35**. At the price of higher complexity, another option to increase the effective switching frequency seen by the boost inductor would be to employ three-level topologies and/or interleaving of several units with smaller power ratings; and also more complex grid filter structures could allow for a higher current ripple in the boost inductors. Emerging technologies such as SiC power semiconductors can be expected to significantly contribute to further weight reduction through higher switching frequencies and consequently reduced sizes of passives. It is this context in which the higher costs of new technologies such as SiC power devices need to be considered on a system-oriented basis.

Other important contributions to material costs are the MFTs and the power semiconductors. The cascaded MV converter also requires quite complex control and communication electronics, therefore their share of the overall costs is clearly higher than in the LV converter.

4.3.4 Comparisons

With the four performance characteristics now determined for both, a typical 1000 kVA LFT and an equally rated, exemplary SST, the two concepts can be compared, first for the classical AC-AC use-case and second for two more modern AC-DC applications.

AC-AC Applications

Here, an AC-AC scenario is considered in which the SST directly replaces an LFT as interface between a three-phase MV AC and a three-phase LV AC grid. **Fig. 4.37a** compares the two cases, where material costs, mass, volume and losses are normalized to the LFT-based solution. In addition, **Tbl. 4.7** presents the comparison results in terms of four performance indices: losses per kVA, material costs per kVA, volume per kVA and weight per kVA. The SST solution

Tbl. 4.7: Characteristic performance indices for 1000 kVA LFT-based and SST-based solutions in AC-AC or AC-DC applications.

	AC-AC			AC-DC		
	LFT	factor	SST	LFT	factor	SST
Losses [W/kVA]	13.0	×2.87	37.3	32.7	×0.53	17.3
Costs [USD/kVA]	11.4	×4.61	52.7	30.0	×1.14	34.1
Volume [dm^3/kVA]	3.4	×0.78	2.7	4.5	×0.35	1.6
Weight [kg/kVA]	2.6	×1.00	2.6	3.9	×0.32	1.3

is about a factor of five more expensive, produces roughly three times higher losses, has similar weight but uses only 80 % of the LFT's volume.

AC-DC Applications

Nowadays, local LV DC systems are coming back in focus for in-building or in-factory power distribution, but also for entire DC microgrids, since many loads (e. g., drives, computers, lighting, etc.) and also generators (e. g., photovoltaics) are essentially devices featuring a DC port. Therefore, the second use-case for an SST is at the interface between a three-phase MV AC grid and an LV DC distribution system.

Mixed 50 % LV DC, 50 % LV AC First, a mixed environment where 50 % of the rated power needs to be provided as LV DC and the other 50 % as standard three-phase LV AC is looked at. The SST thus consists of the 1000 kVA MV converter part and one of the 500 kVA LV converters (cf. **Fig. 4.1**), whereas the LFT-based solution extends the LFT also by one of the 500 kVA units to act as a rectifier.

Fig. 4.37b compares the two approaches. With respect to the pure AC-AC case, the SST-based solution compares much more favorable in this mixed scenario. Note that the modularity of the SST system allows for a variety of different nominal LV AC and DC power ratings, since, e. g., instead of one 500 kVA unit also three 250 kVA units could be employed, etc.

100 % LV DC Finally, a pure AC-DC application is considered, where the SST-based solution is reduced to the MV converter part and on the other hand the LFT needs to be extended by two 500 kVA rectifier/inverter units.

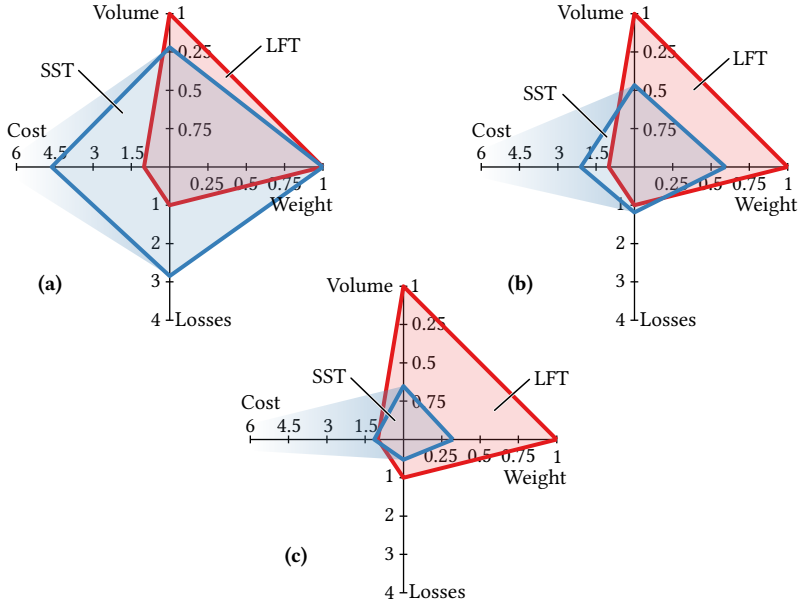


Fig. 4.37: Comparison of LFT and SST performance characteristics, normalized to the LFT-based solutions, **(a)** for AC-AC operation, **(b)** for 50 % AC-AC and 50 % AC-DC operation, and **(c)** for AC-DC operation. Note that the material cost estimates for the SST-based solutions constitute lower bounds only.

The resulting comparison between the SST-based and the LFT-based solution is given in **Fig. 4.37c** and the absolute data in terms of performance indices can again be found in **Tbl. 4.7**. Here, the SST-based solution outperformes the LFT-based solution in all areas except costs: it uses only one third of the LFT-based solution's volume, has only one third of the weight, and produces only about half the losses.

The latter is illustrated by **Fig. 4.38**, where the loss distributions for the three cases are shown. The SST's cascaded MV-side converter can transform from three-phase MV AC to LV DC at an efficiency already close to that of the LFT. Accordingly, once an LV DC output is required and thus the LFT's LV AC output needs to be rectified, the resulting LFT-based system's efficiency cannot compete anymore. However, note that the potentially higher costs of the SST-based solution could be invested in an improvement of the LFT-based solution, e. g., by upgrading the power semiconductors of the LV inverters,

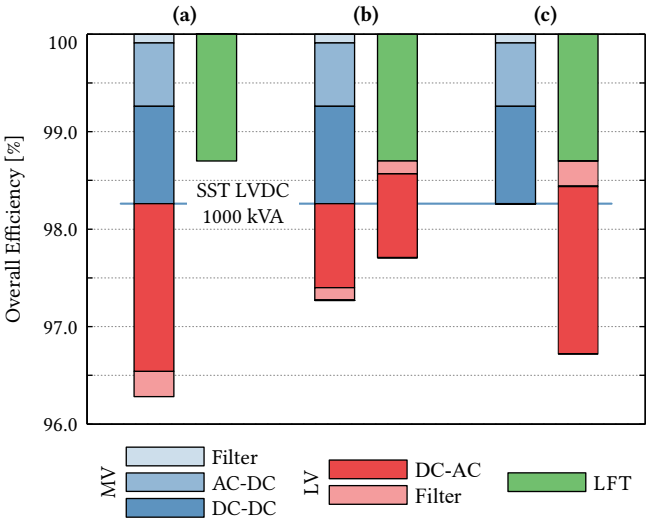


Fig. 4.38: Loss distribution of the three considered application cases, where **(a)** is for full AC-AC operation, **(b)** is for 50 % AC-DC and 50 % AC-AC operation, and **(c)** is for full AC-DC operation. Note that overall system losses at full-load operation, i. e., where AC and DC outputs are loaded with their respective rated power, are considered.

which could reduce the corresponding losses.

It should also be mentioned that in the AC-DC case the same limitations regarding overload capability apply for both solutions, whereas in the AC-AC application a power electronics system cannot compete with the short-term overload capacity of an LFT.

Resource Usage

Environmental concerns are one of the main driving forces behind power electronics and thus also SST research—consider for example the oil-free design of SSTs. Therefore, resource usage is an aspect that should be looked at next to efficiency, too. **Tbl. 4.8** gives an overview on the consumption of copper, iron core material, and silicon per kVA of rated power for the SST, its LV-side and MV-side converter stages, and the LFT. The values for the SST systems can be obtained from the modeling results described above; for the LFT an estimate based on the total weight and the oil mass of 1000 kVA units as given in [166] has been calculated by assuming a 3 mm thick steel

Tbl. 4.8: Specific resource usage.

	SST MV	SST LV	AC-AC SST	LFT (est.)
Copper [kg/kVA]	0.15	0.32	0.47	0.6
Iron [kg/kVA]	0.32	0.63	0.95	1.2
Silicon [mm^2/kVA]	85	22	107	0

enclosure and a typical (according to [169]) ratio of core to copper weight of 2:1.

As expected, the specific consumption of copper and iron in the SST can be reduced by about one fourth compared to the LFT. What is even more interesting is the comparison between the MV-side and the LV-side converter systems: The cascaded MV-side converter requires a high number of power semiconductors to generate a very high quality output voltage waveform, thus reducing the required filter size. While the MV converter's specific usage of copper and core material therefore is only about half the LV converter's (even though the MV stage contains also the DC-DC converters' transformers), this is paid by a fourfold increase in required silicon area, which reflects exactly the different topologies used.

Discussion

The presented analysis indicates that SST technology will have a hard time competing with well proven LF distribution transformer technology in classic AC-AC applications, i. e., replacing an LFT by an SST might not be feasible. Efficiencies of SSTs will remain for the coming years significantly lower than those of LFTs in the AC-AC case.

It should be noted that the LFT material costs are derived from price data of ready-to-buy units, whereas SST material costs are estimated for exemplary prototype designs and rely on component cost models for the main power components only and do not include, e. g., protection equipment, final assembly costs, profit margins or installation costs, although the latter can expected to be comparatively low due to the SST's modular nature. Nevertheless, even the so-obtained lower bound for SST material costs is already significantly higher than for the LFT counterparts. Therefore, and because of the lower efficiency, a standard TCO consideration will prefer an LFT due to its lower price and higher efficiency, which translates into lower energy loss costs. Furthermore, the initially mentioned general notion according to which SSTs

feature significantly lower weight and volume when compared to LFTs needs to be brought into question again when referring to direct replacements of LFTs by SSTs (cf. **Fig. 4.37a**).

On the other hand, in grid applications—in contrast to traction—weight and volume usually are not critical constraints. Furthermore, as power electronic system with an inherently high functionality, an AC-AC SST can replace more equipment than only an LFT, e. g., an LFT plus a voltage regulator or a STATCOM device. SSTs can act as power quality providers and even avoid the need of increasing feeder capabilities (which might seem necessary as a result of increasing penetration of photovoltaic infeed on lower voltage levels) due to their ability of controlling the voltage independent of power flow direction. Also, SSTs enable controlling power flows and thus could act as the "energy routers" of a future Smart Grid. Quantifying the economical impact of these additional features is virtually impossible on a generic basis, which is the reason for considering only material costs in this section, which, however, tries to raise the awareness for seeing SSTs not only as isolated, expensive components but as part of a larger system.

An example for how the specific application scenario can change the outcome of the comparison of SST and LFT solutions can be found in more modern applications such as AC-DC operation, where the SST basically acts as a heavy-duty MV power supply. There, the SST solution outperforms the LFT-based solution quite clearly regarding volume, weight and also efficiency, which likely justifies higher purchase prices in the long run alone due to loss energy costs being roughly halved.

4.3.5 Summary

This section provides a comparison of a 1000 kVA three-phase LFT and an equally rated SST with respect to material costs, weight, volume and losses. As a direct AC-AC replacement for an LFT, the SST solution realizes benefits with respect to volume, but on the other hand is significantly less efficient and has at least five times higher material costs. However, SST-based solutions can clearly outperform conventional LFTs plus LV rectifier systems in modern AC-DC applications, achieving about half the losses and one third of the weight and volume, respectively, although with still significantly higher material costs.

However, the usefulness of an SST can only be judged in the context of a given application; there is not a general SST solution that fits every need. Current state-of-the-art LFT technology evolved over more than a hundred

years, and represents therefore a truly experienced competitor. Thus SSTs, and explicitly also their relation to various application scenarios, regarding both, technical and economical aspects, should be prominently included in any power electronics or energy research agenda. Therefore, **Chapter 7** provides a more comprehensive discussion on the applicability of SST technology in different scenarios (not only in the distribution grid).

5
IFE-Based MVAC-LVDC Interface: The S³T

There are many emerging LV DC applications that could benefit from a power electronics interface to the MV AC distribution grid due to higher power requirements. Such applications include, e. g., datacenters with internal 400 V DC power distribution architectures, larger PV plants, fuel cell or battery storage systems, uninterruptible power supply (UPS) systems, or DC microgrids in general. However, in such stationary applications, the efficiency, robustness and costs of solutions based on conventional LFTs are difficult to attain with power electronic replacements, as has been discussed in Section 4.3. In contrast, especially in environments where volume and weight constraints apply, such as in, e. g., traction, subsea systems, or future aerospace applications, an increase of the isolation stage operating frequency from the grid frequency into the MF range by adding power electronic conversion stages is a competitive approach to meet these requirements (cf., e. g., [19]). Depending on the application, such SSTs acting as a link between an MV and an LV system operate either as a rectifier, as an inverter, or allow a bidirectional power flow. In either case, the power factor at the MV grid should be close to unity, i. e., isolated PFC functionality must be provided. Based on [54], different variants of how to partition this isolated PFC functionality are described in the following.

Isolated AC-DC Converter PFC Functionality Partitioning

An isolated (single-phase) PFC rectifier system performs four distinct tasks: Folding (rectification) of the AC grid voltage into a |AC| voltage, shaping of the input current (current shaping, CS), galvanic isolation (I), and output

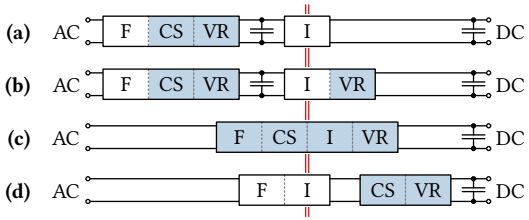


Fig. 5.1: Partitioning and sequencing of the tasks required to perform isolated AC-DC conversion and PFC: Folding (F), current shaping (CS), isolation (I), and output voltage regulation (VR). A shaded background indicates a controllable stage.

voltage regulation (VR). **Fig. 5.1** illustrates different variants of how these functional blocks can be partitioned and/or combined and sequenced.

Variant **(a)** interfaces the AC grid with a folding and a boost stage that draws an appropriately shaped current from the grid to generate a regulated DC voltage, which is then processed by an unregulated isolated DC-DC converter stage, which could be realized as HC-DCM SRC [19, 30, 135]. Since the isolation stage is positioned after the main controlling stage, this concept can be referred to as an *isolated back end* (IBE) system. Such an IBE SST has been analyzed in detail in the previous **Chapter 4**.

If, as in variant **(b)**, the isolation stage is realized as regulated converter, e. g., as DAB topology, complexity but also controllability increases, and it becomes possible to buffer the AC side power fluctuation on the primary side by controlling the power transfer through the isolation stage to a constant value, providing a regulated DC output voltage with very low LF ripple without requiring a large output capacitor [121, 176, 177].

The IBE concept can be realized as multi-cell ISOP system in order to cope with MV voltage levels on the AC side, as shown in **Fig. 5.2a**. Each converter cell consists of a controlled AC-DC rectification stage, a DC buffer capacitor, and an isolated DC-DC converter (cf., e. g., [19, 135, 177]). Hence, a large share of the system complexity (power semiconductors, measurement and control electronics, etc.) is located on the MV side of the isolation barrier.

In a third variant of the isolation, PFC, rectification, and voltage regulation task partitioning, **(c)**, all four functional blocks can be integrated into a single converter stage, which essentially directly switches the (possibly folded) mains voltage to generate a HF AC voltage that is then applied to a HF isolation transformer, as has initially been proposed in 1970 for an "electronic transformer" [37]. In such approaches, the shaping of the grid current as well

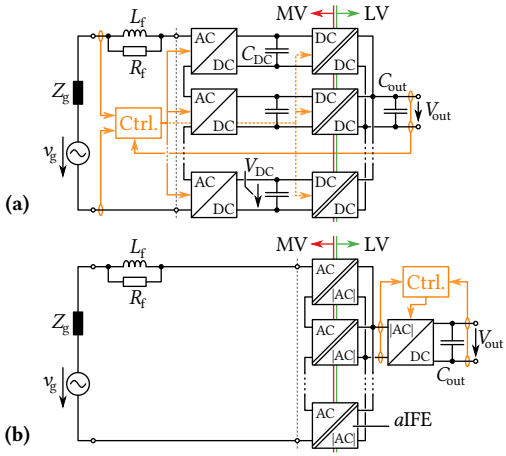


Fig. 5.2: (a) IBE and **(b)** IFE systems in ISOP configuration.

as the output voltage control functionality are integrated into the isolation stage (cf., e. g., [178–186]), which further increases its complexity and hence renders the approach less feasible for ISOP configurations.

The fourth variant, **(d)**, is an inversion of the concepts (a) and (b): a folding and isolation stage is directly connected to the mains, but the current shaping and voltage regulation process is performed by a controlled |AC|-DC conversion stage on the secondary side. Hence, this arrangement is referred to as an *isolated front end* (IFE) system. This has first been proposed in 1985 for a traction application, where the rectified and then chopped line voltage was used to directly feed a 400 Hz transformer and where the current shaping was realized using a (forced-commutated thyristor-based) boost stage connected in series to the secondary side rectifier of the isolation stage [55]. The concept was later extended to a cascaded input structure featuring a transformer with multiple primary windings [56], also for a traction application. The secondary-side ARU was used to control the current in the transformer stray inductance and hence in the grid. Recently, this idea has been applied to LV three-phase applications [57] and to a MV system [187], where both systems are employing three-phase multi-winding transformers. In contrast to these IFE converter realizations that use hard-switched isolation stages, an IGBT-based IFE system with soft-switching, resonant isolation stages in ISOP configuration, but with individual LC filter elements at each cell's AC side, has been proposed in 2013 [58, 59].

With the goal of minimizing the complexity and employing interleaved switching in a multi-cell ISOP configuration, the IFE structure discussed in this thesis does not employ such filter elements at each cell's AC side but only a common (damped) filter inductor, as shown in **Fig. 5.2b** [60]. A large share of the system's complexity, especially the control and measurement circuitry, has been moved to the LV side when compared to the ISOP IBE system. All the regulation tasks, i. e., CS and VR, are provided by a non-isolated boost-type |AC|-DC conversion stage on the LV side, whereas the cascaded isolation stage can act as an autonomous AC-|AC| isolated front end (*a*IFE), whose only task is to provide isolation by means of an MFT, i. e., to tightly couple its input and output voltages without requiring control nor providing regulation, which is conceptually similar to the original "electronic transformer" proposed by McMurray in 1971 [17], and in addition provides natural balancing of the converter cell's input voltages.

Chapter Outline

Section 5.1 derives the structure and the operating principle of the IFE system considered in this thesis, detailing also on the dynamic modeling and ISOP configurations, and briefly discusses additional topological variants of the IFE concept, i. e., three-phase and AC-AC configurations. Then, Section 5.2 provides a detailed analysis of the ZVS behavior of the S³T's isolation stage, discusses the optimum selection of the magnetizing inductance and the interlock time of the bridge legs in order to maximize the ZVS range over the grid period, and also proposes to vary the interlock time over the grid period in order to achieve both, a wide ZVS range and low additional losses. Finally, Section 5.3 describes a control strategy of the S³T that does not require MV-side measurements in the interest of low complexity.

Note that the next **Chapter 6** presents a comparative analysis of the IFE and the IBE concept, which is based on analytic expressions for the main component stresses, and includes a case study considering an all-SiC 25 kW, 6.6 kV AC to 400 V DC SST system—the S³T, which is currently being developed at the Power Electronic Systems Laboratory of ETH Zurich in the scope of a research program funded by the Swiss government [32].

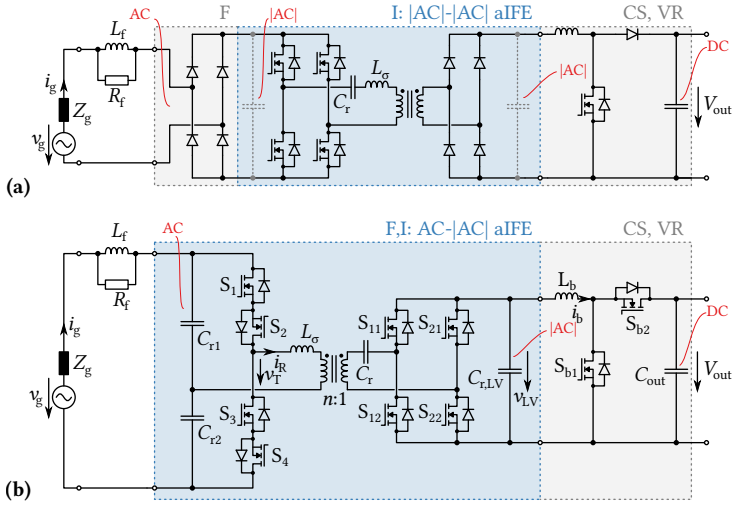


Fig. 5.3: (a) Unidirectional and **(b)** bidirectional single-cell IFE power circuit topologies. Note that C_{r1}, C_{r2}, C_r, and $C_{r,LV}$ are resonant capacitors, not (large capacitance) DC link capacitors.

5.1 Topology Derivation and Operating Principle

In this section, which is based on [54], the IFE topology considered later for the comparative evaluation in **Chapter 6** will be derived and explained on the basis of a single converter cell, considering also a dynamic model. In a second step, the extension to an ISOP configuration will be discussed.

5.1.1 IFE Topology and Key Waveforms

Fig. 5.3a shows an unidirectional single-cell variant of the considered IFE topology, where the folding of the (single-phase) grid voltage is realized by means of a diode rectifier. The circuit can be extended to facilitate bidirectional operation by either replacing the rectifier diodes on the grid side by switches (indirect matrix converter topology), or by integrating the folding/unfolding operation in the *a*IFE's primary-side half-bridge leg using bidirectional switches (direct matrix converter approach), as shown in **Fig. 5.3b**.

Note that in both cases all capacitors (except for the output capacitor,

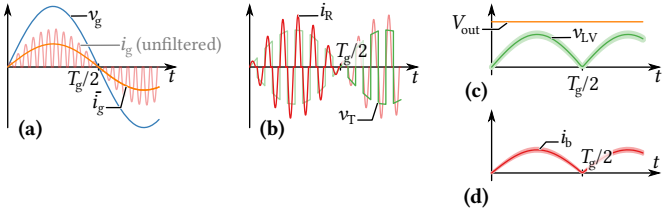


Fig. 5.4: Key waveforms (simplified) of the IFE topology shown in **Fig. 5.3b**, where a very low switching frequency is assumed for illustration purposes.

C_{out}) are only commutation or resonant capacitors, i. e., no energy storage elements. Since in the bidirectional topology the split resonant capacitors C_{r1} and C_{r2} consume capacitive reactive power from the grid (which could be compensated by suitable adaption of the boost stage current reference), high switching frequencies (and therefore high resonance frequencies and small capacitors) are desirable.

Referring to the bidirectional topology, **Fig. 5.4** shows key waveforms of the IFE system for unity power factor rectifier operation, i. e., power flow from the AC to the DC side: the bidirectional switches are modulated with (almost) full duty ratio to chop the grid voltage and to excite resonant current half-cycles in the *a*IFE transformer. On the secondary side, the transformer voltage is rectified (possibly using active synchronous rectification to reduce conduction losses) to recover a folded (and scaled by the turns ratio, $1/n$, and by a factor $1/2$ due to the primary side half-bridge realization) version of the grid voltage across the LV resonant capacitor $C_{r,LV}$—the *a*IFE thus acts as an isolated AC-|AC| converter.

The boost stage, in contrast, operates as a |AC|-DC converter and controls the current in the boost inductor, L_b, to be proportional to the |AC| voltage across $C_{r,LV}$. Because the *a*IFE does not contain any significant energy storage elements (no DC link buffering capacitors), the instantaneous power flow drawn from the grid is equal to the power flow dictated by the boost stage on the LV side—the *a*IFE simply translates the input characteristics of the controlled boost stage to the grid without requiring feedback control by itself. In terms of currents, this means that the local average value of the current pulses in the transformer corresponds to the boost inductor current, and that the same is true for the local average of the grid current (modified by the turns ratio, etc.). Note that the operating mode of the boost stage is identical to that of a non-isolated single-phase PFC rectifier circuit, where it would

Tbl. 5.1: Main specifications of the multi-cell IFE SST considered for the simulations.

Rated power (one phase), P_N	25 kW
Grid voltage (line-to-line RMS), V_N	6.6 kV
Number of cells, n_{cell}	5
Output DC voltage, V_{out}	400 V
Nominal *a*IFE stage switching frequency, f_s	50 kHz
Nominal resonant frequency, f_0	52 kHz
Transformer turns ratio, n	1.8
Stray inductance, L_σ	10 µH
MV resonant cap., $C_{r1} = C_{r2}$	$\approx$ 0.7 µF (f_0 tuning)
LV resonant cap., $C_{r,LV}$	3.5 µF

be directly connected to an input diode rectifier. This illustrates how the IFE approach extends standard load-side converters to interface MV levels without requiring a bulky and heavy LFT.

5.1.2 Dynamic Behavior and Modeling

The transfer behavior, i. e., the dynamics of the *a*IFE stage with respect to terminal voltages and currents can be modeled by a passive equivalent circuit (cf. **Fig. 5.5a**), which illustrates the (local) "DC transformer" and/or actual "|AC| transformer" behavior of the HC-DCM SRC [134,135]. The current flowing in the equivalent circuit, $\bar{i}_R$, corresponds to the local (switching frequency) average of the real transformer current (cf. **Fig. 5.5b**). Assuming the current pulses to be of piecewise sinusoidal shape, the equivalent circuit elements can be calculated as

$$R_{dc} = \frac{\pi^2}{8}\frac{f_0}{f_s}R_{total} \quad \text{and} \quad L_{dc} = \frac{\pi^2}{4}\frac{f_0^2}{f_s^2}L_\sigma, \tag{5.1}$$

where R_{total} is the sum of all series resistances in the current path (i. e., on-state resistances of the switches, winding resistances of the transformer, etc.), and where f_s and f_0 denote the switching and the resonant frequency, respectively. All quantities are referred to the MV side of the *a*IFE cell. Please refer to Section 3.2 for a more detailed derivation and explanation of this dynamic model.

Using the equivalent circuit, the transfer function from the (controlled) boost inductor current to the (local) grid current, $G_i(s) = I_g(s)/I'_{LV}(s)$, can be

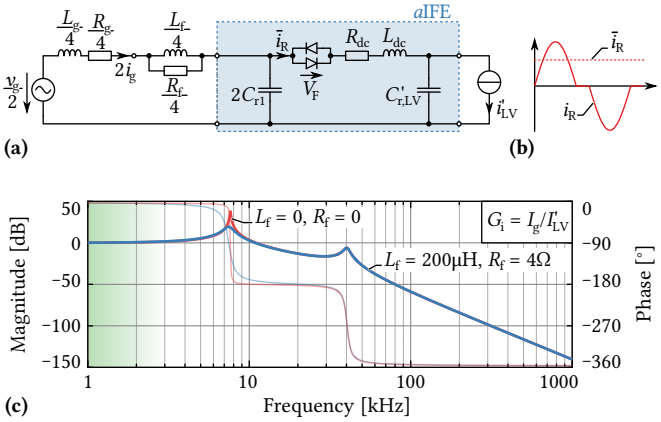


Fig. 5.5: (a, b) Dynamic equivalent circuit (referred to the MV side of the MFT) of the *a*IFE converter including input filter and grid impedances, and **(c)** corresponding transfer function from the boost stage inductor current to the grid current, $G_i(s)$, using the specifications from **Tbl. 5.1** scaled to one instead of five cells. The resulting model parameters are $L_{dc} = 26.7\,\mu H$ and $R_{dc} = 510\,m\Omega$; furthermore, $C_{r1} = 0.68\,\mu F$, $C_{r,LV} = 3.5\,\mu F$, $L_g = 690\,\mu H$ and $R_g = 22\,m\Omega$ have been used for the calculation of the exemplary transfer function.

calculated (cf. **Fig. 5.5c**). The gain of $G_i(s)$ being unity at low frequencies, e. g., at the grid frequency, illustrates that the *a*IFE is a "transparent" isolation stage, in essence similar to an LFT, although featuring significant volume and weight benefits, allowing to interface a standard boost converter to the MV grid. Note that the resonance with the highest amplitude in $G_i(s)$ occurs between the input capacitors and the filter (and inner grid) inductance. Since this resonance may be excited by load steps, appropriate damping, e. g., by using a damped RL input filter, is required. Alternatively, more advanced input filter damping strategies, such as parallel LR damping, could be employed [188].

The *a*IFE stage dynamics are not infinitely fast, which limits the IFE system's capability to source or sink reactive power. As there is no intermediate energy storage on the MV side, the power flow direction through the *a*IFE then would need to change twice per grid period. In case of reactive power operation and/or a phase displacement of voltage and current, the *rectified* grid current would need to undergo step changes—which can be easily performed by the boost converter and its control (cf. also Section 5.3). However, such very fast current changes are limited in bandwidth by the *a*IFE dynamics

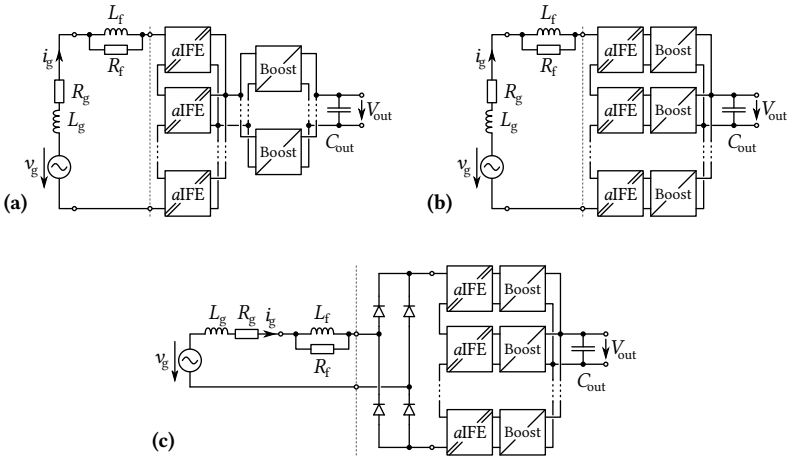


Fig. 5.6: Three ISOP configuration variants of the IFE topology; **(a)** common |AC| LV-side bus and single boost stage employing interleaved sub-units, **(b)** one boost stage per *a*IFE cell, and **(c)** common input rectifier using HV semiconductors (possibly realized as a synchronous rectifier by adding anti-parallel switches to the diodes).

according to $G_i(s)$, causing disturbances in the grid current. However, this constitutes only a minor limitation of the concept, as in many applications only operation at a power factor close to unity is required.

5.1.3 ISOP System Configuration

For interfacing an MV grid, ISOP configurations of several *a*IFE cells can be considered in order to allow a realization with LV semiconductors. **Fig. 5.6** shows three possible ISOP configuration variants of the considered IFE topology.

Since the cells are connected directly in series on the MV side, and because the grid current consists of the superposition of the *rectified* transformer current pulses of the individual cells, interleaving of the SRC carrier signals by $\Delta\varphi_{aIFE} = 180°/n_{cell}$, with n_{cell} denoting the number of cascaded *a*IFE cells, can be employed to cancel switching frequency harmonics and/or to increase the effective switching frequency. However, due to interactions between the resonant circuits via their respective initial conditions on the MV and on the LV side (cf. [131]), the expected cancellation of harmonics is not fully achieved as can be seen from the simulation results shown in **Fig. 5.7** for a system

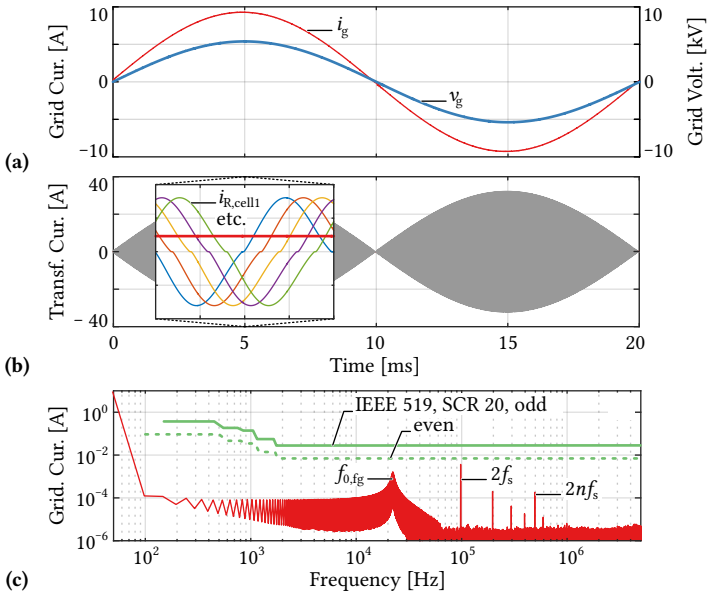


Fig. 5.7: Simulation results of a single-phase ISOP system according to **Fig. 5.6a** (the boost converter is modeled as a current source) and with specifications given in **Tbl. 5.1**. Furthermore, $L_g = 690\,\mu H$, $R_g = 22\,m\Omega$, $L_f = 200\,\mu H$, and $R_f = 10\,\Omega$ are used.

according to **Fig. 5.6a** and with specifications given in **Tbl. 5.1**. Whereas the boost converter is modeled as a current source for the results shown in **Fig. 5.7**, note that also the harmonics of the boost converter stages would be attenuated by the transfer characteristic of the *a*IFE if the (equivalent) boost stage switching frequency is chosen high enough.

As discussed earlier, the HC-DCM SRC has the property of tightly coupling its two terminal voltages. Since in an ISOP structure the voltages on the secondary side are equal for all cells—either because a direct coupling between the LV outputs of the *a*IFE stages exists (cf. **Fig. 5.6a**), or because the boost stages are controlled such that they provide the same input resistance to their *a*IFE cells (cf. **Fig. 5.6b**)—equal voltage sharing among the cells is ensured on the MV side. A more generic, very detailed analysis of natural balancing mechanisms in ISOP systems can be found in [43]. This self-balancing feature is illustrated by simulation results of a system according to **Fig. 5.6a**, where, however, the boost stage is modeled as a controlled current source, and with

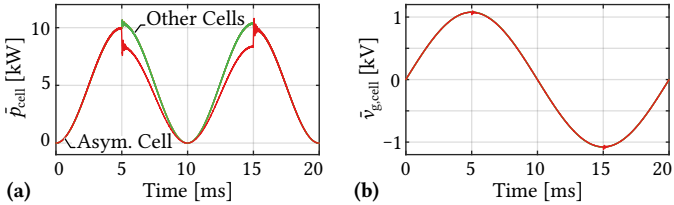


Fig. 5.8: Simulated self-balancing of the cells in ISOP configuration according to **Fig. 5.6a** and with specifications from **Tbl. 5.1**, where the boost converter is modeled as a current source. At $t = 5\,\text{ms}$, a disturbance is introduced by connecting a load resistor (10 % nominal cell power) at the MV terminals of one cell. At $t = 15\,\text{ms}$, the disturbance is removed again. **(a)** Power distribution between the cells, and **(b)** sharing of the input voltage. Note that the waveforms show local average values.

Tbl. 5.2: Effect of cell asymmetries where in case **(a)** a resistor (10 % of nominal cell power) is added in parallel to one cell's MV terminals, and where in case **(b)** one MV-side resonant capacitor of once cell is selected to be 20 % smaller than the nominal value. The data is given relative to the respective nominal values of the balanced state.

	(a)			(b)		
	$\frac{P_{\text{cell}}}{P_{\text{cell,N}}}$	$\frac{\tilde{i}_{\text{R}}}{\tilde{i}_{\text{R,N}}}$	$\frac{\hat{v}_{\text{in}}}{\hat{v}_{\text{in,N}}}$	$\frac{P_{\text{cell}}}{P_{\text{cell,N}}}$	$\frac{\tilde{i}_{\text{R}}}{\tilde{i}_{\text{R,N}}}$	$\frac{\hat{v}_{\text{in}}}{\hat{v}_{\text{in,N}}}$
Cell with asym.	0.84	0.84	0.99	1.00	1.03	1.01
Other cells	1.04	1.04	1.01	1.00	1.00	1.00

specifications given in **Tbl. 5.1**. First, a resistor consuming 10 % of a cell's nominal power (1 kW) is connected in parallel to the MV input terminals of a single cell at $t = 5\,\text{ms}$ and removed after half a mains period. **Fig. 5.8** and the data given in **Tbl. 5.2a** illustrate that the voltage sharing is almost unaffected by the disturbance, and that the minor imbalance in the power flows processed by the individual cells self-balances back to a symmetric distribution as soon as the disturbance is removed at $t = 15\,\text{ms}$. Balancing is also ensured for deviations of the nominal capacitance values of the primary side resonant capacitors, i. e., C_{r1} and C_{r2}, as can be seen from the results in **Tbl. 5.2b**. There, one such input capacitor of one cell is selected 20 % smaller than the nominal value, resulting only in negligible asymmetries of the voltage and/or power handling among the converer cells. Note that this voltage balancing is achieved without active control of the *a*IFE stages. In addition, **Fig. 5.9** illustrates the system's stability during transients.

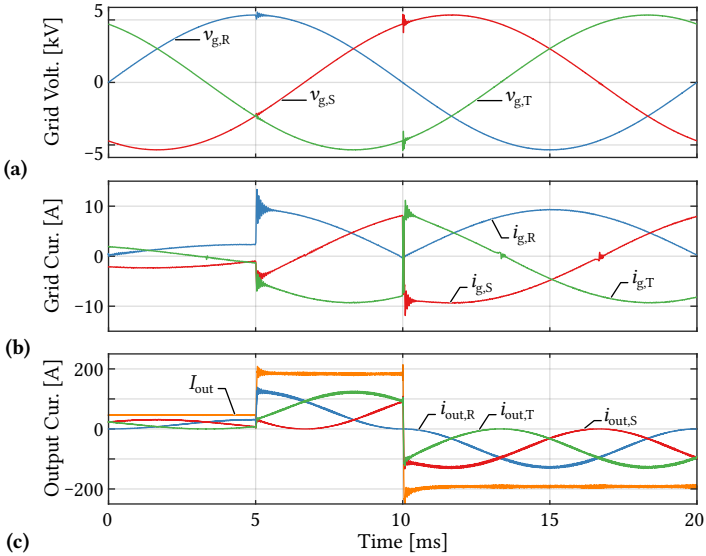


Fig. 5.9: Simulation of a three-phase IFE AC-DC SST system, where three phase stacks according to **Fig. 5.6b** are connected in star configuration. The currents $i_{\text{out,R}}$, $i_{\text{out,T}}$ and $i_{\text{out,S}}$ are the DC-side output currents of the three phase stacks; due to the three-phase configuration, the fluctuating power of the three phase stacks adds up to a constant DC-output power and hence constant overall output current, I_{out}. The specifications are given in **Tbl. 5.1**, i. e., the three-phase power is 75 kW. Furthermore, $L_{\text{g}} = 690\,\mu\text{H}$, $R_{\text{g}} = 22\,\text{m}\Omega$, $L_{\text{f}} = 200\,\mu\text{H}$, and $R_{\text{f}} = 4\,\Omega$ are used. At $t = 5\,\text{ms}$, the load current reference changes from 25 % to 100 %, and at $t = 10\,\text{ms}$, the power flow direction is fully reversed at rated load.

5.1.4 Three-Phase Configurations

By connecting three single-phase IFE systems (cf. **Fig. 5.6**) either in star or in delta configuration, a three-phase IFE SST can be realized. Such configurations allow to reduce the output buffer capacitance requirement, since ideally the power contributions of the three phases add up to a constant value at the common LV output. In contrast to an IBE system, also no energy buffering is required on the MV side of the cascaded cells. **Fig. 5.9** shows simulation results of a three-phase IFE SST in star configuration, considering the specifications from **Tbl. 5.1** for each phase, which results in a three-phase power rating of $3 \cdot 25\,\text{kW} = 75\,\text{kW}$. One boost stage per cell (cf. **Fig. 5.6b**) is employed, switching at 75 kHz (with interleaving between the boost stages of a phase

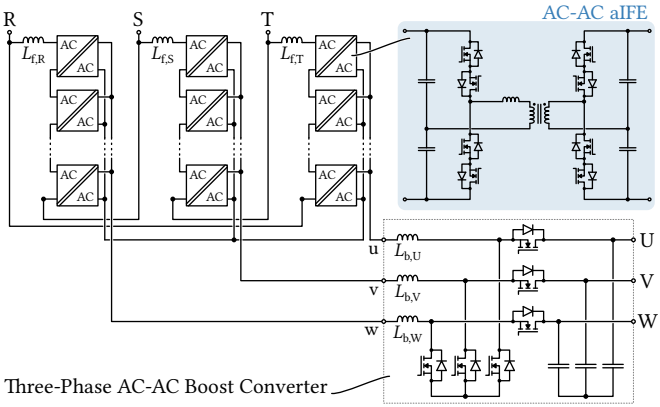


Fig. 5.10: Three-phase IFE SST for AC-AC applications.

stack) and implementing average current control, which is used to perform step changes of the output current (the DC output voltage is impressed by a voltage source) and also a transition from rectifier to inverter operating mode.

5.1.5 AC-AC Operation

In one of the first publications mentioning an "electronic transformer" [17], the HC-DCM SRC has also been used in an AC-AC configuration. **Fig. 5.10** shows a three-phase ISOP arrangement using such AC-AC *a*IFE cells, which is similar to a recent patent by GE [49]. If output voltage control is required, a three-phase AC-AC boost converter can be connected on the LV side (cf. [189] for a review of non-isolated AC-AC converters). Of course, also a single-phase configuration could be realized.

5.1.6 Scott Transformer Configuration

A Scott transformer configuration as shown in **Fig. 5.11a** allows to transform a symmetrical three-phase voltage system into a two-phase system with 90° phase shift between the voltages [190]. This two-phase system can be interfaced using only two appropriately controlled non-isolated single-phase PFC rectifier stages to generate two DC output voltages while ensuring balanced three-phase currents on the input side [191]. In order to reduce weight and volume, the magnetic Scott transformer windings could be replaced by IFE

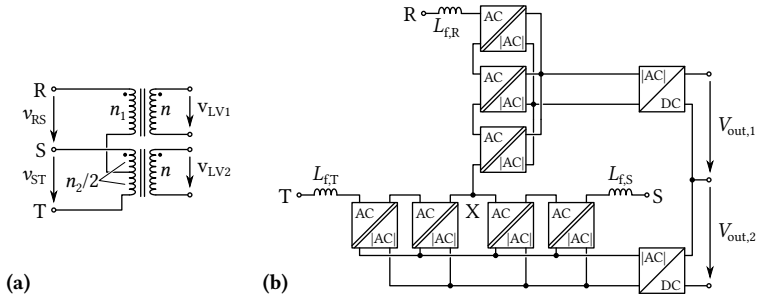


Fig. 5.11: (a) Magnetic Scott transformer, **(b)** IFE-based Scott transformer configuration.

stacks as shown in **Fig. 5.11b**, where the number of cells, the MFT turns ratios and the control of the two |AC|-DC stages must be such that the voltage sharing as well as Ampère's Law of the magnetic Scott transformer are emulated. Please refer to [60] for a more detailed description of the concept.

5.2 ZVS Considerations for IFE SSTs

As has been discussed in the previous section, the IFE approach connects SRC isolation stages operating in the HC-DCM directly to the MV AC grid in an ISOP configuration, but the entire control, i. e., the shaping of the grid current for unity power factor and the output voltage regulation, is carried out by a second, non-isolated conversion stage on the LV side. However, since the isolation stages do not operate with a DC but with an AC or |AC| input voltage, the transformer magnetizing current available for ZVS as well as the voltage to be switched are varying over the grid period. Following [192], and taking into account also component tolerances among the cascaded converter cells, this section provides an in-depth analysis of the ZVS behavior under these conditions, and of the associated losses and EMI considerations, presenting a loss-optimal choice of the magnetizing inductance value and of the dead time (interlock time) of the isolation stages' bridge legs. A time-dependent variation of the latter to achieve ZVS over the entire grid period without an increase of the isolation stage losses is proposed. The considerations are verified at the example of the S³T, an all-SiC 25 kW, 6.6 kV MV AC to 400 V LV DC converter system, using a detailed simulation model, including nonlinear MOSFET capacitances.

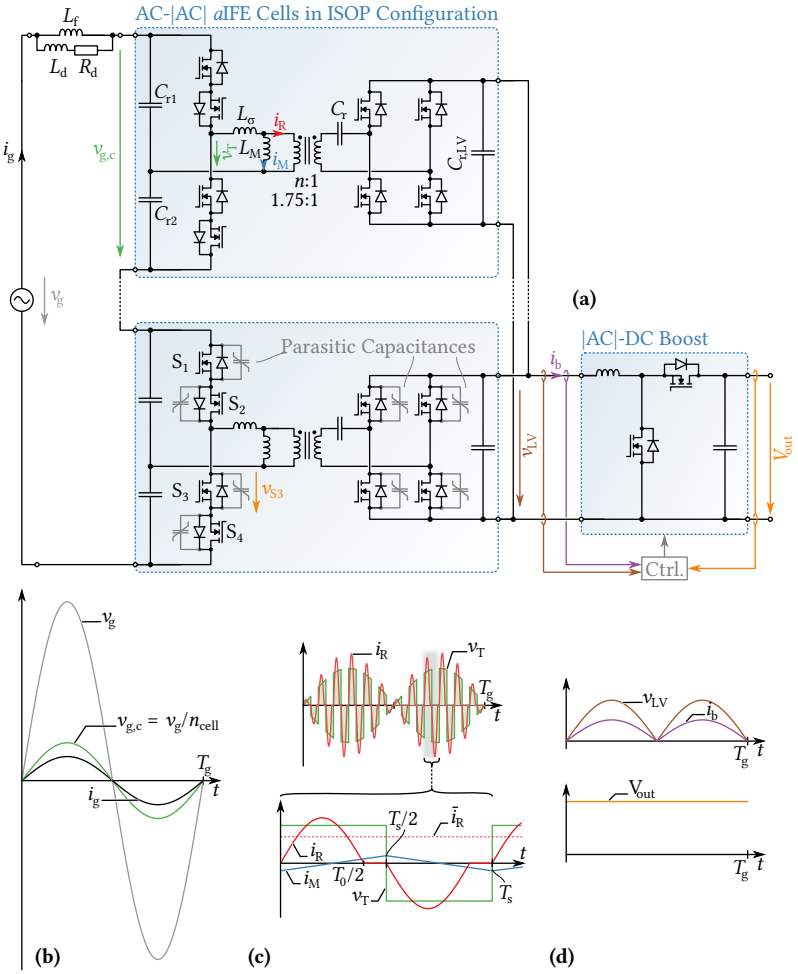


Fig. 5.12: Topology and key waveforms of the Swiss SST (S³T), an all-SiC IFE-based SST capable of providing bidirectional power flow with unity power factor at reduced system complexity. Note that no measurements are required on the MV side, and that C_{r1} and C_{r2}, i. e., the capacitors on floating potential, are only small resonant capacitors. Only two cascaded cells of the full system comprising five cells in an ISOP arrangement are shown. **Tbl. 5.3** gives the S³T's main specifications.

Tbl. 5.3: Main specifications of the S³T.

Rated power, P_N	25 kW
Grid voltage (line-to-line RMS), V_N	6.6 kV
Number of cells, n_{cell}	5
Output DC voltage, V_{out}	400 V
Nominal resonant frequency, f_0	≈ 52 kHz

The Swiss SST (S³T)

In the scope of a research program funded by the Swiss government [32], an all-SiC realization of a 25 kW IFE SST as an interface between a 6.6 kV MV AC grid and a 400 V DC load or source is investigated—the Swiss SST, i. e., S³T [54, 60]. **Fig. 5.12** shows again the considered topology, corresponding key waveforms, and **Tbl. 5.3** gives the main specifications.

The S³T features an ISOP configuration of converter cells, i. e., *a*IFEstages. Each *a*IFE stage is realized as an SRC operated in HC-DCM, which has the property of tightly coupling its terminal voltages in open-loop operation (cf. [17, 38, 135] and **Chapter 3** for details). On their MV side, the *a*IFE cells feature a half-bridge with bidirectional switches to enable an AC input voltage, i. e., direct connection to the grid, by combining the folding of the grid voltage and the switching for the SRC operation, while the second, capacitive leg consists of two (small) resonant capacitors, C_{r1} and C_{r2}. Hence, the envelope of the transformer voltage, v_T, is proportional to the grid voltage, and a scaled and rectified version of the grid voltage, v_{LV}, is obtained after rectification on the secondary side, i. e., the *a*IFE stage is essentially acting as isolated AC-|AC| converter.

As already described in Section 5.1.1, the input current, i_b, of a non-isolated |AC|-DC boost converter connected to the common LV |AC| bus of the *a*IFE cells can be controlled such as to be in phase with v_{LV} and of appropriate magnitude to maintain the output DC voltage at a given value.

Since the *a*IFE stage does not contain significant energy storage elements, the power flow impressed by the |AC|-DC boost converter is directly translated to the grid, ensuring unity power factor operation. Thus, the local average value of the resonant current pulses, $\bar{i}_R$, is proportional to the instantaneous boost inductor current, i_b (and hence also to the grid current, i_g), which can be assumed to be constant over a switching period.

Zero-Voltage Switching in the S³T

There are two reasons to aim for ZVS transitions in a converter: first, switching losses can be reduced to a minimum, and second, EMI noise generated by fast (partially) hard-switched transitions can be avoided. The HC-DCM operating mode of the SRC facilitates to achieve ZVS independent of the load level, since the magnetizing current of the transformer is used to discharge and charge the switches' parasitic output capacitances during the dead time, t_d, at changes of the bridge legs' switching states (cf. **Fig. 5.12c**).

In conventional IBE systems, the isolation stage is operating as DC-DC converter between two constant DC voltages. Accordingly, the envelope of the transformer voltage is constant, and thus a combination of a magnetizing inductance, L_M, (and hence a peak magnetizing current, $\hat{i}_\mathrm{M}$) and a dead time, t_d, can be chosen such as to result in suitable ZVS performance, which has been, e. g., discussed for an IGBT-based design in [193]. In a practical realization, L_M can be adjusted by the transformer design (air gap), or an external shunt inductor may be used. This is then sufficient to ensure ZVS over the entire grid period.

However, this is quite different in case of an IFE system, where the envelope of the switched voltage applied to the transformer is proportional to the grid voltage (cf. **Fig. 5.12**). Thus, the amount of magnetizing current available for ZVS varies over the grid period—but so does the voltage to be switched. Considering the nonlinearity of the parasitic capacitances of power semiconductors (C_oss in the case of MOSFETs), which strongly increase at lower voltages, it needs to be investigated whether it is at all possible to achieve ZVS over the entire grid period, and how to choose the magnetizing inductance and the dead time accordingly. An initial analysis considering IGBTs has been presented in [58, 59], where for given magnetizing inductance and dead time a range of the grid period in which ZVS can be achieved has been identified. However, a more detailed analysis and optimization, considering not only the magnetizing inductance, but also advanced techniques such as variable dead times has not been mentioned.

Therefore, this section provides a detailed analysis of the ZVS behavior of the S³T's isolation stage, considering an optimum choice of L_M and t_d but also proposing a time-dependent variation of the dead time over the grid period. First, a basic configuration consisting of only the MV-side bridge leg and the magnetizing inductance is used to illustrate the basic principles in Section 5.2.1, before then a full analysis and optimization based on detailed simulations of the switching transitions, including non-linear capacitance characteristics as well as the impact of tolerances of the individual converter

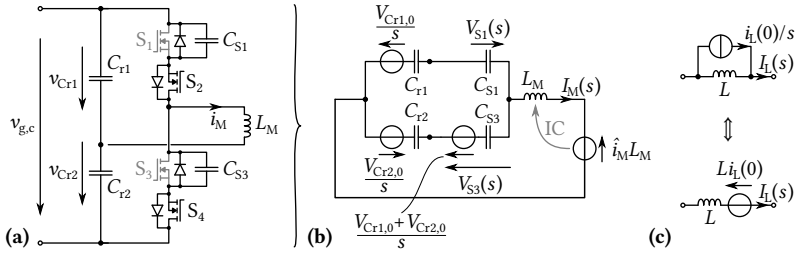


Fig. 5.13: (a) MV-side bridge leg during commutation from S_1 to S_3 and **(b)** corresponding Laplace equivalent circuit, where the voltage source $\hat{i}_M L_M$ represents the initial condition of the magnetizing inductor current. Note that this circuit is valid for a simplified analysis only, because the parasitic capacitances of the LV-side switches are not yet considered. **(c)** Two equivalent variants for representing the initial condition of an inductor in the Laplace domain.

cells' resonant tank components, is presented in Section 5.2.2.

It should be noted that similar considerations regarding DAB converters [66] in AC-DC applications [194], i. e., with varying input voltages, have been carried out, e. g., in [195], however, relying not only on the magnetizing current but utilizing the more complex control possibilities of a DAB. Note also that literature describes various concepts of how to operate a boost converter such as used in the S³T with full ZVS by using, e. g., triangular current mode [196] or clamp switches [197, 198]. Hence, a detailed description of the boost stage ZVS operation is not in the scope of this section.

5.2.1 Basic ZVS Considerations

First, a simplified circuit consisting of only the MV-side bridge leg and the magnetizing inductance, i. e., the circuit shown in **Fig. 5.13a**, is considered, and, without loss of generality, a switching transition from S_1 to S_3 (i. e., for $v_{g,c} > 0\,\mathrm{V}$ where S_2 and S_4 are gated on permanently). The available magnetizing current and also the switched voltage vary with the input voltage of the converter cell, $v_{g,c} = v_g / n_{cell}$, as can be seen in **Fig. 5.14a**. In combination with a given (constant) dead time, t_d, this results in different switching transitions over the grid period as shown in **Fig. 5.14b-e**: In case **(b)**, the dead time is too short, i. e., $v_{S3}(t_d)$ is still larger than zero and an incomplete ZVS transition with the remaining voltage step

$$\Delta V = v_{S3}(t_d) \tag{5.2}$$

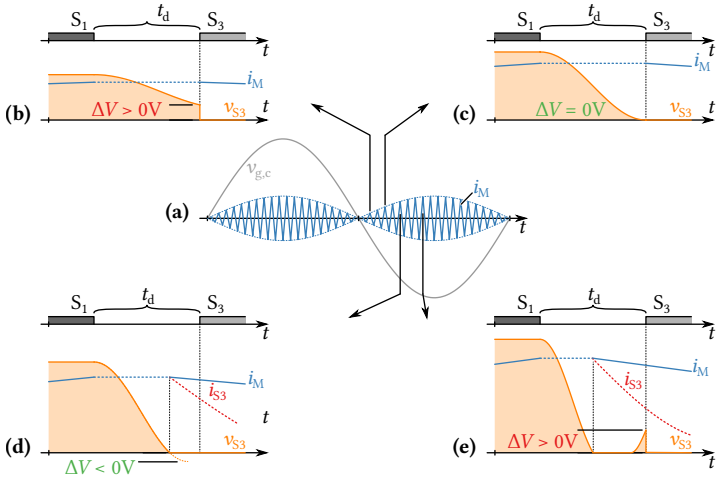


Fig. 5.14: (a) Available magnetizing current over a grid period, and **(b-e)** exemplary switching transitions with ZVS ($\Delta V \leq 0\,\mathrm{V}$) or partial ZVS ($\Delta V > 0\,\mathrm{V}$).

occurs, generating additional switching losses. Case **(c)** is the borderline case, where the ZVS transition fully completes within the dead time ($\Delta V = 0\,\mathrm{V}$), and in case **(d)**, the voltage across S_3 would swing below zero (theoretically $\Delta V < 0\,\mathrm{V}$) if it was not clamped by the anti-parallel diode of S_3. Typically, such a design with $\Delta V < 0\,\mathrm{V}$ over the entire grid period would be aimed for if ZVS operation should be guaranteed.

Finally, the ZVS transition shown in case **(e)** is so fast that the load current of the next resonant pulse, which begins to flow as soon as the anti-parallel diode of S_3 starts to conduct and therefore the MV bridge is applying a fixed voltage to the resonant tank again, reaches the magnetizing current and hence the current through S_3/D_3 changes its sign before S_3 is gated on. Consequently, the parasitic capacitance C_{S3} is charged again until finally S_3 turns on with $\Delta V > 0\,\mathrm{V}$, i. e., only a partial ZVS transition occurs.

Note that which type of transition occurs during what parts of the grid period in general depends on the chosen L_M and t_d, but also on component tolerances, etc., which will be discussed in more detail in Section 5.2.2.

Increasing the dead time and/or reducing the magnetizing inductance (and hence increasing the peak magnetizing current) would speed up the switching transitions, reducing the length of the time interval within the grid period where case (b) appears; but on the other hand, the region where case (e)

Tbl. 5.4: Additional specifications of the S³T (cf. also **Fig. 5.12**).

Nom. res. freq., f_0	52 kHz	Nom. sw. freq., $f_{s,N}$	50 kHz
MV res. cap., $C_{r1,2}$	2.5 µF	Stray inductance, L_σ	10 µH
Res. cap., C_r	5 µF	LV res. cap., $C_{r,LV}$	3.5 µF
Transf. efficiency, η_T	99.6 %	Core to Cu loss at P_N	1 : 1

appears could be increased (note, however, that case (e) does not necessarily appear). Also, a larger dead time corresponds to a reduction of the switching frequency, which in turn increases the RMS value of the resonant current and hence load-dependent conduction losses. A larger magnetizing current causes a load-independent increase of the conduction losses. Thus, the choice of the magnetizing inductance and the dead time has to be carried out carefully in order to meet the criteria of low losses (also in part load operation) and complete ZVS in a wide region of the grid period.

Loss Modeling

As mentioned above, the losses of the isolation stage, i. e., the *a*IFE stage, depend on the chosen L_M, t_d, etc. Note that even though for now only a reduced circuit (cf. **Fig. 5.13a**) is considered, the losses are calculated for a full *a*IFE stage, i. e., including the LV-side semiconductors. The specifications of the S³T are given in **Tbl. 5.3** and in **Tbl. 5.4**. Wolfspeed's upcoming 1700 V/45 mΩ and 900 V/11.5 mΩ SiC MOSFETs are considered [199] (no paralleling, 125 °C junction temperature). Transformer losses are estimated by assuming a full-load transformer efficiency of 99.6 % with a 1:1 distribution of winding and core losses, which yields a corresponding winding resistance that allows a load-dependent modeling of the winding losses.

Conduction Losses (Resonant Current) The grid current, i_g, consists of a component that is in phase with the grid voltage and corresponds to the processed power, but also of a reactive component because of the MV-side capacitors C_{r1} and C_{r2}, i. e.,

$$i_g(t) = \hat{i}_{g,A} \sin\left(2\pi f_g t\right) + \hat{i}_{g,R} \sin\left(2\pi f_g t + \frac{\pi}{2}\right), \tag{5.3}$$

where $\hat{i}_{g,A}$ follows from the processed power and

$$\hat{i}_{g,R} = \hat{v}_g \cdot \left(2\pi f_g \frac{C_{r1,2}}{2n_{cell}}\right). \tag{5.4}$$

As a consequence of the half-bridge configuration employed on the MV side, the local average value of the resonant current pulse, $\bar{i}_{\mathrm{R}}$, must equal twice the local average value of the active component of the grid current, $i_{\mathrm{g,A}}$. Assuming piecewise sinusoidal current pulses, the local RMS value of the resonant current pulses becomes (please refer to **Chapter 6** for detailed derivations)

$$\tilde{i}_{\mathrm{R}} = i_{\mathrm{g,A}} \cdot \frac{\pi}{\sqrt{2}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}}, \tag{5.5}$$

where f_{s} denotes the *effective* switching frequency, i. e,

$$f_{\mathrm{s}} = \frac{1}{T_{\mathrm{s,N}} + 2 \cdot t_{\mathrm{d}}} \quad \text{with} \quad T_{\mathrm{s,N}} = \frac{1}{f_{\mathrm{s,N}}}. \tag{5.6}$$

Loss-wise, a choice of $T_{\mathrm{s,N}} = T_0$, i. e., operation at the border of the DCM mode, would constitute an optimum. However, typically $T_{\mathrm{s,N}}$ has to be chosen sufficiently longer in order to ensure DCM mode even in the case of component value tolerances of the resonant tank elements, which are causing deviations among the different cells' resonant periods ($T_{0,\mathrm{i}}$) in a multi-cell system. For the same reason, the case $T_{\mathrm{s,N}} < T_0$ is not considered here, because then the ZVS behavior would become strongly dependent on the load current, worsening the issues discussed in Section 5.2.2. Note also that a very long t_{d} increases the RMS current and hence conduction and winding losses.

The LV-side switches can be operated with $T_{\mathrm{s,LV}} = k \cdot T_{\mathrm{s,N}}$ with $k < 1$ in order to reduce conduction losses by means of synchronous rectification. To ensure DCM operation, $T_{\mathrm{s,LV}}$ must be sufficiently shorter than $T_{\mathrm{s,N}}$ in order to prevent the resonant current from crossing zero. Note that a negligibly short LV diode conduction interval is assumed for the conduction loss calculations, i. e., only the MOSFETs' on-state resistances are considered.

Conduction Losses (Magnetizing Current) Considering an arbitrary switching period (cf. **Fig. 5.12b** and **Fig. 5.12c**), $v_{\mathrm{g,c}}$ denotes the instantaneous value of the cell's AC input voltage, which is assumed to be constant during the switching period. This voltage is applied to the magnetizing inductance during the active interval,

$$T_{\mathrm{on}} = \frac{T_{\mathrm{s,N}}}{2}, \tag{5.7}$$

increasing the magnetizing current to

$$\hat{i}_{\mathrm{M}} = \frac{1}{2} \cdot \frac{1}{2} \frac{v_{\mathrm{g,c}}}{L_{\mathrm{M}}} \cdot T_{\mathrm{on}} \tag{5.8}$$

at the switching instant. Then, the local RMS value of the magnetizing current becomes

$$\tilde{i}_{\mathrm{M}} = \hat{i}_{\mathrm{M}} \cdot \sqrt{f_{\mathrm{s}} \cdot \left(\frac{T_{\mathrm{s,N}}}{3} + 2 \cdot t_{\mathrm{d}} \right)}, \tag{5.9}$$

generating load-independent conduction losses in the MV-side MOSFETs as well as in the MV transformer winding.

Switching Losses The losses of an incomplete ZVS transition can be estimated based on the MOSFET's output capacitance, C_{oss}, and the remaining voltage, $\Delta V > 0\,\mathrm{V}$, according to the procedure described in [200]. Switching losses for $\Delta V \leq 0\,\mathrm{V}$, i. e., for complete ZVS transitions, are neglected.

Analytical Modeling of Simplified ZVS Transitions

Considering the simplified circuit consisting only of the MV-side bridge leg and the magnetizing inductance as shown in **Fig. 5.13a**, the behavior after the turn-off instant of S_1, i. e., during the dead time, can be modeled in the Laplace domain (cf. **Fig. 5.13b**), where the voltage across S_3, $V_{\mathrm{S3},0} = V_{\mathrm{Cr1},0} + V_{\mathrm{Cr2},0} = v_{\mathrm{g,c}}$, and the current in L_{M}, $I_{\mathrm{M},0} = \hat{i}_{\mathrm{M}}$ as given in (5.8), appear as initial conditions.

During the switching half period prior to the considered turn-off of S_1, only the grid current flows through C_{r2}, whereas the superposition of the grid current and the transformer current flows through C_{r1}. Thus, the two initial conditions $V_{\mathrm{Cr1},0}$ and $V_{\mathrm{Cr2},0}$ are unequal, and can be calculated using

$$V_{\mathrm{Cr1},0} \approx \frac{v_{\mathrm{g,c}}}{2} - \frac{i_{\mathrm{g}} \cdot T_{\mathrm{on}}}{2 \cdot C_{\mathrm{r1}}} \quad \text{and} \quad V_{\mathrm{Cr2},0} \approx \frac{v_{\mathrm{g,c}}}{2} + \frac{i_{\mathrm{g}} \cdot T_{\mathrm{on}}}{2 \cdot C_{\mathrm{r2}}}, \tag{5.10}$$

whereby the short dead time interval is neglected.

The nonlinear output capacitances, $C_{\mathrm{oss}}(v_{\mathrm{ds}})$, of the SiC MOSFETs depend on the applied voltage. Fitting a power function to the datasheet curves allows to express the charge-equivalent capacitance, $C_{\mathrm{Q,eq}}$, as a function of the total voltage, $v_{\mathrm{ds}} = v_{\mathrm{g,c}}$, applied to the device,

$$C_{\mathrm{oss,fit}}(v_{\mathrm{ds}}) = a v_{\mathrm{ds}}^{b} \tag{5.11}$$

$$C_{\mathrm{Q,eq}}(v_{\mathrm{ds}}) = \frac{1}{v_{\mathrm{ds}}} \cdot \int_0^{v_{\mathrm{ds}}} C_{\mathrm{oss,fit}}(v)\, dv = \frac{a v_{\mathrm{ds}}^{b+1}}{(b+1) \cdot v_{\mathrm{ds}}}. \tag{5.12}$$

With that it is possible to describe the voltage across S_3 during the dead time analytically as

$$v_{S3}(t) = \sqrt{\hat{i}_M^2 Z_0^2 + V_{Cr1,0}^2}\cos(\omega_0 t + \varphi) + V_{Cr2,0}, \tag{5.13}$$

where

$$\varphi = \arctan\frac{Z_0 \hat{i}_M}{V_{Cr1,0}}, \quad Z_0 = \sqrt{\frac{L_M}{2C_{Q,eq}}}, \quad \omega_0 = \frac{1}{\sqrt{2L_M C_{Q,eq}}}.$$

Hence, the remaining voltage across S_3 at the end of the dead time interval, i. e., at its turn-on instant, is given by

$$\Delta V = v_{S3}(t_d). \tag{5.14}$$

ZVS Optimization with Constant Dead Time

In the following, the above models are employed to find optimum combinations of a magnetizing inductance, L_M, and a corresponding dead time, t_d. **Fig. 5.15** gives an overview on the implemented optimization routine. L_M and t_d are both swept over specific ranges, resulting in a number of tuples $\{L_M, t_d\}$. For each of these tuples, five different operating points, i. e., power flow levels, are considered (20 %, 40 %, 60 %, 80 % and 100 % of the nominal power, i. e., $p = \{0.2, 0.4, 0.6, 0.8, 1\}$).

For each power level, i. e., for each tuple $\{L_M, t_d, p\}_i$, the analytic models described above are evaluated at 50 equally spaced points during one quarter of a grid period, resulting in 50 values for ΔV and for the relative total *a*IFE stage losses. The 50 loss values are then averaged and the maximum among the 50 values for ΔV is identified. This is then repeated for the other power levels, resulting in five values for ΔV_{max} and five values for $p_{loss,avg}$.

Finally, the worst-case ΔV_{wc} for the given tuple $\{L_M, t_d\}_i$ is identified by finding the maximum among the ΔV_{max} values obtained for the five power levels. An aggregated representation of the losses is calculated by averaging the $p_{loss,avg}$ values obtained for the five power levels. It would be possible to account for a load profile by introducing weighting factors in this averaging process, which is, however, not done here. Thus, the optimization routine assigns a tuple $\{\Delta V_{wc}, p_{loss}\}_i$ to each tuple $\{L_M, t_d\}_i$. ΔV_{wc} is the maximum switched voltage during a grid period for any considered power level, and p_{loss} denotes the relative losses averaged over all considered power levels.

Fig. 5.16a and **Fig. 5.16b** show the resulting $\{\Delta V_{wc}, p_{loss}\}$ in dependence of $\{L_M, t_d\}$. In both figures, the trajectories corresponding to either lowest

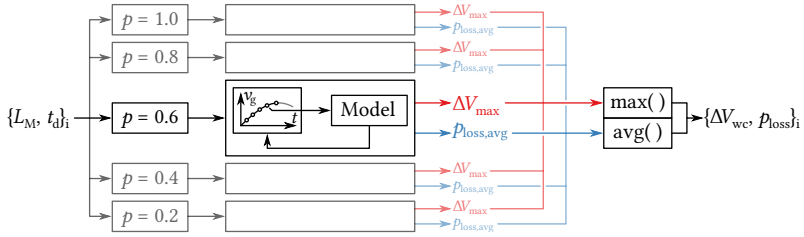


Fig. 5.15: Schematic representation of the ZVS optimization procedure with constant dead time. The optimization routine assigns to each tuple $\{L_\mathrm{M}, t_\mathrm{d}\}_\mathrm{i}$ a tuple $\{\Delta V_\mathrm{wc}, p_\mathrm{loss}\}_\mathrm{i}$, i. e., a worst-case ΔV_wc and averaged relative losses, p_loss. Please refer to the text for a more detailed description.

Tbl. 5.5: Resulting designs of ZVS optimization with analytic models. A: minimum p_loss; B: $\Delta V_\mathrm{wc} \leq 0\,\mathrm{V}$ and min. losses; C: minimum p_loss and $\Delta V_\mathrm{wc} \leq 0\,\mathrm{V}$ for variable dead time, t_d.

	A	B	C
L_M	0.97 mH	0.66 mH	1.02 mH
t_d	250 ns	540 ns	variable

averaged losses, p_loss, (blue) or lowest worst-case ΔV_wc (red) are indicated. Since the two trajectories do not coincide, it is not possible to obtain minimum p_loss *and* minimum ΔV_wc for a given L_M if the same constant t_d is used.

Following these trajectories, **Fig. 5.16c** shows the corresponding dependence of p_loss and ΔV_wc on the magnetizing inductance. As expected, low values of L_M correspond to lower ΔV_wc, because more magnetizing current is available, but also to higher losses due to the higher RMS current. Considering the red trajectory (lowest worst-case ΔV_wc), full-range ZVS can be achieved with $L_\mathrm{M} \leq 1.25\,\mathrm{mH}$. Considering the blue trajectory (minimum losses), full-range ZVS could only be achieved with very small magnetizing inductances, which still would cause high losses.

Two specific designs are now analyzed in more detail; the corresponding parameters are given in **Tbl. 5.5**. Design A is the design with minimum p_loss, however, with $\Delta V_\mathrm{wc} \approx 80\,\mathrm{V}$, i. e., it only achieves ZVS within a limited part of the grid period, as can be seen from the plot of ΔV over half a grid period in **Fig. 5.17a**. Note that this is no issue regarding losses, since the switching losses resulting from the incomplete ZVS transitions with a maximum

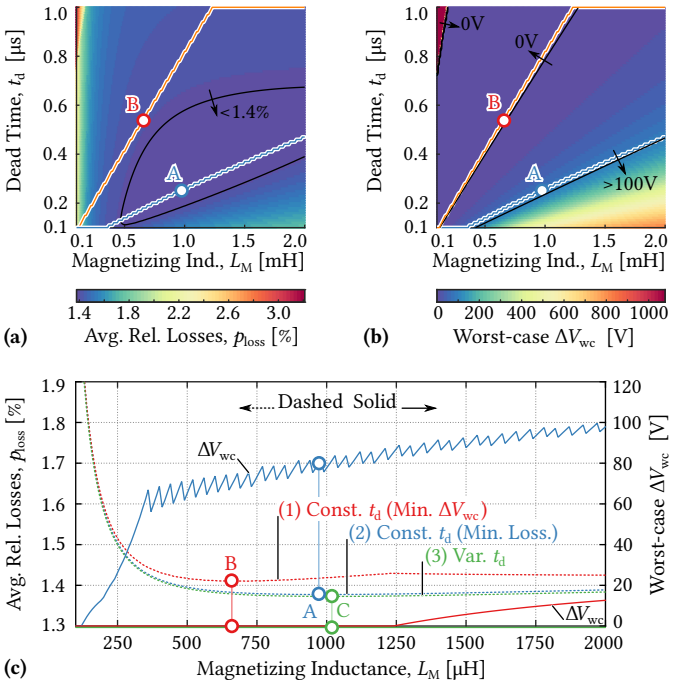


Fig. 5.16: Results for the analytic ZVS considerations using the model from **Fig. 5.13** and the routine shown in **Fig. 5.15**. **(a)** averaged relative losses, p_{loss}, and **(b)** worst-case switched voltage, ΔV_{wc}, in dependence of $\{L_M, t_d\}$. Following the highlighted trajectories in (a) and (b), **(c)** shows the corresponding dependencies of p_{loss} (dahsed lines) and ΔV_{wc} (solid lines) on the magnetizing inductance (note that the respective values of t_d are according to the trajectories given in (a) and (b)). The blue trajectory (trace 1) corresponds to minimum p_{loss}, the red trajectory (trace 2) corresponds to minimum ΔV_{wc}, and trace 3 is for a variable dead time. If ZVS should be obtained over the entire grid period with a constant dead time, the minimum possible losses (design B) are higher than the minimum possible losses without full-range ZVS (design A). If the dead time is variable, low losses *and* full-range ZVS can be obtained (design C). Note that the ragged appearance of the ΔV_{wc} trace is due to the limited resolution of the L_M and t_d search ranges.

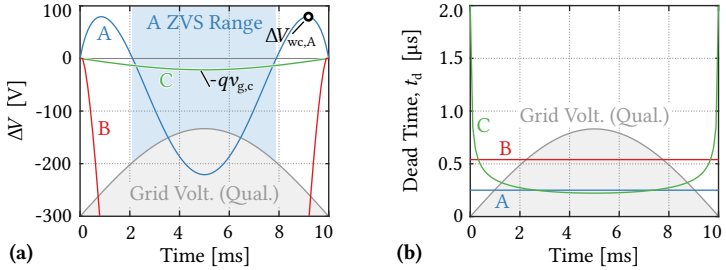


Fig. 5.17: (a) Switched voltage, ΔV, over half a grid period for the three example designs from **Fig. 5.16c** and **Tbl. 5.5**. For design A, also the worst-case switched voltage, ΔV_{wc} is indicated. **(b)** shows the corresponding dead times, t_{d}, over half a grid period.

residual voltage of only around 100 V are negligible for the considered SiC FETs (< 0.5 W). Nevertheless, the partial hard-switching during certain parts of the grid period might be a concern regarding potential EMI signature degradations.

In contrast, design B is the minimum-loss design that in addition (and in contrast to design A) also realizes full-range ZVS (cf. **Fig. 5.17a**), i. e., $\Delta V_{\mathrm{wc}} \leq 0\,\mathrm{V}$, by utilizing a lower magnetizing inductance (corresponding to a higher magnetizing current) and a longer dead time (cf. **Tbl. 5.5**). However, as expected, this results in higher losses compared to design A (cf. **Fig. 5.16c**).

ZVS Optimization with Variable Dead Time

Apparently, it is not possible to obtain $\Delta V \leq 0\,\mathrm{V}$ over the entire grid period without an increase of the total losses if a constant dead time is used. This situation can be improved by introducing a time-varying dead-time. From (5.13), the dead time to provide guaranteed ZVS with a certain margin specified by q (i. e., $\Delta V^* \stackrel{!}{=} -q v_{\mathrm{g,c}}$) can be calculated according to

$$t_{\mathrm{d}}^* = \frac{1}{\omega_0} \cdot \left[\pi - \arctan\left(\frac{Z_0 \hat{i}_{\mathrm{M}}}{V_{\mathrm{Cr1,0}}} \right) - \arccos\left(\frac{V_{\mathrm{Cr2,0}} + q v_{\mathrm{g,c}}}{\sqrt{\hat{i}_{\mathrm{M}}^2 Z_0^2 + V_{\mathrm{Cr1,0}}^2}} \right) \right]. \tag{5.15}$$

Optimizing again by sweeping L_{M} (but calculating the required variable dead times for each case with (5.15)) yields trace 3 in **Fig. 5.16c**. As can be seen, full-range ZVS, i. e., $\Delta V_{\mathrm{wc}} \leq 0\,\mathrm{V}$, can be achieved for all values of L_{M}.

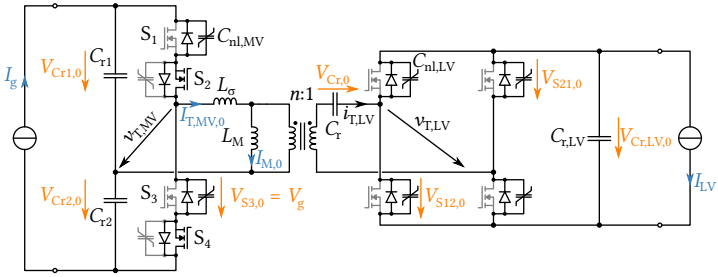


Fig. 5.18: Full *a*IFE circuit, including non-linear MOSFET capacitances, which is used to simulate the ZVS transitions for given initial conditions. These initial conditions are also highlighted in the figure.

Specifically, design C with parameters given in **Tbl. 5.5** achieves minimum losses. **Fig. 5.17b** shows the corresponding variable t_d^* over half a grid period. Note that design C features almost the same L_M as design A, and that the variable dead time of design C is similar to the constant dead time of design A over wide ranges of the grid period, which explains the similar (low) losses. However, in contrast to design A, design C provides complete ZVS over the entire grid period, as can be seen in **Fig. 5.17a**.

5.2.2 Advanced ZVS Analysis and Optimization

The above basic considerations exemplify the trade-offs regarding the ZVS-behavior of the *a*IFE stage. However, the situation is more complicated in reality, as can be seen from **Fig. 5.18**, which shows the full circuit of an *a*IFE stage with the initial conditions for a transition from S_1 to S_3 indicated—it is not sufficient to consider only the MV-side bridge and the magnetizing current for the following reasons:

LV Side Parasitic Capacitances First, the LV-side bridge must be included, since its switches also feature parasitic capacitances, which affect the MV-side switching transitions, because they provide an additional current path for the magnetizing current during the dead time.

Stray Inductance Second, the stray inductance, L_σ, must be considered, too, because it forms a resonant circuit with the parasitic capacitances of both bridges, giving rise to a current oscillation that is superimposed on the

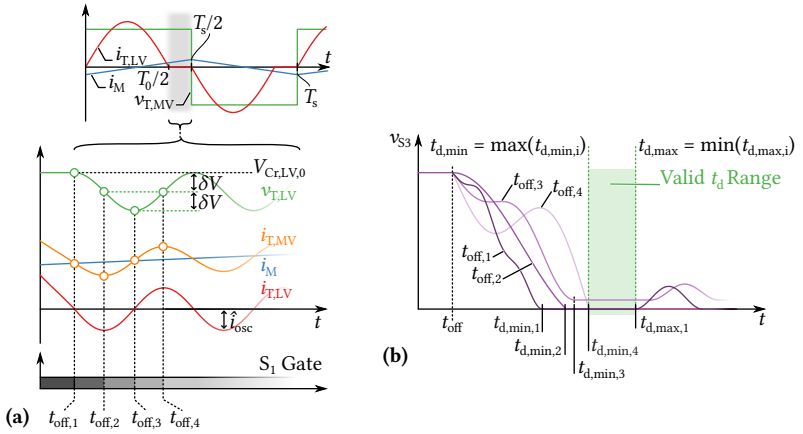


Fig. 5.19: (a) Parasitic HF oscillation during the current zero interval. The actual turn-off instant of S_1 may occur at any time relative to this HF oscillation; four representative cases are indicated as $t_{off,\{1,2,3,4\}}$, whereby $t_{off,1}$ constitutes the nominal case (the switching occurs at the same instant as the resonant current, $i_{T,LV}$ becomes zero). **(b)** Exemplary switching transitions for different initial conditions (e. g., switching at $t_{off,1}$, $t_{off,2}$, $t_{off,3}$ or $t_{off,4}$). The shapes and durations of the transitions vary, some may not swing to zero completely, and some may start to swing back to positive voltage values at some point. Thus, a dead time $t_{d,min} \leq t_d \leq t_{d,max}$ must be chosen if ZVS shall be obtained.

magnetizing current and hence also affects the MV-side switching transitions. Note that the superimposed oscillation can especially also cause an early rise of the voltage across S_3 (cf. **Fig. 5.14e** or curve for $t_{off,1}$ in **Fig. 5.19b**).

Diodes It is important to highlight that, third, also the diodes of both bridges play an important role: As soon as the voltage across a certain diode/capacitance combination becomes higher than the junction voltage, the diode is forward biased and hence the behavior of the circuit changes. If it is a diode on the MV side, this initiates the start of the next resonant current pulse, which might cause a rise of the voltage across S_3 if the switch is not turned on in time (cf. **Fig. 5.14e**). If it is a diode on the LV side, the impedance of the current path on the LV side becomes lower, which means that less current is available to complete the switching transition on the MV side, possibly preventing a $\Delta V \leq 0\,\mathrm{V}$ even for a very long dead time (cf. the curve for $t_{off,3}$ in **Fig. 5.19b**).

Component Tolerances As discussed above, typically $T_{s,N} > T_0$ is chosen, resulting in an interval where the LV transformer current in theory is zero while the MV bridge is still actively applying a voltage (cf. zoomed view in **Fig. 5.12c**). In reality, however, the stray inductance and the LV parasitic capacitances are forming an only very lightly damped resonant circuit once the LV-side diodes stop conducting, causing the current in L_σ and also the voltages across the LV parasitic capacitances, e. g., v_{S12}, to oscillate, which is illustrated in **Fig. 5.19a**.

Therefore, the initial conditions of the actual switching transition depend on where relative to this HF oscillation the actual switching, i. e., the turn-off of S_1, occurs; the four extreme cases are indicated in the figure. In addition to the specific values of the involved components and hence the frequency of the parasitic oscillation, this is also influenced by the ratio $T_{s,N}/T_0$, which depends on the specific values of the resonant tank components, e. g., L_σ. In a single cell system it would be possible to tune $T_{s,N}$ such as to switch always under nominal conditions, i. e., at the instant when the resonant current, $i_{T,LV}$, reaches zero and hence the current in the stray inductance equals the peak magnetizing current ($i_{T,MV} = \hat{i}_M$) and v_{S12} equals the LV-side voltage, v_{LV}. This situation corresponds to switching at $t_{off,1}$ in **Fig. 5.19a**. However, such a tuning of $T_{s,N}$ is not possible in multi-cell systems, because $T_{0,i}$ may vary among the cells.

Therefore, in order to calculate the worst-case ΔV_{wc}, and/or the required t_d, all four extreme initial conditions indicated in **Fig. 5.19a** must be considered for a single switching transition, each resulting in a specific variant of this switching transition—for example those corresponding to the four curves shown in **Fig. 5.19b**. Note that now, in order to obtain ZVS for all cells, the dead time has to be chosen in a window between a minimum and a maximum value, and note further that there might be situations where $\Delta V \leq 0\,\mathrm{V}$ cannot be achieved under all conditions, e. g. for all cells, even with long dead times.

Detailed ZVS Modeling

The effects described above are very hard or even impossible (diodes) to capture with an analytical, Laplace-based model. Therefore, a simulation-based approach using GeckoCIRCUITS, which is capable of handling non-linear capacitances [201], and which can be scripted from MATLAB, is employed in the following to simulate ZVS transitions using the circuit shown in **Fig. 5.18**.

Initial Conditions In addition to the initial conditions discussed already in Section 5.2.1 ($I_{M,0}$, $V_{Cr1,0}$ and $V_{Cr2,0}$) the simulation circuit from **Fig. 5.18**

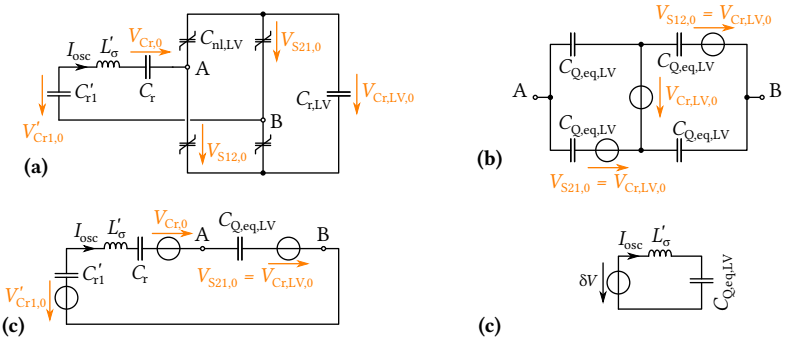


Fig. 5.20: Derivation of the equivalent circuit for the simplified calculation of HF oscillations during the zero-current interval (cf. **Fig. 5.19**). All quantities are referred to the LV side of the transformer. **(a)** Relevant part of the full circuit shown in **Fig. 5.18**; **(b)** simplification of the LV-side bridge, where $C_{\mathrm{nl,LV}}$ is replaced by the charge equivalent capacitance, $C_{\mathrm{Q,eq,LV}}$, and where $C_{\mathrm{r,LV}}$ is neglected because $C_{\mathrm{r,LV}} \gg C_{\mathrm{Q,eq,LV}}$; **(c)** intermediate simplification step where the circuit part from (b) has been replaced by it's Thévenin equivalent; and **(d)** final equivalent circuit where all initial conditions are summarized as a voltage source, δV, and where $C'_{\mathrm{r1}} \gg C_{\mathrm{Q,eq,LV}}$ and $C_{\mathrm{r}} \gg C_{\mathrm{Q,eq,LV}}$ are neglected.

requires additional initial conditions, which can be found from similar considerations as before:

$$V_{\mathrm{Cr},0} \approx \frac{1}{2} \cdot \frac{1}{C_{\mathrm{r}}} \cdot \left(2 \cdot i_{\mathrm{g,A}} \cdot n \cdot \frac{T_{\mathrm{s,N}}}{2} \right) \tag{5.16}$$

$$V_{\mathrm{Cr,LV},0} \approx \max \left(\frac{V_{\mathrm{Cr1},0}}{n} - 2 \cdot V_{\mathrm{f,LV}} \right) \tag{5.17}$$

The remaining initial conditions, i. e., $I_{\mathrm{T,MV},0}$ and $V_{\mathrm{S12},0} = V_{\mathrm{S21},0}$, vary for the four switching conditions at $t_{\mathrm{off},1\ldots4}$ shown in **Fig. 5.19b**. Referring all quantities to the LV side of the transformer, the four cases can be approximated as follows: once the resonant current becomes zero (i. e., at $t_{\mathrm{off},1}$ in **Fig. 5.19a**), a HF oscillation between the elements shown in **Fig. 5.20a** occurs, i. e., between L'_{σ}, the two LV bridge legs' parasitic capacitances, the series resonant capacitor, C_{r}, and the MV-side resonant capacitor, C'_{r1}.

The LV-bridge part of the equivalent circuit can be redrawn as shown in **Fig. 5.20b**, where the parasitic capacitances of the LV-side bridge legs are approximated by their charge-equivalent capacitance, $C_{\mathrm{Q,eq,LV}}$. Furthermore, $C_{\mathrm{r,LV}}$ is neglected because $C_{\mathrm{r,LV}} \gg C_{\mathrm{Q,eq,LV}}$. Applying Thévenin's theorem

and combining with the full circuit from **Fig. 5.20a** results in the intermediate simplification step shown in **Fig. 5.20c**. Thus, the initial conditions can be summarized as a total excitation voltage of

$$\delta V = V_{\mathrm{Cr1},0}/n - V_{\mathrm{Cr,LV},0} - V_{\mathrm{Cr},0}, \tag{5.18}$$

whereby $V_{\mathrm{S12},0} = V_{\mathrm{S21},0} = V_{\mathrm{Cr,LV},0}$, as holds at $t_{\mathrm{off},1}$, has been utilized. Because $C'_{\mathrm{r1}} \gg C_{\mathrm{Q,eq,LV}}$ and $C_{\mathrm{r}} \gg C_{\mathrm{Q,eq,LV}}$, C'_{r1} and C_{r} are then neglected in order to obtain the simple equivalent circuit in **Fig. 5.20d**. The characteristic impedance of this LC circuit is given by

$$z_0 = \sqrt{\frac{L_\sigma}{n^2} \cdot \frac{1}{C_{\mathrm{Q,eq,LV}}(V_{\mathrm{Cr,LV},0})}}, \tag{5.19}$$

and hence the amplitude of the oscillatory current becomes

$$\hat{i}_{\mathrm{osc}} = \frac{\delta V}{z_0}. \tag{5.20}$$

As shown in **Fig. 5.19a**, δV and $\hat{i}_{\mathrm{osc}}$ can be used to approximate the four sets of remaining initial conditions valid at $t_{\mathrm{off},1\ldots4}$, respectively, by adding and/or subtracting δV and $\hat{i}_{\mathrm{osc}}$ from $V_{\mathrm{Cr,LV},0}$ and $I_{\mathrm{M},0}$, respectively. Note that the (small) change of the magnetizing current, etc. during this short oscillatory interval is neglected, as is also a damping of the HF oscillation.

Optimization Procedure Generally, the optimization procedure is very similar as for the simplified case described above (cf. **Fig. 5.15**). There, analytic models have been employed to calculate the worst-case ΔV_{wc} and averaged relative losses, p_{loss}, for given tuples $\{L_{\mathrm{M}}, t_{\mathrm{d}}\}$ in case of constant t_{d} values over the grid period, or for given L_{M} in case of variable t_{d}. This procedure is changed and extended in the following two aspects:

- Instead of the analytic models, an approach based on simulations of the switching transitions, including nonlinear MOSFET capacitances, is employed (Wolfspeed C2M0045170D 1700 V/45 mΩ on the MV side, Wolfspeed X3M0010090X-ES 900 V/13 mΩ on the LV side [199]). To do so, the circuit shown in **Fig. 5.18** is parametrized with appropriate initial conditions and then simulated in GeckoCIRCUITS. In case of constant t_{d}, the simulation of a certain transition yields the switched voltage, ΔV, or, alternatively, the required dead time t_{d}^* for ΔV to become minimal, i. e., ideally equal to zero.

Tbl. 5.6: Resulting designs of the advanced ZVS optimization. Please refer to the text for a detailed description.

	W	X	M	N	Y	N'
L_M	1 mH	0.1 mH	0.525 mH	0.65 mH	0.225 mH	0.65 mH
t_d	400 ns	750 ns	variable	variable	300 ns	450 ns

- Because of the parasitic HF oscillations described above, each transition (i. e., for each tuple $\{L_M, t_d, p, v_g\}$) is simulated four times, whereby the four initial conditions corresponding to $t_{off,1\ldots4}$ are considered, respectively. From the four simulations, either the maximum ΔV (in case of constant t_d) can be obtained, or the suitable range of the dead time, $t_{d,min} \leq t_d \leq t_{d,max}$, such that the maximum ΔV among the four cases becomes minimal (cf. **Fig. 5.19b**) can be obtained.

The relative losses are calculated in the same way as described above, however, considering always a switching transition under nominal conditions, i. e., at $t_{off,1}$ according to **Fig. 5.19a**. Since, as discussed above, the switching losses under partial ZVS conditions are typically small, this is a feasible approximation.

Results of Detailed ZVS Analysis

As **Fig. 5.16** presents the results from the analytical ZVS considerations, **Fig. 5.21** shows the results of the detailed, simulation-based ZVS analysis and optimization. Again, **Fig. 5.21a** shows averaged relative losses and **Fig. 5.21b** shows the worst-case ΔV_{wc} in dependence of $\{L_M, t_d\}$, i. e., for cases considering a constant t_d over the grid period. Three trajectories are indicated: minimum p_{loss} (blue), minimum worst-case ΔV_{wc} assuming nominal switching conditions (i. e., switching at $t_{off,1}$) (orange), and minimum worst-case ΔV_{wc} considering all four switching conditions (i. e., switching at $t_{off,1\ldots4}$) (red). Following these trajectories, **Fig. 5.21c** shows the corresponding dependencies of p_{loss} and ΔV_{wc} on the magnetizing inductance, respectively. These dependencies are similar to the analytical results shown in **Fig. 5.16**.

Several specific designs listed in **Tbl. 5.6** are now analyzed in more detail. These designs are indicated in **Fig. 5.21c**, and **Fig. 5.22a** shows corresponding ΔV traces over half a grid period. Furthermore, **Fig. 5.22b** shows the corresponding relative losses as a function of the operating point, i. e., the power level.

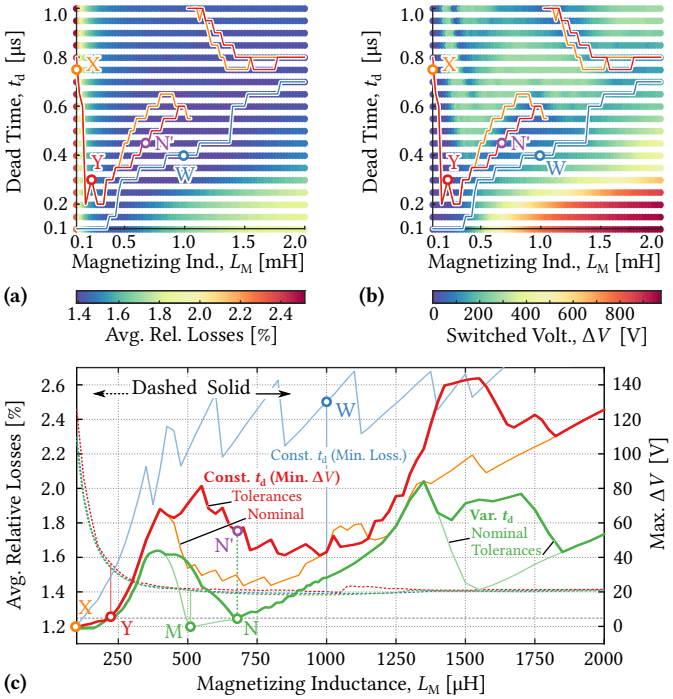


Fig. 5.21: Results of the advanced ZVS considerations. **(a)** averaged relative losses, p_{loss}, and **(b)** worst-case switched voltage, ΔV_{wc}, in dependence of $\{L_{\text{M}}, t_{\text{d}}\}$. Following the highlighted trajectories in (a) and (b), **(c)** shows the corresponding dependencies of p_{loss} (dashed lines) and ΔV_{wc} (solid lines) on the magnetizing inductance (note that the respective values of t_{d} are according to the trajectories given in (a) and (b)). The blue trajectory corresponds to minimum p_{loss}, the orange trajectory is for minimum ΔV_{wc} assuming switching at $t_{\text{off},1}$, and the red trajectory is for minimum ΔV_{wc} considering all four switching conditions, i. e., switching at $t_{\text{off},1\ldots4}$. The green curves in (c) are for cases where t_{d} is varied during the grid period such as to achieve minimum ΔV_{wc} for a given L_{M}; the bold curve considers component tolerances among the converter cells by taking into account the four different sets of initial conditions (cf. **Fig. 5.19**). Please refer to the text for a detailed explanation of the different highlighted designs. Note that the ragged appearance of the ΔV_{wc} traces is due to the limited resolution of the L_{M} and t_{d} search ranges.

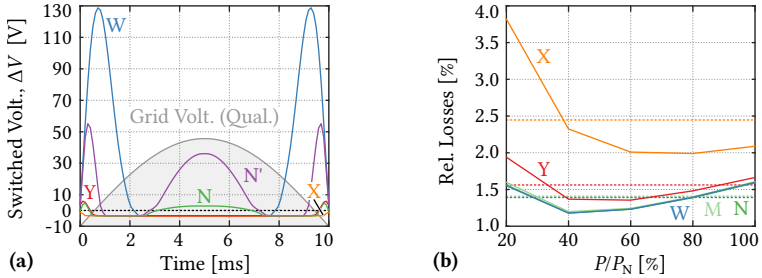


Fig. 5.22: (a) Switched voltage over half a grid period for different designs (W and X are for switching under nominal conditions, i. e., at $t_{\mathrm{off},1}$; Y, N and N' consider all four switching conditions, i. e., switching at $t_{\mathrm{off},1\ldots4}$, and thus show the worst-case ΔV curve that is to be expected in a multi-cell system). **(b)** Calculated efficiency curves for specific designs. In addition, also the averaged relative losses (as, e. g., shown in **Fig. 5.21**) are indicated.

- Design W is the minimum loss design using a constant t_{d}, which, in contrast, still shows quite high maximum ΔV values in the vicinity of the zero-crossing of the grid voltage.
- Design X: also using a constant t_{d}, this design realizes a worst-case ΔV_{wc} of almost 0 V, however, with much higher losses as a consequence of its higher magnetizing current and the longer dead time. Since these losses are independent of the load, especially the part-load efficiency suffers.
- Design M: considering now a variable t_{d}, this is the design that achieves lowest ΔV if only switching under nominal conditions (i. e., at $t_{\mathrm{off},1}$) is considered. This is the design that would be chosen in case a tuning of $f_{\mathrm{s,N}}$ to achieve these conditions would be possible, e. g., in a single-cell system. As design X, design M realizes also a worst-case ΔV_{wc} close to 0 V, however, with losses that are much lower and comparable to those of design W.
- Design N is the variable dead time design with the lowest worst-case ΔV_{wc} considering all four switching conditions (i. e., switching at $t_{\mathrm{off},1\ldots4}$), achieving $\Delta V_{\mathrm{wc}} \leq 10\,\mathrm{V}$, which is less than 1 % of $\hat{v}_{\mathrm{g,c}}$. Note again that the losses are comparable to those of design W. This design constitutes the optimal choice for a multi-cell system, where the switching conditions may vary among the cells due to component tolerances.

- Design Y is a design with constant dead time that shows comparable worst-case ΔV_{wc} values as design N. However, this comes at the price of higher losses.

- Design N': finally, design N' is a design using the same L_{M} as design N, but a constant dead time such as to result in lowest worst-case ΔV_{wc}, which is, as expected, significantly higher than that achievable with a variable t_{d}.

The basic trade-offs are thus similar to those identified for the simplified case discussed earlier. However, it can be seen in **Fig. 5.21c** that the range of suitable L_{M} values is quite constrained if low worst-case ΔV_{wc} (to reduce EMI originating from partial hard switching) *and* low losses shall be achieved, even in case a variable dead time is used. One reason for this is that there are situations where the voltage across S_3 does not swing completely to zero at all, because the LV-side diodes start to conduct early. This is an effect that could not be captured with the simplified, analytical model.

Considering design N (optimized for minimum ΔV_{wc} considering all four variants of the switching transitions), **Fig. 5.23a** shows the resulting minimum and maximum boundaries for the dead time as a function of the cell AC input voltage, $v_{\mathrm{g,c}}$. Note that for low input voltages, the two curves intersect, i. e., $\min(t_{\mathrm{d,max}}) < \max(t_{\mathrm{d,min}})$, indicating that a certain dead time might be too short for switching at, e. g., $t_{\mathrm{off},2}$, whereas it is already too long if the switching occurs at, e. g., $t_{\mathrm{off},4}$ (cf. **Fig. 5.19a**). Depending on tolerances, the switching conditions vary among the cells. This is the reason why for many L_{M} values it is not easily possible to obtain $\Delta V_{\mathrm{wc}} \leq 0\,\mathrm{V}$, i. e., full-range ZVS for all cells, even with a variable dead time.

Verification

In order to implement the variable dead time of design N in a full system simulation consisting of five cascaded converter cells, each fully modeled with nonlinear parasitic capacitances on the MV and on the LV side, a look-up table (LUT) is used to store the required dead time as a function of the cell's input voltage. According to **Fig. 5.23a**, $t_{\mathrm{d,LUT}}$ is obtained by taking a weighted average,

$$t_{\mathrm{d,LUT}} = \frac{1}{3} \cdot \left(2 \cdot \max\left(t_{\mathrm{Min}}\right) + \min\left(t_{\mathrm{d,max}}\right)\right) . \tag{5.21}$$

This value is limited to $\max(t_{\mathrm{d,min}})$ for values of $v_{\mathrm{g,c}}$ where $\max(t_{\mathrm{d,min}}) > \min(t_{\mathrm{d,max}})$, resulting in the orange curve shown in the figure.

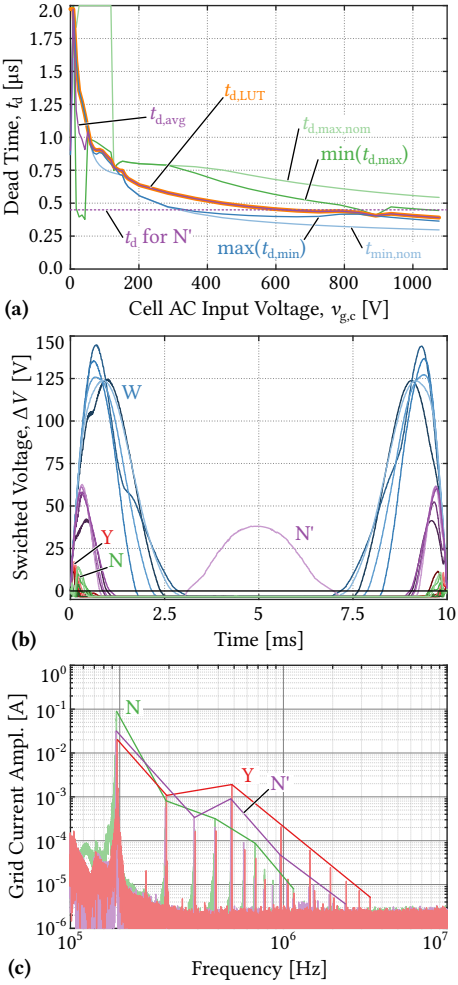


Fig. 5.23: (a) Valid t_d range for design N and chosen $t_{d,LUT}$ for the look-up table used in the full-system simulation; **(b)** simulated ΔV of the five converter cells for different designs (cf. **Fig. 5.21**), and **(c)** corresponding grid current spectra.

In each of the five cascaded *a*IFE cells used in the simulation model, the value of L_σ is varied slightly (9.5 µH, 9.75 µH, 10 µH, 10.25 µH, 10.5 µH) in order to create non-equal resonant frequencies among the cells and hence emulate tolerances, which cause varying switching conditions among the cells as discussed above. **Fig. 5.23b** shows the simulated ΔV values (obtained by sampling the voltage across, e. g., S_3, when it is turned on) for various designs over half a grid period. A good agreement with the predictions from the optimization (cf. **Fig. 5.22a**) can be observed. It can also be seen how the ΔV values vary between the different cells; e. g., for design N' only one cell switches under conditions that cause a loss of ZVS in the middle of the grid period. Note that this has to be expected, considering that the constant t_d of design N' violates the limits (i. e., $\max(t_{\mathrm{d,min}})$ and $\min(t_{\mathrm{d,max}})$) not only for low but also for high voltages according to **Fig. 5.23a**.

In order to reduce the harmonic content of the grid current, the S³T's *a*IFE stages are operated in an interleaved manner (cf. Section 5.1.3). Therefore, **Fig. 5.23c** shows the resulting spectra of the grid current for three designs. It can be seen that design N (variable dead time), has a higher peak at around 100 kHz, i. e., twice the individual *a*IFE stage switching frequency, indicating that a variable dead time compromises the interleaving of the cells (even though the dead time variation is the same for all cells). On the other hand, the higher order harmonics are spread over a wider frequency range, resulting in lower peaks. It is also interesting to notice that design Y, which achieves low ΔV_wc by means of a large magnetizing current and long but constant t_d, suffers from even higher peaks at higher frequencies, which is a consequence of the magnetizing current distorting the voltages across the input capacitors to a degree that visibly worsens the harmonic content of the grid current.

Discussion

The above detailed analysis of the ZVS behavior of the HC-DCM SRC in |AC|-DC applications, e. g., IFE-based SSTs such as the S³T, can be summarized in a few design guidelines.

If EMI is not of concern, a combination of a magnetizing inductance and a dead time that results in low (or lowest) losses can easily be identified. However, such designs typically do not achieve complete ZVS over the entire grid period.

If, in contrast, the maximum worst-case switched voltage should be limited to very low values, e. g., 10 V or ideally even 0 V (full-range ZVS), there are two options: first, another combination of magnetizing inductance and dead time that fulfills this requirement can be found. However, increased losses

and especially a massively reduced part-load efficiency are the price to pay. Furthermore, the HF harmonic content of the grid current is increased.

Second, the dead time could be varied over the grid period, which allows to use a comparably large magnetizing inductance and hence results in low losses. On the other hand, the implementation of a variable dead time increases the complexity, and a variable dead time compromises the interleaved operation of the *a*IFE stages, resulting in a slightly higher harmonic amplitude at about twice the *a*IFE stage switching frequency, whereas in contrast, harmonic peak values at higher frequencies are reduced.

Note that for applications where bidirectional power flow is required, the presented analysis could be repeated also for the case where the LV-side bridge is actively switching in order to identify a suitable magnetizing inductance and, possibly variable, dead times for both bridges.

It is thus possible to achieve ZVS over the entire grid period, however, either at the price of increased complexity or increased losses. With the aim of low complexity solutions, another option could be to use a constant dead time, causing a loss of ZVS in a sufficiently narrow region around the grid voltage zero crossings only, and then to simply stop switching the *a*IFE stages around these zero crossing, which is a concept employed, e. g., in single-phase LV PFC rectifier circuits operating in triangular current mode (TCM) [202]. This would basically trade EMI performance (no partial hard switching) against grid current distortions at lower frequencies, and could be a pragmatic approach that would allow to keep the control complexity low.

5.2.3 Summary

This section provides a detailed analysis of the ZVS behavior of the resonant isolation stages of an IFE SST, using the example of the S³T, an all-SiC 25 kW, 6.6 kV AC to 400 V DC IFE-based SST. Essentially, these resonant isolation stages are SRCs operated in HC-DCM, however, not with DC but with grid-frequency |AC| input and output voltages. Thus, the magnetizing current available for ZVS varies over the grid period, as does the voltage that needs to be switched. The magnetizing inductance and the dead time can be chosen such as to result in lowest overall losses, however, without achieving complete ZVS over the entire grid period. If full-range ZVS is required, e. g., to reduce EMI emissions, a larger magnetizing current and/or a longer dead time must be used, both increasing the losses. As an alternative, the dead time can be varied during the grid period, which allows to obtain both, (almost) full-range ZVS and low losses, however, with a slightly more complicated modulation

Tbl. 5.7: Estimation of the input voltage polarity from the LV transformer voltage and the gating signals for the MV switches.

Meas. Transf. LV Volt.	MV On-Switches	Est. Grid Volt. Pol.
$v_{\mathrm{T,LV,meas}} > 0$	S_1/S_2	$v_{\mathrm{g,c}} > 0$
$v_{\mathrm{T,LV,meas}} < 0$	S_1/S_2	$v_{\mathrm{g,c}} < 0$
$v_{\mathrm{T,LV,meas}} > 0$	S_3/S_4	$v_{\mathrm{g,c}} < 0$
$v_{\mathrm{T,LV,meas}} < 0$	S_3/S_4	$v_{\mathrm{g,c}} > 0$

scheme including, e. g., a lookup table for the dead time. The analysis includes also the effects of component tolerances among the cascaded converter cells in a multi-cell IFE SST, and is finally verified using a very detailed simulation model, including nonlinear MOSFET capacitances and component tolerances.

5.3 Control Considerations

An important benefit of the IFE concept is its low complexity on the MV side, especially the absence of any measurement circuits there, as indicated in **Fig. 5.2**. In the following, it is briefly described how the S³T's isolation front end can be modulated and how the entire S³T system can be controlled without requiring MV-side measurements.

5.3.1 Input Voltage Polarity Estimation

When the MV-side bridge of an *a*IFE cell is realized with bidirectional switches in order to directly interface the AC grid (other options will be described in the next **Chapter 6**), the bridge leg integrates the folding of the grid voltage and the chopping of the input AC voltage for the SRC operation. In order to apply the proper gating commands to the four switches on the MV side, the polarity (not the value!) of the input AC voltage needs to be known.

During startup, one of the bidirectional pairs, e. g., S_1/S_2, can be turned on. It is then sufficient to measure the voltage (polarity) on the LV side of the transformer (of at least one converter cell), to deduce the polarity of the grid voltage (cf. **Tbl. 5.7**), which allows then to turn on the folding switch of the other bidirectional pair, and to start the switching operation. As an example, consider the circuit in **Fig. 5.3b** and the polarity of $v_{\mathrm{g,c}}$ as indicated. Turning on S_1/S_2 results in $v_{\mathrm{T,LV,meas}} > 0\,\mathrm{V}$, which corresponds to a positive grid voltage polarity. Hence, S_2 and S_4 would be the folding switches and

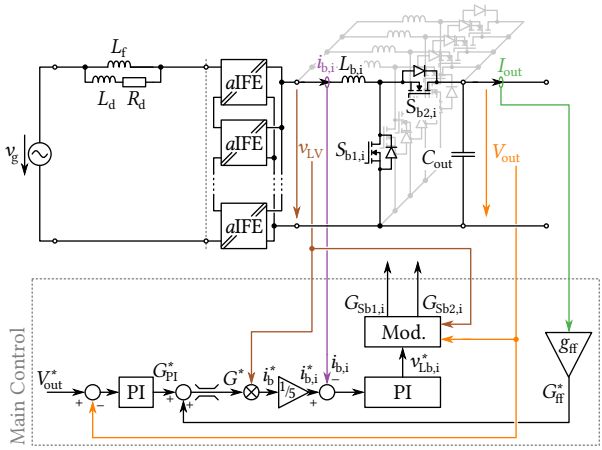


Fig. 5.24: Overview of the S³T's control structure that utilizes only LV-side measurements (input polarity estimation not shown).

therefore be turned on continuously (as long as the polarity of $v_{g,c}$ remains unchanged), whereas S_1 and S_3 would start HF switching.

During steady state, the grid voltage polarity can be monitored in the same way, and the gating signals for the isolation stage bridges can be generated appropriately.

5.3.2 System-Level Control without MV Measurements

Fig. 5.24 shows again the S³T topology and the control circuit required to regulate the output voltage, V_{out}, and to operate with unity power factor at the grid side. Note that only LV-side quantities are measured. Furthermore, the grid filter is realized using a parallel RL damping branch which is designed according to the procedure given in [188], resulting in $L_f = 400\,\mu H$, $L_d = 100\,\mu H$, and $R_d = 25.5\,\Omega$. The boost converter is implemented using five parallel stages (i. e., combinations of $L_{b,i}$, $S_{b1,i}$ and $S_{b2,i}$), which are based on the same power semiconductors as the LV stages of the *a*IFE cells. Each of these boost stages features its own current control loop, which regulates the stage's boost current, $i_{b,i}$, according to the reference value $i^*_{b,i} = 1/N \cdot i^*_b$, where $N = 5$ denotes the number of parallel boost converters. A switching frequency of 50 kHz, a boost inductance of 200 µH, and a common output DC capacitor of 10 mF are considered here. Furthermore, a (damped) decoupling

inductor of 40 µH (not shown in the figure) is connected at the output of each *a*IFE stage in order to reduce interactions of the LV resonant capacitors of the *a*IFE stages.

To control the average value of the output voltage (i. e., the voltage ripple caused by the single-phase power fluctuation cannot be removed, and C_{out} must be chosen such that this voltage ripple remains within desired limits), a PI controller acts on the output voltage deviation (at frequencies sufficiently lower than twice the grid frequency) and generates a reference conductance, G^*_{PI}. Additionally, the output load current, I_{out}, is measured and used to calculate a feed-forward value for the required reference conductance with

$$G^*_{\text{ff}} = \frac{8n^2 n^2_{\text{cell}}}{\hat{v}^2_{\text{g}}} \cdot V^*_{\text{out}} \cdot I_{\text{out}}, \tag{5.22}$$

where $n = 1.75$ denotes the *a*IFE stage transformer turns ratio and $n_{\text{cell}} = 5$ the number of cascaded *a*IFE cells. The feed-forward conductance, G^*_{ff}, and the output voltage controller output, G^*_{PI}, are summed and the resulting conductance $G^* = G^*_{\text{ff}} + G^*_{\text{PI}}$ is then used to calculate a current reference for the boost inductor current, $i^*_{\text{b}} = G^* \cdot v_{\text{LV}}$. This reference value is distributed equally among the interleaved boost converters as mentioned above. Note that G^* can be limited in order to avoid excessive currents.

Fig. 5.25 shows simulation results of the S³T with the output voltage controller setup described above, where a step of the output current, I_{out}, from 31.25 A (50 %) to 62 A (100 %, i. e., rated current) is considered. It can be seen that the deviation of the average output voltage (i. e., without considering the voltage ripple at twice the grid frequency) remains small, which is largely due to the fast reaction of the feed-forward path on the change of the load current. The PI controller then quickly brings the average output voltage back to the nominal value of 400 V. Note also that the power factor at the MV grid side is very close to unity.

5.3.3 Compensation of MV Side Capacitive Reactive Power Consumption

However, since the (comparably small) MV-side resonant capacitors of the *a*IFE cells are directly connected to the grid (cf. **Fig. 5.12**), the fundamental-frequency reactive power that is consumed by these capacitors does not depend on the load. Therefore, the fundamental frequency power factor (displacement power factor), $\cos\varphi_{(1)}$, becomes worse for lower output power levels, as can be seen from **Fig. 5.26a**.

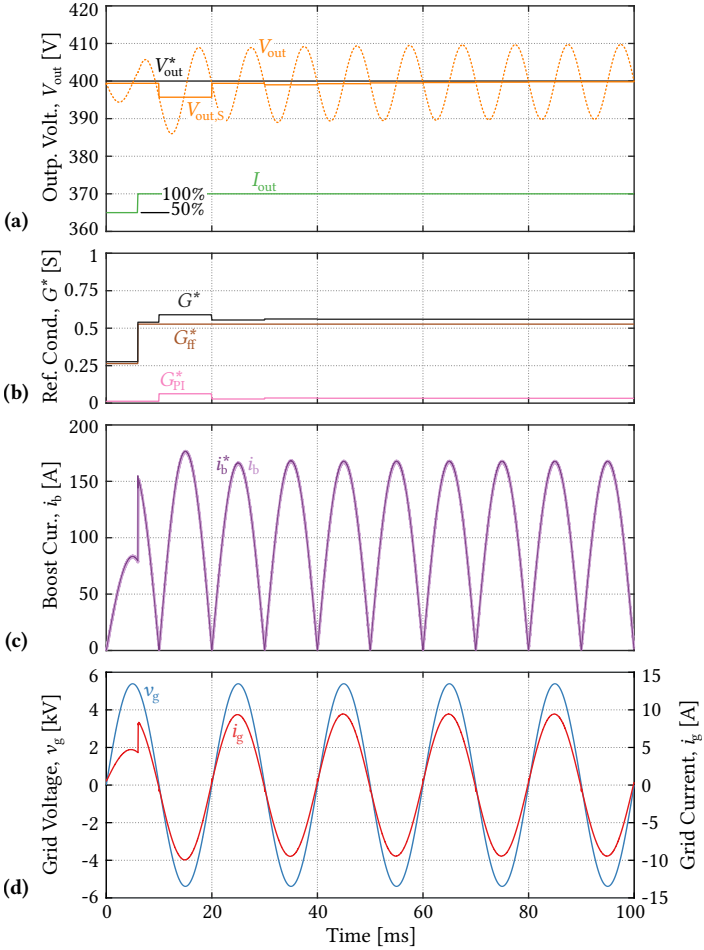


Fig. 5.25: Simulated controller behavior for a step from 50 % to 100 % (rated) load current. **(a)** Output voltage, **(b)** reference conductances, **(c)** boost inductor current reference and real value (note: superposition of the individual stages' boost currents that is seen by the *a*IFE stage), and **(d)** MV-side grid voltage and current.

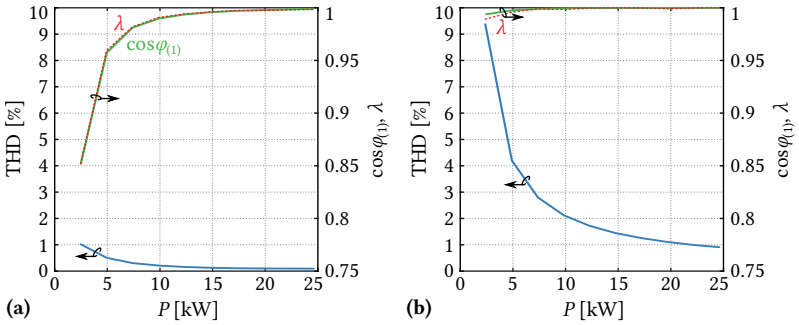


Fig. 5.26: Fundamental-frequency power factor, $\cos\varphi_{(1)}$, power factor, λ, and THD in dependence of the output power **(a)** without and **(b)** with compensation of the capacitive reactive power of the MV-side resonant capacitors.

By either considering a feed-forward approach or by measuring the grid current and voltage directly, it is possible to provide the reactive power consumed by the MV-side capacitors from the LV side, if the boost stage current reference is adjusted accordingly. However, as has been discussed in Section 5.1, then the limited bandwidth of the *a*IFE stages causes glitches in the grid current at the zero crossings of the grid voltage. Also, the dynamic property of the boost stage current control loop affects this, however, with an interleaved converter approach a high bandwidth can be achieved. In any case, **Fig. 5.26b** shows that it is possible to ensure very high $\cos\varphi_{(1)}$ also at lower power levels with this approach, i. e., that it is possible to compensate the reactive power consumed by the MV-side capacitors. On the other hand, the associated distortions in the grid current cause the THD to increase significantly. This is also reflected in the power factor, λ, which includes also the distortion reactive power caused by higher harmonics. Thus, λ is lower than $\cos\varphi_{(1)}$ for lower output power levels.

6 Comparative Evaluation of the IFE and the IBE Concepts

Following [54], a generic comparison of an IFE MVAC-LVDC SST (cf. **Fig. 6.1a**) and a corresponding IBE system (cf. **Fig. 6.1b**), both with resonant isolation stages, will be provided, considering the realization effort for the main components (power semiconductors and transformers) and their stresses. A brief case study will be presented after this theoretical comparison in order to render the discussion more tangible.

6.1 Generic Comparative Evaluation

The generic comparative evaluation is based on analytic expressions for the main component stresses found in both, IFE and IBE SSTs, which will be derived in the following.

Number of Cascaded Cells

In a cascaded cells system, the number of required cells follows from the peak phase voltage, $\hat{v}_\mathrm{g} = \sqrt{2}V_\mathrm{ph}$, the semiconductor voltage blocking capability, $V_\mathrm{B,MV}$, its utilization, u, and the nominal modulation index, M_N, as

$$N_\mathrm{IFE} = \frac{\sqrt{2}V_\mathrm{ph}}{uV_\mathrm{B,MV}} \qquad N_\mathrm{IBE} = \frac{\sqrt{2}V_\mathrm{ph}}{M_\mathrm{N}uV_\mathrm{B,MV}}. \tag{6.1}$$

Thus, $N_\mathrm{IFE}/N_\mathrm{IBE} = M_\mathrm{N} < 1$ highlights the IFE's advantage in terms of the required total MV blocking voltage (or number of cascaded cells), which is a result of shifting the boost function to the LV side. Note that for a physical realization of course $\lceil N_\mathrm{IFE} \rceil$ and $\lceil N_\mathrm{IBE} \rceil$ needed to be considered.

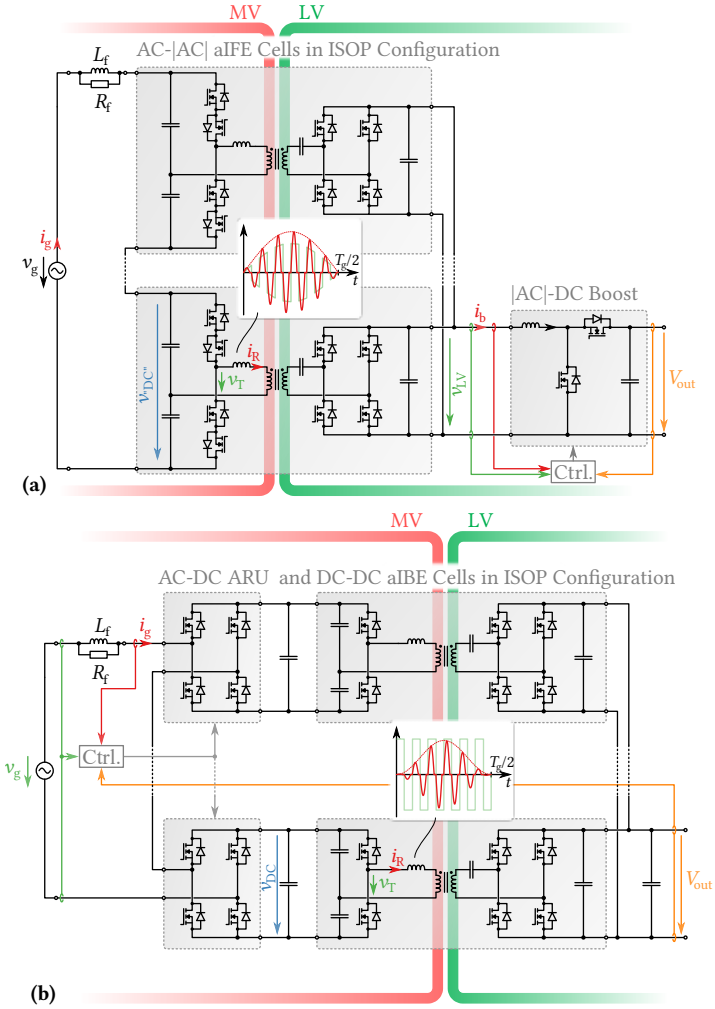


Fig. 6.1: Power circuits of the IFE **(a)** and the IBE **(b)** MVAC-LVDC SSTs considered in the comparative evaluation. Note that the number of cascaded cells is different for the two systems (cf. (6.1)), and that the boost stage of the IFE system would be realized in practice from several smaller boost stages using parallel interleaving.

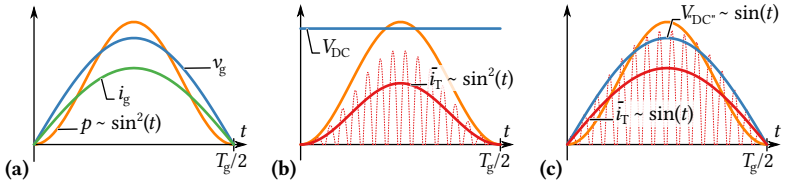


Fig. 6.2: Power transfer in **(a)** a single-phase grid, **(b)** in an IBE, and **(c)** in an IFE system.

Transformers

A key difference between the IFE and the IBE system is the envelope of the switched transformer voltage. Assuming unity power factor operation, the power in single-phase systems (or also in phase-modular three-phase ISOP systems) is proportional to a $\sin^2$-function, as illustrated in **Fig. 6.2a**. In an IBE system based on resonant isolation stages such as considered here, this power fluctuation is transferred through the transformers, as has been discussed in Section 4.1. Because the DC voltage is rather constant, the local average value of the transformer current also follows a $\sin^2$-function (cf. **Fig. 6.2b**). However, this is different in the IFE system, where the envelope of the transformer voltage is proportional to a sin-function, resulting in the local average of the transformer current also being proportional to a sin-function (cf. **Fig. 6.2c**). Hence, the transformer RMS current of the IFE system can be derived starting with the relation

$$\overline{i}_{\mathrm{R,IFE}}(t) \cdot \overline{v}_{\mathrm{T,IFE}}(t) \stackrel{!}{=} \frac{\overline{p}_{\mathrm{g}}(t)}{N_{\mathrm{IFE}}}, \tag{6.2}$$

where $\overline{x}$ denotes a local average value over half a switching cycle. With

$$\overline{p}_{\mathrm{g}}(t) = 2P \sin^2(2\pi f_{\mathrm{g}} t) \tag{6.3}$$

and, in the case of a half-bridge configuration (factor 1/2),

$$\overline{v}_{\mathrm{T,IFE}}(t) = \frac{\sqrt{2}}{2N_{\mathrm{IFE}}} V_{\mathrm{ph}} \sin(2\pi f_{\mathrm{g}} t), \tag{6.4}$$

the local average value of the MV-side transformer current in a single cell becomes

$$\overline{i}_{\mathrm{R,IFE}}(t) = \frac{2\sqrt{2}P}{V_{\mathrm{ph}}} \sin(2\pi f_{\mathrm{g}} t), \tag{6.5}$$

where P denotes the rated power of a single-phase system and V_{ph} the phase RMS voltage. Assuming piecewise sinusoidal transformer current pulses, the relation between local average and local RMS values is given by (cf. Section 3.2.1)

$$\tilde{i}_{\mathrm{R,IFE}}(t) = \sqrt{\frac{\pi^2}{8} \cdot \frac{f_0}{f_\mathrm{s}}} \cdot \bar{i}_{\mathrm{R,IFE}}(t), \tag{6.6}$$

where f_0 and f_s are the resonant and the switching frequency of the SRC stage, respectively. The transformer RMS current over a grid period can then be calculated with

$$\tilde{I}_{\mathrm{R,IFE}} = \sqrt{2 f_\mathrm{g} \int_0^{\frac{1}{2f_\mathrm{g}}} \tilde{i}_{\mathrm{R,IFE}}(t)^2 dt} = \frac{\sqrt{2}}{2} \cdot \frac{\pi P}{V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_\mathrm{s}}}. \tag{6.7}$$

Likewise, the transformer current for the IBE system becomes

$$\tilde{I}_{\mathrm{R,IBE}} = \frac{\sqrt{6} M_\mathrm{N}}{4} \cdot \frac{\pi P}{V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_\mathrm{s}}}. \tag{6.8}$$

Note that a direct comparison of the results for the transformer currents of the IFE and the IBE system is not meaningful, since the rated power per transformer is lower for the IBE system, because $N_{\mathrm{IBE}} > N_{\mathrm{IFE}}$, i. e., the currents differ because $\bar{i}_{\mathrm{R,IBE}} \propto \sin^2(2\pi f_\mathrm{g} t)$ and $\bar{i}_{\mathrm{R,IFE}} \propto \sin(2\pi f_\mathrm{g} t)$, but also because of M_N and hence the different number of cascaded cells.

Instead, the area products of the transformers can be calculated as

$$(A_\mathrm{c} A_\mathrm{w})_{\mathrm{IFE}} = \frac{\sqrt{2} V_{\mathrm{ph}}}{2 N_{\mathrm{IFE}}} \cdot \frac{\tilde{I}_{\mathrm{R,IFE}}}{k f_\mathrm{s} B_{\mathrm{max}} J_{\mathrm{rms}}} \quad \text{and} \tag{6.9}$$

$$(A_\mathrm{c} A_\mathrm{w})_{\mathrm{IBE}} = \frac{\sqrt{2} V_{\mathrm{ph}}}{2 M_\mathrm{N} N_{\mathrm{IBE}}} \cdot \frac{\tilde{I}_{\mathrm{R,IBE}}}{k f_\mathrm{s} B_{\mathrm{max}} J_{\mathrm{rms}}}. \tag{6.10}$$

Considering (6.1), the area product of a single transformer of the IFE system is larger than that of an IBE system's transformer because of the difference in RMS currents only; however, the IBE system requires more transformers. The "total" area products of the IFE and the IBE concept compare as

$$\frac{N_{\mathrm{IFE}} \cdot (A_\mathrm{c} A_\mathrm{w})_{\mathrm{IFE}}}{N_{\mathrm{IBE}} \cdot (A_\mathrm{c} A_\mathrm{w})_{\mathrm{IBE}}} = \frac{2}{\sqrt{3}} \approx 1.15, \tag{6.11}$$

and the ratio of the total transformer volumes accordingly as

$$\frac{V_{\mathrm{T,IFE}}}{V_{\mathrm{T,IBE}}} \propto \frac{N_{\mathrm{IFE}} \cdot (A_{\mathrm{c}} A_{\mathrm{w}})_{\mathrm{IFE}}^{3/4}}{N_{\mathrm{IBE}} \cdot (A_{\mathrm{c}} A_{\mathrm{w}})_{\mathrm{IBE}}^{3/4}} = \left(\frac{2^3 M_{\mathrm{N}}}{3\sqrt{3}} \right)^{\frac{1}{4}} \approx 1.05, \tag{6.12}$$

where $M_{\mathrm{N}} = 0.8$ has been assumed to obtain a numerical result. The total usage of active materials is thus comparable.

In order to analyze the transformer losses, it is now assumed that identical transformers are used in both systems. Core loss densities can be estimated using the Steinmetz equation, $p_{\mathrm{c}} = k f^{\alpha} \hat{B}^{\beta}$, where $\beta \approx 2 \ldots 2.5$ for typical core materials suitable for MFTs. Whereas in the IBE system, $\hat{B}$ is constant and hence the transformer core loss density is given by

$$p_{\mathrm{c,IBE}} = k f_{\mathrm{s}}^{\alpha} B_{\mathrm{max}}^{\beta}, \tag{6.13}$$

it varies with the grid voltage in the IFE system (cf. **Fig. 6.2c**), i. e., $\hat{B}_{\mathrm{IFE}}(t) = B_{\mathrm{max}} \sin(2\pi f_{\mathrm{g}} t)$, if the same maximum flux density, B_{max} is allowed in both systems. Therefore, the core loss density in the IFE system can be found by averaging over a grid period,

$$p_{\mathrm{c,IFE}} = \frac{2}{T_{\mathrm{g}}} \int_0^{T_{\mathrm{g}}/2} k f_{\mathrm{s}}^{\alpha} B_{\mathrm{max}}^{\beta} \sin^{\beta}(2\pi f_{\mathrm{g}} t) dt. \tag{6.14}$$

For $\beta = 2$, this integral can be solved analytically, resulting in

$$p_{\mathrm{c,IFE}} = 1/2 \cdot k f_{\mathrm{s}}^{\alpha} B_{\mathrm{max}}^{\beta}, \tag{6.15}$$

i. e., $p_{\mathrm{c,IFE}} / p_{\mathrm{c,IBE}} \leq 1/2$ for $\beta \geq 2$. In contrast, the winding loss densities scale with the current densities squared and since the same core geometries are assumed, with the transformer RMS currents according to

$$\frac{p_{\mathrm{w,IFE}}}{p_{\mathrm{w,IBE}}} = \left(\frac{\tilde{I}_{\mathrm{R,IFE}}}{\tilde{I}_{\mathrm{R,IBE}}} \right)^2 = \frac{4}{3 M_{\mathrm{N}}^2} \approx 2.08. \tag{6.16}$$

Assuming further that the IBE transformers are designed with a 1:1 ratio between core and winding losses at rated power, the total transformer losses compare as

$$\frac{p_{\mathrm{T,IFE}}}{p_{\mathrm{T,IBE}}} = \frac{N_{\mathrm{IFE}} \cdot \left(\frac{1}{2} \frac{p_{\mathrm{c,IFE}}}{p_{\mathrm{c,IBE}}} + \frac{1}{2} \frac{p_{\mathrm{w,IFE}}}{p_{\mathrm{w,IBE}}} \right)}{N_{\mathrm{IBE}} \cdot \left(\frac{1}{2} + \frac{1}{2} \right)} = \left(\frac{M_{\mathrm{N}}}{4} + \frac{2}{3 M_{\mathrm{N}}} \right), \tag{6.17}$$

Tbl. 6.1: Expressions for the semiconductor currents and the transformer turns ratio in the IFE and IBE converter cells.

	$\tilde{I}_{\mathrm{ARU}}$	$\tilde{I}_{\mathrm{SRC,MV}}$	n	$\tilde{I}_{\mathrm{SRC,LV}}$
IFE		$\frac{\pi P}{2V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}}$	$\frac{uV_{\mathrm{B,MV}}}{2V_{\mathrm{out}}M_{\mathrm{N}}}$	$n_{\mathrm{IFE}} \cdot \tilde{I}_{\mathrm{SRC,MV,IFE}}$
IBE	$\frac{2\sqrt{2}P}{V_{\mathrm{ph}}}$	$\frac{\sqrt{3}\pi P M_{\mathrm{N}}}{4V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}}$	$\frac{uV_{\mathrm{B,MV}}}{2V_{\mathrm{out}}}$	$n_{\mathrm{IBE}} \cdot \tilde{I}_{\mathrm{SRC,MV,IBE}}$

	$\tilde{I}_{\mathrm{B,Shunt}}$	$\tilde{I}_{\mathrm{B,Series}}$
IFE	$\frac{2\sqrt{3}Pn_{\mathrm{IBE}}}{3V_{\mathrm{ph}}} \cdot \sqrt{3 - \frac{4\sqrt{2}V_{\mathrm{ph}}}{\pi N_{\mathrm{IFE}} n_{\mathrm{IFE}} V_{\mathrm{out}}}}$	$\frac{4\sqrt{3}P}{3} \cdot \sqrt{\frac{\sqrt{2}n_{\mathrm{IFE}}}{\pi V_{\mathrm{ph}} N_{\mathrm{IFE}} V_{\mathrm{out}}}}$
IBE		

resulting in 1.03 for $M_{\mathrm{N}} = 0.8$. Accordingly, the total transformer losses are comparable. Note that with the assumption of using the same core and winding arrangement, the total transformer volume of the IFE system amounts to only M_{N} (< 1) times that of the IBE concept. An optimized IFE transformer would thus use a slightly different core geometry, offering a larger winding window and a smaller core cross section, because a higher utilization of the core (with sufficient margin towards saturation) could be tolerated.

Power Semiconductors

A comparison of the semiconductor requirements of two different converter topologies can be based on the sum of all devices' RMS currents [203], since

$$P_{\mathrm{cond}} \propto \sum \tilde{I}_{\mathrm{x}} \propto A_{\mathrm{chip}}. \tag{6.18}$$

The RMS currents of the power semiconductors in the SRC isolation stages can be calculated from the transformer currents, and, on the LV side, the transformer turns ratio, n. The RMS currents of the IBE cells' ARUs follow from the grid current, and the RMS currents of the IFE's boost stage switches (considering one boost stage per IFE cell) can be analytically calculated, too. **Tbl. 6.1** contains the corresponding expressions. Note that it is assumed that all rectifier stages operate actively, i. e., only FETs are considered.

Using the number of devices according to **Fig. 6.1** and N_{IFE} and N_{IBE}, respectively, the sums of the MV-side and of the LV-side semiconductor RMS currents can be compared (assuming $f_{\mathrm{s}} = f_0$ and $M_{\mathrm{N}} = 0.8$ for the numerical

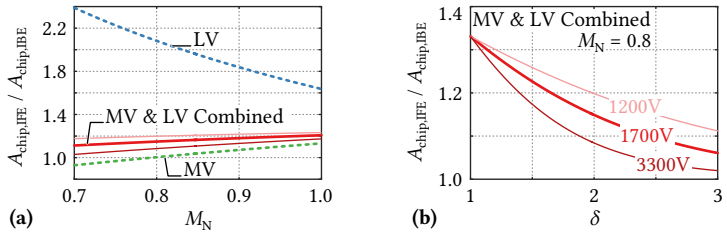


Fig. 6.3: Ratio of the chip area requirements of IFE and IBE systems as a function of the nominal modulation index, M_N, in **(a)**, and in **(b)** as a function of δ in $r_{on} \propto V_B^{\delta}$ for $M_N = 0.8$. For the combined metric, $u = 0.66$, $f_s = f_0$, $V_{out} = 400\,V$ is assumed, and three different MV semiconductor blocking voltages are considered. Note that the three curves in (b) intersect for $\delta = 1$, i. e., for $r_{on} \propto V_B$, where hence the MV-side conduction losses do not depend on the chosen blocking voltage for a given total chip area.

result),

$$\frac{\sum \tilde{I}_{x,MV,IFE}}{\sum \tilde{I}_{x,MV,IBE}} = \frac{4\pi M_N}{\sqrt{3}\pi M_N + 4\sqrt{2}} \approx 1.00, \quad \text{and} \quad \frac{\sum \tilde{I}_{x,LV,IFE}}{\sum \tilde{I}_{x,LV,IBE}} = f(M_N) \approx 2.08. \tag{6.19}$$

Fig. 6.3a shows these ratios, which according to (6.18) correspond to the ratios of the required chip area, as a function of M_N, which is the only variable these metrics depend on. The semiconductor area requirement on the LV side is thus significantly larger for the IFE than for the IBE.

In order to merge the ratios for the MV and for the LV side into a single characteristic value, the theoretical scaling of the specific on-state resistance with the blocking voltage is considered, which for SiC FETs is given by [93, 204]:

$$r_{on} \propto V_B^{\delta} \qquad \delta \approx 2 \ldots 2.5 \tag{6.20}$$

In order to account for the lower specific on-state resistance, and the hence lower chip area requirement for the same loss density (as implied by the linear sum of device RMS currents in (6.18)) of the LV-side power devices, the contributions of the LV devices' RMS currents need to be scaled according to

$$\tilde{I}'_{x,LV,\ldots} = \left(\frac{V_{B,LV}}{V_{B,MV}}\right)^{\delta} \cdot \tilde{I}_{x,LV,\ldots}, \quad \text{where} \quad V_{B,LV} = \frac{V_{out}}{u_{LV}}, \tag{6.21}$$

and where u_{LV} denotes the blocking voltage utilization of the LV-side semiconductors, which is assumed to be equal to u on the MV side. From that, an

aggregated ratio of the total chip area requirements of both concepts can be derived as

$$\frac{A_{\text{chip,IFE}}}{A_{\text{chip,IBE}}} \propto \frac{\sum \tilde{I}_{\text{x,MV,IFE}} + \sum \tilde{I}'_{\text{x,LV,IFE}}}{\sum \tilde{I}_{\text{x,MV,IBE}} + \tilde{I}'_{\text{x,MV,IBE}}} \approx 1.15, \tag{6.22}$$

where the numerical value is given for $\delta = 2$, $M_{\text{N}} = 0.8$, $u = 0.66$, $V_{\text{out}} = 400\,\text{V}$, $V_{\text{B}} = 1700\,\text{V}$, and $f_{\text{s}} = f_0$. Hence, the IFE system requires about 15 % more chip area than the IBE system, generating also higher conduction losses.

Note that this ratio, in addition to M_{N}, also depends on the utilization, $u = u_{\text{LV}}$, the LV output DC voltage, V_{out}, and the MV-side device blocking voltage, V_{B}; however, it does not depend on the rated power, P, nor on the voltage level, V_{ph}. **Fig. 6.3a** and **Fig. 6.3b** show the dependency of this ratio on M_{N}, and on δ, respectively, where also three different values for V_{B} are considered. In the scope of further analysis, additional effects such as the dependence of the permissible loss density in the semiconductors on the blocking voltage as well as costs per chip area should be included into the considerations.

Another performance index to compare the semiconductor effort is the required relative VA rating [203], which is given by

$$\frac{1}{P} \cdot \sum i_{\text{x,max,IFE}} v_{\text{x,max,IFE}} = \frac{4(2\pi M_{\text{N}} + \pi + 1)}{M_{\text{N}}}, \tag{6.23}$$

$$\frac{1}{P} \cdot \sum i_{\text{x,max,IBE}} v_{\text{x,max,IBE}} = \frac{8(\pi M_{\text{N}} + 1)}{M_{\text{N}}}, \tag{6.24}$$

where $i_{\text{x,max}}$ and $v_{\text{x,max}}$ denote the peak current and the maximum switching voltage of the individual devices. Note that for the analytic expression again $f_{\text{s}} = f_0$ has been assumed. The ratio between these performance indices then becomes

$$\frac{\frac{1}{P} \cdot \sum i_{\text{x,max,IFE}} u_{\text{x,max,IFE}}}{\frac{1}{P} \cdot \sum i_{\text{x,max,IBE}} u_{\text{x,max,IBE}}} = \frac{2M_{\text{N}}\pi + \pi + 1}{2(M_{\text{N}}\pi + 1)} \approx 1.3, \tag{6.25}$$

which means that the installed total switching power is about 30% higher in the IFE (for $M_{\text{N}} = 0.8$).

In addition to conduction losses, also switching losses arise in the IFE's boost stage and in the IBE's ARUs, which will be briefly addressed in the case study in Section 6.2. In contrast, the isolation stages operate with ZVS—although not over the entire grid period in the IFE case due to the varying voltage, which has been analyzed in Section 5.2.

Since each switch requires a separate gate drive unit (GDU), the total switch count is an interesting characteristic. From **Fig. 6.1** it follows that the

total number of switches becomes $n_{\text{switch,IFE}} = (4+4+2) \cdot N_{\text{IFE}}$ (assuming one boost stage per cell) and $n_{\text{switch,IBE}} = (4+2+4) \cdot N_{\text{IBE}}$, respectively. Thus, the IFE system requires only M_{N} (< 1) times the number of individual switches and GDUs compared to the IBE converter.

Summary of Theoretical Considerations

Tbl. 6.2 summarizes the key results of the generic comparative analysis of an IFE and an IBE SST system. The IFE system requires less series connected cells, approximately the same total transformer volume, but clearly a higher effort in terms of power semiconductors. However, this additional effort is on the LV side, and typically semiconductor prices scale with blocking voltage. Also the reduced number of individual switches and hence GDUs might alleviate the result of the chip area comparison to some extent.

In addition to the IFE system discussed above and shown in **Fig. 6.1a**, also the results for an IFE* system are shown in **Tbl. 6.2**. The converter cells of an IFE* system do not use bidirectional switches, but a dedicated active full-bridge rectifier on the AC side and a simple half-bridge on the SRC's MV side, i. e., their MV side structure is identical to that of an IBE cell—with two important differences: the capacitor is only a resonant capacitor, and the active rectifier is not used to shape the current but switches only at grid frequency to fold the grid voltage. Such an approach would slightly lower the semiconductor effort in terms of chip area requirement and relative VA rating, but on the other hand the complexity and the number of semiconductors, GDUs, etc. would increase.

Further Aspects

Other Magnetic Components In addition to the transformer, the IFE system requires boost inductors on the LV side and a smaller grid filter inductor on the MV side, whereas the IBE concept only requires a single boost/filter inductor on the MV side. Discussing the design trade-offs is beyond the scope of this generic comparative analysis; however, it should be mentioned that the IFE systems' boost stages could operate in TCM [205] or with higher current ripple, because the *a*IFE stage acts as a low-pass filter towards the grid if the (effective) boost stage switching frequency is chosen high enough, whereas on the other hand, the current stress seen by the IBE system's boost inductor is lower, and also the HF content of the current, since the input current quality must already comply with grid harmonic standards.

Tbl. 6.2: Summary of the comparative analysis for $M_N = 0.8$ and $f_s = f_0$, and for the aggregated A_{chip} (cf. (6.22)) also assuming $\delta = 2$, $u = 0.66$, $V_{out} = 400\,V$, and $V_B = 1700\,V$.

	IFE	IFE*	IBE
N	0.80	0.80	1.00
$N \cdot (A_c A_w)$	1.15	1.15	1.00
V_T	1.05	1.05	1.00
n_{switch}	0.80	0.96	1.00
Rel. *VA*-rating	1.30	1.17	1.00
A_{chip}	1.15	1.11	1.00

Capacitors The IFE system requires only small resonant capacitors on the MV side of the cells, reducing the physical size of the assemblies on floating potential, and one larger capacitor to buffer the single-phase power fluctuation on the LV side (which could be made smaller in case of a three-phase configuration).

In contrast, the IBE converter requires a certain share of the energy buffering to be performed on the MV side in order to provide a reasonably constant DC voltage for the ARU stage, which is the case even in a three-phase configuration. If a controllable isolation stage (e. g., a DAB) would be used in the IBE system, the energy buffering could be forced to take place on the MV side, where a comparatively high voltage ripple could be tolerated, while the isolation stage would transfer only DC power, reducing RMS currents and enabling a perfectly flat DC output voltage without significant capacitance on the LV side.

Common-Mode Currents and Isolation Stress In an IBE system, the entire MV-side assemblies of the cascaded cells change their potential with respect to earth at a dv/dt defined by the switching actions of the lower cells in the stack, which may give rise to very high common-mode currents to ground, possibly requiring appropriate countermeasures (cf. Section 4.2), and which would also increase the dv/dt stress seen by the isolation barrier [206].

The IFE system's cells, however, are essentially connected to each other by means of a capacitive voltage divider. The maximum dv/dt depends on the value of C_{r1} and the transformer currents; it is in any case orders of magnitudes lower than that of power semiconductor switching transitions. This

Tbl. 6.3: Specifications for the case study.

Grid voltage (line-to-line RMS), V_N	6.6 kV
Grid voltage (phase RMS), V_{ph}	3.81 kV
Rated Power, P_N	25 kW
Nominal modulation index, M_N	0.8
SRC switching frequency, f_s	50 kHz
SRC resonant frequency, f_0	≈ 52 kHz
ARU/Boost converter switching frequency, $f_{s,b}$	25 kHz
DC output voltage	400 V
N_{IFE}, n_{IFE}	5, 1.75:1
N_{IBE}, n_{IBE}	6, 1.40:1

is beneficial with respect to converter EMI emissions and isolation material stress.

6.2 Case Study: The S³T

In order to exemplify the above theoretical considerations, this section briefly considers a 25 kW, 6.6 kV AC (line-to-line) to 400 V DC all-SiC realization of an IFE-based SST that is developed in the scope of a research program funded by the Swiss government [32], and accordingly denominated as Swiss SST (S³T). **Tbl. 6.3** shows additional specifications considered for this case study, where Wolfspeed's upcoming 1700 V/45 mΩ (C2M0045170D) and 900 V/11.5 mΩ (X3M0010090X-ES) SiC MOSFETs are considered [199] (no paralleling, 125 °C junction temperature). ZVS switching losses are neglected, and hard switching losses of the ARU or the boost stages are modeled using datasheet values. It is assumed that the same transformers are used for all systems, and that the IBE transformers feature an efficiency of 99.5 % at rated power with a 1:1 distribution of core and winding losses.

Fig. 6.4 shows a comparison of calculated semiconductor and transformer losses of the three concepts discussed in the last section (IFE, IFE*, and IBE systems) as a function of the output power. The IBE system benefits from its lower RMS currents at high output power levels, which could be further improved at the cost of higher complexity by using a controllable DAB isolation stage, whereas the IFE system realizes lower part-load losses due to lower switching and transformer core losses. Note also that the realization effort of

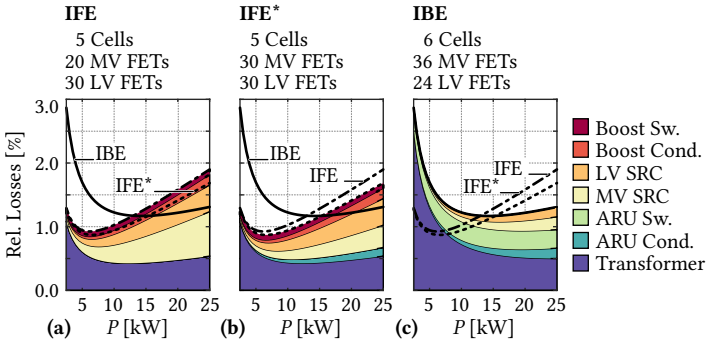


Fig. 6.4: Relative semiconductor and transformer losses for the three systems considered in the case study.

the IFE system is lower, because only 50 power semiconductors and GDUs are required compared to 60 in the IBE, and because the number of (identical) transformers is lower (5 instead of 6), too. In contrast, the IFE* system uses the same number of semiconductors as the IBE system, and the changed MV-side circuit structure helps to reduce conduction losses compared to the IFE. Note that additional losses of the boost and filter inductors, the capacitors, the control circuitry, etc. are not considered here but will be subject of further publications containing a more detailed, hardware-based comparison of the S³T-IFE SST and a corresponding IBE system realization.

6.3 Summary

This chapter provides a detailed derivation of the key component stresses of IFE-based MVAC-LVDC SSTs, which enables a very generic comparison of the IFE converter with the mostly used IBE concept. The IFE approach allows to minimize complexity on the MV side, since all control and measurement tasks can be performed by a secondary side non-isolated boost-type |AC|-DC stage (cf. also Section 5.3), whereas a resonant *a*IFE converter provides isolation by means of MFTs, thereby reducing size and weight compared to an LFT.

Because the boost stage is moved to the secondary side, the total MV-side blocking voltage, i. e., the number of cascaded cells, can be reduced. Also, the cells' MV-side assemblies do not change their potential at high dv/dt, reducing issues with common-mode ground currents. However, this comes at the cost of a higher effort in terms of required power semiconductor chip

area (factor 1.15) and higher RMS currents in the isolation stage, including the MFTs, when compared to an IBE system. On the other hand, results of a case study considering the 25 kW, 6.6 kV AC to 400 V DC all-SiC S³T show that the IFE approach generates lower switching and transformer core losses, resulting in lower total losses for part load operation.

Thus, following an SST development vector pointing towards maximum simplification instead of maximum performance (and therefore high complexity), the IFE concept might have advantages in applications where weight and volume constraints are the main driver to move from LF to MF isolation stages and where low complexity is desirable, and where part-load operation is dominant. Such an application could, e. g., be auxiliary supplies in traction applications, as, e. g., used for climate control units, lighting, etc. of individual coaches. The IFE approach would allow to interface these auxiliary supplies directly to an MV bus running along a train and thereby removing the need for additional LV buses.

7 Critical Evaluation of SST Applicability

So far, two SST topologies or concepts—IBE and IFE—have been discussed in **Chapter 4**, **Chapter 5**, and **Chapter 6**. These topologies differ in their suitability for certain applications, since the focus on the trade-offs between flexibility, efficiency, complexity is set differently.

Generally, SSTs have been proposed for different applications, e. g., for smart distribution grids (cf., e. g., [9–14, 16, 32, 33, 49, 207, 208]), for traction systems (cf., e. g., [19, 24, 26–31, 113]), and for MF potential separation as also considered for DC-DC applications such as collecting grids of offshore wind parks [129].

Therefore, this chapter discusses the applicability of SST technology in different applications and environments in a more generic way, with the aim of identifying applications where SSTs provide benefits over alternative solutions. Section 7.1 covers applications in a future smart grid, where also competing technologies are briefly covered, Section 7.2 discusses applications of SSTs in environments where weight and/or space constraints apply, such as in traction, Section 7.3 briefly mentions DC-DC applications, e. g., in future DC grids, and finally Section 7.4 provides an overall critical discussion of the SST applicability.

7.1 Grid Applications

The main task of a transformer in the distribution grid at the interface between MV and LV levels is to provide galvanic isolation and voltage scaling—tasks that can also be provided by an SST. However, as will be discussed in Sec-

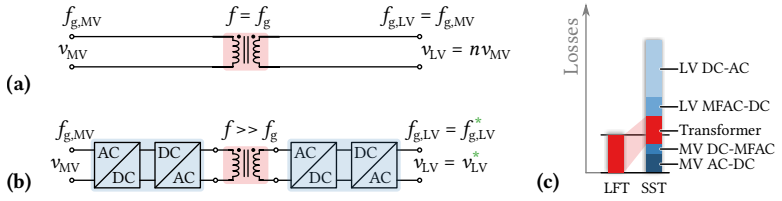


Fig. 7.1: "Efficiency challenge" faced when replacing an LFT **(a)** with an AC-AC SST **(b)**: the additional conversion stages create losses, whereas the efficiency gain of the transformer itself is only minor **(c)**. Note that for reasons of clarity only a single-phase system is shown; however, the considerations apply equally to a three-phase system.

tion 7.1.1, always with an efficiency disadvantage. Furthermore, an SST might not be directly compatible with existing grid infrastructure (cf. Section 7.1.2). On the other hand, SSTs can provide more functionality than conventional LFTs, e. g., voltage regulation. Therefore, Section 7.1.3 provides an overview on competing technologies that can be employed to add required controllability to (parts of) the distribution grid.

7.1.1 Galvanic Separation and Voltage Scaling

As has been discussed in Section 4.3 on the specific example of a 1 MVA SST interfacing a 10 kV MV grid to a 400 V LV grid, the SST is not competitive as a direct AC-AC replacement of an LFT in terms of efficiency and certainly also procurement costs. Slight benefits in terms of weight and volume are typically not highly important in distribution grid applications. The outcome of this specific comparison supports the general notion that an SST faces what could be called an "efficiency challenge" in distribution grid applications. Considering **Fig. 7.1**, an SST always adds two AC-AC conversion stages to the actual magnetic isolation transformer when compared to a conventional LFT—and, regardless of their specific realization (e. g., as matrix-type AC-AC stages, or as AC-DC-AC topologies with intermediate DC buses, etc.) these additional conversion stages generate losses.

However, the efficiency of grid-style LFTs is typically very high, i. e., in the range of 98.5 %...99.5 %. Even if it might be possible to slightly increase the efficiency of an MFT by a disproportional usage of active materials, which might be economically feasible due to the comparably small overall size, a significant increase of the MFT's efficiency above the LFT's efficiency cannot be expected (cf., e. g., [145, 209–211]). Therefore, there is simply no loss budget

to accommodate the losses created by the additional AC-AC conversion stages of an SST, as can be seen from the qualitative diagram in **Fig. 7.1c**.

If an LV DC interface is required, e. g., to connect a PV generation plant to the MV grid, the LV-side DC-AC conversion stage of the SST is not required, whereas on the other hand the LFT must be extended by a LV inverter/rectifier. As discussed on the specific example in Section 4.3, then the efficiency challenge can be alleviated. The main reason is that the comparably lossy LV side DC-AC conversion stage is basically shifted from the SST-based to the LFT-based solution. Note that this LV DC-AC stage contributes a large share of the total additional conversion losses, since it processes high currents (because of the low voltage) and needs to be hard-switched in order to control the grid current, e. g., in order to achieve PFC operation. On the other hand, the MV-side AC-DC conversion stage of the SST processes much lower currents, and, if a cascaded-cells converter is employed, very low switching frequencies can be used. The DC-DC stage of the SST can typically be operated using soft-switching techniques (cf. **Chapter 3**), which especially improves the efficiency of the LV-side HFAC-DC rectification/inversion stage (when compared to the grid-connected LV DC-AC stage, which is hard-switched).

All in all, loss-wise it is always challenging to not utilize an already available AC voltage to operate the isolation transformer, because the otherwise required additional power electronic conversion stages generate additional losses, whereas the efficiency of the transformer itself cannot be increased significantly by increasing the operating frequency (note, however, that this is different for applications where weight and volume constraints apply and where hence an LFT with smaller size and hence lower efficiency would need to be employed, as will be discussed in detail in Section 7.2). Therefore, a direct replacement of an LFT by an SST system in the distribution grid might not be feasible; especially considering also the compatibility issues discussed in the next section.

7.1.2 Compatibility with Existing Infrastructure

Typically, the protection of LV distribution grids is realized by means of fuses, whereby the *selectivity* of the protection scheme is an important criterion, which, in essence, means that only the protection device closest to a fault should trip, implying also that the distribution transformer at the interface between the MV and the LV grid must be able to deliver high short-circuit currents for some time. This is no problem for an LFT, because it can deliver up to 25 times its rated current for several seconds. However, obviously this

is not possible without a significant overrating of the power devices of an SST, because the thermal time constants of the power semiconductor chips are in the order of milliseconds only; furthermore, a correspondingly high saturation limit of the filter inductors would be required [102].

Therefore, advanced protection concepts would be required in an LV grid that is interfaced to MV by an SST. Such concepts typically involve communication between the SST and breakers and/or other switching devices in the grid [16, 212], where also the SST's capability of limiting its short-circuit current could be utilized—this again contributes to the notion that an SST cannot be seen as a direct replacement for an LFT in the distribution grid. In contrast, an SST basically requires a grid environment that is adapted to the specific characteristics of an SST, e. g., by providing communication among protection relays. Such adaptions are not easy to implement in existing distribution grids, though. Note that in contrast, e. g., in a traction application the LV side of the SST is in a self-contained environment, which can much more easily be tailored to suit the capability of the SST.

Furthermore, as is comprehensively discussed in [102], the protection of an SST in a grid environment, e. g., against overvoltages on the MV AC side caused by lightning strikes or switching actions, but also against short circuits in the MV or LV grid, is in general highly challenging, and might impose significant constraints on the design of an SST, e. g., by requiring minimum values for filter inductances or DC link capacitors.

7.1.3 Controllability and Competing Approaches

As has been discussed in the previous two sections, an SST is not well suited as direct replacement of an AC-AC LFT only. However, in addition to isolation and voltage scaling, an SST can provide advantageous functionalities, such as reactive power compensation, active filtering of harmonics, voltage regulation, etc., by utilizing the controllability of the additional conversion stages (cf. **Fig. 7.1**).

However, there are other approaches that can add certain functionality or controllability to the distribution grid, too, but which, in contrast to an SST, do not require that the entire power flow is processed by a stage with comparably low efficiency. Note that the aim is not to provide a fully detailed description of these alternative approaches, but to give an impression of what alternative technologies exist that can provide many of the features advertised for SSTs in grid applications.

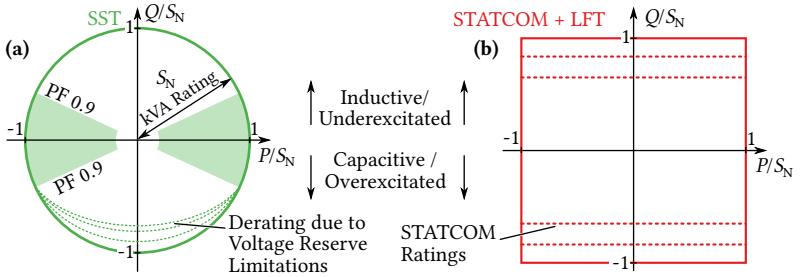


Fig. 7.2: Operating range in the PQ-plane for **(a)** an SST and **(b)** for a combination of an LFT and a dedicated STATCOM (the small voltage drop caused by the LFT's inner impedance is neglected).

Reactive Power Compensation

Reactive power compensation can be provided by static VAr compensation systems, which are essentially shunt inductor or capacitor banks that can be switched by mechanical or thyristor switches, or in order to provide a more granular control of the reactive current, the thyristors can be operated using firing delay-angle control [213]. Already in 1976, it has been proposed to use three-phase AC-DC inverters with a DC bus, but without an external energy supply (which is possible since reactive power compensation is essentially moving instantaneous power between the phases), to provide reactive power compensation [214]. Today, such devices are referred to as STATCOMs and are widely employed in the grid. Compared to the static VAr compensation systems mentioned above, STATCOMs feature much faster dynamics [213], i. e., a higher degree of controllability, which allows, e. g., to compensate voltage harmonics, flicker, etc.

Of course, also the power electronic stages of an SST can be operated such as to provide reactive power to the grid. If SST topologies with a DC bus are considered, a complete decoupling of the reactive power of the MV and the LV side can be achieved. However, on either side, the SST's output current, i. e., the apparent power is limited. Following requirements for generating plants connected to the MV grid [215], a typical dimensioning could be such that the maximum output current allows to provide operation at rated active power transfer with $\cos\varphi = \pm 0.9$. Therefore, the amount of reactive power that can be provided beyond the $\cos\varphi = \pm 0.9$ band is dependent on the amount of active power processed, as can be seen from **Fig. 7.2a**.

In contrast, a combination of an LFT and a dedicated STATCOM does

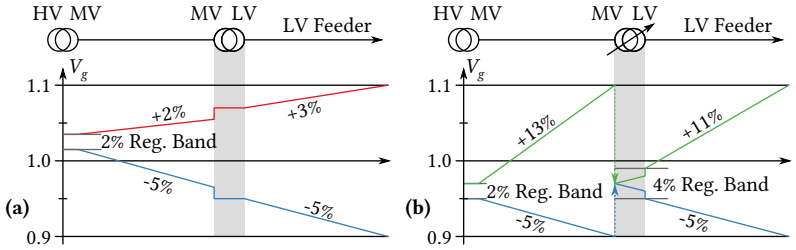


Fig. 7.3: (a) Voltage band usage in a conventional distribution grid and **(b)** improvement if a voltage regulation transformer is employed at the MV-LV interface. The example data is taken from [217].

not show this coupling of active and reactive power flows (cf. **Fig. 7.2b**). Furthermore, the STATCOM does not process the full power flow, but only the actually required reactive power, which allows for a correspondingly smaller dimensioning and/or lower overall losses.

Voltage Band Violations

The grid voltage in the MV and LV distribution grids must be within a tolerance band of ±10 % around the nominal value [216]. Since distribution grids have been designed for a power flow profile from sources on higher voltage levels to loads on lower voltage levels, typically the set point for the HV-MV transformers is chosen slightly above the nominal voltage, which allows to accommodate a 5 % voltage drop along the lines in the MV distribution grid, and another 5 % along the LV feeders (cf. **Fig. 7.3a**) [217].

However, with the increasing penetration of distributed generation on the LV levels, the power flow profile might invert in cases of, e. g., high infeed of solar power. Accordingly, the voltage profile along the distribution grid lines is inverted, too. As can be seen from the example in **Fig. 7.3a**, the upper limit of the voltage band is reached quickly, typically before the (thermal) capacity of the distribution grid to transmit the generated power is exhausted.

Voltage Regulation Distribution Transformers If the voltage transfer ratio at the MV-LV interface could be controlled, this situation could be significantly improved, as can be seen in **Fig. 7.3b**. An SST could provide this kind of voltage transfer ratio adjustment, because its LV output is controllable.

However, another option which is already available industrially (cf., e. g.,

[218]) and employed in the grid is based on (mechanical) automatic on-load tap-changers, which extend a conventional LFT to a "Voltage Regulation Distribution Transformer". Such on-load tap-changers can adjust the voltage transfer ratio of a transformer in about 10–20 steps, and, for an example based on vacuum-switching technology, achieve high lifetimes of several 100'000 switching operations [218].

Since essentially only the number of turns of one winding (typically on the MV side due to lower currents being switched) is changed, none of the favorable characteristics of an LFT (high efficiency, high robustness, etc.) is compromised, whereas, considering the typically comparably slow changes of the power flow-direction, the required controllability to avoid voltage band violations, i. e., to fully utilize the available transmission capacity of the infrastructure, can be provided.

Distribution Series Voltage Regulators Similarly, distribution voltage regulators feature an auto-transformer and a mechanical tap-changing system in order to inject a series voltage into a feeder line [219], allowing also to adjust the voltage. However, in contrast to a voltage regulation distribution transformer, these devices can be installed at any given point in the distribution grid, not only at the MV-LV interface, which facilitates retrofitting operations; furthermore, a single MV-side system can be used to control the MV voltage for several MV-LV transformers.

Active Series Voltage Regulators Targeting rather the protection of sensitive loads in the LV grid, active series voltage regulators feature a power electronics converter that can inject a series voltage by means of an injection transformer, whereby the converter is fed from the power line [220]. Such systems feature higher dynamics than solutions based on tap-changers and can hence provide fast correction of voltage sags. Furthermore, filtering of harmonics or reactive power compensation is possible, too. In contrast to an SST, the power electronic converter processes only a fraction of the total power, which, in essence, is a similar concept as the "Hybrid SSTs" discussed in the next subsection, however, with the possibility to place the unit, e. g., close to sensitive loads.

Hybrid SSTs

As discussed above, an SST is hardly competitive with an LFT in terms of cost, robustness, and efficiency. Nevertheless, additional controllability is often a

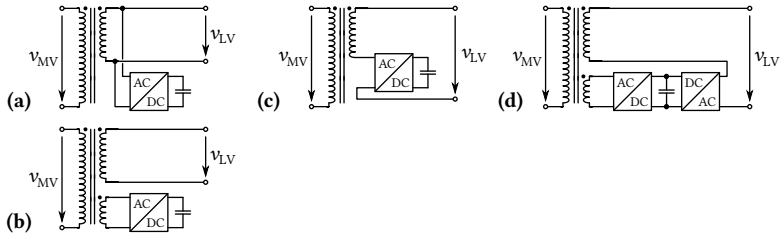


Fig. 7.4: Different realization options of hybrid SSTs as described in [221]. In all cases, the power electronic converters are only rated at a fraction of the total power.

feature that is required already in today's distribution grids. However, as can be seen from the successful deployment of voltage regulation distribution transformers, etc., it is often sufficient to provide *some* controllability, not *full* controllability of voltages and currents that could be achieved with an SST.

Therefore, a combination of a highly efficient and robust LFT with a power electronic converter that can provide the required amount of controllability, however, without processing the bulk power, could be an attractive solution [221, 222]. **Fig. 7.4** shows the four main configurations of such hybrid SSTs, where basically a shunt connection (**a**) and (**b**) or a series connection (**c**) of the power electronics to the LV-side winding can be distinguished.

Configuration (**d**) is basically a back-to-back connection of a shunt and a series converter, which allows for the highest flexibility, since the DC bus of the series stage can exchange active power with the grid by means of the shunt stage [222]. Therefore, arbitrary (within the converter ratings) voltages can be injected in series to the LFT's LV winding voltage in order to provide harmonic filtering, power factor correction, flicker control, etc. However, the power electronic converters are processing only a comparably small fraction of the total power, which does not degrade the overall efficiency compared to the LFT as significantly as if the LFT would be replaced by an SST.

Summary

An in-depth discussion of the alternative concepts introduced in this section would be beyond the scope of this thesis. However, the examples discussed indicate that there are alternative ways of addressing the challenges in modern distribution grids than to replace LFTs with SSTs. In contrast to an SST, these alternative solutions do provide a more narrow, however often sufficient, control range, but, on the other hand, either avoid the use of power electronics

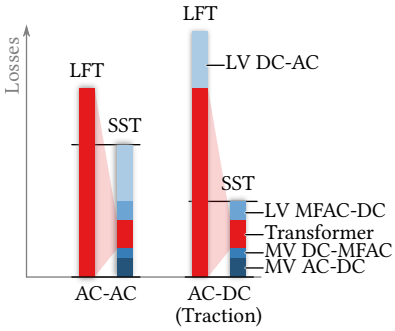


Fig. 7.5: "Efficiency challenge" in a weight/volume restricted environment: The achievable efficiency gain in the transformer itself justifies the additional conversion stages for both, AC-AC and AC-DC (e. g., traction) applications.

altogether, thereby retaining the high efficiency and robustness of an LFT, or limit the power processed by added power electronic stages to only a fraction of the total power, which allows to suitably balance the controllability requirement and the degradation of the overall efficiency.

7.2 Volume/Weight-Constrained Applications

Traction applications are the most prominent example of applications where weight and space for the isolation stage are constrained, as has been discussed in **Chapter 1**. This has led to several companies pursuing the development of SSTs for traction applications [19, 24, 28–31], resulting in various prototypes and even a shunting locomotive equipped with a fully functional SST, which has been field tested on the Swiss railways [19].

Considering that the efficiency of an LF traction transformer is comparably low (around 90 % [20–22]) as a result of increased current density in the windings to meet space and weight requirements, the loss budget that is available for the additional conversion stages of an SST is much higher than in grid applications. This is illustrated by **Fig. 7.5**, where a clear efficiency benefit of the SST-based solution can be identified. This corresponds to the findings from [19], where a 2 %...4 % efficiency improvement and a simultaneous significant weight reduction has been reported for the shunting locomotive SST prototype mentioned above.

Other applications where weight and space for an isolation stage might be

limited comprise the nacelles of wind turbines [49, 129], or even flying wind turbines [223, 224], future navy warships [225] as well as future civilian ships such as cruise liners [67, 68], where local MV AC and/or MV DC grids will be employed for on-board power distribution. Also, future subsea applications such as oil drilling infrastructures may benefit from an MV AC or MV DC connection to the surface or to the shore, and correspondingly could rely on low-weight subsea SST systems [70]. Furthermore, MV DC power distribution is even envisioned for future all-electric aircraft employing distributed propulsion concepts [71], where, e. g, IFE-based SSTs with low complexity could be utilized to supply LV loads such as avionics from a main MV DC bus. Note that many of these applications are pure DC applications, where, as will be discussed in the next section, an SST is the only possibility to provide galvanic separation and high voltage transfer ratios.

Finally, even in grid applications, specifically in underground distribution networks in areas with high population densities, e. g., city centers, where space is scarce and expensive, SSTs (e. g., of the AC-AC matrix-type, cf. Section 1.3) could find application in order to increase the power rating that can be installed in a given space [49].

7.3 DC-DC Applications

As already mentioned in the previous section, there are many emerging applications that could be based on (MV) DC distribution, e. g., ships [67, 68, 225] or subsea applications [70], industrial applications in general [226], or DC microgrids [227]. Another prominent example are collecting grids for offshore wind parks, where a DC collecting grid has significant benefits over an AC solution, e. g., because of the significant capacitive loading represented by long HV cables [228–230].

As a recent example, [129] describes the concept of a DC collecting grid for an offshore wind park, where essentially a HC-DCM SRC (cf. **Chapter 3**) with a high turns ratio of the MFT is used to interface the 2 kV DC bus of the wind turbine's inverter to a 50 kV local DC collecting grid, and where an M2LC-based DC-DC SST system with MF isolation is considered to step-up the voltage further to 320 kV for the HVDC transmission to the shore.

Thus, if galvanic isolation or significant step-up or step-down of the voltage is required in such DC distribution networks, a transformer must be used—however, a transformer requires an AC voltage to operate. Therefore, DC-AC and AC-DC conversion stages are required, and the selection of the transformer operating frequency is a free parameter that is subject to

optimization. In contrast to AC-AC or AC-DC applications, there is no AC voltage that could directly be used to operate the transformer, and hence the additional conversion stages are required in any case—there is no alternative to using a conversion system that can be seen as an SST.

7.4 Discussion and Future Applications

This chapter has summarized important aspects of the applicability of SST technology in various scenarios. AC-AC applications in the distribution grid seem difficult because of the "efficiency challenge": Even if an MFT could be built with a slightly higher efficiency than an LFT, the losses of the additional conversion stages result in a lower overall efficiency of the AC-AC SST system compared to an LFT. In addition, compatibility with existing grid infrastructure might be an issue: E. g., an SST cannot deliver several times its rated current in order to trip fuses. Possibly required (basic) controllability could be provided to the distribution grid also by other means such as, e. g., LFTs equipped with highly efficient automatic on-load tap changers, or active series voltage regulators, where only a fraction of the total power needs to be processed by the power electronics. Also, hybrid SSTs, i. e., combinations of an LFT and a power electronic converter rated only at a fraction of the power to provide certain regulation functionalities (e. g., reactive power compensation or active filtering of harmonics, etc.) are an interesting approach.

On the other hand, there is no alternative to an SST if galvanic separation is required in future DC grids, e. g., in DC collecting grids for wind parks. In such isolated DC-DC conversion systems, the operating frequency of the isolation transformer can be selected arbitrarily without increasing the number of power processing stages, which is in contrast to the previously discussed AC-AC (or, similarly, also AC-DC) application, where a direct connection, i. e., without intermediate conversion stages, of a mains frequency, i. e., LF, transformer to the available AC voltages generally provides higher efficiency.

If, on the other hand, as in traction applications or also in future naval, subsea or aerospace applications, space and weight constraints do apply, an SST might be the only solution to simultaneously achieve high volumetric and gravimetric power densities and high efficiency for MV-connected isolated AC-AC or AC-DC power conversion systems.

8
Conclusion

Raised awareness for environmental acceptability and sustainable usage of limited resources directly drives developments in all fields related to the generation, transmission, and usage of (electrical) energy. Accordingly, many political agendas contain targets to, e. g., increase the share of energy generated from renewable sources and to boost energy efficiency. Electricity is a very important energy carrier, since it can be distributed easily and employed in a wide range of applications, ranging from heating and industrial production to transportation. Furthermore, electricity can be generated on a large scale from renewable sources such as hydro, (offshore) wind or solar power. However, especially solar power is subject to strong fluctuations caused by the weather, the time of day, shading, etc. Additionally, in Europe solar power is mostly harvested by means of comparatively small PV installations, e. g., on residential or office buildings. Such distributed generation plants are thus often connected to the LV distribution grid.

However, the distribution grid traditionally is designed for a power flow from central generating stations over several decreasing voltage levels to customers connected at low voltage levels. It is not designed to cope with a high share of power infeed on low voltage levels, which might cause a reversal of the power flow when compared to the design case, and hence cause problems such as, e. g., violations of the allowable voltage band around the nominal grid voltage. This is only one example that is used to illustrate the type of challenges the distribution grid faces today, which furthermore include, e. g., an increasing importance of power quality due to sensitive loads, or the conflict between the requirement to increase transmission capacities and the difficulty to actually build new power lines.

Power electronic systems can be employed to address such challenges. For example, DC transmission or local DC distribution systems can increase

the utilization of (possibly existing) copper wires, or STATCOM devices can compensate reactive power locally to relieve the (AC) distribution system and to control grid voltages.

A solid-state transformer (SST) is a special kind of such a power electronic converter system, which not only complements an existing distribution grid with additional functionality, but aims at replacing existing LFTs at the interface between an MV and an LV grid. An SST also provides galvanic isolation and voltage scaling by means of an MFT, however, the additionally present power electronic conversion stages can be used to provide added functionality. Therefore, SSTs are envisioned to, e. g., act as energy routers and control the power flows in a future smart grid, provide an LV DC bus to interface distributed generation systems with an inherent DC output such as PV, etc., or as interfaces between local (DC) microgrids and the mains.

Whereas the available control possibilities are the main motivation to consider SSTs for smart grid applications, the MF isolation stage has another benefit: reduced volume and weight when compared to a conventional LFT. This renders SSTs also highly interesting for applications in environments where the weight and the volume that are available for an MV-LV transformation and isolation stage are limited, which is often the case in transportation applications such as traction.

In accordance with the initially mentioned goals to improve the energy efficiency also in transportation applications, SSTs can contribute twofold: first, lighter power conversion equipment can be mounted on a train's roof, which increases the available space for passengers and/or goods. Second, direct efficiency improvements are possible when compared to an LFT, since the latter needs to be built with high current densities and hence comparably high losses if a small construction volume must be achieved. Other future transportation applications that are being or will be electrified to an ever higher degree comprise civilian or navy ships, subsea applications (oil and gas drilling), or even future all-electric aircraft.

Thus, SST technology has received high interest from both, industry and academia, during the past two decades. In the following, the aspects that this thesis contributes to the corresponding body of knowledge are briefly summarized.

8.1 Results and Conclusions

The thesis starts with a discussion of how the five main modern SST topologies can be derived by combining three key concepts that have emerged 30 to

50 years ago: Matrix-type AC-AC topologies are well suited for pure AC-AC applications in weight and volume constrained environments, because in contrast to the other topologies they do not require bulky DC capacitors. Isolated Back End (IBE) topologies have been widely analyzed and are a suitable choice for AC-DC (or mixed AC-DC and AC-AC) applications, such as, e. g., in traction. Isolated Front End (IFE) topologies offer reduced complexity but also reduced flexibility, and hence could find use in niche applications, e. g., as simple MVAC-LVDC power supplies in weight and volume restricted environments. Topologies based on the modular multilevel converter (M2LC) could benefit from the single, fully rated transformer, which may facilitate the challenging isolation system design, and should therefore be investigated further. Finally, single-cell topologies employing HV SiC devices feature very low system complexity, but might suffer from reliability challenges because of the difficulty of implementing redundancy in a non-modular system.

Regarding the cascaded MV-side AC-DC conversion stage found in, e. g., IBE SSTs, either few cascaded cells based on HV power semiconductors or many cascaded cells employing LV power semiconductors can be used in order to interface to the 10 kV grid. A comprehensive analysis of this trade-off, first based on generic, analytic calculations, and in a second step employing a full efficiency versus power density $\eta\rho$-Pareto optimization, is therefore carried out, which is facilitated by the introduction of an empirical model of the dependency of power semiconductors' (Si IGBTs and diodes) loss-relevant parameters on the rated blocking voltage and current. It is found that designs based on 1200 V or 1700 V devices (corresponding to 15 or 11 cascaded full-bridge cells per phase stack, respectively) achieve the most suitable trade-off between power density and efficiency for a 1 MVA system connected to the 10 kV grid. Efficiencies above 99 % are possible at a power density of roughly $5\,\mathrm{kW/dm^3}$.

Such multi-cell designs that employ a comparably high number of cascaded converter cells, and hence show a high overall component count, may raise reliability concerns. However, thanks to their modularity, multi-cell systems lend themselves to adding redundant converter cells. Therefore, the reliability of multi-cell systems is analyzed, taking into account the highly beneficial effect of redundant cells. It is shown that if similar costs of the redundancy are allowed, the resulting reliability of systems with many converter cells is comparable to that of systems using only few converter cells (and hence power semiconductors with high blocking voltages). However, it has to be kept in mind that there are so-called "reliability bottlenecks", e. g., the control system, which may limit the reliability improvement that can be

achieved by adding redundant converter cells.

Before then more detailed considerations regarding first an IBE and in the second part regarding an IFE SST system are made, a comprehensive analysis of the SRC operated in HC-DCM is given. The HC-DCM SRC provides a fixed transfer ratio between its input and output voltage, which depends only slightly on the load. This renders the converter highly attractive for applications in multi-cell SSTs, where it serves as, e. g., the isolation stage between the individual cells' DC buses on floating potential and a common LV DC bus. However, the voltage transfer ratio shows certain dynamics. Therefore, a high-level model for these dynamics, which is based on a passive equivalent circuit, is re-derived on a generic basis and then experimentally verified for the special case of DC link capacitors that are comparatively small when compared to the series resonant capacitor. Finally, the model allows to optimize the choice of the cells' DC capacitance values in phase-modular IBE SST applications (where each cell processes a power that fluctuates with twice the mains frequency) such that a small volume and low losses can be achieved. This is exemplified on the *MEGAlink* IBE SST system, which is a multi-cell SST with a distribution grid-scale power rating of 1 MVA, acting as an interface between a 10 kV AC MV grid, a 800 V LV DC bus and/or the 400 V AC grid.

Considering an IGBT-based design of a 52.5 kW HC-DCM SRC DC-DC isolation stage connecting a 2.2 kV DC bus to a 800 V DC bus, a model for the behavior of the stored charge in the IGBT devices is experimentally verified for the characteristic current waveforms in the HC-DCM SRC, and this information is then used to approximate switching losses under the ZCS/ZVS conditions found in the converter. This facilitates an efficiency versus power density $\eta\rho$-Pareto optimization, which reveals that efficiencies in excess of 99 % are achievable, and that comparatively low switching frequencies in the range of 7 kHz…9 kHz result in the most suitable trade-off between power density and efficiency.

The MV-side assemblies (heat sinks, DC capacitors, etc.) of the cascaded AC-DC converter cells of a multi-cell IBE SST topology change their potential with respect to ground every time one of the cells accommodated at a lower position in the phase stack switches. Since the dv/dt values of power semiconductor switching transitions are quite high, considerable common-mode currents are generated in order to charge the parasitic capacitances between the cells' MV-side assemblies and surrounding grounded structures. By means of an analytic description of these common-mode currents, including potential resonances with parasitic inductances in the current path, it is shown that

placing common-mode chokes at the AC terminals of each cell is a feasible possibility to mitigate the common-mode currents while contributing only negligibly to the overall SST volume and losses.

The common-mode issue is not present in the other class of SST topologies that is investigated in this thesis. These are based on the IFE approach, which is analyzed considering isolated single-phase AC-DC PFC applications such as MVAC-LVDC auxiliary power supplies in traction applications, or interfacing a larger PV generating plant directly to the MV grid. So far, the IFE approach has not yet received much attention in literature. In an IFE system, the four distinct tasks that are required to perform isolated PFC functionality (folding of the grid voltage, isolation and voltage scaling, grid current control, and output voltage control) are arranged in an inverted sequence when compared to the IBE approach: first, an integrated folding and isolation stage, which is typically realized as an ISOP configuration of HC-DCM SRC converter cells operating as AC-|AC| converters, is connected directly to the MV AC grid. The grid current shaping and the output voltage control is performed by a non-isolated |AC|-DC boost converter stage that is located on the LV side of the isolation barrier. Therefore, IFE systems show reduced complexity, especially on the MV side. Considering the all-SiC S^3T, a 25 kW interface between a 6.6 kV MV grid and a 400 V DC bus, the topology and the operating principle of an IFE SST system which is slightly simplified when compared to the few other published variants is derived and described in detail.

The operating conditions for the HC-DCM SRC are different in an IFE system than in an IBE system, where the converter acts as a DC-DC converter, and where the transformer magnetizing current can be utilized in order to realize load-independent ZVS. In an IFE system, however, the input and output voltages are essentially folded AC voltages, i. e., |AC| voltages. Hence, the ZVS behavior changes during the grid period, because the magnetizing current available for ZVS, the required voltage swing, and also the nonlinear parasitic capacitances of the SiC MOSFETs change with the grid voltage. A comprehensive analysis of these conditions is given, including the effects of component tolerances of the resonant tank elements, and it is discussed how to choose the magnetizing inductance and the interlock time of the bridge legs such as to achieve lowest losses and/or a wide ZVS range. If ZVS over the entire grid period is required, e. g., in order to avoid EMI emissions generated by (partially) hard-switched transitions, a high magnetizing current and/or a long interlock time are required, both increasing losses. Therefore, a variation of the interlock time over the grid period is proposed, which allows to achieve low losses and (almost) full-range ZVS, although with a

slightly higher complexity. Using a detailed simulation model of the S³T that includes nonlinear MOSFET capacitances as well as component tolerances, the approach is verified. Thus, considering well-known approaches to achieve full-range ZVS also for the non-isolated secondary-side AC-DC boost converter stages, and the aforementioned avoidance of common-mode ground currents found in multi-cell IBE systems, an IFE-based SST can be realized such as to generate only low HF EMI disturbances, which might be beneficial in certain environments.

Furthermore, it is also briefly discussed how the S³T control system can be realized, and how the grid current as well as the output voltage can be controlled without requiring any MV-side measurement circuitry. Although reactive power operation on the MV side is possible (however, with degraded harmonic quality of the output current), an IFE SST is mostly suited for bidirectional operation with a power factor close to unity. IFE SSTs are thus suitable for applications where a (bidirectional) isolated MVAC-LVDC interface is required, and where weight and volume are limited, but where no added features such as reactive power compensation are needed, as, e. g., in case of auxiliary power supplies operating directly from an MV grid.

Eventually, analytic expressions of the main component stresses in IFE and IBE SSTs are derived, which facilitate a generic comparative analysis of multi-cell IBE and IFE SST systems. It is found that the IFE approach requires less cascaded converter cells (for the same grid voltage), and, as mentioned above, that these cascaded cells do not change their potential with respect to ground with high dv/dt values, which avoids the aforementioned common-mode ground current issues of IBE systems. On the other hand, higher RMS currents in the isolation stage of the IFE topology necessitate an increase of the total semiconductor chip area by roughly 15 %, however, fewer individual switches (and hence fewer gate drive units) can be used. The overall effort regarding the MFTs themselves is comparable. This generic analysis is complemented by a case study considering the aforementioned ratings of the S³T. The results indicate that the IFE generates lower total switching losses and lower transformer core losses, which results in the IFE showing a higher part-load efficiency than the IBE, however, the full-load efficiency is lower because of the higher RMS currents.

Finally, the applicability of SST technology in three different application areas is evaluated. A quantitative study comparing a 1 MVA, 10 kV to 400 V AC-AC SST with an equally rated LF distribution transformer, considering the four performance indices, i. e., losses, volume, weight, and cost, reveals that the SST solution is not competitive in such an application because of

higher losses and significantly higher costs. This is less pronounced in AC-DC applications, however, even there the main advantages of the SST-based solution, i. e., reduced volume and weight, are typically not very important in stationary grid applications. On a more generic level, also the "efficiency challenge" describes this situation. If there is already an AC voltage available that could be used to operate the isolation transformer, any solution that adds an additional conversion stage in order to operate the transformer at another frequency causes additional losses in this converter stage. In an environment without weight and volume constraints, however, the efficiency of an MFT cannot be expected to be significantly higher than that of an LFT, even if the overall smaller volume may allow for a lower utilization of the active materials (i. e., lower current densities and/or lower flux density amplitudes) from an economical point of view. Therefore, the overall system losses are increasing.

Furthermore, significant challenges regarding the protection and the robustness of comparably sensitive, complex SST systems in a harsh grid environment do exist. Limited overload/overcurrent capability compromises the compatibility with existing grid protection concepts that rely on high fault currents, e. g., in order to trip fuses or trigger fault relays.

However, in a grid application an SST is more than just a replacement for an LFT because it provides additional control functionality, i. e., an SST might provide the functionality of, e. g., an LFT plus a STATCOM system. Therefore, important challenges that the distribution grid is facing are summarized, and state-of-the-art solutions other than SSTs are discussed. It is shown that there are numerous alternative solutions, which may not have a control range as flexible as that of an SST, but still can provide *sufficient* control capability to the distribution grid. These solutions, however, do either not rely on power electronics at all (e. g., automatic on-load tap-changers), which implies low losses and high robustness, or they are based on power electronics, but do not process the full power flow with these less efficient stages (e. g., active series voltage regulators or hybrid SSTs). Therefore, and because of significant challenges regarding the protection and the robustness of comparably sensitive SST systems, the feasibility of employing SSTs in distribution grids remains at least questionable; the most promising area being applications as interfaces between an MV AC mains and an LV DC microgrid, i. e., as AC-DC conversion systems.

On the other hand, SSTs show clear benefits in applications where the weight and/or space that is available for an isolation stage between an MV and an LV level is limited, because significantly higher power densities can

be realized than with conventional LFTs. Examples for such applications in weight and/or volume-limited environments include traction vehicles, ships, nacelles of wind turbines, and future aerospace applications. Note that in contrast to applications in the distribution grid, where the immense amount of existing infrastructure cannot easily be adapted to the specific requirements of SSTs, e. g., regarding protection concepts, here the operating environment of the SST (at least on one side) can more easily be designed accordingly (consider, e. g., the stand-alone environment on a ship). Furthermore, since an LFT with reduced size and weight inevitably shows comparably high losses due to the required high utilization of its active materials, e. g., high winding current densities, the aforementioned efficiency challenge does not exist for weight and/or volume-constrained environments. In contrast, SST-based solutions may even allow for improved power density *and* efficiency.

Similarly, in DC-DC applications, e. g., in future MV DC collecting grids for large PV or wind generating stations, SST technology in the wider sense is applicable. There, conversion stages from DC to AC and back from AC to DC are required in order to provide galvanic separation and/or high voltage transfer ratios by means of a magnetic transformer. In contrast to AC-AC or AC-DC applications, there is no alternative solution that does not require such conversion stages, which would allow to avoid the corresponding conversion losses.

8.2 Outlook and Future Research Challenges

The evolution of SST topologies that are suitable for specific applications and which offer desirable characteristics such as high efficiency and high power density, high reliability and robustness, fault tolerance, modularity, etc. is a highly interesting and ongoing process. In any case, however, significant research challenges remain.

It can be expected that SSTs may find their first real industrial use in applications where volume and/or weight restrictions apply, and/or where MVDC-LVDC conversion is required. Such applications include future civilian or navy ships with on-board MV AC and/or MV DC grids, traction applications, collecting grids for offshore wind parks, and aerospace applications such as future all-electric aircraft. Applications of SSTs in the distribution grid as AC-AC interfaces, i. e., direct replacements of conventional LFTs, are rather unlikely. However, in the context of DC microgrids and/or for the interfacing of renewable energy sources to the distribution grid, i. e., providing MVAC-LVDC conversion, there might be potential applications. In any

case, more detailed evaluations of system-level benefits need to be carried out in order to fully clarify system-wide impacts and possible benefits of SSTs employed in the distribution grid, whereby it is important to not neglect alternative concepts. Also, research regarding hybrid SSTs seems promising and important in this context.

In addition to the high reliability requirements common to all potential application areas, other major challenges in the further development of SST technology are the protection of comparably sensitive power electronic systems against mains overvoltages, e. g., lightning strikes, and short-circuit currents that are to be expected in harsh traction and grid environments, and the design of the MFTs, where the trade-off between high isolation requirements and the thermal management needs to be mastered. Furthermore, the impact of the mixed-frequency electrical field stress on insulation materials needs to be understood better.

With the availability of HV SiC power semiconductors, single-cell SST solutions become possible. However, it needs to be clarified whether such a single-cell approach or rather a multi-cell approach is a more suitable solution, or, if the best of both worlds can be achieved using a "fewer cells" approach, i. e., stick to multi-cell topologies and benefit from inherent features such as modularity and the accordingly simple implementation of redundancy concepts, however, employing cells with higher DC voltages and thus utilizing power semiconductors with higher blocking voltages, e. g., 3.3 kV, which would reduce the system complexity.

All in all, SST technologies are still facing a high number of smaller and larger design and research challenges—not only such of technical nature, but also related to economical, political and other aspects—which need to be addressed by future research projects. Also, the fast development of emerging concepts such as the all-electric aircraft or the increased deployment of local MV DC grids, e. g., on future ships or in subsea applications, likely will generate further opportunities for SSTs to reveal their potential.

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