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Comparative Evaluation of Three-Phase Si and SiC AC-AC Converter Systems

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presented by
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Abstract

In academia, for more than thirty years, Matrix Converters have been considered as one of the future converter concepts for variable speed drives for industry and more recently also for More Electric Aircraft or renewable energy applications. However, despite intensive research for the last decades, Matrix Converters have until now only achieved low market penetration. In industry, the most widely used bidirectional, low-voltage ac-ac converter topology is the two-level Voltage Source Back-to-Back Converter.

The main objective of this PhD thesis is to derive and investigate the key criteria required for a systematic comparative evaluation of ac-ac converter systems. Based on a suggested set of criteria, a comprehensive comparison of the Voltage Source Back-to-Back Converter, the Current Source Back-to-Back Converter, the Indirect Matrix Converter, and the Conventional (direct) Matrix Converter is performed for a 15 kW permanent magnet synchronous motor drive.

The comparison involves the investigation of the required silicon chip area for a defined maximum admissible thermal loading of the power semiconductors, the passive components including the EMI input filter, the total losses and achievable efficiency, and a prediction of the resulting converter volume. A particular focus is on the experimental investigation and performance analysis of normally-on SiC JFET prototype devices, which are close to commercialization.

With this comparative evaluation, a systematic procedure is presented that ultimately enables to identify advantageous application areas of the considered converter topologies.

Kurzfassung

Seit nunmehr dreissig Jahren wird der Matrixumrichter in der akademischen Gemeinschaft intensiv erforscht und als eine vielversprechende Schaltungstopologie für zukünftige effiziente und kompakte Antriebssysteme für Industrie- und Luftfahrtanwendungen diskutiert. Trotz intensiver Forschung konnte sich der Matrixumrichter in kommerziellen Antriebssystemen bisher jedoch nicht etablieren. Der industriell am weitesten verbreitete bidirektionale dreiphasige Umrichter für Niederspannungsantriebe ist der Zweipunkt-Spannungszwischenkreisumrichter.

Das Hauptziel dieser Dissertation liegt im Eruieren und Herleiten verschiedener Schlüsselkriterien und Vergleichsmethoden und dem anschliessenden Durchführen einer systematischen und ganzheitlichen Bewertung verschiedener dreiphasiger Umrichtersysteme. Basierend auf den gefundenen Bewertungskriterien wird ein umfassender Vergleich zwischen dem Spannungs- und Stromzwischenkreisumrichter, dem Indirekten Matrixumrichter und dem Direkten Matrixumrichter zur Speisung eines 15 kW Antriebs mit einer Permanentmagnet-Sychnronmaschine präsentiert. Der Vergleich umfasst die Bestimmung der benötigten Chipfläche der Leistungshalbleiter für einen gegebenen Arbeitspunkt, die Prädiktion der leitungsgebundenen elektromagnetischen Störaussendung, die Modellierung der passiven Komponenten einschliesslich des EMV Eingangsfilters, die Berechnung des erreichbaren Gesamtwirkungsgrads und die Vorhersage des resultierenden Umrichtervolumens. Ein besonderes Augenmerk wird dabei auf die Untersuchung von selbstleitenden SiC JFET-Prototypenhalbleitern gelegt, welche kurz vor der Markteinführung stehen und einer vergleichenden Bewertung mit Si IGBTs neuster Generation. Verschiedene Hardwareprototypen wurden implementiert, um das Betriebsverhalten der betrachteten Umrichter experimentell zu untersuchen und die Modelle zu parametrieren und

zu verifizieren. Mit dieser Vergleichsstudie wird ein systematisches Verfahren aufgezeigt, welches ermöglicht, die Anwendungsfelder der untersuchten Umrichterkonzepte zu bestimmen und analytisch zu beschreiben. Damit wird implizit die Basis für eine technisch-kommerzielle Bewertung verschiedener Schaltungstopologien und Komponententechnologien für Umrichtersysteme gelegt.

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Finally, but most importantly I would like to express my heartiest thanks to my family for providing me with a stable, loving, and stimulating upbringing, and for supporting me in many different ways throughout my life, my studies, and my PhD.

Publications

Affirmation

The results presented in this thesis were generated during my PhD research from January 2006 to December 2009 at PES Laboratory, D-ITET, ETH Zurich. Parts of this work have already been published or are being published in the journals, conference proceedings, or articles listed below.

Additional papers, out of the scope of this thesis, were published in the topic area of *Teaching Experimental Power Electronics*.

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3. J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM Converter Power Density Barriers," in *Proc. 4th IEEE/IEEJ Power Conversion Conference PCC '07*, Apr. 2–5, 2007, pp. 9–29.

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List of Symbols

Acronyms

3L-NPC	Three-Level Neutral Point Clamped
AC	Alternating Current
Al_2O_3	Aluminum Oxide (DBC substrate)
AlN	Aluminum Nitride (DBC substrate)
AlSiC	Aluminum Silicon Carbide (DBC substrate)
B6-VSI	B6 (three-phase) diode bridge rectifier with Voltage Source Inverter
B6-ZSI	B6 (three-phase) diode bridge rectifier with Z-Source Inverter
BFOM	Baliga Figure-of-Merit
BJT	Bipolar Junction Transistor
CAL	Controlled Axial Lifetime
CE	Conducted Emission
CISPR	International Special Committee on Radio Interference (original french abbreviation)
CM	Common Mode
CMC	Conventional or Direct Matrix Converter
CMOSVM	Common-Mode-Optimal clamping Space Vector Modulation (reference modulation for CMC)
CoolMOS	Trade mark of Infineon's charge compensated silicon MOSFET technology
CSBBC *or* CLBBC	Current Source Back-to-Back Converter *or* Current DC-Link Back-to-Back Converter
CSI	Current Source Inverter

CSR	Current Source Rectifier
CSPI	Cooling System Performance Index
CSVM	Conventional Space Vector Modulation (IMC)
DBC	Direct Bonded Copper
DC	Direct Current
DM	Differential Mode
DSP	Digital Signal Processor
DTC	Direct Torque Control
ECPE	European Center for Power Electronics
EMC	Electromagnetic Compatibility
EmCon	Emitter Controlled
EMI	Electromagnetic Interference
F3EC	Fundamental Frequency Front-End Converter
FCE	Field Charge Extraction
FOC	Field-Oriented Control
FOM	Figure-of-Merit
FPGA	Field Programmable Gate Array
FPQ	Failure Prediction Quadruple
FS	Field-Stop
GaN	Gallium Nitride
GND	Ground
GTO	Gate Turn-off Thyristor
HCMC	Hybrid Conventional Matrix Converter
HEV	Hybrid Electric Vehicle
HF	High Frequency
HIMC	Hybrid Indirect Matrix Converter
HVSVM	High Voltage Space Vector Modulation (IMC)
HVZCS	High Voltage Zero Current Switching (reference modulation for IMC)
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IGBT	Insulated Gate Bipolar Transistor
IGCT	Insulated Gate Commutated Thyristor
IM	Induction Motor
IMC	Indirect Matrix Converter, also known as Two-Stage (rarely 18-Switch) Matrix Converter
ISM	Industrial, Scientific, and Medical (for EMC)
ISVM	Improved Space Vector Modulation (IMC)
JBS	Junction Barrier Schottky (diode)
JFET	Junction Field Effect Transistor

KFOM	Kolar Figure-of-Merit
LF	Low Frequency
LISN	Line Impedance Stabilizing Network
LVSVM	Low Voltage Space Vector Modulation
MBS	Monolytic Bidirectional Switch
MC	Matrix Converter
MEA	More Electric Aircraft
MOSFET	Metal Oxide Field Effect Transistor
MPS	Merged PiN Schottky (diode)
MTTF	Mean Time To Failure
NPT	Non-Punch-Through
NZSVM	Non-Zero Space Vector Modulation (CMC)
OP	Operating Point
PC	Personal Computer
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PE	Protective Earth
PFC	Power Factor Correction
PLC	Programmable Logic Controller
PLD	Programmable Logic Device
PLL	Phase Locked Loop
PMSM	Permanent Magnet Synchronous Motor
PP	Polypropylene
PP-MC	Poly-Phase Matrix Converter
PT	Punch-Trough
PWM	Pulse Width Modulation
QP	Quasi-Peak (used for EMC measurements)
RB-IGBT	Reverse Blocking IGBT
RC-IGBT	Reverse Conducting IGBT
SAC2	Semiconductor Area Based Converter Comparison
S-A-X	Unidirectional Direct Matrix Converter
SBD	Schottky Barrier Diode
SFOM	Schlangenotto Figure-of-Merit
Si	Silicon
SiC	Silicon Carbide
SLS	Switching Loss Shifting (IMC)
SMC	Sparse Matrix Converter
SSPVU	Switching Sequence Prediction and Verification Unit (CMC)
STSC	Sparse T-Source Converter

SV	Space Vector
SVM	Space Vector Modulation
T&FS	Trench and Field Stop
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TLSVM	Three-Level Space Vector Modulation
TSI	T-Source Inverter
USMC	Ultra Sparse Matrix Converter
VMOS	Vertical Metal Oxide Semiconductor (structure)
VR-VSI	VIENNA Rectifier with Voltage Source Inverter
VSBBC *or*	Voltage Source Back-to-Back Converter *or*
VLBBC	Voltage DC-Link Back-to-Back Converter
VSD	Variable Speed Drive
VSI	Voltage Source Inverter
VSMC	Very Sparse Matrix Converter
VSR	Voltage Source Rectifier
ZCS	Zero Current Switching
ZSC	Z-Source Converter
ZVS	Zero Voltage Switching

Abbreviations

ac	Alternating current
act	Active
aux	Auxiliary
avg	Average or averaged
const	Constant
ct	Coating
d	Direct component
dc	Direct current
dem	Demand or demanded
ff	Feedforward
flt	Filtered
ini	Initial
inp	Input or input stage
max	Maximum or maximal
min	Minimum or minimal
n	Electron, negative charge carrier

nom	Nominal
out	Output or output stage
p	Hole, positive charge carrier
pp	Peak-to-peak
q	Quadrature component
res	Resonance
rms	Root mean square
tor	Toroidal
tot	Total

Variables

A_{chip}	Total power semiconductor chip area
$A_{\mathrm{chip,SM}}$	Total chip area of a semiconductor module
A_{core}	Core cross sectional area
A_{SF}	Surface area
A_{SM}	Base area of the semiconductor module
Att	Attenuation
B	Magnetic flux density
$C_{\mathrm{CM},n}$	Common mode capacitance of n-th input filter stage
$C_{\mathrm{DM},n}$	Differential mode capacitance of n-th input filter stage
C_{DC}	DC-link capacitance
$C_{\mathrm{F,inp}}$	Input (filter) capacitance
$C_{\mathrm{F,out}}$	Output (filter) capacitance
$C_{\mathrm{iss,max}}$	Maximum input capacitance of a transistor
$C_{\mathrm{oss,eq}}$	Energy equivalent output capacitance of a transistor
$C'_{\mathrm{PCB,ll}}$	PCB layer-to-layer capacitance per unit area
$C'_{\mathrm{SM,PE}}$	Semiconductor module capacitance to PE per unit area
$C_{\mathrm{sw,eq}}$	Switching energy equivalent capacitance of a semiconductor device
$C_{\mathrm{th,CS}}$	Thermal capacitance of the cooling system
E_{crit}	Critical electric field
E_{G}	Band gap energy
E_{PC}	Precharging energy

E_{off}	Semiconductor turn-off loss energy
E_{on}	Semiconductor turn-on loss energy
E_{rr}	Diode reverse recovery loss energy
$E_{\mathrm{S/D}}$	Transistor or diode switching loss energy
ESL	Equivalent series inductance
ESR	Equivalent series resistance
G	Conductance
H_{K}	Knoope hardness
I_{SC}	Short-circuit current
J	Current density
K_{B}	Bulk module
K_{S}	Shear module
L_{B}	Boost inductance
$L_{\mathrm{CM},n}$	Common mode inductance of n-th input filter stage
L_{DC}	DC-link inductance
$L_{\mathrm{DM},n}$	Differential mode inductance of n-th input filter stage
L_{S}	Stator inductance
M_1	Modulation index of the input stage
M_2	Modulation index of the output stage
M_{12}	Modulation index from the input to the output stage (MC)
M_{M}	Motor torque
$M_{\mathrm{M},0}$	Motor torque at stand-still
N_{A}	Acceptor doping concentration
N_{D}	Donator doping concentration
N_{L}	Number of turns (inductor)
P_1	Real input power
P_2	Real output power
P_{aux}	Power consumption of the auxiliary supply
P_{CS}	Power consumption of the cooling system
P_{drv}	Power consumption of the gate driver
P_{cond}	Conduction losses
P_{core}	Core losses
P_{L}	Inductor losses
P_{semi}	Semiconductor losses
P_{semi}	Semiconductor losses
P_{sw}	Switching losses

Q_1	Reactive input power
Q_2	Reactive output power
Q_G	Gate charge
Q_S	Storage charge
R_DS	Drain-source on-resistance
R_on	On-resistance
R_PC	Resistance in the precharging path
R_S	Stator resistance
$R_\mathrm{th,CS}$	Thermal resistance of the cooling system
R_w	Wire resistance
S_1	Apparent input power
S_2	Apparent output power
T	Temperature
T_A	Ambient temperature
T_del	Delay time
T_J	Junction temperature
T_L	Inductor temperature
T_P	Pulse period
U_BD	Break down voltage
U_DSS	Specified drain source blocking voltage
$U_\mathrm{pinch-off}$	Pinch-off voltage
$U_\mathrm{S/D,F}$	Transistor or diode forward voltage drop
$U_\mathrm{S/D,R}$	Transistor or diode reverse voltage drop
V_C	Capacitor volume
V_CS	Volume of the cooling system
V_drv	Volume of the gate driver
V_L	Inductor volume
V_SM	Volume of the semiconductor module
W	Energy, work
Z_M	Motor impedance
$Z_\mathrm{th,JA}$	Thermal impedance between junction and ambient
$Z_\mathrm{th,JS}$	Thermal impedance between junction and sink
d	Relative turn-on time (modulation)
d_i	Inner (core) diameter
d_w	Wire diameter
f_1	Electrical input frequency
f_2	Electrical output frequency
$f_\mathrm{Clk,PWM}$	PWM generator clock frequency
$f_{\mathrm{c},n}$	n-th corner frequency

f_{sw}	Switching frequency
h_{C}	Height of the capacitor case
h_{CS}	Height of the cooling system
h_{SM}	Height of the semiconductor module
i	Link current
i_1	Input current
i_2	Output current
i_{A}, i_{B}, i_{C}	Output phase (A, B, C) currents
i_{a}, i_{b}, i_{c}	Input phase (a, b, c) currents
i_{cond}	Conducted current
i_{C}	Collector current (when used for transistors)
i_{DC}	DC-link current
i_{DS}	Drain-source current
i_{F}	Forward current
i_{SD}	Source-Drain current
i_{sw}	Switched current
k_{BFOM}	Ratio of the BFOM
k_{SFOM}	Ratio of the SFOM
l_{CS}	Length of the cooling system
l_{SM}	Length of the semiconductor module
m_{C}	Weight of the capacitor
m_{CS}	Weight of the cooling system
m_{drv}	Weight of the gate driver
m_{L}	Weight of the inductor
n_{i}	Intrinsic carrier density
q	Surface charge density
r_{F}	Differential forward resistance
r_{R}	Differential reverse resistance
s_n	Switching function of n-th switching state
t	Time
t_{rise}	Rise time
u	Link voltage
u_1	Input phase voltage
u_2	Output phase voltage
u_{A}, u_{B}, u_{C}	Output phase (A, B, C) voltages
$u_{\mathrm{A,0}}$, $u_{\mathrm{B,0}}$, $u_{\mathrm{C,0}}$	Output terminal (A, B, C) voltages referenced to ground
u_{a}, u_{b}, u_{c}	Input phase (a, b, c) voltages
u_{com}	Commutation voltage
u_{DC}	DC-link voltage

u_{DS}	Drain-source voltage
u_{F}	Forward voltage (drop)
u_{GS}	Gate-source voltage
u_{N}	Mains voltage
$u_{\mathrm{n,0}}$	Voltage between the negative bus and ground
$u_{\mathrm{p,0}}$	Voltage between the positive bus and ground
u_{R}	Reverse voltage (drop)
u_{SD}	Source-drain voltage
v_{sat}	Saturation drift velocity
u_{sw}	Switched voltage
w_{CS}	Width of the cooling system
w_{n}	Width of the n-doped drift region
w_{SCL}	Width of the space charge layer
$w_{\mathrm{S/D}}$	Transistor or diode switching loss energy function
w_{SM}	Width of the semiconductor module
Φ_1	Input current-to-voltage displacement angle
Φ_2	Output current-to-voltage displacement angle
Ψ_{P}	Motor flux
α	Thermal coefficient
δ_{u}	Relative voltage variation
ε	Permittivity
ε_{r}	Relative permittivity
$\gamma_{\mathrm{A_{chip-SM}}}$	Ratio of the chip area to the base plate area semiconductor module
γ_{V}	Volumetric scaling factor
γ_{w}	Wire winding factor
γ_{μ}	Permeability scaling factor
η	Efficiency
λ_{th}	Thermal conductivity
μ_{n}	Electron mobility
μ_{p}	Hole mobility
ρ_{C}	Density of the capacitor
ρ_{Cu}	Specific dc resistance of copper
ρ_{L}	Density of the inductor
ρ_{SM}	Density of the semiconductor module
σ_{on}	Specific conductivity in the on-state
ς_{th}	Specific thermal power flow
$\tau_{1\ldots6}$	Absolute turn-on times (modulation)
τ_{C}	Capacitor time constant

τ_{th}	Thermal time constant
φ_1	Input (reference) phase angle
φ_2	Output (reference) phase angle
φ_{M}	Motor shaft angle
φ_{mod}	Phase displacement between the modulation of the input and the output stage
ω_{M}	Angular mechanical frequency of the motor

Definitions

x, $x(t)$	General, time-varying quantity or signal
X	DC component (large-signal) if used for general quantities or rms value if used for ac quantities (unless differently specified)
$\tilde{x}$	AC component (small-signal)
$\hat{X}$	Peak value
$\vec{x}$, $\vec{x}(t)$	Time-varying space vector
$\underline{x}$	General single column vector ($n \times 1$), typically used for the notation of quantities in different reference frames, e.g. $\underline{x} = [x_{\mathrm{d}}\ x_{\mathrm{q}}]^T = \begin{bmatrix} x_{\mathrm{d}} \\ x_{\mathrm{q}} \end{bmatrix}$ or for complex numbers, e.g. $\underline{Z} = \lvert\underline{Z}\rvert \cdot e^{j\varphi_Z}$
*	Reference value
**	Estimated value

Constants

$e_0 = 1.602 \cdot 10^{-19}\,\mathrm{C}$	Elementary (unit) charge
$k = 5.6704 \cdot 10^{-8}\,\mathrm{W/(m^2K^4)}$	Stefan-Boltzmann constant
$\varepsilon_0 = 8.854 \cdot 10^{-12}\,\mathrm{As/(Vm)}$	Permittivity of free space
$\mu_0 = 1.257 \cdot 10^{-6}\,\mathrm{Vs/(Am)}$	Permeability of free space

Contents

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Chapter 1

Introduction

Electric drives convert electrical energy into mechanical energy. They serve as linking system components between an electrical source and a mechanical load, and typically consist of a power electronic circuit and an electric motor. Electric drives have become an essential part in our society and found their way in our daily life, for example in home and residential appliances such as air conditioning systems, washing machines, heat pumps, or power tools or in transport, in particular for electric and hybrid electric vehicles.

Electric drives are the most widely applied drive engines for providing mechanical power. According to surveys presented by the European Center for Power Electronics (ECPE) [1], approximately 60% of the worldwide industrial electrical energy consumption is used for electric drives. This figure does not only show their significance in terms of energy consumption, but also highlights the achievable energy savings if highly efficient variable speed drives with optimized power electronic converters and motors are implemented.

Due to their diversified applicability, electric drives have become a key system component for industry, transportation, and consumer products.

1.1 Electric Drive Technology

1.1.1 Historical Review

1800–1875 Discovery of the Fundamentals for Electric Drives

Hans Christian Oerstedt discovered in **1820** that a magnetic needle is deflected in the proximity to a current conducting wire. In the same year, André Marie Ampère made his fundamental discovery of the interaction between electric currents and magnetic fields. These discoveries resulted in a strong development of "Electromagnetic Machines". These machines, however, were only rarely implemented in practical applications due to the lack of powerful electric sources.

An important step forward occurred in **1831** when Michael Farrady discovered the electro-magnetic induction. This effect was soon adopted for electric generators to provide more powerful electric sources.

In **1866**, Werner von Siemens developed the so-called "Dynamo Machine", a DC generator that used the remanence flux of the magnetic poles to generate the initial excitation.

1875–1920 Electric Drives for Industry and Craft

Michael von Dolivo-Dobrowolski invented in **1889** the three-phase squirrel cage induction machine, which became the most widely used motor type in industry. He also gave distinction to the term "rotary current".

Two years later, in **1891**, the first three-phase electric transmission line (175 km), from Lauffen am Neckar to Frankfurt am Main, Germany, was installed. Therewith, the basis for a large-scale implementation of electric energy transmission and drive systems was established. Concurrently, the Ward-Leonard system was introduced and soon became one of the most widely used concepts for electric motor speed variation.

During the following years, the performance and operating behavior of electric machines and drive systems were steadily improved. Auxiliary resistor circuits and Ward-Leonard systems allowed the implementation of first variable speed drives. These new electric drive solutions led to a gradual replacement of the steam and gas engine drives technology.

1920–1950 Spreading of Electric Drives

From **1920** onwards, electric drives were applied in industry, transportation, craft, agriculture, and even in home appliances. The number of electric drives increased rapidly. Two different development directions can be observed: integrated solutions, where the electric motor was integrated in an application specific machine or standardized, general purpose drives for mass production.

In order to achieve speed variability, besides star-delta switching with electro-magnetic circuit breakers, resistor circuits, and Ward-Leonard systems, around **1930**, first controlled power amplifiers using gas filled tubes (thyratorns) were developed and applied. This was the **birth of modern power electronics** in electric drives technology.

One of the most important invention for electrical engineering and electronics was made in **1947** when John Bardeen, William Shockley, and Walter Brattain from the Bell Laboratories presented the first working controllable silicon (Si) switch, the transistor.

1950–1970 Switched Converters for Electric Drives

With the development of power semiconductors, such as the power diode in **1952** and the thyristor in **1957**, the replacement of the gas or vacuum tube technology was initiated. At the same time control technology improved rapidly due to the analog electronic components provided by the novel silicon transistor technology.

The first Bipolar Junction Transistors (BJTs) with substantial voltage and current handling capabilities were introduced in the **1960s** and enabled the implementation of a new generation of pulse-width modulated power converters for motor drives. Both, the new power semiconductors as well as the improvements in control technology stimulated the spreading of electric drives.

Since 1970 Electric Drives with Micro-Processors

The availability and introduction of micro-processors resulted in a development stimulus in the electric drive technology. The so far analog controllers were replaced by digitally controlled power electronic converters. The development of the field-oriented control by Blaschke in **1971** and its implementation in micro-processor controlled drives

enabled to operate three-phase ac motors with similar control performance and quality as dc motors. The steadily increasing performance of micro-processors and the development of application specific Digital Signal Processors (DSPs), first introduced by NEC and AT&T in **1980**, enabled the implementation of more complex control algorithms and converter modulation schemes.

A similar development occurred in the area of power semiconductors with the invention and implementation of new devices such as GTOs, IGBTs, IGCTs, high-voltage and charge compensated MOSFETs, etc. to mention just the most important ones. The availability of IGBTs finally provided the basis for modern low-voltage drive systems.

Since the late **1980s**, new wide-bandgap power semiconductor materials different from Si with favorable properties, such as silicon carbide (SiC) or gallium nitride (GaN), have been investigated to develop semiconductor devices. In **2001**, Siemens presented the first SiC Schottky barrier diode. Besides diodes, since **2003** also first SiC prototype switching devices, primarily normally-on SiC Junction Field Effect Transistors (JFET) produced by SiCED, have become available.

Currently, in **2010**, electric drives are about to find their way into new applications such as Hybrid Electric Vehicles (HEVs) or More Electric Aircraft (MEA) applications, where the well-established but heavy hydraulic actuation systems are replaced by electro-hydraulic or purely electric actuators. Power semiconductor manufacturers are launching first commercially available SiC transistors and thus are providing the components for a possible new generation of power converters for electric drive applications.

1.1.2 State-of-the-Art Electric Drives

Modern electric drives are extremely diversified and available with a wide variety of options in order to best match them to the target application. The mechanical energy, provided to the load machine, has to be supplied according to the demanded load and mission profile to enable proper control of the process quantities. In current motion control applications with multiple axis, the individual axis are driven by single servo drives, which are typically coordinated with a superordinate bus system, and thus are replacing the traditional drive concept with centralized electric motor, upright shaft, and different gearboxes.

A schematic of a typical state-of-the-art electric Variable Speed Drive (VSD) is depicted in Fig. 1.1. The two key components of a VSD are the power converter and the electric motor. As a result of the ever increasing digitalization in electric drive technology, the power converters have steadily gained in complexity and importance compared to the actual electric motor. A modern power converter is not any more simply a power amplifier, a linking device between source and load that allows for motor control, but a high-end power and signal electronics system that implements additional functionality, such as communication interfaces, protection circuitry, fault detection and handling, input and output filtering, active damping, motor and load machine parameter estimation, algorithms for automated commissioning and process control optimization, etc. Consequently, for a state-of-the-art electric VSD the transitions between power electronics, drive, automation, and embedded system technology have become seamless.

(The above historical review of electric drive technology is based on [2].)

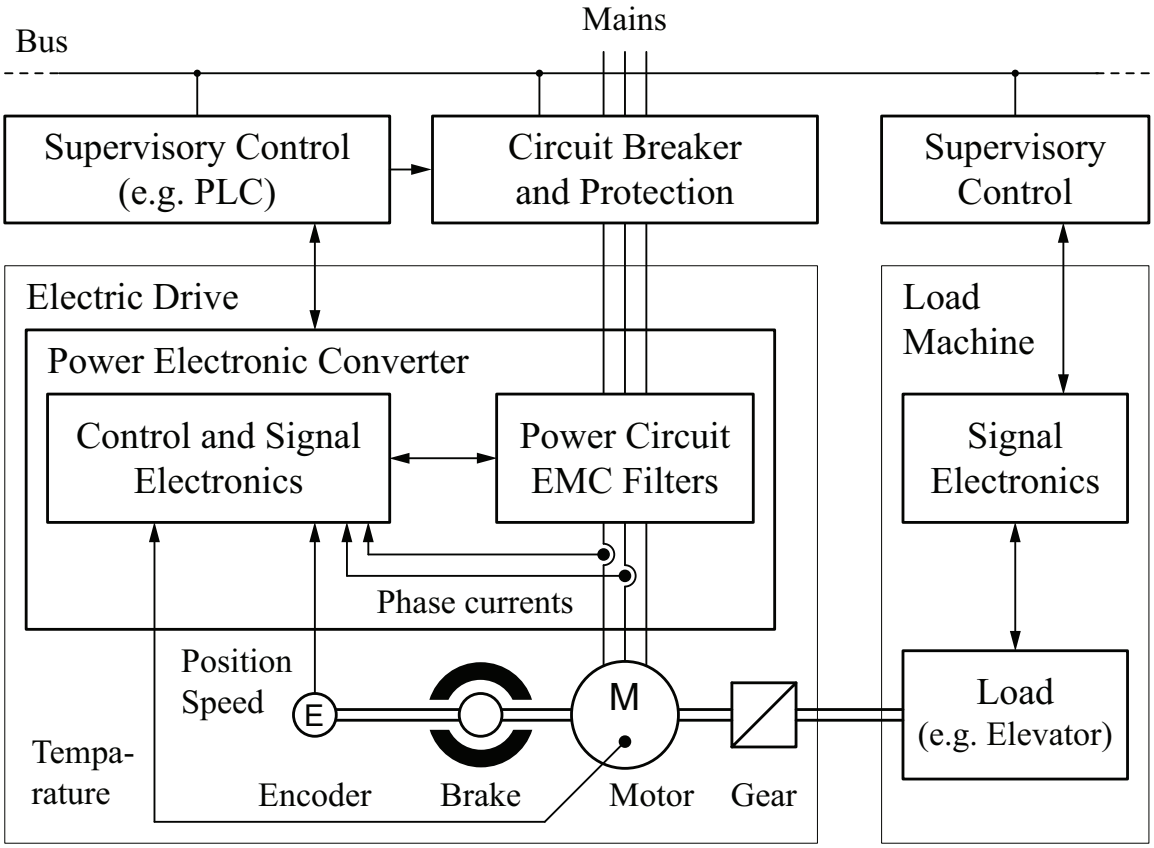


Fig. 1.1: Schematic of a modern electric drive with a load machine.

1.2 Purpose of this PhD Thesis

1.2.1 Motivation

For the last three decades, a wide variety of different converter topologies, modulation schemes, control algorithms, and power semiconductor devices have been analyzed and suggested for electric drive applications. In spite of the large amount of conducted research, investigations performing a comprehensive comparison of different bidirectional ac-ac converter topologies still are very rare.

A detailed analysis, performed as a preparation of this work, revealed that there is still a need to conduct further research in the topic area of ac-ac converters if more holistic questions are addressed. Such questions involve converter comparisons, drive system optimizations, or the assessment of the impact of new semiconductor technologies on different converter topologies as for instance the currently emerging SiC transistors. These fundamental findings form the basis of the research objectives, questions, and hypotheses investigated in this PhD thesis.

1.2.2 Research Task

The aim of the proposed research is to perform a systematic evaluation and comparison of three-phase, bidirectional, hard-switched, unity power factor input, ac-ac converters for low-voltage motor drive application, utilizing conventional silicon and state-of-the-art silicon carbide power semiconductors. The topologies to be investigated are the Voltage Source Back-to-Back Converter, the Current Source Back-to-Back Converter, the Indirect Matrix Converter, and the Conventional (direct) Matrix Converter, with a particular focus on the Indirect Matrix Converter.

1.2.3 Research Objectives

The aspired research objectives are:

- To identify the characteristic properties and components of ac-ac converters and to derive adequate analytical models.
- To acquire the required but unknown characteristic data of the SiC prototype devices through experimental measurements.
- To investigate the relationship(s) between semiconductor losses, semiconductor chip area, thermal properties, and cooling system requirements.
- To analyze the EMI input filter and passive component requirements.
- To gain through analysis of the characteristic system quantities a better insight into the interdependencies of inner parameters of ac-ac power converter topologies.
- To develop a systematic converter comparison that allows for a holistic assessment.
- To investigate the hypothesis, frequently stated in scientific publications, that Matrix Converters (MCs) have superior properties in terms of achievable efficiency and power density compared to conventional converter topologies.
- To practically verify the theoretical findings and concepts with industry-oriented converter prototypes.
- To hopefully provide, with the suggested methodology of comparison, a tool to analyze and assess the potential of current and future power semiconductor technologies for ac-ac converters.

1.3 Thesis Structure

1.3.1 Chapter Overview

The thesis layout displays the progression of research, leading the reader step-by-step to the final comparative evaluation of the Voltage Source Back-to-Back Converter, the Current Source Back-to-Back Converter, the Indirect Matrix Converter, and the Conventional Matrix Converter.

Chapter 1 includes an introduction to the electric drive technology, states the main research aim and research objectives, and provides the literature and ac-ac power converter topology review.

Chapter 2 discusses the most important power semiconductor transistors and diodes for low-voltage drives including SiC devices with their basic physical properties. Special attention is paid to 1200 V Si IGBTs and normally-on SiC JFETs.

Chapter 3 investigates possible Space Vector Modulation (SVM) schemes for the considered converter topologies and describes the implementation of the selected modulation schemes. Furthermore, an overview of the main converter control properties is provided.

Chapter 4 summarizes the analytical power semiconductor loss modeling of the individual converter topologies. Different characteristic converter operating points are identified and analyzed regarding semiconductor losses and loading.

Chapter 5 presents a new Semiconductor chip Area based Converter Comparison (SAC2) linking the power semiconductor losses, with the cooling system requirements. This comparison eventually enables a trade-off study between converter efficiency, volume, and cost and thus provides a tool for motor drive optimization.

Chapter 6 The first part is dedicated to the dimensioning of the passive components. Various control, energy, and voltage and current ripple based design criteria are derived. Scaling laws for the capacitor and inductor component volumes and weights are presented. The second part focuses on modeling Conducted Emission (CE) Electromagnetic Interference (EMI) levels.

Chapter 7 describes the actual ac-ac power converter topology comparison and assessment, which is systematically performed using the concepts and data derived in the previous chapters.

Chapter 8 concludes the thesis with a discussion of the results, the thesis conclusions, and an outlook on possible future work.

In the **Appendices A–B**, the implemented hardware prototypes including their key figures and results and the developed measurement setups are presented.

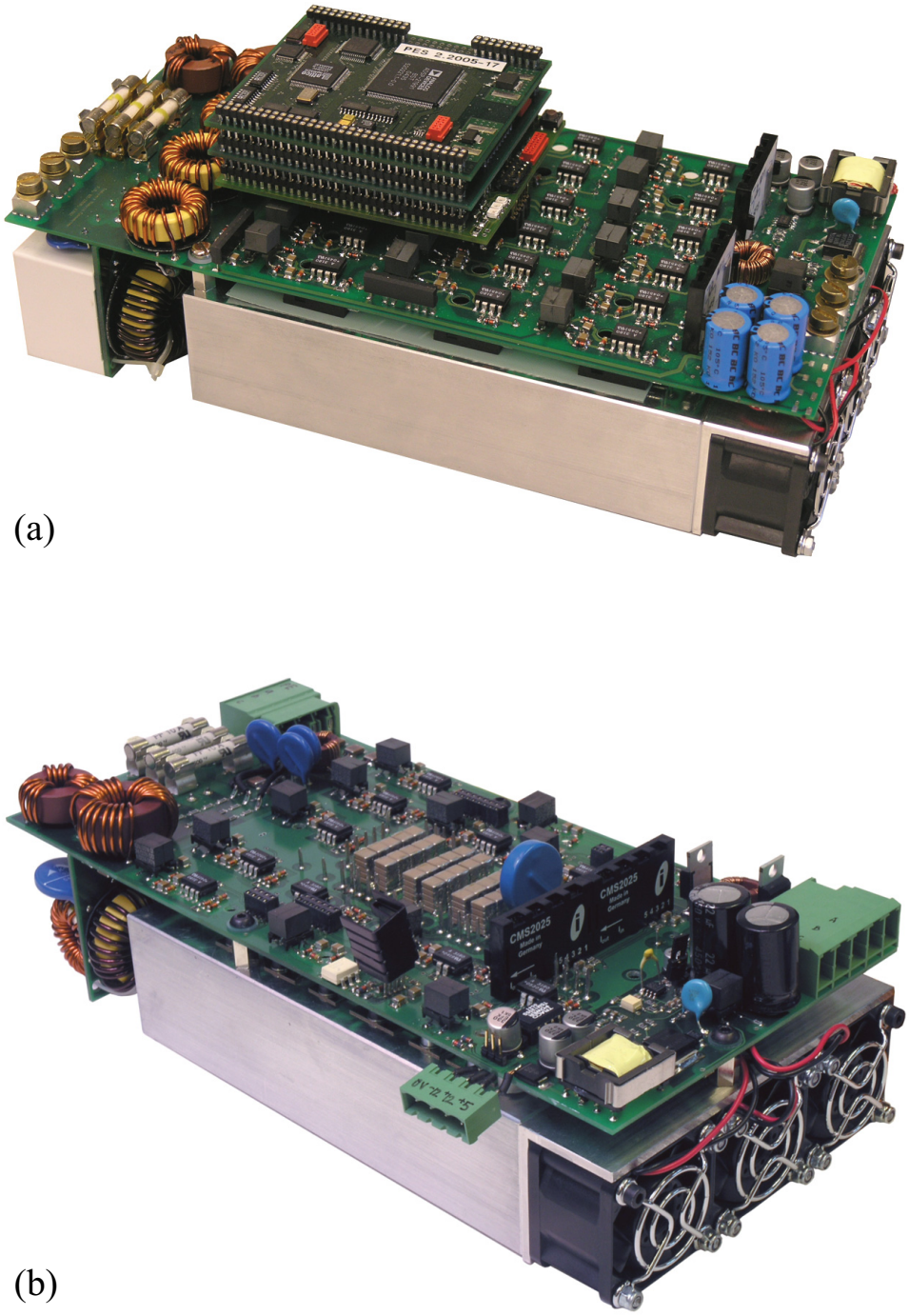
1.3.2 Hardware Overview

A major part of this research work is formed by the various converter hardware prototypes that were implemented for experimental verification of the analytical and numerical converter models or for converter and component data acquisition. The evaluation of real in-system performance data is of particular importance for analyzing prototype or pre-commercial SiC transistors as detailed data sheets of such devices were and still are not available. This fact makes hardware prototypes an indispensable prerequisite, particularly for the investigation of all-SiC converter systems and motivates the numerous converter prototypes designed and implemented during this PhD thesis.

Fig. 1.2 and Fig. 1.3 provide an overview of the constructed converters prototypes. The ac-ac converter topologies and semiconductor technology configurations were combined such that with a minimum number of prototypes a maximum number of topological variations results. The implemented prototypes can be subdivided into two groups:

- all-Si or Si IGBT and SiC diode ac-ac converters (cf. Fig. 1.2) with a switching frequency range of 20 kHz to 50 kHz and
- highly compact, high switching frequency, all-SiC ac-ac converters (cf. Fig. 1.3) with a nominal switching frequency of up to 200 kHz.

All hardware prototypes were designed and constructed at the PES Laboratory of ETH Zurich mainly as part of industry research projects.



(a)

(b)

Fig. 1.2: (a) RB-IGBT Indirect Matrix Converter (RB IMC) and **(b)** Si-SiC Ultra Sparse Matrix Converter (Si-SiC USMC) hardware prototypes.

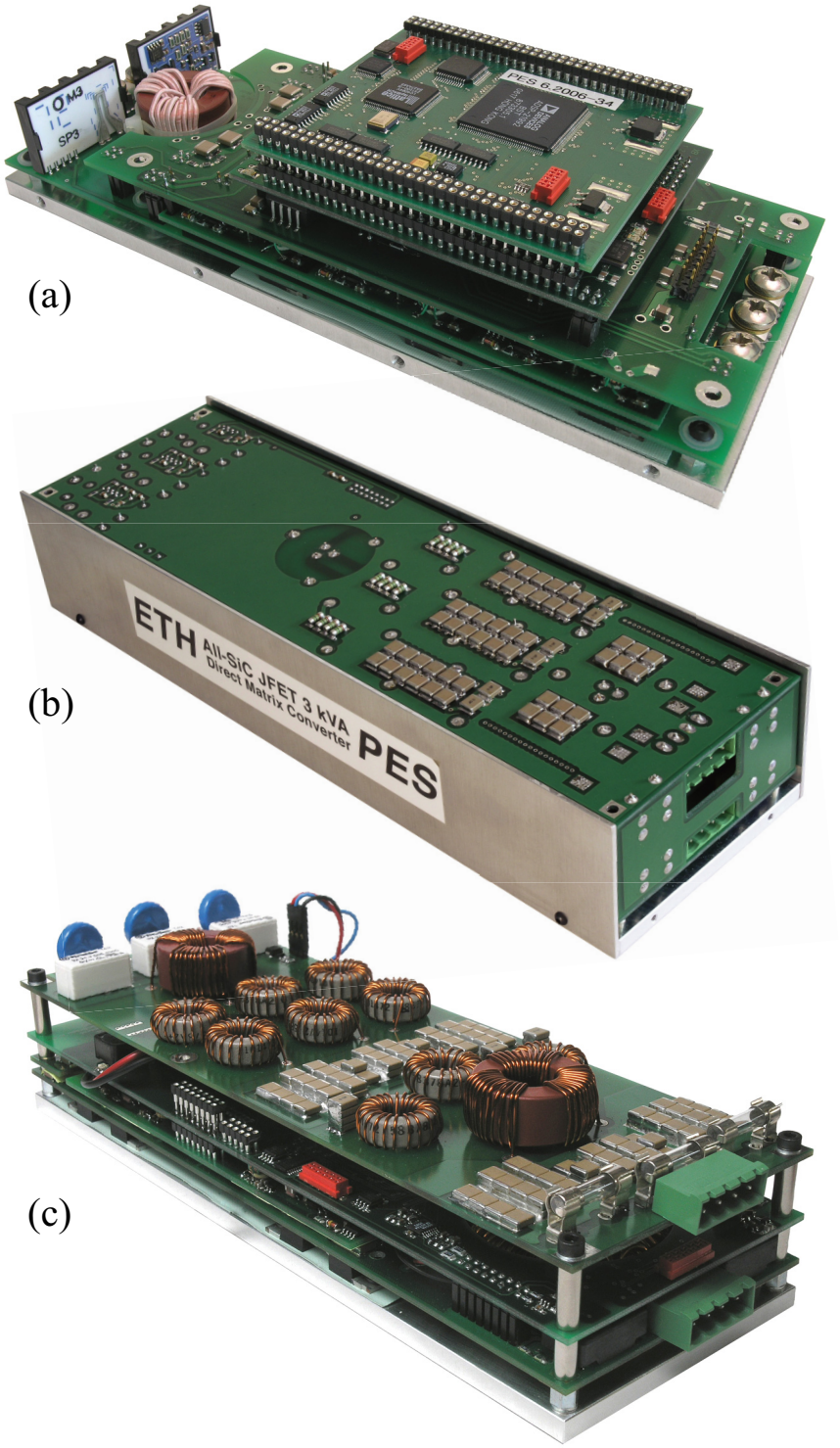


Fig. 1.3: (a) All-SiC Indirect Matrix Converter (All-SiC IMC), **(b)** All-SiC Conventional Matrix Converter (All-SiC CMC), and **(c)** All-SiC Current Source Back-to-Back Converter (All-SiC CSBBC) hardware prototypes.

1.4 Literature Review

1.4.1 Overview

The literature review is subdivided into two parts. First of all, a summary of the development of low-voltage ac-ac converters (definition cf. Tab. 1.1), required for the comparative evaluation performed in this thesis, is presented. Subsequently, the literature comparing different ac-ac converter topologies is reviewed, and commonly applied methods of comparison are discussed.

1.4.2 Review of AC-AC Converter Topologies

The development of ac-ac converters has been closely related to the advancement of power semiconductor technology and the availability of suitable semiconductor devices. Virtually every modern low-voltage VSD utilizes a self-commutated, switch-mode inverter as a power electronic interface between the rectified mains and the electric motor. The present and well-established self-commutated converter topologies evolved from the line-commutated thyristor converters, with the manufacturing of BJTs with increased power handling capability and in particular with the development of the IGBT technology in the 1980s.

The line-commutated converters were typically used for generating variable dc voltages or supplying dc motors. In current industrial VSD systems mainly three-phase ac motors are applied, due to their robustness, low-maintenance, and high reliability. Consequently, the requirement of a modern ac-ac converter is to generate from a three-phase mains input with typically a constant voltage amplitude and a fixed angular frequency (apart from specialist applications with variable frequency input, as e.g. in MEA applications) an output voltage or current

IEC Voltage Range	*AC*	*DC*
Extra-Low-Voltage	$< 50\,\mathrm{V}$ (rms)	$< 120\,\mathrm{V}$
Low-Voltage	$50 - 1000\,\mathrm{V}$ (rms)	$120 - 1500\,\mathrm{V}$
High-Voltage	$> 1000\,\mathrm{V}$ (rms)	$> 1500\,\mathrm{V}$

Tab. 1.1: IEC voltage range definition.

with a variable amplitude and a variable angular frequency. For motor drives, featuring frequent or long braking intervals in their load cycles, as found for example for elevators, cranes, or in motion control applications with high moments of inertia, it is environmentally, economically, and technologically worthwhile to apply bidirectional ac-ac converters. Such converters are capable of feeding energy back into the mains, and therewith may not only improve the overall energy efficiency of the drive system, but also enable to reduce the overall installation volume as large braking resistors can be omitted.

The requirements for state-of-the-art bidirectional, ac-ac converters for motor drive applications can be summarized as follows:

- competitive price level,
- high reliability,
- high efficiency,
- high input and output power quality, i.e.
  - unity input power factor,
  - low harmonic content in input current and output voltage,
  - smooth motor operation (low acoustic noise and vibrations),
- low EMI,
- compact case with low cooling requirements,
- modularity,
- versatile configurability,
- high user friendliness, and
- simple commissioning and maintenance.

For the last three decades, a large number of investigations have been performed and published in the subject area of low-voltage ac-ac converters for motor drive applications. The following review aims at summarizing the key bidirectional, hard-switched ac-ac converter topologies and their basic properties. If available also the corresponding unidirectional implementations are presented.

Voltage Source Back-to-Back Converter

The most popular and industrially, indisputably most widely used bidirectional ac-ac converter topology is the two-level Voltage Source Back-to-Back Converter (VSBBC), also known as Voltage DC-Link Back-to-Back Converter (VLBBC), depicted in Fig. 1.4.

The VSBBC is a two-stage topology that consists of a back-to-back connection of a Voltage Source Rectifier (VSR) input stage and a Voltage Source Inverter (VSI) output stage, which is decoupled by the dc-link capacitor C_{DC}. The dc-link capacitor serves as an energy storage element and impresses a constant voltage across the dc-link. The inductors L_{B}, placed between the input terminals (a, b, c) and the midpoints of the input bridge-legs, enable input power factor correction under the restriction of boost operation of the input stage. Therefore, these inductors are often termed as boost-inductors. Due to the polarity of the power diodes the dc-link voltage is confined to positive values.

For most applications, the VSBBC is connected to an inductive load (electric motor), as indicated in Fig. 1.4, and in this case features sinusoidal input and output currents with a certain current ripple. The VSR input stage is controlled such that a sinusoidal mains current is drawn that is in phase (motor operation) or opposite-phase (generator

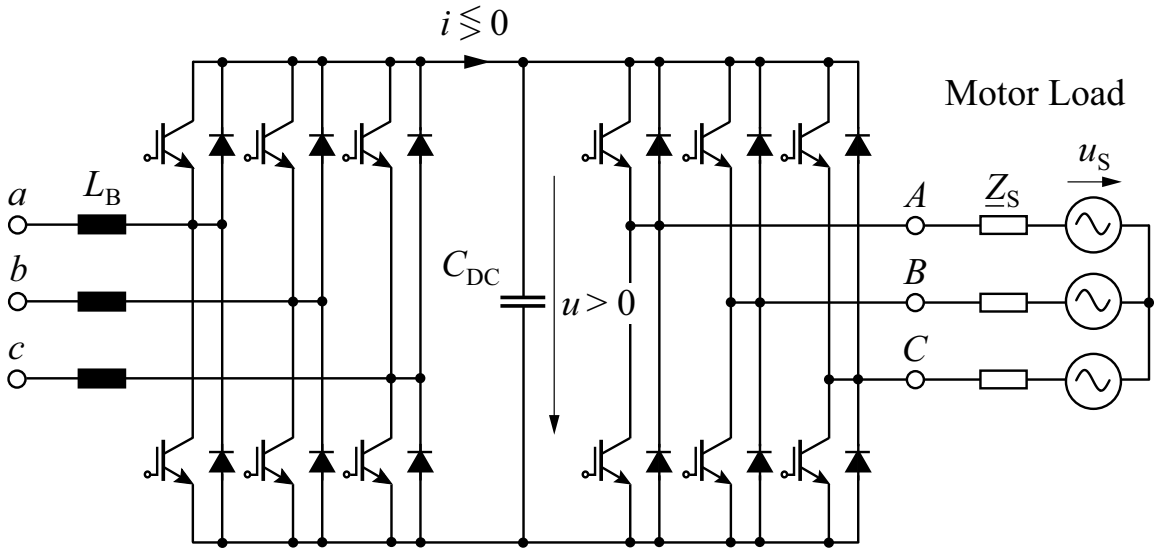


Fig. 1.4: Voltage Source Back-to-Back Converter (VSBBC), supplying a permanent magnet synchronous machine (PMSM) with equivalent stator phase impedance $\underline{Z}_{\mathrm{S}}$ and back-emf voltage u_{S}.

operation) with the corresponding mains phase voltage and controls the dc-link voltage to a constant value. The VSI output stage controls the load; for an electric motor the speed and available torque. As both, the input and output stage of the VSBBC are hard-switched, conduction and switching losses are generated in both stages. For the implementation of the VSBBC, 12 discrete power transistors and 12 anti-parallel diodes are required, or 12 Reverse Conducting IGBTs (RC-IGBTs), as currently produced for example by ABB, Infineon, or Mitsubishi. (For the following schematics of ac-ac converter topologies, the load equivalent circuit is not shown.)

If only unidirectional power flow without sinusoidal input currents is required, the switches in the input stage can be omitted. This results in a Voltage Source Inverter topology with a passive B6 diode bridge front-end (B6-VSI), as shown in Fig. 1.5. The B6-VSI is the most frequently applied topology for VSDs in industry due to its simplicity and high nominal efficiency of up to approximately 98.5% for switching frequencies below 10 kHz. Compared to the VSBBC, the B6-VSI cannot provide sinusoidal input currents, and therefore, depending on the power quality requirements, bulky harmonic input filters have to be added.

In order to enable unidirectional power flow with sinusoidal input currents, the passive diode rectifier of the B6-VSI can be extended with three switches and twelve diodes as illustrated in Fig. 1.6 leading to the well-known active VIENNA Rectifier (VR) [3]. (An implementation

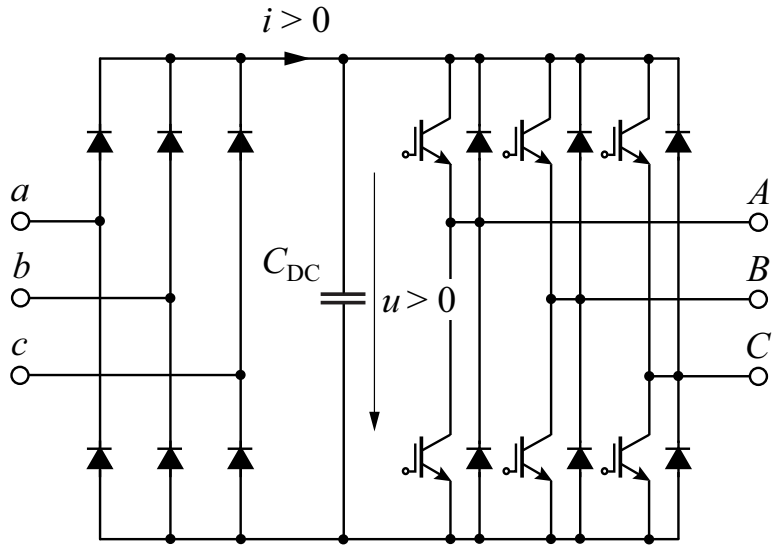


Fig. 1.5: Diode bridge rectifier with Voltage Source Inverter (B6-VSI).

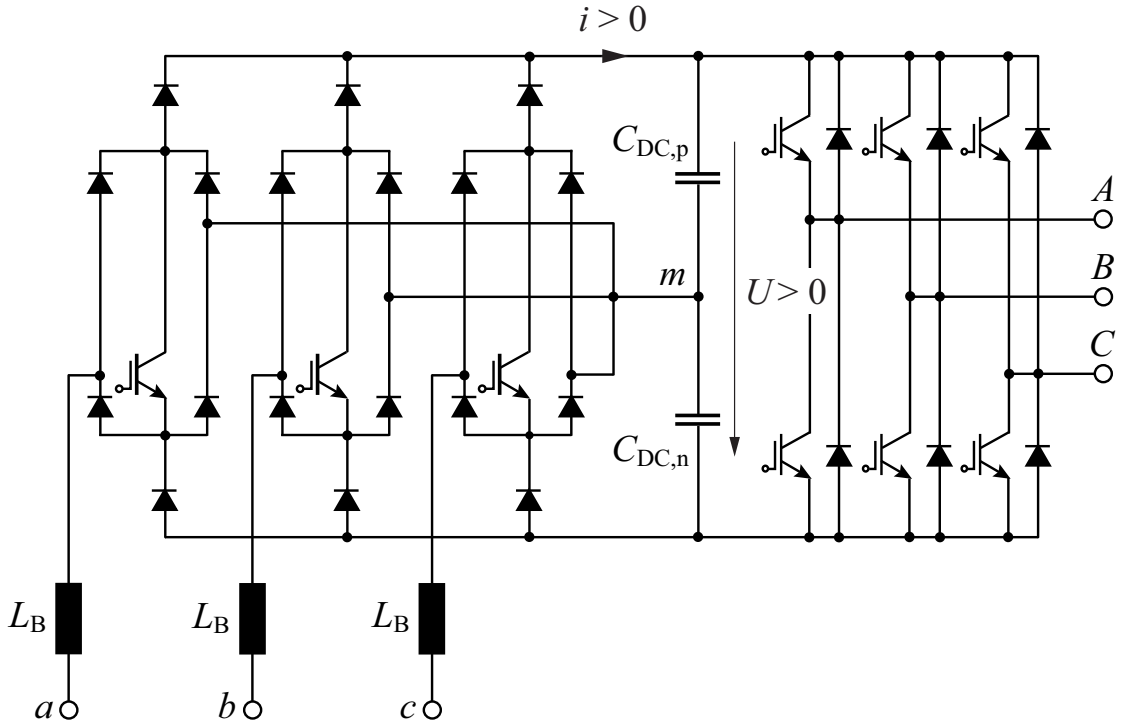


Fig. 1.6: VIENNA Rectifier with Voltage Source Inverter (VR-VSI).

with six switches is also possible). The resulting unidirectional ac-ac converter topology is a VIENNA Rectifier connected to a Voltage Source Inverter (VR-VSI). Contrary to the active two-level VSR in Fig. 1.4 with six switches and six diodes, the VR is a three-level topology and thus allows the implementation of semiconductors with half of the blocking voltage and reducing the value of the boost inductors L_B. This enables a high efficiency and a compact implementation in particular for power levels and switching frequencies, where the semiconductor losses are dominated by the switching losses.

A variety of different scientific papers has been published for the past decades due to the versatile applicability of VSBBCs. Most of the investigations have been performed in the topic area of control, application specific evaluations, and reduction of the dc-link capacitor value.

With the further development of control theory most of the novel control concepts such as state feedback control, deadbeat control, or model predictive control have been applied to voltage source converters [4–18]. Furthermore, advanced control concepts and converter models have been investigated to provide active damping or filtering [19–22] and thus to improve the converter input and output power quality.

Another focus of research addresses the volume reduction of the passive components of the VSBBC in particular the reduction of the dc-link capacitor [23–32], as it considerably contributes to the overall converter volume and cost.

Many different modulation schemes have been developed for the VSBBC. They can be subdivided into Pulse Width Modulation (PWM) based schemes, utilizing different carrier signals, and Space Vector (SV) based modulation schemes. For motor drive applications, the Space Vector Modulation (SVM) has established as it allows for a mathematical description of the drive from the converter input to the motor axes using the same concept. The modulation techniques for voltage-source-type converters are known for a long time [33,34]. More recent research [35,36] has been analyzing modulation schemes in terms of reducing semiconductor losses and improving electromagnetic compatibility (EMC).

Current Source Back-to-Back Converter

Compared to the VSBBC, the Current Source Back-to-Back Converter (CSBBC), shown in Fig. 1.7, features an inductor L_{DC} as energy storage element in the dc-link. The CSBBC, also referred to as Current DC-Link Back-to-Back Converter (CLBBC), consists of a back-to-back connection of a Current Source Rectifier (CSR) and a Current Source Inverter (CSI) with unidirectional dc-link current $i > 0$, imposed by the circuit topology. Power reversal is achieved by reversal of the dc-link voltage u.

Consequently, the requirements for the power switching devices of the VSBBC and CSBBC are complementary. The anti-parallel transistor-diode configuration of the VSBBC enables bidirectional current flow but only unipolar voltage blocking, whereas the transistor-diode series connection of the CSBBC enables only unidirectional current flow but bipolar voltage blocking. The conduction losses of the CSBBC are higher than for the VSBBC as there are always four semiconductor devices in the current path between an input and output terminal due to the series connection of transistor and diode compared to two as in the VSBBC. In addition, the volumetric energy storage density of capacitors is significantly higher (cf. Sec. 6) compared to inductors, which allows for a more compact implementation of the VSBBC compared with the CSBBC for an equal amount of energy storage.

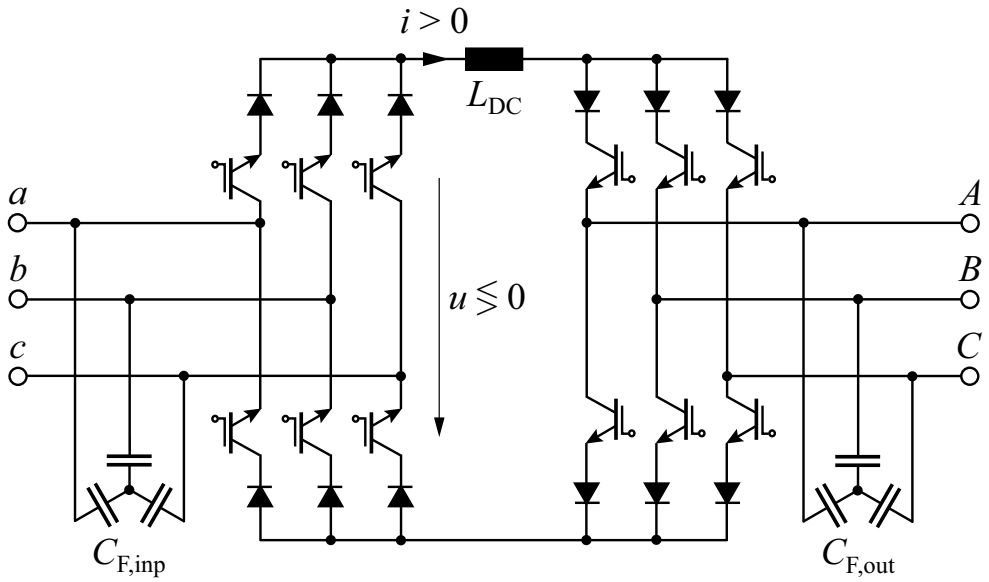


Fig. 1.7: Current Source Back-to-Back Converter (CSBBC) including input and output filter capacitors.

The star connected capacitors $C_{\mathrm{F,inp}}$ (a delta connection is also possible), placed across the input terminals (a, b, c), provide decoupling from the inductive mains and impressed input voltages and thus allow for sinusoidal input currents for buck operation of the input stage. As a result of its dual functional principle compared to the VSBBC, the CSBBC demands impressed input and output voltages instead of impressed currents and thus requires additional output capacitors $C_{\mathrm{F,out}}$. This can be considered as an advantage as well as a disadvantage of this topology. The output power quality benefits from the implementation of the converter output capacitors as with these capacitors a sinusoidal output filter is integrated. However, the disadvantage with the voltage impressed output in terms of the overall volume is that the motor stator inductance is not directly used to smooth the output currents. The implementation of the CSBBC requires 12 discrete power transistors with 12 series diodes or 12 Reverse Blocking IGBTs (RB-IGBTs), currently produced for instance by Fuji or IXYS.

Industrial low-voltage CSBBC systems are available but are typically utilized for special applications. Adequate applications of CSBBCs are for example low-inductance motor drives, where a sinusoidal output filter is already demanded. In this case the CSBBC topology might allow for a more compact implementation as only one dc-link inductor

instead of three output filter inductors, compared with the VSBBC, would be required. Generally, current-source-type converter topologies are more widely used for high power applications.

Due to the additional energy storage at the converter output, provided by the output capacitors, the CSBBC is more intricate to control than the VSBBC. It is obvious that oscillations are likely to occur between the input capacitors and the mains, as both the mains system and the input stage of the CSBBC are voltage impressed. Consequently, for the past two decades, research on current source converters has mainly been analyzing control concepts and active damping and filtering strategies to improve the dynamic performance and operating behavior [37–49].

Smart converter control allows also for reducing the conduction losses and therewith increasing the converter efficiency by controlling the dc-link current depending on the load requirements instead of controlling it to a constant nominal value. A similar control strategy would be possible for the VSBBC by varying the dc-link voltage depending on the operating conditions. A conventional control approach analogous to the VSBBC, using cascaded dynamic feedback loops, can also be applied for the CSBBC. In such a control scheme the input stage controls the dc-link current and provides sinusoidal input currents, whereas the output stage controls the output voltage and the load current.

Another field of research of the CSBBC has been the investigation and further development of modulation schemes [50–59] targeting a reduction of the semiconductor losses and the switching harmonics.

Different investigations [60–62] have also been performed to analyze and improve the harmonic behavior of the CSBBC through selected modulation strategies providing harmonic elimination.

Application oriented research [63–67] with specific CSBBC designs, tailored to optimally suit the application requirements, have proven that the CSBBC can be a viable alternative to the VSBBC.

Z-Source Converter

The Z-source converter concept uses a combination of capacitors and inductors as energy storage elements in the intermediate link to provide enhanced functionality. Its development was motivated by the disadvantages of the well-established B6-VSI such as the limited input-to-output voltage transfer ratio and the inrush and harmonic currents, generated

by the diode rectifier. If a B6-VSI is operated at under-voltage, the nominal terminal voltage of the load might not be achievable as the VSI can only be operated as a buck (step-down) converter. If the load is an Induction Motor (IM), the efficiency of the motor might then be lowered [68].

The unidirectional Z-Source Inverter with a three-phase diode rectifier front-end (B6-ZSI) according to Fig. 1.8 employs a LC network in the dc-link, the Z-source, and provides a solution to the limited output voltage range of the B6-VSI. The B6-ZSI can generate a higher output voltage than the line-to-line input voltage as boost (step-up) operation is enabled by the Z-source network. Compared to converter topologies with a boost-type dc-dc converter in the intermediate link or a boost-type active front-end, no additional power transistors or boost inductors are required apart from the components for the Z-source. The passive components of the B6-ZSI can be minimized for general purpose applications, as described in [68], and a mains under-voltage of approximately 25% can be compensated.

Compared to the conventional VSI that typically is either in the active-state (link current is equal to one of the output phase currents) or zero-state (link current is zero), for the ZSI there is a third state often termed as "shoot-through" state. During the shoot-through state the input diodes are not conducting and the diode rectifier is disconnected

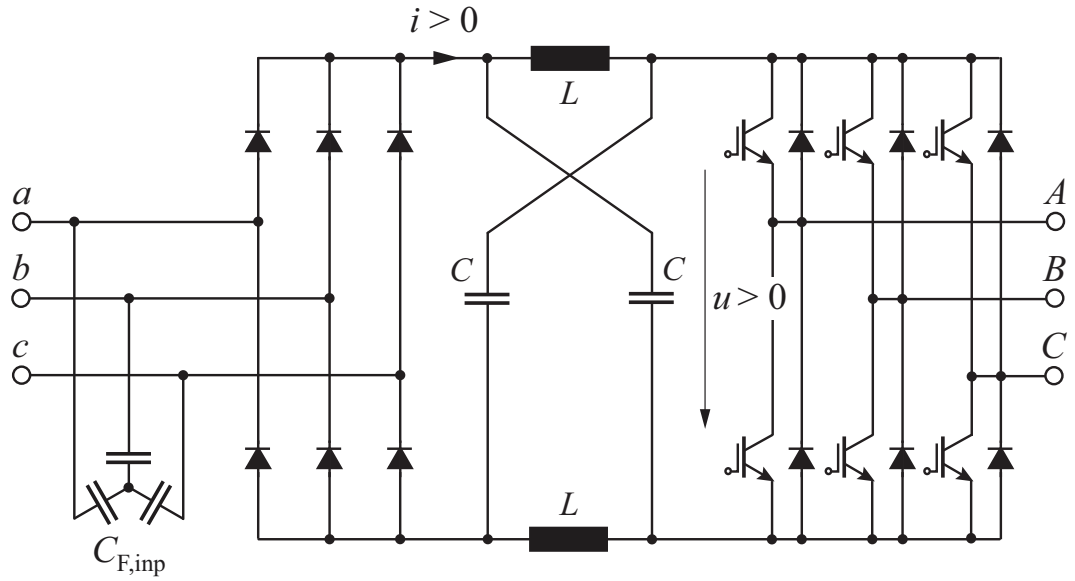


Fig. 1.8: Diode bridge rectifier with Z-Source Inverter (B6-ZSI).

from the Z-source. The shoot-through state is used every switching cycle during the zero-state period generated by the PWM modulation scheme, in order to enable voltage step-up functionality. The duration of the shoot-through interval depends on the desired voltage step-up ratio. A simple modulation scheme for the ZSI is proposed in [69]. More sophisticated PWM schemes can be found in [70, 71]. Similar to the converters with current-source-type input stages, the B6-ZSI requires impressed voltages at the input and thus input capacitors $C_{\mathrm{F,inp}}$.

If regenerative operation is required, the unidirectional B6-ZSI can be extended by adding anti-parallel power transistors to the rectifier diodes. This results in the bidirectional Z-Source Converter (ZSC) [72], depicted in Fig. 1.9. Regarding its semiconductor configuration, the ZSC is identical to the VSBBC. The inverter of the ZSC is operated without shoot-through states, using only active and freewheeling states. Together with the motor inductances, the inverter acts as a boost converter. In order to feed energy back into the mains, the Z-source is connected to the mains by two transistors, which is referred to in [68] as "shoot-back state".

To summarize, according to [73] the Z-source concept has several advantages, such as a variable input-to-output voltage transfer ratio enabling a better usage of a motor load at mains under-voltage, reduced inrush and harmonic currents, and ride-through operation capability. However, if the ZSC should offer the same flexibility regarding its sup-

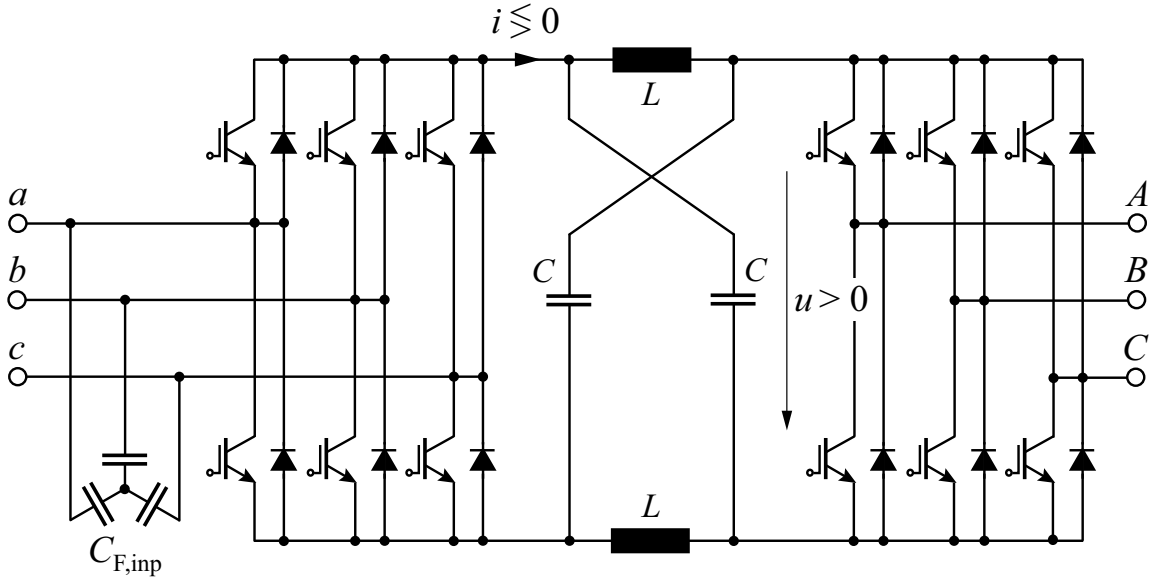


Fig. 1.9: Z-Source Converter (ZSC).

ply voltage range as the B6-VSI with a maximum line-to-line voltage of typically 530 V ($460V + 15\%$) and more, for its inverter stage semiconductors with a blocking voltage higher than 1200 V are necessary. In standard Si technology this would mean that IGBTs with a blocking voltage of 1600 V or 1700 V must be utilized. The aforementioned expected increase in efficiency at mains under-voltage of the overall ZSI drive is then affected by an increase of the semiconductor losses due to their higher blocking voltage.

Compared to the previously presented VSBBC and CSBBC, the Z-source topology is comparatively new. One of the first publications, detailing the B6-ZSI with its operating modes, is [69] and dates back to 2003. Since then, researchers have been analyzing various ZSC related aspects. A particular focus has been on proper dimensioning [68, 74], modulation [75, 76], control of different operating modes [71, 77], and on application specific research [73, 78, 79].

Alternative implementation variants of the *LC* Z-source network are so-called T-source networks, more recently suggested in [80]. According to [80], the Z-source circuit can be replaced by a T-source structure, as shown in Fig. 1.10, leading to a T-Source Inverter (TSI) with a passive diode rectifier front-end similar to the B6-ZSI. Compared to the Z-source, the T-source network utilizes coupled inductors, which are equivalent to non-galvanically isolated transformers (auto-transformers).

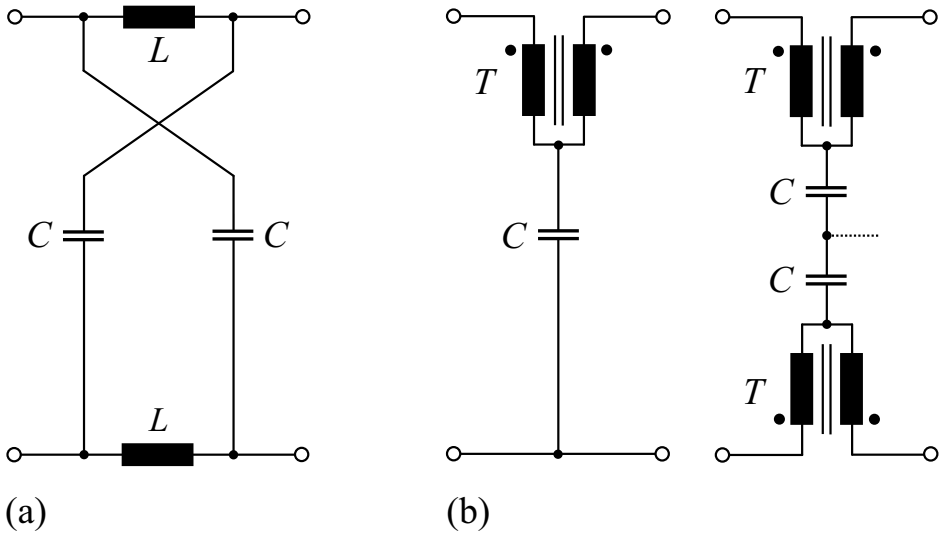


Fig. 1.10: (a) Z-source and **(b)** alternative asymmetrical and symmetrical T-source network.

Fundamental Frequency Front-End Converter

With the goal of ever increasing power density and reliability, efforts have been made in finding converter concepts that allow for three-phase ac-ac conversion without any intermediate energy storage element. The physical basis of such converter systems is provided by the constant instantaneous power generated by a symmetrical three-phase mains system which allows delivery of constant electrical power to the load without energy storage elements in the power circuit.

A converter topology, where the dc-link capacitor is omitted, or differently considered, is implemented with the filter capacitors on the mains side, is the Fundamental Frequency Front-End Converter (F3EC), depicted in Fig. 1.11. This topology was suggested in [81] and analyzed in more detail in [82, 83]. Due to the absence of an intermediate energy storage, the F3EC should hence also be considered as a MC.

The power circuit of the F3EC is identical to the VSBBC apart from the missing dc-link capacitor and the different configuration of the input filtering elements. With the absence of the dc-link capacitor, a limiting component regarding converter operating temperature and lifetime is omitted. The input stage of the F3EC is operated as a synchronous

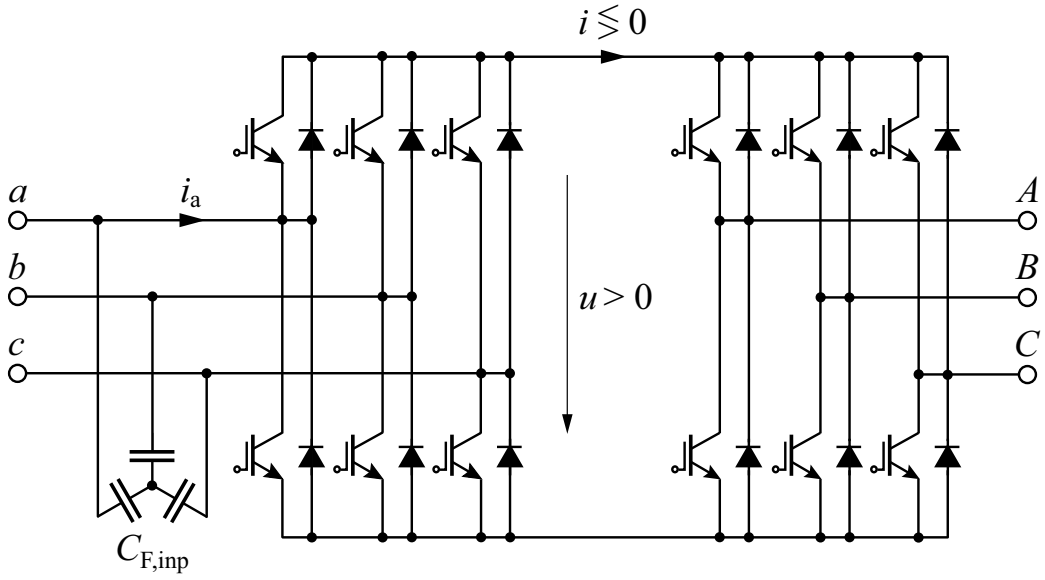


Fig. 1.11: Indirect ac-ac converter with a voltage link without energy storage, known as Fundamental Frequency Front-End Converter (F3EC).

three-phase rectifier. Its conduction state is directly defined by the mains voltage and cannot be influenced by modulation. The load current segments, generated by the VSI output stage, are supplied by the input capacitors through the input stage diodes with the highest line-to-line voltage across them. As the impressed load current segments are directly fed to the converter input, a voltage impressed input is required, which is provided by the input filter capacitors $C_{\mathrm{F,inp}}$. This explains the earlier statement, that the F3EC topology can be considered as a VSBBC with its dc-link energy storage placed on the input side.

The power transistors of the input stage are turned on and off in synchronization with the frequency of the mains voltage. Consequently, the switching frequency of the input stage transistors equals the mains frequency. This fact has given the name to this topology. In order to avoid mains phase short-circuits, only the switches that are connected in anti-parallel to a conducting diode might be turned on. Thus, the input stage transistors do not actively influence the formation of the link voltage; they solely permit a link current reversal.

Negative link currents occur for output current-to-voltage displacement angles $\Phi_2 > \pi/6$, or when the converter is operated in regeneration (generator) mode. The switching transitions of the input stage power transistors occur at the zero-crossing of the corresponding line-to-line voltages. Compared to conventional converter topologies with dc-link energy storage, the switching losses of the input stage of the F3EC are negligible. This results in higher energy conversion efficiency. Theoretically, no brake chopper in the link is required as the F3EC enables energy feedback into the mains. For a practical drive system, however, the bidirectional power flow capability rather allows for downsizing than omitting the brake chopper circuit in order to enable braking of the motor also in case of mains failures.

The variation of the link voltage with six times the mains frequency, defined by the envelope of the line-to-line mains voltages according to Fig. 1.12, represents a fundamental disadvantage of the F3EC topology. The minimum link voltage is equal to

$$u_{\min} = \frac{3}{2}\hat{U}_1 \tag{1.1}$$

and limits the maximum amplitude of the output voltage to

$$\hat{U}_{2,\max} = \frac{2}{3}\frac{\sqrt{3}}{2}u_{\min} = \frac{\sqrt{3}}{2}\hat{U}_1 = 0.866\,\hat{U}_1\,, \tag{1.2}$$

when operated with sinusoidal modulation. Later, we will find the same input-to-output voltage transfer ratio for the matrix converters.

For a constant power transfer between mains and load, a variation of the local mean value of the link current occurs that is inversely proportional to the variation of the link voltage that follows a six-pulse pattern. This means that for calculating the modulation function of the VSI output stage, the link voltage needs to be measured. This variation is compensated by adaptation of the output stage modulation index in order to provide a constant fundamental output voltage amplitude. Only six (discrete) input current space vectors are possible (cf. Sec. 3.1.4), which change with mains frequency, as the front-end is switched with the mains frequency. Therefore, the input currents resulting after low-pass filtering (input filter capacitors $C_{\mathrm{F,inp}}$ in combination with input filter inductors and mains inductance) are block-shaped as shown in Fig. 1.12. The variation of the link current appears always in the two input phases conducting the load current. Despite this, the F3EC exhibits a relatively high power factor of $\lambda \approx 0.95$. However, the (low frequency) harmonic content of the input currents is comparatively high because of the $\pi/3$-wide intervals with zero phase current.

Although the F3EC generates less mains current harmonics than a conventional B6-VSI (cf. Fig. 1.5) with passive diode rectifier front-end, it shows a higher harmonic current distortion as the VSBBC or CSBBC, and therefore is limited to applications, where such distortion levels are tolerable.

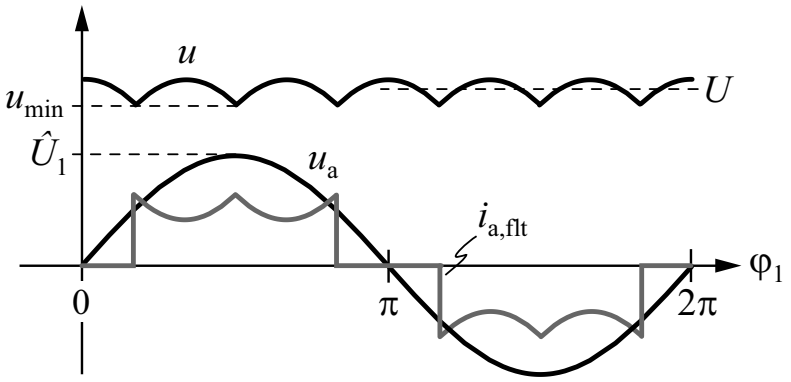


Fig. 1.12: Waveform of the link voltage u, the average link voltage U, the mains phase voltage u_{a}, and the filtered mains input current $i_{\mathrm{a,flt}}$ for motor operation.

Matrix Converter

Ac-ac converter topologies without any energy storage in the intermediate link are referred to as Matrix Converters (MCs). They can provide simultaneous amplitude and frequency transformation of three-phase voltage-current systems.

The Conventional (direct) Matrix Converter (CMC, Fig. 1.13(a)) performs the voltage and current conversion in one semiconductor stage. Alternatively, the Indirect Matrix Converter (IMC, Fig. 1.13(b)) topology features a two-stage (indirect) power conversion. In the IMC circuit separate stages are provided for the current and voltage conversion similar to the VSBBC and the CSBBC. However, no energy storage element is implemented in the intermediate link.

By definition, the F3EC is also a MC, but without Power Factor Corrector (PFC) functionality at the input. In the following, the derivation of the IMC is summarized based on the F3EC, as suggested in [84]. In order to enable sinusoidal input currents, the F3EC topology in Fig. 1.11 has to be modified such that the conduction state of the converter input stage can be directly controlled by modulation and is not anymore determined by the largest mains line-to-line input voltage. The anti-parallel transistor-diode configuration in the input stage of the F3EC has to be extended such that bidirectional current flow and current blocking and bipolar voltage blocking are enabled. This requires a transistor in series with each diode (e.g. S_{ap} in series with D_{ap}, cf. Fig. 1.14), and a diode must be place in series with each transistor (e.g. D_{pa} in series with S_{pa}, cf. Fig. 1.14). This finally leads to the Indirect Matrix Converter (IMC) topology. The resulting transistor-diode configuration of the input stage of the IMC with two transistors and two diodes is known as a four-quadrant switch or a bidirectional switch. The current paths between the series connected transistor and diode can be interconnected as shown in Fig. 1.14.

Considering the VSBBC and CSBBC, the IMC consists of an input stage, formed by two anti-parallel CSRs, which is connected without any intermediate energy storage to a VSI output stage. From this topological view, it is immediately clear that for bidirectional power flow the IMC requires a CSR input stage with four quadrant switches, which is equivalent to two anti-parallel CSRs, due to the VSI output stage where only positive link voltages u are allowed. To summarize, the IMC is a combination of the CSR and VSI topology.

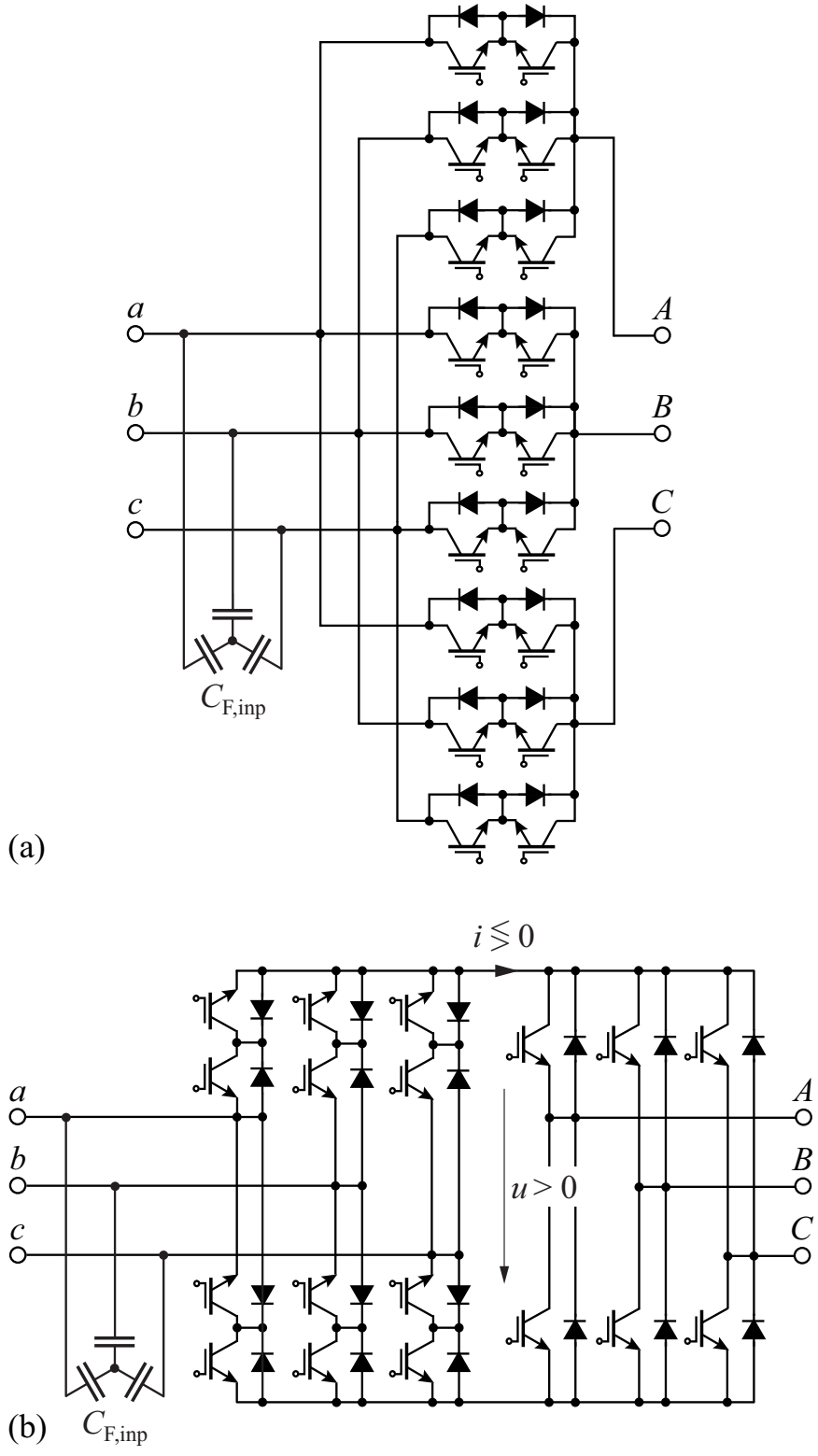


Fig. 1.13: (a) Conventional (direct) Matrix Converter (CMC) and **(b)** Indirect Matrix Converter (IMC).

The IMC requires capacitors at the converter input to provide impressed voltages similar to the CSBBC. The impressed dc-link current, which is required by the CSR input stage of the IMC, is generated by switching the impressed load current with the VSI output stage to the link of the IMC. The same current and voltage transfer also occurs in the CMC but without a physically implemented link. Consequently, for MCs the voltage transformation from the input to the output occurs simultaneously with the current transformation from the output to the input; however, in contrast to the VSBBC or CSBBC there is no intermediate energy storage.

Regarding their basic functionality both MC topologies are equivalent. Their different physical implementation merely results in different operating characteristics, which are going to be addressed in this work. Compared to the previously considered two-level VSBBC or CSBBC, MCs are inherently quasi three-level converters as all three line-to-line input voltages can be switched to the converter output terminals. The term "quasi three-level" is used as the three voltage levels constantly change with the phase of the input current.

Due to the absence of an intermediate energy storage, MCs are often termed as "all-Si" ac-ac converters. However, in order to avoid misun-

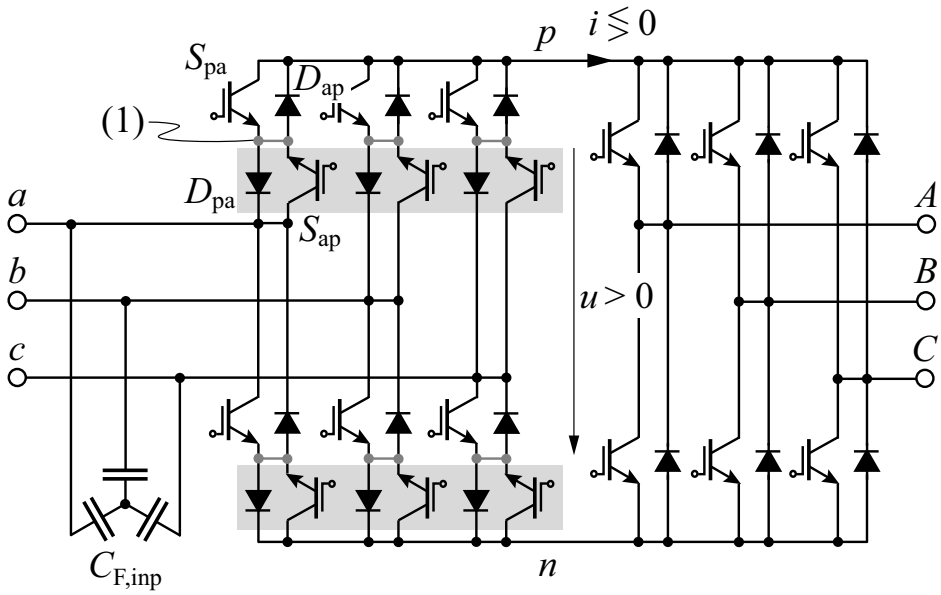


Fig. 1.14: Derivation of the IMC topology by extending the F3EC topology. The components added to the F3EC topology are shown on gray background. (1) Optional connection between IGBT and diode.

derstanding, it should be pointed out that also MCs require reactive components for a practical implementation. Those include the input capacitors to provide a voltage impressed input and additional passive components for the input filter to meet the EMC standards. From this perspective, it could be stated that in MCs the intermediate energy storage has been shifted to the converter input filter and/or to the load!

The advantages often claimed for the matrix converter are listed below:

- MCs offer a potential for a compact and light weight implementation due to the absence of intermediate storage elements.
- Compared with the VSBBC, no dc-link capacitor is required for MCs, which could limit the lifetime of the converter due to thermal aging if implemented with electrolytic capacitors.
- MCs in general feature a lower dependency of their overall semiconductor losses on the switching frequency compared with standard converter concepts. This allows (with current semiconductor technologies) for an increased converter efficiency if higher switching frequencies ($> 20\,\mathrm{kHz}$) are needed. However, it should be noted that MCs also require more semiconductor devices.
- The dc control equivalent of a MC is a buck-type dc-dc converter without any intermediate energy storage. The output inductor of the buck converter corresponds to the stator inductance of the motor. This allows the MC to supply a passive RL load or an induction machine without any feedback control.

The main disadvantages of the MC concept are as follows:

- As inherently given by the topology, MCs can only provide output voltage amplitudes lower than the input voltage (buck operation). Their stationary intrinsic maximum input-to-output voltage transfer ratio (for sinusoidal modulation) is limited to $\sqrt{3}/2 \approx 86.6\%$ similar to the F3EC.
- It is often stated that for MC drive systems no standard machines can be utilized due to the limited output voltage. This is definitely true for standard IEC Induction Motors (IMs), developed to be supplied directly from the mains. However, mod-

ern permanent magnet synchronous motors (PMSMs) are typically designed for operation with a B6-VSI with a nominal dc-link voltage which corresponds approximately to the line-to-line input voltage of MCs. This is one explanation of why several standard PMSMs can be found that match well with the output voltage range of MCs as long as reduced performance is tolerable during mains under-voltage. An optimal matching of the motor voltage and converter output voltage is essential for best overall drive performance, which then involves a custom motor design for MCs.

- Abrupt changes in the load torque are directly transferred to the converter input as a result of the missing intermediate energy storage. This demands a careful design of the MC input filter, and might even restrict the application area of MCs.

CMC and IMC topologies require in their basic configuration 18 power transistors and 18 diodes as shown in Fig. 1.13. For the CMC, the implementation with 18 Reverse Blocking IGBTs (RB-IGBTs) is favored due to low conduction losses. The corresponding semiconductor configuration for the IMC requires 12 RB-IGBTs for the input stage and 6 Reverse Conducting IGBTs (RC-IGBTs) for the output stage. An alternative implementation variant for the IMC with 9 single half-bridge modules is presented in Fig. 1.15.

The world's first commercial MC was presented by the Japanese drive manufacturer Yaskawa in 2005 with the product name Varispeed AC. This converter series is based on the CMC topology and is implemented with 1200 V RB-IGBTs produced by Fuji Electric. According to Yaskawa, typical applications for their MC result from two main advantages of their product: power regeneration functionality and low total harmonic distortion ($< 8\%$). Both characteristics should contribute to reasonable application in roller dynamometer test benches of the automotive industry, gear box test benches, elevators, escalators, cranes, or centrifuges.

One year later in 2006, Fuji Electric, another Japanese company, announced also a new MC product, the FRENIC-MX with an output power of 45 kW. Similar to Yaskawa, Fuji also selected the CMC topology. Since the product launch, Fuji has not been heavily advertising their MC. Currently, the FRENIC-MX series seems to be not longer part of Fuji's official product portfolio.

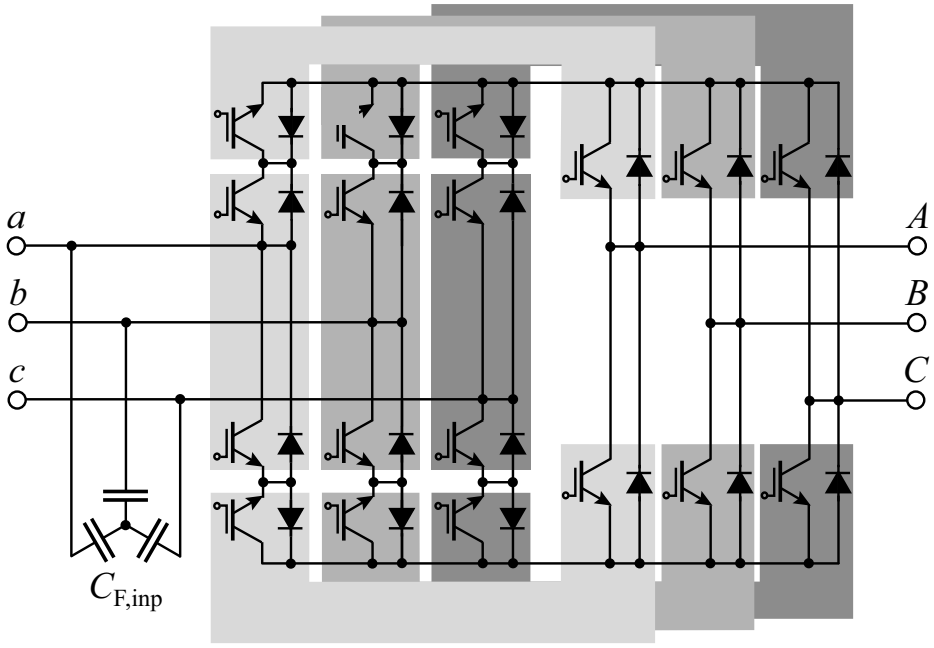


Fig. 1.15: IMC implemented with nine half-bridge modules.

Meanwhile, Yaskawa extended their matrix converter product line with the FSDrive-MX1S medium voltage MC series for input voltages of 3.3 kV and 6.6 kV with a maximum output power of 2.5 MW and 5 MW. The increased blocking voltage capability is achieved through a modular interconnection of multiple three-phase CMCs, leading to a poly-phase matrix converter, which is connected to the three-phase medium voltage mains and optionally also to the load with multi-pulse transformers.

MCs are frequently considered as a future converter concept for VSDs or more recently for aircraft or renewable energy applications. However, despite intensive research for the last three decades, MCs have until now only achieved low market penetration. The reason for this might be, apart from technical limitations (e.g. no voltage step-up capability), the more elaborate design procedure and the more complex cascaded modulation scheme compared to converters with dc-link energy storage.

Nevertheless, in the academic community, research on the MC and its modified topologies is still very popular, given the number of papers published in this topic area and the numerous technical sessions held at conferences about MCs. The following compilation provides a brief overview of the development of MCs and then presents the main topological variations.

Already in 1923, Hazeltine Research Corporation filed a patent [85] for a matrix type power converter based on electro-mechanical switches. The forced commutated CMC, as depicted in Fig. 1.13(a), evolved out of the line commutated Cyclo-Converters, and was proposed in the 1970' for example by [86, 87]. During its process of development, it has therefore also been referred to as a forced-commutated Cyclo-Converter. The modern pulse-width modulated CMC was first described in [88, 89] at the beginning of the 1980'. Approximately eight years later, first international publications [90, 91] appeared, investigating the IMC topology. For the following years, academic research mainly focused on the CMC topology.

The next big step with regard to the further development of MC topologies occurred in 2001 with the invention of the reduced switch IMC topologies known as Sparse Matrix Converters (SMCs) [92–94]. Since then, numerous topological extensions or combinations of the basic CMC and IMC topology have been suggested such as: the Indirect Three-Level (Sparse) Matrix Converter topologies [84, 92, 95, 96] to reduce the output current harmonics, the full-bridge IMC topology for supplying an open winding ac machine with a limited common-mode voltage [97], or different Hybrid CMC (HCMC) or IMC (HIMC) topologies [98–100] to extend the output voltage range. Unfortunately, the extended functionality is mostly achieved at the expense of a higher hardware implementation effort and an even more complex modulation and control scheme, compared to the already demanding modulation and control of the basic CMC topology with 18 transistors and 18 diodes.

Besides the investigation of MC topologies, different aspects related to the MC concept have been analyzed. The following overview aims at identifying and summarizing the main research areas of MCs.

In order to enable proper operation of the MC, the application of adequate modulation schemes, which allow for safe commutation, is essential. This is of particular importance for the CMC topology as the commutation sequence depends in general on the sign of the commutation voltage and/or the sign of the current. Therefore, research activities focused on the analysis and development of modulation schemes for the CMC [101–115].

The change of the switching state of the CMC must be executed considering the input voltage and the output current in order to avoid failures. This generally requires a multi-step commutation strategy. Suit-

able commutation schemes were first described in [103, 116]. The standard commutation scheme requires four steps. Depending on the switching states and the actual input voltages and output currents the four-step commutation scheme can be reduced to a three-, a two-, or even a one-step commutation scheme [117–119]. In order to further increase commutation safety, intelligent gate drive circuits, specifically designed for the CMC, were suggested [120, 121] that measure the voltage across the transistor in order to detect the direction of the current.

The modulation scheme of the IMC [122–131] is significantly less critical and complex compared with the CMC and offers enough degrees-of-freedom to enhance functionality. As is shown in Chap. 3, the IMC topology allows for either zero current switching of the input stage or zero voltage switching of the output stage. Two of the most important findings of research on modulation schemes for the IMC are the basic space vector representation of the IMC modulation [122] and the reactive power transfer modulation scheme [128], which can be also applied to CMCs.

The lack of a dc-link energy storage element affects the operational safety of MCs in case of failures as for example over-voltages cannot be limited by a dc-link capacitor as in the VSBBC, and no additional return path for the load current is provided. The investigation of protection and clamping circuits and their control schemes was important for the practical application of MCs [132–137]. Regarding protection circuitry, the IMC features a topological advantage compared to the CMC. The link and therefore also the converter output terminals of the IMC can be clamped to a defined voltage (e.g. via a capacitor supplied by the mains with a three-phase diode rectifier) with only two additional diodes, compared to six additional diodes required the output terminals of the CMC.

In order to prove the concept of MCs in practical systems, numerous application specific research projects have been conducted until now, starting with the investigation of ac motor drives supplied by CMCs [90, 138, 139] or IMCs [140–143]. The drive system integration capability of MCs was demonstrated by attaching a CMC directly to a motor leading to the so-called Matrix Converter Motor (MCM) [144, 145]. Motivated by their expected potential for a light weight and compact implementation, MCs have been widely analyzed for aerospace applications [146–149] and are still considered as a alternative converter concept for MEA. More recent investigations suggested the MC also for wind-

Fig. 1.16: Former (light gray) and present (dark gray) countries, with considerable research activities on MC.

turbine generator systems [150, 151], micro-turbine based distributed generation systems [152], drive systems for locomotives [153], deep-sea robots [154], contact-less energy transmission [155], direct interfaces for ac and dc supplies for fuel cell and battery applications [156], or ac utility power units [157].

Another field of study was the investigation of semiconductor losses. Simulation based as well as analytical calculation based methods, using approximated loss data were suggested for calculating the semiconductor losses of the CMC [158–160]. A systematic method for an analytically closed calculation of semiconductor losses for the IMC and SMC topologies was first presented in [92, 161] and was later extended to the CMC topology [162]. Additionally, different semiconductor technologies have been compared for MCs such as the RB-IGBT technology [163–167], the SiC switch technology [168–170], or integrated four-quadrant switches, known as Monolytic Bidirectional Switch (MBS) [171, 172].

Most of the motor control schemes, known from motor drives supplied with voltage source converters, were applied and analyzed for MCs: Direct Torque Control (DTC) [173–175], sliding mode control [176], dead

Index	*University*	*Country*
1	University of Bologna	Italy
	University of Milan	
2	Concordia University, Montreal	Canada
	University of Toronto	
3	University of Colorado at Boulder	USA
	University of Minnesota	
	University of Wisconsin-Madison	
	Virginia Polytechnic Institute	
4	Kagoshima University	Japan
	Nagaoka University of Technology	
	Nagoya University	
	Nagasaki University	
5	RWTH Aachen University	Germany
	University of Braunschweig	
	University of Karlsruhe (TH)	
	Technical University Chemnitz	
6	University of Concepcion	Chile
7	University of Bradford	UK
	University of Manchester	
	University of Nottingham	
8	"Polytechnica" University of Timisoara	Romania
9	Aalborg University	Denmark
10	University of Tampere	Finland
11	EPFL Lausanne	Switzerland
	ETH Zurich[a]	

[a]Presumably demonstrated the first All-SiC CMC and All-SiC IMC

Tab. 1.2: Former and present countries and their universities with considerable research activities on MCs. (The countries are sorted chronologically with respect to the beginning of the research activities, whereas the universities are listed alphabetically.)

Company	*MC Topology*	*Year*	*Publication*
ABB & Daimler Benz	CMC	1997	[186]
ABB	CMC	2002	[187]
	CMC	2008	[188]
Alstom	CMC	2003	[189]
	PP-MC[a]	2009	[190]
Bosch	SAX	2004	[191]
Danfoss	CMC	2002	[192]
Fuji Electric	CMC	2004	[193]
Hitachi Electric	CMC	2006	[194]
Mitsubishi Electric	CMC	2004	[195]
Rockwell Automation	CMC	2002	[196]
	CMC	2008	[197]
Siemens	CMC	2002	[198]
Smith Aerospace	CMC	2004	[199]
Toyo Electric	CMC	2007	[200]
Westinghouse	CMC	1992	[201]
Yaskawa	CMC	2002	[202]
	ARCP-MC[b]	2009	[203]

[a] Poly-Phase Matrix Converter

[b] Auxiliary Resonant Commutated Pole Matrix Converter

Tab. 1.3: Compilation of publicly reported research on MCs in industry. Currently, only Yaskawa offers MCs in their product portfolio.

beat control [177], sensorless control [178–180], and Model Predictive Control (MPC) [181, 182]. A rather special control scheme is the regeneration control [183], avoiding energy feedback into the mains for (bidirectional) CMCs as is currently required for MEA applications. Another control related topic was the analysis of methods [184, 185] to investigate control stability of MCs.

A brief overview of the worldwide academic and industrial activities in the topic area of MCs is provided due to its importance in the academic community. Fig. 1.16 depicts the worldwide research activities on MCs

with the legend in Tab. 1.2, listing the corresponding universities. The main academic MC research centers are located in Europe, Japan, and the USA (sorted in alphabetical order) as can be seen in Fig. 1.16.

Through evaluation of publications and technical literature, drive manufacturers are identified that have performed research on MCs and publicly reported on their results. A summary of this evaluation is provided in Tab. 1.3, showing that numerous companies sponsored or performed investigations on MCs or still have activities in this topic area. Nevertheless, only a few launched a MC as a product.

Reduced Matrix Converter – S-A-X Converter

Reducing the implementation effort of ac-ac converter topologies is well known from voltage dc-link converter systems. If bidirectional operation is not required, the input switches of the VSBBC can be omitted, leading to the B6-VSI topology, which is widely used in industry. The same

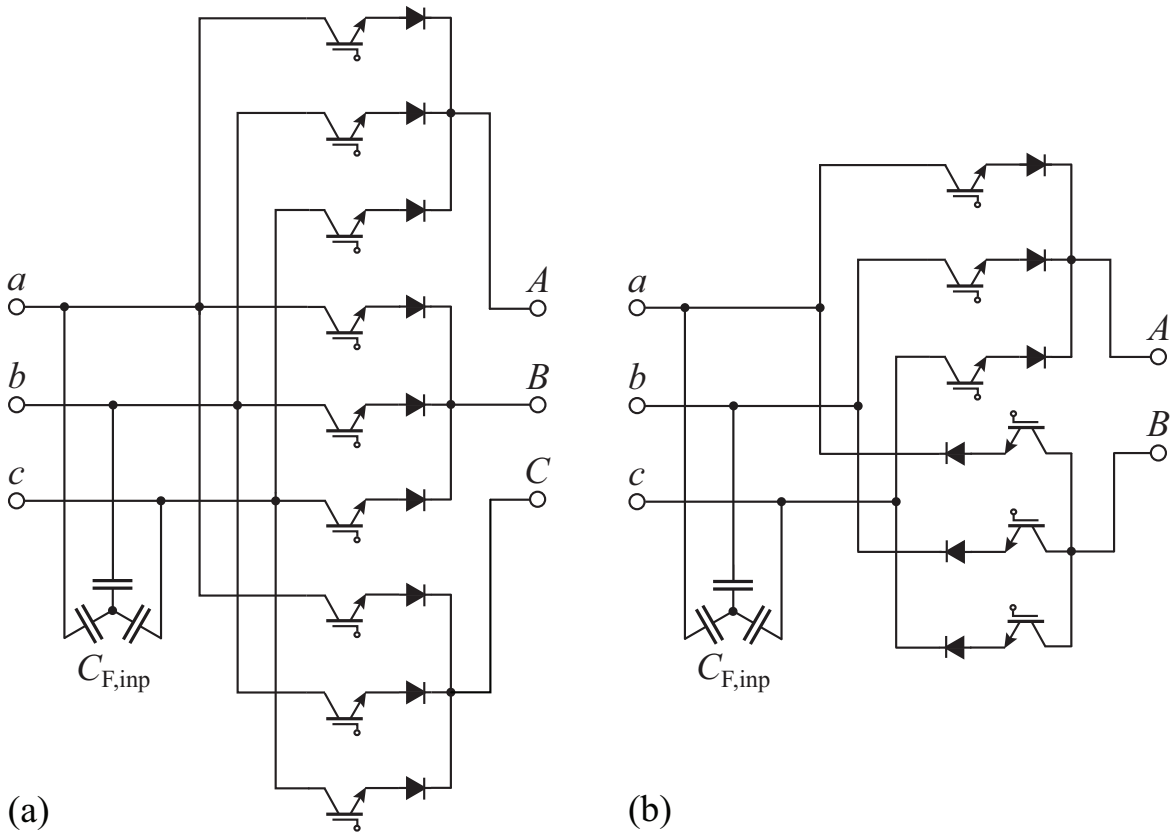


Fig. 1.17: S-A-X Converter topologies. Circuit variant with **(a)** 9 switches (3×3) and **(b)** 6 switches (3×2).

concept can be applied to MCs. The CMC topology can be simplified and restricted to unidirectional operation, by omission of the reverse current path. Possible circuit topologies are shown in Fig. 1.17 and referred to as S-A-X converters [191]. The number of semiconductor components can then be reduced to 6 power transistors and 6 diodes (or 6 RB-IGBTs) compared to 18 power transistors and 18 diodes (or 18 RB-IGBTs) as for the CMC.

The main motivation for reduced CMCs, besides minimizing the implementation effort, is to enable a simplified, rectifier-based one-step commutation scheme. This allows the current to commutate immediately without a special sequence, which is typically required for the CMC. In addition, due to the missing reverse current path and the unidirectional, strictly positive output currents, the input phases of the S-A-X converter cannot be short-circuited as is possible for the CMC.

Two operating modes are known for the S-A-X converter topology in Fig. 1.17(a) with nine switches and nine diodes (3×3). The first mode allows the generation of a three-phase voltage-current system at the converter output with a dc-offset in the output currents as no reverse current flow is possible. In order to drive a standard three-phase motor, decoupling of the ac- and dc-components is required. This can be achieved by means of a transformer, which is connected between the converter output and the motor. The primary windings of the transformer are supplied by the converter output, and their star-point is connected to the star-point of the input capacitors $C_{\mathrm{F,inp}}$. Another possibility is to utilize motors with special winding configurations that compensate the stator field components, generated by the dc-offset in the phase currents.

The S-A-X converter topology, shown in Fig. 1.17(b), features three input phases and two output phases (3×2), with three series connected switch-diode configurations in the forward current leg and three in the reverse current leg. This S-A-X converter topology corresponds to the circuit topology of the CSR in which the dc-link inductance is shifted to the load. Two load terminals are connected to the two output phases of the S-A-X converter for supplying a symmetrical three-phase load, whereas the third load terminal is connected to the mains star-point. The switches are modulated such that a sinusoidal current with dc-offset results. Compared to the topology with nine switches and nine diodes (cf. Fig. 1.17(a)), this topology has lower conduction losses and does not cause a dc-loading of the input mains system.

Depending on the implementation variant (3×3 or 3×2), S-A-X converters have been suggested for drives requiring an isolation transformer, for decentralized drive systems, or for contactless energy transmission [204]. However, the handling of all operating and failure modes of such a drive systems seems to be very challenging as the S-A-X converter concept imposes many restrictions.

Sparse Matrix Converter

The input stage of the IMC, as illustrated in Fig. 1.14, is implemented with six four-quadrant switches and can be operated with a positive and negative link voltage. For the six-switch inverter output stage, however, a positive link voltage $u > 0$ is mandatory due to the freewheeling diodes in the output stage (cf. Fig. 1.14). Since only positive link voltages are tolerable for the IMC topology, it is obvious to aim for simplification of the IMC input stage by restricting its voltage blocking capability to positive link voltages.

The derivation of a simplified input stage bridge-leg of the IMC is shown in Fig. 1.18. If the input phase a of the IMC is connected for both

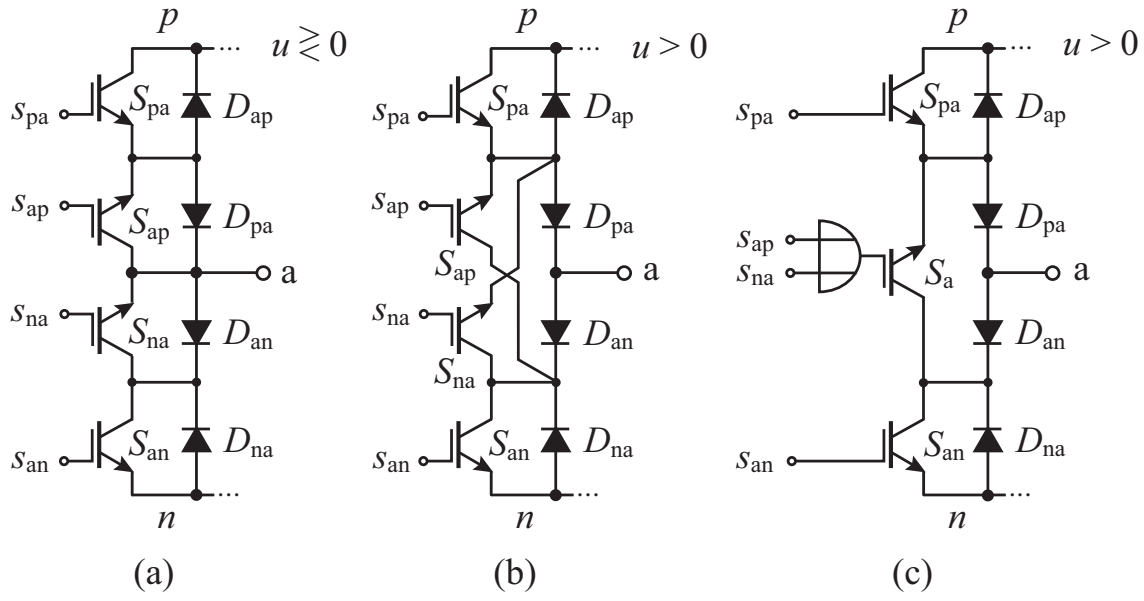


Fig. 1.18: Derivation of the SMC input stage bridge-leg [92]. **(a)** Typical IMC bridge-leg with bipolar voltage blocking capability ($u > 0$, $u < 0$), **(b)** simplified bridge-leg with restricted voltage blocking capability to positive link voltages ($u > 0$), and **(c)** SMC bridge-leg.

current directions with the positive bus p (S_{ap} and S_{pa} are switched-on and S_{an} and S_{na} are switched-off), the positive link voltage always appears as a blocking voltage across S_{an}. Thus, the function of S_{na} is limited to providing a current path from the negative bus n via D_{na} to the input phase a. For this reason, no direct connection of the emitter of S_{na} with a is required. The current return path can be provided via S_{na} and D_{pa}. An analogous consideration for S_{ap} and D_{an} leads to the parallel connection of S_{ap} and S_{na} as shown in Fig. 1.18(b). This parallel switch configuration can be replaced by a single switch S_{a}, depicted in Fig. 1.18(c), resulting in a simplified bridge-leg configuration for the input stage with three instead of four switches. The gate of S_{a} is controlled by a "wired-OR" connection of the gate signals for S_{ap} and S_{na} and consequently means for a practical implementation that S_{a} is switched-on whenever S_{pa} or S_{an} are switched-on. The simplified bridge-leg configuration in Fig. 1.18(c) thus enables a reduced implementation effort of the IMC from 18 switches and 18 diodes to 15 switches and 18 diodes.

The resulting reduced-switch IMC, shown in Fig. 1.19, is called Sparse Matrix Converter (SMC) [92, 205]. (It should be noted that despite reducing the number of switches, only a small reduction of the required semiconductor chip area can be expected for the SMC, compared to the standard IMC topology with 18 switches, as the switch S_{a} requires

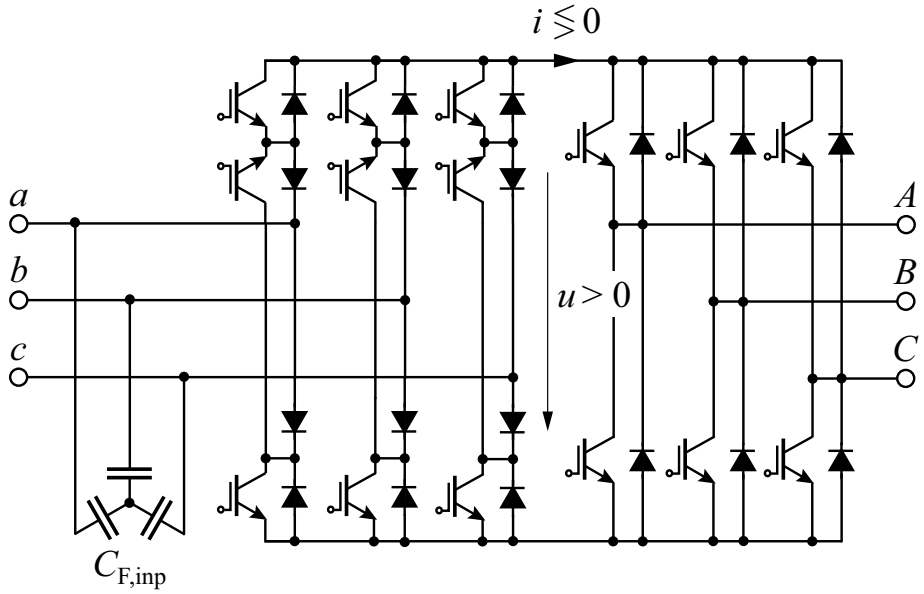


Fig. 1.19: Sparse Matrix Converter (SMC) [92].

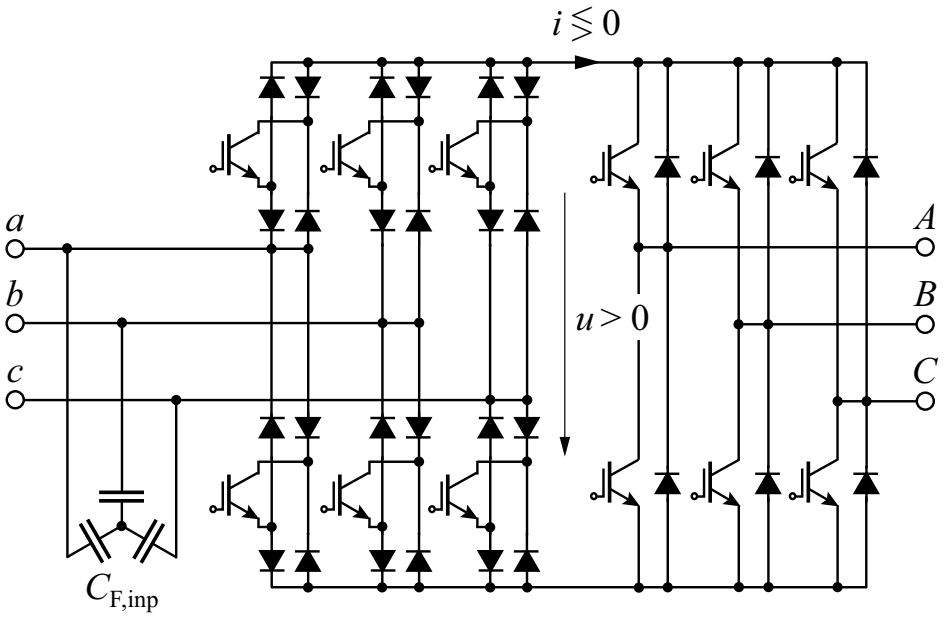


Fig. 1.20: Very Sparse Matrix Converter (VSMC).

approximately twice the current rating compared to the switches S_{ap} and S_{na}.) Depending on the current direction and the switching state either two or three devices are in the current path of an SMC input bridge-leg. The SMC typically has higher conduction losses compared with the standard IMC topology for similarly designed input stages, as per input stage bridge-leg of the SMC more than two devices are in the current path.

A further reduction of the number of transistors in the input stage is possible by implementing the four-quadrant switches with only a single switch and four diodes (Graetz configuration). This leads to another fully bidirectional variant of the IMC topology, the Very Sparse Matrix Converter (VSMC), shown in Fig. 1.20. Its four-quadrant switches cannot be controlled independently with respect to the current direction. However, this controllability is not required, when using the standard modulation scheme A (cf. Fig. 3.9). The switching of the transistors of the input stage then takes place at zero current within the freewheeling intervals of the output stage. Thus, only a safety interval is required between the turn-off of a four-quadrant switch and the turn-on of another four-quadrant switch. Compared to the IMC with 18 switches, in the input stage of the VSMC three instead of two devices are in the current path of a four-quadrant switch (per phase), which leads to higher conduction losses for the VSMC topology.

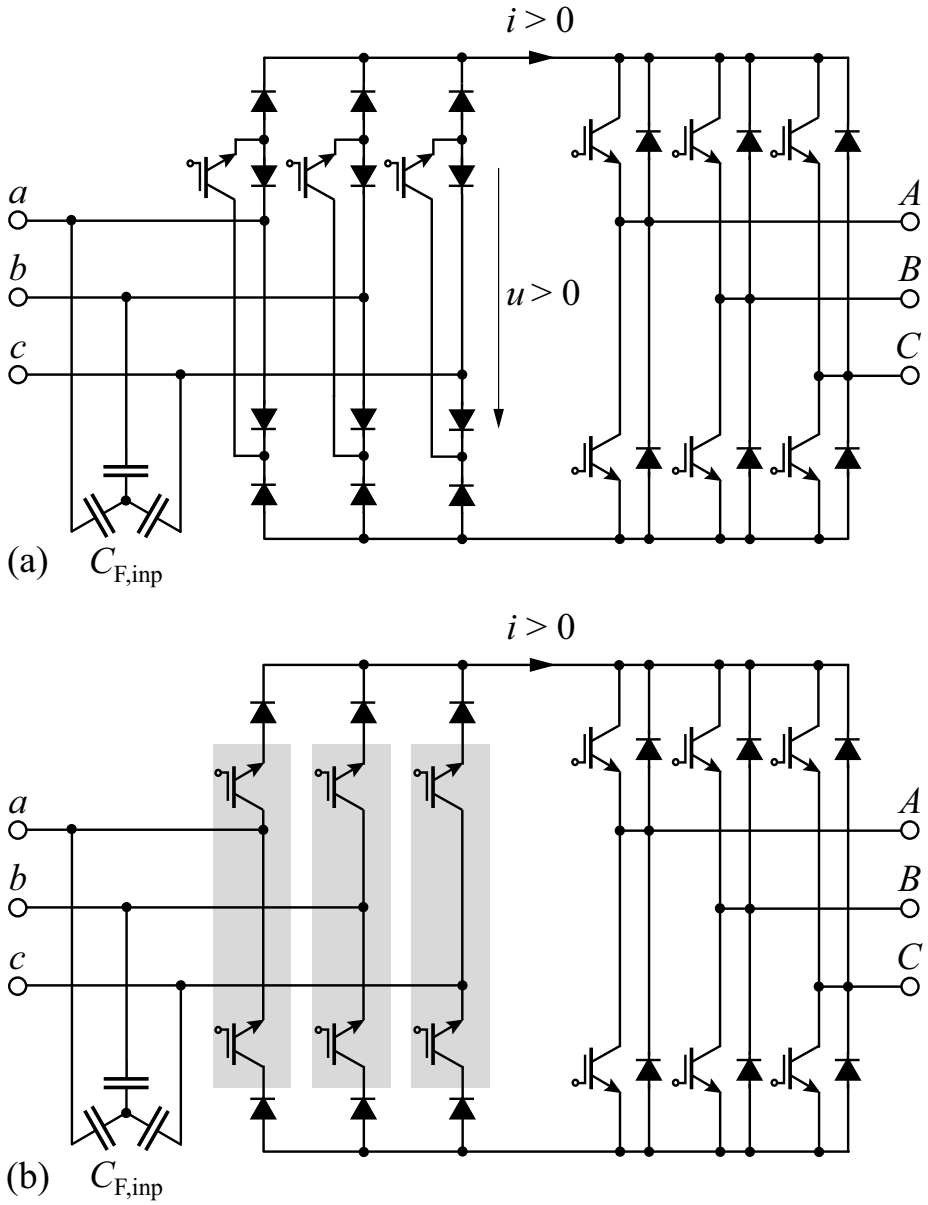


Fig. 1.21: Unidirectional Ultra Sparse Matrix Converter (USMC) with **(a)** 3 transistors and 12 diodes and **(b)** 6 transistors (three half-bridges, on gray background) and 6 diodes in the input stage.

A more comprehensive simplification of the IMC topology is possible by limiting the converter to unidirectional power flow. The switches S_{an} and S_{pa} according to Fig. 1.18(c) only conduct current for negative link currents $i < 0$ and thus can be omitted when connected to passive, mainly ohmic RL loads. The resulting topology is the Ultra Sparse Matrix Converter (USMC) [92], depicted in Fig. 1.21(a). Negative link voltages as well as negative link currents have to be avoided for the

USMC due to the unidirectional input stage and the unipolar output stage. This limits the operation of the USMC with reference to [92] and Fig. 7 and Fig. 10 in [84] and Fig. 3 and Fig. 11 in [143] to

$$\Phi_1 \in \left[-\frac{\pi}{6}, +\frac{\pi}{6}\right] \quad \text{and} \quad \Phi_2 \in \left[-\frac{\pi}{6}, +\frac{\pi}{6}\right]. \tag{1.3}$$

In addition to the topology shown in Fig. 1.21(a), the USMC can also be implemented with six switches in the input stage as in Fig. 1.21(b). This circuit variant exhibits lower conduction losses but a greater implementation effort compared to the variant in Fig. 1.21(a).

Sparse T-Source Converter

The maximum output voltage of MCs is limited to 86.6% of the input voltage as previously stated. In order to complete the review of ac-ac converters, a new topology is presented that overcomes this limitation and still maintains the advantages of IMCs of comparatively low switching losses. The resulting bidirectional topology, shown in Fig. 1.22, consists of a SMC circuit with a T-source network integrated into the link, and is referred to as Sparse T-Source Converter (STSC).

The passive T-source network actually links a bidirectional and unipolar CSR with a bidirectional and unipolar VSI and implements voltage

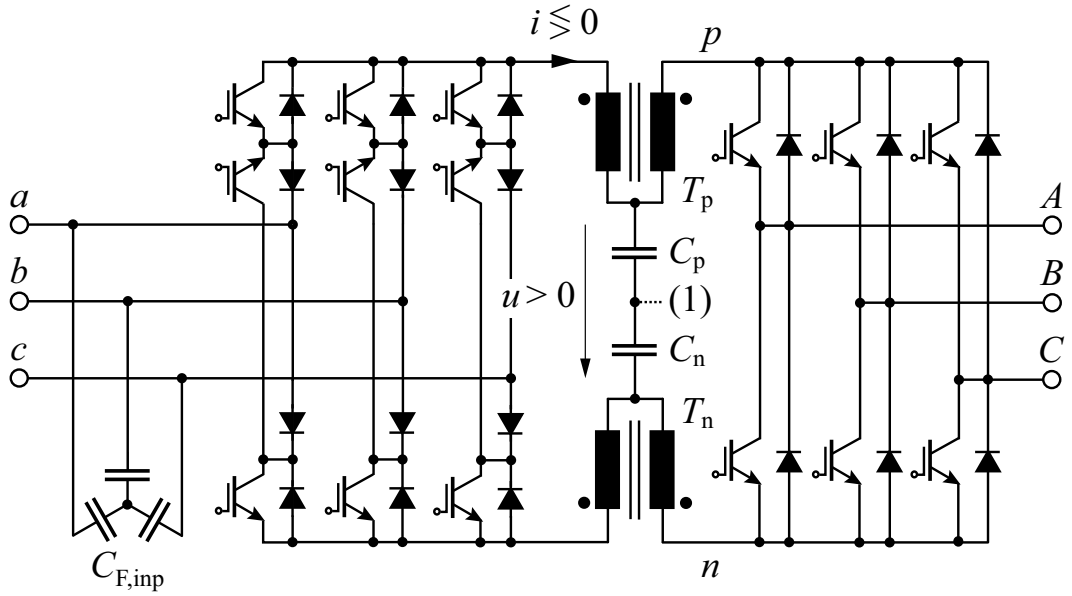


Fig. 1.22: Sparse T-Source Converter (STSC). (1) Optional connection to the star-point of an output filter.

step-up functionality with the coupled inductors (high frequency auto-transformers T_p and T_n). The input stage is modulated similarly to a CSR and can be operated in the simplest control scheme at a fixed modulation index (duty cycle) of for instance 80%. The output stage is controlled like a conventional VSI. The switching state of the input stage is changed, whenever the output stage is in the freewheeling state, as is possible for the IMC. This modulation strategy reduces the level of the switched current of the input stage and consequently its switching losses as only the magnetizing current of the auto-transformers and not the transferred load current is switched.

Compared to the VSBBC and CSBBC with dc-link energy storage the STSC requires only a minimal intermediate energy storage, which indicates his relation to MCs. This matches well with the properties of a transformer. The T-source network just provides a small amount of intermediate energy storage mainly with the capacitors C_p and C_n. In the auto-transformers T_p and T_n, only magnetizing energy is stored. The maximum converter output voltage can be adjusted by changing the turns ratio of T_p and T_n.

The volume of the T-source network is determined by the volume of its transformers and is reduced with increasing switching frequency. For increasing current levels (power levels), the volume of the transformers growth less compared to a dc-link capacitor of a VSBBC as no energy has to be stored. The blocking voltage stress on the output stage devices is significantly higher compared to MCs or VSBBCs due to the transformer, which is a significant disadvantage of the STSC. Another challenge of this topology is the requirement for a low leakage inductance transformer design.

In view of the already demanding operating behavior of MCs in general and in particular their limitation to handle failure modes, the STSC with even additional passive components in the link currently does not seem to be a viable alternative for industrial ac-ac converters, but is only of academic interest. For this reason, no further details of the STSC are presented in this work.

1.4.3 Comparisons of AC-AC Converters

The preceding review of ac-ac converters shows that for the past decades many different topologies and their properties have been analyzed and described in the literature. Despite the broad spectrum of these partially very detailed investigations, research work performing a holistic comparison of ac-ac converter topologies for drive applications is very rare.

Most of the investigations focus on a performance comparison based on semiconductor loss calculations or measurements and typically involve two different converter topologies. Three main setups for ac-ac converter comparisons can be found in the literature: comparisons between the MC and VSBBC, between the VSBBC and CSBBC, and between the CMC and IMC. In [187, 206–208], the semiconductor losses and the design of the CMC and VSBBC are compared to identify the potential benefits and risks of the MC technology. [208] suggests an electro-thermal simulation based approach to analyze the thermal stress of the power semiconductors. The performance and implementation effort of a VSMC and VSBBC are described in [209]. Semiconductor loss and efficiency comparisons between the VSBBC and CSBBC are performed in [210–213]. Performance assessments between the CMC and IMC are investigated in [214, 215].

Another topic area of comparison deals with the converter modulation. [216] describes a unified modulation scheme for voltage and current source topologies. In [217] the CMC and IMC are analyzed regarding their SVM schemes.

Further research work investigated the input and output power quality of different converter topologies. In [218], the harmonic behavior of the VSR and CSR and in [219] of the CMC and IMC is compared.

Contrary to most of the other topology comparisons, a systematic evaluation is presented in [220,221] not only comparing two but multiple ac-ac converter topologies. With the proposed method, the individual topologies are analyzed using weight as a comparison metric.

A rather novel approach are reliability based comparisons of converter topologies, gaining steadily in importance, as they allow an estimation of the Mean Time To Failure (MTTF) and ultimately the medium-to-long-term cost of a certain converter concept. However, the challenge with this approach is to obtain adequate reliability data and models.

First publications on ac-ac converters, using failure rates of the individual components, compare the reliability between the CMC and the VSBBC [222] and between the CMC and the 18-Pulse Rectifier [223] for MEA applications. Another method for determining the reliability is presented in [224] for the CMC and determines the thermal stress of the semiconductors and therewith the MTTF figure of the power module.

1.4.4 Classification

In order to complete the review of bidirectional, low-voltage, forced commutated ac-ac converters, a possible classification of ac-ac converter topologies is depicted in Fig. 1.23. Different criteria for classification are possible such as for example the number of power conversion stages, the type of power conversion, the number of semiconductor devices, or the required galvanically isolated gate drive voltage levels.

In the overview at hand, the individual converter topologies are classified with respect to the internal (integrated) energy storage in the main power circuit, which is inspired by the classification presented in [84]. This leads to the following three main categories of ac-ac converters: converters with dc-link energy storage, hybrid matrix converters, and matrix converters. Hybrid matrix converter topologies are a mixture of matrix converters and converters with intermediate energy storage.

Although the fact that the analysis in this work is confined to two-level topologies, the Three-Level Neutral Point Clamped VSBBC (3L-NPC VSBBC) is listed as well for completeness. The converter names marked with "u" (e.g. USMC$^{\mathrm{u}}$) refer to unidirectional topologies.

1.5 Summary

In this chapter an overview of the key bidirectional, hard-switched ac-ac converter topologies including their properties is presented that are suitable for low-voltage application. Bidirectional ac-ac converters can be basically classified into topologies with intermediate energy storage and without intermediate energy storage. The four converter topologies investigated in this work are the VSBBC and the CSBBC with dc-link energy storage and the CMC and IMC without intermediate energy storage.

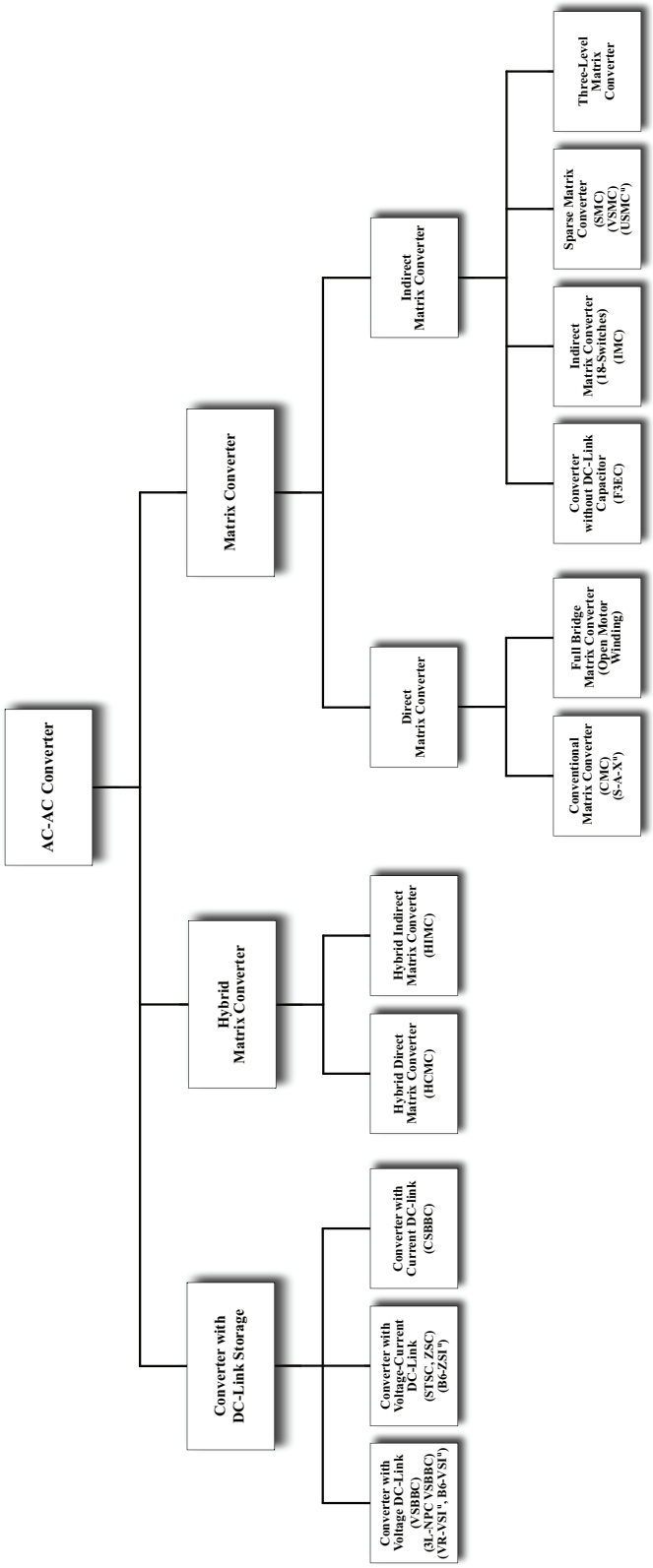


Fig. 1.23: Classification of ac-ac converter topologies.

The detailed literature review reveals that although a wide variety of different aspects have been investigated for the considered converter topologies, research work performing a comprehensive comparison of ac-ac converters is very rare. This finding forms the basic motivation for this thesis to develop a methodology that allows for a holistic comparison of ac-ac converter systems, and then to perform such a comparison for the VSBBC, CSBBC, IMC and CMC. A further contribution based on the literature review is the compilation of former and present countries and their universities with considerable research activities in the topic area of MCs, and an overview of the research on MCs in industry. It shows that the main research centers for MCs are in North America, Chile, Europe, and Japan and that currently only Yaskawa, a Japanese drives manufacturer, offers commercial MCs.

Most of the industrial, state-of-the-art, low-voltage ac-ac converters belong to the category of converters with dc-link energy storage and are mainly voltage-source-type topologies. Therefore, the properties of the VSBBC serve as benchmark for the converter topology comparison performed in this thesis, as it is the most widely used bidirectional ac-ac converter.

Chapter 2

Power Semiconductor Devices

The requirements for state-of-the-art semiconductor switching devices are demanding. In the on-state, their on-state voltage drop (forward voltage drop) and on-resistance should be as low as possible to reduce the conduction losses, and they should be capable of conducting sufficiently high currents. In the off-state, the power semiconductors should provide an adequate blocking voltage capability to guarantee safe operation. In addition, the switching losses should be minimal. Furthermore, the semiconductor material should have minimal degradation effects, withstand elevated temperature levels to enable safe transient device overloading, be insensitive to high irradiation levels, and allow for simple and thermo-mechanical, stress-minimal packaging to ensure long-term reliability.

Strong efforts have been undertaken in the research and further development of existing and also new power semiconductor technologies for the past decades, such as the silicon carbide (SiC) technology, due to the key position and significance of semiconductor devices in power electronic converter systems. First of all in this chapter, a summary of the potential benefits of SiC power devices compared with the Si devices is presented. Then a brief overview of state-of-the-art Si and SiC power semiconductors, suitable for low-voltage ac-ac converters, is provided that are commercially available or close to commercialization.

Special attention is directed to the normally-on SiC Junction Field Effect Transistor (JFET). Thereby, the challenges of its normally-on characteristic in terms of the application in a power circuit are discussed. Next, the design and implementation of a suitable gate drive circuit for the normally-on SiC JFET are described, followed by an experimental switching performance analysis and conduction and switching loss measurements.

This chapter concludes with a semiconductor loss evaluation and modeling for different characteristic semiconductor devices and technology configurations, applicable to ac-ac converters.

2.1 Silicon and Silicon Carbide

2.1.1 Basic Material Properties

Currently, primarily two semiconductor materials are used to fabricate power semiconductor devices: silicon and silicon carbide. Compared with silicon, silicon carbide (4H-SiC) has an approximately three-times higher band gab energy E_{G}, an approximately ten-times higher critical electric field E_{crit}, a two-times higher average saturation carrier drift velocity v_{sat}, a three-times higher maximum operating junction temperature $T_{\mathrm{J,max}}$ and higher thermal conductivity λ_{th}, and provides a chemical inertness and irradiation hardness. Further properties of silicon and silicon carbide are summarized in Tab. 2.1.

A higher critical electric field allows for thinner drift regions, higher doping concentrations $N_{\mathrm{A}}, N_{\mathrm{D}}$, higher specific conductivity σ_{on}, and a smaller chip area A_{chip} for a given breakdown voltage. It further enables the implementation of power devices with an increased blocking and break down voltage. A higher saturation carrier drift velocity allows for higher operating frequencies suitable for high switching frequency applications. Consequently, silicon carbide features excellent material properties for the implementation of high-voltage, high switching frequency, and high temperature power semiconductor devices. Unfortunately, some of the potential advantageous of SiC material properties cause considerable technological difficulties in the device fabrication process of SiC devices, as for example material defects or degradation effects, which are not all solved yet.

Various silicon carbide structures exist, such as 3C-SiC, 4H-SiC, and 6H-SiC, whereas 4H-SiC, and 6H-SiC are typically used for power devices. 4H-SiC is the preferred material due to its two-times higher electron mobility μ_{n} compared with 6H-SiC. Additionally, the much lower thermal minority carrier generation of 4H-SiC results in lower device leakage currents.

Fig. 2.1 visualizes the main properties of silicon and 4H silicon carbide for power devices, normalized to silicon. It is important to note that besides the actual electrical and thermal properties also the mechanical and thermo-mechanical material properties are crucial for power semiconductor devices in terms of packaging and reliability. As can be seen in the diagram below, the largest differences between 4H-SiC and Si are the high critical electric field and the low intrinsic carrier density

Property	*Unit*	Si	4H-SiC	6H-SiC
E_{G}	eV	1.12	3.26	3.02
E_{BD}	MV/cm	0.3	2.8	2.5
n_{i}	$1/\mathrm{cm}^3$	$1.4 \cdot 10^{10}$	$5 \cdot 10^{-9}$	$1.6 \cdot 10^{-6}$
μ_{n}	$\mathrm{cm}^2/\,(\mathrm{Vs})$	1500	900	400
μ_{p}	$\mathrm{cm}^2/\,(\mathrm{Vs})$	450	115	100
$v_{\mathrm{sat,n}}$	cm/s	$1 \cdot 10^7$	$2 \cdot 10^7$	$2 \cdot 10^7$
ε_{r}	-	11.9	9.66	9.66
$T_{\mathrm{J,max}}$	°C	≈ 200	≈ 600	≈ 700
λ_{th}	W/ (Kcm)	1.5	3.9	4.9
α	ppm/K	2.5	2.2	2.2
ρ	$\mathrm{g/cm}^3$	2.3	3.2	3.2
K_{B}	GPa	100	205	205
K_{S}	GPa	50	200	195
H_{K}	$\mathrm{kg/mm}^2$	1100	2400	2400

Tab. 2.1: Material properties of silicon and 4H and 6H silicon carbide at 25°C, compiled from [225–227].

n_{i}, enabling the implementation of power devices with high blocking voltage and small on-state resistance and/or chip area. SiC is characterized by its superior thermal conductivity and maximum junction temperature compared with Si. The main difference in the mechanical properties is found in the high structural hardness of SiC, increasing the requirements for the interface materials between the SiC chips and the package. Another challenge in the packaging technology is to utilize the high temperature operation capability of SiC whilst maintaining the demanded power device reliability.

Contrary to the Si technology, which is very well established in the semiconductor industry for the fabrication of integrated circuits, power devices, or photovoltaic cells, the SiC technology is mainly driven by the increasing demand for nitride based devices (light emitting diodes or lasers), where it has become the substrate of choice due to its favorable thermal and structural properties. This explains that competitive SiC

power device production with corresponding Si devices could not yet be achieved, which is even complicated by the challenging and elaborate process technology of silicon carbide.

2.1.2 Figures-of-Merit

Figures-Of-Merit (FOMs) for semiconductor devices enable an analytical assessment of the device performance for different semiconductor technologies. In the following, the most intuitive FOMs, suggested for comparing Si and SiC power devices, are presented. The potential benefits of SiC devices are investigated and described based on [225] by

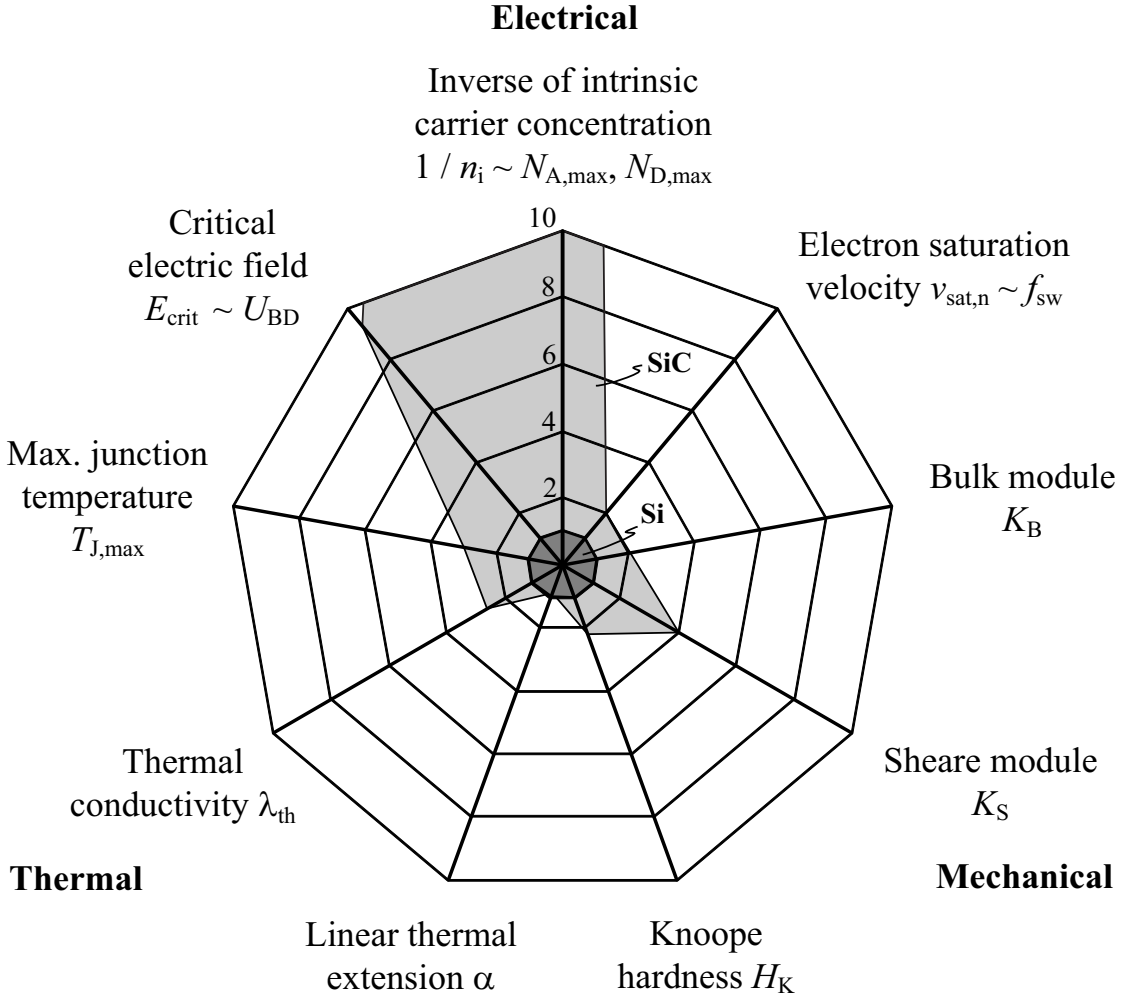


Fig. 2.1: Visualization of main electrical, thermal, and mechanical properties of Si (dark gray area) and 4H-SiC (light gray area), normalized to silicon.

estimating the dependencies between the forward voltage drop, the breakdown voltage, and the on-state resistance for a vertical MOSFET (VMOS) structure.

Assuming an abrupt pn^- junction and neglecting the built-in voltage, the device breakdown voltage U_{BD} can be estimated according to [228].

$$U_{\mathrm{BD}} = \frac{E_{\mathrm{crit}} w_{\mathrm{SCL}}}{2} \tag{2.1}$$

w_{SCL} is the total width of the space charge layer. The space charge layer primarily extends into the n^- drift region (one-sided junction) due to the lightly doped n^- drift region, and under the breakdown condition extends across the whole drift region, in this simplified model. For this special case, the space charge width w_{SCL} equals the width of the resulting drift region w_{n}.

The specific conductivity σ_{on} in the on-state of a VMOS structure (forward conduction) is mainly determined by the resistance of the drift region and may then be written as

$$\sigma_{\mathrm{on}} = \frac{e_0 \mu_{\mathrm{n}} N_{\mathrm{D}}}{w_{\mathrm{n}}} \tag{2.2}$$

if the influence of the channel resistance is neglected. The doping concentration of the drift region is denoted with N_{D} and the electron mobility with μ_{n}. By using the Poisson equation, which relates the excess electron and hole concentration to an internal electric field, (2.1) becomes

$$\frac{\varepsilon E_{\mathrm{crit}}}{w_{\mathrm{n}}} = e_0 N_{\mathrm{D}} \ . \tag{2.3}$$

By combining (2.1) and (2.2) the specific on-state conductivity reduces to

$$\sigma_{\mathrm{on}} = \frac{1}{A_{\mathrm{chip,act}} R_{\mathrm{on}}} = \frac{e_0 \mu_{\mathrm{n}} E_{\mathrm{crit}}^3}{4\, U_{\mathrm{BD}}^2} \ , \tag{2.4}$$

where $A_{\mathrm{chip,act}}$ corresponds to the active chip area and R_{on} to the on-state resistance. In [229], Baliga suggests the relationship between conductivity, electron mobility, and critical electric field as an assessment criterion for semiconductor device properties, which is known as the Baliga Figure-Of-Merit (BFOM)

$$\mathrm{BFOM} = \varepsilon \mu_{\mathrm{n}} E_{\mathrm{crit}}^3 \ . \tag{2.5}$$

The ratio of the BFOM for 4H-SiC and Si

$$k_{\mathrm{BFOM,SiC-Si}} = \frac{\mathrm{BFOM}_{\mathrm{4H-SiC}}}{\mathrm{BFOM}_{\mathrm{Si}}} \tag{2.6}$$

is approximately 400. Using (2.4), it can be shown that a 4H-SiC semiconductor device would allow for a twenty-times ($\sqrt{400} = 20$) higher breakdown voltage compared with an equivalent Si devices with the same active chip area $A_{\mathrm{chip,act}}$ and the same on-resistance R_{on}.

As can be immediately seen by inspection of (2.4), the chip area $A_{\mathrm{chip,act}}$ of the SiC device would be considerably smaller than that of the Si device, provided that the breakdown voltage U_{BD} and the on-resistance R_{on} are the same. Although the conduction losses would be equal for a constant device current I (as R_{on} is identical), the power loss density in the SiC device would be considerably higher. Furthermore, the smaller chip area of the SiC device would lead to a higher thermal resistance between the chip and the heat sink than for the Si device. Together with the increased power loss, this would result in a higher junction temperature of the SiC device compared with the Si device, which is a limitation of the BFOM.

In order to avoid this discrepancy, Schlangenotto et al. [230] suggests a Figure-Of-Merit (SFOM) which is formed by extension of the BFOM and performs the device comparison for a constant on-state conduction loss density ρ_{cond}

$$\rho_{\mathrm{cond}} = \frac{R_{\mathrm{on}} I^2}{A_{\mathrm{chip,act}}} = \frac{I^2}{A_{\mathrm{chip,act}}^2 \, \sigma_{\mathrm{on}}} = \mathrm{const}\ . \tag{2.7}$$

Using (2.4), the required active chip area can be calculated as

$$A_{\mathrm{chip,act}} = \frac{I}{\sqrt{\rho_{\mathrm{cond}} \, \sigma_{\mathrm{on}}}} = \frac{2\, I U_{\mathrm{BD}}}{\sqrt{\rho_{\mathrm{cond}}} \, \sqrt{\varepsilon \mu_{\mathrm{n}} E_{\mathrm{crit}}^3}}\ . \tag{2.8}$$

The on-resistance is then given by

$$R_{\mathrm{on}} = \frac{1}{A_{\mathrm{chip,act}} \, \sigma_{\mathrm{on}}} = \frac{2\, U_{\mathrm{BD}} \sqrt{\rho_{\mathrm{cond}}}}{I \sqrt{\varepsilon \mu_{\mathrm{n}} E_{\mathrm{crit}}^3}} \sim \frac{1}{\sqrt{\mathrm{BFOM}}}\ . \tag{2.9}$$

The conclusion is that the superior material properties of silicon carbide should not be primarily utilized to reduce the chip size but also to reduce the on-resistance. For a holistic assessment, both the static device

parameters (e.g. breakdown voltage and on-resistance) and the dynamic behavior need to be considered. In the SFOM, the dynamic behavior is modeled by considering the capacitive surface charge density q of the space charge layer, which is assumed to be inversely proportional to the chip area.

$$q \propto \frac{1}{A_{\mathrm{chip,act}}} \quad \Longrightarrow \quad q_{\mathrm{S}} = \frac{Q_{\mathrm{S}}}{A_{\mathrm{chip,act}}} = e_0 N_{\mathrm{D}} w_{\mathrm{n}}(u_{\mathrm{sw}}) \tag{2.10}$$

The charge Q_{S}, which might be designated as an equivalent stored charge, causes losses during the switching transients when charging and discharging the space charge layer. The width of the space charge layer (and the drift region) is not anymore constant as for the presented breakdown condition in (2.1), but is now dependent on the switched voltage u_{sw}. The capacitive switching loss energy $w_{\mathrm{Q,sw}}$ of an entire switching cycle, resulting from Q_{S}, is given by

$$w_{\mathrm{Q,sw}} = Q_{\mathrm{S}} u_{\mathrm{sw}} \ . \tag{2.11}$$

By substituting (2.1), (2.3), and (2.11) into (2.10), the charge density q_{S} can be written as

$$\begin{aligned} q_{\mathrm{S}} = \frac{Q_{\mathrm{S}}}{A_{\mathrm{chip,act}}} &= \frac{w_{\mathrm{Q,sw}}}{A_{\mathrm{chip,act}} u_{\mathrm{sw}}} \\ &= e_0 N_{\mathrm{D}} W_{\mathrm{n}} \sqrt{\frac{u_{\mathrm{sw}}}{U_{\mathrm{BD}}}} = \varepsilon E_{\mathrm{crit}} \sqrt{\frac{u_{\mathrm{sw}}}{U_{\mathrm{BD}}}} \ . \end{aligned} \tag{2.12}$$

Finally, for the overall device assessment the ratio between the specific conductivity σ_{on} and the charge density q_{S} is determined.

$$\frac{\sigma_{\mathrm{on}}}{q_{\mathrm{S}}} = \frac{\mu_{\mathrm{n}} E_{\mathrm{crit}}^2}{4\sqrt{u_{\mathrm{sw}} U_{\mathrm{BD}}^3}} \tag{2.13}$$

For the SFOM, we then obtain

$$\mathrm{SFOM} = \mu_{\mathrm{n}} E_{\mathrm{crit}}^2 \ . \tag{2.14}$$

If the ratio of the SFOMs for 4H-SiC and Si is calculated

$$k_{\mathrm{SFOM,SiC-Si}} = \frac{\mathrm{SFOM}_{\mathrm{4H-SiC}}}{\mathrm{SFOM}_{\mathrm{Si}}} \tag{2.15}$$

4H-SiC performs better by a factor of 52 compared with Si.

Many of the existing FOMs are based on semiconductor-physical parameters and therefore are appropriate to assess the potential of different semiconductor materials. However, for a straightforward comparison of real power devices they can hardly be applied as the required parameters can typically not be found in data sheets. A pragmatic solution has been suggested by Kolar et al. [231] with a FOM formed by the ratio of the conductance G and the energy equivalent device output capacitance $C_{\mathrm{oss,eq}}(u_{\mathrm{sw}})$, which depends on the switched voltage u_{sw}.

$$\mathrm{KFOM} = \sqrt{\frac{G}{C_{\mathrm{oss,eq}}(u_{\mathrm{sw}})}} = \sqrt{\frac{G'}{C'_{\mathrm{oss,eq}}(u_{\mathrm{sw}})}} \tag{2.16}$$

It is shown in [231] that the KFOM is proportional to the resulting power density of a power electronic converter system. In order to enable simple scaling of the device chip area, the ratio can also be expressed by the conductance G' and output capacitance $C'_{\mathrm{oss,eq}}(u_{\mathrm{sw}})$, normalized to the chip area. The conductivity G accounts for the device conduction losses and the output capacitance $C_{\mathrm{oss,eq}}(u_{\mathrm{sw}})$ for the switching losses, caused by the charging and discharging of the device output capacitance. In this consideration, the ideal device features a maximal conductivity and a minimal output capacitance, leading to a maximal value of the KFOM. The KFOM is closely related to (2.13) and thus to the SFOM.

The comparison of the BFOM and SFOM anticipates superior performance of SiC devices. An experimental evaluation of state-of-the-art SiC power devices, described in Sec. 2.4, however relativizes the actual performance gain of SiC power devices predicted by the BFOM or SFOM. An evaluation based on the KFOM aims at providing a more realistic assessment.

Silicon carbide has been considered for many years as the most promising semiconductor material for future power semiconductor devices. Meanwhile, the gallium-nitride (GaN) device technology is emerging for power devices where similar performance as with silicon carbide is expected, but many fabrication processes from the Si technology can be adopted.

2.2 Suitable Devices for AC-AC Converters

Industrial, three-phase, low-voltage PWM ac-ac converter for drive applications with a nominal input voltage of 400 V (rms), as considered in this work, require power semiconductor devices with a blocking voltage capability of 1200 V. An overview of suitable devices is provided in Tab. 2.2.

Present unipolar Si power transistors have beneficial properties compared to bipolar devices, such as moderate on-state conduction losses and low switching losses, for blocking voltages of up to approximately 600 V due to the band gap energy and critical electric field of silicon. For a blocking voltage capability of 1200 V, bipolar devices are primarily utilized. Si high-voltage Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) or Super-Junction (SJ) MOSFETs (CoolMOS technology) are typically not used for motor drive converters as the appropriate blocking voltage cannot be provided (present CoolMOS devices $U_{\mathrm{DSS,max}} = 900\,\mathrm{V}$) and too large chip areas would be required to

Transistor	*Freewheeling Diode*
Si high-voltage MOSFET	Si NPT PiN diode
Si SJ MOSFET (CoolMOS $\leq 900\,\mathrm{V}$)	Si PT PiN diode
Si NPT IGBT	Si PiN diode with FS
Si PT IGBT	Si FCE PiN diode
Si SPT IGBT	
Si T&FS IGBT	
Si RB-IGBT	
Si RC-IGBT	
SiC normally-on JFET (e.g. SiCED)	SiC Schottky diode
SiC normally-off JFET (e.g. SemiSouth)	
SiC BJT (e.g. TranSiC)	

Tab. 2.2: Si and SiC power semiconductor devices, suitable for low-voltage ac-ac converters and available in large enough quantities for implementing converter prototypes (Sep. 2009).

achieve the demanded low level of conduction losses. Additionally, the switching performance of the intrinsic body diodes is unfavorable. For this reason, state-of-the-art low-voltage motor drive converter systems are mainly implemented with Si IGBTs and Si PiN freewheeling diodes. The first part of the converter topology evaluation is thus performed for latest generation Si IGBT and diode devices.

Another, for cost reason still rarely applied option in industry, is to replace the Si PiN diode by a SiC Schottky Barrier Diode (SBD), leading to a hybrid configuration of a Si transistor and a SiC freewheeling diode. This combination would generally allow for significantly reducing the dynamic losses in the power devices, particularly the turn-on losses of the IGBT and the turn-off losses of the diode.

In addition, there are two IGBT based devices with extended functionality: the Reverse Blocking IGBT (RB-IGBT) and the Reverse Conducting IGBT (RC-IGBT). The RB-IGBT can block forward and reverse voltages and thus allows the replacement of a serial connection of an IGBT and a diode with a single chip. The RC-IGBT features unipolar voltage blocking similar to a conventional IGBT but enables reverse current flow. It allows the replacement of an anti-parallel connection of IGBT and diode with a single chip. Both devices, the RB-IGBT and the RC-IGBT, simplify the implementation of power circuits due to the reduction of the number of separate devices. However, the simplification is achieved at the expense of flexibility in combining arbitrary IGBTs with diodes.

In order to assess the potential of SiC switches and ultimately the performance of all-SiC ac-ac converter systems, adequate devices have to be found. When this thesis was started, the device of choice was (and still is) the 1200 V normally-on SiC JFET produced by SiCED due to its reported promising properties, ruggedness, flexible applicability, and finally also its availability in large enough quantities to implement converter prototype systems. Compared with other SiC transistors, this JFET has an integrated anti-parallel body diode. Meanwhile, also other 1200 V SiC transistors can be obtained as pre-commercial devices as for example normally-off SiC JFETs from SemiSouth or SiC BJTs from TranSiC. Another option would be 1200 V SiC MOSFETs announced by CREE.

In the following, a brief summary of Si IGBTs, Si RB-IGBTs, Si PiN diodes, SiC JFETs, and SiC Schottky diodes is presented. These devices

are utilized in the hardware prototypes implemented in this work.

2.2.1 Si IGBT

Various types of IGBTs exist which differ in terms of semiconductor structure, properties, or processing technology. Traditionally, there were two types of IGBTs the Punch-Through (PT) devices, where the electric field "punches through" the drift region during voltage blocking, and the Non-Punch-Through (NPT) devices, where the electric field does not punch through the drift region. Independent of the actual structural details, the term PT is nowadays used for comparatively thick IGBT chips, made from epitaxial wafers, which contain an n^+ buffer or a field stop layer, whereas the term NPT is associated with thinner chips fabricated from (cheaper) float zone wafers, which do not have an additional n^+ layer. An overview of the different IGBT device structures is presented in Fig. 2.2.

Two main technological trends can be observed in the further devel-

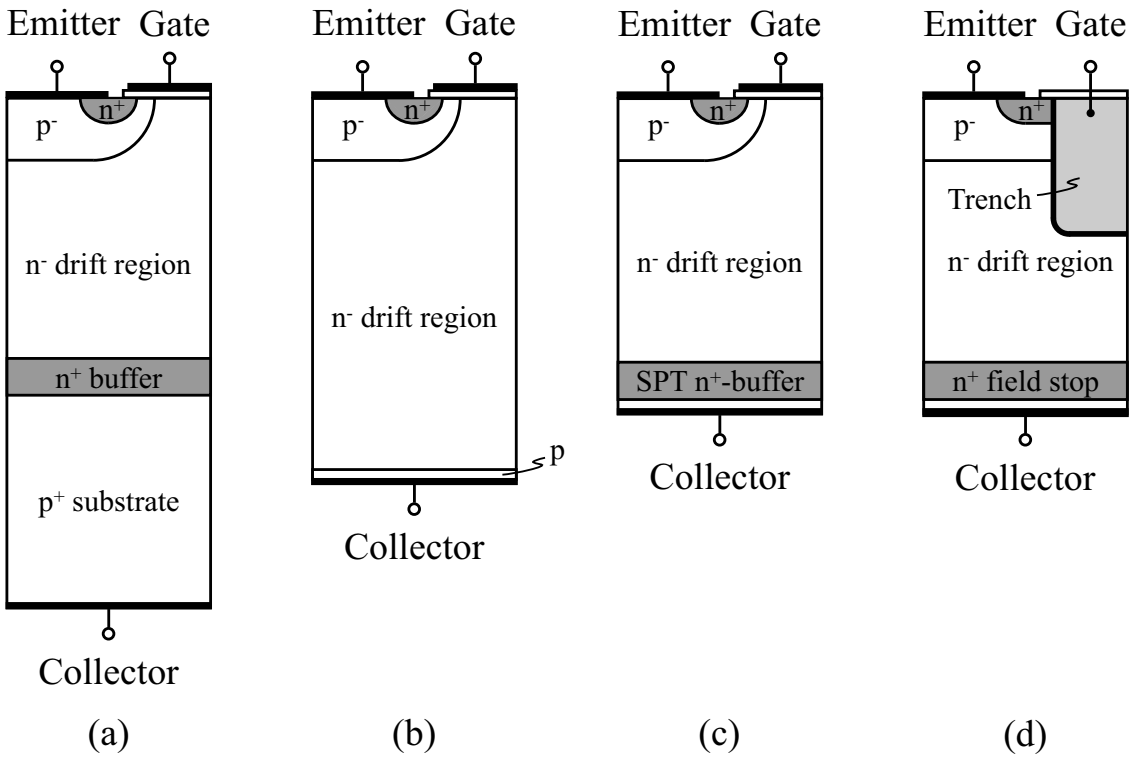


Fig. 2.2: Schematic structure of different IGBT technologies. **(a)** PT, **(b)** NPT, **(c)** SPT, and **(d)** T&FS IGBT.

opment of IGBT devices: the Trench and Field-Stop (T&FS) [232] and the Soft-Punch-Through (SPT) [233] technology. The T&FS IGBT design utilizes an n^+ buffer layer below the n^- substrate as a field stop layer. The deep trench gate combined with the back side emitter enables a low saturation voltage and a reduction of the chip area. The SPT chip structure is based on a planar gate NPT IGBT technology. It requires an additional n^+ buffer layer below the n^- substrate similar to the T&FS technology that prevents a "punch-through breakdown" of the device as the thickness of the n^- layer is minimized. Due to the narrow n^- layer, lower on-state and switching losses can be achieved compared to an NPT IGBT.

The currently latest generations of 1200 V devices of both new technologies are denoted as Trench or T&FS IGBT 4 and SPT+ IGBT. A comparison of these technologies, performed in [234], reveals that the static and dynamic loss of both IGBT technologies are in the same range. The difference is found in the ratio between the power losses and chip area: the Trench 4 chips allow for a current density of 130 A/cm^2 [235] whereas the current density of SPT+ chips is 115 A/cm^2 [236].

2.2.2 Si Reverse Blocking IGBT

The Reverse Blocking IGBT (RB-IGBT) features a symmetrical voltage blocking capability. This means that in its off-state, it can block forward as well as reverse voltages. Commercial devices are available for a blocking voltage of typically 1200 V and rarely 600 V. The RB-IGBT has been mainly applied for current source converter or matrix converter topologies, where bidirectional or reverse blocking power switches are required [195, 237, 238]. The implementation effort of a bidirectional switch can be significantly reduced as the anti-parallel wiring of two series connections of an IGBT and diode can be replaced by two anti-parallel connected RB-IGBTs as depicted in Fig. 2.3. This allows lowering the number of semiconductor dies for a bidirectional switch from four to two.

The on-state losses of a RB-IGBT are lower compared to an IGBT and a diode with an equivalent current rating that are connected in series as described in [239]. Therefore, it is generally believed that using RB-IGBTs instead of discrete series connections of IGBTs and diodes would not only simplify the power circuit layout but also decrease the semiconductor losses. However, depending on the device optimization

the dynamic behavior of RB-IGBTs may exhibit large tail currents during device turn-off, as reported in [167].

The basic structure of a RB-IGBT is shown in Fig. 2.4. The RB-IGBT is similar to a conventional IGBT, as it is usually fabricated based on a NPT device, except for a deep diffusion collector wall surrounding the active chip area. This collector isolation allows the RB-IGBT to block negative collector-emitter (reverse) voltage. The production of RB-IGBTs is more elaborate and the devices are more expensive

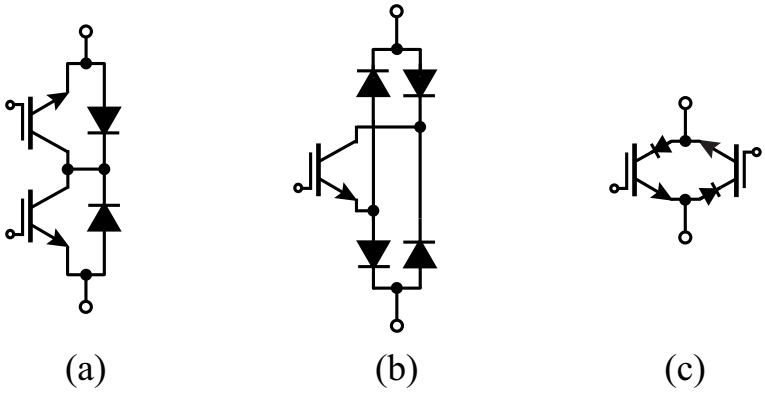


Fig. 2.3: Different IGBT configurations for bidirectional switches. **(a)** Common-collector IGBT, **(b)** "Graetz" single IGBT, and **(c)** anti-parallel RB-IGBT configuration.

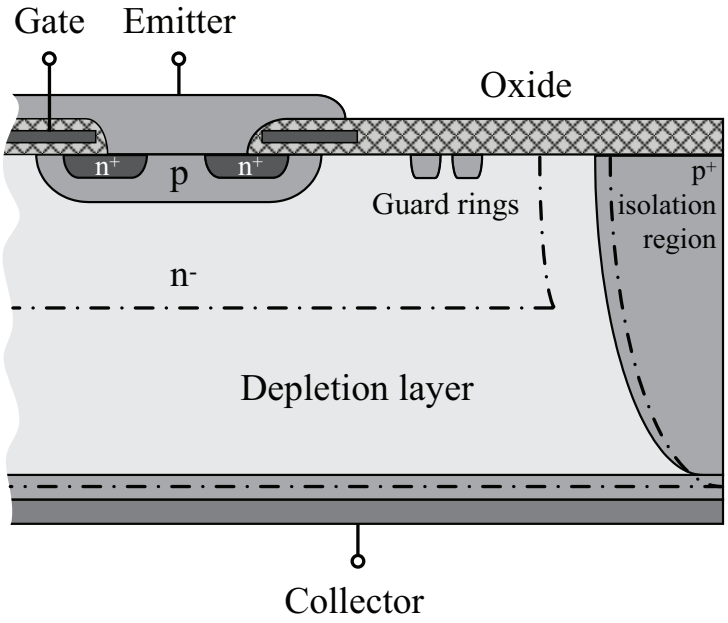


Fig. 2.4: Schematic structure of a RB-IGBT.

compared with conventional IGBTs. Different new fabrication processes have been developed and reported, mainly by Japanese semiconductor device manufacturers [166, 240], to reduce device cost. Currently, the RB-IGBTs seem to be disappearing from the market due to the lack of applications.

2.2.3 Si PiN Freewheeling Diode

Modern fast semiconductor switches require fast and powerful freewheeling diodes, as they significantly influence the turn-on losses of the switches. The freewheeling diode is typically commutated at every turn-on of the switch from its conduction to blocking state. A soft- and fast-recovery behavior with a low reverse-recovery charge is desired. There are two main types of power diodes to be distinguished: Si Schottky diodes and Si PiN junction diodes. Mainly Si PiN diodes are applied for the considered blocking voltage level of 1200 V. A schematic structure of a typical Si PiN power diode is depicted in Fig. 2.5.

The intermediate layer is not intrinsic but lightly n doped (n^-). Either a PT or a NPT design can be selected similar to the IGBT. PT and NPT refers in this case to the extension of the electric field in the n^- layer, and on whether it reaches during voltage blocking the n^+ cathode region. In terms of the forward voltage drop a PT design is desirable.

A variety of measures have been taken to optimize the static and

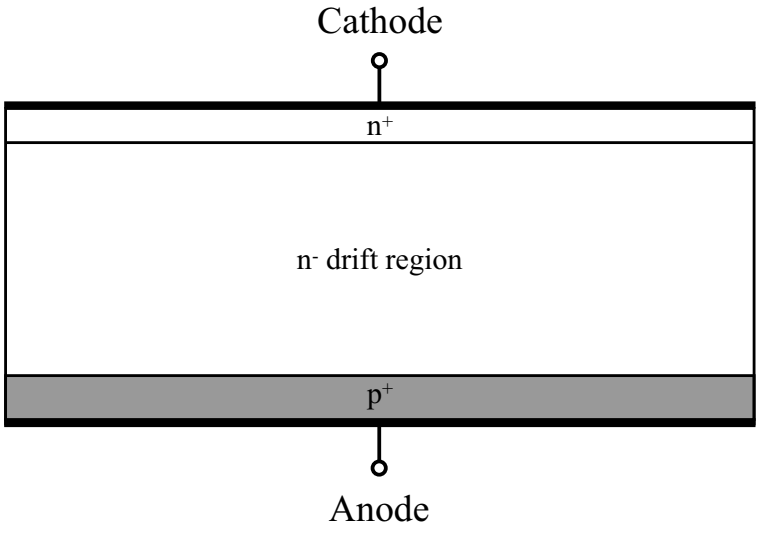


Fig. 2.5: Schematic structure of a Si PiN power diode.

dynamic behavior of PiN power diodes. One possibility is to apply the concept of Controlled Axial Lifetime (CAL) by implanting recombination centers (He-ions) at the pn junction. This improves the ratio between the on-state forward voltage drop and the reverse recovery peak current, which results in diodes with high dynamic ruggedness [241].

A further option is to implement anode emitters with low doping, which enable small reverse recovery currents without special techniques like helium irradiation induced recombination centers to reduce the injection efficiency of the anode. This approach is known as emitter controlled (EmCon) technology [242,243]. In the latest generation EmCon4 diodes, a deep Field Stop (FS) layer is integrated in order to further improve the soft recovery behavior and to prevent a current snap-off especially at low current levels.

Another state-of-the-art PiN diode technology applies the principle of Field Charge Extraction (FCE) to enable soft reverse recovery behavior. The FCE diode structure consists on the cathode side of a SPT buffer and additional p^+ islands in the cathode contact region [244].

2.2.4 SiC JFET

Basic Device Structure

The Junction Field Effect Transistor (JFET) is the simplest electronic switching device that is based on the field effect to change its conduction state. In the JFET an electric field perpendicular to the semiconductor surface is used to control the current flow (resistance) in a semiconducting channel area between the drain and source device terminals. The current flows by majority carriers as in other unipolar devices. Contrary to the MOSFET, the field occurs across a conventional pn junction depletion layer in the bulk region without the requirement for a gate oxide layer. By applying a bias voltage between the gate and source terminal, the channel is "pinched-off" and the current flow between drain and source is impeded.

The JFET offers several advantages like negligible minority free-carrier charge storage, low noise, high input impedance, and high frequency operation. The simplicity of the structure, which requires only pn junctions as functional elements, is the main motivation for the implementation of SiC JFETs with high voltage blocking, fast switching, and high temperature operation capability. Additionally, its structure is beneficial in

terms of long-term stability and ruggedness due to the absence of a gate oxide and the integration of the functional parts inside the device body [245]. The SiC JFET has also proven short-circuit robustness [246] and excellent cosmic ray resistance [247].

Currently, two main trends can be identified in the SiC JFET development: the normally-on lateral-vertical [248, 249] device concept, fabricated by SiCED (Infineon), and the normally-off purely vertical [250,251] implementation promoted, for instance, by SemiSouth, Denso, or Hitachi. A schematic cross section of these two SiC JFET structures is depicted in Fig. 2.6. Purely vertical structures enable typically lower area-specific on-resistance, as a higher channel density can be achieved compared with the lateral-vertical implementation. According to [252], the disadvantages often associated with purely vertical SiC JFETs are: the sensitivity to deviations in the fabrication process, the comparatively high Miller capacitance, difficulties to integrate an anti-parallel body diode, and limitations regarding short-circuit and avalanche performance. Under these considerations the lateral-vertical JFET structure seems to be advantageous despite its normally-on characteristic.

The basic operation of the normally-on lateral-vertical SiC JFET is briefly described by means of Fig. 2.6(a). If the gate-source voltage $u_{\mathrm{GS}} = 0\,\mathrm{V}$, a lateral n-channel exists underneath the gate structure (n^- epilayer 2) that links the n^{++} source contact region via the vertically implemented drift region (n^- epilayer 1) with the n^{++} drain contact

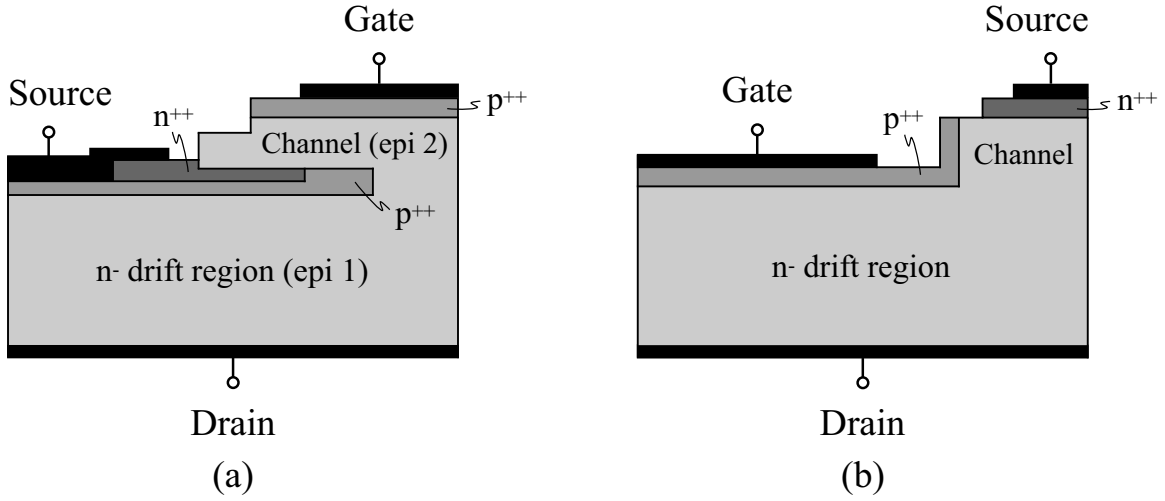


Fig. 2.6: Schematic structure of a **(a)** lateral-vertical and **(b)** purely vertical SiC JFET.

region. Thus, a conducting channel exists between the drain and source terminal, and the device is in its on-state. In order to switch the device off, a negative gate-source voltage $u_{\mathrm{GS}} < 0\,\mathrm{V}$ is required. If the gate-source voltage is reduced from 0 V to negative values, the pn junction below the gate structure is reverse biased, and the resistance of the lateral n-channel increases. If the pinch-off voltage level $U_{\mathrm{pinch-off}}$ is reached, the channel is fully diminished (pinched-off), and the device is blocking.

In this work, primarily the 1200 V normally-on SiC JFET from SiCED with a chip size of 2.4 mm by 2.4 mm is investigated and implemented in the converter prototypes.

The pinch-off voltage of the first devices tested varied between −13 V to −27 V due to the fabrication process, whereas most of the devices had a pinch-off voltage greater than −24 V. Meanwhile, the pinch-off voltage variation could be reduced to approximately $-17 \pm 0.8\,\mathrm{V}$. Reverse current flow is provided by the integrated body diode, even if the channel is blocking. This diode is formed by the p^{++} layer, connected to the source, the n^{-} epilayer 1, and the n^{++} drain region. The body diode hence features a similar structure to that of a PiN diode.

Normally-On vs. Normally-Off

The normally-off characteristic of a power transistor generally is a significant advantage in terms of operational safety of power electronic systems during start-up or regarding failure handling and facilitates the implementation of SiC switches from a conceptual point of view. The normally-off behavior of SiC switching device is therefore frequently advertised as a guarantee for a "drop-in" replacement of a Si power transistor by a SiC transistor. However, in many cases the gate drive circuit needs to be adapted in order to fully exploit the SiC device performance, even if it is a normally-off device such as the SiC JFET from SemiSouth [253]. From this perspective, the resulting effort for modifying the gate drive circuit can be assumed to be similar, independent on whether a normally-off or a normally-on SiC JFET is applied for the replacement of a silicon transistor.

The SiC JFET from SiCED can be utilized either as a normally-on, or if connected in series with a low-voltage MOSFET, as a normally-off device (cascode configuration [254, 255], also known as "Baliga configuration" [256]). In order to further increase the blocking voltage, multi-

ple JFETs in a cascode configuration can be connected in series, leading to the so-called "SuperCascode" [257]. It should be noted that the normally-on characteristic is not a precondition for a cascode configuration.

The question that evidently arises in the context of this work is, on whether the normally-on behavior may be beneficially used for ac-ac converters. An evaluation of different converter topologies and switch configurations leads to the following conclusions: The best match be-

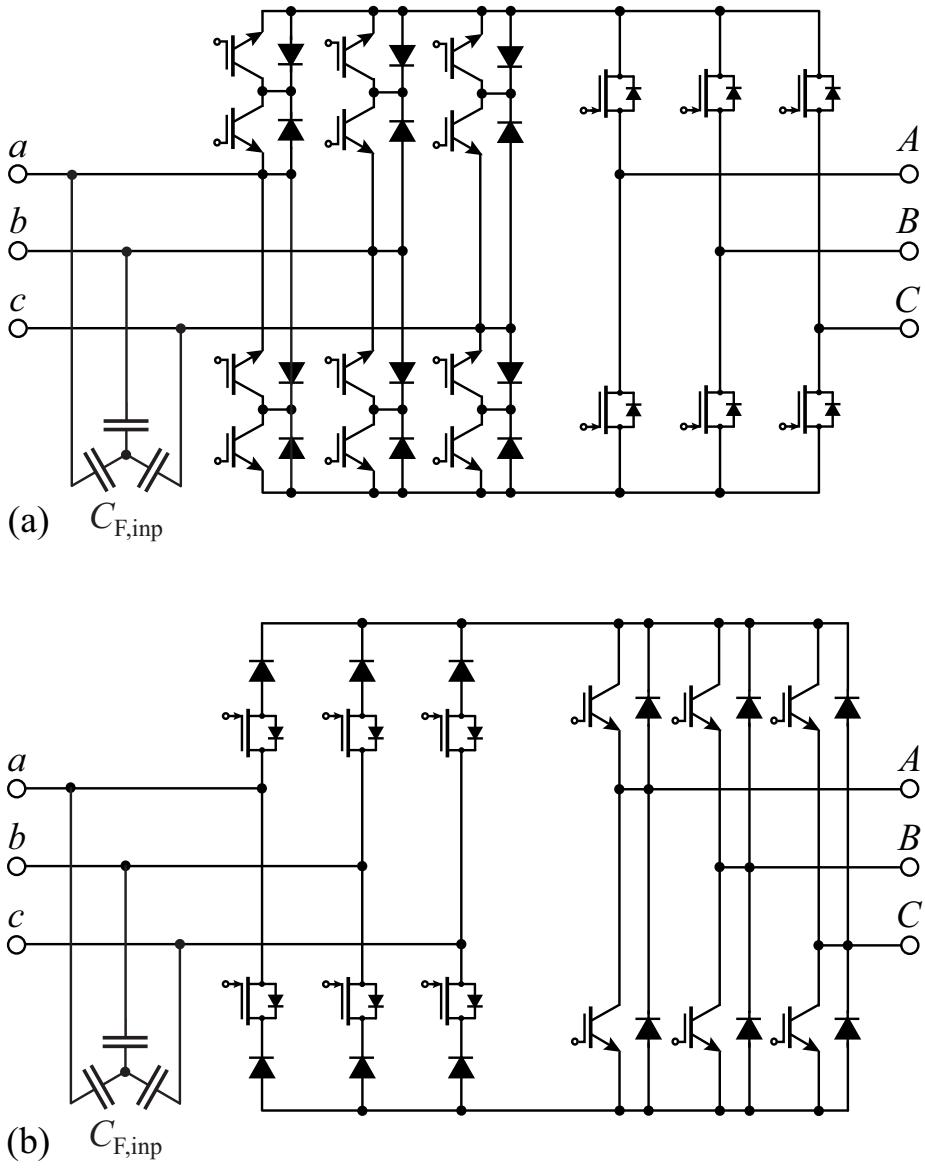


Fig. 2.7: **(a)** IMC with normally-on SiC JFETs in the output stage and **(b)** USMC with normally-on SiC JFETs in the input stage.

tween power semiconductor and converter topology can be achieved with current-source-type converter topologies as for example with the CSBBC, shown in Fig. 1.7, as it naturally favors the normally-on characteristics. Under fault conditions, such as for example power loss of the gate driver supply, a natural freewheeling path is provided for the dc-link inductor current as the JFETs become conducting. The same argument is also valid for a three-phase buck-type CSR [258, 259].

Another option is to only partly replace normally-off devices of a power circuit by normally-on SiC JFETs such that the converter topology as a whole provides "cascode functionality", and the normally-on behavior of the JFETs does not affect the main operating behavior. A precondition for such a switching device replacement obviously is that the SiC JFET would allow for a considerable loss reduction. The first example in Fig. 2.7(a) shows an IMC in which only the Si IGBTs of the output stage are replaced by normally-on SiC JFETs with anti-parallel body diodes. The switching losses, which are generated for the standard modulation scheme (cf. Fig. 3.10(a), modulation scheme A) mainly in the switches of the output stage, can be considerably reduced by utilizing SiC JFETs. Mains phase short-circuiting in case of gate drive supply failures is inhibited by the (normally-off) Si IGBTs in the input stage. Another possibility is found with an USMC topology, as presented in Fig. 2.7(b), in which only the Si IGBTs of the input stage are replaced by normally-on SiC JFETs, whereas the output stage is implemented with conventional Si IGBTs and diodes. This semiconductor configuration would be particularly attractive for the modulation scheme, where the input stage is switched hard and the output stage is switched at zero voltage (cf. Fig. 3.10(b), modulation scheme B). The major part of the switching losses would then occur in the SiC JFETs and consequently be low. In order to further reduce the semiconductor losses, the diodes of the input stage could be implemented with SiC Schottky diodes.

The third example, depicted in Fig. 2.8, refers to a three-level T-type VSI [260], of which the bidirectional switches to the midpoint m are implemented by a common-drain configuration of two in anti-series connected normally-on SiC JFETs with anti-parallel body diodes. The output stage bridge-legs are implemented with conventional Si IGBTs and diodes. The normally-on behavior of the JFETs has no influence on the current path between the positive bus p and the midpoint m and the current path between m and the negative bus n as the normally-on JFETs are connected in series with a normally-off IGBT (intrinsic

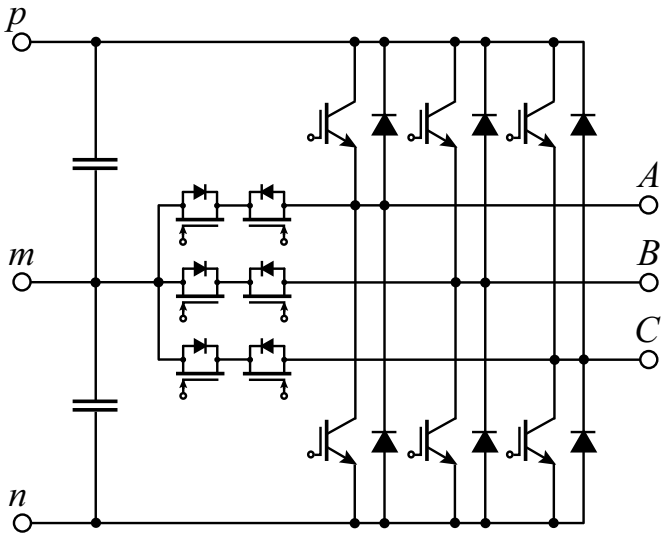


Fig. 2.8: Three-level T-type VSI with normally-on SiC JFETs for the switches between the midpoint m and the output terminals A, B, C.

cascode configuration). The common-drain configuration of the JFETs is advantageous compared with the common-source configuration as it requires only five isolated gate drive voltage levels. It further enables a passive turn-off of the three JFETs connected to the midpoint m during precharging of the dc-link capacitors by providing a negative bias for their gates with a high-ohmic resistive voltage divider connected between m and n. This T-type VSI topology may be applied to fully utilize the low-voltage range (e.g. 690 V mains applications) and consequently would require 1200 V SiC JFETs and 1700 V Si IGBTs and diodes.

2.2.5 SiC Schottky Diode

SiC Schottky diodes [261, 262] are the first commercialized SiC power devices introduced as a product in 2001 by Infineon. The main benefit of the SiC Schottky diode is the almost complete elimination of the reverse recovery charge that exists in the conventional bipolar Si PiN power diodes. State-of-the-art 1200 V SiC power diodes are implemented as Junction Barrier (JBS) and Merged PiN Schottky barrier (MPS) diodes, in which short regions of pn and Schottky barrier junctions are alternated. A simplified SiC MPS diode structure is illustrated in Fig. 2.9. The advantages of the integrated JBS or MPS SiC diode structures can be summarized as follows: At lower (nominal) current levels, the MPS

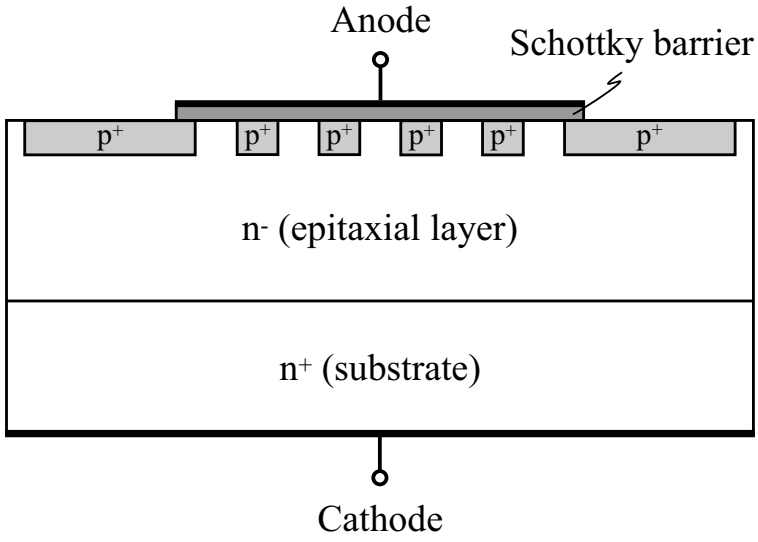


Fig. 2.9: Schematic structure of a SiC MPS diode.

diode behaves like a conventional SiC JBS diode. Above a certain current level, the p^+ regions of the MPS structure start to inject carriers and thus limit the forward voltage drop. The MPS diode features now the characteristic of a SiC PiN diode. Thus, by integrating an MPS structure the forward voltage drop at high currents can be lowered, and the surge current capability of the diode can be improved [263].

2.3 SiC JFET Gate Driver

2.3.1 Circuit Concept

Various challenges are faced in designing a high-frequency gate driver circuit for normally-on SiC JFETs such as varying pinch-off voltages at a comparatively large negative voltage of up to $-24\,\mathrm{V}$, high $\mathrm{d}v/\mathrm{d}t$ of $15\,\mathrm{kV}/\mu\mathrm{s}$, and the requirement for a small gate signal propagation delay in the isolation circuitry. The suggested gate drive topology is based on a driver concept with a capacitor in series to the gate resistor, which was demonstrated in [249]. A separate gate signal and driver power supply path are provided. This enables to select the switching state of the JFETs without temporal restrictions contrary to a boots-trap solution [264].

The gate driver circuit utilizes an Analog Devices magnetic isolator (ADuM1100), with a common mode immunity of up to $25\,\mathrm{kV}/\mu\mathrm{s}$ and

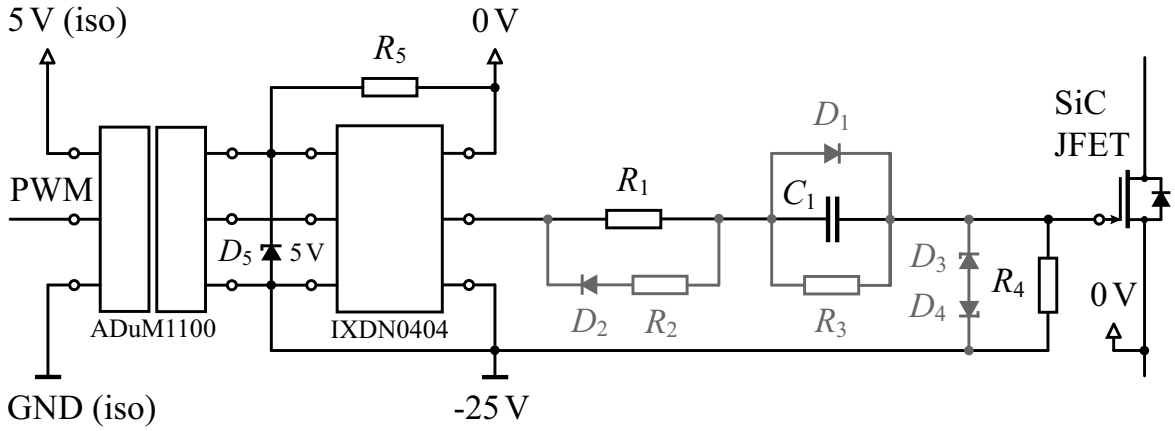


Fig. 2.10: Circuit schematic of the normally-on SiC JFET gate driver.

a propagation delay variation between 10 ns to 18 ns, and an IXYS 4 A gate driver IC (IXDN404). The −25 V supply is generated with an isolated point-of-load dc-dc converter off a 5 V auxiliary voltage bus, which is implemented with a Maxim H-bridge IC (MAX256), and a custom made transformer with a toroidal core from EPCOS (R6.3, T38). A schematic of the circuit is shown in Fig. 2.10. The black colored components are mandatory, the gray colored components could be provided to enhance functionality and safety.

2.3.2 Principle of Operation

The gate driver circuit requires a capacitor in series with the JFET gate to block any dc current that would flow due to the variation in the JFET pinch-off voltage and the onset of a gate-source diode (reverse) breakdown. This can occur because −25 V is applied to all JFETs to ensure that the maximum pinch-off voltage level of −24 V is exceeded for all JFETs to guarantee safe turn-off. However, if a JFET with a considerably lower pinch-off voltage level is in the circuit, then the gate-source diode reverse voltage rating may be exceeded by applying the −25 V and a negative gate current would start to flow. The series resistance R_1 is used to adjust the turn-on switching speed of the JFET. The turn-off switching speed can be controlled with R_2 and D_2. In order to always guarantee a gate-source voltage close to 0 V during turn-on, the diode D_1 is connected in parallel to the series capacitor C_1, preventing a voltage drop u_{C1} across the capacitor that is larger than the forward voltage drop of D_1. The resistor R_3 provides high-ohmic discharging for

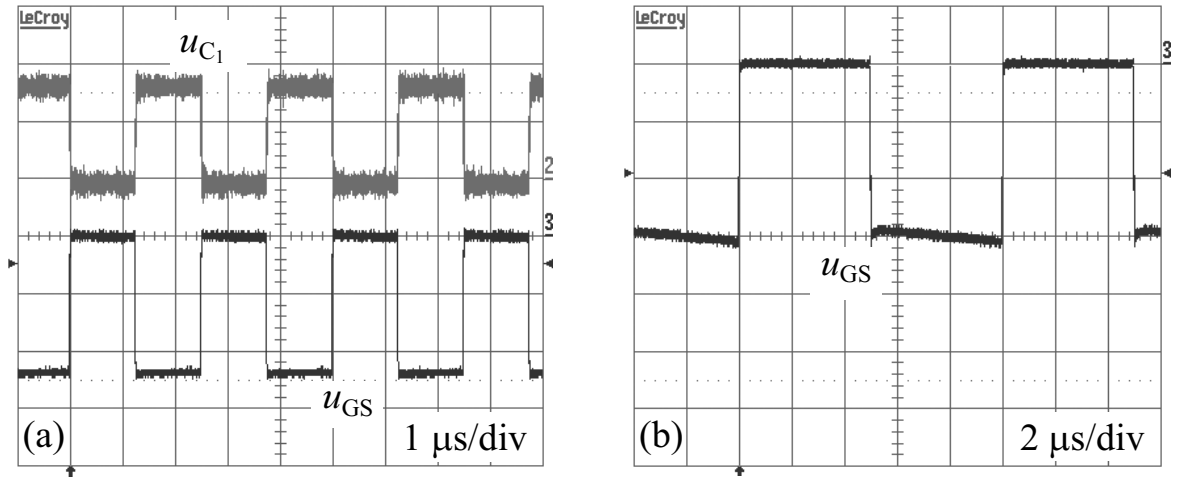


Fig. 2.11: SiC JFET gate driver waveforms. **(a)** Desired operation: u_{C_1}, 1 V/div; u_{GS}, 10 V/div for $C_1 = 47\,\text{nF}$ and $R_1 = 10\,\Omega$. **(b)** Undesired operation as the gate-source voltage is too small to turn off the JFET: u_{GS}, 5 V/div for $C_1 = 1\,\text{nF}$ and $R_1 = 10\,\Omega$.

C_1. The Zener-diodes D_3 and D_4 protect the gate, and the resistor R_4 is used to turn-off the JFET if the driver IC output is high-ohmic.

Fig. 2.11(a) demonstrates the functional principle of the series capacitor C_1 for a JFET with a pinch-off voltage of $-23.5\,\text{V}$. When the JFET is on ($u_{GS} = 0\,\text{V}$), the voltage drop across C_1 is zero ($u_{C_1} = 0\,\text{V}$). During turn-off the gate-source voltage is clamped to $-23.5\,\text{V}$ as the gate-source junction starts conducting at the pinch-off level. The voltage difference between the driver IC output and the gate drops across the series capacitor C_1. Without this capacitor, the current flowing into the gate, when the JFET is turned off, would only be limited by the series resistors R_1, R_2, and the internal gate resistance, which could thermally destroy the gate-source junction or the bond wires. The series capacitor C_1 and the resulting input capacitance of the JFET form a capacitive divider. Therefore, the value of C_1 needs to be selected considering the power semiconductor parameters. If the capacitance is too small, a voltage drop across C_1 occurs during the switching transient, which prevents the JFET from proper turn-off. This effect is demonstrated in Fig. 2.11(b).

The value for C_1 must be selected based on device measurements. The measured input capacitance when the device is turned off ($u_{GS} = U_{\text{pinch-off}}$ and $u_{DS} = 0\,\text{V}$) is considered as the maximum (worst case)

value $C_{\mathrm{iss,max}}$ and equals approximately 1 nF. Proper switching (turn-off) of the JFET can be achieved if C_1 is selected at least ten times larger than the resulting input capacitance of the JFET. For the actual converter prototypes, a value of 47 nF is selected for C_1. A further increase of the capacitance does not improve the switching behavior.

2.4 Power Device Loss Data

In order to assess different power device technologies for ac-ac converter applications, accurate semiconductor loss data is required. The semiconductor losses can be subdivided, as commonly known, into conduction losses and switching losses. The forward and reverse characteristics

$$u_{\mathrm{F/R}}(i, T_{\mathrm{J}}) = U_{\mathrm{F/R}}(T_{\mathrm{J}}) + r_{\mathrm{F/R}}(i, T_{\mathrm{J}}) \cdot i \tag{2.17}$$

are modeled as a function of the device current i and the junction temperature T_{J} with a forward (or reverse) voltage drop $U_{\mathrm{F/R}}$ and a forward (or reverse) differential resistance $r_{\mathrm{F/R}}$. It should be noted that for unipolar devices $U_{\mathrm{F/R}} = 0\,\mathrm{V}$, whereas for bipolar devices the current dependency of $r_{\mathrm{F/R}}$ is not required.

The switching loss energy of an entire switching cycle $E_{\mathrm{on,off}}$ is described based on the turn-on energy E_{on} and the turn-off energy E_{off} (or for diodes alternatively reverse recovery energy E_{rr}), where the actual switching energies depend on the switched current i_{sw}, the switched voltage u_{sw}, and the junction temperature T_{J}.

$$E_{\mathrm{on,off}}\big|_{i_{\mathrm{sw}},u_{\mathrm{sw}},T_{\mathrm{J}}} = E_{\mathrm{on}}\big|_{i_{\mathrm{sw}},u_{\mathrm{sw}},T_{\mathrm{J}}} + E_{\mathrm{off}}\big|_{i_{\mathrm{sw}},u_{\mathrm{sw}},T_{\mathrm{J}}} \tag{2.18}$$

This generalized calculation approach is applicable to all power devices and ac-ac converter topologies considered and ultimately allows the determination of the average semiconductor losses (cf. Chap. 4). The loss data can be obtained from various manufacturers for conventional 1200 V Si IGBTs and PiN power diodes, preferably from power modules as their data sets are typically more comprehensive compared with data sets from discrete components. However, for the transistor-diode configurations implemented with SiC JFETs and SiC JBS diodes, that were considered in this work, adequate loss data is missing and therefore needs to be experimentally determined. The following compilation

presents results of the conduction and switching loss measurements performed for a bridge-leg configuration of SiC JFETs and Si IGBTs with Si PiN and SiC JBS diodes.

2.4.1 Measurement Equipment

The semiconductor losses are measured using the equipment below:

- oscilloscope: LeCroy, Waverunner, LT584L, 2.5 GHz,
- passive low-voltage probes:
  - LeCroy, PP005, 10 : 1, 500 V, 500 MHz,
  - PMK, PHV621, 100 : 1, 2 kV, and
- current transducer: custom, implemented with a R6.3 toroidal core (EPCOS, MnZn ferrite, T38), cf. [265], pp. 48–51.

The current is measured with a custom current transducer, which is put over the drain or the collector pin of the package. For the conduction loss measurements, the drain-source or the collector-emitter voltage is measured with the PP005 voltage probe, and for the switching loss measurements with the PHV621 voltage probe. The delay between the voltage and current measurement signal on the scope is compensated to ensure accurate loss data.

2.4.2 Normally-on SiC JFET

At least two different device configurations are required for a comprehensive semiconductor loss evaluation:

- a series configuration of a SiC JFET with an additional switch and a freewheeling diode (Fig. 2.12(a)) to determine the conduction losses and
- a half-bridge configuration of two SiC JFETs (Fig. 2.12(b)) to measure the switching losses.

The series connection of the JFET with, for instance, a Si IGBT and a SiC Schottky freewheeling diode is required to avoid strong chip heating during the conduction loss measurement process. By applying just

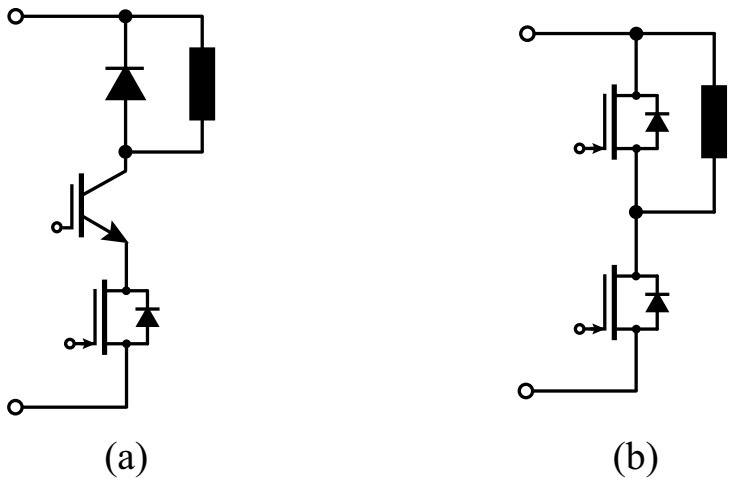


Fig. 2.12: Power device configurations for **(a)** conduction loss and **(b)** switching loss measurement.

a short current pulse (typically 0.1 ms to 0.3 ms) and measuring the device voltage drop with an accurate low-voltage oscilloscope probe, the influence of the chip temperature rise on the measurement result can be minimized. The half-bridge configuration is used to measure the JFET turn-on, turn-off, and body diode turn-off (reverse recovery) switching losses. The JFET body diode is not a Schottky diode and therefore exhibits a stored charge. The implemented devices are 1200 V normally-on SiC JFETs provided by SiCED and packaged in a standard TO-220 package, with a typical (suggested) current rating of 5 A to 6 A. The SiC

	SiC JFET	*SiC SBD*
Manufacturer	SiCED	CREE
Part number	Prototype	C2D10120A
Blocking voltage	1200 V	1200 V
Rated current	6 A	10 A
Chip dimensions	2.4 mm × 2.4 mm	3.1 mm × 3.1 mm
Total chip area	5.8 mm^2	9.8 mm^2
Active chip area	≈ 4 mm^2	≈ 7 mm^2

Tab. 2.3: SiC JFET and SiC Schottky Barrier Diode (SBD) chip data.

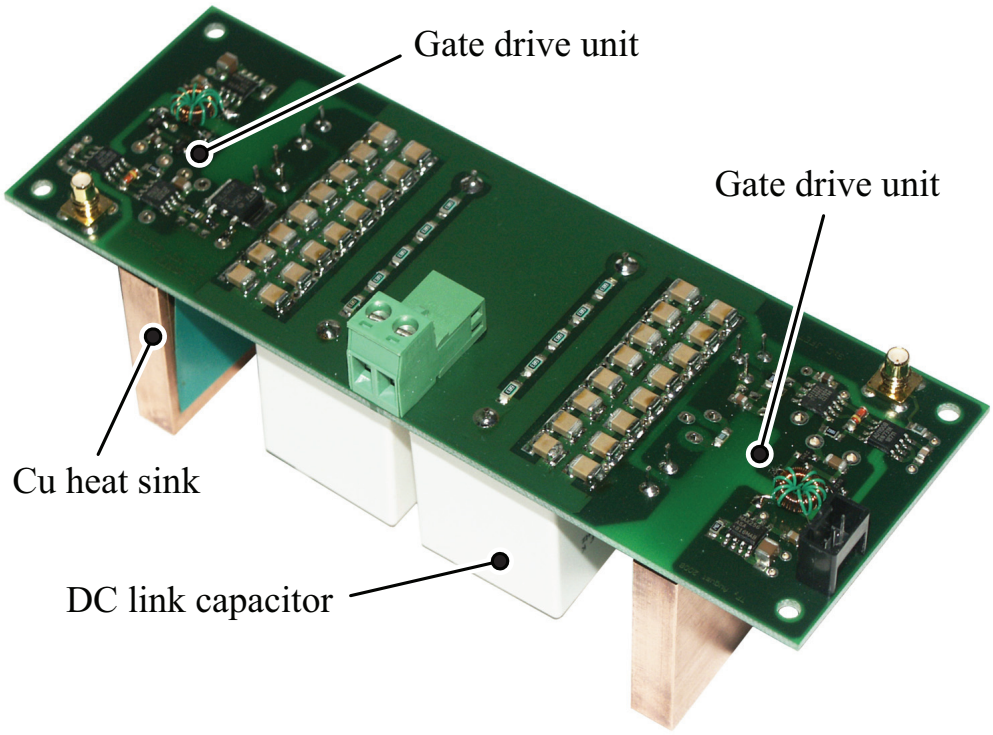


Fig. 2.13: Example of a power semiconductor loss measurement board.

JFET device chip data are summarized in Tab. 2.3 and contrasted with the chip data of a 1200 V SiC Schottky diode from CREE (C2D10120A) rated for 10 A. This diode is implemented in the All-SiC JFET CSBBC (cf. Sec. A.6). Switching losses should ideally be measured with the actual converter hardware in order to properly account for the influence of the circuit layout, especially if fast switching devices such as JFETs are utilized. However, in a typical converter design process this is not possible and an additional loss measurement board is required. The following brief calculation of the specific layer-to-layer capacitance $C'_{\mathrm{PCB,ll}}$ per unit area $A_0 = 1\,\mathrm{cm}^2$ of a standard 4-layer Printed Circuit Board (PCB) highlights the difficulty. Assuming a constant relative permettivity $\varepsilon_{\mathrm{r,FR4}} = 4.5$ of the FR4 insulator base material and a distance between the layers of $d_0 = 0.53\,\mathrm{mm}$, the specific layer-to-layer capacitance can be estimated as follows

$$C'_{\mathrm{PCB,ll}} = \frac{\varepsilon_0\,\varepsilon_{\mathrm{r,FR4}} A_0}{d_0} = 7.5\,\mathrm{pF/cm}^2 \approx 10\,\mathrm{pF/cm}^2\,. \tag{2.19}$$

If the total capacitive charge of the selected SiC diode $Q_{\mathrm{C}} = 61\,\mathrm{nC}$ is compared with the charge of the board capacitor at the rated diode blocking voltage of 1200 V, it is found that for a PCB area of less than

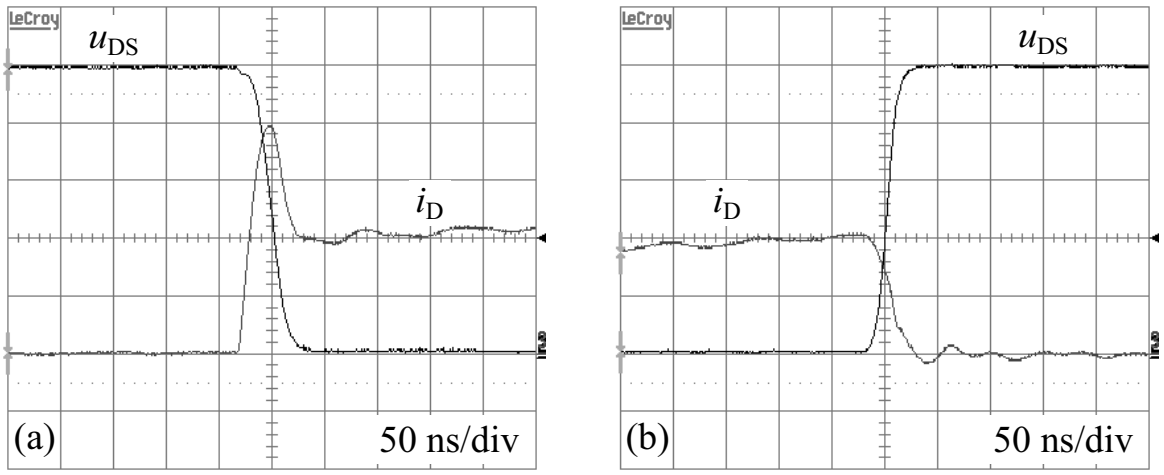


Fig. 2.14: SiC JFET switching waveforms at 500 V, 6 A, and a junction temperature of 125°C. **(a)** Turn-on: i_D, 3 A/div; u_{DS}, 100 V/div. **(b)** Turn-off: i_D, 3 A/div; u_{DS}, 100 V/div.

2.5 cm by 2.5 cm the same capacitive charge is stored in the layer-to-layer capacitor as in the diode. This uncertainty is mitigated by implementing an optimized gate driver circuit and commutation path layout similar as in the final converter power circuit layout. An example of such a measurement board layout is depicted in Fig. 2.13. Typical switching waveforms, from the bridge-leg configuration according to Fig. 2.12(b), are shown in Fig. 2.14. The average switching speed achieved at 500 V is in the range of 30 ns to 40 ns.

Fig. 2.15 presents the conduction behavior of the JFET channel and the integrated anti-parallel body diode for different junction temperatures. The reverse conduction behavior is investigated for both cases: when the JFET channel is turned off (only the body diode is conducting), and when it is turned on (channel and diode may conduct in parallel). As a consequence of the high voltage drop across the body diode compared with the channel, the JFET should be always turned-on for negative drain-source current flow to reduce the conduction losses. The body diode would then be solely used as a commutation diode.

$$R_{\mathrm{DS,on}}(I_{\mathrm{DS}}, T_{\mathrm{J}}) = \left(272\,\mathrm{m\Omega} + 40\frac{\mathrm{m\Omega}}{\mathrm{A}} I_{\mathrm{DS}}\right)\left(\frac{T_{\mathrm{J}} + 273.15\,\mathrm{K}}{298.15\,\mathrm{K}}\right)^{2.0} \quad (2.20)$$

dependent. By evaluation of the measurement data the (forward) on-resistance $R_{\mathrm{DS,on}}$ may be approximated as a function of the drain-source current I_{DS} and the junction temperature T_{J}. The measured JFET turn-

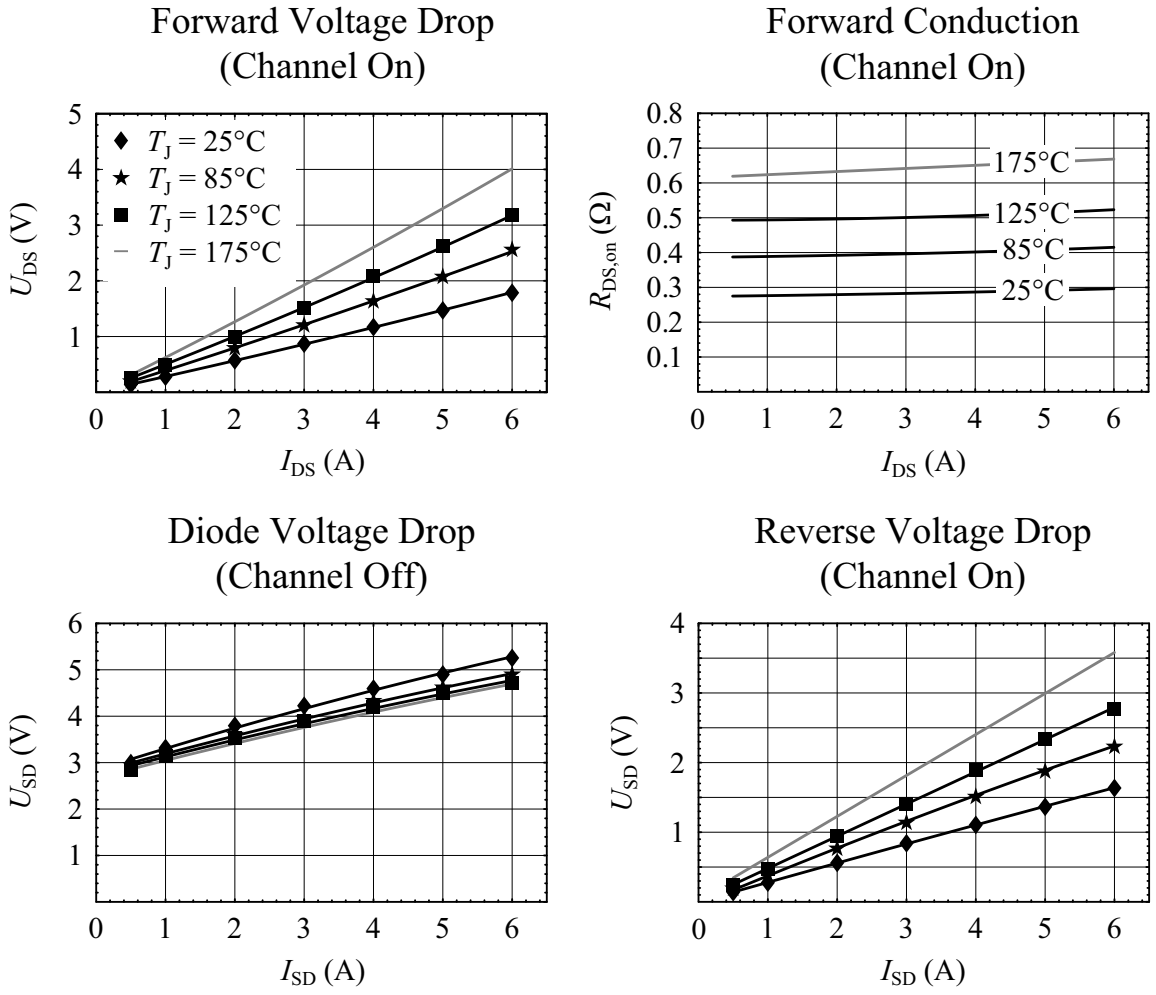


Fig. 2.15: SiC JFET conduction behavior for a junction temperature of $T_J = 25°C$ to $T_J = 175°C$.

k_i	*Unit*	$E_{S,on,off,25}$	$E_{D,off,25}$	$E_{S,on,off,175}$	$E_{D,off,175}$
k_1	$\frac{\mu J}{A}$	$-8.57 \cdot 10^{-2}$	$-2.89 \cdot 10^{-1}$	1.33	$-9.71 \cdot 10^{-1}$
k_2	$\frac{\mu J}{A^2 V}$	$2.01 \cdot 10^{-3}$	$-8.93 \cdot 10^{-6}$	$1.97 \cdot 10^{-3}$	$5.58 \cdot 10^{-4}$
k_3	$\frac{\mu J}{AV}$	$-7.33 \cdot 10^{-3}$	$-1.63 \cdot 10^{-3}$	$-2.01 \cdot 10^{-2}$	$4.46 \cdot 10^{-3}$
k_4	$\frac{\mu J}{AV^2}$	$3.63 \cdot 10^{-5}$	$4.20 \cdot 10^{-6}$	$4.74 \cdot 10^{-5}$	$2.32 \cdot 10^{-5}$
k_5	$\frac{\mu J}{V}$	$5.42 \cdot 10^{-2}$	$2.09 \cdot 10^{-2}$	$7.32 \cdot 10^{-2}$	$2.88 \cdot 10^{-2}$

Tab. 2.4: SiC JFET switching loss coefficients k_1 to k_5 evaluated for the sum of JFET turn-on and turn-off losses $E_{S,on,off}$ and the body diode turn-off losses $E_{D,off}$ for a junction temperature of 25°C and 175°C.

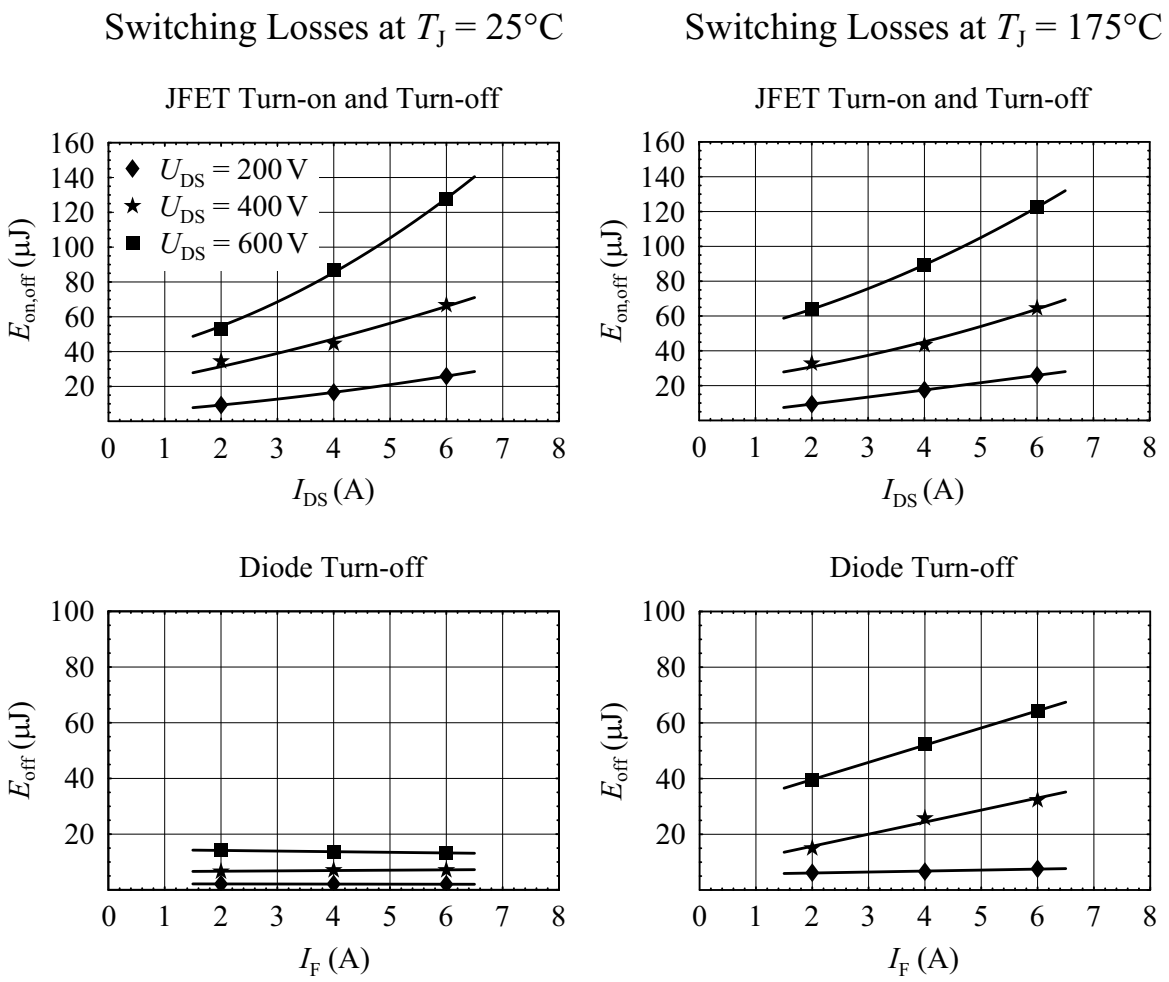


Fig. 2.16: SiC JFET switching losses at a junction temperature of $T_J = 25°C$ and $T_J = 175°C$.

on, turn-off, and body diode turn-off (reverse recovery) losses are shown in Fig. 2.16 as a function of the switched voltage and the switched current. The JFET turn-on and turn-off switching losses vary less than 10% in the considered junction temperature range of 25°C to 175°C. Therefore, only the loss energies for a junction temperature of 25°C and 175°C are plotted. The body diode turn-on losses are negligible. For simplifying further loss calculations, the switching loss energies are approximated with a loss polynomial function that depends on the switched current i_{sw} and the switched voltage u_{sw}.

$$w(i_{sw}, u_{sw}) = k_1 \cdot i_{sw} + k_2 \cdot i_{sw}^2 \cdot u_{sw} + k_3 \cdot i_{sw} \cdot u_{sw} + k_4 \cdot i_{sw} \cdot u_{sw}^2 + k_5 \cdot u_{sw} \quad (2.21)$$

The individual terms of i_{sw} and u_{sw} are related to the actual loss generation. The product $i_{sw} \cdot u_{sw}$, for instance, represents the power loss due to

the overlapping of voltage and current during the switching transients. Depending on the characteristics of the nonlinear capacitances of the switching devices (e.g. output capacitance of a transistor), it may be advantageous to replace $k_5 \cdot u_{\mathrm{sw}}$ by $k_5 \cdot u_{\mathrm{sw}}^2$. However, for the SiC JFET, a linear term of u_{sw} in the loss polynomial leads to a better matching between the fitted and measured loss energies. The junction temperature dependent loss coefficients k_1 to k_5 are compiled in Tab. 2.4. The loss data of the SiC JFET are mean values of multiple measurements and should be understood as a realistic approximation for a practical converter system, implemented with discrete components and standard 4-layer PCB technology.

2.4.3 Si IGBT with SiC Schottky Diode

Another option for reducing the transistor switching losses instead of utilizing SiC switch technology is to combine a Si IGBT with a SiC Schottky freewheeling diode. Such a device configuration is investigated based on the commercially available 1200 V FII50-12E bridge-leg module with Si NPT3 IGBTs (third generation) and Si fast recovery diodes from IXYS, implemented in an ISOPLUS-i4 package. The Si IGBT is rated for 32 A, whereas the freewheeling diodes are rated for 25 A at a case temperature of $T_{\mathrm{C}} = 90°\mathrm{C}$. Fig. 2.17 shows the DBC substrate, the semiconductor chips, and the bond wires of an open FII50-12E device. These modules are implemented in the IMC prototype with an output power of 6 kW, leading to a nominal device peak current of 15 A.

A custom module (FII50-12E-SiC) was developed in which each Si diode chip was replaced by two SiC Schottky diode chips from SiCED-Infineon each rated for 15 A, such that for the desired junction temper-

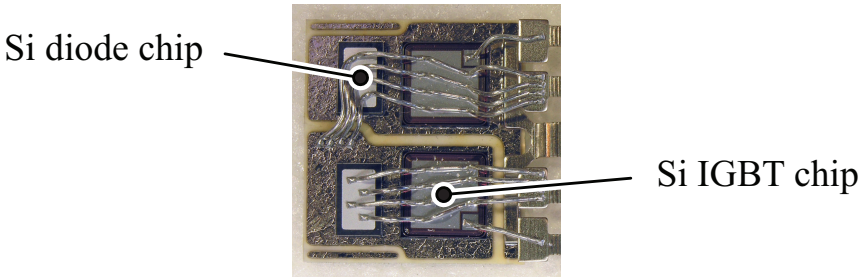


Fig. 2.17: Open FII50-12E (IXYS) bridge-leg module, showing the DBC substrate and the bonding of the Si IGBT and Si diode chips.

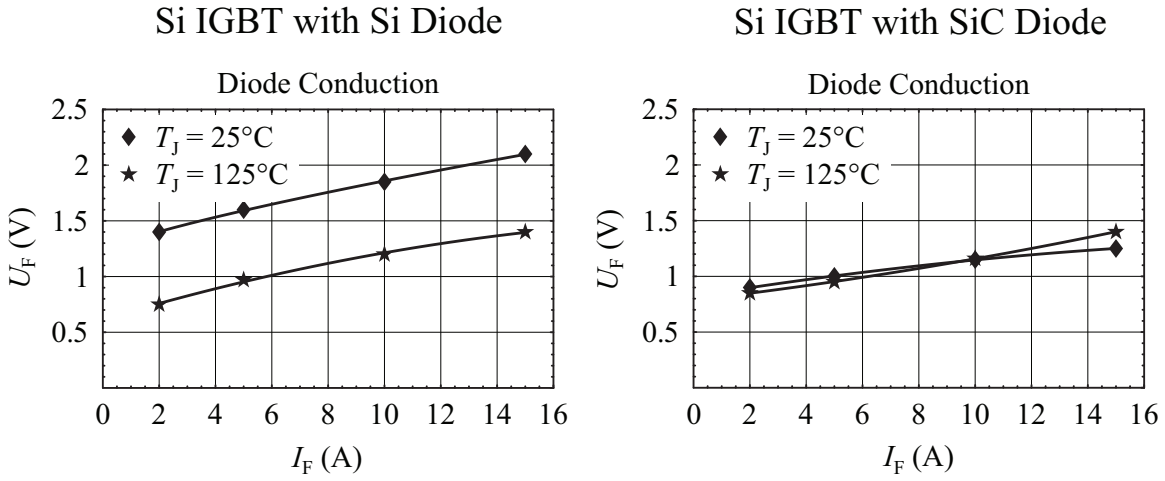


Fig. 2.18: Si and SiC freewheeling diode forward voltage drop U_F at a junction temperature of $T_J = 25°C$ and $T_J = 125°C$.

ature of 125°C and the nominal device peak current of 15 A the same diode forward voltage drop occurs as with the silicon diodes. With these two modules, a pragmatic loss comparison is enabled as the same DBC substrate and chip wiring layout is applied. In Fig. 2.18, the diode conduction behavior of both modules is illustrated, indicating that for a diode current of 15 A and a junction temperature of 125°C, the forward voltage drop U_F of the Si and SiC diode is identical as requested.

Fig. 2.19 presents a comparison of the IGBT turn-on, turn-off, and diode turn-off losses for both modules at a junction temperature of 125°C. In Fig. 2.20, the switching loss data is shown for a switched current of 15 A, evaluated for various junction temperatures. The IGBT turn-on losses with a SiC freewheeling diode are significantly reduced, on average by a factor of 2.5, whereas the IGBT turn-off losses are hardly affected by the diode technology. As expected, the SiC Schottky diode turn-off losses are negligible compared with the turn-off losses of the Si diode.

Apart from the different reverse recovery behavior, the most significant difference between Si PiN and SiC Schottky diodes regarding conduction behavior is found in the temperature coefficient, which is negative for Si PiN diodes and positive for SiC Schottky diodes.

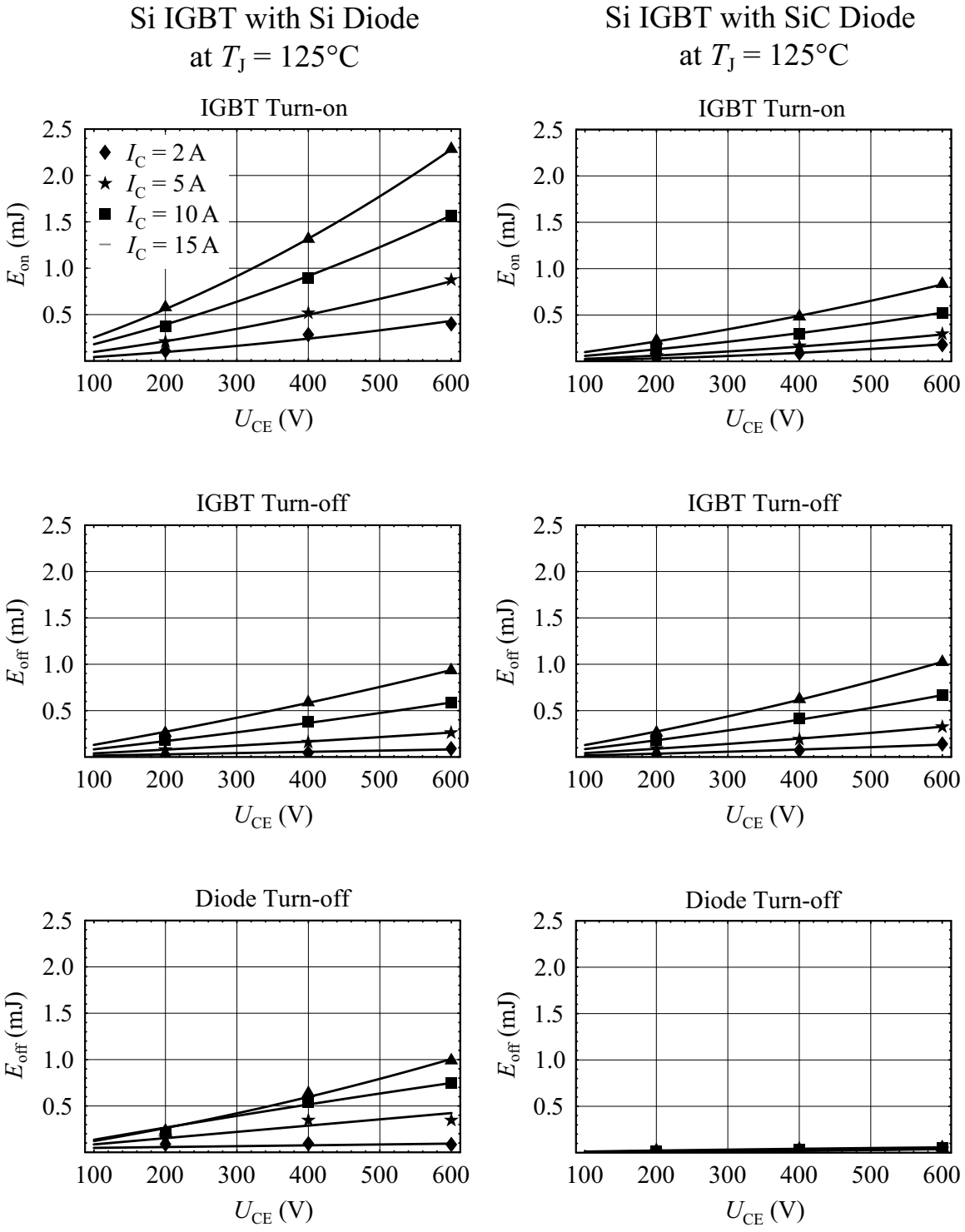


Fig. 2.19: Comparison of the switching losses of a Si IGBT and diode bridge-leg module (FII50-12E) with a custom module with SiC Schottky diodes (FII50-12E-SiC) at a junction temperature of $T_J = 125°C$.

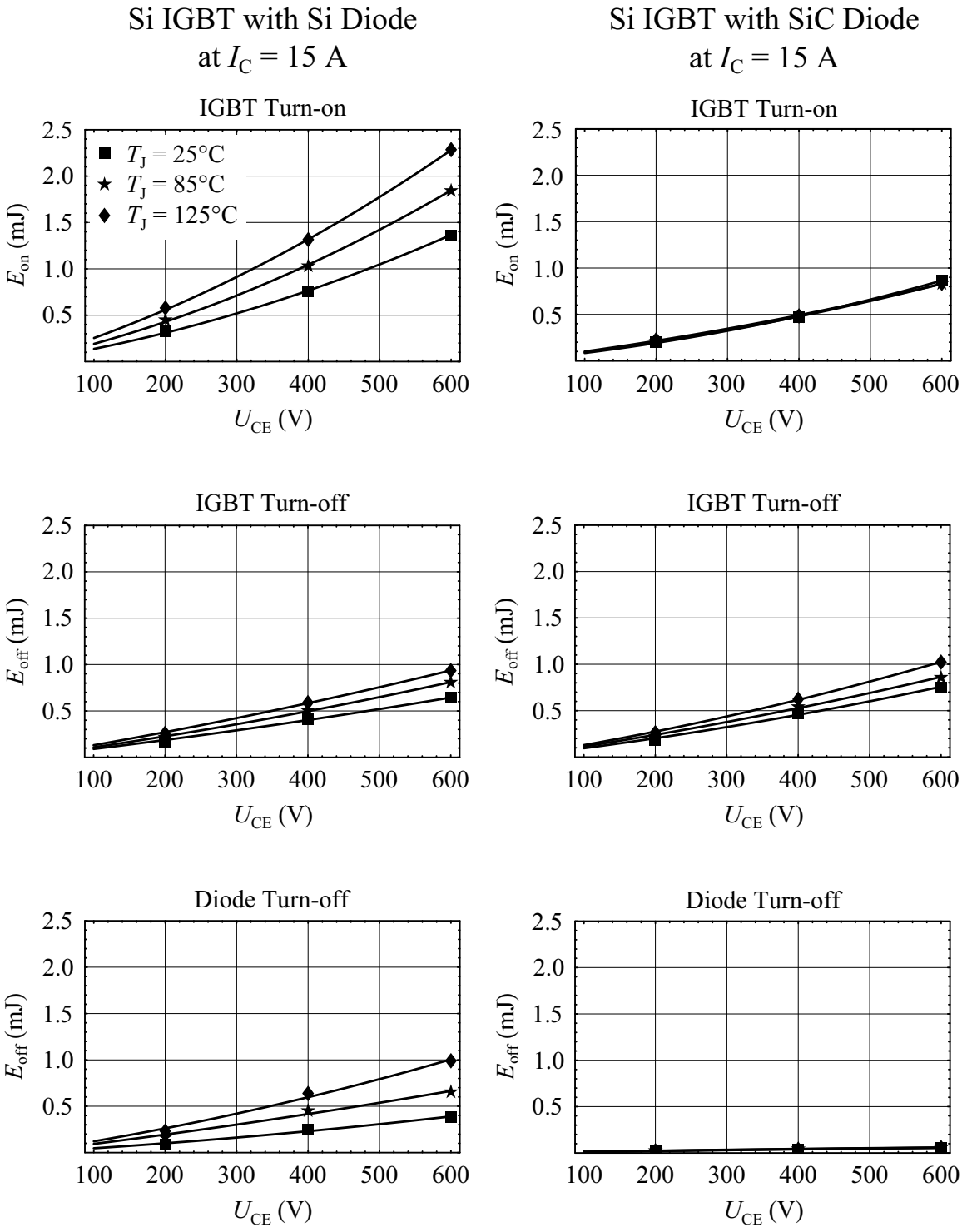


Fig. 2.20: Comparison of the switching losses of a Si IGBT and diode bridge-leg module (FII50-12E) with a custom module with SiC Schottky diodes (FII50-12E-SiC) at a switched current of $I_C = 15\,\mathrm{A}$.

2.5 Initial Semiconductor Technology Assessment

So far, two semiconductor configurations have been presented as an alternative to 1200 V Si IGBTs and Si diodes: Firstly, Si IGBTs with SiC diodes and secondly SiC JFETs. The question that arises is on how they compare or on how to assess the performance of different semiconductor devices and technologies.

For a given set of power devices with ideally similar blocking voltage, current rating, packaging, and cooling requirements the most straightforward method is to simply compare the conduction and switching losses. In practice, for a fixed blocking voltage class but different semiconductor technologies the ratings of the available devices vary, especially if prototype or pre-series devices are considered. Therefore, an adequate measure is required. For this purpose, the semiconductor chip area is introduced as an additional assessment quantity, as in the SFOM (cf. Sec. 2.1.2), since various device properties are determined by the chip area.

- The on-state resistance (voltage drop) decreases with an increasing chip area and thus, for a constant current, the conduction losses reduce.
- The thermal impedance between junction and case decreases with an increasing chip area and hence enhances the chip cooling.
- Consequently, the chip current handling capability rises with an increasing chip area.
- The device capacitances increase with an increasing chip area, leading to higher switching losses.
- The reliability of the device is declining for an increasing chip area.
- The chip cost is proportional to the chip area.

The most desirable power semiconductor chip technology would therefore enable minimal conduction and switching losses for a defined chip area when a certain voltage and current level is switched. These criteria form the basis of a measure for the semiconductor chip technology assessment suggested below. The FOM presented in (2.16) is formed by

the ratio of the conductivity G and the energy equivalent device output capacitance $C_{\mathrm{oss,eq}}(u_{\mathrm{sw}})$ for a given switched voltage level u_{sw}. The conductance accounts for the conduction losses and the output capacitance for the dynamic losses caused by the charging and discharging of the output capacitance. This modeling approach of the dynamic losses is suitable for switching devices or switching transients where the loss energy, caused by the overlapping of the voltage and current transients, is negligible. For typical transistors of ac-ac converters, such as IGBTs, this is not the case and the energy loss due to the overlapping of voltage and current during the switching transients needs to be considered. By simply replacing the energy equivalent device output capacitance $C_{\mathrm{oss,eq}}$ in (2.16) by the switching energy equivalent device capacitance $C_{\mathrm{sw,eq}}$, an extended total Figure-Of-Merit FOM_{semi} can be defined that allows modeling the total dynamic loss energy.

$$FOM_{\mathrm{semi}} = \frac{G(A_{\mathrm{chip,act}}, i_{\mathrm{cond}}, T_{\mathrm{J}})}{C_{\mathrm{sw,eq}}(A_{\mathrm{chip,act}}, i_{\mathrm{sw}}, u_{\mathrm{sw}}, T_{\mathrm{J}})} \tag{2.22}$$

The suggested FOM_{semi} represents the chip area specific ratio of the conduction to the switching losses. Both the conductance and the equivalent capacitance are determined for a defined active chip area $A_{\mathrm{chip,act}}$ and junction temperature T_{J} and depend on the average conducted current i_{cond}, the switched current i_{sw}, and the switched voltage u_{sw}. The switching energy equivalent capacitance equals to

$$C_{\mathrm{sw,eq}}(A_{\mathrm{chip,act}}, i_{\mathrm{sw}}, u_{\mathrm{sw}}, T_{\mathrm{J}}) = \frac{2\ (E_{\mathrm{on}} + E_{\mathrm{off}})}{U^2}\bigg|_{A_{\mathrm{chip,act}}, i_{\mathrm{sw}}, u_{\mathrm{sw}}} . \tag{2.23}$$

With the above figure-of-merit, four different 1200 V power device configurations suitable for ac-ac converters are assessed: third generation Si NPT3 IGBTs with anti-parallel Si HiPerFRED diodes (IXYS), latest (fourth) generation Si T&FS IGBTs with anti-parallel EmCon4 diodes (Infineon), Si NPT3 IGBTs with anti-parallel SiC Schottky diodes (custom module), and normally-on SiC JFETs (SiCED). In this comparison, the performance of the different switching devices is investigated for a half-bridge configuration as shown in Fig. 2.12(b) for a switched voltage of 600 V and a current level of 35 A. For the NPT3 IGBT devices, the data of the IXYS FII50-12E IGBT modules, analyzed in Sec. 2.4.3, is adopted. The loss data of the T&FS IGBT4 with EmCon4 diode are generated by evaluation of different 35 A power modules from Infineon.

The reference value for the active chip area equals 24 mm^2 and is determined by the T&FS IGBT4 chip. The active chip area of the NPT3 IGBT chip differs only by 4% from the reference value and is compensated by linear scaling of the semiconductor losses. As the active chip area of the considered normally-on SiC JFET is only 4 mm^2, six devices in parallel are assumed in this calculation and the loss data, presented in Sec. 2.4.2, is scaled accordingly. 1200 V Si MOSFETs are not included in this comparison as for the same chip area the considered current level of 35 A could not be conducted due to the comparatively high resulting on-resistance of approximately $R_{\mathrm{DS,on}} = 4.5\,\Omega$ at 25°C (cf. e.g. IXYS IXFP 3N120 MOSFET).

The resulting values of the FOM_{semi} are plotted versus the junction temperature in Fig. 2.21(a). The latest generation T&FS IGBTs perform better at least by 15% than the older NPT3 IGBTs. By replacing the Si HiPerFRED freewheeling diode of the FII50-12E module by SiC Schottky diodes, the FOM of the NPT3 IGBT can be raised by 60%. The normally-on SiC JFET outperforms the Si IGBT and diode technology at least by a factor of 7. If Si NPT3 IGBTs are combined with SiC Schottky diodes, the gain is reduced to a factor of 5. These performance indicators for 1200 V devices can be considered as a more realistic estimation than the results of the BFOM and the SFOM presented in Sec. 2.1.2, predicting a general SiC-to-Si switching device performance gain of approximately 20 to 50. To summarize, for a blocking voltage of 1200 V the normally-on SiC JFET considered are beneficial in terms of losses compared with currently available Si or hybrid Si transistor and SiC diode device configurations.

Finally, in Fig. 2.21(b), a comparison between the conductivity of the T&FS IGBT4 technology and the normally-on SiC JFET technology is presented, again for the same active power transistor chip area of 24 mm^2. Only for junction temperatures below 75°C the considered normally-on SiC JFET technology provides higher conductivity and thus lower conduction losses than the Si IGBT4 technology. This is obviously not an intrinsic limitation of the SiC JFET technology but is caused by the different temperature characteristics of unipolar (SiC JFET) and bipolar (Si IGBT) power devices and the actual design of the normally-on SiC JFET. Nevertheless, for ac-ac converters that are primarily sensitive to conduction losses, the considered normally-on SiC JFET might not provide the expected improvement especially if aiming for higher operating temperatures. With respect to Fig. 2.1, indicating

superior conductivity of SiC compared with Si, it might be desirable for a future generation of SiC JFETs to further optimize the devices for low on-state resistance at the expense of switching performance, in

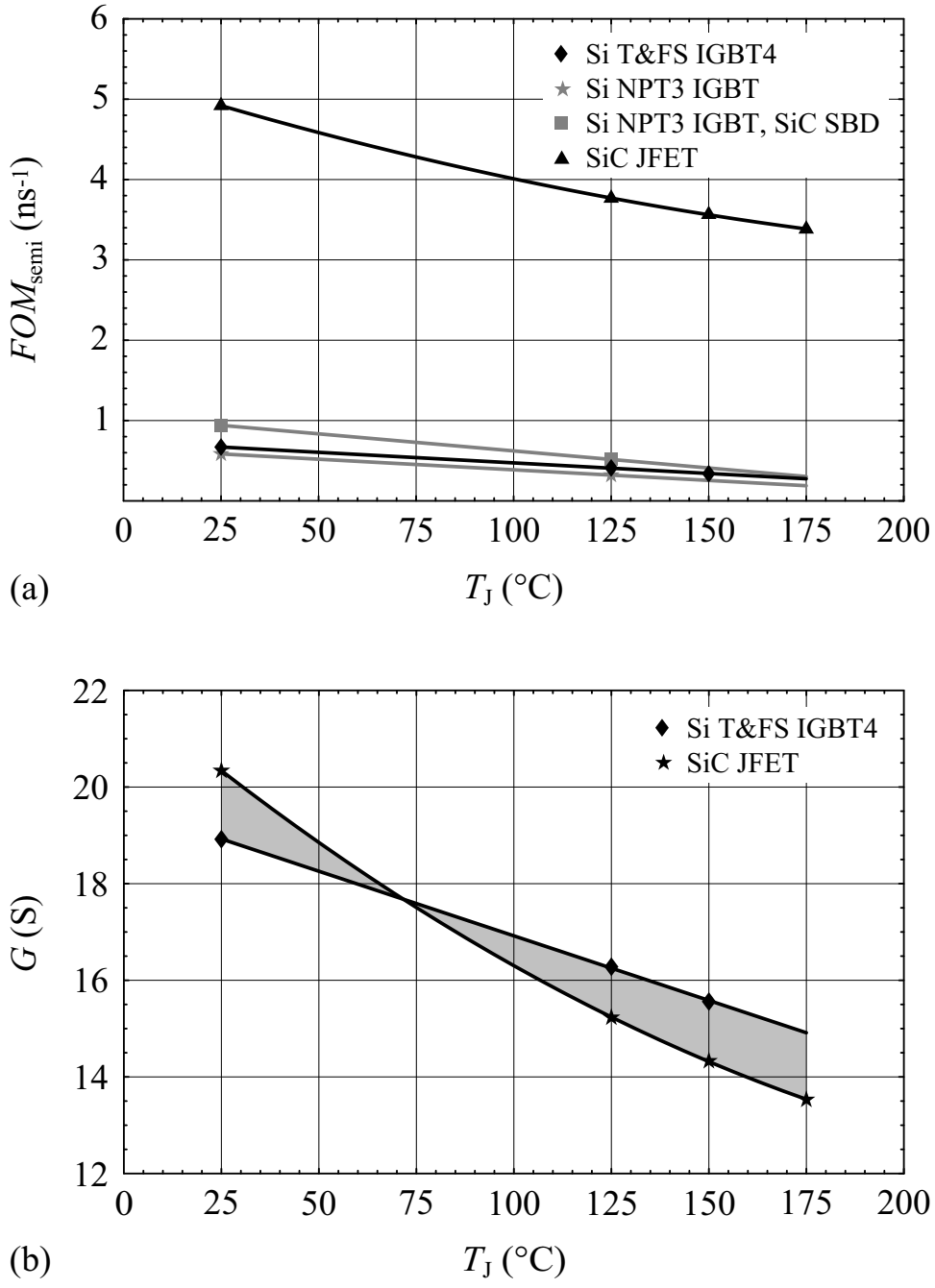


Fig. 2.21: Comparison of 1200 V power transistors and diodes with an active transistor chip area of 24 mm^2. **(a)** FOM_{semi} versus junction temperature T_{J} at a current level of 35 A and a switched voltage of 600 V. **(b)** Conductance G versus junction temperature T_{J} at 35 A.

order to outperform the conduction behavior of Si IGBTs at least in the temperature range from 25°C to 175°C for the same active chip area.

2.6 Semiconductor Cost

A key issue in the discussion of the application of SiC power switch technology is semiconductor costs. Unfortunately, a clearly defined price level for future commercial SiC power transistors has not yet been communicated by the semiconductor industry. The pricing pressure for SiC switching devices is enormous due to the well established Si technology with a vast variety of well-known and reliable devices. In Tab. 2.5, the approximate costs of the main commercially available power semiconductor technologies are summarized.

Semiconductor Technology	*Cost* ($/cm^2)	
	600 V	1200 V
Si T&FS IGBT	7	10.5
Si NPT IGBT	4.5	6
Si CoolMOS	14.5	15.5[a]
Si fast recovery PiN diode	3.5	4
SiC Schottky barrier diode	90	100

[a] 900 V CoolMOS transistor

Tab. 2.5: Overview of typical semiconductor costs per square centimeter for a blocking voltage of 600 V and 1200 V, provided by a semiconductor power module manufacturer (Sep. 2009).

2.7 Summary

For three-phase low-voltage ac-ac converters, power semiconductors with a blocking voltage capability of typically 1200 V are utilized. Currently available state-of-the-art 1200 V silicon power devices are Trench and Field-Stop and Soft-Punch-Through IGBTs and emitter-controlled diodes or diodes with a controlled axial lifetime.

A modified figure-of-merit for power semiconductors is suggested to compare the latest Si IGBTs (T&FS IGBT4) with the normally-on SiC JFETs provided by SiCED. With this figure-of-merit it is shown that for an equal active transistor chip area, the 1200 V normally-on SiC JFET is superior in terms of losses compared with latest generation Si IGBT and Si diode or hybrid Si IGBT and SiC diode configurations as long as the junction temperatures are below 75°C. However, contrary the popular belief, for junction temperatures above 75°C, the area specific (equivalent) on-resistance of the SiC JFET is higher than for the Si IGBT4, for instance. In conclusion, the difference in performance between the considered 1200 V Si IGBT4 devices and the normally-on SiC JFETs is not that significant, particularly not for industrial applications with switching frequencies where the total semiconductors losses are dominated by the conduction losses.

In order to test the normally-on SiC JFET in a circuit, a high-speed gate driver based on [249] is presented, which can provide the comparatively high negative voltage of −25 V to turn-off the JFET and handle different pinch-off voltage levels.

Additionally, a custom 1200 V IGBT phase-leg (half-bridge) module with anti-parallel SiC Schottky freewheeling diodes is developed to quantify the expected reduction of the switching losses. The contribution of this investigation is that the turn-on losses of the IGBT can be reduced by up to 60%, when the Si diodes are replaced by SiC Schottky diodes providing the same forward voltage drop at the nominal operating point as the Si diodes.

Chapter 3

Modulation and Control

The basic functionality, the electrical properties, and the semiconductor losses of ac-ac converters are significantly determined by the implemented modulation schemes. In this chapter, the space vector modulation schemes for the considered ac-ac converter topologies are briefly discussed and the resulting space vector diagrams are shown.

Based on the modulation of the VSBBC and CSBBC, the modulation scheme for the IMC is developed similar to the approach in [84], and a generalized description is provided, demonstrating the relationship between the VSBBC, the CSBBC, and the IMC topology. The modulation of the CMC is described by mapping the switching states of the IMC to the corresponding switching states of the CMC topology. Subsequently, the challenges regarding the commutation of the CMC are pinpointed, and the concepts of different multi-step commutation schemes are discussed.

Next, the relationship between the converter topology and its basic control structure is presented and an overview of the typically controlled converter system quantities is provided. Finally, the impact of the control on the design of the main energy storage (passive) components is discussed.

3.1 Modulation

3.1.1 Mains System Definition

For the considerations in this work, a symmetrical three-phase voltage-current mains system is assumed with a voltage amplitude $\hat{U}_1$, a current amplitude $\hat{I}_1$, and a current-to-voltage displacement angle Φ_1.

$$
\begin{aligned}
u_\mathrm{a} &= \hat{U}_1 \cos\left(\omega_1 t\right) \\
u_\mathrm{b} &= \hat{U}_1 \cos\left(\omega_1 t - \frac{2\pi}{3}\right) \\
u_\mathrm{c} &= \hat{U}_1 \cos\left(\omega_1 t + \frac{2\pi}{3}\right)
\end{aligned} \tag{3.1}
$$

$$
\begin{aligned}
i_\mathrm{a} &= \hat{I}_1 \cos\left(\omega_1 t - \Phi_1\right) \\
i_\mathrm{b} &= \hat{I}_1 \cos\left(\omega_1 t - \frac{2\pi}{3} - \Phi_1\right) \\
i_\mathrm{c} &= \hat{I}_1 \cos\left(\omega_1 t + \frac{2\pi}{3} - \Phi_1\right)
\end{aligned} \tag{3.2}
$$

3.1.2 Criteria for Modulation Schemes

The possible modulation schemes of the considered ac-ac converter topologies may differ, for instance, in terms of losses, harmonics, complexity, or involved transitions per switching cycle. In order to enable a fair comparison, it is hence essential to apply the same selection criteria for the modulation schemes. The following listing specifies the criteria with descending priority. The desired modulation scheme should:

- allow for low power semiconductor losses in the entire converter operating range,
- uniformly distribute the losses to the individual devices,
- minimize the number of required (lossy) switching transitions,
- enable safe commutation, and
- be beneficial regarding resulting EMI behavior.

3.1.3 Voltage Source Back-to-Back Converter

Various SVM schemes are known for voltage-source-type topologies. They are typically classified as symmetrical or full-wave symmetrical, discontinuous or half-wave symmetrical, and non-zero vector SVM [266–268]. The selected modulation scheme for the VSBBC is described by considering only the PWM VSI output stage. The switching function is defined by

$$s_i = 0, 1 \qquad\qquad i = A, B, C \tag{3.3}$$

according to the denomination of the switches in Fig. 3.1. In the following explanations, the safety interval (interlock delay) $T_{\mathrm{del}} > 0$ between the switching of the high-side switch $S_{\mathrm{p}i}$ and the low-side switch $S_{i\mathrm{n}}$ is neglected for simplification. The switching function $s_i = 1$ means that the corresponding output phase (A, B, C) is connected to the positive dc-bus p and $s_i = 0$ that the corresponding output phase is connected to the negative dc-bus n. Consequently, s_i can directly be considered as the control signal for the high-side switch $S_{\mathrm{p}i}$. $S_{\mathrm{p}i}$ is turned-on if $s_i = 1$ and turned-off if $s_i = 0$. The control signal for the low-side switch $S_{i\mathrm{n}}$ is generated by negation of s_i. The switching state of the VSI output stage can then be described by the triple $k = (s_{\mathrm{A}}, s_{\mathrm{B}}, s_{\mathrm{C}})$, formed by the switching functions of the individual output phases or alternatively by replacing s_i with the corresponding connection to the dc-bus p or n. The state (100), for instance, is then translated to (pnn), which is the naming convention utilized for further considerations.

The (two-level) VSI features $2^3 = 8$ switching states that form with the definition of the output voltage space vector

$$\begin{aligned}\vec{u}_{2,\mathrm{k}} &= \frac{2}{3}\left(u_{\mathrm{A},k} + \underline{a}u_{\mathrm{B},k} + \underline{a}^2 u_{\mathrm{C},k}\right) \\ &= \frac{2}{3}U\left(\left(s_{\mathrm{A}} - \frac{1}{2}\right) + \underline{a}\left(s_{\mathrm{B}} - \frac{1}{2}\right) + \underline{a}^2\left(s_{\mathrm{C}} - \frac{1}{2}\right)\right) \\ \underline{a} &= \mathrm{e}^{j\frac{2\pi}{3}}\end{aligned} \tag{3.4}$$

the space vector diagram depicted in Fig. 3.2(a). The switching states $\vec{u}_{2,(\mathrm{pnn})}$, $\vec{u}_{2,(\mathrm{ppn})}$, $\vec{u}_{2,(\mathrm{npn})}$, $\vec{u}_{2,(\mathrm{npp})}$, $\vec{u}_{2,(\mathrm{nnp})}$, and $\vec{u}_{2,(\mathrm{pnp})}$ are referred to as active states with a voltage space vector magnitude of $2/3\,U$ and $\vec{u}_{2,(\mathrm{nnn})}$ and $\vec{u}_{2,(\mathrm{ppp})}$ as zero or freewheeling states with a voltage space vector magnitude equal to zero. The reference output voltage space vector $\vec{u}_2^*$ is typically formed by two adjacent voltage vectors as shown

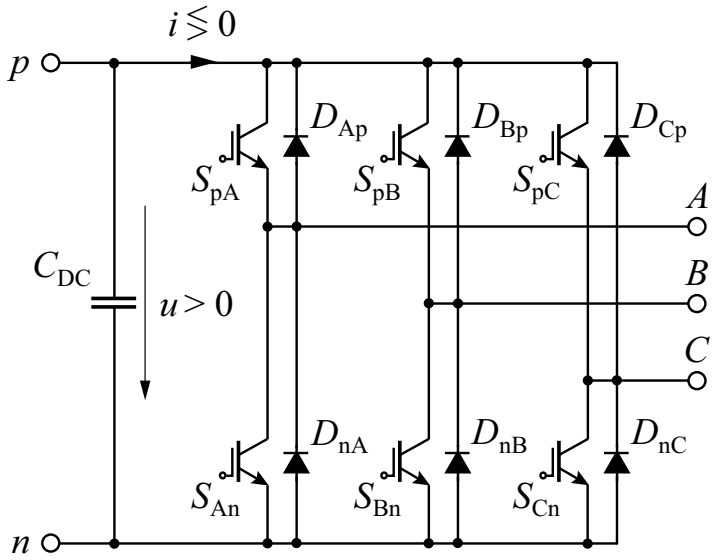


Fig. 3.1: Voltage Source Inverter (VSI) topology, showing the denomination of the transistors and the diodes.

in Fig. 3.2(b). For a general phase angle $\varphi_{\vec{u}_2^*}$ of $\vec{u}_2^*$ within the interval $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$, the reference output voltage vector can be calculated as

$$\begin{aligned}\vec{u}_2^* = \frac{1}{T_\mathrm{P}} \int_0^{T_\mathrm{P}} \vec{u}_{2,k}\, \mathrm{d}t_\kappa &= d_{(\mathrm{pnn})} \cdot \vec{u}_{2,(\mathrm{pnn})} + d_{(\mathrm{ppn})} \cdot \vec{u}_{2,(ppn)} + d_0 \cdot \vec{0} \\ &= d_{(\mathrm{pnn})} \frac{2}{3} U + d_{(\mathrm{ppn})} \frac{2}{3} U \mathrm{e}^{j\frac{\pi}{3}} \ , \end{aligned} \tag{3.5}$$

where t_κ refers to the local time within a pulse period T_P. The relative turn-on times $d_{(\mathrm{pnn})}$ and $d_{(\mathrm{ppn})}$ of the space vectors $\vec{u}_{2,(\mathrm{pnn})}$ and $\vec{u}_{2,(\mathrm{ppn})}$ with respect to T_P are given by

$$d_{(\mathrm{pnn})} = M_2 \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right) \tag{3.6}$$

$$d_{(\mathrm{ppn})} = M_2 \sin\left(\varphi_{\vec{u}_2^*}\right) \tag{3.7}$$

with the modulation index

$$M_2 = \frac{\hat{U}_2^*}{\frac{1}{\sqrt{3}} U} = [0 \ldots 1] \tag{3.8}$$

for sinusoidal modulation. During the remaining relative zero or freewheeling state interval

$$d_0 = d_{(\mathrm{nnn})} + d_{(\mathrm{ppp})} = 1 - \left(d_{(\mathrm{pnn})} + d_{(\mathrm{ppn})}\right) \tag{3.9}$$

the zero voltage space vectors $\vec{u}_{2,(\mathrm{ppp})}$ and/or $\vec{u}_{2,(\mathrm{nnn})}$ are applied. In summary, the desired output voltage vector $\vec{u}_2^*$ is formed by the dc-link voltage. Contrary to the voltage conversion the transformation of the output phase currents into the dc-link is determined not only by the output current amplitude $\hat{I}_2$, the switching state, and the modulation index M_2, but also by the phase displacement Φ_2 between $\vec{i}_2$ and $\vec{u}_2^*$. The mean value of the dc-link current is thus given by

$$i_{\mathrm{avg}} = I = \frac{3}{2\sqrt{3}} M_2 \hat{I}_2 \cos\left(\Phi_2\right) \ . \tag{3.10}$$

As the instantaneous sum of the modulated output terminal voltages referenced to ground ($u_{\mathrm{A},0}$, $u_{\mathrm{B},0}$, $u_{\mathrm{C},0}$) differs from zero, a zero sequence voltage is generated, which is referred to as common-mode (CM) voltage $u_{2,\mathrm{CM}}$.

$$u_{2,\mathrm{CM}} = \frac{1}{3}\left(u_{\mathrm{A},0} + u_{\mathrm{B},0} + u_{\mathrm{C},0}\right) \tag{3.11}$$

The following summary of modulation strategies is considered for a general phase angle $\varphi_{\vec{u}_2^*}$ of $\vec{u}_2^*$ within the interval $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$. The zero state time interval is equally distributed between the switching state (nnn) and (ppp) for symmetrical SVM, leading to the switching sequence

$$\begin{aligned} \ldots \Big|_{t_\kappa=0} (nnn) - (pnn) - (ppn) - (ppp) \Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} \\ (ppp) - (ppn) - (pnn) - (nnn) \Big|_{t_\kappa=T_\mathrm{P}} \ldots \end{aligned} \tag{3.12}$$

It is advantageous to reverse the switching sequence at half of the pulse period $T_\mathrm{P}/2$ to guarantee that only one bridge-leg needs to be switched, when the next voltage space vector is applied. Within a pulse period T_P six switching transitions are required. This strategy further allows the minimization of the CM voltage steps between the individual switching states.

In discontinuous or half-wave symmetrical SVM, only one of the two possible zero vectors is utilized. $\vec{u}_2^*$ is then formed by three instead of four voltage space vectors per pulse period compared with the symmetrical SVM. Thus, the number of switching transitions is reduced from six to four and therewith also the switching losses and the number of CM voltage pulses are lowered. The maximum amplitude of the CM

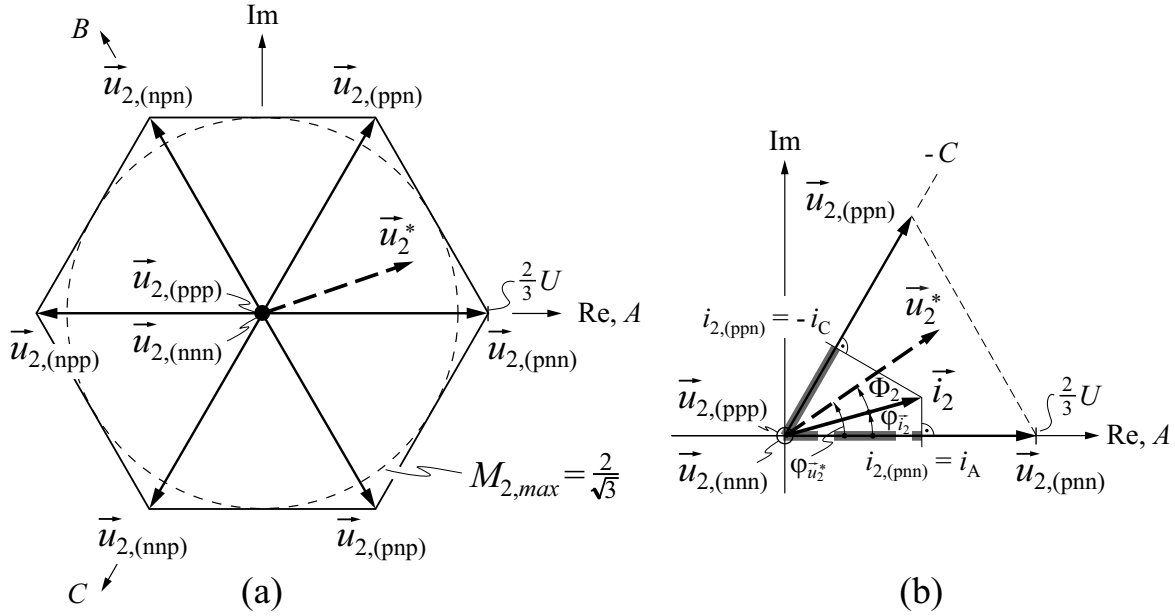


Fig. 3.2: (a) Space vector diagram for the VSI. **(b)** Voltage space vector sector showing the formation of the dc-link current i by projection of the current space vector $\vec{i}_2$ onto the instantaneous voltage space vectors $\vec{u}_{2,(\mathrm{pnn})}$ and $\vec{u}_{2,(\mathrm{ppn})}$.

voltages remains the same as for symmetrical SVM. Two different main switching sequences are possible

$$\ldots \Big|_{t_\kappa=0} (nnn) - (pnn) - (ppn) \Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} (ppn) - (pnn) - (nnn) \Big|_{t_\kappa=T_\mathrm{P}} \ldots \tag{3.13}$$

and

$$\ldots \Big|_{t_\kappa=0} (ppp) - (ppn) - (pnn) \Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} (pnn) - (ppn) - (ppp) \Big|_{t_\kappa=T_\mathrm{P}} \ldots , \tag{3.14}$$

whereas the switching sequence reversal at half of the pulse period is applied for the same reasons as stated above.

Another possibility to form the desired voltage space vector without any zero voltage vector is to apply two additional active vectors during the zero state interval that cancel each other [269]. A suitable switching

sequence to form $\vec{u}_2^*$ is

$$\ldots \Big|_{t_\kappa=0} (pnp) - (pnn) - (ppn) - (npn) \Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} (npn) - (ppn) - (pnn) - (pnp) \Big|_{t_\kappa=T_\mathrm{P}} \ldots \tag{3.15}$$

The advantage of this non-zero vector strategy is that the maximum CM voltages are limited to the voltage level of the active switching states [270]. However, similar to the symmetrical SVM six switching transitions occur within a pulse period.

The analysis in this research work is based on a discontinuous SVM scheme, formed by combining the sequence in (3.13) and (3.14), as this provides the best compromise between switching losses and CM voltage pulses. In this modulation scheme, the zero vector remains the same for an interval of $\pi/3$. For this purpose, the space vector diagram is subdivided into 12 instead of only 6 sectors as illustrated in Fig. 3.3(a). Within the gray shaded sectors the zero vector $\vec{u}_{2,(\mathrm{ppp})}$ is selected, whereas in the other sectors $\vec{u}_{2,(\mathrm{nnn})}$ is utilized. Assuming an output current-to-voltage phase displacement angle $\Phi_2 = 0$, it can be seen that for instance in the sectors I and XII, where the maximum current occurs in the output phase A, the bridge-leg connected to the phase A is not switched but clamped. Hence, the gray shaded sectors are also denoted as clamping sectors or intervals. The clamping of the bridge-leg conducting the largest current is beneficial in terms of reducing the switching losses. The resulting switching sequences are summarized in Tab. 3.1. The clamping sectors would then be shifted by $+\Phi_2$ for an output phase displacement different from zero, such as $\Phi_2 \approx \pi/6$, when supplying induction machines. Loss-optimal clamping may be achieved by steadily tracking Φ_2 and adapting the clamping interval boundaries. Fig. 3.3(b) depicts the space vector diagram for loss-optimal clamping with the modified sector boundaries, which is valid for $0 \leq \Phi_2 \leq \pi/6$.

The same discontinuous SVM scheme is utilized for the input stage (VSR) of the VSBBC as has been illustrated for the output stage (VSI). The modulation of the input and output stage is synchronized with a phase displacement $\varphi_\mathrm{mod} = 0$, such that the dc-link voltage ripple is minimized [271]. This leads to a center-alignment of the input and output stage pulse pattern. Contrary to the symmetrical SVM, where a minimum of the dc-link voltage ripple occurs at $\varphi_\mathrm{mod} = 0$ and $\varphi_\mathrm{mod} = \pi$, for the discontinuous SVM there is only one minimum at $\varphi_\mathrm{mod} = 0$.

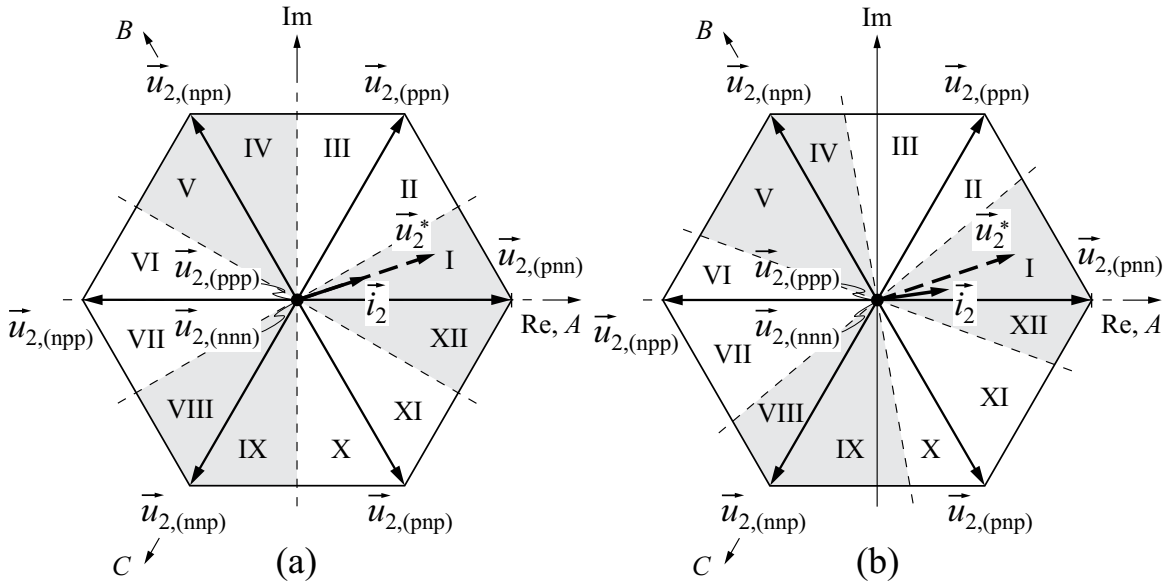


Fig. 3.3: Space vector diagram of the selected loss-optimal modulation scheme for the VSBBC, shown for the output stage **(a)** for $\Phi_2 = 0$ and **(b)** for $0 \leq \Phi_2 \leq \pi/6$.

Sector	*Switching Sequence* $(0 \ldots T_\mathrm{P})$
I	$\ldots (pnn) - (ppn) - (ppp) - (ppn) - (pnn) \ldots$
II	$\ldots (ppn) - (pnn) - (nnn) - (pnn) - (ppn) \ldots$
III	$\ldots (ppn) - (npn) - (nnn) - (npn) - (ppn) \ldots$
IV	$\ldots (npn) - (ppn) - (ppp) - (ppn) - (npn) \ldots$
V	$\ldots (npn) - (npp) - (ppp) - (npp) - (npn) \ldots$
VI	$\ldots (npp) - (npn) - (nnn) - (npn) - (npp) \ldots$
VII	$\ldots (npp) - (nnp) - (nnn) - (nnp) - (npp) \ldots$
VIII	$\ldots (nnp) - (npp) - (ppp) - (npp) - (nnp) \ldots$
IX	$\ldots (nnp) - (pnp) - (ppp) - (pnp) - (nnp) \ldots$
X	$\ldots (pnp) - (nnp) - (nnn) - (nnp) - (pnp) \ldots$
XI	$\ldots (pnp) - (pnn) - (nnn) - (pnn) - (pnp) \ldots$
XII	$\ldots (pnn) - (pnp) - (ppp) - (pnp) - (pnn) \ldots$

Tab. 3.1: Switching sequences of the selected loss-optimal modulation scheme for the VSBBC (cf. Fig. 3.3(a), shown for the output stage for $0 \leq \Phi_2 \leq \pi/6$.

3.1.4 Current Source Back-to-Back Converter

The considered SVM for the CSBBC is described by means of its input (rectifier) stage, as this facilitates later the explanation of the modulation for the IMC.

The switching state of the CSR is defined with $l = (xy)$, for example, based on the denomination of the individual switches as shown in Fig. 3.4. The first digit of l ("a") designates the input phase connected to the positive bus p, whereas the second digit ("b") designates the input phase connected to the negative bus n. The safety interval (over-lapping delay time) $T_{\mathrm{del}} < 0$ required to commutate the current between the individual phases is again neglected.

Compared with the previously presented VSI topology the CSR provides $3^2 = 9$ instead of eight switching states that can be represented with the corresponding input current space vector.

$$\vec{i}_{1,l} = \frac{2}{3}\left(i_{\mathrm{a},l} + \underline{a} i_{\mathrm{b},l} + \underline{a}^2 i_{\mathrm{c},l}\right) \tag{3.16}$$
$$\underline{a} = \mathrm{e}^{j\frac{2\pi}{3}}$$

The resulting input current space vector diagram is shown in Fig. 3.5(a). There are again active and zero states to be distinguished. The switching states forming the current space vectors $\vec{i}_{1,(\mathrm{ab})}$, $\vec{i}_{1,(\mathrm{ac})}$, $\vec{i}_{1,(\mathrm{bc})}$, $\vec{i}_{1,(\mathrm{ba})}$, $\vec{i}_{1,(\mathrm{ca})}$, and $\vec{i}_{1,(\mathrm{cb})}$ are denoted as active states with a space vector magnitude of $2/\sqrt{3}I$, and $\vec{i}_{1,(\mathrm{aa})}$, $\vec{i}_{1,(\mathrm{bb})}$, and $\vec{i}_{1,(\mathrm{cc})}$ are occurring for the zero states. The desired input voltage space vector $\vec{i}_1^{\,*}$ is then typically formed by two adjacent current vectors as depicted in Fig. 3.5(b). For a general phase angle $\varphi_{\vec{i}_1^{\,*}}$ of $\vec{i}_1^{\,*}$ within the interval $\varphi_{\vec{i}_1^{\,*}} \in [-\pi/6, \pi/6]$ the reference input current vector is given by

$$\begin{aligned}\vec{i}_1^{\,*} = \frac{1}{T_{\mathrm{P}}}\int_0^{T_{\mathrm{P}}} \vec{i}_{1,l}\,\mathrm{d}t_\kappa &= d_{(\mathrm{ab})}\cdot\vec{i}_{1,(\mathrm{ab})} + d_{(\mathrm{ac})}\cdot\vec{i}_{1,(ac)} + d_0\cdot\vec{0} \\ &= d_{(\mathrm{ab})}\frac{2}{\sqrt{3}}I\mathrm{e}^{-j\frac{\pi}{6}} + d_{(\mathrm{ac})}\frac{2}{\sqrt{3}}I\mathrm{e}^{j\frac{\pi}{6}}\ .\end{aligned} \tag{3.17}$$

The relative turn-on times $d_{(\mathrm{ab})}$, $d_{(\mathrm{ac})}$, and d_0 equal to

$$d_{(\mathrm{ab})} = M_1\cos\left(\varphi_{\vec{i}_1^{\,*}} + \frac{\pi}{3}\right) \tag{3.18}$$

$$d_{(\mathrm{ac})} = M_1\cos\left(\varphi_{\vec{i}_1^{\,*}} - \frac{\pi}{3}\right) \tag{3.19}$$

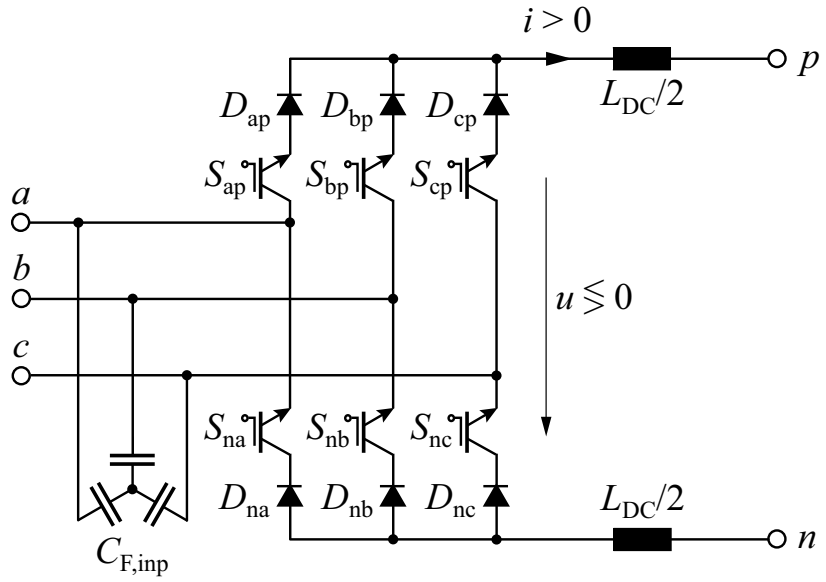


Fig. 3.4: Current Source Rectifier (CSR) topology, indicating the designation of the transistors and diodes.

$$d_0 = 1 - \left(d_{(\mathrm{ab})} + d_{(\mathrm{ac})}\right) \ . \tag{3.20}$$

The range of the modulation index M_1 for sinusoidal modulation is given by

$$M_1 = \frac{\hat{I}_1^*}{I} = [0 \ldots 1] \ . \tag{3.21}$$

It should be noted that the input (mains) current amplitude $\hat{I}_1^*$ and the phase displacement angle Φ_1^* are typically predefined in order to fulfill the converter power balance. The desired input current vector $\vec{i}_1^*$ is directly generated from the dc-link current. The output voltage (dc-link voltage) of the CSR depends on the input voltage amplitude $\hat{U}_1$, the switching state, the modulation index M_1, and the required phase displacement angle Φ_1^*. The mean value of the dc-link voltage equals to

$$u_{\mathrm{avg}} = \frac{3}{2} M_1 \hat{U}_1 \cos\left(\Phi_1^*\right) \ . \tag{3.22}$$

Similar to the VSI also for the CSR a CM voltage is generated at its output terminals across the link. Assuming that the star-point of the mains system at the input of the CSR and thus also the star-point of the input capacitors $C_{\mathrm{F,inp}}$ is at ground potential, the resulting CM voltage seen in the link can be written as

$$u_{\mathrm{CM,link}} = \frac{u_{\mathrm{p},0} + u_{\mathrm{n},0}}{2} \ , \tag{3.23}$$

where $u_{\mathrm{p},0}$ is the voltage between the positive bus and ground and $u_{\mathrm{n},0}$ the voltage between the negative bus and ground.

A variety of different modulation schemes for current source converters can be found in the literature [52,54,210,272], which are classified in a similar way as for voltage source converters. Basically in all these modulation strategies, usually two active vectors and one or two zero vectors are used per pulse period. The main differences between the individual modulation strategies are found in the number of switching transitions involved in one modulation cycle, the semiconductor losses, and the different dependencies between the semiconductor losses and the reference current-to-voltage displacement angle. Aiming for low switching losses, it is hence beneficial to keep a transistor in the on-state within a pulse period, which can be achieved by proper selection of the zero vector. This functionality is provided by the following three switching sequences, whereas (3.24) features two zero states and (3.25) and (3.26) only one.

$$\ldots \Big|_{t_\kappa=0} (ac) - (aa) - (ab) \Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} (ab) - (aa) - (ac) \Big|_{t_\kappa=T_\mathrm{P}} \ldots \quad (3.24)$$

$$\ldots \Big|_{t_\kappa=0} (ac) - (ab) - (aa) \Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} (aa) - (ab) - (ac) \Big|_{t_\kappa=T_\mathrm{P}} \ldots \quad (3.25)$$

$$\ldots \Big|_{t_\kappa=0} (ab) - (ac) - (aa) \Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} (aa) - (ac) - (ab) \Big|_{t_\kappa=T_\mathrm{P}} \ldots \quad (3.26)$$

Regarding the overall average losses, the modulation scheme based on (3.25) is the most desirable. The magnitude of the CM voltage of the zero state is maximal as the phase with the largest instantaneous voltage is clamped.

In the selected modulation scheme for the VSBBC, the switching losses are reduced by clamping the phase conducting the largest current. The same principle can be applied to the CSBBC. The switched current always equals the dc-link current for current source converters. Therefore, the clamping strategy cannot influence the switched current level but should minimize the commutation voltage, when the dc-link current is commutated from one phase to another. With this goal in mind an alternative switching sequence to (3.25) with the same average losses but a different zero state can be found

$$\ldots \Big|_{t_\kappa=0} (ac) - (ab) - (bb) \Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} (bb) - (ab) - (ac) \Big|_{t_\kappa=T_\mathrm{P}} \ldots , \quad (3.27)$$

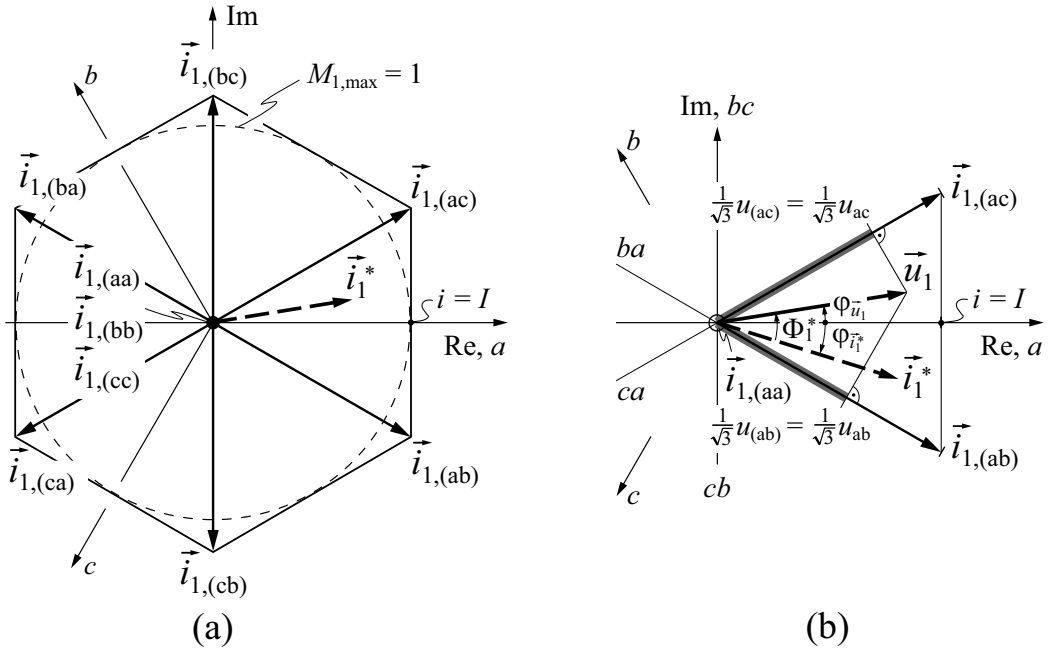


Fig. 3.5: (a) Space vector diagram for the CSR. **(b)** Current space vector sector showing the formation of the dc-link voltage u by projection of the voltage space vector $\vec{u}_1$ onto the instantaneous current space vectors $\vec{i}_{1,(\mathrm{ab})}$ and $\vec{i}_{1,(\mathrm{ac})}$.

leading to a lower magnitude of the zero state CM voltage. Nevertheless, by comparing the modulation schemes in (3.25) and (3.27), the resulting modulating scheme based on (3.25) provides a more uniform loss distribution and thus is selected for the CSBBC. For that purpose the current space vector diagram of the CSR, depicted in Fig. 3.6, is again subdivided into 12 sectors. Minimal switching losses can then be achieved by applying the switching sequence (3.25) to the sector I and mapping it accordingly to the other sectors. In the gray shaded sectors, the switch connecting the corresponding input phase with the positive bus is not switched, whereas in the other sectors the switch connecting the corresponding input phase with the negative bus is not switched.

Utilizing this modulation scheme, the magnitude of the average commutation voltage is formed in sector I, for example, by $|u_{\mathrm{ab}}|$ and $|u_{\mathrm{bc}}|$ and thus is minimized as the line-to-line voltage with the largest instantaneous magnitude $|u_{\mathrm{ac}}|$ does not appear as a commutation voltage, which corresponds to the clamping in the VSBBC. The resulting switching sequences are listed in Tab. 3.2. If the desired phase displacement Φ_1^* differs from zero, the sector boundaries can be shifted as is

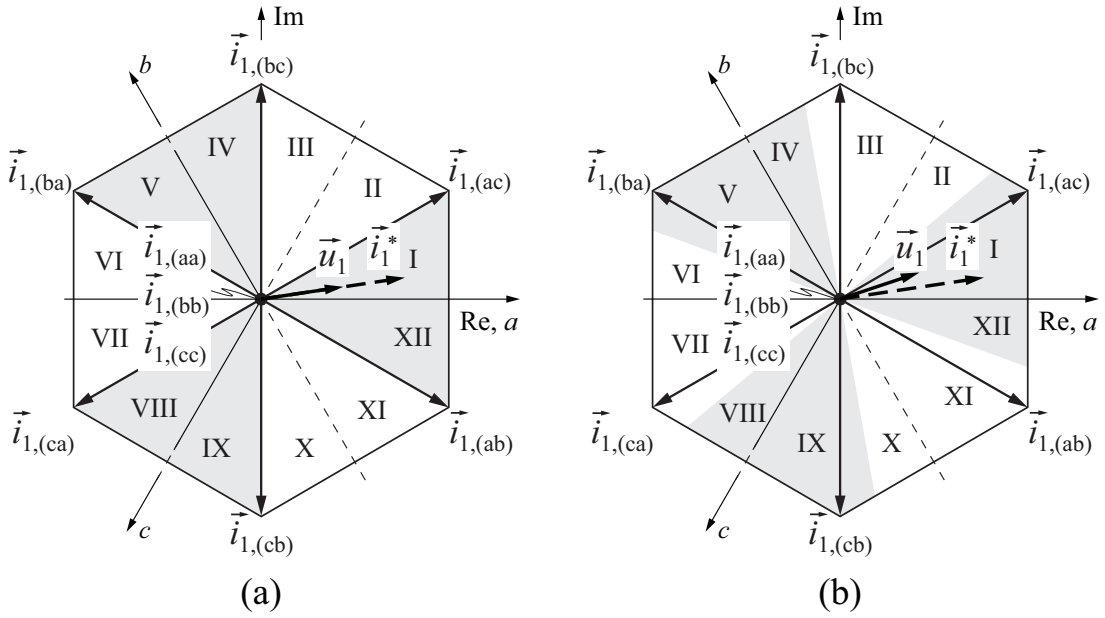


Fig. 3.6: Space vector diagram of the selected loss-optimal modulation scheme for the CSBBC, shown for the input stage **(a)** for $\Phi_1^* = 0$ and **(b)** for $0 \leq \Phi_1^* \leq \pi/6$.

Sector	*Switching Sequence* $(0 \ldots T_\mathrm{P})$
I	$\ldots(ac) - (ab) - (aa) - (ab) - (ac)\ldots$
II	$\ldots(ac) - (bc) - (cc) - (bc) - (ac)\ldots$
III	$\ldots(bc) - (ac) - (cc) - (ac) - (bc)\ldots$
IV	$\ldots(bc) - (ba) - (bb) - (ba) - (bc)\ldots$
V	$\ldots(ba) - (bc) - (bb) - (bc) - (ba)\ldots$
VI	$\ldots(ba) - (ca) - (aa) - (ca) - (ba)\ldots$
VII	$\ldots(ca) - (ba) - (aa) - (ba) - (ca)\ldots$
VIII	$\ldots(ca) - (cb) - (cc) - (cb) - (ca)\ldots$
IX	$\ldots(cb) - (ca) - (cc) - (ca) - (cb)\ldots$
X	$\ldots(cb) - (ab) - (bb) - (ab) - (cb)\ldots$
XI	$\ldots(ab) - (cb) - (bb) - (cb) - (ab)\ldots$
XII	$\ldots(ab) - (ac) - (aa) - (ac) - (ab)\ldots$

Tab. 3.2: Switching sequences of the selected loss-optimal modulation scheme of the CSBBC, shown for the input stage for $0 \leq \Phi_1^* \leq \pi/6$.

shown Fig. 3.5(b), in this case by $+\Phi_1^*$, to provide loss-optimal clamping [273] and to maintain the same level of switching losses. Analogous to the VSBBC, for the CSBBC the same SVM scheme is utilized for the output stage (CSI) as has been derived for the input stage (CSR). The modulation of both stages is also synchronized with a displacement angle $\varphi_{\mathrm{mod}} = 0$ in order to minimize the dc-link current ripple.

3.1.5 Indirect Matrix Converter

The SVM for the IMC is typically derived by a sequential approach, starting with calculating the voltage transformation from the converter input to the output to form a sinusoidal output voltage with the desired amplitude, followed by determining the current conversion from the output back to the input such that sinusoidal input currents are generated. A detailed description of various methods of derivation can be found in [131]. This section aims at providing an intuitive description of the modulation for the IMC based on the SVM of the current and voltage source converter as presented in [84].

With regard to its modulation, the IMC topology, depicted in Fig. 3.7, represents a combination of the input stage of the CSBBC, with the dc-link inductor shifted to the load (e.g. motor inductance), and the output stage of the VSBBC, with the dc-link capacitor shifted to the mains side (input capacitors $C_{\mathrm{F,inp}}$). For a given input voltage $\vec{u}_1$, the modulation of the converter is implemented such that only positive mains line-to-line voltages are switched to the link in order to prevent mains phase short-circuiting due to the polarity of the diodes of the output stage. The desired output voltage $\vec{u}_2^*$ is generated simultaneously with a sinusoidal input current $\vec{i}_1^*$ with a phase displacement angle Φ_1^* relative to $\vec{u}_1$. The input current amplitude is formed by the load current segments, which are transferred through the output stage and the link to the input, such that the power balance between input and output is fulfilled. Consequently, the resulting input current amplitude is determined by the load. On the converter input side, only the input current phase angle $\varphi_{\vec{i}_1^*}$ and therewith the input current-to-voltage displacement angle Φ_1^* may be actively controlled by the modulation.

In the following, the SVM of the IMC is described based on the space vector representation of current and voltage source converters. The modulation of the input stage is visualized by the space vector diagram of the CSR (cf. Fig. 3.8(a)) and the modulation of the output stage by the

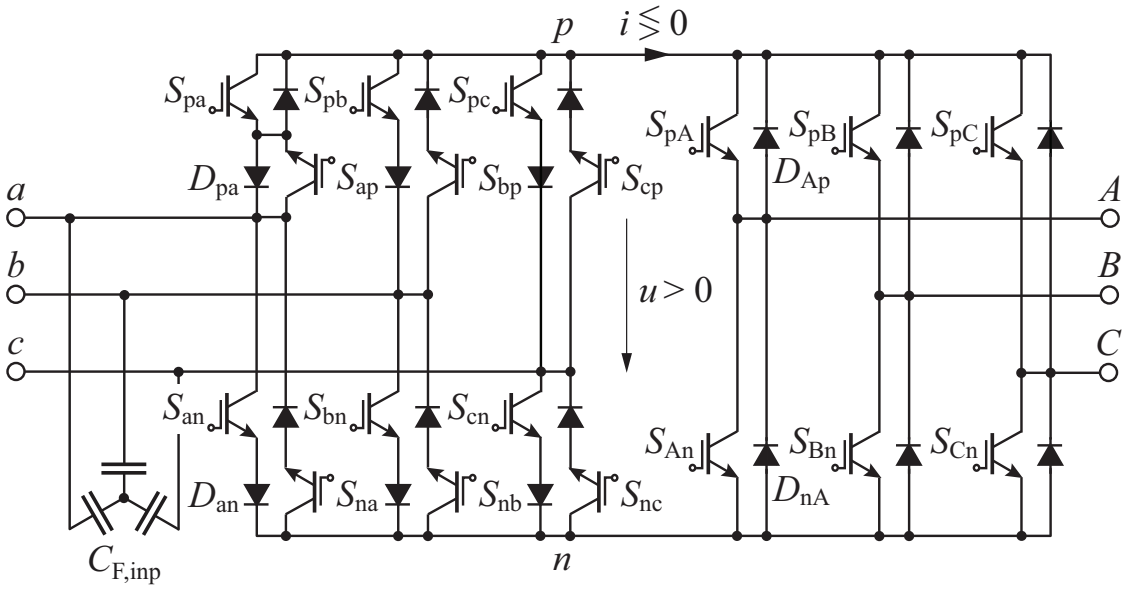


Fig. 3.7: Indirect Matrix Converter (IMC) topology, showing the denomination of the switching devices.

space vector diagram of the VSI (cf. Fig. 3.8(b)). For the explanation of the input-to-output voltage conversion, the phase angle at the input is limited to the interval $\varphi_{\vec{u}_1} \in [0, \pi/6]$. By projecting of $\vec{u}_1$ onto the space vector axes, the resulting link voltages can be found. Within the considered interval, positive dc-link voltages are generated for the switching states (ab), (ac), and (bc) of the input stage or correspondingly, for the line-to-line voltages u_{ab}, u_{ac}, and u_{bc}. For each of these link voltages, a space vector hexagon is formed for the output stage, whereas the size of the individual space vector hexagons changes with the instantaneous amplitude of the line-to-line voltages. This results in a total of 18 active output voltage vectors and different zero output voltage vectors. The zero voltage vector can be generated either only by the freewheeling states (nnn) or (ppp) of the output stage or only by the freewheeling states (aa), (bb), (cc) of the input stage or by combination of all. Thus, the IMC can provide up to three different output voltage levels. Contrary to a three-level voltage source converter, for the IMC the three voltage levels vary as a function of $\varphi_{\vec{u}_1}$. For example for $\varphi_{\vec{u}_1} = 0$, u_{ab} equals to u_{ac} and the outer two hexagons in Fig. 3.8(b) are congruent and thus only 12 active voltage vectors are available.

For the output-to-input current conversion, the consideration is restricted, in this case to the output current phase angle interval $\varphi_{\vec{i}_2} \in$

$[0, \pi/6]$ with $i_\mathrm{A} > 0$, $i_\mathrm{B} < 0$, and $i_\mathrm{C} < 0$. In this angle interval, positive link currents occur for the output stage switching states (pnn), (ppn), and (pnp) leading to $i_{(\mathrm{pnn})} = i_\mathrm{A}$, $i_{(\mathrm{ppn})} = -i_\mathrm{C}$, and $i_{(\mathrm{pnp})} = -i_\mathrm{B}$. Negative link currents are generated for the inverse output stage switching states (npp), (nnp), and (npn) leading to $i_{(\mathrm{npp})} = -i_\mathrm{A}$, $i_{(\mathrm{nnp})} = i_\mathrm{C}$, and $i_{(\mathrm{npn})} = i_\mathrm{B}$. Depending on the switching states of the input stage the link currents are translated into the corresponding input current space vectors, as shown in Fig. 3.8(a).

If the output stage is in the zero state (nnn) or (ppp), no link current and thus no input current is formed. The same applies to the zero states (aa), (bb), and (cc) of the input stage, which close the link current path across the input stage and thus prevent a current flow to the mains.

Finally, the desired output voltage vector $\vec{u}_2^*$ can be generated simultaneously with the desired input current phase angle $\varphi_{\vec{i}_1^*}$ through an appropriate combination of input and output stage switching states. $\varphi_{\vec{i}_1^*}$ is determined based on the phase angle $\varphi_{\vec{u}_1}$ of the input voltage $\vec{u}_1$ and the desired phase displacement angle Φ_1^*. In order to enable a continuous rotation of the input current space vector $\vec{i}_1$ and the output voltage space vector $\vec{u}_2^*$, at least two different active input stage and two different active output stage switching states and a zero state have to be combined in the switching sequence of the IMC. In order to obtain the maximal possible output voltage amplitude, the input switching states resulting in the largest (ac) and second largest (medium) (ab) instantaneous link voltage have to be selected. Consequently, in the considered intervals of the phase angles $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$ and $\varphi_{\vec{u}_2^*} \in [0, \pi/6]$, the resulting active switching states are $(ac)(ppn)$, $(ac)(pnn)$, $(ab)(ppn)$, $(ab)(pnn)$, with the zero states $(xx)(ppp)$ and $(xx)(nnn)$ or $(aa)(xxx)$, $(bb)(xxx)$, and $(cc)(xxx)$.

Two fundamentally different modulation schemes may be found for the IMC based on these switching states. In the standard modulation scheme, the input stage is first kept in the switching state (ac) while the output stage cycles through the switching state sequence $(pnn)-(ppn)-(ppp)$. Then, the input stage switching state is changed to (ab) and subsequently the same output stage switching state sequence is repeated, advantageously in reverse order $(ppp)-(ppn)-(pnn)$. Therewith, the first pulse half-period is completed and the same switching sequence is repeated in inverse order. Thus, for a complete switching sequence of the input stage, the switching sequence of the output stage

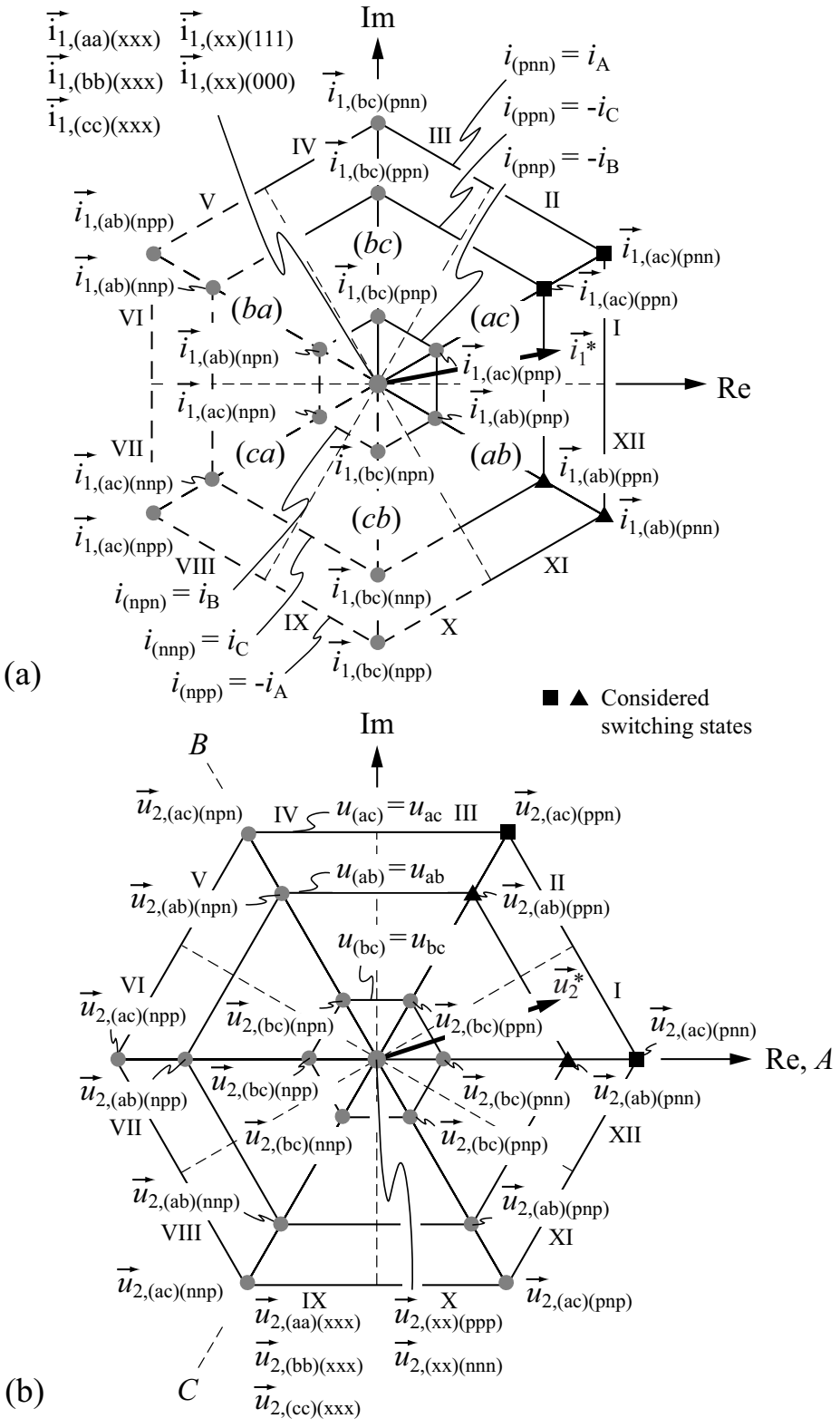


Fig. 3.8: Space vector diagrams of the IMC for **(a)** the input stage and **(b)** the output stage.

is run through twice for two different link voltage levels u_{ac} and u_{ab}. Accordingly, the switching frequency of the output stage is twice the switching frequency of the input stage. The resulting switching sequence may be written as

$$\begin{aligned}\ldots \Big|_{t_\kappa=0} &(ac)(pnn) - (ac)(ppn) - (ac)(ppp) - \\ &(ab)(ppp) - (ab)(ppn) - (ab)(pnn)\Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} \\ &(ab)(pnn) - (ab)(ppn) - (ab)(ppp) - \\ &(ac)(ppp) - (ac)(ppn) - (ac)(pnn)\Big|_{t_\kappa=T_\mathrm{P}} \ldots \end{aligned} \tag{3.28}$$

As can be seen in (3.28), the switching sequence of the output stage is embedded in the switching sequence of the input stage. The advantage of this modulation scheme is that the switching state of the input stage is changed during the freewheeling state of the output stage, i.e. when no current flows in the link. Consequently, Zero-Current-Switching (ZCS) of the input stage is enabled, and no switching losses occur in the input stage apart from losses due to component parasitics. The resulting link voltage and current waveforms are depicted in Fig. 3.9(a).

An alternative modulation scheme is given by interchanging the input and output stage switching cycle. Starting with the same input and output switching state $(ac)(pnn)$, the switching state of the output stage remains fixed while the input stage is cycled through the switching states $(ac)-(ab)-(aa)$. The switching state of the output stage is then changed from (pnn) to (ppn). Afterward, the input stage is cycled through the preceding switching sequence in reverse order $(aa)-(ab)-(ac)$, and the first pulse half-period ends. During the second half of the pulse period, the first half of the sequence is repeated in reverse order and results in

$$\begin{aligned}\ldots \Big|_{t_\kappa=0} &(ac)(pnn) - (ab)(pnn) - (aa)(pnn) - \\ &(aa)(ppn) - (ab)(ppn) - (ac)(ppn)\Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} \\ &(ac)(ppn) - (ab)(ppn) - (aa)(ppn) - \\ &(aa)(pnn) - (ab)(pnn) - (ac)(pnn)\Big|_{t_\kappa=T_\mathrm{P}} \ldots \end{aligned} \tag{3.29}$$

Surprisingly, this switching state sequence has not until recently [84,131] been described in literature for IMCs, despite its similarity to known

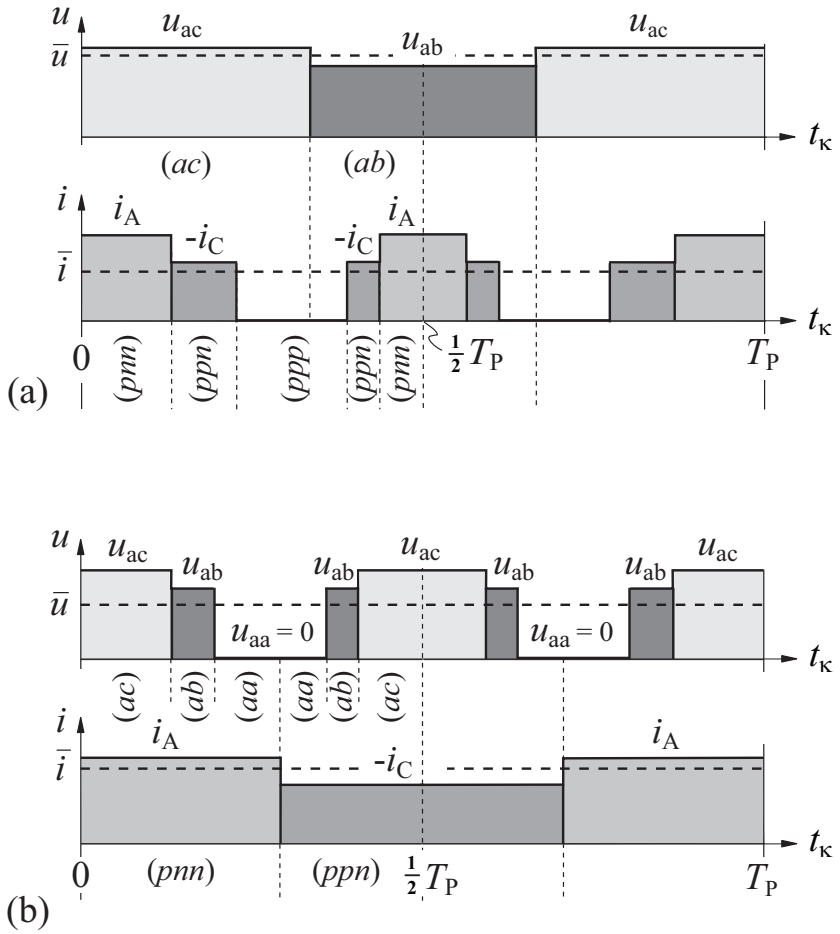


Fig. 3.9: Schematic representation of the link voltage u and link current i waveforms for the modulation scheme **(a)** enabling ZCS of the input stage (modulation strategy A), and **(b)** enabling ZVS of the output stage (modulation strategy B).

switching sequences for current source converters. Contrary to the ZCS modulation scheme, in the alternative modulation scheme the switching sequence of the input stage is embedded in the switching sequence of the output stage. The switching state of the output stage is changed within the freewheeling interval of the input stage and thus occurs at zero link voltage. The resulting link voltage and link current waveforms are depicted in Fig. 3.9(b). Switching losses in the output stage are avoided apart from losses resulting from component parasitics as a result of the Zero-Voltage-Switching (ZVS) strategy. The switching losses primarily occur in the input stage. However, the disadvantage with the ZVS modulation scheme is that a fairly intricate multi-step commutation scheme is required, to provide always a path for the link current and to prevent

short-circuiting of the mains input phases. The challenge with the ZVS modulation scheme can be best explained by comparison with a current source converter. The switching state transition of a CSR, for instance, is obtained by a strategy with overlapping commutation, whereas the overlapping of the turn-on and turn-off of the two switches in the commutation path ensures that there is always a path for the link current. Short-circuiting of the input phases cannot occur as the current source topology provides bipolar voltage blocking and unidirectional current flow. Contrary to the CSR, in the IMC overlapping commutation by turning on and turning off simultaneously both switches, forming the bidirectional switches in the commutation path, is not possible, as it would immediately lead to a short-circuit of a mains line-to-line voltage. Instead, a multi-step commutation, which typically involves four steps as there are four switches in the commutation path, has to be applied. An example of a four-step commutation scheme is provided in Tab. 3.3 for the switching transition $(ac)(pnn) - (ab)(pnn)$ of the sequence given in (3.29) for $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$, $\Phi_1^* \approx 0$, and $\varphi_{\vec{u}_2^*} \in [0, \pi/6]$. ("1" means that the corresponding switch is turned on, "0" that it is turned off.)

The switching sequence in this commutation scheme only depends on the measured converter input voltages. In the considered interval of the input current $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$, the input line-to-line voltage u_{bc} is positive ($u_{\mathrm{bc}} > 0$). The switch S_{nb} can then be turned on in the initial state (step 0), shown in Tab. 3.3, without changing the switching state of the converter. Correspondingly, also the switch S_{cn} in the last commutation step (step 4) may be turned on without affecting the switching state. This fact can be utilized to reduce the number of commutation steps and finally enables the implementation of a two-step commutation scheme, providing ZVS of the output stage for an IMC topology. The resulting switching sequence is presented in Tab. 3.4. The two-step commutation strategy is first described in [117] for the CMC.

For the implementation of the ZVS modulation scheme for a bidirectional IMC an input stage topology is required that allows for independent control of the switches for both current directions. Therefore, this modulation scheme cannot be applied to the VSMC. A special case regarding ZVS of the output stage is found with the unidirectional USMC. The functionality of its input stage is identical with a CSR as only unidirectional link currents are possible. Thus, the application of the ZVS modulation scheme for the USMC is simplified significantly. In this case,

the input stage of the USMC is modulated identically to a CSR with overlapping switch commutation. Hence, a multi-step commutation is not required.

Opposed to the ZVS modulation scheme, the application of the ZCS modulation scheme for an IMC is very simple and safe and can be directly implemented as shown in (3.28). Only a small interlock delay (safety time) is required to avoid short-circuiting of the mains phases as the bidirectional switches of the input stage can be switched at zero current, and the two switches forming a bidirectional switch can be

Switch	*Step* 0	*Step* 1	*Step* 2	*Step* 3	*Step* 4
S_{ap}	1	1	1	1	1
S_{pa}	1	1	1	1	1
S_{bn}	0	0	0	1	1
S_{nb}	0	1	1	1	1
S_{cn}	1	1	1	1	0
S_{nc}	1	1	0	0	0

Tab. 3.3: Standard four-step commutation for the ZVS modulation scheme, shown for the switching transition $(ac)(pnn) - (ab)(pnn)$ for $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$, $\Phi_1^* \approx 0$, and $\varphi_{\vec{u}_2^*} \in [0, \pi/6]$.

Switch	*Step* 0	*Step* 1	*Step* 2
S_{ap}	1	1	1
S_{pa}	1	1	1
S_{bn}	0	0	1
S_{nb}	**1**	1	1
S_{cn}	1	1	**1**
S_{nc}	1	0	0

Tab. 3.4: Suggested two-step commutation for the ZVS modulation scheme, shown for the switching transition $(ac)(pnn) - (ab)(pnn)$ for $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$, $\Phi_1^* \approx 0$, and $\varphi_{\vec{u}_2^*} \in [0, \pi/6]$. The highlighted switching signals do not affect the overall switching state of the converter.

turned on and turned off simultaneously. Likewise, the commutation of the output stage is unproblematic as simply an interlock delay between the high-side and low-side switch of a bridge-leg is required similar to voltage source converters. In conclusion, for a practical implementation of a bidirectional IMC, the ZCS modulation scheme is clearly preferred to the ZVS modulation scheme. Both modulation schemes lead approximately to the same complexity for the unidirectional USMC. Finally, it should be pointed out that for the ZVS modulation scheme an appropriate selection of the input stage power devices is essential. If the input stage is implemented with RB-IGBTs and the output stage with conventional IGBTs, as is a possible semiconductor configuration for IMCs, the application of the ZVS strategy for the output stage would lead to significantly higher losses than the ZCS strategy for the input stage, due to the rather unfavorable switching behavior of RB-IGBTs [167].

The resulting voltage and current transfer ratio of the IMC does not depend on whether the ZCS or ZVS modulation scheme is selected. The input-to-output voltage transformation can be determined by substituting (3.8), which describes the relationship between the link voltage and the output voltage of the VSI, into (3.22), which indicates the formation of the link voltage of the CSR as a function of the mains input voltage.

$$\hat{U}_2 = \frac{1}{\sqrt{3}} M_2 u_{\mathrm{avg}} = \frac{1}{\sqrt{3}} M_2 \frac{3}{2} M_1 \hat{U}_1 \cos\left(\Phi_1^*\right) = \frac{\sqrt{3}}{2} M_{12} \hat{U}_1 \cos\left(\Phi_1^*\right)$$
$$M_1 = [0 \ldots 1] \qquad M_2 = [0 \ldots 1] \qquad M_{12} = [0 \ldots 1] \tag{3.30}$$

The maximum output voltage of the IMC for sinusoidal modulation is obtained for $M_{12} = 1$ and $\Phi_1^* = 0$ and is limited to

$$\hat{U}_{2,\max} = \frac{\sqrt{3}}{2} \hat{U}_1 \ . \tag{3.31}$$

The output-to-input current transformation is calculated accordingly and can be written as

$$\hat{I}_1 = \frac{\sqrt{3}}{2} M_{12} \hat{I}_2 \cos\left(\Phi_2\right) \ . \tag{3.32}$$

As can be seen from (3.32), for a purely reactive load ($\Phi_2 = \pm\pi/2$) without any additional measures, no stationary input current can be formed ($\hat{I}_1 = 0$).

In the two basic modulation strategies considered so far, the output voltage is always formed with the largest and medium instantaneous line-to-line voltages in order to enable the formation of the maximum output voltage. This input voltage selection is hence referred to as High output Voltage SVM (HVSVM) scheme (Fig. 3.8, $\vec{i}_{1,(\mathrm{ac}),(\mathrm{xxx})}$, $\vec{i}_{1,(\mathrm{ab}),(\mathrm{xxx})}$, $\vec{u}_{2,(\mathrm{ac}),(\mathrm{xxx})}$, and $\vec{u}_{2,(\mathrm{ab}),(\mathrm{xxx})}$ for $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$ and $\Phi_1^* = 0$) and is applicable in the whole output voltage range.

$$\hat{U}_2 = \left[0 \ldots \frac{\sqrt{3}}{2}\right] \hat{U}_1 = [0\% \ldots 86.6\%]\, \hat{U}_1 \tag{3.33}$$

The resulting characteristic waveform of the link voltage is shown in Fig. 3.10(a). If only a reduced output voltage is required

$$\hat{U}_2 = \left[0 \ldots \frac{1}{2}\right] \hat{U}_1 = [0\% \ldots 50\%]\, \hat{U}_1 \ , \tag{3.34}$$

it is advantageous to select the medium and lowest positive instantaneous line-to-line voltages (Fig. 3.8, $\vec{i}_{1,(\mathrm{ab}),(\mathrm{xxx})}$, $\vec{i}_{1,(\mathrm{bc}),(\mathrm{xxx})}$, $\vec{u}_{2,(\mathrm{ab}),(\mathrm{xxx})}$, and $\vec{u}_{2,(\mathrm{bc}),(\mathrm{xxx})}$ for $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$ and $\Phi_1^* = 0$) to generate the output voltage, as the switching losses of the output stage are reduced. Additionally, the modulation index of the output stage has to be increased compared to the HVSVM, and thus the transistors and the freewheeling diodes of the converter output stage are more equally loaded for the same output voltage than with the HV modulation scheme. Correspondingly, this strategy is called Low output Voltage SVM (LVSVM) and leads to the link voltage according to Fig. 3.10(b). The disadvantages of the LVSVM are that the current ripple at the converter input is larger for $M_{12} > 0.2$ compared with the HVSVM [131]. Furthermore, the risk of input phase short-circuits is increased at the transitions $\varphi_1 = \{0, \pi/3, 2\pi/3, \pi, 4\pi/3, 5\pi/3\}$ for $\varphi_1 = \varphi_{\vec{i}_1^*} = \varphi_{\vec{u}_1}$, when the link voltage is close to zero ($u \approx 0$). Due to the voltage ripple across the input capacitors $C_{\mathrm{F,Inp}}$, the link voltage can temporarily become negative ($u < 0$) at these transitions, and the corresponding input phases are short-circuited across the freewheeling diodes of the output stage. This can be avoided if within a safety interval of $\pm 5^\circ$ at the critical transitions, the HVSVM scheme is applied. In order to reduce the output current ripple for output voltages in the range of

$$\hat{U}_2 = \left[\frac{1}{2} \ldots \frac{\sqrt{3}}{2}\right] \hat{U}_1 = [50\% \ldots 86.6\%]\, \hat{U}_1 \ , \tag{3.35}$$

all three line-to-line voltages can be utilized within a pulse period to form the desired output voltage vector (Fig. 3.8, $\vec{i}_{1,(\mathrm{ac}),(\mathrm{xxx})}$, $\vec{i}_{1,(\mathrm{ab}),(\mathrm{xxx})}$, $\vec{i}_{1,(\mathrm{bc}),(\mathrm{xxx})}$, $\vec{u}_{2,(\mathrm{ac}),(\mathrm{xxx})}$, $\vec{u}_{2,(\mathrm{ab}),(\mathrm{xxx})}$, and $\vec{u}_{2,(\mathrm{bc}),(\mathrm{xxx})}$ for $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$ and $\Phi_1^* = 0$). This modulation scheme enables to minimize the output current ripple by minimizing the freewheeling or zero vector intervals and is based on a combination of the HVSVM and LVSVM strategy. The resulting waveform of the link voltage is depicted in Fig. 3.10(c). This modulation scheme is referred to as Three-Level output voltage SVM (TLSVM) as three different link voltage levels are available to form the required output voltage and clearly demonstrates the "quasi three-level" characteristic of MCs [274].

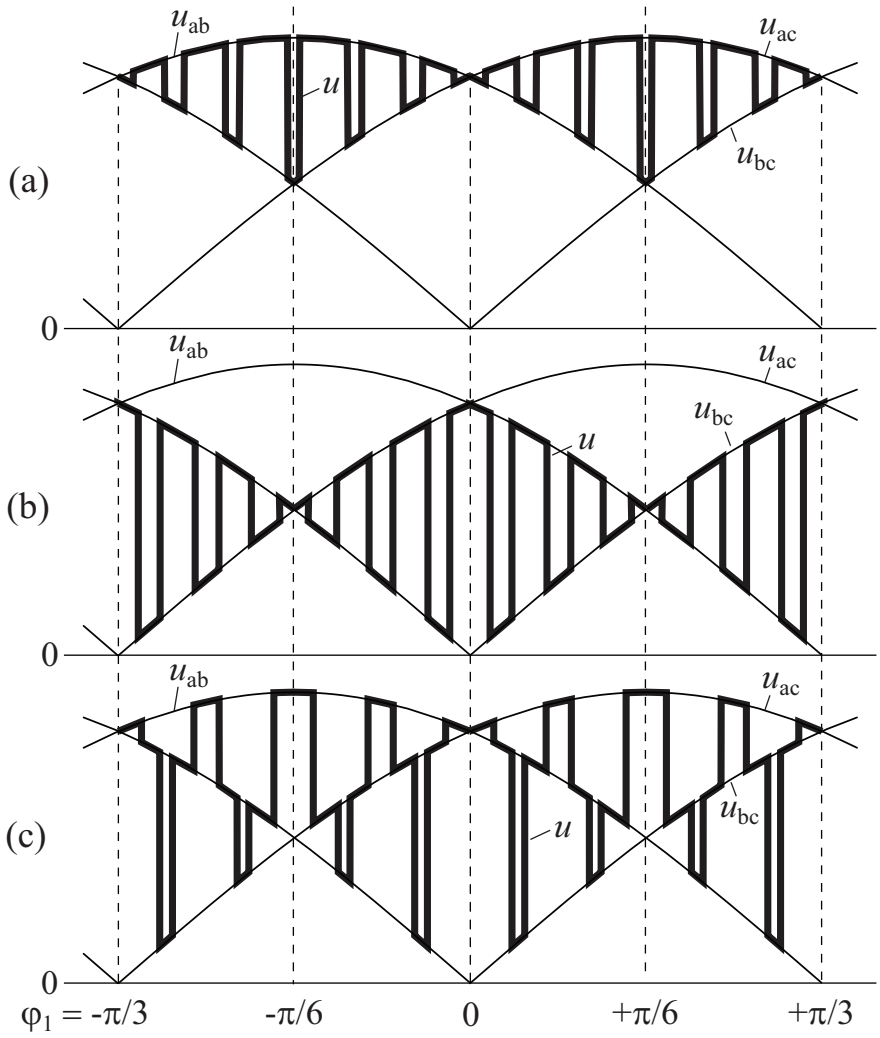


Fig. 3.10: Link voltage waveforms for the **(a)** HVSVM, **(b)** LVSVM, and **(c)** TLSVM for ZCS of the input stage ($\varphi_1 = \varphi_{\vec{i}_1^*} = \varphi_{\vec{u}_1}$).

Various combinations of the modulation and commutation schemes are possible to change the operating characteristics or to extend the operating range of IMCs. In the following, several extended and alternative modulation schemes are briefly introduced. An overview of the most important SVM schemes is compiled in Tab. 3.5.

The Switching Loss Shifting (SLS) modulation strategy [127] aims at balancing the switching losses between the input and output stage. If the IMC, for instance, is operated with the ZCS strategy of the input stage, switching losses are only generated in the output stage. This leads to a non-uniform semiconductor loss distribution. In the SLS modulation scheme, a part of the commutations generating switching losses is performed such that the switching losses do not any more occur in the output stage but in the input stage. The shifting of the losses is achieved by initiating and terminating the freewheeling state of the output stage by means of switching the corresponding switches of the input stage at current. This switching strategy is only possible for positive link currents $i > 0$ and thus restricts the application of the SLS strategy to loads leading to a phase displacement angle at the output of $|\Phi_2| \leq \pi/6$.

As an alternative to the modulation schemes enabling ZCS of the input stage or ZVS of the output stage, also modulation schemes that were originally developed for the CMC and hence require a multi-step commutation scheme can be applied to the IMC. Such a modulation scheme is the so-called Conventional Space Vector Modulation (CSVM). The switching sequence of the CSVM is designed based on the optimization rules presented in [275] to minimize the number of commutations per switching state transitions. The resulting switching sequence for $\varphi_{\vec{i}_1^*} \in [0, \pi/3]$, $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$, and $\Phi_1^* = 0$ is

$$\begin{aligned} \ldots \Big|_{t_\kappa=0} & (ab)(pnn) - (ab)(ppn) - (ac)(ppn) - \\ & (ac)(pnn) - (ac)(nnn) \Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} \\ & (ac)(nnn) - (ac)(pnn) - (ac)(ppn) - \\ & (ab)(ppn) - (ab)(pnn) \Big|_{t_\kappa=T_\mathrm{P}} \ldots \end{aligned} \tag{3.36}$$

As can be seen from the switching sequence in (3.36), for the CSVM the switching losses occur in the input and the output stage and thus the power semiconductors are more evenly loaded compared with the HV- or LVSVM.

An Improved Space Vector Modulation (ISVM), providing a lower maximum CM voltage compared to the CSVM, is suggested in [276]. The ISVM is based on the CSVM, and for $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$ $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$, and $\Phi_1^* = 0$, the switching sequence is identical to (3.36). However, for $\varphi_{\vec{i}_1^*} \in [\pi/6, \pi/3]$ and $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$ the switching sequence is then changed to

$$\begin{aligned} \ldots \Big|_{t_\kappa=0} & (ab)(nnn) - (ab)(pnn) - (ab)(ppn) - \\ & (ac)(ppn) - (ac)(pnn) \Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} \\ & (ac)(pnn) - (ac)(ppn) - (ab)(ppn) - \\ & (ab)(pnn) - (ab)(nnn) \Big|_{t_\kappa=T_\mathrm{P}} \ldots \end{aligned} \tag{3.37}$$

Thus, the zero states in the ISVM are generated using always the input voltage with the medium instantaneous magnitude, and therewith, the maximum CM voltage is lowered. In addition to the CM voltage reduction, the ISVM leads to lower switching losses.

Another possibility to limit the CM voltage to the maximum voltage of the active states is to use no zero states [177]. This modulation scheme is referred to as Non-Zero Space Vector Modulation (NZSVM). It is derived from the CSVM, whereas the zero state interval is subdivided into three intervals. The switching sequence of the NZSVM for $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$, $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$, and $\Phi_1^* = 0$ then equals to

$$\begin{aligned} \ldots \Big|_{t_\kappa=0} & (cb)(pnn) - (ab)(pnn) - (ab)(ppn) - \\ & (ac)(ppn) - (ac)(pnn) - (bc)(pnn) \Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} \\ & (bc)(pnn) - (ac)(pnn) - (ac)(ppn) - \\ & (ab)(ppn) - (ab)(pnn) - (cb)(pnn) \Big|_{t_\kappa=T_\mathrm{P}} \ldots \end{aligned} \tag{3.38}$$

The main disadvantage of the NZSVM is the increased number of switching transitions compared with the CSVM or the ISVM, as a pulse period consists of 11 instead of only 9 different states.

Basically, the input current of MCs is proportional to the real output power, as can be seen from (3.32). Thus, also the reactive power at the converter input depends on the real output power. The Reactive

Power SVM (RPSVM) schemes, presented in [128], enable to generate reactive power at the converter input for a purely reactive load or to generate reactive power at the converter input for a real load. The basic principle is to utilize the fundamental feature of MCs that enables to separate the formation of the desired output voltage space vector $\vec{u}_2^*$ from the formation of the desired input current space vector $\vec{i}_1^*$. In this way, the switching sequence is subdivided into two intervals, where in one interval the required output voltage with an average input current equal to zero is generated, and in the other interval the required reactive input current is formed with an average output voltage equal to zero.

Unfortunately, the extended converter functionality such as the reduction of the CM voltage with the ISVM or the reactive power transfer with the RPSVM is achieved at higher complexity and lower robustness of the modulation or commutation scheme. Therefore, for a practical implementation of a bidirectional IMC, the HV strategy with ZCS of

Modulation Scheme	*Reference*
High Voltage SVM (HVSVM)	
- ZCS of input stage	[84, 92]
- ZVS of output stage[a]	[84, 277]
- SLS between input and output stage	[127, 131]
Low Voltage SVM (LVSVM)	
- ZCS of input stage	[127]
- ZVS of output stage[a]	[131]
- SLS between input and output stage	[127, 131]
Three-Level SVM (TLSVM)	
- ZCS of input stage	[131, 274]
- ZVS of output stage[a]	[131]
Conventional SVM (CSVM)[a]	[275, 278]
Improved SVM (ISVM)[a]	[276, 278]
Non-Zero SVM (NZSVM)[a]	[177, 278]
Reactive Power SVM (RPSVM)	[128, 131, 279]

[a] Requires a specific (multi-step) commutation scheme.

Tab. 3.5: Overview of modulation schemes for IMCs.

the input stage (HVZCS) provides the best compromise, as it covers the entire output voltage range at low losses and enables a simple and safe commutation and implementation. Therefore, it is defined as the reference modulation scheme for the IMC in this research work. The only limitation of the HVZCS modulation scheme is that a minimal duration of the freewheeling interval of the output stage is required to enable a safe commutation of the input stage. In practice, the maximum modulation index thus must be limited to $M_{12,\max} \approx 98\%$, which leads to a small reduction of the maximum attainable output voltage.

Regarding the clamping strategy for the output stage, two main possibilities exist. Firstly, the same loss-optimal clamping may be utilized as shown for the VSI. Alternatively, the clamping of the output stage can be synchronized with the phase $\varphi_{\vec{u}_1}$ of the input voltage. This enables to minimize the CM voltage generated by the IMC, and hence is referred to as CM-optimal clamping. The zero states (nnn) and (ppp) of the output stage can then be determined as shown in Tab. 3.6. According to [131], the CM-optimal clamping allows for a reduction of the rms value of the CM voltage only by 6% and leads to an increase in the total average semiconductor losses. As efficiency is given higher priority for the selection of the modulation scheme than the generated CM voltage, the loss-optimal clamping is favored and the CM-optimal clamping is considered as an additional option at low output frequencies to reduce the locale average semiconductor losses. To conclude with, the following relationship between the clamping strategy of the CSR, VSI, and IMC

$\varphi_{\vec{u}_1}$	*Zero State*
$[0 \ldots \pi/6]$	(ppp)
$[\pi/6 \ldots \pi/2]$	(nnn)
$[\pi/2 \ldots 5\pi/6]$	(ppp)
$[5\pi/6 \ldots 7\pi/6]$	(nnn)
$[7\pi/6 \ldots 3\pi/2]$	(ppp)
$[3\pi/2 \ldots 11\pi/6]$	(nnn)
$[11\pi/6 \ldots 0]$	(ppp)

Tab. 3.6: Zero states of the output stage for the HVZCS modulation scheme with CM-optimal clamping.

shall be mentioned. The loss-optimal clamping strategy of the VSI (cf. Tab. 3.1), results also in loss-optimal clamping for the IMC (at maximum output voltage), whereas the optimal clamping of the CSR (cf. Tab. 3.2), applied to the output stage of the IMC, leads to CM-optimal clamping.

The relative turn-on times of the HV modulation scheme for sinusoidal SVM can be determined based on the relative turn-on times of the CSR and VSI, given in (3.6), (3.7), (3.18), and (3.19). Compared to the CSR and VSI, the switching sequence of the IMC features four different active states (cf. Fig. 3.9) instead of only two. Therefore, also four different turn-on times are required apart from the zero state. The relative turn-on times of the IMC can be directly calculated by combination and multiplication of the relative turn-on times of the CSR and VSI as the IMC topology consists of a CSR input stage and a VSI output stage. By utilizing the definition for M_{12} according to (3.30) and assuming that Φ_1^* equals to zero, the relative turn-on times of the active states for $\varphi_{\vec{i}_1^*} \in [-\pi/6, \pi/6]$ and $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$ can be calculated to

$$d_{(\mathrm{ac})(\mathrm{pnn})} = M_{12} \cos\left(\varphi_{\vec{i}_1^*} - \frac{\pi}{3}\right) \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right) \tag{3.39}$$

$$d_{(\mathrm{ac})(\mathrm{ppn})} = M_{12} \cos\left(\varphi_{\vec{i}_1^*} - \frac{\pi}{3}\right) \sin\left(\varphi_{\vec{u}_2^*}\right) \tag{3.40}$$

$$d_{(\mathrm{ab})(\mathrm{ppn})} = M_{12} \cos\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{3}\right) \sin\left(\varphi_{\vec{u}_2^*}\right) \tag{3.41}$$

$$d_{(\mathrm{ab})(\mathrm{pnn})} = M_{12} \underbrace{\cos\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{3}\right)}_{\text{from CSR}} \underbrace{\cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right)}_{\text{from VSI}} . \tag{3.42}$$

The remaining relative zero state or freewheeling time then equals to

$$\begin{aligned} d_0 &= d_{(\mathrm{ac})(\mathrm{ppp})} + d_{(\mathrm{ab})(\mathrm{ppp})} \\ &= 1 - \left(d_{(\mathrm{ac})(\mathrm{pnn})} + d_{(\mathrm{ac})(\mathrm{ppn})} + d_{(\mathrm{ab})(\mathrm{ppn})} + d_{(\mathrm{ab})(\mathrm{pnn})}\right) \geq 0 . \end{aligned} \tag{3.43}$$

It does not matter when within the freewheeling interval the switching state of the input stage is changed, since during this interval the output voltage equals to zero. The total freewheeling time is typically equally distributed between the two input states of a switching sequence.

$$d_{(\mathrm{ac})(\mathrm{ppp})} = d_{(\mathrm{ab})(\mathrm{ppp})} = \frac{d_0}{2} \tag{3.44}$$

If Φ_1^* differs from zero, the relative turn-on times are modified according to (3.30) and may be written as

$$\begin{aligned} d_{(\mathrm{ac})(\mathrm{pnn})} &= \frac{M_{12}}{\cos\left(\Phi_1^*\right)} \cos\left(\varphi_{\vec{i}_1^*} - \frac{\pi}{3}\right) \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right) \\ &= \frac{M_{12}}{\cos\left(\Phi_1^*\right)} \sin\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{6}\right) \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right) \qquad (3.45) \\ d_{(\mathrm{ac})(\mathrm{ppn})} &= \frac{M_{12}}{\cos\left(\Phi_1^*\right)} \cos\left(\varphi_{\vec{i}_1^*} - \frac{\pi}{3}\right) \sin\left(\varphi_{\vec{u}_2^*}\right) \\ &= \frac{M_{12}}{\cos\left(\Phi_1^*\right)} \sin\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{6}\right) \sin\left(\varphi_{\vec{u}_2^*}\right) \qquad (3.46) \\ d_{(\mathrm{ab})(\mathrm{ppn})} &= \frac{M_{12}}{\cos\left(\Phi_1^*\right)} \cos\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{3}\right) \sin\left(\varphi_{\vec{u}_2^*}\right) \\ &= \frac{M_{12}}{\cos\left(\Phi_1^*\right)} \sin\left(\varphi_{\vec{i}_1^*} - \frac{\pi}{6}\right) \sin\left(\varphi_{\vec{u}_2^*}\right) \qquad (3.47) \\ d_{(\mathrm{ab})(\mathrm{pnn})} &= \frac{M_{12}}{\cos\left(\Phi_1^*\right)} \cos\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{3}\right) \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right) \\ &= \frac{M_{12}}{\cos\left(\Phi_1^*\right)} \sin\left(\varphi_{\vec{i}_1^*} - \frac{\pi}{6}\right) \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right) . \qquad (3.48) \end{aligned}$$

Φ_1^* cannot be arbitrarily chosen as for $|\Phi_1^*| > \pi/6$ the link voltage can temporarily become negative ($u < 0$), which would result in a short-circuit of the input phases that are connected to the link. (3.45) to (3.48) are only valid for $|\Phi_1^*| \leq \pi/6$. An extension of the operating range to $|\Phi_1^*| > \pi/6$ can be achieved by inversion of the switching states of the output state, which is explained in detail in [131].

The derivation of (3.39) to (3.42) for the relative turn-on times can be verified by the following consideration. First, $\varphi_{\vec{i}_1^*}$ and $\varphi_{\vec{u}_2^*}$ are assumed to be constant within the intervals given above, and the corresponding input current space vector $\vec{i}_1^*$ and output voltage space vector $\vec{u}_2^*$ is formed. Next, $\varphi_{\vec{u}_2^*}$ is still kept constant and $\varphi_{\vec{i}_1^*}$ is varied within the interval $[-\pi/6, \pi/6]$. In order to keep on generating the same output voltage space vector with a constant magnitude, the resulting average link voltage of the active states should remain constant. This corresponds exactly to the conditions of the link voltage of a CSR and is represented by the cosine terms labeled with "from CSR" in (3.39) to (3.42). The formation of the link voltage is depicted in Fig. 3.11. If the average link voltage of the active states is now assumed to be constant

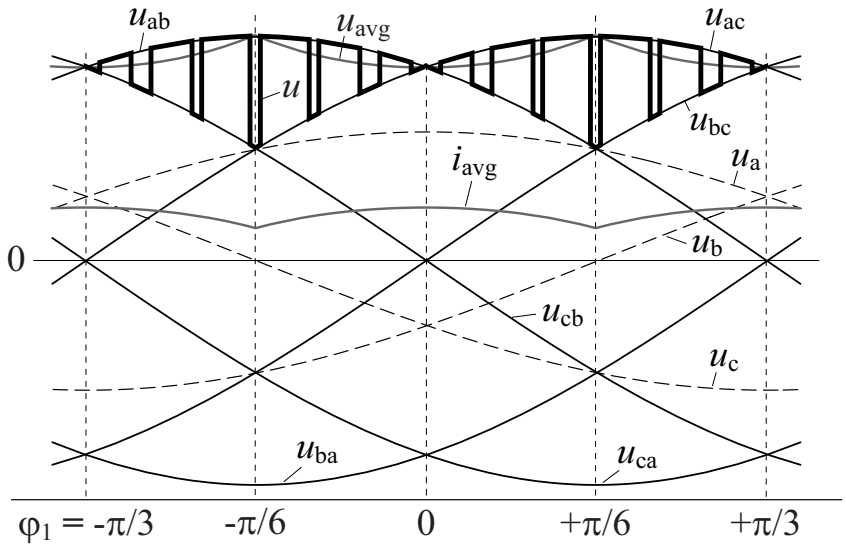


Fig. 3.11: Instantaneous link voltage u, average link voltage u_{avg}, and average link current i_{avg} for the HVZCS modulation scheme ($\varphi_1 = \varphi_{\vec{i}_1^*} = \varphi_{\vec{u}_1}$), averaged over a switching period T_{P}.

and $\varphi_{\vec{u}_2^*}$ is varied within the interval $[0, \pi/3]$, the desired rotating output voltage vector $\vec{u}_2^*$ (with a constant magnitude) is generated if the relative turn-on times are additionally modulated as required for a VSI. This is represented by the cosine and sine terms labeled with "from VSI" in (3.39) to (3.42). The same consideration can also be performed in reverse order for the formation of the input current space vector $\vec{i}_1^*$ and finally proves the calculation of the relative turn-on times in a figurative way. The modulation functions of the additional modulation schemes can be calculated correspondingly.

Considering Fig. 3.11, it is found that with this modulation scheme only real power is transferred across the link as already stated. The average power (flow) in the link P_{link} is constant and may be calculated based on the average link voltage and current according to

$$P_{\mathrm{link}} = \frac{3}{\pi} \int_0^{\frac{\pi}{3}} u(\varphi_1) i(\varphi_1)\, d\varphi_1 = u_{\mathrm{avg}} \cdot i_{\mathrm{avg}} = \mathrm{const.} \tag{3.49}$$

The resulting input and output space vector diagrams of the IMC are each subdivided into 12 sectors as for the VSI (cf. Fig. 3.3) and the CSR (cf. Fig. 3.6), leading to 144 different input and output sector combinations. An extract of the resulting switching sequences for the selected HVZCS modulation scheme is listed in Tab. 3.7.

Input	*Output*	*Switching Sequence* $(0 \ldots T_\mathrm{P}/2)$
I	I	$\ldots(ac)(pnn)-(ac)(ppn)-(ac)(ppp)$
		$(ab)(ppp)-(ab)(ppn)-(ab)(pnn)\ldots$
I	II	$\ldots(ac)(ppn)-(ac)(pnn)-(ac)(nnn)$
		$(ab)(nnn)-(ab)(ppn)-(ab)(ppn)\ldots$
I	III	$\ldots(ac)(ppn)-(ac)(npn)-(ac)(nnn)$
		$(ab)(nnn)-(ab)(npn)-(ab)(ppn)\ldots$
I	IV	$\ldots(ac)(npn)-(ac)(ppn)-(ac)(ppp)$
		$(ab)(ppp)-(ab)(ppn)-(ab)(npn)\ldots$
I	V	$\ldots(ac)(npn)-(ac)(npp)-(ac)(ppp)$
		$(ab)(ppp)-(ab)(npp)-(ab)(npn)\ldots$
I	VI	$\ldots(ac)(npp)-(ac)(npn)-(ac)(nnn)$
		$(ab)(nnn)-(ab)(npn)-(ab)(npp)\ldots$
I	VII	$\ldots(ac)(npp)-(ac)(nnp)-(ac)(nnn)$
		$(ab)(nnn)-(ab)(nnp)-(ab)(npp)\ldots$
I	VIII	$\ldots(ac)(nnp)-(ac)(pnp)-(ac)(ppp)$
		$(ab)(ppp)-(ab)(pnp)-(ab)(nnp)\ldots$
I	IX	$\ldots(ac)(nnp)-(ac)(pnp)-(ac)(ppp)$
		$(ab)(ppp)-(ab)(pnp)-(ab)(nnp)\ldots$
I	X	$\ldots(ac)(pnp)-(ac)(nnp)-(ac)(nnn)$
		$(ab)(nnn)-(ab)(nnp)-(ab)(pnp)\ldots$
I	XI	$\ldots(ac)(pnp)-(ac)(pnn)-(ac)(nnn)$
		$(ab)(nnn)-(ab)(pnn)-(ab)(pnp)\ldots$
I	XII	$\ldots(ac)(pnn)-(ac)(pnp)-(ac)(ppp)$
		$(ab)(ppp)-(ab)(pnp)-(ab)(pnn)\ldots$
II	I	$\ldots(ac)(pnn)-(ac)(ppn)-(ac)(ppp)$
		$(bc)(ppp)-(bc)(ppn)-(bc)(pnn)\ldots$

Tab. 3.7: Switching sequences of the IMC for the selected HVZCS modulation scheme at $\Phi_1^* = 0$, shown for various combinations of the input (reference current $\vec{i}_1^*$) and output (reference voltage $\vec{u}_2^*$) sectors.

3.1.6 Conventional Matrix Converter

In this section, the space vector modulation of the CMC is described based on the IMC. Contrary to the IMC, for the CMC each input phase a, b, c can be directly connected with each output phase A, B, C via a four-quadrant switch. The CMC topology in Fig. 3.12(a) may therefore be represented as a switching matrix as depicted in Fig. 3.12(b) and features a total of $3^3 = 27$ possible switching states.

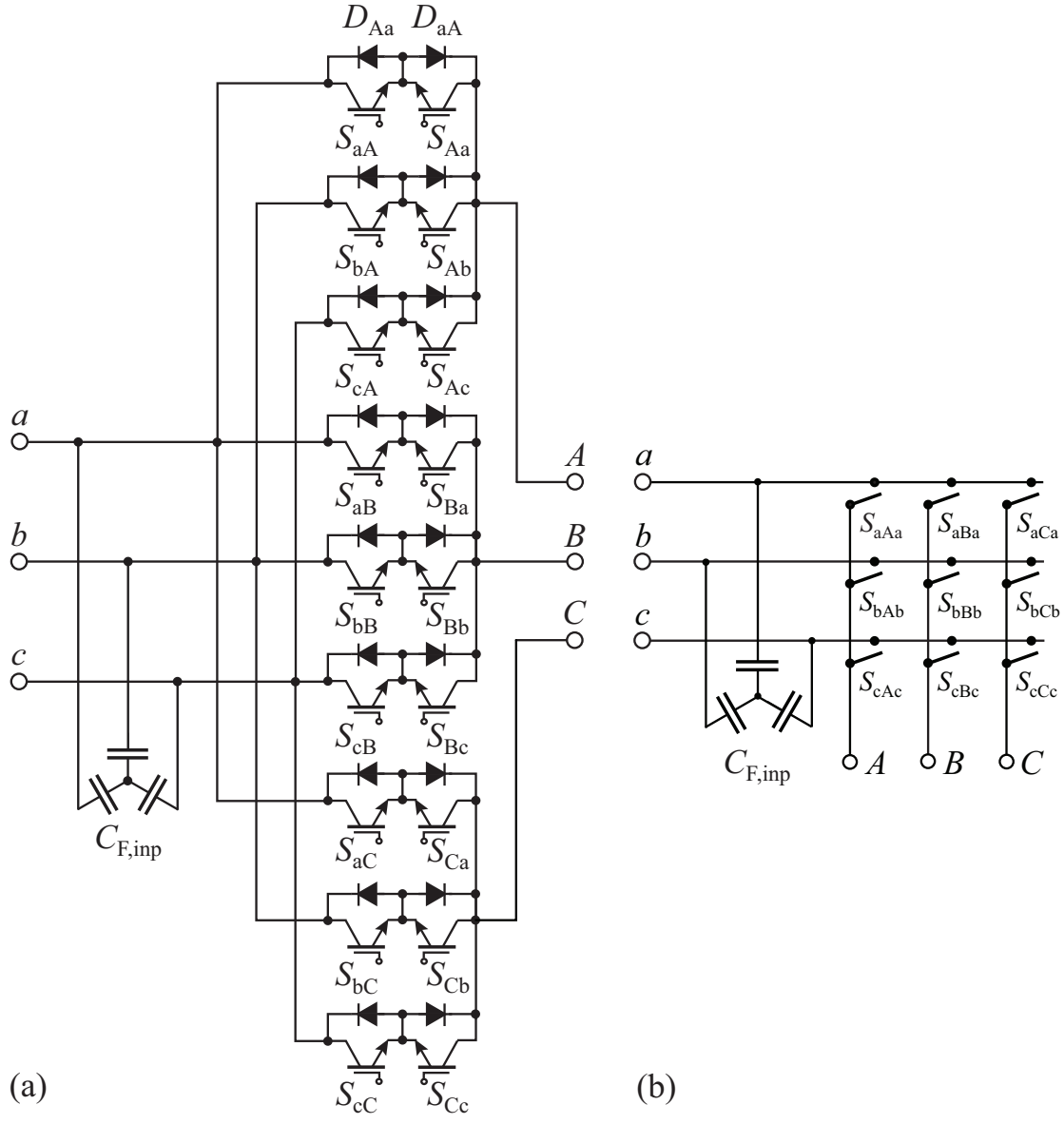


Fig. 3.12: (a) Conventional Matrix Converter (CMC) topology and **(b)** its representation as a switching matrix, indicating the designation of the switching devices.

The switching states are coded using a triple as for example (acb), which means that the input phase a is connected to the output phase A, the input phase c is connected to the output phase B, and the input phase b is connected to the output phase C. Depending on the connections between the input and output phases, the switching states may be classified into three groups according to Tab. 3.8.

For the switching states of Group 1, all output phases are connected to the same input phase, and a zero output voltage space vector is generated ($\vec{u}_2 = \vec{0}$). These switching states are hence referred to as zero or freewheeling states. For all 18 states of Group 2, always two output phases are connected to the same input phase. The third output phase is switched to one of the remaining input phases, and thus an output voltage space vector different from zero ($\vec{u}_2 \neq \vec{0}$) is formed. The states of Group 2 correspond exactly to the active switching states of the IMC. Finally, Group 3 consists of the remaining six switching states, which generate rotating output voltage or input current space vectors as each output phase is connected to a different input phase. These states are only possible for the CMC but not for the IMC topology. The use of rotating space vectors has been widely discussed when the CMC was first introduced, but has become less important with the availability fast switching IGBT devices. For this reason, the following considera-

Group	*Switching States*			*Description*
1	(aaa)	(bbb)	(ccc)	Zero states
2	(cca)	(ccb)	(aab)	
	(aac)	(bbc)	(bba)	
	(acc)	(bcc)	(baa)	Active states with non-
	(caa)	(cbb)	(abb)	rotating space vectors
	(cac)	(cbc)	(aba)	
	(aca)	(bcb)	(bab)	
3	(abc)	(cab)	(bca)	Active states with
	(acb)	(cba)	(bac)	rotating space vectors

Tab. 3.8: Classification of the switching states of the CMC.

tions are limited to the switching states of Group 1 and 2, which are also known from the IMC. The modulation of the CMC can then be simply considered with reference to a fictitious IMC, and the required switching sequences can be obtained by recoding the corresponding switching states of the IMC. The switching state $(ab)(pnn)$ of the IMC, for instance, is then translated into the switching state (abb) of the CMC. For both topologies, the same input current and output voltage space vector is generated. The resulting space vector diagrams of the CMC are depicted in Fig. 3.13 and are identical to those of the IMC.

With this approach, all modulation schemes of the IMC can be mapped to the CMC topology. The HVZCS modulation schemes with CM-optimal clamping (cf. Tab. 3.6) and with loss-optimal clamping (reference modulation scheme for the IMC, cf. Tab. 3.7) are of particular interest for the CMC, as they have proven to be advantageous for the IMC. The mapping of the modulation scheme with loss-optimal clamping reveals that, for example, the switching sequence of the IMC for $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$, $\varphi_{\vec{u}_2^*} \in [\pi/6, \pi/3]$, $\Phi_1^* = 0$, and $\Phi_2 = 0$

$$\begin{aligned}\ldots \Big|_{t_\kappa=0} &(ac)(ppn) - (ac)(pnn) - (ac)(nnn) - \\ &(ab)(nnn) - (ab)(pnn) - (ab)(ppn)\Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} \\ &(ab)(ppn) - (ab)(pnn) - (ab)(nnn) - \\ &(ac)(nnn) - (ac)(pnn) - (ac)(ppn)\Big|_{t_\kappa=T_\mathrm{P}} \ldots \end{aligned} \tag{3.50}$$

results in an undesirable switching sequence for the CMC

$$\begin{aligned}\ldots \Big|_{t_\kappa=0} &(aac) - (acc) - (ccc) - \\ &(bbb) - (abb) - (aab)\Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} \\ &(aab) - (abb) - (bbb) - \\ &(ccc) - (acc) - (aac)\Big|_{t_\kappa=T_\mathrm{P}} \ldots , \end{aligned} \tag{3.51}$$

due to the sequenced switching of freewheeling states $(bbb) - (ccc)$ and $(ccc) - (bbb)$. In a practical system, the commutation of all output phases between two input phases does not occur simultaneously and leads to intermediate switching states and additional switching losses.

However, by applying the modulation scheme with CM-optimal clamping to the CMC, the switching of the freewheeling state can be avoided. The switching sequence of the IMC with CM-optimal clamping for the same intervals of $\varphi_{\vec{i}_1^*}$ and $\varphi_{\vec{u}_2^*}$ then equals to

$$\begin{aligned}\ldots\Big|_{t_\kappa=0} &(ac)(pnn)-(ac)(ppn)-(ac)(ppp)- \\ &(ab)(ppp)-(ab)(ppn)-(ab)(pnn)\Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} \\ &(ab)(pnn)-(ab)(ppn)-(ab)(ppp)- \\ &(ac)(ppp)-(ac)(ppn)-(ac)(pnn)\Big|_{t_\kappa=T_\mathrm{P}}\ldots\end{aligned} \tag{3.52}$$

and is mapped to the following switching sequence of the CMC

$$\begin{aligned}\ldots\Big|_{t_\kappa=0} &(acc)-(aac)-(aaa)- \\ &(aaa)-(aab)-(abb)\Big|_{t_\kappa=\frac{T_\mathrm{P}}{2}} \\ &(abb)-(aab)-(aaa)- \\ &(aaa)-(aac)-(acc)\Big|_{t_\kappa=T_\mathrm{P}}\ldots\,.\end{aligned} \tag{3.53}$$

Besides the absence of undesired state transitions, there are additional advantages for the CMC involved in this modulation scheme. Contrary to the IMC, according to [131], for the CMC the average semiconductor losses do not increase for the CM-optimal clamping compared to the loss-optimal clamping as no sequenced switching of freewheeling states occurs. The commutations always occur between the two largest input line-to-line voltages without any zero voltage crossing and thus enables the implementation of a voltage dependent, robust multi-step commutation scheme. This modulation strategy is described in detail in [280]. Nevertheless, the commutation sequence of the CMC still depends on measurement signals, which is not the case for the IMC.

It is also possible to map the modulation schemes of the IMC, allowing for ZVS of the output stage, to the CMC. The disadvantage of the resulting switching sequences, however, is that two output phases are switched simultaneously. This again may lead to undesired intermediate switching states and increases the switching losses. Therefore, these modulation schemes are not further considered for the CMC. Alternatively, also the CSVM or the ISVM can be utilized for the CMC.

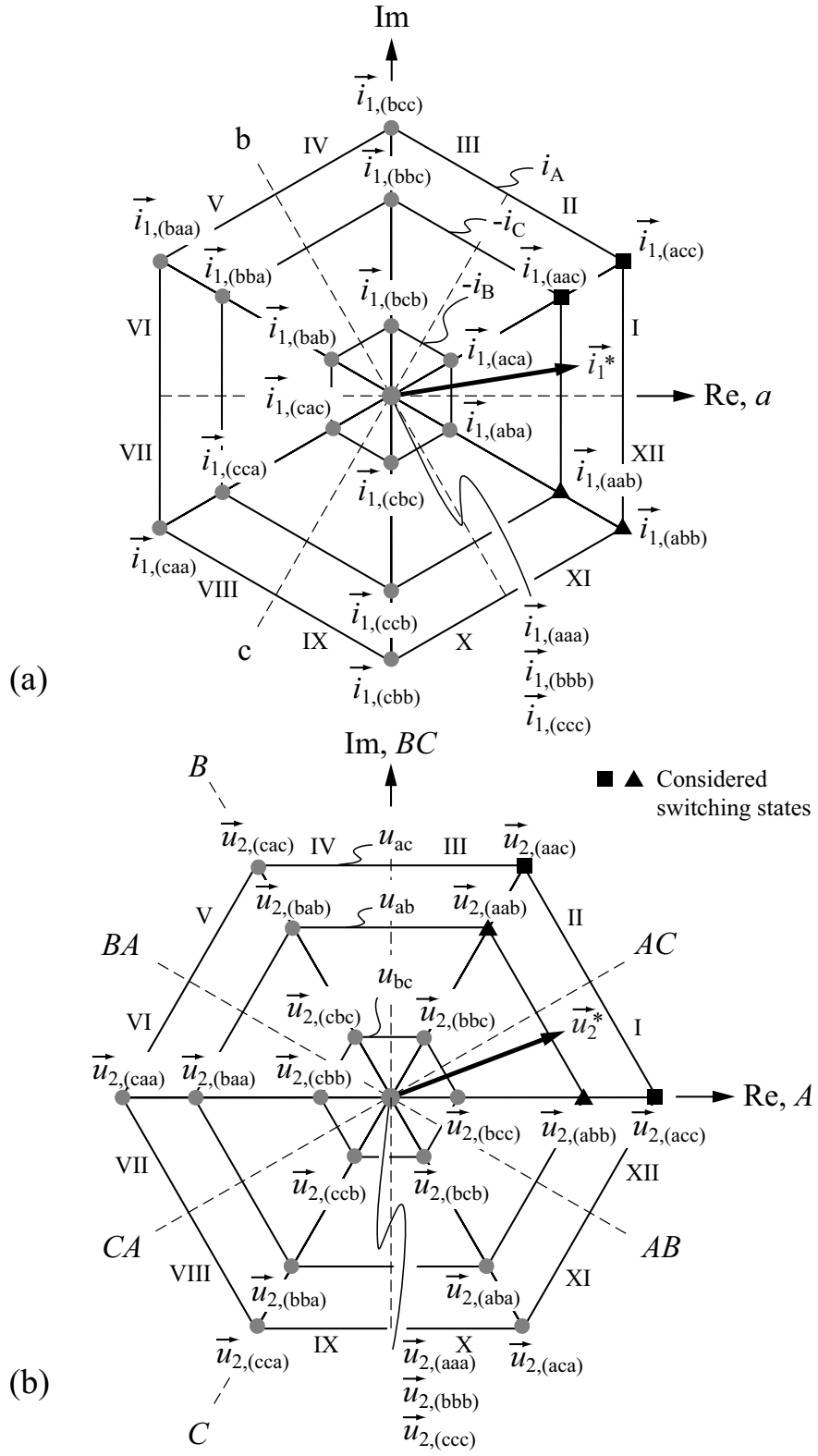


Fig. 3.13: Space vector diagrams of the CMC for **(a)** the input stage and **(b)** the output stage for the switching states of Group 1 and 2.

Due to the benefits stated above, the switching strategy with CM-optimal clamping is selected as the reference modulation scheme for the CMC in this work and is denoted as CMOSVM. An extract of the resulting switching sequences is summarized in Tab. 3.9. The input and output space vector diagrams are again subdivided into 12 sectors each; and the calculation of the relative turn-on times can be directly adopted from (3.45) to (3.48) of the IMC.

Opposed to the IMC, the change of the switching state of the CMC must be accomplished considering the impressed input voltage and the impressed output current. Suitable multi-step commutation schemes were first suggested in [103, 116]. The commutation is thereby executed depending on the sign of the commutation voltage (voltage difference of those input phases between which the commutation is carried out, in this case u_{ab}) or/and depending on the sign of the current in the output phase that is to be switched to another input phase. In Fig. 3.14(a), the commutation sequence of a voltage dependent four-step commutation scheme, suitable for the selected CMOSVM scheme, is presented

Input	*Output*	*Switching Sequence* $(0 \ldots T_{\mathrm{P}}/2)$
I	I, II	$\ldots(acc)-(aac)-(aaa)-(aab)-(abb)\ldots$
I	III, IV	$\ldots(cac)-(aac)-(aaa)-(aab)-(bab)\ldots$
I	V, VI	$\ldots(cac)-(caa)-(aaa)-(baa)-(bab)\ldots$
I	VII, VIII	$\ldots(cca)-(caa)-(aaa)-(baa)-(bba)\ldots$
I	IX, X	$\ldots(cca)-(aca)-(aaa)-(aba)-(bba)\ldots$
I	XI, XII	$\ldots(acc)-(aca)-(aaa)-(aba)-(abb)\ldots$
II	I, II	$\ldots(aac)-(acc)-(ccc)-(bcc)-(bbc)\ldots$
II	III, IV	$\ldots(aac)-(cac)-(ccc)-(cbc)-(bbc)\ldots$
II	V, VI	$\ldots(caa)-(cac)-(ccc)-(cbc)-(cbb)\ldots$
II	VII, VIII	$\ldots(caa)-(cca)-(ccc)-(ccb)-(cbb)\ldots$
II	IX, X	$\ldots(aca)-(cca)-(ccc)-(ccb)-(bcb)\ldots$
II	XI, XII	$\ldots(aca)-(acc)-(ccc)-(bcc)-(bcb)\ldots$

Tab. 3.9: Switching sequences of the CMC for the selected CMOSVM scheme for $\Phi_{\underline{1}}^{*}=0$, shown for various combinations of the input (reference current $\vec{i}_1^{\,*}$) and output (reference voltage $\vec{u}_2^{\,*}$) sectors.

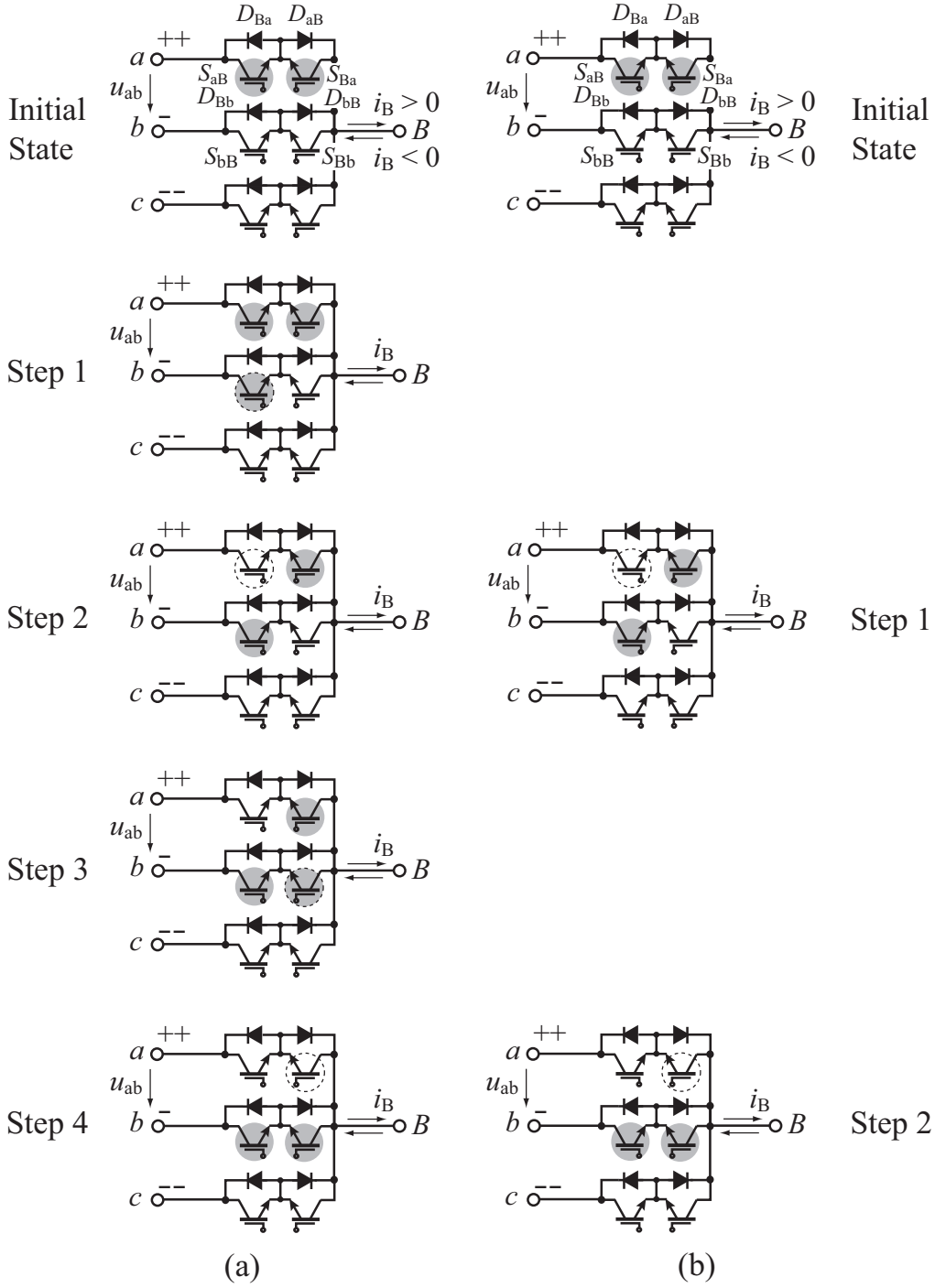


Fig. 3.14: Voltage dependent **(a)** four-step and **(b)** two-step commutation scheme for the transition of the connection $a-B$ to $b-B$, assuming $u_a > u_b > u_c$, $u_a > 0$ (++), $u_b < 0$ (−), and $u_c < 0$ (−−). The transistors shown on a gray background are in the on-state; a dashed line surrounding a transistor indicates a change of the switching state.

for the switching state transition $(aab) - (abb)$ of a single branch of the CMC. The transistors on a gray background are in the on-state and those surrounded by a dashed line indicate that a change of the switching state has happened in the present commutation step. Prior to a transistor turn-off, the corresponding transistor of the branch that is going to carry the current has to be switched on in order to always provide a current path. The transistor S_{bB}, that has to be turned on in the first step, is selected such that no input phase short-circuit occurs for the applied commutation voltage. This requires the series diode D_{bB} to block the commutation voltage. Consequently, two current paths are available for $i_{\mathrm{B}} > 0$ and therefore, in the second step the transistor S_{aB} is turned off. In the third step, S_{Bb} can be turned on and D_{Ba} blocks the commutation voltage. Finally, in the fourth step, the transistor S_{Ba} can be turned off as well. Hence, a bidirectional current path between the input phase b and the output phase B is established.

As proposed in [119], the standard four-step commutation strategy can also be reduced to a three-, two-, or even a one-step commutation. The two-step commutation, derived from the four-step commutation in Fig. 3.14(a), is depicted in Fig. 3.14(b). The strategy is to always keep as many transistors as possible in the on-state to minimize the number of commutation steps, when a switching state transition is required. The advantage of the two-step commutation of providing additional freewheeling paths for the output current is outweighed by a higher sensitivity to voltage measurement errors and an increased complexity as the number of device state combination is doubled compared to the four-step strategies.

In this work, the voltage-based four-step commutation strategy shown in Fig. 3.14(a) is applied for the implementation of the CMOSVM. The reliability of the commutation is further increased by utilizing besides the measured input voltages also the measured output currents to verify the commutation sequence.

3.1.7 Implementation

Finally, the actual implementation of the modulation schemes is briefly discussed. By considering the modulation schemes of the individual converter topologies, it can be seen that all selected modulation scheme require four different active states per pulse period. This allows the implementation of a configurable, generic modulator, which is applicable to

all four converter topologies and shall be presented in the following. The modulation functions are given for $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$ and $\varphi_{\vec{u}_2^*} \in [0, \pi/6]$, assuming $\Phi_1^* = 0$ ($\varphi_{\vec{i}_1^*} = \varphi_{\vec{u}_1}$) and $\Phi_2 = 0$, which corresponds to the input and output sector I in the space vector diagrams.

VSBBC

The modulation of the input and output stage of the VSBBC is implemented according to the following timing diagram. The interlock delay ($T_{\mathrm{del}} > 0$), utilized to avoid short-circuits in the bridge-legs during the switching state transitions, are not shown.

Input Stage

$(pnn)'$	$(ppn)'$	$(ppp)'$	$(ppn)'$	$(pnn)'$
τ_1	τ_2	τ_3	τ_2	τ_1

Output Stage

(pnn)	(ppn)	(ppp)	(ppn)	(pnn)
τ_4	τ_5	τ_6	τ_5	τ_4

0 $T_{\mathrm{P}}/2$ T_{P}

The absolute turn-on times τ_1 to τ_6 of the resulting six intervals within a pulse period T_{P} can be calculated to

$$\tau_1 = \frac{T_{\mathrm{P}}}{2}\, d_{(\mathrm{pnn})'} = \frac{T_{\mathrm{P}}}{2} M_1 \cos\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{6}\right) \tag{3.54}$$

$$\tau_2 = \frac{T_{\mathrm{P}}}{2}\, d_{(\mathrm{ppn})'} = \frac{T_{\mathrm{P}}}{2} M_1 \sin\left(\varphi_{\vec{i}_1^*}\right) \tag{3.55}$$

$$\tau_3 = \frac{T_{\mathrm{P}}}{2}\, d_{(\mathrm{ppp})'} = 2\left(\frac{T_{\mathrm{P}}}{2} - \tau_1 - \tau_2\right) \tag{3.56}$$

$$\tau_4 = \frac{T_{\mathrm{P}}}{2}\, d_{(\mathrm{pnn})} = \frac{T_{\mathrm{P}}}{2} M_2 \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right) \tag{3.57}$$

$$\tau_5 = \frac{T_{\mathrm{P}}}{2}\, d_{(\mathrm{ppn})} = \frac{T_{\mathrm{P}}}{2} M_2 \sin\left(\varphi_{\vec{u}_2^*}\right) \tag{3.58}$$

$$\tau_6 = \frac{T_{\mathrm{P}}}{2}\, d_{(\mathrm{ppp})} = 2\left(\frac{T_{\mathrm{P}}}{2} - \tau_4 - \tau_5\right) \ . \tag{3.59}$$

(3.54) to (3.59) are valid for $\varphi_{\vec{i}_1^*} = \varphi_{\vec{u}_1} \in [0, \pi/3]$ (input sector I and II) and $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$ (output sector I and II). The modulation index

of the input stage M_1 and of the output stage M_2 is defined as

$$M_1 = \frac{\sqrt{3}\,\hat{U}_1^*}{U} = [0\ldots1] \tag{3.60}$$

$$M_2 = \frac{\sqrt{3}\,\hat{U}_2^*}{U} = [0\ldots1]\ . \tag{3.61}$$

CSBBC

The modulation of the CSBBC can be implemented by applying the same structure for the timing of the switching states as for the VSBCC. The overlapping delay time ($T_{\mathrm{del}} < 0$) in order to always provide a current path during the switching state transitions, are not depicted in the timing diagram below.

Input Stage

(ac)	(ab)	(aa)	(ab)	(ac)
τ_1	τ_2	τ_3	τ_2	τ_1

Output Stage

(AC)	(AB)	(AA)	(AB)	(AC)
τ_4	τ_5	τ_6	τ_5	τ_4

0 $T_{\mathrm{P}}/2$ T_{P}

The absolute turn-on times τ_1 to τ_6 of the resulting six intervals within a pulse period T_{P} can be determined as follows

$$\tau_1 = \frac{T_{\mathrm{P}}}{2}\,d_{(\mathrm{ac})} = \frac{T_{\mathrm{P}}}{2} M_1 \cos\left(\varphi_{\vec{i}_1^*} - \frac{\pi}{3}\right) \tag{3.62}$$

$$\tau_2 = \frac{T_{\mathrm{P}}}{2}\,d_{(\mathrm{ab})} = \frac{T_{\mathrm{P}}}{2} M_1 \cos\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{3}\right) \tag{3.63}$$

$$\tau_3 = \frac{T_{\mathrm{P}}}{2}\,d_{(\mathrm{aa})} = 2\left(\frac{T_{\mathrm{P}}}{2} - \tau_1 - \tau_2\right) \tag{3.64}$$

$$\tau_4 = \frac{T_{\mathrm{P}}}{2}\,d_{(\mathrm{AC})} = \frac{T_{\mathrm{P}}}{2} M_2 \cos\left(\varphi_{\vec{i}_2^*} - \frac{\pi}{3}\right) \tag{3.65}$$

$$\tau_5 = \frac{T_{\mathrm{P}}}{2}\,d_{(\mathrm{AB})} = \frac{T_{\mathrm{P}}}{2} M_2 \cos\left(\varphi_{\vec{i}_2^*} + \frac{\pi}{3}\right) \tag{3.66}$$

$$\tau_6 = \frac{T_{\mathrm{P}}}{2}\,d_{(\mathrm{AA})} = 2\left(\frac{T_{\mathrm{P}}}{2} - \tau_4 - \tau_5\right)\ . \tag{3.67}$$

(3.62) to (3.67) are valid for $\varphi_{\vec{i}_1^*} \in [-\pi/6, \pi/6]$ (input sector I and XII) and $\varphi_{\vec{i}_2^*} \in [-\pi/6, \pi/6]$ (output sector I and XII). The modulation index of the input stage M_1 and of the output stage M_2 of the CSBBC is defined as

$$M_1 = \frac{\hat{I}_1^*}{I} = [0 \dots 1] \tag{3.68}$$

$$M_2 = \frac{\hat{I}_2^*}{I} = [0 \dots 1] \ . \tag{3.69}$$

IMC

Opposed to the VSBBC and the CSBBC, the modulation of the input and output stage of the IMC is cascaded and leads to the following timing diagram. The interlock delay and safety times of the input and output stage switches are not depicted.

Input and Output Stage

(ac) (pnn)	(ac) (ppn)	(ac) (ppp)	(ab) (ppp)	(ab) (ppn)	(ab) (pnn)
τ_1	τ_2	τ_3	τ_4	τ_5	τ_6

0 $T_\mathrm{P}/2$

The absolute turn-on times τ_1 to τ_6 of the resulting six intervals within a pulse half-period $T_\mathrm{P}/2$ can be calculated to

$$\tau_1 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{ac})(\mathrm{pnn})} = \frac{T_\mathrm{P}}{2} M_{12} \cos\left(\varphi_{\vec{i}_1^*} - \frac{\pi}{3}\right) \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right) \tag{3.70}$$

$$\tau_2 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{ac})(\mathrm{ppn})} = \frac{T_\mathrm{P}}{2} M_{12} \cos\left(\varphi_{\vec{i}_1^*} - \frac{\pi}{3}\right) \sin\left(\varphi_{\vec{u}_2^*}\right) \tag{3.71}$$

$$\tau_3 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{ac})(\mathrm{ppp})} = \frac{1}{2}\left(\frac{T_\mathrm{P}}{2} - \tau_1 - \tau_2 - \tau_5 - \tau_6\right) \tag{3.72}$$

$$\tau_4 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{ab})(\mathrm{ppp})} = \frac{1}{2}\left(\frac{T_\mathrm{P}}{2} - \tau_1 - \tau_2 - \tau_5 - \tau_6\right) \tag{3.73}$$

$$\tau_5 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{ab})(\mathrm{ppn})} = \frac{T_\mathrm{P}}{2} M_{12} \cos\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{3}\right) \sin\left(\varphi_{\vec{u}_2^*}\right) \tag{3.74}$$

$$\tau_6 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{ab})(\mathrm{pnn})} = \frac{T_\mathrm{P}}{2} M_{12} \cos\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{3}\right) \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right) \ . \tag{3.75}$$

(3.70) to (3.75) are valid for $\varphi_{\vec{i}_1^*} \in [-\pi/6, \pi/6]$ (input sector I and XII) and $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$ (output sector I and II). The modulation index M_{12} is defined as

$$M_{12} = \frac{2\,\hat{U}_2^*}{\sqrt{3}\,\hat{U}_1} = [0 \ldots 1] \ . \tag{3.76}$$

CMC

The individual commutation steps of the selected four-step commutation scheme are visualized with the vertical bars in the timing diagram below.

(acc)	(aac)	(aaa)	(aaa)	(aab)	(abb)
τ_1	τ_2	τ_3	τ_4	τ_5	τ_6

0 $T_\mathrm{P}/2$

The absolute turn-on times τ_1 to τ_6 (neglecting the commutation time) of the resulting six intervals within a pulse half-period $T_\mathrm{P}/2$ can be determined as follows

$$\tau_1 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{acc})} = \frac{T_\mathrm{P}}{2} M_{12} \cos\left(\varphi_{\vec{i}_1^*} - \frac{\pi}{3}\right) \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right) \tag{3.77}$$

$$\tau_2 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{aac})} = \frac{T_\mathrm{P}}{2} M_{12} \cos\left(\varphi_{\vec{i}_1^*} - \frac{\pi}{3}\right) \sin\left(\varphi_{\vec{u}_2^*}\right) \tag{3.78}$$

$$\tau_3 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{aaa})} = \frac{1}{2}\left(\frac{T_\mathrm{P}}{2} - \tau_1 - \tau_2 - \tau_5 - \tau_6\right) \tag{3.79}$$

$$\tau_4 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{aaa})} = \frac{1}{2}\left(\frac{T_\mathrm{P}}{2} - \tau_1 - \tau_2 - \tau_5 - \tau_6\right) \tag{3.80}$$

$$\tau_5 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{aab})} = \frac{T_\mathrm{P}}{2} M_{12} \cos\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{3}\right) \sin\left(\varphi_{\vec{u}_2^*}\right) \tag{3.81}$$

$$\tau_6 = \frac{T_\mathrm{P}}{2}\, d_{(\mathrm{abb})} = \frac{T_\mathrm{P}}{2} M_{12} \cos\left(\varphi_{\vec{i}_1^*} + \frac{\pi}{3}\right) \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right) \ . \tag{3.82}$$

(3.77) to (3.82) are valid for $\varphi_{\vec{i}_1^*} \in [-\pi/6, \pi/6]$ (input sector I and XII) and $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$ (output sector I and II). The modulation index M_{12} is defined identically to the IMC as

$$M_{12} = \frac{2\,\hat{U}_2^*}{\sqrt{3}\,\hat{U}_1} = [0 \ldots 1] \ . \tag{3.83}$$

Conclusions

- For the selected modulation schemes, the same modulator based on six turn-on times τ_1 to τ_6, can be applied to all four topologies.
- The computational effort for the modulation functions of the considered converter topologies is approximately the same.
- The multi-step commutation of the CMC is the most intricate regarding the actual implementation. The complexity of implementation of the modulation scheme for the VSBBC, CSBBC, and IMC is identical as they require the same number of different switching states per pulse period and similar safety concepts for the commutation (interlock delay or overlapping time intervals).
- Contrary to the IMC and CMC, the modulation of the input and output stage of the VSBBC and CSBBC do not depend on each other as shown by the individual timing diagrams, apart from a (optional) common clock basis (center-aligned SVM).
- For arbitrary input and output sector combinations, the turn-on times can be calculated by an angular transformation of the voltage and current reference vectors to the scope of validity of the equations for τ_1 to τ_6, since the modulation functions are $\pi/3$-periodic.

3.2 Control

3.2.1 Overview

In addition to the modulation, the control significantly impacts the performance of the investigate converter topologies and should therefore be considered as a further assessment criterion. The overall control system of an electric drive involves the interaction of the actual converter control and the motor control. The motor of choice is the PMSM due to its high power density and efficiency [281] and the absence of a magnetizing current compared to the IM.

The focus of this consideration is to investigate the typically controlled or controllable system variables, the estimation of the implementation effort of a simple control for a PMSM, and the identification of basic limitations in the operating behavior, which are relevant to decide on the converter topology and for the drive dimensioning. In doing so, parameters of commercially available PMSMs are assumed (cf. e.g. Lust LTi Drives, LST PMSM series: stator inductance $L_\mathrm{S} = 1\,\mathrm{mH} \ldots 5\,\mathrm{mH}$ and stator resistance $R_\mathrm{S} = 25\,\mathrm{m\Omega} \ldots 200\,\mathrm{m\Omega}$ for a power level of 5 kW to 15 kW). A detailed analysis of different control concepts and their performance, however, remains out of consideration in this work. Intense research has already been conducted in this topic area. The corresponding references are provided in Sec. 1.4.2.

3.2.2 Considered Control Concept

Cascaded feedback control combined with feedforward control is a widespread control concept for industrial low-voltage drive systems. Therefore, this concept is applied for the following investigations and is also utilized to control the converter prototypes implemented in the course of this thesis. An example of such a cascaded feedback control scheme is depicted in Fig. 3.15 for the IMC.

The main purpose of the control for general drive applications is to enable speed (voltage) and torque (current) control of the motor and to ensure sinusoidal currents and unity power factor at the converter input. For motion control applications, additionally, position control is required, which is of minor importance for this comparison and thus is disregarded. The control is typically implemented in the rotating dq reference frame to enable a uniform description of the drive system

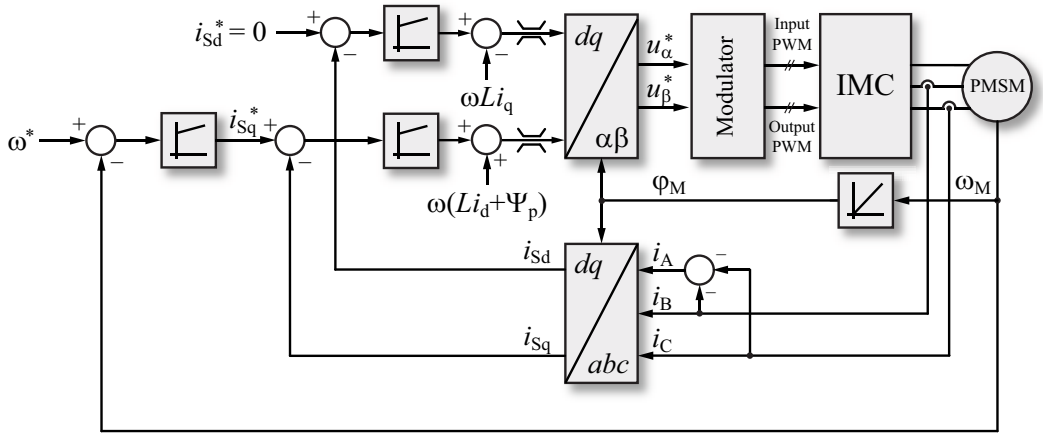


Fig. 3.15: Implemented, simple, cascaded feedback control scheme for a MC to control a PMSM.

from the mains input to the motor shaft. The corresponding system variables are specified in Fig. 3.16 for all converter topologies. In order to simplify the notation of the variables in the dq reference frame, the following convention is used

$$\underline{x}(t) = \begin{bmatrix} x_\mathrm{d}(t) \\ x_\mathrm{q}(t) \end{bmatrix} \ . \tag{3.84}$$

It is important to note the difference between the unfiltered and filtered input current ($\underline{i}_1$, $\underline{i}_{1,\mathrm{flt}}$) and output current ($\underline{i}_2$, $\underline{i}_{2,\mathrm{flt}}$) for the CSBBC, the IMC, and the CMC. The filtered input current always refers to the current flowing from the input terminals (a, b, c) to the input capacitors $C_{\mathrm{F,inp}}$, whereas the unfiltered input current refers to the current flowing from the input capacitors to the semiconductors (cf. CSBBC, IMC, and CMC in Fig. 3.16). For the CSBBC, the unfiltered output current then corresponds to the current flowing between the semiconductors and the output capacitors $C_{\mathrm{F,out}}$, and the filtered output current to the current flowing between the output capacitor and the output terminals (A, B, C).

In this work, cascaded PI feedback controllers are used. The fundamental principle of cascaded feedback control is based on the difference of system time constants. The closed-loop bandwidth of the innermost ("fastest") loop typically needs to be approximately a factor of 10 below the switching frequency f_sw. The control performance is enhanced by feedforward of off-line calculated, measured, or estimated system variables.

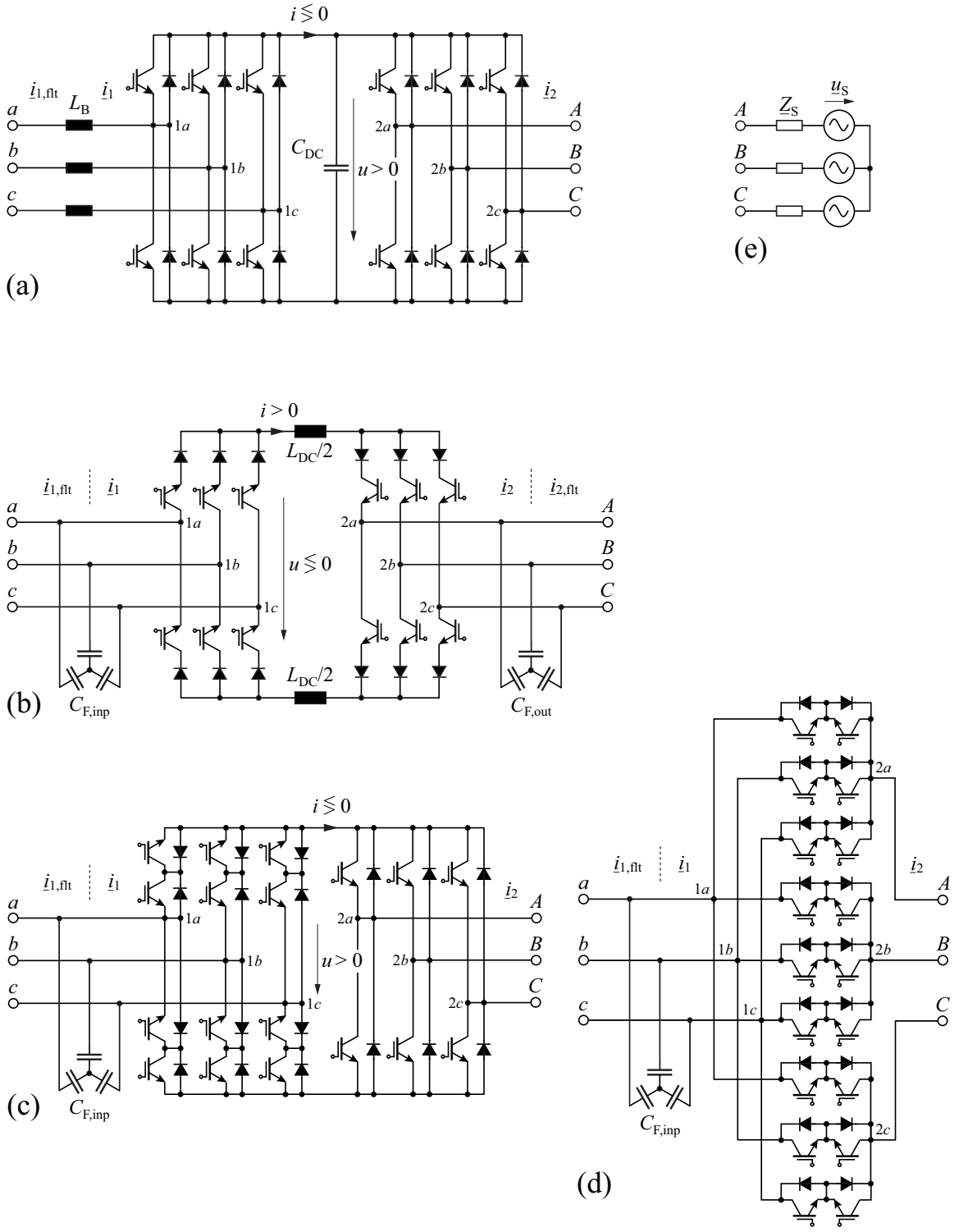


Fig. 3.16: Definition of the filtered and unfiltered input current ($\underline{i}_1$, $\underline{i}_{1,\mathrm{flt}}$) and output current ($\underline{i}_2$, $\underline{i}_{2,\mathrm{flt}}$) and labeled nodes for the **(a)** VSBBC, **(b)** CSBBC, **(c)** IMC, and **(d)** CMC; **(e)** equivalent circuit of the motor.

3.2.3 Control Properties

In order to compare the main control properties, the individual converter topologies are analyzed regarding

- typical control variables,
- common feedforward and auxiliary control,
- required measurement signals, and
- characteristic operating modes

for a basic feedback control scheme as specified in Sec. 3.2.2. From a control point of view there is no significant difference between the input-to-output behavior of the IMC and CMC. Hence, it is sufficient to restrict the considerations to MCs in general. The resulting control properties for the VSBBC, CSBBC, and MC are compiled in Tab. 3.10, Tab. 3.11, and Tab. 3.12. The variables $f_{\mathrm{c},i}$ are used to indicate the typical relationship between the 3 dB closed-loop bandwidth of the individual control loops, whereby it is assumed that

$$f_{\mathrm{c},1} \geq f_{\mathrm{c},2} \geq f_{\mathrm{c},3} \geq f_{\mathrm{c},4} \; . \tag{3.85}$$

In the following, the major differences of the individual converter topologies are briefly discussed.

Motor Control

Both the VSBBC and the MC feature a switched voltage-source-type output. Consequently, the standard control scheme for PMSMs with an outer speed control loop and two inner current control loops can be applied. The inner control loops enable to independently control the torque (q-axis current i_{Sq}) and the flux (d-axis current i_{Sd}) of the PMSM. If field-weakening operation of the PMSM is not considered, the reference d-axis stator current always equals to zero ($i^*_{\mathrm{S,d}} = 0$). (3.86) and (3.87) represent the stator quantities of the PMSM in the dq reference frame, assuming $L_{\mathrm{S}} = L_{\mathrm{Sd}} = L_{\mathrm{Sq}}$ and $d\Psi_{\mathrm{P}}/dt = 0$.

$$L_{\mathrm{S}} \frac{di_{\mathrm{Sd}}}{dt} + R_{\mathrm{S}} i_{\mathrm{Sd}} = u_{\mathrm{Sd}} + \omega_2 L_{\mathrm{S}} i_{\mathrm{Sq}} \tag{3.86}$$

$$L_{\mathrm{S}} \frac{di_{\mathrm{Sq}}}{dt} + R_{\mathrm{S}} i_{\mathrm{Sq}} = u_{\mathrm{Sq}} - \omega_2 L_{\mathrm{S}} i_{\mathrm{Sd}} - \Psi_{\mathrm{P}} \omega_2 \tag{3.87}$$

The d- and q-axis current control loops are decoupled by feedforward of the stationary equations of the PMSM (cf. Fig. 3.15) according to (3.88) and (3.89), derived from (3.86) and (3.87).

$$u_{2\mathrm{d,ff}} = -\omega_2 L_\mathrm{S} i_\mathrm{Sq} \tag{3.88}$$

$$u_{2\mathrm{q,ff}} = \omega_2 L_\mathrm{S} i_\mathrm{Sd} + \Psi_\mathrm{P}\omega_2 \tag{3.89}$$

For the input current controllers of the VSBBC, the corresponding decoupling and feedforward control concept can be applied as is utilized for the PMSM at the converter output

Although the CSBBC has output filter capacitors $C_\mathrm{F,out}$, in principal the same cascaded control scheme for the PMSM can be utilized as for the VSBBC and MC. The prerequisite is to account for the output capacitors in the control model. In the following consideration for the CSBBC, a simple control scheme is assumed, in which the dc-link inductor current, the speed of the PMSM, and the motor currents (output currents) are controlled. With reference to Fig. 3.16(b), the differential equations for $C_\mathrm{F,out}$ can be calculated to

$$C_\mathrm{F,out}\frac{du_\mathrm{Cd}}{dt} = i_\mathrm{2d} - i_\mathrm{2d,flt} + \omega_2 C_\mathrm{F,out} u_\mathrm{Cq} \tag{3.90}$$

$$C_\mathrm{F,out}\frac{du_\mathrm{Cq}}{dt} = i_\mathrm{2q} - i_\mathrm{2q,flt} - \omega_2 C_\mathrm{F,out} u_\mathrm{Cd}\ . \tag{3.91}$$

Solving (3.90) and (3.91) for u_Cd and u_Cq and substituting

$$u_\mathrm{Sd} = u_\mathrm{Cd} \qquad u_\mathrm{Sq} = u_\mathrm{Cq} \qquad i_\mathrm{2d,flt} = i_\mathrm{Sd} \qquad i_\mathrm{2q,flt} = i_\mathrm{Sq} \tag{3.92}$$

in (3.86) and (3.87) leads to

$$\begin{aligned} L_\mathrm{S}\frac{di_\mathrm{Sd}}{dt} + R_\mathrm{S} i_\mathrm{Sd} = &\left(i_\mathrm{2q} - i_\mathrm{Sq} - C_\mathrm{F,out}\frac{du_\mathrm{Cq}}{dt}\right)\frac{1}{\omega_2 C_\mathrm{F,out}} \\ &+ \omega_2 L_\mathrm{S} i_\mathrm{Sq} \end{aligned} \tag{3.93}$$

$$\begin{aligned} L_\mathrm{S}\frac{di_\mathrm{Sq}}{dt} + R_\mathrm{S} i_\mathrm{Sq} = &\left(-i_\mathrm{2d} + i_\mathrm{Sd} + C_\mathrm{F,out}\frac{du_\mathrm{Cd}}{dt}\right)\frac{1}{\omega_2 C_\mathrm{F,out}} \\ &- \omega_2 L_\mathrm{S} i_\mathrm{Sd} - \Psi_\mathrm{P}\omega_2\ . \end{aligned} \tag{3.94}$$

The equations required to compensate the reactive current of the output filter and to feedforward the stationary currents of the PMSM can be

determined by setting the terms with derivations in (3.93) and (3.94) equal to zero and solving for $i_{2\mathrm{d}}$ and $i_{2\mathrm{q}}$.

$$i_{2\mathrm{d,ff}} = \left(1 - \omega_2^2 C_{\mathrm{F,out}} L_{\mathrm{S}}\right) i_{\mathrm{Sd}} - \omega_2 C_{\mathrm{F,out}} R_{\mathrm{S}} i_{\mathrm{Sq}} - \omega_2^2 C_{\mathrm{F,out}} \Psi_{\mathrm{P}} \quad (3.95)$$

$$i_{2\mathrm{q,ff}} = \left(1 - \omega_2^2 C_{\mathrm{F,out}} L_{\mathrm{S}}\right) i_{\mathrm{Sq}} + \omega_2 C_{\mathrm{F,out}} R_{\mathrm{S}} i_{\mathrm{Sd}} \quad (3.96)$$

A complete decoupling of the d- and q-axis is achieved if additionally the derivations of the capacitor voltages are considered. Hence, the motor control for the CSBBC is more intricate compared with the VSBBC and MC.

Controlled versus Impressed Input Currents

The characteristics of the converter topologies regarding voltage and current impression, identified in Sec. 1.4.2, are to be found again in control. The VSBBC allows for (direct) feedback control of the input currents $\underline{i}_1 = \underline{i}_{1,\mathrm{flt}}$ that are impressed in the boost inductors L_{B}. The CSBBC also permits feedback control of the input currents. However, the filtered input currents $\underline{i}_{1,\mathrm{flt}}$ at the input terminals are impressed by the differential mode filter inductors $L_{\mathrm{DM},2}$ (cf. Fig. 3.18). Accordingly, the input currents are controlled by controlling the voltages across the input capacitors. The dynamics of the input current control loop is proportional to $1/C_{\mathrm{F,inp}}$ and therefore lower compared with the VSBBC. In the simplest control scheme as considered here, active (damping) control of the input currents is omitted.

Unlike the VSBBC and CSBBC, the MC does not provide controllability of the input current amplitude independent of the output voltage $\underline{u}_2$ and output current $\underline{i}_2$ as the input current is impressed by the load. Only the phase angle $\varphi_{\underline{i}_1^*}$ of the reference input current can be adjusted to compensate the reactive input filter current and is implemented by feedforward control. Consequently, feedback control of the unfiltered currents $\underline{i}_1$ and the filtered currents $\underline{i}_{1,\mathrm{flt}}$ is not possible for MCs.

Voltage Step-up and Reactive Power Compensation

Output voltage step-up (boost operation) and reactive input power compensation capability are desired features of ac-ac converters. Both the VSBBC and the CSBBC provide voltage step-up functionality and thus can maintain the nominal output voltage also at reduced input voltages.

This enables a less conservative motor design with a higher nominal voltage and a lower nominal current. As already previously described, the maximum output voltage of MCs is limited to 86.6% of the input voltage, and hence the control, for example, cannot compensate for a mains voltage dip (if the modulation index is maximum, $M_{12} = 1$) since output voltage step-up operation is not possible.

The reactive power compensation capability of the VSBBC and the CSBBC is primarily limited by the component ratings, whereas for MCs there are different restrictions given by the topology. For the selected modulation schemes of the CMC and IMC, the real input power P_1 and the reactive input power Q_1 can be quantified by the following equations if the converter losses are neglected.

$$P_1 = \frac{3\sqrt{3}}{4} M_{12} \hat{U}_1 \hat{I}_2 \cos\left(\Phi_1^*\right) \cos\left(\Phi_2\right) \tag{3.97}$$

$$Q_1 = \frac{3\sqrt{3}}{4} M_{12} \hat{U}_1 \hat{I}_2 \sin\left(\Phi_1^*\right) \cos\left(\Phi_2\right) \tag{3.98}$$

$$S_1 = |\underline{S}_1| = \left| \begin{bmatrix} P_1 \\ Q_1 \end{bmatrix} \right| = \sqrt{P_1^2 + Q_1^2} \tag{3.99}$$

For the selected modulation of the IMC, the reference input phase displacement angle is limited to $\Phi_1^* \in [-\pi/6 \ldots \pi/6]$ to restrict the link

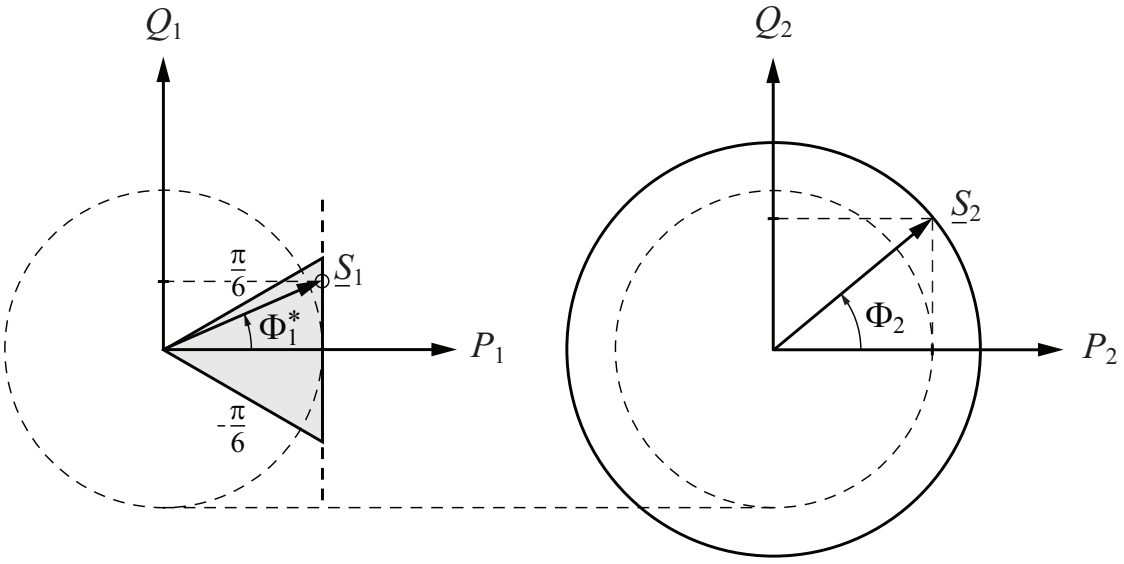


Fig. 3.17: Formation of the apparent input power $\underline{S}_1$ of the CMC and IMC based on the apparent output power $\underline{S}_2$.

voltage to positive values. With respect to (3.30), the maximum output voltage amplitude

$$\hat{U}_{2,\max} = \frac{\sqrt{3}}{2}\hat{U}_1 \cos\left(\Phi_1^*\right) \tag{3.100}$$

is limited by Φ_1^*. In terms of providing a maximum output voltage control range, a large input phase displacement angle should be avoided for both, the IMC and the CMC.

Fig. 3.17 visualizes the formation of the apparent input power $\underline{S}_1$ based on the apparent output power $\underline{S}_2$. The limiting operating point regarding reactive input power compensation of a MC supplying a PMSM drive occurs at high speed (maximum output voltage) and no load. In this case the output current amplitude is minimal and the input phase displacement should be zero in order not to reduce the maximum output voltage. Consequently, according to (3.98), also the reactive input power is minimal. Even by applying special reactive power modulation strategies (cf. Tab. 3.5, RPSVM) if the instantaneous output current equals to zero, also the instantaneous input current is zero, which is a fundamental property of MCs. These interdependencies demonstrate in a figurative way the limitations of reactive input power control for drive systems with MCs.

Startup and Emergency Shutdown

The converter startup and emergency shutdown behavior impacts the reliability and robustness of the overall drive system and hence is compared for the individual converter topologies. Thereby it is assumed that resistors with a positive temperature coefficient are implemented in series with the input phases of the EMI input filters to enable a soft charging of the filter capacitors when the converter system is connected to the mains. After the precharging of the filter capacitors, the PTC resistors can be bypassed by a relay.

The converter startup is uncritical for all considered topologies. The simplest startup procedure can be performed for the MC due to its buck-type characteristic and lacking intermediate energy storage element. The regular modulation can be utilized during startup. The input stage of the CSBBC features also a buck-type characteristic and thus does not require specific startup circuitry similar to the MC. On the contrary, the VSBBC requires precharging of the dc-link capacitor prior to activation of the regular modulation. A possible measure of comparison is the

startup energy loss, which is significantly larger than the energy loss for charging the input filter capacitors. With regards to this consideration, the VSBBC is disadvantageous compared with the CSBBC and MC due to the energy loss E_{PC}, generated during the precharging interval $[0 \ldots \tau_{\mathrm{PC}}]$ in the resistance R_{PC} of the precharging path.

$$E_{\mathrm{PC}} = \int_0^{\tau_{\mathrm{PC}}} R_{\mathrm{PC}}\, i_{\mathrm{PC}}^2\, dt \approx \frac{1}{2} C_{\mathrm{DC}} \left(\sqrt{6}\, U_1\right)^2 = 3\, C_{\mathrm{DC}} U_1^2 \,. \qquad (3.101)$$

The emergency shutdown is considered for the scenario of a motor phase over-current, such that the motor currents cannot anymore be feedback controlled and a converter shutdown is inalienable. With the VSBBC, emergency shutdown is handled by deactivating the PWM signals of the output stage switches as a freewheeling path for the motor currents across the output stage diodes and the dc-link capacitor is inherently provided. For the CSBBC, enabling emergency shutdown capability is more elaborate. A solution is to implement powerful passive over-voltage protection devices for the output capacitors that can dissipate the whole energy stored in the drive train. In case of an over-current, the output stage is then switched to a zero state and the motor is de-energized with the limited voltage of the output capacitors. The MC features the most unfavorable emergency shutdown procedure. Due to the lack of a freewheeling path, the converter needs to be switched to a zero state when a severe failure is detected. This leads to a short circuit of the motor terminals and results in transient motor currents that may exceed the nominal motor current by a factor of three [282] and hence increases the stress on the power semiconductors and the risk for a demagnetization of the PMSM. Thus, when supplying motor loads with high inertia and/or are operating at high speed, particularly for MCs but also for CSBBCs a clamp circuit combined with a brake chopper and for VSBBCs a brake chopper across the dc-link capacitor should be implemented that can dissipate the energy of the load during emergency shut-down.

3.2.4 Dimensioning of Passive Components

Finally, the relationship between the control and the dimensioning of selected passive components is briefly discussed. The basic idea is to identify those passive components which have a limiting impact on the operating behavior of the converter. This is typically given for the main

energy storage elements of a converter topology. Obviously, a control based design is only one possibility besides additional design criteria such as maximum voltage or current ripple (cf. Sec. 6.3).

From an energy point of view the main purpose for an intermediate energy storage element in ac-ac converters is to decouple the load from the mains and vice versa. Two main strategies can be identified for the sizing of the energy storage element:

- A large energy storage combined with a suitable ("smooth") converter control is implemented to minimize the feedback of load changes to the mains, accepting an increase in converter volume.
- A small energy storage combined with a suitable ("stiff") converter control is implemented to minimize the converter volume, accepting an increase in mains feedback.

For the subsequent calculations the second strategy is pursued as the converter volume and therewith also the converter cost are typically higher prioritized than the mains feedback.

DC-Link Capacitor of the VSBBC

The dc-link capacitor is the main energy storage of the VSBBC. In order to limit the dc-link voltage variation, caused by a load change, it should be sized with respect to the control. The variation of the dc-link voltage during a power reversal is minimized by using the estimated output power as a feedforward signal for the current controller of the input stage. The instantaneous output power p_2^{**} is estimated based on the reference output voltages $u_{2\mathrm{d}}^*$ and $u_{2\mathrm{q}}^*$ of the output current controller and the measured output currents $i_{2\mathrm{d}}$ and $i_{2\mathrm{q}}$. The feedforward current of the input stage $i_{1\mathrm{d,ff}}$ then equals to

$$i_{1\mathrm{d,ff}} = \frac{2\,p_2^{**}}{3\,u_{1\mathrm{d}}} = \frac{u_{2\mathrm{d}}^* i_{2\mathrm{d}} + u_{2\mathrm{q}}^* i_{2\mathrm{q}}}{u_{1\mathrm{d}}}\,. \tag{3.102}$$

For a sufficiently accurate estimation ($\pm 5\%$) of the output power, the change of the link voltage due to a load change is not design-critical for the dc-link capacitor [283] if the load change is initiated by the converter control. In this case the coupling of the input and output stage control ensures that the dc-link voltage remains above the line-to-line voltage level.

The worst case occurs for an instantaneous load drop at nominal motor operation, which is caused by changing load or the motor contactor and therefore cannot be pre-controlled by the converter control. The input currents, impressed in the boost inductors L_B, then need to be controlled to zero as fast as possible in order to limit the dc-link voltage overshoot Δu_DC. Assuming regular sampling, the worst case dead time between the load drop and the effect of the control on the PWM signals of the input stage is two pulse periods ($2\,T_\mathrm{P}$). The relation between the pulse period and the switching frequency f_sw for the selected modulation scheme of the VSBBC is

$$T_\mathrm{P} = \frac{1}{f_\mathrm{sw}} \,. \tag{3.103}$$

For an allowable relative overshoot of the dc-link voltage

$$\delta_{\mathrm{u_{DC}}} = \frac{\Delta u_\mathrm{DC}}{U_\mathrm{DC}} \,, \tag{3.104}$$

the minimum value of the dc-link capacitance can then be calculated to

$$C_\mathrm{DC,min} = \frac{P_2}{18\,U_\mathrm{DC}\delta_{\mathrm{u_{DC}}}\eta^2} \left(\frac{\sqrt{3}\,L_\mathrm{B}P_2}{U_1^2 \left(\sqrt{2}\,U_1 + \frac{U_\mathrm{DC}}{\sqrt{3}} \right)} + \frac{36\,\eta}{U_\mathrm{DC} f_\mathrm{sw}} \right) \,, \tag{3.105}$$

whereas η represents the converter efficiency.

DC-Link Inductor of the CSBBC

The minimum value of the dc-link inductance is determined based on the same considerations as for the boost inductors of the VSBBC. Contrary to the VSBBC, a step-change of the load is rather uncritical as the dc-link current and the voltage across the output capacitors can be limited by switching the input and output stage of the CSBBC into a zero state.

In order to enable proper control of the dc-link current, the maximum dc-link current rise time from zero to its nominal value has to be limited to at least two pulse periods if the same sampling strategy is applied as for the VSBBC. Otherwise, a dc-link current overshoot of up to 100% of its nominal value would be possible. Assuming a worst case voltage of $3/\sqrt{2}U_1$ across the dc-link inductor, which occurs when the

output voltage equals zero ($U_2 = 0$), we then obtain for the minimum inductance

$$L_{\mathrm{DC,min}} = \frac{9\,U_1^2\eta}{P_2 f_{\mathrm{sw}}}\ . \tag{3.106}$$

A current ripple based design of the dc-link inductor typically leads to a higher minimal inductance (cf. Sec. 6.3) than for a control based design.

Filter Components of the MC

The main electrical energy storage of the MC is provided by the input capacitors $C_{\mathrm{F,inp}}$, which are part of the EMI input filter. The first DM stages of such a filter are presented in Fig. 3.18. Variations of the load (motor) currents are directly transferred to the input capacitors due to the absence of an intermediate energy storage element. If the current drawn from the input capacitors ($\underline{i}_1$) is larger than the current ($\underline{i}_{1,\mathrm{flt}}$) supplied through the DM inductors $L_{\mathrm{DM,2}}$ to the input capacitors, the capacitor voltage drops. Consequently, also the maximum converter output voltage is reduced as boost operation is not possible. From a control perspective it is hence reasonable to constrain the voltage drop Δu_{C} across the input capacitors by limiting the slope of the q-axis motor (output) current in the dq reference frame $di_{2\mathrm{q}}/dt$. For unity input power factor, the slope of the output current is transformed to a corresponding slope $di_{1\mathrm{d}}/dt$ of the input current.

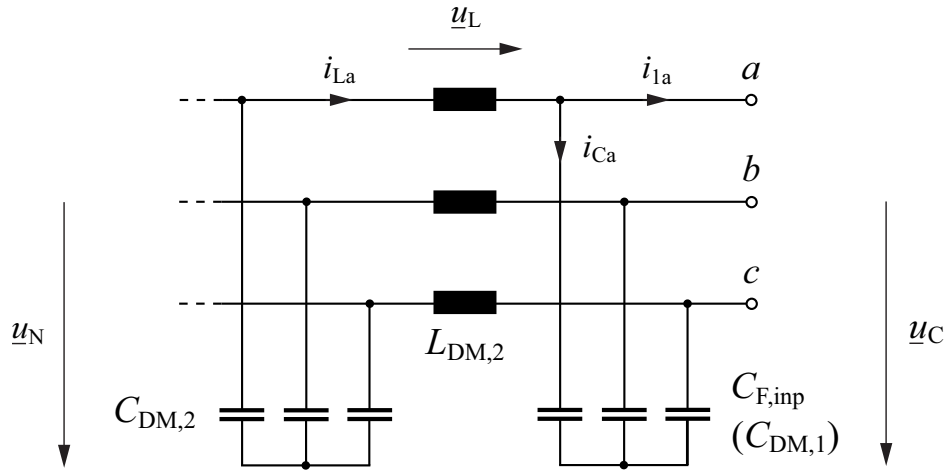


Fig. 3.18: Segment of a differential mode EMI input filter for a MC (or CSBBC), showing the first DM stage ($C_{\mathrm{F,inp}}$, $L_{\mathrm{DM,2}}$) and the capacitors ($C_{\mathrm{DM,2}}$) of the second DM stage.

The loop and node equations for the input filter segment, shown in Fig. 3.18, may be written as

$$\underline{u}_{\mathrm{N}} = \underline{u}_{\mathrm{L}} + \underline{u}_{\mathrm{C}} \tag{3.107}$$

$$\underline{i}_{\mathrm{L}} = \underline{i}_{\mathrm{C}} + \underline{i}_{1} \ . \tag{3.108}$$

Assuming unity input power factor with reference to $\underline{u}_1$ and $\underline{i}_1$, the voltage drop occurs in the d-axis capacitor voltage u_{Cd} when the load current is increased. The required differential equation can be derived from (3.108) and is given by

$$u_{\mathrm{Nd}} = \left(C_{\mathrm{F,inp}} \frac{d^2 u_{\mathrm{Cd}}}{dt^2} + \frac{di_{1\mathrm{d}}}{dt} \right) L_{\mathrm{DM},2} + u_{\mathrm{Cd}} \tag{3.109}$$

if the coupling between the d- and q-axis is neglected, which is allowable as is shown later in this section (cf. Fig. 3.19). Solving (3.109) for u_{Cd} leads to

$$u_{\mathrm{Cd}} = U_{\mathrm{Nd},0} + L_{\mathrm{DM},2} \frac{di_{1\mathrm{d}}}{dt} \left[\cos\left(\frac{t}{\sqrt{C_{\mathrm{F,inp}} L_{\mathrm{DM},2}}} \right) - 1 \right] \ . \tag{3.110}$$

Considering the output-to-input current transformation of MCs, the slope of the q-axis output current, which corresponds to the change of the motor torque in the dq reference frame, results at maximum modulation index $M_{12} = 1$ in the following slope of the d-axis input current

$$\frac{di_{1\mathrm{d}}}{dt} = \frac{\sqrt{3}}{2} \frac{di_{2\mathrm{q}}}{dt} \ . \tag{3.111}$$

By evaluating (3.110) for the minimum capacitor voltage and using (3.111), the relation between the voltage drop across the input filter capacitors Δu_{Cd} and the slope of the q-axis output current can be determined. Thereby it is assumed that the current rise time t_{rise} from zero to its nominal value is greater or equal than half of the period of the resonance frequency of $C_{\mathrm{F,inp}}$ and $L_{\mathrm{DM},2}$, which is given for typical filter and load (motor) parameters. The drop of the input capacitor voltage for a given slope of the q-axis output current can then be calculated to

$$\left. \frac{di_{2\mathrm{q}}}{dt} \right|_{\mathrm{max}} = \frac{\hat{U}_{\mathrm{N}} \delta_{\mathrm{uC}}}{\sqrt{3} L_{\mathrm{DM},2}} \qquad t_{\mathrm{rise}} \geq \pi \sqrt{C_{\mathrm{F,inp}} L_{\mathrm{DM},2}} \ , \tag{3.112}$$

whereas the relative voltage drop across the input capacitors is defined as

$$\delta_{\mathrm{uC}} = \frac{\Delta u_{\mathrm{Cd}}}{\hat{U}_{\mathrm{N}}} \ . \tag{3.113}$$

For given filter component parameters and a given constant slope of the q-axis output current, the voltage drop of the d-axis input filter capacitor voltage may be written as

$$\Delta u_{\mathrm{Cd}} = \sqrt{3} L_{\mathrm{DM},2} \frac{di_{2\mathrm{q}}}{dt} \qquad t_{\mathrm{rise}} \geq \pi \sqrt{C_{\mathrm{F,inp}} L_{\mathrm{DM},2}} \ . \tag{3.114}$$

Fig. 3.19 presents waveforms of the input capacitor voltage u_{Cd} for different input frequencies comparing the calculation in the dq reference frame with the calculation according to (3.110) for typical filter parameters such as $C_{\mathrm{F,inp}} = 30\,\mu\mathrm{F}$ and $L_{\mathrm{DM},2} = 150\,\mu\mathrm{H}$. The maximum slope of the load current for $\delta_{u_{\mathrm{C}}} = 10\%$ equals to $108\,\mathrm{A/ms}$. As can be seen, for an input mains frequency of 50 Hz, the coupling terms between the d- and q-axis can be neglected and the simplifications made in (3.109) do not lead to a significant error.

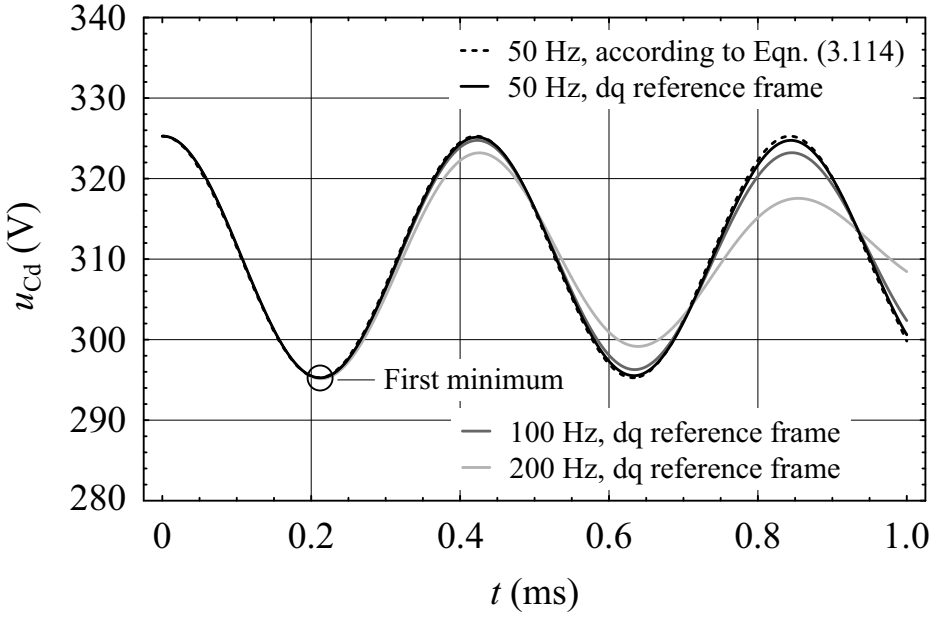


Fig. 3.19: Waveforms of the input capacitor voltage u_{Cd}, calculated for an input frequency of 50 Hz, 100 Hz, and 200 Hz in the dq reference frame and for comparison for 50 Hz according to (3.110). The slope of the load current starts at $t = 0$. $C_{\mathrm{F,inp}} = 30\,\mu\mathrm{F}$, $L_{\mathrm{DM},2} = 150\,\mu\mathrm{H}$, and $\hat{U}_{\mathrm{N}} = 325\,\mathrm{V}$.

Criterion	*Description*
Typical control variables (Feedback control)	Feedback control of the input stage Outer loop: dc-link voltage u ($f_{c,3}$) Inner loops: input currents $\underline{i}_1$ ($f_{c,1}$) Feedback control of the output stage Outer loop: motor speed ω_M ($f_{c,4}$) Inner loops: motor currents $\underline{i}_S$ ($f_{c,2}$) (equals to $\underline{i}_2$) 6 main feedback control loops
Feedforward control	Feedforward of the estimated output power to the input current controller Feedforward of the input voltage and the machine model Compensation of the reactive input filter current
Auxiliary control	PLL to track the phase angle $\varphi_{\underline{u}_1}$ Hysteresis control for an optional brake chopper in the dc-link
Measurement signals	3 input voltages u_a, u_b, u_c 1 dc-link voltage u_{DC} 2 (or 3) input currents, e.g. i_a, i_b 2 (or 3) output currents, e.g. i_A, i_B 1 rotary encoder
Boost operation	$U_2 > U_1$ possible
Reactive power transfer	Possible
Startup procedure	Precharging of the dc-link capacitor
Emergency shutdown	Noncritical, due to the freewheeling path across the dc-link capacitor
Equivalent dc-circuit	Boost-buck-type converter

Tab. 3.10: Properties of a basic cascaded feedback control scheme for a VSBBC based PMSM drive.

Criterion	*Description*
Typical control variables (Feedback control)	Feedback control of the input stage Loop: dc-link current i_{DC} ($f_{\mathrm{c},1}$) Feedback control of the output stage Outer loop: motor speed ω_{M} ($f_{\mathrm{c},4}$) Inner loops: motor currents $\underline{i}_{\mathrm{S}}$ ($f_{\mathrm{c},2}$) (equals to $\underline{i}_{2,\mathrm{flt}}$) 4 main feedback control loops
Feedforward control	Feedforward of the estimated output power to the dc-link current controller Feedforward of the input voltage and the machine model Compensation of the reactive input and output filter current
Auxiliary control	PLL to track the phase angle $\varphi_{\underline{u}_1}$, $\varphi_{\underline{u}_2}$ Hysteresis control of an optional clamp across the dc-link inductor
Measurement signals	3 input voltages u_{a}, u_{b}, u_{c} 3 output voltages u_{A}, u_{B}, u_{C} 1 dc-link current i_{DC} 2 (or 3) output currents, e.g. i_{A}, i_{B} 1 rotary encoder
Boost operation	$U_2 > U_1$ possible
Reactive power transfer	Possible
Startup procedure	No precharging required
Emergency shutdown	Over-voltage protection of the output capacitors $C_{\mathrm{F,out}}$ required
Equivalent dc-circuit	Buck-boost-type converter

Tab. 3.11: Properties of a basic cascaded feedback control scheme for a CSBBC based PMSM drive.

Criterion	*Description*
Typical control variables (Feedback control)	Feedback control Outer loop: motor speed ω_{M} ($f_{\mathrm{c},4}$) Inner loops: motor currents $\underline{i}_{\mathrm{S}}$ ($f_{\mathrm{c},2}$) (equals to $\underline{i}_2$) 3 main feedback control loops
Feedforward control	Feedforward of the input voltage to the output current controller Feedforward of the machine model Compensation of the reactive input filter current, results in a reduction of the maximum output voltage (**!**)
Auxiliary control	PLL to track the phase angle $\varphi_{\underline{u}_1}$ Hysteresis control of an optional clamp across the link (IMC)
Measurement signals	3 input voltages u_{a}, u_{b}, u_{c} 1 link voltage u (IMC) 2 (or 3) output currents, e.g. i_{A}, i_{B} 1 rotary encoder
Boost operation	Not possible, $U_{2,\max} = 0.866 \cdot U_1$
Reactive power transfer	Possible with the RPSVM scheme (cf. Tab. 3.5)
Startup procedure	No precharging required
Emergency shutdown	Special sequence required to provide in all cases a current path
Equivalent dc-circuit	Buck-type converter

Tab. 3.12: Properties of a basic cascaded feedback control scheme for a MC (CMC or IMC) based PMSM drive.

3.3 Summary

The modulation schemes of the VSBBC, CSBBC, IMC, and CMC have to be selected based on predefined criteria, in order to enable a fair comparison. In this selection process, the total semiconductor losses, the loss distribution to the individual devices, the commutation safety, and the EMI behavior are considered for different modulation schemes. The evaluation indicates that for all four converter topologies, discontinuous SVM schemes with only one freewheeling state per pulse period provide the best compromise. Starting from known commutation strategies, the discontinuous modulation schemes are adapted, if necessary, such that for all topologies loss- and/or CM-optimal clamping can be applied.

A configurable, generic modulator based on six relative turn-on times is suggested, which can be utilized to implement the modulation schemes of all four considered ac-ac converters. It is shown, that the calculation of the relative turn-on times of the VSBBC, CSBBC, IMC, and CMC requires approximately the same computational effort. The actual implementation of the modulator for the CMC is more intricate due to the multi-step commutation strategy.

Furthermore, a novel three-level output voltage SVM for the IMC topologies is proposed that can apply all three line-to-line input voltage levels at the converter output. This modulation scheme is specifically designed for an output voltage range from 58% to 100% of the maximum output voltage of MCs and minimizes the current ripple at the converter output by minimizing the duration of the freewheeling interval.

The major contribution of this investigation on modulation and control is the derivation of control based dimensioning criteria for the main energy storage elements of all four converter topologies. The results reveal that particularly for the MC the design of the first DM input filter stage ($C_{\mathrm{F,inp}}$, $L_{\mathrm{DM,1}}$) is critical for limiting the voltage variation across the input filter capacitors $C_{\mathrm{F,inp}}$ for a given slew rate of the converter output (load) current.

Chapter 4

Semiconductor Losses

With the modulation schemes defined, the characteristic electrical properties of the converter topologies under comparison are determined, and therewith the semiconductor losses can be modeled.

For that purpose, design-relevant operating points in the mission profile of ac-ac converters for motor drive applications are identified in the torque-speed plane, and a generalized procedure to calculate the resulting semiconductor losses is provided. Analytical equations are presented for all considered converter topologies to calculate the average semiconductor losses at different design-relevant operating points.

To conclude with, the similarities and the differences between the semiconductor losses of the individual topologies are briefly discussed.

4.1 Design-Relevant Operating Points

Bidirectional ac-ac converters for drive applications feature a wide range of different operating points in their mission profiles, reaching from stochastic (pulsed) start-stop operation to long-term continuous operation. For the dimensioning of the power semiconductors and for the semiconductor loss calculation, it is hence essential to identify adequate operating points.

The constraint is that at nominal operation all converter topologies provide the same electrical output power $P_{2,\mathrm{nom}}$ and, if for all drives the same motor efficiencies are assumed, the same mechanical shaft power $P_{\mathrm{M,nom}} < P_{2,\mathrm{nom}}$. Furthermore, the resulting operating points should be considered as stationary operating points in which the system can be operated without any temporal restrictions. A method to determine the required operating points is to consider the operating range of the drive system in the torque-speed plane for stationary continuous operation (S1 operation, continuous duty according to IEC 60034-1).

For the selection of design-relevant operating points, it should be noted that the semiconductor losses are modulated with the electrical input and/or output frequency of the converter. The time constant of the

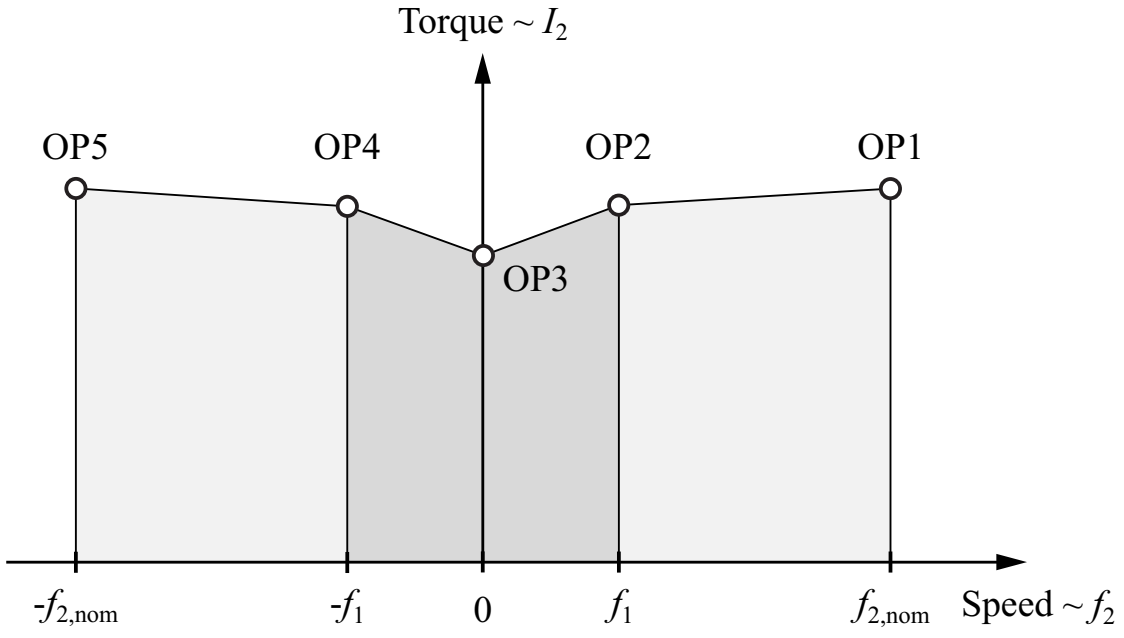


Fig. 4.1: Characteristic operating points of a bidirectional drive system, shown in two quadrants of the torque-speed plane.

thermal impedance between junction and sink of typical IGBT power modules is in the millisecond range. This means that the lower the resulting frequency that modulates the semiconductor losses is, the more is the modulation (pulsation) of the losses seen in a variation of the semiconductor junction temperature. Consequently, in order to limit the maximum junction temperature over the whole operating range to a desired value, the maximum output current and thus the available torque has to be reduced, for instance, at low output frequencies.

Fig. 4.1 depicts the design-relevant operating points that have been identified in the torque-speed plane based on the above considerations. For symmetry reasons, it is sufficient to consider only two instead of four quadrants.

- **OP1/OP5**: motor/generator operation at nominal motor speed (nominal electrical output frequency $f_2 = \pm f_{2,\mathrm{nom}}$) and nominal motor torque $M_{\mathrm{M,nom}}$.

- **OP2/OP4**: motor/generator operation at reduced motor speed (electrical output frequency equals the input frequency, $f_2 = \pm f_1$) and at motor torque $M_{\mathrm{M}} \leq M_{\mathrm{M,nom}}$.

- **OP3**: motor operation at electrical stand-still (electrical output frequency equals to zero, $f_2 = 0\,\mathrm{Hz}$) and at stand-still torque $M_{\mathrm{M},0}$. At this operating point it is assumed that the output voltage is typically restricted to 2% to 5% of the topology dependent maximum output voltage level. This is due to the ohmic voltage drop of the PMSM and the cable at stand-still.

From an application point of view, the operating points at nominal operation (OP1 and OP5) and at stand-still (OP3) are relevant for all four considered ac-ac converter topologies. Of particular interest are OP2 and OP4, which are critical operating points for the CMC only.

In order to enable a fair comparison, the switching frequency f_{sw} of the converters is defined with respect to the change of the switching states. It is selected such that at the converter output the frequency of the switching state transitions is identical for all converter topologies. The switching frequency of the input stage of the VSBBC and CSBBC is selected to be equal to the switching frequency of their output stage.

4.2 Semiconductor Loss Calculation

4.2.1 Loss Modeling

The average transistor and diode conduction losses $P_{\mathrm{cond,S/D}}$ are modeled with a junction temperature T_{J} dependent forward (or reverse) voltage drop $U_{\mathrm{S/D,F}}$ and a differential forward (or reverse) resistance $r_{\mathrm{S/D,F}}$ leading to

$$P_{\mathrm{cond,S/D}}(T_{\mathrm{J}}) = U_{\mathrm{S/D,F}}(T_{\mathrm{J}}) \cdot I_{\mathrm{S/D,avg}} + r_{\mathrm{S/D,F}}(T_{\mathrm{J}}) \cdot I^2_{\mathrm{S/D,rms}} \,. \tag{4.1}$$

$I_{\mathrm{S/D,avg}}$ and $I_{\mathrm{S/D,rms}}$ denote the average and the root mean square (rms) current of a certain time interval T_1.

$$I_{\mathrm{S/D,avg}} = \frac{1}{T_1} \int_0^{T_1} i_{\mathrm{S/D}} \, dt \qquad I_{\mathrm{S/D,rms}} = \sqrt{\frac{1}{T_1} \int_0^{T_1} i^2_{\mathrm{S/D}} \, dt} \tag{4.2}$$

The average transistor or diode switching losses $P_{\mathrm{sw,S/D}}$ are calculated based on the switching loss energy functions of the transistor or diode $w_{\mathrm{S/D,tot}}$. These switching loss energy functions model the loss energies of an entire switching cycle (turn-on and turn-off) depending on the switched current i, the switched voltage u, and the junction temperature T_{J}. For the transistors, the turn-on and turn-off losses are considered. However, for the bipolar diodes only the reverse-recovery (turn-off) losses are considered, whereas the forward-recovery losses are neglected. The mean switching loss energy $E_{\mathrm{S/D}}$ is then determined by averaging of $w_{\mathrm{S/D,tot}}$ over T_1.

$$E_{\mathrm{S/D}}\left(T_{\mathrm{J}}\right) = \frac{1}{T_1} \int_0^{T_1} w_{\mathrm{S/D,tot}}\left(i, u, T_{\mathrm{J}}\right) dt \tag{4.3}$$

The resulting overall switching losses for a given switching frequency f_{sw} may then be calculated as

$$P_{\mathrm{sw,S/D}}(T_{\mathrm{J}}) = f_{\mathrm{sw}} \cdot E_{\mathrm{S/D}}\left(T_{\mathrm{J}}\right) \,. \tag{4.4}$$

The total average semiconductor losses of a power device $P_{\mathrm{semi,S/D}}$ can then be expressed as the sum of the conduction and switching losses.

$$P_{\mathrm{semi,S/D}}(T_{\mathrm{J}}) = P_{\mathrm{cond,S/D}}(T_{\mathrm{J}}) + P_{\mathrm{sw,S/D}}(T_{\mathrm{J}}) \tag{4.5}$$

This loss calculation method is applicable to all considered ac-ac converter topologies and enables to determine the average semiconductor losses.

4.2.2 Procedure

In the following, the equations for the global average and rms currents and the average switching losses are provided for different design-relevant operating points of all investigated ac-ac converters. The individual quantities are calculated for the selected modulation schemes described in Chap. 3 for loss-optimal clamping (VSBBC, CSBBC, and IMC, cf. Fig. 3.3(b), Fig. 3.6(b), and Fig. 3.8) and CM-optimal clamping (CMC, cf. Fig. 3.13 and Tab. 3.9). The used calculation procedure is an extension of the approach shown in [131].

$I_{\mathrm{S/D,...,avg}}$ and $I_{\mathrm{S/D,...,rms}}$ refer to the global average and rms transistor or diode currents. $P_{\mathrm{sw,S/D,...}}$ describes the global average transistor or diode switching losses. The term "global" is used as these mean values are determined by averaging over at least one input and/or output period, but is not explicitly stated in the following.

Due to the requirement for unity input power factor, the phase displacement angle Φ_1 at the input is assumed to be either zero for motor operation or π for generator operation. The phase displacement angle Φ_2 at the output is limited to $0 \leq \Phi_2 \leq \pi/6$ for motor operation and to $\pi \leq \Phi_2 \leq 7\pi/6$ for generator operation. Consequently, the equations can be applied for drives utilizing a PMSM ($\Phi_2 \approx 0$) or an IM ($\Phi_2 \approx \pi/6$).

For OP3, if required, multiple worst case conditions are provided. Thereby, the phase displacement angle at the output is assumed to be zero as the comparison in this work is performed for a PMSM.

4.3 Loss Calculation of the VSBBC

The relevant operating points of the VSBBC are nominal motor operation (OP1), nominal generator operation (OP5), and motor operation at stand-still (OP3). The following mathematical relations are utilized for the loss calculation. $U_{\mathrm{DC}} = U$ indicates the dc-link voltage.

$$i_{\mathrm{a}} = \hat{I}_1 \cos\left(\varphi_1 - \Phi_1\right) \tag{4.6}$$

$$i_{\mathrm{A}} = \hat{I}_2 \cos\left(\varphi_2 - \Phi_2\right) \tag{4.7}$$

Calculation of the Average Transistor Current of the Output Stage $I_{\mathrm{S,out,avg}}$ for $0 \leq \Phi_2 \leq \pi/6$

The method to calculate the average and rms currents is presented, as an example, for the average transistor current of the output stage $I_{\mathrm{S,out,avg}}$. The averaging is based on the space vector calculus and is performed for the transistor S_{pA} of the output phase A (cf. Fig. 3.1). The relative turn-on times d_α and d_β are derived from (3.6) and (3.7), where $M_2 = [0 \ldots 1]$.

$$d_\alpha(\varphi_0) = M_2 \cos\left(\varphi_2 - \varphi_0 + \frac{\pi}{6}\right) \tag{4.8}$$

$$d_\beta(\varphi_0) = M_2 \sin(\varphi_2 - \varphi_0) \tag{4.9}$$

The average transistor current $I_{\mathrm{S,out,avg}}$ is calculated by averaging the current in the transistor S_{pA} over the individual sectors of the space vector hexagon.

$$I_{\mathrm{S,out,avg,1}} = \int_0^{\frac{\pi}{6}+\Phi_2} i_{\mathrm{A}} d\varphi_2 \tag{4.10}$$

$$I_{\mathrm{S,out,avg,2}} = \int_{\frac{\pi}{6}+\Phi_2}^{\frac{\pi}{3}} \left(d_\alpha(0) + d_\beta(0)\right) i_{\mathrm{A}} d\varphi_2 \tag{4.11}$$

$$I_{\mathrm{S,out,avg,3}} = \int_{\frac{\pi}{3}}^{\frac{\pi}{2}+\Phi_2} d_\alpha\left(\frac{\pi}{3}\right) i_{\mathrm{A}} d\varphi_2 \tag{4.12}$$

$$I_{\mathrm{S,out,avg,4}} = \int_{\frac{\pi}{2}+\Phi_2}^{\frac{3\pi}{2}+\Phi_2} 0 \cdot i_{\mathrm{A}} d\varphi_2 \tag{4.13}$$

$$I_{\mathrm{S,out,avg,5}} = \int_{\frac{3\pi}{2}+\Phi_2}^{\frac{5\pi}{3}} d_\beta\left(\frac{4\pi}{3}\right) i_{\mathrm{A}} d\varphi_2 \tag{4.14}$$

$$I_{\mathrm{S,out,avg,6}} = \int_{\frac{5\pi}{3}}^{\frac{11\pi}{6}+\Phi_2} \left(d_\alpha\left(\frac{5\pi}{3}\right) + d_\beta\left(\frac{5\pi}{3}\right)\right) i_{\mathrm{A}} d\varphi_2 \tag{4.15}$$

$$I_{\mathrm{S,out,avg,7}} = \int_{\frac{11\pi}{6}+\Phi_2}^{2\pi} i_{\mathrm{A}} d\varphi_2 \tag{4.16}$$

$$\Longrightarrow \qquad I_{\mathrm{S,out,avg}} = \frac{1}{2\pi}\left(\sum_{i=1}^{7} I_{\mathrm{S,out,avg},i}\right)$$

$$= \frac{6 + \sqrt{3}\pi M_2 \cos(\Phi_2)}{12\pi} \cdot \hat{I}_2 \tag{4.17}$$

4.3.1 Nominal Motor Operation (OP1)

Input Stage Average and RMS Currents ($\Phi_1 = 0$)

$$I_{\mathrm{S,inp,avg}} = \frac{6 - \sqrt{3}\pi M_1}{12\pi} \cdot \hat{I}_1 \tag{4.18}$$

$$I^2_{\mathrm{S,inp,rms}} = \frac{4\pi - \sqrt{3}\,(3 + 4M_1)}{24\pi} \cdot \hat{I}_1^2 \tag{4.19}$$

$$I_{\mathrm{D,inp,avg}} = \frac{6 + \sqrt{3}\pi M_1}{12\pi} \cdot \hat{I}_1 \tag{4.20}$$

$$I^2_{\mathrm{D,inp,rms}} = \frac{2\pi + \sqrt{3}\,(3 + 4M_1)}{24\pi} \cdot \hat{I}_1^2 \tag{4.21}$$

Input Stage Switching Losses ($\Phi_1 = 0$)

$$P_{\mathrm{sw,S,inp}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{-\frac{\pi}{2}}^{-\frac{\pi}{6}} w_{\mathrm{S,tot}}\left(i_{\mathrm{a}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_1 + \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} w_{\mathrm{S,tot}}\left(i_{\mathrm{a}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_1 \right) \tag{4.22}$$

$$P_{\mathrm{sw,D,inp}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{-\frac{\pi}{2}}^{-\frac{\pi}{6}} w_{\mathrm{D,tot}}\left(i_{\mathrm{a}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_1 + \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} w_{\mathrm{D,tot}}\left(i_{\mathrm{a}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_1 \right) \tag{4.23}$$

Output Stage Average and RMS Currents ($0 \leq \Phi_2 \leq \pi/6$)

$$I_{\mathrm{S,out,avg}} = \frac{6 + \sqrt{3}\pi M_2 \cos\left(\Phi_2\right)}{12\pi} \cdot \hat{I}_2 \tag{4.24}$$

$$I^2_{\mathrm{S,out,rms}} = \frac{2\pi + \sqrt{3}\left(3 + 4M_2 \cos\left(\Phi_2\right)\right)}{24\pi} \cdot \hat{I}_2^2 \tag{4.25}$$

$$I_{\mathrm{D,out,avg}} = \frac{6 - \sqrt{3}\pi M_2 \cos\left(\Phi_2\right)}{12\pi} \cdot \hat{I}_2 \tag{4.26}$$

$$I^2_{\mathrm{D,out,rms}} = \frac{4\pi - \sqrt{3}\left(3 + 4M_2 \cos\left(\Phi_2\right)\right)}{24\pi} \cdot \hat{I}_2^2 \tag{4.27}$$

Output Stage Switching Losses ($0 \leq \Phi_2 \leq \pi/6$)

$$P_{\mathrm{sw,S,out}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{6}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_2 + \int_{\frac{\pi}{6}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_2 \right) \tag{4.28}$$

$$P_{\mathrm{sw,D,out}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{6}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_2 + \int_{\frac{\pi}{6}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_2 \right) \tag{4.29}$$

4.3.2 Nominal Generator Operation (OP5)

Input Stage Average and RMS Currents ($\Phi_1 = \pi$)

$$I_{\mathrm{S,inp,avg}} = \frac{6 + \sqrt{3}\pi M_1}{12\pi} \cdot \hat{I}_1 \tag{4.30}$$

$$I^2_{\mathrm{S,inp,rms}} = \frac{2\pi + \sqrt{3}\left(3 + 4M_1\right)}{24\pi} \cdot \hat{I}_1^2 \tag{4.31}$$

$$I_{\mathrm{D,inp,avg}} = \frac{6 - \sqrt{3}\pi M_1}{12\pi} \cdot \hat{I}_1 \tag{4.32}$$

$$I^2_{\mathrm{D,inp,rms}} = \frac{4\pi - \sqrt{3}\left(3 + 4M_1\right)}{24\pi} \cdot \hat{I}_1^2 \tag{4.33}$$

Input Stage Switching Losses ($\Phi_1 = \pi$)

$$P_{\mathrm{sw,S,inp}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{\frac{\pi}{2}}^{\frac{5\pi}{6}} w_{\mathrm{S,tot}}\left(i_{\mathrm{a}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_1 + \int_{\frac{7\pi}{6}}^{\frac{3\pi}{2}} w_{\mathrm{S,tot}}\left(i_{\mathrm{a}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_1 \right) \tag{4.34}$$

$$P_{\mathrm{sw,D,inp}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{\frac{\pi}{2}}^{\frac{5\pi}{6}} w_{\mathrm{D,tot}}\left(i_{\mathrm{a}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_1 + \int_{\frac{7\pi}{6}}^{\frac{3\pi}{2}} w_{\mathrm{D,tot}}\left(i_{\mathrm{a}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_1 \right) \tag{4.35}$$

Output Stage Average and RMS Currents ($\pi \leq \Phi_2 \leq 7\pi/6$)

$$I_{\mathrm{S,out,avg}} = \frac{6 + \sqrt{3}\pi M_2 \cos(\Phi_2)}{12\pi} \cdot \hat{I}_2 \tag{4.36}$$

$$I^2_{\mathrm{S,out,rms}} = \frac{4\pi - \sqrt{3}\,(3 - 4M_2 \cos(\Phi_2))}{24\pi} \cdot \hat{I}_2^2 \tag{4.37}$$

$$I_{\mathrm{D,out,avg}} = \frac{6 - \sqrt{3}\pi M_2 \cos(\Phi_2)}{12\pi} \cdot \hat{I}_2 \tag{4.38}$$

$$I^2_{\mathrm{D,out,rms}} = \frac{2\pi + \sqrt{3}\,(3 - 4M_2 \cos(\Phi_2))}{24\pi} \cdot \hat{I}_2^2 \tag{4.39}$$

Output Stage Switching Losses ($\pi \leq \Phi_2 \leq 7\pi/6$)

$$P_{\mathrm{sw,S,out}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{6}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_2 + \int_{\frac{\pi}{6}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_2 \right) \tag{4.40}$$

$$P_{\mathrm{sw,D,out}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{6}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_2 + \int_{\frac{\pi}{6}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, U_{\mathrm{DC}}, T_{\mathrm{J}}\right) d\varphi_2 \right) \tag{4.41}$$

4.3.3 Total Semiconductor Losses (OP1 or OP5)

The total average semiconductor losses $P_{\mathrm{semi,tot}}$ at OP1 or OP5 can be calculated by summing the semiconductor losses of all input and output stage transistors and diodes.

$$\begin{aligned} P_{\mathrm{semi,tot}} = {} & 6\,\big(U_{\mathrm{S,F,inp}} I_{\mathrm{S,inp,avg}} + r_{\mathrm{S,F,inp}} I^2_{\mathrm{S,inp,rms}} + \\ & U_{\mathrm{D,F,inp}} I_{\mathrm{D,inp,avg}} + r_{\mathrm{D,F,inp}} I^2_{\mathrm{D,inp,rms}} + \\ & P_{\mathrm{sw,S,inp}} + P_{\mathrm{sw,D,inp}}\big) + \\ & 6\,\big(U_{\mathrm{S,F,out}} I_{\mathrm{S,out,avg}} + r_{\mathrm{S,F,out}} I^2_{\mathrm{S,out,rms}} + \\ & U_{\mathrm{D,F,out}} I_{\mathrm{D,out,avg}} + r_{\mathrm{D,F,out}} I^2_{\mathrm{D,out,rms}} + \\ & P_{\mathrm{sw,S,out}} + P_{\mathrm{sw,D,out}}\big)\big|_{\mathrm{OP1} \vee \mathrm{OP5}} \end{aligned} \tag{4.42}$$

4.3.4 Motor Operation at Stand-Still (OP3)

The worst case semiconductor stresses for motor operation at electrical stand-still occur in the output stage of the VSBBC. The maximum semiconductor losses are determined for the transistor S_{pA} and the diode D_{nA} of the bridge-leg of the output phase A.

Output Stage Transistor S_{pA} and Diode D_{nA} at $\varphi_2 = 0$ ($\Phi_1 = 0$ and $\Phi_2 = 0$)

$$I_{\mathrm{SpA,avg}} = \hat{I}_2 \tag{4.43}$$

$$I^2_{\mathrm{SpA,rms}} = \hat{I}_2^2 \tag{4.44}$$

$$I_{\mathrm{DnA,avg}} = 0 \tag{4.45}$$

$$I^2_{\mathrm{DnA,rms}} = 0 \tag{4.46}$$

$$P_{\mathrm{sw,SpA}} = 0 \tag{4.47}$$

$$P_{\mathrm{sw,DnA}} = 0 \tag{4.48}$$

Output Stage Transistor S_{pA} and Diode D_{nA} at $\varphi_2 = \pi/6$ ($\Phi_1 = 0$ and $\Phi_2 = 0$)

$$I_{\mathrm{SpA,avg}} = \frac{\sqrt{3}}{2} M_2 \cdot \hat{I}_2 \tag{4.49}$$

$$I^2_{\mathrm{SpA,rms}} = \frac{3}{4} M_2 \cdot \hat{I}_2^2 \tag{4.50}$$

$$I_{\mathrm{DnA,avg}} = \frac{\sqrt{3}}{2} (1 - M_2) \cdot \hat{I}_2 \tag{4.51}$$

$$I^2_{\mathrm{DnA,rms}} = \frac{3}{4} (1 - M_2) \cdot \hat{I}_2^2 \tag{4.52}$$

$$P_{\mathrm{sw,SpA}} = f_{\mathrm{sw}} w_{\mathrm{S,tot}} \left(\frac{\sqrt{3}}{2} \hat{I}_2, U_{\mathrm{DC}}, T_{\mathrm{J}} \right) \tag{4.53}$$

$$P_{\mathrm{sw,DnA}} = f_{\mathrm{sw}} w_{\mathrm{D,tot}} \left(\frac{\sqrt{3}}{2} \hat{I}_2, U_{\mathrm{DC}}, T_{\mathrm{J}} \right) \tag{4.54}$$

4.4 Loss Calculation of the CSBBC

Similar to the VSBBC, the relevant operating points of the CSBBC are nominal motor operation (OP1), nominal generator operation (OP5), and motor operation at stand-still (OP3). The subsequent mathematical relations are required for the loss calculation. $I_{\mathrm{DC}} = I$ denotes the dc-link current, $u_{\mathrm{com,inp}}$ refers to the commutation voltage of the input stage, and $u_{\mathrm{com,out}}$ to the commutation voltage of the output stage.

$$u_{\mathrm{com,inp}} = \sqrt{3}\,\hat{U}_1 \sin\left(\varphi_1 - \Phi_1\right) \tag{4.55}$$

$$u_{\mathrm{com,out}} = \sqrt{3}\,\hat{U}_2 \sin\left(\varphi_2 - \Phi_2\right) \tag{4.56}$$

4.4.1 Nominal Motor Operation (OP1)

Input and Output Stage Average and RMS Currents

The average transistor and diode current and the rms transistor and diode current of the input and output stage are identical and do neither depend on the phase displacement at the input nor on the phase displacement at the output.

$$I_{\mathrm{S,inp,avg}} = I_{\mathrm{S,out,avg}} = I_{\mathrm{D,inp,avg}} = I_{\mathrm{D,out,avg}} = I_{\mathrm{avg}} = \frac{1}{3} \cdot I_{\mathrm{DC}} \tag{4.57}$$

$$I^2_{\mathrm{S,inp,rms}} = I^2_{\mathrm{S,out,rms}} = I^2_{\mathrm{D,inp,rms}} = I^2_{\mathrm{D,out,rms}} = I^2_{\mathrm{rms}} = \frac{1}{3} \cdot I^2_{\mathrm{DC}} \tag{4.58}$$

Input Stage Switching Losses ($\boldsymbol{\Phi_1 = 0}$)

$$P_{\mathrm{sw,S,inp}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_0^{\frac{\pi}{3}} w_{\mathrm{S,tot}}\left(I_{\mathrm{DC}}, u_{\mathrm{com,inp}}, T_{\mathrm{J}}\right) d\varphi_1 + \int_{\frac{2\pi}{3}}^{\pi} w_{\mathrm{S,tot}}\left(I_{\mathrm{DC}}, u_{\mathrm{com,inp}}, T_{\mathrm{J}}\right) d\varphi_1 \right) \tag{4.59}$$

$$P_{\mathrm{sw,D,inp}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{\pi}^{\frac{4\pi}{3}} w_{\mathrm{D,tot}}\left(I_{\mathrm{DC}}, -u_{\mathrm{com,inp}}, T_{\mathrm{J}}\right) d\varphi_1 + \int_{\frac{5\pi}{3}}^{2\pi} w_{\mathrm{D,tot}}\left(I_{\mathrm{DC}}, -u_{\mathrm{com,inp}}, T_{\mathrm{J}}\right) d\varphi_1 \right) \tag{4.60}$$

Output Stage Switching Losses ($0 \leq \Phi_2 \leq \pi/6$)

$$P_{\mathrm{sw,S,out}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{\Phi_2}^{\frac{\pi}{3}+\Phi_2} w_{\mathrm{S,tot}} \left(I_{\mathrm{DC}}, u_{\mathrm{com,out}}, T_{\mathrm{J}}\right) d\varphi_2 + \int_{\frac{2\pi}{3}+\Phi_2}^{\pi+\Phi_2} w_{\mathrm{S,tot}} \left(I_{\mathrm{DC}}, u_{\mathrm{com,out}}, T_{\mathrm{J}}\right) d\varphi_2 \right) \tag{4.61}$$

$$P_{\mathrm{sw,D,out}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{\pi+\Phi_2}^{\frac{4\pi}{3}+\Phi_2} w_{\mathrm{D,tot}} \left(I_{\mathrm{DC}}, -u_{\mathrm{com,out}}, T_{\mathrm{J}}\right) d\varphi_2 + \int_{\frac{5\pi}{3}+\Phi_2}^{2\pi+\Phi_2} w_{\mathrm{D,tot}} \left(I_{\mathrm{DC}}, -u_{\mathrm{com,out}}, T_{\mathrm{J}}\right) d\varphi_2 \right) \tag{4.62}$$

4.4.2 Nominal Generator Operation (OP5)

Input and Output Stage Average and RMS Currents

$$I_{\mathrm{S,inp,avg}} = I_{\mathrm{S,out,avg}} = I_{\mathrm{D,inp,avg}} = I_{\mathrm{D,out,avg}} = I_{\mathrm{avg}} = \frac{1}{3} \cdot I_{\mathrm{DC}} \tag{4.63}$$

$$I^2_{\mathrm{S,inp,rms}} = I^2_{\mathrm{S,out,rms}} = I^2_{\mathrm{D,inp,rms}} = I^2_{\mathrm{D,out,rms}} = I^2_{\mathrm{rms}} = \frac{1}{3} \cdot I^2_{\mathrm{DC}} \tag{4.64}$$

Input Stage Switching Losses ($\Phi_1 = \pi$)

$$P_{\mathrm{sw,S,inp}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{\pi}^{\frac{4\pi}{3}} w_{\mathrm{S,tot}} \left(I_{\mathrm{DC}}, u_{\mathrm{com,inp}}, T_{\mathrm{J}}\right) d\varphi_1 + \int_{\frac{5\pi}{3}}^{2\pi} w_{\mathrm{S,tot}} \left(I_{\mathrm{DC}}, u_{\mathrm{com,inp}}, T_{\mathrm{J}}\right) d\varphi_1 \right) \tag{4.65}$$

$$P_{\mathrm{sw,D,inp}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{0}^{\frac{\pi}{3}} w_{\mathrm{D,tot}} \left(I_{\mathrm{DC}}, -u_{\mathrm{com,inp}}, T_{\mathrm{J}}\right) d\varphi_1 + \int_{\frac{2\pi}{3}}^{\pi} w_{\mathrm{D,tot}} \left(I_{\mathrm{DC}}, -u_{\mathrm{com,inp}}, T_{\mathrm{J}}\right) d\varphi_1 \right) \tag{4.66}$$

Output Stage Switching Losses ($\pi \leq \Phi_2 \leq 7\pi/6$)

$$P_{\mathrm{sw,S,out}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{\Phi_2}^{\frac{\pi}{3}+\Phi_2} w_{\mathrm{S,tot}} \left(I_{\mathrm{DC}}, u_{\mathrm{com,out}}, T_{\mathrm{J}} \right) d\varphi_2 + \int_{\frac{2\pi}{3}+\Phi_2}^{\pi+\Phi_2} w_{\mathrm{S,tot}} \left(I_{\mathrm{DC}}, u_{\mathrm{com,out}}, T_{\mathrm{J}} \right) d\varphi_2 \right) \tag{4.67}$$

$$P_{\mathrm{sw,D,out}} = \frac{1}{2\pi} f_{\mathrm{sw}} \left(\int_{\pi+\Phi_2}^{\frac{4\pi}{3}+\Phi_2} w_{\mathrm{D,tot}} \left(I_{\mathrm{DC}}, -u_{\mathrm{com,out}}, T_{\mathrm{J}} \right) d\varphi_2 + \int_{\frac{5\pi}{3}+\Phi_2}^{2\pi+\Phi_2} w_{\mathrm{D,tot}} \left(I_{\mathrm{DC}}, -u_{\mathrm{com,out}}, T_{\mathrm{J}} \right) d\varphi_2 \right) \tag{4.68}$$

4.4.3 Total Semiconductor Losses (OP1 or OP5)

The total average semiconductor losses of the CSBBC at OP1 or OP5 may be calculated by summing the semiconductor losses of all input and output stage transistors and diodes similar to the VSBBC. Compared with the VSBBC, the average and rms currents are the same for all power devices.

$$\begin{aligned} P_{\mathrm{semi,tot}} = 6 \big(& \left(U_{\mathrm{S,F,inp}} + U_{\mathrm{D,F,inp}} + U_{\mathrm{S,F,out}} + U_{\mathrm{D,F,out}} \right) I_{\mathrm{avg}} + \\ & \left(r_{\mathrm{S,F,inp}} + r_{\mathrm{D,F,inp}} + r_{\mathrm{S,F,out}} + r_{\mathrm{D,F,out}} \right) I_{\mathrm{rms}}^2 + \\ & P_{\mathrm{sw,S,inp}} + P_{\mathrm{sw,D,inp}} + \\ & P_{\mathrm{sw,S,out}} + P_{\mathrm{sw,D,out}} \big) \big|_{\mathrm{OP1} \vee \mathrm{OP5}} \end{aligned} \tag{4.69}$$

4.4.4 Motor Operation at Stand-Still (OP3)

At this operating point the worst case semiconductor stresses occur in the output stage of the CSBBC. The maximum semiconductor losses are determined for the transistor S_{pA} and the diode D_{pA} of the phase-leg of the output phase A. The switching losses of the transistor and the diode can be neglected at OP3 as the output voltage and thus the commutation voltage is close to zero.

Output Stage Transistor S_{pA} and Diode D_{pA} at $\varphi_2 = 0$ ($\Phi_1 = 0$ and $\Phi_2 = 0$)

$$I_{\mathrm{SpA,avg}} = \hat{I}_2 \tag{4.70}$$

$$I^2_{\mathrm{SpA,rms}} = \hat{I}_2^2 \tag{4.71}$$

$$I_{\mathrm{DpA,avg}} = \hat{I}_2 \tag{4.72}$$

$$I^2_{\mathrm{DpA,rms}} = \hat{I}_2^2 \tag{4.73}$$

$$P_{\mathrm{sw,SpA}} = 0 \tag{4.74}$$

$$P_{\mathrm{sw,DpA}} = 0 \tag{4.75}$$

Side note: At stationary electrical stand-still, the output stage of the CSBBC with its filtering capacitors may be considered as a boost type dc-dc converter which is operated with a switched input voltage.

4.5 Loss Calculation of the IMC

The relevant operating points of the IMC are the same as for the VSBBC and the CSBBC: nominal motor operation (OP1), nominal generator operation (OP5), and motor operation at stand-still (OP3). The following mathematical relations are utilized for the loss calculation.

$$u_{\mathrm{ab}} = \sqrt{3}\,\hat{U}_1 \cos\left(\varphi_1 + \frac{\pi}{6}\right) \tag{4.76}$$

$$u_{\mathrm{ac}} = \sqrt{3}\,\hat{U}_1 \cos\left(\varphi_1 - \frac{\pi}{6}\right) \tag{4.77}$$

$$i_{\mathrm{A}} = \hat{I}_2 \cos\left(\varphi_2 - \Phi_2\right) \tag{4.78}$$

$$i_{\mathrm{C}} = \hat{I}_2 \cos\left(\varphi_2 + \frac{2\pi}{3} - \Phi_2\right) \tag{4.79}$$

4.5.1 Nominal Motor Operation (OP1)

Input Stage Average and RMS Currents ($\Phi_1 = 0$ and $0 \leq \Phi_2 \leq \pi/6$)

Due to the bidirectional switches in the input stage of the IMC, the current path of the input stage can be subdivided into a forward and a return path with the corresponding transistor and diode average and rms forward currents $I_{\mathrm{S/D,F,inp,avg}}$ and $I_{\mathrm{S/D,F,inp,rms}}$ and reverse currents $I_{\mathrm{S/D,R,inp,avg}}$ and $I_{\mathrm{S/D,R,inp,rms}}$.

The forward path involves all power semiconductors that enable a current flow from the mains to the positive bus p and from the negative bus n back to the mains (cf. Fig. 3.7). Likewise, the reverse path involves all power semiconductors that enable a current flow from the mains to the negative bus n and from the positive bus p back to the mains. For a phase displacement angle of $0 \leq \Phi_2 \leq \pi/6$, the link current is greater or equal than zero ($i \geq 0$) and thus the reverse currents $I_{\mathrm{S/D,R,inp,avg}}$ and $I_{\mathrm{S/D,R,inp,rms}}$ equal to zero.

The derivation of the equation for $I_{\mathrm{S/D,F,inp,avg}}$ is shown as an example for the calculation of the average and rms input currents at OP1. The required total relative turn-on times d_α and d_β are derived from (3.39) to (3.42), and $M_{12} = [0 \ldots 1]$.

$$d_\alpha(\varphi_0) = M_{12}\cos(\varphi_1)\cos\left(\varphi_2 - \varphi_0 + \frac{\pi}{6}\right) \tag{4.80}$$

$$d_\beta(\varphi_0) = M_{12}\cos(\varphi_1)\sin(\varphi_2 - \varphi_0) \tag{4.81}$$

For the input currents, we then obtain the equations below.

$$\begin{aligned} I_{\mathrm{S,F,inp,avg}} &= I_{\mathrm{D,F,inp,avg}} \\ &= \frac{3}{\pi^2}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}}\left[\int_0^{\frac{\pi}{6}+\Phi_2} d_\alpha(0)\, i_{\mathrm{A}} - d_\beta(0)\, i_{\mathrm{C}}\, d\varphi_2 + \right. \\ &\qquad \left. \int_{\frac{\pi}{6}+\Phi_2}^{\frac{\pi}{3}} d_\alpha(0)\, i_{\mathrm{A}} - d_\beta(0)\, i_{\mathrm{C}}\, d\varphi_2\right] d\varphi_1 \\ &= \frac{\sqrt{3}M_{12}\cos(\Phi_2)}{2\pi}\cdot\hat{I}_2 \end{aligned} \tag{4.82}$$

$$I^2_{\mathrm{S,F,inp,rms}} = I^2_{\mathrm{D,F,inp,rms}} = \frac{M_{12}\left(3 + 2\cos(2\Phi_2)\right)}{2\pi^2}\cdot\hat{I}_2^2 \tag{4.83}$$

$$I_{\mathrm{S,R,inp,avg}} = I_{\mathrm{D,R,inp,avg}} = I^2_{\mathrm{S,R,inp,rms}} = I^2_{\mathrm{D,R,inp,rms}} = 0 \tag{4.84}$$

Output Stage Average and RMS Currents ($\Phi_1 = 0$ and $0 \leq \Phi_2 \leq \pi/6$)

The average and rms currents of the output stage are calculated based on the same principle as shown for the VSBBC in (4.17).

$$I_{\mathrm{S,out,avg}} = \frac{2 + \sqrt{3} M_{12} \cos\left(\Phi_2\right)}{4\pi} \cdot \hat{I}_2 \tag{4.85}$$

$$I^2_{\mathrm{S,out,rms}} = \frac{\pi\left(2\pi + 3\sqrt{3}\right) + 12\sqrt{3} M_{12} \cos\left(\Phi_2\right)}{24\pi^2} \cdot \hat{I}_2^2 \tag{4.86}$$

$$I_{\mathrm{D,out,avg}} = \frac{2 - \sqrt{3} M_{12} \cos\left(\Phi_2\right)}{4\pi} \cdot \hat{I}_2 \tag{4.87}$$

$$I^2_{\mathrm{D,out,rms}} = \frac{\pi\left(4\pi - 3\sqrt{3}\right) - 12\sqrt{3} M_{12} \cos\left(\Phi_2\right)}{24\pi^2} \cdot \hat{I}_2^2 \tag{4.88}$$

Output Stage Switching Losses ($\Phi_1 = 0$ and $0 \leq \Phi_2 \leq \pi/6$)

The voltage-source-type output stage of the IMC is modulated similarly to the VSBBC with loss-optimal clamping. Contrary to the VSBBC, the switched voltage, which corresponds to the link voltage, is not constant, but varies with the input phase angle φ_1 (cf. Fig. 3.10(a)). Consequently, the average switching losses of the output stage have to be calculated by averaging over the switched link voltage and the switched output current.

f_{sw} refers to the switching frequency of the output stage and is twice the switching frequency of the input stage for the selected modulation scheme.

$$\begin{aligned} P_{\mathrm{sw,S,out}} = \frac{3}{2\pi^2} \frac{f_{\mathrm{sw}}}{2} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} \Bigg[& \int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{6}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + \\ & \qquad w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 + \\ & \int_{\frac{\pi}{6}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + \\ & \qquad w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 \Bigg] d\varphi_1 \end{aligned} \tag{4.89}$$

$$P_{\mathrm{sw,D,out}} = \frac{3}{2\pi^2}\frac{f_{\mathrm{sw}}}{2}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}}\Bigg[\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{6}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 + \int_{\frac{\pi}{6}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2\Bigg] d\varphi_1 \quad (4.90)$$

4.5.2 Nominal Generator Operation (OP5)

Input Stage Average and RMS Currents ($\boldsymbol{\Phi_1 = \pi}$ and $\boldsymbol{\pi \leq \Phi_2 \leq 7\pi/6}$)

For a phase displacement angle of $\pi \leq \Phi_2 \leq 7\pi/6$, the link current is less or equal than zero ($i \leq 0$), and thus the mean forward currents $I_{\mathrm{S/D,F,inp,avg}}$ and $I_{\mathrm{S/D,F,inp,rms}}$ equal to zero, whereas the reverse currents $I_{\mathrm{S/D,R,inp,avg}}$ and $I_{\mathrm{S/D,R,inp,rms}}$ are different from zero.

$$I_{\mathrm{S,F,inp,avg}} = I_{\mathrm{D,F,inp,avg}} = I^2_{\mathrm{S,F,inp,rms}} = I^2_{\mathrm{D,F,inp,rms}} = 0 \quad (4.91)$$

$$I_{\mathrm{S,R,inp,avg}} = I_{\mathrm{D,R,inp,avg}} = -\frac{\sqrt{3}M_{12}\cos\left(\Phi_2\right)}{2\pi}\cdot\hat{I}_2 \quad (4.92)$$

$$I^2_{\mathrm{S,R,inp,rms}} = I^2_{\mathrm{D,R,inp,rms}} = \frac{M_{12}\left(3+2\cos\left(2\Phi_2\right)\right)}{2\pi^2}\cdot\hat{I}_2^2 \quad (4.93)$$

Output Stage Average and RMS Currents ($\boldsymbol{\Phi_1 = \pi}$ and $\boldsymbol{\pi \leq \Phi_2 \leq 7\pi/6}$)

$$I_{\mathrm{S,out,avg}} = \frac{2+\sqrt{3}M_{12}\cos\left(\Phi_2\right)}{4\pi}\cdot\hat{I}_2 \quad (4.94)$$

$$I^2_{\mathrm{S,out,rms}} = \frac{\pi\left(4\pi-3\sqrt{3}\right)+12\sqrt{3}M_{12}\cos\left(\Phi_2\right)}{24\pi^2}\cdot\hat{I}_2^2 \quad (4.95)$$

$$I_{\mathrm{D,out,avg}} = \frac{2-\sqrt{3}M_{12}\cos\left(\Phi_2\right)}{4\pi}\cdot\hat{I}_2 \quad (4.96)$$

$$I^2_{\mathrm{D,out,rms}} = \frac{\pi\left(2\pi+3\sqrt{3}\right)-12\sqrt{3}M_{12}\cos\left(\Phi_2\right)}{24\pi^2}\cdot\hat{I}_2^2 \quad (4.97)$$

Output Stage Switching Losses ($\Phi_1 = \pi$ and $\pi \leq \Phi_2 \leq 7\pi/6$)

$$P_{\mathrm{sw,S,out}} = \frac{3}{2\pi^2}\frac{f_{\mathrm{sw}}}{2}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}}\Bigg[\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{6}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right)+ w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right)d\varphi_2+ \int_{\frac{\pi}{6}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right)+ w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right)d\varphi_2\Bigg]d\varphi_1 \quad (4.98)$$

$$P_{\mathrm{sw,D,out}} = \frac{3}{2\pi^2}\frac{f_{\mathrm{sw}}}{2}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}}\Bigg[\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{6}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right)+ w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right)d\varphi_2+ \int_{\frac{\pi}{6}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right)+ w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right)d\varphi_2\Bigg]d\varphi_1 \quad (4.99)$$

4.5.3 Total Semiconductor Losses (OP1 or OP5)

As a result of the restriction imposed on the phase displacement angle Φ_2 at OP1 and OP5, either the transistors and diodes of the forward current path or of the reverse current path are conducting for a constant phase displacement angle at the output. Consequently, only six of the twelve power semiconductors of the input stage need to be considered for the calculation of the total average semiconductor losses.

$$\begin{aligned} P_{\mathrm{semi,tot}} = {} & 6\left(U_{\mathrm{S,F,inp}} I_{\mathrm{S,F/R,inp,avg}} + r_{\mathrm{S,F,inp}} I^2_{\mathrm{S,F/R,inp,rms}} + \right. \\ & \left. U_{\mathrm{D,F,inp}} I_{\mathrm{D,F/R,inp,avg}} + r_{\mathrm{D,F,inp}} I^2_{\mathrm{D,F/R,inp,rms}}\right) + \\ & 6\left(U_{\mathrm{S,F,out}} I_{\mathrm{S,out,avg}} + r_{\mathrm{S,F,out}} I^2_{\mathrm{S,out,rms}} + \right. \\ & U_{\mathrm{D,F,out}} I_{\mathrm{D,out,avg}} + r_{\mathrm{D,F,out}} I^2_{\mathrm{D,out,rms}} + \\ & \left. P_{\mathrm{sw,S,out}} + P_{\mathrm{sw,D,out}}\right)\Big|_{\mathrm{OP1}\,\vee\,\mathrm{OP5}} \end{aligned} \quad (4.100)$$

4.5.4 Motor Operation at Stand-Still (OP3)

At this operating point the maximum semiconductor stresses occur in the output stage of the IMC and are calculated for the transistor S_{pA} and the diode D_{nA} of the bridge-leg of the output phase A. Due to the voltage-source-type output stage the maximum losses in S_{pA} and D_{nA} are generated at $\varphi_2 = 0$ or $\varphi_2 = \pi/6$ similar to the VSBBC.

Output Stage Transistor S_{pA} and Diode D_{nA} at $\varphi_2 = 0$ ($\Phi_1 = 0$ and $\Phi_2 = 0$)

$$I_{\mathrm{SpA,avg}} = \hat{I}_2 \tag{4.101}$$

$$I^2_{\mathrm{SpA,rms}} = \hat{I}_2^2 \tag{4.102}$$

$$I_{\mathrm{DnA,avg}} = 0 \tag{4.103}$$

$$I^2_{\mathrm{DnA,rms}} = 0 \tag{4.104}$$

$$P_{\mathrm{sw,SpA}} = 0 \tag{4.105}$$

$$P_{\mathrm{sw,DnA}} = 0 \tag{4.106}$$

Output Stage Transistor S_{pA} and Diode D_{nA} at $\varphi_2 = \pi/6$ ($\Phi_1 = 0$ and $\Phi_2 = 0$)

$$I_{\mathrm{SpA,avg}} = \frac{3\sqrt{3}M_{12}}{2\pi} \cdot \hat{I}_2 \tag{4.107}$$

$$I^2_{\mathrm{SpA,rms}} = \frac{9M_{12}}{4\pi} \cdot \hat{I}_2^2 \tag{4.108}$$

$$I_{\mathrm{DnA,avg}} = \frac{\sqrt{3}\,(\pi - 3M_{12})}{2\pi} \cdot \hat{I}_2 \tag{4.109}$$

$$I^2_{\mathrm{DnA,rms}} = \frac{3\,(\pi - 3M_{12})}{4\pi} \cdot \hat{I}_2^2 \tag{4.110}$$

$$P_{\mathrm{sw,SpA}} = \frac{3}{\pi}\frac{f_{\mathrm{sw}}}{2}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} w_{\mathrm{S,tot}}\left(\hat{I}_2\cos\left(\frac{\pi}{6}\right), u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + w_{\mathrm{S,tot}}\left(\hat{I}_2\cos\left(\frac{\pi}{6}\right), u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_1 \tag{4.111}$$

$$P_{\mathrm{sw,DnA}} = \frac{3}{\pi}\frac{f_{\mathrm{sw}}}{2}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} w_{\mathrm{D,tot}}\left(\hat{I}_2\cos\left(\frac{\pi}{6}\right), u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + w_{\mathrm{D,tot}}\left(\hat{I}_2\cos\left(\frac{\pi}{6}\right), u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_1 \tag{4.112}$$

4.6 Loss Calculation of the CMC

Due to its fully symmetrical power circuit, all transistors and all diodes of the CMC are evenly loaded if the input frequency f_1 is different from the output frequency f_2 and both are different from zero. Besides nominal motor operation (OP1), nominal generator operation (OP5), and motor operation at stand-still (OP3), also motor operation (OP2) and generator operation (OP4) at equal input and output frequency need to be considered as further relevant operating points (cf. Sec. 4.1). The equations (4.76) to (4.79) from the IMC are utilized for the loss calculation.

4.6.1 Nominal Motor Operation (OP1)

Average and RMS Currents ($\Phi_1 = 0$)

$$I_{\mathrm{S,avg}} = I_{\mathrm{D,avg}} = \frac{1}{3} \cdot \frac{1}{2\pi} \int_0^{2\pi} i_{\mathrm{A}}\big|_{i_{\mathrm{A}}>0}\, d\varphi_2$$
$$= \frac{1}{6\pi} \int_{-\frac{\pi}{2}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} i_{\mathrm{A}}\, d\varphi_2 = \frac{1}{3\pi} \cdot \hat{I}_2 \tag{4.113}$$

$$I^2_{\mathrm{S,rms}} = I^2_{\mathrm{D,rms}} = \frac{1}{3} \cdot \frac{1}{2\pi} \int_0^{2\pi} i^2_{\mathrm{A}}\big|_{i_{\mathrm{A}}>0}\, d\varphi_2$$
$$= \frac{1}{6\pi} \int_{-\frac{\pi}{2}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} i^2_{\mathrm{A}}\, d\varphi_2 = \frac{1}{12} \cdot \hat{I}^2_2 \tag{4.114}$$

Interestingly, the average and rms currents do neither depend on the selected modulation scheme nor on phase displacement angles!

Switching Losses ($\Phi_1 = 0$ and $0 \leq \Phi_2 \leq \pi/6$)

The average switching losses can be determined by averaging over one input and output period as the time constant of the thermal impedance between junction and sink $\tau_{\mathrm{th,JS}}$[1] is in general larger than 100 ms for standard 1200 V IGBT power modules with a current rating greater or equal than 10 A (cf. e.g. FP10R12W1T4, Infineon, 1200 V/ 10 A PIM power module with a diode rectifier and a VSI). $\tau_{\mathrm{th,JS}}$ increases with increasing current rating (chip size) of the power module.

[1] Time to reach 90% of the stationary value of the thermal impedance $Z_{\mathrm{th,JS}}$.

$$
\begin{aligned}
P_{\mathrm{sw,S}} = \frac{1}{4\pi^2}\frac{f_{\mathrm{sw}}}{2}\Bigg[& \int_{-\frac{\pi}{2}}^{-\frac{\pi}{6}} \int_{-\frac{\pi}{2}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_2 d\varphi_1 + \\
& \int_{-\frac{\pi}{6}}^{0} \Bigg(\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{3}} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + \\
& \qquad w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 + \\
& \qquad \int_{\frac{\pi}{3}}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + \\
& \qquad\qquad w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 \Bigg) d\varphi_1 + \\
& \int_{0}^{\frac{\pi}{6}} \Bigg(\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{3}} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + \\
& \qquad w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 + \\
& \qquad \int_{\frac{\pi}{3}}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + \\
& \qquad\qquad w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 \Bigg) d\varphi_1 \\
& \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} \int_{-\frac{\pi}{2}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 d\varphi_1 \Bigg]
\end{aligned}
\tag{4.115}
$$

$$
\begin{aligned}
P_{\mathrm{sw,D}} = \frac{1}{4\pi^2}\frac{f_{\mathrm{sw}}}{2}\Bigg[& \int_{-\frac{\pi}{2}}^{-\frac{\pi}{6}} \Bigg(\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{3}} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_2 + \\
& \qquad \int_{\frac{\pi}{3}}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_2 \Bigg) d\varphi_1 + \\
& \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} \Bigg(\int_{-\frac{\pi}{2}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_2 + \\
& \qquad w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 \Bigg) d\varphi_1 + \\
& \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} \Bigg(\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{3}} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 + \\
& \qquad \int_{\frac{\pi}{3}}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 \Bigg) d\varphi_1 \Bigg]
\end{aligned}
\tag{4.116}
$$

4.6.2 Generator Operation (OP5)

The resulting average and rms currents and the switching losses at OP5 are identical to those at OP1 owing to the symmetry of the power circuit of the CMC.

Average and RMS Currents ($\boldsymbol{\Phi_1 = \pi}$)

$$I_{\mathrm{S,avg}} = I_{\mathrm{D,avg}} = \frac{1}{3\pi} \cdot \hat{I}_2 \tag{4.117}$$

$$I^2_{\mathrm{S,rms}} = I^2_{\mathrm{D,rms}} = \frac{1}{12} \cdot \hat{I}^2_2 \tag{4.118}$$

Switching Losses ($\boldsymbol{\Phi_1 = \pi}$ and $\boldsymbol{\pi \leq \Phi_2 \leq 7\pi/6}$)

$$\begin{aligned}
P_{\mathrm{sw,S}} = \frac{1}{4\pi^2}\frac{f_{\mathrm{sw}}}{2}\Bigg[& \int_{-\frac{\pi}{2}}^{-\frac{\pi}{6}} \int_{-\frac{\pi}{2}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_2 d\varphi_1 + \\
& \int_{-\frac{\pi}{6}}^{0} \Bigg(\int_{-\frac{\pi}{2}+\Phi_2}^{\frac{2\pi}{3}} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + \\
& \qquad w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 + \\
& \qquad \int_{-\frac{2\pi}{3}}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + \\
& \qquad w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 \Bigg) d\varphi_1 + \\
& \int_{0}^{\frac{\pi}{6}} \Bigg(\int_{-\frac{\pi}{2}+\Phi_2}^{\frac{2\pi}{3}} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + \\
& \qquad w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 + \\
& \qquad \int_{-\frac{2\pi}{3}}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) + \\
& \qquad w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 \Bigg) d\varphi_1 \\
& \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} \int_{-\frac{\pi}{2}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 d\varphi_1 \Bigg]
\end{aligned} \tag{4.119}$$

$$P_{\mathrm{sw,D}} = \frac{1}{4\pi^2}\frac{f_{\mathrm{sw}}}{2}\Bigg[\int_{-\frac{\pi}{2}}^{-\frac{\pi}{6}}\Bigg(\int_{-\frac{\pi}{2}+\Phi_2}^{\frac{2\pi}{3}} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_2 + \int_{-\frac{2\pi}{3}}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_2\Bigg) d\varphi_1 + \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}}\Bigg(\int_{-\frac{\pi}{2}+\Phi_2}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_2 + \int_{-\frac{2\pi}{3}}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2\Bigg) d\varphi_1 + \int_{\frac{\pi}{6}}^{\frac{\pi}{2}}\Bigg(\int_{-\frac{\pi}{2}+\Phi_2}^{\frac{2\pi}{3}} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2 + \int_{-\frac{2\pi}{3}}^{\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(i_{\mathrm{A}}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_2\Bigg) d\varphi_1\Bigg] \quad (4.120)$$

4.6.3 Total Semiconductor Losses (OP1 or OP5)

The total average semiconductor losses at OP1 or OP5 can again be determined by summing all loss components of the transistors and diodes.

$$P_{\mathrm{semi,tot}} = 18\left(U_{\mathrm{S,F}} I_{\mathrm{S,avg}} + r_{\mathrm{S,F}} I_{\mathrm{S,rms}}^2 + U_{\mathrm{D,F}} I_{\mathrm{D,avg}} + r_{\mathrm{D,F}} I_{\mathrm{D,rms}}^2 + P_{\mathrm{sw,S}} + P_{\mathrm{sw,D}}\right)\Big|_{\mathrm{OP1}\,\vee\,\mathrm{OP5}} \quad (4.121)$$

4.6.4 Motor or Generator Operation at Equal Input and Output Frequency (OP2 or OP4)

If at the output of the CMC a voltage with exactly the same frequency as the input frequency is generated ($f_1 = f_2$), then always the same semiconductors are loaded, and thus the output current needs to be reduced compared to the nominal value to limit the junction temperature. Consequently, operating the CMC at equal input and output frequencies can be considered as a sort of an "electrical stand-still" in terms of the loading of the semiconductors.

The absolute value of the input frequency and output frequency is identical at the operating points OP2 and OP4. For motor operation at OP2, the input phase angle φ_1 and output phase angle φ_2 change in the same direction, whereas for generator operation at OP4 they change in

the opposite direction. Thus, the output phase angle can be expressed as a function of the input phase angle with a constant angular shift Φ_{12}.

$$\text{OP2:} \quad \varphi_2 = \varphi_1 + \Phi_{12} \tag{4.122}$$

$$\text{OP4:} \quad \varphi_2 = -\varphi_1 - \Phi_{12} \tag{4.123}$$

The semiconductor stresses are investigated by calculating for OP2 the losses of the transistor S_{aA} and the diode D_{aA} and for OP4 the losses of the transistor S_{Aa} and the diode D_{Aa}. Under these assumptions, the maximum semiconductor losses in the corresponding power devices occur for $\Phi_{12} = 0$. The current in the output phase A may then be written as

$$\text{OP2:} \quad i_{\mathrm{A},\varphi_1^+} = \hat{I}_2 \cos\left(\varphi_1 - \Phi_2\right) \tag{4.124}$$

$$\text{OP4:} \quad i_{\mathrm{A},\varphi_1^-} = \hat{I}_2 \cos\left(-\varphi_1 + \Phi_2\right). \tag{4.125}$$

Transistor S_{aA} and Diode D_{aA} at $\varphi_2 = \varphi_1$ ($\Phi_1 = 0$ and $0 \leq \Phi_2 \leq \pi/6$)

At OP2, the average and rms transistor and diode currents become maximum for $\Phi_2 = 0$, and thus the total semiconductor losses of S_{aA} and D_{aA} are determined for this phase displacement angle. As can be seen in (4.129), for $\Phi_2 = 0$, the switching losses of D_{aA} equal to zero.

$$\begin{aligned} I_{\mathrm{SaA,avg}}\big|_{\Phi_2=0} &= I_{\mathrm{DaA,avg}}\big|_{\Phi_2=0} \\ &= \frac{3+\sqrt{3}M_{12}}{6\pi} \cdot \hat{I}_2 \end{aligned} \tag{4.126}$$

$$\begin{aligned} I^2_{\mathrm{SaA,rms}}\big|_{\Phi_2=0} &= I^2_{\mathrm{DaA,rms}}\big|_{\Phi_2=0} \\ &= \frac{8\left(3\sqrt{3}+2\pi\right) - 3\left(9-4\sqrt{3}\pi\right)M_{12}}{192\pi} \cdot \hat{I}_2^2 \end{aligned} \tag{4.127}$$

$$\begin{aligned} P_{\mathrm{sw,SaA}} = \frac{1}{2\pi}\frac{f_{\mathrm{sw}}}{2}\Bigg[&\int_{-\frac{\pi}{2}+\Phi_2}^{-\frac{\pi}{6}} w_{\mathrm{S,tot}}\left(i_{\mathrm{A},\varphi_1^+}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_1 + \\ &\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} w_{\mathrm{S,tot}}\left(i_{\mathrm{A},\varphi_1^+}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_1 \Bigg] \end{aligned} \tag{4.128}$$

$$P_{\mathrm{sw,DaA}} = \frac{1}{2\pi}\frac{f_{\mathrm{sw}}}{2}\int_{-\frac{\pi}{2}}^{-\frac{\pi}{2}+\Phi_2} w_{\mathrm{D,tot}}\left(-i_{\mathrm{A},\varphi_1^+}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_1 \tag{4.129}$$

Transistor S_{Aa} and Diode D_{Aa} at $\varphi_2 = -\varphi_1$ ($\Phi_1 = \pi$ and $\pi \leq \Phi_2 \leq 7\pi/6$)

The maximum average and rms transistor and diode currents at OP4 are found for $\Phi_2 = \pi$, and thus the total semiconductor losses of S_{Aa} and D_{Aa} are calculated for this phase displacement. Opposed to OP2, at OP4 for $\Phi_2 = \pi$, the switching losses of S_{Aa} equal to zero.

$$\begin{aligned} I_{\mathrm{SAa,avg}}\big|_{\Phi_2=\pi} &= I_{\mathrm{DAa,avg}}\big|_{\Phi_2=\pi} \\ &= \frac{3+\sqrt{3}M_{12}}{6\pi} \cdot \hat{I}_2 \end{aligned} \tag{4.130}$$

$$\begin{aligned} I^2_{\mathrm{SAa,rms}}\big|_{\Phi_2=\pi} &= I^2_{\mathrm{DAa,rms}}\big|_{\Phi_2=\pi} \\ &= \frac{8\left(3\sqrt{3}+2\pi\right) - 3\left(9-4\sqrt{3}\pi\right)M_{12}}{192\pi} \cdot \hat{I}_2^2 \end{aligned} \tag{4.131}$$

$$P_{\mathrm{sw,SAa}} = \frac{1}{2\pi}\frac{f_{\mathrm{sw}}}{2}\int_{-\frac{\pi}{2}}^{-\frac{3\pi}{2}+\Phi_2} w_{\mathrm{S,tot}}\left(i_{\mathrm{A},\varphi_1^-}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_1 \tag{4.132}$$

$$\begin{aligned} P_{\mathrm{sw,DAa}} = \frac{1}{2\pi}\frac{f_{\mathrm{sw}}}{2}\Bigg[&\int_{-\frac{3\pi}{2}+\Phi_2}^{-\frac{\pi}{6}} w_{\mathrm{D,tot}}\left(-i_{\mathrm{A},\varphi_1^-}, u_{\mathrm{ab}}, T_{\mathrm{J}}\right) d\varphi_1 + \\ &\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} w_{\mathrm{D,tot}}\left(-i_{\mathrm{A},\varphi_1^-}, u_{\mathrm{ac}}, T_{\mathrm{J}}\right) d\varphi_1 \Bigg] \end{aligned} \tag{4.133}$$

By comparing the results, it can be seen that at OP2 for $\Phi_2 = 0$, no switching losses are generated in the diodes. Correspondingly, at OP4 for $\Phi_2 = \pi$, no switching losses are generated in the transistors.

4.6.5 Motor Operation at Stand-Still (OP3)

At this operating point the worst case semiconductor stresses are again investigated for the transistor S_{aA} and the diode D_{aA}. The maximum losses occur at $\varphi_2 = 0$.

Transistor $S_{\mathbf{aA}}$ and Diode $D_{\mathbf{aA}}$ at $\varphi_{\mathbf{2}} = \mathbf{0}$ ($\Phi_{\mathbf{1}} = \mathbf{0}$ and $\Phi_{\mathbf{2}} = \mathbf{0}$)

$$I_{\mathrm{SaA,avg}} = I_{\mathrm{DaA,avg}} = \frac{1}{3} \cdot \hat{I}_2 \tag{4.134}$$

$$I^2_{\mathrm{SaA,rms}} = I^2_{\mathrm{DaA,rms}} = \frac{1}{3} \cdot \hat{I}^2_2 \tag{4.135}$$

$$P_{\mathrm{sw,SaA}} = \frac{1}{2\pi} \frac{f_{\mathrm{sw}}}{2} \left[\int_{-\frac{\pi}{2}}^{-\frac{\pi}{6}} w_{\mathrm{S,tot}} \left(\hat{I}_2, u_{\mathrm{ab}}, T_{\mathrm{J}} \right) d\varphi_1 + \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} w_{\mathrm{S,tot}} \left(\hat{I}_2, u_{\mathrm{ac}}, T_{\mathrm{J}} \right) d\varphi_1 \right] \tag{4.136}$$

$$P_{\mathrm{sw,DaA}} = \frac{1}{2\pi} \frac{f_{\mathrm{sw}}}{2} \left[\int_{-\frac{\pi}{6}}^{-\frac{\pi}{6}} w_{\mathrm{D,tot}} \left(\hat{I}_2, u_{\mathrm{ab}}, T_{\mathrm{J}} \right) + w_{\mathrm{D,tot}} \left(\hat{I}_2, u_{\mathrm{ac}}, T_{\mathrm{J}} \right) d\varphi_1 \right] \tag{4.137}$$

4.7 Summary

Analytical equations to calculate the average and rms currents of all power semiconductors of the VSBBC, CSBBC, IMC, and CMC and the average conduction and switching losses are derived for the selected SV modulation schemes. Opposed to previous work, the resultant equations are presented for various characteristic converter operating points, that are: nominal motor operation (OP1), nominal generator operation (OP5), motor operation at zero output frequency (OP3), and for the CMC also motor and generator operation at equal input and output frequency (OP2, OP4).

Due to the selected modulation schemes with loss-optimal clamping, the switching losses of the VSBBC, the CSBBC, and the IMC at OP1 and OP5 do not depend on the phase displacement angles Φ_1 and Φ_2 in the considered ranges of $0 \leq \Phi_2 \leq \pi/6$ and $\pi \leq \Phi_2 \leq 7\pi/6$ for $\Phi_1 = 0$ and $\Phi_1 = \pi$. Contrary to the two-stage topologies, the conduction losses of the CMC remain constant at OP1 and OP5, independent of the phase displacement angles.

The semiconductor loss generation and the worst case conditions of the IMC at OP3 are identical to those of the VSBBC as a result of the

voltage-source-type output stage of the IMC and the similarity of the modulation for their output stage. The CSBBC is the only topology that features virtually no switching losses in the output stage at OP3, as the commutation voltage is close to zero due to the low modulation index of the output stage at this operating point. At OP3, the loss equations of the CMC have a similar structure as those of the input stage of the CSBBC at OP1. This can be verified by considering the impressed output current of the CMC at electrical stand-still as the impressed dc-link current of the CSBBC and comparing the power semiconductors in the current path of both converter topologies.

The worst case semiconductor stresses of the CMC at OP2 or OP4 are less severe compared with the worst case semiconductors stresses in the output stage of the VSBBC or IMC at OP3, as the transistor and diode losses of the CMC are still modulated with the output frequency $f_2 = \pm f_1$.

Chapter 5

Semiconductor Area Based Comparison

The power semiconductors and their packages are core components of any power electronic converter. They do not only determine the key performance figures such as efficiency, power density, switching frequency range, and partly EMI emissions, but also contribute to the overall converter costs by approximately 25% [284]. For any comprehensive converter topology comparison, a distinct figure-of-merit is essential to assess the semiconductor-expenditure-to-converter-performance relationship.

In this chapter, a novel semiconductor chip area based method for comparison of power electronic converter systems is presented. It allows the determination of the total semiconductor chip area and the optimal partitioning of the transistor and diode chip areas of a converter topology depending on the operating point and predefined boundary conditions. With this data, the resulting semiconductor losses and therewith also the volume and the weight of the semiconductor module and the cooling system can be calculated. Additionally, the knowledge of the required transistor chip areas enables an estimation of the power consumption, the volume, and the weight of the gate drivers.

5.1 Semiconductor Area Based Converter Comparison

5.1.1 Basic Concept

Semiconductor related comparisons of power converters are frequently applied. A commonly used method is to compare different converter topologies by determining the losses using the same semiconductors for all topologies, as shown in [210, 215, 285]. In this approach, the semiconductors have to be selected such that they fulfill the ratings of all compared converter topologies and thus are not matched to the individual topologies. Another possibility, presented in [208], is to perform the comparison based on the thermal stress of the power semiconductors. In this method the rating of the compared converter topologies is adapted depending on the operating point in order not to exceed the thermal limits of the semiconductor devices. The general limitation with these methods is that the semiconductor chip area required by the individual converter topologies is not considered and possibly only a simple semiconductor device of the converter under investigation could limit its performance and thus significantly affect the result of the comparison.

The basic concept of the Semiconductor chip Area based Converter Comparison (SAC2) can be best explained with Fig. 5.1, depicting an IGBT with an anti-parallel diode, which is a standard semiconductor configuration in many PWM power electronic converters. Depending on the applied voltage $u_{\mathrm{S/D}}$, the average and the rms values of the current $i_{\mathrm{S/D}}$, the current direction, the switching frequency, and the modulation

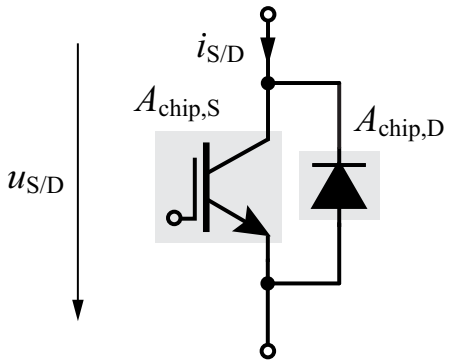


Fig. 5.1: IGBT with anti-parallel diode implemented with two semiconductor chips.

scheme, the IGBT and diode are loaded differently. This consequently leads to unequal semiconductor losses for the IGBT and diode chip. The total power loss is dissipated through the thermal interface, in this case through the base plate of the power module to the heat sink, as shown in Fig. 5.2. The transistor and diode current rating is proportional to the active chip area $A_{\mathrm{chip,act}}$, whereas the resulting thermal impedance between the junction and the heat sink $\underline{Z}_{\mathrm{th,JS}}$ depends on the total chip area $A_{\mathrm{chip}} > A_{\mathrm{chip,act}}$, the semiconductor module assembly, and the cooling system. The electrical equivalent circuit of the thermal impedance corresponds to a RC network with low-pass characteristic and can be written as a complex transfer function $G_{\mathrm{th,JS}}(\omega)$. The resulting time behavior of the junction temperature T_{J} can be calculated based on the heat sink temperature T_{S} and the Fourier transform $P_{\mathrm{chip}}(\omega)$ of the semiconductor chip losses p_{chip}.

$$T_{\mathrm{J}}(t) = T_{\mathrm{S}}(t) + \mathcal{F}^{-1}\left\{G_{\mathrm{th,JS}}(\omega) \cdot P_{\mathrm{chip}}(\omega)\right\} \tag{5.1}$$

Thereby it is assumed that for the time behavior of the semiconductor losses, $P_{\mathrm{chip}}(\omega)$ exists or that it can be represented sufficiently accurately by superposition of a finite number of sinusoidal functions (Fourier series). If only the average stationary junction temperature is of interest, $G_{\mathrm{th,JS}}(\omega)$ in (5.1) can be replaced by the corresponding thermal resistance $R_{\mathrm{th,JS}}$ and $P(\omega)$ by the average semiconductor chip losses P_{chip} leading to

$$T_{\mathrm{J}} = T_{\mathrm{S}} + R_{\mathrm{th,JS}} \cdot P_{\mathrm{chip}} \,. \tag{5.2}$$

The important point is that if the same transistor and diode chip configuration is implemented in different converter topologies and analyzed regarding losses at different operating points, it is most likely that for one topology the transistor chip is over- and the diode chip is underdimensioned, whereas for an another topology the opposite is true. That is exactly where the SAC2 provides benefits. The implemented algorithm allows the determination of the minimum required semiconductor area for the individual transistor and diode chips for a given converter topology, operating point, and semiconductor module assembly such that the maximum average transistor and diode junction temperatures $T_{\mathrm{J,max}}$ and the maximum junction temperature swings $\Delta T_{\mathrm{J,max}}$ are equal or less than a predefined maximum value. This method does not only guarantee optimal chip area partitioning and semiconductor material usage but also provides a common basis for converter topology comparisons: the required total semiconductor chip area. Furthermore,

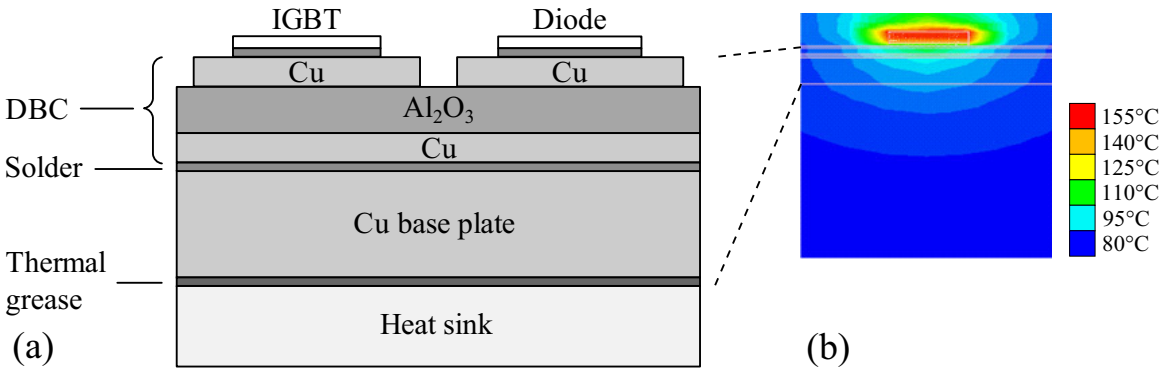


Fig. 5.2: **(a)** Cross-section of the considered semiconductor module assembly. **(b)** Typical thermal simulation result of a single chip for the module assembly on the left, showing the heat spreading.

the chip area data can be directly used to determine the semiconductor costs. Another advantage seen in the SAC2 is that with the average junction temperature, the junction temperature swing, and the associated loss energy also the reliability of the power module may be modeled, which however is not investigated in depth in this thesis.

The SAC2 is obviously also applicable to semiconductor technologies where the transistor and diode are integrated in a single chip, as for instance for Si RC-IGBTs or SiC JFETs. In this case, the loss data of the transistor and diodes is not utilized to find an optimal partitioning of the transistor and diode chip area, but to minimize the total chip area and to identify on whether the investigated device technology leads to a balanced thermal loading of the chip for transistor and diode operation.

5.1.2 Algorithm

The algorithm developed for the SAC2 comprises three sequential steps: the initialization, the calculation, and the post-processing. The corresponding flowchart is depicted in Fig. 5.3.

In the initialization step, the calculation software is parameterized with the characteristic model equations of the selected converter topology, the load, the semiconductor technology, the operating point, etc. The start values for the transistor and diode chip areas are set by default to the minimal possible chip areas. In order to reduce the calculation time, the chip areas are typically initialized with a start value which is determined by the analytical semiconductor model equations

(cf. Chap. 4). The chip area determination is implemented with a conditional loop and is applied separately to all transistor and diode chips of the considered converter. In this loop the chip area is increased by an incremental area ΔA_{chip} as long as the maximum average junction temperature or the maximum junction temperature swing specified are exceeded. In every optimization step, the resulting losses and the thermal impedance are recalculated for the incremented chip area value, considering boundary conditions such as the maximum chip current density. Symmetry relations of the converter topologies are utilized to minimize the calculation effort. When the minimal chip areas are determined, various post-processing calculations can be performed on the captured data such as for example calculating the ratio between the transistor and diode chip areas to estimate the total semiconductor costs.

A point of criticism of the SAC2 may arise from the fact that commercial power semiconductor chips are only available with a limited number of different chip sizes and the result of the chip area optimization would therefore not be applicable to a practical converter system. However, by comparing for instance the available power 1200 V IGBT4 T&FS chip portfolio from Infineon, it is found that 11 different chip sizes between $7\,\mathrm{mm}^2$ and $142\,\mathrm{mm}^2$ are available, thus providing a sufficiently small grading for selecting the chip area. An even better matching of the calculated and implementable chip area can be achieved with SiC power devices, which currently feature a small chip area compared to Si devices and thus need to be paralleled anyway for higher current ratings.

5.2 Semiconductor Models

The prerequisite for a SAC2 are sufficiently accurate semiconductor models. In Chap. 2, the properties and losses of suitable Si and SiC power semiconductors for ac-ac converters are investigated. Due to their performance and the diversity of available devices and power modules, the latest (fourth) generation of 1200 V Trench and Field-Stop Si IGBTs (T&FS IGBT4) and the corresponding 1200 V Emitter Controlled (EmCon4) Si diodes from Infineon are selected as reference silicon technologies for this research work. Both device technologies are rated for a maximum junction temperature of 175°C. The 1200 V normally-on SiC JFETs, manufactured by SiCED, are selected as reference technology for silicon carbide switching devices.

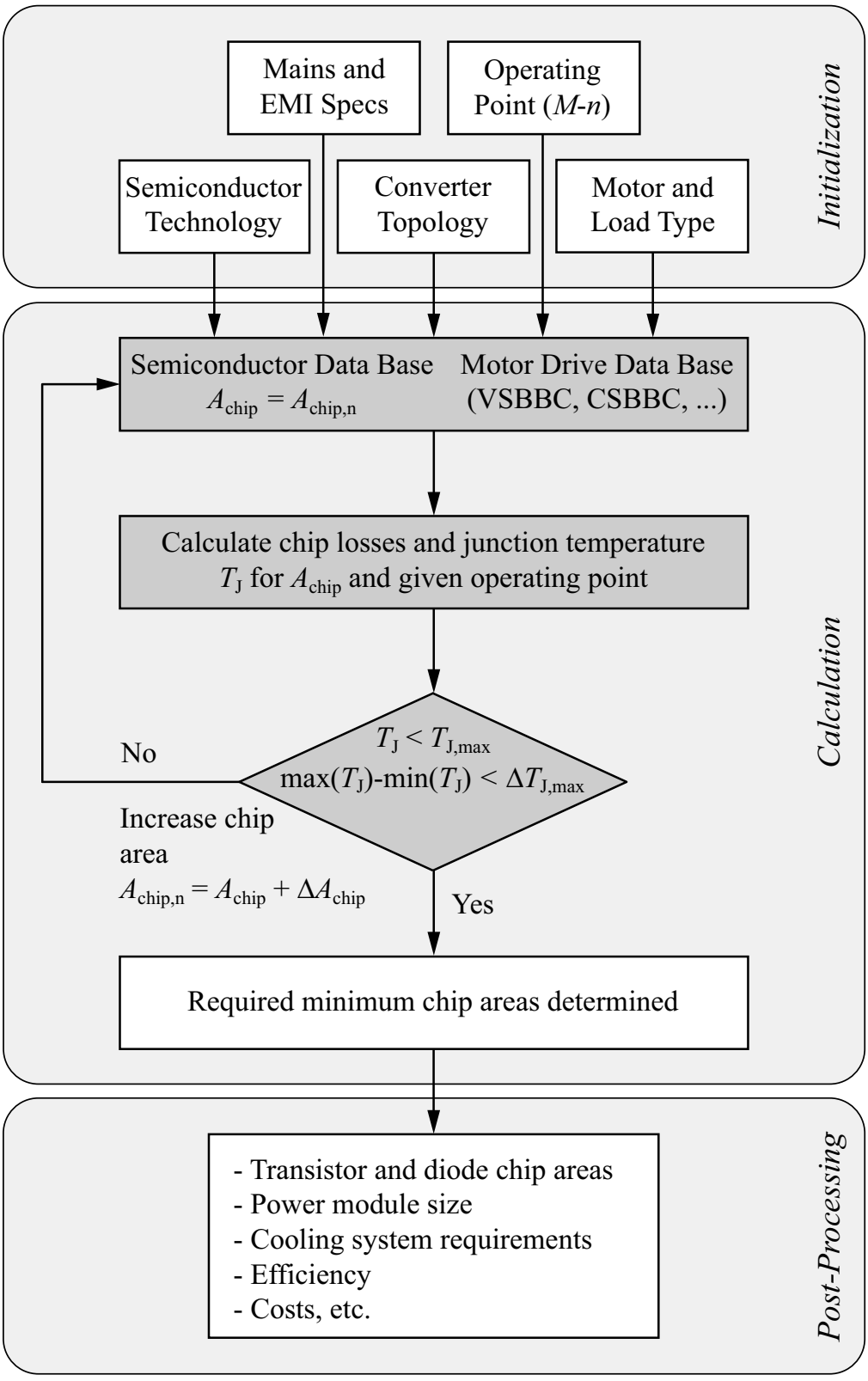


Fig. 5.3: Simplified flowchart of the SAC2.

The required semiconductor loss and chip size data of the T&FS IGBTs and the EmCon diodes is determined based on a statistical analysis of power module data sheets and manufacturer data, whereas for the SiC JFETs the essential data is primarily derived from the measurement results compiled in Sec. 2.4.2. The extracted data is fitted to a set of voltage, current, chip area, and temperature dependent model equations with reference to [286–288] and Sec. 4.2.1.

5.2.1 Basic Relations

The key semiconductor chip quantities required for a SAC2 are the active chip area $A_{\mathrm{chip,act}}$ and the total chip area $A_{\mathrm{chip,tot}}$. The nominal current rating of the chip is proportional to the active chip area, whereas the differential resistance and thermal resistance (impedance) between the semiconductor junction and the case or the heat sink are inversely proportional to the total chip area. This enables to express the transistor and diode loss modeling quantities, defined in (4.1) to (4.5), not only as a function of the device current, the voltage, and the junction temperature but additionally also as a function of the active chip area. The total chip area is utilized to determine the thermal impedance and thus the cooling properties of the semiconductor chip. Hence, the active and total chip areas provides the linkage between the electrical and thermal properties of a semiconductor chip. The ratio between the total and the active chip area of the selected semiconductor technologies is presented in Fig. 5.4.

The relation between the nominal chip current density for a given active chip area at a given junction temperature can be expressed with the nominal transistor or diode chip current density

$$J_{\mathrm{S/D,nom}} = \frac{I_{\mathrm{S/D,avg}}}{A_{\mathrm{chip,act}}} \,. \tag{5.3}$$

The chip current density is mainly determined by the cooling properties of the chip and can be up to $140\,\mathrm{A/cm^2}$ at $T_{\mathrm{J}} = 175°\mathrm{C}$ for the considered Si IGBT4 and packaging technology. The same nominal chip current density is assumed for the SiC JFETs as the JFET devices of the implemented converter prototypes are operated at this chip current density. The admissible repetitive peak current density for a duration of the peak currents of 1 ms is higher by a factor of two for the IGBTs and even higher by a factor of three for the JFETs. The maximum junction temperature of all power semiconductors is set to $T_{\mathrm{J}} = 175°\mathrm{C}$. For

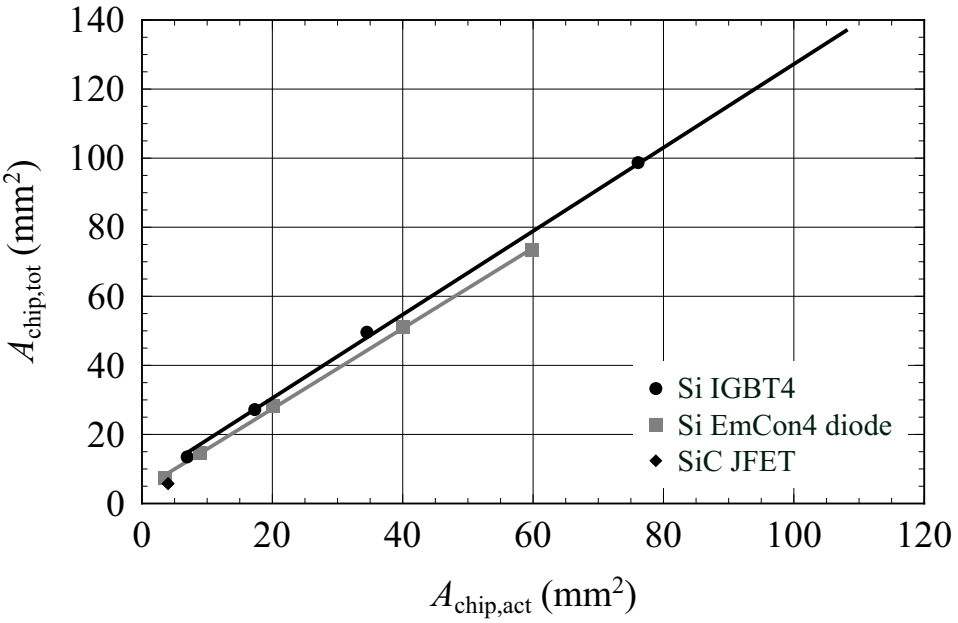


Fig. 5.4: Relation between the active chip area $A_{\text{chip,act}}$ and the total chip area $A_{\text{chip,tot}}$. The ratio of the total to the active chip area reduces for increasing chip areas. However, it does not exactly converge to one as an inactive chip boundary remains for manufacturing purposes.

the IGBT4 and the EmCon4 diode, this limitation is imposed by the Si semiconductor technology, whereas for the SiC JFET it is given by the standard packaging technology utilized for the prototype devices.

For reasons of conciseness, in the following, only the key equations of the semiconductor loss models are presented, which are valid within the ranges of values specified in Tab. 5.1.

Parameter	*Range of Value*
Active chip area	$A_{\text{chip,act}} = [6 \ldots 120]\,\text{mm}^2$
IGBT4 chip current density	$J_{\text{IGBT4,nom}} = [0 \ldots 140]\,\frac{A}{\text{cm}^2}$
EmCon4 chip current density	$J_{\text{EmCon4,nom}} = [0 \ldots 260]\,\frac{A}{\text{cm}^2}$
JFET chip current density	$J_{\text{JFET,nom}} = [0 \ldots 140]\,\frac{A}{\text{cm}^2}$
Junction temperature	$T_{\text{J}} = [25 \ldots 175]\,^\circ\text{C}$

Tab. 5.1: Ranges of values of the key semiconductor chip parameters within the semiconductor loss models are valid.

5.2.2 1200 V T&FS Si IGBT4 and 1200 V EmCon4 Si Diode

Conduction Losses

The IGBT and diode on-state losses are modeled with an active chip area and junction temperature dependent forward voltage drop $U_{\mathrm{S/D,F}}$ and differential resistance $r_{\mathrm{S/D,F}}$ as both the IGBT and the diode are bipolar devices. (The forward voltage drop is represented as a function of the active chip area to account for possible chip area dependent changes in the doping profile and therewith in the conduction behavior.) The corresponding mathematical relations are provided in (5.4) and (5.5) for the IGBT and in (5.6) and (5.7) for the diode. The numerical values $k_{i,j}$ of the loss parameters immediately allow the identification of the sensitivities of the individual input quantities.

$$U_{\mathrm{S,F}}(A_{\mathrm{chip,act}}, T_{\mathrm{J}}) = k_{1,\mathrm{U_S}} A_{\mathrm{chip,act}} + k_{2,\mathrm{U_S}} T_{\mathrm{J}} + k_{3,\mathrm{U_S}} \tag{5.4}$$

$$k_{1,\mathrm{U_S}} = -2.353 \cdot 10^{-4} \tfrac{\mathrm{V}}{\mathrm{mm^2}} \quad k_{2,\mathrm{U_S}} = -1.348 \cdot 10^{-3} \tfrac{\mathrm{V}}{\mathrm{°C}}$$

$$k_{3,\mathrm{U_S}} = 9.525 \cdot 10^{-1}\,\mathrm{V}$$

$$r_{\mathrm{S,F}}(A_{\mathrm{chip,act}}, T_{\mathrm{J}}) = k_{1,\mathrm{r_S}} \left(\frac{1}{\mathrm{mm^2}} A_{\mathrm{chip,act}} \right)^{k_{2,\mathrm{r_S}} \left(T_{\mathrm{J}} + k_{3,\mathrm{r_S}} \right)} \tag{5.5}$$

$$k_{1,\mathrm{r_S}} = 2.990 \cdot 10^{-3}\,\Omega \quad k_{2,\mathrm{r_S}} = -9.896 \cdot 10^{-1} \tfrac{1}{\mathrm{°C}}$$

$$k_{3,\mathrm{r_S}} = 185.4\,\mathrm{°C}$$

$$U_{\mathrm{D,F}}(A_{\mathrm{chip,act}}, T_{\mathrm{J}}) = k_{1,\mathrm{U_D}} A_{\mathrm{chip,act}} + k_{2,\mathrm{U_D}} T_{\mathrm{J}} + k_{3,\mathrm{U_D}} \tag{5.6}$$

$$k_{1,\mathrm{U_D}} = 1.354 \cdot 10^{-4} \tfrac{\mathrm{V}}{\mathrm{mm^2}} \quad k_{2,\mathrm{U_D}} = -1.928 \cdot 10^{-3} \tfrac{\mathrm{V}}{\mathrm{°C}}$$

$$k_{3,\mathrm{U_D}} = 1.010\,\mathrm{V}$$

$$r_{\mathrm{D,F}}(A_{\mathrm{chip,act}}, T_{\mathrm{J}}) = k_{1,\mathrm{r_D}} \left(\frac{1}{\mathrm{mm^2}} A_{\mathrm{chip,act}} \right)^{k_{2,\mathrm{r_D}} \left(T_{\mathrm{J}} + k_{3,\mathrm{r_D}} \right)} \tag{5.7}$$

$$k_{1,\mathrm{r_D}} = 6.551 \cdot 10^{-4}\,\Omega \quad k_{2,\mathrm{r_D}} = -9.971 \cdot 10^{-1} \tfrac{1}{\mathrm{°C}}$$

$$k_{3,\mathrm{r_D}} = 404.8\,\mathrm{°C}$$

Switching Losses

The switching loss energies are modeled separately for the IGBT and the diode. Thereby, it is important to extract the switching loss energies from the manufacturer data at consistent switching conditions and realistic switching speeds for all considered chip areas. For that purpose, the chip area specific current rise-time during turn-on and the voltage rise-time during turn-off are considered for verification and always the lowest practically achievable switching energies specified by the manufacturer are adopted for the models. This leads to an area specific current rise-time during turn-on of the IGBT in the range of $70\,\mathrm{A}/(\mathrm{mm}^2\mu\mathrm{s})$ for the smallest considered chip with an active chip area of $7\,\mathrm{mm}^2$ to $40\,\mathrm{A}/(\mathrm{mm}^2\mu\mathrm{s})$ for the largest chip with an active chip area of $113\,\mathrm{mm}^2$. The minimum voltage rise-time during turn-off equals to $3.5\,\mathrm{kV}/\mu\mathrm{s}$.

(5.8) represents the sum of the IGBT turn-on and turn-off loss energies $w_{\mathrm{S,tot}}$ of an entire switching cycle as a function of the active chip area, the junction temperature, the switched forward current $i_{\mathrm{S,F}}$, and the switched forward voltage $u_{\mathrm{S,F}}$. The additional turn-on losses of the IGBT, resulting from the reverse recovery charge of a freewheeling diode with a similar current rating as the IGBT, are included in the loss parameters. This enables to use this switching loss equation to all considered ac-ac converter topologies, as transistor turn-on losses are always generated when the current is commutated from a diode to a transistor.

$$\begin{aligned} w_{\mathrm{S,tot}}(A_{\mathrm{chip,act}}, i_{\mathrm{S,F}}, u_{\mathrm{S,F}}, T_{\mathrm{J}}) = \\ \left(k_{1,\mathrm{wS}} A_{\mathrm{chip,act}} + k_{2,\mathrm{wS}} A_{\mathrm{chip,act}}^2 + k_{3,\mathrm{wS}} A_{\mathrm{chip,act}} i_{\mathrm{S,F}} + \right. \\ \left. k_{4,\mathrm{wS}} i_{\mathrm{S,F}}^2 + k_{5,\mathrm{wS}} i_{\mathrm{S,F}}\right) \left(T_{\mathrm{J}} + k_{6,\mathrm{wS}}\right) \left(k_{7,\mathrm{wS}} u_{\mathrm{S,F}} + k_{8,\mathrm{wS}}\right) \end{aligned} \tag{5.8}$$

$$\begin{aligned} k_{1,\mathrm{wS}} &= 9.741 \cdot 10^{-5} \tfrac{1}{\mathrm{mm^2}} & k_{2,\mathrm{wS}} &= -1.244 \cdot 10^{-8} \tfrac{1}{\mathrm{mm^4}} \\ k_{3,\mathrm{wS}} &= -1.937 \cdot 10^{-6} \tfrac{1}{\mathrm{A\,mm^2}} & k_{4,\mathrm{wS}} &= 1.203 \cdot 10^{-6} \tfrac{1}{\mathrm{A^2}} \\ k_{5,\mathrm{wS}} &= 6.939 \cdot 10^{-4} \tfrac{1}{\mathrm{A}} & k_{6,\mathrm{wS}} &= 120.5\,^{\circ}\mathrm{C} \\ k_{7,\mathrm{wS}} &= 1.998 \cdot 10^{-3} \tfrac{\mathrm{mJ}}{^{\circ}\mathrm{C\,V}} & k_{8,\mathrm{wS}} &= -1.989 \cdot 10^{-1} \tfrac{\mathrm{mJ}}{^{\circ}\mathrm{C}} \end{aligned}$$

Accordingly, in (5.9) the turn-off (reverse recovery) energy of the diode $w_{\mathrm{D,tot}}$ is approximated as a function of the active chip area, the junction temperature, the diode forward current $i_{\mathrm{D,F}}$ prior to turn-off, and the reverse (blocking) voltage $u_{\mathrm{D,R}}$ after turn-off.

$$w_{\mathrm{D,tot}}(A_{\mathrm{chip,act}}, i_{\mathrm{D,F}}, u_{\mathrm{D,R}}, T_{\mathrm{J}}) = \tag{5.9}$$
$$\left(k_{1,\mathrm{w_D}} A_{\mathrm{chip,act}} + k_{2,\mathrm{w_D}} A_{\mathrm{chip,act}}^2 + k_{3,\mathrm{w_D}} A_{\mathrm{chip,act}} i_{\mathrm{D,F}} + k_{4,\mathrm{w_D}} i_{\mathrm{D,F}}^2 + k_{5,\mathrm{w_D}} i_{\mathrm{D,F}}\right)\left(T_{\mathrm{J}} + k_{6,\mathrm{w_D}}\right) k_{7,\mathrm{w_D}} u_{\mathrm{D,R}}$$

$$k_{1,\mathrm{w_D}} = 1.996 \cdot 10^{-4} \tfrac{1}{\mathrm{mm^2}} \qquad k_{2,\mathrm{w_D}} = -6.670 \cdot 10^{-7} \tfrac{1}{\mathrm{mm^4}}$$
$$k_{3,\mathrm{w_D}} = 3.549 \cdot 10^{-6} \tfrac{1}{\mathrm{A\,mm^2}} \qquad k_{4,\mathrm{w_D}} = -8.617 \cdot 10^{-7} \tfrac{1}{\mathrm{A^2}}$$
$$k_{5,\mathrm{w_D}} = 1.902 \cdot 10^{-4} \tfrac{1}{\mathrm{A}} \qquad k_{6,\mathrm{w_D}} = 98.73\,^{\circ}\mathrm{C}$$
$$k_{7,\mathrm{w_D}} = 1.667 \cdot 10^{-3} \tfrac{\mathrm{mJ}}{^{\circ}\mathrm{C\,V}}$$

5.2.3 1200 V Normally-on SiC JFET

Compared with the IGBT, the normally-on SiC JFET is a unipolar device and features an intrinsic anti-parallel diode. This leads to three possible conduction states. As only one chip size could be investigated for the SiC JFET, the dependency of the loss models on the active chip area is determined by linearly scaling the determined loss quantities of the SiC JFET prototype devices with respect to their active chip areas.

Conduction Losses

JFET Forward Conduction

In this conduction state, only the JFET channel of the chip is utilized and the current flows from the drain to the source terminal. The forward resistance $r_{\mathrm{S,F}}$ (drain-source on-resistance), given in (5.10), is modeled depending on the active chip area, the junction temperature, and the transistor forward current $i_{\mathrm{S,F}}$.

$$r_{\mathrm{S,F}}(A_{\mathrm{chip,act}}, i_{\mathrm{S,F}}, T_{\mathrm{J}}) = \frac{k_{1,\mathrm{r_S}} + k_{2,\mathrm{r_S}} i_{\mathrm{S,F}}}{A_{\mathrm{chip,act}}} \left(\frac{T_{\mathrm{J}} + k_{3,\mathrm{r_S}}}{k_{4,\mathrm{r_S}}}\right)^{k_{5,\mathrm{r_S}}} \tag{5.10}$$

$$k_{1,\mathrm{r_S}} = 1.088 \cdot 10^{-2}\,\Omega\,\mathrm{mm^2} \qquad k_{2,\mathrm{r_S}} = 1.587 \cdot 10^{-2} \tfrac{\Omega\,\mathrm{mm^2}}{\mathrm{A}}$$
$$k_{3,\mathrm{r_S}} = 273.15^{\circ}\mathrm{C} \qquad k_{4,\mathrm{r_S}} = 298.15^{\circ}\mathrm{C}$$
$$k_{5,\mathrm{r_S}} = 2.0$$

Diode Forward Conduction

When the JFET channel is in the off state and the current flow direction is from the source to the drain terminal, the intrinsic diode is conducting. The diode characteristic is represented by an equivalent forward voltage drop $U_{\mathrm{D,F}}$ and a differential forward resistance $r_{\mathrm{D,F}}$ shown in (5.11) and (5.12). It should be highlighted again that the intrinsic body diode of the JFET is not a SiC Schottky barrier diode but a conventional SiC PiN diode.

$$U_{\mathrm{D,F}}(T_{\mathrm{J}}) = k_{1,\mathrm{U_D}} T_{\mathrm{J}}^2 + k_{2,\mathrm{U_D}} T_{\mathrm{J}} + k_{3,\mathrm{U_D}} \tag{5.11}$$

$$k_{1,\mathrm{U_D}} = -2.047 \cdot 10^{-6} \tfrac{\mathrm{V}}{^\circ\mathrm{C}^2} \quad k_{2,\mathrm{U_D}} = -8.373 \cdot 10^{-4} \tfrac{\mathrm{V}}{^\circ\mathrm{C}}$$
$$k_{3,\mathrm{U_D}} = 2.935\,\mathrm{V}$$

$$r_{\mathrm{D,F}}(A_{\mathrm{chip,act}}, T_{\mathrm{J}}) = \frac{k_{1,\mathrm{r_D}} T_{\mathrm{J}} + k_{2,\mathrm{r_D}}}{A_{\mathrm{chip,act}}} \tag{5.12}$$

$$k_{1,\mathrm{r_D}} = 1.893 \cdot 10^{-3} \tfrac{\Omega\,\mathrm{mm}^2}{^\circ\mathrm{C}} \quad k_{2,\mathrm{r_D}} = 1.623\,\Omega\,\mathrm{mm}^2$$

JFET Reverse and Diode Forward Conduction

In this conduction state, the JFET is turned on, and the current flows from the source to the drain terminal. Depending on its magnitude and the junction temperature, the current may flow in the JFET channel as well as in the reverse diode. At a junction temperature of 175°C, for instance, the current flows in the channel and in the diode if it is larger than 6 A. For the considered maximum chip current density of $140\,\mathrm{A/mm^2}$, it is sufficient to approximate the conduction behavior only with a reverse resistance $r_{\mathrm{SD,R}}$ according to (5.13), which depends on the active chip area and the junction temperature.

$$r_{\mathrm{SD,R}}(A_{\mathrm{chip,act}}, T_{\mathrm{J}}) = \frac{k_{1,\mathrm{r_{SD}}} T_{\mathrm{J}} + k_{2,\mathrm{r_{SD}}}}{A_{\mathrm{chip,act}}} \tag{5.13}$$

$$k_{1,\mathrm{r_{SD}}} = 8.444 \cdot 10^{-3} \tfrac{\Omega\,\mathrm{mm}^2}{^\circ\mathrm{C}} \quad k_{2,\mathrm{r_{SD}}} = 8.290 \cdot 10^{-1}\,\Omega\,\mathrm{mm}^2$$

Switching Losses

The sum of the turn-on and turn-off loss energy of the JFET $w_{\mathrm{S,tot}}$ is again expressed as a function of the active chip area, the junction temperature, the switched forward current $i_{\mathrm{S,F}}$, and the switched forward voltage $u_{\mathrm{S,F}}$. Correspondingly, the diode turn-off energy loss (reverse recovery energy) $w_{\mathrm{D,tot}}$ is modeled depending on the active chip area, the junction temperature, the diode forward current $i_{\mathrm{D,F}}$ and the diode reverse voltage $u_{\mathrm{D,R}}$. The resulting mathematical relations are compiled in (5.14) and (5.15).

$$w_{\mathrm{S,tot}}(A_{\mathrm{chip,act}}, i_{\mathrm{S,F}}, u_{\mathrm{S,F}}, T_{\mathrm{J}}) = \tag{5.14}$$
$$A_{\mathrm{chip,act}}\left(k_{1,\mathrm{w_S}}\frac{i_{\mathrm{S,F}}}{A_{\mathrm{chip,act}}} + k_{2,\mathrm{w_S}}\frac{i_{\mathrm{S,F}}^2 u_{\mathrm{S,F}}}{A_{\mathrm{chip,act}}^2} + k_{3,\mathrm{w_S}}\frac{i_{\mathrm{S,F}}u_{\mathrm{S,F}}}{A_{\mathrm{chip,act}}} + k_{4,\mathrm{w_S}}u_{\mathrm{S,F}}^2 + k_{5,\mathrm{w_S}}u_{\mathrm{S,F}}\right)\left(k_{6,\mathrm{w_S}}\frac{i_{\mathrm{S,F}}}{A_{\mathrm{chip,act}}} + \left(\frac{T_{\mathrm{J}} + k_{7,\mathrm{w_S}}}{k_{8,\mathrm{w_S}}}\right)^{k_{9,\mathrm{w_S}}}\right)$$

$$k_{1,\mathrm{w_S}} = 1.246\cdot 10^{-1}\,\frac{\mu\mathrm{J}}{\mathrm{A}} \qquad k_{2,\mathrm{w_S}} = 1.792\cdot 10^{-3}\,\frac{\mu\mathrm{J\,mm^2}}{\mathrm{A^2\,V}}$$
$$k_{3,\mathrm{w_S}} = -4.661\cdot 10^{-3}\,\frac{\mu\mathrm{J}}{\mathrm{A\,V}} \qquad k_{4,\mathrm{w_S}} = 6.375\cdot 10^{-6}\,\frac{\mu\mathrm{J}}{\mathrm{V^2\,mm^2}}$$
$$k_{5,\mathrm{w_S}} = 3.881\cdot 10^{-3}\,\frac{\mu\mathrm{J}}{\mathrm{V\,mm^2}} \qquad k_{6,\mathrm{w_S}} = 6.168\,\frac{\mathrm{mm^2}}{\mathrm{A}}$$
$$k_{7,\mathrm{w_S}} = 273.15°\mathrm{C} \qquad k_{8,\mathrm{w_S}} = 298.15°\mathrm{C}$$
$$k_{9,\mathrm{w_S}} = 3.306\cdot 10^{-1}$$

$$w_{\mathrm{D,tot}}(A_{\mathrm{chip,act}}, i_{\mathrm{D,F}}, u_{\mathrm{D,R}}, T_{\mathrm{J}}) = \tag{5.15}$$
$$A_{\mathrm{chip,act}}\left(k_{1,\mathrm{w_D}}\frac{i_{\mathrm{D,F}}}{A_{\mathrm{chip,act}}} + k_{2,\mathrm{w_D}}\frac{i_{\mathrm{D,F}}^2 u_{\mathrm{D,R}}}{A_{\mathrm{chip,act}}^2} + k_{3,\mathrm{w_D}}u_{\mathrm{D,R}}^2 + k_{4,\mathrm{w_D}}u_{\mathrm{D,R}}\right)\left(k_{5,\mathrm{w_D}}\frac{i_{\mathrm{D,F}}}{A_{\mathrm{chip,act}}} + \left(k_{6,\mathrm{w_D}}\frac{i_{\mathrm{D,F}}}{A_{\mathrm{chip,act}}} + 1\right)\left(\frac{T_{\mathrm{J}} + k_{7,\mathrm{w_D}}}{k_{8,\mathrm{w_D}}}\right)^{k_{9,\mathrm{w_D}}}\right)$$

$$k_{1,\mathrm{w_D}} = -3.517\cdot 10^{-2}\,\frac{\mu\mathrm{J}}{\mathrm{A}} \qquad k_{2,\mathrm{w_D}} = -1.383\cdot 10^{-5}\,\frac{\mu\mathrm{J\,mm^2}}{\mathrm{A^2\,V}}$$
$$k_{3,\mathrm{w_D}} = 7.451\cdot 10^{-6}\,\frac{\mu\mathrm{J}}{\mathrm{V^2\,mm^2}} \qquad k_{4,\mathrm{w_D}} = 8.409\cdot 10^{-4}\,\frac{\mu\mathrm{J}}{\mathrm{V\,mm^2}}$$
$$k_{5,\mathrm{w_D}} = -2.157\,\frac{\mathrm{mm^2}}{\mathrm{A}} \qquad k_{6,\mathrm{w_D}} = 2.258\cdot 10^{-1}\,\frac{\mathrm{mm^2}}{\mathrm{A}}$$
$$k_{7,\mathrm{w_D}} = 273.15°\mathrm{C} \qquad k_{8,\mathrm{w_D}} = 298.15°\mathrm{C}$$
$$k_{9,\mathrm{w_D}} = 1.615$$

5.3 Semiconductor Module

5.3.1 Module Assembly

In order to determine the thermal impedance between the semiconductor junction and the heat sink, a well defined thermal interface between the chip and the heat sink is required. For that purpose, a model of a semiconductor module is developed, which is inspired by the EconoPACK3 from Infineon with a footprint size of 122 mm × 62 mm. The reason for selecting this module type is that a VSBBC topology integrated in the EconoPACK3 is available as commercial product (F12-series, Infineon) and thus provides a volumetric reference for the integration of a bidirectional ac-ac converter in a semiconductor module.

The modeled semiconductor module features a standard assembly with a 3 mm thick copper base plate and a 380 μm thick aluminum oxide (Al_2O_3) substrate. The cross section of the selected module assembly is depicted in Fig. 5.2(a) and the corresponding layer thicknesses are compiled in Tab. 5.2. For the thermal grease layer between the power module base plate and the heat sink, a rather conservative value of 100 μm is assumed compared to the commonly assumed thickness of 50 μm.

Module Layer	*Thickness* (mm)
Si chip	0.115
Solder	0.09
Cu top layer	0.3
Al_2O_3 (substrate)	0.38
Cu bottom layer	0.3
Solder	0.2
Cu base plate	3.0
Thermal grease	0.1

Tab. 5.2: Thickness of the individual layers of the semiconductor module model.

5.3.2 Thermal Impedance

The dependency of the thermal impedance $\underline{Z}_{\mathrm{th,JS}}$ between the semiconductor junction and the heat sink on the total chip area is determined by transient thermal simulations with the simulation software ICEPAK. The simulations are performed for five different total chip areas between $10\,\mathrm{mm}^2$ and $142\,\mathrm{mm}^2$, using the previously defined semiconductor module assembly with the material parameters summarized in Tab. 5.3. Fig. 5.5 depicts a schematic top view on the semiconductor module model. The light gray shaded area indicates the chip placement region.

The size of the copper plane (top copper layer of the substrate) on top of which the chip is soldered, significantly impacts the heat spreading and therewith the thermal properties of the semiconductor chip. In order to provide well defined conditions for determining the thermal properties of different chip areas, a spacing $d_{\mathrm{Cu,chip}}$ between the edge of the chip and the copper plane needs to be specified. The trade-off is that by increasing this spacing, the thermal impedance is reduced, whereas the parasitic capacitance between the copper plane under the chip and the base plate increases proportionally to the area of this plane, which is undesirable regarding EMI. A detailed analysis for the considered module assembly reveals that a spacing larger than 1.5 mm to 2.0 mm does not provide significant benefits in terms of reducing the thermal impedance between the junction and sink, which is in accordance to guidelines provided by semiconductor module manufacturers. Consequently, $d_{\mathrm{Cu,chip}}$ is set to 1.5 mm. The transient thermal simulations for the five different

Material	ρ (g/cm^3)	λ_{th} (W/(m K))	c_{th} (J/(kg K))
Aluminum (Al)	2.7	205	900
Ceramic (Al_2O_3)	4.1	25	880
Copper (Cu)	8.9	388	397
Silicon gel	1.0	0.2	-
Silicon (Si)	2.3	180	770
Solder	8.3	50	200
Thermal grease	1.3	1	-

Tab. 5.3: Density, thermal conductivity, and specific heat capacity of the materials utilized for modeling the semiconductor module.

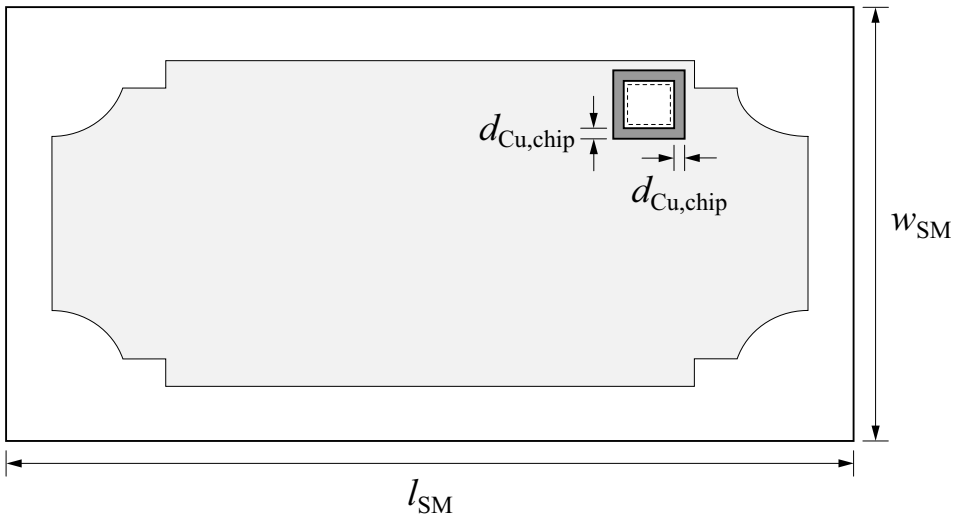


Fig. 5.5: Top view on the module model with a single semiconductor chip. The light gray shaded area highlights the allowable chip placement region and the dark gray area the copper plane under the chip.

chip areas are run sequentially. The semiconductor chip is placed in the corner, as shown in Fig. 5.5, in order to obtain a conservative result for the thermal impedance.

From the implemented converter prototype systems it is known that for an optimized, custom aluminum heat sink with forced air cooling a Cooling System Performance Index (CSPI) [289] between $10\,\mathrm{W/(K\,dm^3)}$ to $12\,\mathrm{W/(K\,dm^3)}$ can be implemented with a justifiable manufacturing expenditure. The typical height of such a cooling system equals to $h_{\mathrm{CS,typ}} = 5\,\mathrm{cm}$. Assuming a CSPI of $11\,\mathrm{W/(K\,dm^3)}$, the specific thermal power flow through the heat sink cooling surface can be calculated to

$$\varsigma_{\mathrm{th,P_{CS}}} = CSPI \cdot h_{\mathrm{CS,typ}} = 550 \frac{\mathrm{W}}{\mathrm{K\,m^2}} \,. \tag{5.16}$$

This quantity is utilized to define the boundary conditions required for the thermal simulations. The resulting thermal impedance curves are approximated with *RC* networks and interpolated with chip area dependent functions as the thermal impedance is inversely proportional to the total chip area. Fig. 5.6 presents the equivalent circuit for the thermal impedance between the semiconductor junction and the heat sink of the cooling system and between the heat sink and the ambient air. Another modeling approach for the semiconductor module is to determine the thermal impedance $\underline{Z}_{\mathrm{th,JC}}$ between the junction and

the case (base plate) of the semiconductor module independently for all semiconductor chips and to apply a common thermal impedance between the case and the heat sink. The disadvantage with this approach is that the resulting junction temperature of a single heavily loaded chip tends to be too low as the model does not account for the local temperature rise of the base plate under the chip. Therefore, this model is not utilized.

The thermal impedance between the junction and the heat sink $\underline{Z}_{\mathrm{th,JS}}$ is modeled with a fourth-order foster network ($R_{1\ldots4,\mathrm{th,JS}}$, $C_{1\ldots4,\mathrm{th,JS}}$), whereas the cooling system (heat sink) is represented by a first-order equivalent ($R_{\mathrm{th,CS}}$, $C_{\mathrm{th,CS}}$). (5.17) to (5.20) present the functions of the resulting thermal resistances $R_{1\ldots4,\mathrm{th,JS}}$.

$$R_{1,\mathrm{th,JS}}(A_{\mathrm{chip,tot}}) = k_{1,\mathrm{R_1}} \left(\frac{1}{\mathrm{mm}^2} A_{\mathrm{chip,tot}} \right)^{k_{2,\mathrm{R_1}}} + k_{3,\mathrm{R_1}} \left(\frac{1}{\mathrm{mm}^2} A_{\mathrm{chip,tot}} \right)^{k_{4,\mathrm{R_1}}} \tag{5.17}$$

$$k_{1,\mathrm{R_1}} = 58.62 \tfrac{\mathrm{K}}{\mathrm{W}} \qquad k_{2,\mathrm{R_1}} = -2.48$$
$$k_{3,\mathrm{R_1}} = 3.02 \cdot 10^{-2} \tfrac{\mathrm{K}}{\mathrm{W}} \qquad k_{4,\mathrm{R_1}} = -6.90 \cdot 10^{-2}$$

$$R_{2,\mathrm{th,JS}}(A_{\mathrm{chip,tot}}) = k_{1,\mathrm{R_2}} \left(\frac{1}{\mathrm{mm}^2} A_{\mathrm{chip,tot}} \right)^{k_{2,\mathrm{R_2}}} + k_{3,\mathrm{R_2}} \left(\frac{1}{\mathrm{mm}^2} A_{\mathrm{chip,tot}} \right)^{k_{4,\mathrm{R_2}}} \tag{5.18}$$

$$k_{1,\mathrm{R_2}} = 3.48 \tfrac{\mathrm{K}}{\mathrm{W}} \qquad k_{2,\mathrm{R_2}} = -3.23 \cdot 10^{-1}$$
$$k_{3,\mathrm{R_2}} = -1.30 \tfrac{\mathrm{K}}{\mathrm{W}} \qquad k_{4,\mathrm{R_2}} = -1.49 \cdot 10^{-1}$$

$$R_{3,\mathrm{th,JS}}(A_{\mathrm{chip,tot}}) = k_{1,\mathrm{R_3}} \left(\frac{1}{\mathrm{mm}^2} A_{\mathrm{chip,tot}} \right)^{k_{2,\mathrm{R_3}}} \tag{5.19}$$

$$k_{1,\mathrm{R_3}} = 5.09 \tfrac{\mathrm{K}}{\mathrm{W}} \qquad k_{2,\mathrm{R_3}} = -7.72 \cdot 10^{-1}$$

$$R_{4,\mathrm{th,JS}}(A_{\mathrm{chip,tot}}) = k_{1,\mathrm{R_4}} \left(\frac{1}{\mathrm{mm}^2} A_{\mathrm{chip,tot}} \right)^{k_{2,\mathrm{R_4}}} \tag{5.20}$$

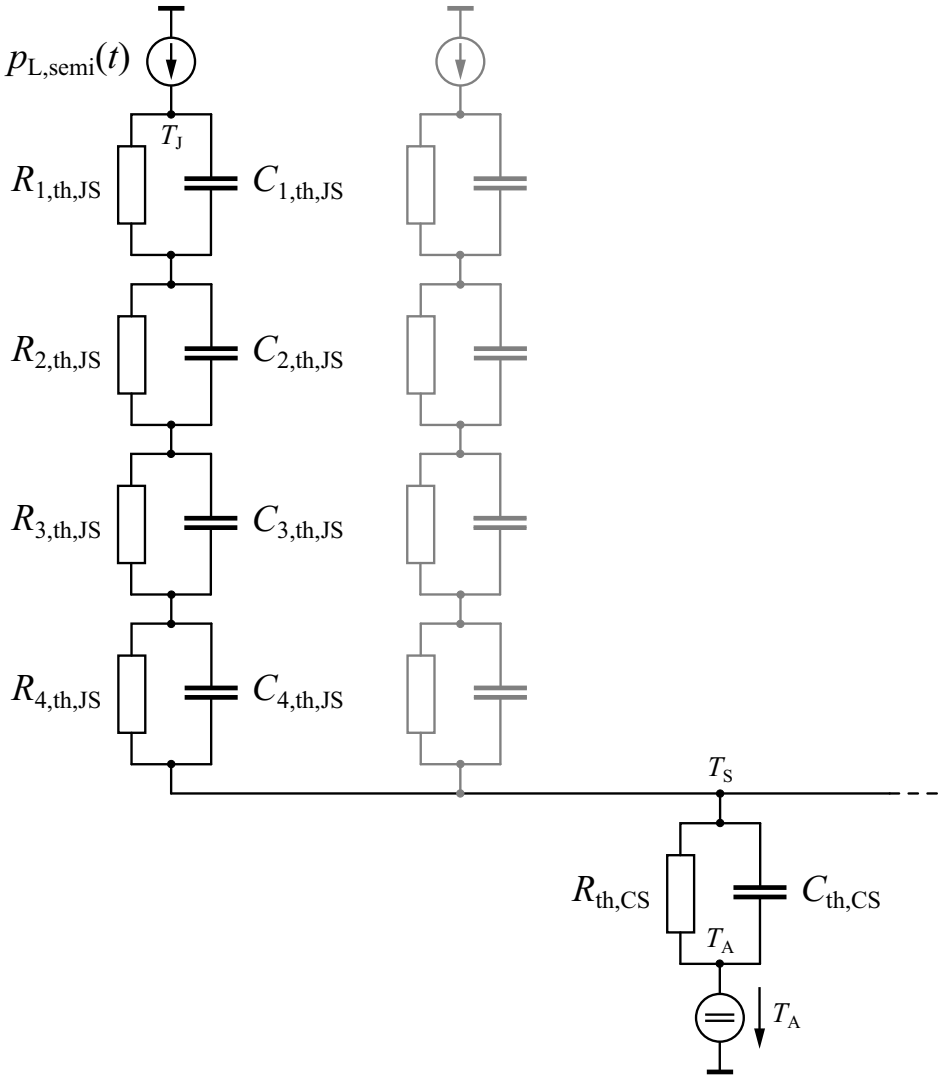


Fig. 5.6: *RC* network to model the thermal impedance between the junction, the heat sink, and the ambient air.

$$k_{1,\mathrm{R}_4} = 3.94 \cdot 10^{-1}\,\frac{\mathrm{K}}{\mathrm{W}} \quad k_{2,\mathrm{R}_4} = -2.91 \cdot 10^{-1}$$

The corresponding time constants $\tau_{1\ldots4,\mathrm{th,JS}}$ of the impedance function of $Z_{\mathrm{th,JS}}$ are obtained by (5.21) to (5.24).

$$\tau_{1,\mathrm{th,JS}}(A_{\mathrm{chip,tot}}) = k_{1,\tau_1} A_{\mathrm{chip,act}} + k_{2,\tau_1} \tag{5.21}$$

$$k_{1,\tau_1} = 4.28 \cdot 10^{-6}\,\frac{\mathrm{s}}{\mathrm{mm}^2} \quad k_{2,\tau_1} = 5.92 \cdot 10^{-4}\,\mathrm{s}$$

$$\tau_{2,\mathrm{th,JS}}(A_{\mathrm{chip,tot}}) = k_{1,\tau_2} A_{\mathrm{chip,act}} + k_{2,\tau_2} \tag{5.22}$$

$$k_{1,\tau_2} = 8.94 \cdot 10^{-5}\,\frac{\mathrm{s}}{\mathrm{mm}^2} \quad k_{2,\tau_2} = 7.29 \cdot 10^{-3}\,\mathrm{s}$$

$$\tau_{3,\mathrm{th,JS}} = 5.00 \cdot 10^{-2}\,\mathrm{s} \tag{5.23}$$

$$\tau_{4,\mathrm{th,JS}}(A_{\mathrm{chip,tot}}) = k_{1,\tau_4} A_{\mathrm{chip,act}}^3 + k_{2,\tau_4} A_{\mathrm{chip,act}}^2 + k_{3,\tau_4} A_{\mathrm{chip,act}} + k_{4,\tau_4} \tag{5.24}$$

$$k_{1,\tau_4} = 1.37 \cdot 10^{-7}\,\tfrac{\mathrm{s}}{\mathrm{mm}^6} \quad k_{2,\tau_4} = -2.95 \cdot 10^{-5}\,\tfrac{\mathrm{s}}{\mathrm{mm}^4}$$
$$k_{3,\tau_4} = 1.30 \cdot 10^{-3}\,\tfrac{\mathrm{s}}{\mathrm{mm}^2} \quad k_{4,\tau_4} = 5.20 \cdot 10^{-1}\,\mathrm{s}$$

The equivalent thermal capacitances $C_{1\ldots4,\mathrm{th,JS}}$ can then be calculated using the following relation

$$C_{i,\mathrm{th,JS}}(A_{\mathrm{chip,tot}}) = \frac{\tau_{i,\mathrm{th,JS}}}{R_{i,\mathrm{th,JS}}}\ . \tag{5.25}$$

By solving the differential equation resulting from the RC network and substitution the functions for $R_{1\ldots4,\mathrm{th,JS}}$ and $\tau_{1\ldots4,\mathrm{th,JS}}$, the step response, i.e. the transient thermal impedance between the junction and the heat sink can be expressed as a function of the total chip area.

$$Z_{\mathrm{th,JS}}(A_{\mathrm{chip,tot}}, t) = \sum_{i=1}^{4} R_{i,\mathrm{th,JS}} \left(1 - e^{\frac{-t}{\tau_{i,\mathrm{th,JS}}}}\right) \tag{5.26}$$

Accordingly, the step response of the thermal impedance between the junction and the ambient air may be approximated by

$$Z_{\mathrm{th,JA}}(A_{\mathrm{chip,tot}}, t) = \sum_{i=1}^{4} R_{i,\mathrm{th,JS}} \left(1 - e^{\frac{-t}{\tau_{i,\mathrm{th,JS}}}}\right) + R_{\mathrm{th,CS}} \left(1 - e^{\frac{-t}{\tau_{\mathrm{th,CS}}}}\right)\ . \tag{5.27}$$

$$\tau_{\mathrm{th,CS}} = C_{\mathrm{th,CS}} R_{\mathrm{th,CS}}$$

The stationary thermal resistance between the junction and the heat sink $R_{\mathrm{th,JS}}$ and between the junction and the ambient air $R_{\mathrm{th,JA}}$ equals to

$$R_{\mathrm{th,JS}}(A_{\mathrm{chip,tot}}) = \lim_{t\to\infty} Z_{\mathrm{th,JS}}(A_{\mathrm{chip,tot}}, t) = \sum_{i=1}^{4} R_{i,\mathrm{th,JS}} \tag{5.28}$$

$$R_{\mathrm{th,JA}}(A_{\mathrm{chip,tot}}) = \sum_{i=1}^{4} R_{i,\mathrm{th,JS}} + R_{\mathrm{th,SA}}\ . \tag{5.29}$$

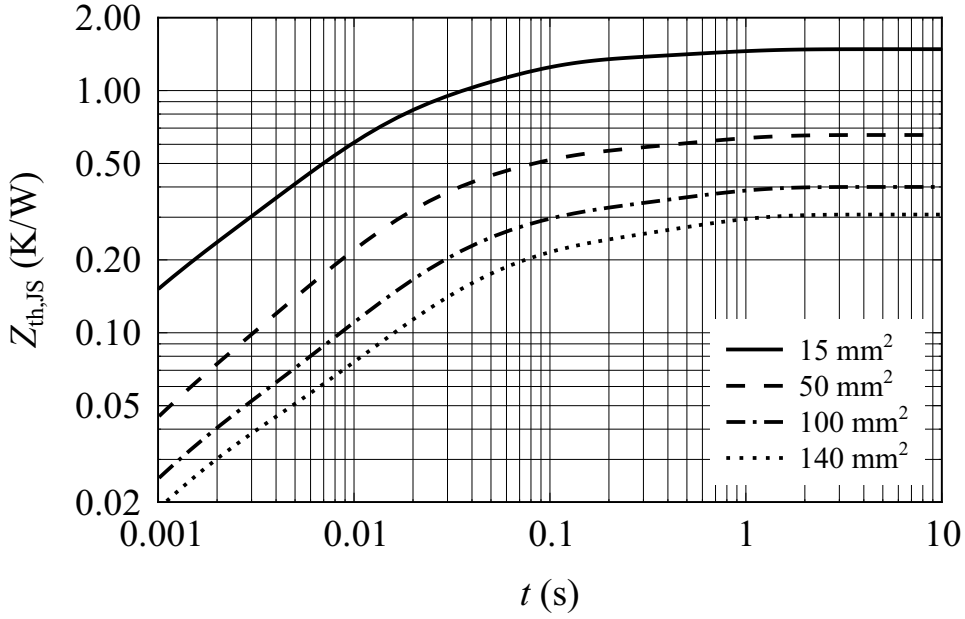


Fig. 5.7: Transient thermal impedance $Z_{\mathrm{th,JS}}$ for various total chip areas and a CSPI of $11\,\mathrm{W/(K\,dm^3)}$, calculated with the semiconductor module model.

Finally, in Fig. 5.7 the transient thermal impedance $Z_{\mathrm{th,JS}}$ is plotted using (5.26) for four different chip areas. The stationary values show good agreement (deviation $\leq \pm 6\%$) with manufacturer data of the same semiconductor module assembly.

5.3.3 Volume

The total required semiconductor chip area of a power electronic converter can be used to determine the volume of its semiconductor module. For that purpose, the ratio

$$\gamma_{\mathrm{A_{chip-SM}}} = \frac{A_{\mathrm{chip,SM}}}{A_{\mathrm{SM}}} \tag{5.30}$$

between the total implemented chip area of a semiconductor module $A_{\mathrm{chip,SM}}$ and the area of the base plate A_{SM} needs to be determined. By inspection of different semiconductor modules with the same assembly as employed for the considered module model, a realistic value for $\gamma_{\mathrm{A_{chip-SM}}}$ is found to be 15%. Assuming a constant height of the semiconductor module of $h_{\mathrm{SM}} = 15\,\mathrm{mm}$, the volume of the module can then

be calculated to

$$V_{\mathrm{SM}}(A_{\mathrm{chip,SM}}) = \frac{A_{\mathrm{chip,SM}}}{\gamma_{\mathrm{A_{chip-SM}}}} h_{\mathrm{SM}} \ . \tag{5.31}$$

With reference to Fig. 5.5, it is assumed that the length l_{SM} of the semiconductor module remains constant and only the width w_{SM} is varied to modify the base plate area of the module. This corresponds to a parallel connection of multiple modules, as typically found in industrial converter systems to increase the current rating. The width of the semiconductor module is then given by

$$w_{\mathrm{SM}}(A_{\mathrm{chip,SM}}) = \frac{A_{\mathrm{chip,SM}}}{l_{\mathrm{SM}} \gamma_{\mathrm{A_{chip-SM}}}} = \frac{A_{\mathrm{SM}}}{l_{\mathrm{SM}}} \ . \tag{5.32}$$

The required electrical and mechanical parameters of the semiconductor module are compiled in Tab. 5.4. In order to provide a relation between the average semiconductor losses P_{semi} and the base plate area A_{SM}, the maximum specific power flow through the base plate $\varsigma_{\mathrm{P_{SM},max}}$ is limited to $10\,\mathrm{W/cm^2}$ based on manufacturer data.

$$\frac{P_{\mathrm{semi}}}{A_{\mathrm{SM}}} \leq \varsigma_{\mathrm{P_{SM},max}} \tag{5.33}$$

Parameter	*Value*
Length	$l_{\mathrm{SM}} = 122\,\mathrm{mm}$ (constant)
Nominal width	$w_{\mathrm{SM,nom}} = 62\,\mathrm{mm}$ (variable)
Height	$h_{\mathrm{SM}} = 15\,\mathrm{mm}$
Volumetric density	$\rho_{\mathrm{SM}} = 2.4\,\mathrm{g/cm^3}$
Maximum specific power flow through the base plate	$\varsigma_{\mathrm{P_{SM},max}} = 10\,\mathrm{W/cm^2}$
Ratio of chip-to-base-plate area	$\gamma_{\mathrm{A_{chip-SM}}} = 0.15$

Tab. 5.4: Electrical and mechanical parameters of the module model.

5.3.4 Weight

By comparing volume and weight of various power converter topologies implemented in an EconoPACK3 (reference module), an average density ρ_{SM} of 2.4 g/cm^3 is found. Thus, the weight of the semiconductor module can be estimated as a function of the total implemented chip area.

$$m_{\mathrm{SM}}(A_{\mathrm{chip,SM}}) = V_{\mathrm{SM}}\rho_{\mathrm{SM}} = \frac{A_{\mathrm{chip,SM}}}{\gamma_{\mathrm{A_{chip-SM}}}} h_{\mathrm{SM}}\rho_{\mathrm{SM}} \tag{5.34}$$

5.4 Cooling System

5.4.1 Design

The cooling system design aims for a simple and compact construction with an average CSPI of 11 W/(K dm^3) as specified for the thermal simulations (cf. Sec. 5.3.2). The demanded characteristics can be achieved with a forced air cooled, optimized aluminum heat sink. For the custom heat sink, a sub-optimum design, suggested in [290], is applied to simplify the manufacturing while still maintaining superior cooling performance compared to commercially available extruded aluminum heat sinks. The schematic profile and the cross section of a single heat sink element are depicted in Fig. 5.8. Such a heat sink element consists of a high-performance 12 V dc fan from Sanyo Denki (SanAce 40, GA-series) and a custom aluminum heat sink with a length l_{S} between 142 mm and 202 mm, a width w_{S} of 40 mm, and a height h_{S} of 46 mm. Depending on

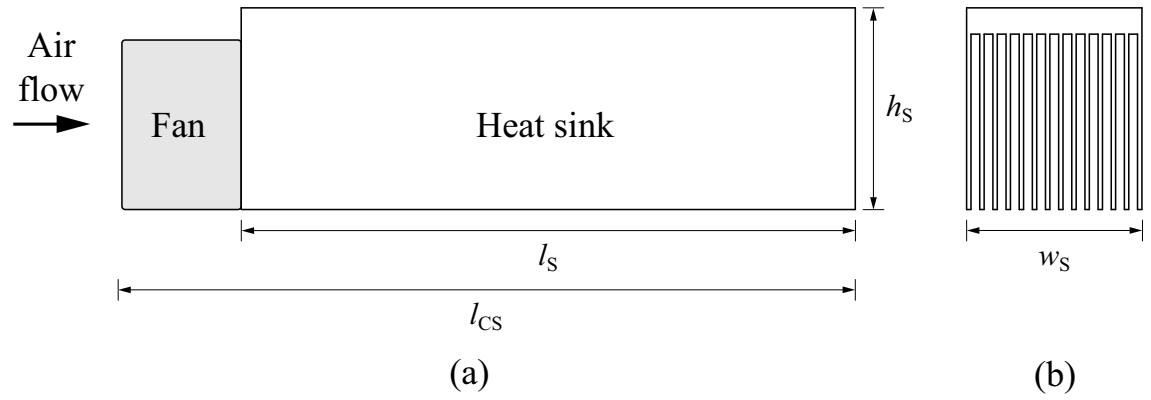


Fig. 5.8: (a) Schematic profile and **(b)** cross section of a heat sink element, showing the dimensions and the direction of the air flow.

the cooling requirements and the base plate area of the semiconductor module, n_S heat sink elements are arranged in parallel, thus forming a heat sink such that the required thermal resistance of the cooling system is obtained and the base plate area of the module is smaller than the base area of the heat sink. (Obviously the resulting heat sink is finally manufactured from a single piece of aluminum.) The length of the heat sink hence can be varied continuously within the given margins, whereas the width of the heat sink can only be varied by increments of 40 mm depending on the number of paralleled heat sink elements n_S. This restriction is motivated by the fact that only a limited number of different high performance fans is available, and that from a logistic point of view it is too costly to develop custom fans matching the cross section of any heat sink design. The overall dimensions of the cooling system are then given by

$$l_{CS} = l_S + 28\,\text{mm} = [170 \ldots 230]\,\text{mm} \tag{5.35}$$

$$w_{CS} = n_S w_S = 40\,\text{mm} \cdot n_S \tag{5.36}$$

$$h_{CS} = h_S = 46\,\text{mm}\,. \tag{5.37}$$

The components and dimensions of the designed cooling system are summarized in Tab. 5.5.

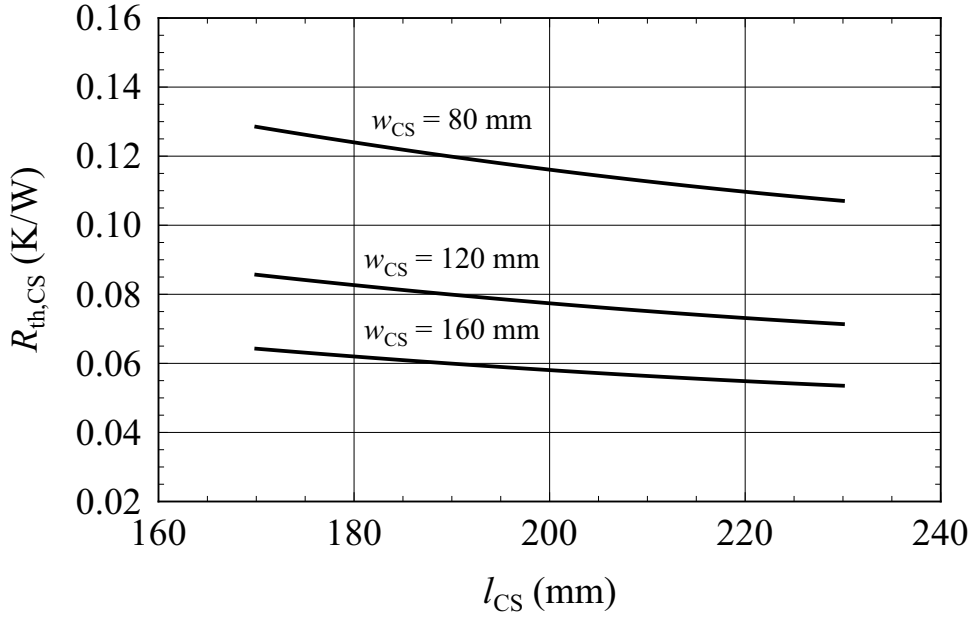


Fig. 5.9: Thermal resistance $R_{th,CS}$ of the cooling system depending on its length l_{CS} and width w_{CS}.

5.4.2 Thermal Resistance

The thermal resistance of the cooling system between the heat sink and the ambient air $R_{\mathrm{th,CS}}$ is determined according to (11) to (14) in [290]. For that purpose, the heat sink (cf. Fig. 5.8) is modeled by the thermal resistance of the base plate, the fins, and the interface between the fin surface and the air flow through the heat sink. Ultimately, the resulting thermal resistance of the cooling system $R_{\mathrm{th,CS}}$ can be represented as a function of the length l_{CS} and width w_{CS} of the cooling system. In Fig. 5.9, the thermal resistance of the cooling system is plotted as a function of its length.

$$R_{\mathrm{th,CS}}(l_{\mathrm{CS}}, w_{\mathrm{CS}}) = \left(k_{1,\mathrm{R_{CS}}} l_{\mathrm{CS}}^2 + k_{2,\mathrm{R_{CS}}} l_{\mathrm{CS}} + k_{3,\mathrm{R_{CS}}}\right) \frac{1}{w_{\mathrm{CS}}} \tag{5.38}$$

$$k_{1,\mathrm{R_{CS}}} = 1.50 \cdot 10^{-4} \tfrac{\mathrm{K}}{\mathrm{W\,mm}} \quad k_{2,\mathrm{R_{CS}}} = -8.86 \cdot 10^{-2} \tfrac{\mathrm{K}}{\mathrm{W}}$$
$$k_{3,\mathrm{R_{CS}}} = 21.01 \tfrac{\mathrm{K\,mm}}{\mathrm{W}}$$

5.4.3 Thermal Capacitance

In the model of the thermal impedance $Z_{\mathrm{th,JS}}$ between the semiconductor junction and the heat sink, the effective thermal capacitance of the base plate underneath the chip within the heat spreading region is considered to accurately describe the transient response. Hence, the total thermal capacitance of the base plate does not need to be determined separately. The thermal capacitance of the cooling system $C_{\mathrm{th,CS}}$ can be simply approximated by the thermal capacitance of the aluminum of the heat sink as a function of the length l_{CS} and width w_{CS} of the cooling system.

$$C_{\mathrm{th,CS}}(l_{\mathrm{CS}}, w_{\mathrm{CS}}) = \left(k_{1,\mathrm{C_{CS}}} l_{\mathrm{CS}} + k_{2,\mathrm{C_{CS}}}\right) w_{\mathrm{CS}} + k_{3,\mathrm{C_{CS}}} \tag{5.39}$$

$$k_{1,\mathrm{C_{CS}}} = 4.78 \cdot 10^{-2} \tfrac{\mathrm{J}}{\mathrm{K\,mm^2}} \quad k_{2,\mathrm{C_{CS}}} = -1.45 \tfrac{\mathrm{J}}{\mathrm{K\,mm}}$$
$$k_{3,\mathrm{C_{CS}}} = 16.5 \tfrac{\mathrm{J}}{\mathrm{K}}$$

5.4.4 Volume

The volume of the cooling system V_{CS} is the boxed volume of the heat sink and the fans and is modeled using the length l_{CS} and width w_{CS}

of the cooling system.

$$V_{\mathrm{CS}}(l_{\mathrm{CS}}, w_{\mathrm{CS}}) = (k_{1,\mathrm{V_{CS}}} l_{\mathrm{CS}} + k_{2,\mathrm{V_{CS}}})\, w_{\mathrm{CS}} \tag{5.40}$$

$$k_{1,\mathrm{V_{CS}}} = 4.60 \cdot 10^{-2}\,\frac{\mathrm{cm}^3}{\mathrm{mm}^2} \quad k_{2,\mathrm{V_{CS}}} = -1.68 \cdot 10^{-1}\,\frac{\mathrm{cm}^3}{\mathrm{mm}}$$

The free space required for a proper air intake of the fans is not considered. By dividing (5.38) by (5.40), the resulting CSPI can be determined.

$$CSPI = [11.3 \ldots 12.8]\,\frac{\mathrm{W}}{\mathrm{K\,dm}^3} \tag{5.41}$$
$$\text{for } l_{\mathrm{CS}} = [230 \ldots 170]\ \mathrm{mm}$$

As can be seen in (5.41), the achieved CSPI is above $11\,\mathrm{W/(K\,dm^3)}$ as demanded by the design specifications.

Component	*Parameter*	*Value*
Heat sink	Manufacturer	Custom
	Material	Aluminum (e.g. Ac-112)
	Length	142 mm . . . 202 mm
	Width	80 mm, 120 mm, 160 mm, 200 mm
	Height	46 mm
	Fin height	40 mm
	Fin thickness	≈ 1 mm
	Fin spacing	2 mm
Fan	Manufacturer	Sanyo Denki
	Type	SanAce 40, 9GA0412P3J01
	Rated voltage	12 V
	Rated input power	5.88 W
	Rated speed	18 000 rpm
	Air flow	$0.67\,\mathrm{m^3/min} = 23.7\,\mathrm{CFM}$
	Static pressure	535 Pa
	Dimensions	40 mm × 40 mm × 28 mm
	Weight	53 g

Tab. 5.5: Cooling system component specifications.

5.4.5 Weight

With the density of aluminum and the weight of a fan, the total weight of the cooling system m_{CS} is given by the length l_{CS} and width w_{CS} of the cooling system.

$$m_{\mathrm{CS}}(l_{\mathrm{CS}}, w_{\mathrm{CS}}) = \left(k_{1,\mathrm{m_{CS}}} l_{\mathrm{CS}} + k_{2,\mathrm{m_{CS}}}\right) w_{\mathrm{CS}} + k_{3,\mathrm{m_{CS}}} \tag{5.42}$$

$$k_{1,\mathrm{m_{CS}}} = 5.33 \cdot 10^{-2} \tfrac{\mathrm{g}}{\mathrm{mm^2}} \quad k_{2,\mathrm{m_{CS}}} = -3.20 \cdot 10^{-1} \tfrac{\mathrm{g}}{\mathrm{mm}}$$
$$k_{3,\mathrm{m_{CS}}} = 18.4\,\mathrm{g}$$

5.4.6 Fan Power Consumption

The fan power consumption P_{CS} can be calculated with the number of the heat sink elements n_{S} as every element is equipped with a fan.

$$P_{\mathrm{CS}}(n_{\mathrm{S}}) = 5.9\,\mathrm{W} \cdot n_{\mathrm{S}} \tag{5.43}$$

5.5 Gate Driver

5.5.1 Losses

The SAC2 also enables to estimate the losses of the gate driver as the active transistor chip area $A_{\mathrm{S,chip,act}}$ is proportional to the gate charge. For a given gate charge Q_{G}, a difference between the maximum and minimum gate-emitter or gate-source voltage $U_{\mathrm{GE/S,max}}$ and $U_{\mathrm{GE/S,min}}$, and a switching frequency f_{sw}, the losses generated in the gate resistor can be calculated to

$$P_{\mathrm{G}} = Q_{\mathrm{G}} \left(U_{\mathrm{GE/S,max}} - U_{\mathrm{GE/S,min}}\right) f_{\mathrm{sw}} \,. \tag{5.44}$$

The required values of the gate charge are determined from data sheets and SPICE models provided by the semiconductor manufacturer for a switched voltage of 600 V and a nominal chip current density of $140\,\mathrm{A/cm^2}$. In order to provide a fair comparison between the IGBT and the JFET, the difference between the maximum and minimum gate voltage is set to 18 V. Thereby, it is assumed that the gate-emitter voltage u_{GE} of the IGBT is switched between -3 V and $+15$ V, whereas the gate-source voltage u_{GS} of the JFET is switched between -18 V and

0 V. In (5.45) and (5.46) the resulting gate charge of the IGBT and the JFET are approximated as a function of the active transistor chip area.

$$Q_{\mathrm{G,IGBT}}\left(A_{\mathrm{S,chip,act}}\right) = 6.5\frac{\mathrm{nC}}{\mathrm{mm}^2}A_{\mathrm{S,chip,act}} + 4.9\,\mathrm{nC} \tag{5.45}$$

$$Q_{\mathrm{G,JFET}}\left(A_{\mathrm{S,chip,act}}\right) = 11.0\frac{\mathrm{nC}}{\mathrm{mm}^2}A_{\mathrm{S,chip,act}} \tag{5.46}$$

The losses in the gate resistor can be utilized to estimate the resulting gate driver losses P_{drv}. For that purpose, a model of a gate driver circuit is developed, which comprises a H-bridge oscillator and a transformer for the galvanically isolated gate driver power supply, a magnetic coupler for the gate signal isolation, and a gate driver IC with a half-bridge MOSFET output stage. The power consumption of the driver IC is derived from the IXDN4xx gate driver series from IXYS and verified with the results of gate driver power consumption measurements performed with the hardware prototypes. The overall power consumption of the gate driver is then given by

$$\begin{aligned} P_{\mathrm{drv}}(P_{\mathrm{G}}, f_{\mathrm{sw}}) &= \frac{P_{\mathrm{G}}}{0.053\ln\left(\frac{1}{\mathrm{Hz}}f_{\mathrm{sw}}\right) + 0.074} + 0.1\,\mathrm{W} \\ f_{\mathrm{sw}} &= [1\ldots300]\,\mathrm{kHz} \end{aligned} \tag{5.47}$$

and thus can be expressed with (5.44) to (5.46) as a function of the active chip area and the switching frequency. The constant term of 0.1 W accounts for the stand-by losses of the gate driver. (5.47) is valid for switching frequencies between 1 kHz and 300 kHz.

5.5.2 Volume

The gate driver model allows the calculation of the boxed volume of the gate driver based on the active chip area $A_{\mathrm{S,chip,act}}$ and the required power of the gate driver P_{drv}.

$$V_{\mathrm{drv}}(A_{\mathrm{S,chip,act}}, P_{\mathrm{drv}}) = \begin{cases} \text{If } A_{\mathrm{S,chip,act}}P_{\mathrm{drv}} \leq 20\,\mathrm{W\,mm^2} \\ 6.0\,\mathrm{cm}^3 \\ \text{If } A_{\mathrm{S,chip,act}}P_{\mathrm{drv}} > 20\,\mathrm{W mm^2} \\ 3\cdot10^{-3}\frac{\mathrm{cm}^3}{W\mathrm{mm}^2}\,A_{\mathrm{S,chip,act}}P_{\mathrm{drv}} \\ \qquad +5.9\,\mathrm{cm}^3 \end{cases} \tag{5.48}$$

It should be noted that only the components of the gate driver supply and the driver IC scale with the active chip area and the switching frequency.

5.5.3 Weight

Correspondingly, also the weight of the gate driver can be estimated based on the active transistor chip area $A_{\mathrm{S,chip,act}}$ and the required power of the gate driver P_{drv}.

$$m_{\mathrm{drv}}(A_{\mathrm{S,chip,act}}, P_{\mathrm{drv}}) = \begin{cases} \text{If } A_{\mathrm{S,chip,act}} P_{\mathrm{drv}} \leq 20\,\mathrm{Wmm^2} \\ 9.0\,\mathrm{g} \\ \text{If } A_{\mathrm{S,chip,act}} P_{\mathrm{drv}} > 20\,\mathrm{Wmm^2} \\ 9 \cdot 10^{-3} \frac{\mathrm{g}}{W\mathrm{mm^2}} A_{\mathrm{S,chip,act}} P_{\mathrm{drv}} \\ \qquad +8.8\,\mathrm{g} \end{cases} \tag{5.49}$$

5.6 Classification of Junction Temperature Variations

To conclude with, the origin of periodic variations of the junction temperature of ac-ac converters for drive systems are briefly discussed and classified. By analyzing the formation of the semiconductor losses in the considered converters, four characteristic sources can be identified:

1. The variation of the junction temperature $\Delta T_{\mathrm{J,f_{sw}}}$ with the switching frequency at a fixed operating point of the drive system.

2. For matrix-type converters, the variation of the junction temperature $\Delta T_{\mathrm{J,f_1}}$, $\Delta T_{\mathrm{J,f_2}}$, and $\Delta T_{\mathrm{J,|f_1-f_2|}}$ with the electrical input frequency f_1, the electrical output frequency f_2 of the converter and with the difference between the input and the output frequency $|f_1 - f_2|$ at a fixed operating point of the drive system.

3. The variation of the average junction temperature $\Delta T_{\mathrm{J,OP}i-j}$ due to a change of the operating point (OPi to OPj), demanded by the mission profile of the drive system.

4. The variation of the junction temperature during failure modes or emergency shut-down of the drive system.

For a given operating point, converter design and assembly concept, the variation of the junction temperature according to point 1, 2, and 4 can only be lowered by increasing the semiconductor chip area and thus can be utilized as comparison or optimization criteria for the SAC2. By contrast, the variation and the gradient of the average junction temperature, addressed in point 3, may be influenced by the control scheme if reduced control performance of the converter system is tolerable. The fan motor of a ventilation system, for example, could be accelerated slowly by ramping-up the motor current in such a way that a smooth transition of the average junction temperature from its low to its high level is ensured in order to increase the lifetime of the power converter. Such a control strategy might be referred to as "Lifetime Enhancing Control Scheme".

5.7 Summary

The performance and cost of a power electronic converter system are substantially determined by the power semiconductors. In a converter trade-off study, it is hence essential to carefully consider and compare the semiconductor requirements and their impact on the overall system performance.

It is difficult to identify with known approaches a common (fair) basis for comparison. For this purpose, a new Semiconductor chip Area based Converter Comparison (SAC2) is suggested that allows the calculation of the total semiconductor chip area and the optimal partitioning of a total chip area to the transistors and diodes of a converter topology depending on the operating point and predefined boundary conditions, such as for instance the maximum average junction temperature. The suggested SAC2 does not only guarantee best semiconductor material usage, but implicitly provides with the chip area information a distinct characteristic quantity for comparison.

In order to perform the SAC2, semiconductor loss models of the considered Si IGBT4, EmCon4 diode, and SiC JFET technology are derived that enable to determine the conduction and switching losses as a function of the chip area, the device current and voltage, and the junction temperature. The required relationship between the chip area and the chip cooling properties is obtained by numerical simulation of the transient thermal impedance between the junction and the heat sink

surface of a typical module assembly (reference module: EconoPACK3, Infineon) for a predefined cooling system. Different placements of the chips within the module are investigated and the worst case (highest thermal impedance) for a given chip area is selected.

The semiconductor losses, the required cooling system performance, and the gate driver requirements of the compared converter topologies can be calculated for the considered operating point based on the resulting chip data. Models are developed that ultimately allow the determination of the volume, weight, and power consumption of the cooling system and the gate drivers.

The actual mechanical placement of the individual chips of a circuit topology in the semiconductor module has a minor impact on the resulting junction temperature and therewith on the total chip area determined by the SAC2, as for a typical ratio of the chip-to-base-plate-area of 15%, which is valid for the selected module assembly, the thermal coupling between the chips is low. By considering the thermal impedance between the junction and the heat sink and not between the junction and the base plate, the impact of the heat spreading due to the base plate is implicitly included in the thermal impedance model, which further reduces the influence of the placement of the chips on their thermal properties. However, if a SAC2 is performed for custom modules with a high integration density, the mechanical placement data of the chips should be used as additional input parameters.

Chapter 6

Passives and EMI

Capacitors and inductors, generally referred as passive components, play a key role in ac-ac converter systems. They are utilized to provide local energy storage and filtering of switched discontinuous voltages and currents to ultimately enable compliance to power quality and EMC standards. Passive components have a significant impact on the overall converter volume and weight due to their physical properties and therefore need to be considered when comparing different converter concepts.

In this chapter, firstly, the relation between the volume and weight of capacitors and inductors are derived for commonly used capacitor and inductor technologies. Subsequently, the EMI noise models of all considered converter topologies for line conducted emissions including a motor load are determined. Based on that, an EMI input filter topology and a filter design procedure are presented in order to provide compliance to the EMC standards.

Finally, the influence of the passive component design on the converter performance is discussed and design guidelines are provided. This chapter concludes with a set of EMI measurements providing practical evidence of the suitability of the suggested passive component and filter design for a drive system with an IMC.

6.1 Passive Components

6.1.1 Capacitors

A frequently used argument in favor of the MC is that with the absence of the dc-link capacitor, a converter lifetime limiting component due to thermal aging is implicitly omitted. This argument shall provide the starting point for the subsequent investigation of dc-link and EMI suppression capacitors.

With respect to state-of-the-art capacitor technologies, the above argument has to be considered carefully, which is briefly shown by the following example. For that purpose, a foil and an electrolytic dc-link capacitor are considered that both provide a capacitance of 100 μF at an operating temperature of 85°C. Despite the maximum dc-link voltage of the considered VLBBC is assumed with 770 V (+10% of the nominal voltage of 700 V), the operating voltage of the dc-link capacitor is selected with 900 V to ensure a sufficiently long service lifetime. In this example, the dc-link capacitance is implemented with polypropylene foil capacitors (3277x-series, EPCOS) and a series-parallel connection of 450 V aluminum electrolytic capacitors (B43699-series, EPCOS). In order to highlight the characteristics of the considered capacitor technologies, the dc-link capacitors are designed for a minimum useful life of 100 000 h at a constant operating temperature of 70°C and a boxed volume of 250 cm^3 based on the rated voltage and the tolerable rms current ripple at 10 kHz using reliability data provided by the manufacturer [291, 292]. The characteristic quantities of the two dc-link capacitors are summarized in Tab. 6.1 and lead to the following conclusions:

- With both technologies a considerable useful life of the dc-link capacitor can be achieved.
- Under the restriction of a given maximum volume, foil capacitors should be selected, if maximizing the allowable current ripple and the lifetime are the relevant design criteria. However, if maximizing the capacitance is the relevant design criterion, electrolytic capacitors should be considered.
- The specific weight of both capacitor technologies are similar.

From this perspective the provided internal energy storage at a specified lifetime of the energy storage components or simply the lifetime of the

Parameter	*Foil Capacitor*	*Electrolytic Capacitor*
Component	B3277x, EPCOS	B43699, EPCOS
Capacitance	100 μF	230 μF
Volume	250 cm^3	250 cm^3
Weight	300 g	290 g
Max. current at 10 kHz	50 A	14 A
Operating voltage	900 V	900 V
Operating temperature	70°C	70°C
Useful life	170 000 h	100 000 h

Tab. 6.1: Polypropylene foil versus electrolytic dc-link capacitors.

passive components are more adequate criteria for comparing different converter concepts than the rather general argument of "thermal aging of the dc-link capacitor" stated above.

In order to enable superior capacitor lifetime, the considerations are restricted to polypropylene foil and Class II ceramic multi-layer capacitors that are made of a ferroelectric X7R dielectric. Fig. 6.1 to Fig. 6.4 present the volume and weight of the two characteristic capacitor types that are required for ac-ac converters: dc-link and EMI suppression ac capacitors. In this comparison, X2 capacitors, providing a peak surge voltage capability of 2.5 kV and Y2 capacitors with a peak surge voltage capability of 5 kV, both rated for a continuous rms voltage of 305 V, are considered for EMI suppression. The X-type capacitors are typically placed between a phase and a common star-point or across two phases and thus are utilized for Differential Mode (DM) filtering. The Y-type capacitors are connected between the phase and ground and are required for Common Mode (CM) filtering. The reference manufacturers selected is EPCOS for foil capacitors and Murata for ceramic capacitors as components of these manufactures are implemented in the hardware prototypes. The component ratings of different manufacturers are very similar and do not need to be considered separately.

The volume of the foil capacitors is given by the boxed volume of their cubical cases. The volume of the ceramic capacitors is determined based on 2220 chip capacitors (foot print area: 5.7 mm × 5.0 mm), whereby a

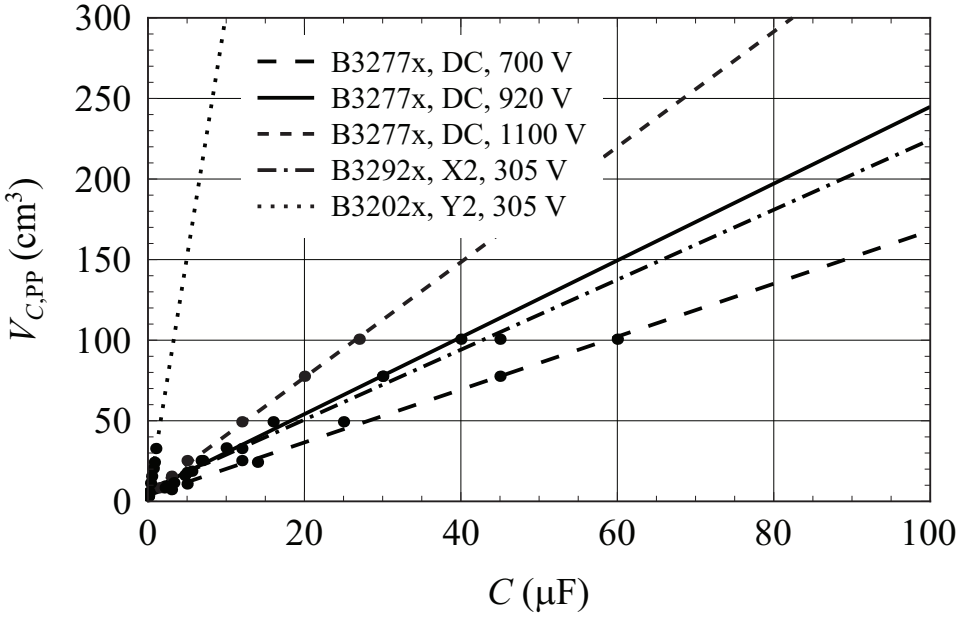


Fig. 6.1: Volume versus capacitance of polypropylene (PP) foil dc-link, X2, and Y2 capacitors from EPCOS at $T_{\mathrm{op}} = 85°\mathrm{C}$.

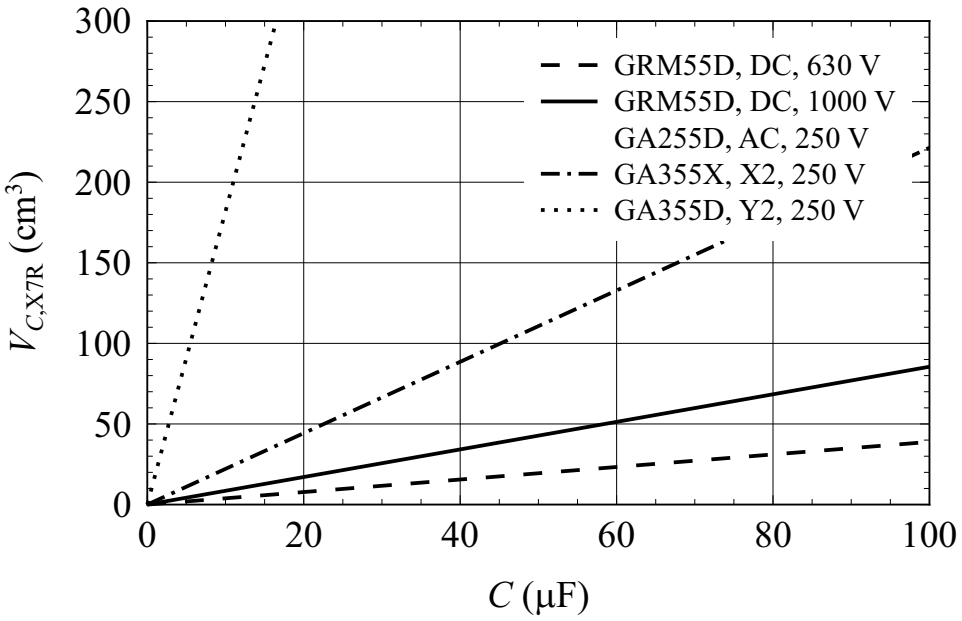


Fig. 6.2: Volume versus capacitance of X7R ceramic dc-link, ac, X2, and Y2 capacitors from Murata at $T_{\mathrm{op}} = 85°\mathrm{C}$.

volumetric fill factor of 65% is assumed to ensure proper mechanical mounting (cf. Chap. A.3, ceramic input capacitors of the USMC prototype). This corresponds approximately to the achievable fill factor of

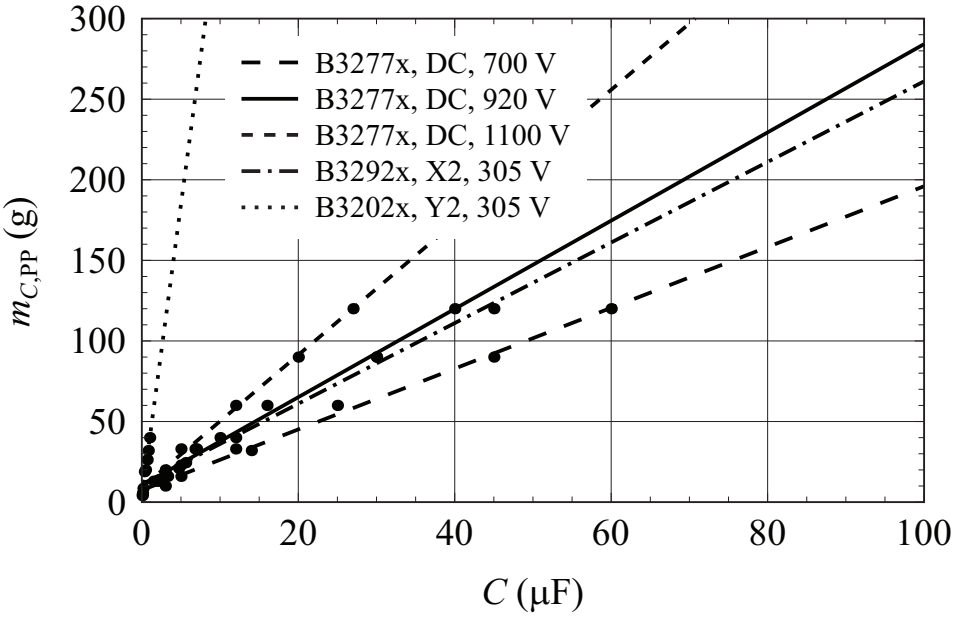


Fig. 6.3: Weight versus capacitance of polypropylene (PP) foil dc-link, X2, and Y2 capacitors from EPCOS at $T_{\mathrm{op}} = 85°\mathrm{C}$.

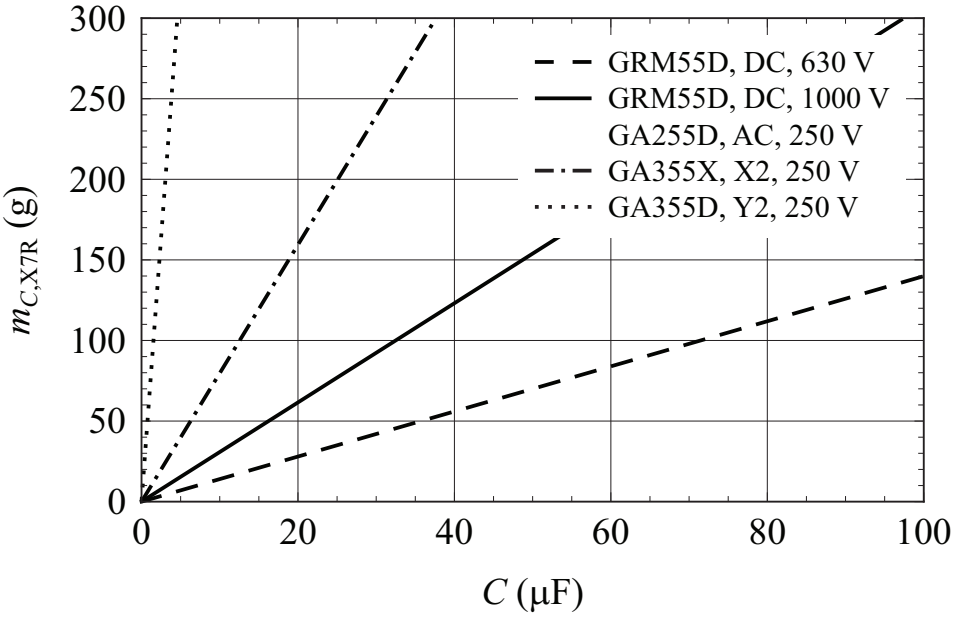


Fig. 6.4: Weight versus capacitance of X7R ceramic dc-link, ac, X2, and Y2 capacitors from Murata at $T_{\mathrm{op}} = 85°\mathrm{C}$.

commercially available pre-stacked chip capacitor assemblies. By comparing Fig. 6.1 with Fig. 6.2 and Fig. 6.3 with Fig. 6.4, it can be seen that X7R ceramic capacitors generally enable a more compact imple-

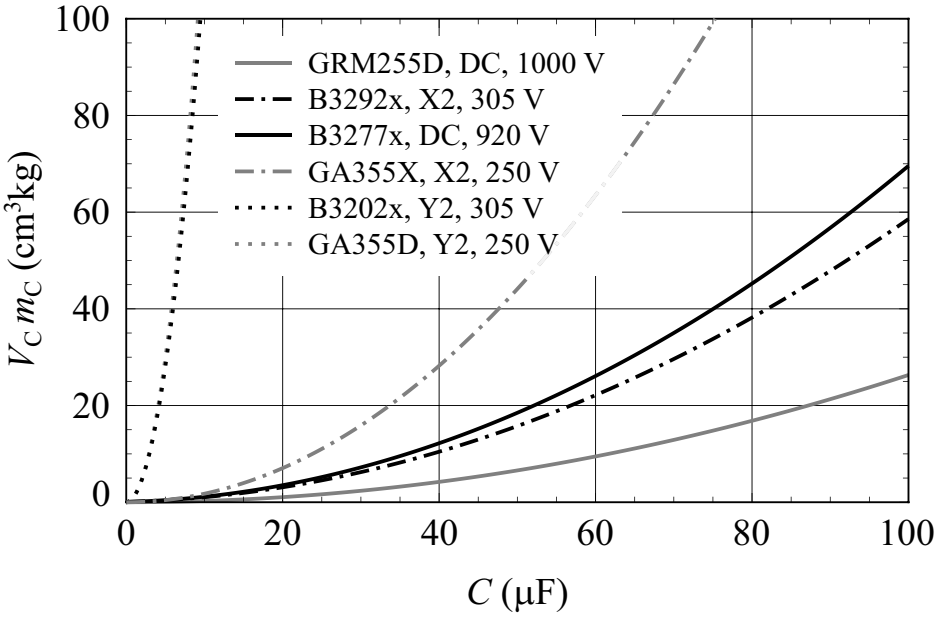


Fig. 6.5: Product of volume and weight of polypropylene foil capacitors (B3277x-, B3292x-, and B3202x-series, EPCOS) and X7R ceramic capacitors (GRM255- and GA355-series, Murata).

mentation of a given capacitance at the cost of a higher weight compared to polypropylene foil capacitors. In order to find the best compromise between the volume and weight, the product of the capacitor volume V_C and weight m_C is formed and plotted in Fig. 6.5. The evaluation shows that for dc-link capacitors the volume-weight-product of X7R ceramic capacitors is half as large as for polypropylene foil capacitors, whereas for X2 capacitors it is exactly contrariwise. When ceramic capacitors are utilized, it is important to account for the temperature and voltage dependent variations of the capacitance. Ferroelectric Class II

Parameter	*DC-Link*	*EMI Suppression*
Part number	B3277x-series	B3292x-series (X2) B3202x-series (Y2)
Rated voltage at 85°C	920 V	305 V (rms)
Operating temperature	70°C	70°C
Desired useful life	> 100 000 h	> 100 000 h

Tab. 6.2: Specifications for the selected EPCOS capacitors.

dielectrics are sensitive to dc voltages. In all cases, a decrease in the dielectric constant occurs under dc-bias that depends on the number and the thickness of the individual dielectric layers. Basically, the larger the number and thickness of the layers is, the lower is the reduction of the capacitance under dc-bias. For X7R capacitors, the reduction typically varies between 10% to 30% [293]. Consequently, for X2 capacitors, the ceramic X7R dielectric does neither provide an advantage regarding the volume nor regarding the weight. In order to provide an industry oriented converter design, in the comparative evaluation performed in this work only foil capacitors are considered. Therefore, the following considerations are limited to metalized polypropylene foil capacitors.

The volume per capacitance scales with the rated voltage and the surge voltage capability. If the relation between volume and capacitance is evaluated for instance for the dc-link capacitors (B3277x-series, EPCOS), it is found that the volume scales for a given rated voltage linearly with the capacitance and for a given capacitance with the square of the rated voltage, which is proportional to the stored energy.

$$V_{\mathrm{C}}(C,U) \propto C \text{ and } \propto U^2 \tag{6.1}$$

The subsequent relations are all based on single capacitor devices (no parallel connection), which explains why the capacitance value is limited to $40\,\mu$F. As can be seen in Fig. 6.1, the volume of the 920 V dc-link capacitors, which are going to be used for the VSBBC, scales similarly with the capacitance as for the considered X2 capacitors. The resulting scaling between the volume V_{C} and the capacitance, evaluated for an operating temperature T_{op} of 70°C, yields to

$$V_{\mathrm{C}}(C) = k_{1,\mathrm{V_C}} C + k_{2,\mathrm{V_C}} \qquad 0.47\,\mu\mathrm{F} \leq C \leq 40\,\mu\mathrm{F}\ . \tag{6.2}$$

$$k_{1,\mathrm{V_C}} = 2.38 \cdot 10^6 \tfrac{\mathrm{cm}^3}{\mathrm{F}} \qquad k_{2,\mathrm{V_C}} = 6.45\,\mathrm{cm}^3$$

This scaling law is used to determine the volume of the dc-link and X2 capacitors. By utilizing the average density of foil capacitors $\rho_{\mathrm{C,avg}}$, the resulting weight of the capacitors can be calculated.

$$m_{\mathrm{C}}(C) = \rho_{\mathrm{C,avg}} V_{\mathrm{C}}(C) \qquad \rho_{\mathrm{C,avg}} \approx 1.3 \tfrac{\mathrm{g}}{\mathrm{cm}^3} \tag{6.3}$$

The remaining dependencies to be considered are the relation between the capacitor losses, the capacitor lifetime and the capacitance value. The capacitor losses scale with the volume of the dielectric material and

therewith with the capacitance and with the resulting current ripple at a given operating voltage. The resulting total losses can be modeled with an Equivalent Series Resistance (ESR). For the considered polypropylene capacitor technology, the ESR represents the dielectric and the ohmic (skin effect) losses of the metallic contacts. Evaluated for a current ripple frequency of 10 kHz and an operating temperature of 70°C, the ESR of the selected dc-link capacitors can be expressed as

$$ESR_{\mathrm{C_{DC},10k}}(C) = \frac{\tan\delta}{2\pi f C} = k_{1,\mathrm{ESR}} \left(\frac{1}{\mathrm{F}}\, C\right)^{k_{2,\mathrm{ESR}}} \quad . \qquad (6.4)$$
$$2\,\mu\mathrm{F} \leq C \leq 40\,\mu\mathrm{F}$$

$$k_{1,\mathrm{ESR}} = 6.07 \cdot 10^{-4}\,\Omega \qquad k_{2,\mathrm{ESR}} = -1.89 \cdot 10^{-1}$$

In order to meet the lifetime requirements of the dc-link capacitors of at least 100 000 h (cf. Tab. 6.2), the rms current ripple of the dc-link capacitors needs to be limited. The maximum tolerable current ripple, determined for a current ripple frequency of 10 kHz and an operating temperature of 70°C, is then given by

$$I_{\mathrm{C_{DC},rms,10k}}(C) = k_{1,\mathrm{I_{C,10k}}}\, C + k_{2,\mathrm{I_{C,10k}}} \quad 2\,\mu\mathrm{F} \leq C \leq 40\,\mu\mathrm{F}\,. \qquad (6.5)$$

$$k_{1,\mathrm{I_{C,10k}}} = 3.92 \cdot 10^{5}\,\frac{\mathrm{A}}{\mathrm{F}} \qquad k_{2,\mathrm{I_{C,10k}}} = 4.87\,\mathrm{A}$$

For current ripple frequencies different from $f = 10\,\mathrm{kHz}$, the maximum allowable current ripple may be approximated by

$$I_{\mathrm{C_{DC},rms,f'}}(I_{\mathrm{C_{DC},rms,f}}, f, f') \approx I_{\mathrm{C_{DC},rms,f}} \left(\frac{1 + (f\tau_{\mathrm{C}})^2}{1 + (f'\tau_{\mathrm{C}})^2}\right)^{\frac{1}{4}} \quad . \qquad (6.6)$$

Thereby, the time constant τ_{C} is used to model the frequency dependency of the dissipation factor of the capacitor. The progression of τ_{C} can be modeled as a function of the capacitance and the case height h_{C} of the capacitor. The fundamental relations can be found in [291].

$$\tau_{\mathrm{C}}(C, h_{\mathrm{C}}) = \frac{k_{1,\tau_{\mathrm{C}}} h_{\mathrm{C}}^2 + k_{2,\tau_{\mathrm{C}}} h_{\mathrm{C}} + k_{3,\tau_{\mathrm{C}}}}{C} + k_{4,\tau_{\mathrm{C}}} \qquad (6.7)$$

$$k_{1,\tau_{\mathrm{C}}} = 1.12 \cdot 10^{-12}\,\frac{\mathrm{Fs}}{\mathrm{mm^2}} \qquad k_{2,\tau_{\mathrm{C}}} = -6.77 \cdot 10^{-11}\,\frac{\mathrm{Fs}}{\mathrm{mm}}$$
$$k_{3,\tau_{\mathrm{C}}} = 1.08 \cdot 10^{-9}\,\mathrm{F\,s} \qquad k_{4,\tau_{\mathrm{C}}} = 2.59 \cdot 10^{-5}\,\mathrm{s}$$

$$h_{\mathrm{C_{DC/X2}}}(C) = \begin{cases} \text{If } 2\,\mu\text{F} \leq C < 9.5\,\mu\text{F} & 31.5\,\text{mm} \\ \text{If } 9.5\,\mu\text{F} \leq C < 25\,\mu\text{F} & 41.5\,\text{mm} \\ \text{If } 25\,\mu\text{F} \leq C \leq 40\,\mu\text{F} & 57.5\,\text{mm} \end{cases} \tag{6.8}$$

For polypropylene X2 capacitors of typical input filters, the resulting losses are significantly lower than for an equally sized dc-link capacitor in a VSBBC as the voltage respectively the current ripple of the input filter capacitors is low. The losses are mainly determined by the reactive currents generated by the mains voltage and are uncritical for 50 / 60 Hz applications. An exception is provided by the input filter capacitors $C_{\mathrm{F,inp}}$ of the MC and the input and output filter capacitors $C_{\mathrm{F,inp}}$ and $C_{\mathrm{F,out}}$ of the CSBBC as they absorb block-shaped (switched) currents. The resulting series resistance of the considered X2 capacitors is approximately two to three times larger than for dc-link capacitors of equal capacitance.

$$R_{\mathrm{S,C_{X2}}}(C) = k_{1,\mathrm{R_{S,X2}}} \left(\frac{1}{\mathrm{F}}\, C \right)^{k_{2,\mathrm{R_{S,X2}}}} \qquad 0.47\,\mu\text{F} \leq C \leq 40\,\mu\text{F} \tag{6.9}$$

$$k_{1,\mathrm{R_{S,X2}}} = 1.97 \cdot 10^{-4}\,\Omega \qquad k_{2,\mathrm{R_{S,X2}}} = -3.69 \cdot 10^{-1}$$

By using (6.9) and the dissipation factor for polypropylene, the resulting ESR of the X2 capacitors can be approximated by

$$ESR_{\mathrm{C_{X2}}}(C, f) \approx R_{\mathrm{S,C_{X2}}}(C) + \frac{\tan(\delta_{\mathrm{D}})}{2\pi f C}\,. \tag{6.10}$$

$$0.47\,\mu\text{F} \leq C \leq 40\,\mu\text{F} \qquad \tan(\delta_{\mathrm{D}}) = 2 \cdot 10^{-4}$$

In terms of a worst case estimation, this has to be considered together with (6.5) as a constraint for the X2 input filter capacitors of the MC and the input and output filter capacitors of the CSBBC. An additional important constraint for the X2 capacitors is given by the maximum admissible voltage rise and fall time, which is inversely proportional to the lead spacing of the capacitor case. The physical reason is that the block-shaped foil capacitor structure can be compared with an LC (line) network. The wider the lead spacing is, the larger is the capacitor block and thus the parasitic inductance. In order to ensure that the whole capacitor structure can homogeneously absorb the a voltage variation, the rate of change of the voltage has to be reduced with increasing capacitance (capacitor volume). With reference to [291], the maximum

time derivation of the capacitor voltage for the selected X2 capacitors is limited to

$$\left|\frac{du_{\mathrm{C}}(C)}{dt}\right|_{\max} \leq k_{1,\mathrm{du_C}} C + k_{2,\mathrm{du_C}} \sqrt[3]{C} + k_{3,\mathrm{du_C}} \; . \tag{6.11}$$

$$0.47\,\mu\mathrm{F} \leq C \leq 40\,\mu\mathrm{F}$$

$$k_{1,\mathrm{du_C}} = 2.30 \cdot 10^6 \frac{\mathrm{V}}{\mathrm{F}\mu\mathrm{s}} \qquad k_{2,\mathrm{du_C}} = -8.91 \cdot 10^3 \frac{\mathrm{V}}{\sqrt[3]{\mathrm{F}}\mu\mathrm{s}}$$
$$k_{3,\mathrm{du_C}} = 2.52 \cdot 10^2 \frac{\mathrm{V}}{\mu\mathrm{s}}$$

Finally, the resonance frequency of the X2 capacitors needs to be modeled to derive a second-order impedance equivalent of the capacitors for the EMI input filter design. The resonance frequency can then be calculated as

$$f_{\mathrm{res_{X2}}}(C) = k_{1,\mathrm{f_{res}}} \left(\frac{1}{\mathrm{F}}\, C\right)^{k_{2,\mathrm{f_{res}}}} + k_{3,\mathrm{f_{res}}} \; . \tag{6.12}$$

$$k_{1,\mathrm{f_{res}}} = 19.73\,\mathrm{Hz} \qquad k_{2,\mathrm{f_{res}}} = 8.37 \cdot 10^{-1}$$
$$k_{3,\mathrm{f_{res}}} = 6.59 \cdot 10^4\,\mathrm{Hz}$$

The Y capacitors have a marginal impact on the filter volume as the maximum allowable capacitance is limited by the specified current in the Protective Earth (PE) conductor and is small compared to the required DM input capacitors. Assuming a maximum tolerable PE current of $I_{\mathrm{CM,Y,max}} \leq 3\,\mathrm{mA}$ (residential application), for a $400\,\mathrm{V}\,/\,50\,\mathrm{Hz}$ mains system, the maximum Y capacitance value is then limited to

$$C_{\mathrm{Y,tot,max}} \leq \frac{I_{\mathrm{CM,Y,max}}}{2\pi U_1 f_1} = 41.5\,\mathrm{nF} \; . \tag{6.13}$$

By inspection of the curves in Fig. 6.1, this Y capacitance value hardly contributes to the overall filter volume and is accounted for with a default volume of $8.5\,\mathrm{cm}^3$. Thereby it is assumed that the total Y capacitance is implemented with 18 identical 2.2 nF capacitors, in order to provide enough degree-of-freedom for the placement of the capacitors.

The second-order impedance equivalent of the capacitors equals to

$$\underline{Z}_{\mathrm{C}}(T,f) = \frac{1}{j2\pi f C(T,f)} + j2\pi f ESL_{\mathrm{C}}(T) + ESR_{\mathrm{C}}(T,f) \; . \tag{6.14}$$

The dielectric leakage resistance (modeled in parallel to C) can be neglected for the considered frequency range. The equivalent series inductance ESL_{C} typically varies within 5 nH to 25 nH and is adopted from manufacturer data sheets.

6.1.2 Differential Mode Inductors

DM inductors are required to implement the boost inductors of the VSBBC, the dc-link inductor(s) of the CSBBC, and obviously the DM filter inductors of all topologies. In this comparison, gapped amorphous tape-wound C-core inductors (comparable with gapped toroidal cores) and toroidal powder core inductors are considered. They provide a good compromise between achievable inductance per volume, ac and dc magnetization properties. Additionally, these inductors feature a soft saturation curve, which is desirable regarding the converter control. The materials selected are the amorphous core alloy Powerlite 2605SA1 from Metglas and the powder core alloys High Flux HF 60, and Molypermalloy MPP 60, manufactured by Magnetics. A summary of the core material data including the intended application of the individual materials is provided in Tab. 6.3

Parameter	*2605SA1*	*MPP 60*	*HF 60*
Manufacturer	Metglas	Magnetics	Magnetics
Core shape	$2 \times$ C	Toroidal	Toroidal
Saturation flux density	1.56 T	0.75 T	1.5 T
Density	$7.2\,\mathrm{g/cm^3}$	$8.0\,\mathrm{g/cm^3}$	$7.6\,\mathrm{g/cm^3}$
Relative core loss at			
$\hat{B} = 0.1\,\mathrm{T},\ f = 10\,\mathrm{kHz}$	$28\,\mathrm{mW/cm^3}$	$16\,\mathrm{mW/cm^3}$	$78\,\mathrm{mW/cm^3}$
$\hat{B} = 0.1\,\mathrm{T},\ f = 50\,\mathrm{kHz}$	$0.31\,\mathrm{W/cm^3}$	$0.16\,\mathrm{W/cm^3}$	$0.56\,\mathrm{W/cm^3}$
Application	L_{B}, L_{DC}	L_{B}, L_{DC}	L_{DM} (filter)
Switching frequency	$< 20\,\mathrm{kHz}$	$> 20\,\mathrm{kHz}$	–
Conductor	Multi-wire	Single-wire	Single-wire
Winding structure	Multi-layer	Single-layer	Single-layer

Tab. 6.3: Core material and inductor parameter overview.

The main inductor parameters are the inductance at zero current $L_{\mathrm{DM},0}$, the inductance at the peak current value L_{DM} and the rms inductor current $I_{\mathrm{L,rms}}$ at a given frequency and temperature. Based on these quantities, the inductors are designed such that the desired DM inductance L_{DM} is provided at the peak inductor current $\hat{I}_{\mathrm{L}} = \sqrt{2} I_{\mathrm{L,rms}}$ and the inductance value drops at the peak current to $\gamma_\mu = 80\%$ of its initial value at zero current. This inductor design enables at a minimal input voltage (nominal voltage -20%) an inductance of typically 60% of $L_{\mathrm{DM},0}$. The main steps in the DM inductor design process are exemplarily shown for the toroidal input filter inductors (HF 60 powder cores) and can be summarized as follows.

The core data are extracted from the manufacturer data sheets to generate a core data base. The start value of the wire diameter d_{w} (current conducting cross section) is selected such that a maximum rms current density $J_{\mathrm{w,max}}$ of $8\,\mathrm{A/mm^2}$ results, whereby an insulation coating thickness of $d_{\mathrm{ct}}/2 = 0.05\,\mathrm{mm}$ is assumed. In order to minimize the parasitic winding capacitance, only single-layer designs are considered. The maximum number of turns $N_{\mathrm{L,max}}$ for a core with an inner diameter d_{i} is then given by

$$N_{\mathrm{L,max}} = \frac{\pi}{\gamma_{\mathrm{w}}} \left(\frac{\sqrt{\pi J_{\mathrm{w}}}\, d_{\mathrm{i}}}{2\sqrt{I_{\mathrm{L,rms}}} + \sqrt{\pi J_{\mathrm{w}}}\, d_{\mathrm{ct}}} - 1 \right) , \tag{6.15}$$

whereas γ_{w} accounts for the spacing between the individual wires. The required effective core cross section A_{core} can be expressed by the flux linkage equation

$$A_{\mathrm{core}} = \frac{\hat{I}_{\mathrm{L}} L_{\mathrm{DM}}}{\mu_0 \mu_{\mathrm{r,ini}} \gamma_\mu H_{\mathrm{max}}(f, \gamma_\mu \mu_{\mathrm{r,ini}})\, N_{\mathrm{L}}} \tag{6.16}$$

$$\gamma_\mu = 80\% \qquad \mu_{\mathrm{r,ini}} = 60$$

and is used by substituting N_{L} with (6.15) to find the smallest core. The inductance at zero current and at the peak current for the selected core can be calculated to

$$L_{\mathrm{DM},0}(\hat{I}_{\mathrm{L}}, N_{\mathrm{L}}) = A_{\mathrm{L},0}(f) \cdot N_{\mathrm{L}}^2 \tag{6.17}$$

$$L_{\mathrm{DM}}(\hat{I}_{\mathrm{L}}, N_{\mathrm{L}}) = A_{\mathrm{L}}(\hat{I}_{\mathrm{L}}, f) \cdot N_{\mathrm{L}}^2 \tag{6.18}$$

and is utilized to verify, on whether the analytically found design fulfills the requirements.

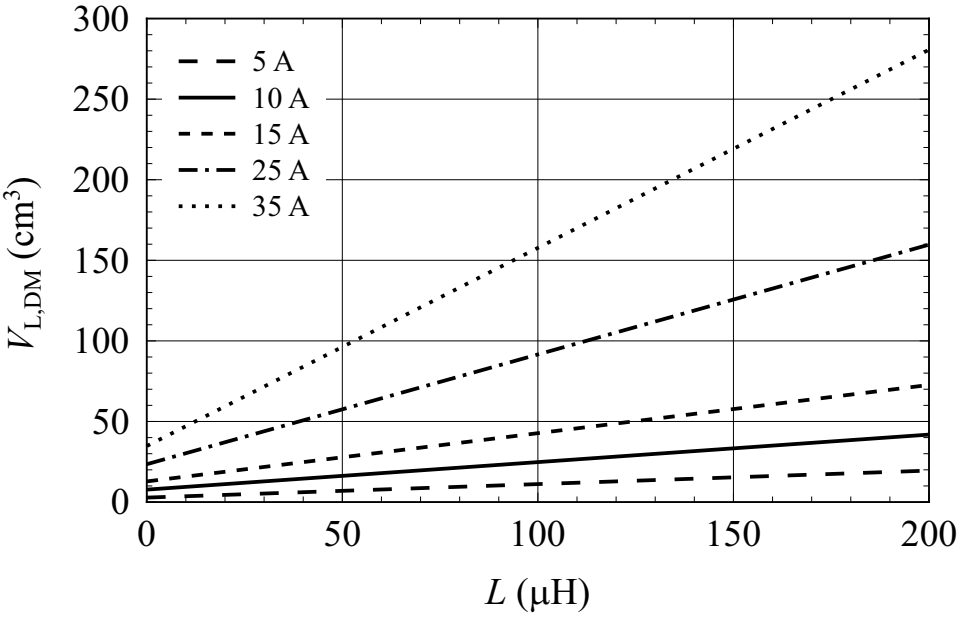


Fig. 6.6: Volume versus inductance of single-layer, toroidal DM filter inductors based on High Flux 60 core material (Magnetics) that are utilized for the DM inductors of the EMI input filter.

In analogy to the capacitors, the inductor volume scales for a given peak current approximately linearly with the inductance and for a given inductance approximately with the square of the peak current, which again corresponds to the stored energy.

$$V_{\mathrm{L_{DM}}}(\hat{I}_{\mathrm{L}}, L) \propto L \text{ and } \propto \hat{I}_{\mathrm{L}}^2$$

The resulting relation between the boxed inductor volume and the inductance of toroidal HF 60 cores is depicted in Fig. 6.6 as a function of the peak inductor current and can be expressed as

$$\begin{aligned} V_{\mathrm{L_{DM}}}(\hat{I}_{\mathrm{L}}, L) = & \\ & \left(k_{1,\mathrm{V,L_{DM}}} \hat{I}_{\mathrm{L}}^2 + k_{2,\mathrm{V,L_{DM}}} \hat{I}_{\mathrm{L}} + k_{3,\mathrm{V,L_{DM}}}\right) L + \\ & \left(k_{4,\mathrm{V,L_{DM}}} \hat{I}_{\mathrm{L}}^2 + k_{5,\mathrm{V,L_{DM}}} \hat{I}_{\mathrm{L}} + k_{6,\mathrm{V,L_{DM}}}\right) . \end{aligned} \tag{6.19}$$

$$\begin{aligned} k_{1,\mathrm{V,L_{DM}}} &= 8.32 \cdot 10^2 \, \tfrac{\mathrm{cm}^3}{\mathrm{A^2H}} & k_{2,\mathrm{V,L_{DM}}} &= 4.91 \cdot 10^3 \, \tfrac{\mathrm{cm}^3}{\mathrm{AH}} \\ k_{3,\mathrm{V,L_{DM}}} &= 3.84 \cdot 10^4 \, \tfrac{\mathrm{cm}^3}{\mathrm{H}} & k_{4,\mathrm{V,L_{DM}}} &= 3.12 \cdot 10^{-3} \, \tfrac{\mathrm{cm}^3}{\mathrm{A^2}} \\ k_{5,\mathrm{V,L_{DM}}} &= 9.42 \cdot 10^{-1} \, \tfrac{\mathrm{cm}^3}{\mathrm{A}} & k_{6,\mathrm{V,L_{DM}}} &= -2.02 \, \mathrm{cm}^3 \end{aligned}$$

For the above scaling factors $k_{i,\mathrm{V,L_{DM}}}$, the inductance value and the

peak inductor current are restricted to

$$\hat{I}_\mathrm{L} L = [50 \ldots 4000]\,\mathrm{A}\mu\mathrm{H} \qquad \hat{I}_\mathrm{L} = [5 \ldots 35]\,\mathrm{A}\,.$$

The corresponding scaling factors for the MPP 60 and Powerlite 2605SA1 core material are compiled in Tab. 6.4.

The ratio between the weight of the core material and the copper wire within the boxed inductor volume $V_{\mathrm{L_{DM}}}$ is not constant. The weight of the inductor thus can be estimated by using an average density $\rho_{\mathrm{L_{DM},avg}}$.

$$\begin{aligned} m_{\mathrm{L_{DM}}}(\hat{I}_\mathrm{L}, L) &= \rho_{\mathrm{L_{DM},avg}} V_{\mathrm{L_{DM}}}(\hat{I}_\mathrm{L}, L) \\ \rho_{\mathrm{L_{DM},avg}} &\approx 3.0 \tfrac{\mathrm{g}}{\mathrm{cm}^3} \end{aligned} \tag{6.20}$$

The major loop core losses at the mains frequency, referred to as Low-Frequency (LF) core losses, are modeled with the standard Steinmetz equation according to

$$P_{\mathrm{core,LF,L_{DM}}}(\hat{B}, f) = k \cdot \left(\frac{\hat{B}}{\mathrm{T}}\right)^{\alpha} \cdot \left(\frac{f}{\mathrm{Hz}}\right)^{\beta}\,. \tag{6.21}$$

The Steinmetz parameters are summarized in Tab. 6.5. The minor loop core losses due to the current ripple, referred to as High-Frequency (HF) core losses, are more intricate to estimate, as the bias of the core varies with the mains frequency. If the Steinmetz parameters were known as a function of the dc-bias, the HF core losses could be determined by a calculation approach based on the modified Steinmetz equation [294]. However, the Steinmetz parameters are typically only provided for zero dc-bias and sinusoidal excitation. The pragmatic approach, chosen here, is to perform core loss measurements on sample inductors with a square-wave voltage that is generated with a switched bridge-leg. This bridge-leg was implemented with two normally-on 1200 V SiC JFETs to enable switching frequencies of up to 800 kHz at a dc-bus voltage of 600 V. The measurement results prove that for the chosen DM inductor design, the core losses hardly depend on the resulting dc-bias of the minor loop and that the HF core losses can be approximated by the first component of the Fourier-series ($n = 1$) of the resulting flux density.

$$P_{\mathrm{core,HF,L_{DM}}}(\hat{B}, T, f) \approx k \cdot \left[\sum_{i=1}^{n} \left(\frac{\hat{B}_i}{\mathrm{T}}\right)^{\alpha} \cdot \left(\frac{f_i}{\mathrm{Hz}}\right)^{\beta}\right] \tag{6.22}$$

Parameter	*2605SA1*	*MPP 60*	*HF 60*
$k_{1,\mathrm{V},\mathrm{L_{DM}}}$ $\left(\frac{\mathrm{cm}^3}{\mathrm{A^2H}}\right)$	$7.09 \cdot 10^{-5}$	$2.08 \cdot 10^{3}$	$8.32 \cdot 10^{2}$
$k_{2,\mathrm{V},\mathrm{L_{DM}}}$ $\left(\frac{\mathrm{cm}^3}{\mathrm{AH}}\right)$	$1.19 \cdot 10^{-2}$	$-4.23 \cdot 10^{3}$	$4.91 \cdot 10^{3}$
$k_{3,\mathrm{V},\mathrm{L_{DM}}}$ $\left(\frac{\mathrm{cm}^3}{\mathrm{H}}\right)$	$-5.89 \cdot 10^{-2}$	$6.19 \cdot 10^{4}$	$3.84 \cdot 10^{4}$
$k_{4,\mathrm{V},\mathrm{L_{DM}}}$ $\left(\frac{\mathrm{cm}^3}{\mathrm{A^2}}\right)$	$1.44 \cdot 10^{-1}$	$-2.59 \cdot 10^{-2}$	$3.12 \cdot 10^{-3}$
$k_{5,\mathrm{V},\mathrm{L_{DM}}}$ $\left(\frac{\mathrm{cm}^3}{\mathrm{A}}\right)$	-5.90	1.88	$9.42 \cdot 10^{-1}$
$k_{6,\mathrm{V},\mathrm{L_{DM}}}$ (cm^3)	$8.22 \cdot 10^{1}$	-4.70	-2.02
$\rho_{\mathrm{L_{DM}},\mathrm{avg}}$ $\left(\frac{\mathrm{g}}{\mathrm{cm}^3}\right)$	≈ 2.9	≈ 2.9	≈ 3.0
Range of $\hat{I}_\mathrm{L}$ (A)	$5 \ldots 35$	$5 \ldots 35$	$5 \ldots 35$
Range of $\hat{I}_\mathrm{L} L$ (AμH)	$250 \ldots 8000$	$50 \ldots 3000$	$50 \ldots 4000$

Tab. 6.4: Volumetric scaling factors, average density, and range of validity of the considered DM inductors at $8\,\mathrm{A/mm^2}$.

This quasi-linear loss behavior results from the selected core material and the applied inductor design, limiting the variation of the relative permeability in operation to $\gamma_\mu = 80\%$ of its initial value $\mu_{\mathrm{r,ini}}$.

The wire losses can be calculated by means of the wire resistance R_w, which is split into a dc (low-frequency) component $R_{\mathrm{w,DC}}$ and an ac (high-frequency) component $R_{\mathrm{w,AC}}$. Under the assumption that the wire diameter is significantly larger than the skin depth, the resulting wire resistance is approximated by

$$\begin{aligned} R_\mathrm{w}(T, f, l_\mathrm{w}) &= R_{\mathrm{w,DC}} + R_{\mathrm{w,AC}} \\ &\approx \frac{4\, l_\mathrm{w}}{\pi\, d_\mathrm{w}^2} \left(\rho_\mathrm{Cu}(T) + \sqrt{\frac{f\, \rho_\mathrm{Cu}(T)\, \mu_\mathrm{w}}{\pi}} \right) . \end{aligned} \tag{6.23}$$

The temperature dependency of the specific dc resistance of copper ρ_Cu is modeled by

$$\rho_\mathrm{Cu}(T) = \rho_{\mathrm{Cu},20} \left(1 + \alpha_{\mathrm{Cu,T}} \left(T - 20^\circ\mathrm{C}\right)\right) . \tag{6.24}$$

$$\rho_{\mathrm{Cu},20} = 1.76 \cdot 10^{-8}\,\Omega\mathrm{m} \qquad \alpha_{\mathrm{Cu,T}} = 3.9 \cdot 10^{-3}\,\frac{1}{^\circ\mathrm{C}}$$

If not differently specified, the default wire temperature is 20°C. The maximum (worst case) wire temperature is assumed with 100°C for the inductor design.

Parameter	*2605SA1*	*MPP 60*	*HF 60*
$k\ \left(\frac{\mathrm{mW}}{\mathrm{T\,cm^3\,s}}\right)$	$1.38 \cdot 10^{-3}$	$6.40 \cdot 10^{-3}$	$3.39 \cdot 10^{-1}$
α	1.74	2.24	2.56
β	1.51	1.41	1.23

Tab. 6.5: Steinmetz parameters of the considered DM inductor materials for sinusoidal excitation, normalized to $\mathrm{mW/cm^3}$.

It is assumed that the toroidal DM and CM filter inductors are passively cooled, whereas the boost and dc-link inductors are placed in the air flow of the cooling system. For passive cooling, the relation between the average inductor temperature T_L and the total inductor losses $P_\mathrm{L,tot}$ can be expressed as a function of the inductor surface area $A_\mathrm{SF,L}$ and the ambient temperature T_A. The relation between the inductor surface area and the volume for the considered toroidal cores is shown in Fig. 6.7.

$$\begin{gathered} T_\mathrm{L} = R_\mathrm{th,L}(A_\mathrm{SF,L}, \Delta T_\mathrm{LA})\, P_\mathrm{L_{tor},tot} + T_\mathrm{A} \\ \Delta T_\mathrm{LA} = T_\mathrm{L} - T_\mathrm{A} \end{gathered} \tag{6.25}$$

The maximum average inductor temperature is limited to 100°C. The relation between the inductor surface area and the inductor volume for the considered HF 60 DM filter inductors may be written as

$$A_\mathrm{SF,L_{DM}}(\hat{I}_\mathrm{L}, L) = k_{1,\mathrm{A_{SF}}} \left(\frac{V_\mathrm{L_{DM}}}{\mathrm{cm^3}} \right)^{k_{2,\mathrm{A_{SF}}}} + k_{3,\mathrm{A_{SF}}}\ . \tag{6.26}$$

$$\hat{I}_\mathrm{L} L = [50 \ldots 4000]\,\mathrm{A\mu H} \qquad \hat{I}_\mathrm{L} = [5 \ldots 35]\,\mathrm{A}$$

$$\begin{aligned} k_{1,\mathrm{V,A_{SF}}} &= 7.84\,\mathrm{cm^2} & k_{2,\mathrm{V,A_{SF}}} &= 6.03 \cdot 10^{-1} \\ k_{3,\mathrm{V,A_{SF}}} &= -5.84\,\mathrm{cm^2} \end{aligned}$$

For the sake of brevity, a detailed model of the resulting thermal resistance of the DM inductor $R_\mathrm{th,L_{DM}}$ and its surface area is not presented, as different empirical relations are provided by core manufacturers. Based on [295, 296], the thermal resistance of the DM inductors in free air and for a low-profile arrangement is modeled as a function of the inductor surface area and the difference ΔT_LA between the average

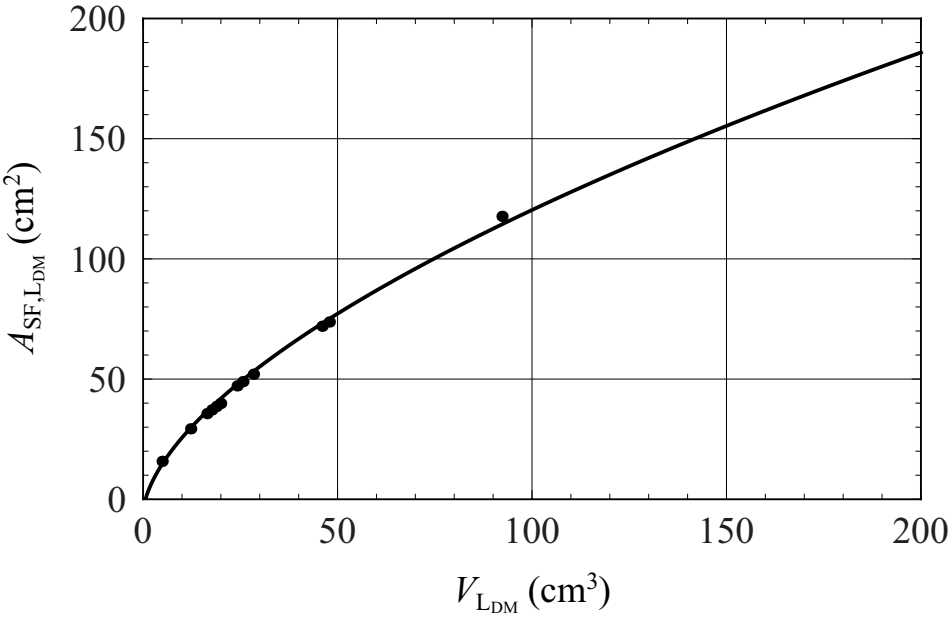


Fig. 6.7: Relation between the surface and the volume of toroidal DM inductors.

inductor temperature and the ambient temperature.

$$R_{\mathrm{th,L_{DM}}}(A_{\mathrm{SF,L_{DM}}}, \Delta T_{\mathrm{LA}}) = \left(k_{1,\mathrm{R_{th,L}}} \Delta T_{\mathrm{LA}} + k_{2,\mathrm{R_{th,L}}}\right) \left(\frac{A_{\mathrm{SF,L_{DM}}}}{\mathrm{cm}^2}\right)^{k_{3,\mathrm{R_{th,L}}}}$$

$$A_{\mathrm{SF,L_{DM}}} = [5 \ldots 200]\,\mathrm{cm}^2 \qquad \Delta T_{\mathrm{LA}} = [10 \ldots 40]\,\mathrm{K} \tag{6.27}$$

$$k_{1,\mathrm{R_{th,L}}} = -5.04 \tfrac{1}{\mathrm{W}} \qquad k_{2,\mathrm{R_{th,L}}} = 6.70 \cdot 10^2 \tfrac{\mathrm{K}}{\mathrm{W}}$$

$$k_{3,\mathrm{R_{th,L}}} = -1.00$$

The impact of the temperature on the lifetime of the considered inductors is significantly less critical compared to capacitors as for the selected cores no temperature sensitive compound material is utilized. A temperature dependent variation of the core parameters is not required as within the considered temperature range from 20°C to 100°C the permeability of the selected core materials changes less than 3%.

The second-order impedance equivalent of the inductors is given by

$$\underline{Z}_{\mathrm{L}}(\hat{I}_{\mathrm{L}}, T, f) = \left(\frac{1}{R_{\mathrm{w}}(T, f) + R_{\mathrm{core,s}}(\hat{I}_{\mathrm{L}}, f) + j2\pi L_{\mathrm{DM}}(\hat{I}_{\mathrm{L}}, f)} + j2\pi f C_{\mathrm{p}} \right)^{-1}. \tag{6.28}$$

The parallel winding capacitance C_p is determined according to [297] or adopted from measurement data. $R_\mathrm{core,s}$ models the core losses at the considered operating point by a series resistance and is calculated based on (6.22).

6.1.3 Common Mode Inductors

For the CM filter inductors, toroidal cores from Vacuumschmelze (VAC) are considered with a tape-wound, nanocrystalline core, which is fabricated of the core material Vitroperm 500 F. The main design parameters of a CM inductor are the impedance $|\underline{Z}|$ (insertion loss) provided at a certain frequency, the CM saturation current and/or the corresponding voltage-time area product, and the rms DM inductor current. In order to minimize the parasitics, again a single-layer winding design is assumed. The main design steps are similar to those shown for the DM inductors and therefore are not presented here. The scaling law for the boxed CM inductor volume, evaluated at 100 kHz, equals to

$$\begin{aligned} V_{\mathrm{L_{CM}}}(\hat{I}_\mathrm{L}, |\underline{Z}|) = \\ \left(k_{1,\mathrm{V},\mathrm{L_{CM}}} \hat{I}_\mathrm{L}^2 + k_{2,\mathrm{V},\mathrm{L_{CM}}} \hat{I}_\mathrm{L} + k_{3,\mathrm{V},\mathrm{L_{CM}}}\right) |\underline{Z}| + \\ \left(k_{4,\mathrm{V},\mathrm{L_{CM}}} \hat{I}_\mathrm{L}^2 + k_{5,\mathrm{V},\mathrm{L_{DM}}} \hat{I}_\mathrm{L} + k_{6,\mathrm{V},\mathrm{L_{CM}}}\right) . \end{aligned} \tag{6.29}$$

$$\begin{aligned} k_{1,\mathrm{V},\mathrm{L_{CM}}} &= 9.78 \cdot 10^{-5} \tfrac{\mathrm{cm}^3}{\mathrm{A}^2\Omega} & k_{2,\mathrm{V},\mathrm{L_{CM}}} &= 7.82 \cdot 10^{-4} \tfrac{\mathrm{cm}^3}{\mathrm{A}\Omega} \\ k_{3,\mathrm{V},\mathrm{L_{CM}}} &= 5.85 \cdot 10^{-5} \tfrac{\mathrm{cm}^3}{\Omega} & k_{4,\mathrm{V},\mathrm{L_{CM}}} &= 1.48 \cdot 10^{-2} \tfrac{\mathrm{cm}^3}{\mathrm{A}^2} \\ k_{5,\mathrm{V},\mathrm{L_{CM}}} &= 5.71 \cdot 10^{-1} \tfrac{\mathrm{cm}^3}{\mathrm{A}} & k_{6,\mathrm{V},\mathrm{L_{CM}}} &= 4.49\,\mathrm{cm}^3 \end{aligned}$$

The peak inductor DM current and CM impedance values for the above scaling factors $k_{i,\mathrm{V},\mathrm{L_{CM}}}$ are limited to

$$\hat{I}_\mathrm{L}\,|\underline{Z}| = [4 \ldots 50]\,\mathrm{A k}\Omega \qquad \hat{I}_\mathrm{L} = [5 \ldots 35]\,\mathrm{A} .$$

The weight of the CM inductor thus can be approximated using an average density $\rho_{\mathrm{L_{CM}},\mathrm{avg}}$. By considering (6.20), it follows that the density of the DM filter inductors is twice the density of the CM filter inductors.

$$\begin{aligned} m_{\mathrm{L_{CM}}}(\hat{I}_\mathrm{L}, |\underline{Z}|) &= \rho_{\mathrm{L_{CM}},\mathrm{avg}} V_{\mathrm{L_{CM}}}(\hat{I}_\mathrm{L}, |\underline{Z}|) \\ \rho_{\mathrm{L_{CM}},\mathrm{avg}} &\approx 1.6 \tfrac{\mathrm{g}}{\mathrm{cm}^3} \end{aligned} \tag{6.30}$$

CM inductors have core losses similar to any other magnetic component. However, for the considered filter topology (cf. Sec. 6.5.2) and

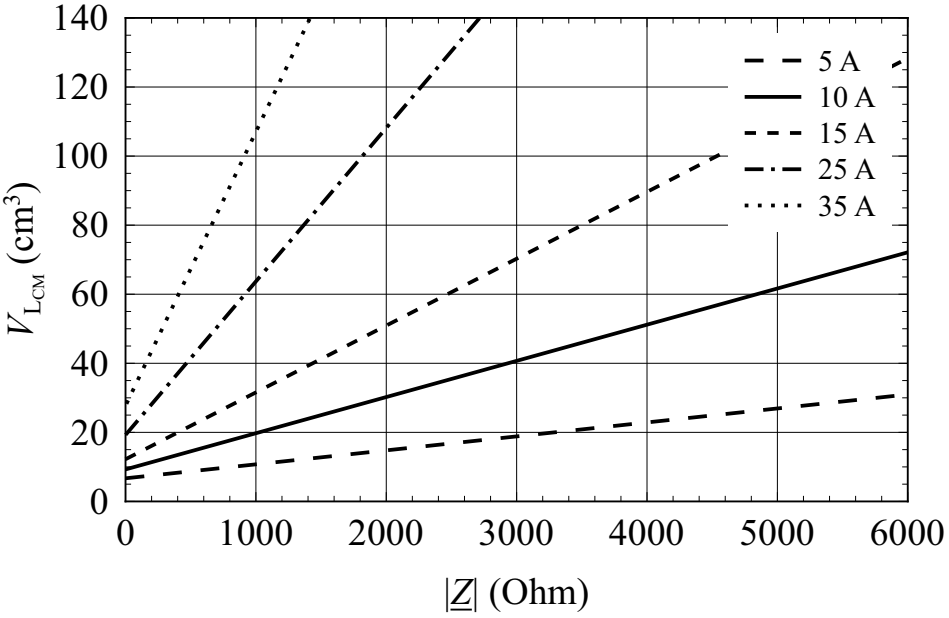


Fig. 6.8: Volume versus impedance of the CM filter inductors based on Vitroperm 500 F core material (Vacuumschmelze).

switching frequency range considered in the comparative evaluation of ac-ac converters, the losses of the CM inductors are dominated by the copper losses, and hence the core losses can be neglected.

For the CM inductors the same second-order impedance equivalent model, according to (6.28), is applied as for the DM inductors.

6.2 Energy Storage

6.2.1 Topological Relations

The internal energy storage is a key feature of a converter system and has to be considered when comparing different converter concepts. Concerning the energy flow, the dc-link capacitor C_{DC} of the VSBBC enables to decouple load variations from the mains input and to absorb the discontinuous (block-shaped) dc-link currents generated by the switching of the input and output stage. In analogy to the VSBBC, the dc-link inductor(s) L_{DC} of the CSBBC decouple load variations from the mains input and absorb the discontinuous dc-link voltages that result from the switching of the input and output stage. Correspondingly, the input capacitors $C_{\mathrm{F,inp}}$ of the MC provide the major energy storage between

the mains and the load and smooth the discontinuous input currents that are impressed by the load. The input capacitors are the key passive components due to the absence of intermediate energy storage that limit the feedback of load changes into the mains and determine the control behavior of a MC system. From a topological view, in MCs the intermediate energy storage of the VSBBC or CSBBC has been shifted to the input filter and the load.

The boost inductors L_{B} of the VSBBC absorb the discontinuous (switched) voltages of the input stage, whereas the input filter capacitors $C_{\mathrm{F,inp}}$ of the MC and CSBBC smooth the discontinuous currents generated by the input stage. Both the boost inductors and the input filter capacitors ultimately enable continuous input currents. For switching frequencies of industrial converter systems, the stored energy in the boost inductors and input filter capacitors is low compared with the stored energy of the dc-link capacitor or dc-link inductor.

In summary, VSBBCs have impressed currents at the input (boost inductors) and output (inductive load). In contrary, CSBBCs have impressed input and output voltages (input and output filter capacitors). MCs, however, require impressed voltages at the input (input capacitors) and impressed currents at the output (inductive load), which again represents the topological relation of its input with a CSR and its output with a VSI.

The input currents have a continuous sinusoidal waveform with a certain distortion level for all four converter topologies. In order to comply to the specified power quality and EMI standards, these remaining distortions have to be attenuated by an EMI input filter, which again provides a certain amount of energy storage by its passive components.

6.2.2 Energy Content of Capacitors and Inductors

Next, the energy content of dc and three-phase ac capacitors and inductors is determined. For dc-link capacitors and inductors, the energy content equals to

$$W_{\mathrm{C_{DC}}} = \frac{1}{2} C_{\mathrm{DC}} U_{\mathrm{DC}}^2 \qquad W_{\mathrm{L_{DC}}} = \frac{1}{2} L_{\mathrm{DC}} I_{\mathrm{DC}}^2 \,. \tag{6.31}$$

Assuming a symmetrical three-phase (input) voltage-current system with a phase voltage U_1 and a phase current I_1, the energy content

of three star-connected filter capacitors C_F and three phase inductors L_F (boost inductors or DM filter inductors) is given by

$$W_{\mathrm{C_F}} = \frac{3}{4} C_\mathrm{F} \hat{U}_1^2 \qquad W_{\mathrm{L_F}} = \frac{3}{4} L_\mathrm{F} \hat{I}_1^2 \,. \tag{6.32}$$

First, the dc-link capacitance of the VSBBC and dc-link inductance of the CSBBC are compared for a given input phase voltage U_1, a dc-link voltage U_DC, and a dc-link current $I_\mathrm{DC} = 2P/(3\hat{U}_1)$ (at maximum modulation index of the CSR), whereby the losses are neglected. Under the assumption of equal dc-link energy storage, the ratio between the dc-link capacitance and dc-link inductance can be calculated to

$$\frac{1}{2} C_\mathrm{DC} U_\mathrm{DC}^2 = \frac{1}{2} L_\mathrm{DC} I_\mathrm{DC}^2 = \frac{1}{2} L_\mathrm{DC} \left(\frac{2\,P}{3\,\hat{U}_1} \right)^2 \tag{6.33}$$

$$\frac{C_\mathrm{DC}}{L_\mathrm{DC}} = \frac{4\,P^2}{9\,\hat{U}_1^2 U_\mathrm{DC}^2} \propto \frac{V_{\mathrm{C_{DC}}}}{V_{\mathrm{L_{DC}}}} \,. \tag{6.34}$$

As can be seen from (6.34), independent of the volumetric scaling factor between the dc-link capacitors and dc-link inductors, for a given mains phase voltage U_1, the higher the converter power, the smaller becomes the dc-link inductor compared with the dc-link capacitor. This is one reason why current-source-type converters are favorably applied for higher power levels. Another interesting aspect is the comparison of the energy storage density of the capacitors utilized for VSBBCs and MCs. By determining the required capacitor volume, using (6.2), it is found that for the considered foil capacitors and an input rms phase voltage of $U_1 = 230\,\mathrm{V}$, the energy storage density in a MC is three-times lower compared to a VSBBC with a typical dc-link voltage of $U_\mathrm{DC} = 700\,\mathrm{V}$.

6.3 Dimensioning of the Passives

6.3.1 Control and Energy Based Criteria

In order to meet the dynamic requirements that are imposed by the load, for all four converter concepts a minimal internal energy storage needs to be provided. For the VSBBC and CSBBC, the energy storage is implemented by the dc-link capacitor C_DC and/or by the dc-link inductor L_DC, whereas for the MC the internal energy storage is mainly

provided by the input capacitors $C_{\mathrm{F,inp}}$. The suggested control based dimensioning criteria are derived and described in Sec. 3.2.4.

DC-Link Capacitor and DC-Link Inductor

The worst case considered for the VSBBC occurs for a step change from nominal motor operation to no-load, which is initiated by the load and therefore cannot be pre-controlled (prevented) by the converter control. In order to limit the relative overshoot of the dc-link voltage $\delta_{\mathrm{u_{DC}}} = \Delta u_{\mathrm{DC}}/U_{\mathrm{DC}}$, a minimal dc-link capacitance is required that can be calculated to

$$C_{\mathrm{DC}} \geq \frac{P_2}{18\,U_{\mathrm{DC}}\delta_{\mathrm{u_{DC}}}\eta^2}\left(\frac{\sqrt{3}\,L_{\mathrm{B}}P_2}{U_1^2\left(\sqrt{2}\,U_1+\frac{U_{\mathrm{DC}}}{\sqrt{3}}\right)}+\frac{36\,\eta}{U_{\mathrm{DC}}f_{\mathrm{sw}}}\right), \tag{6.35}$$

assuming regular sampling and a worst case dead time of two pulse periods ($2\,T_{\mathrm{P}} = 2\,f_{\mathrm{sw}}^{-1}$). The corresponding control based criterion for the dc-link inductance of the CSBBC yields to

$$L_{\mathrm{DC}} \geq \frac{9\,U_1^2\eta}{P_2 f_{\mathrm{sw}}}\,. \tag{6.36}$$

Besides the control based design criterion, the minimal dc-link capacitance may also be determined by an energy based dimensioning guideline, which is typically represented by a capacitance value per output power. The minimum dc-link capacitance of HEVs, for instance, is selected between $5\,\mu$F/kVA to $10\,\mu$F/kVA for typical dc-link voltages and switching frequencies [298]. Energy based criteria are either used to ensure a certain ride-through capability or can be considered as a simplification of (6.35) when the dc-link voltage and the switching frequency remain constant or vary only within a small range as in the above example for HEVs.

Input Capacitors

A similar criterion can be derived for the input capacitors $C_{\mathrm{F,inp}}$ of the MC by considering the input EMI filter (cf. Fig. 6.11). Opposed to the VSBBC, a step change of the load from nominal motor operation to no-load is uncritical regarding over-voltages across the input capacitors, as

the stored energy in the total DM inductance of the second filter stage $L_{\mathrm{DM,2,tot}} = L_{\mathrm{DM,2}} + L_{\mathrm{DM,2,d}}$ is low compared with the energy stored in the capacitors $C_{\mathrm{F,inp}}$. The design relevant operating condition occurs, when the current drawn from the input capacitors $C_{\mathrm{F,inp}}$ is larger than the current supplied to them, and thus the capacitor voltage u_{C} drops. Consequently, also the maximum converter output voltage is reduced, in case the maximum modulation index is already applied. From a control perspective it is hence reasonable to constrain the voltage drop Δu_{C} across the input capacitors. Assuming that the capacitor voltage is in phase with the inductor current $i_{\mathrm{L_{DM,2}}}$ (unity power factor) and a load step is initiated by increasing the q-axis motor current at the output $i_{2\mathrm{q}}$, a voltage drop of the d-axis capacitors voltage u_{Cd} is observed. The voltage drop Δu_{Cd} depends on the DM inductance $L_{\mathrm{DM,2,tot}}$ (forming together with the input filter capacitors a resonant circuit), the input capacitor $C_{\mathrm{F,inp}}$, and the variation of the input current due the variation of the load current. As is shown in Sec. 3.2.4, for mains frequencies of 50 Hz / 60 Hz and typical filter parameters, the voltage drop $\Delta u_{\mathrm{Cd}} = \delta_{\mathrm{u_C}} \hat{U}_1$ across the input capacitors can be calculated to

$$\Delta u_{\mathrm{Cd}} = L_{\mathrm{DM,2,tot}} \frac{di_{1\mathrm{d}}}{dt} \left[\cos\left(\frac{t}{\sqrt{C_{\mathrm{F,inp}} L_{\mathrm{DM,2,tot}}}} \right) - 1 \right] . \tag{6.37}$$

By inspection of (6.37), two cases for the duration of the current rise time t_{rise} have to be distinguished.

$$t_{\mathrm{rise}} < \pi \sqrt{C_{\mathrm{F,inp}} L_{\mathrm{DM,2,tot}}} \quad \text{and} \quad t_{\mathrm{rise}} \geq \pi \sqrt{C_{\mathrm{F,inp}} L_{\mathrm{DM,2,tot}}} \tag{6.38}$$

Typically, the second case is design relevant, and the capacitance of the filter capacitors only indirectly limits the voltage drop Δu_{Cd} across the input filter capacitors with the ratio of $L_{\mathrm{DM,2,tot}}/C_{\mathrm{F,inp}}$ that results from the filter design.

The relative voltage drop is assumed with $\delta_{\mathrm{u_{DC}}} = \delta_{\mathrm{u_{Cd}}} = 10\%$ for both the VSBBC and the MC.

6.3.2 Ripple Based Criteria

DC-Link Capacitor and DC-Link Inductor

The voltage ripple across the dc-link capacitor generally is not a relevant design criterion for the VSBBC, except for converters with a reduced

dc-link capacitance or for two-phase operation. For a center-aligned synchronization of the modulation of the input and output stage of the VSBBC, an input rms phase voltage of $U_1 = 230\,\mathrm{V}$, and a dc-link voltage of $U_{\mathrm{DC}} = 700\,\mathrm{V}$, the maximum rms dc-link capacitor current equals to

$$I_{\mathrm{C_{DC}},\mathrm{rms},\mathrm{max}} \approx 0.60 \cdot \hat{I}_2 \tag{6.39}$$

for a maximum modulation index of the output stage $M_2 = 1$ and a phase displacement at the output of $\Phi_2 = 0$.

Similar to the VSBBC, also for the CSBBC the dc-link inductor is mostly dimensioned based on the control performance or the stored energy, whereby the maximum current ripple is considered as a subordinate design criterion. However, for CSBBCs that operate at high switching frequencies in order to minimize the volume of the dc-link inductor [299], the dc-link current ripple becomes design relevant. The required dc-link inductance for the considered modulation scheme to limit the maximum peak-to-peak dc-link current ripple to

$$\Delta i_{\mathrm{L_{DC}},\mathrm{pp},\mathrm{max}} = \delta_{\mathrm{i_L},\mathrm{pp}}\, I_{\mathrm{DC}} \tag{6.40}$$

can be calculated to

$$L_{\mathrm{DC}} = \frac{3\left(2-\sqrt{3}\right)\hat{U}_1}{4\, I_{\mathrm{DC}} f_{\mathrm{sw}} \delta_{\mathrm{i_L},\mathrm{pp}}}\,. \tag{6.41}$$

Thereby, it is assumed that the modulation of the input and output stage is again center-aligned sychronized.

Boost Inductors

The boost inductors L_{B} of the VSBBC are designed based on the current ripple at the switching frequency. In this comparison they are dimensioned for a maximum peak-to-peak current ripple $\Delta i_{\mathrm{L_B},\mathrm{pp},\mathrm{max}}$ of $\delta_{\mathrm{i_L},\mathrm{pp}} = 20\%$ of the input current amplitude $\hat{I}_1$.

$$\Delta i_{\mathrm{L_B},\mathrm{pp},\mathrm{max}} = \delta_{\mathrm{i_L},\mathrm{pp}}\, \hat{I}_1 \tag{6.42}$$

$\delta_{\mathrm{i_L},\mathrm{pp}}$ typically varies within 5% to 40% depending on the converter system and the application area. The inductance value of the boost inductors can be calculated as follows.

$$L_{\mathrm{B}} = \frac{1}{\hat{I}_1 f_{\mathrm{sw}} \delta_{\mathrm{i_L},\mathrm{pp}}} \left(\hat{U}_1 - \frac{3\,\hat{U}_1^2}{2\, U_{\mathrm{DC}}} \right) \tag{6.43}$$

Input and Output Capacitors

In analogy to the boost inductors of the VSBBC, the input and output filter capacitors $C_{\mathrm{F,inp}}$ and $C_{\mathrm{F,out}}$ of the CSBBC are dimensioned for a maximum peak-to-peak voltage ripple. Besides the control based dimensioning criterion, also for the MC the voltage ripple across the input capacitors at the switching frequency needs to be considered.

In order to enable safe operation, the maximum peak-to-peak voltage ripple $\Delta u_{\mathrm{C_F,pp}}$ across the input and output filter capacitors should be limited to $\delta_{\mathrm{u_{C,pp}}} = 20\%$ of the input voltage amplitude $\hat{U}_1$ and output voltage amplitude $\hat{U}_2$, respectively and can be calculated to

$$\text{CSBBC:} \qquad C_{\mathrm{F,inp/out}} = \frac{I_{\mathrm{DC}}}{4\,\hat{U}_1 f_{\mathrm{sw}} \delta_{\mathrm{u_C,pp}}} \tag{6.44}$$

$$\text{MC:} \qquad C_{\mathrm{F,inp}} = \frac{\hat{I}_2}{4\,\hat{U}_1 f_{\mathrm{sw}} \delta_{\mathrm{u_C,pp}}} \; . \tag{6.45}$$

The switching frequency f_{sw} in the above equation for the MC refers to the switching frequency of the output stage when considering the IMC. The maximum voltage ripple across the input capacitors is is obtained for $\Phi_2 = 0$ for the considered modulation scheme.

Compared with the current ripple in boost inductors, the voltage ripple across the input capacitors of the CSBBC and MC has a stronger impact on the operating behavior of the converter, since the voltage measurement signal directly affects the modulation, or even determines the commutation sequence as in the case of the CMC. Therefore, in this comparison, the maximum ripple $\Delta u_{\mathrm{C,pp,max}}$ is limited to $\delta_{\mathrm{u_C,pp}} = 10\%$ of the input voltage amplitude.

In analogy to the dc-link capacitor, ultimately, also for the input capacitor $C_{\mathrm{F,inp}}$ of the MC (main energy storage), the current loading is determined. For the selected modulation schemes of the CMC and IMC, the maximum rms current $I_{\mathrm{C_F,rms,max}}$ of the input capacitors occurs at two-third of the maximum modulation index and $\Phi_2 = 0$ and equals to

$$I_{\mathrm{C_F,rms,max}} \approx 0.41 \cdot \hat{I}_2 \; . \tag{6.46}$$

6.4 Power Quality

6.4.1 Standards

The motivation for power quality standards is to limit the harmonic current injection from individual loads into the supplying mains, in order to avoid unacceptable voltage distortion levels and to define and limit the overall harmonic distortion of the mains voltage provided by the utility (power supplier). The essential standards are EN50160, IEC 61000 (IEC 61000-3-4), IEEE 519, IEEE 1159, UL 1741, and DO-160D for airborne equipment.

IEEE 519, for instance, suggests a shared responsibility between the power supplier and the consumer for controlling the harmonic voltage and current levels. The power supplier has to control the harmonic voltage distortion (cf. Tab. 6.6), whereas the consumer has to ensure that the current harmonics injected at the Point of Common Coupling (PCC) are within given limits.

The two important figures for assessing the input power quality of a switched power electronic converter system are the Total Harmonic Distortion (THD) or the Total Demand Distortion (TDD). For the input current I_1, the THD and the TDD are defined as follows.

$$THD_{\mathrm{I_1}} = \frac{\sqrt{\sum_{h=2}^{h=\infty} I_{1,(h)}^2}}{I_{1,(1)}} \tag{6.47}$$

$$TDD_{\mathrm{I_1}} = \frac{\sqrt{\sum_{h=2}^{h=\infty} I_{1,(h)}^2}}{I_{1,\mathrm{dem}}} \tag{6.48}$$

Opposed to the THD, the TDD is referred to the 15 or 30 minutes average maximum demand current (in this case the maximum demand input current $I_{1,\mathrm{dem}}$). The limits should be applied for the worst case under normal operation. Tab. 6.7 summarizes the recommended current distortion limits for a bus voltage between 120 V and 69 kV, whereby I_{SC} equals to the available short circuit current at the PCC.

Compared to the IEEE 519, the IEC 61000-3-4 standard does not only define limits for the individual equipment but for the whole system installation.

Bus Voltage at PCC	*Individual Voltage Distortion* (%)	Maximum Voltage *THD* (%)
$\leq 69\,\mathrm{kV}$	3.0%	5.0%
$115\,\mathrm{kV} \ldots 161\,\mathrm{kV}$	1.5%	2.5%
$\geq 161\,\mathrm{kV}$	1.0%	1.5%

Tab. 6.6: Recommended voltage distortion limits for different bus voltage levels according to IEEE 519.

Parameter	$\frac{I_{\mathrm{SC}}}{I_{1,\mathrm{dem}}} < 20$	$\frac{I_{\mathrm{SC}}}{I_{1,\mathrm{dem}}} < 20 \ldots 50$	$\frac{I_{\mathrm{SC}}}{I_{1,\mathrm{dem}}} < 50 \ldots 100$
$h < 11$	4.0	7.0	10.0
$11 \leq h < 17$	2.0	3.5	4.5
$17 \leq h < 23$	1.5	2.5	4.0
$23 \leq h < 35$	0.6	1.0	1.5
$35 \leq h$	0.3	0.5	0.7
TDD	5.0	8.0	12.0

Tab. 6.7: Recommended current distortion limits for a general distribution system ($120\,\mathrm{V} \ldots 69\,\mathrm{kV}$) according to IEEE 519.

According to the IEEE 519 standard, the maximum voltage THD for low-voltage mains systems is limited to 5%. Assuming an ohmic behavior of the load, the same distortion level is found for the input current. For this purpose, the design goal for the four investigated ac-ac converters is to limit the total harmonic distortion of the the input current to $\leq 5\%$.

6.4.2 THD Measurement

With state-of-the-art power analyzers, mains frequencies of up to 2.5 kHz can be tracked with the integrated PLL circuits. This high fundamental frequency tracking capability is required for aircraft power systems with a nominal mains frequency range of 400 Hz to 800 Hz to provide an adequate resolution for the FFT calculation.

For standard 50 Hz/60 Hz mains systems, the THD is typically determined up to the hundredth harmonic (5 kHz/6 kHz) of the fundamental

frequency. This harmonic range is also considered for the THD calculations and measurements performed in this work.

6.4.3 THD and Switching Frequency

The input current THD requirements can be utilized to determine the suitable (maximum) switching frequency for a given mains frequency f_1. For converter systems with an active rectifer input stage (PFC), as considered, the higher the switching frequency f_{sw}, the more input current vectors $N_{\vec{\mathrm{I}}_1}$ can be formed per mains period $T_1 = f^{-1}$.

$$N_{\vec{\mathrm{I}}_1} = \frac{f_{\mathrm{sw}}}{f_1} \tag{6.49}$$

The higher the switching frequency, the lower is the number of different possible duty cycle values N_{PWM} due to the digital implementation of the PWM generators with a finite clock frequency $f_{\mathrm{Clk,PWM}}$.

$$N_{\mathrm{PWM}} = \frac{f_{\mathrm{Clk,PWM}}}{f_{\mathrm{sw}}} \tag{6.50}$$

A suitable switching frequency regarding the THD can be found when $N_{\vec{\mathrm{I}}_1}$ equals to N_{PWM}, assuming that the digital control is executed every pulse period $T_{\mathrm{P}} = f_{\mathrm{sw}}^{-1}$. By equalizing (6.49) and (6.50) and solving for f_{sw}, the searched switching frequency $f_{\mathrm{sw,THD}}$ can be calculated to

$$\frac{f_{\mathrm{sw}}}{f_1} = \frac{f_{\mathrm{Clk,PWM}}}{f_{\mathrm{sw}}} \tag{6.51}$$

$$f_{\mathrm{sw,THD}}(f_1, f_{\mathrm{sw}}) = \sqrt{f_1 f_{\mathrm{Clk,PWM}}}\ . \tag{6.52}$$

Evaluated for a mains frequency of 50 Hz, 400 Hz, and 800 Hz leads to

$$f_{\mathrm{sw,THD,50Hz}} = 70.7\,\mathrm{kHz} \tag{6.53}$$

$$f_{\mathrm{sw,THD,400Hz}} = 200.0\,\mathrm{kHz} \tag{6.54}$$

$$f_{\mathrm{sw,THD,800Hz}} = 282.3\,\mathrm{kHz}\ . \tag{6.55}$$

The PWM clock frequency $f_{\mathrm{Clk,PWM}}$ is assumed with 100 MHz for the above calculation as is used in the hardware prototypes. This corresponds to an absolute PWM resolution of 10 ns.

The maximum switching frequency for the comparative evaluation of the ac-ac converters is selected with $f_{\mathrm{sw,max}} = 72\,\mathrm{kHz}$ based on (6.53).

6.5 EMI Input Filter

6.5.1 EMI Standards

In this work EMC standards, that are published by the International Special Committee on Radio Interference CISPR, are considered, which have also been adopted by the IEC. The most important documents are the CISPR 11, the CISPR 16, and the CISPR 22 standard. The CISPR 11 standard defines the disturbance voltage limits for Conducted Emissions (CE), the CISPR 16 the measurement equipment and setups, and the CISPR 22 the measurement data processing.

The emissions limits for drive systems, investigated in this thesis, are typically defined in the product specific standard EN 61800-3. As shown in [300], this standard comprises two different sets of disturbance limits for industrial drives. The limits are identical to CISPR 11 Class B, whereas the second limits depend on the branch of industry and on the agreement among manufacturers. This second set of limits often leads to a relaxation of the allowable disturbance levels compared to the ones of the CISPR 11 Class A. Consequently, in practice the disturbance limits defined in CISPR 11 are also valid for ac drive systems and thus can be applied for the EMI filter design of ac-ac converter systems.

According to CISPR 11, Group 1 contains all Industrial, Scientific, and Medical (ISM) equipment and appliance in which there is intentionally generated and/or used conductively coupled radio-frequency energy which is necessary for the functioning of the equipment.

Frequency (MHz)	*Class A* (dB/μV)		*Class B* (dB/μV)	
	Quasi-peak	Average	Quasi-peak	Average
0.15 ... 0.5	79	66	66 ... 56[a]	56 ... 46[a]
0.5 ... 5	73	60	56	46
5 ... 30	73	60	60	50

[a] Linearly decreasing with logarithm of frequency

Tab. 6.8: Mains terminal (conducted emission) disturbance voltage limits for Class A and Class B Group 1 ISM equipment according to CISPR 11 (fourth edition, 2003-03).

Class A refers to equipment suitable for use in all establishments other than domestic and those directly connected to a low-voltage mains supply which supplies buildings used for domestic purposes. Consequently, Class A equipment is intended for use in an industrial environment. Class B equipment is equipment suitable for use in domestic establishments and in establishments directly connected to a low-voltage mains supply which supplies buildings for domestic purposes. The considered Class A and Class B disturbance voltage limits for the conducted emission are summarized in Tab. 6.8. A detailed description of the different EMC standards, the measurement data processing, and the required measurement equipment can be found in [300] (Chap. 1 and Chap. 2).

It should be noted that in this work only the CE disturbance levels within the frequency range of 150 kHz to 30 MHz are considered, which is defined by the EMC standards.

6.5.2 EMI Input Filter Design

Impact Factors

The EMI input filter design is a multi-dimensional design problem. The main factors impacting the filter design in dependency of the frequency are depicted in Fig. 6.9.

The input filter should allow for a highly efficient power transfer at the mains frequency with a minimal voltage-to-current phase lag and meet the specified CE EMI and power quality standards. Additionally, in order to avoid oscillations that could occur at resonance (corner) frequencies of the input filter above the converter input current control bandwidth and/or around the switching frequency, passive damping has to be provided. In the frequency range of the input current control bandwidth, filter resonances should be avoided. If this is not possible, active damping concepts have to be implemented. An overview of active damping strategies for input filters is provided in [301].

Filter Topology

Fig. 6.10 shows the corner frequencies for a one-, two-, and three-stage LC EMI input filter, providing all an attenuation of 100 dB at 150 kHz. Thereby, it is assumed that the corner frequencies of the two-stage filter ($f_{\mathrm{c},2}$) and the three-stage filter ($f_{\mathrm{c},3}$) are each identical. Regarding

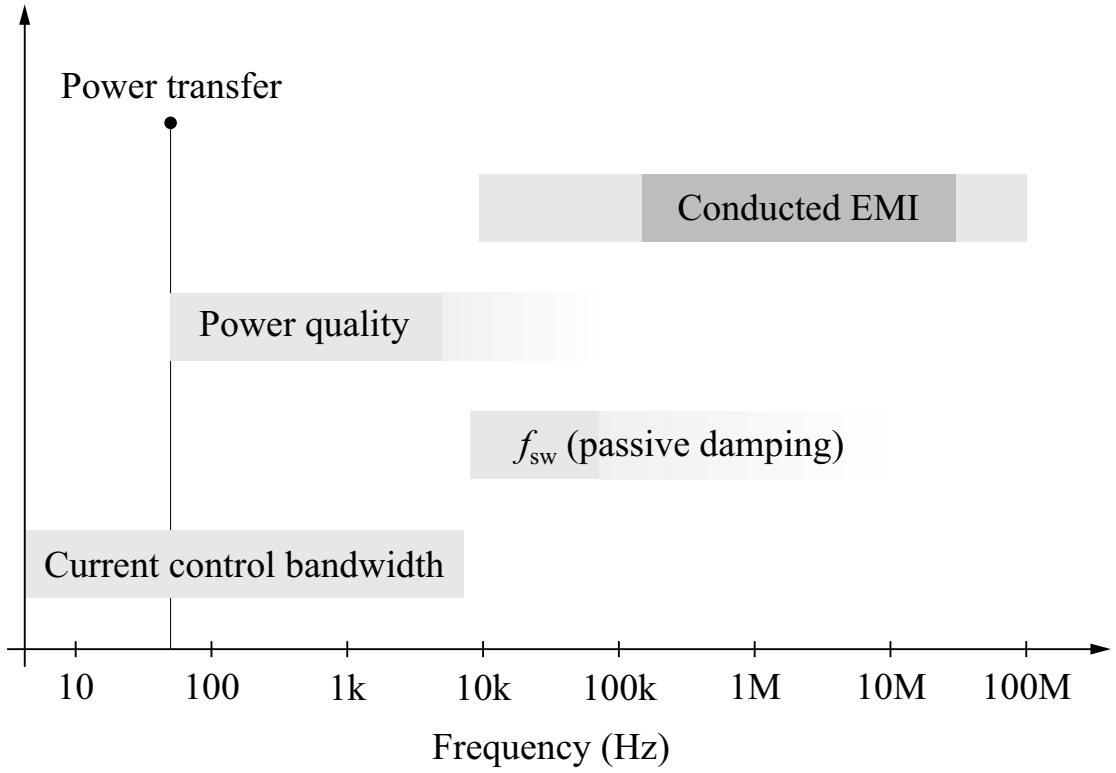


Fig. 6.9: Main impact factors on the EMI input filter design in dependence of the frequency with increasing priority on the ordinate.

the resulting filter volume the three-stage filter leads to the most compact filter solution, which can be immediately seen by considering the attenuation $Att_{\mathrm{LC},1}$ of a single LC filter (single-stage filter).

$$Att_{\mathrm{LC},1}(\omega) = 20 \cdot \lg\left(\frac{1}{|1-\omega^2 CL|}\right) \propto 20 \cdot \lg\left(\frac{\omega_{\mathrm{c},1}}{\omega}\right)^2 \tag{6.56}$$

$$\omega_{\mathrm{c},1} = \frac{1}{\sqrt{CL}}$$

As can be seen in (6.56), the filter attenuation is proportional to ω^{-2}. Correspondingly, for a three-stage LC filter with identical corner frequencies, the filter attenuation is proportional to ω^{-6}. The product of C and L of the three-stage filter is smaller compared to that of the single-stage filter for an equal filter attenuation

$$CL\big|_{\text{3-stage}} = \sqrt[3]{CL}\big|_{\text{1-stage}} \tag{6.57}$$

and thus enables a more compact implementation. However, under the assumption of equal (or similar) corner frequencies of all filter stages,

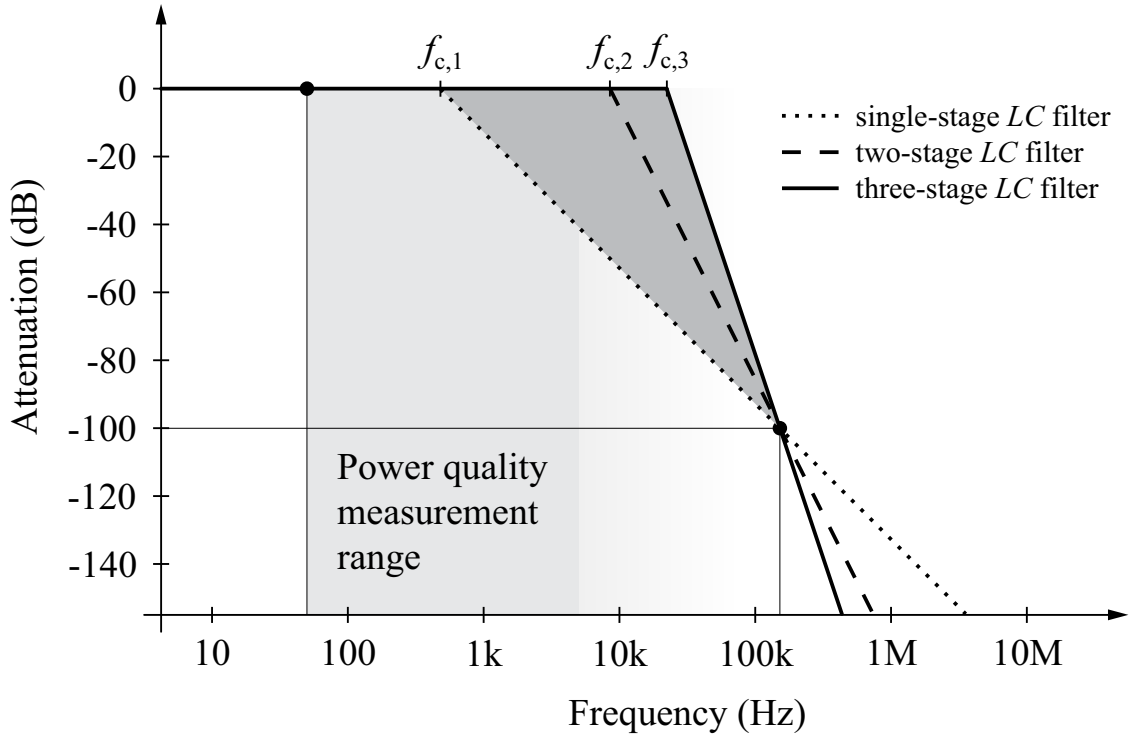


Fig. 6.10: Corner frequencies $f_{c,i}$ of a one-, two-, and three-stage LC input filter to obtain an attenuation of 100 dB at 150 kHz, assuming identical corner frequencies for the two- and three-stage filter each.

the disadvantage of a three-stage filter is that no attenuation can be provided in the lower frequency range which is relevant for power quality (cf. Fig. 6.10). This means that the specified power quality standards together with the selected switching frequency f_{sw} leads to a limitation of the number of input filter stages and additionally defines the selection of the individual corner frequencies. The gray shaded triangle in Fig. 6.10 represents the available optimization area for the EMI input filter design with respect to power quality and input impedance requirements for a maximum number of three LC filter stages. (Example: For a MC with a switching frequency above 100 kHz and a maximum electrical output frequency of 2 kHz, it is assumed that load variations occur at 1 kHz. These periodic load variations are transfered to the converter input and impair the input current quality if the corner frequencies of the input filter are selected above 1 kHz.)

Although different advanced filtering concepts have been presented for ac-ac converters, as for instance in [302] for the CMC, in this comparison a conventional multi-stage LC filter topology is applied, in order

to establish comparability with commercial EMI filters. The considered filter topology is presented in Fig. 6.11. $C_{\mathrm{DM},1}$ corresponds to the input filter capacitors $C_{\mathrm{F,inp}}$ of the CSBBC, CMC, or IMC. The boost inductors L_{B} of the VSBBC (not shown here) are connected to the terminals a_1, b_1, and c_1 and represent the DM filtering inductors $L_{\mathrm{DM},1}$ of the input filter. The protection devices (e.g. varistors) are not shown. This consideration simplifies the modeling of the DM and CM noise sources. The corner frequencies of the individual filter stages are selected differently. Only the last capacitor stage ($C_{\mathrm{DM},1}$) is equipped with bleeding (discharging) resistors R_{b}.

The main attenuation is provided with the first two DM and CM stages. The third capacitor stage $C_{\mathrm{DM},3}$ together with the (DM) leakage inductance $L_{\mathrm{CM,2,lk}}$ of $L_{\mathrm{CM},2}$ is utilized to suppress the HF-noise above 5 MHz and thus hardly contributes to the overall volume. If possible $L_{\mathrm{DM},2}$ is implemented with the leakage inductance $L_{\mathrm{CM,1,lk}}$ of $L_{\mathrm{CM},1}$.

6.5.3 Filter Design Procedure

Main Steps

The first step in the filter design is to investigate the parameter variations of the passive components. The A_{L}-value respectively the permeability of the considered High Flux HF 60 DM inductor material varies within ±8%. For the Vitroperm 500 F material, which is utilized for the CM inductors, a permeability variation of +45%/−25% is specified. The variation of the capacitance for the considered polypropylene foil capacitor technologies is limited to ±10%. These parameter variations provide a natural physical limitation for the optimization and minimization of passive components in general and particularly for EMI input filters.

In the following, the specified nominal values are adopted for the calculation models, whereas the component variations are utilized to determine the minimal design margin of the filter attenuation. Thus, for the DM filter attenuation, a minimal margin of +3.3 dB and for the CM filter attenuation a minimal margin of +6.8 dB is required. An additional safety margin of 3 dB is added in this comparison. The resulting filter design margins is set to 6 dB for the DM attenuation and 10 dB for the CM attenuation. The actual difference of the noise spectrum of the individual converter topologies has a minor impact on

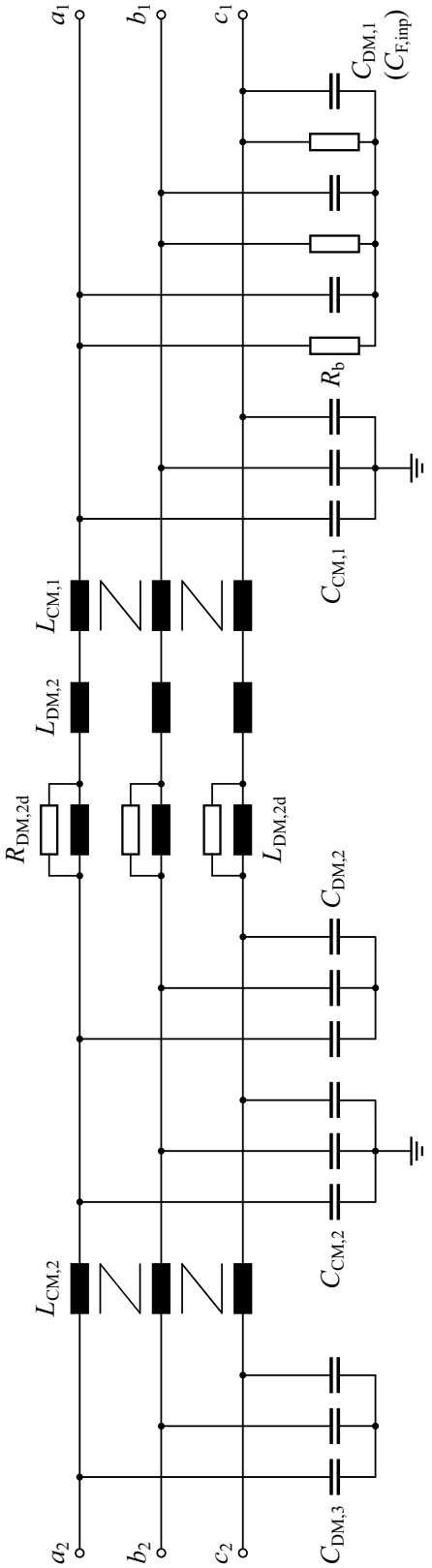


Fig. 6.11: Considered multi-stage input EMI filter topology.

the resulting filter size due to the variation of the filter component parameters. Assuming a difference of the DM noise level of 50% just corresponds to the DM filter design margin.

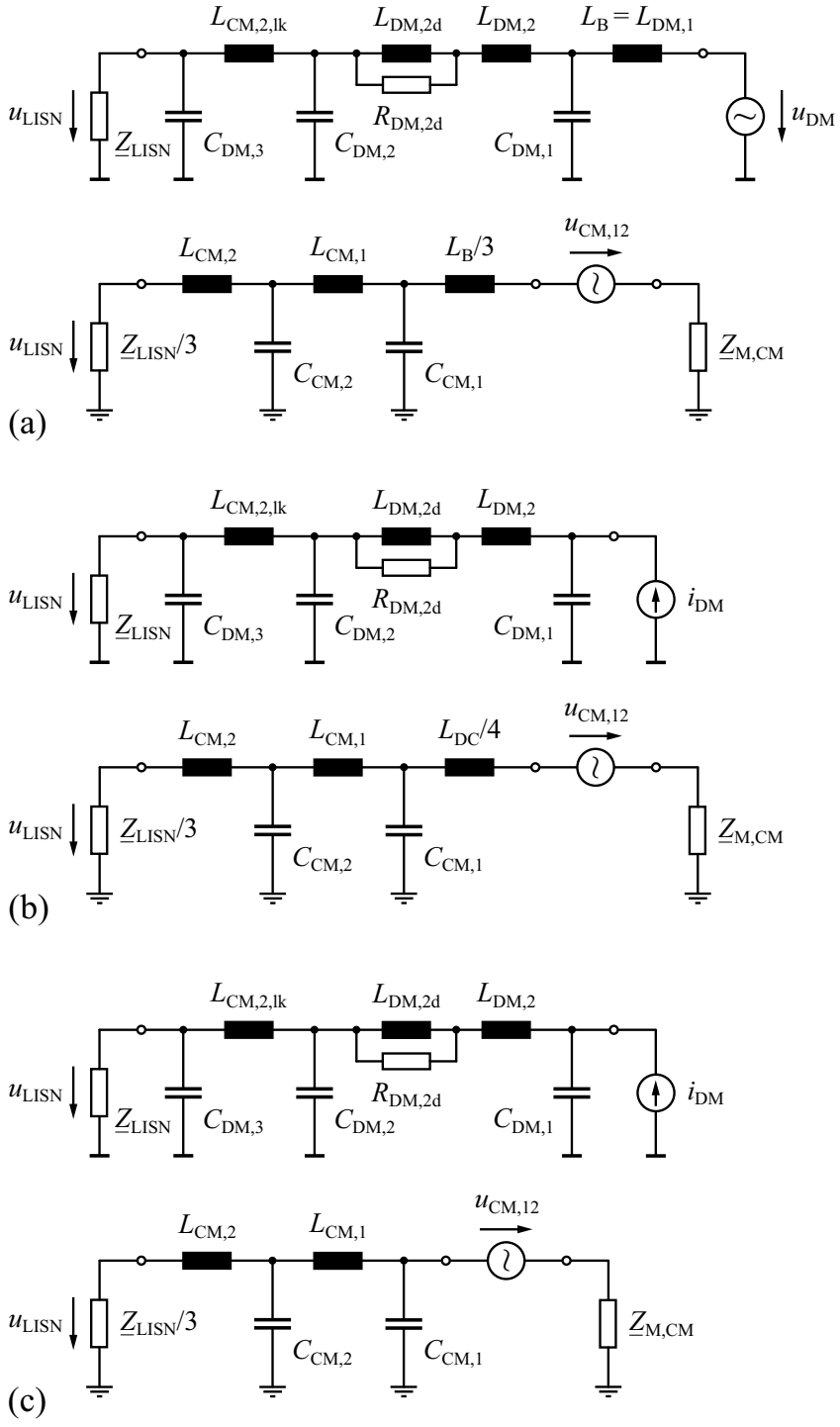


Fig. 6.12: Simplified DM and CM equivalent circuits for **(a)** the VSBBC, **(b)** the CSBBC, and **(c)** the MC (CMC or IMC).

The next step is to design the input capacitors $C_{\mathrm{F,inp}}$ and boost inductors L_{B} according to the ripple, control performance, and energy based criteria defined in Sec. 6.3. Therewith, all three converter topologies are operational, and the required filter attenuation can be calculated. The filters are designed for nominal converter operation to meet the CISPR 11 Class A or B Quasi-Peak (QP) level for conducted emission (cf. Tab. 6.8). The required simplified DM and CM equivalent circuits are depicted in Fig. 6.12. The dc-link inductance L_{DC} of the CSBBC is equally split between the positive and the negative dc-bus, leading to a resulting dc-link CM inductance of $L_{\mathrm{DC}}/4$.

The resulting DM and CM noise sources i_{DM}, u_{DM}, and $u_{\mathrm{CM,12}}$ are analytically calculated with the modulation functions derived in Sec. 3.1. $u_{\mathrm{CM,12}}$ represents the resulting equivalent CM voltage between the converter input and output and may be calculated to

$$u_{\mathrm{CM,12}} = \frac{u_{\mathrm{1a,0}} + u_{\mathrm{1b,0}} + u_{\mathrm{1c,0}}}{3} - \frac{u_{\mathrm{2A,0}} + u_{\mathrm{2B,0}} + u_{\mathrm{2C,0}}}{3} \,. \tag{6.58}$$

$u_{\mathrm{1a,0}}$, $u_{\mathrm{1b,0}}$, and $u_{\mathrm{1c,0}}$ are the voltages between the connecting nodes of the input phases to the bridge-legs of the input stage and ground (cf. Fig. 3.16). Correspondingly, $u_{\mathrm{2A,0}}$, $u_{\mathrm{2B,0}}$, and $u_{\mathrm{2C,0}}$ indicate the voltage between the connecting nodes of the output phases to the bridge-legs of the output stage and ground. The CM voltages at the converter input and output are actually calculated relative to the voltage midpoint of the converter. However, when the difference between these CM voltages is formed to determine $u_{\mathrm{CM,12}}$, the midpoint voltage cancels, and $u_{\mathrm{CM,12}}$ can be directly calculated with reference to ground according to (6.58).

The actual filter design is performed with a custom developed, automated filter design software, implemented in MATLAB, that incorporates the filter transfer function, the second-order equivalents of the passive components, and models of the whole CE measurement setup. A detailed description of the CE measurement chain can be found in [300] and is not repeated here for the sake of brevity. It consists of the following main components:

- the Line Impedance Stabilizing Network (LISN)
- the test receiver,
- the power converter (DUT), which is supplied from the LISN, and
- the load (motor).

In this case the LISN for the required three-phase converter is implemented with three single-phase LISNs. The DM impedance of each of the considered $50\,\Omega/50\,\mu$H LISNs is given by

$$\underline{Z}_{\mathrm{LISN}} = \frac{\omega^2 C_{\mathrm{LISN}} L_{\mathrm{LISN}} R_{\mathrm{term}} - j\omega L_{\mathrm{LISN}}}{\omega^2 C_{\mathrm{LISN}} C_{\mathrm{LISN}} - 1 - j\omega C_{\mathrm{LISN}} R_{\mathrm{term}}} \,. \tag{6.59}$$

$$C_{\mathrm{LISN}} = 250\,\mathrm{nF} \quad L_{\mathrm{LISN}} = 50\,\mathrm{nH} \quad R_{\mathrm{term}} = 50\,\Omega$$

Correspondingly, the three-phase CM impedance of the LISN can be determined by paralleling the three LISNs.

For the DM filter design, the impact of the load is marginal and is neglected. However, for the CM filter design, a second-order equivalent of the CM impedance $\underline{Z}_{\mathrm{M,CM,HF}}$ of the motor load is used. The impedance is parameterized based on measurement results of a PMSM (LST-series, LTi Drives) including a 3 m long motor cable.

$$\underline{Z}_{\mathrm{M,CM,HF}} = \frac{1}{j2\pi C_{\mathrm{M,CM,HF}}} + j2\pi f L_{\mathrm{M,CM,HF}} + R_{\mathrm{M,CM,HF}} \tag{6.60}$$

$$C_{\mathrm{M,CM,HF}} = 2\,\mathrm{nF} \quad L_{\mathrm{M,CM,HF}} = 435\,\mathrm{nH} \quad R_{\mathrm{M,CM,HF}} = 2.1\,\Omega$$

The impedance parameters are valid within the frequency range of 100 kHz to 8 MHz, which is required for the high-frequency CM filter design. In order to ensure that the CM inductors do not saturate in the frequency range of the electrical input and output frequency of the converter, a low-frequency equivalent CM impedance of the load $\underline{Z}_{\mathrm{M,CM,LF}}$ is required. For the considered load setup, it is given by

$$\underline{Z}_{\mathrm{M,CM,LF}} \approx \frac{1}{j2\pi C_{\mathrm{M,CM,LF}}} + R_{\mathrm{M,CM,LF}} \,. \tag{6.61}$$

$$C_{\mathrm{M,CM,LF}} = 6\,\mathrm{nF} \quad R_{\mathrm{M,CM,LF}} = 0.4\,\Omega$$

The parasitic capacitance to the heat sink (grounded) per unit area (cm^2) of the considered semiconductor module assembly can be approximated by

$$C'_{\mathrm{SM,PE}} \approx 20 \frac{\mathrm{pF}}{\mathrm{cm}^2} \,. \tag{6.62}$$

By comparing the load impedance data of $\underline{Z}_{\mathrm{M,CM,HF}}$ and $\underline{Z}_{\mathrm{M,CM,LF}}$ with $C'_{\mathrm{PM,PE}}$ justifies the omission of this capacitance in the derived DM and CM equivalents in Fig. 6.12.

The DM noise of the CMC and IMC are identical for the considered modulation schemes, and the CM noise spectrum mainly differs in the low-frequency range at multiples of the input and output frequencies. Thus, it is sufficient to consider the EMI filter requirements for MCs in general.

Filter Volume Optimization

The remaining question is on how to optimally design the individual filter stages in order to obtain a compact EMI filter. The degrees-of-freedom for the CM filter design are restricted due to the limitation of the maximum Y2 capacitance (cf. Sec. 6.1.1). Thus, for all converter topologies the same inductor is utilized for $L_{\mathrm{CM},1}$, and a total CM capacitance of 40 nF is implemented. The difference in the required CM attenuation is compensated with the second inductor $L_{\mathrm{CM},2}$. Consequently, the overall filter volume can mainly be minimized by an adequate design of the DM filter stages with regard to the volumetric scaling factors of the capacitors and inductors. The basic principle can be best explained by considering the corner frequency $f_{\mathrm{c,DM}}$ of a single LC filter stage (e.g. $C_{\mathrm{DM},2}$ and $L_{\mathrm{DM},2}$ in Fig. 6.11).

$$f_{\mathrm{c,DM}} = \frac{1}{2\pi\sqrt{C\,L}} \tag{6.63}$$

The lower the corner frequency, the higher is the filter attenuation. The linkage between the total filter volume $V_{\mathrm{F,tot}}$ and the attenuation can be established by expressing the capacitance and inductance value as a function of the component volume.

$$C = \frac{V_{\mathrm{C}}}{\gamma_{\mathrm{V,C}}} \qquad L = \frac{V_{\mathrm{L}}}{\gamma_{\mathrm{V,L}}} \qquad \gamma_{\mathrm{V,LC}} = \frac{\gamma_{\mathrm{V,L}}}{\gamma_{\mathrm{V,C}}} \tag{6.64}$$

By substituting C and L in (6.63) with (6.64), the corner frequency is then given by

$$\begin{aligned} f_{\mathrm{c,DM}} &= \frac{1}{2\pi\sqrt{\frac{V_{\mathrm{C}}}{\gamma_{\mathrm{V,C}}}\frac{V_{\mathrm{L}}}{\gamma_{\mathrm{V,L}}}}} = \frac{1}{2\pi\sqrt{\frac{V_{\mathrm{C}}}{\gamma_{\mathrm{V,C}}}\frac{V_{\mathrm{F,tot}}-V_{\mathrm{C}}}{\gamma_{\mathrm{V,L}}}}} \\ &= \frac{\gamma_{\mathrm{V,C}}}{2\pi}\sqrt{\frac{\gamma_{\mathrm{V,LC}}}{V_{\mathrm{C}}\left(V_{\mathrm{F,tot}}-V_{\mathrm{C}}\right)}}\,. \end{aligned} \tag{6.65}$$

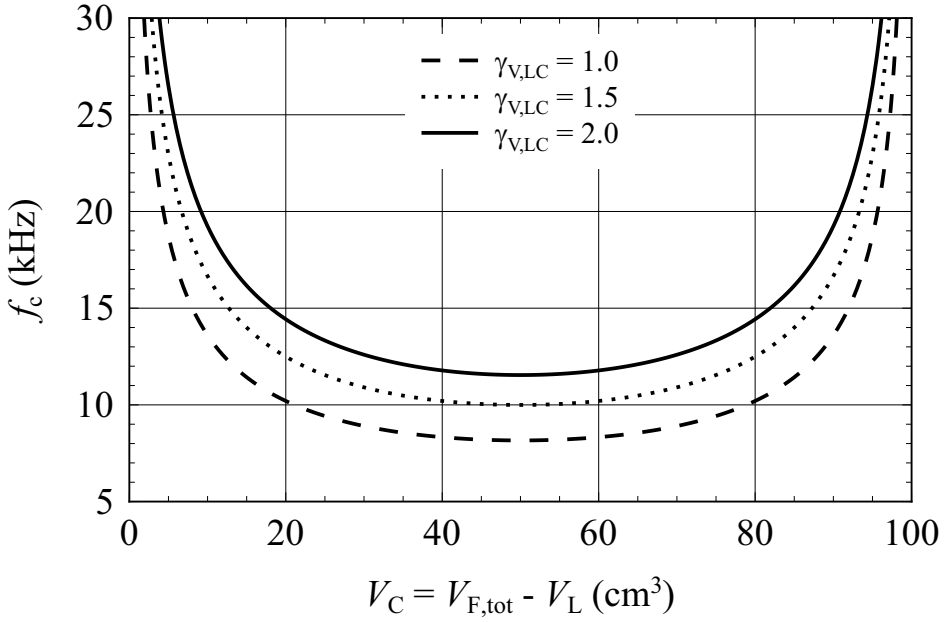


Fig. 6.13: Corner frequency f_c of an LC filter for different partitioning of the total allowable filter volume of 100 cm^3 between capacitors and inductors.

$f_{c,DM}$ is minimum and thus the attenuation is maximum for

$$V_{C,opt} = V_{L,opt} = \frac{V_{F,tot}}{2} \,. \tag{6.66}$$

In other words, independent of the volumetric scaling $\gamma_{V,LC}$ between the capacitors and inductors, the maximum attenuation of a single LC filter stage at a minimal filter volume is achieved if one half of the total filter volume is utilized for the capacitors and the other half for the inductors. The absolute value of the filter attenuation evidently varies depending on $\gamma_{V,LC}$, however, the criterion of optimality remains invariant. This is a well-known result of the optimization problem, where the product of two factors (in this case $V_C/\gamma_{V,C} \cdot V_L/\gamma_{V,L}$) is maximized under the constraint that the sum of the two factors is limited ($V_{F,tot} = V_C + V_L$). This optimization approach was suggested in [298] for optimizing the drive train of an electric vehicle. The same design guideline can also be applied for maximizing the attenuation and minimizing the weight of an LC filter stage. In Fig. 6.13, the resulting corner frequency is plotted versus the partitioning of the capacitor and inductor volume for different scaling factors between the inductor volume and its inductance and the volumetric scaling of capacitors provided in (6.2). The minimum of the

corner frequency is flat and always occurs at $V_C = V_L = V_{F,tot}/2$, as shown in Fig. 6.13.

It is important to note that the above design guidelines are not sufficient for an optimal filter design. The implemented filter design algorithm additionally ensures that

- the filter resonances do neither occur at the switching frequency nor at the beginning of the EMI measurement range at 150 kHz,
- passive damping according to [303] is provided for the resonances above the current control bandwidth of the converter,
- the output impedance of the filter is minimized (i.e. in a multistage filter the higher the value of a DM capacitor stage is, the closer it is placed at the converter input terminals),
- the lifetime based loading limits of the passive components (cf. Sec. 6.1.1) are fulfilled,
- the total reactive power of the filter including the input capacitors (C_F) is below 15% of the nominal converter output power, and
- a nominal efficiency of the EMI input filter of at least 99.6% is achieved.

Special attention is directed to the sizing of the input filter capacitors $C_{F,inp}$ of the MC in order to fulfill the requirements for the input power factor. For that purpose, in the above filter design algorithm the total reactive power of the input filter is limited to 15% of the nominal converter output power $P_{2,nom}$. With reference to (3.98) the desired maximum voltage-to-current displacement angle $\Phi^*_{1,max}$ at the input of the MC can be varied for a practical implementation within $-25°$ to $25°$ in order to limit the reduction of the output voltage to 90% of the maximum output voltage. This design guideline enables to provide unity input power factor down to a minimum output power $P_{2,\Phi_1=1,min}$ of one third of the nominal output power.

$$P_{2,\Phi_1=1,min} = \frac{0.15\, P_{2,nom}\eta}{\tan\left(\Phi^*_{1,max}\right)} \approx 0.31 \cdot P_{2,nom} \qquad \eta = 95\% \qquad (6.67)$$

6.5.4 Limitations of the Suggested EMI Modeling

It is important to briefly discuss the limitations of the considered EMI modeling approach. The applied filter design algorithm uses second-order equivalents of the passive components (cf. (6.14) and (6.29)). However, the resulting filter impedance within the EMI measurement frequency range from 150 kHz to 30 MHz is not only determined by the first-order approximation of the filter components, but obviously also depends on the PCB layout (parasitics) and the radiated electromagnetic coupling between the individual components, as shown in Fig. 6.14.

If the simulated CE noise levels of the implemented hardware prototypes are compared with the EMI measurement results, deviations between the predicted (simulated) and measured noise levels are typically observed for frequencies above several MHz [304]. One reason is that in this frequency range the interaction of the filter components with the PCB parasitics start having an impact on the resulting filter impedances. By inspection of the implemented filter PCB layouts, it is found that the maximum parasitic board capacitances are limited to $C_{\mathrm{PCB,max}} \approx 50\,\mathrm{pF}$. The parasitic capacitance between the

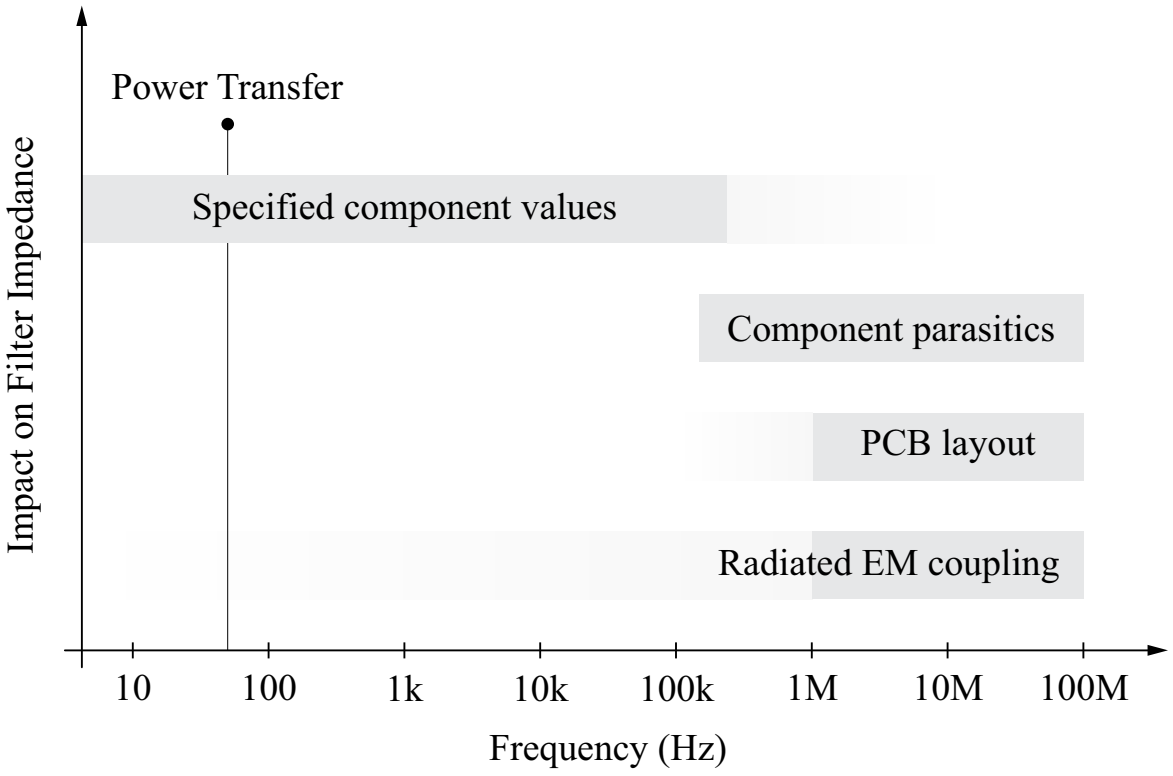


Fig. 6.14: Main impact factors on the input filter impedance in dependence of the frequency with increasing priority on the ordinate.

individual copper layers of a standard 4-layer PCB are compiled in Tab. 6.9. The maximum DM filter inductance utilized in the hardware prototypes equals to 127 μH. Assuming a maximum DM inductance of $L_{\mathrm{DM,max}} = 130\,\mu\mathrm{H}$, the resulting corner (resonance) frequency can be calculated to

$$f_{\mathrm{c,PCB}} = \frac{1}{2\pi\sqrt{C_{\mathrm{PCB,max}}\,L_{\mathrm{DM,max}}}} \approx 1.97\,\mathrm{MHz}\,. \tag{6.68}$$

This simple calculation provides an explanation why deviations from the ideal filter behavior start to occur in the lower MHz range. Additional factors impacting the resulting input filter performance are identified with the EMI measurements performed in Sec. 6.5.5. Nevertheless, the suggested EMI modeling and input filter design procedure is sufficiently accurate to design an input filter that meets the EMI standards (cf. Sec. 6.5.5) and to determine the filter volume, since for the considered switching frequency range, the maximum filter attenuation is required between 150 kHz and 200 kHz, where the suggested EMI modeling procedure provides accurate results.

6.5.5 Experimental Results

To conclude with, practical evidence is provided to verify the suggested EMI modeling and input filter design procedure by a characteristic set of CE noise measurement. The measurements are exemplary shown for the RB IMC prototype (cf. Sec. A.2) with SiC JBS freewheeling diodes in the output stage. The input stage of the converter is switched with 12.5 kHz and the output stage with 25 kHz. Based on the suggested

PCB Layers	*Capacitance per* cm^2
Layer 1 to layer 4	$\approx 2\,\mathrm{pF}$
Layer 1 to layer 3	$\approx 4\,\mathrm{pF}$
Layer 2 to layer 4	$\approx 4\,\mathrm{pF}$
Layer to layer	$\approx 8\,\mathrm{pF}$

Tab. 6.9: Parasitic PCB capacitances per cm^2 in a standard 4-layer PCB (FR4, $\varepsilon_\mathrm{r} = 4.5$) with a total thickness of 1.6 mm and a copper layer thickness of 35 μm.

design procedure, the input filter is dimensioned to meet the CISPR 11 Class A QP noise level. The maximum attenuation has to be provided at 150 kHz at six times the switching frequency of the output stage. The component parameters of the implemented EMI input filter are summarized in Tab. 6.10.

The developed laboratory converter prototypes are not implemented with an enclosure to enable simple access to the hardware for testing. However, when EMI is experimentally investigated, the enclosure has a significant impact on the measurement results, not only for the radiated emissions but also for conducted emissions, since, for instance, the resulting impedance of the ground path on the filter PCB can typically be reduced by utilizing an enclosure and thus the CM filtering performance can be improved. For this reason, the RB IMC is installed in a metal enclosure (cf. Sec. B.2) for measuring EMI. Both the enclosure and the heat sink of the converter are grounded (connected to PE).

Component	*Value*	*Description*
$C_{\mathrm{DM},1}$	$10\,\mu$F, ac $\|\|$ $33\,$nF	MKP, Icel X7R, X2 Murata
$C_{\mathrm{DM},1'}$	$2 \times 10\,$nF	X7R, X2, Murata
$C_{\mathrm{DM},2}$	$2.2\,\mu$F	MKP, X2, Epcos
$C_{\mathrm{DM},3}$	$2 \times 33\,$nF	X7R, X2, Murata
$L_{\mathrm{DM},1}$	$18.3\,\mu$H at $\hat{I}_1 = 13\,$A	High Flux 60, Magnetics 58378, 18 turns, $d_{\mathrm{w}} = 1.2\,$mm
$L_{\mathrm{DM},1\mathrm{d}}$	$24.1\,\mu$H at $\hat{I}_1 = 13\,$A	High Flux 60, Magnetics 58378, 22 turns, $d_{\mathrm{w}} = 1.2\,$mm
$C_{\mathrm{CM},1}$	$3 \times 4.7\,$nF	X7R, Y2, Murata
$C_{\mathrm{CM},2}$	$2 \times 4.7\,$nF	X7R, Y2, Murata
$\lvert Z_{\mathrm{CM},1}\rvert$	$460\,\Omega$	Vitroperm 500 F, VAC W380, 3×7 turns, $d_{\mathrm{w}} = 1.2\,$mm
$\lvert Z_{\mathrm{CM},2}\rvert$	$198\,\Omega$	Vitroperm 500 F, VAC W523, 3×8 turns, $d_{\mathrm{w}} = 1.2\,$mm

Tab. 6.10: Parameters of the implemented EMI input filter for the RB IMC at 150 kHz.

The measurements are performed for motor operation at the nominal line-to-line input voltage of $3 \times 400\,\mathrm{V}$ at $50\,\mathrm{Hz}$ with a three-phase $50\,\Omega/50\,\mu\mathrm{H}$ LISN and a three-phase DM/CM noise separator [300]. The RB IMC supplies an IM (HAC-145, cf. Sec. B.1). The load for the IM is provided by a PMSM (LST-127, cf. Sec. B.1), which is connected to a three-phase resistor. Another power converter is deliberately not utilized for loading the IM in order to avoid any electromagnetic interaction with the RB IMC. A standard unshielded five-wire supply cable and a shielded motor cable, both with a length of 3 m, are utilized for the cabling.

The provided CE measurements can be subdivided into (maximum) Peak (PK) and Quasi-Peak (QP) measurements. Compared with the QP measurements, the PK measurements are considerably faster and are utilized to identify the sensitivities of various modifications on the drive system setup. The final CE measurements to verify the suggested EMI modeling and filter design procedure are performed with the QP detector. Measurements with the PK detector typically lead to noise levels that are 6 dB to 10 dB above the QP noise levels.

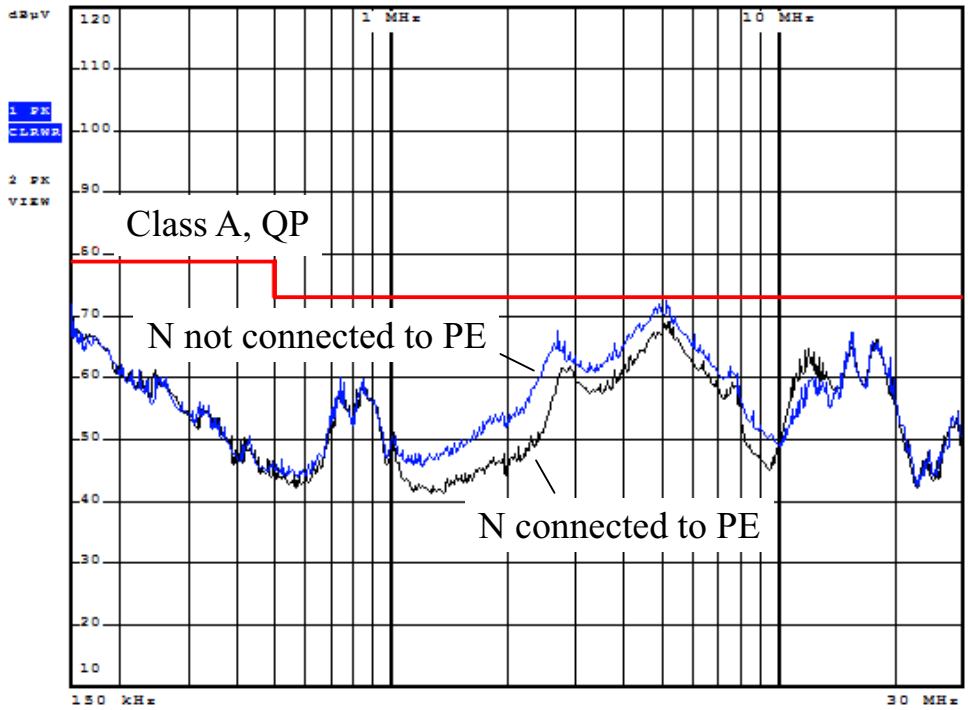


Fig. 6.15: PK CE measurements of the total noise when the neutral conductor (N) is connected and not connected to PE at the mains supply connector terminals of the converter enclosure.

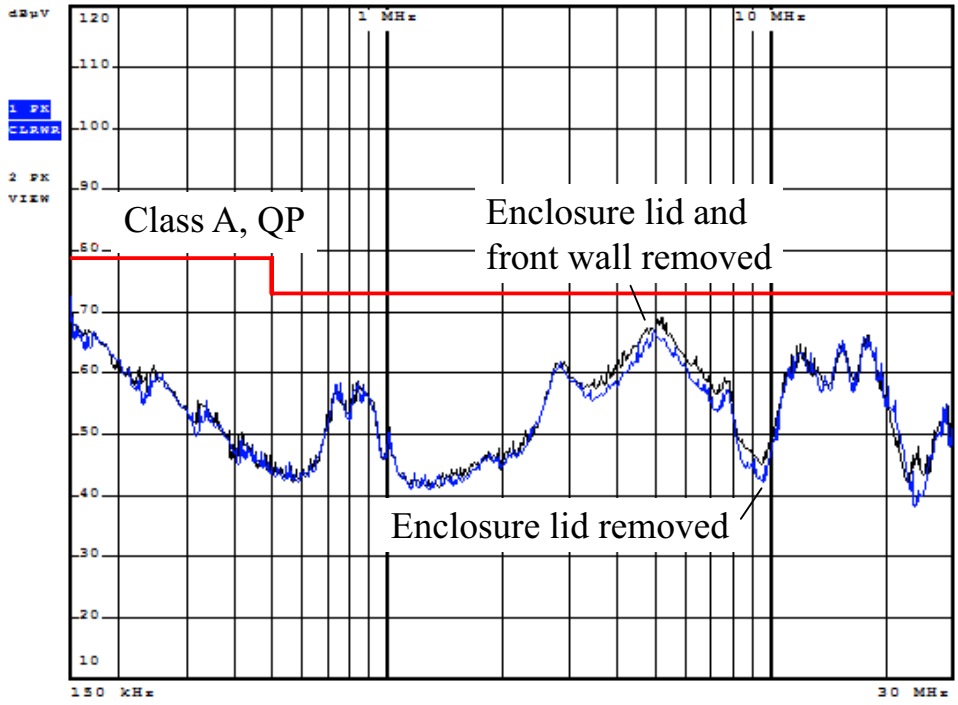


Fig. 6.16: PK CE measurements of the total noise with a removed enclosure lid and a removed front wall and with a removed lid only.

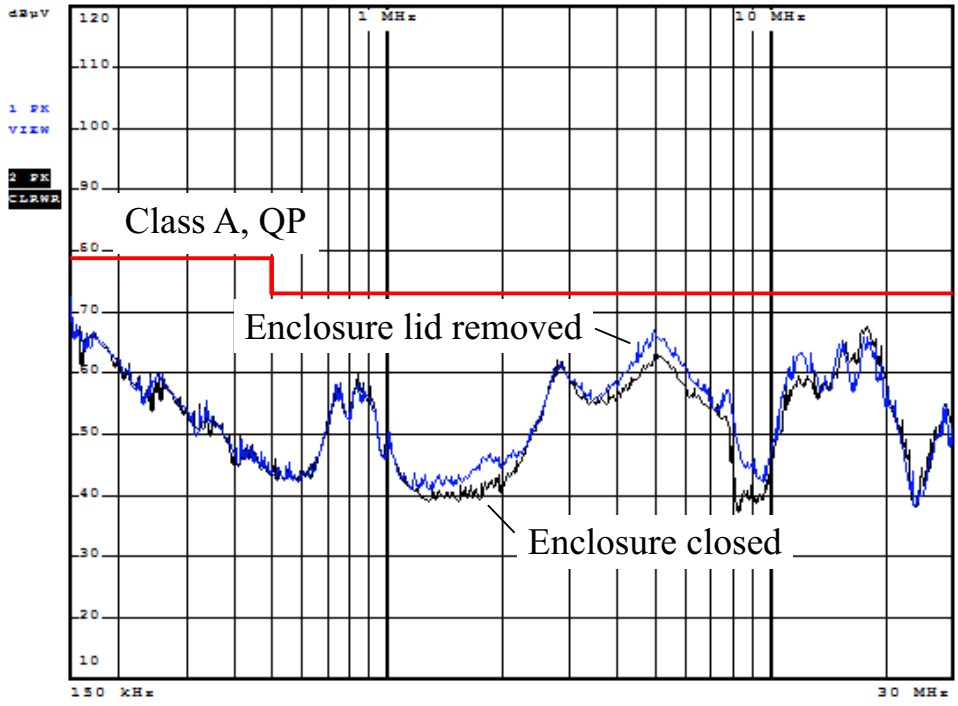


Fig. 6.17: PK CE measurements of the total noise with a removed enclosure lid and with a closed enclosure.

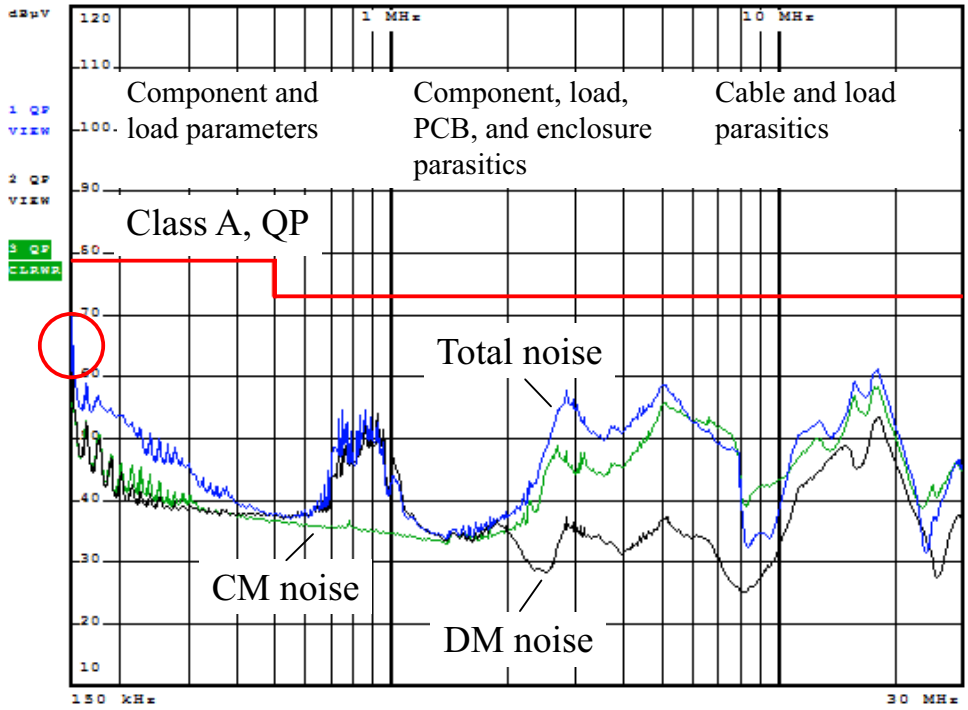


Fig. 6.18: QP CE measurements with a three-phase noise separator, showing the DM, the CM, and the total noise and the dominant parasitics depending on the frequency. The red circle indicates the total noise level at the design relevant frequency of 150 kHz.

The neutral conductor (N) of the standard five-wire supply cable is not required for the IMC. Fig. 6.15 presents the impact on the CE noise level when unused conductors of the supply cable are not properly connected to PE. The two measurements show the difference in the resulting noise when N is only connected to PE at the LISN and is kept floating at the converter enclosure terminals, and when it is connected to PE at the LISN and at the enclosure terminals. As can be seen from the measurement results, when the unused neutral conductor of the supply cable is on both ends of the supply cable connected to PE, the noise level can be reduced by up to 7 dB between 1 MHz and 2 MHz. In Fig. 6.16 and Fig. 6.17, the lid and the front wall of the enclosure are removed separately to investigate the impact on the CE noise level. The measurement results support the initial assumptions. The maximum noise reduction, obtained with a fully closed enclosure compared to a enclosure with removed lid and front wall, equals to 8 dB at 5 MHz.

Ultimately, in Fig. 6.18, the QP measurement results are presented in order to verify the suggested filter design procedure. These measure-

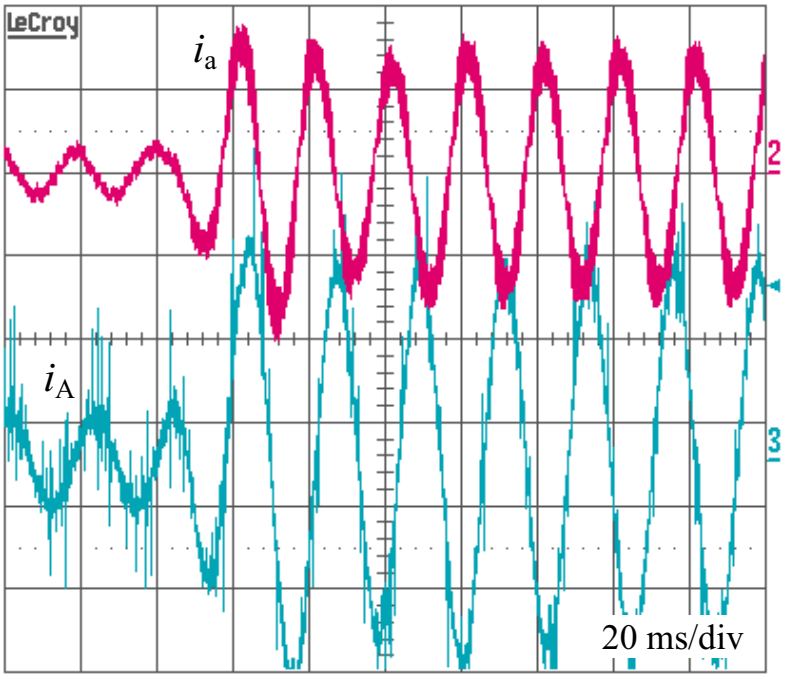


Fig. 6.19: Input and output current waveforms of the RB IMC at an input phase-to-phase voltage of $3 \times 400\,\mathrm{V}$ for a load step from 300 W to 3 kW. i_a: current of the input phase a, 5 A/div; i_A: current of the output phase A, 5 A/div.

ments are performed at a converter output power of 3 kW, which is given by the thermal loading limits of the IM for steady-state operation. This means that the resulting DM noise level is 8 dB lower than at nominal output power of 6 kW of the RB IMC (6 dB for the factor two in power and 2 dB for the lower apparent DM inductance due to the higher currents). As can be seen from the QP noise measurement curves, the RB IMC meets the Class A QP limits over the whole frequency range as desired, even for an increase of the total noise at nominal output power by 8 dB. If the increase of the DM filter inductance due to reduction of the output power to 3 kW is considered in the EMI input filter model, the resulting noise level (cf. red circle in Fig. 6.18) can be predicted accurately at the design relevant frequency of 150 kHz. The dominant noise component at this frequency is DM noise. The deviation between the calculated and the measured noise level is in between 1 dB to 2 dB.

The peak in the DM noise spectrum between 600 kHz and 1 MHz originates from an additional DM capacitor bank $C_{\mathrm{DM},1'} = 20\,\mathrm{nF}$ that was deliberately added between the CM inductor $L_{\mathrm{CM},1}$ and the DM inductor $L_{\mathrm{DM},1}$ (cf. Fig. 6.11 to locate the actual placement) to visualize

the impact of possible resonances between DM capacitor stages and the leakage inductance of CM inductors ($L_{\mathrm{CM,1,lk}} = 2.3\,\mu\mathrm{H}$, measured). The calculation of the resulting resonance frequency based on $C_{\mathrm{DM,1'}}$ and $L_{\mathrm{CM,1,lk}}$ leads to

$$f_{\mathrm{res,C_{DM}L_{CM,lk}}} \approx \frac{1}{2\pi\sqrt{C_{\mathrm{DM,1'}}\,L_{\mathrm{CM,1,lk}}}} = 742\,\mathrm{kHz}\,, \tag{6.69}$$

and justifies the above assumption. For this reason, in the considered EMI filter topology, depicted in Fig. 6.11, no capacitors are placed between the CM and DM inductors.

Fig. 6.19 finally depicts the input and output current waveforms for a load step from 300 W to 3 kW. As can be seen from the measured waveforms, the input current virtually shows no peaking when the load step occurs, which is an experimental prove for a well-damped input filter.

6.6 Summary

The volume, weight, and cost of a power electronic converter system is significantly determined by the passive components. They are mainly required to implement locale energy storage and filters and therefore have also an impact on the dynamic characteristic of the converter.

In this chapter, models of dc-link and EMI filter (suppression) capacitors and inductors are derived to design the storage elements and EMI input filters of the considered ac-ac converter topologies. The polypropylene foil capacitor technology is selected for the filter as well as for the dc-link capacitors as it offers a good compromise between the capacitance per volume, the stability of capacitance regarding operating parameters, and the tolerable rms capacitor current. The core materials are selected to provide good matching between the material properties and the intended usage of the inductor. For boost and dc-link inductors, applied at switching frequencies below 20 kHz and for the CM inductors, amorphous cores are considered, whereas for boost and dc-link inductors for switching frequencies above 20 kHz and for DM filter inductors, powder cores are selected.

Next, the design guidelines for sizing the main energy storage components of the VSBBC, CSBBC, IMC, and CMC are analyzed. The

control based dimensioning criteria, derived in Chap. 3, for the input and output filter capacitors, the dc-link capacitors and inductors, and the boost inductors, are reconsidered and extended with energy and current ripple or voltage ripple based criteria.

The CE EMI filtering concept is based on a multi-stage DM/CM input filter that can be used for all four converter topologies. Commencing from the EMI filter topology, the DM and CM equivalent circuits are derived, and the key filter design steps are discussed. The CMC and IMC do not need to be considered separately, due to the selected modulation schemes and their functional equivalence. The motor load is represented with an impedance function that includes the motor cable.

Besides the derivation of all design equations, the major contribution of this chapter is the linkage that is established between the passive component models, the various design criteria for the main energy storage components, and the actual EMI input filter design. With this approach, a comprehensive basis for a multi-dimensional filter and passive component design is provided.

The theoretical findings are substantiated by CE measurements, which show that the suggested design procedure leads to an input filter design that meets the desired EMC standard. Various test measurements have shown that inadequate grounding of non-utilized conductors in supply cables or the absence of a proper enclosure may lead to a reduction of the EMI attenuation. The converter enclosure plays an important role in the grounding concept of the converter system. Only if a low impedance connection of the EMI input filter to PE is established, the desired filter attenuation can be achieved, which is of particular importance for frequencies above 1 MHz.

This fact highlights the importance of efficient and fast simulation software, which enables to simulate complex electromagnetic structures such as an ac-ac converter in combination with its metal enclosure.

Chapter 7

Comparative Evaluation and Conclusions

In this chapter a systematic comparison of the VSBBC, the CSBBC, the IMC, and the CMC for a 15 kVA drive system with a PMSM is presented, applying the models, the design equations, and the optimization concepts derived in the previous chapters. The results of the comparison are then used to provide a holistic and unbiased assessment of the individual ac-ac converter systems and to analyze the achievable performance gain by utilizing SiC JFETs instead of latest generation Si IGBTs and Si diodes.

This ultimately enables to identify the application areas of the considered converter topologies and the 1200 V SiC JFET technology in the field of industrial low-voltage drives.

7.1 Methodology of the Comparison

7.1.1 Converter and Drive System Specifications

All four converter systems are designed to operate on a balanced three-phase 50 Hz mains system with a nominal rms line-to-line voltage of 3×400 V for a rated, continuous output power of 15 kVA and to meet the CISPR 11 Class B EMI standard for conducted emission. The considered drive system is based on a PMSM to ensure a high electro-mechanical power/torque density. The resulting current-to-voltage displacement angle at the converter output Φ_2 can hence be assumed with $\Phi_2 \approx 0$. The converters are controlled to provide unity power factor at the input, and the dc-link voltage of the VSBBC is assumed with 700 V. The impact of the current-to-voltage displacement on the semiconductor losses of the converter systems is mitigated due to the selected modulation schemes, as shown in Chap. 4. For the VSBBC, for instance, this means that the

	Parameter	*Value*
Electrical	Nominal line-to-line voltage	3×400 V
	Mains frequency	50 Hz
	Rated output power	15 kVA
	Nominal output frequency	150 Hz
	Switching frequency	8 kHz, 32 kHz, 72 kHz
	Power factor at the input at rated output power	> 0.99
	EMI compliance (CISPR 11)	Class B
	DC-link voltage (VSBBC)	700 V
Thermal	Maximum junction temperature	150°C
	Maximum sink temperature	95°C
	Maximum ambient temperature	50°C
	Nominal ambient temperature	20°C

Tab. 7.1: Main electrical and thermal specifications of the converter systems.

semiconductor switching losses remain invariant for the same output current amplitude, independent on whether a PMSM ($\Phi_2 \approx 0$) or a IM ($\Phi_2 \approx \pi/6$) is supplied. However, the highest conduction losses in the transistors of the output stage of the VSBBC occur at ($\Phi_2 = 0$) for motor operation. This fact provides another reason besides the argument with the PMSM why $\Phi_2 = 0$ is a reasonable choice for a comparative evaluation.

In order to enable a fair comparison, the rated voltages of the PMSMs are matched to the corresponding output voltage ranges of the VSBBC, CSBBC, and MC such that at 90% of the maximum output voltage of the individual converters and at an equal electrical output frequency of 150 Hz, all drives deliver the same nominal shaft power. This operating point is defined as the nominal operating point for motor and generator operation (cf. Fig. 4.1, OP1 and OP5). For nominal motor operation, all PMSMs absorb a power of 15 kW. The nominal motor voltage is defined at 90% of the maximum output voltage of each converter to provide sufficent voltage control margin. The main electrical and thermal specifications of the converter systems are summarized in Tab. 7.1.

The switching frequencies are considered within a range of 8 kHz to 72 kHz with three selected main values at 8 kHz, 32 kHz, and 72 kHz. The switching frequency of the input and output stage of the VSBBC and CSBBC is identical. In the case of the IMC, the specified frequency refers to the switching frequency of the output stage. Although the switching frequency of the input stage of the IMC is half the switching frequency of the input stage of the VSBBC and the CSBBC, a fair comparison with the other topologies is still enabled: Firstly, no switching losses are generated in the input stage of the IMC. Secondly, the input current of the IMC contains the spectral components of the switching frequency of the input and the output stage. This leads, with respect to the effective frequency components at the converter input, to similar conditions for the design of the input capacitors of the IMC as for the input capacitors of the CSBBC and CMC or the boost inductors of the VSBBC.

7.1.2 Converter Design Approach

The performed multi-domain ac-ac converter design and optimization approach is visualized in Fig. 7.1 and can be compared with a "trickle-down" design flow. It consists of two main design and parameter adaptation loops: one for the semiconductors and cooling system and the other

for the passive components and EMI input filter. The converter design outputs can be subdivided into electrical and mechanical converter properties, which can be subsequently used for custom post-processing.

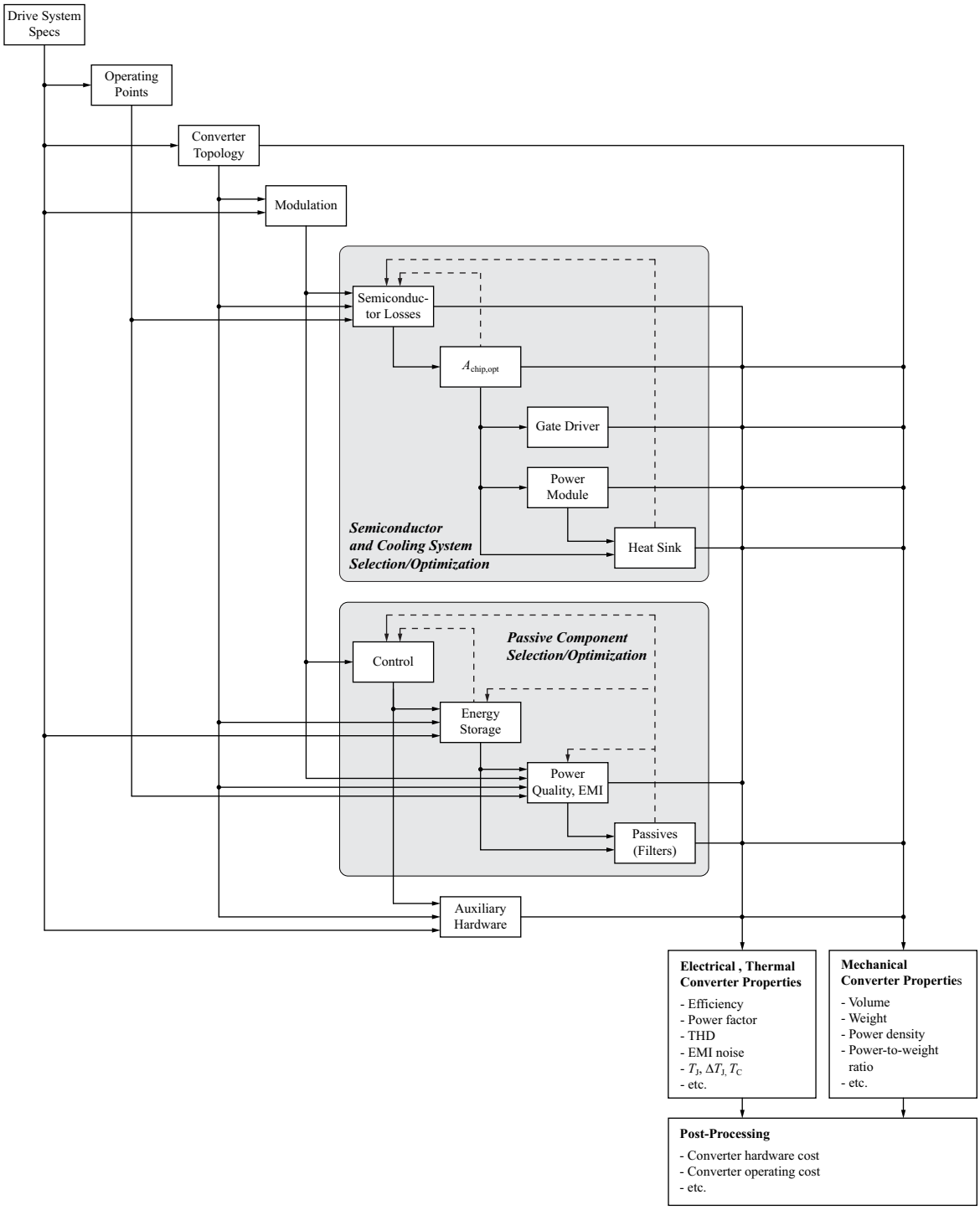


Fig. 7.1: Suggested converter design approach. The iterative design/optimization feedback paths are marked with dashed arrows.

7.2 Transistor Performance Maps

7.2.1 Description of Concept

Prior to performing the actual semiconductor design, a pre-evaluation of possible Si and SiC semiconductor devices is presented, in order to provide a better understanding of their characteristic properties. For that purpose, the concept of transistor performance maps is introduced.

With the possibility provided by the models of the SAC2 to determine the thermal impedance between the junction and the heat sink as a function of the chip area, the relation between the electrical and thermal properties of a semiconductor chip is mathematically described for stationary and transient operating conditions. This allows a refinement of the initial semiconductor assessment performed in Sec. 2.5 by applying the algorithm of the SAC2 to generate various performance maps for the analyzed Si IGBT4 and normally-on SiC JFET technology. For that purpose, a bridge-leg in a buck-type arrangement, according to Fig. 7.2, is considered, which is a typical semiconductor configuration of VSIs. The switches S_1 and S_2 represent the power transistors to be investigated. In the case of the IGBT with a discrete anti-parallel (freewheeling diodes), the diodes are implemented for instance with Si EmCon4 diode chips, whereby the chip area is selected such that the junction temperature of the diodes does not exceed the maximum junction temperature specified for the IGBT. In the case of the JFET, the

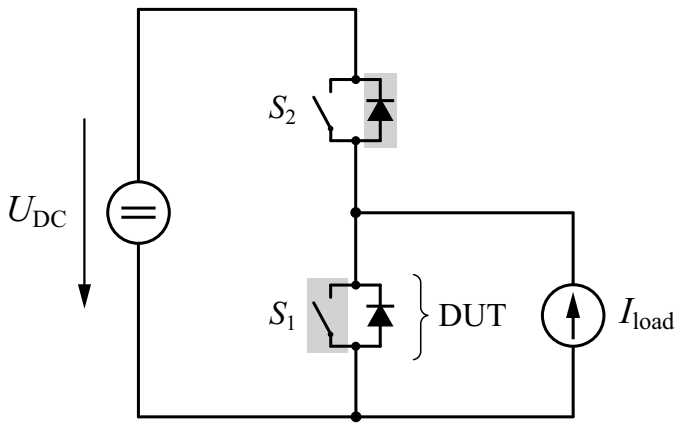


Fig. 7.2: Circuit used to determine the performance maps of the IGBT and the JFET. The transistor S_1 is the Device Under Test (DUT). The devices on gray backgrounds conduct current for $I_{load} > 0$.

anti-parallel diodes are an integral element of the chip and thus cannot be selected independently of the chip area of the JFET.

The power device performance maps are generated for the following operating conditions. The high-side switch S_2 is kept turned off, whereas the low-side switch S_1 is operated at a given switching frequency f_{sw} and a duty cycle D within the interval $D = (0 \ldots 100)\%$. The minimum and maximum duty cycle D_{min} and D_{max} are selected such that a switching of the transistors still occurs. The load current I_{load} may be varied within the interval $I_{\mathrm{load}} = [0 \ldots I_{\mathrm{load,max}}]$. The resulting average and rms transistor currents are given by

$$I_{\mathrm{S,avg}} = D I_{\mathrm{load}} \tag{7.1}$$

$$I_{\mathrm{S,rms}} = \sqrt{D} I_{\mathrm{load}} \, . \tag{7.2}$$

This basically corresponds to the operating range of a bridge-leg of a pulse-width modulated VSI within an electrical half-period of the output. A dc-link voltage U_{DC} of 600 V is selected as this voltage level equals to the average switched voltage of all the considered ac-ac converter topologies. It is further assumed that the semiconductor chips are integrated in a semiconductor module as specified in Fig. 5.2. All additional quantities and relations are adopted from the models and definitions presented in the previous chapters.

7.2.2 Load Current versus Duty Cycle

The performance maps in Fig. 7.3 to Fig. 7.4 compare the maximum load current of the IGBT4 and the JFET technology as function of the duty cycle and the switching frequency at a heat sink temperature of 90°C and 120°C, and a junction temperature of 175°C for a predefined chip area. These comparisons allow the visualization of the impact of the conduction and switching losses on the device performance for given operating conditions. In accordance to Sec. 2.5, an active transistor chip area of 24 mm^2 is selected, which corresponds to a total chip area of 35 mm^2. The maximum load current of 35 A at the maximum duty cycle is determined based on the maximum current density specified for the transistor chips. The gray areas in the figures highlight the difference of the load current between the JFET and the IGBT for the lowest switching frequency, at which the JFET chip allows for a higher load current over the whole duty cycle range than the IGBT. This frequency

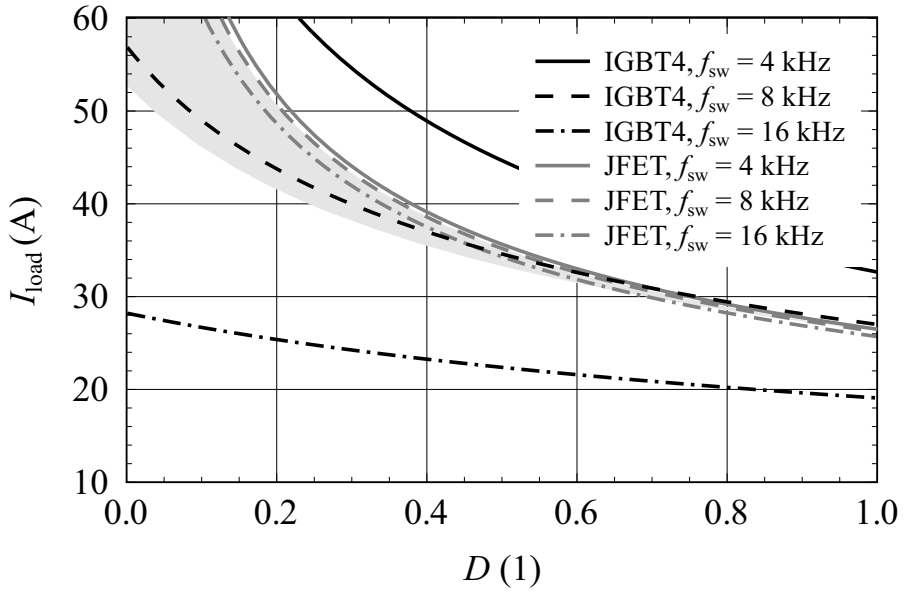


Fig. 7.3: Load current I_{load} versus duty cycle D such that $T_{\text{J}} = 175°\text{C}$ for $A_{\text{chip,act}} = 24\,\text{mm}^2$, $T_{\text{S}} = 90°\text{C}$, and $U_{\text{DC}} = 600\,\text{V}$. The gray shaded area shows the difference in current for the minimum switching frequency of 8.7 kHz, where $I_{\text{load}}|_{\text{JFET}} \geq I_{\text{load}}|_{\text{IGBT4}} \,\forall\, D = (0 \ldots 100)\%$.

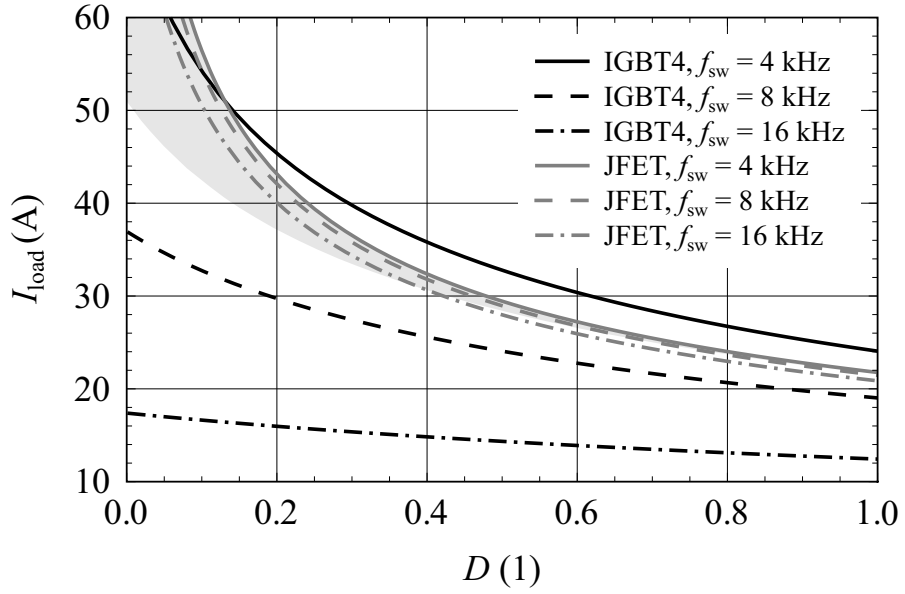


Fig. 7.4: Load current I_{load} versus duty cycle D such that $T_{\text{J}} = 175°\text{C}$ for $A_{\text{chip,act}} = 24\,\text{mm}^2$, $T_{\text{S}} = 120°\text{C}$, and $U_{\text{DC}} = 600\,\text{V}$. The gray shaded area shows the difference in current for the minimum switching frequency of 5.8 kHz, where $I_{\text{load}}|_{\text{JFET}} \geq I_{\text{load}}|_{\text{IGBT4}} \,\forall\, D = (0 \ldots 100)\%$.

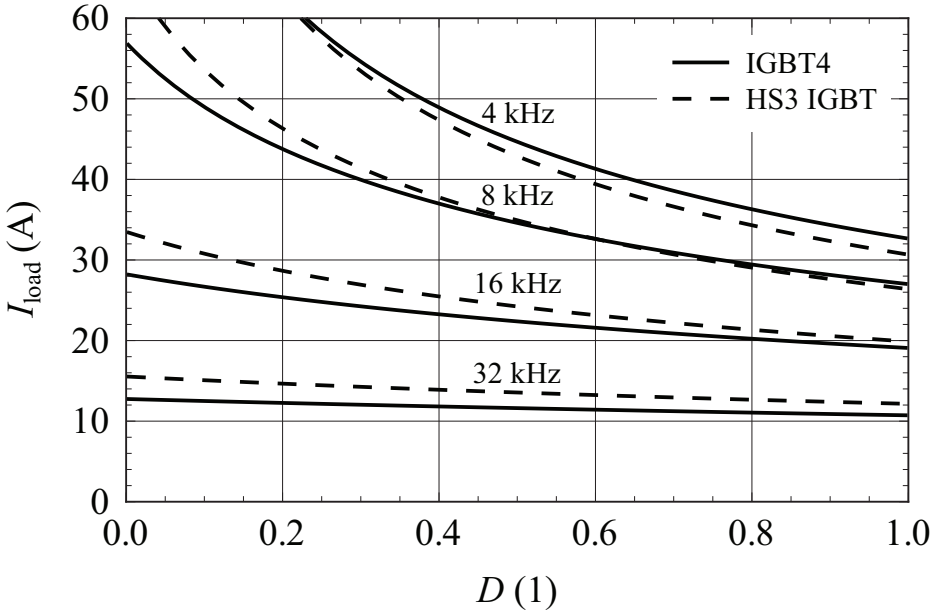


Fig. 7.5: Load current I_{load} versus duty cycle D for the IGBT4 and HS3 IGBT technology such that $T_{\text{J}} = 175°\text{C}$ for $A_{\text{chip,act}} = 24\,\text{mm}^2$, $T_{\text{S}} = 90°\text{C}$, and $U_{\text{DC}} = 600\,\text{V}$.

limit occurs between 6 kHz and 9 kHz for the two considered temperature differences between junction and sink of 55 K and 85 K.

In order to complete the picture of the Si IGBT technology, Fig. 7.5 finally presents a comparison between the considered T&FS IGBT4 technology, optimized for low conduction losses, and the latest generation High-Speed3 (HS3) IGBT technology, both produced by Infineon. The loss data of the high-speed IGBTs are adopted from data sheets of discrete components (IKWxxN120H3 series, TO-247 package). At equal conditions, the HS3 IGBTs have in average 20% higher conduction losses and 15% lower switching losses compared to the standard IGBT4 devices. As can be seen in Fig. 7.5, for switching frequencies below 10 kHz, the IGBT4 technology provides better performance over the whole duty cycle range. Even at 32 kHz, the HS3 IGBT outperforms the IGBT4 only by an increase in the load current of 12% at maximum duty cycle.

7.2.3 Chip Area versus Switching Frequency

In order to identify the appropriate switching frequency range of the different semiconductor technologies, the minimal active chip area required for given operating conditions is determined as a function of

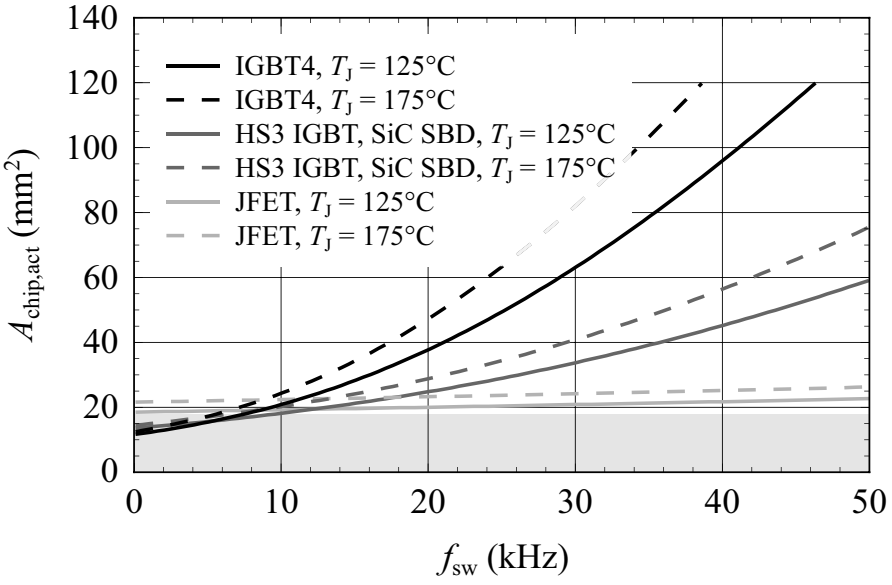


Fig. 7.6: Active chip area $A_{\text{chip,act}}$ versus switching frequency f_{sw} for different junction temperatures $T_{\text{J}} = \{125, 175\}$°C at $D_{\max}$, $I_{\text{load}} = 25\,\text{A}$, $T_{\text{S}} = 90$°C, and $U_{\text{DC}} = 600\,\text{V}$. The gray shaded area represents the minimal chip area required by the specified current density.

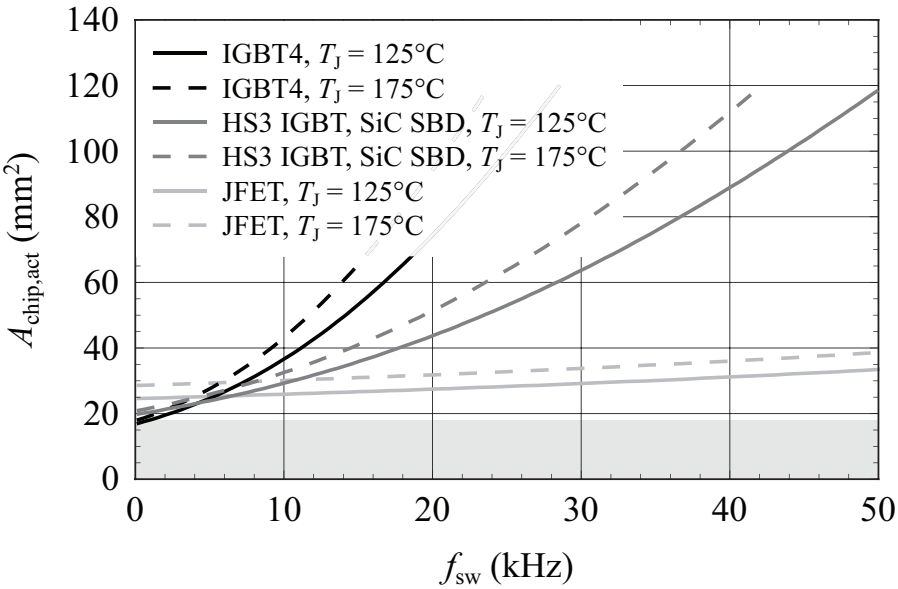


Fig. 7.7: Active chip area $A_{\text{chip,act}}$ versus switching frequency f_{sw} for different junction temperatures $T_{\text{J}} = \{125, 175\}$°C at $D_{\max}$, $I_{\text{load}} = 25\,\text{A}$, $T_{\text{S}} = 120$°C, and $U_{\text{DC}} = 600\,\text{V}$ The gray shaded area represents the minimal chip area required by the specified current density.

the switching frequency. The load current is selected to be 25 A based on the results, shown in Fig. 7.3 and Fig. 7.4 for maximum duty cycle. (For comparison, the peak output current of a 15 kVA VSI with a dc-link voltage of 700 V equals to 25 A.) It should be noted that the specification of the junction temperature, the sink temperature and the chip area implicitly limit the maximum average losses of the switching device. The analysis is performed for the selected IGBT4 and EmCon4 diode technology, the SiC JFET technology, and for completeness also for the HS3 IGBT technology with SiC Schottky freewheeling diodes (SiC SBD). Thereby, the same average reduction ratio of the IGBT turn-on losses with SiC Schottky freewheeling diodes compared to Si diodes of 2.5 is assumed as was experimentally determined in Sec. 2.4.3. The maximum transistor chip area is limited to 120 mm^2 as specified for the semiconductor models.

According to Fig. 7.6 and Fig. 7.7, the following conclusions can be drawn for the considered operating conditions: For switching frequencies below 5 kHz, the required IGBT chip area is smaller than the JFET chip area, independent on whether the IGBT4 or the HS3 IGBT with Si or SiC freewheeling diodes are utilized. This is equivalent to the statement that for an equal chip area the Si IGBTs lead to lower losses than the JFETs. Not until for switching frequencies above 15 kHz the resulting JFET chip area is smaller than the IGBT chip area. However, for HS3 IGBTs with SiC Schottky diodes, a significant reduction of the transistor chip utilizing SiC JFETs occurs only above 20 kHz.

7.3 Converter System Comparison

7.3.1 Required Semiconductor Chip Area

Based on the results of the previous section, the Si T&FS IGBT4 devices with Si EmCon4 freewheeling diodes and the SiC JFETs are selected for the comparative evaluation of the VSCBBC, the CSBBC, the IMC, and the CMC. The Si IGBT4 technologies provides superior performance for switching frequencies below 10 kHz and the SiC JFET technology for switching frequencies above 20 kHz.

In order to provide a common basis for investigating the semiconductor requirements of the considered converter topologies, the suggested SAC2 (cf. Chap. 5) is applied. The implemented optimization algorithm

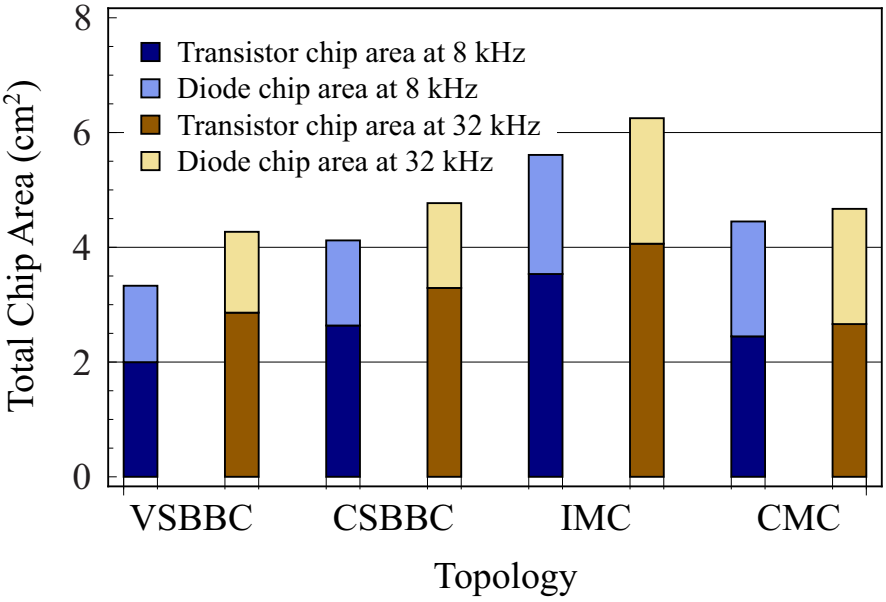


Fig. 7.8: Required total semiconductor chip area of the four converters using Si IGBT4 devices and EmCon4 diodes at 8 kHz and 32 kHz, to provide the rated power of 15 kVA for motor (OP1) and generator (OP5) operation at $T_{\mathrm{J,max}} = 150°\mathrm{C}$.

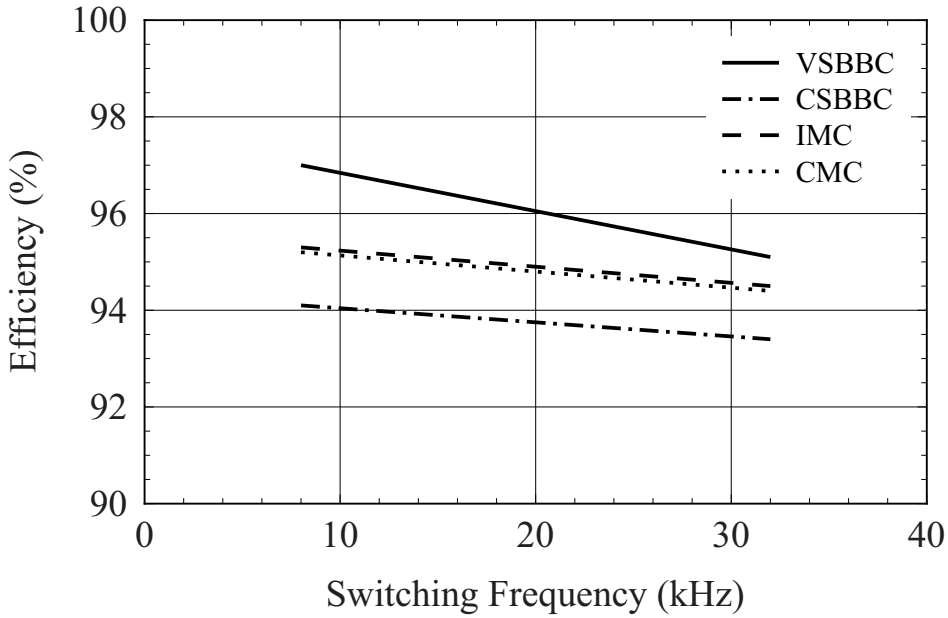


Fig. 7.9: Converter semiconductor efficiency versus switching frequency for Si IGBT4 devices and EmCon4 diodes, evaluated for motor operation (OP1) and a switching frequency range of 8 kHz to 32 kHz.

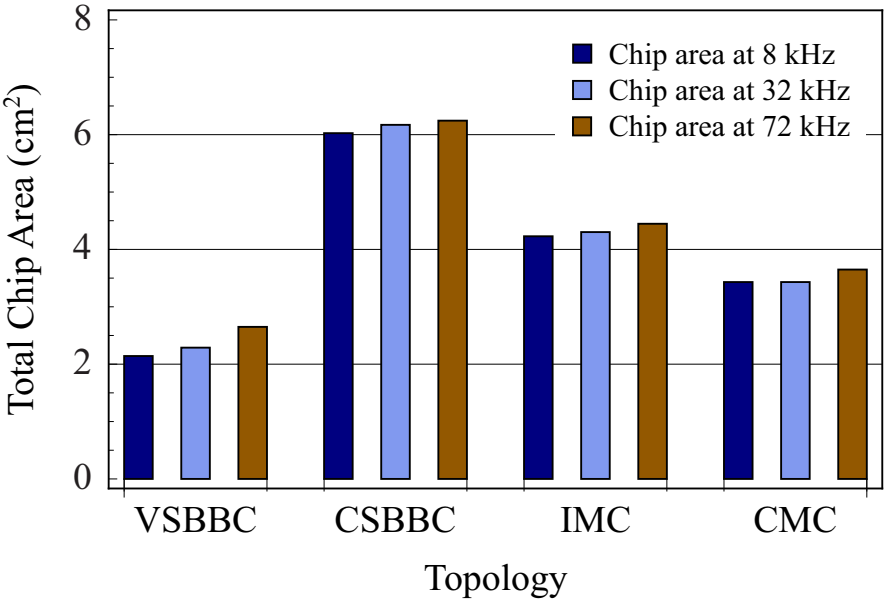


Fig. 7.10: Required total semiconductor chip area of the four converters using normally-on SiC JFETs at 8 kHz, 32 kHz, 72 kHz to provide the rated power of 15 kVA for motor (OP1) and generator (OP5) operation at $T_{\mathrm{J,max}} = 150°\mathrm{C}$.

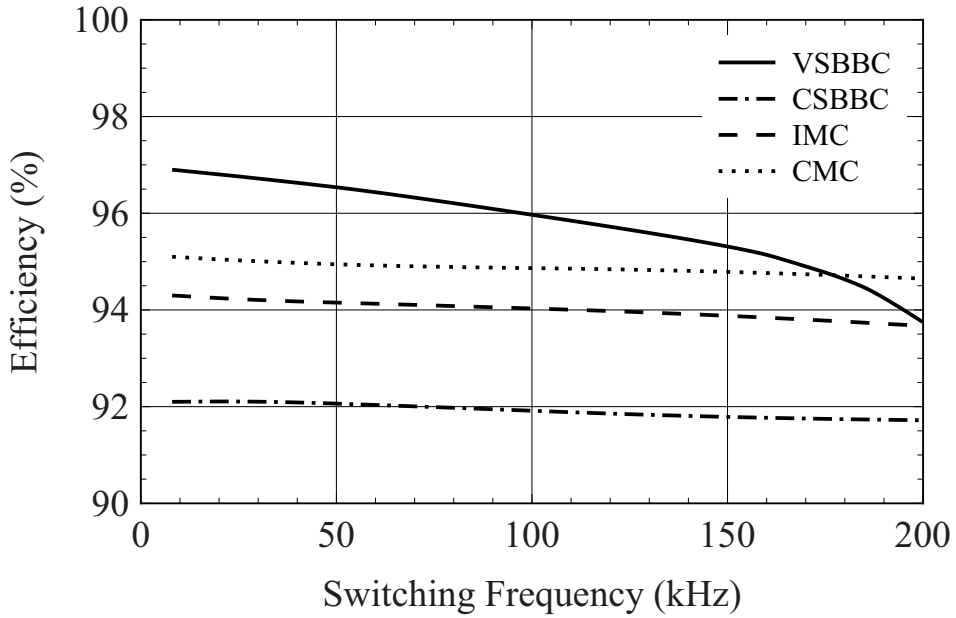


Fig. 7.11: Converter semiconductor efficiency versus switching frequency for SiC JFETs, evaluated for motor operation (OP1) and a switching frequency range of 8 kHz to 200 kHz.

determines the minimum required semiconductor area for the individual transistor and diode chips of all converters at given operating points such that the average junction temperatures of the IGBTs and diodes $T_{\mathrm{J,S/D}}$ are equal or less than a predefined maximum value $T_{\mathrm{J,max}}$.

In this comparison, for all converter topologies the minimum semiconductor chip areas are determined to provide the rated output power of 15 kVA at the specified maximum ambient temperature T_{A} of 50°C and at the maximum junction temperature $T_{\mathrm{J,max}}$ of 150°C for nominal motor and generator operation (cf. Chap. 4, OP1 and OP5). According to the specification, for an ambient temperature of 50°C the cooling system has to designed for an the average heat sink (surface) temperature T_{S} of 95°C. The required total semiconductor areas and the resulting semiconductor converter efficiencies are plotted in Fig. 7.8 to Fig. 7.11. The resulting thermal operating conditions of the semiconductors with a temperature difference between junction and sink of 55 K are demanding but still within the specifications of typical semiconductor modules. However, for an industrial converter design, the junction temperature specifications would be typically lowered for the same ambient temperature.

The special feature of the considered SiC JFETs is that the transistor and diode are integrated in one semiconductor chip, which doubles the frequency of the thermal loading and typically leads to a smaller junction temperature ripple. Regarding the converter implementation with SiC JFETs it is assumed that all semiconductor devices of a converter topology are implemented with SiC JFETs. This means that for the CS-BBC the series diodes are also implemented with JFETs. As the JFET is a unipolar device that can conduct the current in both directions, the JFET channel is always turned on, when the diode is conducting in order to reduce the on-state conduction losses. The intrinsic body diode, hence, is primarily used as a commutation diode, which is conducting during a safety time of 50 ns to 100 ns.

7.3.2 Passive Component Volume

The next step in the comparative evaluation of the four converter systems is to design the passive components and the EMI input filter to meet the CISPR 11 Class B EMI standard for conducted emission according to the design equations and optimization guidelines presented in Sec. 3.2 and Chap. 6.

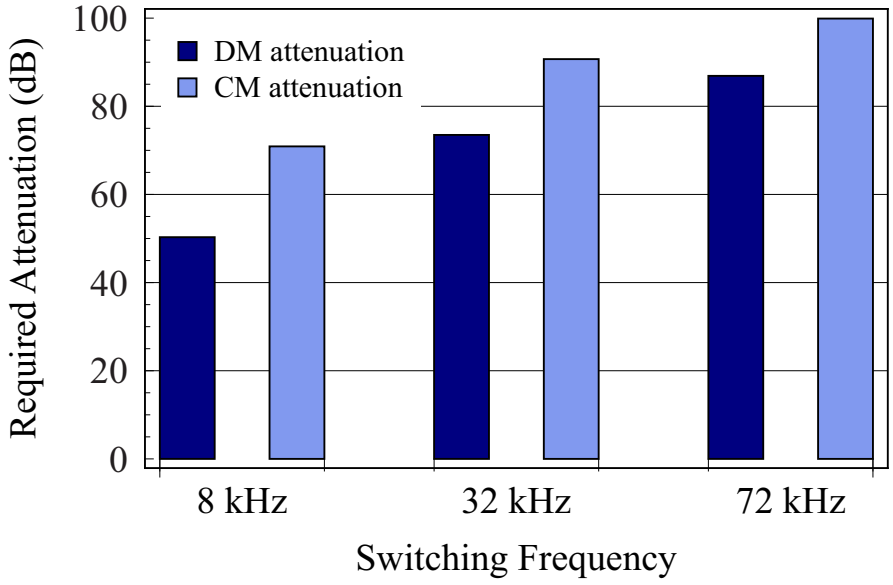


Fig. 7.12: Required DM and CM filter attenuation for the VSBBC at a switching frequency of 8 kHz, 32 kHz, and 72 kHz.

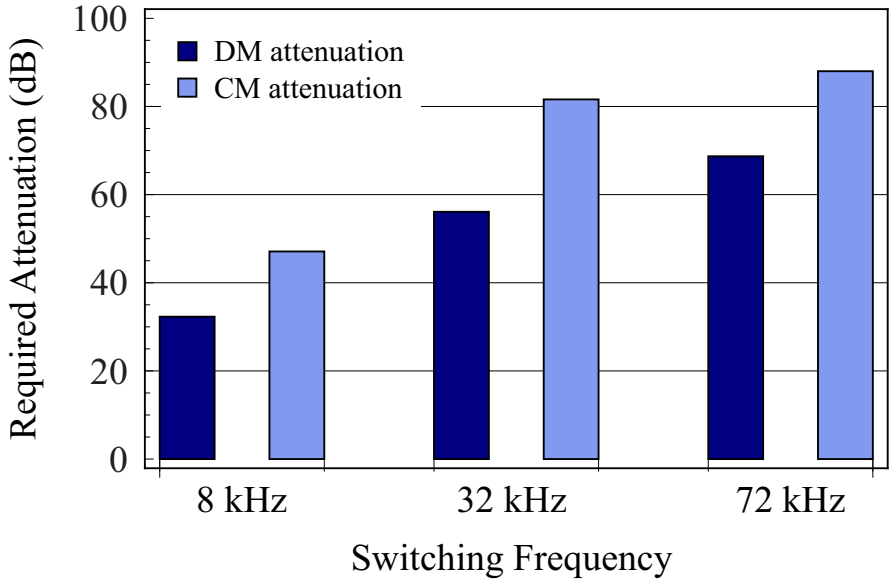


Fig. 7.13: Required DM and CM filter attenuation for the CSBBC at a switching frequency of 8 kHz, 32 kHz, and 72 kHz.

All DM filter inductors are implemented with HF 60 powder core material (overview of core materials for DM inductors, cf. Tab. 6.3). At a switching frequency of 8 kHz, for the boost and dc-link inductors HF 60 powder core material and amorphous 2605SA1 core material are considered. At a switching frequency of 32 kHz, the boost and dc-link inductor

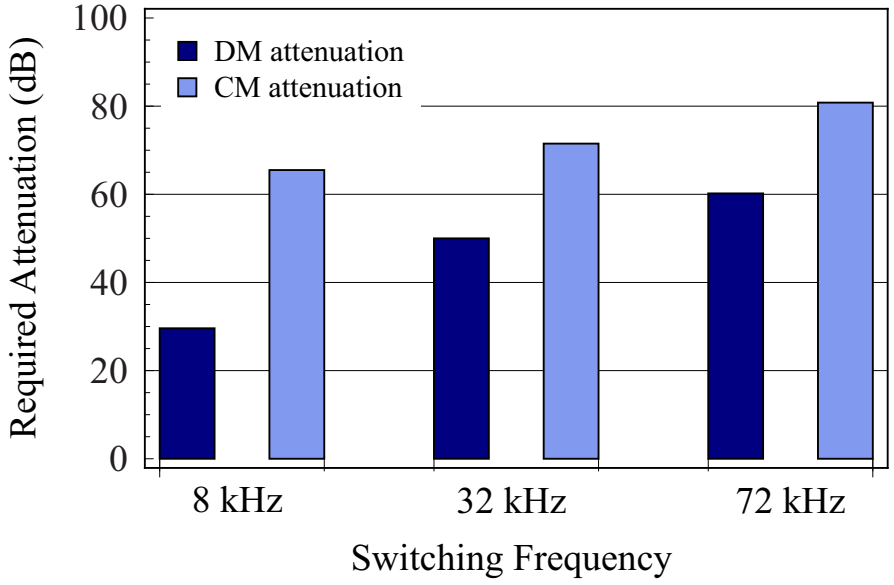


Fig. 7.14: Required DM and CM filter attenuation for the MC at a switching frequency of 8 kHz, 32 kHz, and 72 kHz.

are implemented with HF 60 and at 72 kHz with MPP 60 powder core material. This material selection provides a reasonable compromise between the volume and the losses of the inductors. Only one core material is considered for the CM inductors (cf. Fig. 6.8).

Based on the attenuation requirements, the EMI input filter design is performed by considering the boundary conditions stated in Sec. 6.5 and the interdependencies visualized in Fig. 7.2. The impedance parameters of a typical PMSM including a 3 m long motor cable are adopted from Sec. 6.5. The required DM and CM input filter attenuation of the VSBCC, CSBBC, and MC to meet the specified EMI standard is shown in Fig. 7.12 to Fig. 7.14 for a switching frequency of 8 kHz, 32 kHz, and 72 kHz. The presented attenuation values refer to the (additional) attenuation that has to be provided by the input filter without the attenuation that is already given by the boost inductors L_{B} of the VSBBC or the input capacitors $C_{\mathrm{F,inp}}$ of the CSBBC or MC.

The required boxed volume of the passive components of the EMI input filter components (without the boost inductors of the VSBBC) is presented in Fig. 7.15. Ultimately, Fig. 7.16 depicts the total boxed volume of the passive components without the heat sink and pinpoints the volume reduction when amorphous core material is utilized for the implementation of the boost and dc-link inductors instead of powder

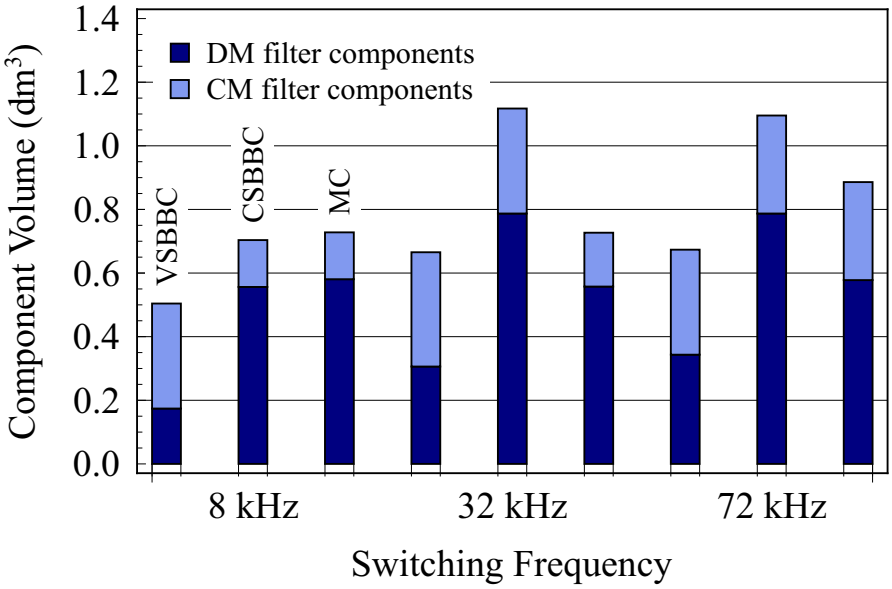


Fig. 7.15: Boxed volume of the EMI input filter components at 8 kHz, 32 kHz, and 72 kHz (without the boost inductors of the VSBBC.)

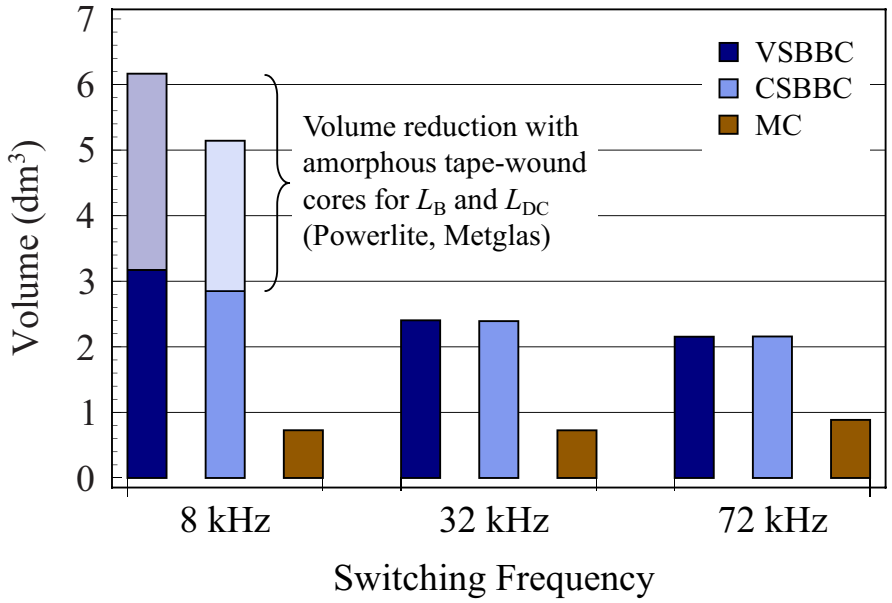


Fig. 7.16: Total boxed volume of the passive components at 8 kHz, 32 kHz, and 72 kHz. At 8 kHz, the achievable volume reduction is shown if the boost and dc-link inductors are implemented with 2605SA1 amorphous core material instead of HF 60 powder core material.

core material. The disadvantage of the amorphous cores is the high costs. For this reason, for standard commercial converter systems with

a switching frequency of 4 kHz to 8 kHz, the boost inductors are typically manufactured with laminated iron cores.

Parameter		VLBBC	CSBBC	IMC	CMC
Output voltage		256 V	201 V	175 V	175 V
Output current		19.6 A	24.9 A	28.6 A	28.6 A
Boost inductors	8 k	1.9 mH	–	–	–
	32 k	0.5 mH	–	–	–
DC-link inductors	8 k	–	3.7 mH	–	–
	32 k	–	0.9 mH	–	–
DC-link capacitors	8 k	102 μF	–	–	–
	32 k	75 μF	–	–	–
Input capacitors	8 k	–	35 μF	38 μF	38 μF
	32 k	–	10 μF	10 μF	10 μF
Output capacitors	8 k	–	34 μF	–	–
	32 k	–	8.5 μF	–	–
Si chip area	8 k	3.3 cm^2	4.1 cm^2	5.6 cm^2	4.5 cm^2
	32 k	4.3 cm^2	4.8 cm^2	6.3 cm^2	4.7 cm^2
Total efficiency	8 k	95.7%	92.7%	94.7%	94.6%
(Si, OP1/OP5)	32 k	94.1%	92.4%	93.9%	93.8%
Passives	8 k	4.0 dm^3	4.7 dm^3	2.1 dm^3	2.2 dm^3
	32 k	3.9 dm^3	4.6 dm^3	2.3 dm^3	2.3 dm^3
SiC chip area	8 k	2.1 cm^2	6.0 cm^2	4.2 cm^2	3.4 cm^2
	32 k	2.3 cm^2	6.2 cm^2	4.3 cm^2	3.5 cm^2
Total efficiency	8 k	95.6%	91.7%	93.7%	94.5%
(SiC, OP1/OP5)	32 k	95.7%	91.1%	93.6%	94.4%
Passives	8 k	4.0 dm^3	5.5 dm^3	2.4 dm^3	2.2 dm^3
	32 k	3.3 dm^3	5.0 dm^3	2.5 dm^3	2.3 dm^3

Tab. 7.2: Converter system design parameter overview for 8 kHz and 32 kHz.

7.3.3 AC-AC Converter Design Output

The key performance figures and component parameters of the designed VSBBC, CSBBC, IMC, and CMC based drive systems are compiled in Tab. 7.2 for a switching frequency of 8 kHz and 32 kHz. In this switching frequency range, the converters can be implemented with both Si IGBTs and diodes and SiC JFETs. This enables a direct comparison of the two different semiconductor technologies. The passive component design obviously is assumed to be identical for the Si and SiC converters.

In respect of the commonly used argument that with a MC the bulky dc-link capacitor of a VSBBC can be omitted, the resulting volume of the dc-link capacitor C_{DC} of the VSBBC and of the input capacitors $C_{\mathrm{F,inp}}$ of the MC are briefly compared. With reference to (6.2) and Tab. 7.2, the dc-link capacitor requires 249 cm^3 and the three input capacitors 291 cm^3 at a switching frequency of 8 kHz. At 32 kHz, the volume of the dc-link capacitor is 185 cm^3 and that of the input capacitors 91 cm^3. Thus, at switching frequencies in the range of 10 kHz, the volume of the dc-link capacitor of the VSBBC and of the three input capacitors of the MC are similar, if both converter concepts are implemented according to the presented design guidelines (for minimal energy storage). Most interestingly, the stored energy in the VSBBC is approximately eight times higher than in the MC.

7.4 Conclusions

7.4.1 Main Results

For the considered 15 kW drive system with PMSMs, both the CMC as well as the IMC enable a more compact implementation than the VSBBC and the CSBBC. For the selected components and design, the MC concept allows for a reduction of the total volume of the passive components including the heat sink by a factor of 1.5 to 2 in the investigated switching frequency range of 8 kHz to 72 kHz. This volume reduction is mainly due to the absence of the boost inductors or dc-link inductors. The VSBBC and the CSBBC require approximately the same volume of the passive components. Unfortunately, the higher achievable power density of MCs is impaired by the lack of desirable, basic converter properties such as output voltage step-up capability, unconstrained re-

active input power compensation, simple feedback control of the input currents, and the possibility for single-phase operation.

The resulting total efficiency at nominal motor or generator operation of all four converters for the considered worst case at a sink temperature of 95°C, a junction temperature of 150°C, and for a minimum semiconductor chip area varies between 91% and 96% for a switching frequency range of 8 kHz to 32 kHz for both implementation variants with Si and SiC power semiconductors. Regarding the efficiency, the VSBBC provides the highest efficiency followed by the MC and the CSBBC. With Si power devices, only for switching frequencies above 30 kHz the MC allows for a higher efficiency compared to the VSBBC. By utilizing SiC JFETs, the switching frequency of equal semiconductor losses (efficiency) occurs at 150 kHz.

For the considered chip area minimal semiconductor design and the switching frequency range of 8 kHz to 32 kHz, the all-SiC converters with SiC JFETs obviously do not lead to a significant increase in the efficiency, but allow for a reduction of the total required semiconductor chip area by a factor of 1.5 to 2 compared to the implementation with the investigated Si power semiconductors, except for the CSBBC. For the CSBBC, the intrinsic anti-parallel body diode cannot be utilized as in the VSBBC and MC and thus additional JFET chips are required for the implementation of the series diodes in the CSBBC.

This chip area reduction at similar electrical converter performance clearly shows that the investigated 1200 V SiC JFETs are beneficial for the implementation of low-voltage VSBBCs and MCs. From a financial point of view, the determined semiconductor chip area reduction implicitly defines the prize level for commercial SiC power semiconductors, which should then be not more than a factor of two more expensive compared to current Si IGBT devices. Currently, this seems to be very difficult to achieve.

CMC versus IMC

Most of the properties of the CMC and IMC are identical or at least can be achieved by adequate modulation and control. The major difference is found in the symmetry of the converter topology of the CMC compared to the IMC, which inherently leads to an even loading of all semiconductors of the CMC and thus allows for a lower semiconductor area than with the IMC. For the considered semiconductor design, the

IMC always requires a larger chip area compared with the VSBBC and CMC. It could hence be stated that the simple commutation of the IMC due to its two-stage structure is achieved at the expense of more power devices in the current path, which results in a higher semiconductor effort compared with the CMC.

The CMC should hence be selected for applications, where the conduction losses are dominant. For high switching frequency applications, where advanced (more expensive) semiconductor devices are indispensable, the IMC should be considered. Such an advanced IMC could hence be built with RC-IGBTs in the input stage that are optimized for resonant switching. (e.g. Infineon, IH-series) and thus provide a low forward voltage drop. The six switches and diodes of the output stage could be implemented with only six normally-on SiC JFETs (SiCED) as they provide an integral body diode. The IMC can then be implemented with 18 chips (similar to a CMC with RB-IGBTs), whereby only 6 SiC JFETs are required. If the same performance should be achieved with a CMC, 18 high-speed IGBTs and 18 SiC diodes (36 chips) or 18 SiC JFETs with body diodes would be required.

7.4.2 MC versus VSBBC Regarding Reliability of Passive Components

From reliability analysis it is known that inductors have a lower failure rate compared with capacitors. Depending on the considered capacitor and inductor technology, the Mean Time Between Failure (MTBF) of inductors can be up to a factor of 3 to 20 longer compared to capacitors [305]. From a conceptual point of view, a reliable topology should hence apply inductors, wherever a high electrical loading occurs as a matter of principle. Correspondingly, capacitors should be implemented, wherever the loading is potentially lower or can even be actively influenced.

Thus, the VSBBC provides an advantageous matching between the intrinsic lifetime of the passive components and their placement in the circuit topology as inductors (the boost inductors L_{B}) are utilized at the input to absorb the switched voltages and therewith the harmonic power. In the MC topology the corresponding components are capacitors (the input capacitors $C_{\mathrm{F,inp}}$) that are not only loaded by the switched load currents but also by the reactive currents at mains frequency, which leads to a non-negligible reduction of the component lifetime particularly when operated at aircraft mains input frequency (360 Hz

to 800 Hz). By inspection of (6.39) and (6.46), the maximum rms current loading per capacitance can be determined. Evaluated, for instance, for the VSBBC and MC that are designed for 32 kHz, it is found that the specific current loading of the input capacitors of the MC equals to 1.7 A/μF, whereas for the dc-link capacitor of the VSBBC it is only 0.7 A/μF. From this perspective it can be stated that with the omission of the dc-link capacitance in the MC, the lifetime limiting passive components are not eliminated but shifted to the mains side.

A further inherent advantage of the VSBBC topology is that the loading of the dc-link capacitors can be minimized by coordinating the modulation of the input and output stage, which is not possible for the input capacitors of the MC. Additionally, the dc-link capacitor allows for a more effective and flexible adjustment of the lifetime, as increasing the dc-link capacitance does not lead to an increase in the reactive power, as is the case for the MC, when more input capacitance is installed.

7.4.3 MC versus VSBBC for More Electric Aircraft Applications

Although the MC is often suggested as an alternative topology for aircraft application with a variable frequency mains system (360 Hz to 800 Hz), apart from its potential for a compact implementation, the properties of the MC do not seem to provide an optimal matching with the stringent requirements of this application area. The high mains frequency and the capacitive input filter result in a high reactive input power, which can only be compensated under the previously stated restrictions and typically at the expense of a (further) reduction of the output voltage. Moreover, the input capacitors of the MC are not only loaded by the switched load currents but are simultaneously exposed to high reactive currents. Additionally, simple feedback control of the input currents as with the VSBBC, is not possible with the MC. From this perspective a voltage source based converter system seems to be the more appropriate solution for an aircraft drive system. This finding is confirmed by the investigation performed in [221], where different converter topologies have been analyzed regarding their suitability for a lightweight, aircraft ac-ac converter system.

Regarding system reliability, shifting the capacitor from the dc-link to the mains input, as is the case for MCs, seems to be disadvantageous for converter systems operated at a high mains frequency, as the capac-

itors are not only loaded with the high-frequency block-shape currents originating from the switching similar to dc-link capacitors, but are additionally loaded by the reactive currents at mains frequency. A 10 μF X2 capacitor, for example, operated at 230 V and 800 Hz leads to a reactive capacitor current of 11.6 A and capacitor losses of approximately 3 W. Therefore, it is not surprising, that the failure rate of a dc-link capacitor can be lower (if properly designed) than the failure rate of the input filter of the input filter of a MC, which is shown by reliability comparison between the VLBBC and the CMC presented in [222].

7.4.4 Converter Application Areas

Due to its multiple intrinsic limitations, the MC does not seem to be the appropriate topology for a general purpose, flexibly configurable, bidirectional, low-voltage ac-ac converter. For such requirements, the VSBBC clearly is the preferred choice. In general, also the CSBBC is less favorable compared to the VSBBC as it has twice as many semiconductor devices in the current path and is more intricate to control compared to a voltage source converter. Additionally, for power reversal, the polarity of the link voltages needs to be changed. If a reduced efficiency is tolerably it may be applied for drives, where a sinusoidal output voltage is required and the space for an additional output filter is not available.

The MC represents a converter concept that aims at minimizing the internal energy storage. This key converter system property should be considered as an assessment criteria on whether the MC matches well its intended application. This means that for ac-ac converter applications that require internal energy storage due to high-load dynamics, single-phase operation capability, extended ride-through capability, or unconstrained reactive power compensation, the MC does not provide the most appropriate solution. Another important aspect when considering the MC as an alternative converter topology is that there should be a certain degree-of-freedom on the system design level to adapt the overall drive system to the MC (e.g. back-emf of the machine) in order to fully exploit its benefits while minimizing the impact of its limitations. A suitable load for a MC can be characterized in general as a load with a high inertia and low dynamic performance requirements. Such "MC friendly" loads and operating conditions are found, for instance, for compressor, fan, or pump drives for 50 Hz / 60 Hz mains application.

For most of these applications, actually only unidirectional power flow is required and thus also a unidirectional MC, could be utilized. Under this restriction a unidirectional IMC, also known as Ultra-Sparse Matrix Converter (USMC) [94] could be applied. However, the strong competitor of the MC technology in this application area obviously is the VSI with a B6 diode bridge rectifier (B6-VSI), which is an industrially well established and reliable converter concept allowing for a high efficiency between 97% and 98%. Since the B6-VSI enables an input power factor above 0.9 and evidently also provides compliance to the considered Class B (CISPR 11) EMI standards, the main advantages of the USMC compared to the B6-VSI is its potential for reducing the volume of the passive components and the sinusoidal input currents. However, by utilizing the same semiconductor technology the USMC cannot achieve the efficiency of the B6-VSI.

In conclusion, in the low-voltage and low-power ac-ac converter segment, the MC technology seems to be restricted to niche-applications.

7.5 Future Work

7.5.1 Reliability of AC-AC Converter Systems

Reliability is one of the most important performance indices of a power electronic converter system. In this work, reliability aspects were considered for the passive component design, particularly for dimensioning the dc-link and filter capacitors, in order to ensure a predefined minimum lifetime. For future research work, the derived inner converter dependencies could be used to derive reliability models of the considered ac-ac converter topologies and to investigate the reliability of the power semiconductors and the semiconductor modules for different converter systems and operating points.

The modeling of reliability to predict the lifetime of a semiconductor module, however, is difficult due to a large number of operating conditions, the lack of data when a module fails in the field, the often long lifetime, and the small production lots compared to other electronic components. These conditions often hinder the compilation of a statistically relevant failure data base, which is a prerequisite for developing accurate models for lifetime prediction.

Traditionally, the main failure modes of power modules are bond wire lift-off and cracks in the interfacing (solder) layers between the chip and the DBC or the DBC and the base plate. These thermo-mechanical failures basically originate from the different thermal expansion of two materials, leading to mechanical stress at the material boundaries. This may result in a damage of the material interface and ultimately in a failure of the semiconductor module.

The aim of the following considerations is to identify quantities, inherently provided by the SAC2, that can be used to assess the reliability of a converter topology with respect to its semiconductor module. Without studying the individual deformation mechanisms such as dislocation glide, dislocation creep, or diffusion creep in detail, all these failure mechanisms have in common that the deformation energy is provided by the difference of the loss energy of the semiconductor chip and the energy dissipated through the cooling system and the surface of the package (conservation of energy). Ultimately, the instantaneous difference of the loss energy and the energy dissipated by the cooling system results in a variation of the junction temperature. This means that the progression of the junction temperature is related to the failure mechanism of a chip in a semiconductor module and can thus be used for failure rate predictions. Consequently, in many models for predicting the reliability of semiconductor modules, the junction temperature is used as an input quantity. A review of models for lifetime prediction of power modules is presented in [306].

Based on the above considerations, a Failure Prediction Quadruple (FPQ) is suggested to compare the failure probability respectively the reliability of the semiconductor modules of the compared ac-ac converter topologies.

$$\mathrm{FPQ} = \left\{ T_\mathrm{J}, \Delta T_\mathrm{J}, \left| \frac{\partial T_\mathrm{J}}{\partial t} \right| \Big|_{\mathrm{avg}}, f_{\Delta \mathrm{T_J}} \right\} \tag{7.3}$$

The lowest failure rate and therewith highest reliability is expected when all elements of the FPQ are minimal. The average junction temperature T_J models the temperature dependent aging mechanisms and can be compared with an activation energy. The variation of the junction temperature (junction temperature swing) ΔT_J accounts for the energy difference involved in a temperature cycle and allows the determination of the minimal and maximal junction temperature. The average gradient

of the junction temperature

$$\left|\frac{\partial T_{\mathrm{J}}}{\partial t}\right|\Bigg|_{\mathrm{avg}} = f_{\Delta \mathrm{T_J}} \int_0^{1/f_{\Delta \mathrm{T_J}}} \left|\frac{\partial T_{\mathrm{J}}}{\partial t}\right| dt \tag{7.4}$$

is a measure for the homogeneity of the temperature variation. Finally, the frequency of the temperature cycle $f_{\Delta \mathrm{T_J}}$ considers the time dependency of the failure mechanisms. The advantages of the SAC2 with respect to the reliability prediction are twofold: Firstly, all quantities of the FPQ can be extracted from the calculation and optimization algorithm of the SAC2. Secondly, when the required semiconductor area of a converter topology is determined for a given operating point, with the criterion of an equal average junction temperature a common basis is not only provided for the comparison of the semiconductor areas but also for the comparison of the failure probability.

It should be noted that the FPQ based failure prediction only provides a comparative criterion. The sensitivities of the four input quantities on the total lifetime and the absolute value of lifetime of a semiconductor module can only be determined with a detailed reliability model, which needs to be parameterized with statistically significant failure data. These data sets depend on many parameters such as the module assembly structure, the packaging technology, the production process, the quality management, and most importantly the test procedure that was used to acquire the failure data. Consequently, the main point in favor of the suggested FPQ based comparative analysis is that it provides general criteria.

7.5.2 Stability of AC-AC Converter Systems in Smart Grids

In a similar manner as in this thesis, a comprehensive stability analysis of three-phase ac-ac converter topologies could be performed in the emerging field of research on smart grids, where many power electronic converter systems are expected to interact with each other in future.

The aim of this research would be to investigate on whether a certain converter concept (e.g. voltage source, current source, or matrix converter) would (inherently) provide significant advantages or disadvantages regarding stability and to identify and quantify stability margins for different characteristic converter topologies.

7.5.3 Advanced Control Strategies for MCs

Although a wide variety of control strategies have already been analyzed for MCs, there are still a few strategies that have been hardly investigated until now. These control strategies, however, might be rather of academic interest as most of the characteristic limitations of MCs remain the same.

One idea is to analyze on whether the motor load of a MC for applications with low dynamic requirements (e.g. fan or pump drives) could be used as a dynamic energy storage by magnetizing and demagnetizing (primarily) the d-axis. This energy might then be used to enhance the converter stability.

Another option is to try to improve the input current quality of MCs by feedback control of the input currents and feedforward control of the output currents at the expense of a reduced output current control performance. A similar approach is suggested in [307] for the input current control of a CSR. Such a control strategy is of particular interest for the USMC in combination with the basic modulation strategy B (cf. Fig. 3.9), which enables ZVS of the output. The switching frequency of the input stage is twice the switching frequency of the output (could theoretically be even more) for this modulation scheme. The input stage could then even be operated such that the relative turn-on times of the input stage are updated at the beginning and in the middle of the pulse period of the output stage (double-up-date mode).

Appendix A

Hardware Prototypes

A.1 Overview

This section presents the ac-ac converter prototypes implemented within the scope of this thesis to experimentally verify the analytical converter models and to investigate the in-system performance of the SiC power semiconductors. For every hardware prototype, firstly, the motivation for its implementation is stated, followed by a brief description of the design, the construction concept, and characteristic measurement results. The description of a converter prototype is completed with a compilation of its main specifications and key performance figures such as the measured efficiency and THD, the power density, the power-to-weight ratio, etc. including an indication of the utilized active semiconductor chip area.

The measurement quantity to be specified at this point is the input current THD which is determined in accordance to the IEC 61000 standards for the first 100 harmonic input current components. For a 50 Hz mains system, this leads to a THD measurement frequency range from 50 Hz to 5 kHz. The THD is measured with a Norma D6100 power analyzer and/or by post-processing of high-resolution current measurement data based on (6.47).

A.2 RB-IGBT Indirect Matrix Converter

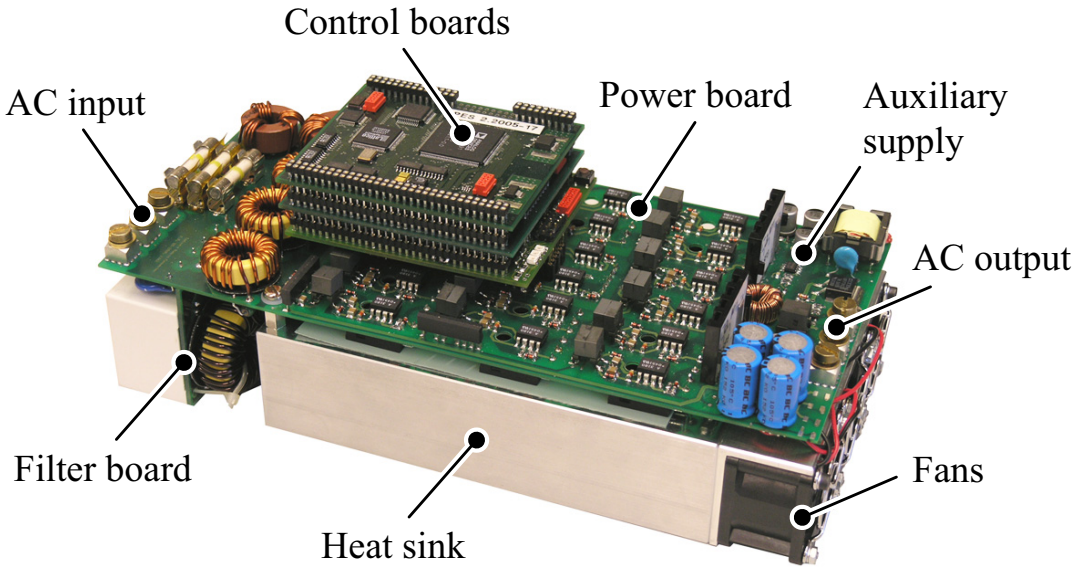


Fig. A.1: Indirect Matrix Converter (RB IMC) prototype, with RB-IGBTs in the input stage and conventional IGBTs in the output stage.

A.2.1 Motivation

The motivation for the implementation of this hardware prototype is to provide an universally applicable IMC system and to simultaneously investigate the performance of RB-IGBTs.

IMCs offer a reduced complexity modulation compared to CMCs as presented in Chap. 1 and Chap. 3. Indirect MC topologies typically have more semiconductor devices in the current path than the CMC topology, which results in higher conduction losses at the nominal operating point. The availability of RB-IGBTs enables the implementation of a bidirectional switch, as required for the input stage of the IMC, by employing only two devices connected in anti-parallel. Thus, the RB IMC prototype with RB-IGBTs in the input stage and conventional NPT IGBTs in the output stage does not only allow for a reduction of the component count of the input stage but also to take advantage of the lower forward voltage drop of the RB-IGBT compared to a series connection of a discrete IGBT and diode with equal current and voltage ratings. However, the switching losses of the utilized RB-IGBTs (IXRH40N120) can be high due to the non-optimal switching behavior

with large tail currents [167]. A solution is to apply a ZCS strategy for the input stage, which is inherently given by the default modulation scheme (HVSMV) considered in this work for the IMC. This enables to benefit from the low on-state characteristics of the RB-IGBTs without increasing the total losses due to their unfavorable switching behavior and indicates that the IMC is a well suited topology for the use of RB-

Quantity	*Value*
Nominal input line-to-line voltage	$3 \times 400\,\mathrm{V}$, $50\,\mathrm{Hz}$
Nominal output power	$6.2\,\mathrm{kW}$
Output line-to-line voltage	$0\,\mathrm{V} \ldots 340\,\mathrm{V}$
Output frequency	$0\,\mathrm{Hz} \ldots \pm 250\,\mathrm{Hz}$
Output current displacement	$0° \ldots 360°$
Input stage switching frequency	$12.5\,\mathrm{kHz}$
Output stage switching frequency	$25\,\mathrm{kHz}$
Maximum ambient temperature	$55°\mathrm{C}$
Default modulation scheme	HVSVM
EMI compatibility standard	CISPR 11, Class A
Input stage semiconductors	1200 V, 28 A RB-IGBTs IXYS, IXRH40N120
Output stage semiconductors	1200 V, 32 A phase-legs, IXYS, FII50-12E
Active chip area of the RB-IGBTs	$464\,\mathrm{mm}^2$
Active chip area of the IGBTs	$144\,\mathrm{mm}^2$
Active chip area of the diodes	$72\,\mathrm{mm}^2$
Efficiency at nominal operation	94.5%
Input current THD (with a HAC-145 IM at 3.3 kW)	5.2%
Power density	$2.5\,\mathrm{kW/liter}$
Specific power	$2.5\,\mathrm{kW/kg}$
Dimensions	$260\,\mathrm{mm} \times 120\,\mathrm{mm} \times 80\,\mathrm{mm}$
Weight	$2.5\,\mathrm{kg}$

Tab. A.1: RB IMC specifications summary.

IGBTs. The specifications of the implemented RB IMC are summarized in Tab. A.1. Additional information about this converter prototype can be found in [167].

In the course of this thesis, the RB IMC prototype served as a "workhorse" for numerous EMI measurements to test the input filter design methods, for the verification of the semiconductor loss models, and for the experimental evaluation of different modulation schemes.

A.2.2 Design

The RB IMC hardware, presented in Fig. A.1, consists of three main parts:

- the power board with the heat sink, which includes the power semiconductors, the gate drives, the auxiliary power supply, the current sensors, and parts of the input filter,
- the filter board with parts of the DM input filter and surge protection, and
- a pluggable stack of control boards that is composed of a, and
  - measurement and signal conditioning board,
  - a PWM generation board with two interconnected PLDs (Lattice ISPMach4512V), incorporating different modulation strategies,
  - and a DSP (Analog Devices ADSP-21992) control board, providing a software link to a computer and hardware monitoring with a scope.

The cooling system is designed based on the calculated semiconductor losses at nominal output power in order to maintain the maximum junction temperatures of all power semiconductors below 130°C. The cooling system comprises three high performance fans (Sanyo Denki, San Ace 40/28 1U) and a customized aluminum heat sink (180 mm × 120 mm × 43 mm), dimensioned according to [308]. The resulting thermal resistance between the heat sink and the ambient air equals to $R_{\mathrm{th,SA}} = 0.07\,\mathrm{K/W}$. The three phase-leg modules of the output stage are placed along the center line of the heat sink as they generate higher losses than the RB-IGBTs of the input stage that are placed on both sides of the output stage devices.

A.2.3 Experimental Results

The switching performance of the RB-IGBTs is investigated using the measurement circuit, shown in Fig. A.2. It enables to simulate the current commutation between two input phases of the IMC. Fig. A.3(a) and Fig. A.3(b) depict the current and voltage waveforms of the RB-IGBT S_{ap} when the load current i_{L} is commutated from S_{ap} to S_{bp} by applying ZCS.

The interlock delay time of the input stage of 1.5 μs is determined based on the switching performance measurements of the RB-IGBTs (cf. Fig. A.3). It is adjusted to minimize the (parasitic) switching losses in the input stage, generated mainly by the tail currents of the RB-IGBTs. A further increase of this delay time would not lead to a considerable reduction of the input stage losses. By lowering the interlock delay of the input stage, the input current waveforms and therewith also the THD can be improved. However, the switching losses would then increase because the time for the remaining charge carriers (causing the tail current) to recombine, before the next switching action takes place, is reduced.

Fig. A.4(a) and Fig. A.4(b) present waveforms of the link voltage u, the current i_{b} of the input phase b, and the current i_{B} of the output phase B. The link voltage features the characteristic shape of the selected HVSVM scheme. The measurements prove that the designed IMC is capable of generating sinusoidal input and output currents, and that the desired matrix converter functionality can be achieved with RB-IGBTs in the input stage.

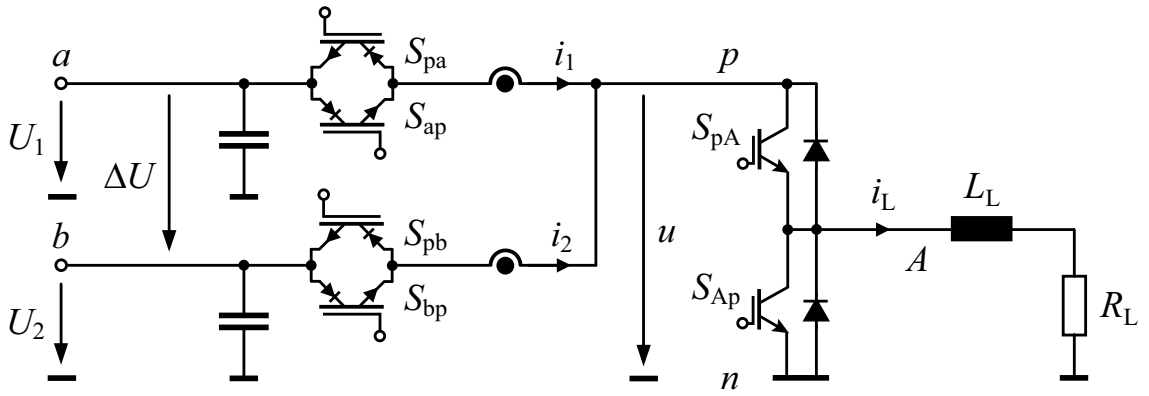


Fig. A.2: Schematic of the switching performance and switching loss measurement circuit for the RB-IGBTs.

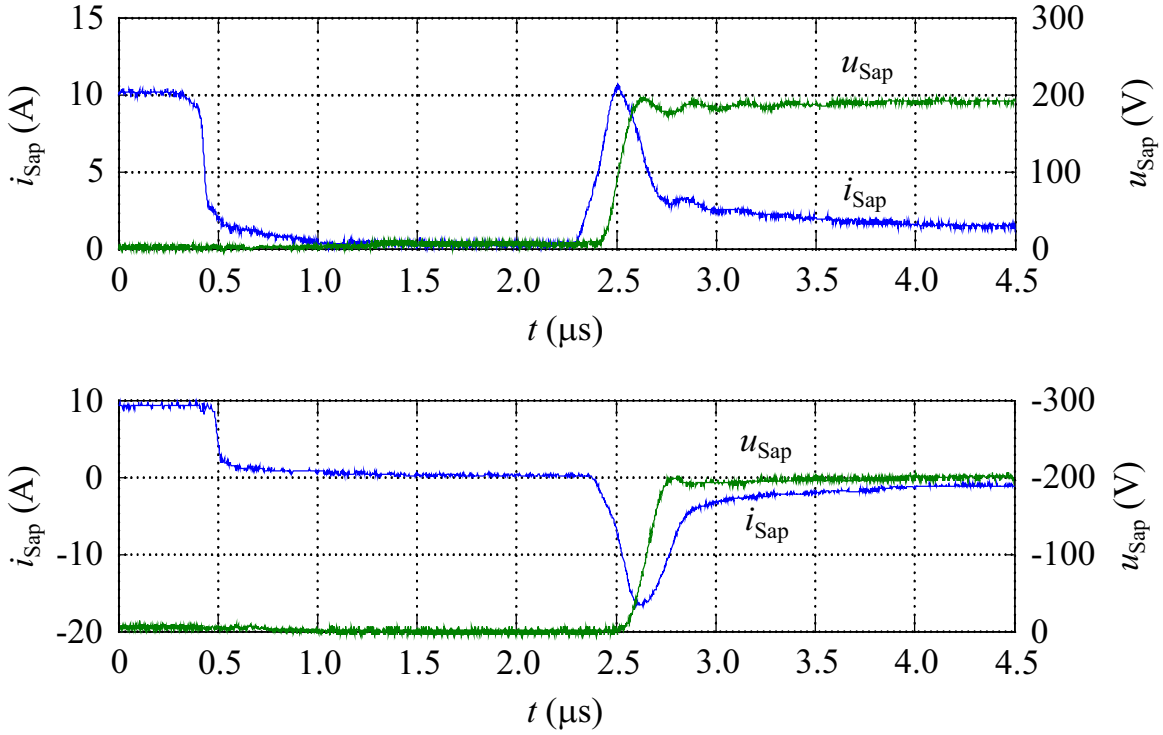


Fig. A.3: Measured **(a)** turn-off and **(b)** turn-on switching waveforms of the RB-IGBT S_{ap}, when ZCS is applied. The commutation voltage equals to $\Delta U = 200\,\mathrm{V}$ and the switched load current to $i_{\mathrm{L}} = 10\,\mathrm{A}$.

An important aspect of the RB IMC is the commutation between the RB-IGBTs of the corresponding input phases when the difference of the two input line-to-line voltage levels applied to the link is zero. In this case also the resulting commutation voltage equals zero, which leads to a slow commutation and results in an increased input current distortion. This occurs six times within a mains period and corresponds to the contractions in the link voltage pattern (cf. Fig. A.4, label (1)).

In order to evaluate the switching behavior of the RB-IGBTs in the RB IMC hardware, the switching waveforms are measured for the situation, where S_{ap} is clamped and the link current is commutated between S_{nb} and S_{nc}. The measurements are performed for the worst case condition, when the RB-IGBTs conduct the maximum output current of the actual operating point, right before the output stage is switched to the active state. The resulting switching transients are presented in Fig. A.5, showing the collector-emitter voltages of the RB-IGBTs S_{nb} and S_{nc}. The achieved switching time is approximately 200 ns.

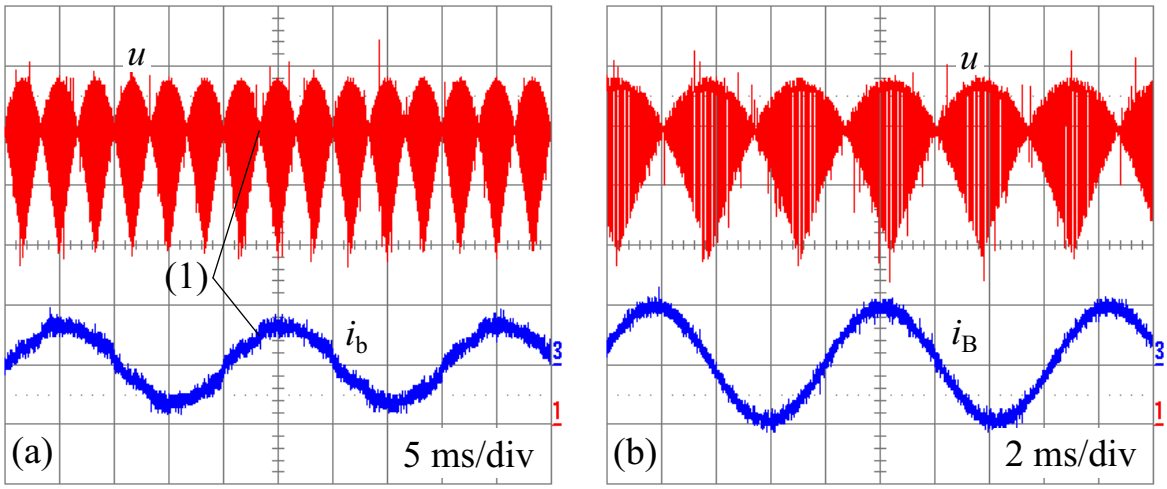


Fig. A.4: Link voltage, input phase current, and output phase current waveforms at $U_1 = 230\,\mathrm{V}$, $f_1 = 50\,\mathrm{Hz}$, and $f_2 = 125\,\mathrm{Hz}$. **(a)** u: link voltage, $100\,\mathrm{V/div}$; i_b: current of the input phase b, $5\,\mathrm{A/div}$. (1) indicates an example of a slight distortion of the input current that occurs at the contractions of the dc-link voltage. **(b)** u: link voltage, $100\,\mathrm{V/div}$; i_B: current of the output phase B, $5\,\mathrm{A/div}$.

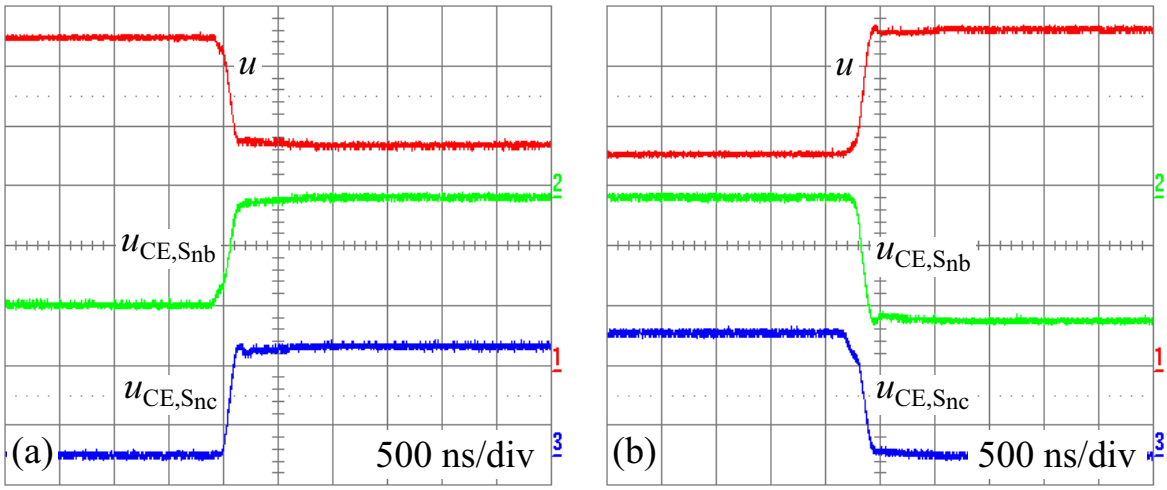


Fig. A.5: Link voltage and collector-emitter voltages of the RB-IGBTs for **(a)** turn-on of S_nb and turn-off of S_nc and **(b)** turn-off of S_nb and turn-on of S_nc at $U_1 = 230\,\mathrm{V}$ and $f_1 = 50\,\mathrm{Hz}$. u: link voltage, $100\,\mathrm{V/div}$; $u_\mathrm{CE,Snb}$: collector-emitter voltage of the RB-IGBT S_nb, $100\,\mathrm{V/div}$; $u_\mathrm{CE,Snc}$: collector-emitter voltage of the RB-IGBT S_nc, $100\,\mathrm{V/div}$.

A.3 Si-SiC Ultra Sparse Matrix Converter

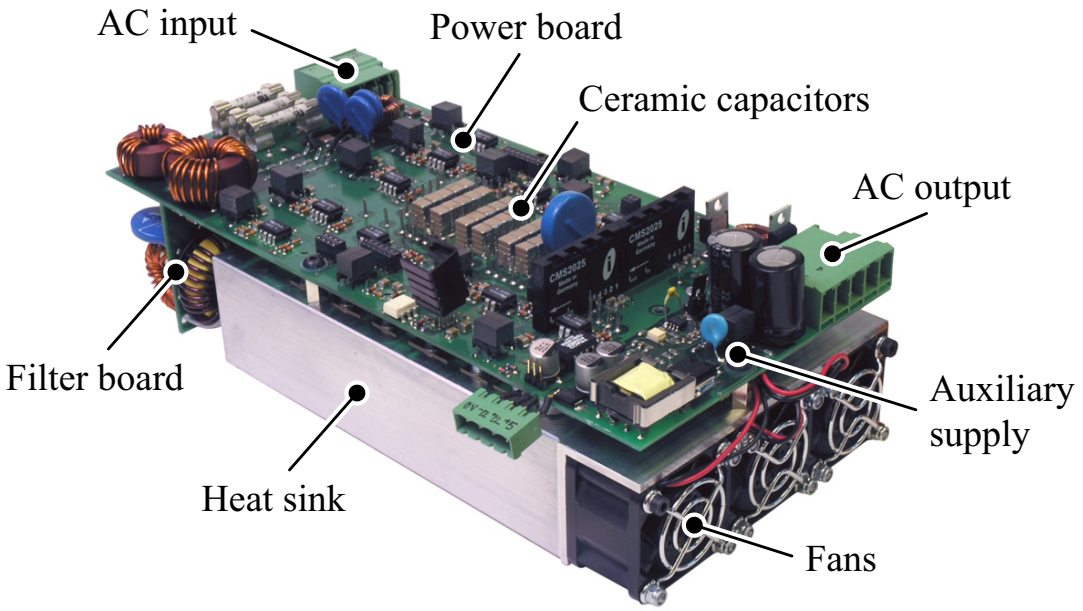


Fig. A.6: Si-SiC Ultra Sparse Matrix Converter (Si-SiC USMC) prototype with Si or SiC Schottky freewheeling diodes in the output stage.

A.3.1 Motivation

The USMC is the simplest topology of the family of Indirect Matrix Converters as it can only provide unidirectional power flow. Similar to the IMC, also for the USMC the HVSVM modulation scheme is applied, which enables zero current commutation of the input stage. The main switching losses are generated in the output stage. The simplified input stage switch configuration of the USMC topology restricts the maximum displacement angle between input and output voltages and currents to $\pm\pi/6$. An active clamp circuit is therefore employed to protect the converter from experiencing over-voltages when the restriction of the phase displacement at the output is not fulfilled.

The purpose for the implementation of this USMC prototype is to experimentally investigate its operating behavior with a PMSM and the achievable performance gain by replacing the 1200 V Si freewheeling diodes of the output stage by SiC Schottky diodes, when the output stage is operated at 50 kHz. Thereby, the SiC Schottky diodes should have an equivalent forward voltage drop at nominal output current as

the conventional Si diodes. A summary of the specifications of the Si-SiC USMC prototype is provided in Tab. A.2. Further technical data on the basic functional principle of an USMC and on the design of this prototype are compiled in [143].

Quantity	*Value*
Nominal input line-to-line voltage	$3 \times 400\,\mathrm{V}$, $50\,\mathrm{Hz}$
Nominal output power	$5.5\,\mathrm{kW}$
Output line-to-line voltage	$0\,\mathrm{V} \ldots 340\,\mathrm{V}$
Output frequency	$0\,\mathrm{Hz} \ldots \pm 250\,\mathrm{Hz}$
Output current displacement angle	$0° \ldots \pm 30°$
Input stage switching frequency	$25\,\mathrm{kHz}$
Output stage switching frequency	$50\,\mathrm{kHz}$
Maximum ambient temperature	55°C
Default modulation scheme	HVSVM
EMI compatibility standard	CISPR 11, Class A
Input stage semiconductors	1200 V, 32 A BD-switches IXYS, FII50-12BD 1200 V, 60 A diodes IXYS, DSEP60-12AR
Output stage semiconductors	1200 V, 32 A phase-legs, IXYS, FII50-12E-SiC
Active chip area of the Si IGBTs	$216\,\mathrm{mm}^2$
Active chip area of the Si diodes	$384\,\mathrm{mm}^2$
Active chip area of the SiC diodes	$36\,\mathrm{mm}^2$
Efficiency at nominal operation	94%
Input current THD (with a LST-127 PMSM at 3 kW)	3.6%
Power density	$2.2\,\mathrm{kW/liter}$
Specific power	$2.2\,\mathrm{kW/kg}$
Dimensions	$260\,\mathrm{mm} \times 120\,\mathrm{mm} \times 80\,\mathrm{mm}$
Weight	$2.5\,\mathrm{kg}$

Tab. A.2: Si-SiC USMC specifications summary.

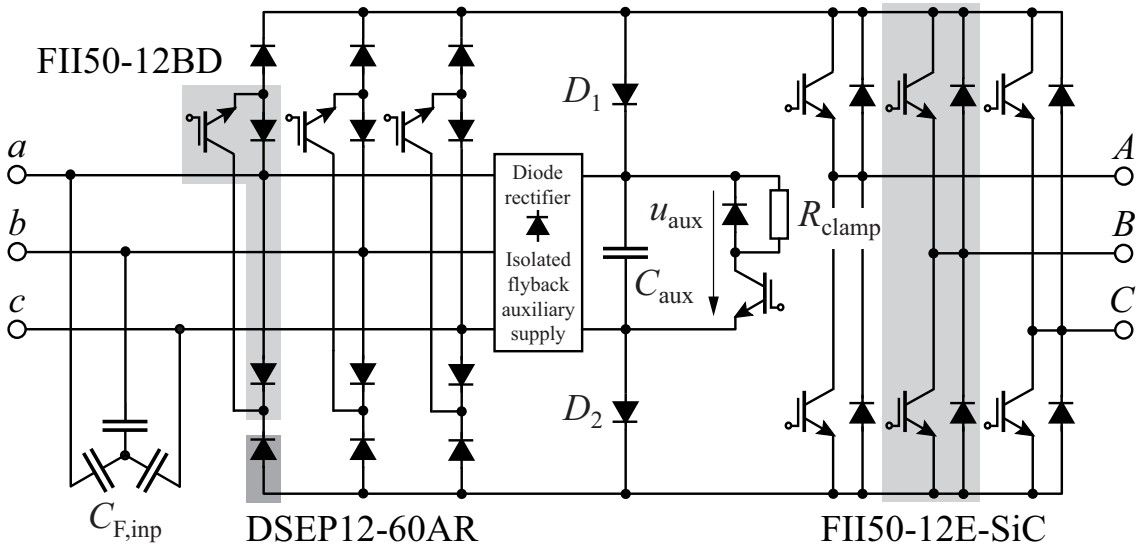


Fig. A.7: Schematic of the USMC, showing the different semiconductor devices and the integration of the active clamp with the auxiliary supply.

A.3.2 Design

The layout and most of the components of the Si-SiC USMC are identical with the RB IMC. The main differences of the USMC hardware, shown in Fig. A.6, are found in the unidirectional input stage and the additional active clamp circuit. The foil capacitors at the input of the RB IMC are replaced by a custom made bank of stacked ceramic chip capacitors (Murata, GA255-series, X7R, 100 nF per chip), which is situated in the center of the power board. All power switching devices are placed directly around these capacitors to minimize the parasitic series inductance for the currents drawn by the input stage to enable high switching frequency operation.

For the all-Si version of the USMC, the same IXYS FII50-12E phase-legs are utilized for the output stage as for the RB IMC. Each IGBT and inner diode combination of an input phase-leg is implemented with an IXYS FII50-12BD module. The additional diodes of the input stage, which are directly connected to the positive or the negative bus of the link, are implemented with discrete IXYS DSEP60-12AR diodes. Customized IXYS FII50-12E-SiC modules are employed (cf. Sec. 2.5) for the semiconductor configuration with SiC Schottky freewheeling diodes in the output stage, providing the same pin-out and bonding as the commercially available FII50-12E devices. The individual semiconductors utilized for this prototype are highlighted in the schematic in Fig. A.7.

Compared with the RB IMC, in the latest USMC prototype, the stack of control boards is replaced by a single measurement and control board that can be directly plugged into the power board. This control board comprises a Texas Instruments TMS320F2808 DSP and a Lattice MachXO LCMXO2280C FPGA. It is important to note, that the whole modulation, PWM generation, and motor control of the USMC is implemented in the DSP. The FPGA is only used for safety reasons to provide hardware error detection and shutdown capability, and to control the active clamp independently of the DSP. This clearly shows that contrary to the CMC, for the practical implementation of an USMC (or IMC), no special control hardware, as for example intelligent gate-drives to detect the direction of the current, is required.

For dynamic regenerative loads such as motors, reverse current flow is unavoidable and a clamp circuit is needed to provide a current path for negative link currents. An active clamp circuit is integrated with the auxiliary supply as depicted in Fig. A.7. The advantage of connecting the clamp circuit across the auxiliary supply capacitor C_{aux} instead of directly across the link is twofold: the auxiliary supply dc-bus voltage provides a more stable voltage measurement than the switched link voltage. If clamping was performed on the link, it would fluctuate significantly, since it contains no storage. Additionally, the clamping diodes D_1 and D_2, implemented with 1200 V, 10 A SiC Schottky diodes (CREE, C2D10120), provide the converter with a ride-through and shutdown capability. During mains power outages, for instance, the motor can be decelerated by feedback controlled generator operation to provide sufficient power to the dc-bus of the auxiliary supply. This keeps the control hardware active and ensures a controlled ride-through or shutdown of the system. Thus, during regeneration of the load the USMC becomes a VSI with a reduced dc-link capacitor ($C_{\mathrm{aux}} = 11\,\mu\mathrm{F}$, $R_{\mathrm{clamp}} = 60\,\Omega$). The clamp is controlled by a hysteresis control of the dc-bus voltage u_{aux} of the auxiliary supply. In parallel to the active clamp, a varistor is implemented to provide passive over-voltage protection.

A.3.3 Experimental Results

The experimental results demonstrate that the reduced switch configuration of the input stage performs as desired and the USMC can generate sinusoidal currents at both the input and output (cf. input current THD in Tab. A.2). The following measurements show waveforms of the

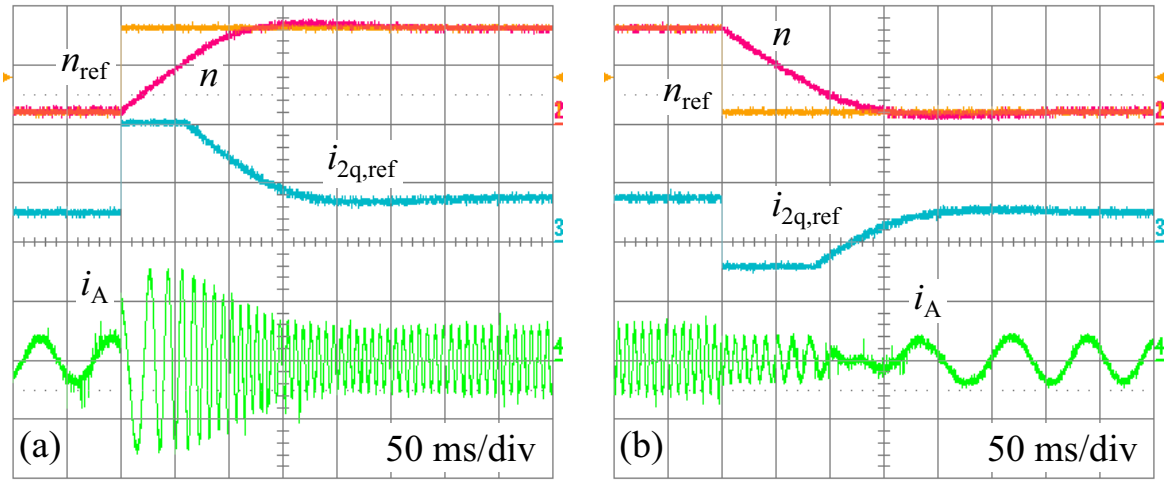


Fig. A.8: (a) Acceleration from 300 rpm to 2700 rpm and **(b)** deceleration from 2700 rpm to 300 rpm at $U_1 = 230\,\mathrm{V}$ and $f_1 = 50\,\mathrm{Hz}$. n_{ref}: reference motor speed, 1800 rpm/div; n: actual motor speed, 1800 rpm/div; $i_{2\mathrm{q,ref}}$: output q-axis reference current, 8 A/div; i_{A}: current of the output phase A, 10 A/div.

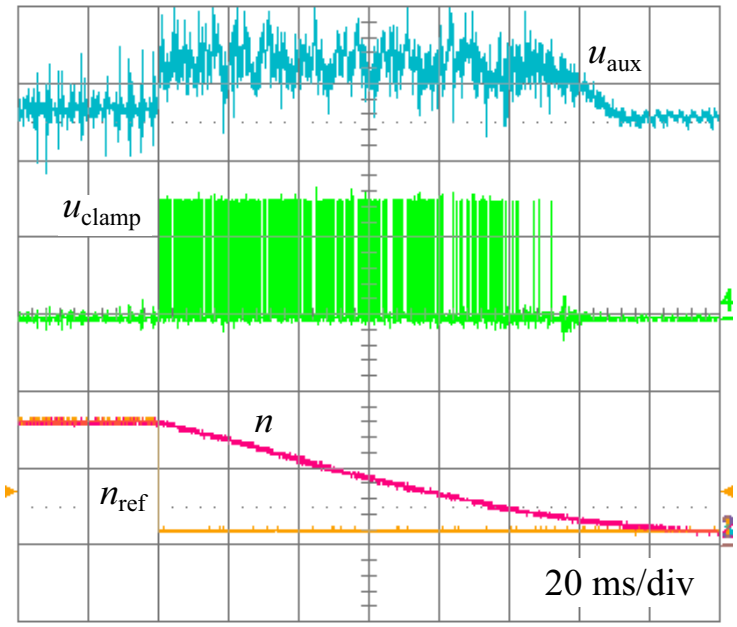


Fig. A.9: Deceleration from 2700 rpm to 300 rpm at $U_1 = 230\,\mathrm{V}$ and $f_1 = 50\,\mathrm{Hz}$. n_{ref}: reference motor speed, 1800 rpm/div; n: actual motor speed, 1800 rpm/div; u_{aux}: dc-bus voltage of the auxiliary supply, 100 V/div; u_{clamp}: clamp control signal, 2 V/div.

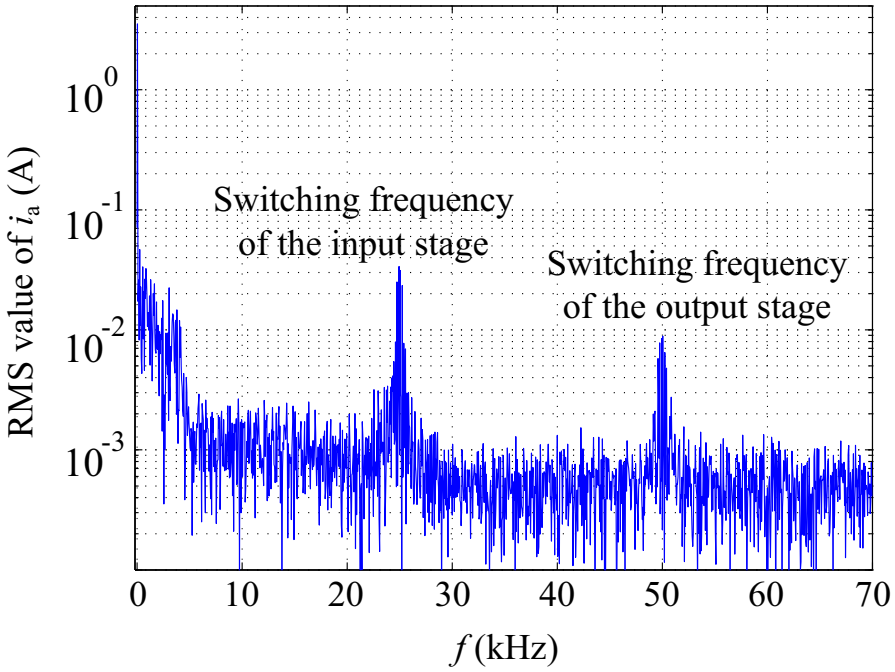


Fig. A.10: Spectrum of the input phase current i_a from 0 kHz to 70 kHz at an output power of 3 kW.

USMC prototype, when supplying a LST-127 PMSM (cf. Tab. A.7). In Fig. A.8(a) and Fig. A.8(b), the accelerating and decelerating process is shown. As can be seen in Fig. A.8(b), during deceleration the measured motor speed n and the output phase current i_A show a continuous progression, indicating that the clamping concept functions properly. Fig. A.9 presents the deceleration process in more detail and demonstrates the ability of the active clamp circuit to protect the converter from experiencing over-voltages.

As is known from Chap. 3, for the selected HVSVM modulation scheme the switching frequency of the input stage is half the switching frequency of the output stage; in this case 25 kHz at the input and 50 kHz at the output. Fig. A.10 presents the spectrum of an input phase current of the USMC, showing the two main spectral components at 25 kHz and 50 kHz. The peak labeled in Fig. A.10 with "Switching frequency of the input stage" is generated by the switching of the output stage. It is therefore only marginally influenced by the actual switching of the input stage as for the HVSVM modulation scheme the input stage is switched at zero current. Consequently, the spectral components at 25 kHz are primarily generated due to the change of the switching

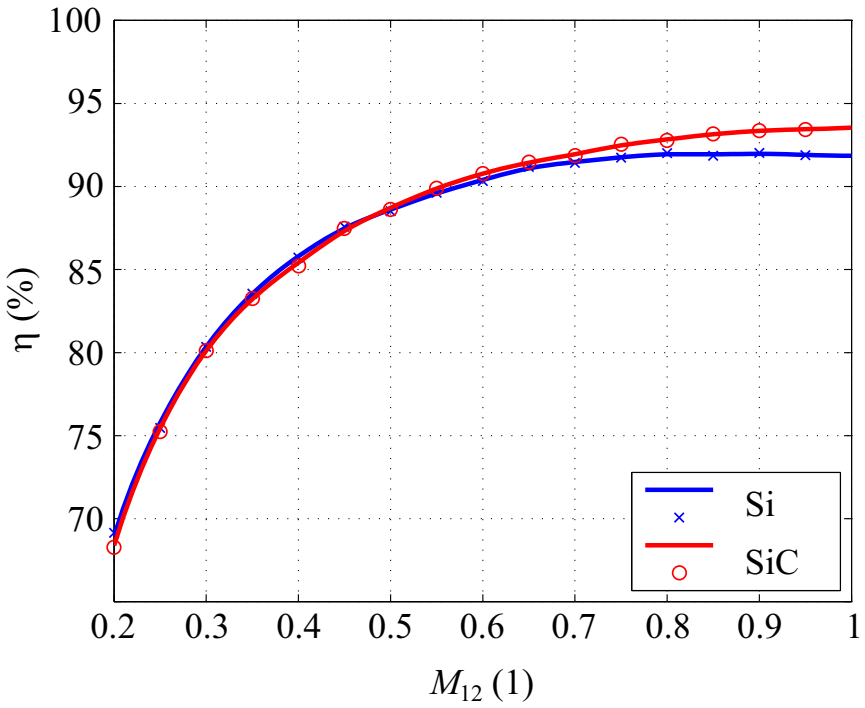


Fig. A.11: Efficiency η versus modulation index M_{12} with Si and SiC Schottky freewheeling diodes.

state and the clamping of the input stage (e.g. state (ac), (ab)), whereas the spectral components at 50 kHz originate from the switching of the output stage.

Finally, the results of the efficiency comparison between the USMC with Si and SiC Schottky freewheeling diodes in the output stage are briefly discussed. The efficiency is defined as

$$\eta = \frac{P_2}{P_1} \,. \tag{A.1}$$

In this comparison, the converter efficiency is measured for a modulation index M_{12}, ranging from 0.2 to 1 at an electrical output frequency $f_2 = 40\,\text{Hz}$. For that purpose, the USMC is connected to a linear three-phase RL load with a resistance of $21.5\,\Omega$ and an inductance of 2.5 mH per phase, leading to a phase displacement angle $\Phi_2 < 2°$. The resistance is adjusted such that for $M_{12} = 1$ the converter is operated at nominal output power. Fig. A.11 depicts the efficiency curves versus the modulation index for both semiconductor configurations. The parameter sweep of M_{12} from 0.2 to 1 corresponds to an output power range of 0.2 kW to 5.5 kW for the given load. As can be seen from the efficiency

curves, for nominal operation at $M_{12} = 1$, the All-Si USMC features an efficiency of 92%. The USMC with SiC diodes achieves an efficiency of 94%, which is equivalent to a reduction of the total semiconductor losses of 25%. As is shown in Sec. 2.4.3, the customized FII50-12E-SiC phase-leg modules with SiC Schottky diodes is designed such that at 15 A, which corresponds to the nominal output current of the USMC, the conduction losses of the Si and SiC diodes are identical. The gain in efficiency with SiC diodes for an increasing modulation index can be explained as follows: Due to the linear characteristic of the load, the output current increases proportionally to the modulation index. Therewith also the turn-off (reverse recovery) losses of the Si freewheeling diodes increase. For a modulation index below 0.6, the converter efficiency is the same for both diode configurations, since the absence of reverse recovery losses of the SiC diodes is outweighed by their higher forward voltage drop at low current levels compared to the Si diodes.

The efficiency measurements clearly show that the mission profile of the drive determines whether the replacement of the Si diodes with SiC diodes is worthwhile and pinpoints the importance of a holistic consideration when selecting the semiconductor technology of an ac-ac converter for a given drive application.

A.4 All-SiC Indirect Matrix Converter

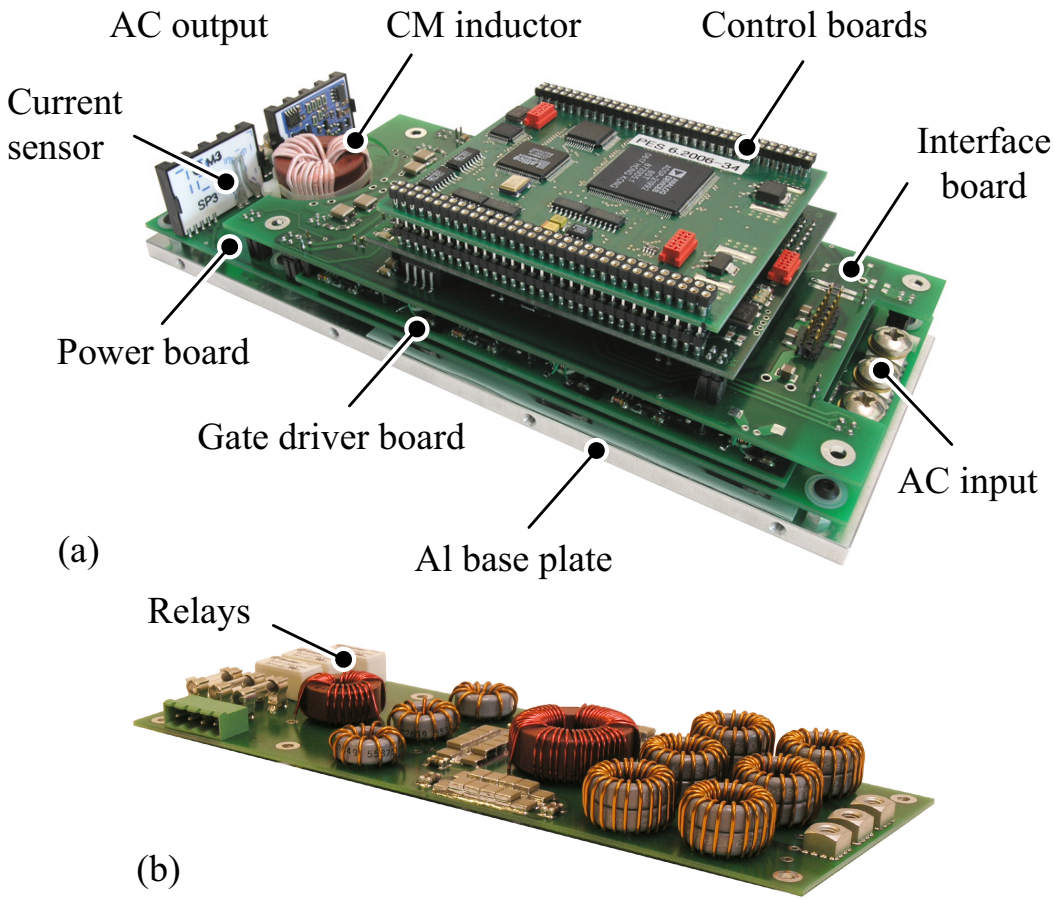


Fig. A.12: (a) All-SiC Indirect Matrix Converter (All-SiC IMC) prototype with **(b)** EMI input filter board.

A.4.1 Motivation

The All-SiC IMC prototype is constructed to analyze the in-system performance of state-of-the-art normally-on SiC JFET pre-series devices for a demanding ac-ac converter application and to verify the converter models. The target switching frequency is set to 200 kHz, well aware that 200 kHz is within the considered (CISPR 11, Class A) EMI measurement range that starts at 150 kHz. The reason for selecting such high switching frequency is to provide a large enough switching frequency range for testing. The main specifications of the All-SiC IMC are compiled in Tab. A.3. Further data of this prototype are summarized in [170].

Different advantages are associated with the IMC topology in view of the properties of the SiC JFETs. Since the IMC comprises both bidirectional switches in the input stage and bridge-legs with anti-parallel diodes in the output stage, it provides an attractive topology for testing new devices. Additionally, the SiC JFETs have an intrinsic body diode and thus enable the implementation of a bidirectional switch with only two devices. Due to the absence of a dc-link capacitor, initial failures that may result from the normally-on characteristic of the JFETs cannot lead to a short circuit of a large energy storage, which would potentially destroy the whole prototype.

Quantity	*Value*
Nominal input line-to-line voltage	$3 \times 400\,\mathrm{V}$, $50\,\mathrm{Hz}$
Nominal output power	$2.8\,\mathrm{kW}$
Output line-to-line voltage	$0\,\mathrm{V} \ldots 326\,\mathrm{V}$
Output frequency	$0\,\mathrm{Hz} \ldots \pm 1000\,\mathrm{Hz}$
Output current displacement angle	$0° \ldots 360°$
Input stage switching frequency	$100\,\mathrm{kHz}$
Output stage switching frequency	$200\,\mathrm{kHz}$
Default modulation scheme	HVSVM
EMI compatibility standard	CISPR 11, Class A
Semiconductors	1200 V, 6 A normally-on SiC JFETs, SiCED
Active chip area of the SiC JFETs	$72\,\mathrm{mm}^2$
Efficiency at nominal operation	93.5%
Input current THD (at nominal operation with an *RL* load)	2.5%
Power density	$2.2\,\mathrm{kW/liter}$
Specific power	$2.8\,\mathrm{kW/kg}$
Dimensions	$220\,\mathrm{mm} \times 80\,\mathrm{mm} \times 73\,\mathrm{mm}$
Weight	$1.0\,\mathrm{kg}$

Tab. A.3: All-SiC IMC specifications summary.

A.4.2 Design

Compared with the physical construction of the RB IMC or the Si-SiC USMC, the All-SiC IMC, shown in Fig. A.12, is designed as a stacked arrangement of PCBs with the SiC JFETs mounted on an aluminum base plate. This base plate has a thickness of 6 mm and forms the thermal interface between the TO-220 packages of the JFETs and an arbitrary cooling system, which can be either a conventional forced air-cooled or a liquid-cooled heat sink or the case of an electric motor.

The splitting of the power circuit into a gate drive and a power board enables a small footprint design and the placement of the ceramic input capacitors (Murata, GA255-series) close to the terminals of the JFETs without increasing the distance from the gate drive circuit to the gate. A further advantage of this design approach is that it allows for a separation of tracks carrying the switching currents from the signal circuitry of the gate driver board.

A CM output filter is constructed with a single toroidal core which is mounted in a cut-out in the power board and the base plate to reduce the CM voltage and the dv/dt applied to the load. The EMI input filter is placed on a separate board. It can be mounted on top of the control boards and connected to the ac input terminals of the power board.

The main control loop of the DSP (Analog Devices, ADSP-21992) is executed at a frequency of 33 kHz and therefore updates the space vector sequences and turn-on times of the JFETs every third pulse period. The pulse patterns are generated by a FPGA (Lattice, MachXO LCMXO2280C) with a resolution of 10 ns, leading to a total of 500 different discrete values for the modulation index.

Special attention is paid to the implementation of the normally-on SiC JFETs as there are three fundamentally different options.

- The most straightforward approach, which is applied to the All-SiC IMC prototype, is to replace every IGBT (with an anti-parallel diode) by a JFET. In order to avoid short-circuiting of the input phases when the converter is connected to the mains, relays are placed on the input filter board.

- Another well-known option, shown in Fig. A.13(a), is to utilize the SiC JFET in a cascode configuration with a low-voltage Si MOSFET by directly connecting the gate of the JFET to the source of the MOSFET and thus forming an normally-off switching device.

- A further possibility, depicted in Fig. A.13(b), is to implement the SiC JFET in series with a low-voltage Si MOSFET, whereby the gate of the JFET is connected to the source of the low-voltage MOSFET with a resistor ($R_3 > R_2$). Opposed to the conventional cascode, which is controlled by the gate of the low-voltage MOSFET, with this modified configuration the MOSFET is merely used prior to the start-up of the converter, to provide the JFET with a normally-off characteristic. For regular operation, the MOSFET is kept in its on-state and the JFET is directly controlled with its own gate.

  Optionally, the voltage drop across the MOSFET (cf. Fig. A.13(b), pin CS) can be used to detect over-currents or for an temperature-compensated signal conditioning circuit even as a current measurement shunt.

A.4.3 Experimental Results

Fig. A.14 provides experimental evidence of the high switching frequency capability of the All-SiC IMC prototype. It shows the characteristic pattern of the link voltage and the output phase current at nominal power and a switching frequency of the output stage of 200 kHz.

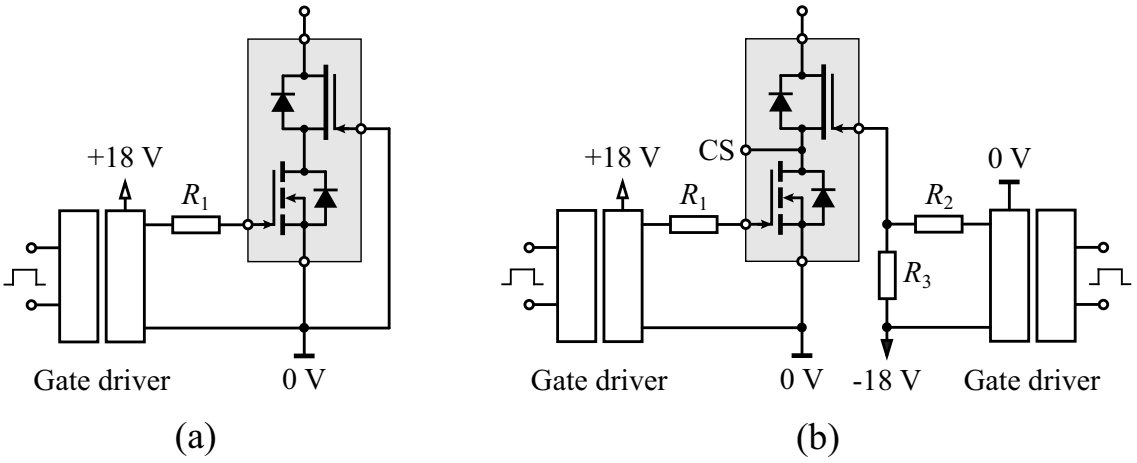


Fig. A.13: Simplified schematics of different cascode configurations of a low-voltage Si MOSFET with a normally-on SiC JFET. **(a)** Standard cascode which is controlled by the gate of the low-voltage MOSFET. **(b)** Modified multi-functional cascode, enabling independent control of the MOSFET and the JFET.

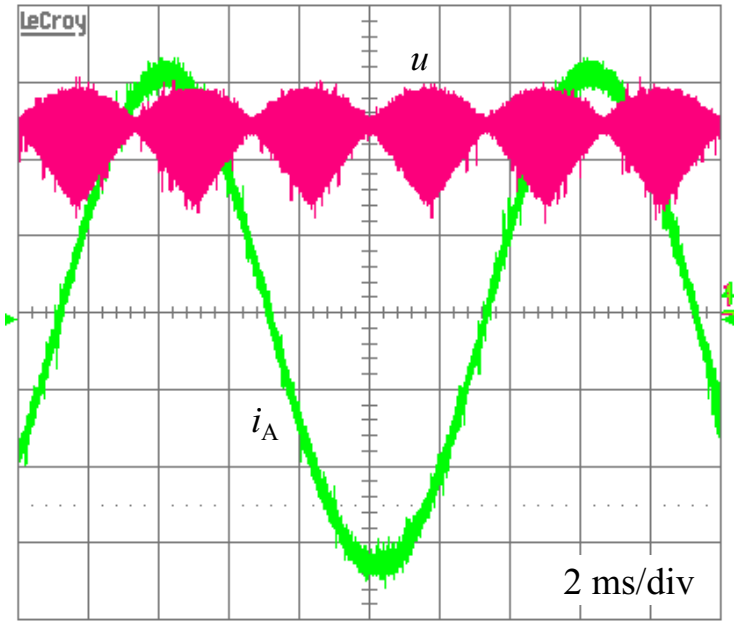


Fig. A.14: Characteristic waveforms of the link voltage and output phase current at $U_1 = 230\,\mathrm{V}$, $f_1 = 50\,\mathrm{Hz}$, and $f_2 = 85\,\mathrm{Hz}$. u: link voltage, $100\,\mathrm{V/div}$; i_A: current of the output phase A, $2\,\mathrm{A/div}$.

This measurement is performed at maximum modulation index and an output frequency of 85 Hz, utilizing an adjustable three-phase RL load with a phase inductance of 2 mH.

A.5 All-SiC Conventional Matrix Converter

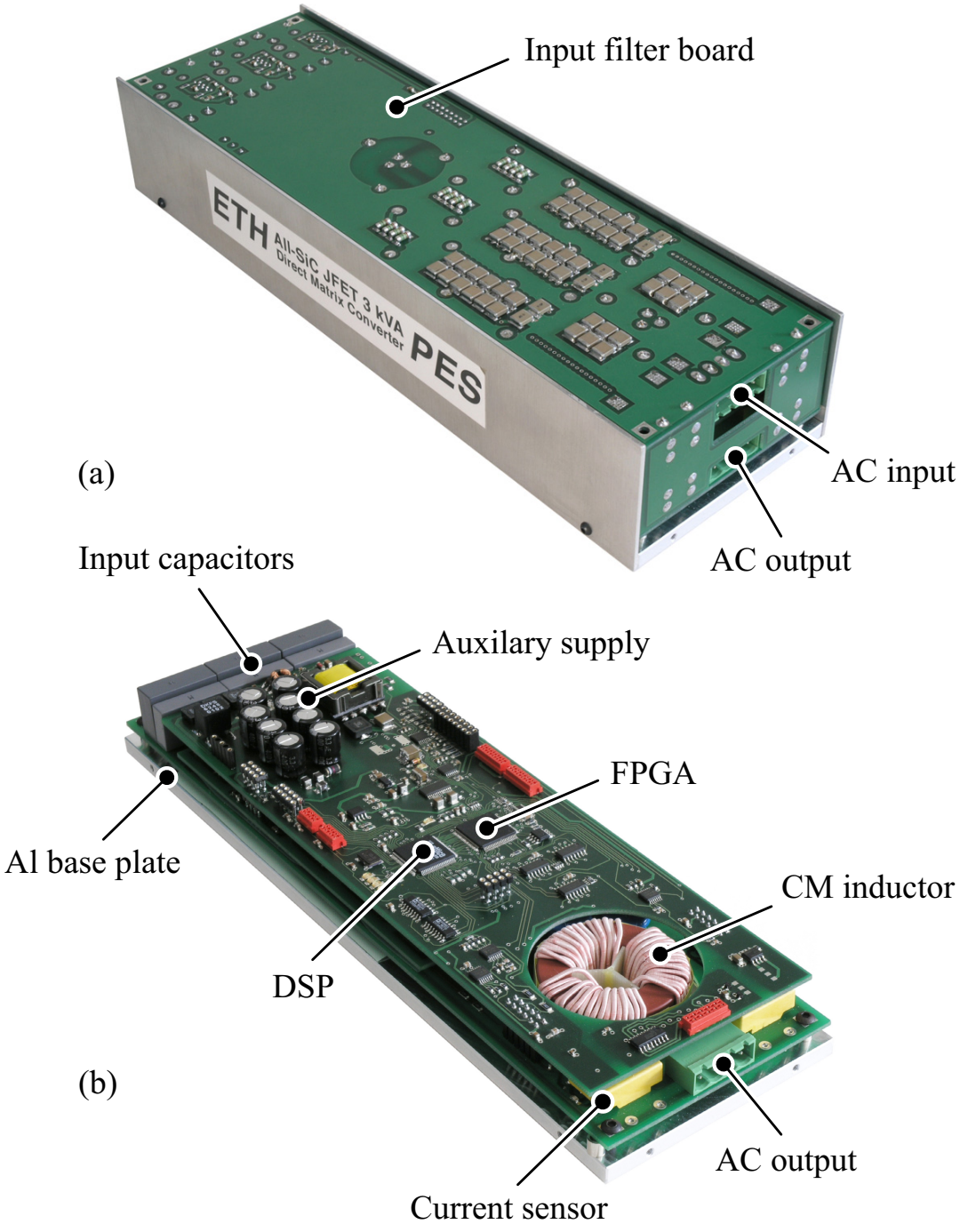


Fig. A.15: All-SiC Conventional Matrix Converter (All-SiC CMC) prototype. **(a)** Assembled and **(b)** opened All-SiC CMC, without the input filter board and the side walls.

A.5.1 Motivation

The All-SiC CMC is implemented to experimentally verify the theoretical findings of the comparison between the CMC and the IMC. Of particular interest are the semiconductor losses and the resulting efficiency if the same SiC chip area is utilized for both topologies. Another advantage of utilizing SiC JFETs is given by their fast and robust switching behavior that enables to use an input voltage measurement based four-step commutation scheme (cf. Fig. 3.14) that requires less than 350 ns for the entire commutation sequence. The switching characteristics of the JFETs further enable an extended switching sequence detection scheme, which is briefly described in the following.

1. The required switching sequence is determined by measuring the largest and second largest input line-to-line voltage for the considered CMOSVM.

2. If the measured input voltages do not allow for a decision on the switching sequence, additionally also the measured output currents are considered. This occurs when the commutation voltage is close or equal to zero.

3. If neither the measured voltages nor the measured currents provide a distinct decision on the switching sequence, there exist different alternative strategies:

   (a) The CMC is kept in the last active (bidirectional conducting) switching state of the present switching sequence.

   (b) The CMC is commutated in a single-step with a minimal interlock delay time, which is determined by the variation of the gate-signal propagation delay of all drives to avoid short-circuiting of the input phases. The application of such a commutation by simply using the parasitic PCB wiring inductance for limiting the current during the commutation is only possible with rugged and fast switching power transistors such as the normally-on SiC JFETs.

The additional research aim associated with the All-SiC CMC hence is to experimentally verify the alternative commutation strategy (cf. list above, 3.(b)). This approach aims to demonstrate that besides the frequently discussed properties, such as high temperature or high switching

frequency operation capability, also the robustness of the normally-on SiC JFETs can be beneficially utilized for the All-SiC CMC without increasing complexity. An alternative approach, presented in [309], is to implement special gate drive circuits that enable to detect the current flow in the IGBTs of a CMC by measuring the collector-emitter voltages. With this information the switching sequence is verified or selected. However, this implies another 18 measurement signals to be processed and checked for plausibility, which increases the hardware and software complexity but not necessarily the converter robustness.

In order to further enhance the safety of the commutation, the implementation of a Switching Sequence Prediction and Verification Unit (SSPVU) is recommended, which, however, is not subject to the investigation of this thesis. The suggested SSPVU is a finite-horizon input voltage and output current emulator, which allows the prediction of the input voltage and output current values for a finite number of future pulse periods, based on previous measurement data. The emulated input voltage and output current of the current pulse period can be used to verify the selection of the switching sequence for the next pulse period.

A.5.2 Design

The design of the All-SiC CMC follows the same concept as applied to the All-SiC IMC with a stacked arrangement of PCBs; starting from the bottom with the aluminum base plate, the power board, the gate driver board, the control and measurement board, and the EMI input filter board. As can be seen in Fig. A.15(a), the filter board, with the inductive components mounted on the bottom side, forms the top cover of the converter. The front and rear wall are implemented with PCBs in order to provide a low-impedance connection between the PE layers of the input filter and the power board, whereas the side walls are manufactured from iron sheets. In order to reduce the CM noise and the dv/dt applied to the load, a CM output filter is integrated, which can be seen in Fig. A.15(b).

Similar to the All-SiC IMC, every bidirectional switch can be implemented by only two SiC JFETs ideally in a common-source configuration. This allows for a reduction of the number of the isolated gate driver voltage levels to nine and thus enables to control the 18 JFETs by only nine two-channel gate driver ICs (e.g. IXYS, IXDN404SI). The converter control and switching sequence generation are implemented

with a DSP (Texas Instruments, TMS320F2808) and a FPGA (Lattice, MachXO LCMXO2280C) providing a resolution of 10 ns for the gate signals. The specifications of the All-SiC CMC are summarized in Tab. A.4.

A.5.3 Experimental Results

Fig. A.16 and Fig. A.17 present the input and output waveforms at nominal output power for an input frequency of 50 Hz and 400 Hz. These measurements are conducted with a three-phase *RL* load with a phase inductance of 2 mH. The investigated commutation scheme works properly as is shown by the input and output current waveforms.

Quantity	*Value*
Nominal input line-to-line voltage	3×400 V, 50 Hz / 400 Hz
Nominal output power	2.8 kW
Output line-to-line voltage	0 V ... 331 V
Output frequency	0 Hz ... $\pm$ 1000 Hz
Output current displacement angle	0° ... 360°
Switching frequency	200 kHz
Default modulation scheme	CMOSVM
EMI compatibility standard	CISPR 11, Class A
Semiconductors	1200 V, 6 A normally-on SiC JFETs, SiCED
Active chip area of the SiC JFETs	72 mm^2
Efficiency at nominal operation	93%
Input current THD (at nominal operation with an *RL* load)	4.6%
Power density	2.2 kW/liter
Specific power	2.2 kW/kg
Dimensions	270 mm $\times$ 82 mm $\times$ 50 mm
Weight	1.3 kg

Tab. A.4: All-SiC CMC specifications summary.

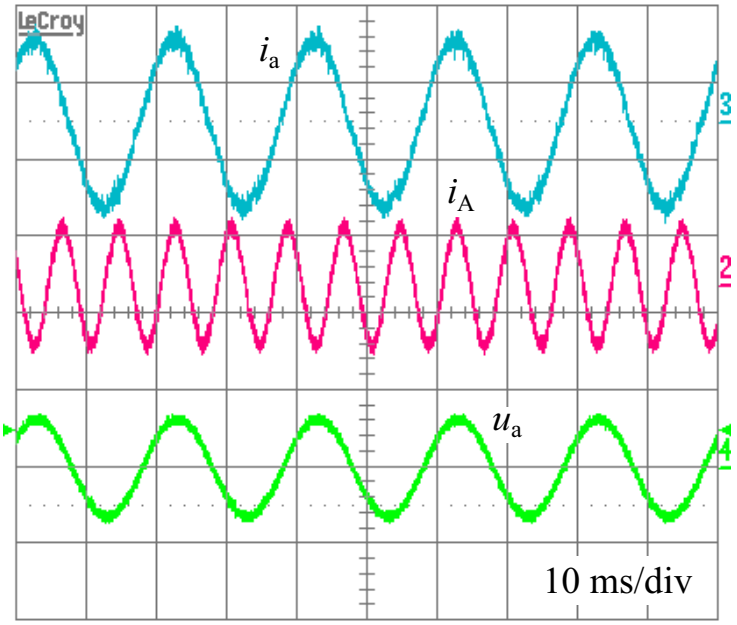


Fig. A.16: Input and output quantities at $U_1 = 230\,\mathrm{V}$, $f_1 = 50\,\mathrm{Hz}$, and $f_2 = 130\,\mathrm{Hz}$. i_a: current of the input phase a, $5\,\mathrm{A/div}$; i_A: current of the output phase A, $10\,\mathrm{A/div}$; u_a: voltage of the input phase a, $500\,\mathrm{V/div}$.

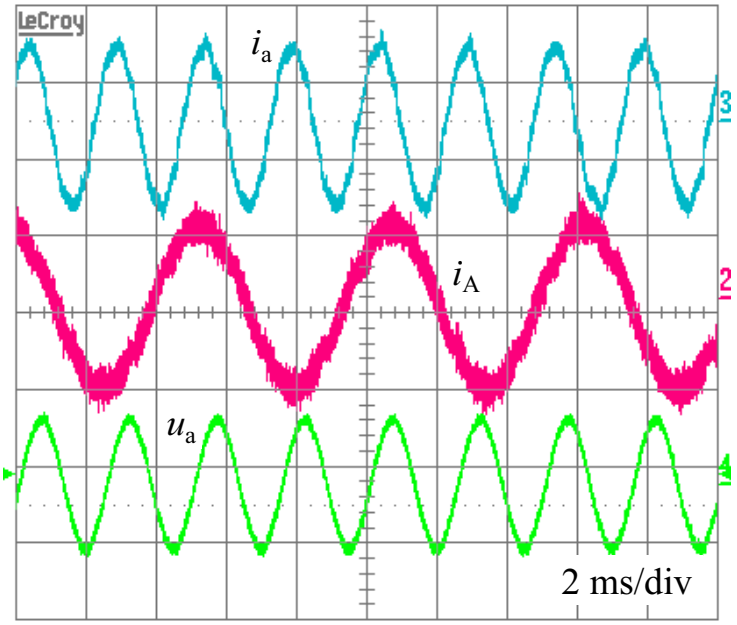


Fig. A.17: Input and output quantities at $U_1 = 230\,\mathrm{V}$, $f_1 = 400\,\mathrm{Hz}$, and $f_2 = 180\,\mathrm{Hz}$. i_a: current of the input phase a, $5\,\mathrm{A/div}$; i_A: current of the output phase A, $10\,\mathrm{A/div}$; u_a: voltage of the input phase a, $500\,\mathrm{V/div}$.

A.6 All-SiC Current Source Back-to-Back Converter

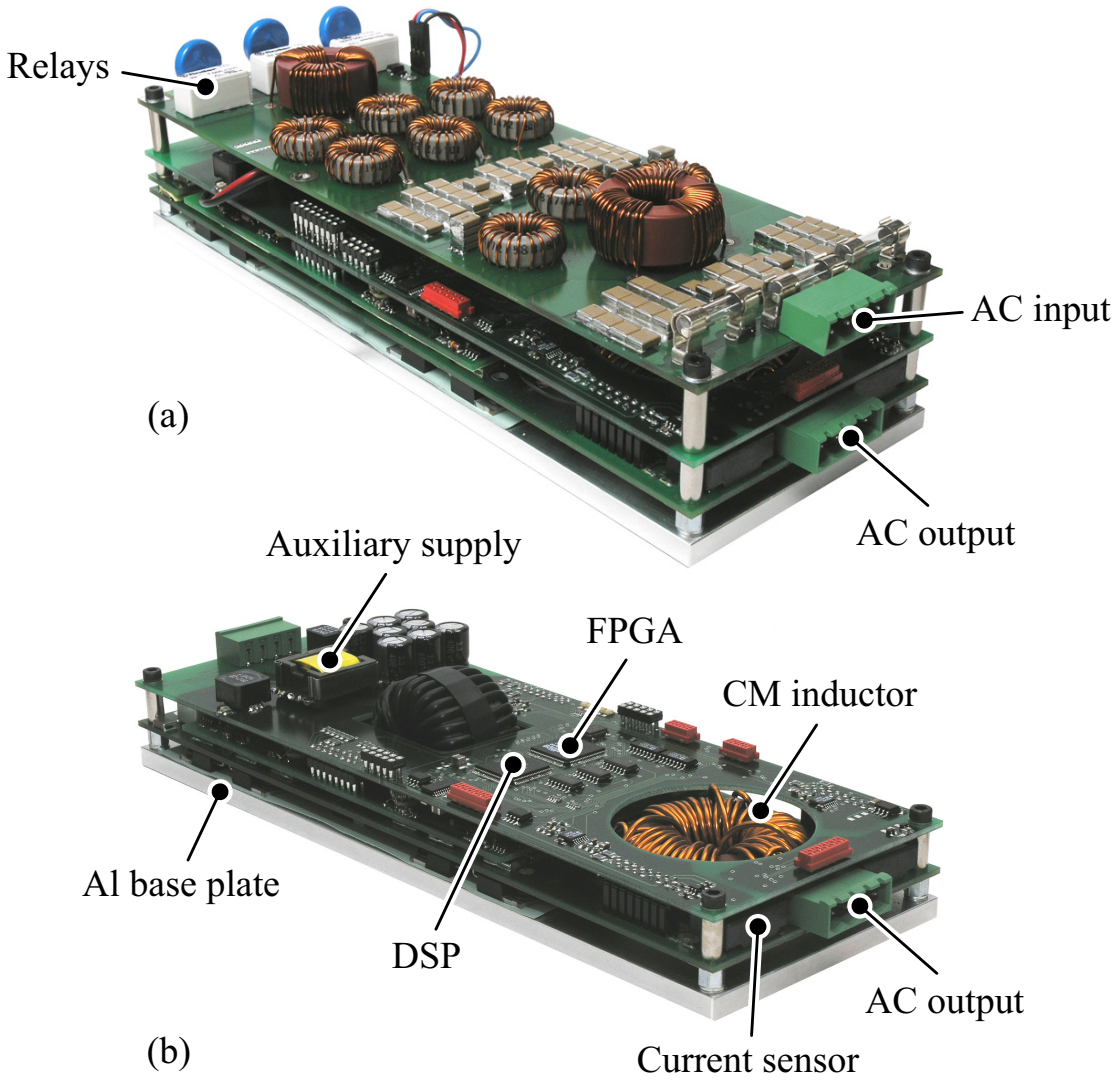


Fig. A.18: All-SiC Current Source Back-to-Back Converter (All-SiC CSBBC) prototype.

A.6.1 Motivation

The question that arises out of the properties of normally-on SiC JFETs is on how they can be best applied to bidirectional ac-ac converter. The performed review of converter topologies shows that the best match can be achieved with a CSBBC. Under fault conditions, such as for example

gate driver supply power loss, a natural freewheeling path is provided for the dc-link inductor current as the JFETs become conducting. An additional advantage is that a short circuit of a phase-leg cannot occur due to the series blocking diodes.

The switching frequency is fixed to 200 kHz to enable a direct performance comparison with the All-SiC IMC and the All-SiC CMC. Another reason for selecting such high switching frequency is to reduce the size and weight of the dc-link inductor as in conventional low-voltage current source converters, the dc-link inductor is one of the most voluminous components.

A.6.2 Design

The physical construction of the All-SiC CLBBC, depicted in Fig. A.18, consists of a planar arrangement of PCBs and is adopted from the All-SiC CMC. The overall design requirements can be summarized as follows.

- The electromechanical construction aims for a compact design to enable motor integration.
- An EMI input filter and a CM output filter have to be integrated to ensure a low EMI noise level at the converter input and output.
- Exclusively, SiC power semiconductors should be implemented.
- Only ceramic capacitors are allowed in the power circuit in order to investigate their performance in ac-ac converters.

The four-layer power board separates the input stage and the output stage with the high-frequency link inductor. The ceramic ac filter capacitors (Murata, GA255-series) are soldered directly on the power board above the JFET switches in order to provide over-voltage protection, a low-impedance connection, and improved filtering.

Different magnetic materials and inductor construction principles such as planar E and SMD ferrite cores, toroidal and E powder cores, and tape wound C-cores have been analyzed regarding losses, size, fringing flux, and cooling performance. Due to the dc-bias caused by the link current, toroidal powder core materials provide the best compromise between losses, cooling and size. The completed dc-link inductor is shown in Fig. A.19 and its key figures are summarized in Tab. A.5.

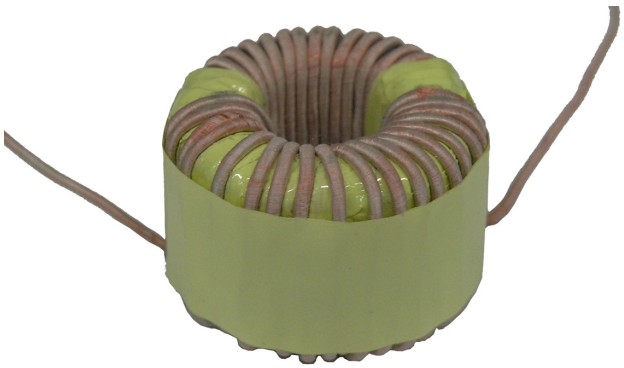


Fig. A.19: Constructed dc-link inductor.

In the All-SiC CSBBC, the SiC series diodes significantly contribute to the overall converter conduction losses as always four diodes are in the dc-link current path. Optionally, the series diodes could be replaced by SiC JFETs, ideally forming a common-drain configuration with the other JFETs of a phase-leg. The common-drain configuration is advantageous as only 10 isolated gate driver power supplies are required compared with 12 for the common-source configuration. Depending on the SiC power-device parameters, replacing the series diodes by JFETs would allow a reduction of the conduction losses.

The specifications of the All-SiC CSBBC are compiled in Tab. A.6. Additional information about this prototype can be found in [310, 311].

Quantity	*Value*
Core	2 stacked Magnetics MPP 55071-A2
Winding	57 turns
Wire	Multi-stranded copper wire (copper cross section 0.8 mm^2)
Inductance	400 μH at 0 A, 200 kHz
	320 μH at 6 A, 200 kHz
Dimensions	Outer diameter: 40 mm; height: 27 mm
Volume	40 cm^3
Weight	120 g

Tab. A.5: Characteristic data of the dc-link inductor.

A.6.3 Experimental Results

Fig. A.20 and Fig. A.21 present characteristic waveforms at nominal output power with a three-phase *RL* load. As can be seen in Fig. A.20, the waveform of the input current i_a and the output current i_A is sinusoidal, whereas the input voltage u_a and the output voltage u_A have a triangular-shaped waveform. This is due to the nonlinear voltage dependency of the X7R ceramic ac capacitors, leading to a reduction of the nominal capacitance of approximately 30% when the capacitor voltage

Quantity	*Value*
Nominal input line-to-line voltage	$3 \times 400\,\mathrm{V}$, $50\,\mathrm{Hz}$
Nominal output power	$2.8\,\mathrm{kW}$
Output line-to-line voltage	$0\,\mathrm{V} \ldots 383\,\mathrm{V}$
Output frequency	$0\,\mathrm{Hz} \ldots \pm 300\,\mathrm{Hz}$
Output current displacement angle	$0° \ldots 360°$
Switching frequency	$200\,\mathrm{kHz}$
Default modulation scheme	Half-wave sym. SVM
EMI compatibility standard	CISPR 11, Class A
Semiconductors	1200 V, 6 A normally-on SiC JFETs, SiCED
	1200 V, 10 A SiC SBDs, CREE, C2D10120
Active chip area of the SiC JFETs	$48\,\mathrm{mm}^2$
Active chip area of the SiC SBDs	$84\,\mathrm{mm}^2$
Efficiency at nominal operation	92%
Input current THD (at nominal output power with a *RL* load)	2.7%
Power density	$2.5\,\mathrm{kW/liter}$
Specific power	$2.5\,\mathrm{kW/kg}$
Dimensions	$230\,\mathrm{mm} \times 80\,\mathrm{mm} \times 60\,\mathrm{mm}$
Weight	$1.1\,\mathrm{kg}$

Tab. A.6: All-SiC CSBBC specifications summary.

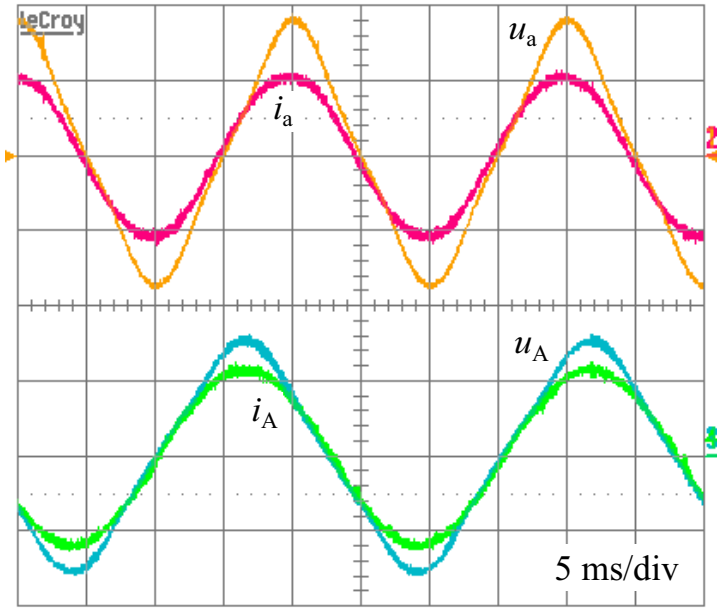


Fig. A.20: Input and output current and voltage waveforms at $U_1 = 230\,\mathrm{V}$, $f_1 = 50\,\mathrm{Hz}$, and $f_2 = 40\,\mathrm{Hz}$. i_a: current of the input phase a, $5\,\mathrm{A/div}$; i_A: current of the output phase A, $5\,\mathrm{A/div}$; u_a: voltage of the input phase a, $200\,\mathrm{V/div}$; u_A: voltage of the output phase A, $200\,\mathrm{V/div}$.

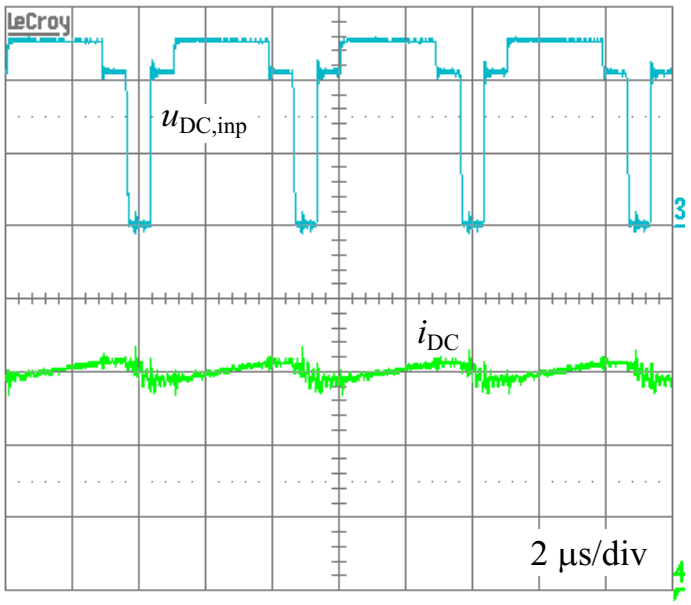


Fig. A.21: DC-link waveforms at $U_1 = 230\,\mathrm{V}$, $f_1 = 50\,\mathrm{Hz}$, and $f_2 = 40\,\mathrm{Hz}$. i_{DC}: dc-link current, $2\,\mathrm{A/div}$; $u_{DC,inp}$: switched link voltage between the input stage and the dc-link inductor, $5\,\mathrm{A/div}$.

is increased from 0 V to the peak value of 325 V of the input phase voltage. The distortion of the input voltage u_a is higher than of the output voltage u_A, which results from the interaction of the three-phase supply (Elgar, SW 5250A) with the ceramic input capacitors. The worst case relative error between the measured and the calculated losses is 6%.

In Fig. A.22, the converter efficiency is plotted for different output power levels, when supplying a three-phase RL load with a resistance of 47 Ω and an inductance of 2 mH per phase. The load is adjusted such that at 95% of the maximum output voltage (for buck operation) the nominal output power of 2.8 kW is supplied to the load. The load parameters are then kept constant and the efficiency is measured for different modulation indeces ranging from 0.4 to 1.

An extract of the measured CE spectrum is depicted in Fig. A.23 to provide experimental evidence that the suggested EMI input filter design method is also applicable to high switching frequency power converters. The prototype All-SiC CLBBC is not constructed with an appropriate enclosure. Therefore, the CISPR 11 Class A CE levels are difficulet to meet over the entire frequency range from 150 kHz to 30 MHz, as the PE interconnection of the individual PCBs is too high impedance (cf. Sec. 6.5, impact of enclosure and PE connection on noise level). For

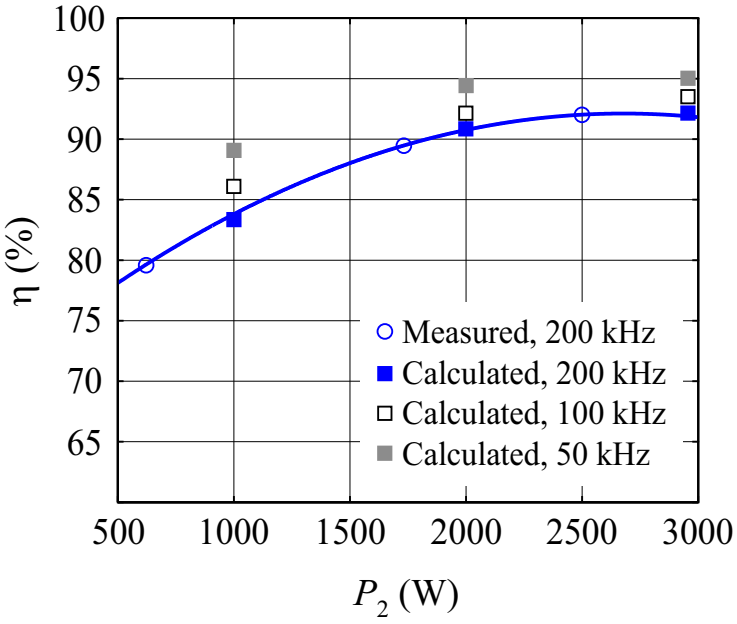


Fig. A.22: Efficiency versus output power at $U_1 = 230$ V for different switching frequencies.

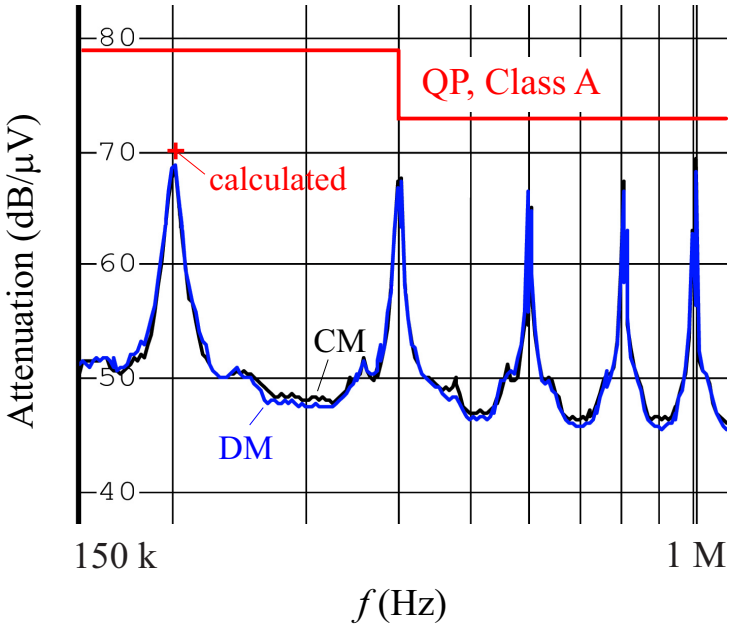


Fig. A.23: Measured DM and CM quasi-peak (QP) noise level.

that reason, Fig. A.23 presents the CE measurement results only in the frequency range of 150 kHz to 1 MHz, which seems to be representative for the given electromechanical construction. As can be clearly seen, the low-frequency performance below 1 MHz meets the CISPR 11 Class A requirements, and the relevant noise peak at 200 kHz for dimensioning the filter fulfills also the design margin of 8 dB.

A.7 Motor Data

Tab. A.7 and Tab. A.8 summarize the main parameters of the electric motors utilized in this work.

Quantity	*Value*
Designation	LST-127-3-30-560
Motor type	PMSM
Rated phase voltage	191 V
Rated phase current	9.5 A
Continuous power	3.5 kW at 150 Hz
Rated speed	3000 rpm
Nominal torque	11 Nm
Inductance per phase	4.5 mH
Resistance per phase	0.5 Ω

Tab. A.7: Parameters of the PMSM from LUST LTi Drives.

Quantity	*Value*
Designation	HAC-145 S 08
Motor type	IM
Rated phase voltage	191 V
Rated phase current	5.4 A
Continuous power	2 kW at 50 Hz
$\cos(\Phi)$	0.77
Rated speed	2880 rpm
Rated torque	6.6 Nm
Inductance per phase	14.0 mH
Resistance per phase	3.3 Ω

Tab. A.8: Parameters of the IM from Bartholdi.

Appendix B

Test and Measurement Setups

B.1 Converter and Motor Drive Test Setup

Fig. B.1 and Fig. B.2 should convey an impression of the typical laboratory converter test setup that was utilized in many variations in the course of this thesis. It consists of the converter prototype, a three-phase linear amplifier, a motor test bench, a PC to interface with the prototype, and measurement equipment.

In Fig. B.3, the constructed motor test bench for dynamic operation of the converter prototypes with a motor load is presented. The test bench comprises two coupled PMSMs from LUST LTi Drives: a LST-127 (cf. Tab. A.7) and a LSH-127 PMSM, both equipped with a rotary encoder. The LST-127 is always supplied and controlled by the ac-ac converter prototypes, whereas the LSH-127 is connected to a LUST CDD 3000 servo drive controller with a diode rectifier and a six-switch inverter. The CDD 3000 features an external brake resistor and is utilized to generated the desired load profile for the converter prototypes by a PLC software (cf. Sec. A.3.3, measurements of the USMC).

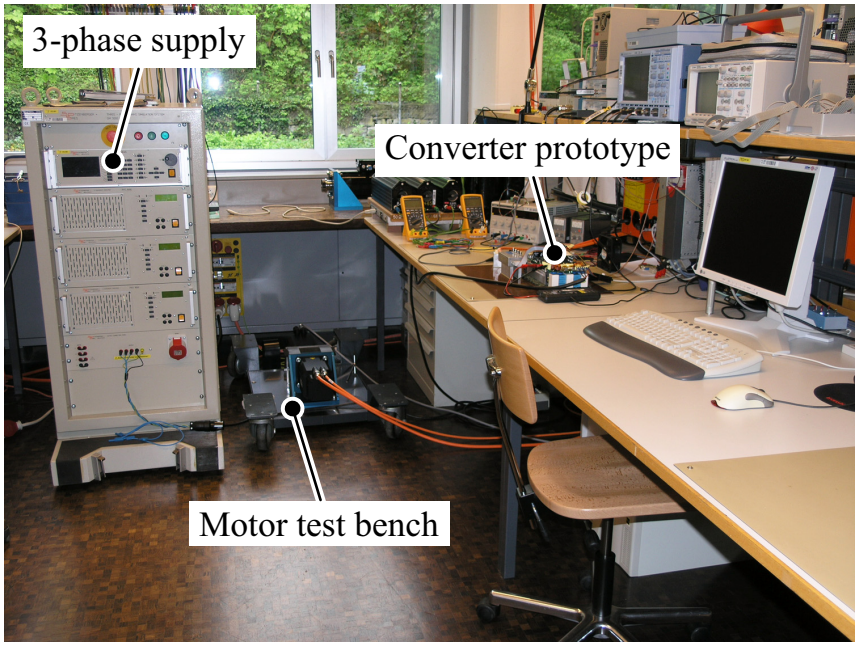


Fig. B.1: Typical laboratory test setup, showing the three-phase supply, the motor test bench, and the converter prototype.

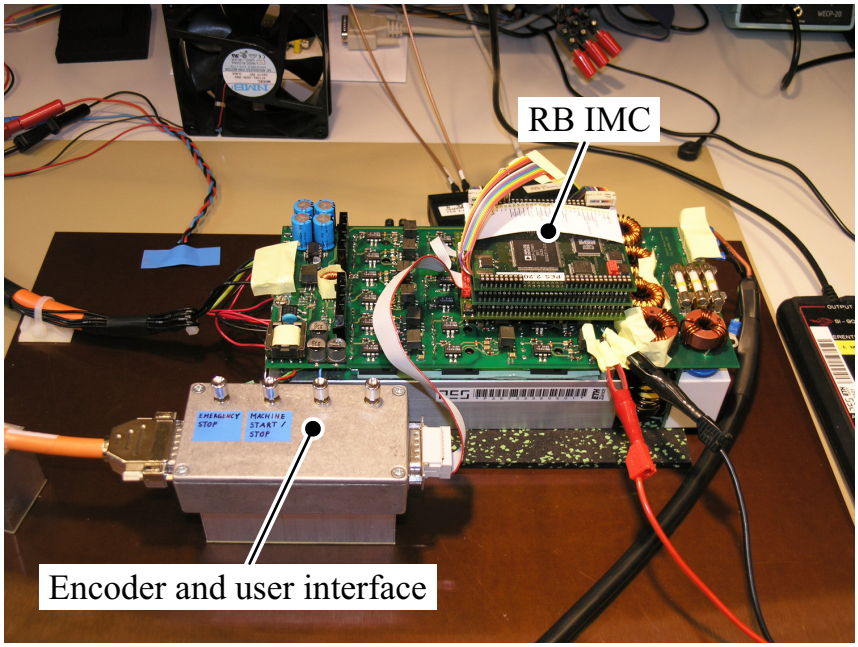


Fig. B.2: RB IMC under test with external encoder and user interface to control the motor.

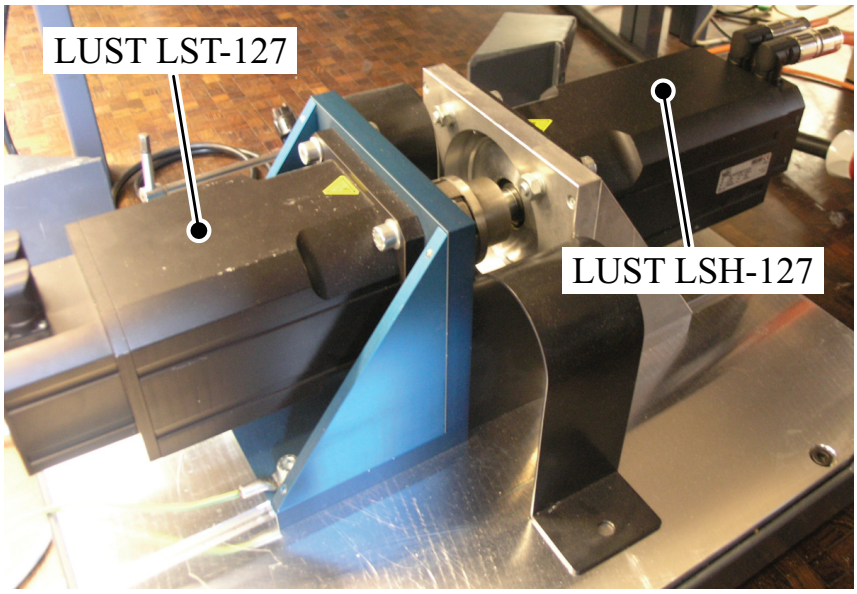


Fig. B.3: Constructed motor test bench with two coupled PMSMs (LST-127 and LSH-127).

B.2 Enclosure for Conducted Emission EMI Measurement

The designed converter prototypes of this work are not implemented with an enclosure to enable direct access to the hardware for measurements. However, for EMI measurements, the enclosure is of significant importance as it impacts the measurement results of the radiated and conducted emission (CE) levels (cf. Sec. 6.5) and generally reduces the radiated emission. Therefore, commercially available converters and external EMI/RFI input and output filters are always implemented in a metal enclosure to enhance the EMI performance. In order to provide a realistic measurement setup for the ac-ac converter prototypes, an EMI measurement enclosure was constructed, which is shown in Fig. B.4. It allows the installation of the hardware prototypes in an enclosure as is done for commercial drive system. The test enclosure further enables by means of two shielded compartments to separate the EMI input filter from the switching converter, as depicted in Fig. B.5, in order to analyze possible coupling effects.

The supply cable, connected between the ac input of the enclosure and the LISN, is a five-wire three-phase mains cable with a conductor cross-section of 1.5 mm^2. The motor is connected to the ac output of

Fig. B.4: Closed EMI measurement enclosure. Outer dimensions: 43.5 cm × 27.5 cm × 30.0 cm.

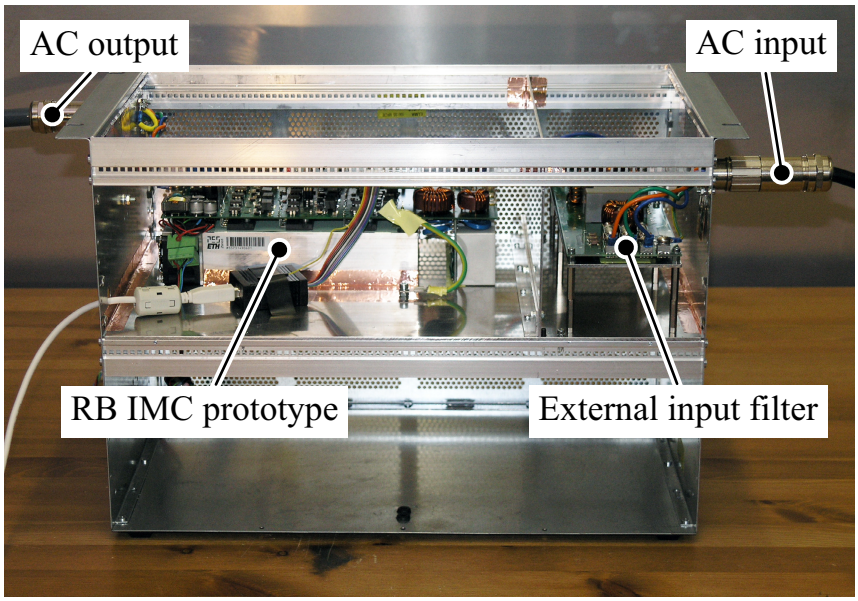


Fig. B.5: Opened EMI measurement enclosure, showing the RB IMC prototype and an external input filter under test. The on-board filter of the RB IMC is by-passed.

the enclosure by a shielded five-wire motor cable with a conductor cross-section of 2.5 mm^2. Both the supply cable and the motor cable have a length of 3 m. M23 industry standard connectors are utilized for the power connectors of the enclosure and the motor.

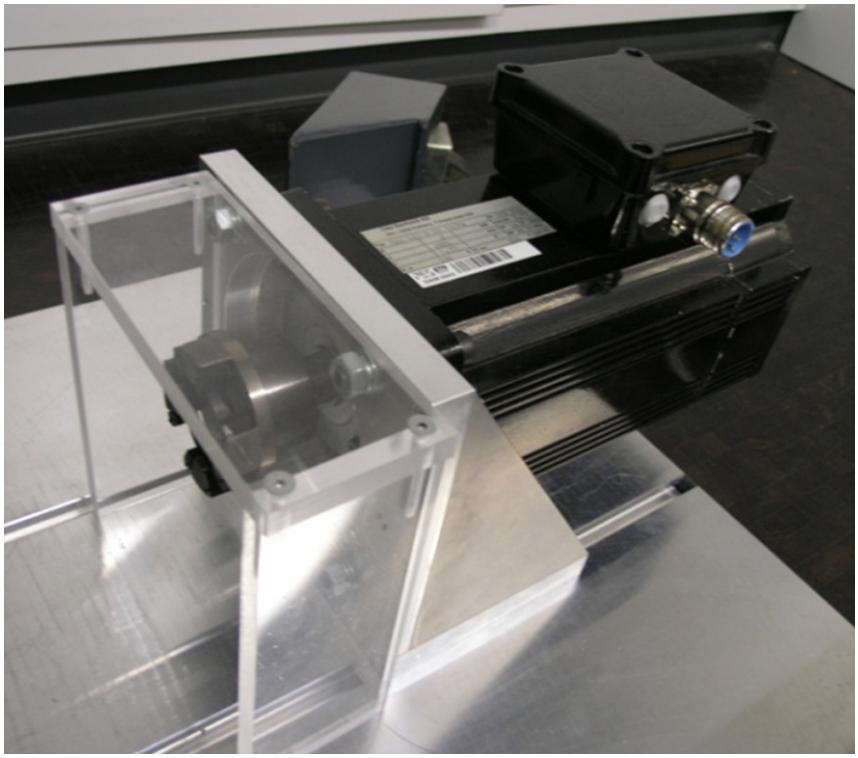


Fig. B.6: HAC-145 IM used for EMI measurements, shown on the motor test bench without the LSH-127 PMSM (load).

The CE EMI measurements of the converter prototypes when connected to a motor are performed with a HAC-145 IM from Bartholdi (cf. Tab. A.8). Thereby, the IM is loaded with the LSH-127 PMSM which is connected to an adjustable three-phase brake resistor. The PMSM is deliberately not controlled by another power converter, to avoid any kind of interference with the prototype converter and filter under test. The IM is controlled with a simple voltage-frequency feedforward control scheme. The earthing of the measurement enclosure is provided by the PE conductor of the three-phase supply cable of the enclosure. The motor case and the test bench are connected by default to PE via the motor cable. An additional interruptible connection between the test bench and PE is established with a separate cable for testing purposes.

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