Tutorial

Matrix Converter

Sparse Matrix Converter
Conventional Matrix Converter

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Industry Relations

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Research

- Ultra High Frequency
- Highly Compact
- Extreme Temperatures

Electromagnetic Integration
Future Energy Distribution

All-SiC Sparse-Matrix-Converter
Active EMI Filters
Fuel-Cell Powered Car
Bi-Directional DC/DC Converter
Three-Port UPS
Meso-Scale Gas Turbine Gen. (800,000rpm)
More-Electric Aircraft Actuator Supply
Interactive Multi-Disciplinary Sim.

Ultra-Comp. Telecom Power Supplies
Utility Interface for Drives
Series/Parallel-Res. X-Ray-Generator
Piezoelectric Actuators
Magnetically Levitated Actuators/Sensors

Topics

2005 2010 2015

Tutorial Schedule

■ Introduction	*J.W. Kolar*	9:00 – 10:00
■ Modulation Schemes I	*J.W. Kolar / F. Schafmeister*	10:00 – 11:00
Coffee Break		
■ Modulation Schemes II	*F. Schafmeister*	11:30 – 13:00
Lunch Break		
■ Design Issues	*F. Schafmeister*	14:00 – 15:30
Coffee Break		
■ Comparison to BBC	*M.L. Heldwein*	16:00 – 17:00
■ Future Developments	*M.L. Heldwein / J.W. Kolar*	17:00 – 17:30

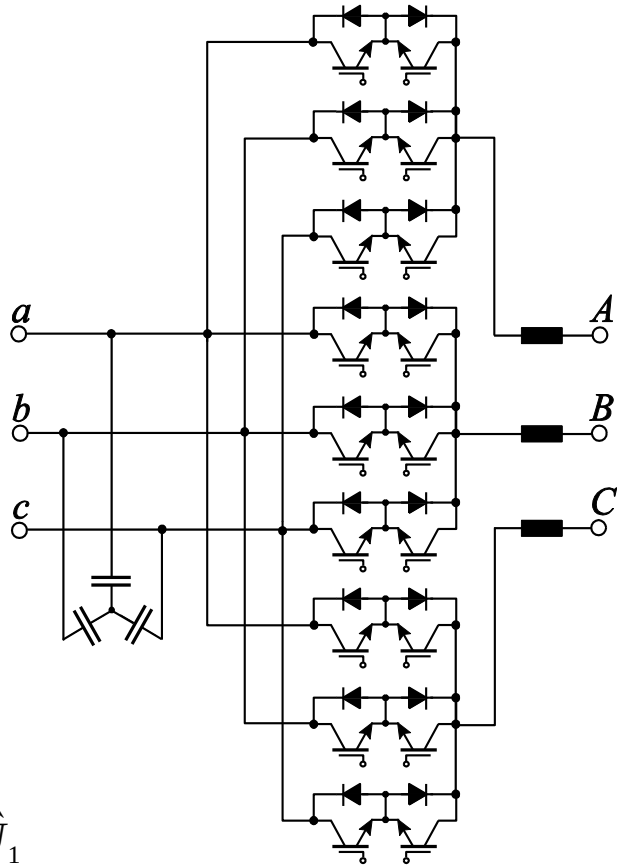
MC Topologies & Modulation Schemes I

Johann W. Kolar

- **Conventional Matrix Converter**
  - Circuit Topology
  - Basic Principle of Operation
- **Sparse Matrix Converter Topologies**
  - Derivation of the Circuit Topology
  - Basic Principle of Operation

Conventional AC-AC Matrix Converter (CMC)

Circuit Topology



$$\hat{U}_{2,\max} = \frac{\sqrt{3}}{2} \cdot \hat{U}_1 = 0.866 \cdot \hat{U}_1$$

Conventional Matrix Converter

Mathematical Description of the Basic Operating Behavior

Voltage Conversion

$$\begin{pmatrix} u_A \\ u_B \\ u_C \end{pmatrix} = \begin{pmatrix} sAa & sAb & sAc \\ sBa & sBb & sBc \\ sCa & sCb & sCc \end{pmatrix} \cdot \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix}$$

$$\underline{u}_{ABC} = \underline{S} \cdot \underline{u}_{abc}$$

Current Conversion

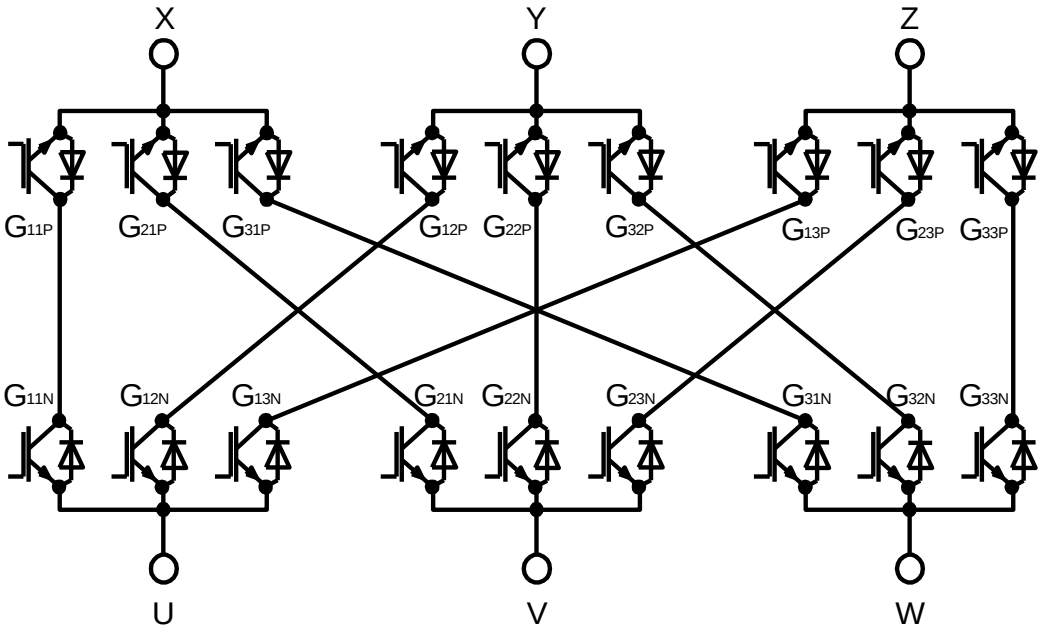
$$\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \begin{pmatrix} sAa & sBa & sCa \\ sAb & sBb & sCb \\ sAc & sBc & sCc \end{pmatrix} \cdot \begin{pmatrix} i_A \\ i_B \\ i_C \end{pmatrix}$$

$$\underline{i}_{abc} = \underline{S}^T \cdot \underline{i}_{ABC}$$

CMC Practical Realization

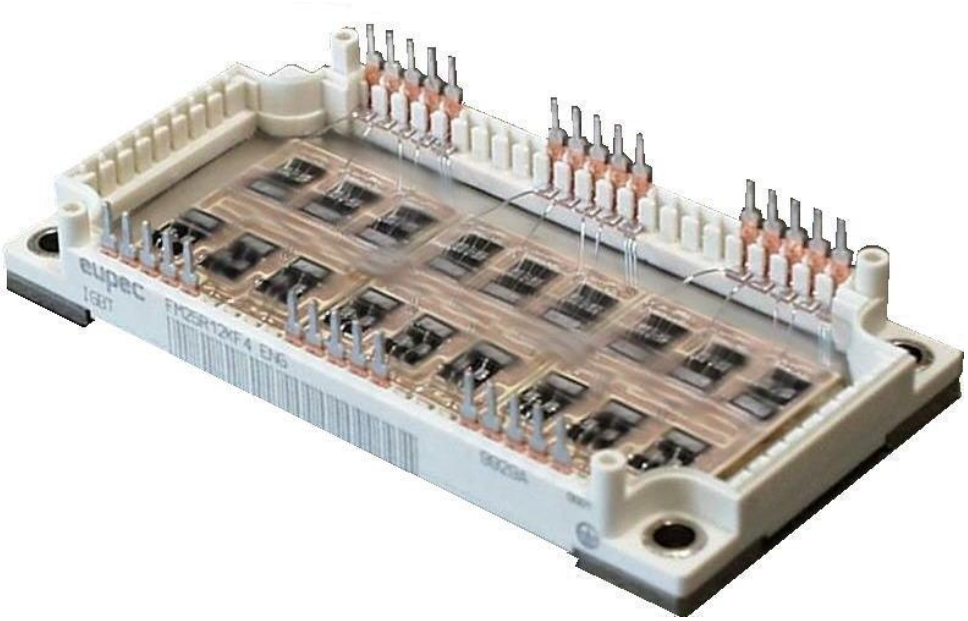
Common Collector Connection of the Bidirectional Switches

Separation of Components forming a Bidirectional Switch



18 Power Transistors
18 Gate Drives
6 Gate Drive Power Supplies
9 Collector Potentials

CMC Power Module (eupec)



EconoPACK 3

- 35 A IGBT3 Chips
- 7.5 kW (100% Overloading Capability)

- 6 Connection Islands
- 6 IGBT Islands
- Conventional Module Technique
- Collector Connections in Module Center
- 3 Equal DCBs

Conventional → Indirect Matrix Converter

Voltage Conversion Splitted into Rectifier and Inverter Operation

$$\begin{pmatrix} u_A \\ u_B \\ u_C \end{pmatrix} = \begin{pmatrix} spA & snA \\ spB & snB \\ spC & snC \end{pmatrix} \cdot \begin{pmatrix} sap & sbp & scp \\ san & sbn & scn \end{pmatrix} \cdot \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix}$$

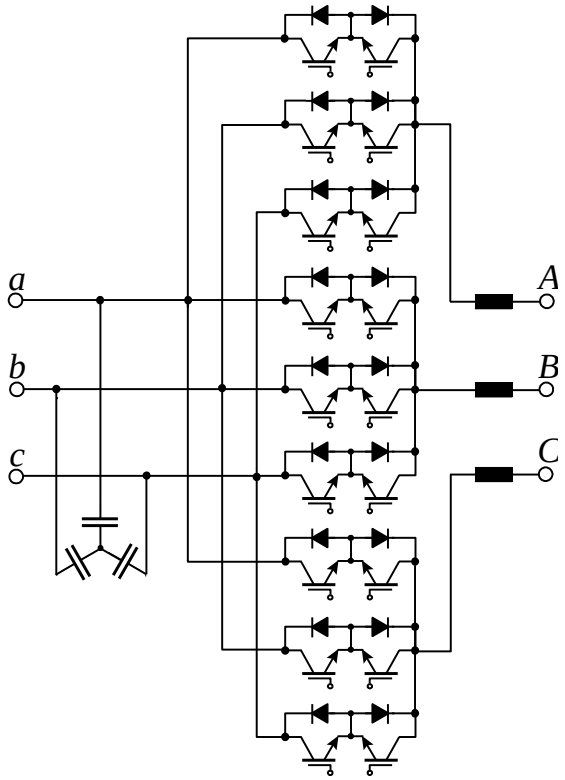
$$\underline{u}_{ABC} = \underline{S}_{WR} \cdot \underline{S}_{GR} \cdot \underline{u}_{abc}$$

$$\underline{u}_{ZK} = \begin{pmatrix} u_p \\ u_n \end{pmatrix} = \underline{S}_{GR} \cdot \underline{u}_{abc}$$

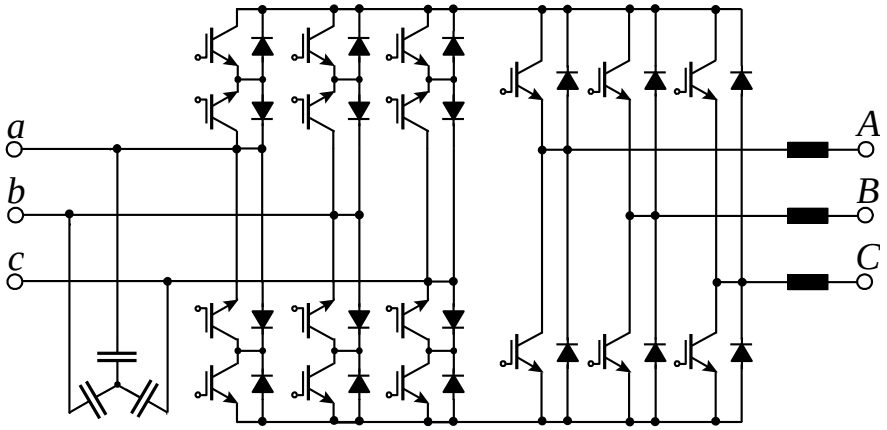
- Introduction of a Fictitious Rectifier and Inverter Stage
- Fictitious DC Link Voltage / DC Link Current
- Modulation as for DC Link Converters

Indirect Matrix Converter Could be Seen as Physical Realization of a Mathematical Concept

Basic Matrix Converter Topologies



Conventional



Indirect

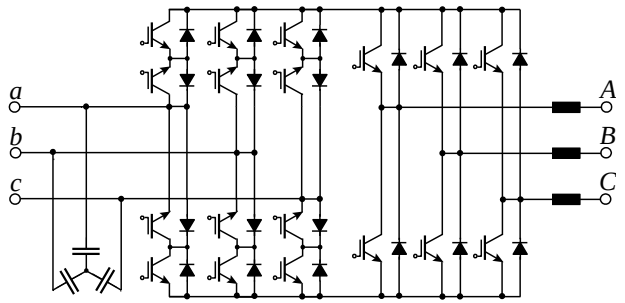
Functional Equivalence of IMC and CMC

Operation of the IMC is Restricted to $u_{pn}>0$, Remaining Switching States Identical to CMC

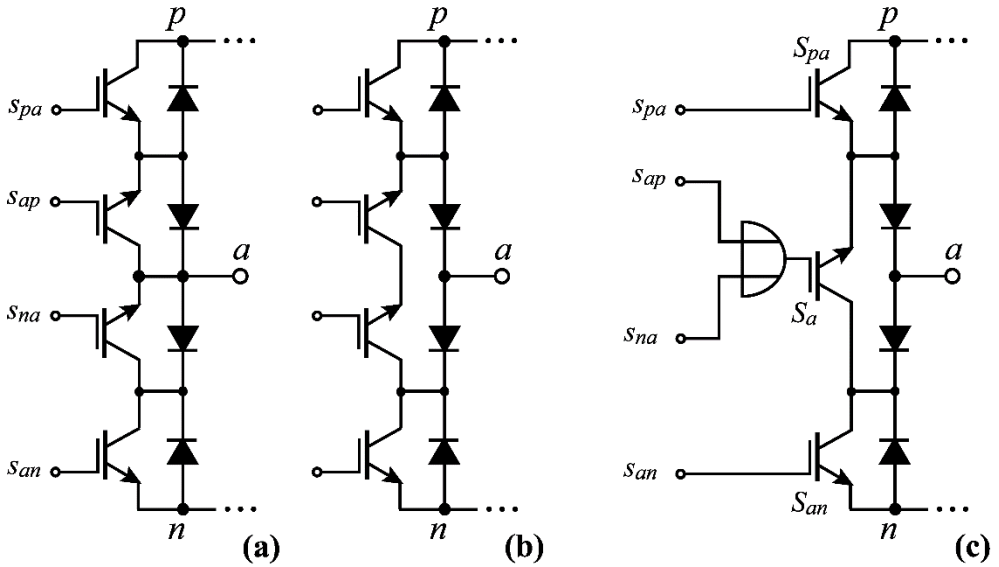
No.	A	B	C	s_{Aa}	s_{Ab}	s_{Ac}	s_{Ba}	s_{Bb}	s_{Bc}	s_{Ca}	s_{Cb}	s_{Cc}	u_{AB}	u_{BC}	u_{CA}	i_a	i_b	i_c
1	a	a	a	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0
2	b	b	b	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0
3	c	c	c	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0
4	a	c	c	1	0	0	0	0	1	0	0	1	$-u_{ca}$	0	u_{ca}	i_A	0	$-i_A$
5	b	c	c	0	1	0	0	0	1	0	0	1	u_{bc}	0	$-u_{bc}$	0	i_A	$-i_A$
6	b	a	a	0	1	0	1	0	0	1	0	0	$-u_{ab}$	0	u_{ab}	$-i_A$	i_A	0
7	c	a	a	0	0	1	1	0	0	1	0	0	u_{ca}	0	$-u_{ca}$	$-i_A$	0	i_A
8	c	b	b	0	0	1	0	1	0	0	1	0	$-u_{bc}$	0	u_{bc}	0	$-i_A$	i_A
9	a	b	b	1	0	0	0	1	0	0	1	0	u_{ab}	0	$-u_{ab}$	i_A	$-i_A$	0
10	c	a	c	0	0	1	1	0	0	0	0	1	u_{ca}	$-u_{ca}$	0	i_B	0	$-i_B$
11	c	b	c	0	0	1	0	1	0	0	0	1	$-u_{bc}$	u_{bc}	0	0	i_B	$-i_B$
12	a	b	a	1	0	0	0	1	0	1	0	0	u_{ab}	$-u_{ab}$	0	$-i_B$	i_B	0
13	a	c	a	1	0	0	0	0	1	1	0	0	$-u_{ca}$	u_{ca}	0	$-i_B$	0	i_B
14	b	c	b	0	1	0	0	0	1	0	1	0	u_{bc}	$-u_{bc}$	0	0	$-i_B$	i_B
15	b	a	b	0	1	0	1	0	0	0	1	0	$-u_{ab}$	u_{ab}	0	i_B	$-i_B$	0
16	c	c	a	0	0	1	0	0	1	1	0	0	0	u_{ca}	$-u_{ca}$	i_C	0	$-i_C$
17	c	c	b	0	0	1	0	0	1	0	1	0	0	$-u_{bc}$	u_{bc}	0	i_C	$-i_C$
18	a	a	b	1	0	0	1	0	0	0	1	0	0	u_{ab}	$-u_{ab}$	$-i_C$	i_C	0
19	a	a	c	1	0	0	1	0	0	0	0	1	0	$-u_{ca}$	u_{ca}	$-i_C$	0	i_C
20	b	b	c	0	1	0	0	1	0	0	0	1	0	u_{bc}	$-u_{bc}$	0	$-i_C$	i_C
21	b	b	a	0	1	0	0	1	0	1	0	0	0	$-u_{ab}$	u_{ab}	i_C	$-i_C$	0
22	a	b	c	1	0	0	0	1	0	0	0	1	u_{ab}	u_{bc}	u_{ca}	i_A	i_B	i_C
23	a	c	b	1	0	0	0	0	1	0	1	0	$-u_{ca}$	$-u_{bc}$	$-u_{ab}$	i_A	i_C	i_B
24	b	a	c	0	1	0	1	0	0	0	0	1	$-u_{ab}$	$-u_{ca}$	$-u_{bc}$	i_B	i_A	i_C
25	b	c	a	0	1	0	0	0	1	1	0	0	u_{bc}	u_{ca}	u_{ab}	i_C	i_A	i_B
26	c	a	b	0	0	1	1	0	0	0	1	0	u_{ca}	u_{ab}	u_{bc}	i_B	i_C	i_A
27	c	b	a	0	0	1	0	0	1	1	0	0	$-u_{bc}$	$-u_{ab}$	$-u_{ca}$	i_C	i_B	i_A

No.	A	B	C	s_{pa}	s_{pb}	s_{pc}	s_{an}	s_{bn}	s_{cn}	s_A	s_B	s_C	u_{AB}	u_{BC}	u_{CA}	u	i_a	i_b	i_c
1	p	p	p	X	X	X	X	X	X	1	1	1	0	0	0	-	0	0	0
10	n	n	n	X	X	X	X	X	X	0	0	0	0	0	0	-	0	0	0
19	X	X	X	1	0	0	1	0	0	X	X	X	0	0	0	0	0	0	0
25	X	X	X	0	1	0	0	1	0	X	X	X	0	0	0	0	0	0	0
31	X	X	X	0	0	1	0	0	1	X	X	X	0	0	0	0	0	0	0
37	a	c	c	1	0	0	0	0	1	1	0	0	$-u_{ca}$	0	u_{ca}	$-u_{ca}$	i_A	0	$-i_A$
38	a	c	c	0	0	1	1	0	0	0	1	1	$-u_{ca}$	0	$-u_{ca}$	u_{ca}	i_A	0	$-i_A$
39	b	c	c	0	1	0	0	0	1	1	0	0	u_{bc}	0	$-u_{bc}$	u_{bc}	0	i_A	$-i_A$
40	b	c	c	0	0	1	0	1	0	0	1	1	u_{bc}	0	$-u_{bc}$	$-u_{bc}$	0	i_A	$-i_A$
41	b	a	a	0	1	0	1	0	0	1	0	0	$-u_{ab}$	0	u_{ab}	$-u_{ab}$	$-i_A$	i_A	0
42	b	a	a	1	0	0	0	1	0	0	1	1	$-u_{ab}$	0	u_{ab}	u_{ab}	$-i_A$	i_A	0
43	c	a	a	0	0	1	1	0	0	1	0	0	u_{ca}	0	$-u_{ca}$	u_{ca}	$-i_A$	0	i_A
44	c	a	a	1	0	0	0	0	1	0	1	1	u_{ca}	0	$-u_{ca}$	$-u_{ca}$	$-i_A$	0	i_A
45	c	b	b	0	0	1	0	1	0	1	0	0	$-u_{bc}$	0	u_{bc}	$-u_{bc}$	0	$-i_A$	i_A
46	c	b	b	0	1	0	0	0	1	0	1	1	$-u_{bc}$	0	u_{bc}	u_{bc}	0	$-i_A$	i_A
47	a	b	b	1	0	0	0	1	0	1	0	0	u_{ab}	0	$-u_{ab}$	u_{ab}	i_A	$-i_A$	0
48	a	b	b	0	1	0	1	0	0	0	1	1	u_{ab}	0	$-u_{ab}$	$-u_{ab}$	i_A	$-i_A$	0
49	c	a	c	1	0	0	0	0	1	0	1	0	u_{ca}	$-u_{ca}$	0	$-u_{ca}$	i_B	0	$-i_B$
50	c	a	c	0	0	1	1	0	0	1	0	1	u_{ca}	$-u_{ca}$	0	u_{ca}	i_B	0	$-i_B$
51	c	b	c	0	1	0	0	0	1	0	1	0	$-u_{bc}$	u_{bc}	0	u_{bc}	0	i_B	$-i_B$
52	c	b	c	0	0	1	0	1	0	1	0	1	$-u_{bc}$	u_{bc}	0	$-u_{bc}$	0	i_B	$-i_B$
53	a	b	a	0	1	0	1	0	0	0	1	0	u_{ab}	$-u_{ab}$	0	$-u_{ab}$	$-i_B$	i_B	0
54	a	b	a	1	0	0	0	1	0	1	0	1	u_{ab}	$-u_{ab}$	0	u_{ab}	$-i_B$	i_B	0
55	a	c	a	0	0	1	1	0	0	0	1	0	$-u_{ca}$	u_{ca}	0	u_{ca}	$-i_B$	0	i_B
56	a	c	a	1	0	0	0	0	1	1	0	1	$-u_{ca}$	u_{ca}	0	$-u_{ca}$	$-i_B$	0	i_B
57	b	c	b	0	0	1	0	1	0	0	1	0	u_{bc}	$-u_{bc}$	0	$-u_{bc}$	0	$-i_B$	i_B
58	b	c	b	0	0	1	0	1	0	1	0	1	u_{bc}	$-u_{bc}$	0	u_{bc}	0	$-i_B$	i_B
59	b	a	b	1	0	0	0	1	0	0	1	0	$-u_{ab}$	u_{ab}	0	u_{ab}	i_B	$-i_B$	0
60	b	a	b	0	1	0	1	0	0	1	0	1	$-u_{ab}$	u_{ab}	0	$-u_{ab}$	i_B	$-i_B$	0
61	c	c	a	1	0	0	0	0	1	0	0	1	0	u_{ca}	$-u_{ca}$	$-u_{ca}$	i_C	0	$-i_C$
62	c	c	a	0	0	1	1	0	0	1	1	0	0	u_{ca}	$-u_{ca}$	u_{ca}	i_C	0	$-i_C$
63	c	c	b	0	1	0	0	0	1	0	0	1	0	$-u_{bc}$	u_{bc}	u_{bc}	0	i_C	$-i_C$
64	c	c	b	0	0	1	0	1	0	1	1	0	0	$-u_{bc}$	u_{bc}	$-u_{bc}$	0	i_C	$-i_C$
65	a	a	b	0	1	0	1	0	0	0	0	1	0	u_{ab}	$-u_{ab}$	$-u_{ab}$	$-i_C$	i_C	0
66	a	a	b	1	0	0	0	1	0	1	1	0	0	u_{ab}	$-u_{ab}$	u_{ab}	$-i_C$	i_C	0
67	a	a	c	0	0	1	1	0	0	0	0	1	0	$-u_{ca}$	u_{ca}	u_{ca}	$-i_C$	0	i_C
68	a	a	c	1	0	0	0	0	1	1	1	0	0	$-u_{ca}$	u_{ca}	$-u_{ca}$	$-i_C$	0	i_C
69	b	b	c	0	0	1	0	1	0	0	0	1	0	u_{bc}	$-u_{bc}$	$-u_{bc}$	0	$-i_C$	i_C
70	b	b	c	0	1	0	0	0	1	1	1	0	0	u_{bc}	$-u_{bc}$	u_{bc}	0	$-i_C$	i_C
71	b	b	a	1	0	0	0	1	0	0	0	1	0	$-u_{ab}$	u_{ab}	u_{ab}	i_C	$-i_C$	0
72	b	b	a	0	1	0	1	0	0	1	1	0	0	$-u_{ab}$	u_{ab}	$-u_{ab}$	i_C	$-i_C$	0

Sparse Matrix Converter



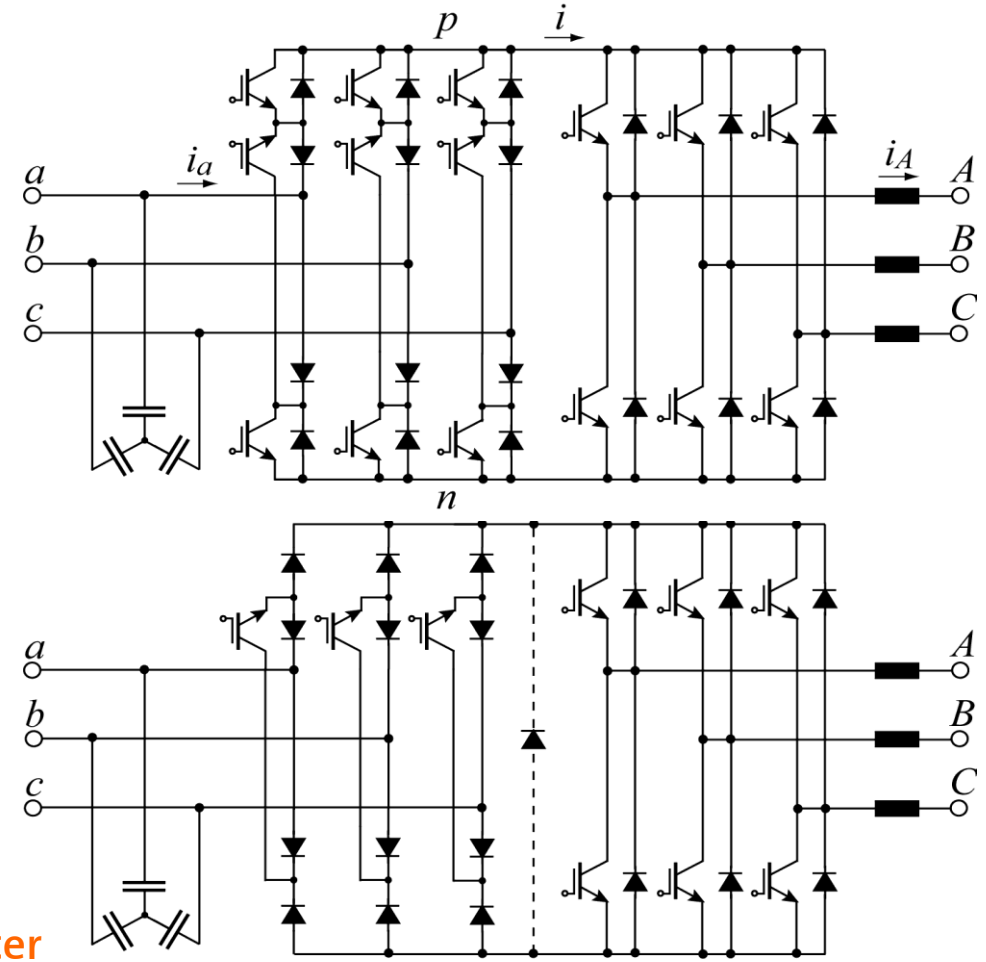
Derivation of the SMC Bridge Leg Topology



As the operation is restricted to $u_{pn}>0$ a blocking of S_{na} within the turn-on interval of S_{ap} is not required and both transistors could be combined in a single transistor S_a

Sparse Matrix Converter Topologies

Bidirectional
Sparse Matrix Converter (SMC)



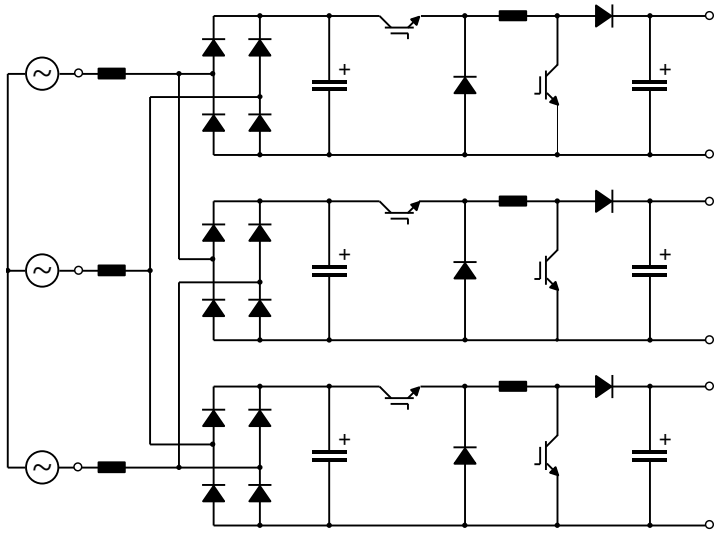
$\Phi_1 \in (-\frac{\pi}{6}, +\frac{\pi}{6})$

$\Phi_2 \in (-\frac{\pi}{6}, +\frac{\pi}{6})$

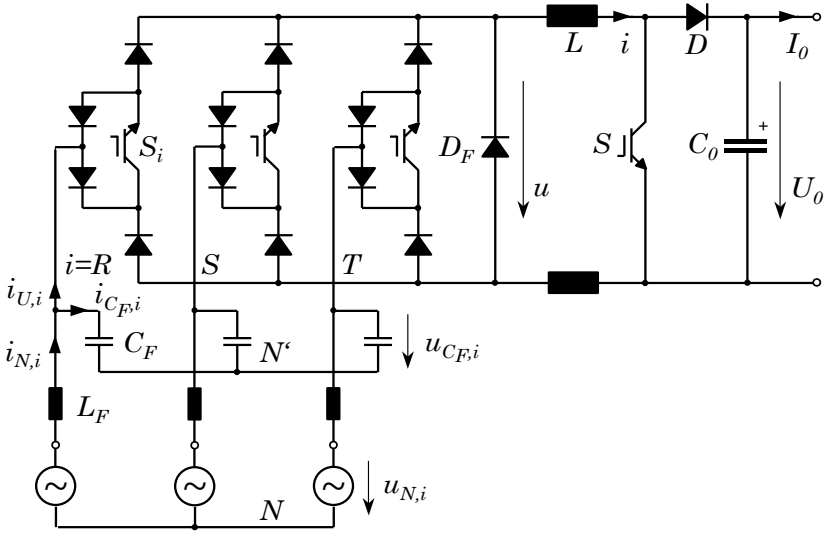
(USMC)
Unidirectional
Ultra Sparse Matrix Converter

USMC Relation to Three-Phase Buck+Boost PWM Rectifier

Modular

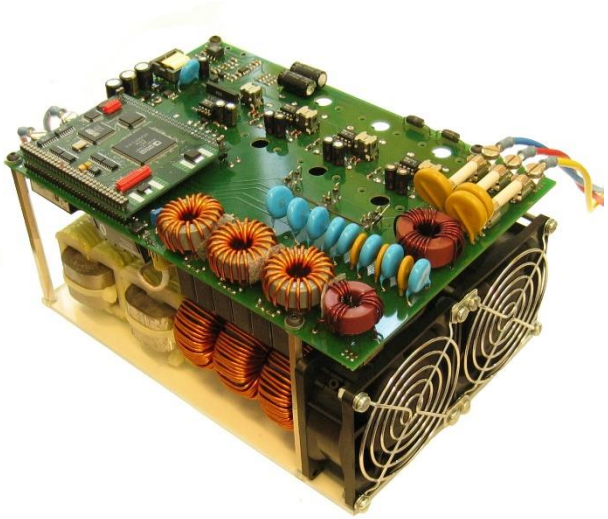


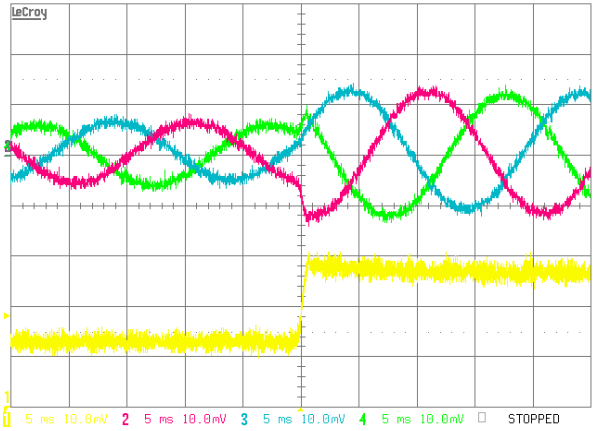
Direct Three-Phase



Three-Phase Buck+Boost Experimental Analysis

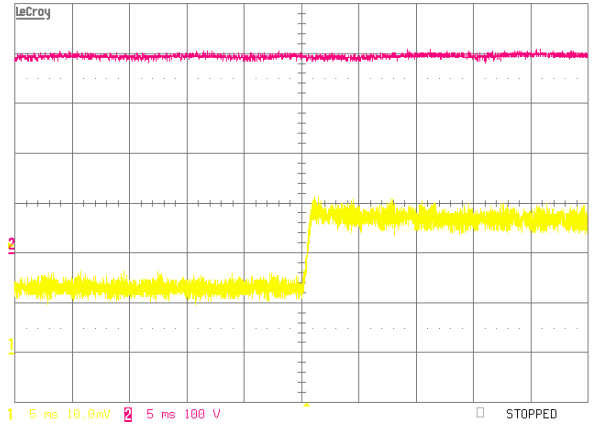
6kW
208...480V_{AC} / 50Hz
400V_{DC}



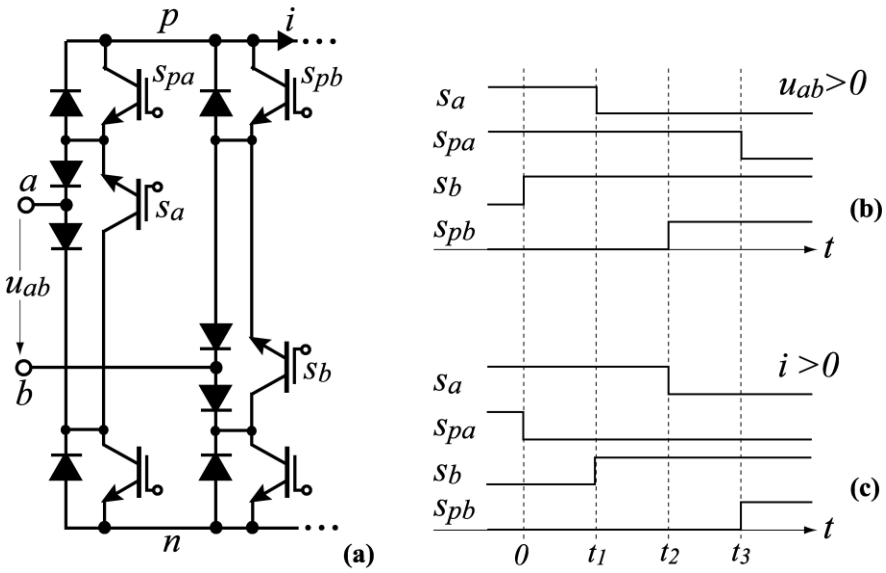


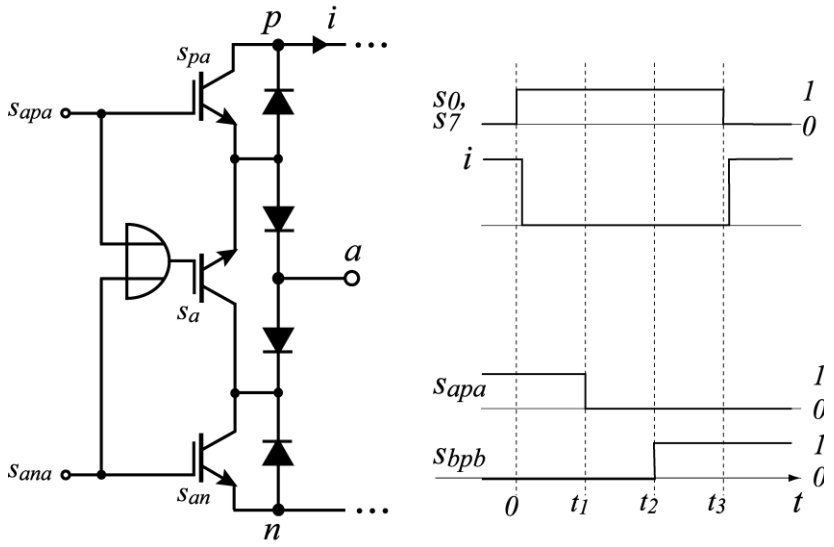
Load Step

2.76kW → 5.52kW



Commutation Strategies



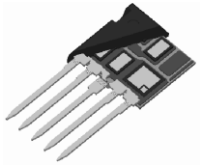


Multi-Step Commutation

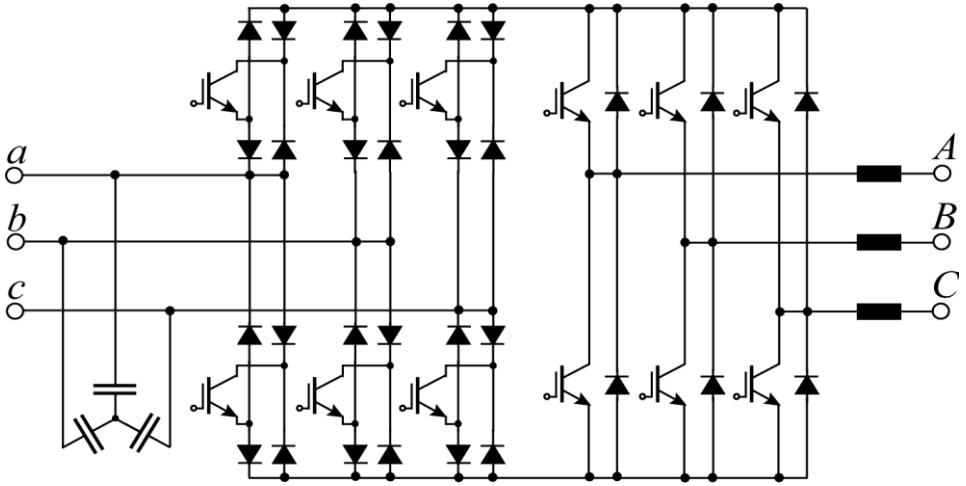
Zero DC Link Current Commutation

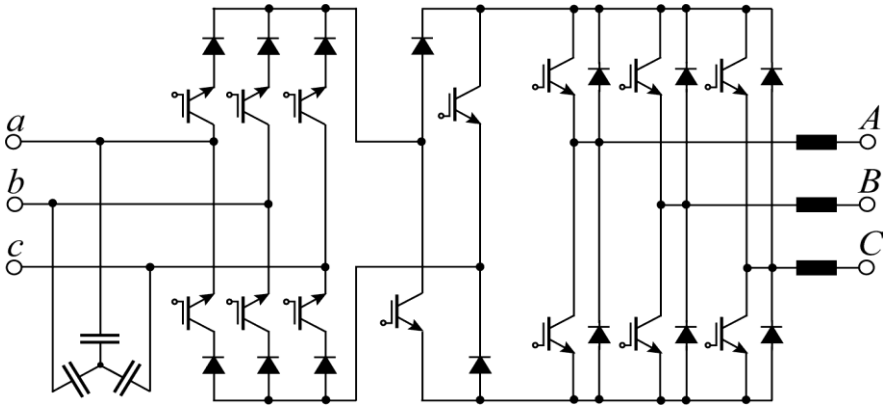
Sparse Matrix Converter Topologies cont.

Very Sparse Matrix Converter (VSMC)



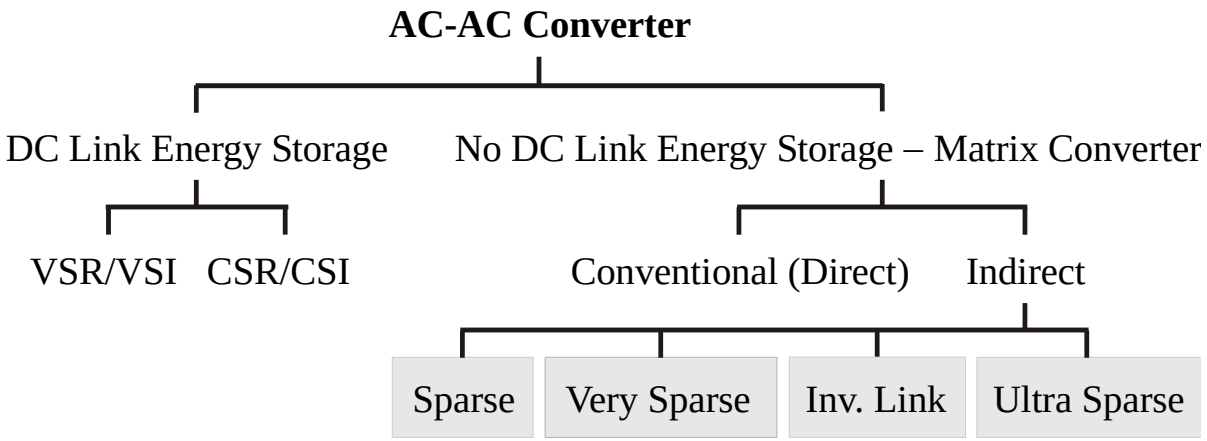
Four-Quadrant Switch
IXYS FIO 50-12BD





Inverting Link Matrix Converter

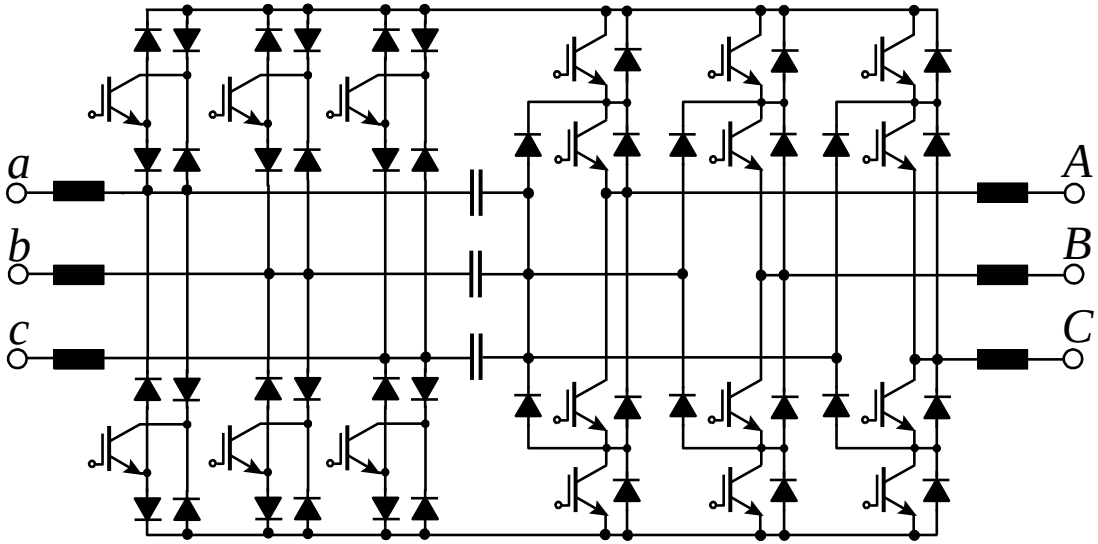
Classification of AC-AC Converter Topologies



Realization Effort

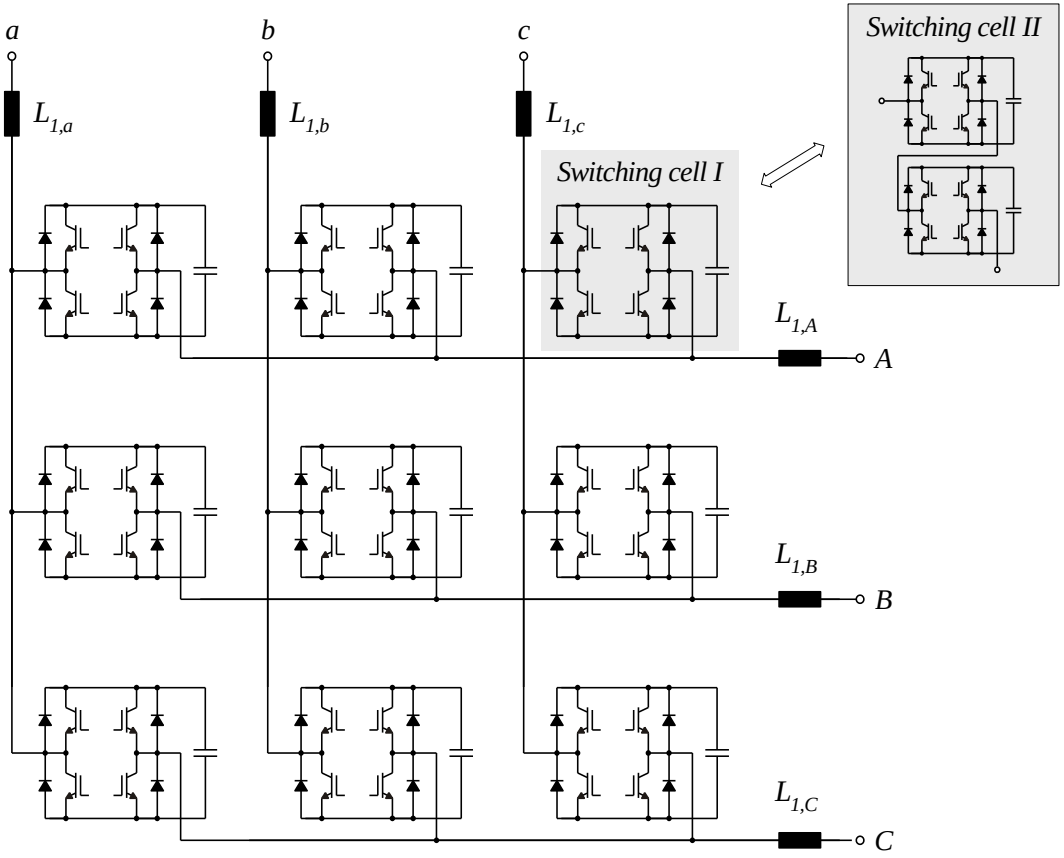
Converter Type	Transistors	Diodes	Isolated Driver Potentials
CMC	18	18	6
IMC	18	18	8
SMC	15	18	7
VSMC	12	30	10
USMC	9	18	7

Multi-Level SMC



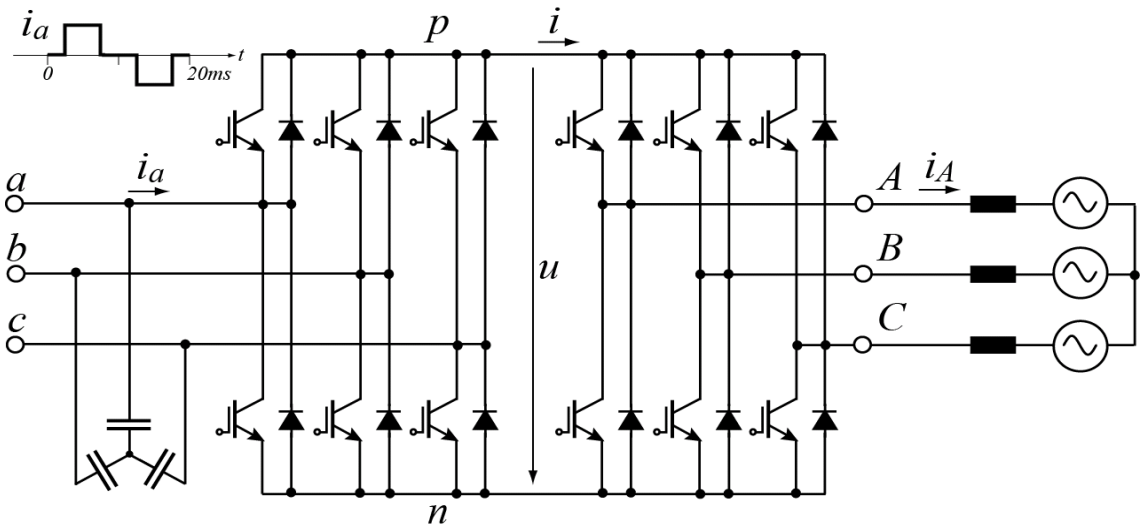
Three-Level-Output Sparse Matrix Converter

Multi-Level CMC



Family of Multi-Level CMC Topologies

Double-Bridge Matrix Converter



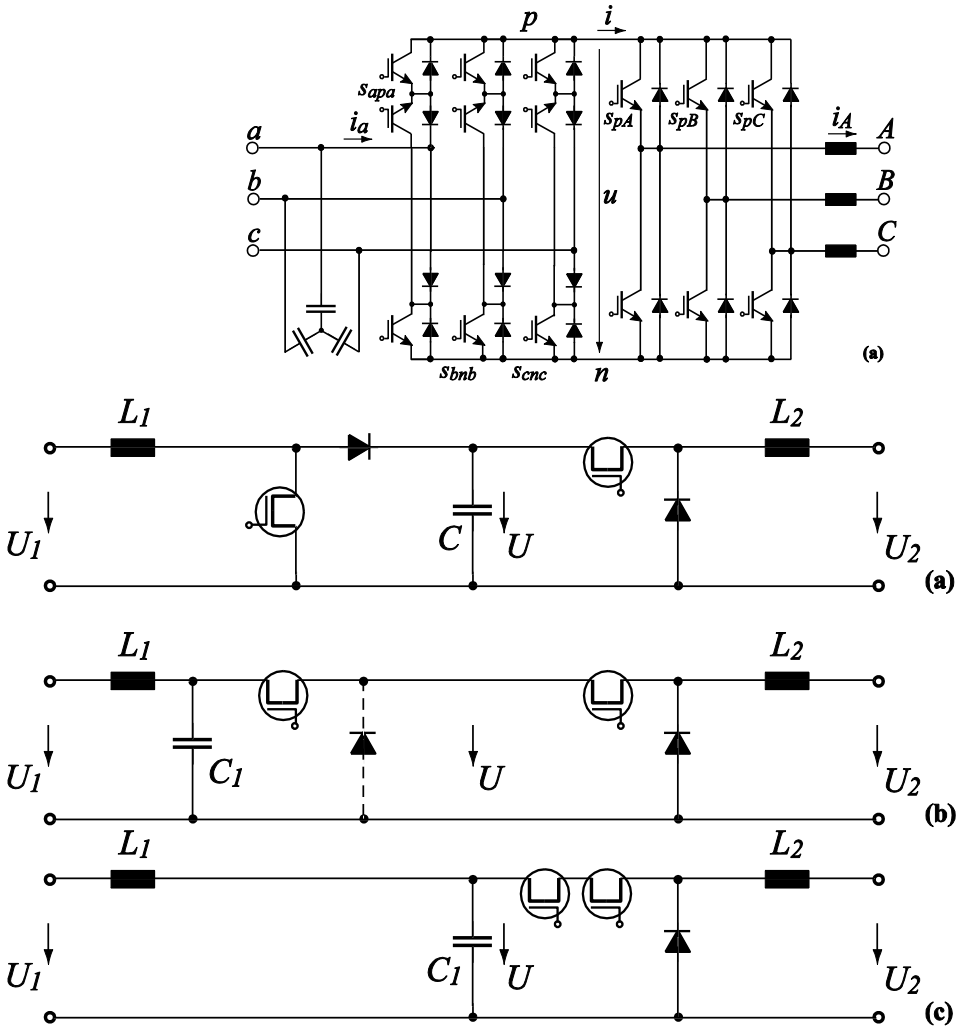
Non-Sinusoidal Input Current

Three-Phase AC-AC Matrix Converter

Advantages / Disadvantages in Comparison to Conventional Voltage DC Link System

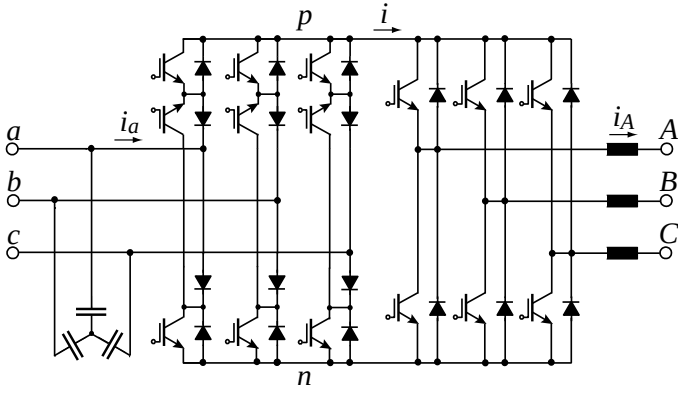
+ No Electrolytic Capacitor
+ No Braking Resistor
+ Lower Volume of Passive Components
+ Lower Switching Losses

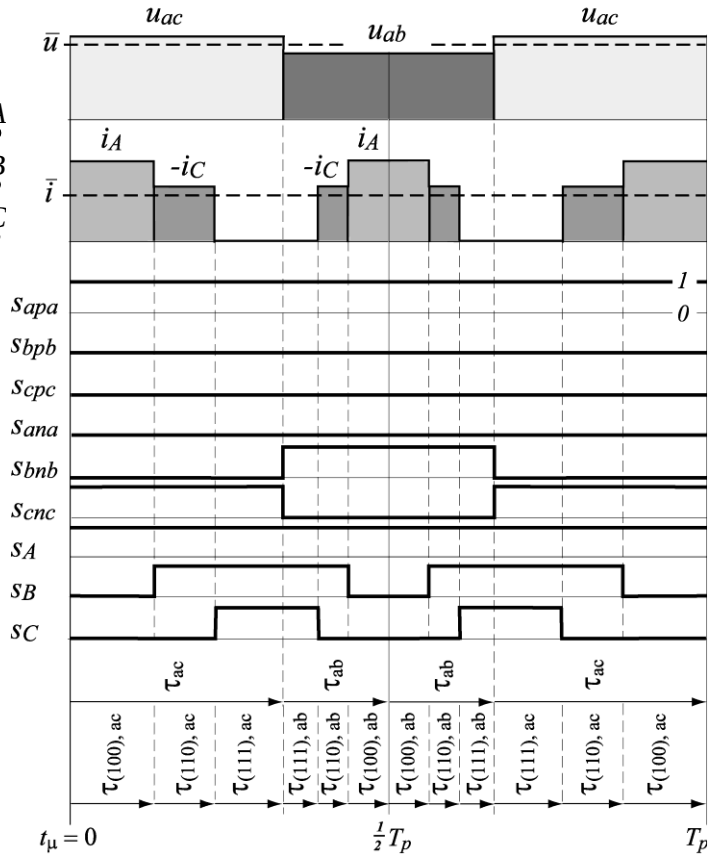
– Lower Output Voltage Range
– More Complex Modulation



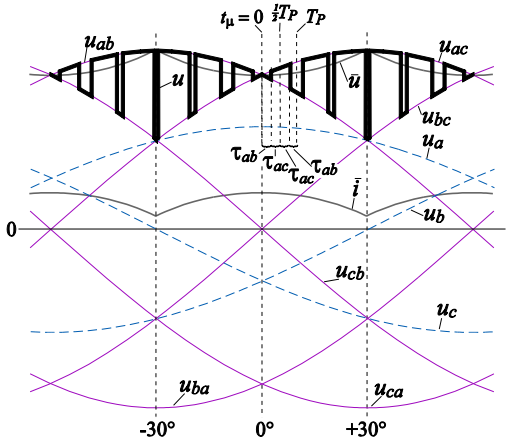
System Behavior

Local





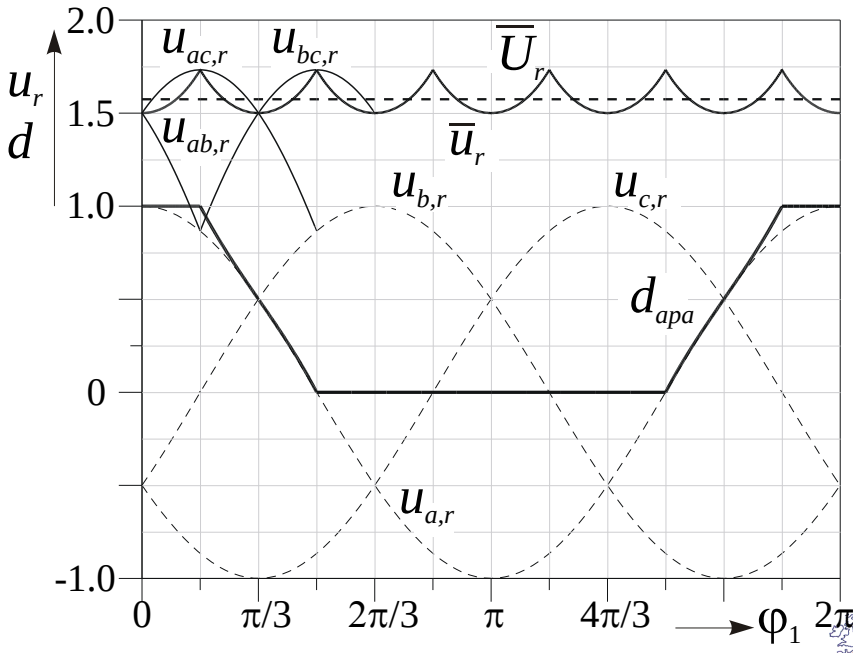
Global



Space Vector Modulation

Clamping of a Phase Input to *p* or *n*

$\varphi_1=\omega_1 t$	u_p	u_n	u
$0 \ldots \pi/6$	u_a	u_b, u_c	u_{ab}, u_{ac}
$\pi/6 \ldots \pi/2$	u_a, u_b	u_c	u_{ac}, u_{bc}
$\pi/2 \ldots 5\pi/6$	u_b	u_a, u_c	u_{ba}, u_{bc}
$5\pi/6 \ldots 7\pi/6$	u_b, u_c	u_a	u_{ba}, u_{ca}
$7\pi/6 \ldots 3\pi/2$	u_c	u_a, u_b	u_{ca}, u_{cb}
$3\pi/2 \ldots 11\pi/6$	u_a, u_c	u_b	u_{ab}, u_{cb}
$11\pi/6 \ldots 0$	u_a	u_b, u_c	u_{ab}, u_{ac}



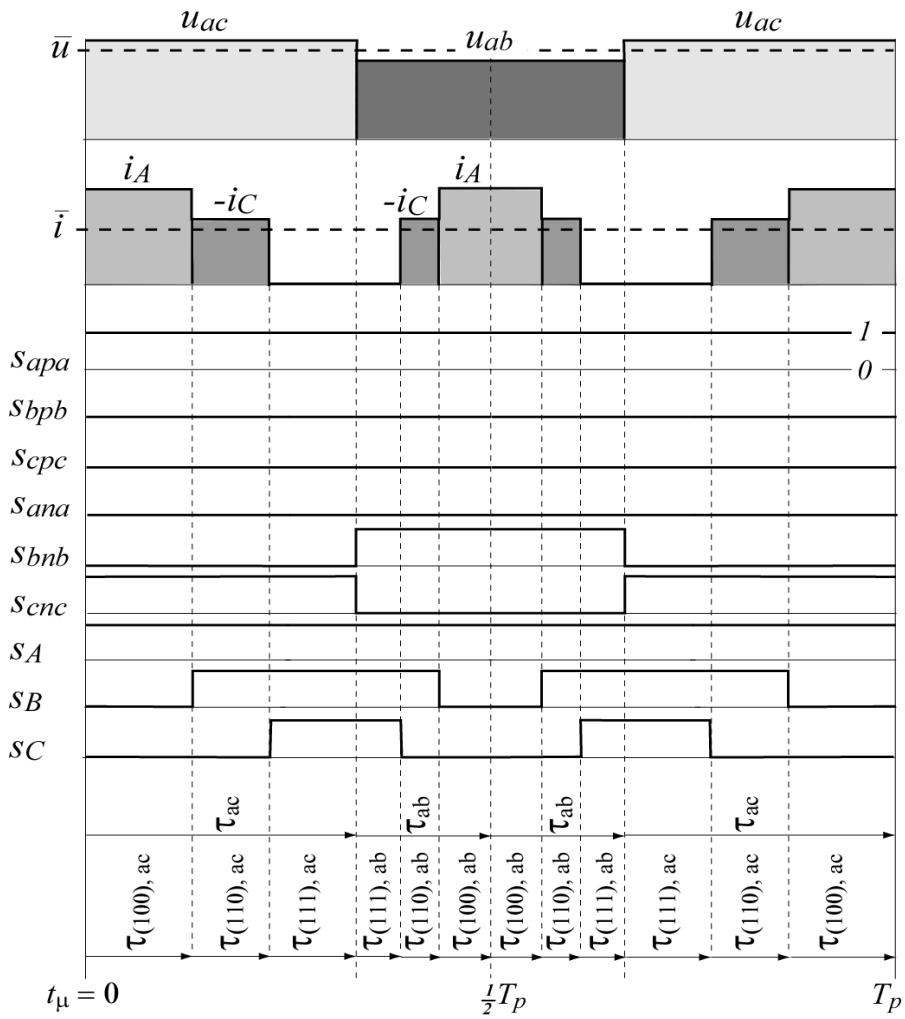
Input Voltages

$$u_a = \hat{U}_1 \cos(\omega_1 t)$$
$$u_b = \hat{U}_1 \cos(\omega_1 t - 2\pi/3)$$
$$u_c = \hat{U}_1 \cos(\omega_1 t + 2\pi/3)$$

Space Vector Modulation

Clamping of each Output Phase over a $\pi/3$-wide Interval for Minimizing Switching Losses

$\varphi_2=\omega_2 t$	u_A	u_B	u_C
0 ... $\pi/6$	u_p	u_p, u_n	u_p, u_n
$\pi/6$ ... $\pi/2$	u_p, u_n	u_p, u_n	u_n
$\pi/2$ ... $5\pi/6$	u_p, u_n	u_p	u_p, u_n
$5\pi/6$ ... $7\pi/6$	u_n	u_p, u_n	u_p, u_n
$7\pi/6$ ... $3\pi/2$	u_n, u_p	u_p, u_n	u_p
$3\pi/2$ ... $11\pi/6$	u_n, u_p	u_n	u_p, u_n
$11\pi/6$ ... 0	u_p	u_n, u_p	u_p, u_n



Space Vector Modulation

Intervals considered

$\varphi_1 = 0...\pi/6$ $\varphi_2 = 0...\pi/6$

Free-wheeling limited to Inverter Stage

$$d_{ab} + d_{ac} = 1$$

Local Average Value of Input Currents

$$\bar{i}_a = (d_{ab} + d_{ac})\,\bar{i}, \qquad \bar{i}_b = d_{ab}\bar{i}, \qquad \bar{i}_c = d_{ac}\bar{i}$$

Ohmic Fundamental Mains Behavior

$$\cos\Phi_1 = 1$$

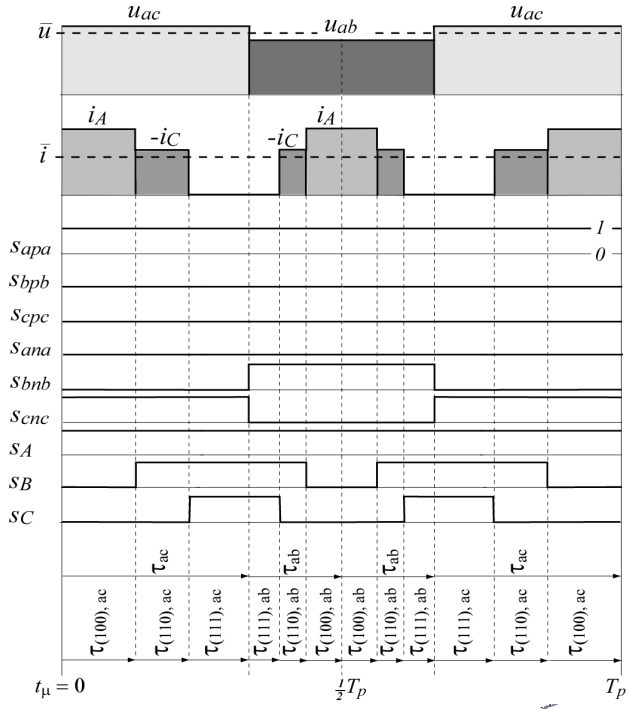
$$\bar{i}_a \sim u_a; \qquad \bar{i}_b \sim u_b; \qquad \bar{i}_c \sim u_c$$

Relative Turn-on Times

$$d_{ac} = -\frac{\bar{i}_c}{\bar{i}_a} = -\frac{u_c}{u_a}; \qquad d_{ab} = -\frac{\bar{i}_b}{\bar{i}_a} = -\frac{u_b}{u_a}$$

Time Intervals

$\tau_{ac} = d_{ac}T_P/2$ $\tau_{ab} = d_{ab}T_P/2$



Identical Phase/Duty Cycle of Active Inverter Switching States (100), (110) in τ_{ac} and τ_{ab}

$$\delta_{(100),ac} = \frac{\tau_{(100),ac}}{\tau_{ac}} = \delta_{(100),ab} = \frac{\tau_{(100),ab}}{\tau_{ab}} = \delta_{(100)} \qquad \underline{u}_{(100)} = \tfrac{2}{3}u$$

$$\delta_{(110),ac} = \frac{\tau_{(110),ac}}{\tau_{ac}} = \delta_{(110),ab} = \frac{\tau_{(110),ab}}{\tau_{ab}} = \delta_{(110)} \qquad \underline{u}_{(110)} = \tfrac{2}{3}ue^{j\frac{\pi}{3}}$$

Generated Output Voltage Space Vector

$$\underline{u}_2^* = \frac{\frac{2}{3}}{\frac{T_P}{2}}(u_{ac}\tau_{(100),ac} + u_{ab}\tau_{(100),ab} + u_{ac}e^{j\frac{\pi}{3}}\tau_{(110),ac} + u_{ab}e^{j\frac{\pi}{3}}\tau_{(110),ab})$$

$$\underline{u}_2^* = \frac{\frac{2}{3}}{\frac{T_P}{2}}(u_{ac}\tau_{ac}\delta_{(100)} + u_{ab}\tau_{bc}\delta_{(100)} + u_{ac}\tau_{ac}\delta_{(110)}e^{j\frac{\pi}{3}} + u_{ab}\tau_{bc}\delta_{(110)}e^{j\frac{\pi}{3}}$$

$$= \tfrac{2}{3}(u_{ac}\frac{\tau_{ac}}{\frac{1}{2}T_P} + u_{ab}\frac{\tau_{ab}}{\frac{1}{2}T_P})\delta_{(100)} + \tfrac{2}{3}(u_{ac}\frac{\tau_{ac}}{\frac{1}{2}T_P} + u_{ab}\frac{\tau_{ab}}{\frac{1}{2}T_P})e^{j\frac{\pi}{3}}\delta_{(110)}$$

$$= \tfrac{2}{3}(u_{ac}d_{ac} + u_{ab}d_{ab})\delta_{(100)} + \tfrac{2}{3}(u_{ac}d_{ac} + u_{ab}d_{ab})e^{j\frac{\pi}{3}}\delta_{(110)}.$$

Local Average Value of the DC Link Voltage

$$\bar{u} = u_{ab}d_{ab} + u_{ac}d_{ac}$$

Output Voltage Space Vector

$$\underline{u}_2^* = \tfrac{2}{3}\bar{u}\delta_{(100)} + \tfrac{2}{3}\bar{u}e^{j\frac{\pi}{3}}\delta_{(110)}$$

Therefore, the Calculating of the Relative On-Times of the Active Switching States of the Output Stage can be directly Based on $\bar{u}$

$$\delta_{(100)} = \frac{\sqrt{3}}{2}\frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}}\cos(\varphi_2^* + \tfrac{\pi}{6})$$

$$\delta_{(110)} = \frac{\sqrt{3}}{2}\frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}}\sin\varphi_2^*$$

$$\tau_{(100),ac} = -\frac{1}{\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_c\cos(\varphi_2^* + \tfrac{\pi}{6})$$

$$\tau_{(100),ab} = -\frac{1}{\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_b\cos(\varphi_2^* + \tfrac{\pi}{6})$$

$$\tau_{(110),ac} = -\frac{1}{\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_c\sin\varphi_2^*$$

$$\tau_{(110),ab} = -\frac{1}{\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_b\sin\varphi_2^*$$

Absolute On-Times

Local Average Value of the DC Link Voltage

$$\bar{u} = \tfrac{3}{2}\hat{U}_1\frac{1}{\cos(\omega_1 t)} \qquad \bar{u}_{\min} = 3/2\,\hat{U}_1$$

Output Voltage System

$$u_A^* = \hat{U}_2^*\cos(\omega_2 t + \varphi_0)$$

$$u_B^* = \hat{U}_2^*\cos(\omega_2 t - \tfrac{2\pi}{3} + \varphi_0)$$

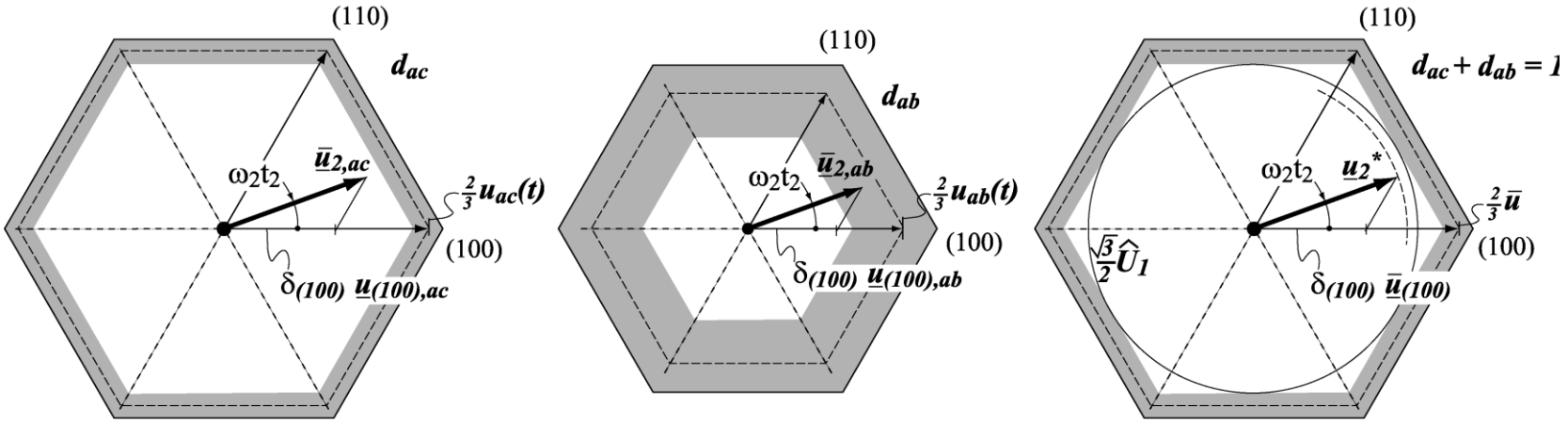
$$u_C^* = \hat{U}_2^*\cos(\omega_2 t + \tfrac{2\pi}{3} + \varphi_0)$$

Voltage Transfer Ratio

$$M = \frac{\hat{U}_2^*}{\hat{U}_1} \le \frac{\sqrt{3}}{2}$$

Output Voltage Formation

$$\hat{U}_{2,\max} = \frac{\sqrt{3}}{2} \cdot \hat{U}_1 = 0.866 \cdot \hat{U}_1$$



Inverter Output Voltage Space Vectors

Average Output Voltage

Variation of $\bar{u}$ makes Necessary a Variation of the Inverter Modulation Index

$$m_2 = \frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}} = \frac{4}{3}\frac{\hat{U}_2^*}{\hat{U}_1}\cos(\omega_1 t)$$

Input Current Formation

Load Phase Currents

$$i_A = \hat{I}_2 \cos(\omega_2 t + \Phi_2)$$
$$i_B = \hat{I}_2 \cos(\omega_2 t - \tfrac{2\pi}{3} + \Phi_2)$$
$$i_C = \hat{I}_2 \cos(\omega_2 t + \tfrac{2\pi}{3} + \Phi_2)$$

Verify Equal Local Average Value $\bar{\imath}$ of the DC Link Current in τ_{ac} and τ_{ab}

$$\bar{i}_{ac} = \frac{1}{\tau_{ac}}(i_A \delta_{(100),ac}\tau_{ac} - i_C \delta_{(110),ac}\tau_{ac}) = i_A \delta_{(100)} - i_C \delta_{(110)}$$
$$\bar{i}_{ab} = \frac{1}{\tau_{ab}}(i_A \delta_{(100),ab}\tau_{ab} - i_C \delta_{(110),ab}\tau_{ab}) = i_A \delta_{(100)} - i_C \delta_{(110)}$$

$$\bar{i} = \bar{i}_{ac} = \bar{i}_{ab} = \frac{3}{4} m_2 \hat{I}_2 \cos\Phi_2 = \hat{I}_2 \frac{\hat{U}_2^*}{\hat{U}_1}\cos\Phi_2 \cos(\omega_1 t)$$

Variation of Input Stage Modulation Index due to Varying $\bar{\imath}$

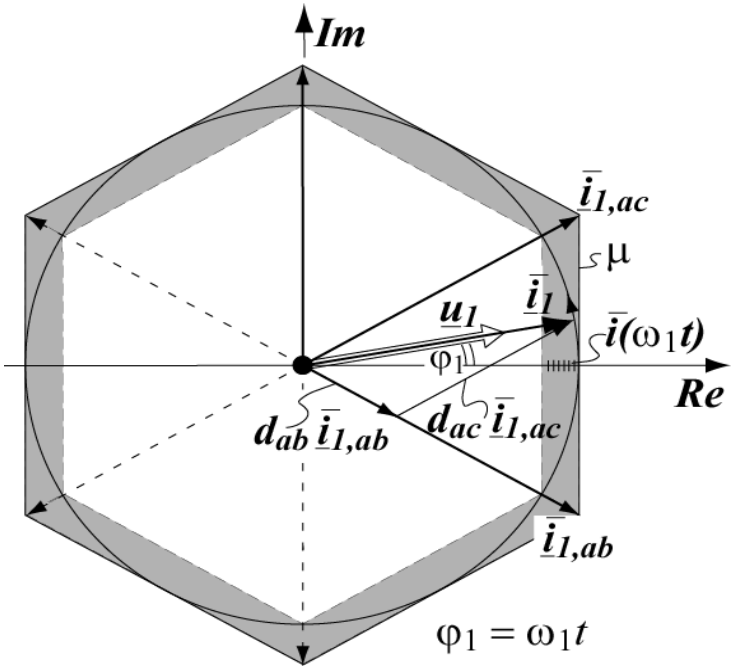
$$m_1 = \frac{|\underline{\bar{i}}_1|}{\bar{i}} = \frac{1}{\cos\omega_1 t}$$

Resulting Input Current Space Vector

$$|\underline{\bar{i}}_1| = \bar{i}\, m_1 = \hat{I}_2 \frac{\hat{U}_2^*}{\hat{U}_1} \cos\Phi_2 \cos(\omega_1 t) \frac{1}{\cos\omega_1 t} = \hat{I}_1$$

Resulting Input Phase Currents

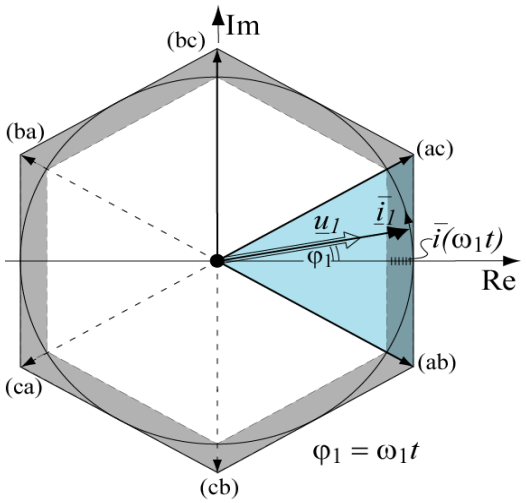
$$\bar{i}_a = \hat{I}_1 \cos(\omega_1 t)$$
$$\bar{i}_b = \hat{I}_1 \cos(\omega_1 t - \tfrac{2\pi}{3})$$
$$\bar{i}_c = \hat{I}_1 \cos(\omega_1 t + \tfrac{2\pi}{3})$$



Space Vector Modulation Summary

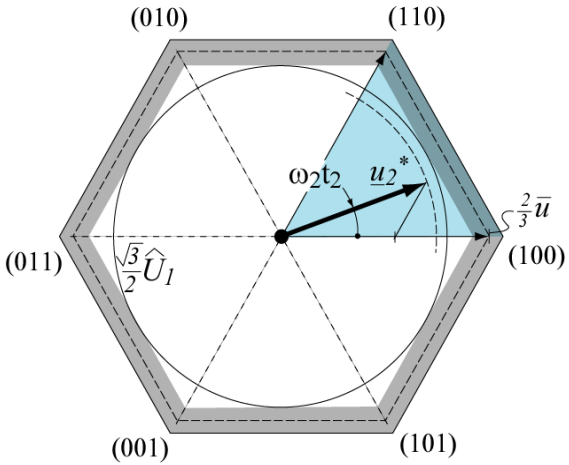
Rectifier Stage

Phase of Resulting
Input Current is Adjustable



Inverter Stage

Output Voltage Vector u_2^*
is Adjustable



Applied Pulse Pattern is Specific for Each Combination of Active Sectors (6 x 6 = 36 Cases) !

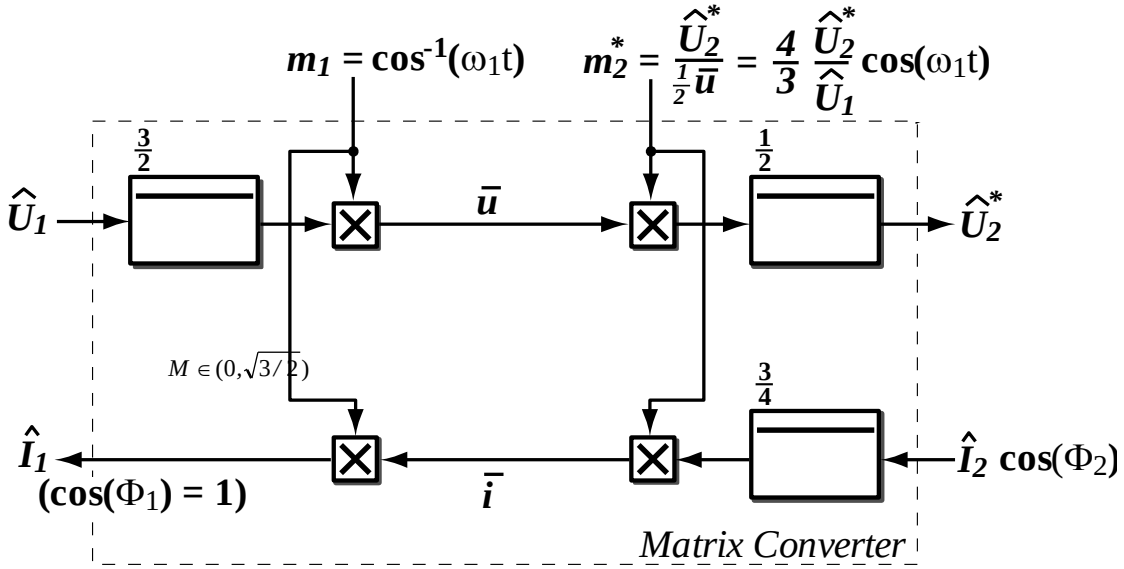
Input/Output Voltage and Current Transfer

$$\hat{I}_1 = m_1 \bar{i} = \tfrac{3}{4} m_1 m_2 \hat{I}_2 \cos\Phi_2$$

$$\frac{\hat{I}_1}{\hat{I}_2} = \tfrac{3}{4} m_1 m_2 \cos\Phi_2$$

$$\tfrac{3}{2}\hat{U}_1\hat{I}_1 = \bar{u}\,\bar{i} = \tfrac{3}{2}\hat{U}_2^*\hat{I}_2\cos\Phi_2$$

$$\frac{\hat{U}_2^*}{\hat{U}_1} = \frac{\hat{I}_1}{\hat{I}_2}\frac{1}{\cos\Phi_2} = \tfrac{3}{4} m_1 m_2$$



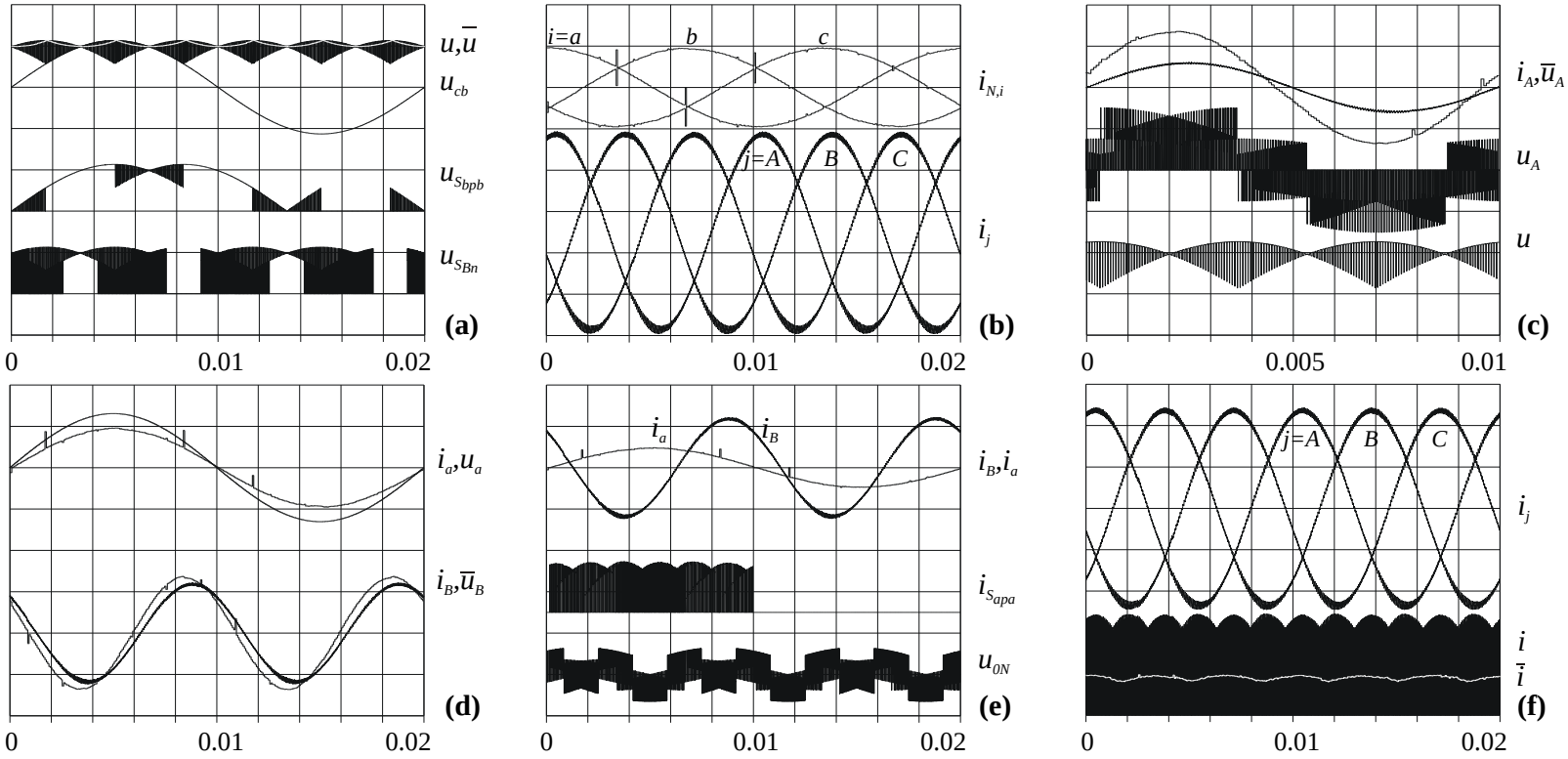
Voltage and Current Transfer Ratio

$$M = \tfrac{3}{4} m_1 m_2$$

$\cos\Phi_1 = 1$ $\quad \hat{U}_2^* = M\hat{U}_1 \quad M \in (0,\sqrt{3}/2)$ $\quad \hat{U}_2^* = M\hat{U}_1\cos\Phi_1$

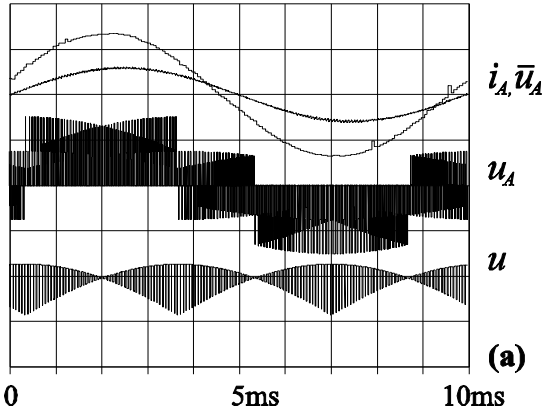
$$\hat{I}_1 = M\hat{I}_2\cos\Phi_2 \qquad \hat{I}_1 = M\hat{I}_2\cos\Phi_2$$

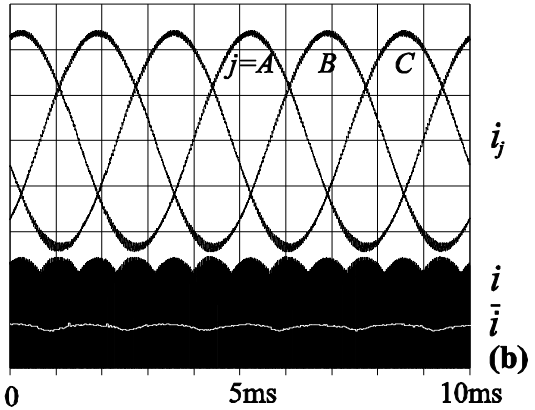
Simulation Results

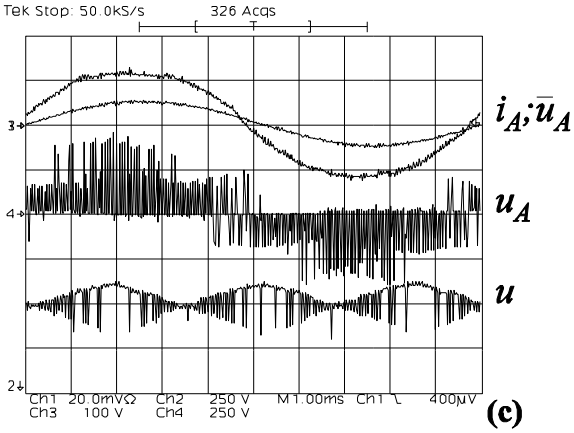


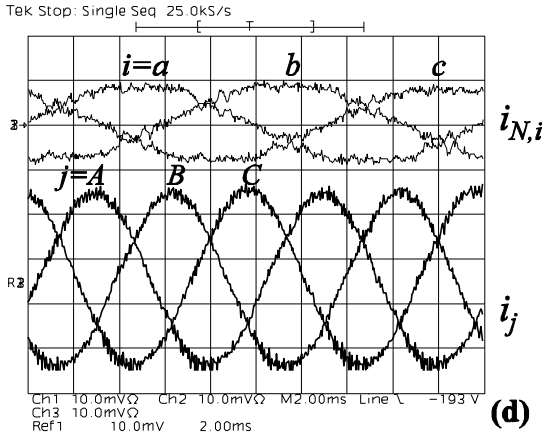
Experimental Analysis

7.5kW
400V_{AC} / 50Hz
2.5kW/dm³



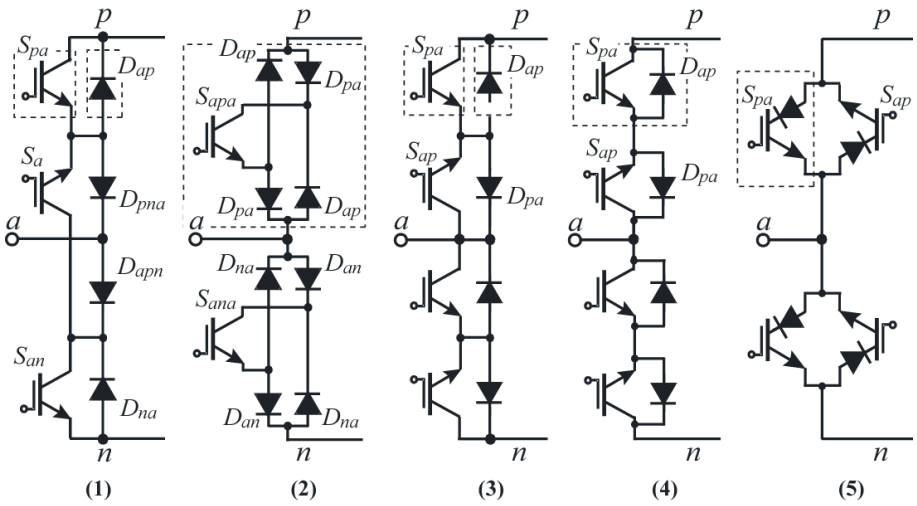


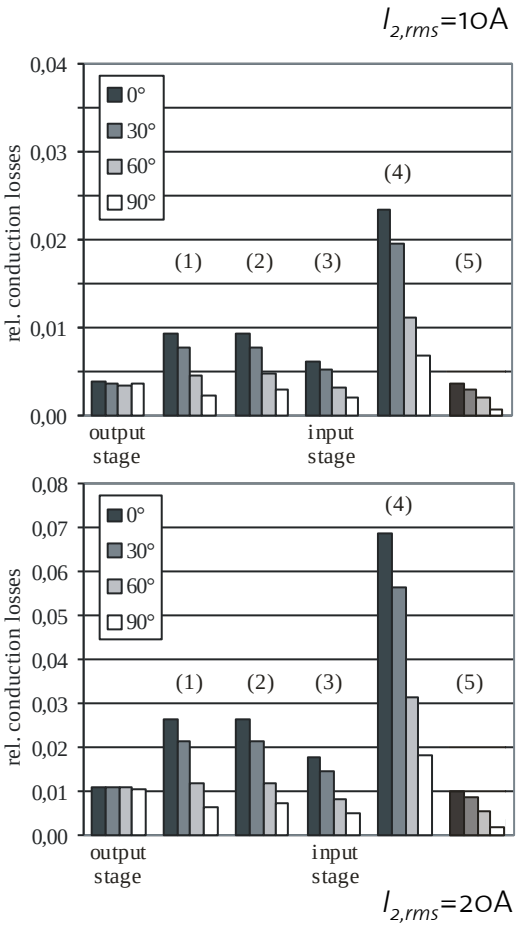




Realization of the Input Stage

Relative Conduction Losses of Input and Output Stage (M_2=1)





Conclusions

- Matrix Converter Functionality can be Achieved Employing Only 12 IGBTs
- High Reliability Due to Zero DC Link Current Commutation
- Lower Switching Losses than Voltage DC Link Rectifier/Inverter Combination
- Relatively Low Output Voltage Range
- ETHZ *Sparse Matrix Converter* Technology Evaluation Package !

Coffee Break…

Modulation Schemes II

Frank Schafmeister

- Conventional Multi-Step Commutation
- Zero DC Link Current Commutation (for SMC / IMC)

- Optimized Output Stg. Clamping

- High Output Voltage (HV)
- Low Output Voltage (LV)

- Switching Loss Shifting (for SMC / IMC)

- Reactive Power Coupling

Voltage Transfer Matrix $\underline{S}_{CMC}$

$$\begin{pmatrix} u_A \\ u_B \\ u_C \end{pmatrix} = \begin{pmatrix} spA & snA \\ spB & snB \\ spC & snC \end{pmatrix} \cdot \begin{pmatrix} sap & sbp & scp \\ san & sbn & scn \end{pmatrix} \cdot \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix}$$

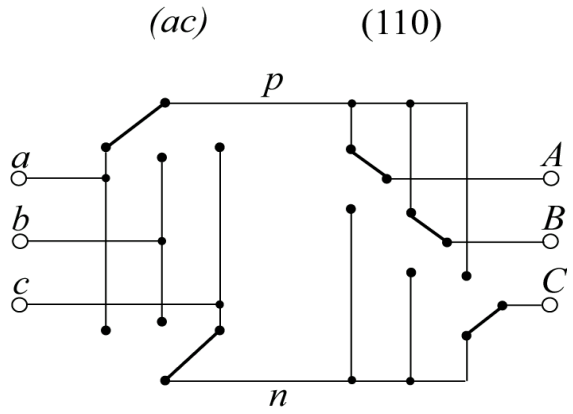
$$\underline{u}_{ABC} = \underline{S}_{Inv} \cdot \underline{S}_{\mathrm{Rect}} \cdot \underline{u}_{abc}$$

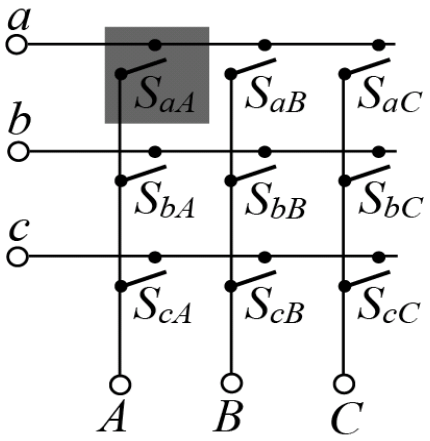
$$\underline{u}_{ABC} = \underline{S}_{CMC} \cdot \underline{u}_{abc}$$

Current Transfer Matrix $\underline{S}_{CMC}^{T}$

$$\underline{i}_{abc} = \underline{S}_{CMC}^{T} \cdot \underline{i}_{ABC}$$

Equivalent Sw. States: IMC ⇄ CMC





$s_{SMC,Rect}$	(ac)			(ab)		
$s_{SMC,Inv}$	(110)	(100)	(000)	(000)	(100)	(110)
$\underline{S}_{CMC}^{T}$	1 1 0 0 0 0 0 0 1	1 0 0 0 0 0 0 1 1	0 0 0 0 0 0 1 1 1	0 0 0 1 1 1 0 0 0	1 0 0 0 1 1 0 0 0	1 1 0 0 0 1 0 0 0
$\delta_{110}+\delta_{100}+$ $+\delta_{000}=1$	δ_{110}	δ_{100}	δ_{000}	δ_{000}	δ_{100}	δ_{110}
$d_{ac}+d_{ab}=1$	d_{ac}			d_{ab}		

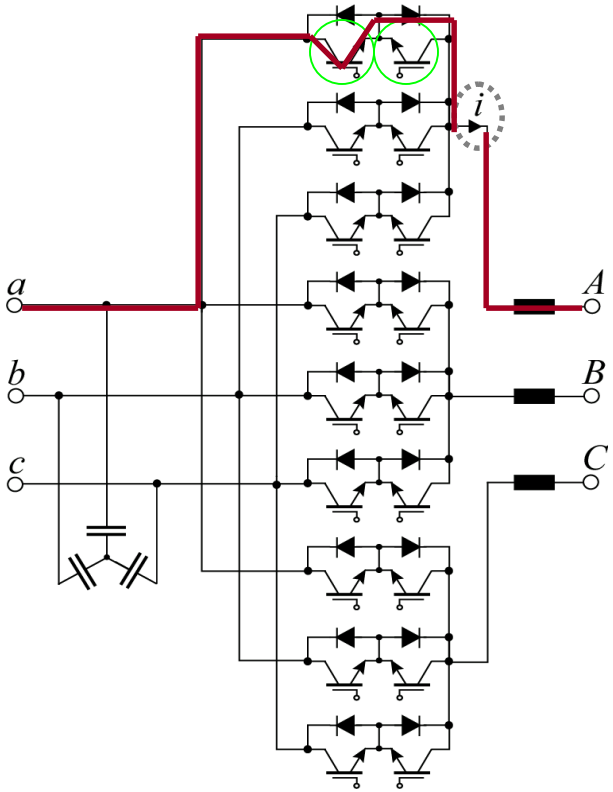
Outline of Presentation

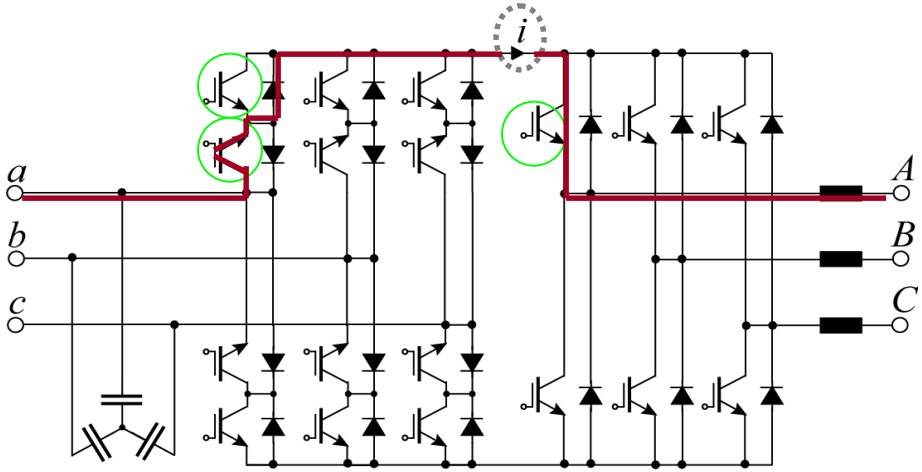
Matrix Modulation Schemes

- **Conventional Multi-Step Commutation**
- Zero DC Link Current Commutation (for SMC / IMC)
- Optimized Output Stg. Clamping
- High Output Voltage (HV)
- Low Output Voltage (LV)
- Switching Loss Shifting (for SMC / IMC)
- Reactive Power Coupling

Commutation
of Matrix Converter

- **Commutation Strategy** for **CMC / IMC: Multi-Step Comm.**
  Constraints: No Interruption of *i*
  No Short Circuit of Mains Phases

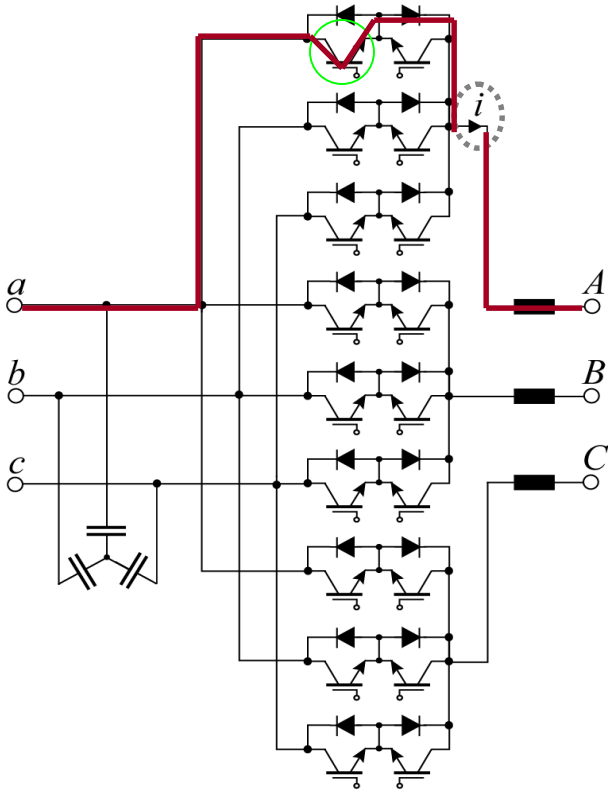




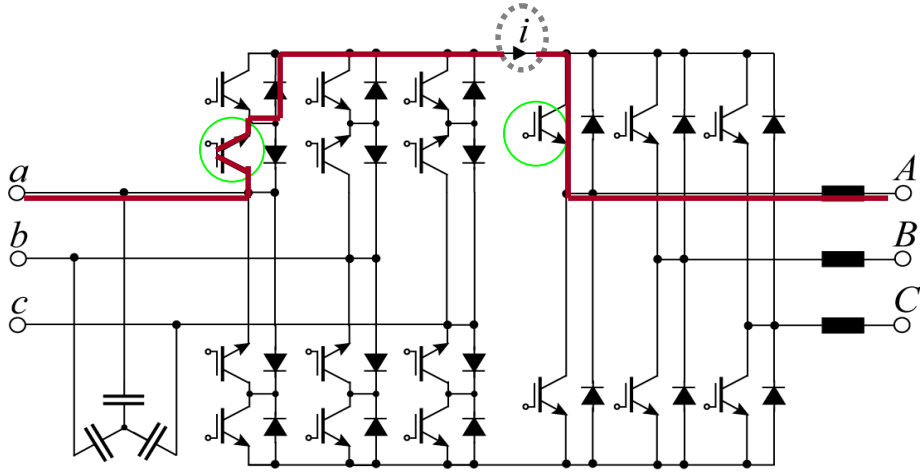
- (exempl. $\underline{i > 0}$, $u_{ab} < 0$, $aA \rightarrow bA$)

Commutation
of Matrix Converter

- **Commutation Strategy** for **CMC / IMC: Multi-Step Comm.**
  Constraints: No Interruption of *i*
  No Short Circuit of Mains Phases



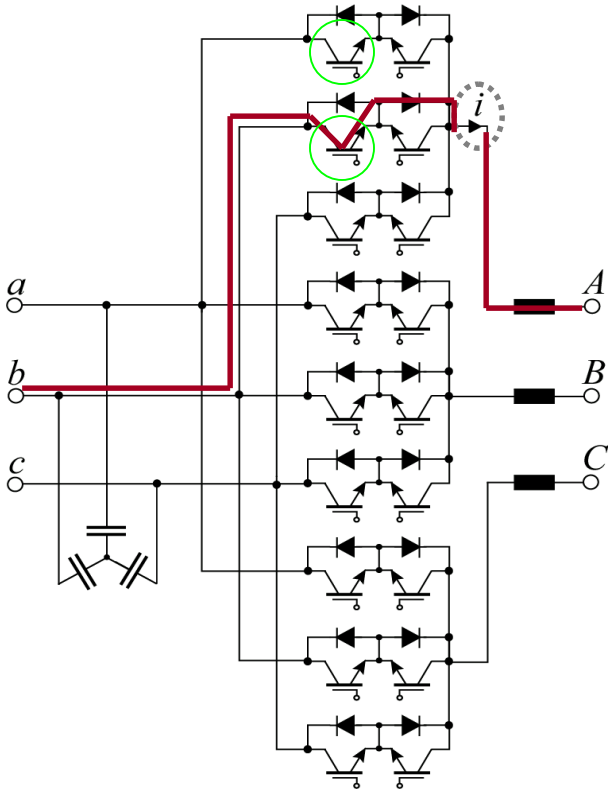
1st Step: off



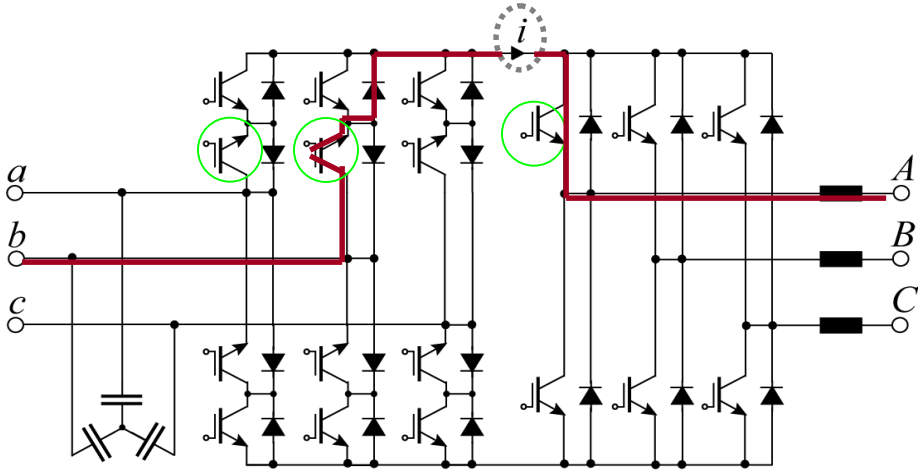
- (exempl. $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$)

Commutation
of Matrix Converter

- **Commutation Strategy for CMC / IMC: Multi-Step Comm.**
  Constraints: No Interruption of *i*
  No Short Circuit of Mains Phases



1st Step: off
2nd Step: on



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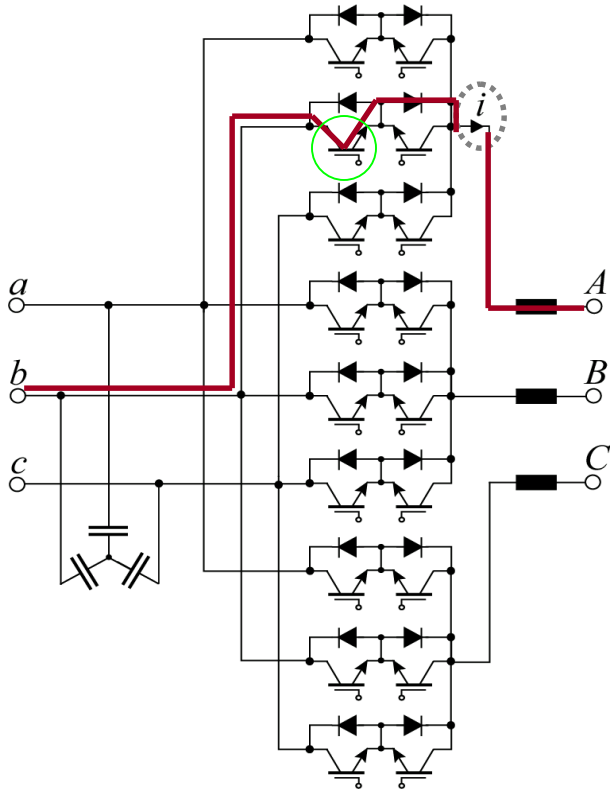
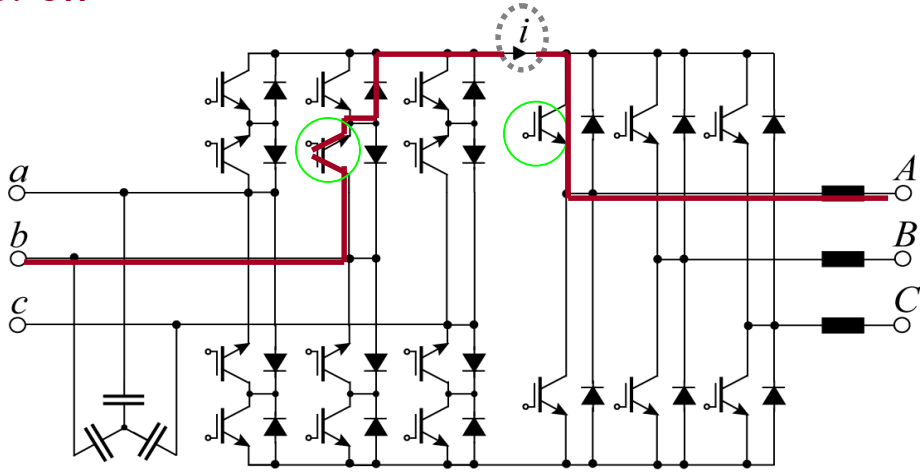


1st Step: off
2nd Step: on
3rd Step: off



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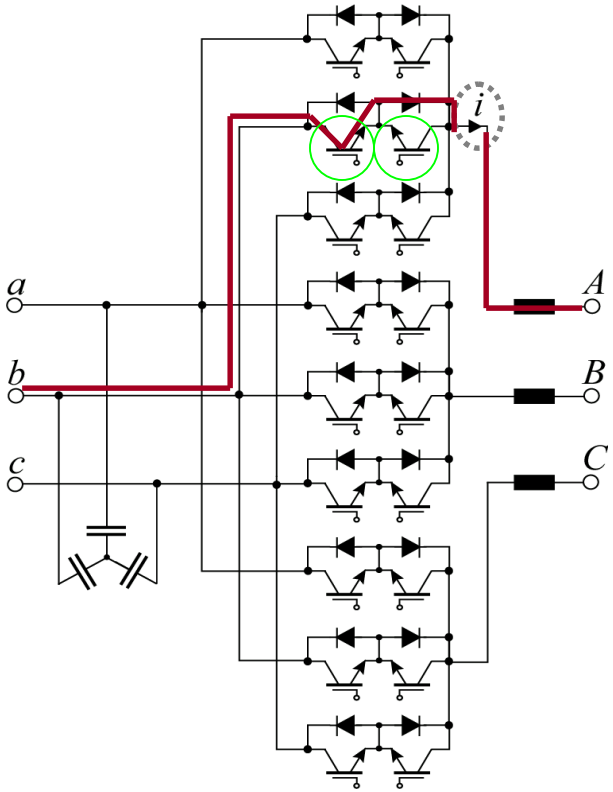
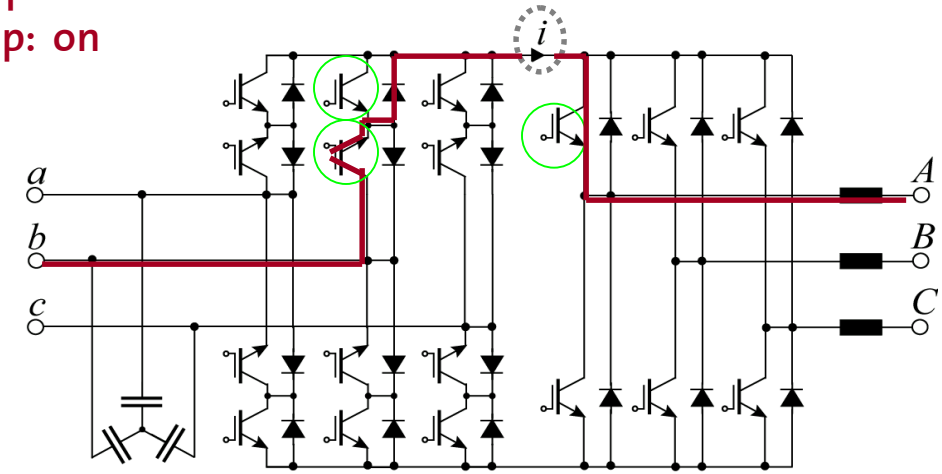


1st Step: off
2nd Step: on
3rd Step: off
4th Step: on



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Commutation
of Matrix Converter

- **Commutation Strategy for CMC / IMC: Multi-Step Comm.**

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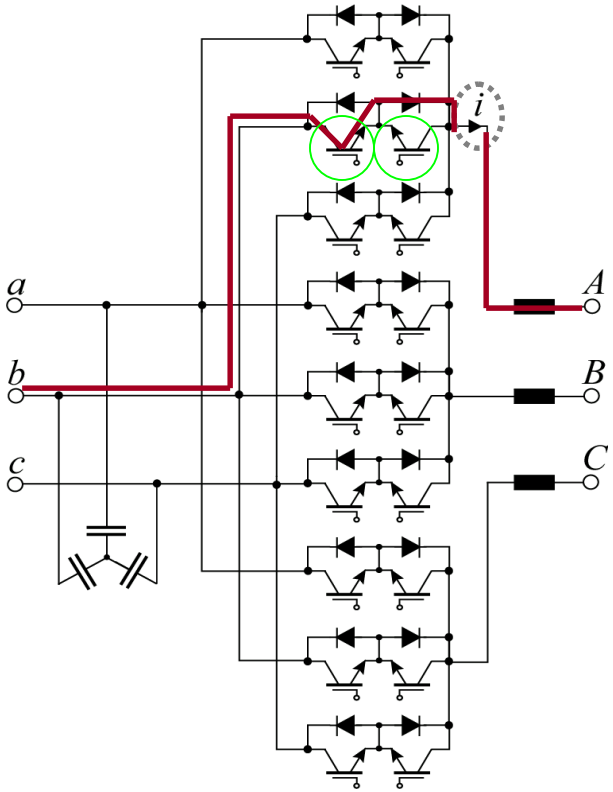
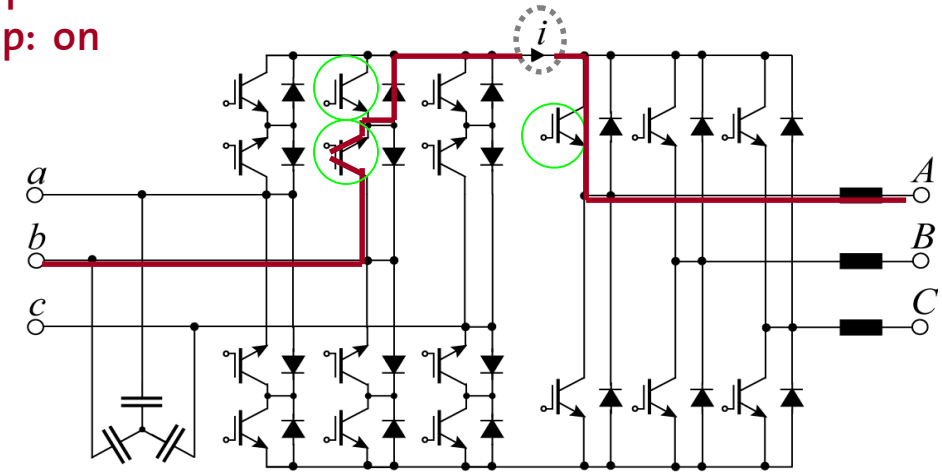
  No Short Circuit of Mains Phases



1st Step: off
2nd Step: on
3rd Step: off
4th Step: on

→ Sequence Depends on (Measured) Current Sign !



- (exempl. $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$)

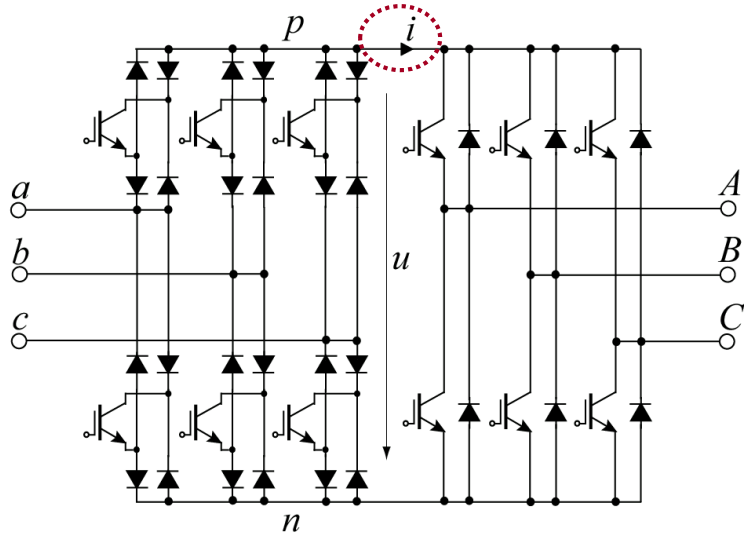
Outline of Presentation

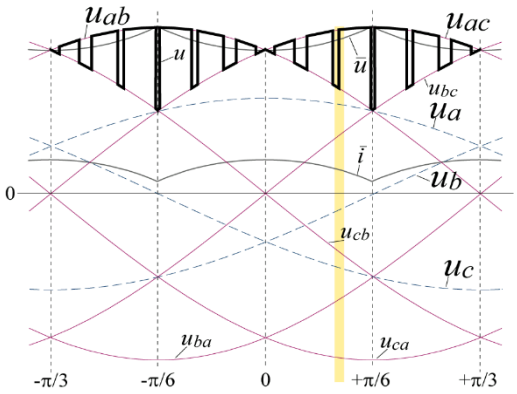
Matrix Modulation Schemes

- Conventional Multi-Step Commutation
- **Zero DC Link Current Commutation (for SMC / IMC)**
- Optimized Output Stg. Clamping
- High Output Voltage (HV)
- Low Output Voltage (LV)
- Switching Loss Shifting (for SMC / IMC)
- Reactive Power Coupling

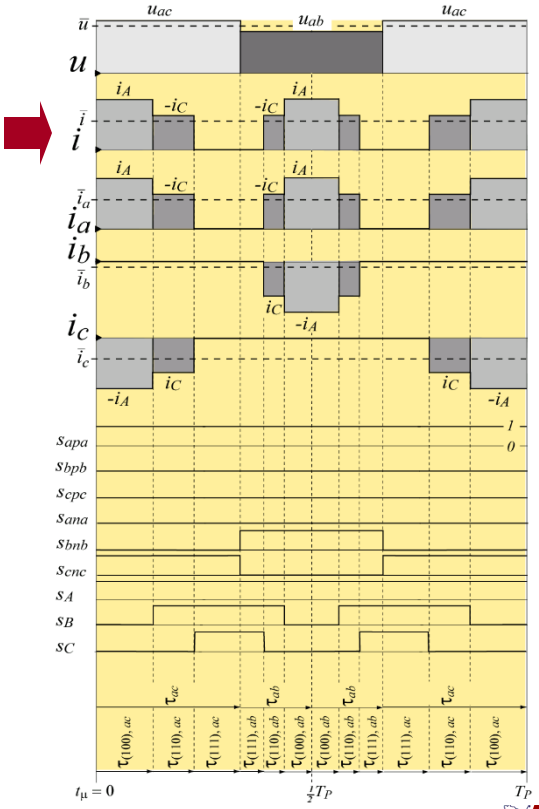
Commutation of Matrix Converter

Commutation Strategy for Sparse MC: Zero DC Link Current Comm. (HV)





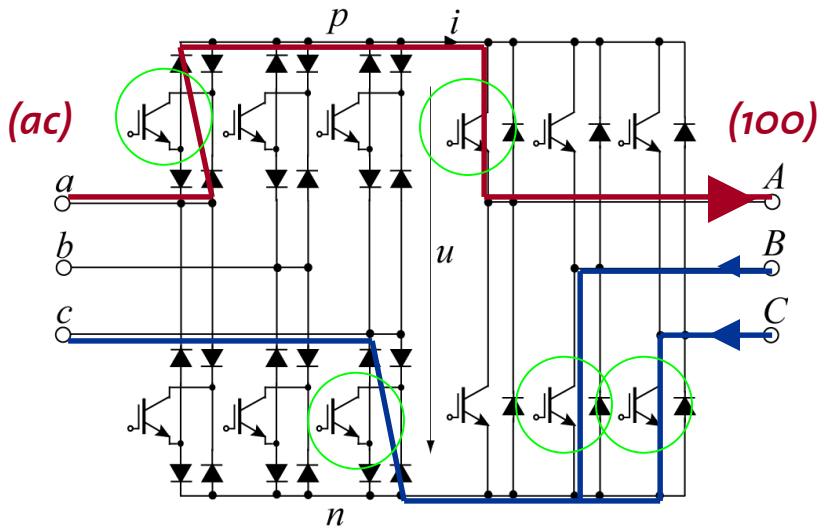
1/3 Mains Period



Pulse Period

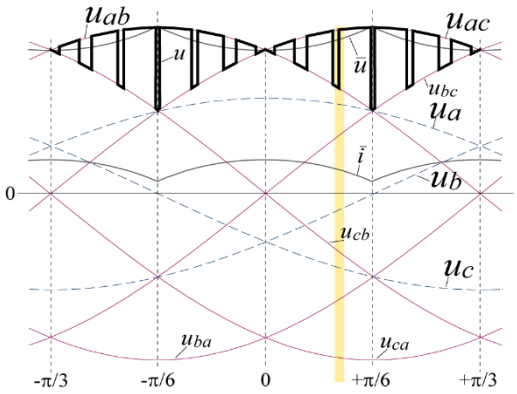
Commutation
of Matrix Converter

- **Commutation Strategy for Sparse MC: Zero DC Link Current Comm. (HV)**

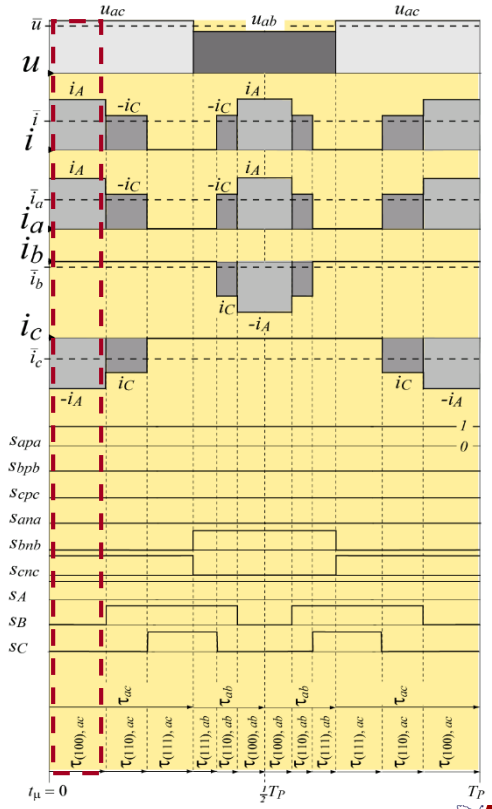


$u = u_{ac}$

$i = i_A$



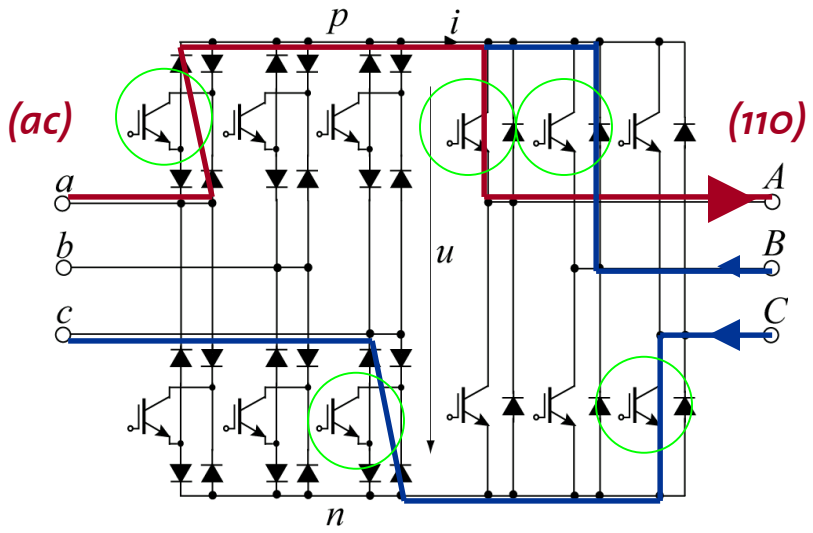
1/3 Mains Period



Pulse Period

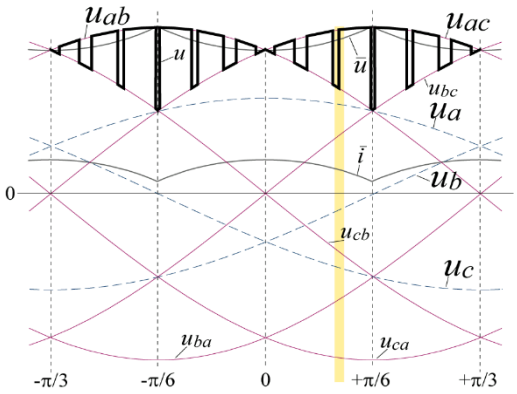
Commutation
of Matrix Converter

- **Commutation Strategy for Sparse MC: Zero DC Link Current Comm. (HV)**

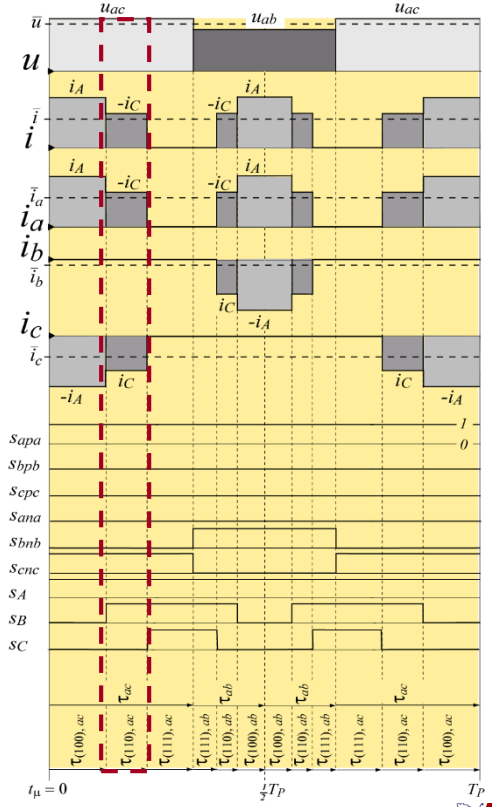


$u = u_{ac}$

$i = -i_C$



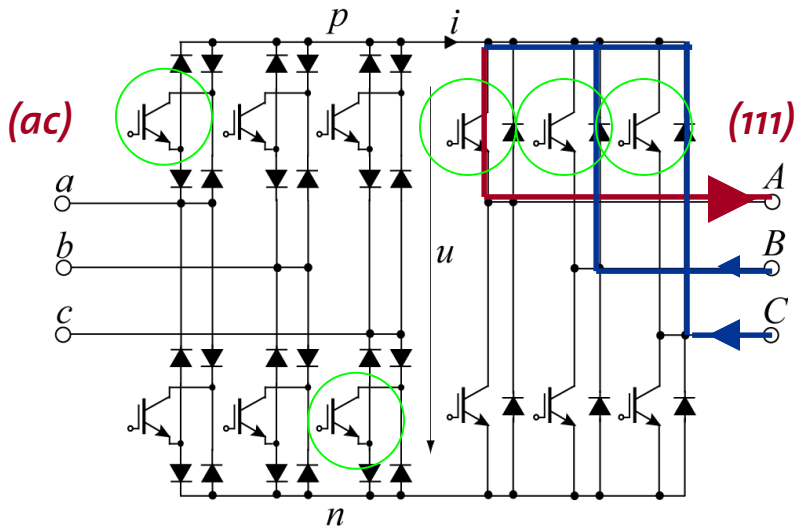
1/3 Mains Period



Pulse Period

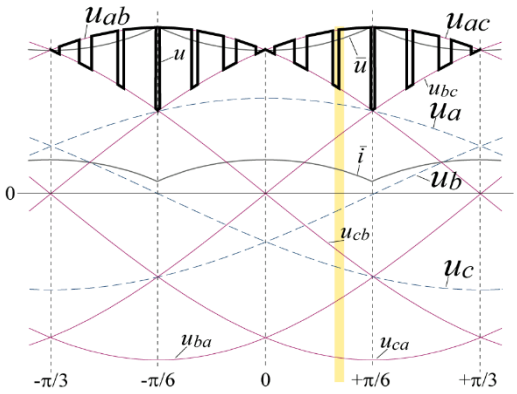
Commutation
of Matrix Converter

- **Commutation Strategy for Sparse MC: Zero DC Link Current Comm. (HV)**

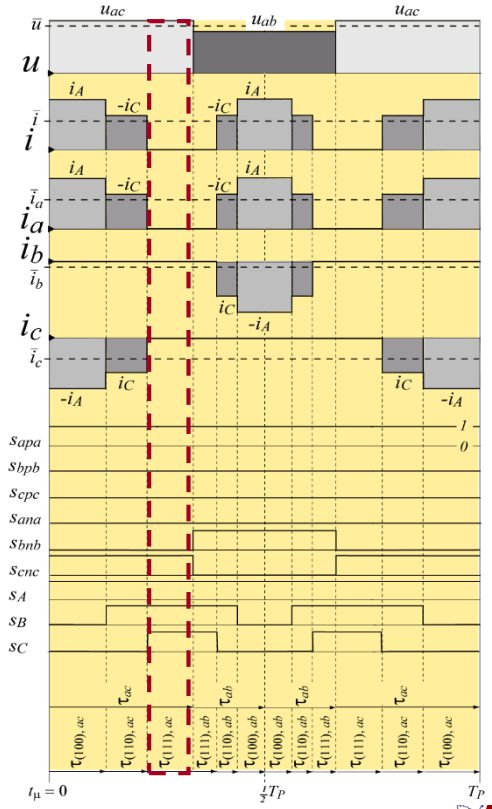


$u = u_{ac}$

$i = 0$



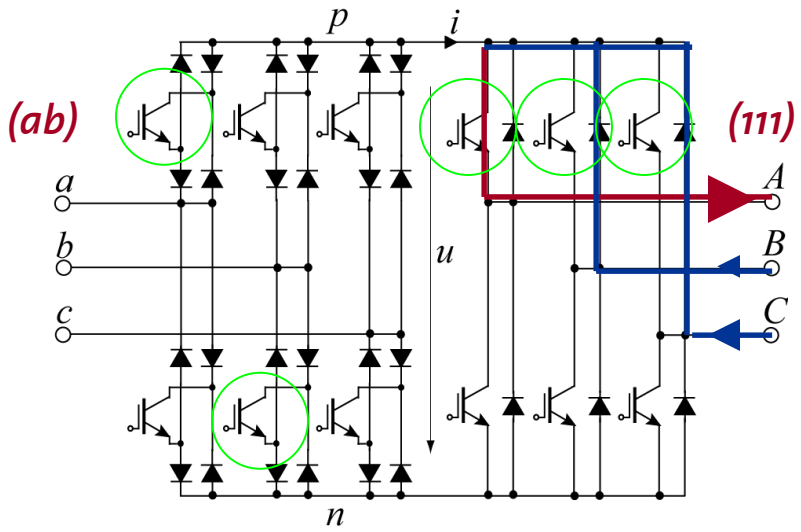
1/3 Mains Period



Pulse Period

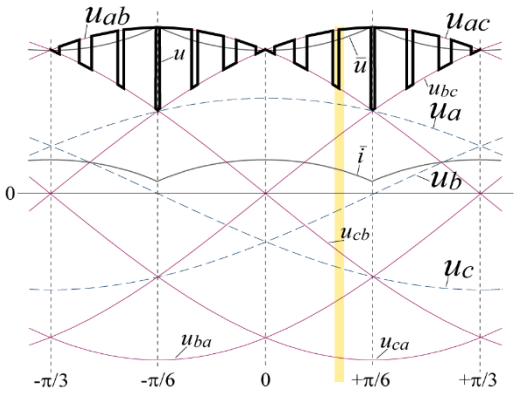
Commutation
of Matrix Converter

- **Commutation Strategy for Sparse MC: Zero DC Link Current Comm. (HV)**

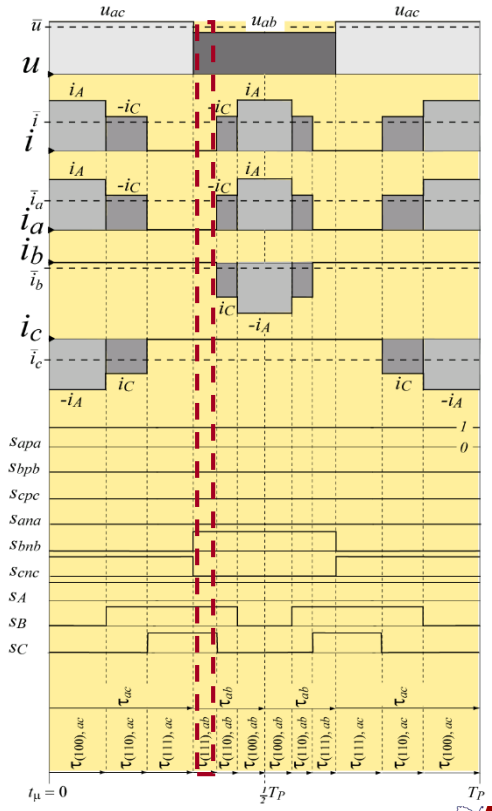


$u = u_{ab}$

$i = o$



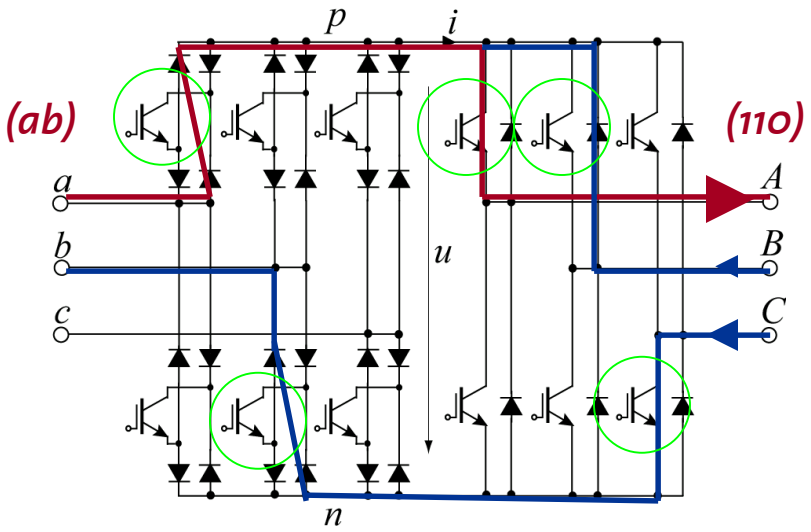
1/3 Mains Period



Pulse Period

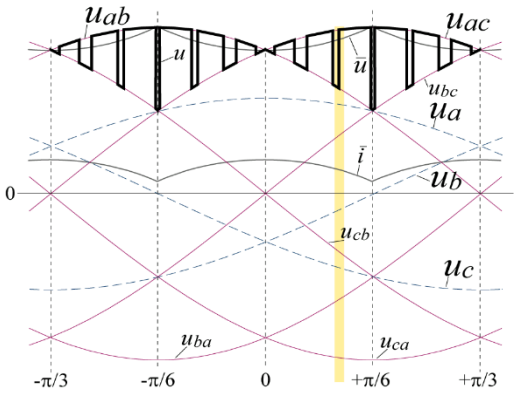
Commutation of Matrix Converter

Commutation Strategy for Sparse MC: Zero DC Link Current Comm. (HV)

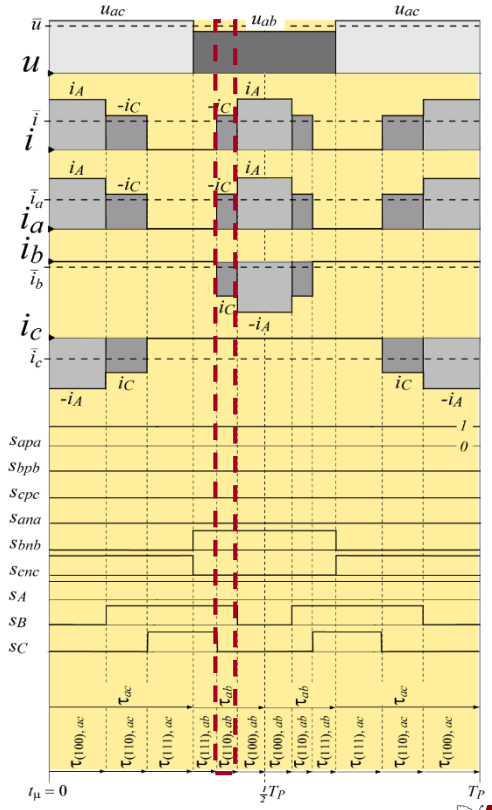


$u = u_{ab}$

$i = -i_C$



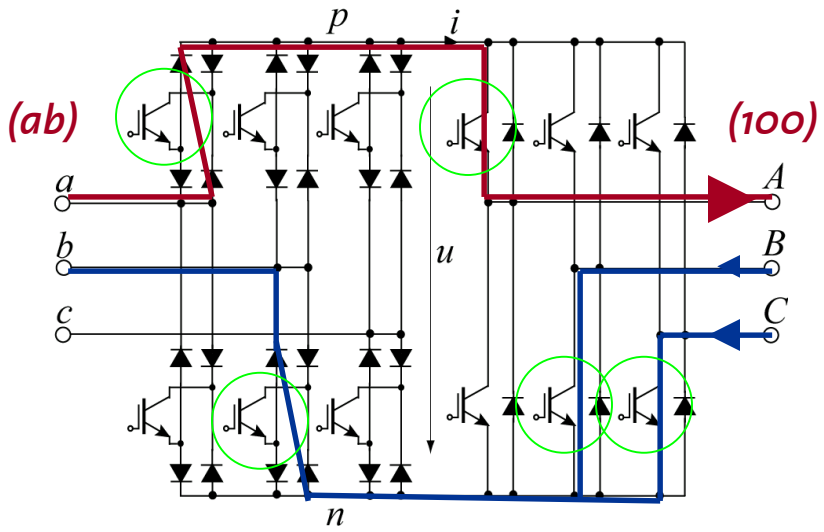
1/3 Mains Period



Pulse Period

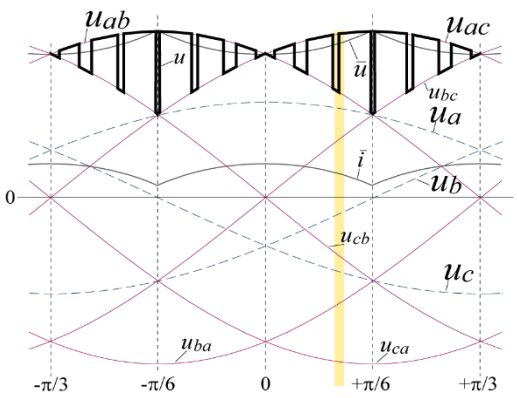
Commutation
of Matrix Converter

- **Commutation Strategy for Sparse MC: Zero DC Link Current Comm. (HV)**

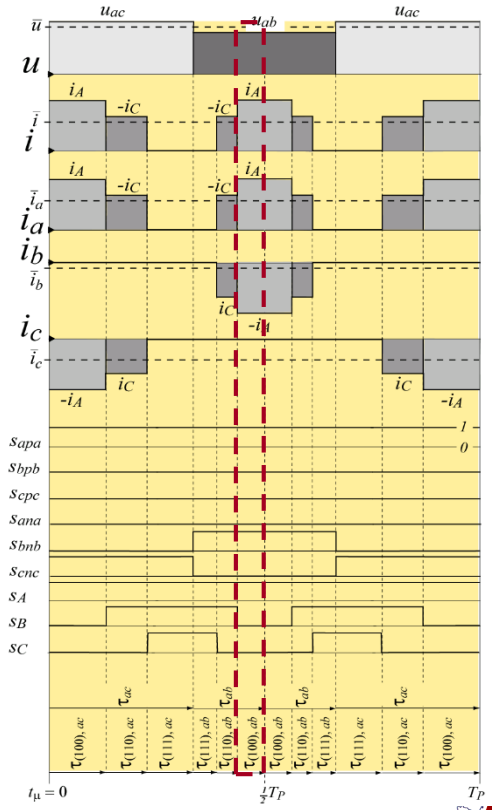


$u = u_{ab}$

$i = i_A$



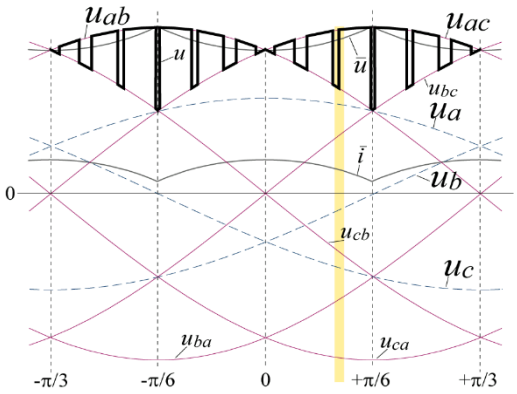
1/3 Mains Period



Pulse Period

Commutation
of Matrix Converter

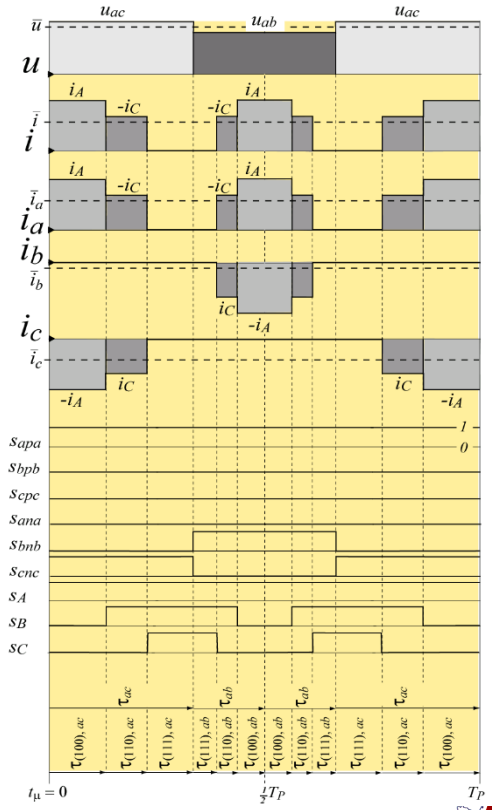
- **Commutation Strategy for Sparse MC: Zero DC Link Current Comm. (HV)**



1/3 Mains Period

- **Simple & Robust**
  because
  Independent of
  (Measured) Current/Voltage Sign

- **Minimum Output Stg.**
  Free-Wheeling Interval has to be ensured



Pulse Period

Modified Modulation Schemes

Why modifying the Conventional (HV) Modulation Scheme ?

- Reduce Converter Losses & Widen System Operating Range (3 Schemes)

  (Reduce Losses → Reduce Switching Losses)

- Extend the Basic Functionality of the MC-System (2 Schemes)

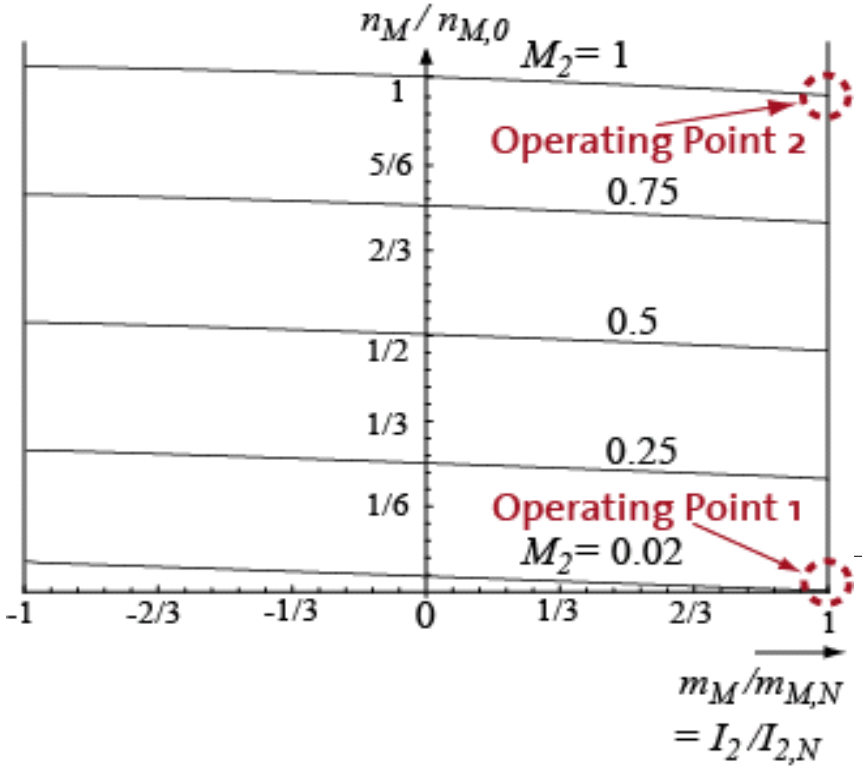
- Reduce Input Current Harmonics (not treated here)

Note: Every Modulation Scheme has Advantages & Disadvantages

→ Reasonable Usage depends on Operating Condition

Basic Consideration
for Drive Application

- Example:
  Steady State **Torque-Speed Characteristic** of a PMSM:



- **Operating Point 1:**
  Nominal Load Torque $m_M = m_{M,N}$,
  Speed Near Zero $n_M \approx 0$
  Outp. Phase Displ. $\Phi_2 \approx 0$

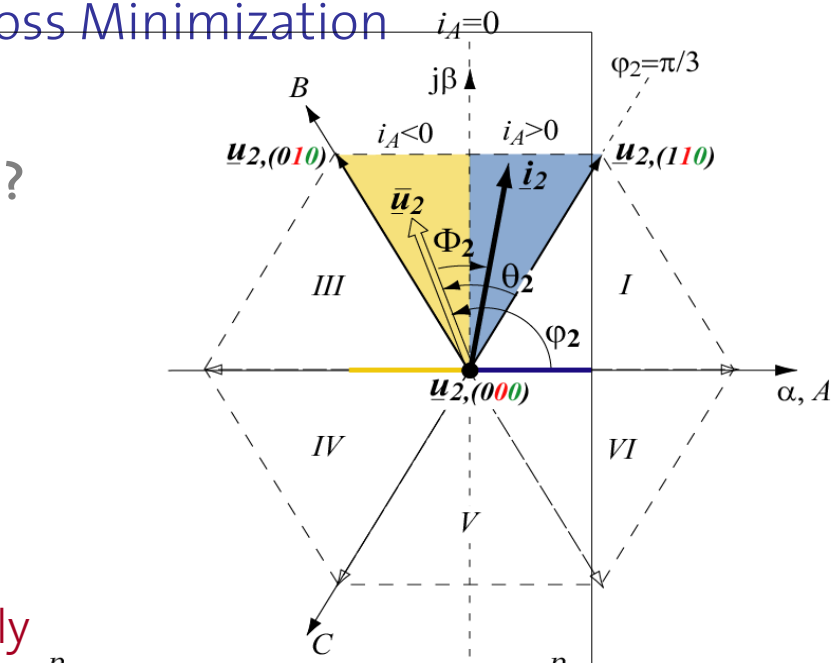
- **Operating Point 2:**
  Nominal Load Torque $m_M = m_{M,N}$,
  Speed Near Zero $n_M \approx n_{M,0}$
  Outp. Phase Displ. $\Phi_2 < 10°$

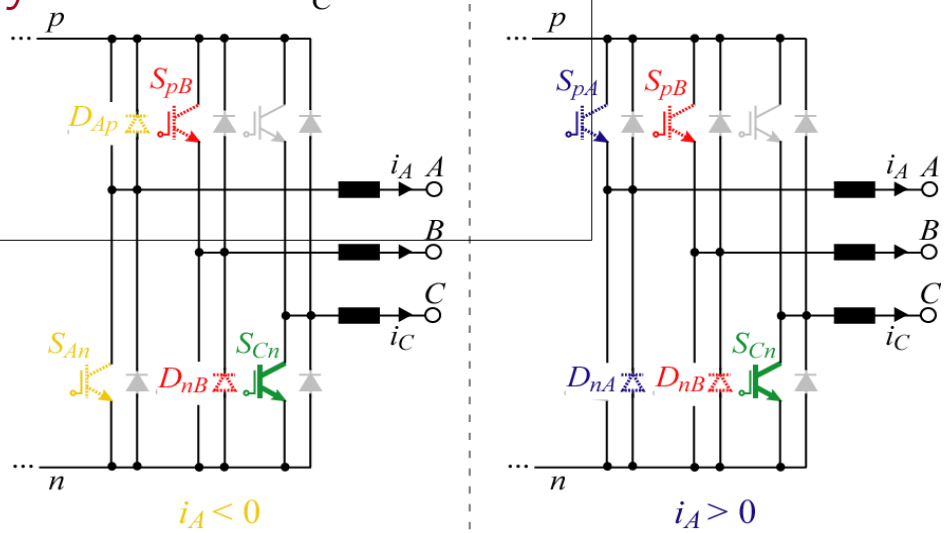
Here:
- Also Focus on **OP1**

Basic Consideration
for SMC Loss Minimization

Where do Switching Losses Occur ?

- For **Conventional Modulation:**
  - ➡ Sw. Losses of Rectifier Stage neglactable
  - ➡ Sw. Losses in Inverter Stage Only

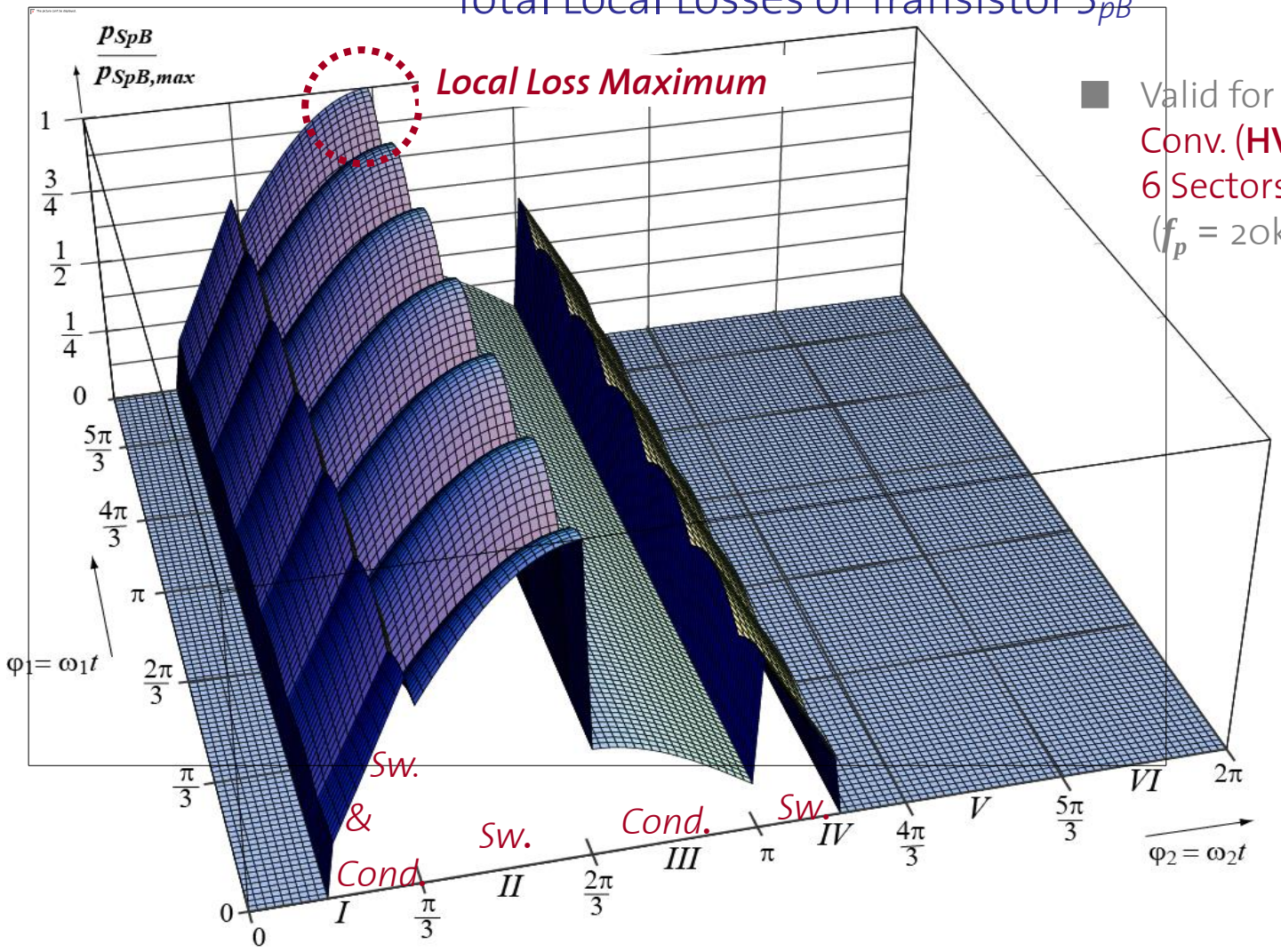




- Positions of $\bar{u}_2$ and i_2 Determine the **Semiconductors** being Subject to Power Losses

3D – Characteristic, SMC

Total Local Losses of Transistor S_{pB}



- Valid for Conv. (**HV**) Modulat., 6 Sectors @ OP1 (f_p = 20kHz)

- A **Whole Input- & Output Period** Combination is Represented (φ_1=0...2π, φ_2=0...2π)

3D - Characteristic
Practical Interpretation

Two Values of Loss Characteristic are Relevant:

- Because of Thermal Time Constant τ_{th}:
  Global Average Value Determines the Max. Load Current for **Normal** Output Frequencies (**OP2**) & Total Converter Efficiency

- **Local Maximum** Value is Determining the Max. Load Current for **Very Low** Output Frequencies (**OP1**)

Aim: 1. Reduce Global Average ➲ Flatten Characteristic

2. Reduce Local Maximum ➲ Equalize sector specific Levels

Outline of Presentation

Matrix Modulation Schemes

- Conventional Multi-Step Commutation
- Zero DC Link Current Commutation (for SMC / IMC)

- **Optimized Output Stg. Clamping** **(1st Measure)**

- High Output Voltage (HV)
- Low Output Voltage (LV) (2nd Measure)

- Switching Loss Shifting (for SMC / IMC) (3rd Measure)

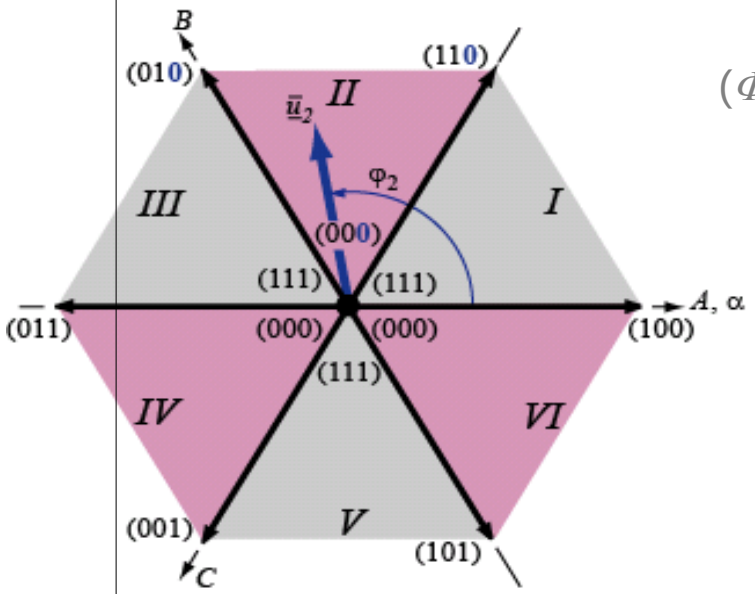
- Reactive Power Coupling

1st Measure:
Optimize Output Stage Clamping

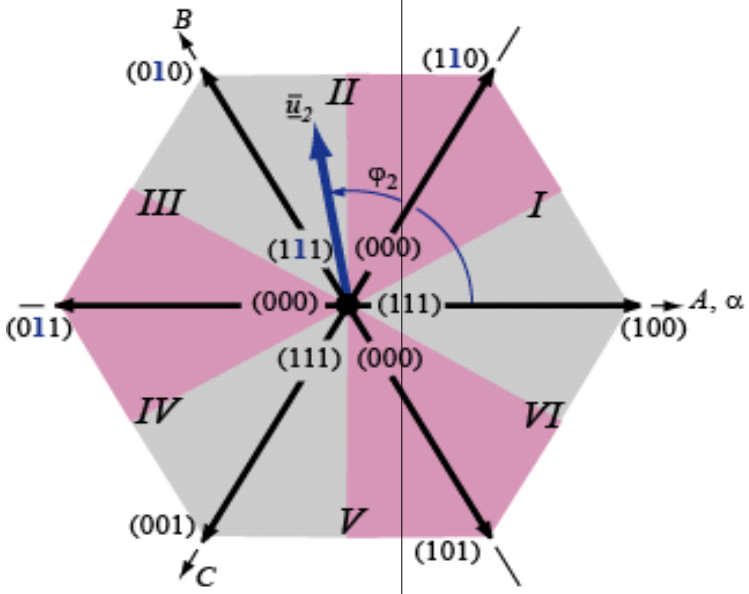
- 6 **Sector** Modulat.

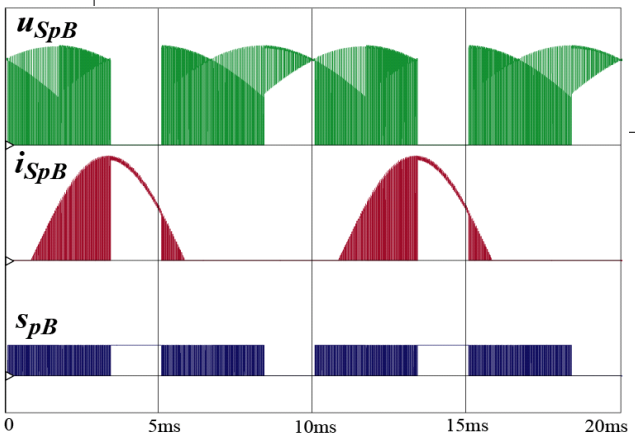
OP 1

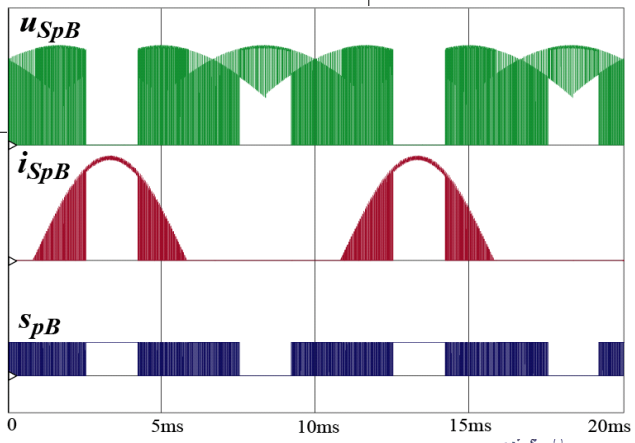
$(\Phi_2 = 0)$



- **12 Sector** Modulat.

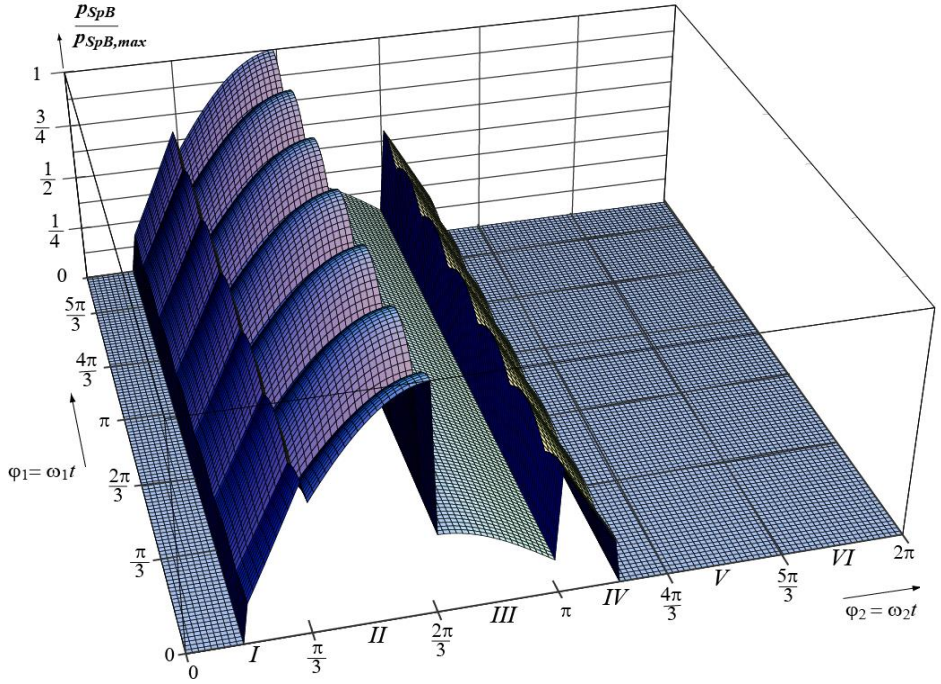






Effect of...

Optim. Output Stage Clamping

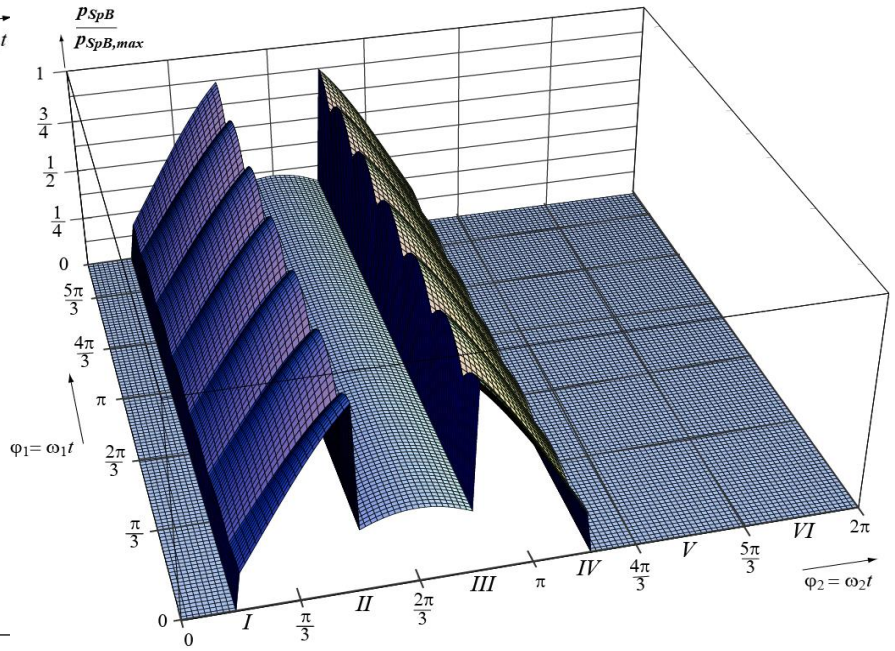


- **6 Sector** Modulat.

OP 1

$(\Phi_2 = 0)$

- **12 Sector** Modulat.



2nd Measure:

Reduce DC Link Voltage

by Modifying **Rectifier Stage Modulation**

Basic Idea: Formation of DC Link Voltage ($\boldsymbol{u}$) from the Two Small Positive Line-Line Input Voltages

Effect: Inverter Stage Modulation does Not Change, but Voltage being Switched by Inverter's Semiconductors ($\boldsymbol{u}$) Reduces Significantly

→ Sw. Losses are Reduced Significantly

→ Max. Output Voltage is Reduced → Low Voltage (**LV**) Modulation

Requirements:
Rect. Stage Modulat.

- Positive DC Link Voltage ($\boldsymbol{u}$)
- Sinusoidal Input Current ($\underline{\boldsymbol{i}}_{\boldsymbol{a,b,c}}$ resp. $\underline{\boldsymbol{i}}_{\boldsymbol{1}}$)

Outline of Presentation

Matrix Modulation Schemes

- Conventional Multi-Step Commutation
- Zero DC Link Current Commutation (for SMC / IMC)

- Optimized Output Stg. Clamping (1st Measure)

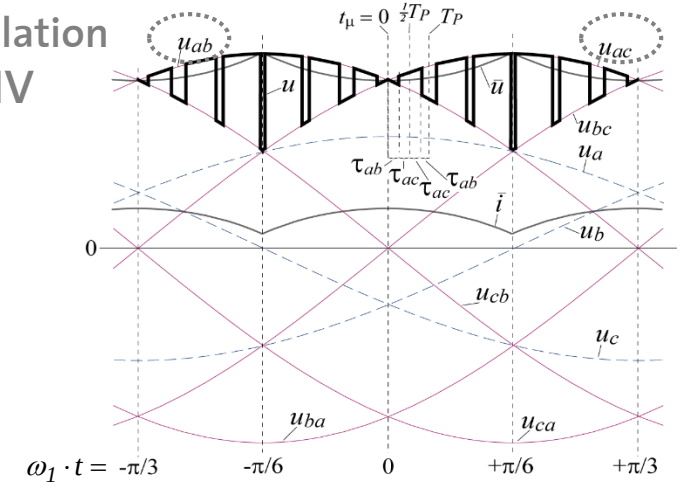
- **High Output Voltage (HV)**
- **Low Output Voltage (LV)** **(2nd Measure)**

- Switching Loss Shifting (for SMC / IMC) (3rd Measure)

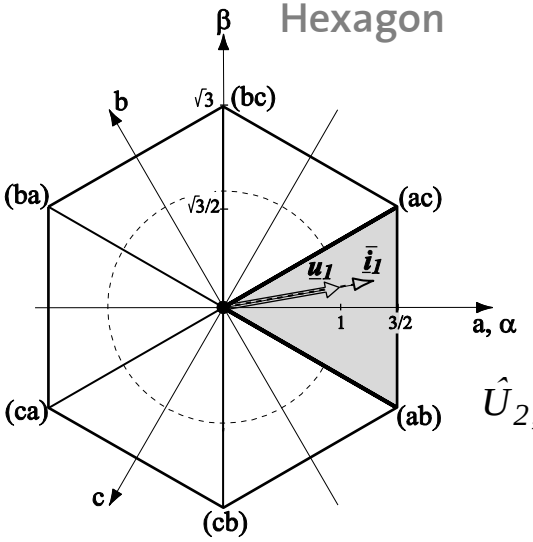
- Reactive Power Coupling

Conventional vs. Low Voltage Modulation:
Basic Principle

- Conventional Modulation HV

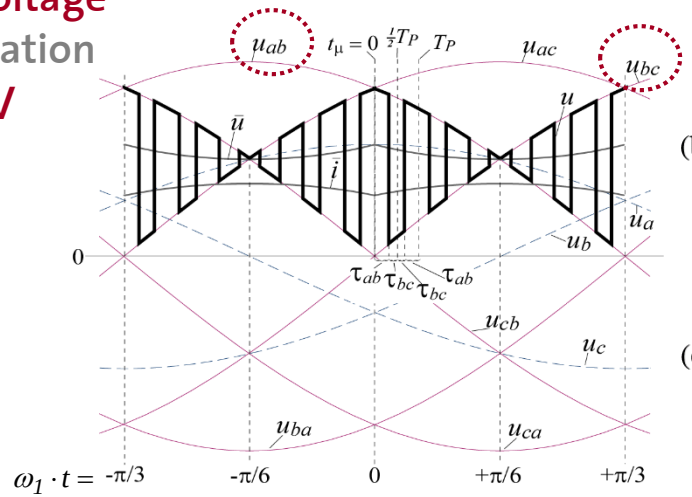


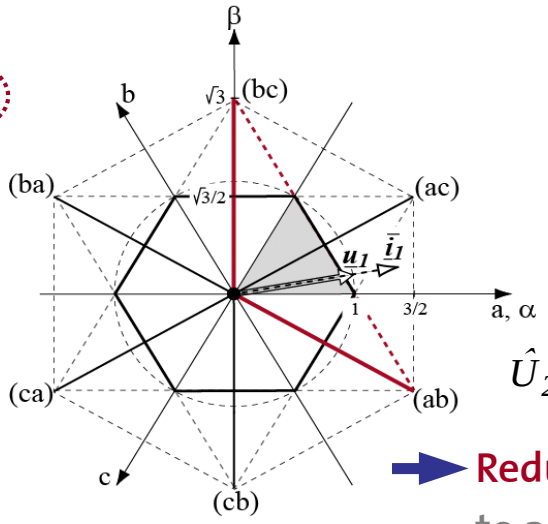
Rectifier Hexagon



$$\hat{U}_{2,max,I} = \frac{\sqrt{3}}{2}\hat{U}_1 \approx 0.86 \cdot \hat{U}_1$$

- Low Voltage Modulation LV





$$\hat{U}_{2,max,II} = \frac{1}{2}\hat{U}_1 = 0.5 \cdot \hat{U}_1$$

→ **Reduction of Sw. Losses** to approx. **60%**

Analytic Equations:
Turn-On-Times & DC Link Volt.

Considering:

$$\bar{i}_a = d_{ab}\,\bar{i}$$
$$\bar{i}_b = (d_{bc} - d_{ab})\,\bar{i}$$
$$\bar{i}_c = -d_{bc}\,\bar{i}$$

and:

$$d_{ab} + d_{bc} = 1$$

$$\bar{i}_a \sim u_a$$
$$\bar{i}_b \sim u_b \qquad (\phi_1 = 0)$$
$$\bar{i}_c \sim u_c$$

Turn-on-Times:

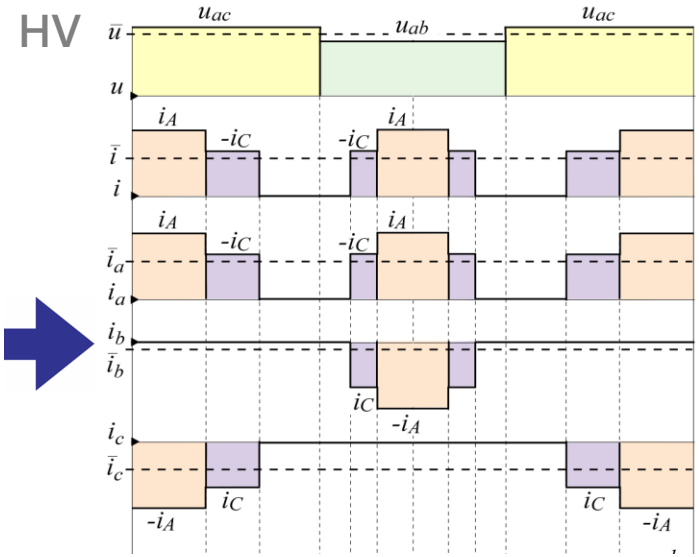
$$\tau_{(100),ab} = \frac{T_p}{\sqrt{3}} \frac{\hat{U}_2}{\hat{U}_1^{\,2}} u_a \cos(\varphi_2 + \tfrac{\pi}{6})$$
$$\tau_{(110),ab} = \frac{T_p}{\sqrt{3}} \frac{\hat{U}_2}{\hat{U}_1^{\,2}} u_a \sin(\varphi_2)$$
$$\tau_{(110),bc} = \frac{T_p}{\sqrt{3}} \frac{\hat{U}_2}{\hat{U}_1^{\,2}} (-u_c) \sin(\varphi_2)$$
$$\tau_{(100),bc} = \frac{T_p}{\sqrt{3}} \frac{\hat{U}_2}{\hat{U}_1^{\,2}} (-u_c) \cos(\varphi_2 + \tfrac{\pi}{6})$$

DC Link Voltage (Local Average):

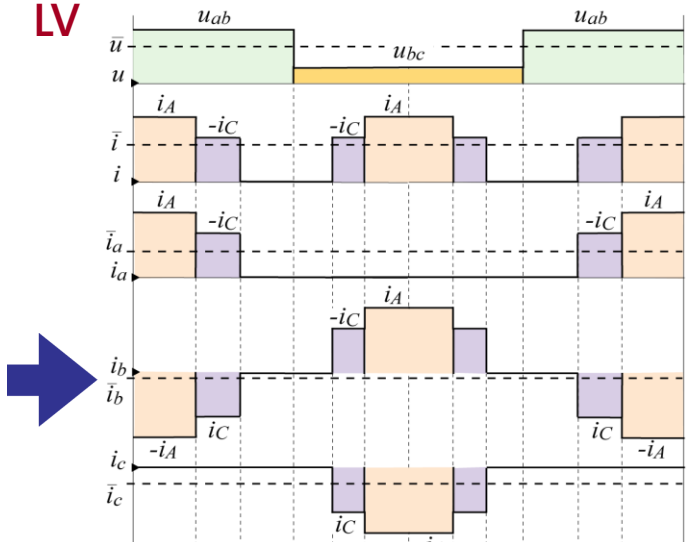
$$\bar{u} = \frac{\sqrt{3}}{2} \hat{U}_1 \frac{1}{\cos(\omega_1 t - \frac{\pi}{6})}$$

Conventional vs. Low Voltage Modulation:
Characteristic Quantities during a Pulse Period

HV



LV



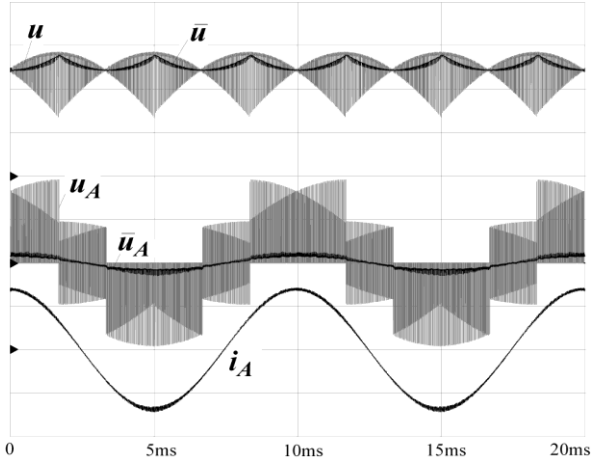
- One Input Phase (*a*) is Clamped to one DC Link Bus Bar (*p*)
- Other Input Phases (*b*,*c*) are Switched to the remaining DC Link Bus Bar (*n*)

- **No** Input Phase is **Clamped** to any DC Link Bus Bar
- **One** Input Phase (*b*) is **Switched** between pos.(*p*) **and** neg.(*n*) Bus Bar

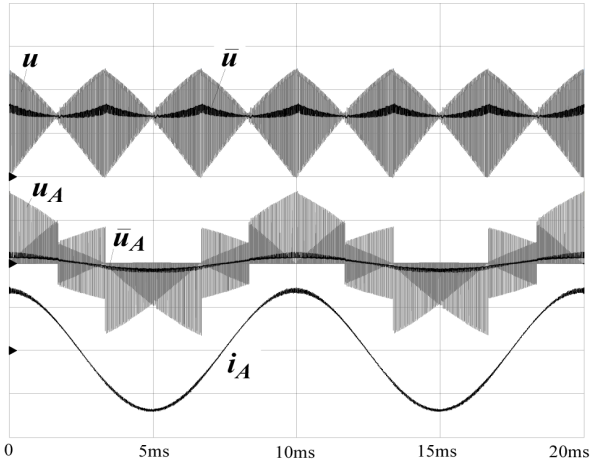
➲ **Current Blocks of Both Polarities appear in One Input Phase (*b*)**

Simulation, HV vs. LV:
Characteristic Quantities

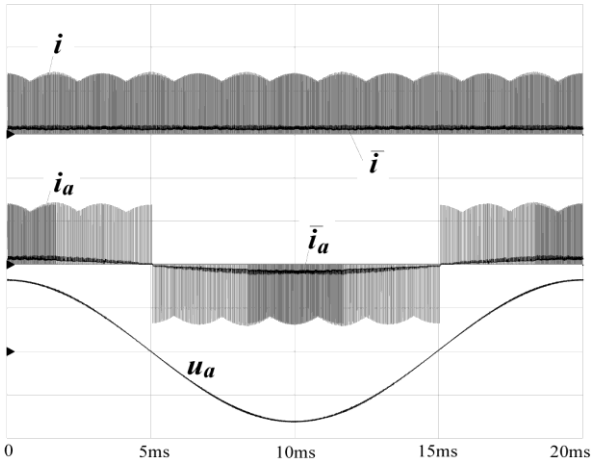
HV



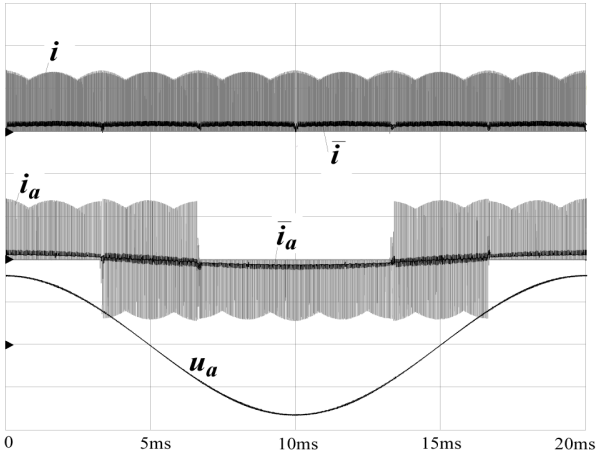
LV



- **Output Voltage Formation**



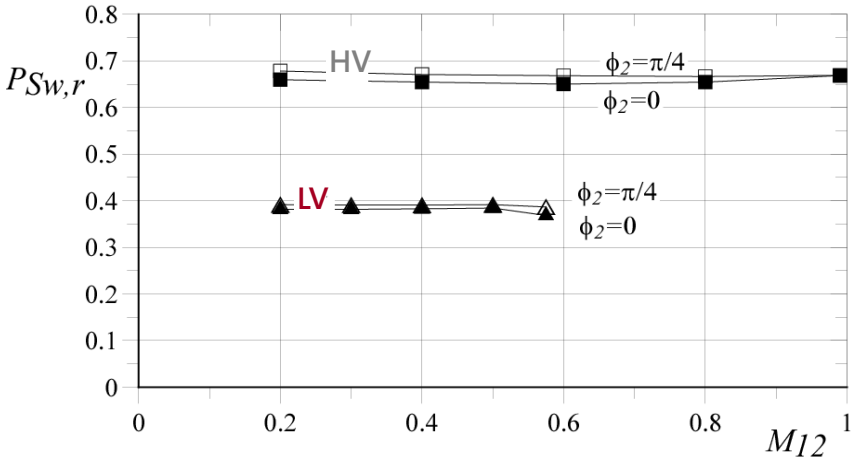
- **Input Current Formation**



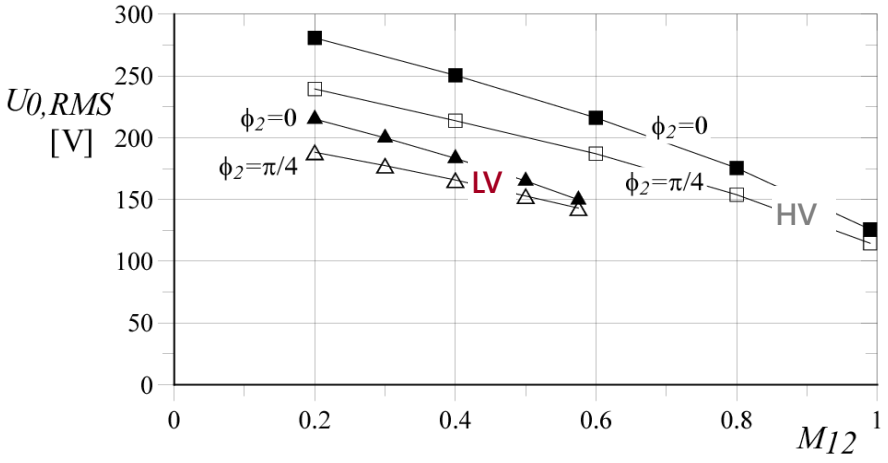
Parameters:
- f_1 = 50Hz
- f_2 = 100Hz
- f_P = 20kHz
- L = 1mH
- C = 9µF

Simulation Results, HV vs. LV:
Sw. Losses, Common Mode Volt.

Switching Losses



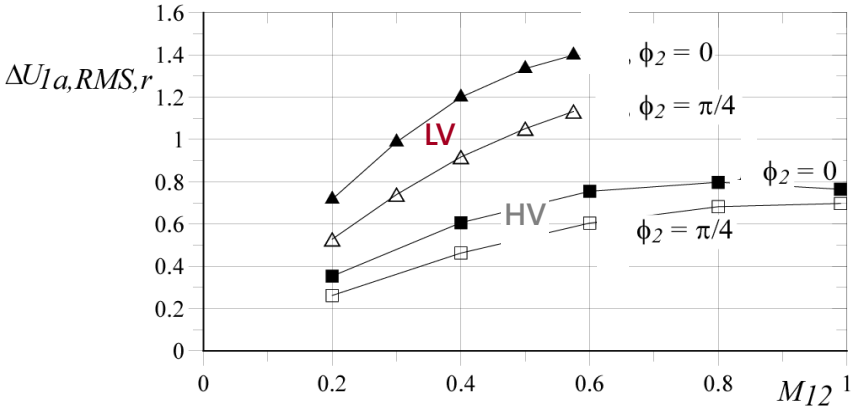
Output Common Mode Voltage



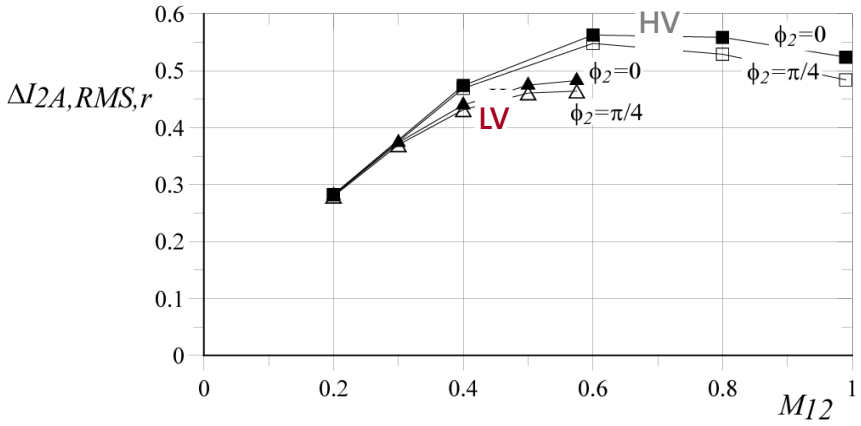
- **Switching Losses are reduced to ≈ 58%**
- **Common Mode Voltage is reduced to ≈ 75%**

Simulation Results, HV vs. LV:

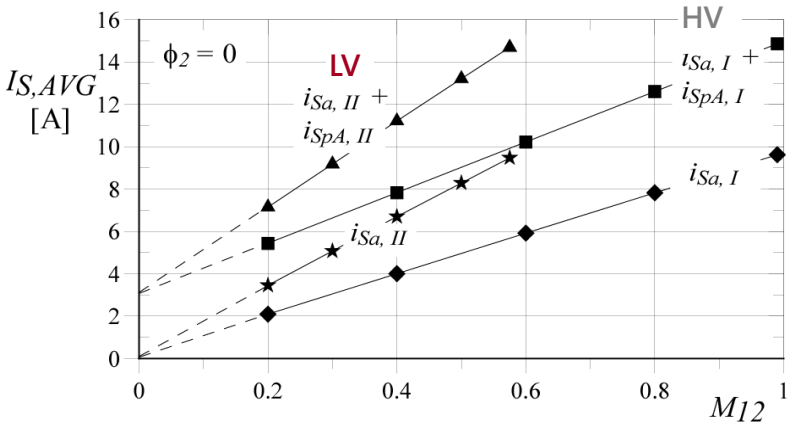
Input Voltage Ripple



Output Current Ripple



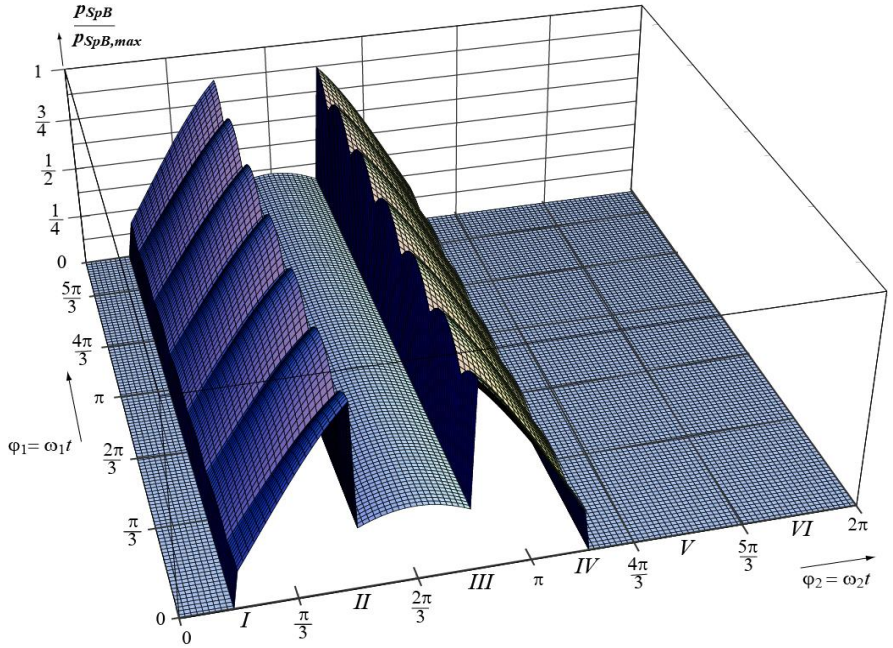
Current Stress



- **Input Voltage Ripple Doubles**
- Output Current Ripple slightly Reduced
- For a given $\hat{U}_2$ (M_{12}) the Component Current Stress Increases (Conduction Losses)

Effect of…

LV – Modulation

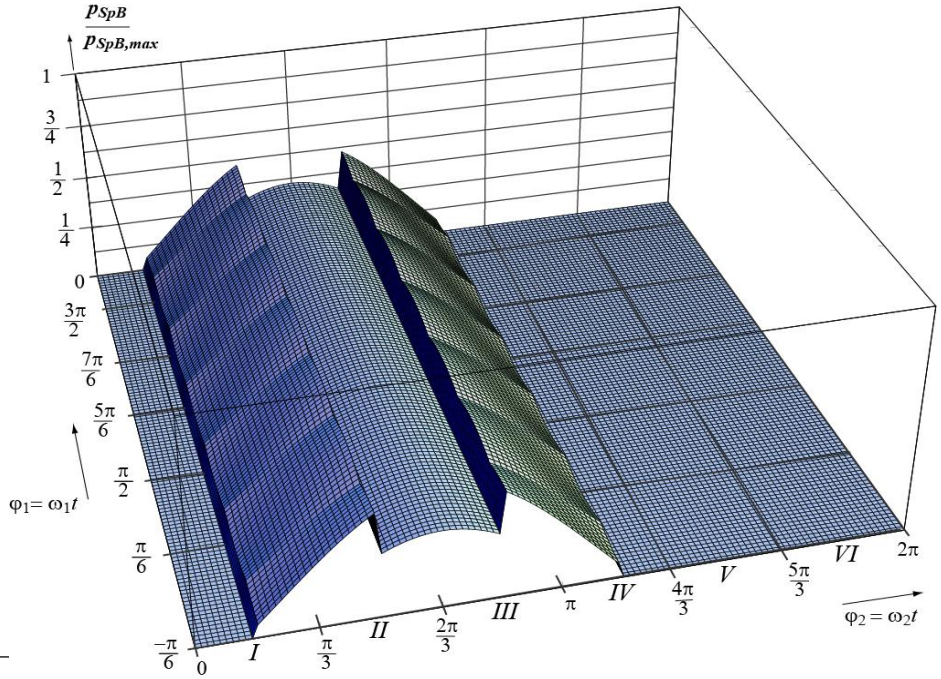


12 Sector, **HV** Modulat.

12 Sector, **LV** Modulat.

+ $P_{Sw,LV} \approx 0.58 \cdot P_{Sw,HV}$
− $\hat{U}_{2,max} = ½\ \hat{U}_1$
− $\Delta U_{1a,LV} \approx 2 \cdot \Delta U_{1a,HV}$

➲ **Higher Output Current** (Torque) at **Low Output Frequency** (Speed)



OP 1

$(\Phi_2 = 0)$

Outline of Presentation

Matrix Modulation Schemes

- Conventional Multi-Step Commutation
- Zero DC Link Current Commutation (for SMC / IMC)

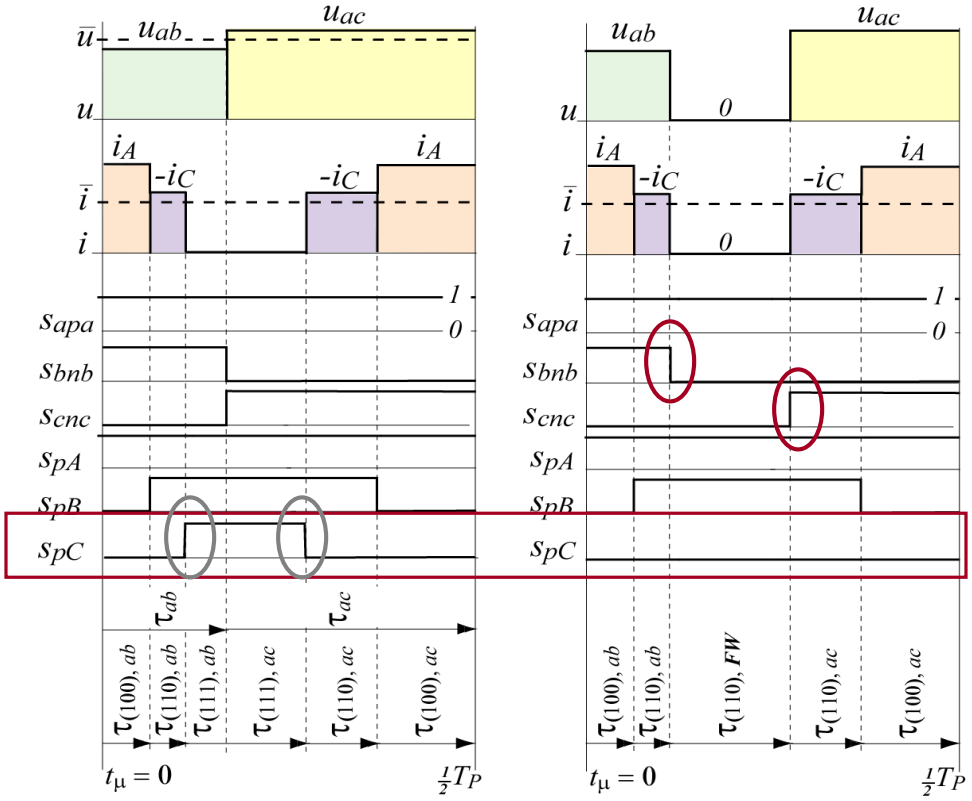
- Optimized Output Stg. Clamping (1st Measure)

- High Output Voltage (HV)
- Low Output Voltage (LV) (2nd Measure)

- **Switching Loss Shifting (for SMC / IMC) (3rd Measure)**

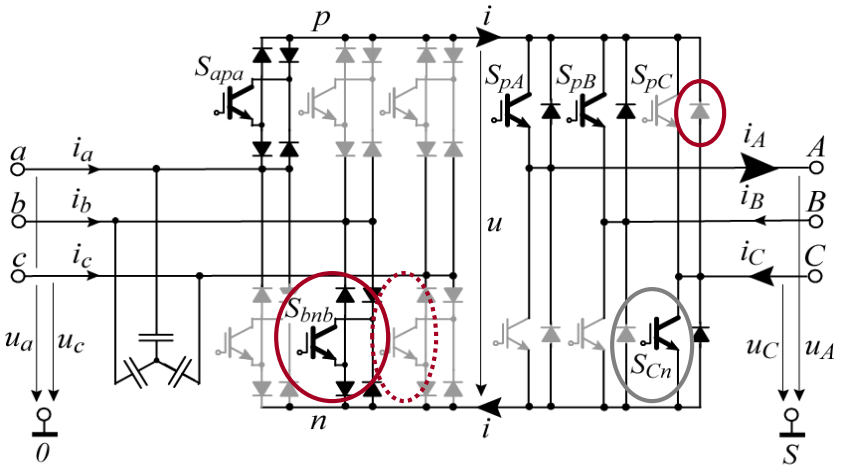
- Reactive Power Coupling

3rd Measure:
Shift Sw. Losses to Rectifier Stage & Split



■ Conventional Modulation
HV
(LV)

■ **Sw.Loss Shift** Modulation
HV, **SLS**
(LV, **SLS**)



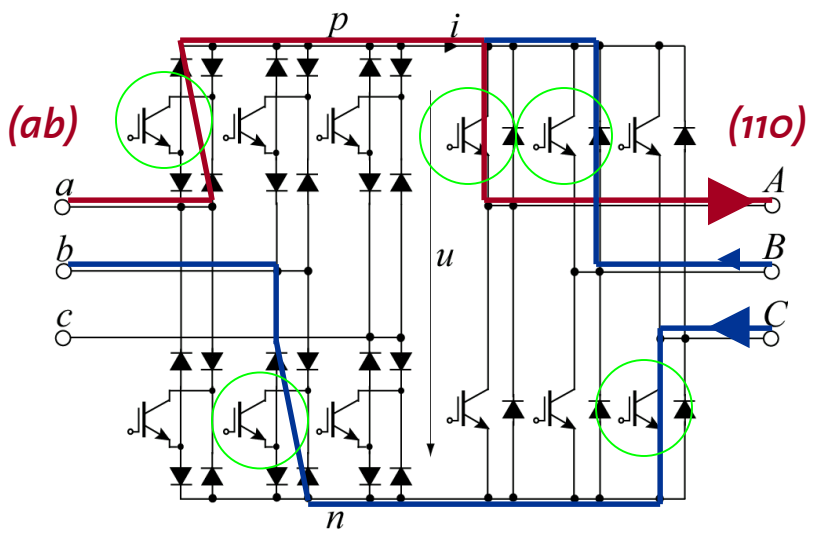
***i* > 0 :**

▶ Sw. Losses of **Most Stressed** Inverter IGBT (S_{Cn}) are **Split** to **Two** Rectifier IGBTs (S_{bnb}, S_{cnc})

➲ For Low Output Frequency (Speed):
S_{Cn} is **Not** the **Bottle-Neck** IGBT anymore

➲ **Higher Output Current (Torque) achievable**

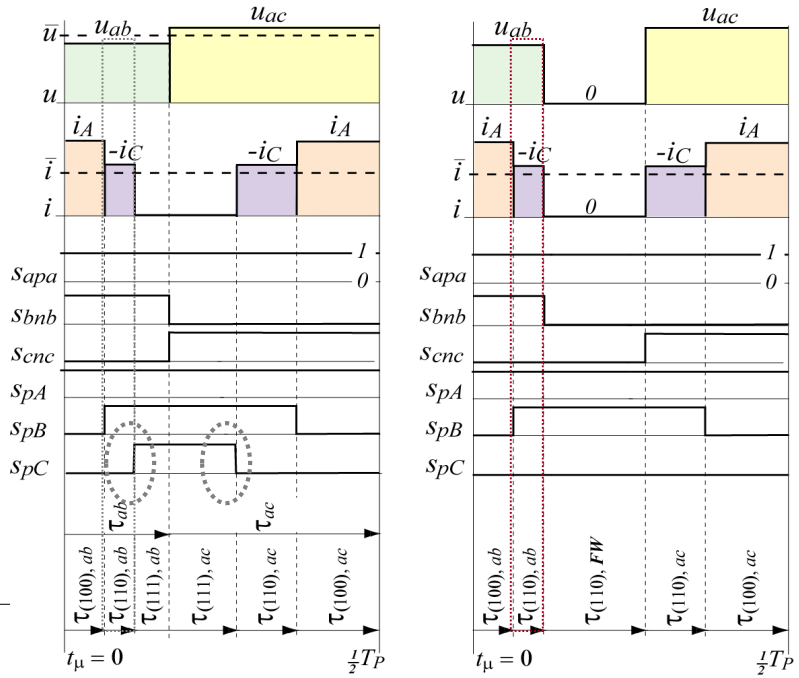
3rd Measure:
Shift Sw. Losses to Rectifier Stage & Split



$u = u_{ab}$

$i = - i_C$

- Conventional Modulation
- Sw.Loss Shift Modulation

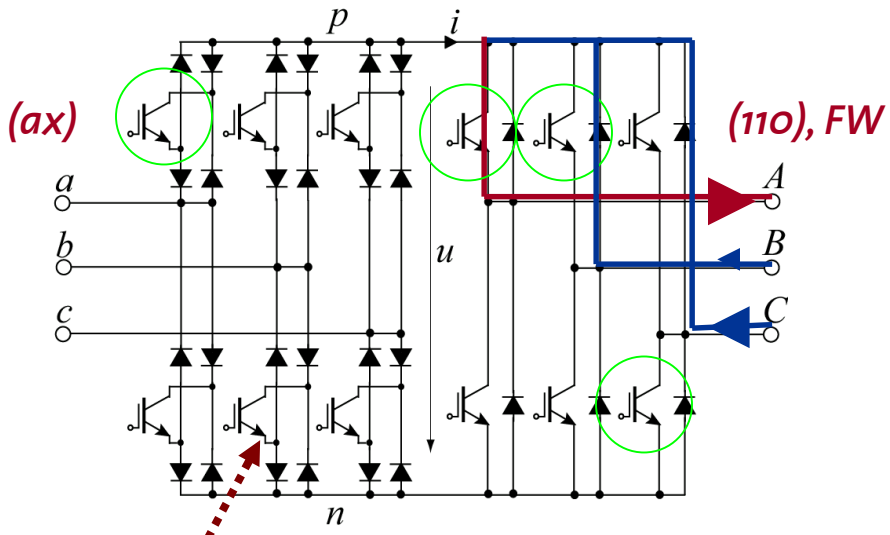


- Shift Part of Sw. Losses to Input Stage
- Split Losses from One Output IGBT to Two Input IGBT

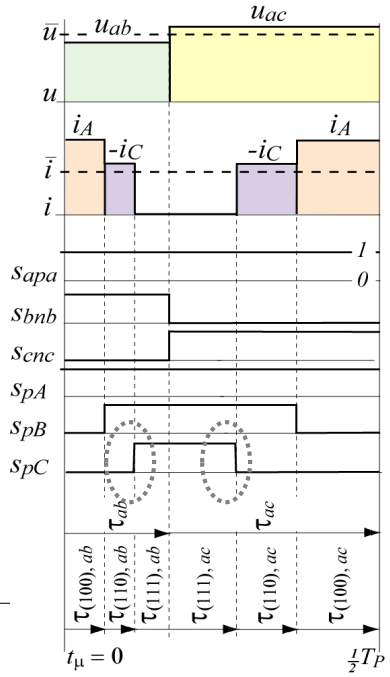
→ More Equal Loss/Temperature Distribution

→ Higher Output Current (Torque) @ Very Low Speed

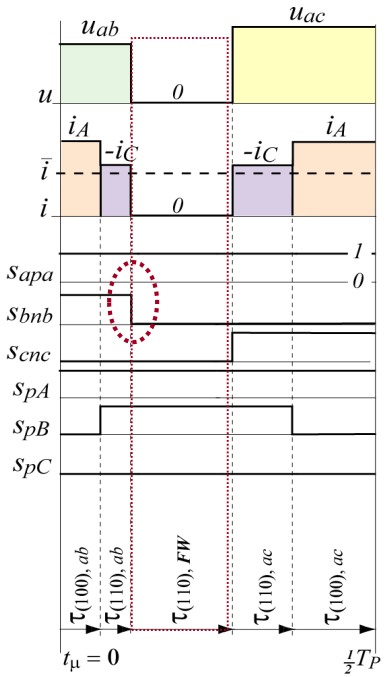
3rd Measure:
Shift Sw. Losses to Rectifier Stage & Split



■ Conventional Modulation



■ Sw.Loss Shift Modulation



- Shift Part of Sw. Losses to Input Stage
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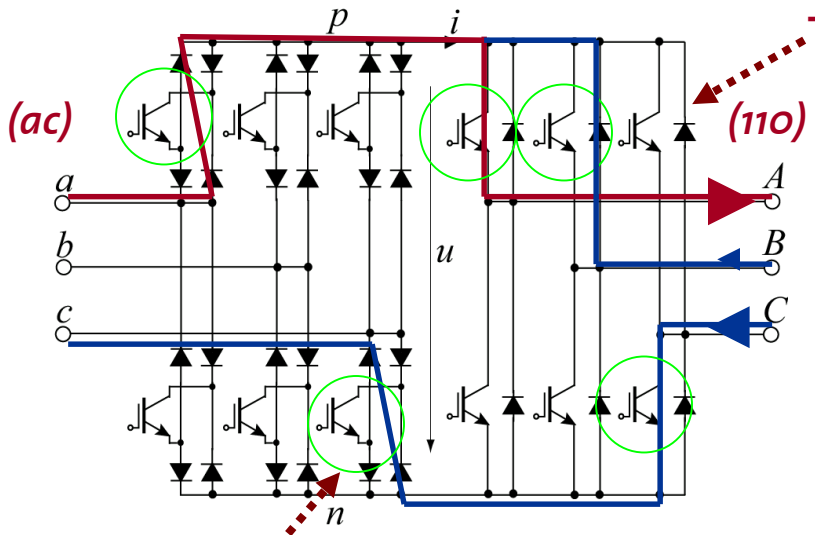
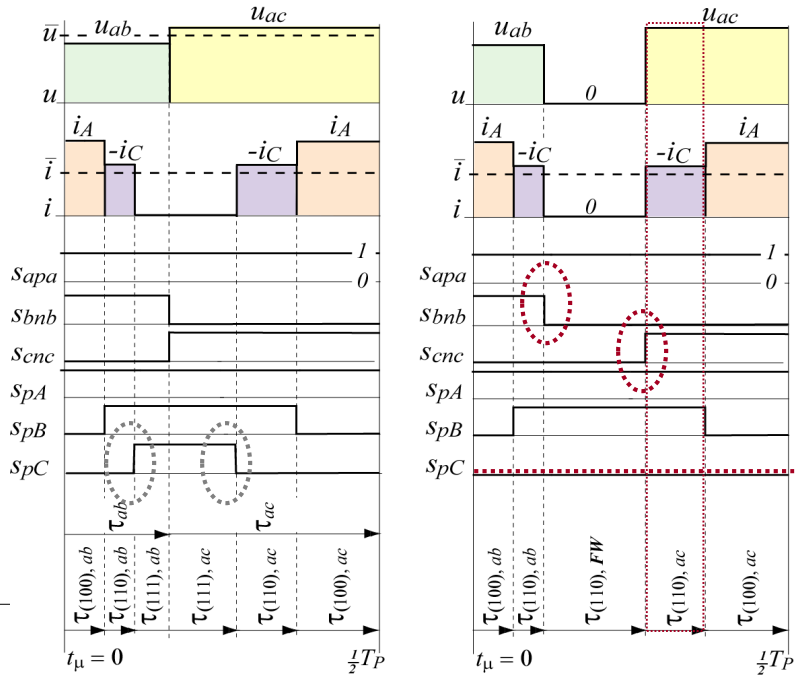
3rd Measure:

Shift Sw. Losses to Rectifier Stage & Split



- Conventional Modulation
- Sw.Loss Shift Modulation



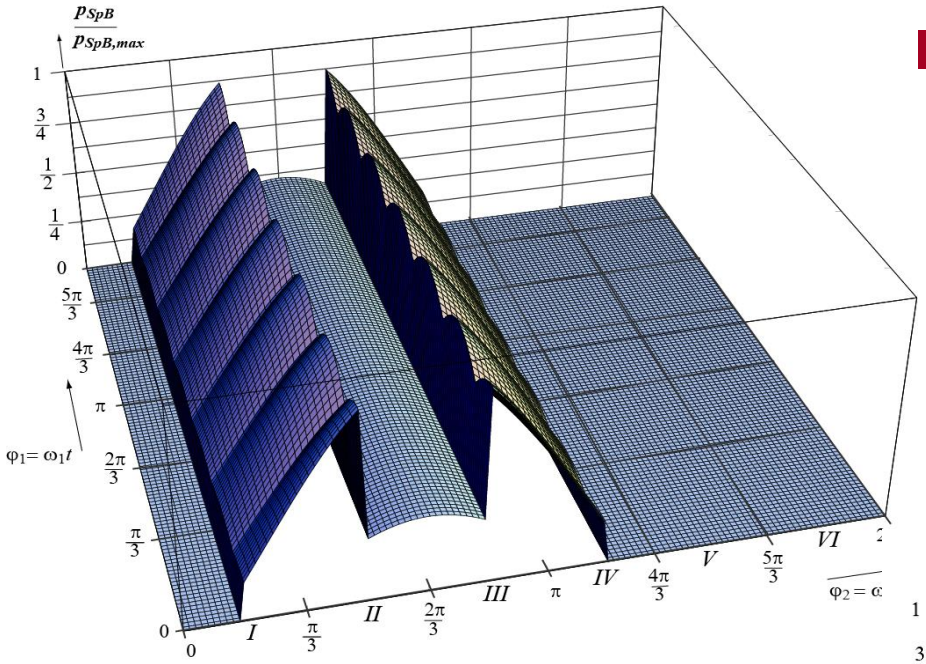
- ▶ **Shift** Part of **Sw. Losses to Input Stage**
- ▶ **Split Losses** from **One** Output IGBT to **Two** Input **IGBT**

→ **More Equal Loss/Temperature Distribution**

→ **Higher Output Current (Torque) @ Very Low Speed**

Effect of...

Sw. Loss Shifting, HV - Modulation

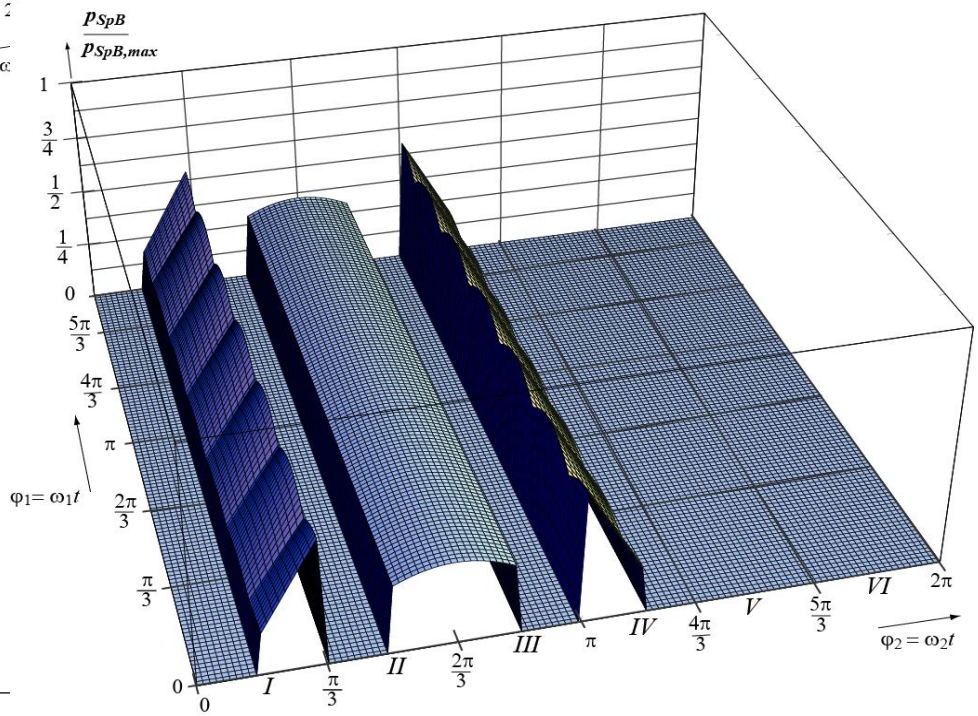


12 Sect, **HV** Modulat.

OP 1

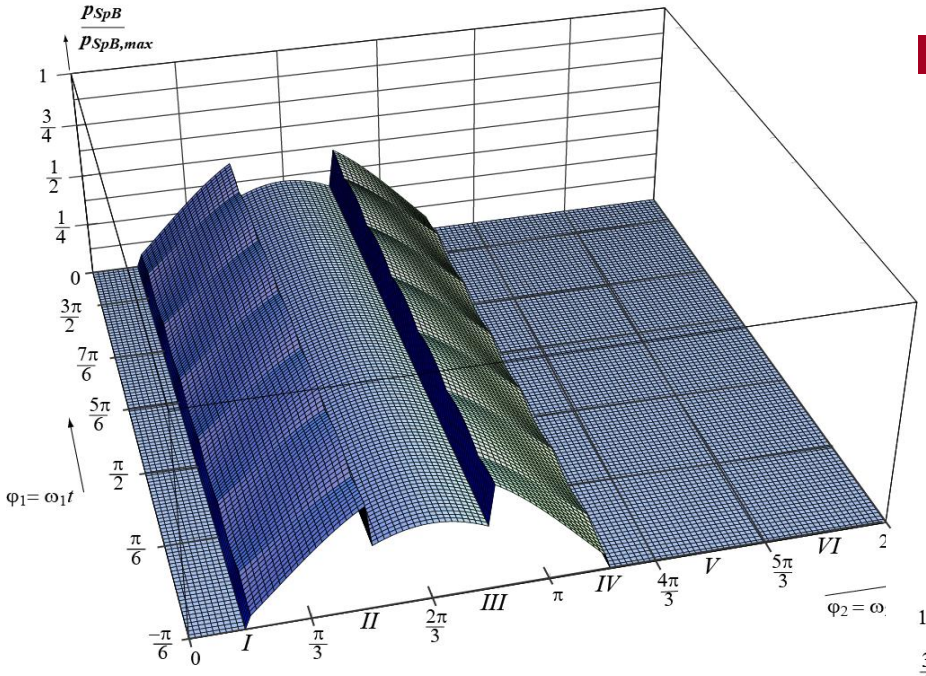
$(\Phi_2 = 0)$

- 12 Sect, HV, **SLS** Modulat.
  - System Overall Efficiency Stays Constant
  - **Works for $i > 0$ Only**
    - $-\pi/6 < \phi_2 < \pi/6$: **Regular** Outp. Clamp.
    - $-\pi < \phi_2 < \pi$: Special Outp. Clamp.
  - **Condition has to be Checked** in Modulat. Algorithm



Effect of...

Sw. Loss Shifting, LV - Modulation

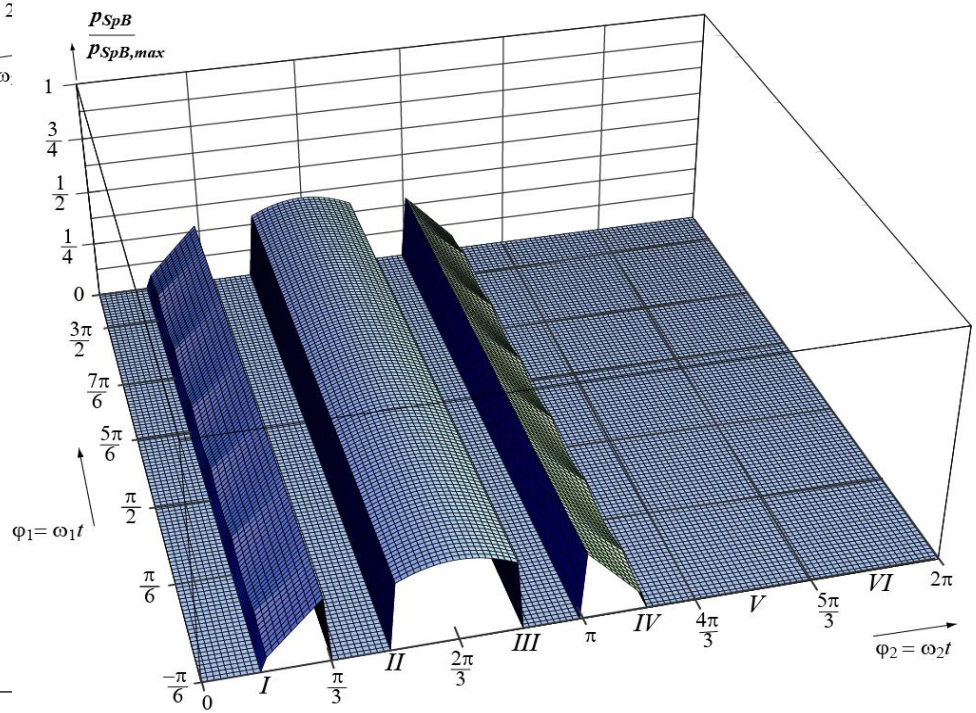


12 Sect, **LV** Modulat.

12 Sect, LV, **SLS** Modulat.

- System Overall Efficiency Stays Constant
- **Works for $i > 0$ Only**
  - $-\pi/6 < \phi_2 < \pi/6$: **Regular** Outp. Clamp.
  - $-\pi < \phi_2 < \pi$: Special Outp. Clamp.

➲ **Condition has to be Checked** in Modulat. Algorithm



OP 1

$(\Phi_2 = 0)$

Outline of Presentation

Matrix Modulation Schemes

- Conventional Multi-Step Commutation
- Zero DC Link Current Commutation (for SMC / IMC)

- Optimized Output Stg. Clamping (1st Measure)

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- Low Output Voltage (LV) (2nd Measure)

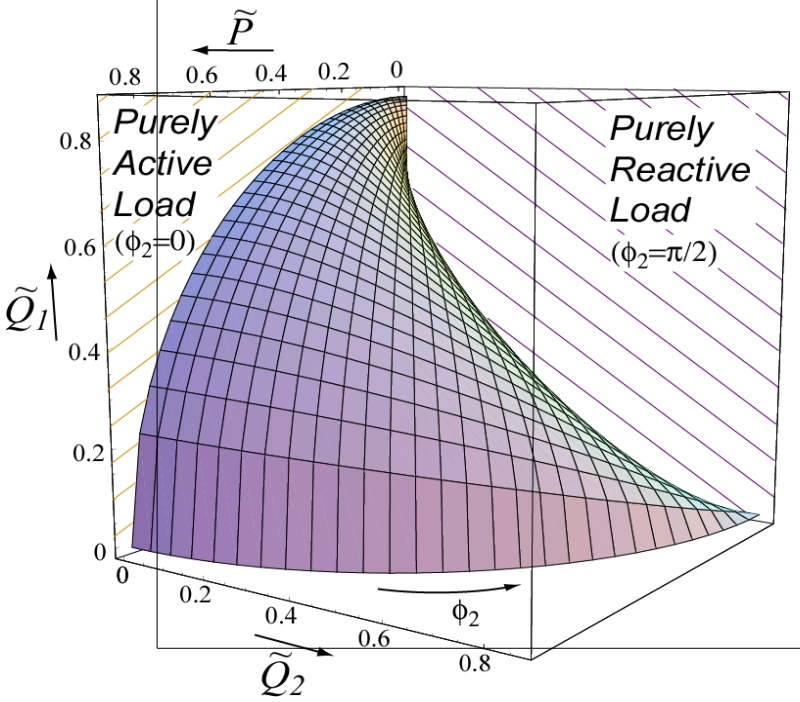
- Switching Loss Shifting (for SMC / IMC) (3rd Measure)

- **Reactive Power Coupling**

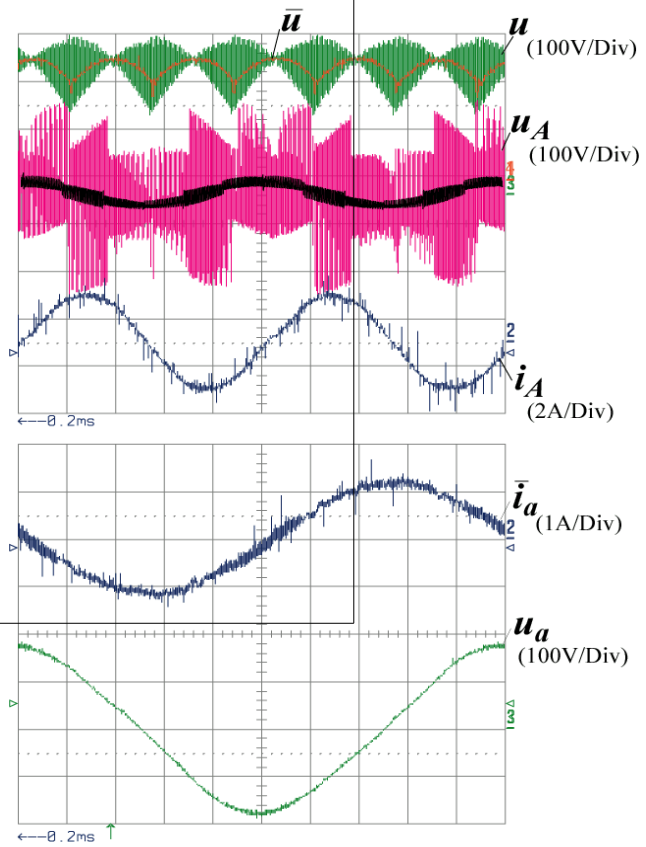
Extending the Conventional MC-Functionality

Input & Output Reactive Power Coupling

- State of the Art



- Novel Results



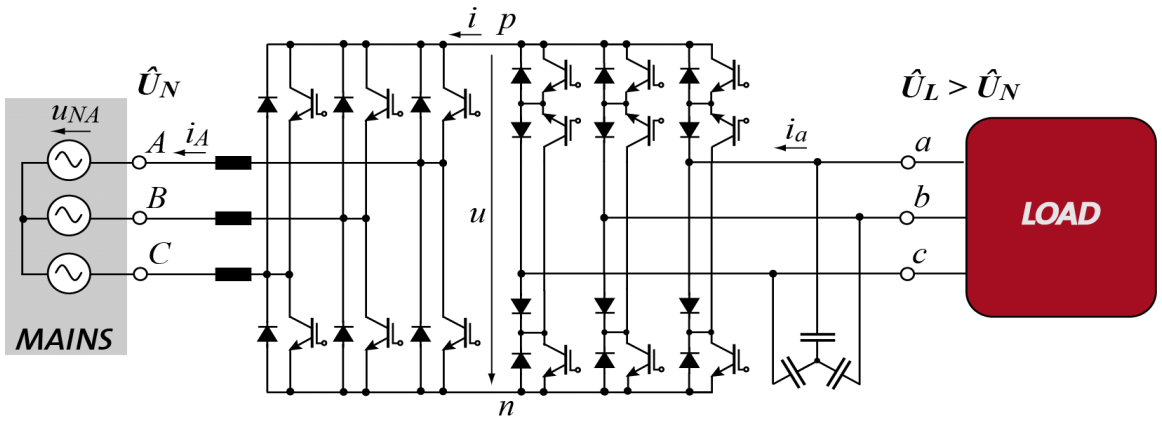
Max.Control Range of **"Conventional"**
(Virtual) DC-link/Indirect Modulation

Extending the Conventional MC-Functionality
Input & Output Reactive Power Coupling

Possible **Applications** of this **Novel Modulation**

- **Compensating Capacitive Mains Currents ($\phi_1 = -\pi$)** drawn by the Input Filter **Even while Driving** Induction Motor with **Zero Load Torque ($\phi_2 = \pi$)**
- Facilitating for Arbitrary ϕ_2 a certain Amount of **Reactive Input Power at Maximum Output Voltage (M_{12}=1)**

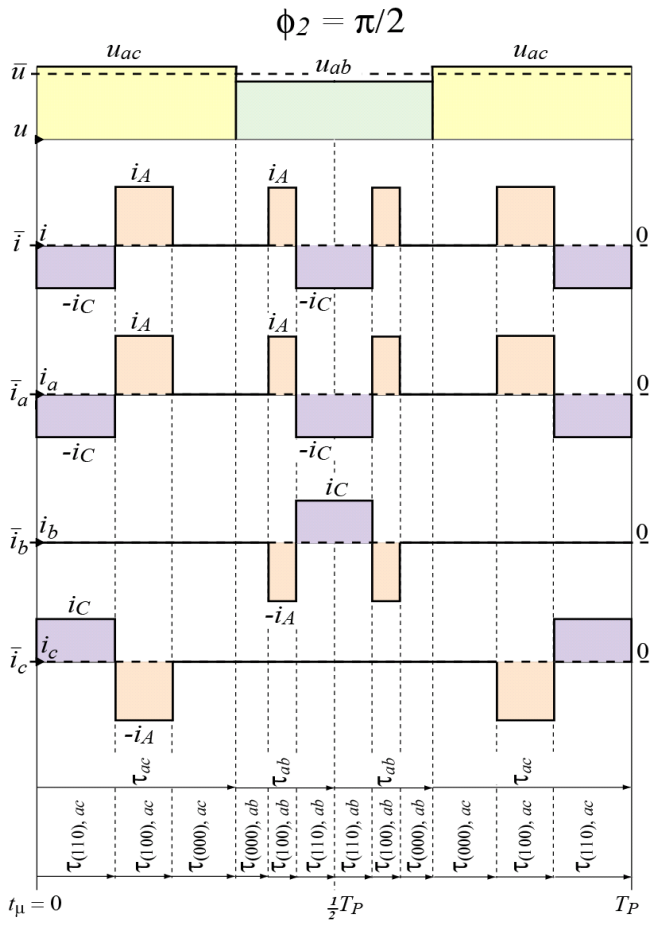
- **Precondition** (No Load Case) for Operating **MC-System in Boost Mode**

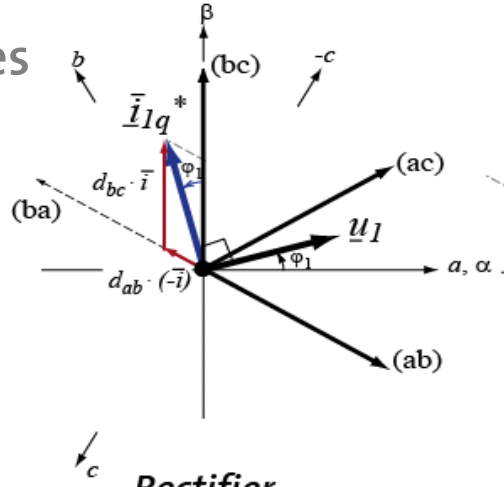


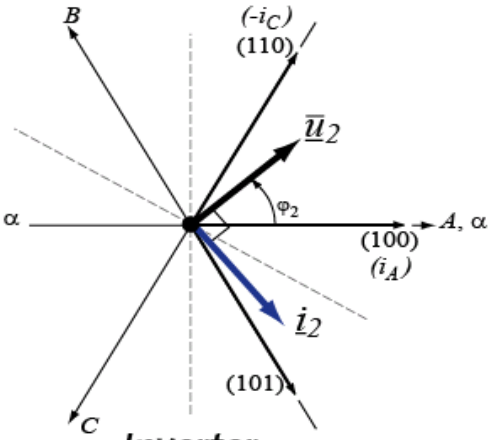
Conventional Modulation Schemes

Operating with Reactive Power

Dilemma for Conventional Schemes







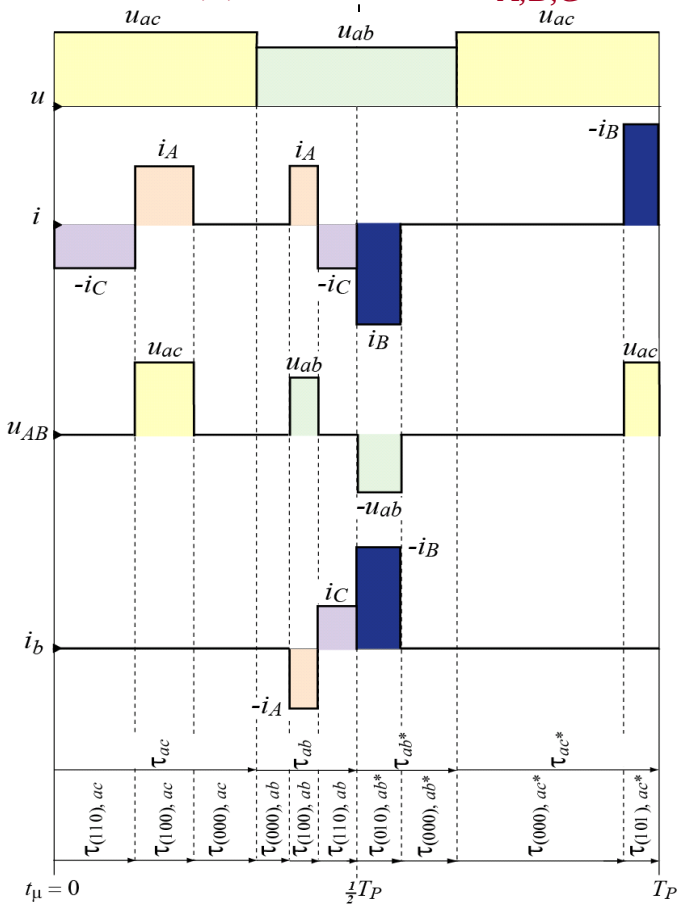
- $\phi_2 = \pm\pi/2$ ➲ No Local Average for i: $(\bar{i} = 0)$
  - ➲ $\hat{I}_1 = 0$
  - ➲ $P_2 = 0$ ➡ $S_1 = 0$
- $\phi_1 = \pm\pi/2$ ➲ No Local Average for u: $(\bar{u} = 0)$
  - ➲ $\hat{U}_2 = 0$
  - ➲ $P_1 = 0$ ➡ $S_2 = 0$

➡ No Reactive Power Transfer/Coupling Possible

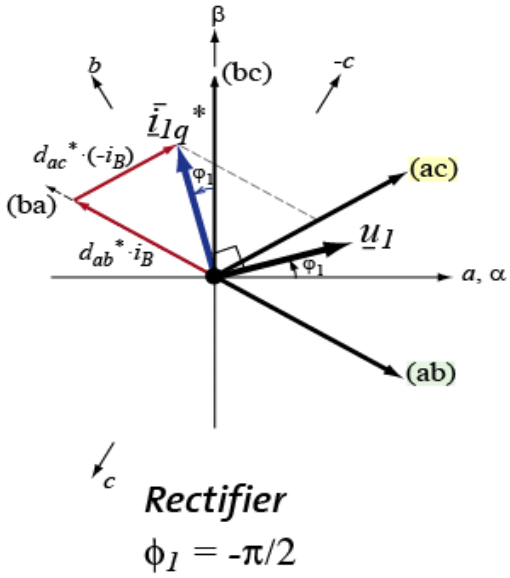
Reactive Power Coupling I (RPCI)

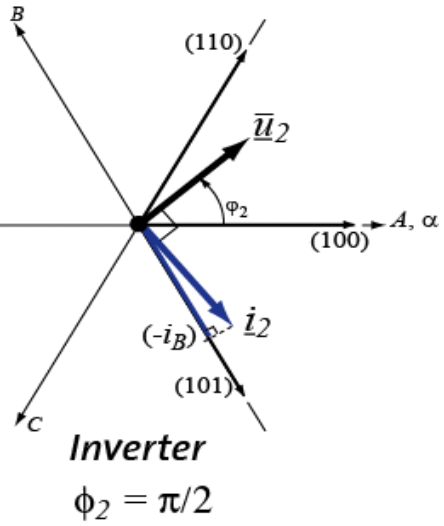
Basic Principle

Outp.Volt.Form. $\bar{p}_u = 0$, $\Delta i_{a,b,c} = 0$ | **Inp.Curr.Form.** $\bar{p}_i = 0$, $\Delta u_{A,B,C} = 0$



▶ $\hat{I}_1 \neq 0,\ \hat{U}_2 \neq 0$ ➡ $S_1 \neq 0,\ S_2 \neq 0$





- **Decouple Output Voltage-** & **Reactive Input Current** Formation
- Use **Largest Output Phase Current** (**-i_B**) for **Input Current Formation** ➲ (**2nd Half** of Pulse Period)
- **Merge Both Halves** finally

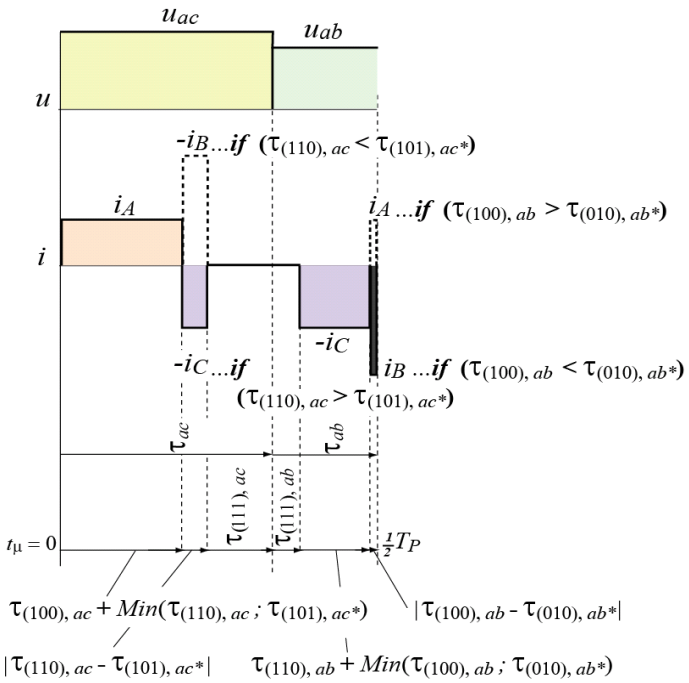
➡ Use **Two** Discrete **Input Vectors** (***ac***, ***ab***)

Reactive Power Coupling I (RPCI)

Pulse Merging & Additional Turn-On-Times

Outp.Volt & Inp.Current Formation

$\bar{p} = 0$



- **Merge Current Blocks to Regain Voltage Modulation Range**

Considering geometrical relations:

$$\frac{\sin(\pi/3-\varphi_1)}{d_{ac}^{\,*}\cdot i_{2,max}} = \frac{\cos(\varphi_1+\pi/6)}{d_{ac}^{\,*}\cdot(-i_B)} = \frac{\sin(\pi/3)}{\hat{I}_{1q}^{\,*}}$$

$$\frac{\sin(\pi/3+\varphi_1)}{d_{ba}^{\,*}\cdot i_{2,max}} = \frac{\cos(\varphi_1-\pi/6)}{d_{ab}^{\,*}\cdot i_B} = \frac{\sin(\pi/3)}{\hat{I}_{1q}^{\,*}}$$

and:

$$i_B = \hat{I}_2\cdot\cos(\varphi_2-2\pi/3-\pi/2) = -\hat{I}_2\cdot\cos(\varphi_2-\pi/6)$$

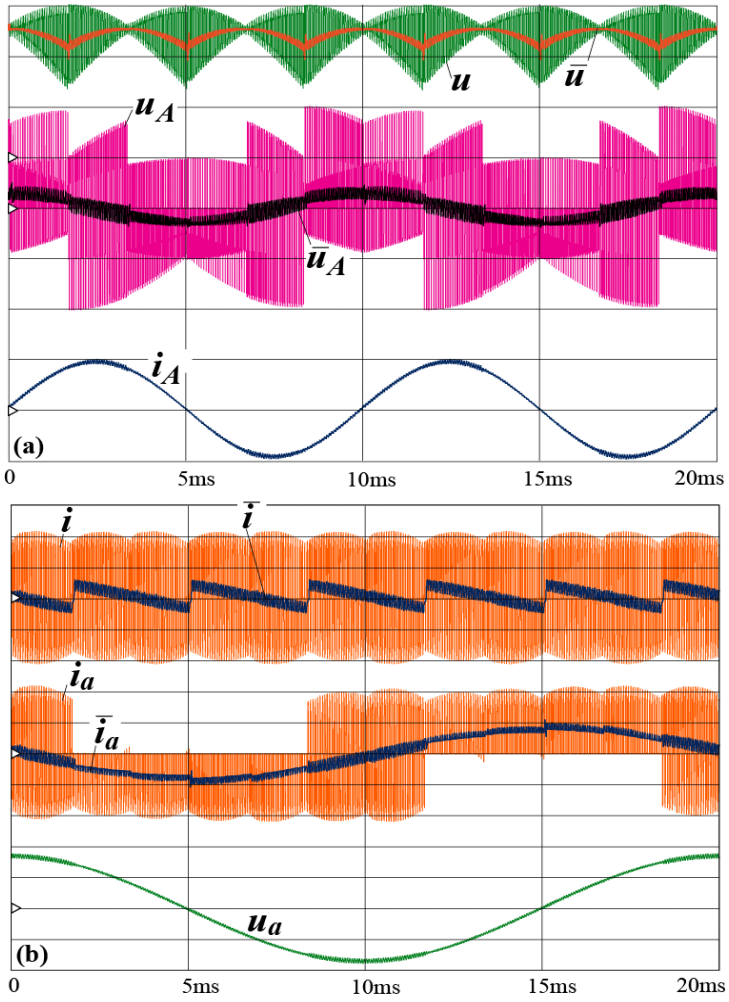
Additional Turn-on-Times:

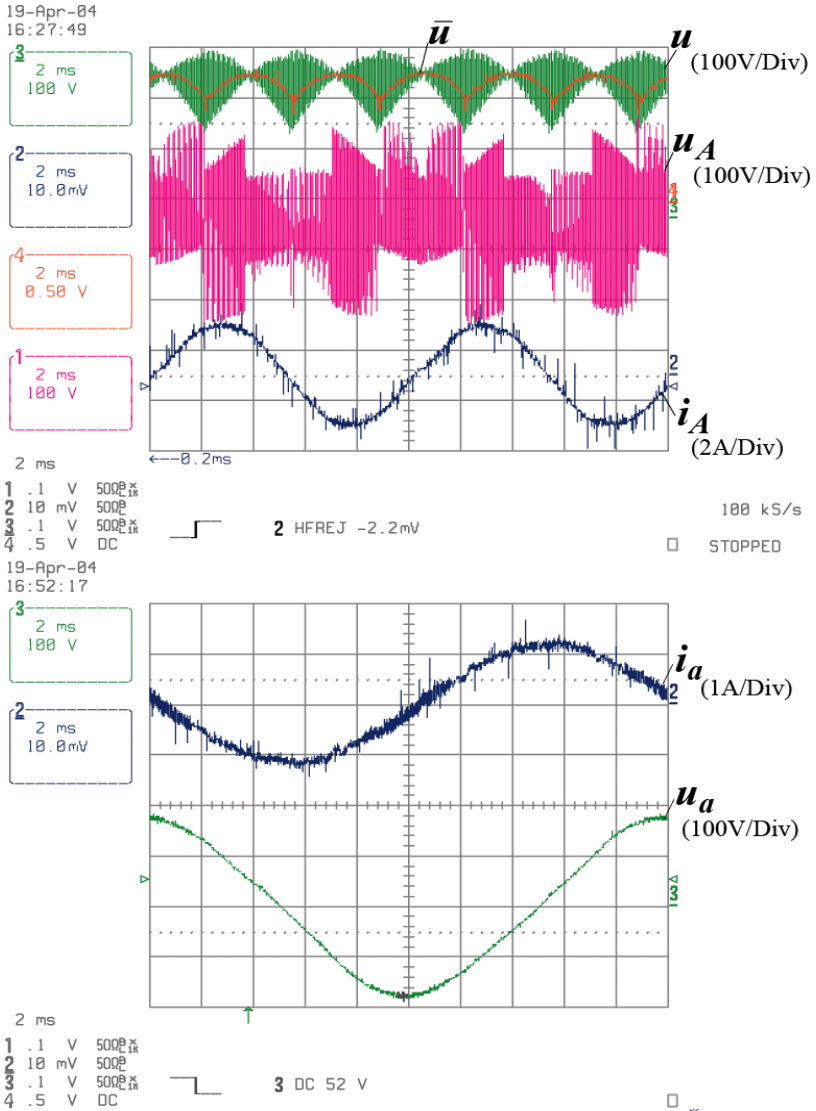
$$d_{ab}^{\,*} = \frac{2}{\sqrt{3}}\frac{\hat{I}_{1q}^{\,*}}{\hat{I}_2}\cdot\frac{\cos(\varphi_1-\pi/6)}{\cos(\varphi_2-\pi/6)}$$

$$d_{ac}^{\,*} = \frac{2}{\sqrt{3}}\frac{\hat{I}_{1q}^{\,*}}{\hat{I}_2}\cdot\frac{\cos(\varphi_1+\pi/6)}{\cos(\varphi_2-\pi/6)}$$

Reactive Power Coupling I (RPCI)

Simulation & Experimental Result

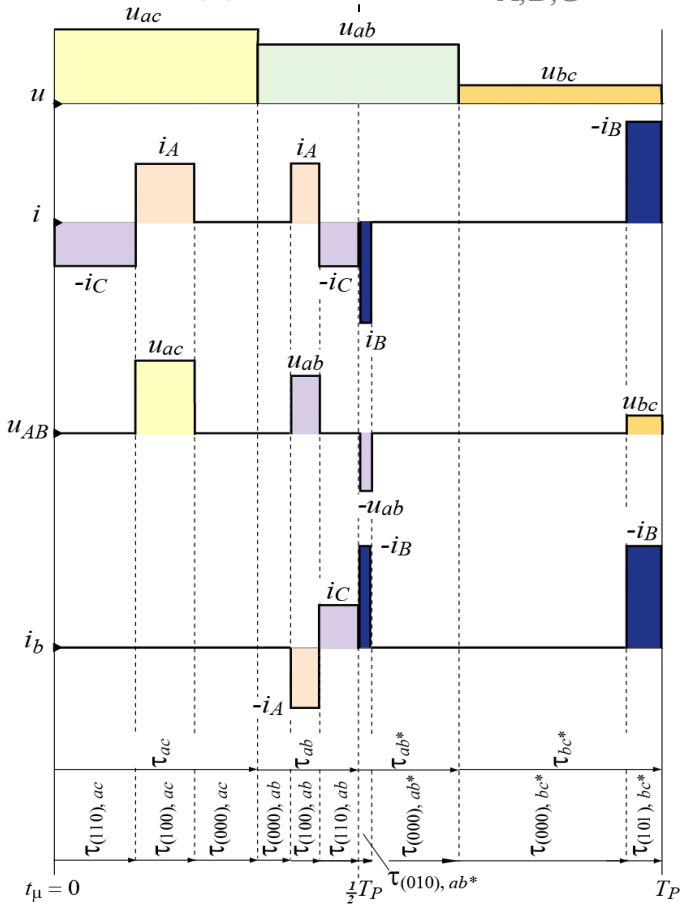




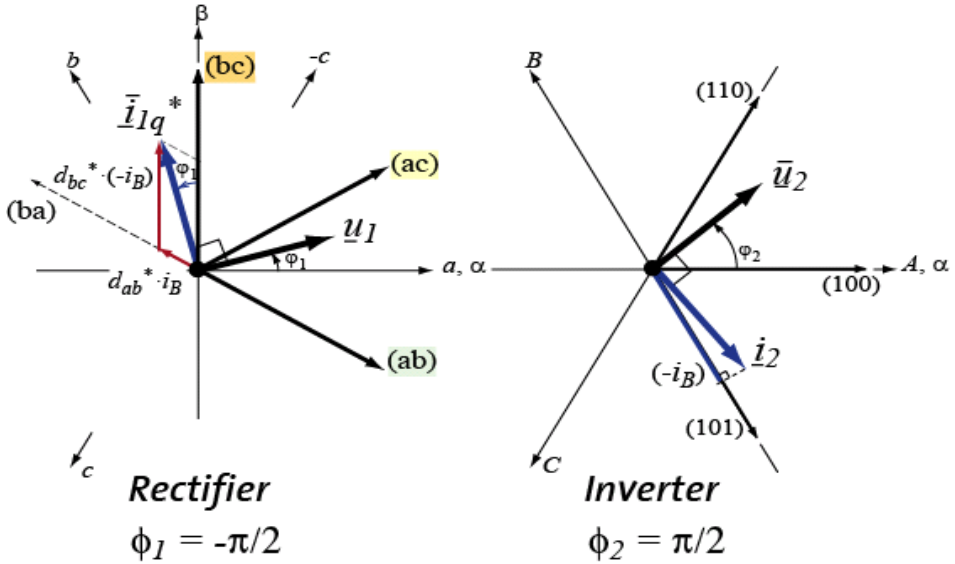
Reactive Power Coupling II (RPCII)

Basic Principle

Outp.Volt.Form. $\bar{p}_u = 0$, $\Delta i_{a,b,c} = 0$ | **Inp.Curr.Form.** $\bar{p}_i = 0$, $\Delta u_{A,B,C} = 0$



▶ $\hat{I}_1 \neq 0,\ \hat{U}_2 \neq 0$ ➡ $S_1 \neq 0,\ S_2 \neq 0$



- Decouple Output Voltage- & Reactive Input Current Formation
- Use Largest Output Phase Current ($-i_B$) for Input Current Formation ➲ (2nd Half of Pulse Period)
- Merge Both Halves finally

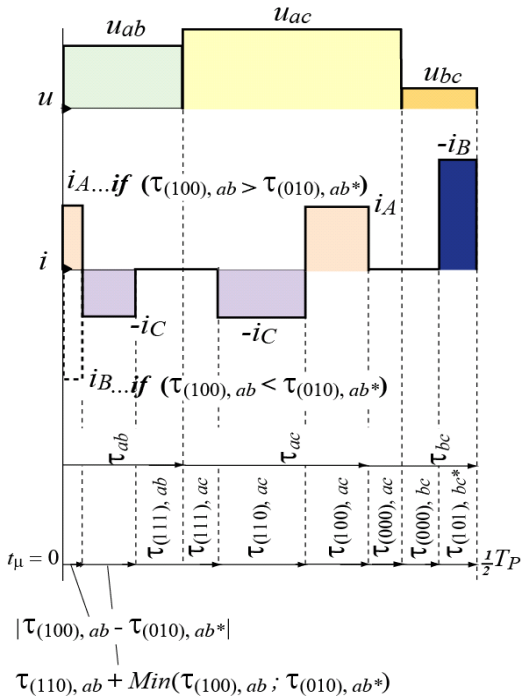
➡ Use **Three** Discrete **Input Vectors** (***ac, ab, bc***)

Reactive Power Coupling II (RPCII)

Pulse Merging & Additional Turn-On-Times

Outp.Volt & Inp.Current Formation

$\bar{p} = 0$



- **Only One** of the Additional **Two** Current Blocks **can be Merged**

Additional Turn-on-Times:

$\varphi_1 > 0$:

$$d_{ab}^{*} = \frac{2}{\sqrt{3}} \frac{\hat{I}_{1q}^{*}}{\hat{I}_2} \cdot \frac{\sin(\varphi_1)}{\cos(\varphi_2 - \pi/6)}$$

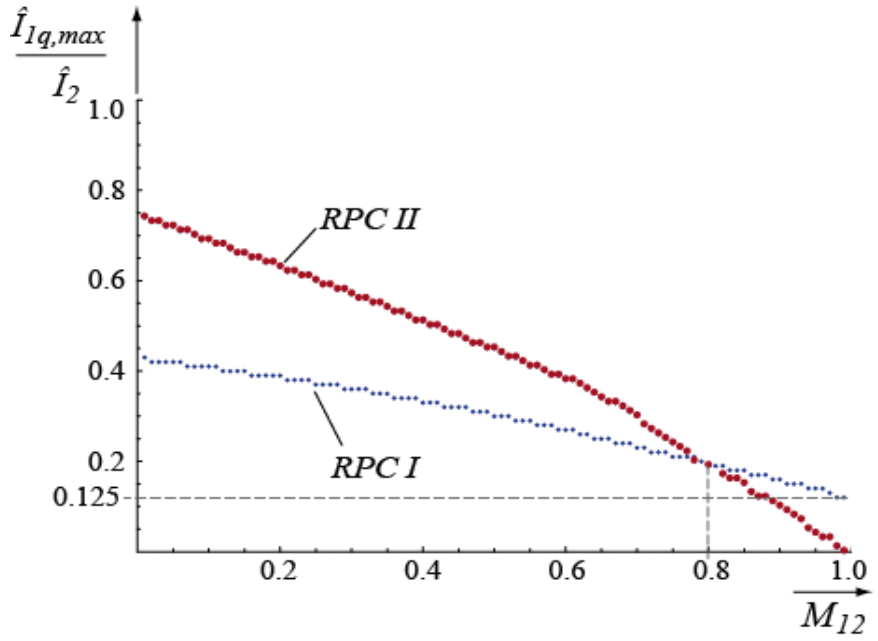
$$d_{bc}^{*} = \frac{2}{\sqrt{3}} \frac{\hat{I}_{1q}^{*}}{\hat{I}_2} \cdot \frac{\cos(\varphi_1 + \pi/6)}{\cos(\varphi_2 - \pi/6)}$$

$\varphi_1 < 0$:

$$d_{ac}^{*} = \frac{2}{\sqrt{3}} \frac{\hat{I}_{1q}^{*}}{\hat{I}_2} \cdot \frac{\sin(|\varphi_1|)}{\cos(\varphi_2 - \pi/6)}$$

$$d_{cb}^{*} = \frac{2}{\sqrt{3}} \frac{\hat{I}_{1q}^{*}}{\hat{I}_2} \cdot \frac{\cos(|\varphi_1| + \pi/6)}{\cos(\varphi_2 - \pi/6)}$$

RPC I vs. RPC II
Operating Limits & Evaluation



- **Intersection** of both Limits:
  $M_{12} = 0.8$

RPC I:

\+ For Large M_{12} ($M_{12} > 0.8$)

\+ Allows Even at Full Output Voltage ($M_{12} = 1$) a Transfer Ratio of $\hat{I}_{1q,max} / \hat{I}_2 = 1/8$

\+ More Easy to Implement

RPC II:

\+ For Small M_{12} ($M_{12} < 0.8$)

\+ Facilitates Large reactive Current Transfer Ratios (up to $\hat{I}_{1q,max} / \hat{I}_2 = 3/4$ @ $M_{12} = 0$)

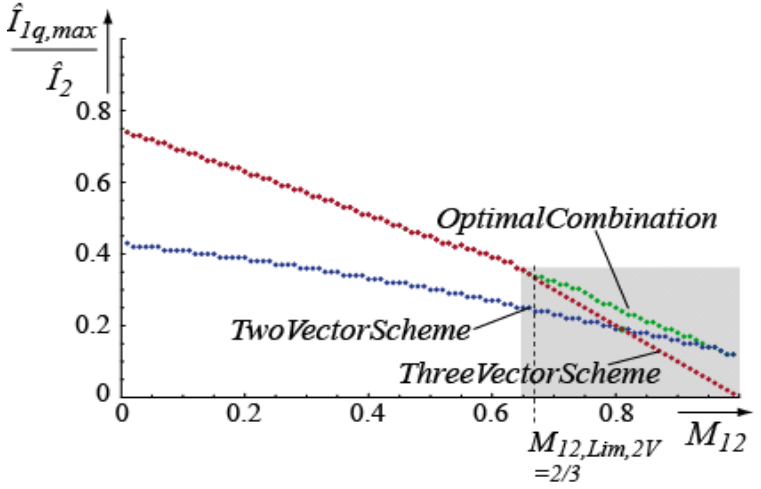
Hybrid Modulation Scheme for MC

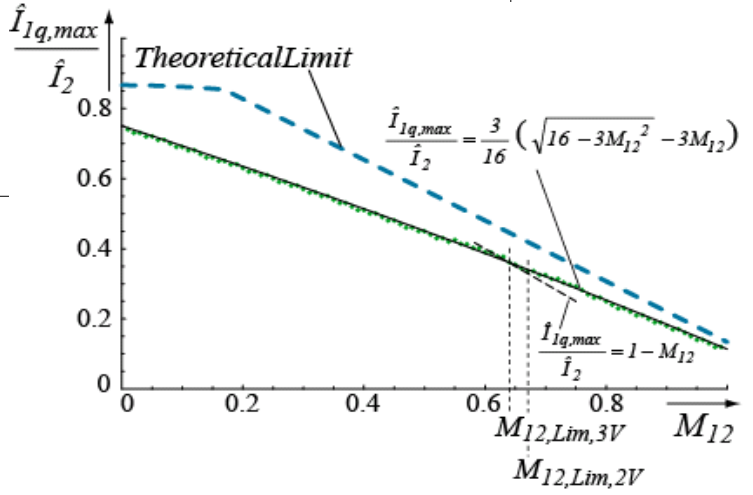
Optimum Combination, ($\phi_2=\pi/2$)

Total Turn-on-Time:

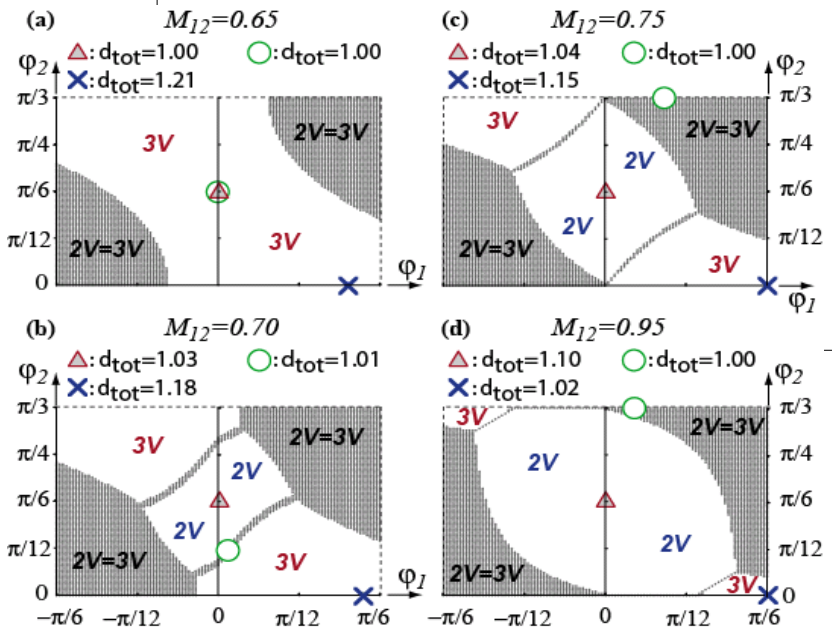
$$d_{tot,2V} = \left|\delta_{(110),ac} - d_{ac}^{*}\right| + \delta_{(100),ac} + Min(\delta_{(110),ac}, d_{ac}^{*}) +$$
$$+ \left|\delta_{(100),ab} - d_{ab}^{*}\right| + \delta_{(110),ab} + Min(\delta_{(100),ab}, d_{ab}^{*})$$
$$\leq 1$$

Operating Limit & Analytical Description:





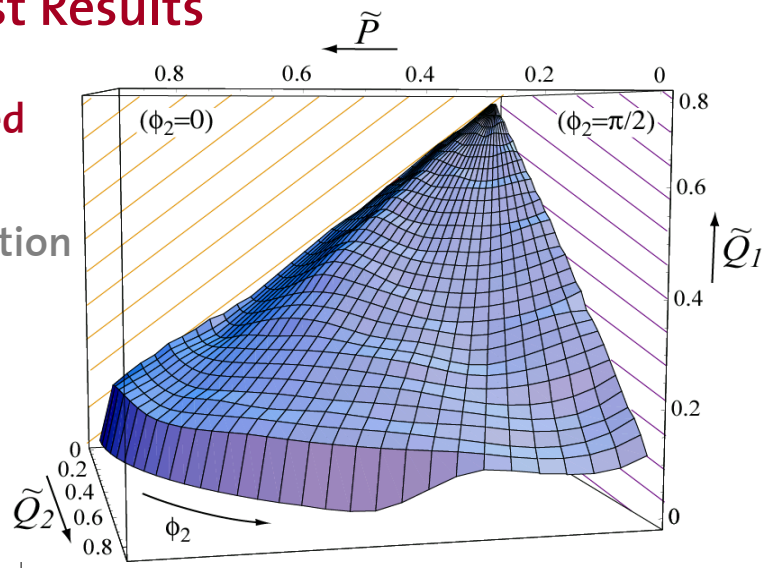
Domains within φ_1-φ_2-Plane:



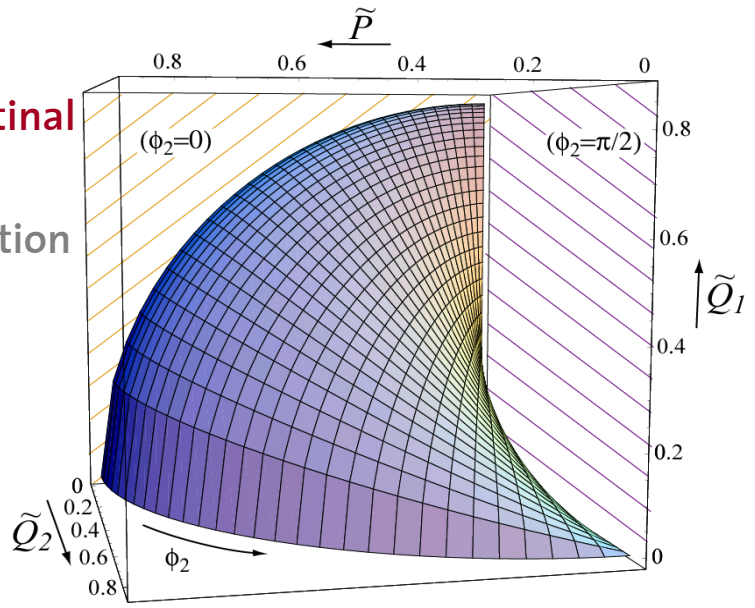
Generalizing the Hybrid Method
for Operation with Arbitrary Load (ϕ_2=0...π/2)

First Results

Proposed Hybrid Modulation

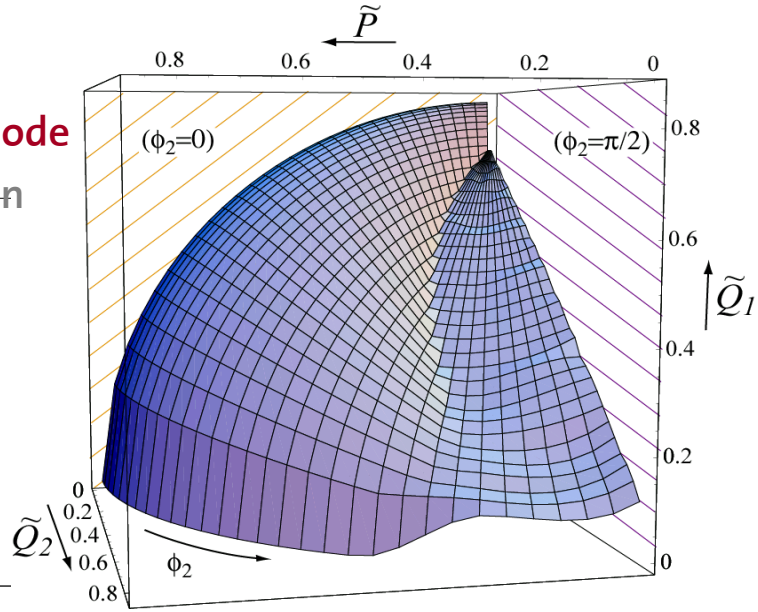


Conventinal Indirect Modulation



- Using various **Case Differentiations** the **Special Cases ϕ_2=0 & ϕ_2=π/2** can be **Utilized to Realize Hybrid Modulation** for the **Entire Range ϕ_2= 0...π/2**

Mixed Mode Operation



- *Mixed Mode Operation* means:
  Q1 is **Either** generated with **Hybrid-**,
  Or with **Conventional** Modulation **Exclusively**

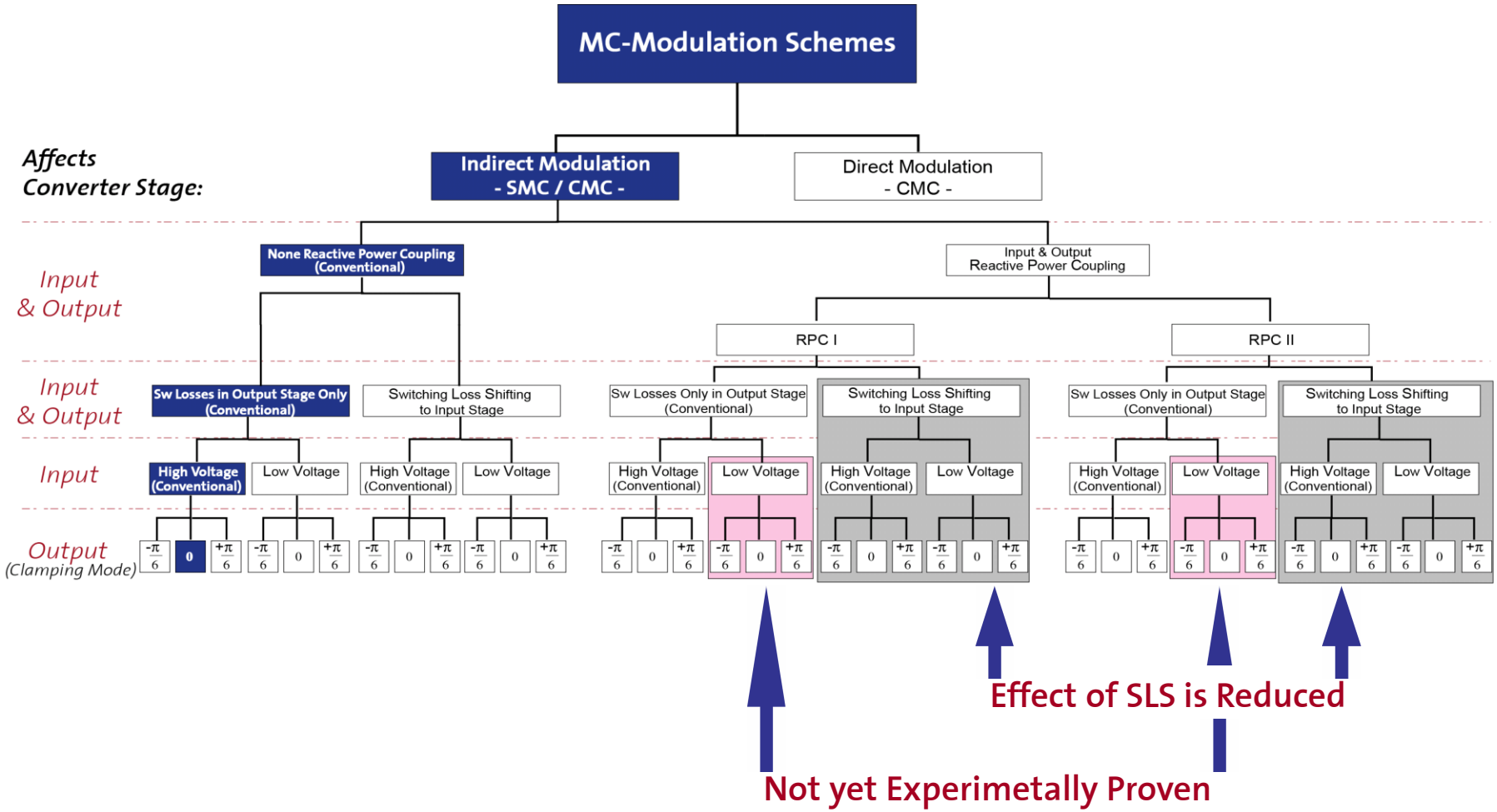
Modified Modulation Schemes

Survey

Conventional:	*Modified:*	*Modulation Differs for:*
High Output Voltage Modulation	**Low Output Voltage Modulation** + Reduced Switching Losses - Max. Output Voltage is Reduced	Input Stage (Formation of DC-link Voltage)
Switching Losses in Output Stage Only	**Switching Loss Shifting to Input Stage** + Shifting & Splitting Switching Losses - Works for Output Phase Displacement $\phi_2 < \pi/6$ & High Output Currents Only	Input- & Output Stage (Commutation Interaction)
None Reactive Power Coupling	**Input & Output Reactive Power Coupling** **RPC I** **RPC II** + Purely Reactive Output Power can be Coupled to Purely Reactive Input Power - Works with "Switching Loss Shifting" in Special Cases Only	Input- & Output Stage (Formation of Reactive Input Current / Output Voltage)

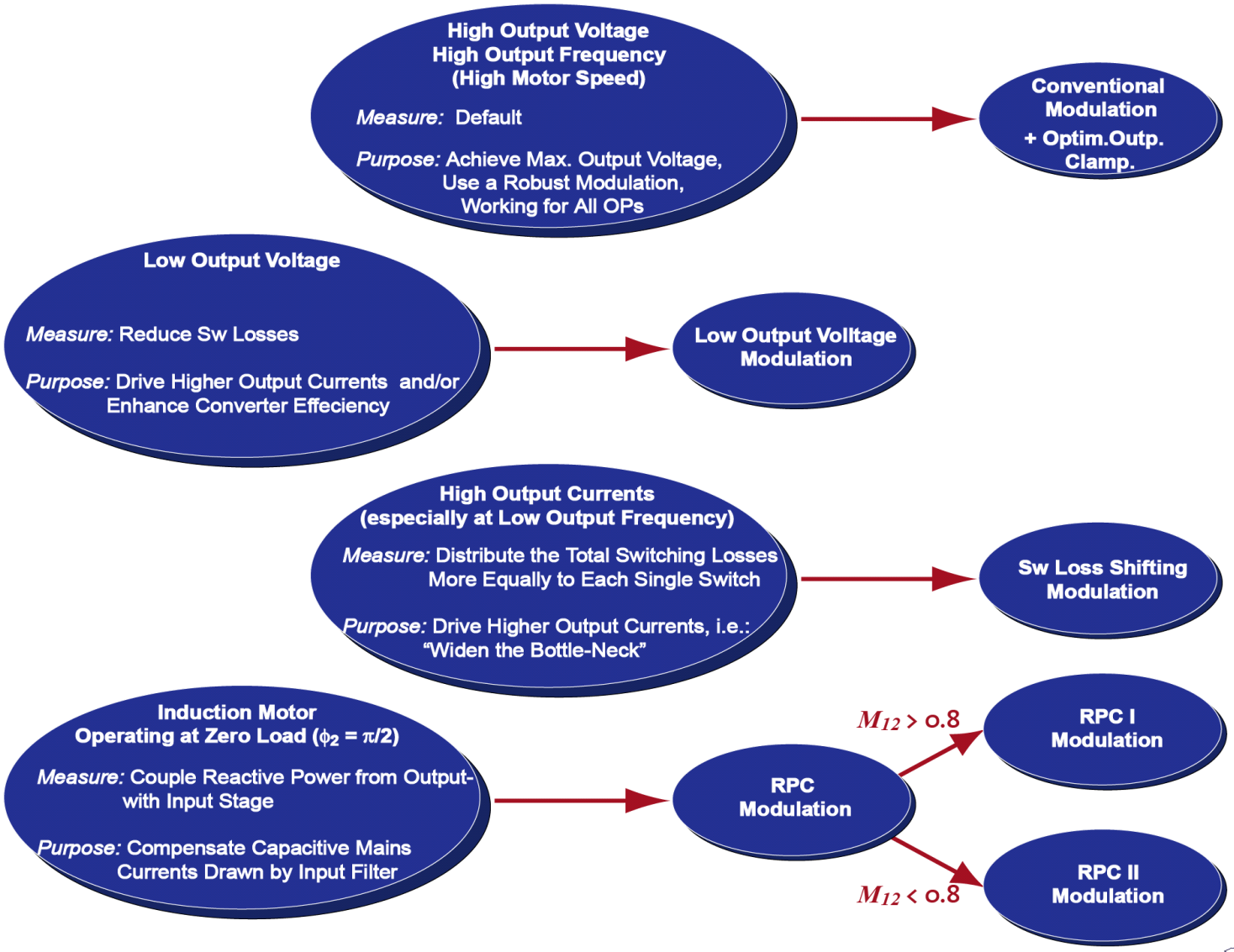
Presented Modulation Schemes

Classification / Possible Combinations

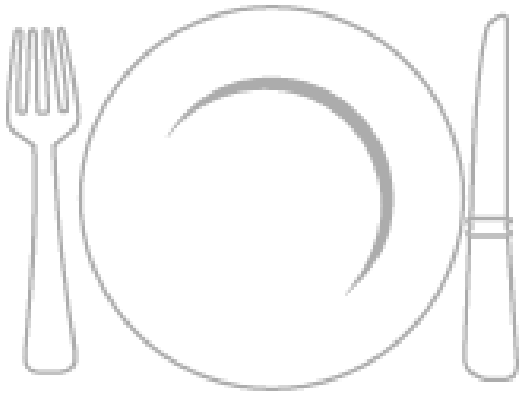


Presented Modulation Schemes

Summary



Lunch Break…



Matrix Converter – Design Issues

Frank Schafmeister and Marcelo L. Heldwein

- Calculation of the Stresses on the Components
- EMI Input Filter Design
- Digital Realization of the System Control
- Power circuit protection
- Active Input Filter Damping
- Unbalanced Mains
- Experimental Analysis / Operating Characteristics

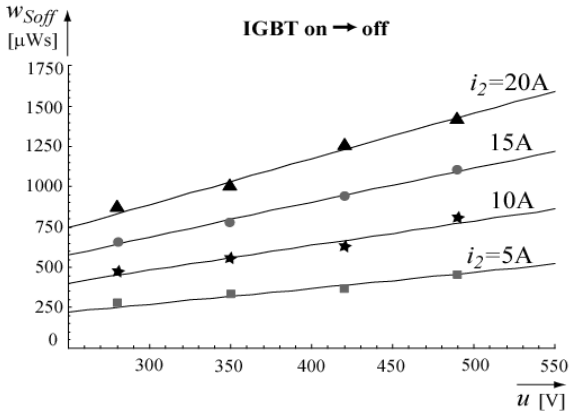
Calculation of the Stresses on the Components

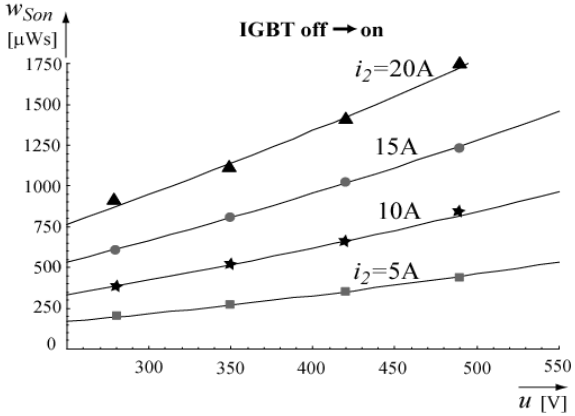
- Aim of presented Calculation Method
  - Providing Dimensioning Equations for Automated Use in Spreadsheet / Applet
- Switching Losses P_{Sw}
  - CMC
  - (V)SMC
- Conduction Losses P_C
  - CMC in Paper
  - (V)SMC in Paper
    (*F. Schafmeister, J. Kolar, "Analytical Calculation of the Conduction and Switching Losses of the Conventional Matrix Converter and the (Very) Sparse Matrix Converter", APEC 2005.*)

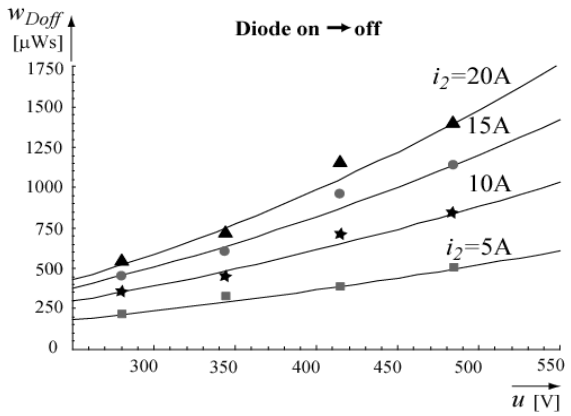
→ Total Losses $P_{tot} = P_{Sw} + P_C$

Switching Losses
Basic Approach

From Measured Data to an **Analytic Model** of the **single Switching Losses:**







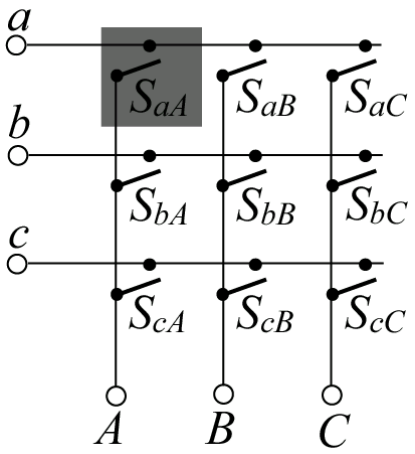
$$w(u,i) = K_1 \cdot u \cdot i_2 + K_2 \cdot u \cdot i_2^{\,2} + K_3 \cdot u^2 + K_4 \cdot u^2 \cdot i_2 + K_5 \cdot u^2 \cdot i_2^{\,2}$$

IGBT- Switching Loss Parameter						
T_j		K_1	K_2	K_3	K_4	K_5
25°C	S_{off}	129	-947 10^{-3}	471 10^{-3}	-84.1 10^{-3}	2.52 10^{-3}
	S_{on}	41.6	1.75	308 10^{-3}	60.7 10^{-3}	-923 10^{-6}
	D_{off}	66.6	-2.54	332 10^{-3}	95.4 10^{-3}	2.90 10^{-3}
120°C	S_{off}	179	-1.31	650 10^{-3}	-116 10^{-3}	3.48 10^{-3}
	S_{on}	70.0	2.94	518 10^{-3}	102 10^{-3}	-1.55 10^{-3}
	D_{off}	97.9	-3.73	488 10^{-3}	140 10^{-3}	4.27 10^{-3}
Units		nWs$(VA)^{-1}$	nWs$(VA^2)^{-1}$	nWs$(V^2)^{-1}$	nWs$(V^2A)^{-1}$	nWs$(V^2A^2)^{-1}$

- **Only Physically Sensible Terms** are Considered for a Least-Square Approximation of the Measured Data

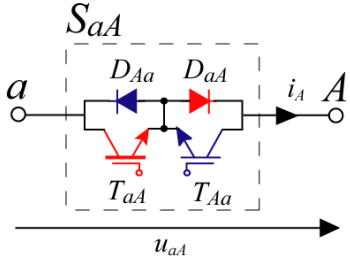
Switching Losses – CMC
Calculation Principle

Summing Up Switching Actions of One Pulse Period
(Exemplary for S_{aA})



$s_{SMC,Rect}$	(ac)			(ab)		
$s_{SMC,Inv}$	(110)	(100)	(000)	(000)	(100)	(110)
$\underline{S}_{CMC}$	1 1 0 0 0 0 0 0 1	1 0 0 0 0 0 0 1 1	0 0 0 0 0 0 1 1 1	0 0 0 1 1 1 0 0 0	1 0 0 0 1 1 0 0 0	1 1 0 0 0 1 0 0 0
$\delta_{110}+\delta_{100}+$ $+\delta_{000}=1$	δ_{110}	δ_{100}	δ_{000}	δ_{000}	δ_{100}	δ_{110}
$d_{ac}+d_{ab}=1$	d_{ac}			d_{ab}		

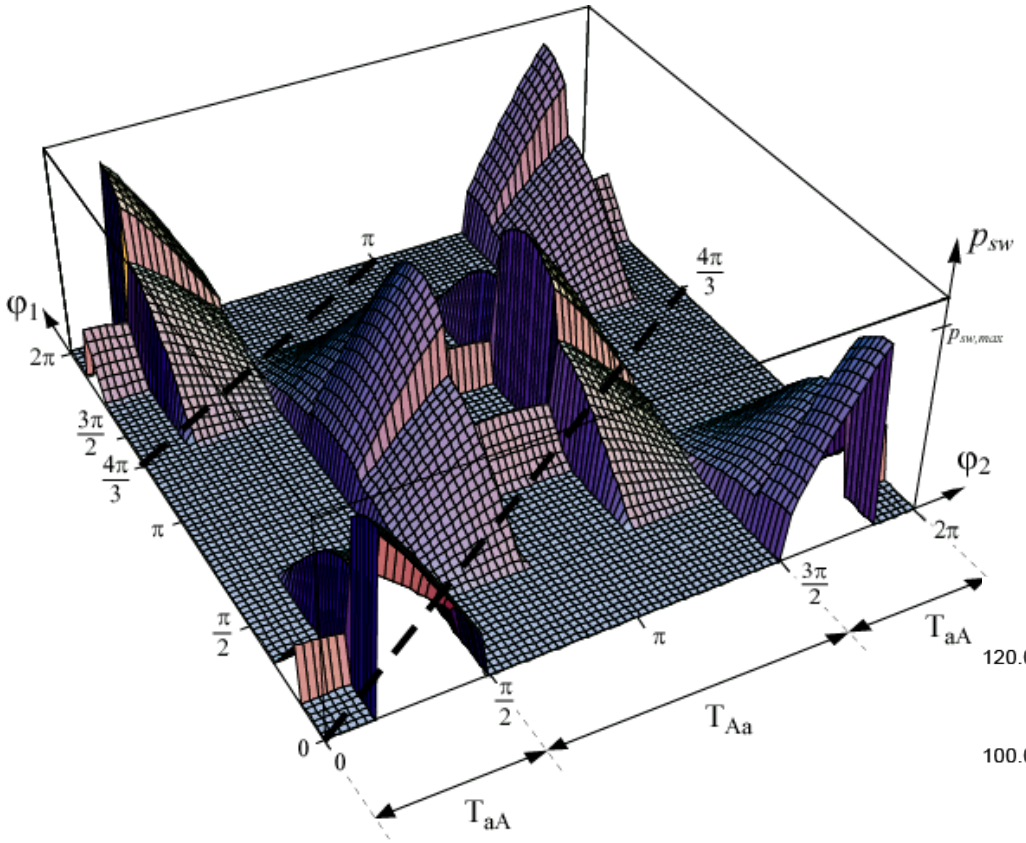
$$p_{Sw} = f_P w_{\Sigma onoff} = p_{Sw}(\varphi_1, \varphi_2)$$ **: Local Losses**



	$u_{aA}>0$	$u_{aA}<0$
$i_A>0$	T_{aA}	D_{aA}
$i_A<0$	D_{Aa}	T_{Aa}

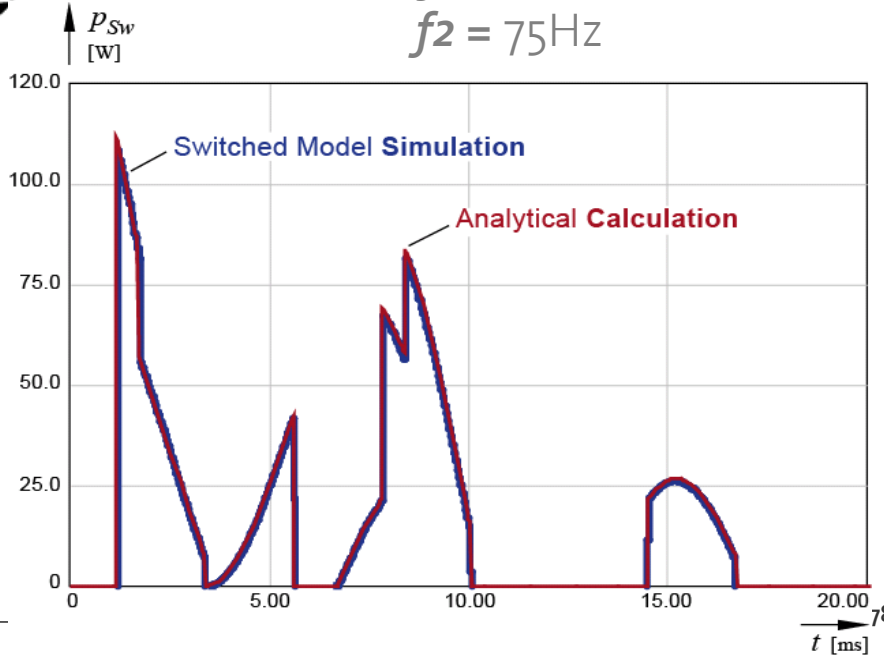
Switching Losses – CMC

Results Local Losses ($\phi_2 = 0$)



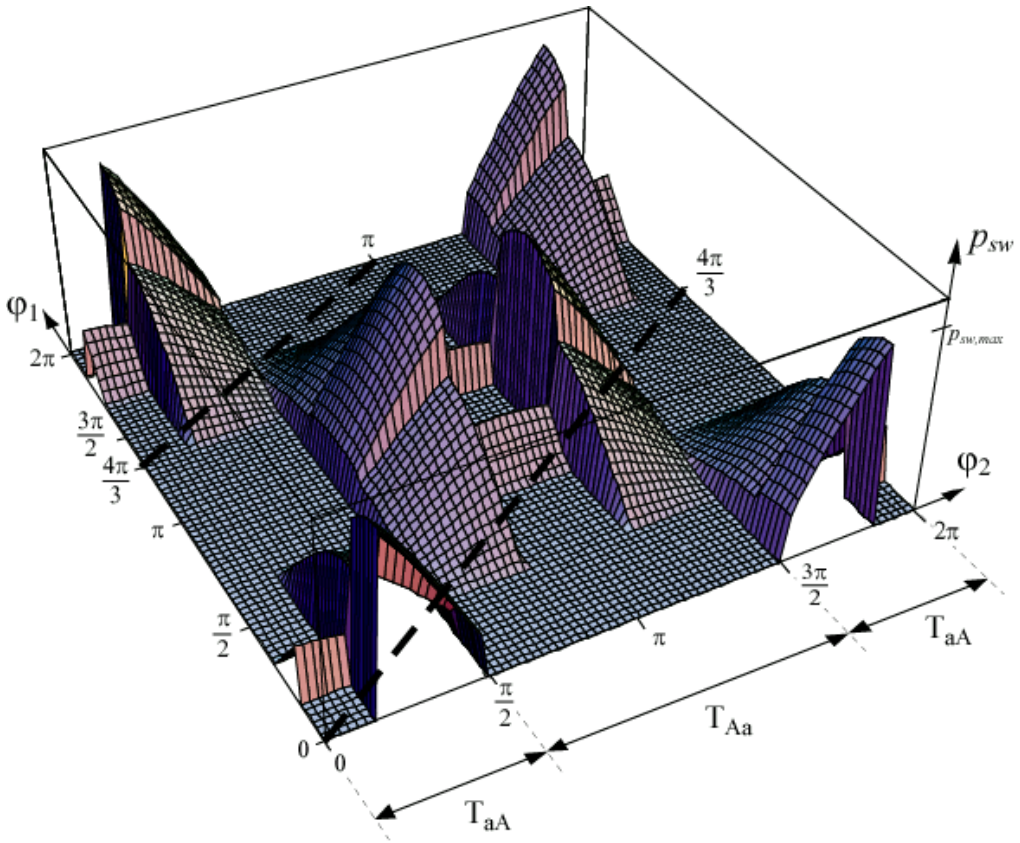
- Max. @ $\varphi_1 = 0 / \pi$ (T_{aA} / T_{Aa})
  $\varphi_2 = 0 / \pi$ (T_{aA} / T_{Aa})
- Transistors Clamped in Output Current Max. ($\varphi_2 = 0 / \pi$), but: BSOs

Verification OP: $f1$ = 50Hz, $f2$ = 75Hz



Losses

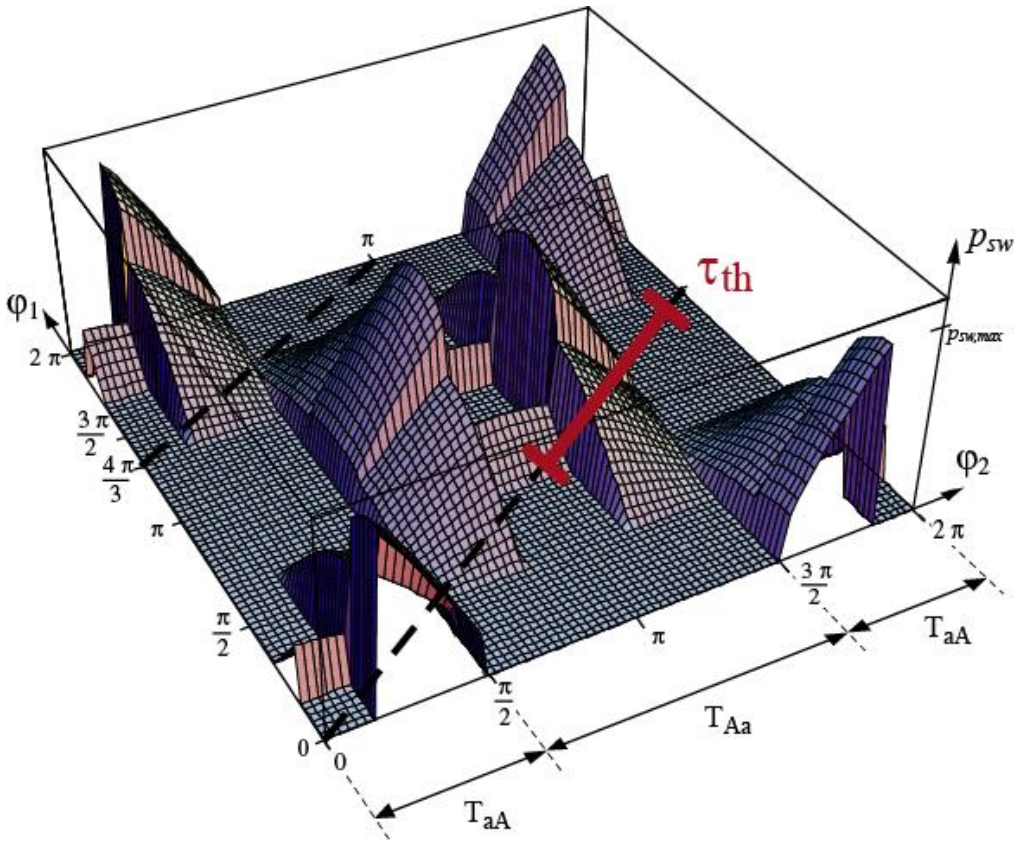
Which Values are Relevant ?

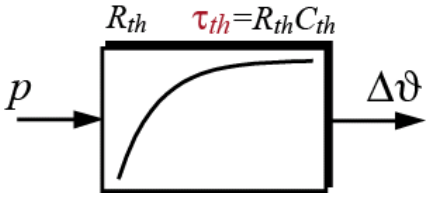


- Total Losses: Global Average over (φ_1, φ_2) → ***Global Losses***

Losses

Which Values are Relevant ?

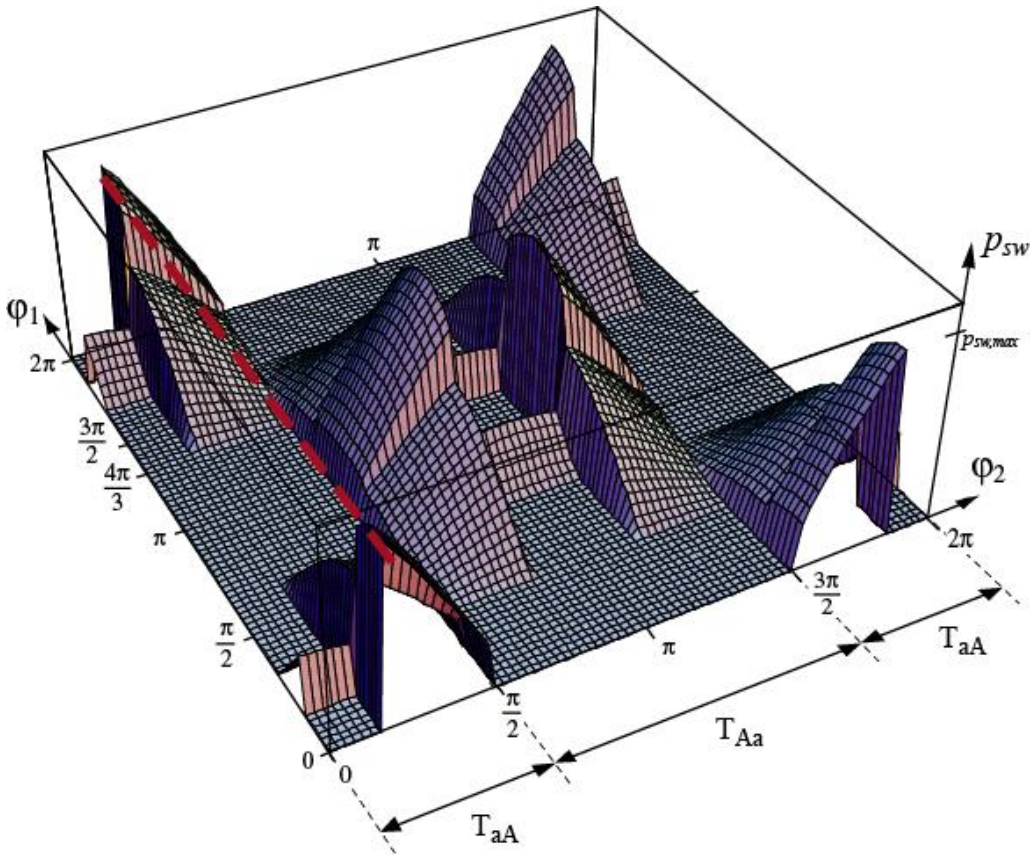




- Total Losses: Global Average over (φ_1, φ_2) → ***Global Losses***
- Junction Temp. Rise: Average over Thermal Time Constant τ_{th}

Losses

Which Values are Relevant ?



➡ ***Global Losses***
(for nearly All OPs)

- **Only Exception:**
  Motor Operation close to Standstill ($f_2 \approx$ 0Hz)

➡ $\text{MaxIn}\varphi_2\{\text{AverageOver}\varphi_1\{p_{Sw}\}\}$ ➡ ***Maximum in $\varphi 2$***

Switching Losses – CMC
Results

Result *Global Losses*

$$P_{Sw,T/D} = \frac{f_P \hat{U}_1}{96\pi^2}\left(22\left(2K_3 + K_5\hat{I}_2^2\right)\pi^2\hat{U}_1 + 12\hat{I}_2\left(12K_1 + \sqrt{3}(8K_1 + 3K_4\hat{U}_1)\right) + \right.$$
$$+ 3\pi\left(4\hat{I}_2(\hat{I}_2K_2 + 10K_4\hat{U}_1) + \sqrt{3}(2K_3\hat{U}_1 + \hat{I}_2^2(8K_2 + K_5\hat{U}_1))\right) -$$
$$- 12\hat{I}_2\left(12K_1 + K_4(3\sqrt{3} + 4\pi)\hat{U}_1\right)\cos\Phi_2 -$$
$$\left. - 3\hat{I}_2^2\left(12\sqrt{3}K_2 + \hat{U}_1K_5(9 + 4\sqrt{3}\pi)\right)\cos(2\Phi_2)\right)$$

Transistors: $K_i \rightarrow K_{i,Ton} + K_{i,Toff}$

Diodes: $K_i \rightarrow K_{i,Doff}$

Entire Converter: $K_i \rightarrow 18(K_{i,Ton} + K_{i,Toff} + K_{i,Doff})$

Result *Maximum in φ2*

$$\hat{\bar{p}}_{Sw,T/D} = \frac{f_P}{16\pi}\left(12\left(3 + 2\sqrt{3}\right)\left(K_1 i_{Sw} + K_2 i_{Sw}^2\right)\hat{U}_1 + 3\left(3\sqrt{3} + 10\pi\right)\left(K_3 + K_4 i_{Sw} + K_5 i_{Sw}^2\right)\hat{U}_1^2\right)$$

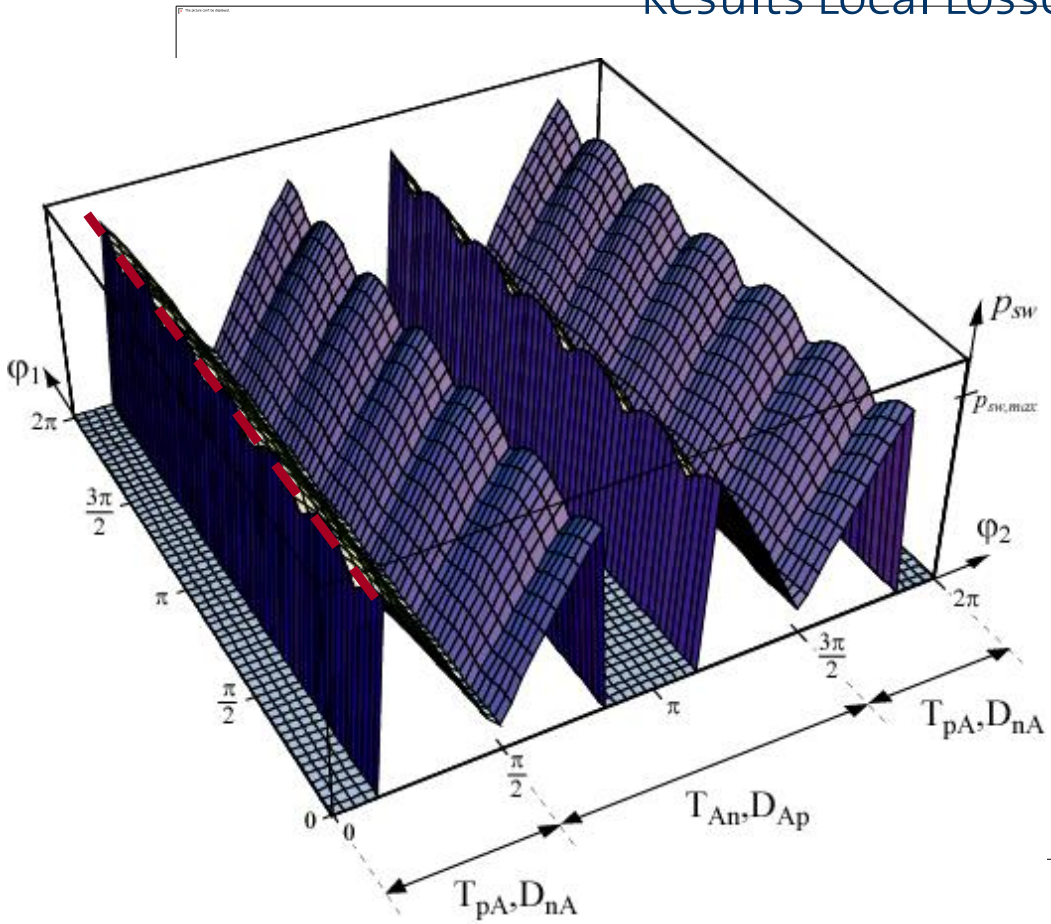
with:

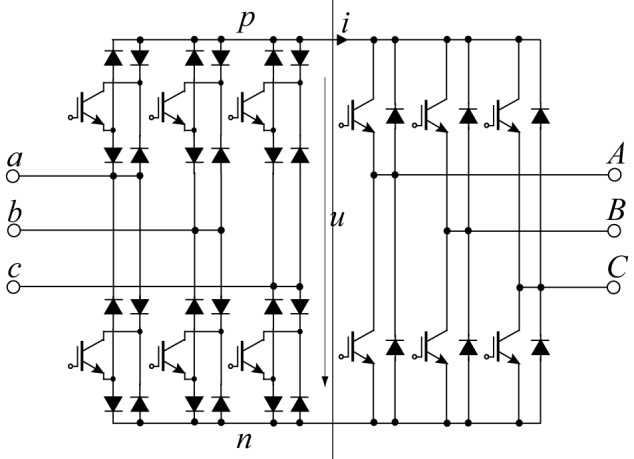
$$i_{Sw} = \hat{I}_2\cos(\Phi_2 - \pi/6) \qquad \text{for} \quad \Phi_2 \in [0 \ldots \pi/6]$$

$$i_{Sw} = \hat{I}_2 \qquad \text{for} \quad \Phi_2 \in [\pi/6 \ldots \pi/2]$$

Switching Losses – (V)SMC

Results Local Losses ($\phi_2 = 0$)





- Transistors Clamped in Output Current Max. (φ_2 = 0 / π), so: No Sw. Losses
- Periodicity in φ_1 is 1/6 of Mains Period
- More Critical Trajectory at Standstill ($f2 \approx$ 0Hz) because of High Average Value

Switching Losses – (V)SMC
Results

- Result *Global Losses*

$$P_{Sw,T/D} = \frac{f_P \hat{U}_1}{32\pi^2}\left(48\hat{I}_2\left(6K_1 + K_2\hat{I}_2\pi\right) + 4\hat{U}_1(3\sqrt{3}+4\pi)\left(6K_4\hat{I}_2 + 2\pi K_3 + \pi K_5\hat{I}_2^2\right)\right) -$$
$$-12\hat{I}_2\left(12K_1 + K_4(3\sqrt{3}+4\pi)\hat{U}_1\right)\cos\Phi_2 - 3\hat{I}_2^2\left(12\sqrt{3}K_2 + \hat{U}_1K_5(9+4\sqrt{3}\pi)\right)\cos(2\Phi_2)\Big).$$

Transistors: $K_i \rightarrow K_{i,Ton} + K_{i,Toff}$

Diodes: $K_i \rightarrow K_{i,Doff}$

Entire Converter: $K_i \rightarrow 6(K_{i,Ton} + K_{i,Toff} + K_{i,Doff})$

- Result *Maximum in φ2*

$$\hat{\bar{p}}_{Sw,T/D} = f_P\left(\left(K_1 i_{Sw} + K_2 i_{Sw}^2\right)\frac{9}{\pi}\hat{U}_1 + \left(K_3 + K_4 i_{Sw} + K_5 i_{Sw}^2\right)\left(\frac{9\sqrt{3}}{4\pi} + 3\right)\hat{U}_1^2\right)$$

with:

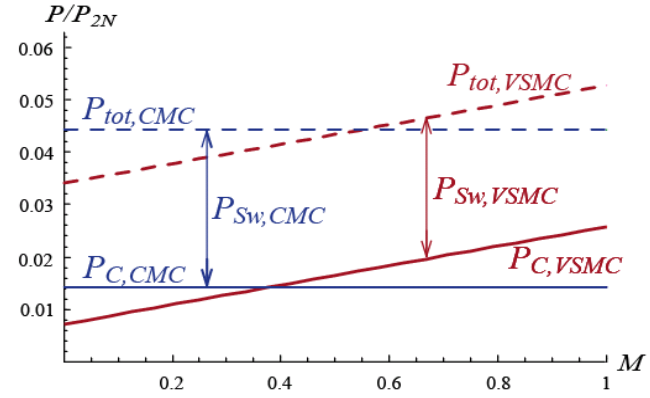
$$i_{Sw} = \hat{I}_2\cos(\Phi_2 - \pi/6) \quad \text{for} \quad \Phi_2 \in [0...\pi/6]$$
$$i_{Sw} = \hat{I}_2 \quad \text{for} \quad \Phi_2 \in [\pi/6...\pi/2]$$

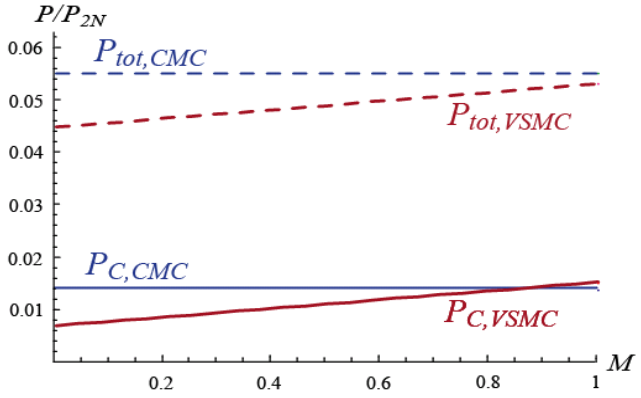
Global Losses Entire Converter

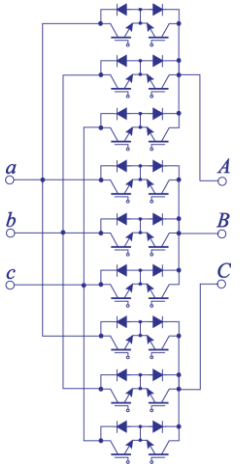
Comparison CMC – VSMC

Total Global Losses $P_{tot} = P_{Sw} + P_C$ in Dependency of M and Φ_2

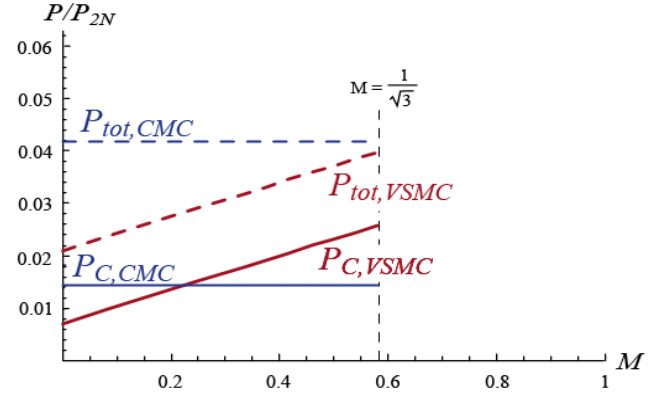
HV-Modulation

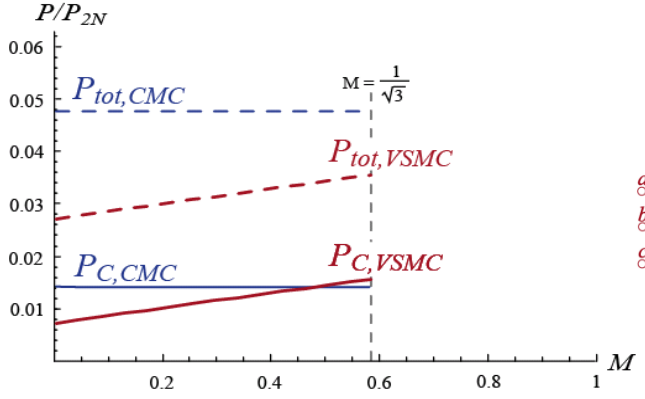


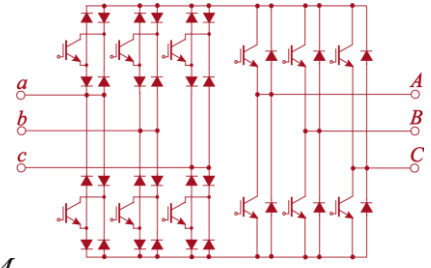




LV-Modulation





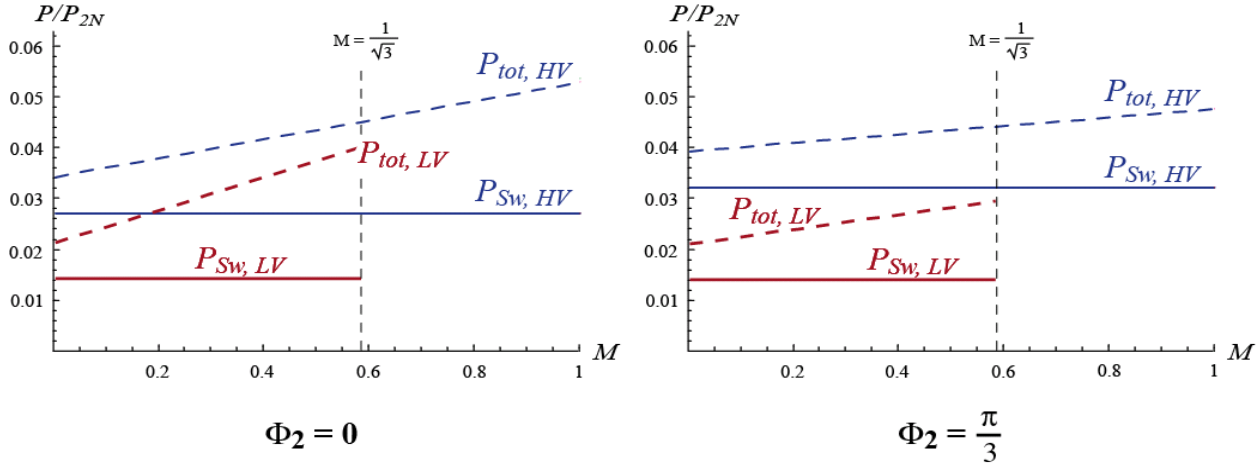


$\Phi_2 = 0$ $\Phi_2 = \frac{\pi}{3}$

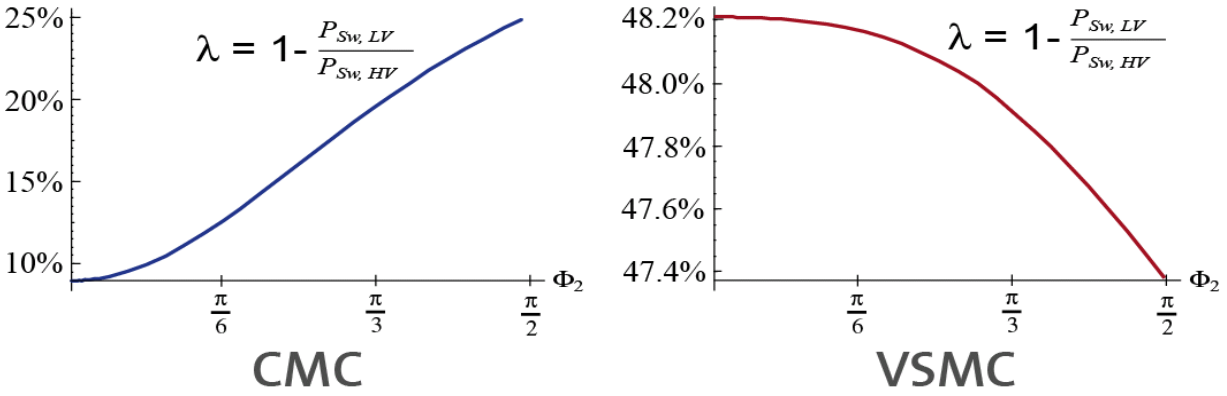
SMC - CMC Performance Comparison

Losses in Dependency of Modulation Index

Comparison: HV vs. LV Modulation for SMC



Sw. Loss Reduction λ achieved with LV: CMC vs. SMC,



Conclusion
of Presented Loss Calc. Method

- CMC & (V)SMC **Sw. & Cond. Loss Equations** are Derived
- **All Analytic Equations show a High Accuracy (Deviation < 8%)**
- Results (***Global Losses*** & ***Local Losses***) will be used for **Automated System Dimensioning** within Spreadsheet / Applet

EMI Input Filter Design

Requirements and critical points

Requirements

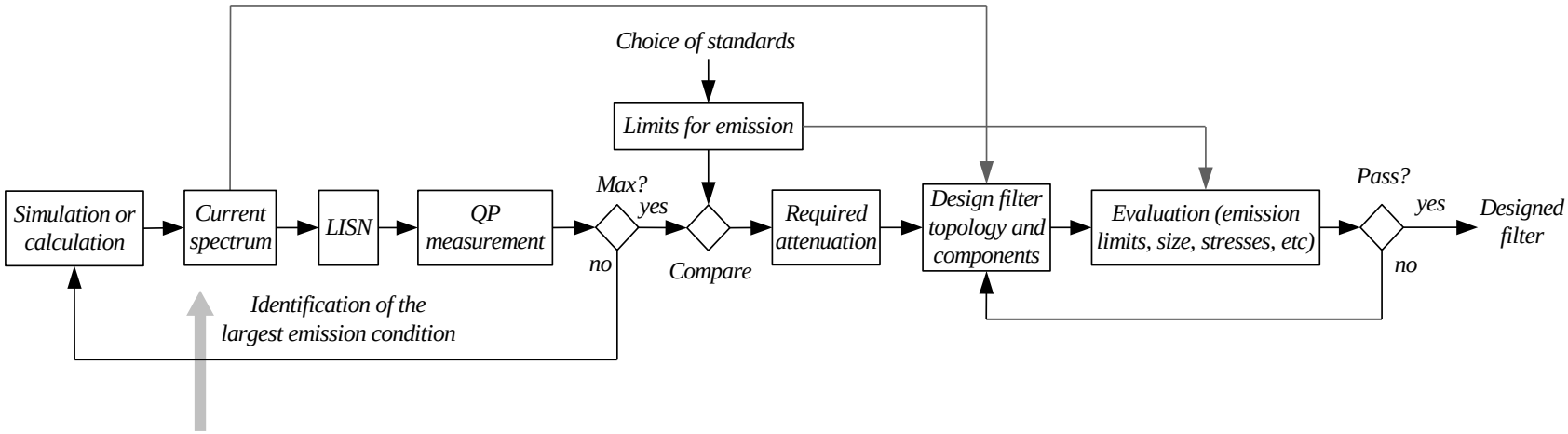
- Fulfillment of international EMC regulations what translates into minimum filter attenuation at given frequencies
- Minimization of input current displacement factor
- Limitation of the energy stored in the filter components, in order to minimize the physical size
- Sufficient or optimum passive damping, in order to avoid oscillations and also for no-load operation with minimum losses in the damping resistors
- Avoidance of filter resonance frequencies at multiples of the switching frequency
- Minimization of the filter output impedance, reducing system stability problems and control design restrictions

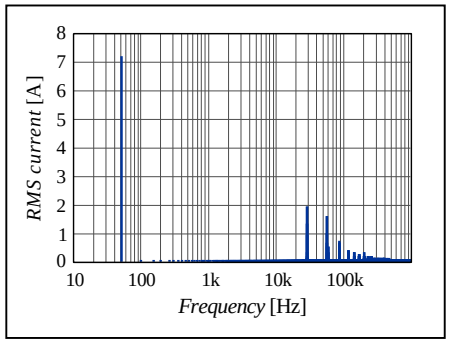
Critical Aspects

- The input current spectrum for a Matrix converter is not obviously calculated
- Uncertainty in the mains impedance
- Modeling of the EMC test receiver
- High-frequency behavior is influenced by parasitics of the filter elements and therefore difficult to predict
- In today's power electronic systems the filter must be as cheap and as small as possible, presenting a low-count in components, must also acquaint for the smallest physical dimensions possible
- System control stability is affected by the inclusion of the filter

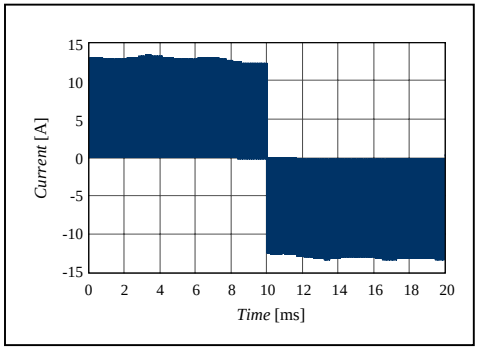
EMI Input Filter Design

Filter Design Procedure

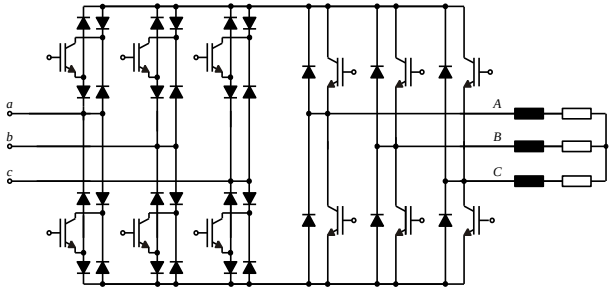




FFT calculation



electric circuit simulation

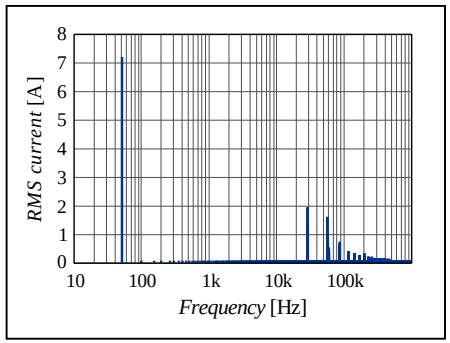


input current spectrum | *input current* | *VSMC*

EMI Input Filter Design

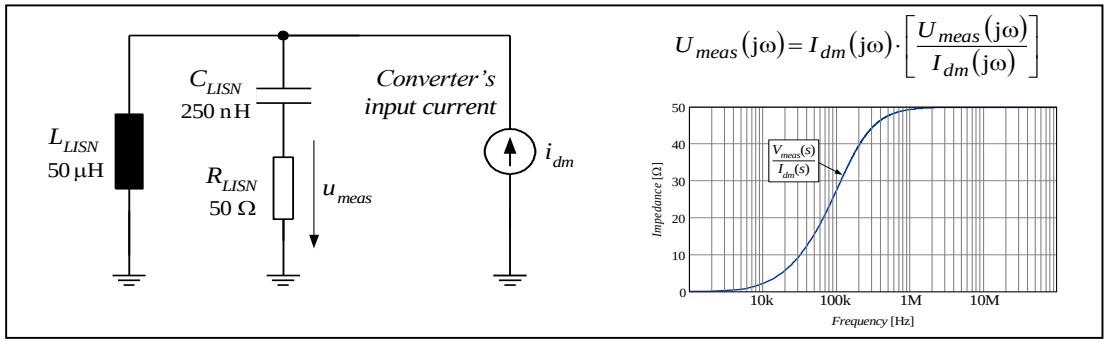
Modeled Spectral Measurement Chain (01)

input current spectrum

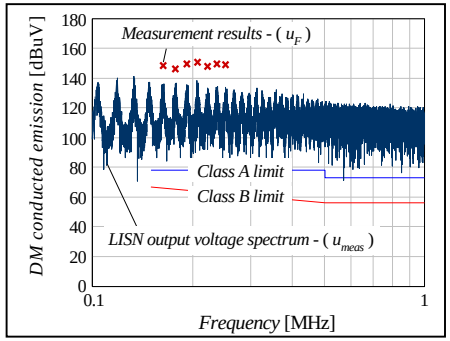


calculation in frequency domain

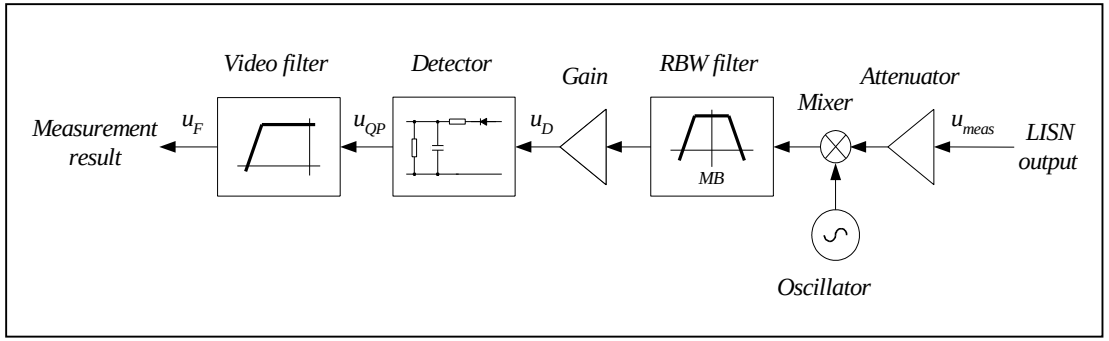
LISN simplified high frequency model



calculations in frequency and time domains



measurement values

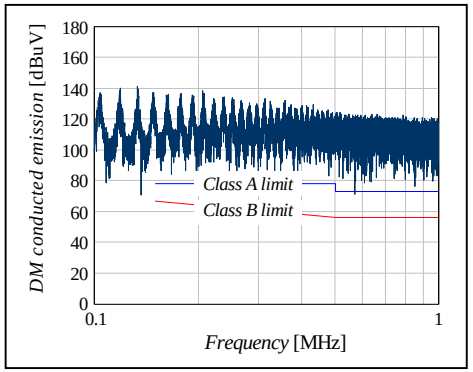


spectral measurement modeled chain

EMI Input Filter Design

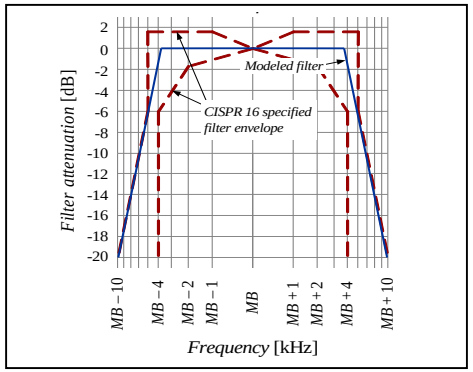
Modeled Spectral Measurement Chain (02)

LISN output voltage spectrum

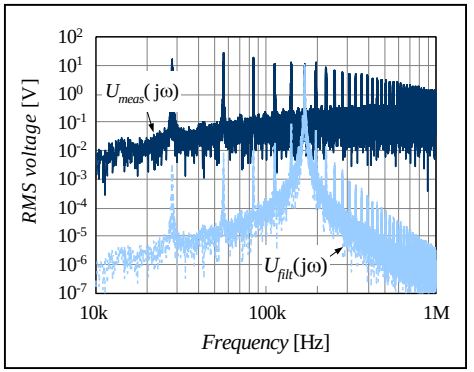


calculation in frequency domain

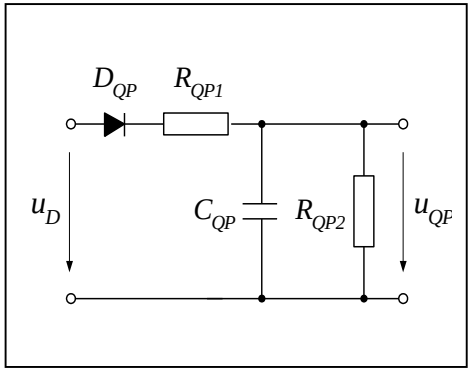
RBW filter



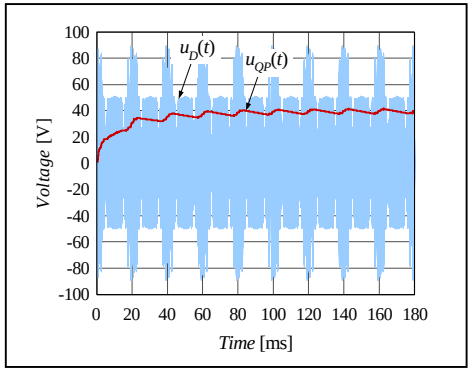
effect of the RBW filtering



calculations in time domain

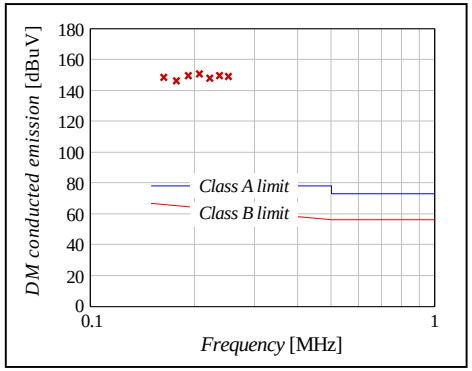


Quasi-Peak detector



effect of the QP detector

averaging of the QP output voltage

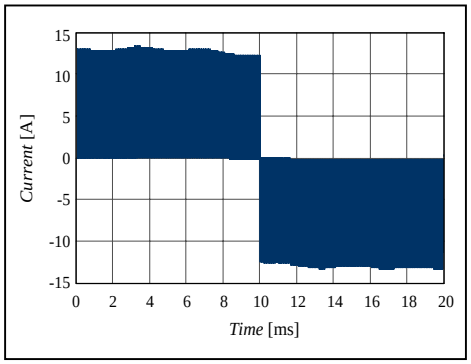


averaged values (final measurement)

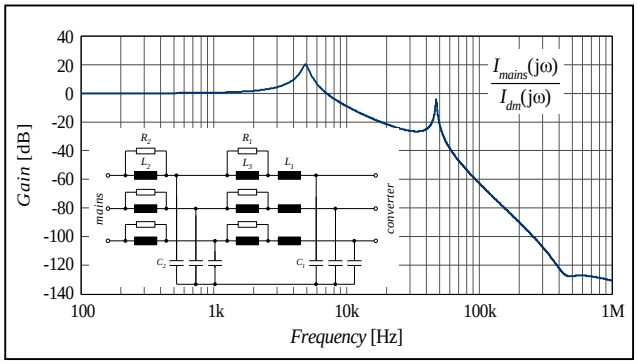
EMI Input Filter Design

Three-phase filter (topology and function) and final result

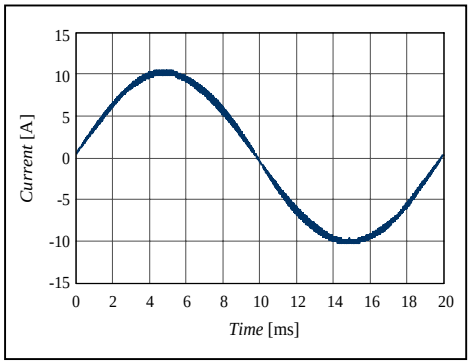
VSMC input current

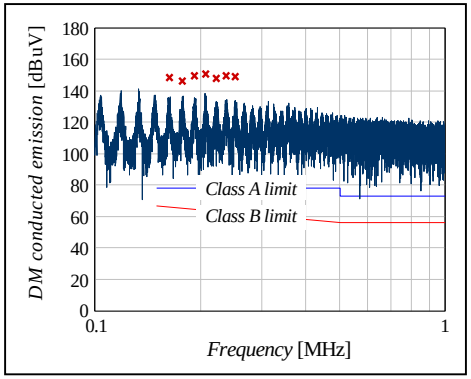


designed three-phase filter

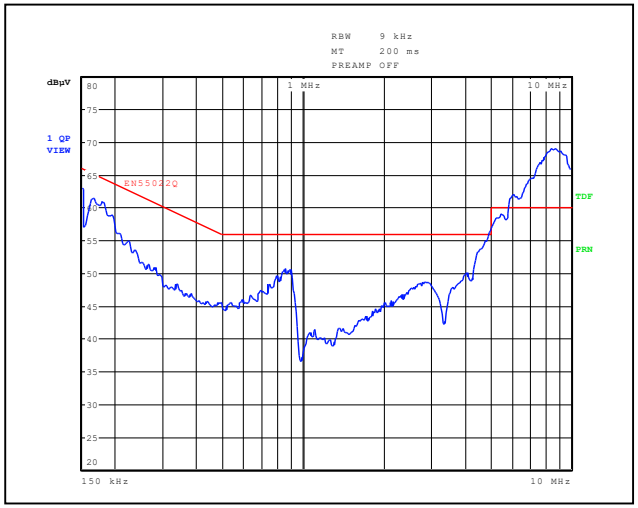


input filtered current

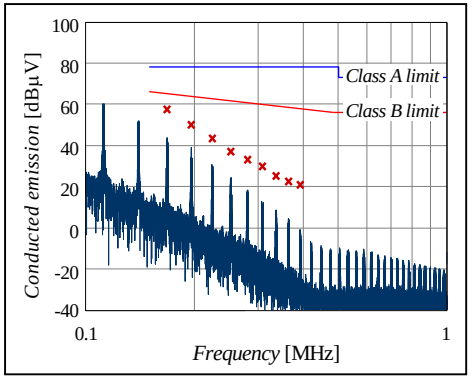




measurement without filter



experimental result (DM conducted emission)



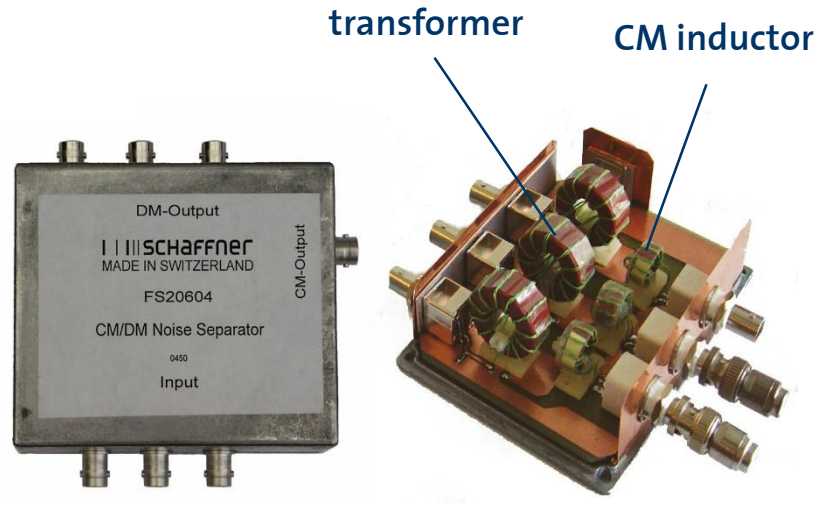
final measurement

EMI Input Filter Design

Three-phase Common / Differential Mode Separator

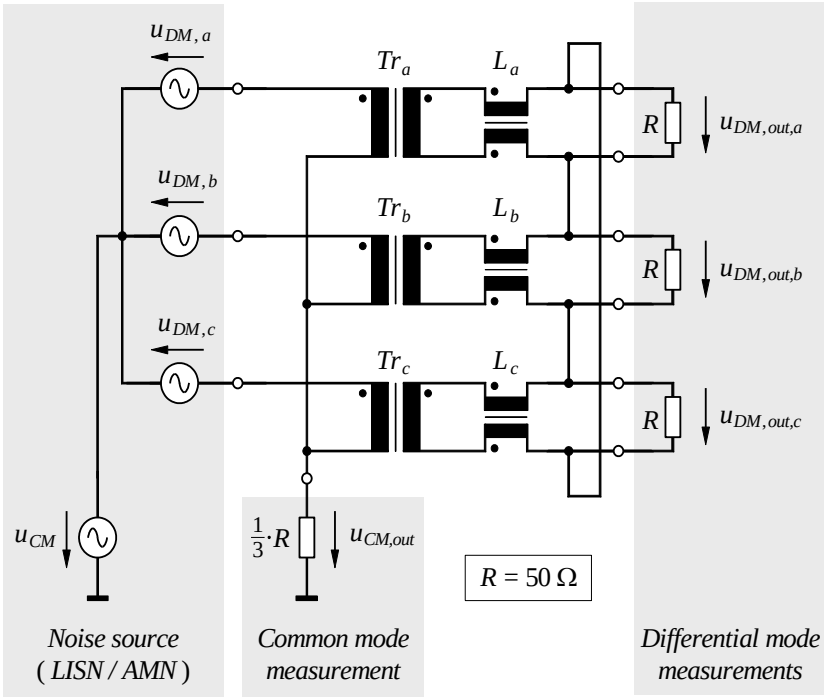
Function

- Allow the measurement of the different emission modes (DM and CM) in order to properly evaluate the performance of designed filters or in order to acquire the emissions information for a filter design.



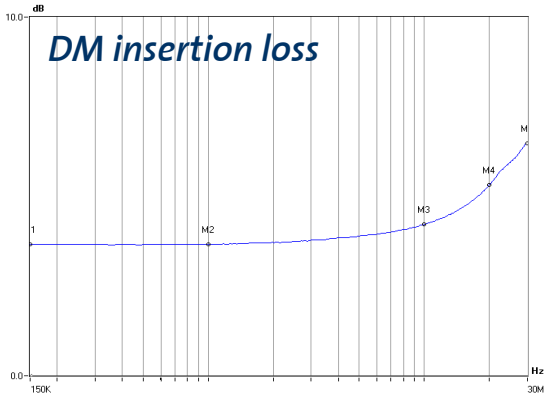
Dimensions: 12.0 x 9.5 x 5.7 cm (4.75x3.75x2.25 in.)

three-phase CM/DM separator basic schematic



EMI Input Filter Design

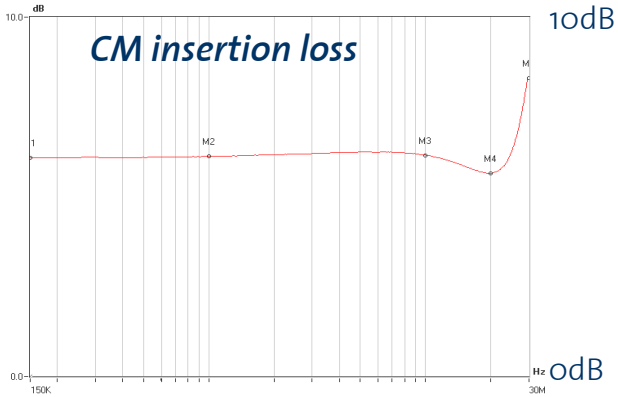
Three-phase Common / Differential Mode Separator



10dB

0dB

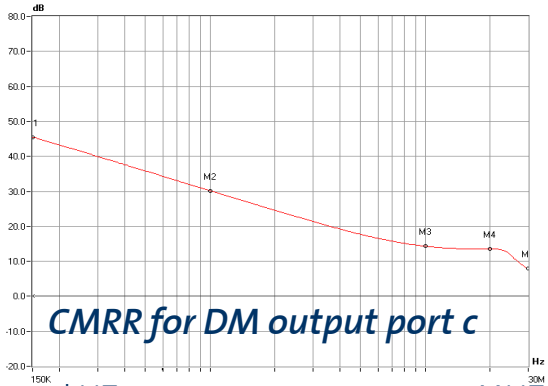
150kHZ 30MHZ



10dB

0dB

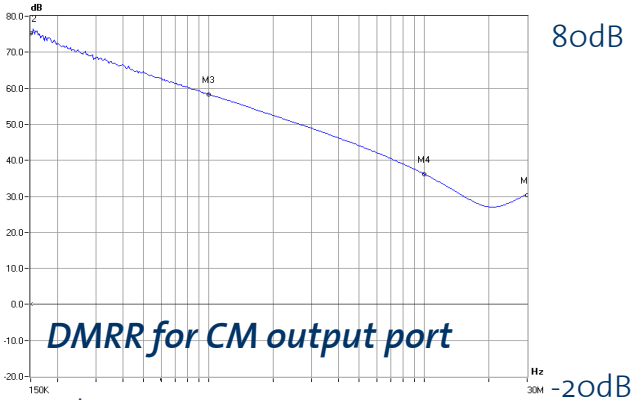
150kHZ 30MHZ



80dB

-20dB

150kHZ 30MHZ



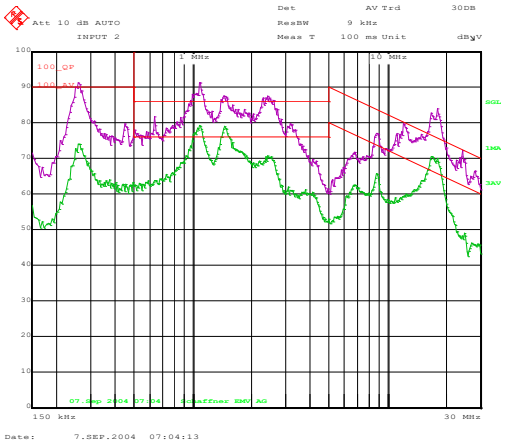
80dB

-20dB

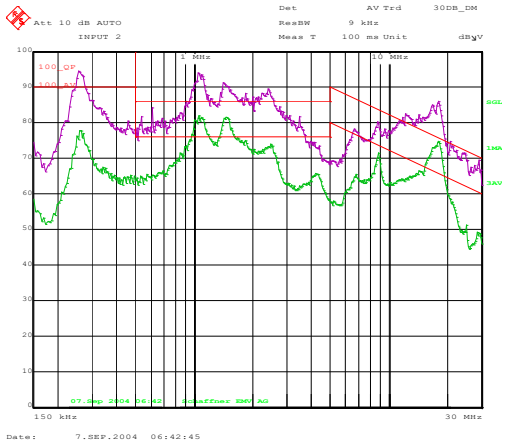
150kHZ 30MHZ

EMI Input Filter Design

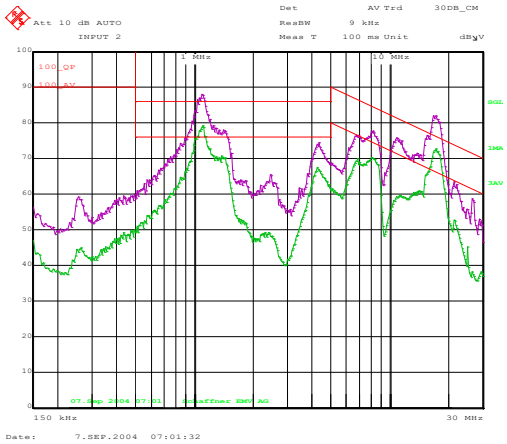
Three-phase Common / Differential Mode Separator



Direct LISN measurement

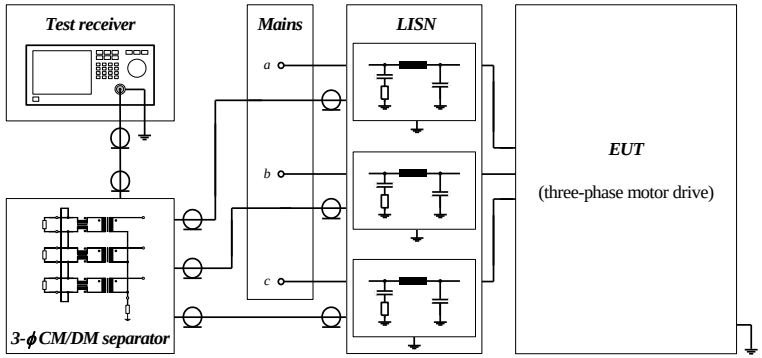


DM separator output



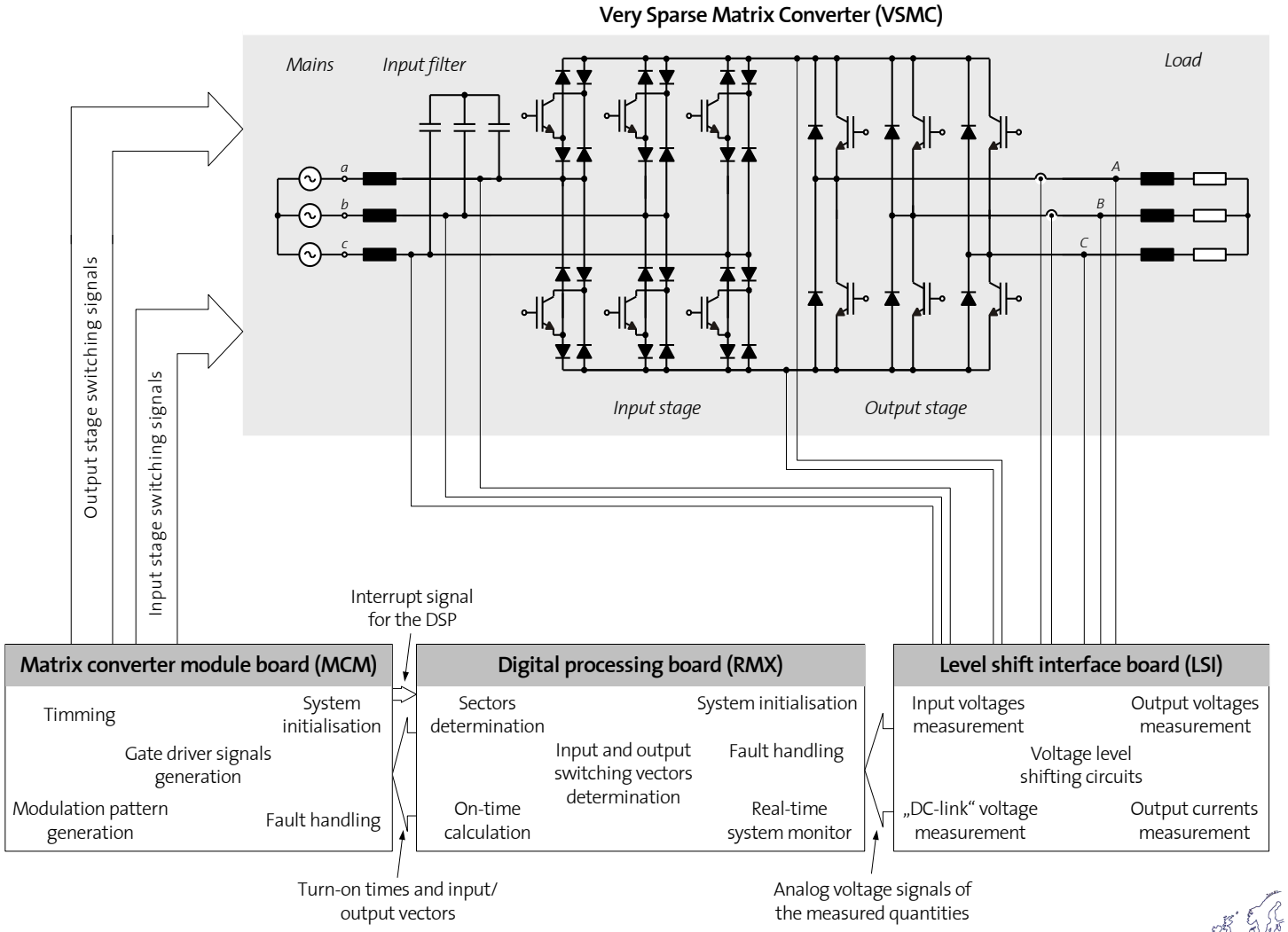
CM separator output

Test setup for the CE measurements



Digital Realization of the System Control

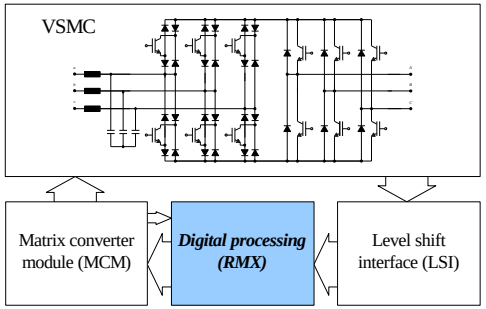
Functional diagram of the system control strategy

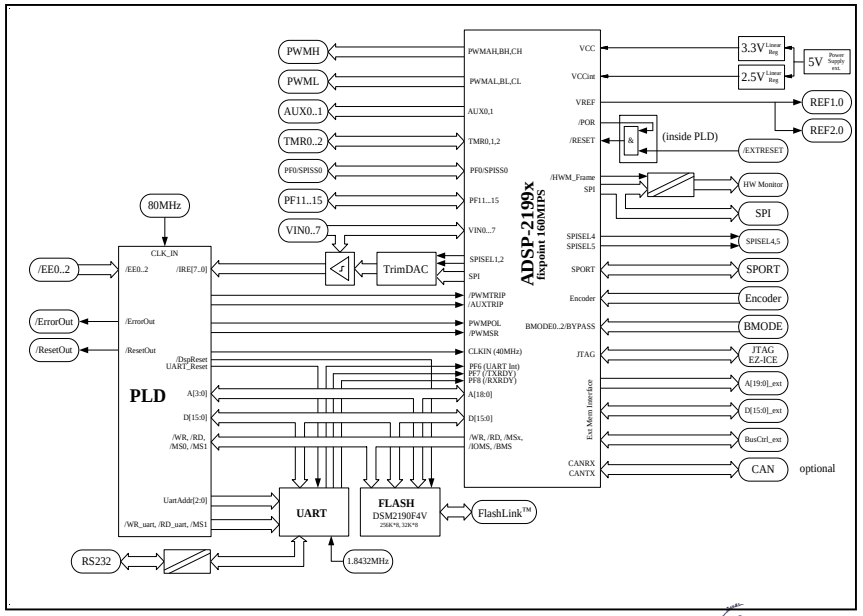


Digital Realization of the System Control

Digital Processing Board (RMX)

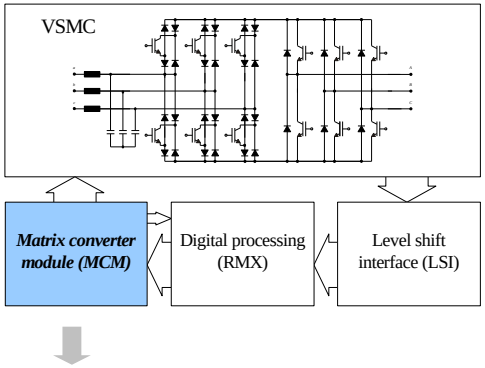
- 16-bit, fixed point DSP Core, up to 160 MIPS
- Built in Watchdog and Power On Reset Circuit
- 40K Words On chip RAM, Configured as 32K Words 24-bit Program RAM and 8K Words 16-bit Data RAM
- 288 KByte non-volatile Flash Memory, programmable via FlashLink™
- External Memory Interface
- 8-Channel, 20 MSPS, 14-bit Analog to Digital Converter
- Digitally configurable Trip Levels for each Ana-log Input Channel
- Three external Error Signal Inputs
- Three Phase 16-bit Center Based PWM Generation Unit with 12.5ns resolution
- Dual 16-bit Auxiliary PWM-Outputs
- SPI Communications Port with Master or Slave Operation
- Synchronous Serial Communications Port (SPORT)
- UART with auto-flow-control
- Three 32-bit Timers
- Ten General Purpose Flag I/O Pins
- 32-bit Encoder Interface Unit
- Optional Controller Area Network (CAN) Interface
- External Hardware Monitor and RS232 Interface
- JTAG Emulation Port
- Multiple Boot Modes
- 1.0V and 2.0V Voltage References
- 5 V Single Supply
- Extendable with individual Modules





Digital Realization of the System Control

Matrix Converter Module board (MCM)

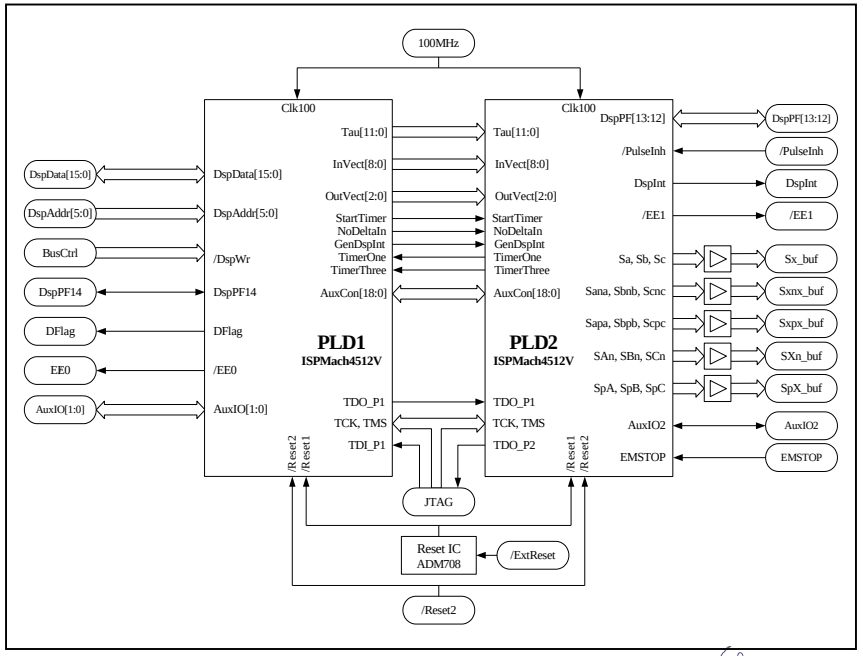


Function

- The translation from the turn-on times and switching vectors into PWM signals is the main function of this board.

Main features

- Two CPLDs running at 100 MHz
- Extension Module for the RMX DSP Controller Module
- Generation of PWM Signals for a Matrix Converter
- Buffered PWM Output
- Multiple PWM Generation Modes
- 5 V Single Supply



Digital Realization of the System Control

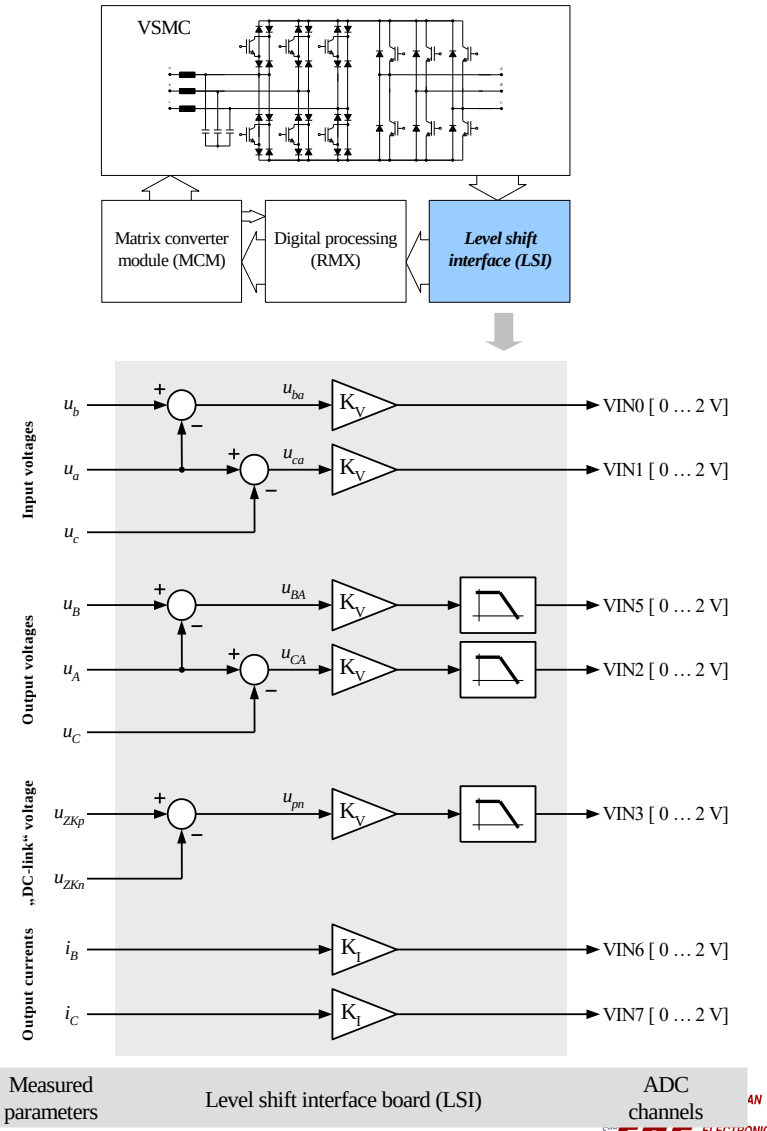
Level Shift Interface board (LSI)

Function

- Provide and interface between the electrical quantities in the power circuits and the ADC converters in the DSP board.

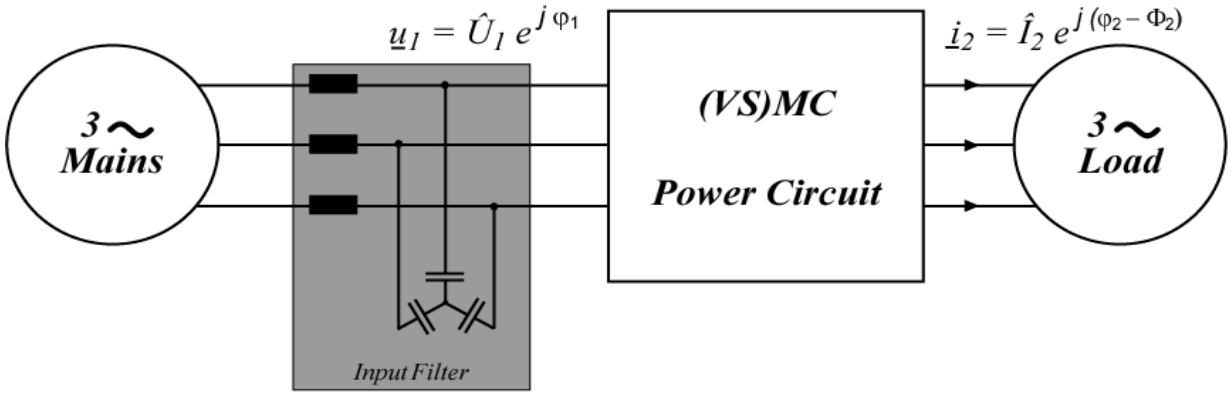
Main features

- Measurement of high voltages through simple resistors/operational amplifier dividers
- Voltages are not insulated (differential measurements)
- High frequency filtering is provided for the signals that present high frequency components
- The current transducers outputs have their signal levels adapted to the DSP levels

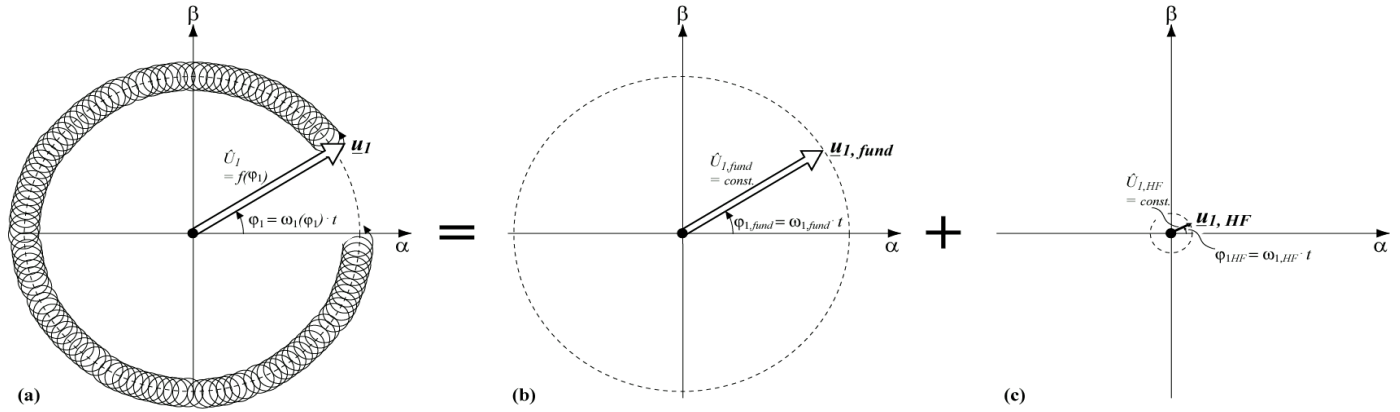


Active Input Filter Damping

Basic Situation



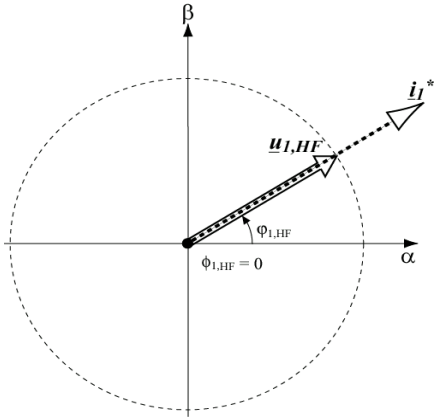
Space Vector Representation of Oscillating Filter Voltage



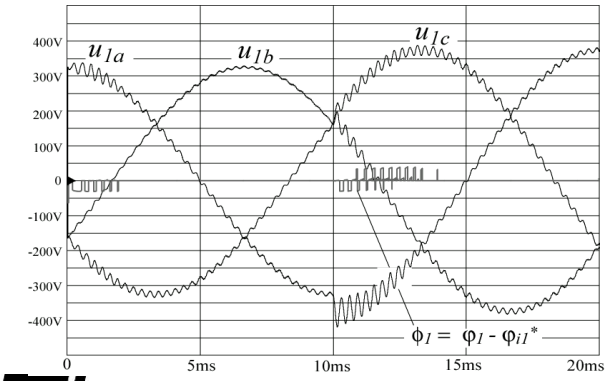
Active Input Filter Damping

1st Approach:

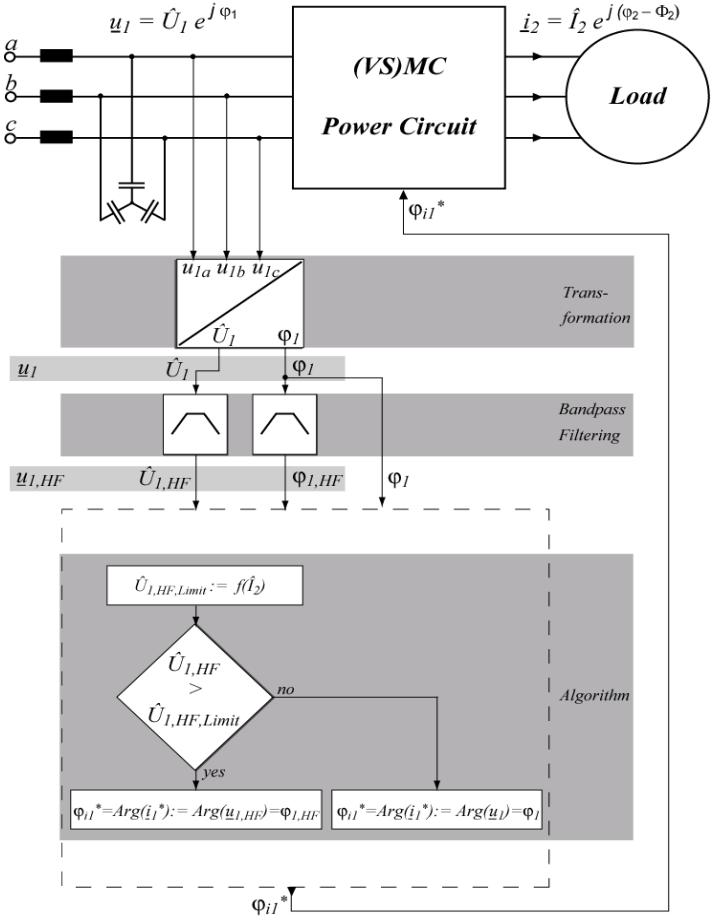
Active Damping by Ohmic HF Behavior at Power Circuit Input



Sim. for passively totally Undamped Filter @ $\hat{I}_2$ = 3A

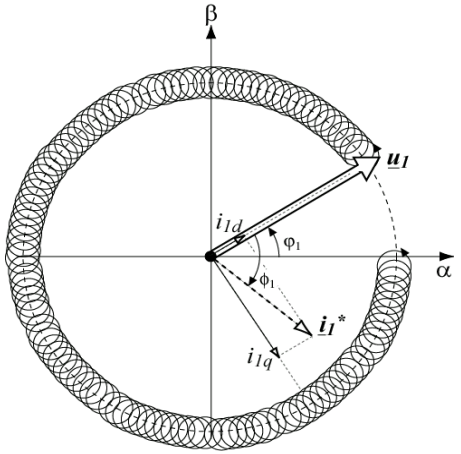


Control Implementation

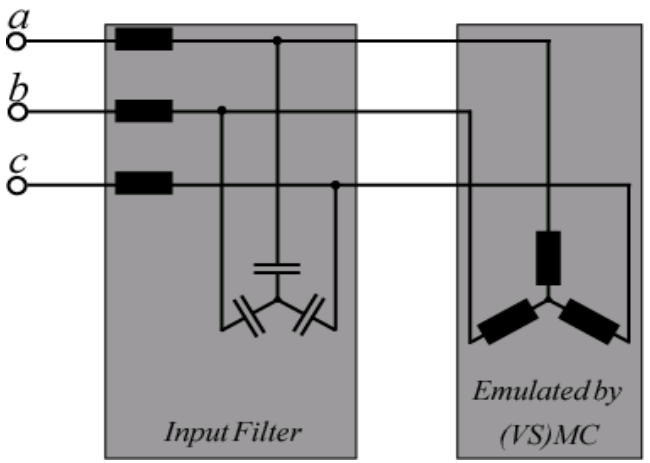


Active Input Filter Damping

2nd Approach:
Active Damping by
Inductive (Capacitive) Behavior
at Power Circuit Input

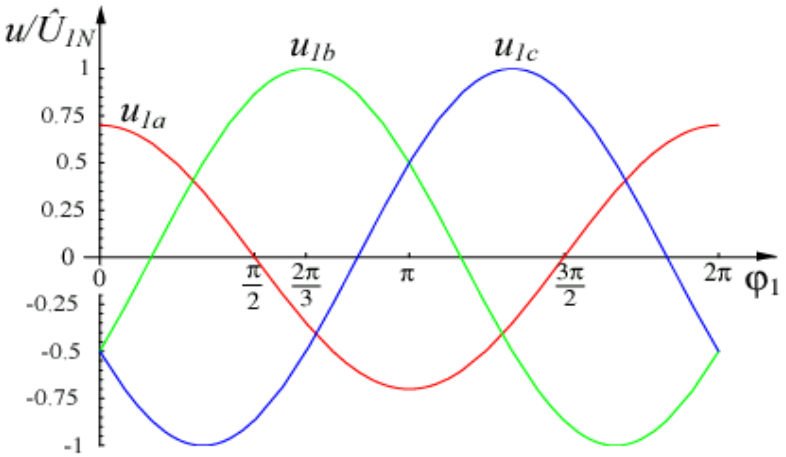


Principle

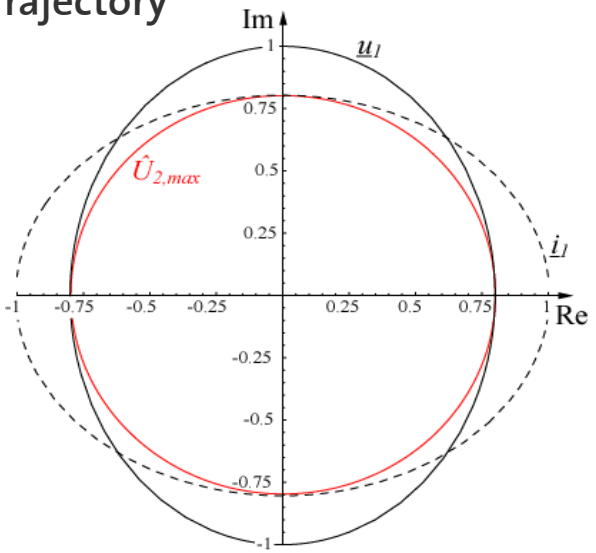


▶Compared to 1st Approach:
Reduced Effectiveness, but
Input Current- & Output Voltage Waveform Quality is fully Preserved

Unbalanced Mains



Trajectory



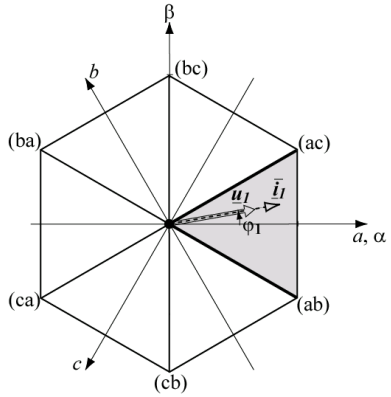
▶As long as $\hat{U}_2^* < \hat{U}_{2,max}$:
Even with Convential Modulation: Unbalanced Mains do Not Affect the Output Voltage System

The varying $\hat{U}_1(t)$ is Measured anyway & Compensated by Adaption of Modulation Index:

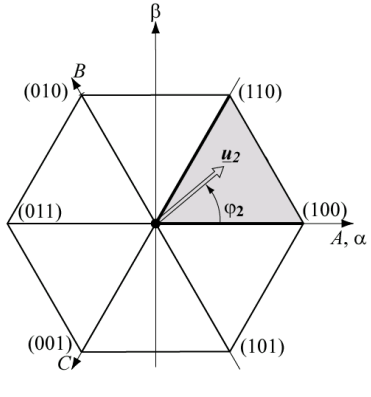
$$M_{12}(t) := \frac{2}{\sqrt{3}} \frac{\hat{U}_2^*}{\hat{U}_1(t)} \in [0...1]$$

Unbalanced Mains

Conventional Modulation



Input Stage



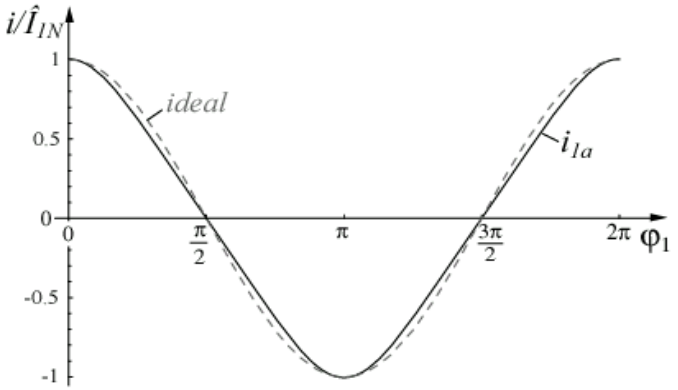
Output Stage

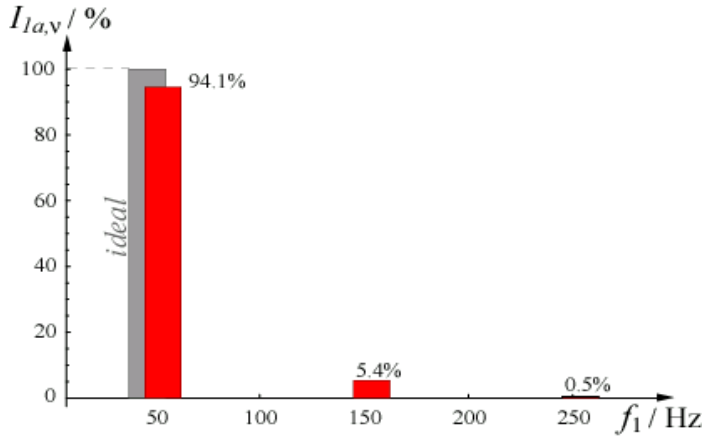
- Relative Turn-On Times

$$d_{ab} = \cos(\varphi_1 + \pi/3)$$
$$d_{ac} = \cos(\varphi_1 - \pi/3)$$
$$\delta_{(100)} = M_{12} \cdot \cos(\varphi_2 + \pi/6)$$
$$\delta_{(110)} = M_{12} \cdot \sin(\varphi_2)$$

$$\delta_{(100),ac} = d_{ac} \cdot \delta_{(100)}$$
$$\delta_{(110),ac} = d_{ac} \cdot \delta_{(110)}$$
$$\delta_{(110),ab} = d_{ab} \cdot \delta_{(110)}$$
$$\delta_{(100),ab} = d_{ab} \cdot \delta_{(100)}$$

Input Current Waveform & Spectrum





▶ But: Conv. Modulation generates a 3rd Order Harmonic in the Input Current

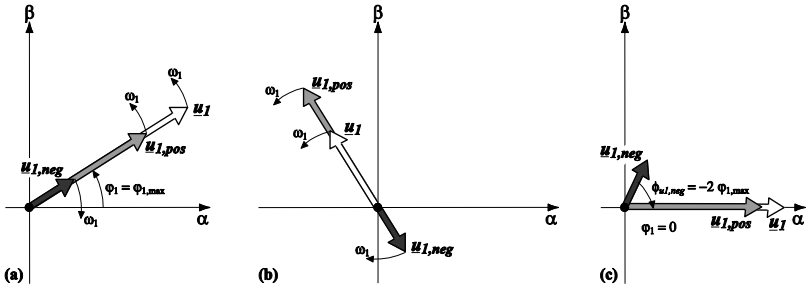
Unbalanced Mains

Improved Modulation

▶Set the desired Active Power Constant

$$p^* = 2\frac{\hat{U}_{1,\max}\cdot\hat{U}_{1,\min}}{\hat{U}_{1,\max}+\hat{U}_{1,\min}}$$

$$q^* = -(\hat{U}_{1,\max}-\hat{U}_{1,\min})\cdot\sin(2\varphi_1+\phi_{u1,neg})$$

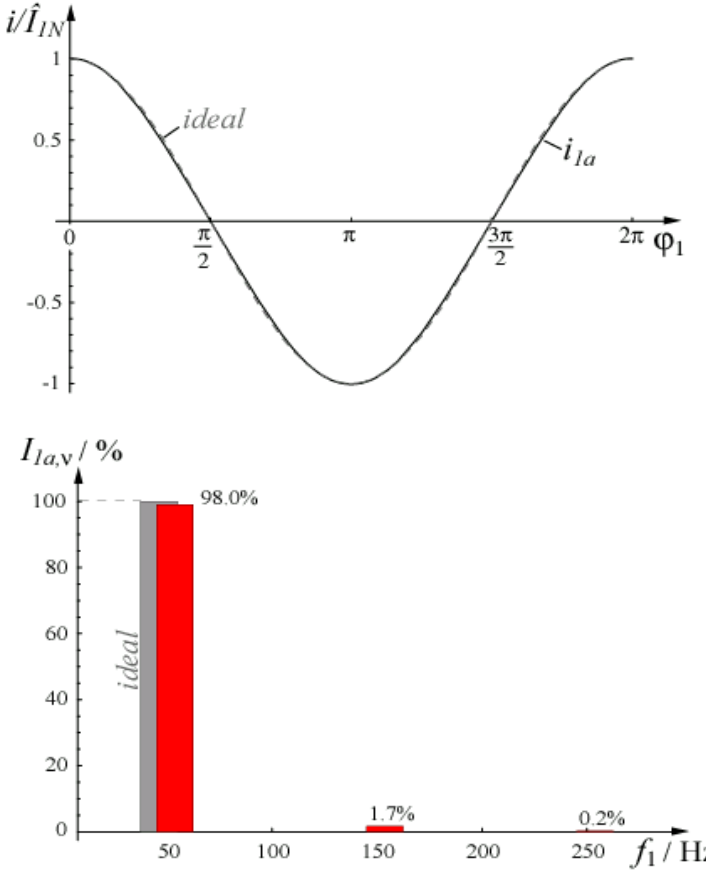


- Adapted Input Values for Conv. Modulation

$$\varphi_{i1}{}^* := \varphi_1 - \phi_{i1,pos} = \arctan\left(\frac{p^* u_{1\beta} - q^* u_{1\alpha}}{p^* u_{1\alpha} + q^* u_{1\beta}}\right)$$

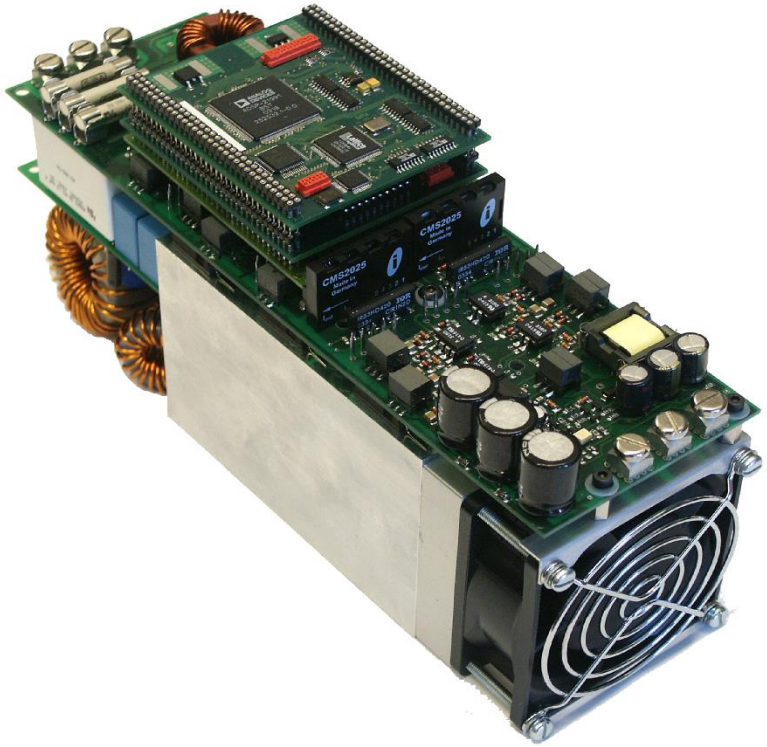
$$M_{12}{}^* = \frac{2}{\sqrt{3}}\cdot\frac{\hat{U}_2{}^*}{\hat{U}_1{}^*}\cdot\frac{1}{\cos(\phi_{i1,pos})}$$

Improved Input Current Waveform & Spectrum



Experimental Analysis / Operating Characteristics

IGBT-VSMC prototype



Input (3~AC)

Input RMS line voltages (U1)	3 x 400 V +15/- 20%
Maximum input RMS current	$I_{1,max}$ = 13 A
Mains frequency	f_1 = 50 Hz
Current displacement angle	ϕ_1 = 0°

Output (3~AC)

Output RMS line voltages (U2)	3 x 0 – 340 V
Maximum output power	S_2 = 6.8 kVA
Output frequency	f_2 = 0 – 500 Hz
Current displacement angle	ϕ_2 = 0° – 90°

Switching frequency: f_p = 20/40 kHz

Power stage topology: Very Sparse Matrix Converter

Power switches technology: Si IGBTs + fast recovery Si diodes

Approximate dimensions: Power part: 240 x 200 x 85 mm
Control part: 90 x 80 x 40 mm

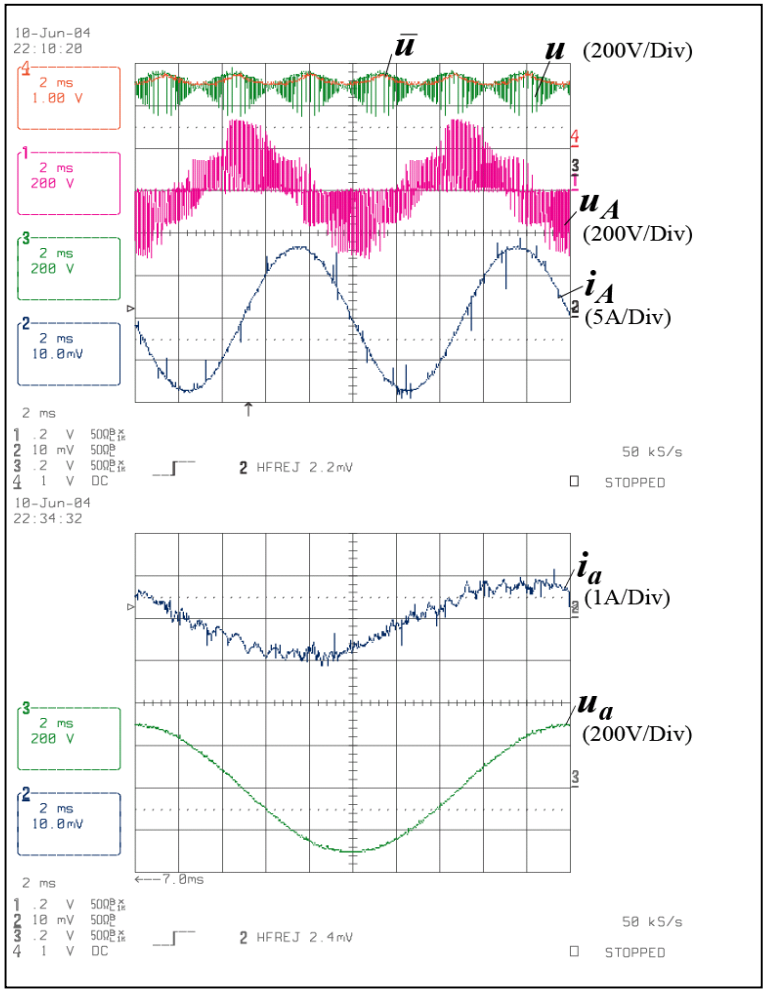
Approximate weight: Power part: 3100 g
Control part: 200 g

Experimental Analysis / Operating Characteristics

IGBT-VSMC measurements – active power transfer

Operating conditions

- V_{in} (RMS) = 230 V
- f_2 = 100 Hz
- M = 0.5
- $f_1 \approx 0°$
- $\measuredangle_2 = 90°$
- Modulation: ***Conventional (HV)***

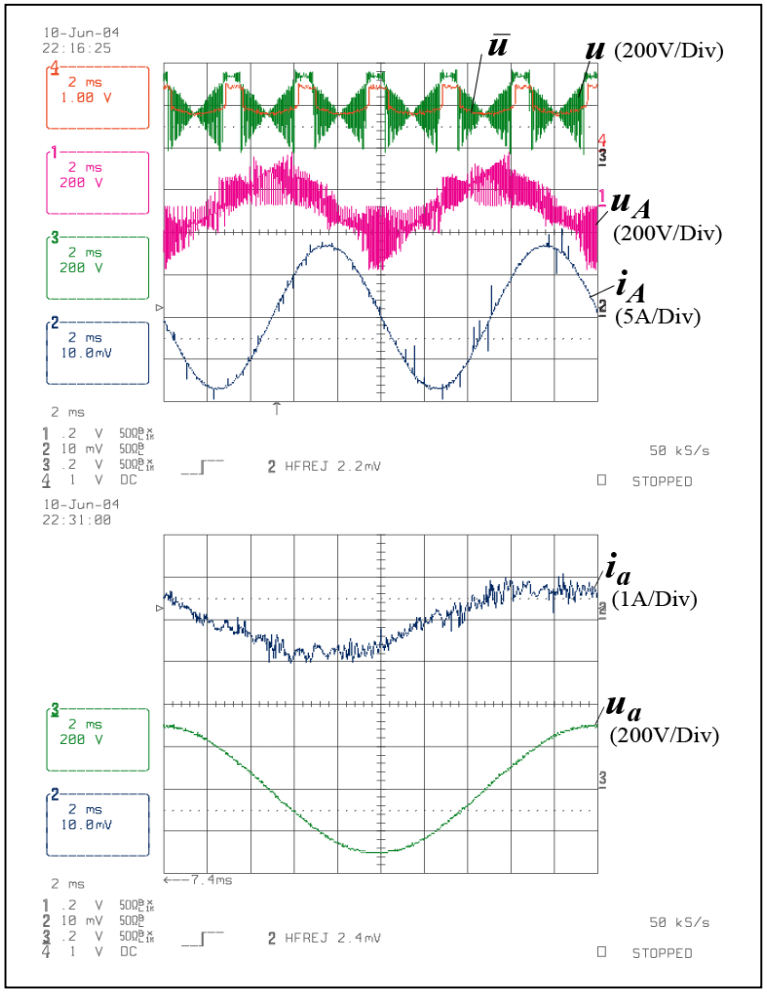


Experimental Analysis / Operating Characteristics

IGBT-VSMC measurements – active power transfer

Operating conditions

- V_{in} (RMS) = 230 V
- f_2 = 100 Hz
- M = 0.3
- $f_1 \approx 0°$
- $\measuredangle_2 = 90°$
- Modulation: ***Low Output Voltage (LV)***

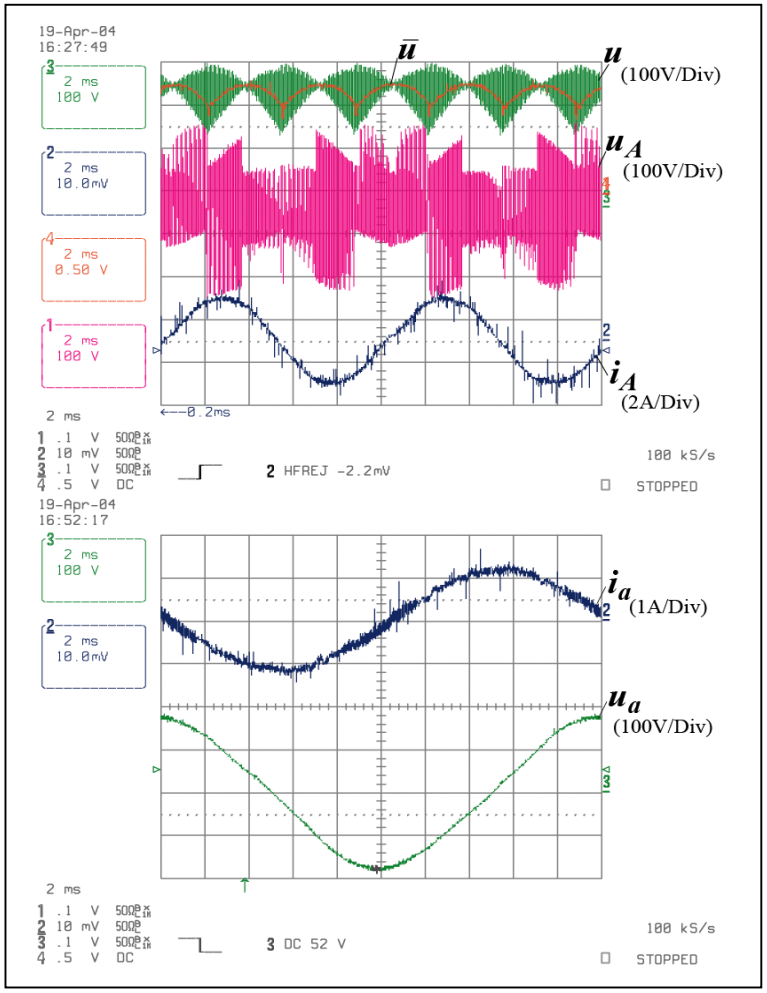


Experimental Analysis / Operating Characteristics

IGBT-VSMC measurements – reactive power coupling

Operating conditions

- V_{in} (RMS) = 120 V
- f_2 = 100 Hz
- M = 0.2
- MI = 0.38
- $\measuredangle_1$ = -90°
- f_2 = 90°
- Modulation: ***RPC I***



Coffee Break…

Comparison to Four-Quadrant Voltage DC Link Converter Systems

Marcelo L. Heldwein and Frank Schafmeister

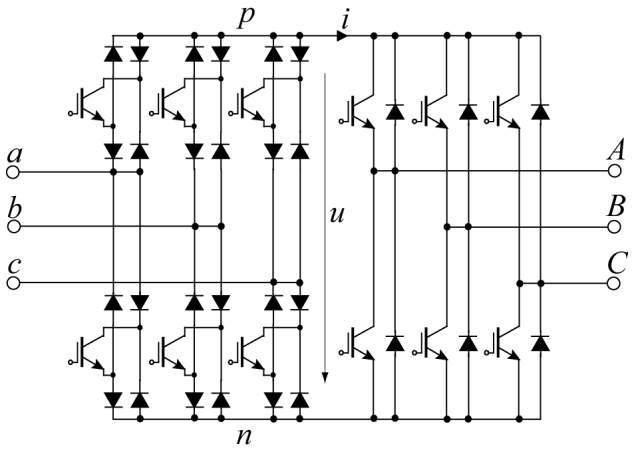
- **Comparison of the Realization Effort**
  Assumptions, design and losses
- **Losses and Efficiency dependent on Operating Point**
  Theoretical limits
- **Power density**
  Physical layout, photographs, dimensions and power density
- **EMI Filtering Effort**
  Design procedure, components, structure and volume

Comparison of the Realization Effort

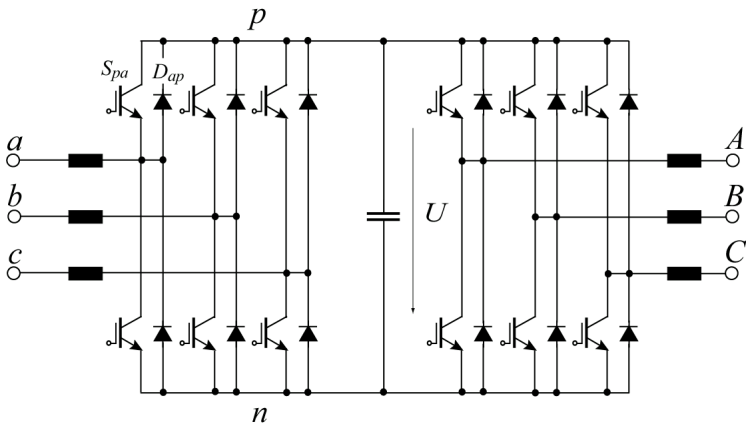
Specifications

Input (3~AC)	400 V, +10%, -15%, 50 Hz
Output (3~AC)	S_2 = 6.8 kVA @ T_{amb} = 45°C
Switching frequency	*SMC*: Input f_p = 20 kHz / Output f_p = 40 kHz *BBC*: Input f_p = 40 kHz / Output f_p = 40 kHz
Dynamic Modulation Margin	ΔM_{min} = 5%
Load	PM Synchronous Motor (PMSM)

VSMC (Very Sparse Matrix Converter)



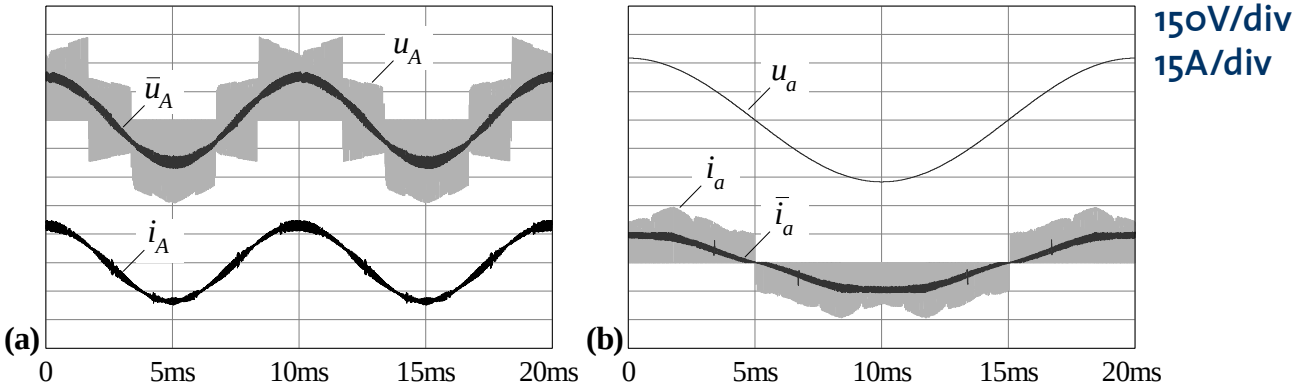
BBC (Back-To-Back Converter)



Comparison of the Realization Effort

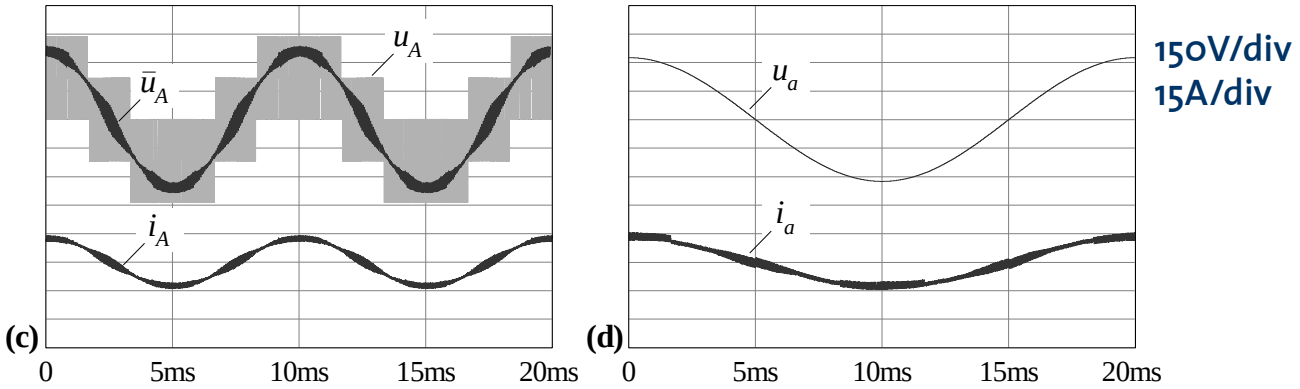
Nominal Point (6.8kW)

VSMC



150V/div
15A/div

BBC



150V/div
15A/div

BBC: - constant DC Bus Voltage at Higher Level (boostable even higher)
- lower Output Currents due to Higher Output Voltage Level

Comparison of the Realization Effort

Approach for an unbiased comparison

Ideally designed motors for each of the topologies

VSMC

$$U_{2,N} = \frac{\sqrt{3}}{2}(1-\Delta M_{\min})\cdot U_{1,\min} = 280V$$

$$I_{2,N} = \frac{P_{2N}}{\sqrt{3}\cdot U_{2,N}} = 14A$$

BBC

$$U_{dc} = (1+\Delta M_{\min})\cdot\sqrt{2}\cdot U_{1,\max} \approx 655V$$

$$U_{2,N} = (1-\Delta M_{\min})\cdot\frac{1}{\sqrt{2}}U_{dc} = U_{1,\max} = 440V$$

$$I_{2,N} = 8.9A$$

U_1 : Input RMS voltage
U_2 : Output RMS voltage
U_{dc} : DC-link voltage
I_1 : Input RMS current
I_2 : Output RMS current
P_2 : Output power

Additionally to these assumptions the BBC DC-link capacitor is minimized

Comparison of the Realization Effort

Choice of the DC-link capacitor for the BBC

$$C_{DC-link,\min} = \frac{L_{in} \cdot P_2^2 \left[\left(E_{dc} - U_{dc}\right)^2 - \left(E_{dc} + U_{dc}\right)^2 \right]}{E_{dc}^2 \cdot U_{dc}^2 \left(\left(\min(u_{dc}) + E_{dc}\right)^2 - \left(U_{dc} + E_{dc}\right)^2 \right)}$$

E_{dc} : Peak input voltage
U_{dc} : DC-link voltage
L_{in} : Boost inductor
U_1 : Input RMS voltage
$i_{1,ripple}$: Input current ripple, peak-to-peak

$$C_{DC-link,\min} \cong 31\mu F$$

Ref.: A. Carlsson, "The back-to-back converter", Masters Thesis; Lund Institute of Technology; Lund, Sweden; (1998)

The capacitor is chosen so that the voltage does not fall below a defined minimum value during the transient from full regeneration to full motoring mode

Choice of the boost inductor for the BBC

$$L_{in,\min} = \frac{U_1 / \sqrt{3}}{2 \cdot \sqrt{6} \cdot f_P \cdot i_{1,ripple}}$$

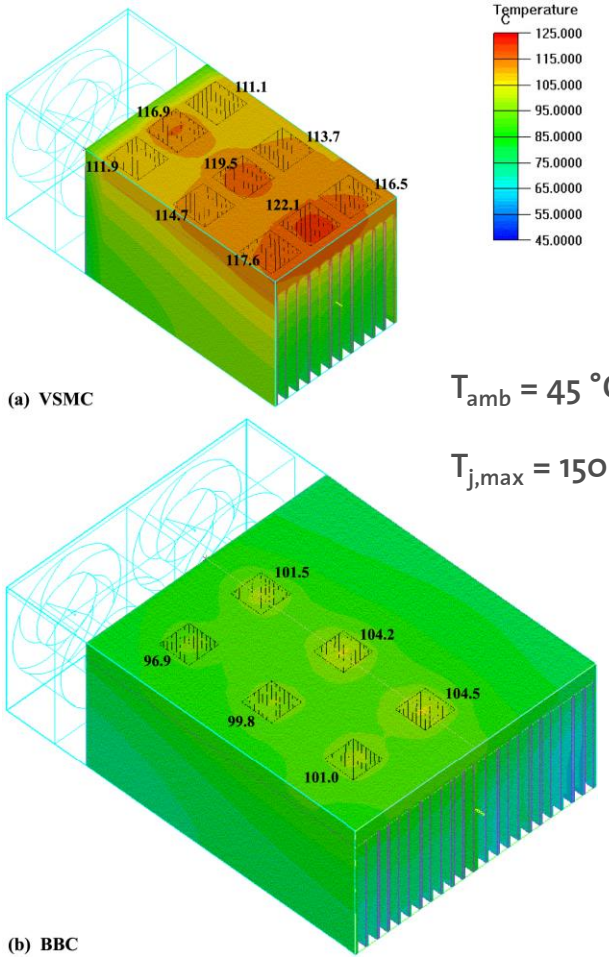
$$L_{in,\min} \cong 1mH$$

The inductor is chosen so that the current ripple at the switching frequency is lower than 20% of the peak input current

Comparison of the Realization Effort

Thermal simulation and main components

BBC requires larger heat sink

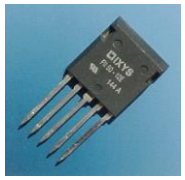


T_{amb} = 45 °C

$T_{j,max}$ = 150 °C

Description		BBC		Very Sparse Matrix
Semicond. Input	3	IXYS FII 50-12E	6	IXYS FIO 50-12BD
Semicond. Output	3	IXYS FIO 50-12E	3	IXYS FII 50-12E
Boost Inductor	3	1mH (toroidal)		Not used
DC-Link Cap.	4	8µF, foil, 400V_{AC}		Not used

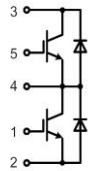
IXYS FIO 50-12E

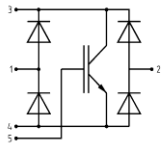


IXYS FIO 50-12BD

$R_{th,diodes}$ = 1.3 °C/W

$R_{th,IGBTs}$ = 0.6 °C/W

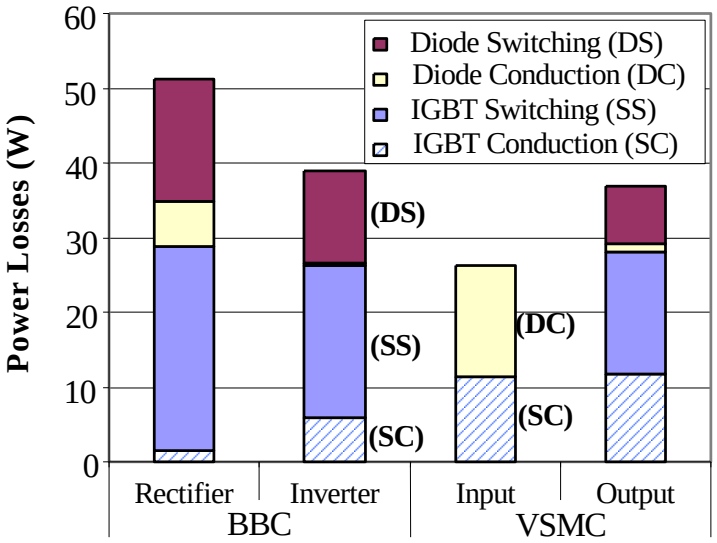




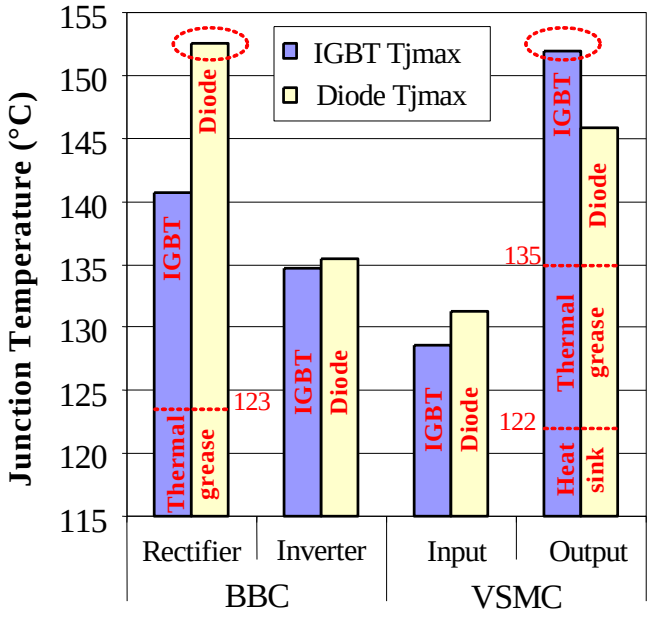
Comparison of the Realization Effort

Losses and thermal limits comparison (@ rated load and nominal input voltage)

Losses distribution



Junction temperatures



VSMC: No Sw. Losses in Input Stage
BBC: Sw. Losses are Dominant in both Stages

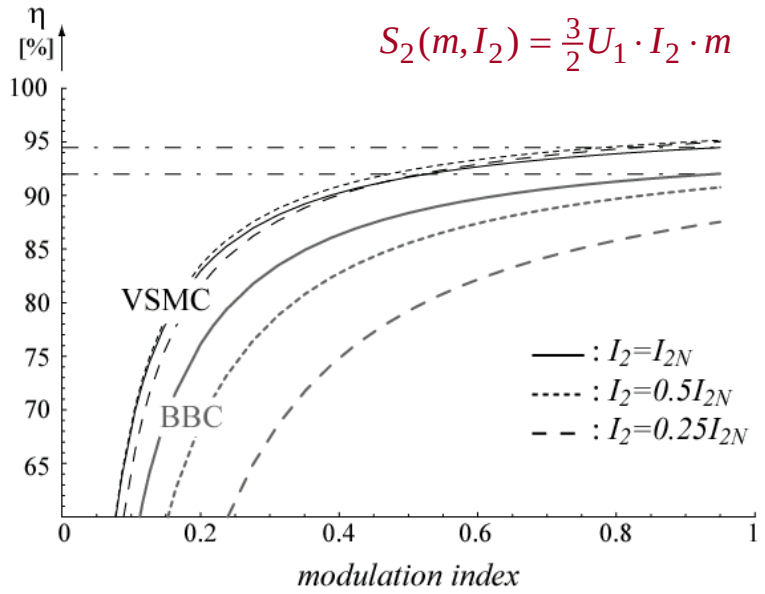
Limiting Device VSMC: *Output IGBT*
Limiting Device BBC: *Rectifier Diode*

Losses and Efficiency dependent on Operating Point

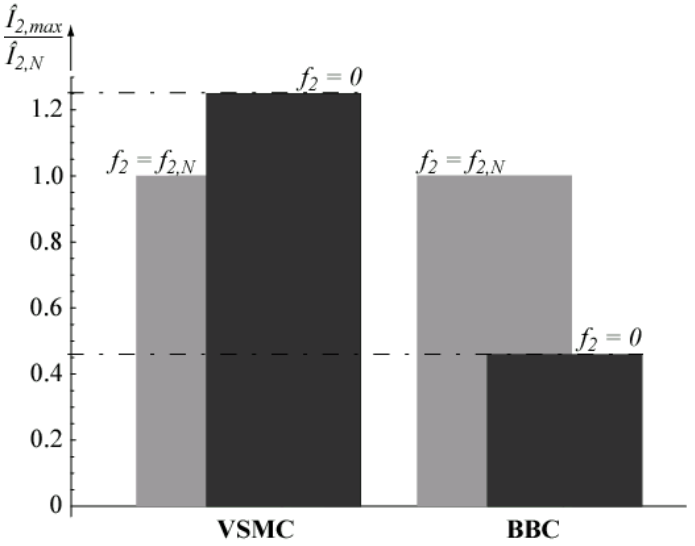
Efficiency

$$\eta = 1 - \frac{P_{Loss}(m, I_2)}{S_2(m, I_2)}$$

$$S_2(m, I_2) = \frac{3}{2} U_1 \cdot I_2 \cdot m$$



Max. Output Current for f_2=0 (Standstill, Most Critical OP)



Due to Special **Modulation Strategies**

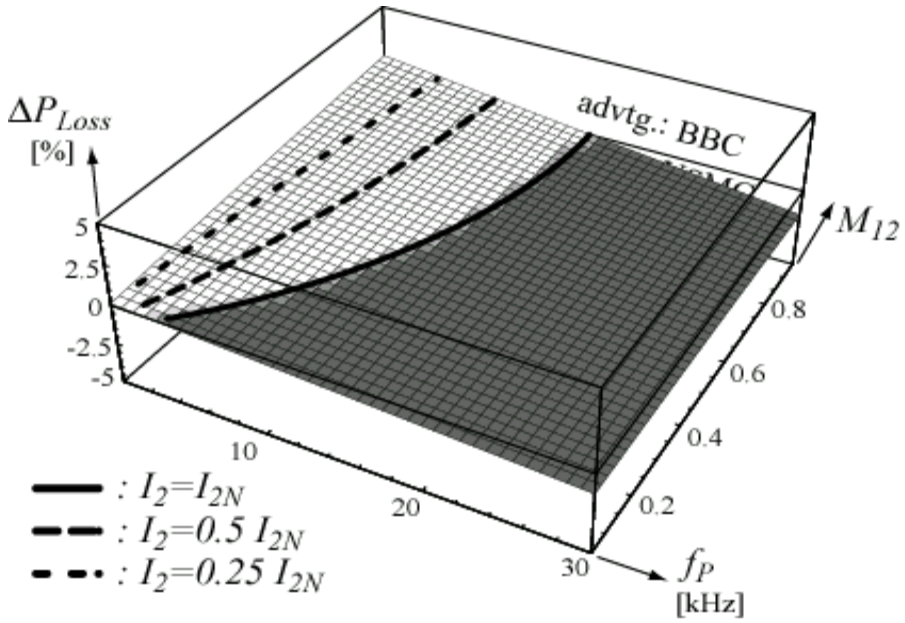
VSMC: Max. Eff.: 94.5 @ Full Modul.
BBC: Max. Eff.: 92.0 @ Full Modul.

VSMC: Max. O.Curr. Ampl.: 1.25 $\hat{I}_{2,N}$
BBC: Max. O. Curr. Ampl.: 0.46 $\hat{I}_{2,N}$

VSMC vs. BBC – Relative Loss Difference in Dependency on Load Condition & f_p

Under Rated Load Condition the critical f_p is about 14kHz

- VSMC is advantageous in Efficiency within Whole Speed-Torque-Plane beyond 14kHz



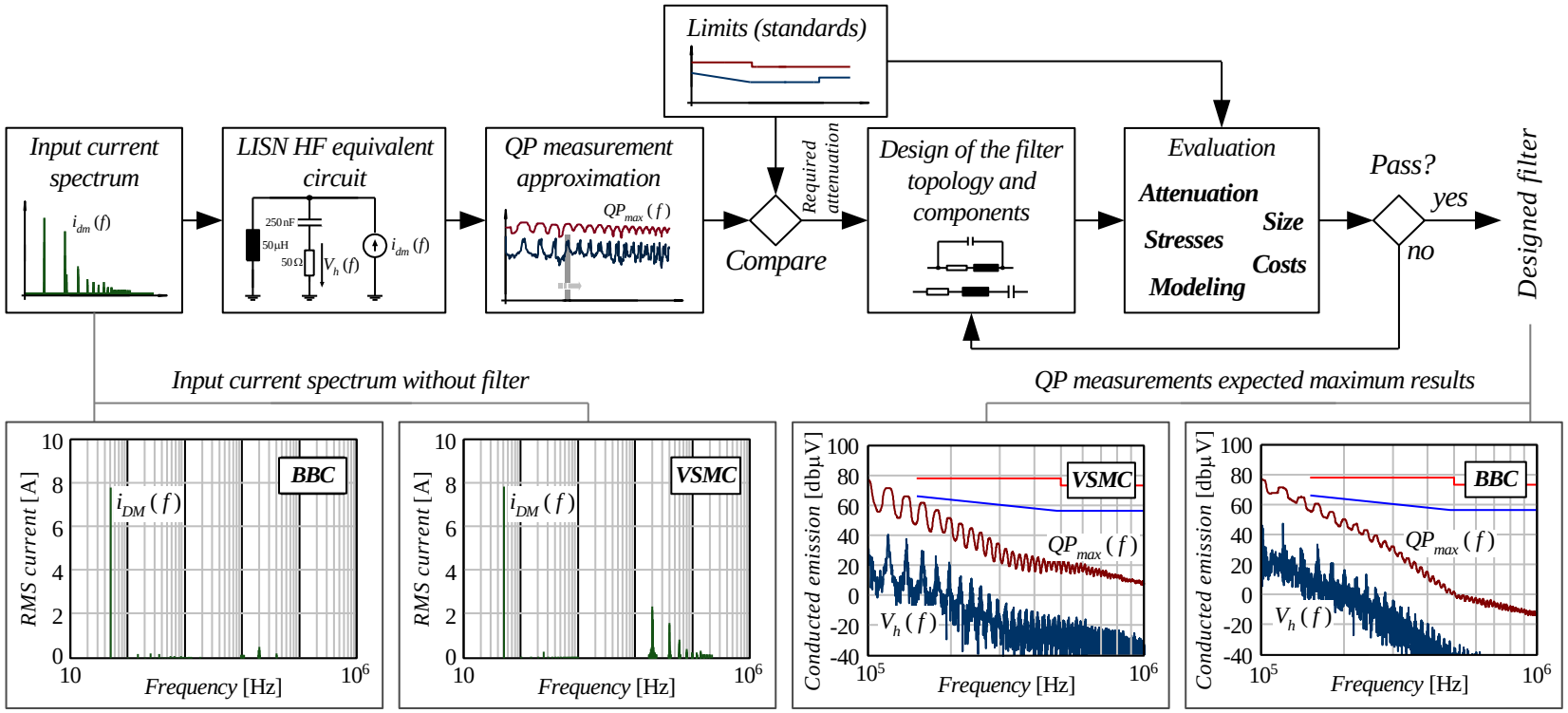
Advantageous Applications

- Appl. requiring Output Filter
- Low Inductance Motors
- Aircraft Appl. (400Hz – 800Hz)

$$\Delta P_{Loss} = (P_{Loss,VSMC} - P_{Loss,BBC}) / P_{2N}$$

EMI Filtering Effort

Design procedure



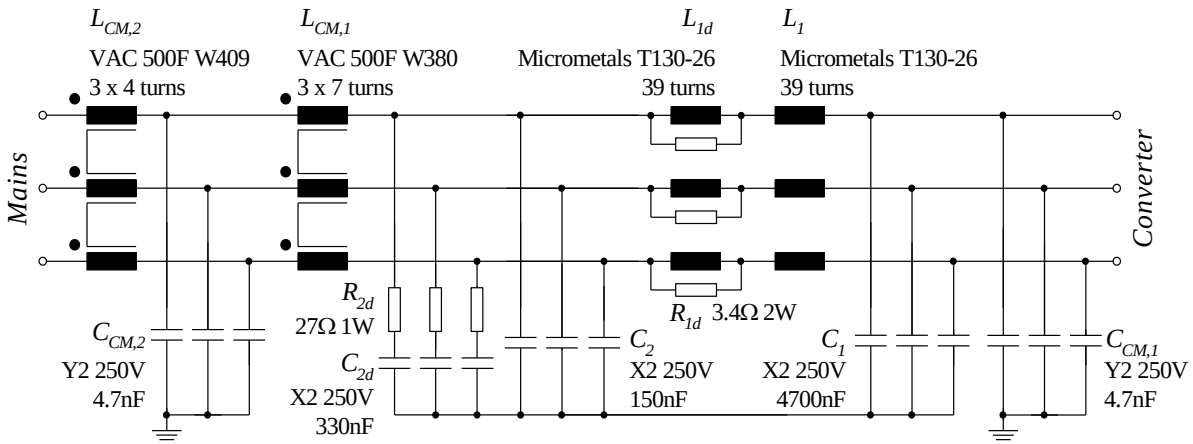
EMI Filtering Effort

Comparison

	Back-to-back	VSMC
Total DM capacitance (for all three-phases)	15.54 mF	36 mF
Total DM inductance (10 kHz)	1.20 mH	1.29 mH
Total CM capacitance	28.2 nF	28.2 nF
Total CM inductance (10 kHz)	36 mH	36 mH
Total filter components volume	325 cm³	360 cm³

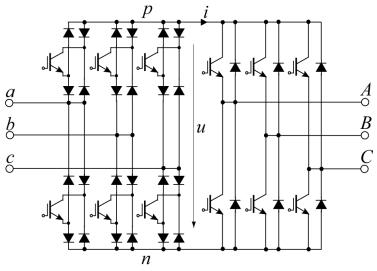
Filter volume for the VSMC is 10% larger

Filter structure for the BBC



Power density

VSMC

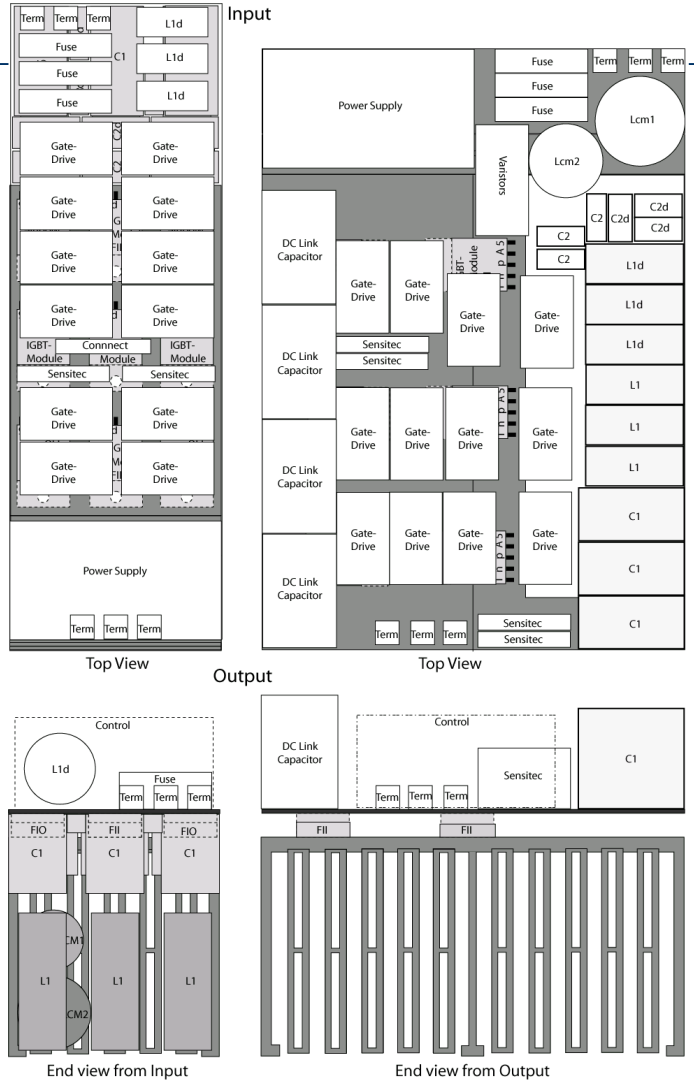


Dimensions:

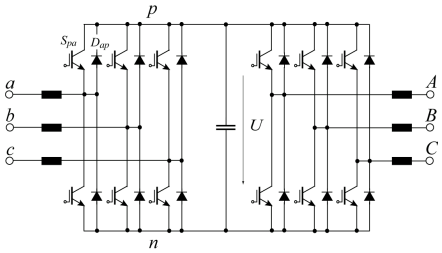
L	26.2 cm
W	8.0 cm
H	11.5 cm

Volume:

approx. 2.4 liters



BBC



Dimensions:

L	22.7 cm
W	16.0 cm
H	13.4 cm

Volume:

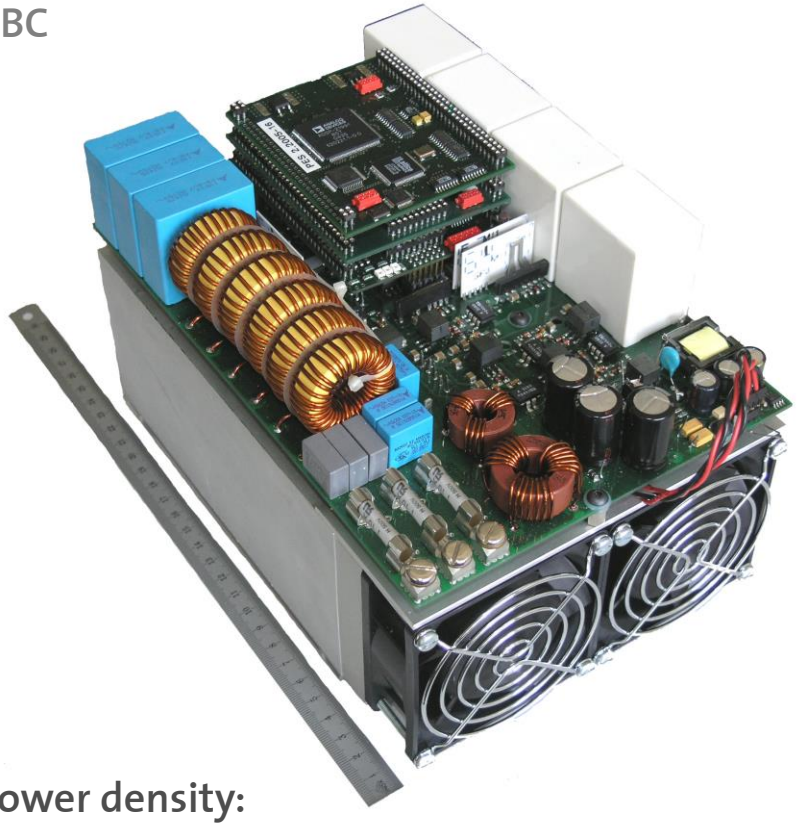
approx. 4.6 liters

Power density

Unbiased Comparison VSMC – BBC

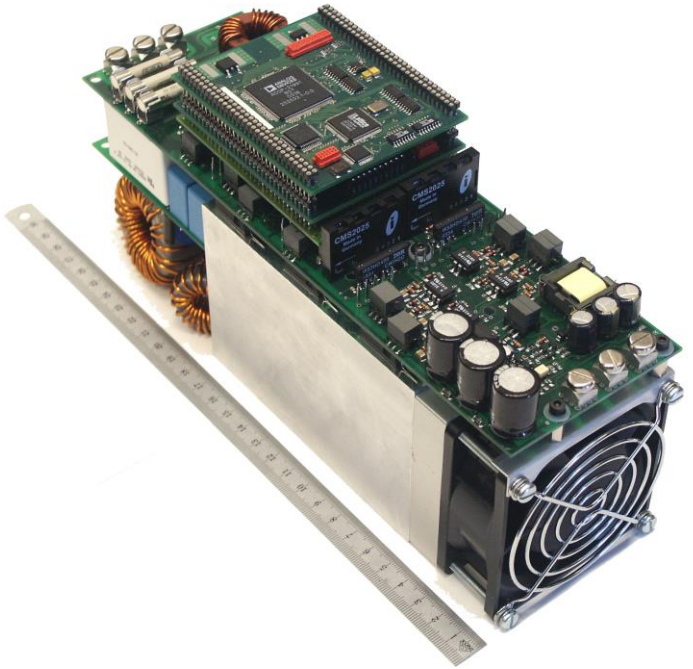
6.8kVA, 340V – 440V, Specially designed PMSM for BBC and VSMC

BBC



Power density:
approx. 1.5 kVA/liters

VSMC



Power density:
approx. 2.8 kVA/liters

Matrix Converter – Future Developments

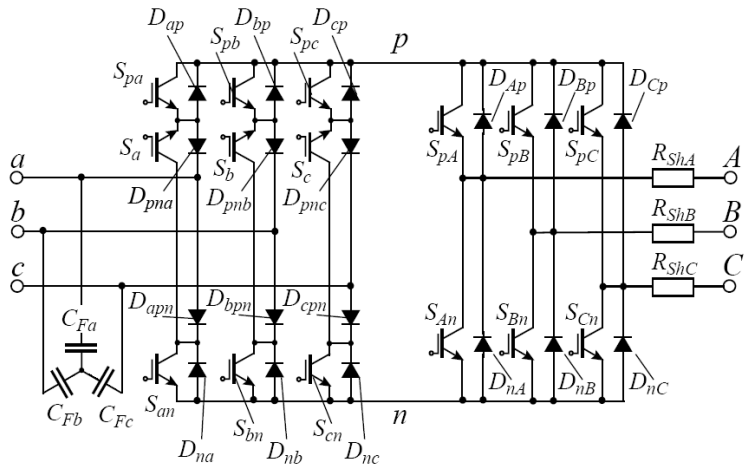
Marcelo L. Heldwein and Johann W. Kolar

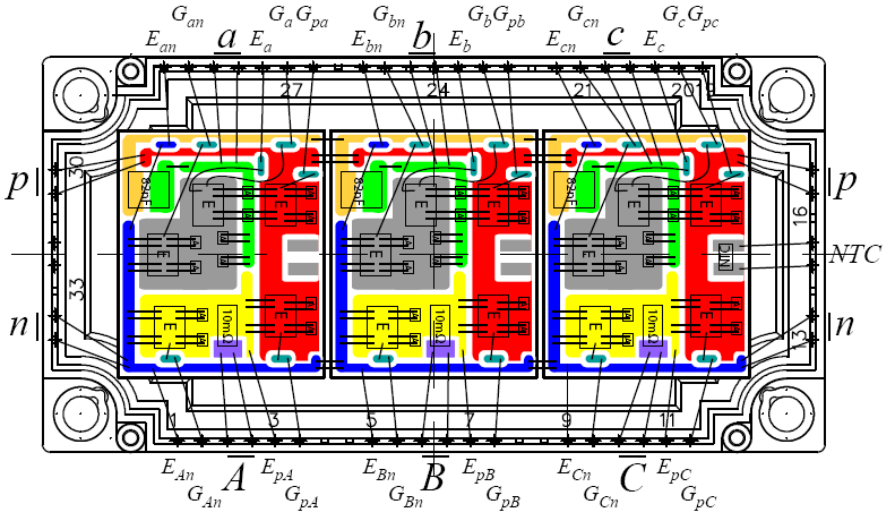
- SMC power module
  - SMC and BBC modules
- Status of power switches
  - IGBTs, Reverse Blocking IGBTs and SiC switches
  - Design examples with RB-IGBTs and SiC JFETs
- Status of industrial products
  - Yaskawa's CMC
- Potential Future Application Areas
- Alternative topologies

SMC Power Module

Design of Power Module using Si IGBTs and SiC Diodes

Fabrication is the next step





EconoPACK™ 3

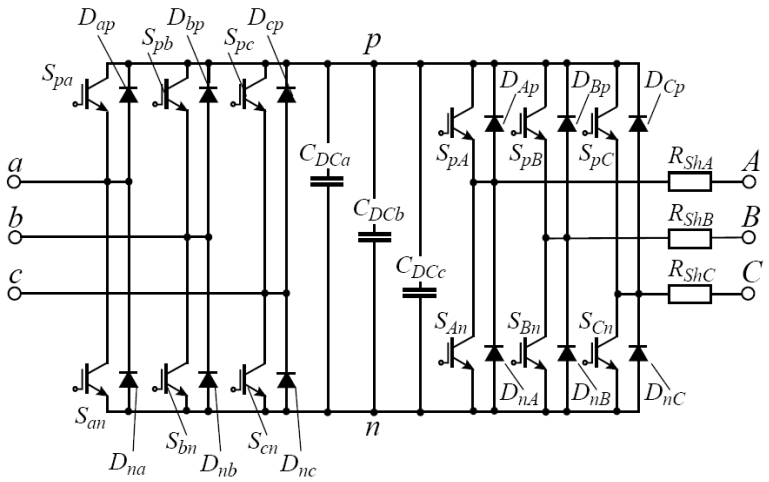
Dimensions: 122 x 62 x 20 mm

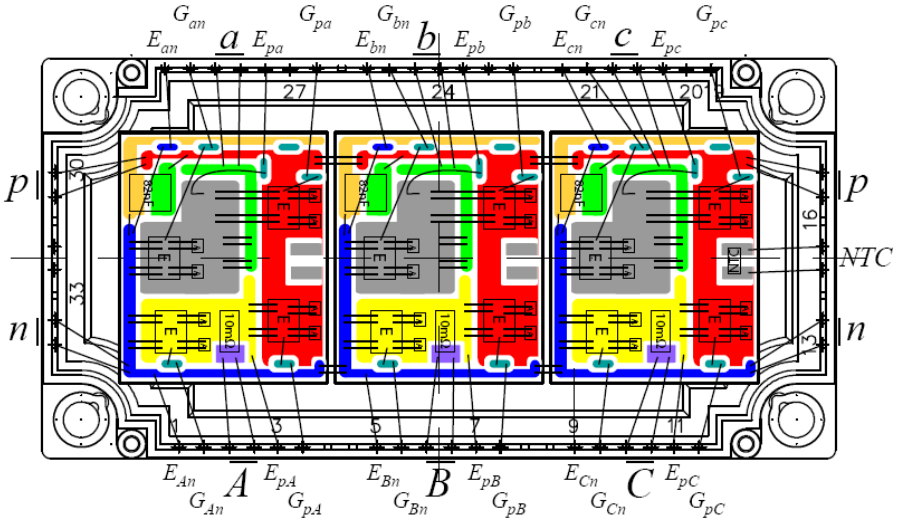
The module integrates also:
- Part of the input filter capacitors
- Phase current resistive sensors
- Temperature sensors (NTC)

BBC Power Module

Design of Back-to-Back Power Module

Fabrication is the next step





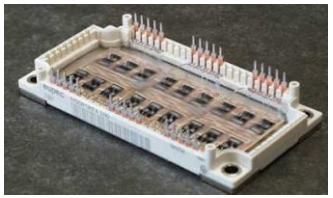
EconoPACK™ 3

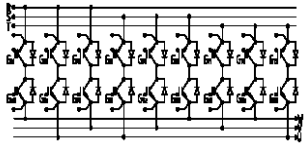
Dimensions: 122 x 62 x 20 mm

The module integrates also:
- Part of the DC-link capacitors
- Phase current resistive sensors
- Temperature sensors (NTC)

Status of Power Semiconductor Technologies

IGBT technology

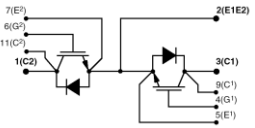




- Complete CMC module
- CMC prototype built by SIEMENS/EUPEC (7.5kW/400V)
- Layout advantages for a CMC
- Compact design
- 35 A / 1.2 kV devices

EUPEC module EconoMAC

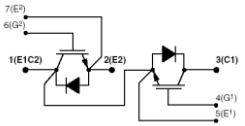
www.eupec.com



- High power matrix converters
- Can also be used in the input stage of IMC / SMC
- 200 A / 1.2 kV devices
- *Switching energy* @ Tc=125°C:
  $E_{t\text{-}off}$ = 20mJ
  $E_{t\text{-}on}$ = 25mJ
  E_{rr} = 13mJ

DYNEX bi-directional DIM200MBS12

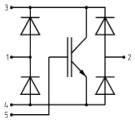
www.dynexsemi.com



- High power matrix converters
- Can be used in output stage of IMC / SMC
- 400 A / 1.2 kV devices
- *Switching energy* @ Tc=125°C:
  $E_{t\text{-}off}$ = 65mJ
  $E_{t\text{-}on}$ = 55mJ
  E_{rr} = 24mJ

DYNEX half-bridge DIM400WHS12

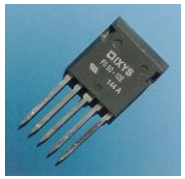
www.dynexsemi.com

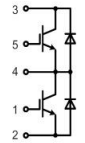


- 7.5kW IGBT-based prototype
- Can be used in input stage of IMC/SMC
- 50 A / 1.2 kV devices
- *Switching energy* @ Tc=125°C:
  $E_{t\text{-}off}$ = 3.0mJ
  $E_{t\text{-}on}$ = 3.6mJ

IXYS bi-directional IXYS FIO 50-12BD

www.ixys.com





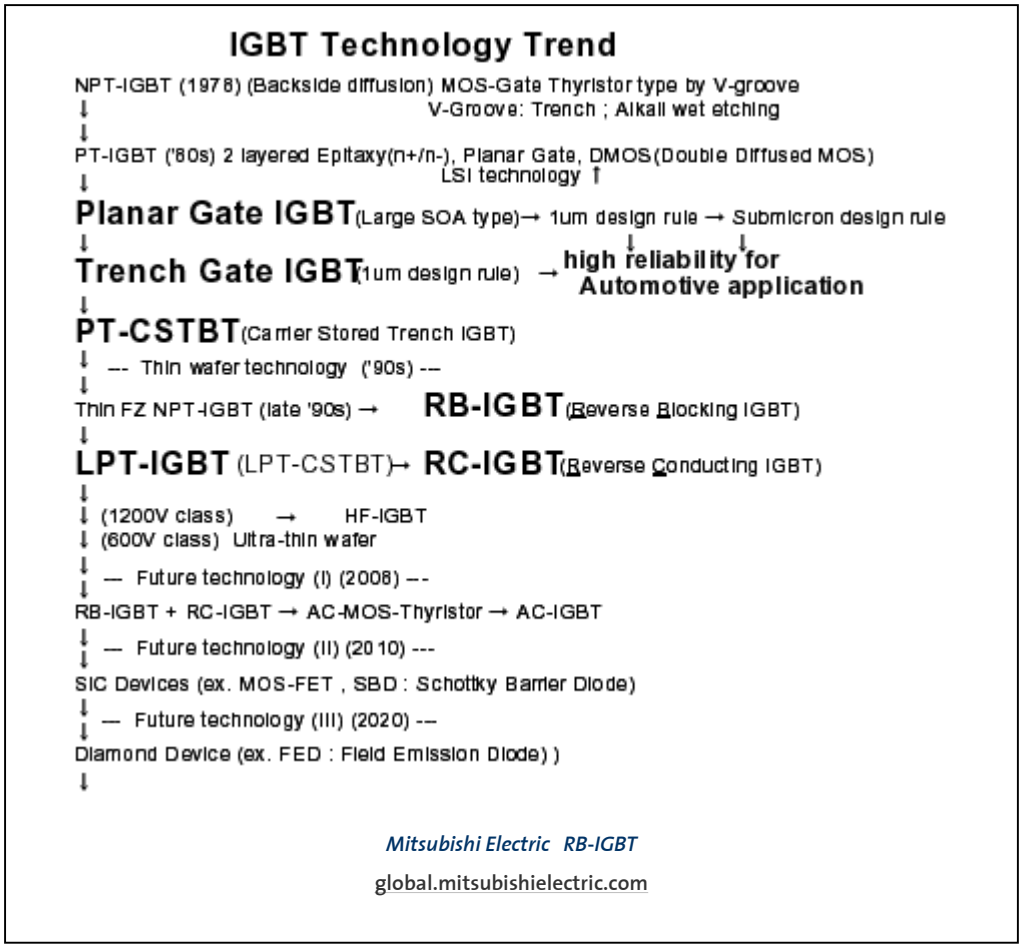
- 7.5kW IGBT-based prototype
- Can be used in output stage of IMC/SMC
- 50 A / 1.2 kV devices
- *Switching energy* @ Tc=125°C:
  $E_{t\text{-}off}$ = 2.2mJ
  $E_{t\text{-}on}$ = 4.6mJ
  E_{rr} = 1.8mJ

IXYS half-bridge IXYS FIO 50-12E

www.ixys.com

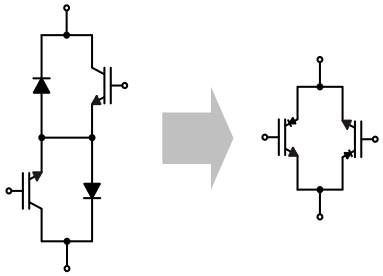
Status of Power Semiconductor Technologies

IGBT technology



Status of Power Semiconductor Technologies

Reverse Blocking – RB-IGBT technology



Advantage

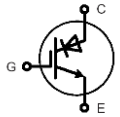
- Bi-directional switch with only one semiconductor in the current path

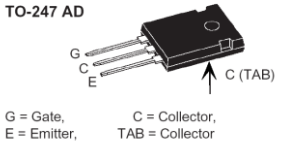
Status

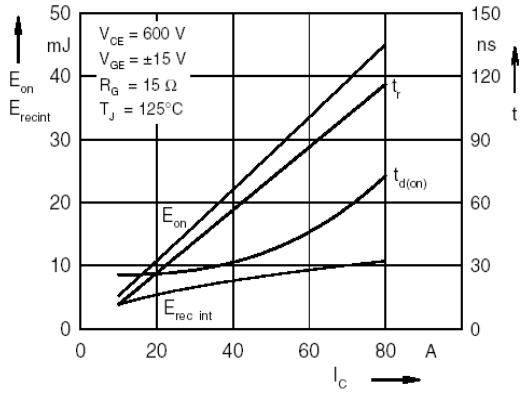
- Only one manufacturer for commercially available devices
- Research (Fuji, Mitsubishi, Rockwell, IXYS) is ongoing in order to increase the voltage blocking capability and decrease switching losses

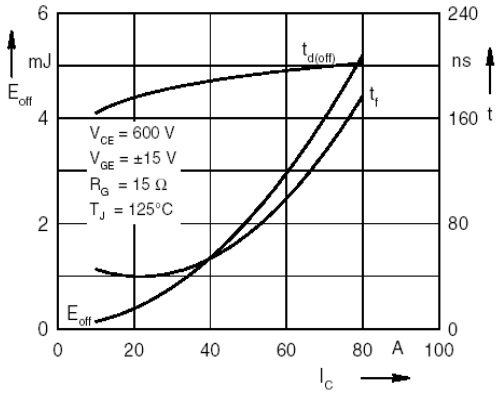
Switch with reverse voltage blocking capability

- Package with a single switch
- Commercially available:
  - 60 A / 600 V devices
  - 60 A / 800 V devices
  - 60 A / 1 kV devices
  - 60 A / 1.2 kV devices









IXYS RB-IGBT IXRH 40N120

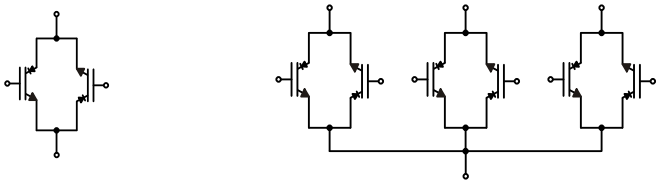
www.ixys.com

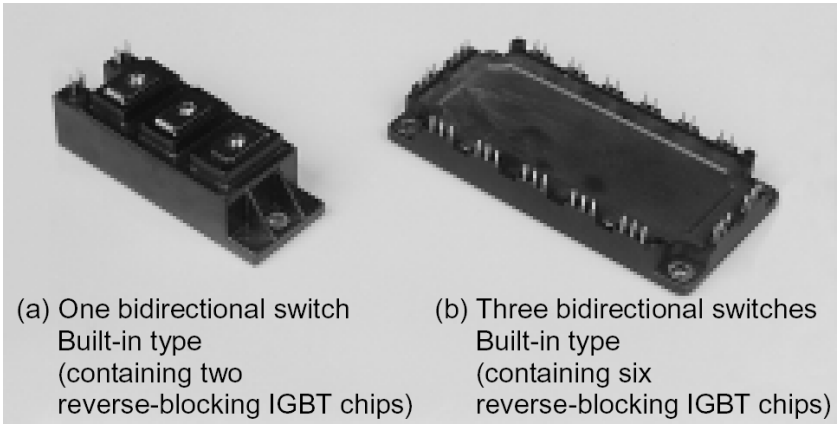
Status of Power Semiconductor Technologies

Reverse Blocking – RB-IGBT technology

Bi-directional switch and Three bi-directional switches modules

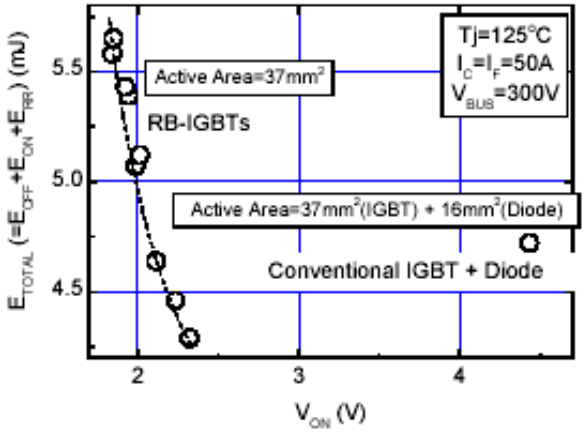
- Layout advantages for a MC
- Compact design
- 50 A / 600 V devices
- Under development

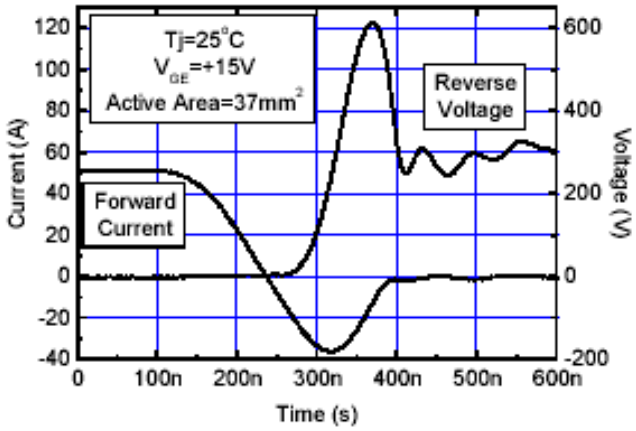




(a) One bidirectional switch Built-in type (containing two reverse-blocking IGBT chips)

(b) Three bidirectional switches Built-in type (containing six reverse-blocking IGBT chips)





Fuji Electric RB-IGBT

www.fujielectric.co.jp

Status of Power Semiconductor Technologies

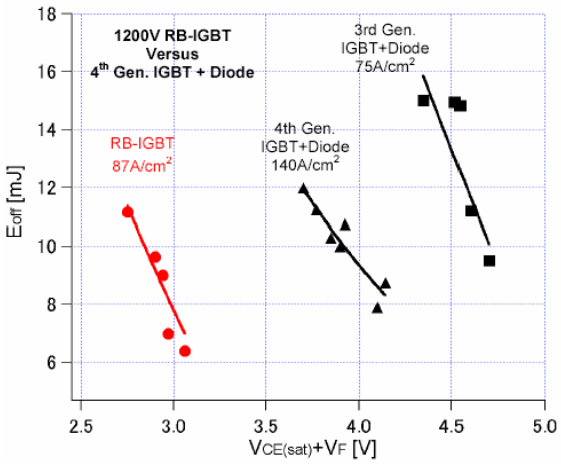
Reverse Blocking – RB-IGBT technology

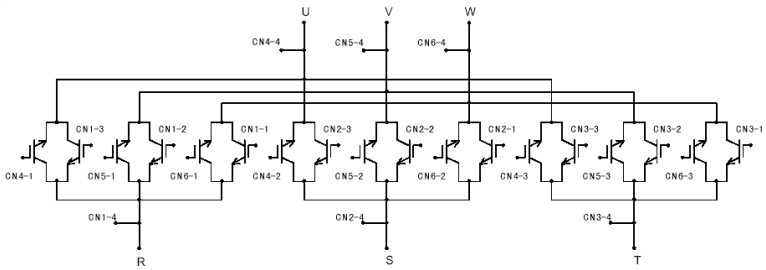
Complete CMC module

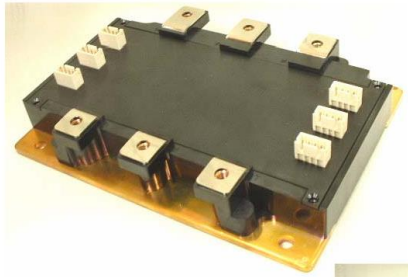
- Layout advantages for a CMC
- Higher efficiency due to lower conduction losses
- Compact design
- 100 A / 1.2 kV devices
- Under development

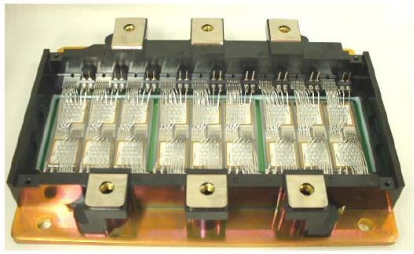
Mitsubishi Electric RB-IGBT

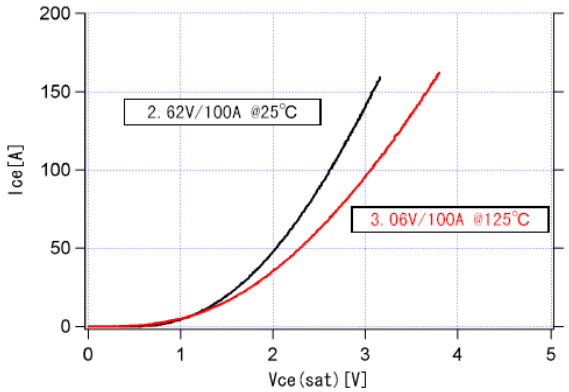
global.mitsubishielectric.com





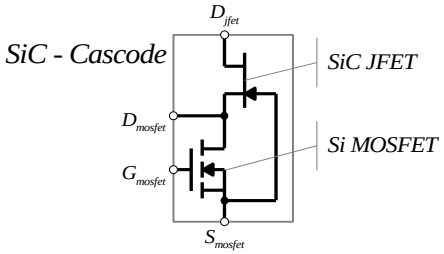


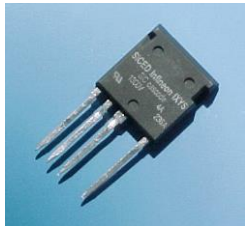




Status of Power Semiconductor Technologies

SiC technology





Characterisitics

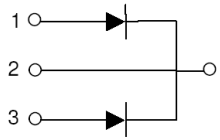
- Normally off device
- Gate strategy is similar to an ordinary MOSFET
- Higher losses due to the MOSFET
- MOSFET intrinsic diode limits maximum dv/dt
- Maximum operating temperature is set by the MOSFET

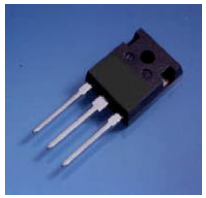
Specification

- 4 A / 1.2 kV devices
- *Switching energy* @ Tc=125°C/4A/400V:
  $E_{t\text{-}off}$ = 15.3 ❍J
  $E_{t\text{-}on}$ = 38.1 ❍J
  E_{rr} = 23.9 ❍J

SiCED/INFINEON cascode (SiC-JFET + Si-MOSFET)

www.siced.de





Specification

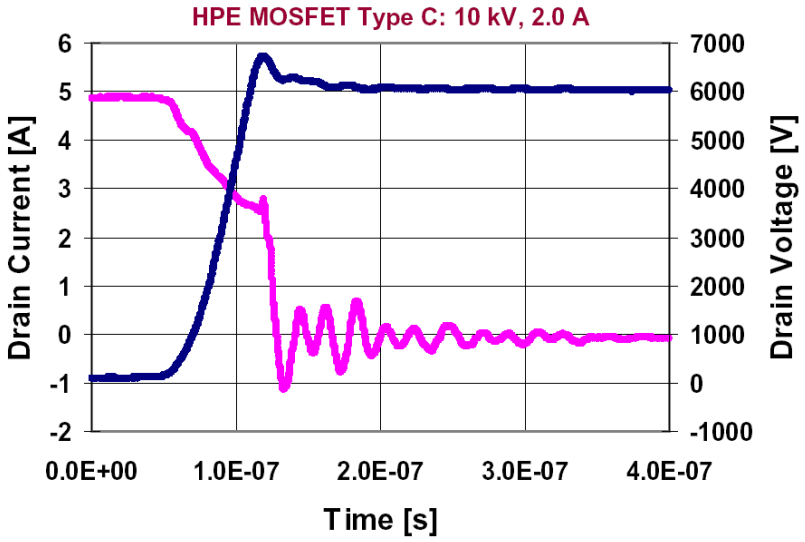
- 20 A / 1.2 kV devices
- TO-247
- Capacitive charge (@ 25°C / 10A / 500A/ns / 1.2kV):
  Q_C = 61nC

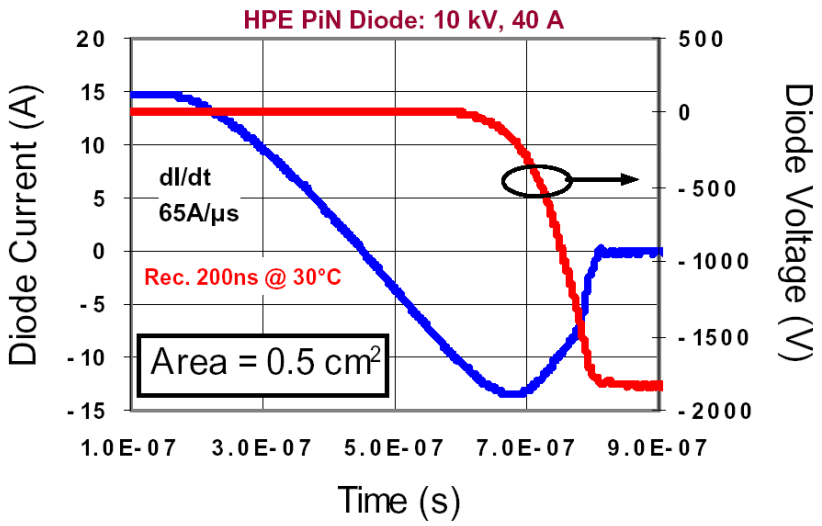
CREE SiC schottky diode CSD20120

www.cree.com

Status of Power Semiconductor Technologies

SiC technology



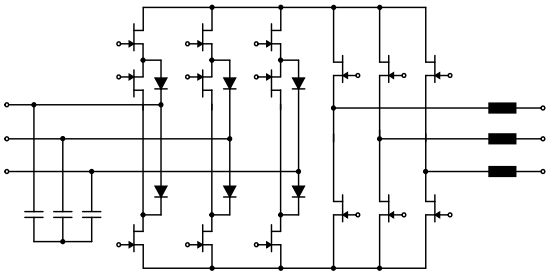


Semiconductor Electronics Division - NIST (SiC-MOSFET)

http://www.eeel.nist.gov/

Status of Power Semiconductor Technologies

Design example – SMC based on SiC technology



Input (3~AC)

Input RMS line voltages (U1)	3 x 400 V +/- 20%
Maximum input RMS current	$I_{1,max}$ = 5 A
Mains frequency	f_1 = 50 Hz
Current displacement angle	φ_1 = 0°

Output (3~AC)

Output RMS line voltages (U2)	3 x 0 – 340 V
Maximum output power	S_2 = 2.5 kVA
Output frequency	f_2 = 0 – 1000 Hz
Current displacement angle	φ_2 = 0° – 90°

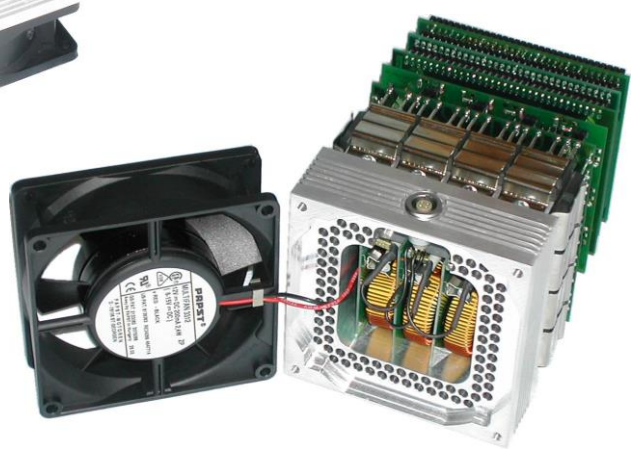
Switching frequency: f_p = 150 kHz

Power stage topology: Sparse Matrix Converter

Power switches technology: SiC/Si cascodes + SiC schottky diodes

Dimensions: 92 x 92 x 160 mm

Weight: 1460 g

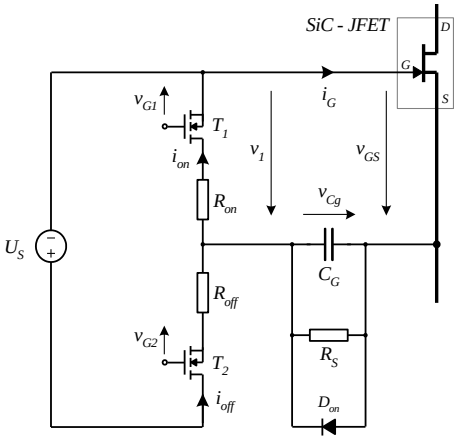


Status of Power Semiconductor Technologies

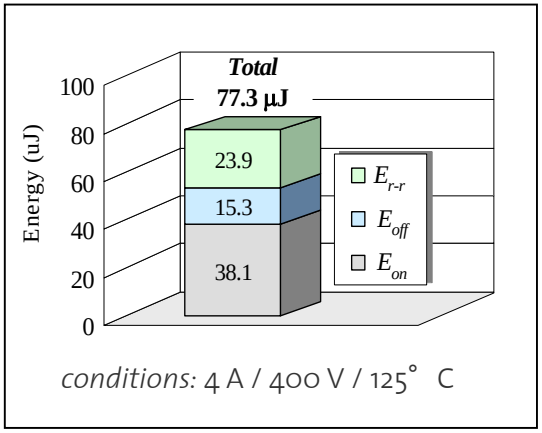
Design example - SiC technology

SiC JFET gate driver requirements

- negative voltage (-20V up to -40V)
- pinch-off voltage is close to the breakdown voltage
- thresholds are not well defined
- new devices are under development
- design with monolithic drivers

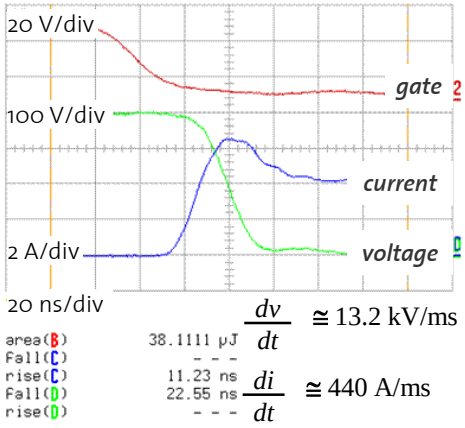


SiC JFET switching energy



conditions: 4 A / 400 V / 125° C

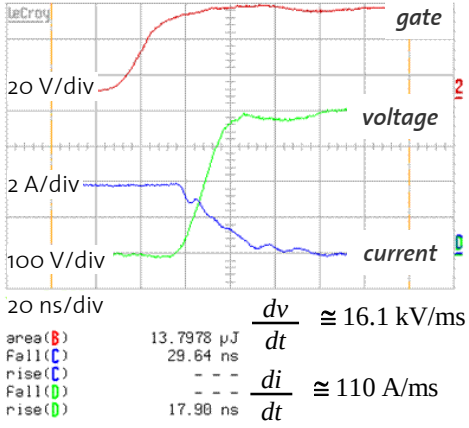
SiC JFET turn-on



$\frac{dv}{dt} \cong 13.2$ kV/ms

$\frac{di}{dt} \cong 440$ A/ms

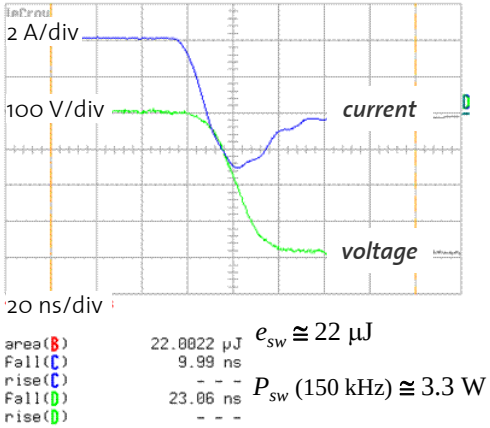
SiC JFET turn-off



$\frac{dv}{dt} \cong 16.1$ kV/ms

$\frac{di}{dt} \cong 110$ A/ms

SiC JFET reverse recovery



$e_{sw} \cong 22$ µJ

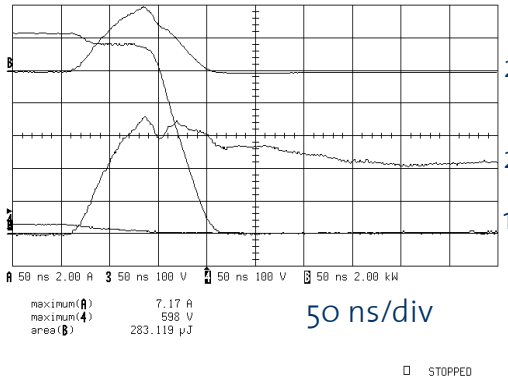
P_{sw} (150 kHz) $\cong 3.3$ W

switching conditions: 4 A / 400 V / 125° C

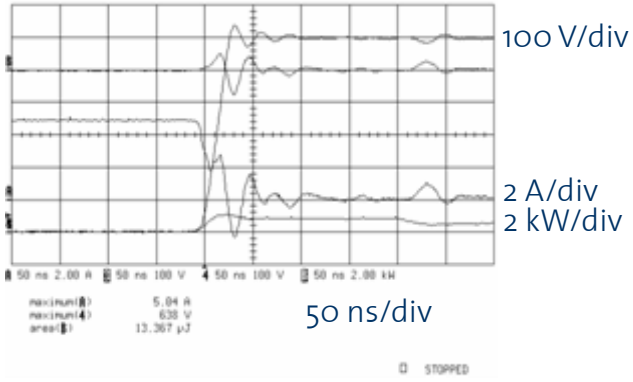
Status of Power Semiconductor Technologies

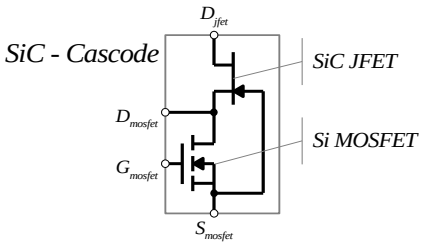
Design example - SiC technology

Cascade turn-on



Cascade turn-off

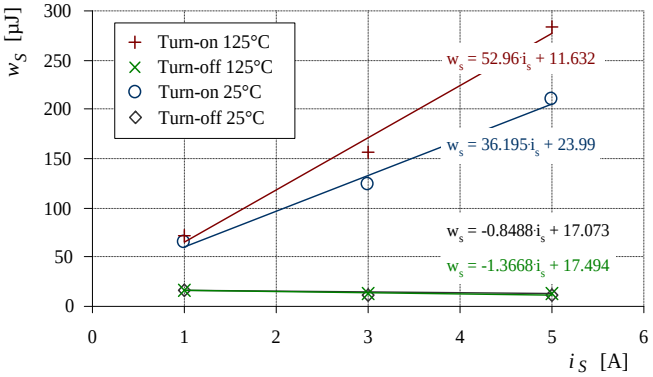




Switching conditions

5A / 600V / 125° C

Cascade switching energy (w_S = 600 V)



Status of Power Semiconductor Technologies

Design example – RB-IGBT technology

Input (3~AC)

Input RMS line voltages (U1)	3 x 400 V +/- 20%
Maximum input RMS current	$I_{1,max}$ = 13 A
Mains frequency	f_1 = 50 Hz
Current displacement angle	$\varphi_1 = 0°$

Output (3~AC)

Output RMS line voltages (U2)	3 x 0 – 320 V
Maximum output power	S_2 = 6.8 kVA
Output frequency	f_2 = 0 – 200 Hz
Current displacement angle	$\varphi_2 = 0° – 90°$

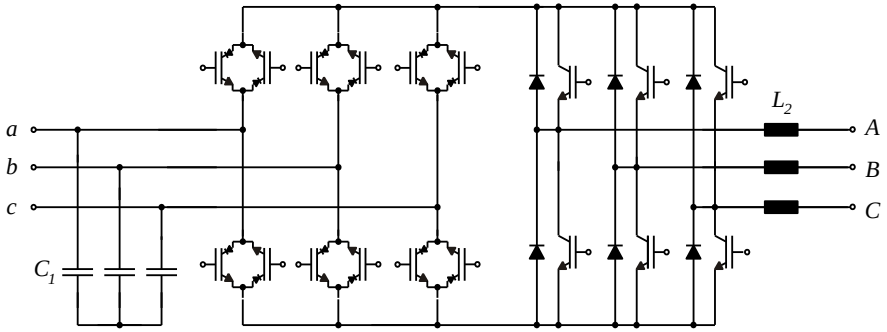
Switching frequency: f_p = 10 kHz

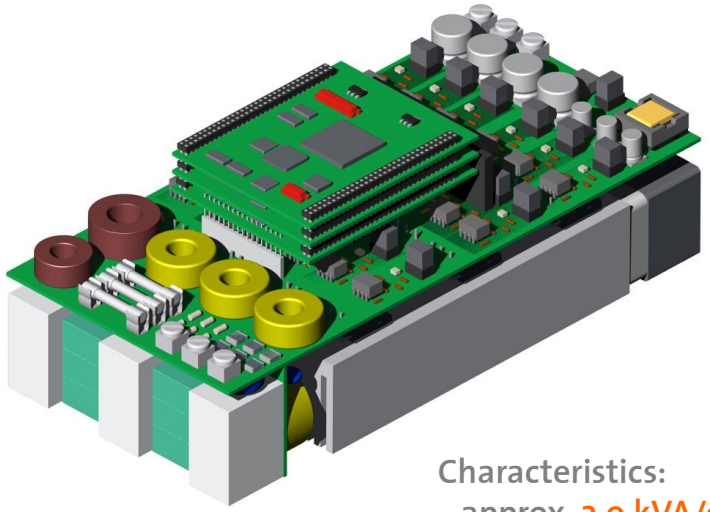
Power stage topology: Indirect Matrix Converter

Power switches technology: Input: Si RB-IGBT
Output: Si IGBTs + fast Si diodes

Dimensions: Power section: 120 x 260 x 76 mm

Estimated weight: Power section: 3200 g



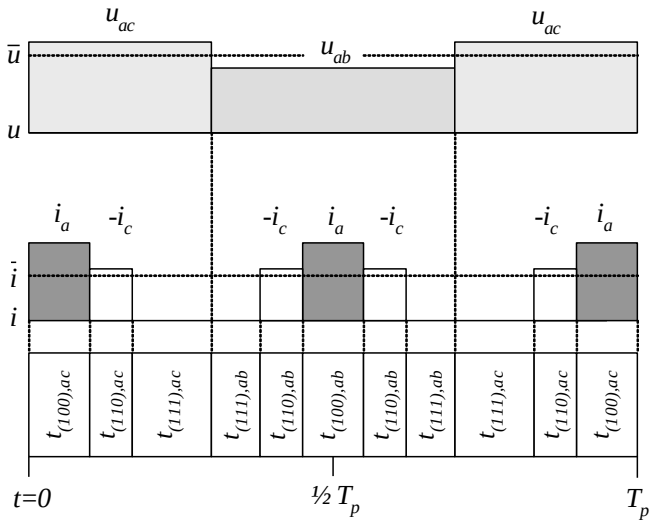


Characteristics:
approx. 2.9 kVA/dm³
approx. 2.1 kW/kg

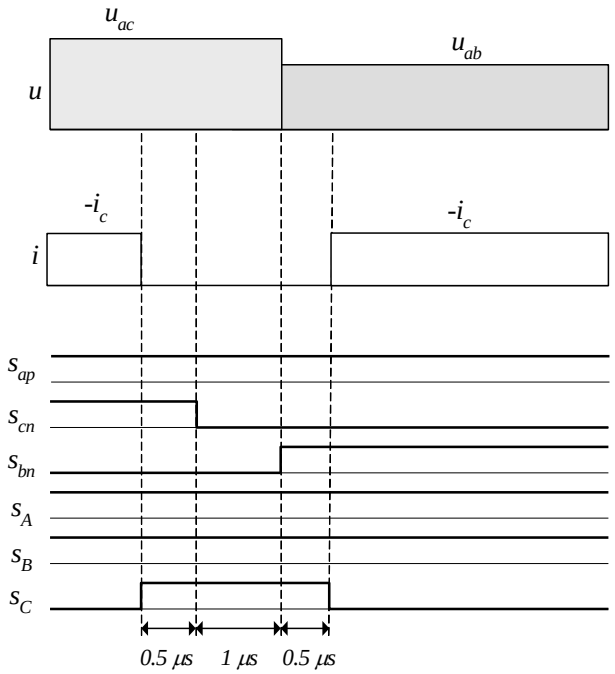
Status of Power Semiconductor Technologies

Design example – RB-IGBT technology

Modulation



Switch Control Delay Times – Interlock Delay Times



Switching frequency: f_p = 10 kHz

Status of Power Semiconductor Technologies

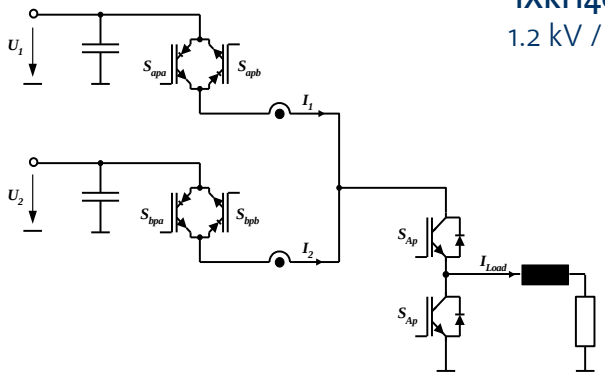
Design example – RB-IGBT technology

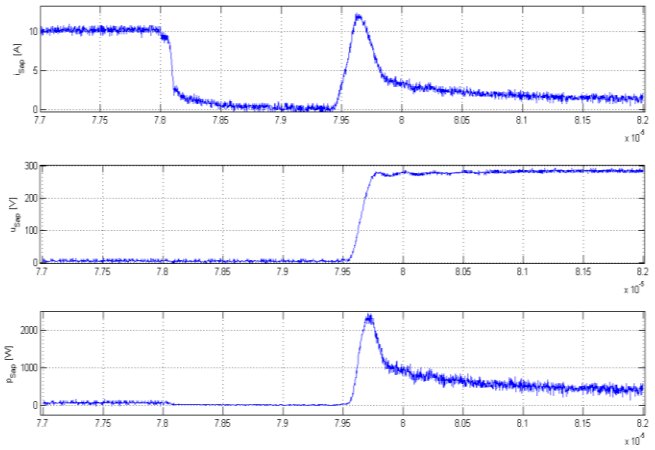
Switching loss measurements

IXYS RB-IGBT

IXRH40N120

1.2 kV / 55 A





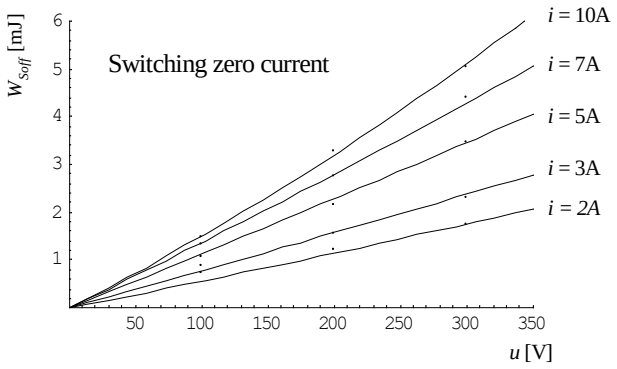
5 A/div

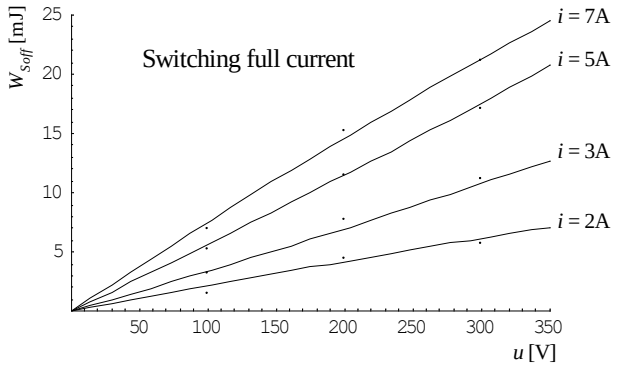
100 V/div

1 kW/div

500 ns/div

$$p = 0.0004175\, i\, u - 0.0000207\, i^2\, u + 2.2065964\, u^2 + 8.4917028\, i\, u^2 - 3.0776863\, i^2\, u^2$$



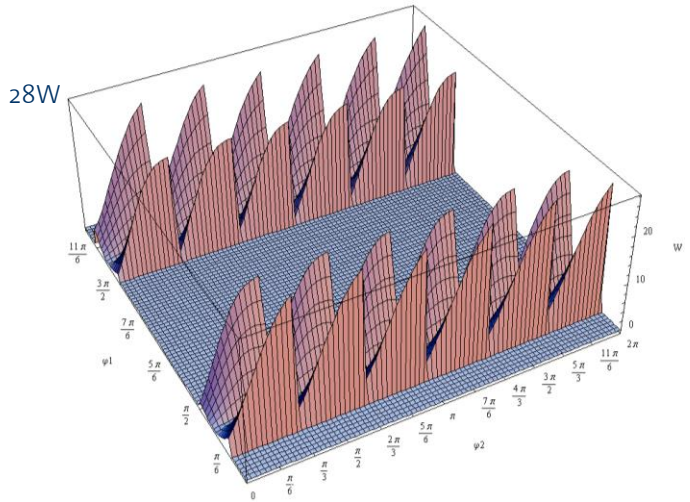


Measurement results switching from low to high input voltage

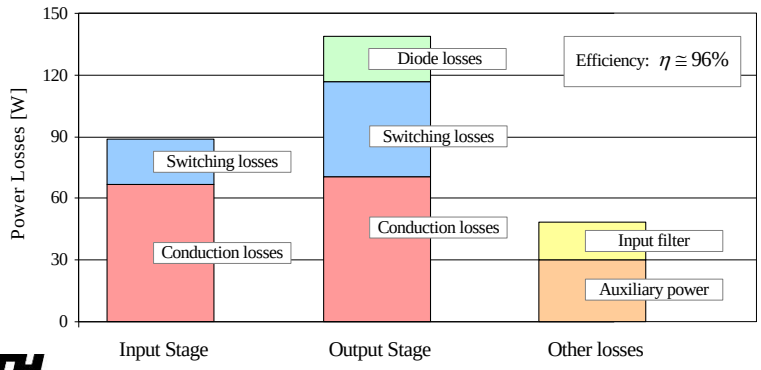
Status of Power Semiconductor Technologies

Design example – RB-IGBT technology

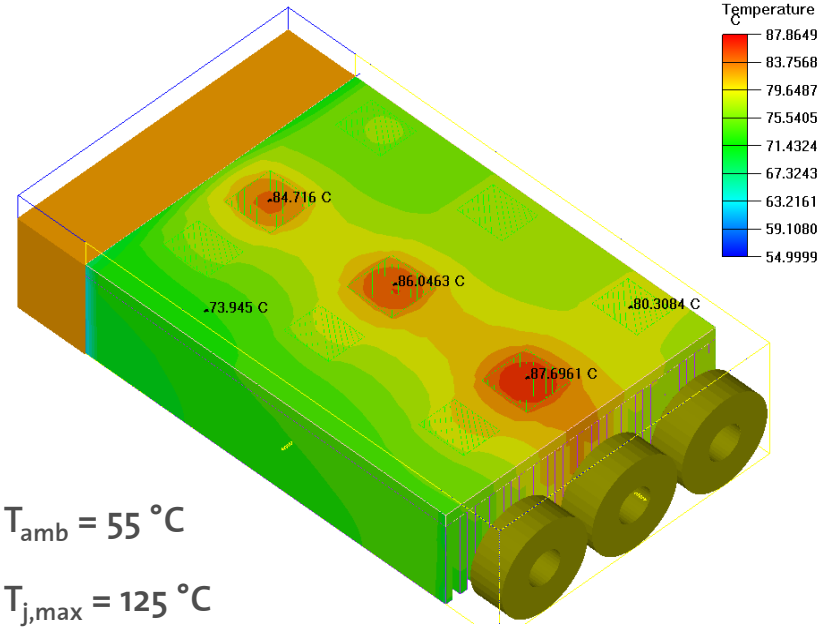
Switching losses in the input stage



Losses distribution



Thermal design through thermal simulations



T_{amb} = 55 °C

$T_{j,max}$ = 125 °C

Industrial products

Matrix Converter – Yaskawa

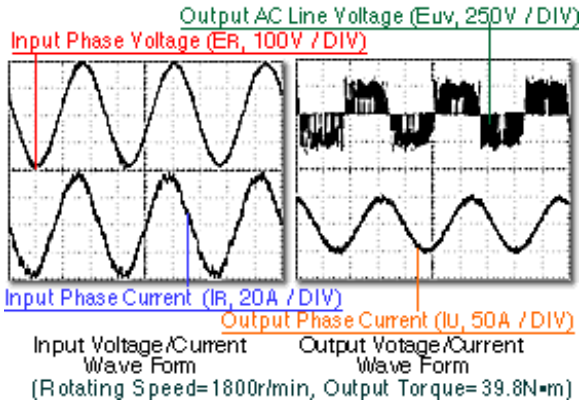
Equipment: YASKAWA's Variable speed AC motor control
-> first commercially available matrix converter drive

Target markets: lifts, cranes and presses

Structure: Conventional Matrix Converter

Specifications:

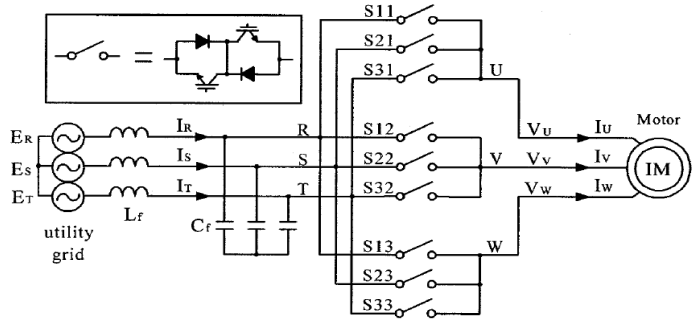
2006: 400 V / 5.5 – 22 kW
Future: 400 V / 5.5 – 75 kW
200 V / 5.5 – 45 kW

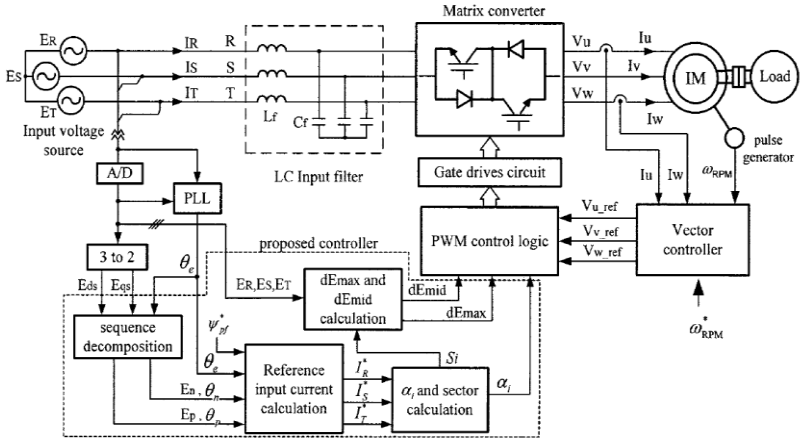


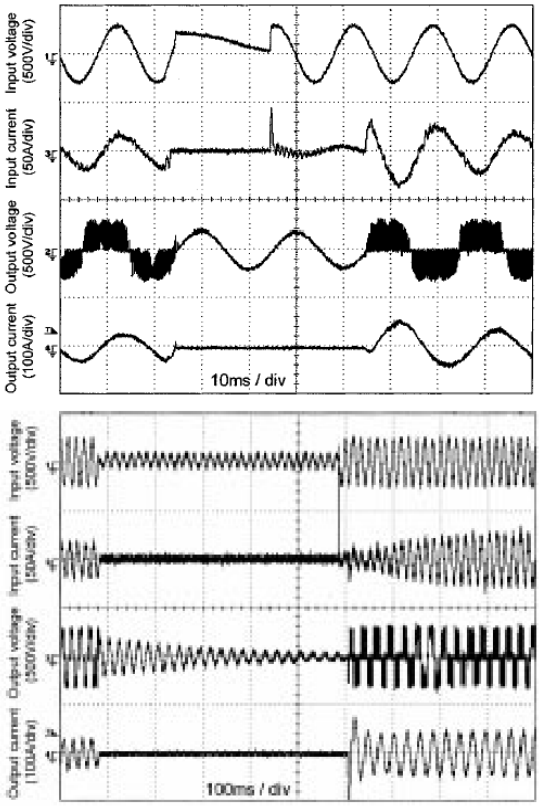
http://www.yaskawa.co.jp/en/technology/gihou/64-2/t11.htm
Source: Yaskawa Technical Review: Vol.64 No.2

Industrial products

Matrix Converter – Yaskawa



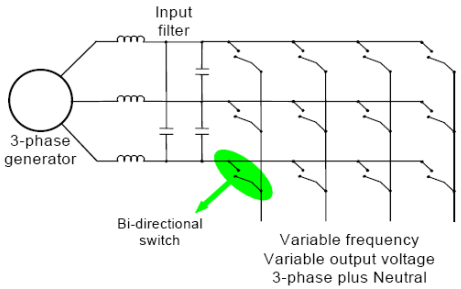




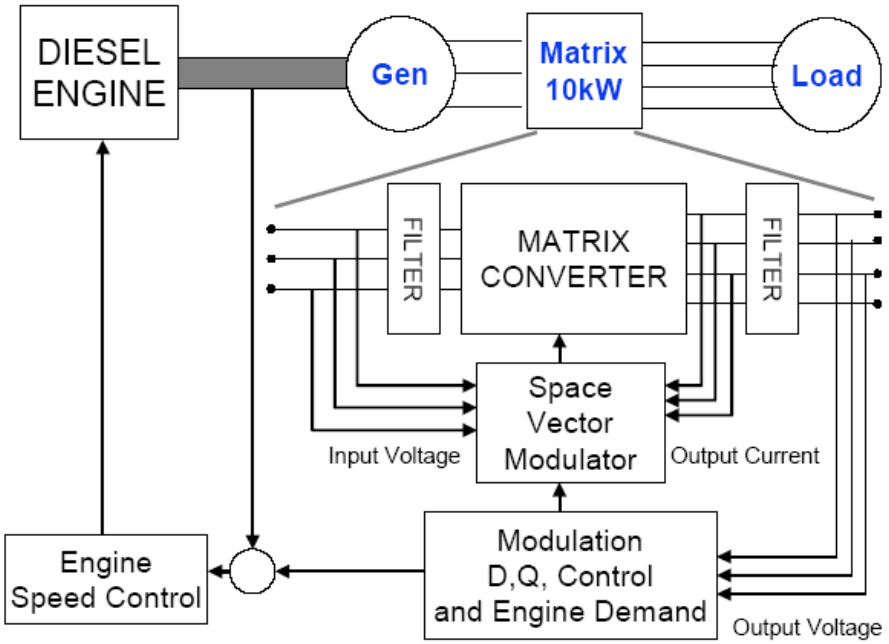
Source: IEEE Transactions on Power Electronics, Vol. 17, No. 5, September 2002

Potential Future Application Areas

Conversion of Variable Frequency 3~AC Power into Fixed Amplitude/Frequency 3~AC Mains



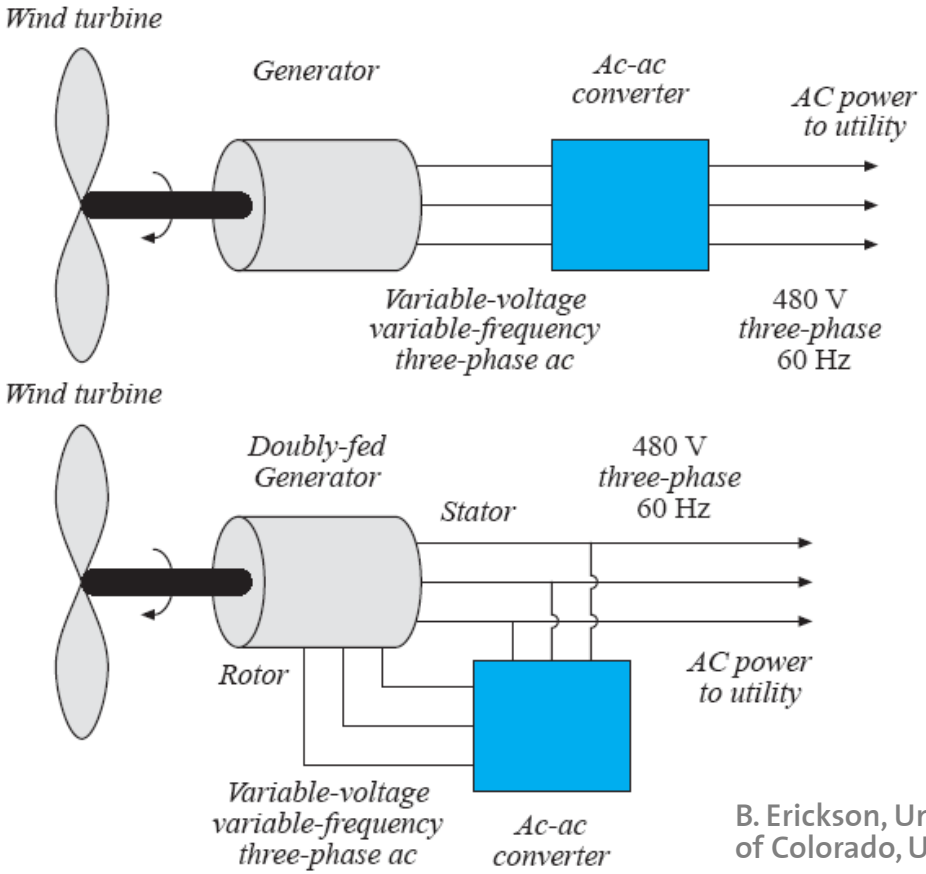
Univ. of Nottingham / UK



- 3-Leg or 4-Leg Matrix Converter for US Army Ground Power Supply
- 50Hz- 400Hz Output Frequency

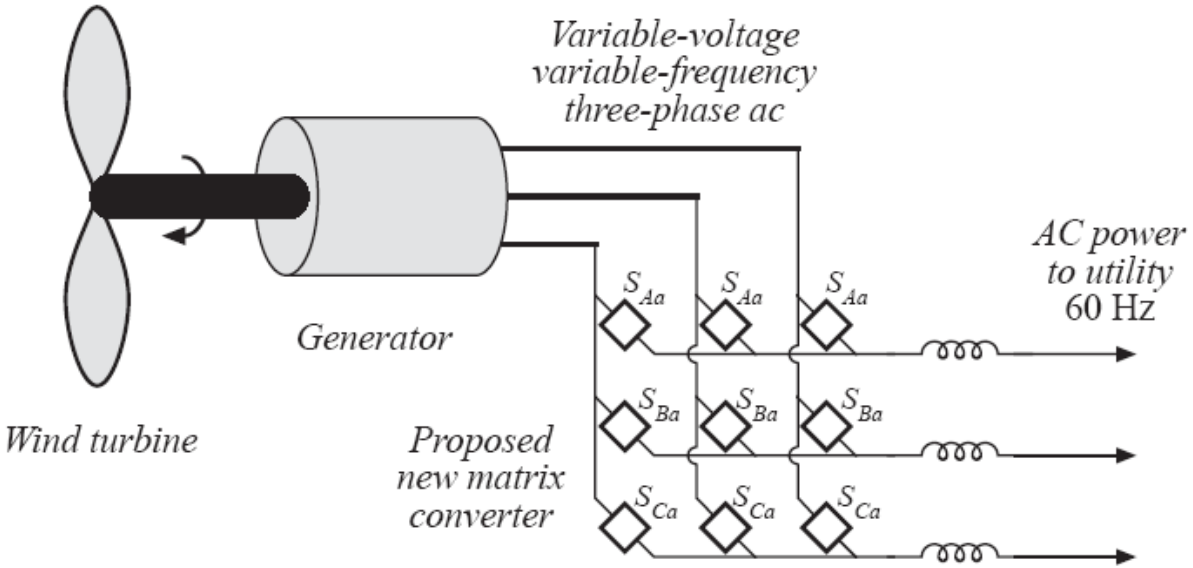
Wind Power Conversion

- High Input and Output Current Quality
- High Efficiency over Wide Speed Range
- Low Volume



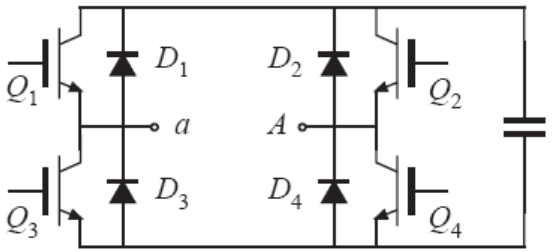
B. Erickson, Univ. of Colorado, USA

Multi-Level Conversion



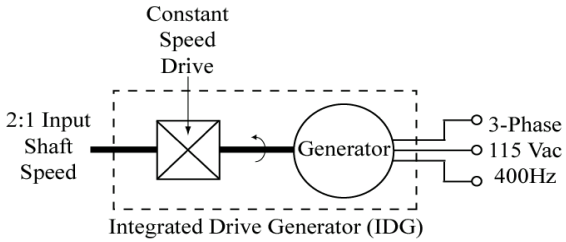
- Step-Up and Step-Down
- Simple Switch Commutation
- Modular Construction

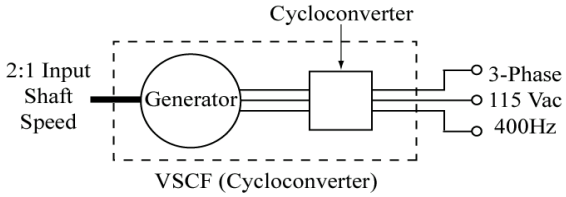
Switch cell:

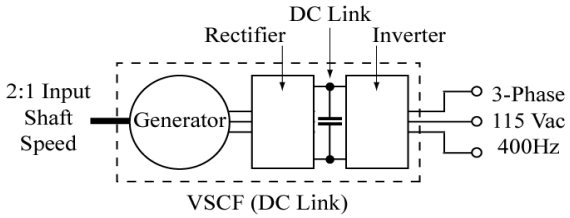


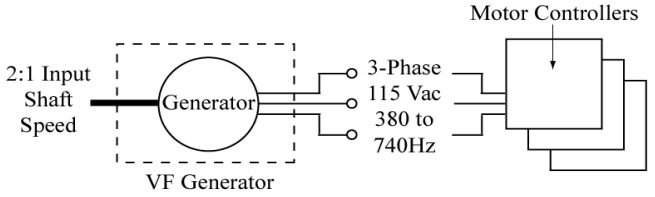
More Electric Aircraft

Variable Frequency Power Generation
Replacement of Hydraulic by Electric System

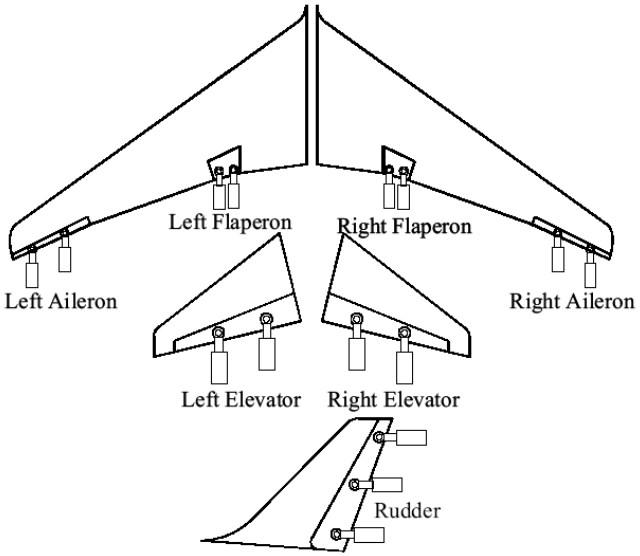








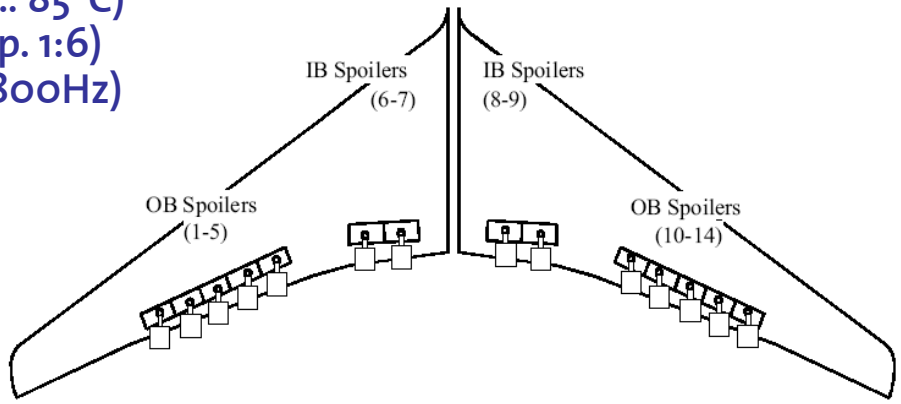
Flight Control Surface Actuation



EHA Electro-Hydrostatic Actuator
EMA Electro-Mechanical Actuator

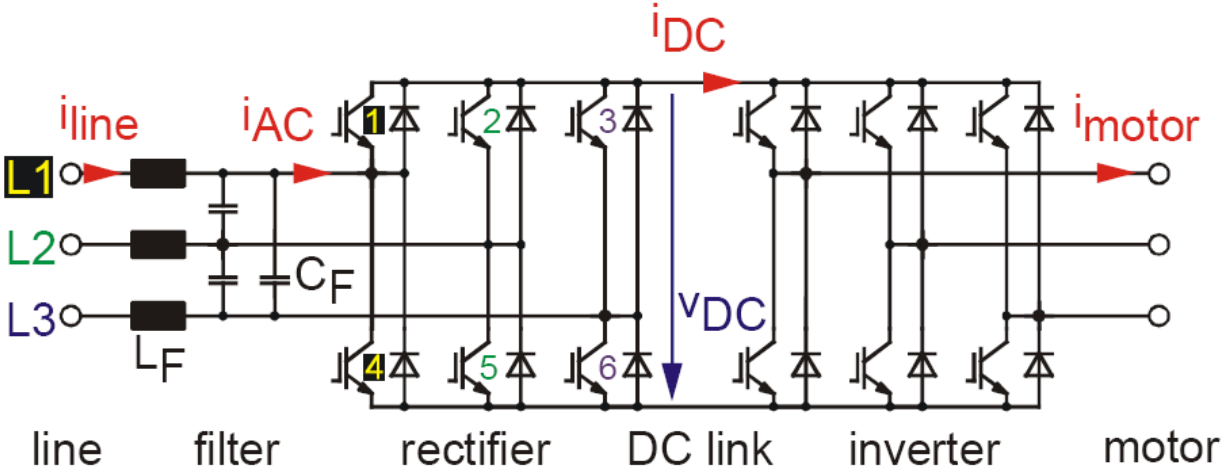
Converter Requirements

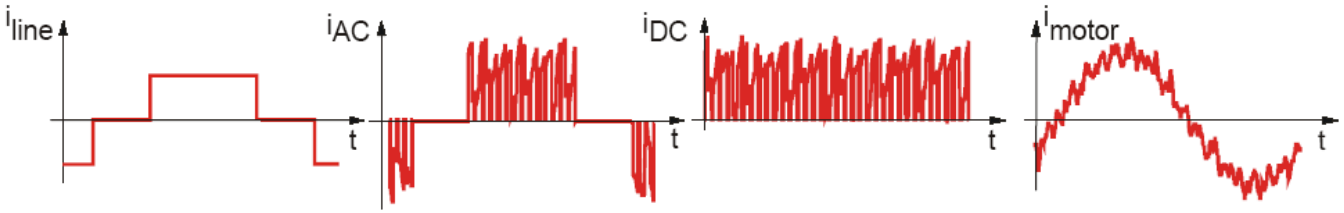
- Extreme Temperature Range (-45°C ... 85°C)
- High Peak-to-Average Load Ratio (typ. 1:6)
- Wide Input Frequency Range (360...800Hz)
- Low Weight and Volume
- Input Current THD (< 5%)
- Low EMI
- Low Input Capacitance/Current Displacement Factor (2.5uF/kVA)
- High Reliability



Alternative Topologies

Back-to-Back Converter without DC Link Capacitor

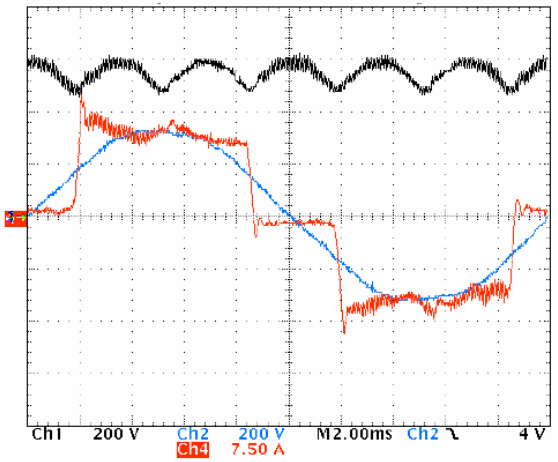




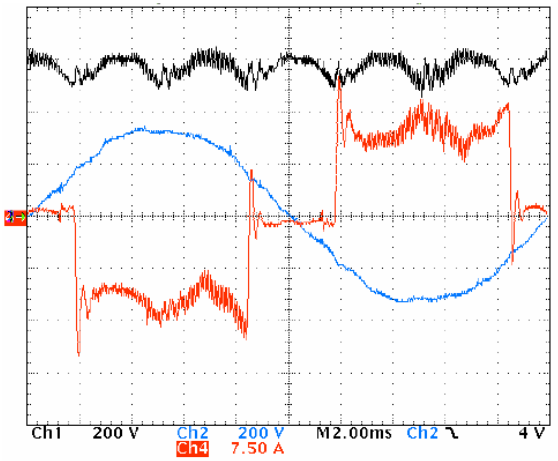
- Line Frequency Switched Input Stage
- Rectangular-Shaped Input Current

Univ. of Erlangen-Nuremberg, Germany

Mains Voltage/Current and DC Link Voltage



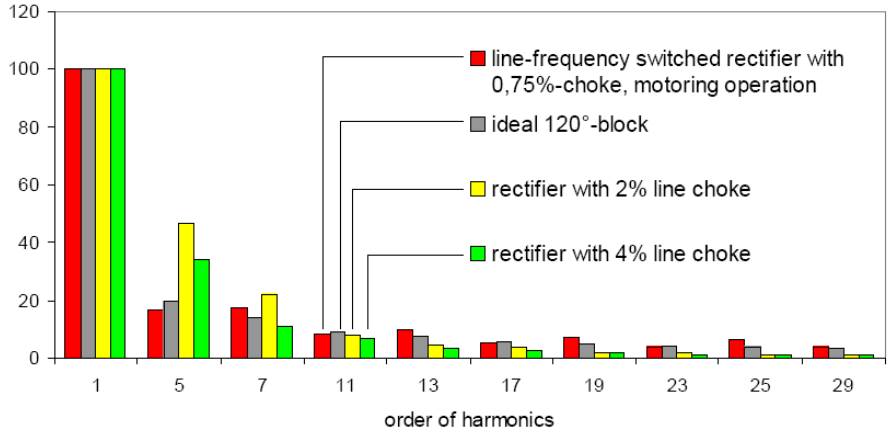
motor operation



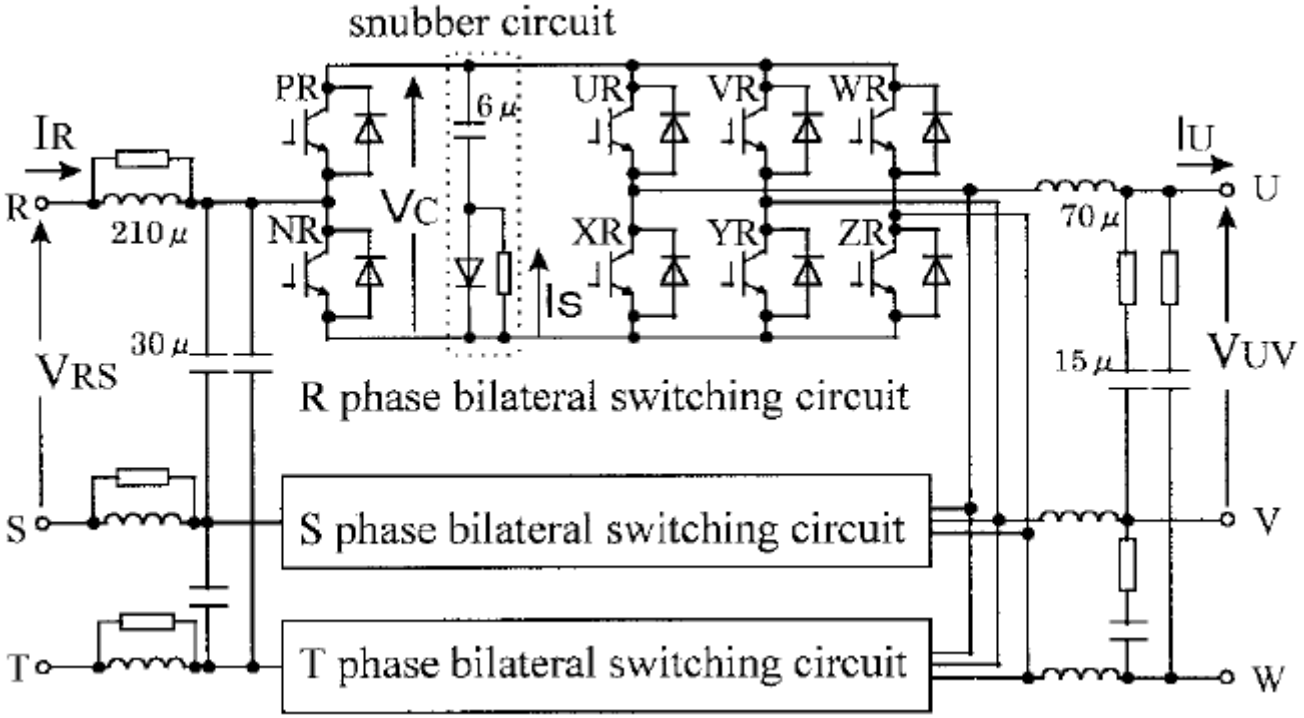
generator operation

- C_{DC}=2.2uF
- f_P=10kHz
- 12.7kVA (7.5kW motor)

LF Mains Current Harmonics



Direct-Linked-Type Frequency Changer



- No Bidirectional Switches Required
- Avoids Clamp Circuit

Fuji Electric, Japan

- Regeneration of Snubber Energy

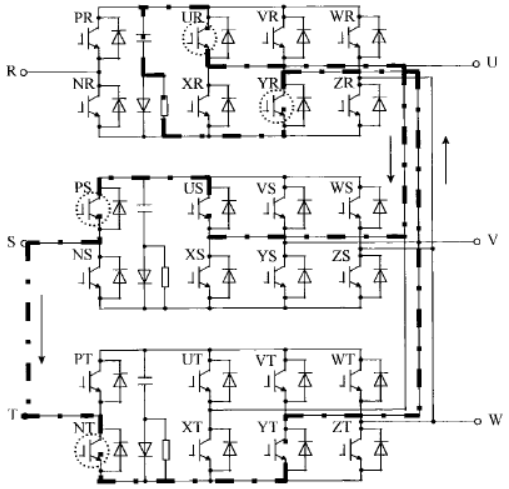
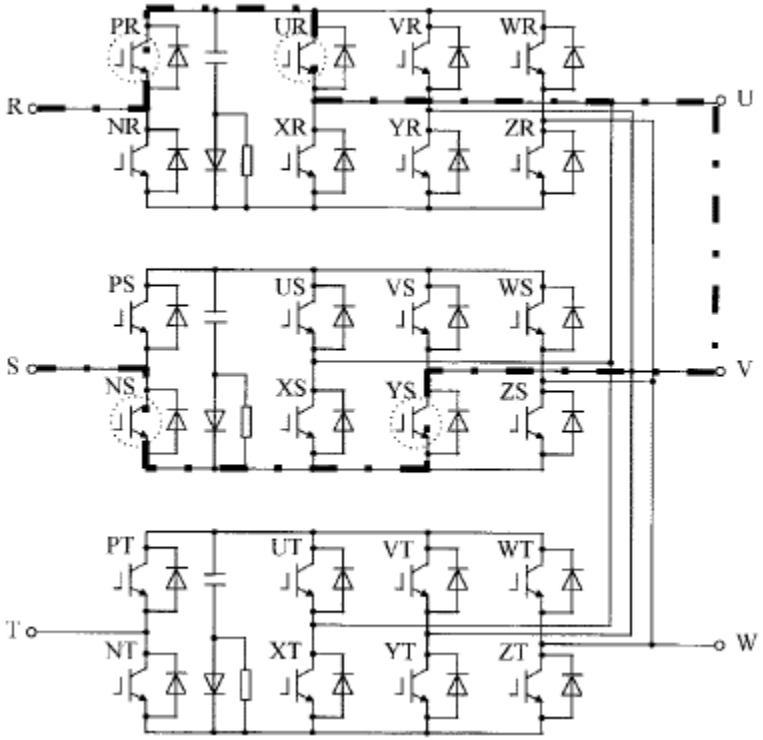
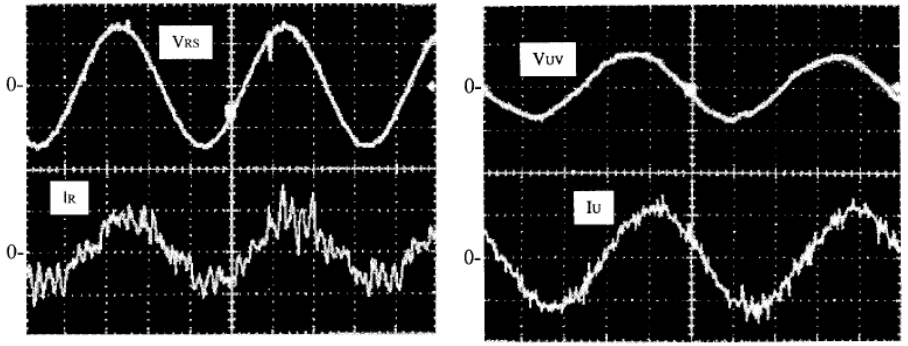


Fig. 11. Regenerative route of snubber energy.



- Bidirectional Connection of Input and Output
- Input Voltage/Current
- Output Voltage/ Current



Thank you very much for your Attention !