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Author(s):
Rothmund, Daniel

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10 kV SiC-Based Medium-Voltage Solid-State Transformer Concepts for 400 V DC Distribution Systems

A thesis submitted to attain the degree of

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presented by

DANIEL ROTHMUND

MSc ETH
born on 20.01.1989
citizen of Germany

accepted on the recommendation of

Prof. Dr. Johann W. Kolar, examiner
Prof. Dr. Hans-Peter Nee, co-examiner

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ETH Zurich
Power Electronic Systems Laboratory
Physikstrasse 3 | ETL H23
8092 Zurich | Switzerland

http://www.pes.ee.ethz.ch

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Für Claudia
und meine Eltern

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Daniel Rothmund

Abstract

At the present time, the globalization and the digital revolution are the main drivers of the global economic growth, which, however, goes hand in hand with a significant increase of the world's energy consumption. To reduce the emission of greenhouse gases despite the rising energy demand, there are clear trends towards an increasing share of electric vehicles (EVs) on the automotive market and towards the integration of more renewable energy into the utility grid. Power electronics is one of the main enabling technologies for this fundamental change, since the distribution of the electrical power is taking place at medium-voltage (MV)-AC, whereas EV batteries or e.g. data centers (on the load-side) and photovoltaic (PV) power plants as well as wind turbines (on the generation-side) represent low-voltage (LV)-DC loads or sources, which means that MV-AC to LV-DC interfaces are required. The state-of-the-art solution for such MV-AC to LV-DC interfaces are low-frequency transformers (LFTs) with subsequent (bidirectional) AC/DC converters. There, the LFT provides the required voltage transfer ratio and galvanic isolation.

For a further reduction of greenhouse gas emissions, the available electrical energy should be utilized to the highest possible extent, i.e. the energy efficiency of the entire power supply chain from the generation-side to the load-side has to be increased. In this context, Solid-State Transformers (SSTs), i.e. power electronic converters with an MV connection and galvanic isolation by means of a medium-frequency (MF) transformer, are a highly attractive alternative for the realization of MV-AC to LV-DC interfaces due to their higher efficiency, high power density, and their additional control features compared to the state-of-the-art solution.

One group of high-power LV-DC loads are e.g. data centers, whose energy demand will increase significantly in the near future due to the exploding internet IP traffic. In data centers, the benefit of utilizing SSTs is even higher than for other applications, since their traditional power supply chain consists of several cascaded conversion stages with a low total efficiency, which can be omitted by the use of MV-AC to 400 V DC SSTs. There, it is intended to supply individual server racks, which can reach power levels in the range of 20 . . . 40 kW, with separate SSTs with the additional advantage of substantially lower cable cross sections and/or lower losses compared to LV distribution. Therefore, a highly efficient 25 kW, 3.8 kV single-phase AC to 400 V DC SST with a

target efficiency of 98 % is realized and experimentally verified in this thesis.

Instead of interfacing the MV-AC grid with a cascaded multi-cell AC/DC converter, which consists of several series-connected converter cells employing e.g. 1200...1700 V semiconductors, a single-cell approach based on the latest generation of 10 kV SiC MOSFETs is selected due to the significantly lower complexity and the higher resulting power density. There, a bidirectional single-cell AC/DC converter faces the MV-AC grid, whereas a subsequent isolated single-cell DC/DC stage converts the intermediate DC-link voltage of 7 kV into 400 V DC. To utilize the full potential of these 10 kV SiC MOSFETs, in this work a complete technology package containing all the required concepts and circuits necessary to realize a highly efficient, highly compact, and reliable 10 kV SiC MOSFET-based MV-AC to LV-DC SST is developed.

To enable an integration of the isolated gate driver into future intelligent MV SiC modules, which would enhance the switching behavior and would significantly simplify the design of MV converters, the volume of the isolated gate driver supply has to be decreased substantially compared to state-of-the-art solutions. Therefore, a highly compact gate driver isolation transformer with a coupling capacitance of only 2.6 pF is realized. Furthermore, the gate driver features an ultra-fast overcurrent protection with a reaction time of only 22 ns and the capability of clearing hard-switching faults and even flashover faults within less than 200 ns at a DC-link voltage of 7 kV.

Since there has not been any switching loss data available for the employed 10 kV SiC MOSFETs (especially in the case of soft-switching), these losses have to be determined experimentally. However, an error analysis shows that electrical soft-switching loss measurements can lead to large errors and therefore these measurement methods are unsuitable. To obtain reliable data for the switching losses, a highly accurate calorimetric soft-switching loss measurement method is developed and the results show that, compared to hard-switching, the soft-switching losses are a factor of 30 lower.

For this reason, the goal is to operate all switches under soft-switching conditions, since this allows for a high efficiency and enables the downsizing of passive components by employing a high switching frequency. Therefore, a novel bidirectional AC/DC converter topology is developed, which enables soft-switching over the entire AC grid period by adding a simple LC-branch to the well-known full-bridge AC/DC

converter, which internally superimposes a high triangular current on the AC grid current to reverse the current direction in each switching cycle. Hence, this concept is called *integrated* Triangular Current Mode (*i*TCM) operation. Furthermore, the design of the required AC-side LCL filter is discussed in detail and a quasi lossless method to eliminate current oscillations in MV cables independently of the cable length is presented. Based on a theoretical analysis, which shows that it is very important in case of MV converters of this power class to minimize parasitic capacitances, a low-capacitive design of the magnetic components and the PCB layout is realized. Highly accurate calorimetric efficiency measurements show that the *i*TCM single-phase AC/DC converter achieves a full-load efficiency of 99.1 %, while it features an unprecedented power density of 3.28 kW/L.

For the subsequent isolated DC/DC back end of the SST, an LLC series resonant converter topology is selected and operated at resonance frequency as "DC transformer" providing a tight coupling of the converter's input and output voltages. In order to achieve soft-switching of all switches under all load conditions and especially for both power flow directions, a special modulation scheme is developed which allows the active sharing of the turn-off current among the MV-side and the LV-side. Furthermore, the MF MV transformer is Pareto-optimized regarding its efficiency and power density and special attention is paid to its MV insulation and the selection and application of a proper insulation material. Calorimetric efficiency measurements show that the isolated DC/DC converter achieves an efficiency of 99.0 % between 50 % rated power and full load, while it features a power density of 3.8 kW/L.

Therefore, the complete MV-AC to LV-DC SST system achieves a full-load efficiency of 98.1 % and a power density of 1.76 kW/L. Compared to an SST with similar specifications presented in 2017 by *Fuji Electric*, which achieves an efficiency of 96 % and a power density of 0.4 kW/L, the SST realized in this work generates less than half the losses and is more than four times smaller.

Kurzfassung

Die heutige Zeit ist massgeblich von der Globalisierung und der digitalen Revolution als stärkste treibende Kräfte für das globale wirtschaftliche Wachstum geprägt, das jedoch mit einer deutlichen Zunahme des weltweiten Energieverbrauchs einhergeht. Um die Emission von Treibhausgasen trotz des steigenden Energiebedarfs zu reduzieren, zeichnen sich klare Trends hin zu einem grösseren Marktanteil von Elektrofahrzeugen (electric vehicles, EV) und zu einer zunehmenden Integration von erneuerbaren Energien in das Energienetz ab. Eine der Schlüsseltechnologien, die diese fundamentale Umstellung ermöglichen, ist die Leistungselektronik, da die Verteilung der elektrischen Energie auf der AC-Mittelspannungsebene (medium-voltage, MV) erfolgt, während sowohl EV Akkus und Datencenter als auch Photovoltaik (PV)-Kraftwerke und Windkraftanlagen Niederspannungs- (low-voltage, LV)-DC-Verbraucher bzw. -Quellen darstellen, weshalb MV-AC zu LV-DC Interfaces zwingend erforderlich sind. Die Standardlösung für derartige Interfaces sind Niederfrequenztransformatoren mit nachgeschalteten (bidirektionalen) AC/DC Konvertern. Dabei stellt der Niederfrequenztransformator die notwendige Spannungsübersetzung und die galvanische Trennung bereit.

Zur Minimierung der Treibhausgasemissionen sollte die vorhandene elektrische Energie so effizient wie möglich genutzt werden, d.h. die Effizienz der gesamten Energieversorgungskette von der Erzeugung bis hin zum Verbraucher muss einen möglichst hohen Wert aufweisen. In diesem Zusammenhang sind Solid-State Transformatoren (SST), d.h. leistungselektronische Konverter mit einem Mittelspannungsanschluss und mittelfrequenter Potentialtrennung aufgrund ihrer höheren Effizienz und Leistungsdichte sowie der zusätzlichen Regelbarkeit eine attraktive Option für die Realisierung von MV-AC zu LV-DC Interfaces, alternativ zu Standardlösungen.

Eine Kategorie von Hochleistungs-LV-DC-Verbrauchern sind z.B. Datencenter, deren Energiebedarf in naher Zukunft aufgrund des rasanten Anstiegs des Datenverkehrs im Internet signifikant zunehmen wird. In Datencentern ist der Einsatz von SSTs noch vorteilhafter als in anderen Applikationen, da die traditionelle Energieversorgungskette aus mehreren kaskadierten Konverterstufen mit entsprechend niedriger Gesamteffizienz besteht, die durch den Einsatz von MV-AC zu 400 V DC SSTs jedoch vermieden werden können. Dabei ist die Energieversorgung einzelner Server-Racks, die einen Leistungsbedarf im Bereich

von 20 . . . 40 kW aufweisen, durch individuelle SSTs vorstellbar, was den Vorteil von deutlich kleineren Kabelquerschnitten und/oder kleineren Verlusten gegenüber einer LV-Energieverteilung mit sich bringt. Aus diesem Grund wird in dieser Arbeit ein 25 kW, 3.8 kV Einphasen-AC zu 400 V DC SST mit einer Zieleffizienz von 98 % realisiert und experimentell verifiziert.

Anstatt das Mittelspannungsnetz über einen kaskadierten Multizellen-AC/DC-Konverter anzukoppeln, der aus mehreren in Serie geschalteten Konverterzellen auf Basis von z.B. 1200...1700 V Halbleitern besteht, wird aufgrund geringerer Komplexität und der daraus resultierenden höheren Leistungsdichte eine Einzellen-Topologie basierend auf der neuesten Generation von 10 kV SiC MOSFETs ausgewählt. Dabei wird ein Einzellen-AC/DC-Konverter an das MV-AC Netz angekoppelt, wobei eine nachfolgende isolierte Einzellen-DC/DC-Stufe die Zwischenkreisspannung von 7 kV in 400 V DC umsetzt. Um das volle Potential dieser Lösung auszuschöpfen, wird ein umfängliches Technologiepaket entwickelt, welches alle erforderlichen Konzepte und Schaltungen enthält, die zur Realisierung eines hocheffizienten, hochkompakten und zuverlässigen 10 kV SiC MOSFET-basierten MV-AC zu LV-DC SSTs benötigt werden.

Um eine Integration des isolierten Gatetreibers in ein zukünftiges intelligentes HV SiC Modul zu ermöglichen, was zu einer Verbesserung des Schaltverhaltens und zu einer deutlichen Vereinfachung des Designprozesses von MV-Konvertern führen würde, muss das Volumen der isolierten Gatetreiber-Spannungsversorgung im Vergleich zu bisherigen Lösungen deutlich reduziert werden. Deshalb wird ein hochkompakter Gatetreiber-Isolationstransformator mit einer Koppelkapazität von nur 2.6 pF realisiert. Des Weiteren verfügt der Gatetreiber über eine ultraschnelle Überstromabschaltung mit einer Reaktionszeit von nur 22 ns, die in der Lage ist, Brückenkurzschlüsse und sogar Kurzschlüsse aufgrund eines Funkenüberschlags bei einer Zwischenkreisspannung von 7 kV innerhalb von weniger als 200 ns sicher abzuschalten.

Seitens des Herstellers werden für 10 kV SiC MOSFETs (insbesondere für weiches Schalten) keine Schaltverlustdaten zur Verfügung gestellt; entsprechend müssen diese Verluste experimentell bestimmt werden. Durch eine Fehleranalyse wird allerdings deutlich, dass elektrische Schaltverlustmessungen für weiches Schalten mit sehr hohen Fehlern behaftet und deshalb ungeeignet sind. Um verlässliche Daten zu erhalten, wird ein hochgenaues kalorimetrisches Schaltverlust-Messverfahren ent-

wickelt, wobei die Resultate zeigen, dass die Schaltverluste bei weichem Schalten um einen Faktor 30 geringer sind als bei hartem Schalten.

Aus diesem Grund ist es das Ziel, alle Schalter weich schaltend zu betreiben, da dies eine höhere Effizienz und eine Volumenreduktion der passiven Komponenten durch die Wahl einer höheren Schaltfrequenz ermöglicht. Dazu wird eine neuartige bidirektionale AC/DC Konvertertopologie entwickelt, die weiches Schalten während der kompletten Netzperiode ermöglicht, indem die bekannte Vollbrücken-AC/DC-Konvertertopologie mit einem einfachen LC-Netzwerk erweitert wird, das brückenintern einen hohen Stromrippel auf den Netzstrom aufprägt, um dadurch die Stromrichtung in jeder Schaltperiode umzukehren bzw. für den jeweils abschaltenden Transistor einen positiven Strom sicherzustellen. Dieses Konzept wird daher als *integrated* Triangular Current Mode (*i*TCM) Betrieb bezeichnet. Weiterhin wird die Auslegung des AC-seitig benötigten LCL-Filters detailliert diskutiert und es wird eine quasi verlustlose Methode zur Eliminierung von Stromoszillationen in der Mittelspannungszuleitung unabhängig von deren Länge aufgezeigt. Basierend auf einer theoretischen Analyse die verdeutlicht, dass es für Mittelspannungskonverter dieser Leistungsklasse von hoher Wichtigkeit ist parasitäre Kapazitäten zu minimieren, wird ein niederkapazitives Design der magnetischen Komponenten und des PCB Layouts realisiert. Mithilfe hochgenauer kalorimetrischer Effizienzmessungen wird gezeigt, dass der *i*TCM AC/DC Konverter eine Volllasteffizienz von 99.1 % erreicht, wobei zu beachten ist, dass das System eine für Mittelspannungs-Einphasen-AC/DC-Konverter bisher unerreichte Leistungsdichte von 3.28 kW/L aufweist.

Als Konvertertopologie für den nachgeschalteten isolierten DC/DC Konverter wird ein LLC Serienresonanzkonverter gewählt, der bei Resonanzfrequenz betrieben wird, womit eine starre Kopplung der Eingangs- und Ausgangsspannung bzw. letztlich ein "DC Transformator" resultiert. Um weiches Schalten für alle Schalter über den kompletten Lastbereich und im Speziellen für beide Energieflussrichtungen zu erreichen, wird ein spezielles Modulationsschema entwickelt, welches eine aktive Aufteilung des Abschaltstroms zwischen der MV- und der LV-Seite erlaubt. Des Weiteren erfolgt eine Pareto-Optimierung des Transformators hinsichtlich Effizienz und Leistungsdichte. Spezielle Beachtung kommt der MV Isolation des Transformators und der Auswahl sowie der Anwendung eines geeigneten Isolationsmaterials zu. Kalorimetrische Effizienzmessungen zeigen, dass der isolierte DC/DC Konverter zwischen

50 % Nennlast und Volllast eine Effizienz von 99.0 % erreicht, während er eine Leistungsdichte von 3.8 kW/L aufweist.

Das komplette MV-AC zu LV-DC SST System erreicht damit eine Volllasteffizienz von 98.1 % und weist eine Leistungsdichte von 1.76 kW/L auf. Im Vergleich zu einem SST mit ähnlichen Spezifikationen, der 2017 von *Fuji Electric* vorgestellt wurde und eine Effizienz von 96 % sowie eine Leistungsdichte von 0.4 kW/L erreicht, generiert das in dieser Arbeit realisierte SST System weniger als die halben Verluste und weist weniger als ein Viertel des Bauvolumens auf.

Abbreviations

2D	Two-Dimensional
3D	Three-Dimensional
AC	Alternating Current
BESS	Battery Energy Storage System
BEV	Battery Electric Vehicle
CAD	Computer Aided Design
CL	Conduction Losses
CM	Common Mode
DAB	Dual Active Bridge
DC	Direct Current
DM	Differential Mode
DOI	Digital Object Identifier
DSP	Digital Signal Processor
DUT	Device Under Test
ESR	Equivalent Series Resistance
EV	Electric Vehicle
FEM	Finite Element Method
FFT	Fast Fourier Transform
FOF	Flashover Fault
FPGA	Field Programmable Gate Array
FUL	Fault Under Load
GDT	Gas Discharge Tube
HF	High-Frequency
HSF	Hard-Switching Fault
HSL	Hard-Switching Losses
HV	High-Voltage
IBE	Isolated Back-End
IEEE	Institute of Electrical and Electronics Engineers
IFE	Isolated Front-End
IGBT	Insulated-Gate Bipolar Transistor
IPT	Inductive Power Transfer
ISOP	Input-Series Output-Parallel
IT	Information Technology
LF	Low-Frequency
LFT	Low-Frequency Transformer
MF	Medium-Frequency
MMLC	Modular Multilevel Converter

MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MV	Medium-Voltage
OCP	Overcurrent Protection
PC	Personal Computer
PCB	Printed Circuit Board
PFC	Power Factor Correction
PHEV	Plug-in Hybrid Electric Vehicle
PI	Proportional-Integral
PV	Photovoltaic
PWM	Pulse-Width Modulation
Si	Silicon
SiC	Silicon Carbide
SL	Switching Losses
SRC	Series Resonant Converter
SSL	Soft-Switching Losses
SST	Solid-State Transformer
UPS	Uninterruptible Power Supply
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Contents

1 Introduction

TODAY'S society and its future development is substantially influenced by the digital revolution and the globalization, which are two of the main drivers for economic growth. This is e.g. reflected in the exploding internet IP traffic, which will triple between 2016 and 2021 (cf. **Fig. 1.1**) whereby the vast amount of data has to be processed in highly energy-demanding data centers; furthermore, passenger and freight transportation on the ground, on the sea, and in the air is rapidly increasing. Due to the tremendous energy consumption, this growth is mainly happening at the expense of the environment. The conspicuous consequences of the resulting climate change, such as the rise of the CO_2 concentration, the global warming, and the rise of the sea level [1], have led to an increasing environmental awareness of society and politics.

To mitigate the effects of the climate change, e.g. in 2010 the European Commission defined the *Europe 2020* strategy [2], which states that by 2020 the greenhouse gas emissions should be reduced by 20...30 % compared to 1990, and the United Nations Climate Change Conference 2015 developed the *Paris Agreement*, whose main goal is to limit the long-term global average temperature increase to well below 2 °C compared to pre-industrial levels [3].

To achieve these goals, a significant decarbonisation of the transportation sector and the electricity generation sector, as well as a substantial increase in energy efficiency are necessary. Therefore, the consumption of fossil fuels has to be reduced, e.g. by the electrification of passenger cars and freight trucks, i.e. by utilizing so-called electric vehicles (EV), as well as the public transport sector. At the same time, the energy required by EVs and other large-scale consumers such as data centers has to be delivered from renewable sources, for instance

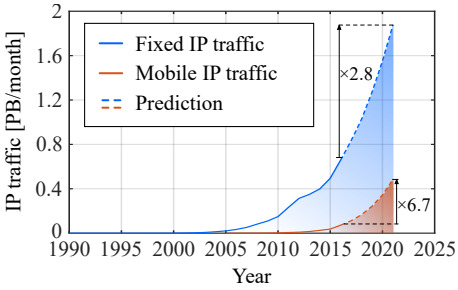

Fig. 1.1: Global internet IP traffic for fixed devices (computers) and mobile devices. Data originates from the Cisco Visual Networking Index [5] and [6].

wind power, solar power, and hydro power in order to reduce the environmental footprint sustainably. One example is the *Lefdal Mine Data Center* in Norway. Its energy consumption is growing from the current 10 MW to 200 MW over the next three years [4], but it is entirely powered from renewable sources.

Representative indicators to demonstrate the current development towards a more environmental-friendly energy policy are e.g. the global number of EVs and the installed renewable power generation capacity. **Fig. 1.2(a)** shows the evolution of the global number of EVs between 2013 and 2017 and as can be seen, the total number of EVs (battery electric vehicles (BEV) and plug-in hybrid electric vehicles (PHEV)) has significantly increased by almost a factor of 10 during this period. Furthermore, **Fig. 1.2(b)** shows the installed wind power and photovoltaic (PV) power generation capacity between 2000 and 2018, which has grown more than fivefold in the last 10 years.

One of the key technologies enabling this fundamental change in the power flow chain between the renewable energy sources and the consumers is power electronics, since e.g. EV batteries and data centers are low-voltage (LV) DC-loads, whereas the typical distribution grids are medium-voltage (MV)-AC grids, i.e. an MV-AC to LV-DC conversion is necessary for interfacing high-power DC-loads to the utility grid. On the generation side, if wind power and PV power is considered, another LV-DC to MV-AC conversion is required, since more and more modern wind-generators are incorporating variable speed drives [9–12] and hence, besides the PV panels, also represent DC-sources seen from their rectifier's DC-link.

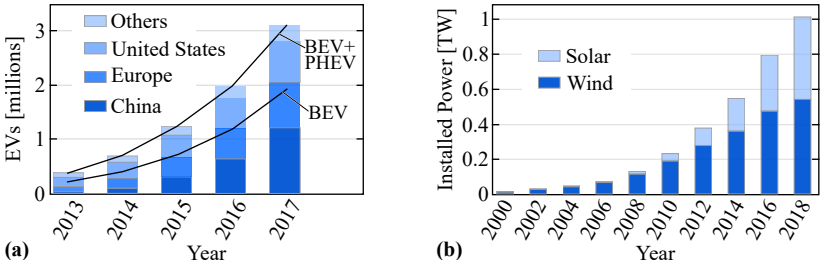

Fig. 1.2: **(a)** Evolution of the global EV stock. Data from [7]. **(b)** Global installed PV power and wind power generation capacity. Data from [8].

To interface an MV-AC grid to an LV-AC grid, usually low-frequency transformers (LFTs), which provide galvanic isolation and the required voltage transfer ratio between the primary-side and the secondary-side, are employed. In case an MV-AC to LV-DC conversion is required, a power electronic AC/DC conversion stage is added on the LV-side of the LFT, as shown in [13] for wind turbines, in [14] for PV power plants, in [15] for EV high-power battery charging, and in [16] for data centers.

1.1 Solid-State Transformer Characteristics and Applications

As a widely discussed alternative to LFTs, Solid-State Transformers (SSTs) could be used to interface an MV grid to an LV grid. There, the term SST (also referred to as Smart Transformer [17], Electronic Transformer [18], Intelligent Universal Transformer [19], Energy Router [20], or Energy Control Center [21]) represents a class of power electronic converters with medium-frequency (MF) galvanic isolation operating between an arbitrary MV grid and an arbitrary LV grid [22–25]. However, in contrast to LFTs, SSTs can not only operate between two AC grids [18, 19, 26–28], but can also directly interface DC grids either on the MV-side [29, 30], the LV-side [31–33], or on both sides [34–39].

The benefits of SSTs are mainly the controllability, i.e. reactive power compensation, fault handling, grid monitoring, and energy routing, as well as a potential increase in power density and efficiency compared to LFT-based solutions. However, it has been shown in [40] that typical SSTs perform worse than LFTs in AC/AC operation, but out-

perform the standard solution (LFT + AC/DC converter) in terms of lower weight, lower volume and lower losses when it comes to MV-AC to LV-DC conversions. Therefore, SSTs are especially well suited for the following applications:

- Data center power supplies [33, 41–43];
- MV-connected high-power EV battery charging [15, 32, 44–46];
- Integration of PV power plants into the MV-AC distribution grid [47–52];
- Connection of wind turbines to the MV-AC distribution grid [53–55];
- Integration of battery energy storage systems (BESS) into the MV-AC grid [13, 15, 48, 56];
- Traction applications [31, 57, 58];
- DC collection grids for large-scale renewable power plants [37, 39, 59–62];
- Integration of power-to-gas facilities for hydrogen generation into the MV-AC grid [63–65]

1.2 SSTs for Data Center Power Supplies

It is estimated that the information and communication technology (ICT) sector currently consumes 10 % of the world's generated electric energy [66] and e.g. in 2014, the 14 million installed servers in the U.S. consumed 1.8 % of the national electricity generation [67]. Furthermore, it is reported that 12 ... 27 % of the energy provided to data centers at MV level is dissipated in the power conversion stages which convert the voltage from several kilovolts down to the chip voltage level [42, 68, 69]. For economical and ecological reasons and due to the strongly increasing internet IP traffic (cf. **Fig. 1.1**) with the resulting demand for more computing power and hence for more electrical energy, the interest of research institutions and industry on more efficient data center power supplies has grown rapidly over the past decade.

Fig. 1.3(a) shows the traditional power supply chain in a data center from the MV-AC grid to the 12 V supply for the servers. An

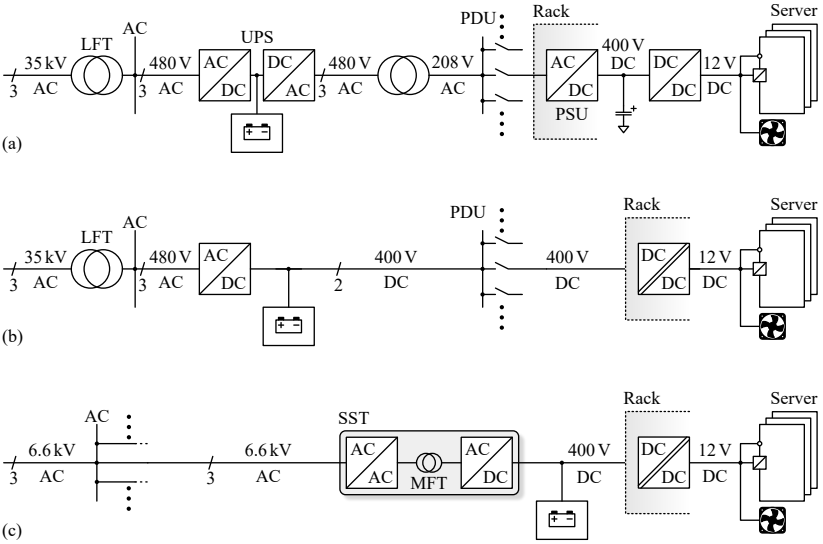

Fig. 1.3: (a) Traditional data center power supply chain from MV-AC to the 12 V DC server supply voltage. **(b)** Power supply chain based on 400 V DC distribution for a reduced complexity and increased efficiency. **(c)** SST-based power supply chain which allows to omit the LFT for an even higher efficiency and power density. The figures are taken from [70] and have been slightly modified.

LFT provides the galvanic isolation from the MV grid and transforms the voltage down to 480 V AC from where an uninterruptible power supply (UPS) with its backup batteries feeds another LFT, which is part of the power distribution unit (PDU), stepping down the voltage to 208 V, since the subsequent conversion stages are only rated for an input voltage range of 90 . . . 264 V [70]. The PDU then feeds the individual server racks, which contain a PFC rectifier and a 400 V/12 V DC/DC converter. As can be noted, there are several cascaded conversion stages, i.e. the total efficiency decreases with each conversion stage and hence is relatively low.

In order to increase the efficiency and to reduce the complexity (and therewith the probability of failure) of the power supply chain of data centers, a shift to 380/400 V DC distribution systems is considered [16, 69] and is partly already implemented [71]. **Fig. 1.3(b)** shows

the block diagram of a 400 V DC distribution-based data center power supply and as can be seen, the UPS, one LFT, and the rack-internal PFC rectifier can be omitted, whereby the backup batteries are now connected to the 400 V DC bus. Consequently, according to [72], an efficiency improvement of 7 % can be expected compared to the traditional power supply chain.

As a further step, SSTs are considered to provide a direct power electronic interface from the MV-AC grid to the 400 V DC bus, in order to improve the efficiency and the power density also of this part of the conversion chain [33,41,42]. There, the power supply of each server rack (which can reach power demands in the range of 20 ... 40 kW [68,73,74]) with a separate SST is intended. **Fig. 1.3(c)** shows the SST-based data center power supply chain, where the SST replaces the bulky LFT and the rectifier by directly interfacing the MV-AC grid. With this concept, the power could be distributed on MV level (e.g. 6.6 kV phase-to-phase rms, i.e. 3.8 kV rms phase-to-neutral) in the data center with the advantage of substantially lower realization efforts and/or cable cross sections and lower ohmic losses compared to LV distribution. Individual single-phase SSTs (single-phase for a low complexity) could then convert the MV-AC into 400 V DC and feed individual server racks or clusters, whereby the three phases of the MV utility grid could be symmetrically loaded. For a cost-effective construction of the building, it would be important that the SSTs are compact and lightweight. Additionally, the SSTs should allow a bidirectional energy flow, e.g. to feed energy from the 400 V DC bus back into the AC grid in case PV power is integrated in the 400 V DC bus and generates more power than required by the servers [75, 76].

To contribute to the reduction of the environmental footprint of data centers (and other applications that require an MV-AC to 400 V DC conversion), this thesis focuses on the realization of a highly efficient and highly compact SST for the supply of single server-racks.

1.3 System Specifications

From the considerations of **Section 1.2**, the system specifications given in **Tab. 1.1** arise for the bidirectional SST treated in this thesis. As can be seen, the efficiency goal of $\eta_{\mathrm{t,SST}} = 98\,\%$ is highly ambitious and has been defined by the *Swiss National Research Program 70* [77] as a part of the *Swiss Energy Strategy 2050*, which specifies a 13 % per

Tab. 1.1: SST Specifications.

Parameter	Symbol	Value
Power	P	25 kW
MV-side AC voltage (rms)	u_g	3.8 kV
LV-side DC voltage	$U_\mathrm{DC,LV}$	400 V
Mains frequency	f_g	50 Hz
Target efficiency	$\eta_\mathrm{t,SST}$	98 %

capita decrease of the electric energy consumption by 2035 compared to the year 2000. Therefore, a substantial increase in energy efficiency compared to standard solutions is necessary and will be one of the main goals of this thesis.

1.4 SST Key Challenges

1.4.1 Interfacing of the MV Grid

One of the key challenges of SST technology is the interfacing of the comparably high voltages with semiconductors on the MV-side of the SST. Up to now, this is typically solved by utilizing multilevel converters based on e.g. 1200 V . . . 1700 V SiC MOSFETs or IGBTs. However, this leads to highly complex topologies with a high number of components and a complex modulation. Instead of sharing the total blocking voltage among several converter cells, the recent development of MV SiC devices with blocking voltages in the 10 . . . 15 kV range enable the direct interfacing of MV with a single-cell converter. In this case, the complexity of the topology is significantly reduced, however for the price of the much more challenging handling of the MV SiC devices compared to LV devices and the insulation of the components for the full voltage instead of only a small share of the total voltage in case of the multi-cell approach.

1.4.2 Medium-Voltage Insulation

The electrical insulation of MV equipment in the AC distribution grid is well-known. E.g. high-power LFTs are typically oil-insulated and can withstand high overvoltages. However, since the power density of LFTs

is comparably low due to their low operating frequency, the additional isolation distances are small compared to the size of the LFT itself. In contrast, in case of SSTs where MF transformers with a considerably higher power density are incorporated, the isolation distances are much more significant. Furthermore, due to the higher power density, the surface area for the extraction of the dissipated heat through the insulation material is considerably lower and therefore, insulation materials with a high thermal conductivity are required for SST applications. Additionally, the combination of MV and MF imposes a high dielectric stress on the insulation [78], such that the insulation material has to feature a low dissipation factor and a high electric breakdown field strength to enable a compact MF MV transformer design. A detailed study on MF MV transformers is given in [79].

1.4.3 Efficiency, Power Density, and Cost

For power electronic converters (including SSTs), there is always an application-specific trade-off between efficiency, power density, and cost, among others [80]. When the state-of-the-art MV-AC to LV-DC solution, i.e. an LFT and a subsequent rectifier is taken as a reference, the SST-based solution can outperform the LFT solution regarding efficiency and power density, whereby the initial cost of an SST is typically higher [40]. However, the higher initial cost of SSTs can eventually be compensated by the lower operating costs due to the lower losses and therefore, the efficiency is one of the most important aspects for the design of SSTs. Considering that space in a data center is rare and thus very expensive (since it could be used for more servers, whose computation power would generate more revenue), the space consumption of the power and signal provisioning systems should be minimized. Accordingly, a high power density of the power supply is desired. This is underlined by the fact that the developed technology in this thesis is not limited to the use in data centers but can also be utilized in even more space-limited applications such as traction or more-electric aircrafts, i.e. a high power density of the developed SST is in general of high relevance.

1.4.4 Reliability

One highly important aspect from the perspective of utility grid operators but, e.g., also for data center operators is the reliability of the

equipment, since equipment failures can potentially cause high economic damage. Whereas LFTs are highly robust and can withstand e.g. lightning impulses, SSTs are much more sensitive and require more complex protection measures [81]. However, for the supply of data centers with a large number of SSTs as intended in this work, the protection measures could be implemented centrally, such that the individual SSTs are connected to a protected MV grid. Furthermore, the approach to supply each server rack with an individual SST automatically offers a high level of redundancy, i.e. if one SST fails, only one server rack is out of operation until the SST is replaced, without affecting the operation of the other servers. In this case, however, the faulty SST has to be disconnected from the MV-AC grid, which is not further discussed in this thesis. Nevertheless, failures of the SSTs have to be avoided by implementing e.g. overcurrent protection features and by a proper design of the MV insulation.

1.5 Suitable MV-AC to LV-DC SST Topologies

In the following, a brief overview over the most promising MV-AC to LV-DC SST topologies and their fundamental functionality is provided.

1.5.1 Isolated Back End SSTs

A common approach to interface an MV-AC grid without the use of MV semiconductors is the series connection of several AC/DC converter modules [42, 57, 58, 82, 83], as shown in **Fig. 1.4**. Thereby, the individual converter cells consist of a PFC AC/DC converter stage and a subsequent isolated back end (IBE) DC/DC stage. To decrease the turns ratio of the MF transformers and to achieve a natural voltage balancing among the converter cells [84], the outputs of the individual isolated DC/DC stages are connected in parallel, such that an input-series output-parallel (ISOP) configuration of the converter cells results. In order to minimize the boost inductance L_f, the AC/DC converters can be operated with phase-shifted carriers, resulting in a switched multilevel AC voltage u_ML, which closely follows the MV grid voltage u_g, and therefore leads to a small input current ripple. Even though multicell converters can achieve a high conversion performance and are very

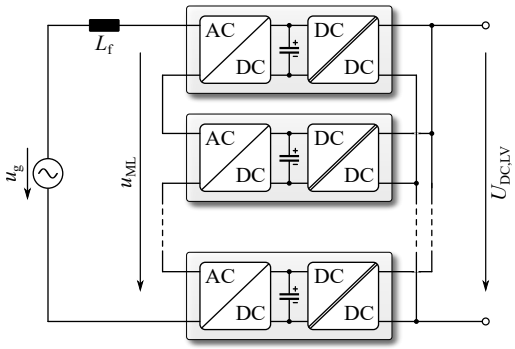

Fig. 1.4: Multi-cell isolated back end realization of an MV-AC to LV-DC SST. The ISOP-connected cells consist of a front end PFC AC/DC stage and an isolated back end DC/DC converter.

flexible due to their modularity, they are also highly complex due to the high number of switches, gate drivers, isolated auxiliary supplies, and voltage/current measurements.

1.5.2 Isolated Front End SSTs

In contrast to an IBE topology, the galvanic isolation can also directly be performed in the front end of the SST, whereas the current shaping is taking place subsequent to the isolation barrier [85, 86]. **Fig. 1.5** shows the isolated front end (IFE) topology, which consists of several ISOP-connected converter cells, each being realized as a series resonant converter (SRC) with bidirectional switches on the AC-side. The SRC is operated with a constant switching frequency and a 50 % duty cycle and, due to the isolation transformer and rectifier stage, generates an isolated and scaled |AC| voltage at its output (the capacitors on both sides of the SRC are comparably small and allow a full LF voltage swing). In case a variable interlock time is implemented, the SRC can be operated under soft-switching conditions [87], enabling a high switching frequency and therefore a compact design of the MF transformer. Eventually, a subsequent single |AC|/DC PFC boost converter performs the current shaping and generates the constant DC output voltage $U_{DC,LV}$.

The advantage of the IFE approach compared to the IBE approach

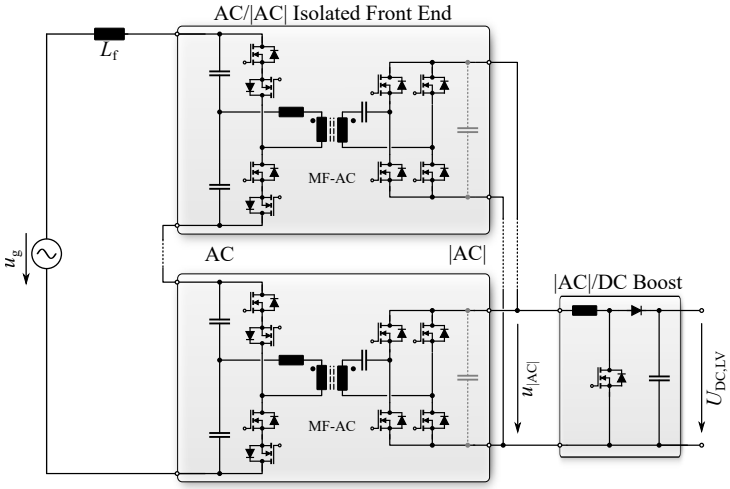

Fig. 1.5: Multi-cell realization of an isolated front end (IFE) SST where each converter cell employs bidirectional switches on the AC-side, an MF isolation transformer, and a rectifier bridge generating a scaled |AC| voltage $U_{|AC|}$. A subsequent single-cell |AC|/DC PFC boost converter shapes the current and generates the DC output voltage.

is the lower number of SiC devices on the MV-side and in general a lower complexity on the MV-side (e.g. no voltage or current measurements), since the current shaping is performed on the LV-side. However, the disadvantage of this topology is the low utilization of the semiconductor chip area and the MF transformer, since these components have to be designed for the peak AC current (and in case of the transformer for the peak AC magnetic flux density), and the resulting lower full-load efficiency compared to an IBE approach [85].

For the sake of completeness, it has to be mentioned that an IFE SST could also be realized as single-cell system employing MV SiC devices, whereby the same advantages and disadvantages as in case of a multi-cell system would appear.

1.5.3 Modular Multilevel Converter-Based SSTs

Another topology that does not require HV switches to interface an MV grid and has gained high interest since its patent registration in

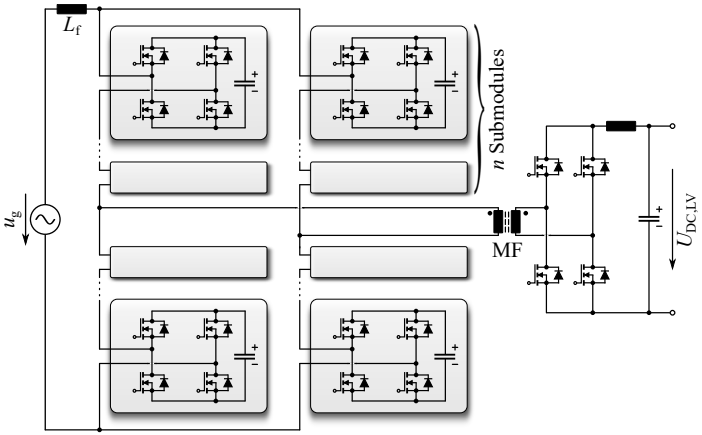

Fig. 1.6: Modular multilevel converter (MMLC) realization of an MV-AC to LV-DC SST.

2001 is the modular multilevel converter (MMLC) [88–90]. **Fig. 1.6** shows a variation of the MMLC, known from [33, 91], for interfacing an MV-AC grid to an LV-DC bus featuring galvanic isolation via an MF transformer. It consists of two inverter legs that are realized as a series-connection of several full-bridge submodules. With a suitable modulation scheme, the MMLC is able to generate an MF-AC voltage at the transformer terminals out of the MV-AC grid voltage without the necessity of supplying the individual submodules from their DC-side. However, in this case each of the converter arms (both inverter legs consist of an upper and a lower converter arm) has to be dimensioned to block the full peak AC grid voltage, which results in a very high number of semiconductors and associated circuitry. At the same time, this also leads to comparably high conduction losses due the high number of switches in the conduction path [33].

1.5.4 Single-Cell IBE SSTs Using MV SiC Devices

As already mentioned, with the new generation of 10 . . . 15 kV SiC MOSFETs, it is possible to interface the MV-AC grid directly with a single-cell converter. Due to the higher efficiency, the IBE topology is preferred over the IFE topology and in this case the SST consists of a single-cell AC/DC PFC rectifier followed by an isolated single-cell DC/DC con-

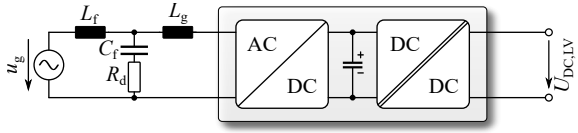

Fig. 1.7: Single-cell IBE realization of an MV-AC to LV-DC SST utilizing MV SiC devices to interface the MV-AC grid.

verter, as shown in **Fig. 1.7**. The EMI noise (which is higher compared multilevel converters due to the lower number of voltage levels) is limited by an additional LCL-filter in front of the PFC rectifier, which is a typical filter structure used for MV converters [58]. The isolated DC/DC converter can e.g. be realized as dual active bridge (DAB) converter or as SRC and is interfaced to the AC/DC stage via an intermediate DC-link. Due to the greatly reduced complexity compared to the multi-cell IBE and IFE topologies as well as to the MMLC approach, a higher power density and possibly also a higher reliability are expected. Furthermore, MV SiC devices with outstanding switching behavior enable completely new dimensions in terms of switching frequency and efficiency compared to standard devices.

In order to explore the limits in efficiency and power density of the single-cell IBE approach, this topology is selected, realized, and tested in detail in this thesis. There, 3$^{\text{rd}}$ generation 10 kV, 20 A SiC MOSFETs of type *CPM3-10000-0350* from *Wolfspeed* are used on the MV-side of the SST.

1.6 Previous Work

In 2017, *Fuji Electric* published an SST system (from now on referred to as *Fuji Electric SST*) for the power supply of IT equipment in data centers directly from the MV-AC grid [92]. The rated power is also 25 kW, and the input and output voltages are 2.4 kV AC (rms), and 54 V DC, respectively. Although the voltage levels are different from the system treated in this thesis, they are sufficiently close to use the *Fuji Electric SST* as a benchmark. The topology of one converter cell is shown in **Fig. 1.8(a)** and the system consists of five of these IBE cells in ISOP configuration. Furthermore, as can be seen, the topology only allows a unidirectional power flow from the MV-side to the LV-side,

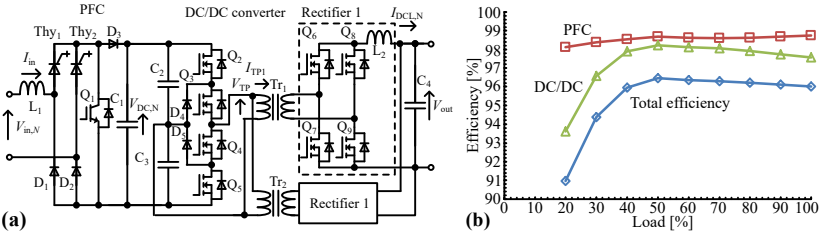

Fig. 1.8: **(a)** Power circuit topology of one of five ISOP-connected converter cells of the *Fuji Electric SST* and **(b)** measured efficiency. The figures are taken from [92].

whereas the SST discussed in this thesis features bidirectional energy flow.

Fig. 1.8(b) shows the measured efficiency curves of the *Fuji Electric SST* and the total efficiency reaches 96 % at full load. Furthermore, a power density of 0.4 kW/L is achieved [92].

1.7 Aims and Contributions

The objective of this thesis is the design and experimental analysis of a 10 kV SiC MOSFET-based 25 kW single-phase 3.8 kV AC to 400 V DC SST with a target efficiency of 98 %. Compared to the *Fuji Electric SST*, this efficiency means that the SST discussed in this thesis should feature half the losses. Furthermore, under this constraint, the power density of the SST should be maximized in order to make it suitable for volume restricted applications.

Besides these performance parameters, also the interaction between the MV-AC grid and the SST as well as the protection of the 10 kV SiC MOSFETs should be taken into account.

To achieve these performance goals and to enable a reliable operation of the SST in the grid, the following points, which have been identified as the main challenges, are treated in detail in this thesis:

- **Highly compact isolated gate driver power supply** - The gate driver of the high-side switch in a bridge-leg configuration is referenced to the switch-node potential and hence must be supplied with electrical energy in a galvanically isolated manner. To limit the CM currents arising from the fast switching transitions,

a low parasitic coupling capacitance across the isolation barrier is mandatory. Typically, air or tape insulated transformers are used in literature for 10 ... 15 kV SiC gate driver power supplies. However, these isolation transformers are showing a large volume [93–96] and in some cases even exceed the volume of the SiC module considerably [97, 98]. To enable an integration of the isolated gate driver into future MV SiC modules, which would significantly simplify the design of MV converters, a highly compact gate driver isolation transformer with a very low coupling capacitance is designed and realized utilizing a special transformer design and an advanced insulation material.

- **Ultra-fast overcurrent protection** - To avoid severe damage of MV converters, whose DC-link capacitors normally store comparably large amounts of energy capable of causing explosions of semiconductor modules, gate drivers for MV switches are typically equipped with an overcurrent protection (OCP) circuit. The reaction times of existing OCP circuits are usually in the microsecond range, and typically OCP circuits are only tested for the standard hard-switching fault (HSF) and the fault under load (FUL) scenarios. However, in MV applications, flashover faults (FOF) with extremely high $\mathrm{d}u/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ values can occur due to insulation failures and are much more critical to handle for an OCP circuit. Therefore, an ultra-fast OCP circuit is realized, which is able to clear a FOF at a DC-link voltage of 7 kV and protects the 10 kV SiC devices from damage even in this worst-case scenario.

- **Accurate calorimetric soft-switching loss measurement method** - Soft-switching losses (SSL) of MOSFETs are typically not given in the device datasheets and therefore have to be determined by measurements. A detailed error analysis shows that electrical measurement methods, such as the double pulse test, are highly inaccurate and hence unsuitable for the measurement of SSL of modern fast-switching SiC MOSFETs. Therefore, a highly accurate transient calorimetric measurement method is developed and used for the determination of the SSL of the employed 10 kV SiC modules. An interesting and important result of these measurements is that the antiparallel SiC JBS diode causes the largest part of the soft-switching losses of the 10 kV SiC module due to losses occurring during the charging/discharging of the parasitic

capacitance of the diode.

- **Impact of parasitics on the design of MV converters** - For LV converters it is commonly known that parasitic commutation loop inductances should be minimized in order to avoid excessive ringing and/or voltage overshoots during the switching transitions. For this reason, low-inductive packaging especially of fast-switching wide bandgap devices has significantly gained in importance with the development of modern SiC and GaN power devices. However, a theoretical analysis shows that parasitic inductances play only a minor role for the MV converter treated in this thesis. In contrast, for MV converters of this power class it is highly important to minimize parasitic capacitances in order to limit the occurring capacitive currents during the switching transitions. These findings have an important impact on the design of the 10 kV SiC MOSFET-based SST, since special attention has to be paid to achieve a low-capacitive design of e.g. the magnetic components and the PCB layouts.

- **Fully soft-switching SST topology** - Despite the outstanding switching performance of MV SiC MOSFETs compared to HV Si IGBTs, their hard-switching losses are still significant and are limiting the achievable efficiency and the power density of MV converters, since they define an upper bound for the switching frequency and hence inhibit the downsizing of passive components. To overcome these limitations, the SST topology is fully soft-switching and therefore, the efficiency and the power density are significantly increased compared to state-of-the-art SSTs. Specifically, a novel bidirectional soft-switching single-phase AC/DC converter topology is developed, whereas the bidirectional LLC series resonant DC/DC converter is operated with a novel modulation scheme to achieve soft-switching for all devices.

- **Calorimetric efficiency measurements** - The simplest method to measure the efficiency of a power electronic converter is to measure its input power and its output power and to calculate the ratio of both power values. However, for highly efficient systems in the range of 99 % efficiency, already small power measurement errors can lead to large errors in the resulting efficiency. A detailed measurement error analysis shows that electrical efficiency measurements are unsuitable for the determination of the efficiency

of the converters developed in this work. Therefore, the losses of the individual semiconductors and the magnetic components are measured with the help of calorimetric measurement methods leading to a significantly higher accuracy. Furthermore, with these measurement methods, the distribution of the losses among the different components within the converters can be determined.

- **EMI filter** - Existing standards for the maximum current harmonics generated by a converter in the MV grid only cover frequencies up to 2.5 kHz [99] or 9 kHz [100], since typically LFTs or converters with low switching frequencies are used in the MV-AC grid [50,101,102]. However, due to the low soft-switching losses of the latest generation of 10 kV SiC MOSFETs, switching frequencies in the 50 ... 100 kHz range are possible. Moreover, the lack of harmonic standards does not mean that no AC-side input filter is needed, since harmonics in this frequency range could e.g. lead to grid resonances or aging of insulation materials in MV cables due to heating from dielectric losses. Therefore, the existing IEEE 519 harmonic standard is extrapolated to higher frequencies and an LCL-filter is designed accordingly.

- **MV-AC cable resonances** - Most commonly, MV converters are connected to the utility grid via MV-AC cables with a certain length. From an electromagnetic field perspective, these cables can be regarded as almost undamped transmission lines with discrete resonance frequencies and high resonant gains. E.g., for a typical MV cable with a length of 500 m, the first resonance frequency is located at around 35 kHz. If the switching frequency of the AC/DC front end of the SST approaches one of these cable resonance frequencies, undesired current oscillations of significant magnitudes can occur. By adding the proposed passive and quasi lossless damping network between the LCL-filter and the MV cable, the oscillations can be completely avoided, independently of the cable length.

- **MV insulation** - One of the most challenging aspects during the design of an MV system is the electrical insulation of the individual components and the insulation coordination within the converter system. Due to the high voltages in combination with the high switching frequencies enabled by the 10 kV SiC MOSFETs under soft-switching conditions, a high dielectric stress is

imposed on the insulation material used to insulate e.g. magnetic components. Therefore, in case of standard insulation materials, considerable dielectric losses are generated, which could lead to local hot spots and finally to the destruction of the insulation. Consequently, to attain a reliable MV insulation, advanced insulation materials with a low dielectric dissipation factor and a high thermal conductivity are required in order to not only generate less dielectric losses, but also to extract the losses generated by the windings through the insulation material.

1.8 Outline of the Thesis

With the goal to guide the reader along the design and realization of the SST system, this thesis is divided into six chapters, which are briefly outlined in the following.

- The development of MV SiC MOSFETs with blocking voltages of 10 kV enables new levels of performance of MV-connected power electronic converters, but also demands for advanced isolated gate drivers and OCP circuits to fully and reliably utilize the potential of these novel MV SiC power semiconductors. Therefore, in **Chapter 2**, a highly compact isolated gate driver with an ultrafast overcurrent protection circuit is designed, constructed and experimentally verified with the goal to enable an integration of this circuitry into future intelligent 10 kV SiC modules in order to simplify the design and to increase the performance of MV converters.

- In **Chapter 3**, the soft-switching losses of the 10 kV SiC modules are determined experimentally, since the device datasheet does not provide any loss values for soft-switching (and for hard-switching). A detailed error analysis shows that electrical measurement methods are unsuitable for the measurement of soft-switching losses and therefore, a highly accurate transient calorimetric measurement method is developed and applied to the 10 kV SiC modules. Additionally, the hard-switching losses are also measured and compared to the soft-switching losses.

- For the design of the bidirectional 3.8 kV AC to 7 kV DC front end converter of the SST, the achievable performance is calcu-

lated in **Chapter 4** in case the standard hard-switched full-bridge PWM converter topology is employed. It is shown that the hard-switching losses significantly limit the efficiency and the power density, since a rather low switching frequency would have to be selected. To improve the efficiency and power density, the 10 kV SiC MOSFETs have to be operated under soft-switching conditions and to achieve this, a novel bidirectional soft-switching AC/DC converter topology, the *integrated* Triangular Current Mode (*i*TCM) topology is developed. Finally, the *i*TCM converter is designed and constructed with a special focus on the required inductors and their MV insulation, the AC-side LCL-filter and the problems arising from the connection of the converter to the MV-AC grid via an MV cable. The converter is experimentally verified at full load and its efficiency and loss distribution are determined accurately by calorimetric measurements.

- **Chapter 5** treats the bidirectional isolated 7 kV/400 V DC/DC converter, which provides the required voltage step down and the mandatory galvanic isolation of the SST. Since the AC/DC front end converter is able to control the voltage, the DC/DC converter can be realized as SRC operated at resonance frequency and therefore acting as "DC transformer", i.e. providing a quasi load-independent voltage transfer ratio. In order to achieve zero voltage switching (ZVS) for all devices in all possible operating points, a novel highly robust modulation scheme is developed. Furthermore, the MV MF transformer is Pareto-optimized and special attention is paid to its MV insulation. The DC/DC converter is constructed and experimentally verified at full load. Finally, the efficiencies and loss distributions of the transformer and the complete DC/DC converter are determined with calorimetric measurement methods with high accuracy.

- At the end of each chapter, short summaries of the obtained results are given and the key findings are highlighted. Final conclusions obtained from the presented study are summarized in **Chapter 6**. The achieved performance is discussed and compared to the *Fuji Electric SST*. Finally, the thesis is concluded with suggestions for potential future research areas.

1.9 List of Publications

Different parts of the research findings presented in this thesis have already been published or will be published in international scientific journals, conference proceedings, or workshops. The publications developed in the course of this thesis are listed below.

Journal Papers

- D. Rothmund, D. Bortis, and J. W. Kolar, "Highly Compact Isolated Gate Driver with Ultrafast Overcurrent Protection for 10 kV SiC MOSFETs," *CPSS Trans. Power Electron. and Appl.*, vol. 3, no. 4, pp. 278-291, 2018.
- D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99.1 % Efficient 10 kV SiC-Based Medium Voltage ZVS Bidirectional Single-Phase PFC AC/DC Stage," *IEEE J. Emerg. Sel. Topics Power Electron.*, 2018.
- D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99 % Efficient 10 kV SiC-Based 7 kV/400 V DC-Transformer for Future Data Centers," *IEEE J. Emerg. Sel. Topics Power Electron.*, 2018.
- D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate Transient Calorimetric Measurement of Soft-Switching Losses of 10 kV SiC MOSFETs and Diodes," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5240–5250, 2018.

Conference Papers

- D. Rothmund, D. Bortis, J. Huber, D. Biadene, and J. W. Kolar, "10 kV SiC-Based Bidirectional Soft-Switching Single-Phase AC/DC Converter Concept for Medium-Voltage Solid-State Transformers," in *Proc. IEEE Int. Symposium on Power Electron. for Distributed Generation Systems (PEDG)*, Florianopolis, Brazil, 2017.
- D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate Transient Calorimetric Measurement of Soft-Switching Losses of 10 kV SiC

MOSFETs," in *Proc. IEEE Int. Symposium on Power Electron. for Distributed Generation Systems (PEDG)*, Vancouver, Canada, 2016.

- D. Rothmund, G. Ortiz, T. Guillod, and J. W. Kolar, "10 kV SiC-Based Isolated DC-DC Converter for Medium-Voltage-Connected Solid-State Transformers," in *Proc. IEEE Appl. Power Electronics Conf. (APEC)*, Charlotte, NC, USA, 2015.
- D. Rothmund, G. Ortiz, and J. W. Kolar, "SiC-Based Unidirectional Solid-State Transformer Concepts for Directly Interfacing 400 V DC to Medium-Voltage AC Distribution Systems," in *Proc. IEEE Int. Telco. Energy Conf. (INTELEC)*, Vancouver, Canada 2014.
- D. Rothmund, J. E. Huber, and J. W. Kolar, "Operating Behavior and Design of the Half-Cycle Discontinuous-Conduction-Mode Series-Resonant-Converter with Small DC Link Capacitors," in *Proc. IEEE Workshop on Control and Model. of Power Electron. (COMPEL)*, Salt Lake City, UT, USA, 2013.

Workshops

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2

Highly Compact Isolated Gate Driver with Ultra-Fast Overcurrent Protection for 10 kV SiC MOSFETs

Silicon Carbide semiconductor technology offers the possibility to manufacture power devices with unprecedented blocking voltages in the range of 10 . . . 15 kV and superior switching characteristics, enabling switching frequencies beyond 100 kHz. To drive these 10 kV SiC devices, the power supply and the gate signal of the (high-side) gate driver require an appropriate galvanic isolation featuring a low coupling capacitance and a high $\mathrm{d}u/\mathrm{d}t$ ruggedness. Since currently no commercially available gate drivers for these specifications exist, a customized isolated gate driver is developed, which, in order to simplify the use of the MV SiC devices, is intended to be integrated into a future intelligent MV SiC module. For this purpose, a highly compact isolated gate driver with an isolation voltage rating of 20 kV is implemented and tested. The realized isolation transformer of the isolated power supply shows a volume of only 3.1 cm^3 and a coupling capacitance of only 2.6 pF, and has been successfully tested at 20 kV DC. Furthermore, an ultra-fast overcurrent protection (OCP) circuit is implemented to protect the expensive SiC modules from destruction due to overcurrents, which e.g. could result from false turn-on of both transistors of a bridge-leg or from short circuits of the load. The OCP circuit reacts within 22 ns to a fault and measurements prove that it can successfully clear both, a hard switching fault (HSF) and even a flashover fault (FOF), where one of the two switches of a bridge-leg configuration is subject to a flashover, in less than 200 ns for a DC-link voltage of 7 kV.

2.1 Introduction

Medium-voltage (MV) SiC devices with blocking voltages of 10...15 kV have gained significant interest in the recent years [105–113], since they enable the simplification of MV-connected power electronics by reducing the number of switches and associated isolated gate drivers compared to modular MV converters based on lower voltage devices [114, 115]. Therefore, possible applications for MV SiC MOSFETs and IGBTs are, besides HVDC transmission, e.g. Solid-State Transformers (SSTs) for future data center power supplies [33, 116, 117], high-power electric vehicle battery charging facilities [118, 119], traction applications [57,120], naval or marine on-board MV-AC or MV-DC distribution systems [121, 122] or even future all-electric aircrafts [123]. However, the MV SiC devices such as the one shown in **Fig. 2.1** feature extremely fast switching speeds with $\mathrm{d}v/\mathrm{d}t$ values of up to 100 kV/µs and, in case of SiC MOSFETs, extremely low soft-switching losses, which allow switching frequencies beyond 100 kHz for DC link voltages in the 5 . . . 10 kV range [124]. Consequently, standard isolated gate driver ICs as well as standard isolated gate driver power supplies and optocouplers are not applicable for the power and signal transmission to the high-side switches, since their isolation voltage rating and $\mathrm{d}v/\mathrm{d}t$ ruggedness are not sufficient. For these reasons, a customized gate driver circuit with a very low coupling capacitance, an isolation voltage in the range of 20 kV for the signal and the power path, and a high $\mathrm{d}v/\mathrm{d}t$ ruggedness are required to guarantee a reliable operation. Furthermore, in case of a fault, an overcurrent protection (OCP) circuit for the highly expensive SiC devices is desired.

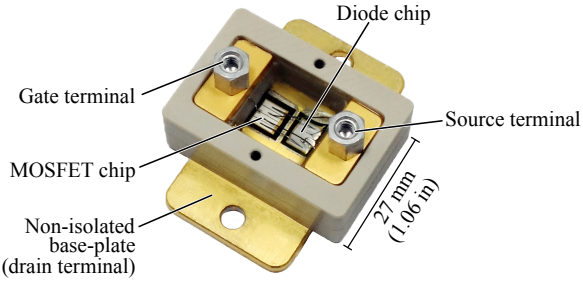

Fig. 2.1: Basic non-isolated 10 kV SiC module containing a SiC MOSFET chip and an antiparallel SiC JBS diode chip [103, 104].

Concerning the electrical performance, the isolated gate driver should in future be integrated into the SiC module, since this enables a reduction of the gate loop inductance and/or enhances the switching performance of the SiC MOSFET, as it is already reported for 650 V GaN and 1200 V SiC devices [125–127]. Moreover, the integration of the isolated gate driver and the OCP into an MV SiC module allows to significantly simplify the design process of MV converters, since the high voltages then only occur at the power terminals of the module, whereas the gate signals and the auxiliary power can be supplied to the module without any additional external isolation measures. Besides the simplification of the MV converter design, this also allows a substantial increase of the MV converter power density, especially by avoiding the large required creepage and clearance distances in air, which can be minimized using a proper insulation material in the isolation transformer and an according insulation coordination. Furthermore, in case of multi-level converters where the auxiliary power is e.g. drawn from the submodule capacitors [128], the integrated isolated power supply can significantly reduce the complexity of the required external auxiliary power supply circuitry.

Fig. 2.2 shows a schematic drawing of a possible future intelligent 10 kV SiC MOSFET module featuring an integrated isolated DC/DC

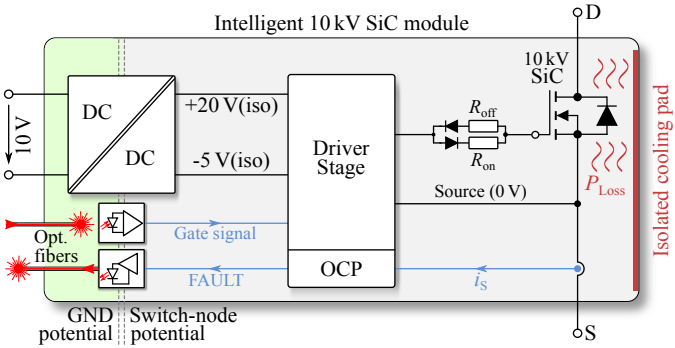

Fig. 2.2: Concept of a future intelligent 10 kV SiC module which also contains the isolated DC/DC converter for the supply of the (high-side) gate driver stage and a fiber optic receiver for the gate signal. Furthermore, an overcurrent protection (OCP) circuit is integrated, which in case of a fault safely turns off the MOSFET and sends an optically isolated FAULT signal to the supervisory control.

converter for the generation of the $+20\,\mathrm{V}/-5\,\mathrm{V}$ driving voltages, a fiber optic receiver and transmitter for the reception of the gate signal and the transmission of the FAULT signal, and the driver stage with an OCP circuit, which measures the device current and safely turns off the MOSFET in case of a fault. Advantageously, the heat is extracted via an isolated cooling pad, which could be realized with e.g. an aluminum nitride plate featuring a high thermal conductivity while at the same time providing electrical insulation. For the integration of the gate driver, the individual components must be highly compact, which is especially important for the isolated power supply, since the gate driver volume is mainly defined by the volume of the isolation transformer. Consequently, the volume of the isolation transformer V_{trans} has to be minimized, which is one of the main objectives of the following considerations.

In literature, most commonly air or tape-insulated transformers with discrete windings [94–98, 129] or PCB windings [93] are used to isolate the power supplies of gate drivers employed in MV SiC applications. In some cases however, these transformers are up to 10 times larger than the 10 kV SiC module shown in **Fig. 2.1**. This can be explained by the large creepage distances required in air (40 mm for 10 kV according to the International Standard IEC 60950-1 [130]). Furthermore, these isolation transformers must be placed in safe distance from other converter circuit components in order to not risk creepage currents, partial discharges or even dielectric breakdowns. In [131], a relatively compact current-transformer-based solution with a common AC-bus has been presented and is intended for the supply of several gate drivers at the same time.

Another possibility to realize the galvanically isolated gate driver power supply is to use inductive power transfer (IPT) coils [132–135]. However, since the electric breakdown field strength of air is comparably small, a large air gap and large creepage paths are necessary, i.e. the overall IPT system will be large and hence is not suited for an integration in a highly compact module.

A further method to supply electric energy to a floating gate driver circuit is to use an optical fiber [136]. Thereby, a powerful laser (e.g. 3...10 W optical power) feeds an optical fiber, which is connected to the laser receiver on the gate driver side converting the laser power back into electric energy. The advantage of this concept is the theoretically infinite $\mathrm{d}v/\mathrm{d}t$ immunity, since apart from the remaining intrinsic ca-

pacitance of the physical components, the coupling capacitance of the optical fiber is basically zero. Furthermore, no creepage distances to the laser receiver are required, such that compact gate driver circuits could be realized with this concept. However, it has to be mentioned that the laser transmitter is very large (e.g. 220 mm × 197 mm × 143 mm (8.66 in × 7.75 in × 5.63 in) for 3 ... 20 W optical power, cf. [137]) and thus is difficult to accommodate. The low receiver efficiency of only 25 % and the high costs are further disadvantages.

Therefore, a highly compact and cost-effective solution for the galvanically isolated power supply of the high-side gate driver circuits for 10 ... 15 kV SiC MOSFETs must be developed, which could be integrated in a future intelligent MV SiC power module.

Furthermore, the gate driver circuit should be equipped with an OCP in order to protect the 10 kV SiC devices (*Wolfspeed CPM3-10000-0350*) from destruction due to overcurrents and/or short circuits. A typical fault scenario is the shoot-through of a bridge-leg configuration, i.e. both switches are erroneously turned on, e.g. due to incorrect or distorted gate signals. For the switch turning on while the complementary switch is already in on-state, this type of fault is called hard switching fault (HSF). In contrast, the switch which is already in the on-state experiences a so-called fault under load (FUL) [138,139]. However, in MV applications, faults due to isolation and/or flashover failures are especially critical due to their extremely fast transients. Accordingly, these so-called flashover faults (FOF) are much more challenging to handle, and in order to also protect the MV SiC MOSFETs in this worst-case scenario, an OCP circuit with FOF clearing capability is developed.

The most common method for the implementation of an OCP is a desaturation detection circuit, which measures the device on-state voltage and compares it to a certain threshold voltage [136]. However, since during the turn-on transition a large blanking time is required until the device is in full on-state, the fault detection time is relatively high and potentially hazardous for the 10 kV SiC devices due to the high instantaneous power dissipation in the chip during e.g. an FOF. Furthermore, the drain voltage has to be sensed and blocked by several series-connected diodes, which have to be separated from the rest of the gate driver circuit by a certain creepage distance, which increases the gate driver volume [140]. As an alternative, the current could be measured with a shunt in the source path, or, if a Kelvin source contact is available (which is not the case for the 10 kV SiC modules at hand,

cf. **Fig. 2.1**), the voltage drop across the parasitic inductance between Kelvin source and power source can be measured and integrated to obtain the device current [141]. Unfortunately, both methods do not offer galvanic isolation, which potentially could lead to undesired CM distortions due to the extremely fast fault transients. Alternatively, the device current could be measured galvanically isolated with a Rogowski coil [142], which is, however, sensitive to external electric and magnetic fields and could therefore lead to false triggering.

In order to avoid the disadvantages of the mentioned OCP methods and to ensure a highly robust and fast protection, an air gapped current transformer in the source path of the MOSFET is used, which features galvanic isolation, a high bandwidth, and does not require a connection to the drain potential. The measured current is subsequently processed by a high-speed analog circuit, which reacts to a fault within 22 ns and safely turns off the device.

In the following, first the galvanically isolated power supply and the realization of the isolation transformer with minimum volume and coupling capacitance will be discussed (**Section 2.2**). Subsequently, the ultra-fast OCP circuit is described in **Section 2.3** and it is experimentally proven that it is able to safely clear both, an FOF and a HSF for a DC-link voltage of 7 kV. Finally, conclusions on the main findings are drawn in **Section 2.4**.

2.2 Isolated Power Supply

The isolated power supply has to provide electric energy to the driver circuit of the power MOSFET, which in case of the high-side switch is referenced to the switch-node potential, i.e. in case of 10 kV SiC MOSFETs to a floating rectangular voltage of e.g. 7 kV amplitude with a frequency of > 100 kHz, and $\mathrm{d}v/\mathrm{d}t$ values of up to 100 kV/µs. Therefore, besides providing the isolated $+20\,\mathrm{V}/-5\,\mathrm{V}$ driving voltages, the power supply needs to feature a sufficient electrical isolation voltage rating. Furthermore, the common-mode (CM) currents through the parasitic isolation transformer coupling capacitance C_{CM} must be kept sufficiently low in order not to disturb the proper operation of the gate driver and the protection circuits. Commercially available isolated power supplies, e.g. for 3.3 kV and 6.5 kV IGBTs, feature coupling capacitances in the range of $20 \ldots 25$ pF and a size of typically $50\,\mathrm{mm} \times 50\,\mathrm{mm} \times 20\,\mathrm{mm}$ [143, 144], whereby MV IGBTs are switching

Tab. 2.1: Specifications of the isolated power supply.

Property	**Symbol**	**Value**
Output voltages	$U_{\mathrm{DC1}}, U_{\mathrm{DC2}}$	$+20\,\mathrm{V}, -5\,\mathrm{V}$
Max. output power	P_{max}	$2\,\mathrm{W}$
Max. coupling capacitance	$C_{\mathrm{CM,max}}$	$3\,\mathrm{pF}$
Isolation voltage	U_{iso}	$20\,\mathrm{kV}$

with rather low $\mathrm{d}v/\mathrm{d}t$ values in the range of $10\,\mathrm{kV/\mu s}$ [145], which is 10 times slower than in case of 10 kV SiC MOSFETs. Consequently, in a 10 kV SiC MOSFET-based converter, C_{CM} must be reduced by roughly a factor of 10 in order to keep the peak CM current in the same range as for Si IGBT-based converters. Although there are devices such as described in [146] featuring an insulation voltage of 12 kV (for one minute) and a coupling capacitance of only 3 pF, the actual allowed operating voltage according to [130] is only 7.2 kV and due to the missing $\mathrm{d}v/\mathrm{d}t$ and CM frequency ratings, also these devices are unsuitable for MV SiC MOSFET applications. Therefore, a customized isolated power supply featuring appropriate insulation ratings has to be realized. However, with standard isolation transformer designs, a low coupling capacitance can only be realized by large distances between the windings and between the windings and the core, whereas on the other hand a significant downsizing is necessary for the integration of the transformer (cf. **Fig. 2.2**). To achieve both, a special transformer concept must be developed (cf. **Section 2.2.2**).

The power consumption of the gate driver circuit at hand is 600 mW at most during operation (including the optical fiber transceivers). In order to provide a sufficiently large margin (e.g. if several 10 kV SiC MOSFETs should be operated in parallel), the isolated power supply is rated for a power of $P = 2\,\mathrm{W}$. **Tab. 2.1** lists the specifications of the power supply as a basis for the design.

2.2.1 Isolated Power Supply Topology

Due to the high isolation voltage requirement of 20 kV, a certain isolation distance is required between the transformers' primary and secondary windings. Consequently, a comparably low magnetic coupling

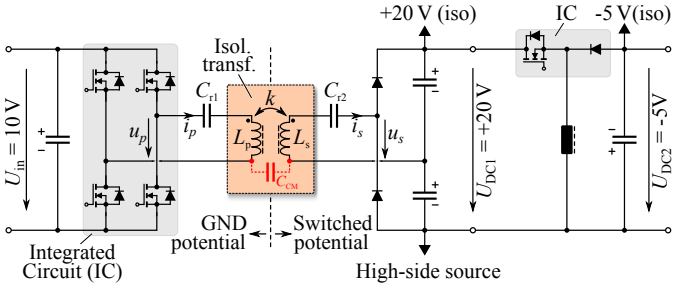

Fig. 2.3: Schematic diagram of the isolated power supply. The isolation transformer is operated in a series-series compensated configuration whereby $L_\mathrm{p} = L_\mathrm{s}$ and $C_\mathrm{r1} = C_\mathrm{r2}$. The subsequent voltage doubler rectifier generates +20 V DC, from where a buck-boost converter generates −5 V DC, which is used for the supply of the analog and logic ICs as well as for the negative biasing of the gate in the off-state of the 10 kV SiC MOSFET.

factor k and hence a relatively large leakage inductance results, which, if not compensated, leads to a load-dependent voltage drop and hence to a load-dependent output voltage of the gate driver supply. To still obtain a stable secondary-side voltage, a feedback-control would be necessary, which would, however, require an isolated transmission of the measured output voltage signal across the isolation barrier, i.e. additional effort which would further increase the risk of a failure of the supply.

To overcome this problem, a topology with a load-independent voltage transfer ratio, namely the series-series compensated resonant converter shown in **Fig. 2.3** is selected. It consists of an H-bridge inverter, a 1 : 1 isolation transformer (i.e. $L_\mathrm{p} = L_\mathrm{s}$), the resonance capacitors C_r1 and C_r2, and a voltage doubler rectifier generating 20 V DC for the positive gate bias of the 10 kV SiC MOSFET. The transformer leakage inductance is compensated by the resonance capacitors and the system is operated at the unity-gain operating point where the output voltage is independent of the load [147]. Furthermore, soft-switching of the primary-side full-bridge (realized with a *MAX13256* IC) can be achieved, enabling a high switching frequency and therefore a more compact design. Furthermore, in this operating point, the transformer currents are sinusoidal and hence beneficial in terms of low high-frequency (HF) losses due to skin-effect and proximity-effect, since no higher current harmonics are present.

According to [147], if only the resistances of the primary and the secondary windings are considered, the highest efficiency (i.e. the lowest rms currents) of the resonant system is achieved when the impedance of the secondary side is matched to the load impedance. For a maximum output power of $P_{\max} = 2\,\mathrm{W}$, a given secondary-side inductance L_s and a secondary-side voltage of $u_\mathrm{s} = U_{\mathrm{DC1}}/2 = 10\,\mathrm{V}$ (half the DC output voltage U_{DC1} due to the voltage doubler rectifier, cf. **Fig. 2.3**), the optimum operating frequency f_0 in order to fulfill the load matching condition at full load is given as

$$f_0 = \frac{8}{\pi^2} \cdot \frac{u_\mathrm{s}^2}{2\pi\sqrt{2} L_\mathrm{s} k P_{\max}}, \tag{2.1}$$

with k as magnetic coupling factor between the transformer's primary side and secondary side. To achieve a load-independent voltage transfer ratio, the resonance capacitors have to be dimensioned as [147]:

$$C_{\mathrm{r1}} = C_{\mathrm{r2}} = \frac{1}{(2\pi f_0)^2 L_\mathrm{s} (1-k)}. \tag{2.2}$$

In this operating point (which is slightly above the resonance), the phase angle of the input impedance seen by the full-bridge is

$$\varphi(Z_{\mathrm{in}}) = \arctan\left(\sqrt{2}\right) = 54.7^\circ \tag{2.3}$$

and hence guarantees ZVS operation of the MOSFETs due to the inductive behavior [147]. Furthermore, due to this particular compensation method, the primary-side rms current is independent of the inductances, the magnetic coupling, and the operating frequency, and can be calculated as

$$i_{\mathrm{p,rms}} = \sqrt{\frac{3}{8}} \cdot \pi \cdot \frac{P_{\max}}{u_\mathrm{s}} = 384\,\mathrm{mA}. \tag{2.4}$$

The secondary-side current is ideally in phase to the rectangular voltage applied from the rectifier and its rms value can be calculated as

$$i_{\mathrm{s,rms}} = \frac{P_{\max}}{u_\mathrm{s}} \cdot \frac{\pi}{2\sqrt{2}} = 222\,\mathrm{mA}. \tag{2.5}$$

2.2.2 Isolation Transformer

In conventional isolation transformers, the primary and the secondary windings are placed on the same magnetic core and are galvanically

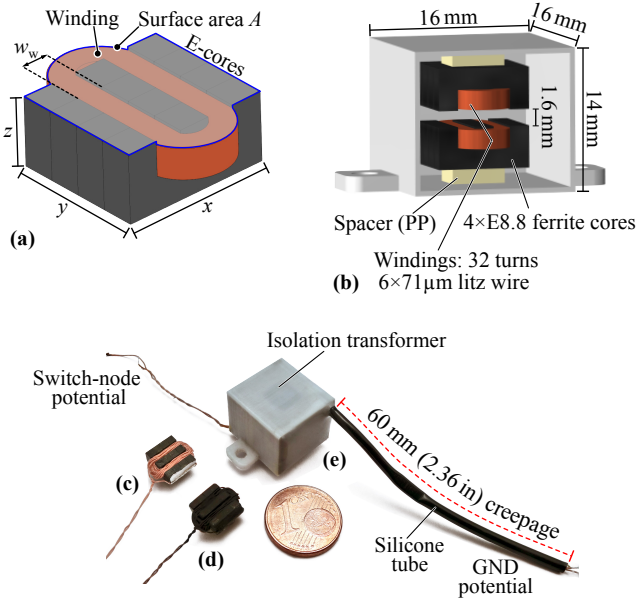

Fig. 2.4: **(a)** Ferrite core half (consisting of several stacked E-cores) with its corresponding winding. **(b)** CAD model of the isolation transformer (outer dimensions 16 mm × 16 mm × 14 mm, i.e. 0.63 in × 0.63 in × 0.55 in) showing the two windings on the ferrite cores, which are separated by a 1.6 mm gap. The 3D-printed housing is then filled up with a special silicone which provides the electrical insulation. **(c)** Picture of the winding (32 turns of 6 × 71 µm litz wire) on four stacked E8.8 ferrite cores. One end of the winding is electrically connected to the stacked cores with the help of conductive silver paint (silver color). **(d)** The whole arrangement is then coated with a semiconductive graphite layer (black color) to define an equipotential surface. **(e)** Photograph of the realized silicone-encapsulated isolation transformer. The necessary creepage distance is provided by the silicone tube.

isolated from each other by means of insulation material between the primary winding and the core, the secondary winding and the core, and between the primary and secondary windings. In case of the application at hand, the differential-mode voltage applied to both transformer windings is $< 50\,\mathrm{V}$ and hence, no further isolation between the primary winding and the core (which in this case would be tied to GND potential) would be necessary. However, the secondary winding would have

to be isolated from both, the core and the primary winding since it is floating on the switched potential of e.g. 7 kV. Consequently, the winding window and therewith the size of the entire magnetic core would have to be chosen sufficiently large, such that the secondary winding could be separated from the core and from the primary winding by approximately 1.6 mm of insulation material thickness to each side, if an (average) electric field strength of 4.5 kV/mm is allowed and the transformer is potted in a suitable insulation material. Since the transformer's power rating is only $P = 2\,\mathrm{W}$ but the isolation distances do not scale with the power but are defined by the isolation voltage, the required winding window would be large compared to the dimensions of a typical 2 W HF transformer without MV isolation and hence, this transformer concept is not suitable for achieving a low volume.

To overcome this limitation and to minimize the volume of the isolation transformer, as many isolation barriers as possible have to be omitted. Therefore, the primary winding and the secondary winding are wound on separate ferrite E-core halves without any isolation distance between the winding and the core. **Fig. 2.4(a)** shows a drawing of one of the core halves with its corresponding winding. There, the core consists of several stacked E-cores to achieve the desired form factor. The two core halves with their respective windings are then separated by a certain distance $d = 1.6\,\mathrm{mm}$ to keep the average electric field strength below 4.5 kV/mm in case of 7 kV CM voltage, similar to the air gap in a conventional transformer [42, 148]. The isolation distance between the two core halves is ensured by mounting them in a 3D-printed enclosure as shown in **Fig. 2.4(b)**. In operation, the primary winding is on GND potential, whereas the secondary winding floats on the switch-node potential. To also define the potential of the ferrite cores, they are connected to one end of the corresponding winding as shown in **Fig. 2.4(c)** and are covered with a thin layer of semiconductive graphite spray (cf. **Fig. 2.4(d)**) to tie the surface of all core halves to the potential of the respective winding. The surface resistance of the graphite spray (*Kontakt Chemie Graphit 33*) is $< 2000\,\Omega/\mathrm{sq}$, which is sufficiently low to define the potential of the surface and at the same time is sufficiently high such that no significant eddy current losses are generated by the high-frequency magnetic field [149]. As an alternative, semiconductive tape could be used to create an equipotential surface.

Consequently, this transformer arrangement can be regarded as plate capacitor from an electric field point of view, which allows to estimate

the coupling capacitance of the transformer as

$$C_{\mathrm{CM}} = \frac{\varepsilon_0 \varepsilon_{\mathrm{r}} A}{d}, \tag{2.6}$$

where A is the surface area of the core halves and the windings (cf. **Fig. 2.4(a)**) and d is the separation distance between the core halves. Since d is already fixed to $d = 1.6\,\mathrm{mm}$, the remaining geometry parameter to minimize the coupling capacitance is the surface area A. With a relative permittivity of $\varepsilon_{\mathrm{r}} = 4.12$ of the selected insulation material, the surface area must be lower than $132\,\mathrm{mm}^2$ to keep the coupling capacitance below the desired value of $C_{\mathrm{CM,max}} < 3\,\mathrm{pF}$, which is roughly 10 times lower than the coupling capacitance of commercially available isolation transformers. To fulfill this condition, four stacked E8.8 ferrite cores (material *N30*) are used ($x = 9\,\mathrm{mm}$ ($0.35\,\mathrm{in}$), $y = 8\,\mathrm{mm}$ ($0.31\,\mathrm{in}$), $z = 4.1\,\mathrm{mm}$ ($0.16\,\mathrm{in}$), cf. **Fig. 2.4(a)**), which results in an almost square-shaped form factor of the core surface, a surface area of $A = 108\,\mathrm{mm}^2$ (including the winding heads), and a theoretical coupling capacitance of $C_{\mathrm{CM}} = 2.5\,\mathrm{pF}$.

In order to analyze the electric field in the isolation transformer, a FEM simulation has been implemented and the simulated electric field distribution is shown in **Fig. 2.5**. As can be seen, the windings are field-free due to the shielding effect of the graphite coating. Furthermore, a high electric field only occurs between the limbs of the ferrite cores and is slightly lower between the windings (due to the slightly larger distance). To decrease the maximum electric field strength, the edges and corners of the ferrite cores have been rounded off and the maximum value of the electric field ($6\,\mathrm{kV/mm}$) is still a factor of four lower than the breakdown field strength of the used silicone encapsulant and therefore uncritical.

As can be noticed from the dimensions of the cores, the isolation gap is comparably large and hence, a rather low magnetic coupling factor k will result. Thus, the transformer acts similar to a pair of inductive power transfer (IPT) coils. There, larger primary-side and secondary-side inductance values are beneficial for ensuring a higher quality factor [150] and lower magnetizing current, and for this reason the number of turns wound on the two core halves should be as high as possible while the thermal limit has to be considered at the same time. Therefore, a maximum current density of $J_{\mathrm{max}} = 15\,\mathrm{A/mm}^2$ is defined. In order to keep the high-frequency losses due to the skin and proximity-effect to a moderate level, litz wire has to be employed for the

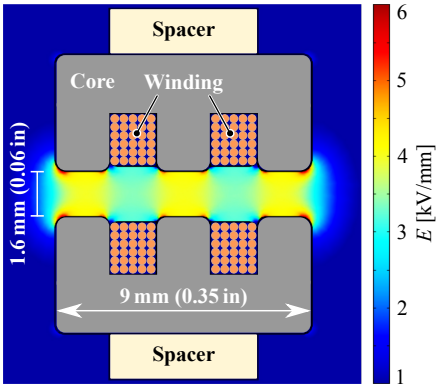

Fig. 2.5: Simulated electric field strength in the isolation transformer. The maximum occurring electric field strength (6 kV/mm) is still a factor of four lower than the breakdown field strength of the used insulation material (24 kV/mm).

primary and secondary windings. For a maximum expected operating frequency of $f_{\max} = 1\,\text{MHz}$, a skin-depth in copper of $\delta_{\text{Cu}} = 65\,\mu\text{m}$ results. Hence, as a compromise between the copper filling factor and the HF losses, a strand diameter of $d_{\text{s}} = 71\,\mu\text{m}$ is selected and with an assumed total copper filling factor of 25 % (i.e. 50 % litz-internal area utilization and a 50 % ratio between the winding area and the available core window area), the maximum achievable number of turns is 34. For practical reasons, a $6 \times 71\,\mu\text{m}$ litz wire and $N = 32$ turns is selected, resulting in a DC-resistance of $R_{\text{DC}} = 620\,\text{m}\Omega$.

To check the feasibility of the transformer design, the magnetic flux density in the ferrite core is determined, whereby it is assumed that the operating frequency is in the range of $[f_{\min}, f_{\max}] = [100\,\text{kHz}, 1\,\text{MHz}]$. Furthermore, due to the series-series compensation of the leakage inductance, the peak value of the sinusoidal voltage applied to the magnetizing inductance of the transformer is approximately equal to the fundamental component of the rectangular voltage applied from the primary side, i.e.

$$\hat{u}_{\text{m}} = \frac{4}{\pi} \cdot u_{\text{p}}. \tag{2.7}$$

Consequently, with the magnetic cross section area A_{m} of the core, the

peak magnetic flux density can be calculated as

$$\hat{B} = \int_0^{\frac{1}{4f}} \frac{\hat{u}_\mathrm{m}}{N \cdot A_\mathrm{m}} \sin(2\pi f t) \cdot \mathrm{d}t = \frac{2u_\mathrm{p}}{\pi^2 N A_\mathrm{m} f}, \tag{2.8}$$

resulting in $\hat{B} = 3.2\,\mathrm{mT} \ldots 32\,\mathrm{mT}$ for the assumed frequency range, which indicates that the ferrite cores are operated far below the saturation limit and hence the design is feasible from a magnetic perspective.

Thermal Model & Selection of the Insulation Material

For a prediction of the temperature distribution inside the transformer and especially in the insulation material which plays a central role for the transformer at hand, a thermal FEM simulation is conducted. As a basis for the simulation, the different loss components, i.e. winding losses, core losses, and dielectric losses are calculated first.

For an estimation of the worst-case winding losses, the AC winding resistance at the highest expected transformer operating frequency ($f_\mathrm{max} = 1\,\mathrm{MHz}$) is calculated. Considering the skin-effect and the proximity-effect, the winding losses can be calculated according to [151] as

$$P_\mathrm{Cu} = R_\mathrm{DC}\left(F_\mathrm{R}\hat{I}^2 + G_\mathrm{R}\hat{H}^2\right), \tag{2.9}$$

where F_R and G_R are the factors describing the skin-effect and the proximity-effect, and $\hat{H}$ depicts the temporal peak value of the magnetic field, which shows a triangular spatial distribution across the winding window width $w_\mathrm{w} = 1.65\,\mathrm{mm}$ (cf. **Fig. 2.4(a)**) and a spatial rms value of [152]

$$\hat{H}_\mathrm{srms} = \frac{N\hat{I}}{\sqrt{3}w_\mathrm{w}}. \tag{2.10}$$

By combining (2.9) and (2.10), the ratio between the effective AC resistance R_AC and the DC resistance R_DC can be derived [151]. For $f_\mathrm{max} = 1\,\mathrm{MHz}$, this factor is $R_\mathrm{AC}/R_\mathrm{DC} = 4.5$, i.e. the effective AC resistance is $R_\mathrm{AC} = 2.8\,\Omega$ for each of the two windings. With the calculated primary-side and secondary-side currents (cf. **Section 2.2.1**), the highest expected winding losses are $P_\mathrm{p,Cu} = 415\,\mathrm{mW}$ and $P_\mathrm{s,Cu} = 138\,\mathrm{mW}$.

Furthermore, a calculation of the core losses with the Steinmetz parameters for *N30* ferrite ($k_\mathrm{c} = 15.88$, $\alpha = 1.31$, and $\beta = 2.45$ [153]) and the determined values for the magnetic flux density leads to 4 mW

at $f = 100\,\mathrm{kHz}$ and $0.3\,\mathrm{mW}$ at $f = 1\,\mathrm{MHz}$, respectively, i.e. the core losses can be neglected.

Due to the comparably high electric field in the isolation transformer and the high switching frequency of the 10 kV SiC MOSFET bridge, the insulation material between the two core halves is exposed to a high dielectric stress and therefore, dielectric losses might become significant and would have to be considered. According to [154], the dielectric losses generated in a capacitance C_{CM} by a rectangular voltage with bottom value 0 V, top value U_{DC}, frequency f_{sw} and 50 % duty cycle can be calculated as

$$P_{\mathrm{d}} \approx \tan\delta \cdot C_{\mathrm{CM}} U_{\mathrm{DC}}^2 \cdot \frac{2 f_{\mathrm{sw}}}{\pi} \ln\left(\frac{2 e^{\gamma} f_{\mathrm{c}}}{f_{\mathrm{sw}}}\right), \tag{2.11}$$

where $\gamma \approx 0.57$ is the Euler-Mascheroni constant, and

$$f_{\mathrm{c}} = \frac{\ln\left(\frac{0.9}{0.1}\right)}{2\pi t_{\mathrm{rise}}} \tag{2.12}$$

is the corner frequency (cf. [154]). Furthermore, t_{rise} is the 10 %...90 % rise time of the switch-node voltage. Thereby, it is important to note that not only the fundamental frequency component of the switch-node voltage but also the higher order harmonics contribute to the dielectric losses. Equation (2.11) already includes the effect of the harmonics and as can be seen, the total dielectric losses are proportional to the dissipation factor $\tan\delta$, the switching frequency f_{sw}, and the square of the voltage, or the electric field, respectively. To show that it is important to select a suitable insulation material, the dielectric losses are first calculated for a typical epoxy-based insulation material, e.g. *Damisol 3418* whose dissipation factor is strongly frequency and temperature dependent [154] and is assumed to be $\tan\delta = 1.2\,\%$ for the following calculations. With a switch-node voltage of 7 kV, a switching frequency of $f_{\mathrm{sw}} = 125\,\mathrm{kHz}$ and a rise time of $t_{\mathrm{rise}} = 100\,\mathrm{ns}$, dielectric losses of $P_{\mathrm{d}} = 430\,\mathrm{mW}$ occur in the insulation material, which is very high compared to the rated power of the isolation transformer. Furthermore, epoxy resins typically feature a rather low thermal conductivity ($0.3\,\mathrm{W/(m\,K)}$ in this case), which means that the extraction of the heat generated by the dielectric losses is impeded and therefore could lead to a thermal runaway.

Fig. 2.6(a) shows the simulated temperature distribution inside the isolation transformer in case of epoxy resin as insulation material and a

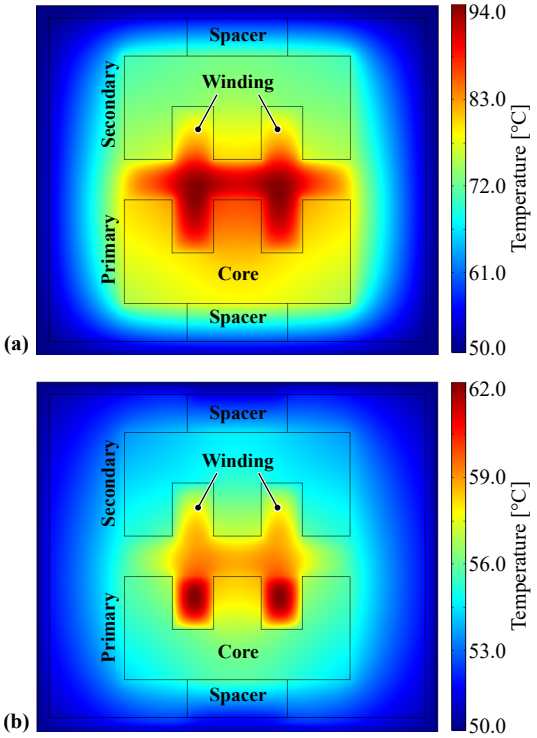

Fig. 2.6: **(a)** Thermal FEM simulation of the temperature distribution inside the isolation transformer in case of epoxy resin as insulation material and a boundary condition of 50 °C at the transformer housing surface. The dielectric losses dominate over the winding and core losses and a temperature increase of 44 K occurs in the insulation material between the core halves. **(b)** Temperature distribution in case of silicone (*Dow Corning TC-4605 HLV*) as insulation material. Due to the much lower dissipation factor and the higher thermal conductivity, the temperature increase is only 12 K in this case.

fixed housing temperature of 50 °C. As can be seen, due to the dielectric losses in the insulation material and the low thermal conductivity of the epoxy resin, a hot spot between the two core halves and a temperature rise of 44 K occurs. Since epoxy resins typically show a significant increase of their dielectric dissipation factor $\tan\delta$ which can reach values of $\tan\delta > 25\,\%$ at higher temperatures in the region of their glass transition temperature [154–156], a thermal runaway is very likely to

Tab. 2.2: Properties of the utilized silicone *Dow Corning® TC-4605 HLV*.

Property	Value
Dielectric strength	24 kV/mm
Dielectric constant ε_r	4.12 @ 100 kHz
Dissipation factor $\tan\delta$	0.63 % @ 100 kHz
Thermal conductivity	1 W/(m K)
Operating temperature	−45 ... 200 °C

happen (especially when a higher surface temperature of the isolation transformer is considered, e.g. the baseplate temperature of 100 °C of a SiC module, which also integrates the transformer, cf. **Fig. 2.2**) and therefore, epoxy resins are unsuitable for MV MF applications.

In contrast, silicone composites typically feature a very low and stable $\tan\delta$ up to temperatures over 200 °C. However, pure silicone rubber typically shows only a low thermal conductivity, which would potentially lead to an undesired heat accumulation similar to **Fig. 2.6(a)**. To increase this value, thermally conductive micro or nanoparticles can be added to the pure silicone, which, on the other hand, leads to an increasing dielectric dissipation factor [157]. Therefore, a compromise between a low $\tan\delta$ and a high thermal conductivity has to be made. The utilized material for the encapsulation of the isolation transformer at hand is the two-component silicone compound *Dow Corning TC-4605 HLV* and the properties of this material are listed in **Tab. 2.2**. With this insulation material, the dielectric losses are only $P_\mathrm{d} = 300\,\mathrm{mW}$. **Fig. 2.6(b)** shows the associated temperature distribution inside the isolation transformer and as can be seen, the temperature increase in the hot spot, which is now located inside the primary-side winding, is only 12 K due to the lower dielectric losses and the higher thermal conductivity. This shows that the selection of a proper insulation material is crucial for the functionality of a highly compact isolation transformer and consequently, with the selected material, the isolation transformer can be operated inside an intelligent 10 kV SiC module with an assumed baseplate temperature, i.e. transformer surface temperature of 100 °C, which would lead to a hot spot temperature of 112 °C inside the transformer.

For a reliable operation of the isolation transformer, the insulation material must be free of air-cavities or other impurities, which could lead to partial discharges and a degradation of the material over time. Therefore, a vacuum pressure potting (VPP) process is used, i.e. the silicone is devolatilized and the transformer is potted under vacuum (30 mbar) before the pressure is increased again to compress possible air or vacuum cavities. The still liquid silicone compound is then cured at a temperature of 120 °C for several hours. More details on the VPP process and the insulation material are given in [117].

In order to provide a sufficiently large creepage distance between the primary-side and secondary-side litz wire connections at the outside of the transformer, a silicone tube is covering the primary-side connecting wires (on GND potential) and is also potted in the silicone insulation material such that there is no other creepage path than the one along the silicone tube. The finalized isolation transformer is shown in **Fig. 2.4(e)**.

Determination of the Transformer Properties

Besides the inductances and the magnetic coupling factor k, which are required to determine the optimum operating frequency, also the parasitic coupling capacitance C_{CM} between the primary side and the secondary side is measured. For this purpose, a *HP 4294A Precision Impedance Analyzer* is used.

The measured value of the coupling capacitance is $C_{\mathrm{CM}} = 2.6\,\mathrm{pF}$, which matches very well with the calculated value of 2.5 pF. Considering the small transformer dimensions, this capacitance value is very low and ensures that the parasitic CM currents stay in a reasonable range even in case of high $\mathrm{d}v/\mathrm{d}t$ values of up to $100\,\mathrm{kV/\mu s}$.

The measurement of the primary-side and the secondary-side inductances leads to $L_{\mathrm{p}} = 23.7\,\mu\mathrm{H}$ and $L_{\mathrm{s}} = 23.4\,\mu\mathrm{H}$ and together with a measured leakage inductance of $L_\sigma = 22\,\mu\mathrm{H}$, the magnetic coupling factor (referenced to the primary side) can be calculated as

$$k = \sqrt{1 - \frac{L_\sigma}{L_{\mathrm{p}}}} = 0.27. \tag{2.13}$$

With these values, the optimum operating frequency $f_0 = 713\,\mathrm{kHz}$, and the values of the resonance capacitors $C_{\mathrm{r1}} = C_{\mathrm{r2}} = 2.88\,\mathrm{nF}$, can be determined with (2.1) and (2.2), respectively.

2.2.3 Experimental Verification of the Isolated Power Supply

For the experimental verification of the isolated gate driver power supply, different stress tests have been performed. To test the DC isolation rating of the designed transformer, a 20 kV DC voltage (which is almost three times higher than the maximum operating voltage of 7 kV) has successfully been applied between the transformer's primary and secondary windings for one hour without breakdown, temperature increase or measurable current flow through the isolation. This proves that the isolation concept is properly working and well overdimensioned to guarantee a long lifetime.

Furthermore, to also test the complete gate driver circuit and the

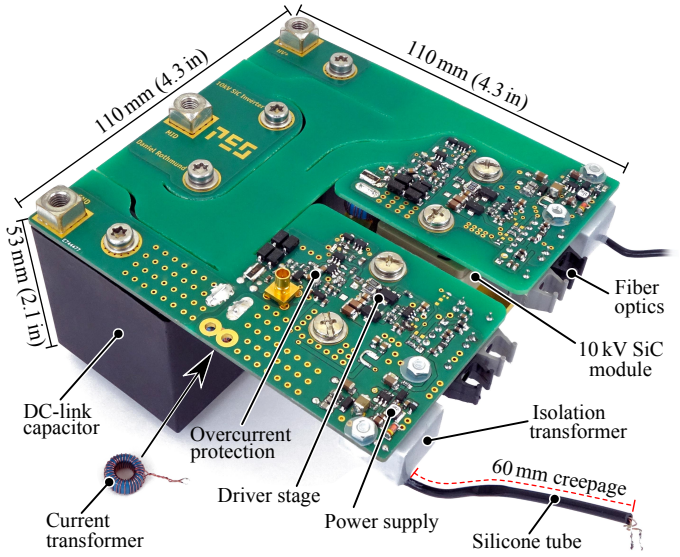

Fig. 2.7: Picture of the 10 kV SiC-MOSFET half-bridge. Due to the encapsulated isolation transformers, no additional isolation distances are required, enabling a highly compact design of the gate driver circuit and the half-bridge. The 10 kV SiC MOSFETs and the current transformers (cf. **Section 2.3.1**) are mounted below the PCB.

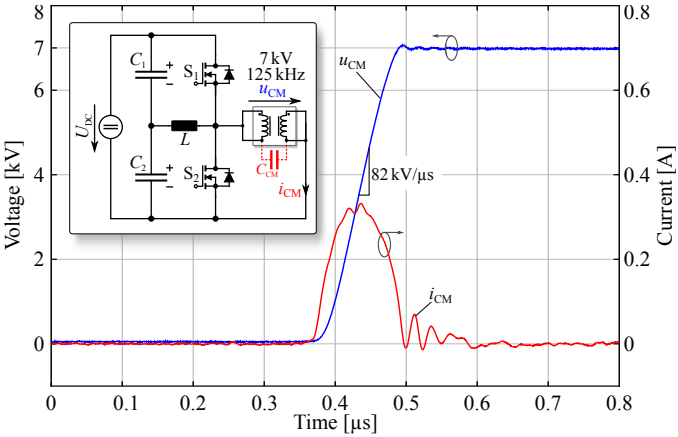

Fig. 2.8: Measured common-mode voltage u_{CM} across the isolation transformer together with the measured capacitive current i_{CM}.

isolation transformer under real operating conditions, a 10 kV SiC-MOSFET-based half-bridge inverter has been designed as shown in **Fig. 2.7**. It consists of a PCB which incorporates the low-side and the high-side MOSFETs together with their respective gate driver and isolated power supply circuits. As can be seen, the isolation transformers are placed on the bottom side of the PCB and enable the construction of a highly compact half-bridge due to their small dimensions. As already mentioned, the silicone tube provides a 60 mm creepage distance to the primary-side driving circuit of the isolation transformer (not shown), which only consists of a *MAX13256* H-bridge IC, an adjustable clock generator IC, and two ceramic DC buffer capacitors.

To expose the isolation transformer to a very high stress, the half-bridge has been operated with a DC-link voltage of 7 kV and a switching frequency of 125 kHz for one hour. There, an inductor has been used as load to enable ZVS and/or to minimize the switching losses of the 10 kV SiC MOSFETs [124]. During this test, the CM current of the high-side isolation transformer has been measured. The corresponding circuit diagram and the according voltage and current waveforms during a rising voltage transition are shown in **Fig. 2.8**. It can be seen that a $\mathrm{d}v/\mathrm{d}t$ of 82 kV/µs leads to a peak CM current of 300 mA. To obtain this peak current from the measured voltage slope, a coupling capacitance of

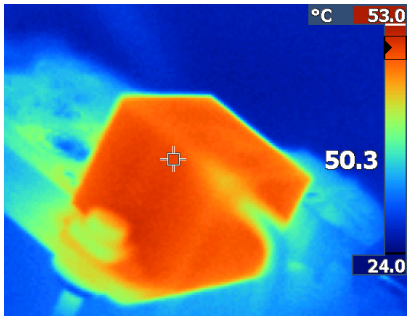

Fig. 2.9: (a) Thermal image of the isolation transformer under operation with a 2 W load and a CM voltage stress of 7 kV, 125 kHz. The average steady-state surface temperature reaches 50 °C under natural convection.

4.1 pF (which is 1.5 pF larger than the measured coupling capacitance of the isolation transformer) must be present. The additional capacitance can be explained by parasitic capacitances of the connection of the PCB to the isolation transformer and/or additional cable capacitances.

During the 7 kV, 125 kHz operation of the entire circuit with a load of 2 W, the steady-state surface temperature of the isolation transformer (cf. **Fig. 2.9**) reaches 50 °C (at an ambient temperature of 25 °C and for natural convection cooling), and as already shown by the thermal FEM simulation in **Fig. 2.6(b)**, the hot spot temperature is estimated to be around 62 °C.

2.3 Ultra-Fast Overcurrent Protection

In MV applications, it is highly recommended to implement an overcurrent and/or short circuit protection for the MV semiconductors due to the high voltages and the corresponding high energies in e.g. the DC-link capacitors, which could lead to serious damage of the hardware in case of a fault. Furthermore, MV SiC devices with blocking voltages of 10...15 kV are still very expensive and are up to now only available as prototype devices.

It is shown in [158] that single 10 kV SiC MOSFETs can survive approximately 8.5 µs under a full short circuit with 6 kV DC-link voltage. However, in [159], a clear relation between the degradation of the MOSFET-chip (i.e. increased $R_{\mathrm{DS,on}}$) and the short circuit duration is

apparent, since the degradation is an effect of the high temperature of the chip and its metallization during a short circuit. Additionally, in case of 10 kV, 100 A SiC MOSFET modules, a short circuit withstanding time of only 3.5 µs at 6 kV has been observed [160]. Therefore, the goal is to realize an ultra-fast overcurrent protection (OCP) with a very short reaction time in order to keep the thermal stress on the 10 kV SiC MOSFET chips as low as possible.

In literature, two major types of faults are described, namely the hard switching fault (HSF), where a MOSFET turns on into a short circuit, and the fault under load (FUL), where a short circuit occurs while the MOSFET is in on-state. In this case, however, the current and voltage slopes are limited by the switching speed of the turning on MOSFET, whereas in MV applications, flashover faults can occur due to insulation failures of e.g. the silica gel in MV semiconductor modules or the insulation material e.g. in the transformer employed in a DC/DC converter. Such faults lead to extremely fast voltage and current transients, which are much more critical to handle for an OCP. Accordingly, the standard HSF and FUL tests, which are currently used as measure for the quality of an OCP circuit, are not covering the actual worst-case scenario, namely an arc flashover across one of the MOSFETs in a bridge-leg configuration while the complementary MOSFET is turned on. Therefore, a flashover fault (FOF) test procedure is introduced where an FOF is applied to a 10 kV SiC MOSFET bridge-leg by using a gas discharge tube (GDT) of type *Bourns SA2-7200-CLT-STD* in the high-side position, which internally ignites a low-ohmic plasma (i.e. a solid short circuit) when the applied voltage exceeds its breakdown voltage, while the low-side switch is in on-state and has to clear the fault.

2.3.1 Functional Principle of the OCP

For the detection of a fault, the device current is measured by means of an air gapped current transformer in the source path of the 10 kV SiC MOSFET as shown in **Fig. 2.10**. Thereby, the air gap avoids the saturation of the core material due to the DC current component and compared to e.g. a current measurement shunt, the current transformer provides galvanic isolation of the measurement signal and improves the immunity against CM distortions.

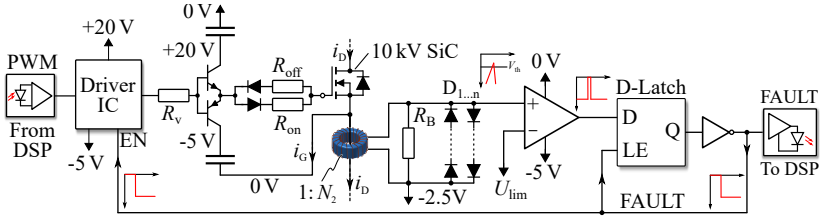

Fig. 2.10: Circuit diagram of the driver stage and the overcurrent protection. The drain current i_D of the MOSFET is measured via a $1 : N_2 = 1 : 30$ air gapped current transformer and the subsequent burden resistor $R_B = 1\,\Omega$. Once the threshold U_{lim} is exceeded, the comparator and consequently also the D-latch changes state and latches the FAULT state. This signal is fed back to the enable input EN of the driver IC (*UCC27531-Q1* from *TI*), leading to a turn-off of the 10 kV SiC MOSFET. The delay of the logic is approximately 22 ns. Furthermore, the FAULT signal is optically transmitted back to the supervisory control.

Design of the Current Transformer

For the measurement of the drain current of the 10 kV SiC MOSFETs, the current transformer has to be designed for a high bandwidth, such that fast overcurrent transients can be measured accurately. Furthermore, the current transformer should not add a significant signal delay to the protection circuit. Consequently, the leakage inductance and capacitance have to be kept small, which can be achieved by choosing a low number of secondary-side turns equidistantly wound on a toroidal ferrite core. As shown in **Fig. 2.10**, the secondary winding is connected to a burden resistor $R_B = 1\,\Omega$ where a current-proportional voltage is measured. If a voltage of 1 V across R_B is desired for an overcurrent threshold of $OCT = 30\,A$, a turns ratio of $1 : N_2 = 1 : 30$ results, i.e. the number of secondary turns on the current transformer is $N_2 = 30$. To operate the ferrite core material in its linear region, the maximum magnetic AC flux density is set to $B_{max,AC} = 75\,mT$ and for an assumed rectangular drain current with 50 % duty cycle, a minimum converter switching frequency of $f_{min} = 30\,kHz$, a bottom value of 0 A, and an amplitude of $i_{d,max} = 30\,A$, a core cross section of $A_m = 7.4\,mm^2$ is required. Therefore, a R10 × 6 × 4 ferrite core (N30 material) with a magnetic cross section area of $7.83\,mm^2$ is selected.

As the drain current of the switches is not a pure AC current but

rather a superposition of an AC and a DC current, the current transformer has to be designed appropriately, such that the DC component does not lead to saturation of the magnetic core. Therefore, an air gap is inserted in the ferrite core. For limiting the magnetic DC flux density to $B_{\mathrm{max,DC}} = 125\,\mathrm{mT}$, the required air gap length is

$$\delta = \frac{\mu_0 \cdot i_{\mathrm{D,DC}}}{B_{\mathrm{max,DC}}} = 150\,\mu\mathrm{m} \tag{2.14}$$

for a maximum DC current component of $i_{\mathrm{D,DC}} = 15\,\mathrm{A}$.

The air gap, however, causes the magnetizing inductance of the current transformer to drop significantly, which increases the AC magnetizing current. For the current transformer at hand, the peak magnetizing current for $f_{\mathrm{min}} = 30\,\mathrm{kHz}$ and 30 A, 50 % duty cycle operation is 7 % of the measured current value, which does not influence the detection of a HSF or an FOF due to the usually large resulting fault currents. For the sake of completeness, it should be noted that the current transformer represents a high-pass system (corner frequency $f_{\mathrm{c}} = 17\,\mathrm{kHz}$) and is not able to measure DC currents, since the DC component only occurs as magnetizing current on the primary side.

Detection of an Overcurrent

In the configuration shown in **Fig. 2.10**, the current transformer is placed below the gate and source contacts of the driver stage, which ensures that only the drain current i_{D} is measured. The secondary side of the current transformer is connected to a burden resistor $R_{\mathrm{B}} = 1\,\Omega$ and the entire circuit is powered from the $0\,\mathrm{V}/-5\,\mathrm{V}$ rails. Since the drain current of the 10 kV SiC device can also be negative, one terminal of the current transformer is connected to a locally generated $-2.5\,\mathrm{V}$ potential, allowing a voltage swing of $\pm 2.5\,\mathrm{V}$ across R_{B}, which corresponds to a drain current of $\pm 75\,\mathrm{A}$. In case of a fault, where much higher currents can occur, the diodes $\mathrm{D}_{1\ldots\mathrm{n}}$ start conducting and clamp the voltage across R_{B} in order to protect the input of the subsequent comparator from overvoltages. The advantage of diode strings compared to a single TVS or Zener diode per direction is the steeper characteristic of pn diodes, i.e. the clamping voltage is less current dependent. The type and the number of series connected diodes is selected such that a clamping voltage of 2.5 V results.

For the detection of an overcurrent, the voltage at the upper rail of R_{B} is compared to the threshold voltage $U_{\mathrm{lim}} = -2.5\,\mathrm{V} + 1\,\mathrm{V} = -1.5\,\mathrm{V}$

(for an overcurrent threshold of 30 A, $R_{\mathrm{B}} = 1\,\Omega$ and $N_2 = 30$) by an ultra-fast comparator. Once the threshold is exceeded, the comparator sets its output to HIGH (0 V) and the subsequent D-latch changes state and latches its output state when LE is LOW (−5 V). This FAULT signal (cf. **Fig. 2.10**) is connected to the enable input EN of the gate driver IC *UCC27531-Q1* from *TI*), which then initiates a turn-off of the 10 kV SiC MOSFET. The delay caused by the logic ICs and the gate driver IC adds up to $T_{\mathrm{react}} \approx 22\,\mathrm{ns}$ between the detection of the overcurrent and the reaction of the gate voltage. Since the gate driver IC does not provide a sufficiently high gate current (but undervoltage lockout, which is the reason for using an IC at all), a BJT totem-pole stage is used to provide a sufficiently high gate current. The gate resistors for turn-on and turn-off are $R_{\mathrm{on}} = 20\,\Omega$ and $R_{\mathrm{off}} = 10\,\Omega$, respectively, according to [124]. Alternatively, a soft turn-off circuit could be implemented, which, in case of a fault, turns off the device with a larger gate resistor as it is done for IGBTs to limit the voltage overshoot. Furthermore, the FAULT signal is also transmitted back to the supervisory control via an optical fiber (30 ns delay) in order to turn-off all devices in the converter system in case of an overcurrent in one of the 10 kV SiC devices. Accordingly, when a fault is detected, after 22 ns, the inner fault loop initiates the turn-off of the device which detected the overcurrent, and after approximately 100 ns, the gate voltages of all other 10 kV devices react. It should be noted that alternatively a direct feedback path to the gate could be implemented for a further reduction of the reaction time.

2.3.2 Flashover Fault Simulation

Before the OCP is tested in hardware and has to show that it is able to safely clear a HSF and an FOF at 7 kV DC-link voltage, a simulation is carried out in order to predict the behavior of the circuit under these extreme conditions. **Fig. 2.11 (a)** shows the simulation model of the bridge-leg in case of an FOF, where an ideal switch is located in the high-side MOSFET position and the low-side MOSFET is replaced by a simple equivalent circuit consisting of a voltage controlled current source, the nonlinear parasitic MOSFET capacitances, the antiparallel body diode, and the package inductances [122]. The current source is controlled by the internal gate voltage $u_{\mathrm{GS,int}}$ across the gate-source

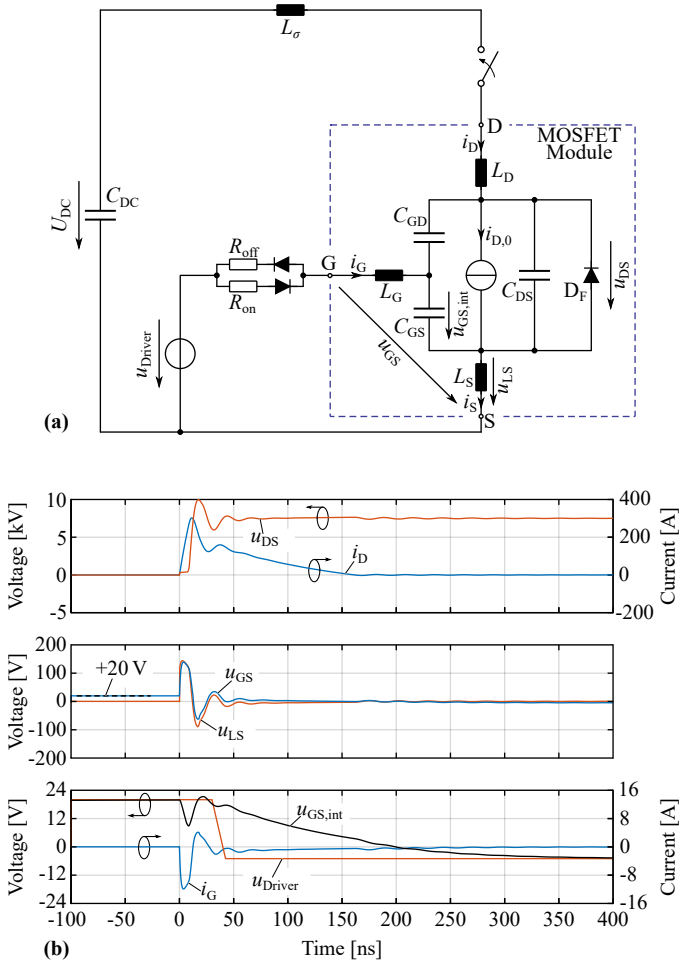

Fig. 2.11: **(a)** Schematic diagram of the MOSFET bridge-leg during a flashover fault (FOF), i.e. a flashover across the high-side MOSFET during the on-state of the low-side MOSFET. For the simulation, the low-side MOSFET is replaced by a simple equivalent circuit consisting of a gate-source voltage-controlled current source and the nonlinear MOSFET capacitances. **(b)** Simulated waveforms during a 7.6 kV FOF. The fault is cleared successfully and although the gate-source voltage u_{GS}, measured at the module terminals, reaches 140 V, the chip-internal gate-source voltage $u_{GS,int}$ is almost unaffected (voltage drop mostly occurring across the parasitic gate inductance and the gate resistor) and the MOSFET is not endangered.

capacitance C_{GS} via

$$i_{\mathrm{D},0} = g_{\mathrm{m}} \left(u_{\mathrm{GS,int}} - U_{\mathrm{th}} \right), \tag{2.15}$$

where U_{th} is the threshold voltage of the MOSFET and g_{m} is its transconductance. In the simulation, the ideal switch is closed at $t = 0$ while the low-side MOSFET is already turned on, i.e. $u_{\mathrm{Driver}} = 20\,\mathrm{V}$. Furthermore, it is assumed that the overcurrent protection will react 30 ns after the fault and will force the driver output voltage u_{Driver} to $-5\,\mathrm{V}$ within another 15 ns.

Fig. 2.11(b) shows the simulated waveforms under these assumptions. Initially, the drain current i_{D} rises with a very high $\mathrm{d}i/\mathrm{d}t$, which in turn induces a high positive voltage $u_{\mathrm{LS}} \approx 140\,\mathrm{V}$ across the source inductance L_{S}. The relatively large gate-source capacitance C_{GS} however keeps its voltage $u_{\mathrm{GS,int}}$ constant and therefore, the external gate-source voltage u_{GS} closely follows the induced voltage u_{LS} with a 20 V offset, while the effect of the gate inductance L_{G} can be neglected in this case. Since also the driver voltage u_{Driver} is still clamped to 20 V, the difference of $u_{\mathrm{GS}} - u_{\mathrm{Driver}} \approx 140\,\mathrm{V}$ peak is applied to the turn-off gate resistor $R_{\mathrm{off}} = 10\,\Omega$, forcing a part of the MOSFET channel current through C_{GS} and leading to a negative gate current of $i_{\mathrm{G}} = \left(u_{\mathrm{GS}} - u_{\mathrm{Driver}} \right) / R_{\mathrm{off}} = -14\,\mathrm{A}$ peak (when the gate inductance L_{G} is neglected). The reader should note that the gate resistors and the diodes should be well dimensioned to withstand the high peak current. Consequently, C_{GS} is discharged (i.e. $u_{\mathrm{GS,int}}$ decreases) and according to (2.15), the MOSFET channel current $i_{\mathrm{D},0}$ decreases again, as can be seen in the figure. Although the channel current decreases, the series inductances L_{S}, L_{D}, and L_{σ} try to keep the current constant and hence, a part of the drain current i_{D} commutates to the output capacitance C_{DS}, resulting in a rapid increase of the drain-source voltage u_{DS} and an inductive voltage overshoot. At the same time, the drain current effectively decreases, and the complete process until this point takes place without any action from the gate driver and is therefore referenced as "self turn-off" of the MOSFET. However, at this point, the decreasing drain current leads to a positive gate current due to the negative induced voltage across L_{S}, such that the MOSFET partly turns on again. Now, the induced voltage is applied to $R_{\mathrm{on}} = 20\,\Omega$, which is twice the value of R_{off} and therefore, the increase of the drain current is only small and the oscillation is damped. Furthermore, it is assumed that the OCP detects the overcurrent within 30 ns and switches the driver

voltage u_{Driver} to $-5\,\mathrm{V}$, thereby actively turning off the remaining drain current. Depending on the application, a higher turn-on gate resistor might be selected to dampen the oscillation even more.

As can be seen in **Fig. 2.11(b)**, due to the self turn-off mechanism and the short reaction time, the OCP is able to clear the FOF within 200 ns, whereby a peak drain current of 320 A is reached. Furthermore, it can be noted that the chip-internal gate-source voltage u_{GS} barely exceeds 20 V and hence stays within the absolute maximum ratings, i.e. the MOSFET chip is not endangered.

2.3.3 Experimental Results

FOF Experiment

Since the results from the FOF simulation show that the OCP is able to successfully clear an FOF in theory, this situation is also tested in real hardware. There, as shown in the schematic in **Fig. 2.12**, the low-side MOSFET is permanently turned on while the high-side MOSFET is substituted by a gas discharge tube (GDT) of type *Bourns SA2-7200-CLT-STD* and the DC-link voltage is increased until the GDT ignites. **Fig. 2.12** shows the measured drain-source voltage u_{DS}, the gate-source voltage u_{GS}, and the drain current i_{D} during an FOF test with a 7.2 kV GDT, which ignited at 7.6 kV (due to tolerances). As can be seen, the waveforms are similar to the simulation, i.e. also in real hardware a self turn-off occurs. Thereby, the drain current reaches a value of 350 A and the drain-source voltage rises in 6 ns to the DC-link level with an unprecedented $\mathrm{d}v/\mathrm{d}t$ of 1.2 MV/µs (which is close to the 100 MHz bandwidth limit of the used voltage probe). The OCP then actively clears the fault within 150 ns and the successful FOF test proves the proper functioning of the OCP under the most extreme conditions. Compared to the simulation, the measured waveforms show more oscillations in the drain current, which can be explained by the fact that the simulation model does not include all parasitics and non-linear effects in the MOSFET. Furthermore, in the experiment, only the external gate-source voltage can be measured and reaches a value of 150 V peak. The simulation shows a very similar external gate-source voltage, which solely occurs due to the inductive voltage drop across the source inductance L_{S}, whereas the gate-source voltage directly on the MOSFET chip does not exceed 20 V during the FOF, which is therefore also assumed for the real FOF experiment.

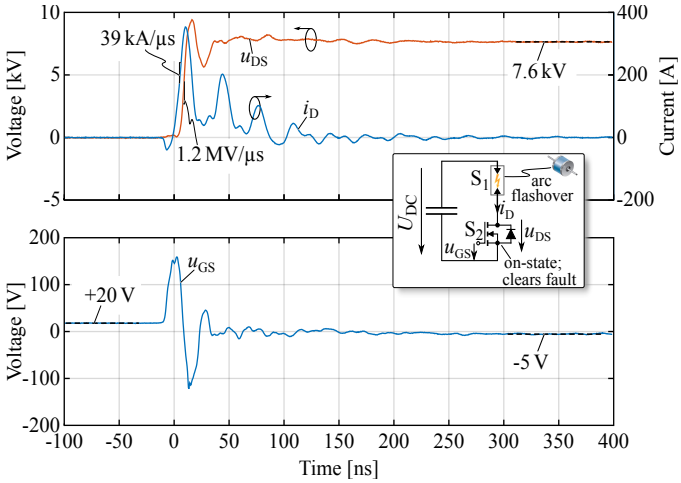

Fig. 2.12: Measured waveforms in case of a flashover fault (FOF) for a DC-link voltage of 7.6 kV. S_2 is in the on-state while S_1 fails to short, e.g. due to an isolation breakdown, which is reproduced with a flashover in a gas discharge tube (GDT) of type *Bourns SA2-7200-CLT-STD*. The current rises with a slope of 39 kA/µs and reaches its peak of 350 A. Due to the self turn-off mechanism, the MOSFET turns itself off and the drain-source voltage rises to the DC-link level within 6 ns, i.e. an unprecedented $\mathrm{d}v/\mathrm{d}t$ of 1.2 MV/µs occurs. After the reaction delay of approximately 22 ns, the gate driver actively brings the gate voltage to −5 V and the fault is cleared within 150 ns.

If the 10 kV SiC module featured a Kelvin source contact, the MOSFET would not be subject to a self turn-off during an FOF, since the gate loop would be decoupled from the power path. However, according to [159], the maximum short circuit current (in case of a usual FUL or HSF) of similar 10 kV SiC MOSFETs from Wolfspeed is self-limited by the MOSFET channel to 270 A for a DC-link voltage of 6 kV and therefore, the presented OCP would also work for modules featuring a Kelvin source contact.

HSF Experiment

The schematic in **Fig. 2.13** shows the situation for the HSF test, where the high-side MOSFET S_1 is in the on-state when the low-side MOS-

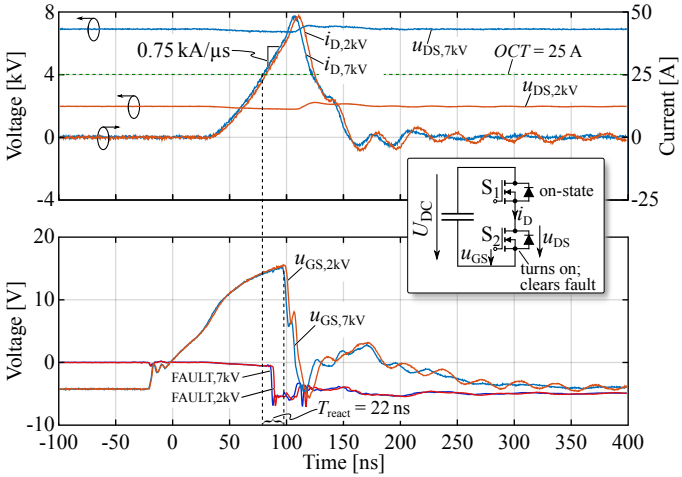

Fig. 2.13: Measured waveforms for a hard switching fault (HSF) for $U_{DC} = 2\,kV$ and $U_{DC} = 7\,kV$. S_1 is in the on-state when S_2 turns on. 22 ns after the drain current reaches the overcurrent threshold (OCT), the gate voltage reacts and S_2 is safely turned off within 150 ns. Almost independently of the DC-link voltage level, the current reaches a maximum of 48 A.

FET S_2 turns on. The measured waveforms of the drain current i_D, the drain-source voltage u_{DS}, the gate-source voltage u_{GS}, and the FAULT signal are shown for a HSF at 2 kV and 7 kV, respectively. With the increasing gate-source voltage, the drain current increases and once it reaches the threshold (25 A in this case), after a short delay the internal FAULT signal, which is connected to the enable input of the driver IC, changes state. The gate driver IC then switches its output to −5 V and the gate-source voltage decreases after the IC's propagation delay has passed. Almost independently of the DC-link voltage, a peak current of 48 A peak is reached and the OCP safely clears the HSF in less than 200 ns. The total reaction time from the point where the current threshold is reached until the gate voltage reacts is $T_{react} = 22$ ns in this case. It should again be noted that a successful HSF experiment alone does not mean that the OCP can protect the switch comprehensively. Only in combination with a successful FOF experiment, it can be stated that the OCP is able to protect the device also in worst-case fault situations.

2.4 Summary

In this chapter, a highly compact isolated gate driver for 10 kV SiC MOSFETs with ultra-fast overcurrent protection is presented. A main challenge for medium-voltage (MV) gate drivers is the galvanic isolation of the gate driver power supply and the low propagation delay isolated signal transmission. In order to obtain a highly compact gate driver circuit, which could be integrated into future MV SiC modules, an encapsulated isolation transformer employed in a resonant converter topology is designed and constructed. There, in contrast to classical transformers with both windings on the same magnetic core, the primary winding and the secondary winding are wound on separate ferrite core halves, which are separated by a small gap that is filled with a silicone insulation material featuring a low dielectric dissipation factor and a high thermal conductivity to ensure a sufficient heat transport from the windings to the surface of the transformer. The dimensions of the realized transformer are 16 mm × 16 mm × 14 mm and the coupling capacitance is only 2.6 pF. The transformer isolation has been successfully tested for 1 hour with a 20 kV DC voltage and for one hour with a 7 kV, 125 kHz switching-node voltage, which proves the functionality of the designed MV isolation transformer.

Furthermore, in order to protect the 10 kV SiC devices from overcurrents and from a possible destruction by short circuits, an ultra-fast overcurrent protection (OCP) circuit is implemented. Thereby, the drain current of the device is measured via a gapped toroidal current transformer. The measured signal is subsequently compared to a predefined threshold by an ultra-fast comparator whose output signal is latched in case of a fault and fed back to the enable input of the gate driver IC, which then initiates the turn-off of the 10 kV SiC device. The delay between the crossing of the overcurrent threshold and the reaction of the gate voltage is only ≈ 22 ns. Measurements prove that the realized OCP is also able to successfully clear a flashover fault (FOF) and a hard switching fault (HSF) at a DC-link voltage of 7 kV within less than 200 ns. Furthermore, during the FOF experiment, an unprecedented $\mathrm{d}v/\mathrm{d}t$ of 1.2 MV/µs has been observed.

Compared to a similar gate driver for 10 kV SiC MOSFETs [93], the gate driver developed in this work is more than a factor of five smaller (while achieving a similar coupling capacitance) and features a 25 times faster OCP circuit.

3

Transient Calorimetric Measurement of Soft-Switching Losses of 10 kV SiC MOSFETs and Diodes

The characterization of soft-switching losses (SSL) of modern HV SiC MOSFETs is a difficult but necessary task in order to provide a sound basis for the accurate modeling of converter systems, such as MV-connected SSTs, where soft-switching techniques are employed to achieve a high converter efficiency. Switching losses, in general, are typically measured with the well-known double-pulse method. In case of SSL measurements, however, this method is very sensitive to the limited accuracy of the measurement of the current and voltage transients, and thus is unsuitable for the characterization of fast switching HV SiC MOSFETs. Therefore, an accurate and reliable calorimetric method for the determination of SSL is developed and applied to 10 kV SiC MOSFET modules. Measured characteristics of the SSL are presented for different DC-link voltages and switched currents. Furthermore, a deeper analysis concerning the origin of the SSL is performed. With the proposed measurement method, it can be experimentally proven that the largest share of the SSL arises from charging and discharging the output capacitance of the MOSFET module and especially of the antiparallel junction barrier Schottky (JBS) diode.

3.1 Introduction

Soft-switching techniques are widely used in power electronic converters for the reduction of switching losses (SL) and EMI emissions, especially in DC/DC applications [161–165] and also in AC/DC and DC/AC applications [166–169]. Although wide bandgap devices such as SiC MOSFETs offer superior switching behavior compared to silicon devices [105, 170–173], the SSL of these devices (especially for high blocking voltages in the range of 10 kV) are not negligible. Therefore, it is important to consider the SSL during the design process, especially in case of higher switching frequencies. However, most of the device datasheets only provide data for hard-switching losses (HSL) which means that it is necessary to experimentally determine the SSL of the particular devices. Since SSL are typically small compared to HSL and conduction losses (CL), it is very challenging to measure SSL accurately under different operating conditions such as different chip temperatures and independently of external factors such as the PCB-layout and parasitic inductances of e.g the DC-link capacitors.

There are basically two types of switching loss measurement methods, namely electrical and calorimetric methods. Electrical methods, such as the well-known double-pulse test, feature the advantage of a rather short measurement time, since only pulse measurements have to be performed. Furthermore, with the same measurement setup both, the HSL and the SSL can be directly determined at different chip temperatures by electrically measuring the device voltage and current during a turn-on and a turn-off transient. However, due to the fast switching transients, the accuracy of the measured waveforms strongly decreases and thus, the measured SL can be highly inaccurate. The limiting factors are, e.g., improper deskew and jitter between the current and voltage probes, signal offsets and amplitude errors, limited bandwidths of the passive or active probes, or any other measurement distortion such as CM noise. In addition, also the post-processing of the measured waveforms is very crucial, e.g. the selection of the proper interval in which the measured power has to be integrated in order to extract the correct loss energy.

In contrast to electrical measurements, with a calorimetric measurement setup, the semiconductor losses, i.e. the sum of the SL and the CL, are determined by measuring the dissipated power of the device under test (DUT) in continuous operation and, since no fast switching tran-

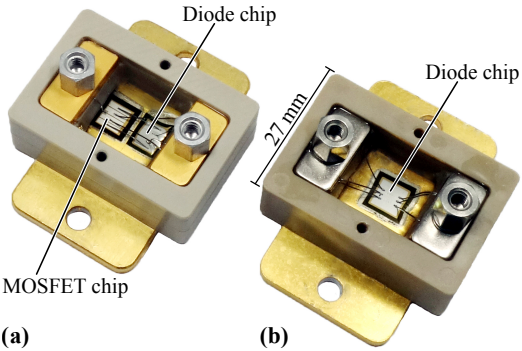

Fig. 3.1: Pictures of the 10 kV SiC devices: **(a)** Co-Pack module with a SiC-MOSFET chip and an antiparallel SiC JBS diode chip, **(b)** discrete packaged 10 kV SiC JBS diode.

sients have to be measured, typically a higher measurement accuracy is achieved. However, the higher accuracy is reflected in a much longer measurement time due to the large thermal time constants of calorimetric measurement setups. There, the total semiconductor losses can be measured either in the thermal equilibrium or in the transient heat-up phase.

Nevertheless, in both calorimetric measurement methods, the CL (which might be in the same range as the SSL) have to be subtracted from the total measured semiconductor losses, in order to obtain the pure SL. Hence, the accuracy achieved with calorimetric measurements strongly depends on the accurate determination of the CL. In principle, the CL can be calculated based on the DUT's on-state resistance $R_{\mathrm{DS,on}}$ given in the manufacturer's datasheet. However, the $R_{\mathrm{DS,on}}$ of the 10 kV SiC MOSFET examined (*CPM3-10000-0350* from *Wolfspeed*, cf. **Fig. 3.1 (a)**), shows a strong dependency on the device current, the chip temperature, the current direction (above approximately 4 A, the antiparallel junction barrier Schottky (JBS) diode (*CPW3-10000-Z020B* from *Wolfspeed*, cf. **Fig. 3.1 (b)**) starts conducting) and even deviates from device to device by more than 20 %, because the MOSFETs at hand are prototype devices.

As can be noticed, both types of measurement methods (electrical and calorimetric) show certain disadvantages in terms of accuracy and separation of switching and conduction losses. However, there is no

quantitative comparison of the measurement accuracy of different measurement methods so far. Therefore, in **Section 3.2**, an overview of electrical and calorimetric measurement methods is given. Based on the performed error analysis it becomes clear that electrical measurement methods known up to now could lead to tremendously wrong results and thus are not suited for SSL measurements. On the other hand, the accuracy achieved with calorimetric measurements strongly depends on the accurate determination of the CL.

In order to separate the CL and the SL directly in the measurement, a novel calorimetric SSL measurement method featuring a superior measurement accuracy is proposed in **Section 3.3**. In **Section 3.4**, this method is applied to the aforementioned 10 kV SiC MOSFETs. The obtained SSL for different DC-link voltages, currents and gate resistors are presented and can be utilized e.g. in the design optimization of MV converters [28, 174, 175]. Furthermore, even though the measured SSL are small, a deeper analysis concerning the origin of the SSL is performed, since they cannot be explained by the overlapping of the MOSFET's drain-source voltage and drain current during the switching transients. Therefore, it is assumed that the SSL are arising to a large extent from the charging and discharging of the parasitic output capacitances of the MOSFET and the antiparallel JBS diode, as also stated in [176,177]. In **Section 3.5**, this assumption is experimentally verified with the proposed measurement method, which on the one hand allows to measure the charging/discharging losses, and on the other hand enables to allocate them to the MOSFET and the JBS diode. To provide a complete data set for the SL of the 10 kV SiC modules at hand, in **Section 3.6** also the HSL are measured and compared to the SSL. **Section 3.7** finally summarizes the chapter.

3.2 Existing SL Measurement Methods

3.2.1 Electrical Measurement Methods

A commonly used electrical method for the measurement of SL is the double-pulse test which is originally intended for the measurement of HSL. **Fig. 3.2(a)** shows the double-pulse test circuit, which consists of a half-bridge, a split DC-link and an inductor. **Fig. 3.2(b)** shows the measured waveforms during a 8 kV, 10 A double-pulse experiment. There, for the measurement of HSL, the low-side MOSFET S_2 is turned

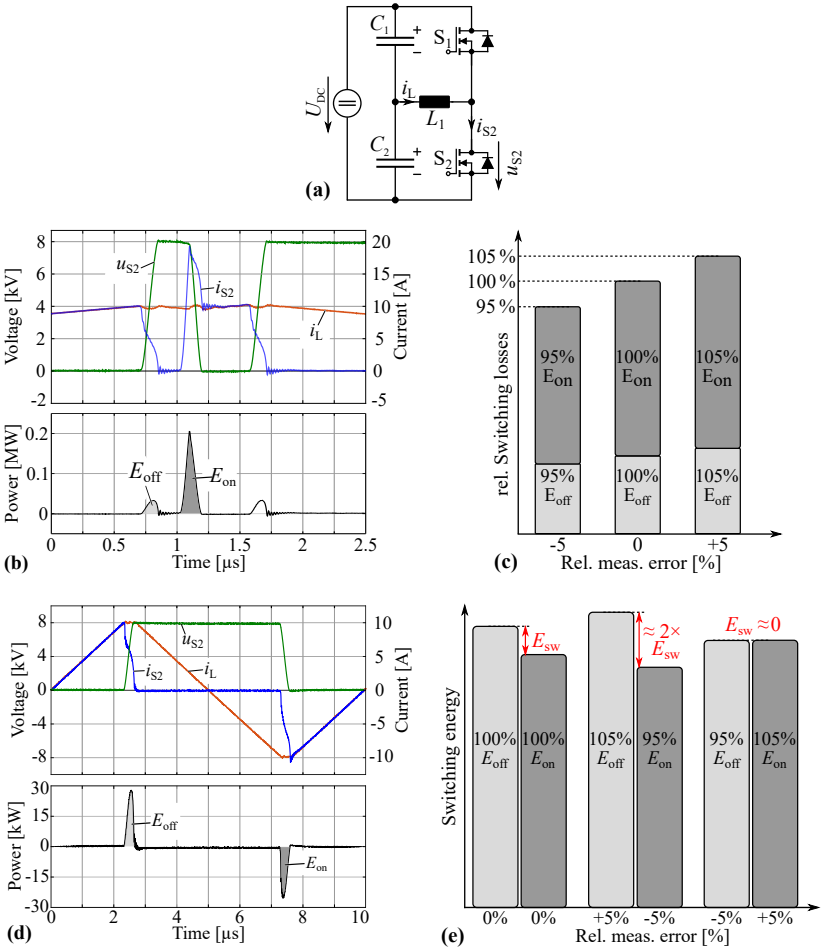

Fig. 3.2: **(a)** Circuit diagram for electrical switching loss measurements. **(b)** Hard-switching waveforms of the inductor current i_{L}, the drain current i_{S2}, and the drain-source voltage u_{S2} of MOSFET S_2 together with the resulting switching energies E_{on} and E_{off}. **(c)** Resulting HSL errors for different switching energy measurement errors. **(d)** Soft-switching waveforms and the corresponding switching energies E_{on} and E_{off}. Note that E_{on} is negative, i.e. energy is regained. **(e)** Soft-switching losses E_{sw} as difference between the absolute values of E_{on} and E_{off}. Small switching energy measurement errors lead to large SSL errors.

on until the desired current in the inductor is reached. S_2 is then turned off and S_1 is turned on (under zero voltage), whereby the turn-off energy E_{off} can be determined by integrating the product of the drain-source voltage u_{S2} and the drain current i_{S2} of MOSFET S2, as indicated in the lower part of **Fig. 3.2(b)**. Shortly after, when the inductor current has not yet changed significantly, S_1 is turned off and S_2 is turned on again. There, the current first commutates from the MOSFET channel of S_1 to its antiparallel diode and is then commutated to the turning on MOSFET S_2. As shown in **Fig. 3.2(b)**, a large transient current occurs through S_2, which is the reverse recovery current of the complementary diode and the capacitive charging current. The corresponding turn-on energy E_{on} can be determined again by the integration of the product of the drain-source voltage u_{S2} and the drain current i_{S2} of MOSFET S_2. As can be seen, both switching energies are positive (i.e. dissipated), while E_{on} is much higher than E_{off} in this case. As shown in **Fig. 3.2(c)**, the total HSL are obtained by adding E_{off} and E_{on} and due to this fact, if the switching energies are prone to a small measurement error of e.g. 5 % each, the total HSL error is as well ±5 %. Therefore, the double-pulse test is well suited for the measurement of HSL.

By adapting the modulation scheme, the double-pulse circuit from **Fig. 3.2(a)** can also be used for the measurement of SSL. Thereby, the switches are continuously operated with a 50 % duty cycle, such that a triangular and offset-free current i_L is formed in the inductor, as shown in **Fig. 3.2(d)**. The switching frequency and the inductance L_1 are selected in such a way that the desired turn-off current (10 A at $U_{DC} = 8\,\text{kV}$ in this example) is reached at the switching instants. For a positive inductor current, the DUT S_2 performs a soft turn-off under ZVS conditions, whereas it turns on under zero voltage for a negative inductor current.

In contrast to the HSL measurements, the turn-on energy in case of soft-switching operation of the bridge-leg is now negative, as can be seen in the lower part of **Fig. 3.2(d)**. This means that a certain amount of energy that has been stored in the nonlinear output capacitance C_{oss} of MOSFET S_2 is flowing back into the DC-link capacitors during the switching transition with negative inductor current (and similarly for S_1 for a positive inductor current). Nevertheless, a small amount of energy is lost during the switching transitions, i.e. $E_{\text{on}} < E_{\text{off}}$. Hence, the net SSL per switching transition are the difference between the absolute

values of the switching energies $E_{\mathrm{sw}} = |E_{\mathrm{off}}| - |E_{\mathrm{on}}|$ (cf. **Fig. 3.2(d)**), since in each switching transition, one of the two MOSFETs stores E_{off} while the other feeds E_{on} back to the DC-link. Since there are two switching transitions per cycle, each of the MOSFETs dissipates the net energy E_{sw} per cycle, such that the corresponding SSL per switch are obtained via $P_{\mathrm{sw}} = E_{\mathrm{sw}} \cdot f_{\mathrm{sw}}$, where f_{sw} denotes the switching frequency.

However, for the measurement of SSL, this method is subject to large measurement errors due to the fact that the SSL only consist of a small portion of E_{on} and E_{off}; e.g. for this particular type of MOSFET, E_{sw} is in the range of less than 10 % of the returned energy $|E_{\mathrm{on}}|$, i.e. $E_{\mathrm{sw}} \approx 0.1 \cdot |E_{\mathrm{on}}|$. In **Fig. 3.2(e)**, E_{sw} can be recognized as the difference between the switching energies $|E_{\mathrm{off}}|$ and $|E_{\mathrm{on}}|$. Assuming that $|E_{\mathrm{off}}| \approx 1.1 \cdot |E_{\mathrm{on}}|$ and that both, E_{on} and E_{off} are subject to a measurement error of ±5 % (which would be already very accurate, having in mind that E_{on} and E_{off} arise from the integration of a multiplication of a measured voltage and a current transition), the measured worst-case switching loss energy would result in $E_{\mathrm{sw,meas}} = 1.05 \cdot |E_{\mathrm{off}}| - 0.95 \cdot |E_{\mathrm{on}}| \approx 1.05 \cdot (1.1 \cdot |E_{\mathrm{on}}|) - 0.95 \cdot |E_{\mathrm{on}}| = 0.205 \cdot |E_{\mathrm{on}}|$, which compared to the assumed $0.1 \cdot |E_{\mathrm{on}}|$ is a relative error of +105 %, as illustrated in **Fig. 3.2(e)**. In the other case, if E_{off} is measured 5 % too small and $|E_{\mathrm{on}}|$ is measured 5 % too large, the relative error is −105 % (cf. **Fig. 3.2(e)**), i.e. energy would even be generated virtually in each switching cycle which clearly is not the case.

This shows that already small measurement errors in the range of a few percent can lead to tremendously wrong results in case of SSL measurements. In order to have a quantitative statement of the achievable accuracy of electrical switching loss measurements, a detailed error analysis is performed in the following.

3.2.2 Error Analysis for Electrical SSL Measurement Methods

Fig. 3.3 shows an illustration of the drain-source voltage u_{S2} and the drain current i_{S2} during a ZVS turn-off. Due to the fast switching time (roughly 100 ns), and the high voltages, an accurate measurement of the voltages and currents to obtain the correct switching energies is very challenging. Besides the ideal voltage waveform, a second waveform with different sources of measurement errors is shown. Thereby, a skew

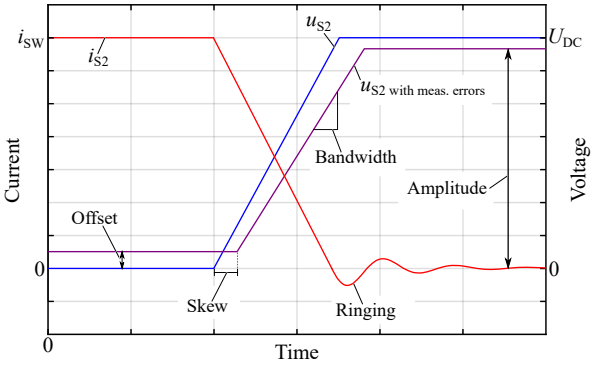

Fig. 3.3: Illustration of the different sources of measurement errors during a ZVS turn-off transition. A perfectly measured voltage waveform as well as a voltage waveform with skew, bandwidth limitation, offset and amplitude error is shown.

between the actual voltage and the measured voltage could occur, which would, as can be seen, have a direct influence on the overlap of voltage and current and thus on the switching energy. Furthermore, a limited bandwidth as well as an amplitude and an offset error of the voltage probe (and also of the current probe) can lead to significant deviations of the measured switching energies. Besides this, ringing of both, the current and/or the voltage would lead to further measurement errors. Therefore, the impact of these error sources on the accuracy of electrical SSL measurements is analyzed.

Skew Error Analysis

Figs. 3.4(a) & **(b)** show measurements of the drain-source voltage u_{S2} and the drain current i_{S2} of MOSFET S_2 in **Fig. 3.2(a)** for 8 kV, 10 A soft turn-off and soft turn-on transitions, respectively. In order to analyze the influence of the probe skew on the measurement accuracy, the originally measured current waveform i_{S2} is delayed for t_{sk}, exemplary selected as 8 ns in the figure for better visualization. Below the waveforms, the power and the cumulated energy in S_2 are shown for both, the original and the skewed measurements. It can be seen that the skewed turn-off energy $E_{off,sk}$ is larger than the original energy whereas the absolute value of the skewed turn-on energy $|E_{on,sk}|$ is smaller than

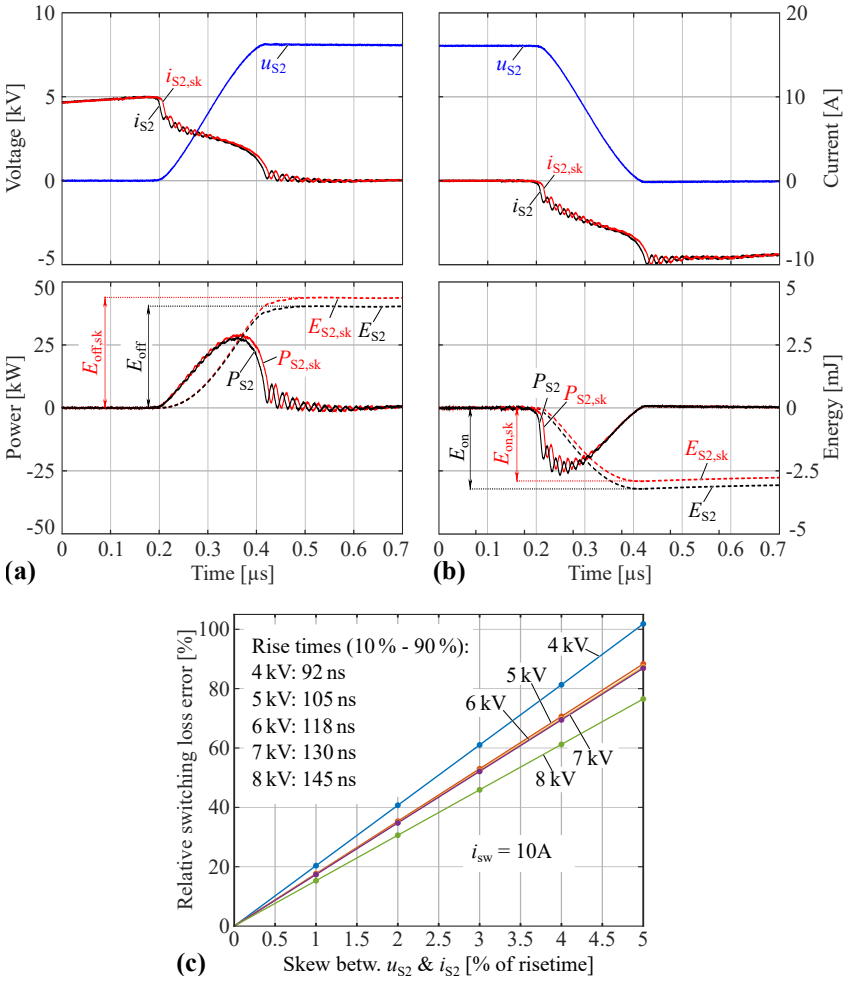

Fig. 3.4: **(a)** & **(b)** Measured turn-off and turn-on waveforms together with the switching power and the switching energies for both, the original and the skewed waveforms. **(c)** Relative switching loss error due to the skew between u_{S2} and i_{S2} for a switched current of 10 A and different DC-link voltages.

the original one. In this case, more energy seems to be dissipated in the turning-off switch whereas less energy seems to be regained from the turning-on switch, leading to an increase of the net SL. If the delay is negative, the overlap of voltage and current decreases compared to its original value, resulting in too low net SL. **Fig. 3.4(c)** shows the relative error of the net SL in dependency of the skew for different DC-link voltages and a switched current of $i_{\mathrm{sw}} = 10\,\mathrm{A}$ (since the effect is almost independent of the switched current). It can be noted that a skew of only 2 % of the switching transition's rise/fall time can lead to a switching loss error of 30...40 %, depending on the voltage. In this particular case, where u_{S2} is in the kilovolt range, the skew of the 20 kV voltage probe (*PHV 4002* from *PMK* in combination with a 12-bit oscilloscope) is the main problem due to the lack of a reference voltage which is necessary for the deskewing of the probe.

Offset & Amplitude Error Analysis

As already mentioned, further sources for measurement errors are possible DC offsets and amplitude errors in the voltage and current measurements during the switching transitions. Especially the 20 kV voltage probe is again causing problems since it is not possible to accurately compensate the probe to a proper low-frequency gain, high-frequency gain (responsible for overshoots) and zero voltage offset at the same time. Furthermore, during the measurements it has been observed that the attenuation of the 20 kV voltage probe, i.e. the passive voltage divider, is strongly temperature dependent, thus a thermal decoupling between the probe and any heating parts must be ensured. Consequently, a compromise between these factors is necessary which means that to a certain extent these effects are always present.

A similar error analysis to the one in **Fig. 3.4** can be performed concerning DC offsets and amplitude errors, assuming a certain DC offset difference or amplitude difference in the voltage measurement between the E_{off} and E_{on} transitions. Accordingly, if the voltage u_{S2} is offset free during the turn-on transition but shows a slight positive offset during the turn-off transition (which could arise from a non-ideal compensation of the voltage probe), the integration will lead to an increased turn-off energy E_{off}, whereas the turn-on energy E_{on} is assumed to be measured correctly for this analysis. Since the net switching loss energy is again only in the range of less than 10 % of E_{on}, the error in the measurement of E_{on} and E_{off} is strongly amplified, which leads to large errors in E_{sw}

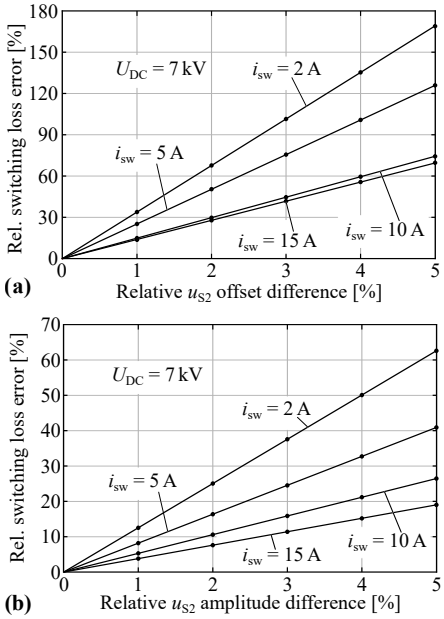

Fig. 3.5: (a) Relative switching loss error due to an offset difference in the u_{S2} drain-source voltage measurements for the determination of E_{off} and E_{on}. **(b)** Relative switching loss error due to a voltage amplitude difference in the u_{S2} drain-source voltage measurements.

as shown in **Fig. 3.5(a)**. Depending on the switched current, an offset difference of only 2 % of the DC-link voltage can lead to a switching loss error of more than 65 %. Similarly, in **Fig. 3.5(b)**, the resulting relative switching loss error caused by an amplitude difference between the voltage measurements during the turn-off and turn-on transitions is given. As an example, if for the measurement of the SSL for 7 kV, 2 A, the amplitude of the rising voltage edge is measured 2 % too large whereas the falling edge is assumed to be measured correctly, this leads to a switching loss error of 25 %.

Bandwidth Error Analysis

Another source of measurement error can be found in the limited bandwidth of active and passive probes since harmonics which are contained

in the original signal and are located above the probe's cut-off frequency are filtered out and thus could lead to wrongly measured waveforms with e.g. decreased voltage and current slopes. Assuming that the transfer functions of the probes show first order low-pass characteristics, the original signal can be reconstructed by transforming the measured signal into the frequency domain, multiplying it with the inverse of the probe's low-pass transfer function and transforming the result back into the time domain. For a voltage probe bandwidth of 100 MHz (according to the datasheet), it turns out that the measured and reconstructed waveforms (voltage rise times in the range of 100 ns) are virtually identical apart from a slight skew which has to be compensated experimentally in order not to cause large switching loss measurement errors, as explained above. Aside from the skew, the bandwidths of the utilized voltage probe and current transformer (with a bandwidth > 100 MHz) are sufficient for this application. However, if the measurement bandwidth is reduced, for the measurements at hand the signal quality starts to suffer as soon as the bandwidth falls below 70 MHz, which in this case is considered as the lower bandwidth limit.

Integration Limit Analysis

Besides the described measurement errors, further errors can be introduced in the post-processing of the measured data. For example the proper selection of the time interval in which the SL are integrated is aggravated by possible ringing, which in consequence results in wrong turn-on and turn-off switching energies. This is also shown in **Figs. 3.4(a) & (b)**, where the current i_{S2} exhibits certain oscillations at the end of each switching transient. In case of the turn-on transition, these current oscillations are, in order to obtain the power P_{S2}, multiplied with u_{S2} which has already decayed to zero at that time. Hence, these oscillations vanish in the power calculation, resulting in a smooth waveform and it is clear where to set the integration limits. However, for the turn-off transition, the current oscillations are multiplied with the full DC-link voltage, leading also to large oscillations in the calculated power waveform and thus making the proper selection of the integration limits more difficult. As an example, **Fig. 3.6** shows a 7 kV, 15 A turn-off transition together with the calculated power and the resulting switching energy, where t_0 denotes the beginning of the integration interval. As can be noted, due to the appearing oscillations in the power waveform, the determination of the integration interval's end

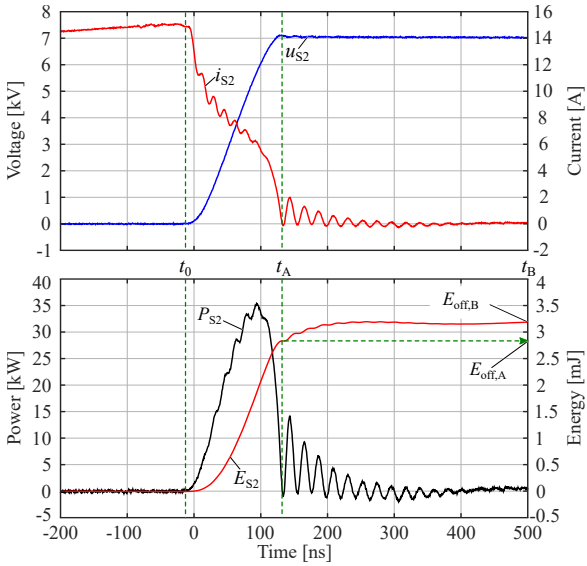

Fig. 3.6: Exemplary measured 7 kV, 15 A turn-off transition together with the power P_{S2} and the energy E_{S2} for the illustration of the influence of the integration limits on the measured SSL. Due to the oscillations, the choice of the end of the integration interval is not clear. t_0 denotes the start of the integration, whereas t_A and t_B are two options to select the end of the integration interval.

is not clear anymore. There are basically two reasonable possibilities to select the integration limit as denoted with t_A and t_B. t_A corresponds to the first zero crossing of the current and t_B is selected such that both, the HF and the LF oscillations have decayed. Accordingly, the obtained turn-off energies are $E_{off,A} = 2.83\,mJ$ and $E_{off,B} = 3.19\,mJ$, whereas the corresponding turn-on energy is $E_{on} = -2.45\,mJ$. The associated SSL are thus $E_{sw,A} = 380\,\mu J$ and $E_{sw,B} = 740\,\mu J$ which results in a relative SSL error of 48.6 % or 94.7 %, depending on which value is considered as the reference. Hence, the post-processing with the selection of the integration limits is very crucial and can lead to similar errors as obtained during the measurement procedure.

Since the impact of the skew, the offset/amplitude difference, the probe bandwidths, and the selection of the integration limits on the measurement error is large and might all in all lead to switching loss

errors higher than 200 % (although the assumed skew, offset and amplitude difference values are very small and fairly realistic), it is concluded that the double-pulse measurement method is unsuitable for the measurement of the SSL in case of the 10 kV SiC devices at hand. Therefore, other measurement methods with improved accuracy have been developed in the recent years as will be shortly described in the following.

Further (Semi-)Electrical SSL Measurement Methods

In [178], for example, SL are measured electrically based on the energy conservation principle during one switching cycle. It is claimed that, in a buck-type circuit, the SL equal the difference between the energy supplied by the DC-link capacitor and the energy stored in the load inductor, i.e. input power minus output power of the bridge-leg. Thus, in contrast to the double-pulse method where a transient MOSFET current is multiplied with a transient MOSFET voltage, with the method proposed in [178], the input power is found by multiplying the MOSFET current with the constant DC-link voltage and the output power is calculated by multiplying the drain-source voltage of the MOSFET with the constant output current. Consequently, the skew between the measured MOSFET voltage and current transients is no longer a problem. Nevertheless, the remaining measurement errors as well as the integration problem still exist. Furthermore, the output current is only constant if HSL are measured; for the measurement of SSL, a triangular current waveform as shown in **Fig. 3.2 (d)** is needed.

In [179] and [180], SL have been measured based on the opposition method, where in contrast to the described pulsed measurements, a full-bridge is operated continuously with an inductive load. Similar to [178], the semiconductor losses are obtained by electrically measuring the DC input power and subtracting the calculated ohmic losses of the inductor based on the inductor's AC-resistance and the measured inductor current. Thus, the AC-resistance of the inductor has to be well-characterized in terms of its frequency and temperature dependency in order to achieve a sufficiently accurate measurement of the semiconductor losses. Beneficially, the inductor is realized as an air core inductor (without magnetic material) in order to not include additional errors due to core losses into the measurement. Furthermore, the pure SL are obtained by subtracting the CL (calculated based on the on-state resistance $R_{\mathrm{DS,on}}$) from the measured total semiconductor losses. However, as already mentioned, since the $R_{\mathrm{DS,on}}$ shows a certain

dependency on the temperature, the current and the current direction - especially for the examined 10 kV SiC MOSFETs - significant measurement errors can be introduced. Thus, this method is not suitable for the underlying application.

For the sake of completeness it should be mentioned that, as a combination of electrical and calorimetric switching loss measurement methods, the inductor losses in the opposition method can also be measured calorimetrically [176]. On the one hand, this leads to more accurate results and on the other hand, a magnetic core material can be used. Nevertheless, the switching and conduction losses still have to be separated.

3.2.3 Calorimetric SL Measurement Methods

Instead of measuring the input and output power of a circuit, a more direct way of measuring SL is to exclusively measure the power dissipation of the switches in a calorimetric manner.

In [181], a half-bridge as part of a synchronous buck converter is operated continuously, whereby the two switches, their gate drivers and the DC-link capacitor are enclosed in a calorimeter in order to measure the power dissipation. In this method, the power dissipation of the gate drives (which are additionally measured electrically) have to be subtracted from the total power in the calorimeter in order to obtain the semiconductor losses. In [182], a similar calorimetric method is presented. Thereby, a metal block is attached to the switches of a half-bridge circuit which is continuously operated. The metal block acts as a thermal capacitance C_{Th} which is heated up by the dissipated power of the switches resulting in a certain temperature increase $\Delta\vartheta$. Based on the given thermal capacitance C_{Th} in combination with the time required to heat up the metal block, the dissipated power can be calculated. The advantage of this method is that the gate driver losses etc. do not influence the measurement due to the thermal decoupling. Still, the challenge for these methods is the separation of the conduction and switching losses.

In order to separate these losses directly in the measurement instead of calculating the CL (with error-prone $R_{\mathrm{DS,on}}$ values) and subtracting them from the total semiconductor losses, a novel calorimetric SSL measurement method featuring a high accuracy is proposed in the following section.

3.3 Functional Principle of the Proposed SSL Measurement Method

The basic idea of the proposed method for the measurement of SSL is on the one hand to measure the semiconductor losses calorimetrically and on the other hand to measure the SL and the CL separately. Therefore, as shown in **Fig. 3.7(a)**, a third MOSFET S_0 is inserted in series to either the low-side switch S_2 or the high-side switch S_1 of the half-bridge. In the following it is assumed that S_0 is connected in series to the high-side switch S_1 since the cooling pad of the DUT is connected to the drain potential of the MOSFET and thus in this configuration is fixed to a stable voltage. Furthermore, the MOSFET module S_0 is mounted on top of a brass block, which absorbs the dissipated semiconductor losses and acts as a thermal capacitance C_{Th} (cf. **Fig. 3.7(a)**). Brass is selected as heat sink material due to its high thermal capacitance per volume. In addition, the brass block is insulated with thermal insulation material in order to minimize the heat transfer to the ambient. Consequently, assuming a constant power dissipation in the semiconductor device S_0, the temperature of the brass block linearly increases over time, whereby the temperature slope is proportional to the dissipated power of S_0. Hence, the power dissipation of S_0 can be calculated as

$$P = \frac{C_{\mathrm{Th}} \cdot \Delta\vartheta}{\Delta\tau}, \tag{3.1}$$

where $\Delta\vartheta$ denotes the temperature difference and $\Delta\tau$ equals the measurement time. Based on (3.1), the dissipated power of S_0 can now be determined by operating the half-bridge continuously, and by measuring the time $\Delta\tau$ which is required to heat the insulated brass block by a certain temperature difference $\Delta\vartheta$, e.g. from 30 °C to 40 °C.

For the basic operation of the modified half-bridge illustrated in **Fig. 3.7(a)**, the series connection of S_0 and S_1 can be considered as one switch, where either S_0 or S_1 is permanently turned on, while the other is complementarily switched with S_2, i.e. the circuit behaves like a conventional half-bridge. Hence, in order to achieve soft-switching transitions in all switches, the half-bridge is continuously operated with a 50 % duty cycle resulting in a triangular current as shown in **Fig. 3.7(c)**. As can be noticed, the shown section corresponds to a point in time in which S_1 is permanently turned on, while S_0 and S_2 are complementarily switching. Consequently, due to the series connection of S_0 and

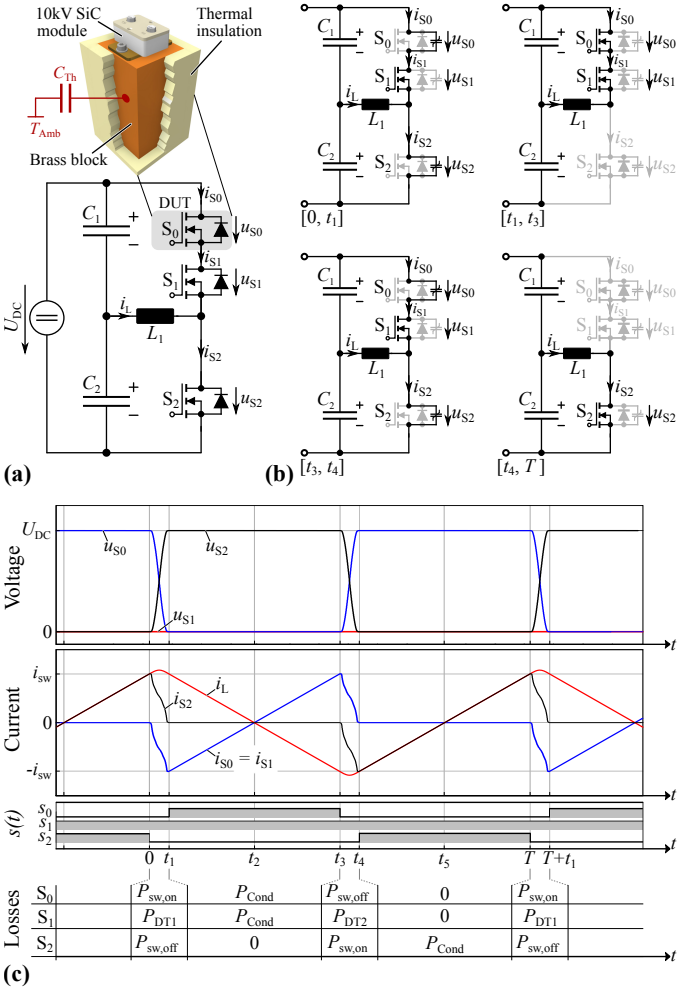

Fig. 3.7: **(a)** Circuit diagram with an additional MOSFET S_0 mounted on a thermally insulated brass block which acts as a thermal capacitance C_{Th}. **(b)** Circuit diagrams showing the current path during the specific time intervals; devices shown with shaded symbols do not conduct current. **(c)** Ideal current and voltage waveforms as well as the gate signals of the three switches and the corresponding share of losses in each time interval.

S_1, the same current is flowing through both switches, which means that the CL in both switches are the same if equal on-state resistances $R_{DS,on}$ are assumed. Furthermore, since only S_0 and S_2 are switching, the SSL are only generated in S_0 and S_2, while S_1 only generates CL. Accordingly, if one would separately measure the losses in both MOSFETs S_0 and S_1 based on (3.1), the SSL generated in S_0 could be directly extracted from the loss difference of the two semiconductor devices.

However, since the on-state resistance $R_{DS,on}$ is strongly varying from device to device in this case, as already mentioned, the SL and the CL cannot be properly separated from each other. Therefore, instead of measuring the losses of two different devices S_0 and S_1 at the same time, in addition to the measurement M_1 discussed above, a second measurement M_2 is performed at the same operating conditions, i.e. the same switched current, DC-link voltage, bridge-leg dead time, switching frequency and temperature range. In measurement M_2, however, the MOSFETs S_0 and S_1 swap their roles such that S_0 is now permanently on and S_1 is complementarily switched with S_2. In this case, S_0 only generates CL ($P_{M2} = P_{Cond}$), while during measurement M_1 the MOSFET S_0 was generating both, SL and CL, i.e. ($P_{M1} = P_{Cond} + P_{sw}$). Hence, the SSL of S_0 within one switching period can be found by subtracting P_{M2} from P_{M1} and dividing the difference by the switching frequency.

Unfortunately, even though in both measurements M_1 and M_2 the CL are measured in the same device for the same operating conditions, the CL are not exactly identical due to the dead time intervals $[0, t_1]$ and $[t_3, t_4]$, where the output capacitances of the switches have to be charged/discharged. In order to emphasize the importance of the dead time intervals in the calculation of the CL, in **Fig. 3.7(c)** the switched current is chosen rather small, which means that the dead time intervals can occupy a significant part of a switching period. It should be noted that the length of the dead time intervals $[0, t_1]$ and $[t_3, t_4]$ is selected in such a way that the corresponding switch is turned on exactly at the moment when its drain-source voltage reaches 0 V, i.e. ideally the antiparallel JBS diodes are not conducting. Actually, since S_1 is connected in series to S_0, in the first measurement M_1 the MOSFET S_1 should only generate CL during the on-state interval of S_0. However, as shown in **Fig. 3.7(b)**, during the dead time intervals $[0, t_1]$ and $[t_3, t_4]$, the current, which flows through the nonlinear output capacitance of

S_0, also flows through the MOSFET channel of S_1, generating additional CL P_{DT1} and P_{DT2} in S_1 ($P_{DT} = P_{DT1} + P_{DT2}$). Consequently, during the second measurement M_2 (S_0 permanently on, S_1 switching), the same additional CL P_{DT} arise in S_0 and thus have to be considered for the calculation of the SSL. To express P_{DT} as a function of P_{Cond}, it is assumed that the CL during the dead time interval $[0, t_1]$ and the conduction interval $[t_1, t_2]$ arise from an ohmic behavior of the MOSFET and can be described by $P = R_{DS,on} \cdot i^2$ if the dependency of the $R_{DS,on}$ on the value and direction of the drain current is neglected for the moment (the resulting error is negligible as will be shown in the error analysis). Consequently, the dead time CL P_{DT} can be calculated as

$$P_{DT} = h_P \cdot P_{Cond}, \text{ where} \tag{3.2}$$

$$h_P = \frac{R_{DS,on} \cdot \int_0^{t_1} i_{S0}^2 \cdot dt}{R_{DS,on} \cdot \int_{t_1}^{t_2} i_{S0}^2 \cdot dt} \approx \frac{\int_0^{t_1} i_{S0}^2 \cdot dt}{\int_{t_1}^{t_2} i_{S0}^2 \cdot dt}. \tag{3.3}$$

Thereby, h_P can be obtained by measuring the drain current of S_0 and by solving the given integrals for the corresponding time intervals.

As will be discussed in **Section 3.4.1**, in order to achieve a high measurement accuracy, the SSL should account for the largest share of the overall power dissipation measured at the brass block, since in this case, the sensitivity of the SSL on calculation errors of h_P as well as on variations in the CL between the two measurements, e.g due to the temperature dependent $R_{DS,on}$ of S_0, is very low. Accordingly, for the dimensioning of the brass block it is assumed that in the worst-case, i.e. for a max. switched current of 15 A, the CL should not exceed 50 % of the SSL, which in contrast to the CL can be adapted via the switching frequency and the inductance value. The $R_{DS,on}$ of the 10 kV SiC MOSFETs at hand is around 0.35 Ω at room temperature, which in the worst-case results in 13 W of CL, and according to this rule in a total power dissipation of 39 W. Furthermore, in order to achieve a minimum relative accuracy of ±1 % for the temperature measurement, the measurement range must be at least $\Delta\vartheta = 10$ K, if an absolute temperature measurement error of ±0.1 K is expected. For the same reason of measurement accuracy, the minimum measurement time $\Delta\tau$ should be at least 2...3 minutes. Hence, the required thermal capacitance and therewith the size of the brass block ($50 \times 50 \times 100$ mm) can

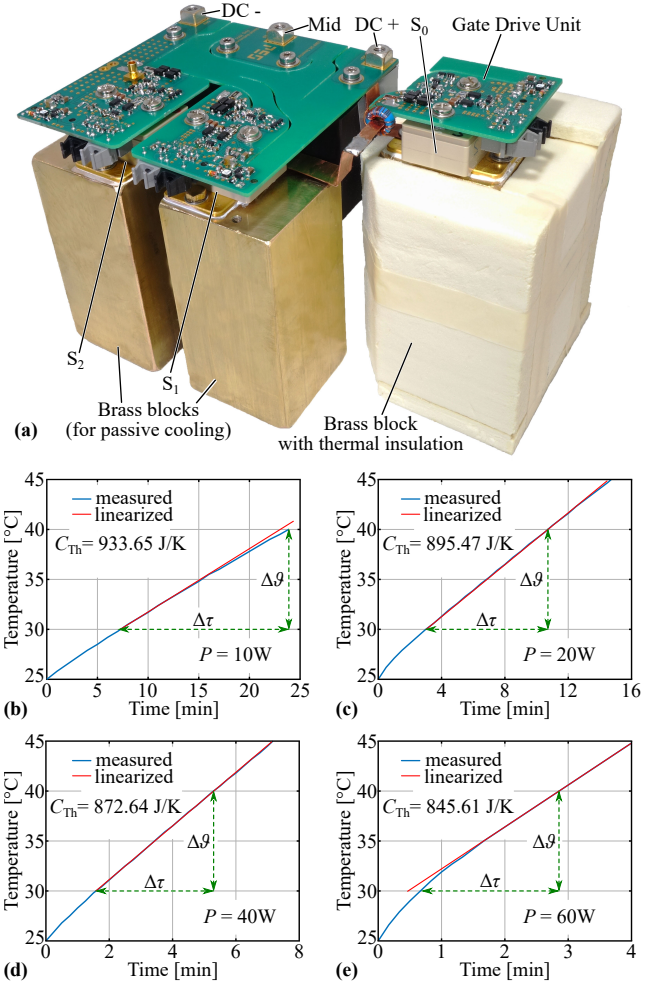

Fig. 3.8: **(a)** 10 kV SiC MOSFET half-bridge with the additional MOSFET S_0 on a thermally insulated brass block ($50 \times 50 \times 100$ mm). **(b)-(e)** Thermal calibration measurements at constant DC power levels, **(b)** 10 W, **(c)** 20 W, **(d)** 40 W, and **(e)** 60 W. Each temperature profile is linearized around the measurement temperature range and the corresponding thermal capacitance is calculated from the given slope. A high linearity can be achieved in the temperature range from 30 °C to 40 °C and the power range from 20 W to 40 W. Thus, all the switching loss measurements are carried out in this power and temperature range.

be calculated based on (3.1). A picture of the corresponding 10 kV SiC hardware setup with the thermally insulated brass block is shown in **Fig. 3.8(a)**. It should be noted that the MOSFETs S_1 and S_2 are also mounted on separate brass blocks instead of heat sinks in order to not distort the measured temperature of the insulated brass block by any air stream.

In order to obtain the precise thermal capacitance of the brass block in the hardware setup, the value C_{Th} has to be calibrated by measurements. Therefore, a constant DC-power is fed into the MOSFET module by driving a feedback-controlled current through the device such that constant power levels of 10 W, 20 W, 40 W and 60 W are reached. Thereby, the hardware configuration (including the copper busbars to the DC-link, the gate driver, and the thermal insulation etc.) must be exactly the same as it is later used for the SSL measurements. **Figs. 3.8(b)-(e)** show the measured temperature profiles of the insulated brass block for the different power ratings. It can be seen that between 30 °C and 40 °C the measurements for 20 W and 40 W are nicely linear, whereas for 10 W and 60 W certain nonlinearities are measured in the temperature curves. Consequently, all SSL measurements are performed in the power range from 20 W to 40 W and in the temperature range from 30 °C to 40 °C. Furthermore, as indicated in **Figs. 3.8(b)-(e)**, the linearized thermal capacitance C_{Th} (a first order thermal equivalent network is assumed) is slightly changing within the selected power range. Therefore, C_{Th} is interpolated iteratively from the calibration measurements for the purpose of obtaining the correct power dissipation.

Due to this limitation in the power range, now the problem of measuring only CL in measurement M_2 arises, since for small switched currents the CL are in the range of only 1...2 W. In order to overcome this problem, the operation principle of the half-bridge has to be modified in such a way that also in the measurement M_2 higher losses are generated in S_0. Therefore, instead of permanently turning on S_0, S_0 and S_1 share the switching actions and therewith the SL among each other as indicated in **Fig. 3.9(a)**. The share of the switching cycles, which is switched by S_0, is defined as the switching cycle share k. A value of $k = 1$ means that S_0 is switching continuously, while S_1 is permanently turned on. As an example, in **Fig. 3.9 (a)**, k is equal to 0.5 which means that S_0 and S_1 are alternatingly switching 50 % of the total switching cycles and are constantly turned on for the other 50 %.

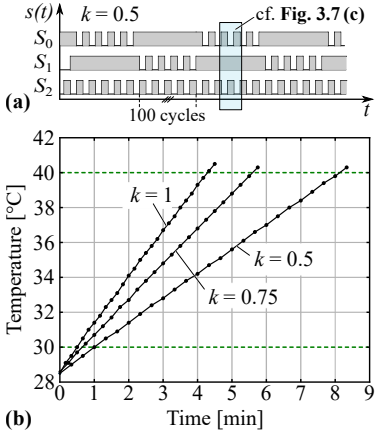

Fig. 3.9: **(a)** Gate signals of the three MOSFETs for the modified modulation scheme exemplarily shown for a switching cycle share of $k = 0.5$. **(b)** Measured temperature curves for $U_{\mathrm{DC}} = 8\,\mathrm{kV}$, $i_{\mathrm{sw}} = 7.5\,\mathrm{A}$ and different values of k.

For practical reasons, $\mathrm{S_0}$ and $\mathrm{S_1}$ are alternated for every 100 switching cycles. In **Fig. 3.9 (b)**, measured temperature profiles at $U_{\mathrm{DC}} = 8\,\mathrm{kV}$ and a switched current of 7.5 A are shown for different values of k. As can be noticed, the measurements follow a linear characteristic, which means that the thermal setup is operated in its linear region as desired.

Accordingly, depending on the selected switching cycle share k, the average losses P_{S0} of $\mathrm{S_0}$ within one measurement can be brought into the optimum power range of 20 W to 40 W and can be expressed in general terms as

$$\begin{aligned} P_{\mathrm{S0}} &= k\,(P_{\mathrm{sw}} + P_{\mathrm{Cond}}) + (1-k)\,(P_{\mathrm{DT}} + P_{\mathrm{Cond}}) \\ &= k \cdot P_{\mathrm{sw}} + P_{\mathrm{Cond}} + (1-k)\,P_{\mathrm{DT}}, \end{aligned} \tag{3.4}$$

where $P_{\mathrm{sw}} = P_{\mathrm{sw,on}} + P_{\mathrm{sw,off}}$ and $P_{\mathrm{DT}} = P_{\mathrm{DT1}} + P_{\mathrm{DT2}}$. Hence, in the first measurement M_1 with $k = 1$, the power dissipated in $\mathrm{S_0}$ is

$$P_{\mathrm{M1}} = P_{\mathrm{S0}}\,(k=1) = P_{\mathrm{sw}} + P_{\mathrm{Cond}}. \tag{3.5}$$

In the second measurement M_2 with $k < 1$, the dissipated power in $\mathrm{S_0}$

is given as

$$P_{\mathrm{M2}} = k \cdot P_{\mathrm{M1}} + (1-k)\,(P_{\mathrm{Cond}} + P_{\mathrm{DT}})\,, \tag{3.6}$$

where $P_{\mathrm{sw}} = P_{\mathrm{M1}} - P_{\mathrm{Cond}}$ from (3.5) is used. Furthermore, based on (3.2), the dead time losses P_{DT} in (3.6) can be substituted by $h_{\mathrm{P}} \cdot P_{\mathrm{Cond}}$, thus the effective CL and SL are given as

$$P_{\mathrm{Cond}} = \frac{P_{\mathrm{M2}} - k \cdot P_{\mathrm{M1}}}{1 - k + (1-k) \cdot h_{\mathrm{P}}}, \tag{3.7}$$

$$P_{\mathrm{sw}} = P_{\mathrm{M1}} - P_{\mathrm{Cond}}, \tag{3.8}$$

and only depend on the two measured losses P_{M1} and P_{M2} as well as on the selected switching cycle share k. For the SSL measurements of the 10 kV SiC MOSFETs, a switching cycle share of $k = 1$ has been chosen for measurement M_1, $k = 0.5$ for measurement M_2 and $k = 0.75$ for a third (verification) measurement, leading to stable and reproducible results. Finally, the SSL per MOSFET and switching period can be determined as $E_{\mathrm{sw}} = P_{\mathrm{sw}}/f_{\mathrm{sw}}$.

3.4 Discussion and Experimental Results

The following section analyzes the accuracy of the proposed SSL measurement method and discusses possible limitations and sources of measurement errors. Finally, the measured SSL are presented and discussed.

3.4.1 Error Analysis for the Proposed SSL Measurement Method

Although calorimetric measurements are probably the most direct and accurate way of measuring power dissipations, there are several effects that have to be considered in order to obtain accurate results. First of all, an accurate and EMI-robust measurement of the brass block temperature is required. Depending on the device package, the cooling terminal might be on drain potential of the MOSFET (which is the case for the 10 kV SiC MOSFETs at hand) such that the metal block including the temperature sensor is on (floating) potential and is possibly exposed to high $\mathrm{d}u/\mathrm{d}t$ values which could disturb the temperature measurement. Furthermore, the position of the temperature sensor on

the metal block must be the same during the calibration and the switching loss measurements. Otherwise, measurement errors could arise due to a possibly inhomogeneous temperature distribution within the metal block. In the given setup, a thermocouple was attached to the top side of the brass block, next to the baseplate of the 10 kV SiC module. A better approach would be to use a fiber optic temperature sensor, which besides EMI-robustness would also provide a galvanic isolation. Generally important for this measurement method is the thermal decoupling of the DUT and its brass block from the ambient (by applying thermal insulation material to the brass block) and especially from other heat sources contained in the hardware setup (such as the other switches) in order to prevent undesired heat transfers to the brass block. This is easily possible for the 10 kV SiC MOSFETs at hand due to the specific package design and the anyway required distances between the switch and other parts of the circuit for the reason of electrical isolation. The measured thermal time constant of the thermally insulated brass block together with the 10 kV SiC module is $\tau_{\mathrm{Block}} = 200\,\mathrm{min}$, which is a factor of 15 larger than the maximum measurement time. This shows that the undesired heat transfers to the ambient and other parts of the setup can be neglected in the given setup. For other device packages and especially lower voltage devices, however, the thermal decoupling of the DUT might be a problem, since a thermal decoupling goes hand in hand with an increase of the commutation loop inductance which could lead to voltage overshoots and ringing. For the employed 10 kV devices operated with DC-link voltages in the kilovolt range, the voltage overshoot caused by the additional inductance of the third switch is negligible and not even measurable.

Since the measurement method includes a measurement of a rather small temperature difference $\Delta\vartheta$ of 10 K, the accuracy of the temperature measurement is the most critical parameter. Assuming a measurement error of $\Delta\vartheta = \pm 0.1\,\mathrm{K}$ (which corresponds to a relative error of $\pm 1\,\%$), a $\pm 2\,\%$ error in the thermal capacitance C_{Th} and a perfect time measurement (since time can be measured very precisely), the worst-case error of a single power measurement is $\pm 3\,\%$ (cf. (3.1), $102\,\% \cdot 101\,\% \approx 103\,\%$). Hence, as a worst-case estimation, if P_{M1} is measured 3 % too high and P_{M2} is measured 3 % too low, the relative errors in the SL are 5.8 % for the 7 kV, 2.5 A case and 15.5 % for the 7 kV, 15 A case, whereby measured values for P_{M1}, P_{M2} and h_{P} (cf. **Tab. 3.1**) are inserted into (3.7) and (3.8) for the error analysis in order

Tab. 3.1: Measured and calculated values for the case of low switched current (7 kV, 2.5 A) and high switched current (7 kV, 15 A).

Parameter	*Value for* 7 kV, 2.5 A	*Value for* 7 kV, 15 A
P_{M1}	37.50 W	38.54 W
P_{M2}	18.84 W	26.99 W
h_{P}	1.1883	0.0731
P_{Cond}	0.09 W	14.38 W
P_{sw}	37.41 W	24.16 W
P_{DT}	0.10 W	1.05 W
f_{sw}	200 kHz	100 kHz

to give practical examples. Compared to the double-pulse method, a 10 to 20 times higher accuracy can be achieved with the proposed calorimetric method. Furthermore, in all of the performed measurements, the $k = 0.5$ and the $k = 0.75$ (reference) measurements match within 5 % error, which demonstrates that the worst-case is not very likely to occur if the measurements are carried out carefully and indicates that the accuracy of the method is very high. As can be noticed, the measurement error increases with increasing switched currents, thus the SL should hold the largest share of the overall measured power dissipation in order to keep the measurement accuracy high. This can be managed by selecting a rather high switching frequency, which however is limited by certain constraints such as the gate drive power capability, the total generated losses on the metal block (which might be too high and result in a nonlinear temperature profile at some point) or the fact that with higher switching frequencies the dead time interval consumes a major part of the overall switching cycle. Another (limited) possibility to increase the measurement accuracy is to increase the temperature difference $\Delta\vartheta$. However, the temperature dependency of the MOSFET's properties might start playing a role for higher values of $\Delta\vartheta$. For example, in the derivation of the SL from the two measurements M_1 and M_2, in equation (3.3) it is assumed that the on-state resistance $R_{\mathrm{DS,on}}$ is constant, however, this is not perfectly true, since the $R_{\mathrm{DS,on}}$ of the 10 kV SiC MOSFETs at hand depends on the temperature as well as on

the direction and the value of the drain current. Hence, the $R_{\mathrm{DS,on}}$ does not completely cancel out in equation (3.3) and leads to a certain calculation error of h_{P}. However, the sensitivity of the SSL on calculation errors of h_{P} is very low. On the one hand, for low switched currents, the switching frequency is selected rather high (cf. **Tab. 3.1**) in order to increase the SL until an optimal power dissipation between 20 W and 40 W on the brass block is achieved. In this case, the dead time indeed consumes a major part of the switching cycle ($h_{\mathrm{P}} \approx 1$), thus the corresponding losses P_{DT} are similar to the CL P_{Cond} (cf. **Tab. 3.1**). Due to the low current rating, however, the SL P_{sw} are orders of magnitude higher than P_{DT} or P_{Cond}. Consequently, calculation errors of h_{P} hardly influence the SL. E.g. with the values given for the 7 kV, 2.5 A measurement in **Tab. 3.1**, the switching loss error stays below 0.012 %, if for the determination of h_{P} a calculation error of $\pm 10\,\%$ is assumed. On the other hand, for high switched currents, the time to charge/discharge the output capacitances of the MOSFETs is short, i.e. $h_{\mathrm{P}} \approx 0$. Hence, errors in the calculation of h_{P} have a negligible impact on the SL. Assuming again an error of $\pm 10\,\%$ in h_{P}, for the case of 7 kV, 15 A (cf. **Tab. 3.1**), the switching loss error is below 0.41 %.

Furthermore, a measurement error could potentially result due to the fact that the chip temperature and therewith the $R_{\mathrm{DS,on}}$ is not equal for the two measurements M_1 and M_2 since the generated losses P_{M1} and P_{M2} are different, which results in distinct junction temperatures. Therefore, the impact of this junction temperature difference on the measuring accuracy is analyzed in the following. As stated above, the influence of the dead time can be neglected ($P_{\mathrm{DT}} \approx 0$), thus with the simplified equations (3.5) and (3.6) and the assumption of equal average CL P_{Cond} within the two measurements, the SL P_{sw} can be immediately expressed by the difference of the two measured losses P_{M1} and P_{M2} as

$$\Delta P_{\mathrm{M12,ideal}} = P_{\mathrm{M1}} - P_{\mathrm{M2}} = P_{\mathrm{sw}}\,(1-k)\,. \tag{3.9}$$

Due to this difference in losses, however, the thermal resistance between the chip and the brass block R_{JB} leads to a higher junction temperature for measurement M_1 compared to M_2, even though both measurements are performed for the same brass block temperature range from 30 °C to 40 °C. Assuming a thermal resistance of $R_{\mathrm{JB}} = 0.5\,\mathrm{K/W}$ (extracted from thermal FEM simulations) and exemplarily measured losses of $P_{\mathrm{M1}} = 30\,\mathrm{W}$ and $P_{\mathrm{M2}} = 20\,\mathrm{W}$, the chip temperature for M_1 would (ideally) pass through the temperature range

from $30\,°\mathrm{C} + R_{\mathrm{JB}} \cdot P_{\mathrm{M1}}...40\,°\mathrm{C} + R_{\mathrm{JB}} \cdot P_{\mathrm{M1}} = 45\,°\mathrm{C}...55\,°\mathrm{C}$, whereby the chip temperature for M_2 passes through the temperature range of $40\,°\mathrm{C}...50\,°\mathrm{C}$, i.e. an average chip temperature difference of 5 K occurs. Consequently, since the on-state resistance $R_{\mathrm{DS,on}}$ of the employed 10 kV SiC MOSFETs features a temperature dependency of $\Delta R_{\mathrm{DS,on}} = 1\,\%/\mathrm{K}$, in this example the actual average CL for M_1 are 5 % higher than for M_2. Hence, considering a linear increase of the $R_{\mathrm{DS,on}}$ with temperature, (3.5) and (3.6) have to be adapted to

$$P_{\mathrm{M1}} = P_{\mathrm{sw}} + (1+\beta)\,\alpha P_{\mathrm{sw}}, \tag{3.10}$$

$$P_{\mathrm{M2}} = k \cdot P_{\mathrm{sw}} + \alpha P_{\mathrm{sw}}, \tag{3.11}$$

with

$$\alpha = \frac{P_{\mathrm{Cond}}}{P_{\mathrm{sw}}} \quad \text{and} \tag{3.12}$$

$$\beta = R_{\mathrm{JB}} \cdot \Delta P_{\mathrm{M12,ideal}} \cdot \Delta R_{\mathrm{DS,on}}, \tag{3.13}$$

where α is the ratio between the CL and the SL (which should always be kept as small as possible by properly selecting the switching frequency) and β is the relative increase of the MOSFET's $R_{\mathrm{DS,on}}$ depending on the loss difference between the two measurements M_1 and M_2. Subtracting (3.10) from (3.11) leads to

$$\begin{aligned} \Delta P_{\mathrm{M12,real}} &= (1 - k + \alpha\beta)\, P_{\mathrm{sw}} \\ &= \Delta P_{\mathrm{M12,ideal}} \left(1 + \frac{\alpha\beta}{1-k}\right). \end{aligned} \tag{3.14}$$

Now, the relative error $e_{\Delta\mathrm{T}}$ introduced by the junction temperature difference between P_{M1} and P_{M2} can be found as

$$e_{\Delta\mathrm{T}} = \frac{\alpha\beta}{1-k}. \tag{3.15}$$

It should be noted that this analysis is also valid for devices with a nonlinear dependency of the $R_{\mathrm{DS,on}}$ on the junction temperature, since in this case, the $R_{\mathrm{DS,on}}$ can be linearized within the relevant temperature range of 10 K from e.g. 45 °C to 55 °C with a high accuracy. For the values given in **Tab. 3.1**, equation (3.15) leads to a relative error $e_{\Delta\mathrm{T}}$ in the range of 0.05 % and 6.87 %, which means that the worst-case error for the measurements following in **Section 3.4.2** is smaller than

7 %. As can be noticed, the error increases with increasing current, since the ratio α between the CL and the SL increases. In order to keep the error small, the objective should be to achieve $\alpha \leq 1$ (which means $P_{M1} - P_{M2} \leq 20\,\text{W}$ for the setup at hand). Nevertheless, if the exact values of R_{JB} and $\Delta R_{DS,on}$ of the MOSFET are known, this error can be corrected in the loss calculation. Finally, it should be noted that the SSL do not or hardly depend on the junction temperature, as will be shown later.

3.4.2 Measurement Results

In order to cover a wide range of applications in which the analyzed 10 kV SiC MOSFETs could be utilized, SSL measurements have been performed for different DC-link voltages, currents and gate resistors. **Fig. 3.10** shows the net measured SSL of the 10 kV SiC MOSFETs for DC-link voltages between 4 kV and 8 kV and switched currents between 2.5 A and 15 A. Unless otherwise noted, the gate resistors are $R_{on} = 20\,\Omega$ and $R_{off} = 10\,\Omega$. It is clearly visible that the SSL depend mainly on the DC-link voltage and increase only slightly with increasing current. This behavior will be discussed in more detail in **Section 3.5**.

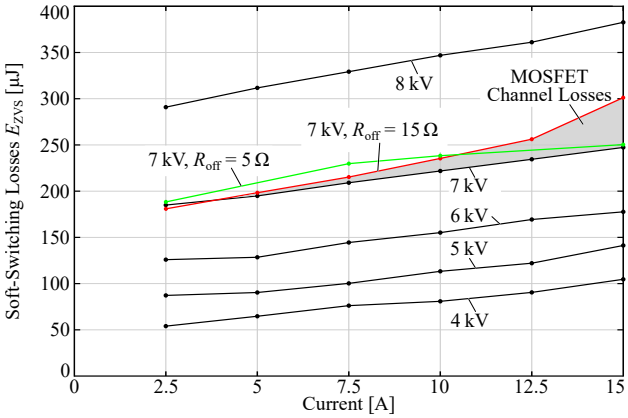

Fig. 3.10: Calorimetrically measured soft-switching losses (SSL) of the 10 kV SiC MOSFETs for different DC-link voltages, switched currents, gate resistors and a measurement temperature range of 30...40 °C. Unless otherwise noted, the turn-off gate resistor is $R_{off} = 10\,\Omega$.

Comparing the three 7 kV curves with different turn-off gate resistors R_{off} in **Fig. 3.10**, it is evident that a turn-off resistor of $R_{\text{off}} = 10\,\Omega$ leads to the lowest SSL. For the case of $R_{\text{off}} = 15\,\Omega$, the dependency on the switched current shows a clear trend towards higher losses for higher switched currents which is an indication for increased channel losses due to a larger overlapping of the voltage and current transients during turn-off. This behavior can be explained by analyzing the soft-switching transitions given in **Fig. 3.11** for 7 kV and 15 A. While the switching transitions are almost equally fast for turn-off gate resistors of 5 Ω and 10 Ω, the switching transition for a gate resistor of 15 Ω is clearly slowed down. Hence, especially for higher switched currents, the higher gate resistance leads to a stronger overlapping of the MOSFET voltage and channel current transients and thus to higher SL. On the other hand, a low turn-off gate resistance of 5 Ω results in stronger oscillations in the drain current due to parasitic inductances introduced by the semiconductor packages and thus causes higher SSL. Consequently, for the 10 kV SiC MOSFETs at hand, the optimum turn-off gate resistance is $R_{\text{off}} = 10\,\Omega$, which could be probably slightly decreased if another package with lower parasitic inductances and/or with Kelvin source connection would be available/used. However, even though the packaging can be improved, a substantial reduction of the SSL is not expected. Furthermore, it should be mentioned that the turn-on resistor

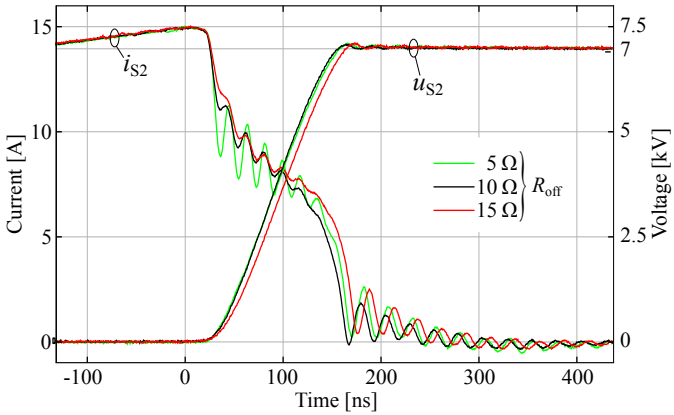

Fig. 3.11: Comparison of soft-switching transitions for different turn-off gate resistors at $U_{\text{DC}} = 7\,\text{kV}$ and $i_{\text{sw}} = 15\,\text{A}$.

does not or hardly influence the SSL.

3.5 Output Capacitance Charging and Discharging Losses

In **Fig. 3.10**, it is clearly visible that the measured SSL are strongly depending on the DC-link voltage (with an approximately quadratic relation $E_{\mathrm{sw}} \sim U_{\mathrm{DC}}^2$) whereas the dependency on the switched current is linear with a rather flat and voltage-independent slope. Furthermore, the SSL curves do not pass through the origin, if they are extrapolated towards zero current. In contrast, the curves show a voltage-dependent offset, which means that there are voltage-dependent residual SSL which cannot be avoided. This indicates that a large share of the SSL might just arise from the charging and discharging of the parasitic output capacitances of the MOSFET and the antiparallel JBS diode, and only a minor share of the SSL is actually caused by the overlap of the MOSFET's voltage and channel-current transients. The loss mechanisms related to the charging/discharging of the nonlinear output capacitance have already been discussed for Superjunction MOSFETs [177, 183], where significant fractions (strongly depending on the device) of the stored energy in the output capacitance are lost during the charging/discharging process. In [184], this effect is explained via a mixed-mode simulation of low-voltage Superjunction MOSFETs. In the following, an accurate calorimetric method to measure the charging/discharging losses (CDL) is presented. Furthermore, in order to identify to which component the CDL have to be allocated, i.e. the MOSFET or the antiparallel JBS diode, on the one hand the proposed method is applied to a module consisting of a 10 kV SiC MOSFET with an antiparallel JBS diode (cf. **Fig. 3.1(a)**), and on the other hand to a module containing only a JBS diode (cf. **Fig. 3.1(b)**).

3.5.1 Description of the Charging/Discharging Loss Measurement Method

For the measurement of the CDL of the 10 kV SiC devices, the same measurement setup as for the determination of the SSL can be used. The DUT is still mounted on a thermally insulated brass block, however, instead of placing the DUT in series, it is now connected in parallel

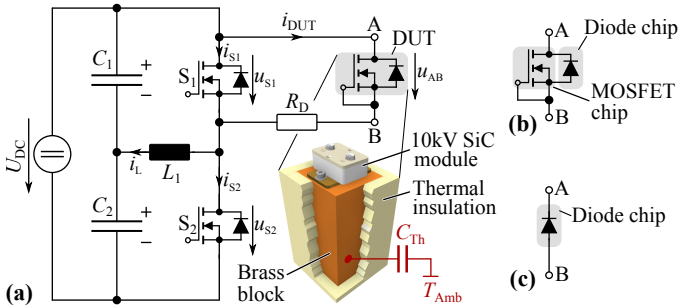

Fig. 3.12: **(a)** Circuit diagram of the charging/discharging loss (CDL) measurement setup. The DUT (permanently turned-off) is connected in parallel to the high-side switch S_1 via a damping resistor R_D. The two possible DUTs: **(b)** Co-Pack module consisting of a SiC-MOSFET chip and an antiparallel JBS diode chip and **(c)** discrete packaged JBS diode.

to the high-side switch S_1 (cf. **Fig. 3.12(a)**), which means that the voltage across the high-side switch is also applied to the DUT. Since only the CDL should be measured, the DUT is permanently kept off by shorting the DUT's gate to the source terminal, thus the DUT only behaves like an additional nonlinear capacitor connected in parallel to the high-side switch S_1. Due to the parasitic inductances of the module packages and the interconnections, a damping resistor R_D is added in series to the DUT in order to avoid any ringing between the DUT and the high-side MOSFET during the switching transitions. In addition, during the on-state of S_1, R_D also prevents the DUT from reverse conduction, i.e. either through the body-diode of the SiC-MOSFET or the antiparallel JBS diode. As shown in **Fig. 3.13 (a)**, there is only a current i_{DUT} flowing through the DUT during the switching transitions, whereas during the conduction intervals of S_1 and S_2 the current i_{DUT} is zero.

The value of R_D was experimentally determined and is set to $R_D = 20\,\Omega$. It should be noted that, due to the device's relatively high blocking voltage compared to its current rating, the voltage drop across R_D during the switching transition is negligible compared to the switched voltage, i.e. $u_{AB} \approx u_{S1}$. Hence, the voltage u_{AB} across the DUT closely follows the high-side MOSFET's voltage u_{S1} and the output capacitance of the DUT is entirely charged and discharged in each switching cycle. Accordingly, even though the voltage across R_D is comparatively small,

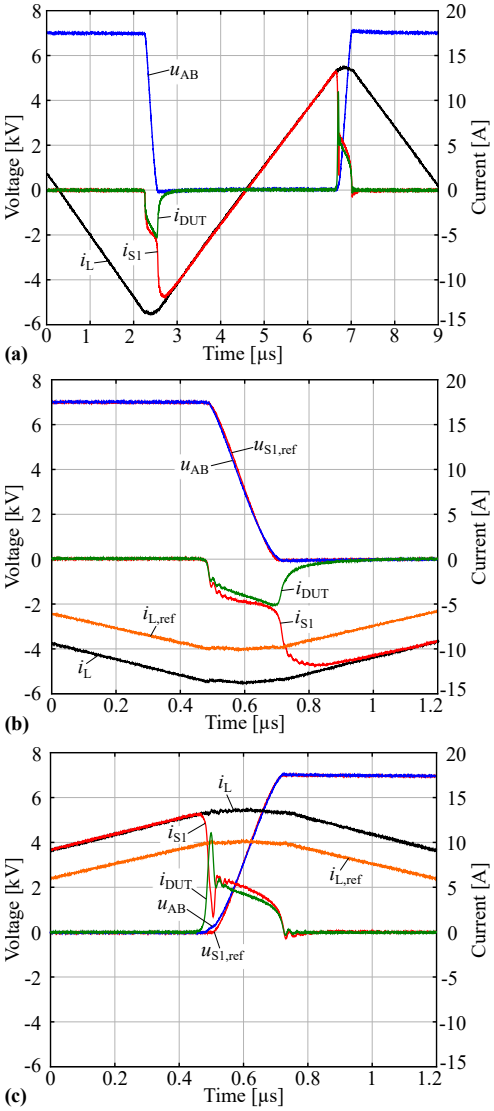

Fig. 3.13: **(a)** Current and voltage waveforms of the 7 kV, 10 A-equivalent CDL measurement. Detailed view of the waveforms **(b)** during the falling voltage transition and **(c)** during the rising voltage transition, where u_{AB} is matched to the voltage slope of $u_{S1,ref}$, which was obtained from the 7 kV, 10 A SSL measurement.

depending on the switching frequency a significant amount of losses is dissipated in R_{D}. Therefore, R_{D} has to be thermally decoupled from the DUT in order not to influence the temperature measurement on the DUT's metal block.

Due to the parallel connection of the DUT to the high-side switch, the effective output capacitance of the half-bridge is increased, which means that compared to the SSL measurements for a given switched current the corresponding voltage slope, i.e. the $\mathrm{d}u/\mathrm{d}t$, is slowed down. In other words, for a given current, in this setup the charging current flowing through the DUT is lower compared to the current flowing through the MOSFET's parasitic output capacitance in the SSL measurements. However, in order to be able to properly assign the CDL to the correct SSL measurements, the DUT has to be tested under the same conditions. In this case, this means that the total switched current, i.e. the inductor current i_{L}, has to be increased in such a way that in both, the CDL measurement and the SSL measurement, the same $\mathrm{d}u/\mathrm{d}t$ is achieved. Consequently, based on $i = C \cdot \mathrm{d}u/\mathrm{d}t$, also the charging current in the DUT has to be the same. Exemplarily, **Figs. 3.13(b) & (c)** show the measured waveforms during the two switching transients of the CDL measurement, which actually correspond to the SSL measurement carried out at $i_{\mathrm{L,ref}} = 10\,\mathrm{A}$. As can be noticed, in order to match the voltage slope u_{AB} to the corresponding voltage slope $u_{\mathrm{S1,ref}}$, the inductor current i_{L} has to be increased to 13.5 A. This ratio between the reference current $i_{\mathrm{L,ref}}$ and the required current i_{L} slightly changes with the DC-link voltage and the current level due to the strong nonlinearity of the devices' output capacitances. However, as can be noticed, there is still a small deviation between u_{AB} and the reference voltage $u_{\mathrm{S1,ref}}$, which in consequence also leads to a slightly different charging current waveform. The reason is that, due to the parallel connection of the DUT and the high-side switch, the effective output capacitance of the high-side switch is larger than the one of the low-side switch and therefore the half-bridge is no longer symmetrical. This asymmetry can be compensated by also adding a DUT to the low-side switch, however, in this case the total output capacitance of the half-bridge is doubled. Consequently, for the SSL measurement at $i_{\mathrm{L,ref}} = 15\,\mathrm{A}$ (cf. **Fig. 3.10**) the corresponding CDL measurement would have to be performed at $i_{\mathrm{L}} = 30\,\mathrm{A}$, which is not possible with the given setup. Nevertheless, regardless whether one or two DUTs are used, the current pulses through the DUT are not equal for both tran-

sitions (cf. **Figs. 3.13(b) & (c)**), since due to the nonlinear output capacitances of the devices, the inductor current i_{L} is not equally divided among the high-side and low-side switches during the switching transitions. **Fig. 3.14** shows the measured input (C_{iss}), reverse transfer (C_{rss}), and output capacitance ($C_{\mathrm{oss,Co-Pack}}$) of the Co-Pack, as well as the measured output capacitance of the discrete JBS diode module (C_{Diode}) as a function of the applied bias voltage. Furthermore, the output capacitance of the MOSFET chip ($C_{\mathrm{oss,MOSFET}}$), which has been obtained by taking the difference $C_{\mathrm{oss,Co-Pack}} - C_{\mathrm{Diode}}$, is shown. It can be seen that the output capacitances of the MOSFET and the JBS diode are strongly nonlinear in the lower voltage range. Furthermore, it is evident that for higher voltages, the capacitance of the JBS diode is twice as high as the output capacitance of the MOSFET chip.

Therefore, in **Fig. 3.13(b)**, for example, the voltage u_{AB} across the DUT is initially at the DC-link voltage level, hence the output capacitance of the DUT and the switch S_1 is small compared to the one of S_2 and only a small part of the inductor current i_{L} is initially flowing through the DUT's output capacitance. On the other hand, when u_{AB} is small, the major part of i_{L} is charging the DUT's output capacitance, as shown in **Fig. 3.13(c)**.

For the actual measurement of the CDL, the same measurement principle as described for the SSL measurements is used (cf. **Section 3.3**). The DUT is mounted on a thermally insulated brass block and the measurement temperature range is again 30 °C...40 °C unless otherwise noted. However, in order to identify which component, i.e. the SiC-MOSFET or the JBS diode, is causing the CDL, two different types of modules, a Co-Pack module containing a SiC-MOSFET with a JBS diode and a module with only a JBS diode, are tested (cf. **Fig. 3.12(b) & (c)** and **Fig. 3.1(a) & (b)**).

3.5.2 Measurement Results

In **Fig. 3.15**, the results of the CDL measurements obtained with the Co-Pack module (denoted as CDL, 30...40 °C (MOSFET + Diode)) are shown together with the results of the SSL measurements for DC-link voltages of 4...7 kV and currents between 2.5 A and 15 A. Surprisingly, at low currents the CDL and the SSL are almost identical and with higher currents, the losses are drifting apart from each other as indicated with the gray areas. This residual loss fraction, which is the loss differ-

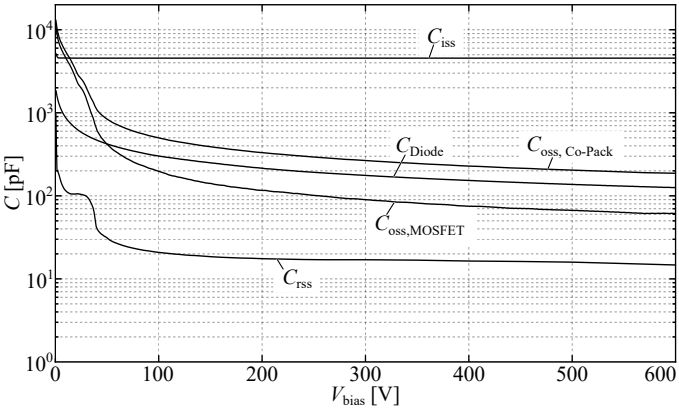

Fig. 3.14: Measured capacitances of the 10 kV SiC devices as function of the applied bias voltage V_{bias}. Note that the output capacitance of the MOSFET chip ($C_{\text{oss,MOSFET}}$) is obtained by subtracting the measured output capacitance of the Co-Pack ($C_{\text{oss,Co-Pack}}$) and the output capacitance of the JBS diode (C_{Diode}).

ence between the SSL and the CDL, should actually correspond to the turn-off losses caused in the MOSFET-channel due to the overlapping of the voltage and current transients. Unexpectedly, the residual losses are increasing with decreasing DC-link voltage. Actually, the residual losses should be independent from the applied DC-link voltage, since on the one hand the MOSFET-channel losses are only generated in the initial period of the switching transition where the MOSFET-channel has not yet completely stopped conducting, and on the other hand the $\mathrm{d}u/\mathrm{d}t$ only depends on the switched current, which consequently results in the same overlapping of voltage and current transients. It is reasonable that the MOSFET-channel losses increase with increasing switched current, however, in this case typically the total SSL would not anymore increase linearly but rather disproportionally as shown in **Fig. 3.10** for a turn-off resistor of $R_{\text{off}} = 15\,\Omega$. Therefore, it is presumed that the deviation between the measured SSL and the CDL is caused by the introduced (and indispensable) damping resistor R_{D}, which on the one hand distorts the current waveform in the DUT - especially at higher currents or $\mathrm{d}u/\mathrm{d}t$-values - and on the other hand the voltage across R_{D} (worst-case is $20\,\Omega \cdot 15\,\text{A} = 300\,\text{V}$) becomes more dominant at lower DC-link voltages. This means that, due to the linear slope of the SSL

with respect to the switched current and the fact that the CDL and the SSL are equal at low current, the two measurements should effectively be more or less equal at higher current ratings.

Notwithstanding the above, the key message of the measurement results is that the SSL are almost exclusively originating from the charging/discharging of the DUT's output capacitance and not from the overlapping of the voltage and current transients. Consequently, the CDL constitute a lower limit for the SSL, independently of the gate driver performance and the packaging inductances of the device, which only affect the already comparably low turn-off losses.

Additionally, the CDL would also directly affect the performance of resonant DC-link inverters which achieve ZVS by forcing the drain-source voltage of the MOSFETs to zero during the current commutation by means of introducing a resonance to the DC-link capacitor [185–187]. Thereby, although the commutation of the load current within one MOSFET half-bridge is performed under zero voltage (and can be

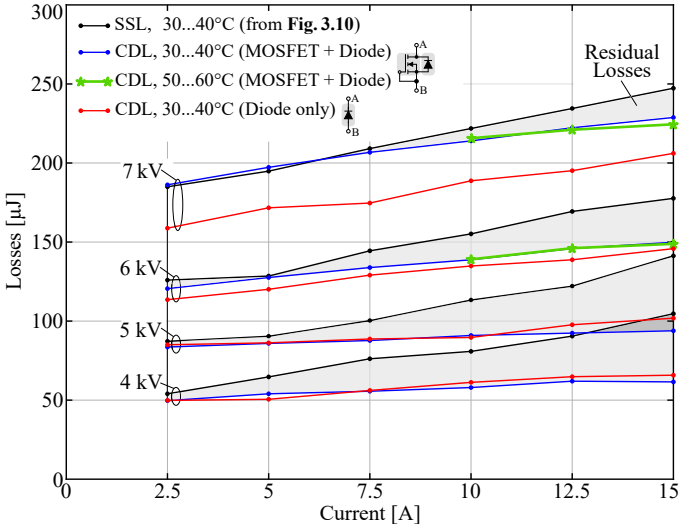

Fig. 3.15: Measured charging/discharging losses (CDL) of the Co-Pack module and the separate JBS diode together with the corresponding soft-switching loss (SSL) curves from **Fig. 3.10**. Note that measurements obtained at 30...40 °C and 50...60 °C are almost identical, i.e. the CDL are independent of the junction temperature.

assumed as lossless), the output capacitances of the MOSFETs still have to be charged and discharged, leading to certain $\mathrm{d}u/\mathrm{d}t$-dependent CDL, which have to be taken into account.

Furthermore, for the analysis of the temperature dependency of the CDL, the measurements were also conducted at a higher brass block temperature range of 50...60 °C (cf. **Fig. 3.15**, denoted as CDL, 50...60 °C (MOSFET + Diode)). As can be seen, the measurements obtained at 30...40 °C and 50...60 °C are almost identical. Hence, the CDL, and since these losses account for the majority of the SSL, also the SSL can be assumed to be independent from the chip temperature, as it is also the case for the HSL measured in [109, 113, 188].

In order to get a better idea about the resulting losses of the underlying application, the CDL, which in this case more or less correspond to the SSL, are set in relation to the stored energy in the parasitic output capacitance. For the tested 10 kV SiC Co-Pack modules, the SSL approximately correspond to $5\% - 10\%$ of the stored energy within the measured current and voltage range which underpins the outstanding switching characteristics of these 10 kV SiC devices and enables the use of comparably high switching frequencies in soft-switched applications.

It is now clear that the CDL of the 10 kV SiC Co-Pack modules at hand are responsible for the largest share of the SSL. However, the question in which component, i.e. the SiC-MOSFET or the JBS diode, the CDL are generated, remains. Therefore, besides the Co-Pack module also a separate discrete JBS diode in an identical package is tested (cf. **Fig. 3.12(c)**). The corresponding CDL measurements are also shown in **Fig. 3.15** (denoted as CDL, 30...40 °C (Diode only)). For DC-link voltages of 4...6 kV, the CDL of the diode are more or less equal to the losses measured with the Co-Pack module. At a DC-link voltage of 7 kV, however, the measured CDL are slightly lower compared to the losses of the Co-Pack module, which means that the MOSFET starts to contribute to the CDL. Nevertheless, based on these measurements, the majority of the CDL, and consequently also of the SSL, have to be attributed to the JBS diode and surprisingly not to the SiC-MOSFET. Unfortunately, the CDL and their distribution among the JBS diode and the MOSFET cannot be estimated by the measurement of their output capacitances, since, although the capacitance of the JBS diode is only two times larger than the output capacitance of the MOSFET (cf. **Fig. 3.14** at higher voltages), almost the entire CDL are generated by the JBS diode. Therefore, it has to be assumed that the CDL loss

mechanisms are not the same in the JBS diode and the MOSFET.

As a consequence, to strongly reduce the SL in converter systems employing soft-switching techniques, the JBS diode could be omitted and instead the body diode of the SiC-MOSFET could be used. Even though the body diode might have a much higher forward voltage drop, the additional CL in the short dead time interval are relatively small compared to the saved SSL. Unfortunately, since a module with a separate SiC-MOSFET was not available, this statement could not be confirmed experimentally.

3.6 Comparison of SSL and HSL

For the selection of a power electronic converter topology, a fundamental question is whether the switches should operate under hard-switching or under soft-switching conditions. As a basis for a decision, switching loss data for both operating modes is required. However, since the 10 kV SiC MOSFETs at hand are prototype devices, the datasheet does not contain any switching loss data yet. Therefore, besides the SSL, which have been discussed in detail in this chapter, also HSL measurements have been conducted. As shown in **Section 3.2.1**, the double-pulse test is well suited for the measurement of HSL and hence, this method has been employed for the determination of the HSL. Thereby, a turn-on gate resistor of $R_{\mathrm{on}} = 20\,\Omega$ and a turn-off gate resistor of $R_{\mathrm{off}} = 10\,\Omega$ have been used.

Fig. 3.16(a) & (b) show the switching energies E_{on} and E_{off}, respectively, for different DC-link voltages and different switched currents. As can be seen, the turn-on energy E_{on} is a linear function of the switched current and shows a voltage dependent offset and slope, whereas the turn-off energy is almost constant for different currents but shows a strongly voltage-dependent offset, since E_{off} mainly consists of the stored energy in the output capacitance C_{oss} of the MOSFET module.

Compared to the SSL in **Fig. 3.10**, the HSL are significantly higher. The SSL within one switching cycle of a bridge-leg are $2E_{\mathrm{ZVS}}$, while the HSL are $E_{\mathrm{on}} + E_{\mathrm{off}}$. E.g. for a switched current of 10 A at a DC-link voltage of 7 kV, the SSL per switching cycle are $2E_{\mathrm{ZVS}} = 440\,\mu\mathrm{J}$, whereas the HSL for the same conditions are $E_{\mathrm{on}} + E_{\mathrm{off}} = 14.25\,\mathrm{mJ}$ per switching cycle, i.e. a factor of 32 higher. For example, with a switching frequency of 10 kHz, the HSL would account for 142.5 W, whereas under

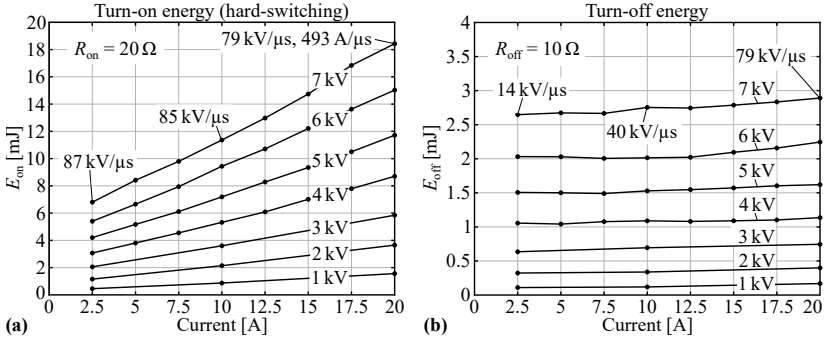

Fig. 3.16: Measured hard-switching energies of the 10 kV SiC MOSFETs for different DC-link voltages and different switched currents. **(a)** Turn-on energy E_{on} and **(b)** turn-off energy E_{off}.

soft-switching conditions, SSL of only 4.4 W would arise. Consequently, the switching losses can be almost eliminated by applying soft-switching techniques, which allows to improve both, the power density and the efficiency of a converter employing the analyzed 10 kV SiC MOSFETs.

3.7 Summary

In this chapter, a novel accurate calorimetric method for the measurement of SSL of 10 kV SiC MOSFETs has been developed. As shown in literature, electrical measurement methods such as the double-pulse test can lead to large measurement errors, and thus are unsuitable for the characterization of the considered 10 kV SiC MOSFET and other fast-switching devices. On the other hand, with calorimetric measurement methods, the total semiconductor losses can be measured accurately. However, the calorimetric methods presented in literature so far were not able to separate the SL from the CL without calculations of e.g. the CL which could result again in certain measurement errors. This disadvantage is eliminated by the proposed measurement method, where an additional switch is introduced which in combination with a novel modulation scheme enables to measure the CL and the SL separately. The error analysis for the proposed measurement method shows that the worst-case error is 15 %, which is a factor of 10 to 20 more accurate

than the accuracy obtained with the double-pulse method. Based on the proposed measurement method, the SSL of the 10 kV SiC MOSFET are examined for different DC-link voltages, switched currents and gate resistors.

Additional CDL measurements revealed that the charging and discharging process of the output capacitances of the MOSFET and the antiparallel JBS diode generate the largest part of the SSL. Furthermore, by testing a Co-Pack module (consisting of a 10 kV SiC-MOSFET in combination with a 10 kV JBS diode) and a separate 10 kV JBS diode module, it could be identified that the major part of the CDL and hence a major part of the SSL surprisingly has to be attributed to the JBS diode and not to the SiC-MOSFET.

Compared to the HSL, the SSL are almost 30 times lower, which enables a higher converter performance. However, the SSL are still relevant in comparison to the CL and therefore have to be considered in the converter design, especially for applications utilizing high switching frequencies.

4

10 kV SiC-Based ZVS Bidirectional PFC Single-Phase AC/DC Stage

Due to their extremely high energy demand, data centers are directly supplied from the MV-AC grid. However, a significant share of this energy is dissipated in the power supply chain, since the MV is reduced step-by-step through multiple power conversion stages down to the chip voltage level. In order to increase the efficiency of the power supply chain, the number of conversion stages must be substantially reduced. In this context, SSTs are considered as a possible solution as they could directly interface the MV-AC grid to a 400 V DC bus, whereby server racks with a power consumption of several tens of kilowatts could be directly supplied from an individual SST. With a focus on the lowest system complexity, the SST ideally should be built as simple two-stage system consisting of an MV AC/DC PFC rectifier stage followed by an isolated DC/DC converter. Accordingly, this chapter focuses on the design and realization of a 25 kW, 3.8 kV single-phase AC to 7 kV DC power factor corrected (PFC) rectifier unit based on 10 kV SiC MOSFETs. A design example shows that the efficiency and the power density would be significantly limited by the SL if a conventional hard-switched topology was used. Therefore, by simply adding an LC-circuit between the switch-nodes of the well-known full-bridge-based PWM AC/DC rectifier, the integrated Triangular Current Mode (iTCM) concept is developed, which only internally superimposes a large triangular current ripple on the AC mains current and thus enables zero voltage switching (ZVS) over the entire AC mains period. Besides the high achievable efficiency, thanks to ZVS also a high switching frequency can be selected, resulting in a high power density.

After the derivation of the *i*TCM topology and modulation, a theoretical analysis shows that the minimization of parasitic capacitances is highly important for MV converters of this power class, and based on this, the design of all main components with a focus on low parasitic capacitances is presented, whereby special attention is paid to the realization of the MV inductors and their electrical insulation, the AC-input LCL-filter to limit EMI emissions, and the challenges arising due to cable resonances when connecting the SST to the MV-AC grid via an MV cable. The calorimetric measurement methods used to accurately determine the converter efficiency are discussed in detail and their accuracy is evaluated with a theoretical error analysis. Despite the large insulation distances required for MV, the realized 25 kW MV PFC rectifier achieves an unprecedented power density and efficiency compared to existing systems.

4.1 Introduction

The growing number of high-power DC loads such as data centers or EV battery charging facilities but also DC sources such as large-scale PV power plants require an MV-AC to LV-DC conversion to connect them to the MV-AC grid. Compared to the state-of-the-art solution consisting of an LFT and an AC/DC converter, SST technology is considered as a more efficient and more compact solution to provide the interface between the MV-AC grid and e.g. a 400 V DC bus [33, 40–42]. In case of data centers, each server rack (with a typical power rating of 20 ... 40 kW [68, 73, 74]) could be supplied by an individual SST from the MV distribution grid with the further advantage of lower cable cross sections and/or lower losses compared to an LV distribution inside the data center.

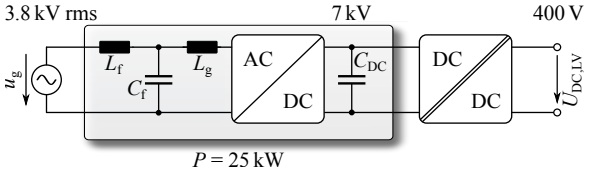

Fig. 4.1: Single-cell realization of an MV-AC to 400 V DC SST. In this chapter the AC/DC converter and the LCL-filter are realized.

One possible solution to directly interface the MV-AC grid with power electronics is to share the high voltage among several series-connected converter modules, which are realized with commercially available 1200 V ... 1700 V SiC MOSFETs or IGBTs. Such a system with five converter cells and a total power of 25 kW has been presented by *Fuji Electric* [92] and achieves a full-load efficiency of 96 % from 2.4 kV AC to 54 V DC and a power density of 0.4 kW/L. With this approach, the individual converter cells have to be isolated from each other and also from the (typically metallic) enclosure due to the different cell potentials. Furthermore, each converter cell contains an isolated DC/DC stage, whose MF transformer also has to be isolated for the full voltage (although the cells, which are on lower potential, could be designed for a lower isolation voltage, it makes sense to dimension all cells for the full voltage in order to improve manufacturability). However, this means that the required isolation distances occur several times within the multi-cell system, which is very space-consuming and hence leads to a rather low power density [92].

To decrease the system volume and the system complexity, the number of components and the number of the space-consuming isolation barriers has to be reduced, which leads to the concept of a single-cell converter with only one isolation transformer. However, up to the present, this approach has only been feasible for very high system powers in the megawatt range, since the only available semiconductors with sufficient blocking voltage were high-power MV GTOs, IGCTs, or IGBTs, which show significant switching losses and are thus unsuitable for the comparably low power of 25 kW and the high switching frequency aimed for in this work.

With the development of the new generation of 10 kV SiC MOSFETs, the approach to interface the MV-AC grid directly with a single-cell converter becomes also feasible for systems with a comparably low power due to the excellent switching behavior of these MV SiC MOSFETs (cf. **Chapter 3**), which allows very high switching frequencies despite the high blocking voltage. **Fig. 4.1** shows the block diagram of a single-cell MV-AC to LV-DC SST consisting of a single-cell AC/DC PFC rectifier followed by an isolated single-cell DC/DC converter. The EMI noise is limited by an AC-side LCL-filter in front of the PFC rectifier, which is a typical filter structure used for MV converters [58]. Due to the greatly reduced complexity compared to the multi-cell approach and the fact that there is only one isolation barrier, a significantly

Tab. 4.1: AC/DC converter specifications.

Parameter	Symbol	Value
Power	P	25 kW
AC voltage (rms)	u_{g}	3.8 kV
DC voltage	U_{DC}	7 kV
Mains frequency	f_{g}	50 Hz
AC/DC target efficiency	$\eta_{\mathrm{t,AC/DC}}$	99 %

higher power density is expected. Furthermore, due to the outstanding conduction characteristics of the 10 kV SiC MOSFETs, which are much closer to the theoretical SiC limit than e.g. 1200 V SiC MOSFETs due to the lower impact of the SiC MOSFET channel resistance compared to the SiC bulk resistance in MV devices [189], also a higher efficiency can be expected (i.e. a series connection of e.g. eight 1200 V SiC MOSFETs to achieve a blocking voltage of 10 kV would result in a higher on-state resistance compared to a single 10 kV SiC MOSFET chip, if an equal chip area is assumed).

Therefore, the bidirectional 25 kW, 3.8 kV AC to 400 V DC SST is realized as a single-cell system employing 10 kV SiC MOSFETs, whereby the focus of this chapter is on the bidirectional AC/DC converter stage, the LCL-filter, and the challenges arising from interfacing the SST to the MV grid via an MV cable, which could be subject to undesired oscillations that need to be avoided by a termination network. The specifications of the AC/DC converter are summarized in **Tab. 4.1** and as can be seen, the targeted full-load efficiency is $\eta_{\mathrm{t,AC/DC}} = 99\,\%$ in order to reach the target efficiency of $\eta_{\mathrm{SST}} = 98\,\%$ for the complete SST in case a 50:50 distribution of the losses between the AC/DC and the DC/DC converters is assumed.

Due to the high voltage blocking capability of the utilized 10 kV SiC MOSFETs, a simple full-bridge-based PWM AC/DC converter topology is selected. However, without further measures, hard-switching and thus comparably high switching losses would occur [104, 109, 110, 190, 191]. Consequently, the achievable efficiency and power density would be strongly restricted, since the switching losses are defining an upper limit for the switching frequency, and hence inhibit a possible downsizing of passive components. The most effective strategy to reduce the switching losses is to apply soft-switching techniques and to profit

from the much lower soft-switching losses compared to hard-switching (cf. **Chapter 3**). Additionally, EMI can be significantly reduced with soft-switching, since the $\mathrm{d}u/\mathrm{d}t$ values are typically much lower than for hard-switching.

Soft-switching can be achieved e.g. with the Triangular Current Mode (TCM) concept [167, 168, 192, 193], where the boost inductance value is reduced to such extent, that the large HF triangular current ripple superimposed to the instantaneous LF grid current leads to a reversal of the current direction in the semiconductors in each switching cycle and accordingly enables ZVS for each switching transition, resulting in extremely low switching losses compared to hard-switching. On the other hand, however, with the TCM operation the boost inductor design becomes more challenging since both, the HF and the LF currents are flowing through the same inductor. In order to keep the HF losses in the inductor low, the employment of HF litz wire with thin strand diameter and HF core materials (e.g. ferrite) is necessary. Unfortunately, litz wire features a low copper filling factor and also the saturation flux density of HF core materials is typically low. However, in order to keep also the LF losses low, a winding with a high copper filling factor (i.e. solid copper wire) and a core material with a high saturation flux density (e.g. amorphous iron, iron powder or nanocrystalline core material) would be needed. Hence, with TCM operation, a reasonable trade-off between HF and LF losses has to be found in the design of the boost inductor.

In order to overcome this disadvantage, the concept of the *integrated* Triangular Current Mode (*i*TCM) operation is developed and applied to the considered 25 kW, 3.8 kV single-phase AC to 7 kV DC converter [194, 195]. By adding an LC-circuit between the switch-nodes of the full-bridge PWM AC/DC converter, the TCM current can be split into HF and LF current components, which are then flowing through two separate inductors. Advantageously, the large TCM ripple current then does not flow towards the grid (as usual for TCM topologies) but is kept internally in the circuit. Accordingly, this concept is called *integrated* Triangular Current Mode (*i*TCM) operation. Since the superposition of HF and LF current, i.e. the TCM current, is only needed in the semiconductor devices to guarantee soft-switching, this current separation enables a dedicated design of the two inductors, i.e. either an optimization for an LF or an HF current, and thus results in an expected efficiency improvement compared to the usual TCM opera-

tion. A further advantage of the *i*TCM concept is that the well-known PWM modulation scheme still can be applied and no additional control or measurement circuitry, e.g. current zero crossing detection, as needed in TCM operation, is required.

This chapter is organized as follows: **Section 4.2** shows that the conventional hard-switched full-bridge AC/DC topology would be subject to high SL and thus would be significantly limited in performance. Therefore, the *i*TCM converter topology and its modulation are developed and explained in detail. In **Section 4.3**, the design procedure of the individual components of the converter is presented. Special attention is paid to the low-capacitive design of the MV inductors and their insulation, as well as the connection of the SST to the MV-AC grid without exciting oscillations in the supplying MV cable. **Section 4.4** shows the experimental setup and explains the applied calorimetric loss measurement methods in detail. In **Section 4.5**, the laboratory setup is briefly discussed and **Section 4.6** presents the experimental results, including characteristic waveforms and the calorimetrically measured converter efficiency and loss distribution. Finally, the chapter is summarized in **Section 4.7**.

4.2 Integrated Triangular Current Mode (*i*TCM) Concept

4.2.1 State-of-the-Art PWM AC/DC Converter Operation

A very common topology to interface a single-phase AC grid to a DC bus with bidirectional power flow capability is the full-bridge-based PFC AC/DC converter topology shown in **Fig. 4.2 (a)**. There, the switches are typically operated with a constant switching frequency and a variable duty cycle (i.e. with PWM) to generate the sinusoidal AC voltage. In the following, it is assumed that only bridge-leg A is pulse-width modulated, whereas bridge-leg B is operated as 50 Hz unfolder in order to not generate a HF CM voltage at switch-node B, which is directly connected to the AC grid, e.g. to an MV cable or an LFT. Without loss of generality, the following would also hold for alternative modulation schemes.

For the operation of this state-of-the-art converter, the boost induc-

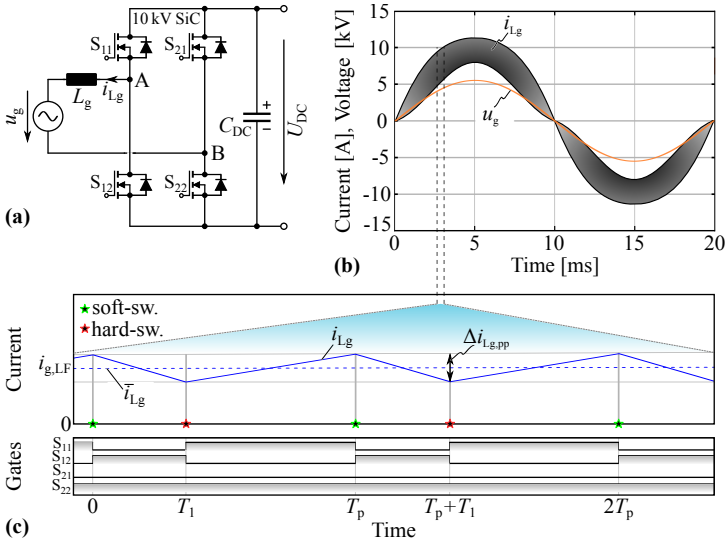

Fig. 4.2: **(a)** Circuit diagram of a bidirectional single-phase full-bridge AC/DC converter. **(b)** Waveforms of the grid voltage u_g and the boost inductor current i_{Lg} over one grid period. **(c)** Detailed view of the current i_{Lg} , the gate control signals, and the corresponding hard- and soft-switching time instants.

tor L_g is typically selected relatively large in order to keep the current ripple $\Delta i_{Lg,pp}$ small, e.g. within 10 %...40 % of the peak LF current. In **Fig. 4.2 (b)**, the grid voltage u_g and the corresponding inductor current i_{Lg} are shown over an entire mains period in case the converter is operated as inverter with a 40 % peak-to-peak current ripple. To analyze the converter operation in more detail, **Fig. 4.2 (c)** shows a magnified view of the boost inductor current i_{Lg} and the corresponding gate control signals. As can be noticed, due to the large inductance value, the inductor current remains positive during the entire switching cycle for the shown time section. Consequently, as indicated in **Fig. 4.2 (c)**, soft-switching is only achieved in the transitions at the time instants $t = k \cdot T_p$ (whereby $k = [0, 1, 2, 3 \ldots]$), whereas hard-switching occurs at the time instants $t = T_1 + k \cdot T_p$.

As can be seen in the results of the conducted switching loss measurements in **Chapter 3**, the hard-switching loss energy of one bridge-

leg consisting of the employed 10 kV SiC MOSFETs during a complete switching cycle is $E_{sw} = E_{on} + E_{off} = 11\,\text{mJ}$, if an average turn-on current of 5 A (average of the lower envelope of the boost inductor current in **Fig. 4.2(b)**) is considered. With this value and the rms current through the MOSFETs, the semiconductor losses are calculated. Furthermore, the losses and the volume of a suitable boost inductor have been calculated and the performance of such a PWM converter is estimated based on these values. **Tab. 4.2** shows the resulting characteristics of the PWM converter in case a switching frequency of 10 kHz is assumed.

As can be seen, the switching losses are twice as high as the conduction losses of the MOSFETs and the required boost inductance value as well as the volume of the boost inductor (consisting of an amorphous core and a litz wire winding with 200 µm strand diameter) are comparably large. Furthermore, the targeted efficiency of $\eta_{t,AC/DC} = 99\,\%$ cannot be reached, while the estimated power density is rather low at the same time, since also the additional filter components to achieve a

Tab. 4.2: PWM Converter Characteristics.

Parameter	**Symbol**	**Value**
Switching frequency	f_{sw}	10 kHz
Switching energy (per cycle)	E_{sw}	11 mJ
Current ripple	$\Delta i_{Lg,pp}$	40 %
Boost inductance	L_g	47 mH
Inductor volume	V_{Lg}	3.25 L
DC-link volume	V_{CDC}	1.9 L
Filter volume	V_{filt}	1.6 L
Bridge volume	V_{bridge}	2.9 L
Inductor losses	P_{Lg}	127 W
MOSFET $R_{DS,on}$, $T_j = 125\,°C$	$R_{DS,on}$	600 mΩ
MOSFET rms current	$I_{FET,rms}$	4.7 A
Switching losses	P_{sw}	110 W
MOSFET conduction losses	P_c	53 W
Aux. losses	P_{aux}	20 W
Filter damping losses	P_d	10 W
Estimated efficiency	η_{PWM}	≈ 98.7 %
Estimated power density	ρ_{PWM}	≈ 2.1 kW/L

smooth grid current would be relatively large. If the volume of passive components such as the boost inductor should be decreased by increasing the switching frequency, the switching losses increase even more, or vice versa, if the switching losses should be decreased, the inductor volume increases. Hence, the performance (efficiency and power density) of the conventional PWM AC/DC converter is mainly and significantly limited by the HSL of the 10 kV SiC MOSFETs.

Therefore, a method for the reduction of the switching losses has to be developed to increase the system performance. Considering again the results of the switching loss measurements in **Chapter 3**, the measured soft-switching loss energies per switching cycle are approximately a factor of 30 lower than the corresponding hard-switching losses, i.e. $2 \cdot E_{\mathrm{ZVS}} \approx 1/30 \cdot (E_{\mathrm{on}} + E_{\mathrm{off}})$. Consequently, if soft-switching can be achieved throughout the entire grid period, the switching losses can be almost eliminated ($110\,\mathrm{W}/30 = 3.66\,\mathrm{W}$).

In order to turn the hard-switching transitions at $t = T_1$ and $t = T_\mathrm{p} + T_1$ (cf. **Fig. 4.2(c)**) into soft-switching transitions, the inductor current needs to reverse its direction during each switching cycle and hence, a higher current ripple is required, as given for the TCM modulation scheme [167, 168, 192, 193]. In the following, an alternative method to achieve soft-switching is developed and the topology is derived step-by-step on the basis of the conventional PWM AC/DC converter topology shown in **Fig. 4.2(a)**.

4.2.2 Derivation of the *i*TCM Topology

As already mentioned, a higher current ripple is required to change the sign of the inductor current in each switching cycle and to enable soft-switching of the MOSFETs. This can e.g. be attained by connecting an inductor L_b with a comparably low inductance value in parallel to L_g, as shown in **Fig. 4.3 (a)**. The grid current i_g is now shared among the two inductors according to the current divider rule and due to the high current ripple in L_b, the grid current i_g is now negative at the time instants $t = T_1$ and $t = T_\mathrm{p} + T_1$. In order to achieve complete soft-switching, the grid current needs to reach the minimum required turn-off current $-I_{\mathrm{ZVS}}$, which can be calculated based on the effective output charge Q_{OSS} of the MOSFETs required to charge/discharge their output capacitances C_{OSS} (and further parasitic capacitances), and the maximum allowed duration of this resonant switching transition (i.e.

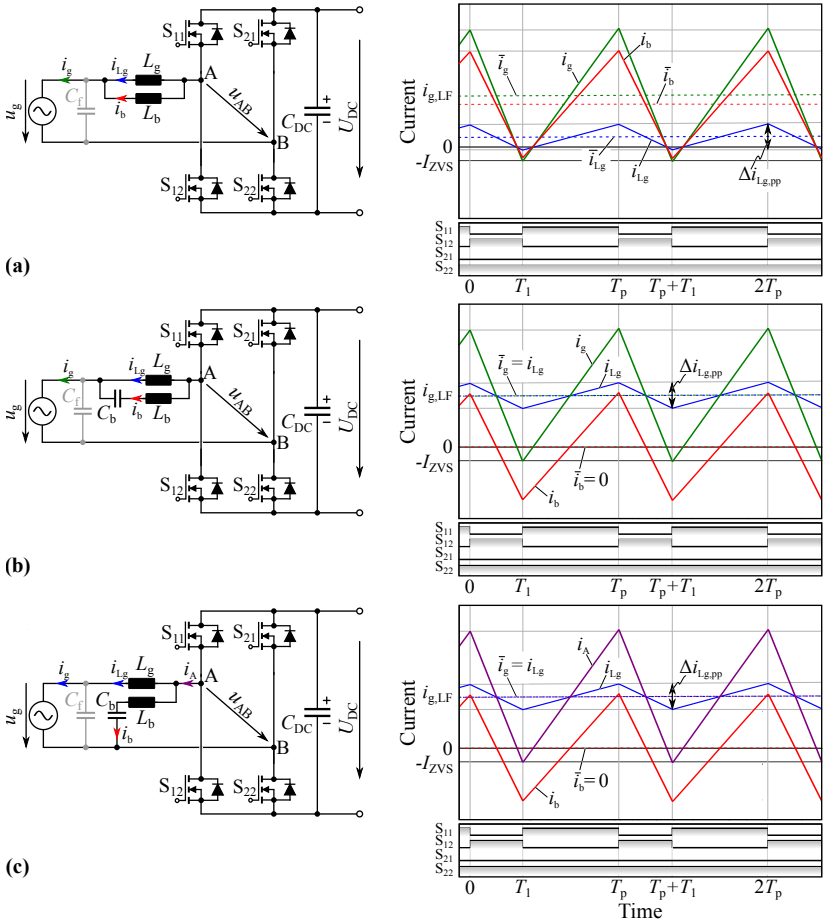

Fig. 4.3: **(a)** Bidirectional full-bridge AC/DC converter with an additional inductor L_b in order to increase the current ripple and to obtain soft-switching. The corresponding waveforms show the grid current i_g as well as the triangular HF current i_b and the boost inductor current i_{Lg}. The average values of the currents are indicated with dotted lines. **(b)** Splitting of the HF and LF currents by adding an LF blocking capacitor C_b in series to L_b. **(c)** HF bypassing of the AC grid by returning the current i_b via C_b back into the full-bridge. The grid current i_g is now again equal to i_g in the original circuit shown in **Fig. 4.2 (a)**. However, soft-switching operation of the MOSFETs is achieved.

the dead time duration T_{dt}). Hence, in order not to limit the duty cycle range and/or to be able to control the input/output voltage in a wide range, T_{dt} has to be small, e.g. $c = 1\,\%$ of the switching period T_{p} [168]. The minimum required current I_{ZVS} can roughly be calculated as

$$I_{\mathrm{ZVS}} = Q_{\mathrm{OSS}}/T_{\mathrm{dt}} = Q_{\mathrm{OSS}}/\left(c \cdot T_{\mathrm{p}}\right) \tag{4.1}$$

and is set to $I_{\mathrm{ZVS}} = 4.5\,\mathrm{A}$ for the converter at hand.

The attained current waveforms in **Fig. 4.3 (a)** are now equal to the current waveforms of a full-bridge converter operated with the usual TCM modulation scheme. The only difference is that the total TCM current is split into two separate currents. Since the same voltage $u_{\mathrm{g}} - u_{\mathrm{AB}}$ is applied to L_{g} and L_{b}, both inductors exhibit current wavevorms of the same shape with LF and HF amplitudes only depending on the ratio of L_{g} and L_{b}. Due to the much smaller inductance of L_{b} compared to L_{g}, the HF but also the LF current is mainly flowing through L_{b} (cf. **Fig. 4.3 (a)**).

In order to prevent any DC or LF current from flowing through L_{b}, a capacitor C_{b} can be added in series to L_{b}, as shown in **Fig. 4.3 (b)**. Consequently, L_{b} now carries only the HF current and L_{g} conducts the total LF current with a small superimposed HF ripple (cf. **Fig. 4.3 (b)**). As can be noted, even if C_{b} is added, the total grid current remains unchanged (assuming that the mains frequency component of u_{AB} is adjusted such, that the mains frequency voltage drop across L_{g} is increased accordingly).

Instead of connecting the $L_{\mathrm{b}}/C_{\mathrm{b}}$-branch directly in parallel to L_{g}, it is also possible to connect it in parallel to the $L_{\mathrm{g}}/C_{\mathrm{f}}$-branch with the purpose of bypassing the AC grid, i.e. guiding the HF current directly back into the full-bridge [195], as shown in **Fig. 4.3 (c)**. Thereby, C_{f} embodies the typically needed filter capacitor. The two currents i_{Lg} and i_{b} are not affected by this modification, since C_{b} still prevents a mains frequency current flow and/or represents a low impedance only for switching frequency components of u_{AB}, resulting in the same currents i_{Lg} and i_{b} as obtained in **Fig. 4.3 (b)**. Hence, soft-switching is still achieved since the current i_{A} (as the sum of the two inductor currents) flowing out of bridge-leg A still changes its sign in each switching cycle. Even though the capacitor C_{b} now has to be designed to block the full grid voltage u_{g}, the advantage of this modification is that the HF current i_{b} is no more flowing into the grid (where an increased filter effort would be necessary), but is kept internally in the circuit. There-

fore, this concept is referred to as *integrated* Triangular Current Mode (*i*TCM).

Compared to the initial full-bridge-based PWM AC/DC converter (cf. **Fig. 4.2 (a)**), the grid current i_g is not affected by the *i*TCM concept and thus, the EMI filter effort towards the AC grid remains the same. However, due to soft-switching in case of *i*TCM operation, the switching losses are drastically reduced compared to the hard-switched PWM converter. Hence, with the *i*TCM concept, a higher switching frequency can be applied, which means that for the same current ripple in L_g, a smaller inductance value L_g can be selected. Therefore, even though an LC-branch has to be added for *i*TCM operation, the power density can be increased compared to PWM operation if the additional volume of the LC-branch is smaller than the saved volume of the typically bulky boost inductor L_g. Consequently, compared to the conventional PWM converter, a higher efficiency and a higher power density are feasible at the same time by employing the *i*TCM concept.

For the operation of the AC/DC converter in an MV-AC grid, the emission of current harmonics should be limited in order to not generate grid resonances. Therefore, an LCL-filter is added and the final *i*TCM topology is shown in **Fig. 4.4(a)**, whereby the LC-branch has been drawn between the two bridge-legs for better visibility. It should be noted that the additional filter stage does not affect the operating principle and therefore the waveforms shown in **Fig. 4.3(c)** are still valid.

4.2.3 *i*TCM Modulation

The derivation of the *i*TCM topology has shown that soft-switching can be achieved on a switching-period timebase. However, for an efficient operation of the converter, it is required that soft-switching is achieved over the entire AC grid period.

Constant Switching Frequency Modulation

For the further investigations, it is still assumed that the bridge-leg B of the *i*TCM converter (cf. **Fig. 4.4(a)**) is operated as unfolder with mains frequency, i.e. 50 Hz and is therefore referenced as LF bridge-leg, whereas the bridge-leg A is pulse-width modulated with a constant switching frequency f_{sw} and is referenced as HF bridge-leg. The corresponding duty cycles d_{HF} and d_{LF} of the HF and the LF bridge-leg are

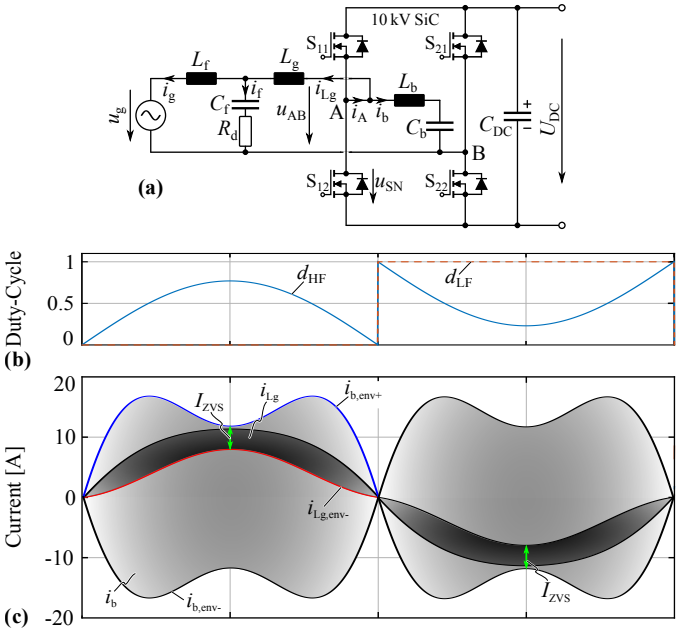

Fig. 4.4: **(a)** Circuit diagram of the MV PFC AC/DC converter with AC-side LCL-filter and additonal LC-branch consisting of L_b and C_b to implement the *integrated* TCM concept, which enables soft-switching over the entire AC mains period. **(b)** Duty cycles d_HF and d_LF of the HF and LF bridge-legs. **(c)** Envelopes of the currents i_b and i_Lg over a mains period in case of a constant switching frequency.

shown in **Fig. 4.4(b)**.

The critical point in the AC grid period where the highest current in L_b is needed to achieve soft-switching, is located at the peak of the AC grid current. **Fig. 4.4(c)** shows the resulting envelopes of the currents i_Lg and i_b in the inductors L_g and L_b, respectively, over an entire grid period in case of a constant switching frequency. The inductance value of L_b can be calculated as a function of the peak-to-peak current ripple r (in % of the peak LF mains current) in the boost inductor L_g in such a way, that a turn-off current of I_ZVS is achieved at the peak of the grid current:

$$L_\mathrm{b} = \frac{\hat{u}_\mathrm{g}^2}{2P\,(2-r) + 2I_\mathrm{ZVS}\hat{u}_\mathrm{g}} \left(1 - \frac{\hat{u}_\mathrm{g}}{U_\mathrm{DC}}\right) \frac{1}{f_\mathrm{sw}}, \tag{4.2}$$

where $\hat{u}_\mathrm{g}$ denotes the peak AC grid voltage ($\hat{u}_\mathrm{g} = \sqrt{2} \cdot u_\mathrm{g}$), U_DC the DC-link voltage, and P the system power. Furthermore, the inductance value of the boost inductor L_g, dimensioned for a maximum current ripple r, can be found as

$$L_\mathrm{g} = \frac{\hat{u}_\mathrm{g}^2}{2 r f_\mathrm{sw} P} \left(1 - \frac{\hat{u}_\mathrm{g}}{U_\mathrm{DC}}\right). \tag{4.3}$$

In **Fig. 4.4(c)**, for symmetrical currents, the switched current can be seen as difference of the upper envelope of i_b ($i_\mathrm{b,env+}$) and the lower envelope of i_Lg ($i_\mathrm{Lg,env-}$), i.e. $i_\mathrm{sw} = i_\mathrm{b,env+} - i_\mathrm{Lg,env-}$, and as can be seen, soft-switching is achieved over the entire grid period. However, instead of keeping the rather low switching frequency of 10 kHz and (as already mentioned) reducing the switching losses by a factor of 30 by operating under soft-switching conditions compared to hard-switching, a compromise between power density and efficiency is made and the switching frequency is increased to 35 kHz. Thereby, the expected switching losses are still very low and at the same time, the volume of the passive components can be decreased significantly.

As can be seen in **Fig. 4.4(c)**, with a constant switching frequency, the switched current is not constant over the grid period but strongly varies. Especially in the proximity of points in time where the duty cycle d_HF is equal to 0.5 and the current ripple reaches its maximum, the switched current is much higher than the required value I_ZVS (indicated by the green arrows). This results in higher rms currents in the inductor L_b and the switches, thus causing higher conduction losses.

Variable Switching Frequency Modulation

In order to avoid these extra losses where $|i_\mathrm{b,env+} - i_\mathrm{Lg,env-}| > I_\mathrm{ZVS}$, the switching frequency can be shaped in such a way that the HF current ripple of i_b is locally reduced and in every switching transient the desired turn-off current I_ZVS is achieved, i.e.

$$|i_\mathrm{b,env+} - i_\mathrm{Lg,env-}| \stackrel{!}{=} I_\mathrm{ZVS}. \tag{4.4}$$

The upper envelope of i_b and the lower envelope of i_Lg can be expressed as

$$i_\mathrm{b,env+} = A\,(t) \cdot \frac{\hat{u}_\mathrm{g}}{2 f_\mathrm{sw} L_\mathrm{b}}, \quad \text{and} \tag{4.5}$$

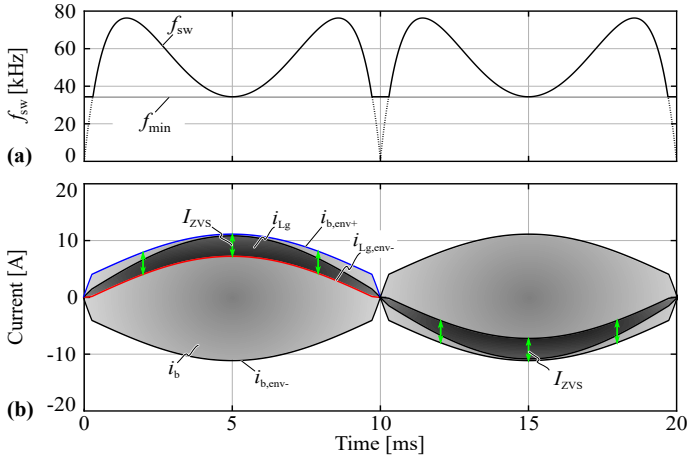

Fig. 4.5: **(a)** Variable switching frequency f_{sw} over an entire grid period. The function is limited to the minimum frequency f_{min}, which corresponds to the value that has been selected for the operation with constant switching frequency (35 kHz). **(b)** Envelopes of the currents i_{b} and i_{Lg} over a mains period. The MOSFETs turn off a constant current I_{ZVS}, as indicated by the green arrows.

$$i_{\mathrm{Lg,env-}} = \frac{2P}{\hat{u}_{\mathrm{g}}} \left|\sin\left(\omega_{\mathrm{g}} \cdot t\right)\right| - A\left(t\right) \cdot \frac{\hat{u}_{\mathrm{g}}}{2 f_{\mathrm{sw}} L_{\mathrm{g}}}, \tag{4.6}$$

with

$$A\left(t\right) = \left|\sin\left(\omega_{\mathrm{g}} t\right)\right| \cdot \left[1 - \frac{\hat{u}_{\mathrm{g}}}{U_{\mathrm{DC}}} \cdot \left|\sin\left(\omega_{\mathrm{g}} t\right)\right|\right], \tag{4.7}$$

where ω_{g} denotes the AC grid angular frequency, P the system power, and f_{sw} the switching frequency. By inserting (4.5) and (4.6) into (4.4) and solving for f_{sw}, the time-dependent switching frequency, which ensures a constant turn-off current I_{ZVS}, can be found as

$$f_{\mathrm{sw}} = \frac{A\left(t\right) \hat{u}_{\mathrm{g}}^2}{4P \left|\sin\left(\omega_{\mathrm{g}} t\right)\right| + 2\hat{u}_{\mathrm{g}} I_{\mathrm{ZVS}}} \cdot \left(\frac{1}{L_{\mathrm{g}}} + \frac{1}{L_{\mathrm{b}}}\right). \tag{4.8}$$

The resulting switching frequency pattern f_{sw} and the envelopes of the currents i_{Lg} and i_{b} are shown in **Fig. 4.5**. Since the inductance values of L_{g} and L_{b} have been designed for the operating point at the peak of the grid current, the switching frequency reaches its minimum $f_{\mathrm{min}} = 35\,\mathrm{kHz}$ exactly at this point and is also artificially limited

to $f_{\min}$ at the zero crossings. As can be seen, the switched current $|i_{\mathrm{b,env+}} - i_{\mathrm{Lg,env-}}|$ is now constant and equal to I_{ZVS} over the entire grid period, as indicated with the green arrows in **Fig. 4.5(b)**.

However, this function holds only for a grid current which is in phase with the grid voltage (i.e. a purely sinusoidal current in this case). Due to the capacitors C_{b} and C_{f} (cf. **Fig. 4.4(a)**), as well as C_{t}, which will be introduced in **Section 4.3.7**, the converter has to deliver a small amount of reactive power, i.e. small LF cosine currents are superimposed on the inductor currents i_{b} and i_{Lg} considered so far. In order to still maintain a constant ZVS current, this deviation from the ideal waveforms has to be compensated by the switching frequency,

$$f_{\mathrm{sw}} = \left(\frac{1}{L_{\mathrm{g}}} + \frac{1}{L_{\mathrm{b}}}\right) \cdot \frac{A\,(t)\,\hat{u}_{\mathrm{g}}^2}{4P\,|\sin\left(\omega_{\mathrm{g}} t\right)| + 2\left(\hat{u}_{\mathrm{g}} I_{\mathrm{ZVS}} + \hat{u}_{\mathrm{g}}^2 \omega_{\mathrm{g}} C_{\mathrm{equ}} \cdot \cos\left(\omega_{\mathrm{g}} t\right)\right)}, \tag{4.9}$$

whereby $C_{\mathrm{equ}} = C_{\mathrm{b}} + C_{\mathrm{f}}$ is the equivalent capacitance causing the LF cosine current.

Fig. 4.6 shows the simulated current waveforms for a peak-to-peak ripple of $r = 40\,\%$ in L_{g} together with the adapted switching frequency pattern, whereby the capacitors C_{b} and C_{f} are taken into account. As can be seen, the capacitive LF current $i_{\mathrm{f,50\,Hz}}$ causes a slight phase-shift between the grid current i_{g} and the boost inductor current i_{Lg}. Nevertheless, with the adapted switching frequency pattern, the turn-off current I_{ZVS} can be kept constant as can be seen in the envelope of the current $i_{\mathrm{A}} = i_{\mathrm{b}} + i_{\mathrm{Lg}}$ flowing out of the HF bridge-leg. The average switching frequency is now 52.6 kHz, i.e. a factor of 5 higher than the original switching frequency of the conventional PWM converter (cf. **Tab. 4.2**).

It should be noted that the maximum switching frequency increases with increasing reactive power, i.e. for excessive reactive power levels, ZVS might be lost if e.g. due to efficiency reasons an upper limit for the maximum switching frequency is defined. The converter at hand is designed to handle reactive powers of approximately $\pm 30\,\%$ of the nominal power.

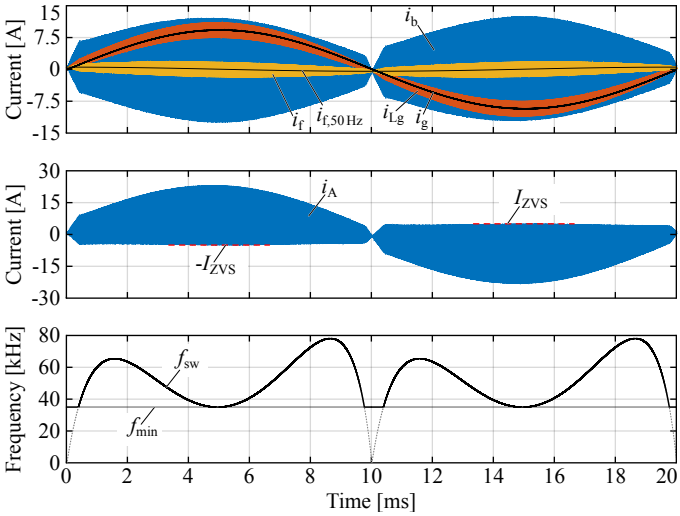

Fig. 4.6: Ideal current waveforms of the *i*TCM converter considering the capacitive line-frequency currents through C_b and C_f which cause a slight asymmetry of the current ripples in L_b and L_g. In order to maintain a constant turn-off current (as can be seen in the current i_A), the switching frequency pattern becomes asymmetric within each mains half-period.

4.3 System Design

In the following, a theoretical analysis of the impact of parasitic inductances and capacitances on the proper operation of power electronic converters is given in dependency of their characteristic impedance. Based on these findings, the individual components are designed and optimized for high efficiency and power density.

4.3.1 General HV-SiC-Based Converter Design Considerations

In the following analysis, the *i*TCM converter with its DC-link voltage of 7 kV and its power rating of 25 kW is compared to a 400 V system with the same power rating, in order to point out an important fundamental difference between the design of MV converters and LV converters regarding parasitic inductances and capacitances.

For each power electronic converter, a characteristic impedance, i.e. the ratio between the switched voltage (the DC-link voltage) and the switched current can be defined [196]:

$$Z_{\mathrm{sw}} = U_{\mathrm{DC}}/I_{\mathrm{L}}. \tag{4.10}$$

This characteristic impedance is a useful quantity to analyze the impact of parasitics on the switching behavior of a bridge-leg. For the analysis of the impact of parasitic inductances, the schematic and the idealized waveforms given in **Fig. 4.7** are considered. If the low-side MOSFET turns off the current I_{L} in a fixed switching time t_{s}, a certain voltage u_σ occurs across the parasitic commutation loop inductance L_σ, which represents the sum of the MOSFET package inductances, the PCB inductances, and the parasitic inductance of the DC-link capacitor. This voltage increases the low-side switch voltage u_{S} and/or causes a switching voltage overshoot, as shown in **Fig. 4.7**. If the impedance of the parasitic commutation loop inductance L_σ is in the same order of magnitude as the characteristic impedance Z_{sw}, the magnitude of the voltage overshoot across the switch is in the same range as the switched voltage U_{DC}. Consequently, to limit the voltage overshoot to a certain value, e.g. $k_{\mathrm{u}} = 10\,\%$ of the DC-link voltage, an upper limit for the value of L_σ can be defined. The induced voltage overshoot and the limiting condition can be expressed as

$$u_\sigma = L_\sigma \frac{I_{\mathrm{L}}}{t_{\mathrm{s}}} \leq k_{\mathrm{u}} \cdot U_{\mathrm{DC}}. \tag{4.11}$$

Reformulating this equation by using (4.10) results in the maximum allowed commutation loop inductance L_σ that leads to the maximum admissible voltage overshoot in dependency of the characteristic impedance Z_{sw} and the switching time t_{s}:

$$L_\sigma \leq k_{\mathrm{u}} \cdot t_{\mathrm{s}} \cdot Z_{\mathrm{sw}}. \tag{4.12}$$

To show the difference between an MV converter and an LV converter from a parasitics point of view, the impedance Z_{sw} of the *i*TCM converter at hand and the impedance of a similar converter with 400 V DC-link voltage are calculated. While the 7 kV system shows an impedance of

$$Z_{\mathrm{sw,7kV}} = 7\,\mathrm{kV}/22.5\,\mathrm{A} = 311\,\Omega \tag{4.13}$$

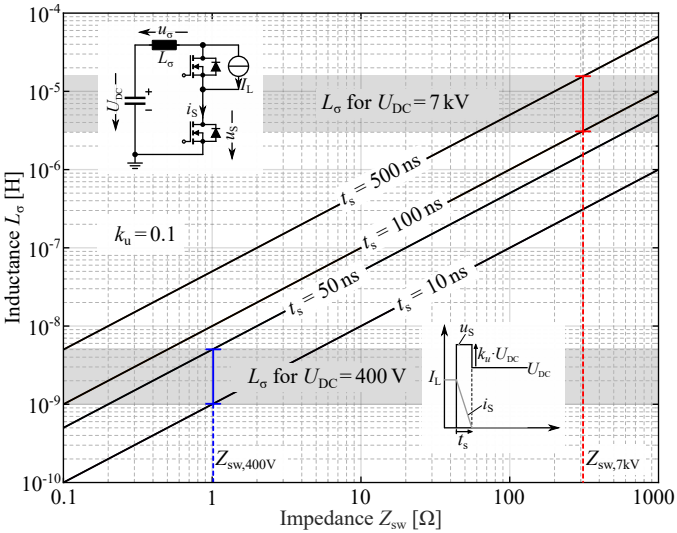

Fig. 4.7: Highest allowed inductance L_σ in the commutation path for a maximum allowed voltage overshoot of $k_u = 10\,\%$ of the switched voltage U_{DC} in dependency of the characteristic impedance Z_{sw} and the switching time t_s. A constant di/dt is assumed. The typical switching speeds (10 ... 100 ns for LV devices and 100 ... 500 ns for MV SiC devices) as well as the impedances $Z_{sw,400V}$ and $Z_{sw,7kV}$, and the resulting ranges of the parasitic inductance L_σ are highlighted.

(in case of an AC/DC converter the maximum switched current is considered and can be read from **Fig. 4.6**), the 400 V system would show an impedance of only

$$Z_{sw,400V} = \left(\frac{400\,V}{7\,kV}\right)^2 \cdot Z_{sw,7kV} \approx 1\,\Omega. \tag{4.14}$$

Furthermore, it has to be considered that for the 7 kV converter, the typical switching time of a 10 kV SiC MOSFET bridge-leg is between $t_s = 100$ ns and $t_s = 500$ ns [124], while typical switching times for a 400 V converter are in the range of $t_s = 10$ ns and $t_s = 50$ ns.

The graph in **Fig. 4.7** shows the impact of Z_{sw} on L_σ for the aforementioned switching times and $k_u = 0.1$. The impedances $Z_{sw,400V}$ and $Z_{sw,7kV}$ are indicated with a blue and a red line, respectively. As can be seen, the commutation loop inductance for a 400 V system has

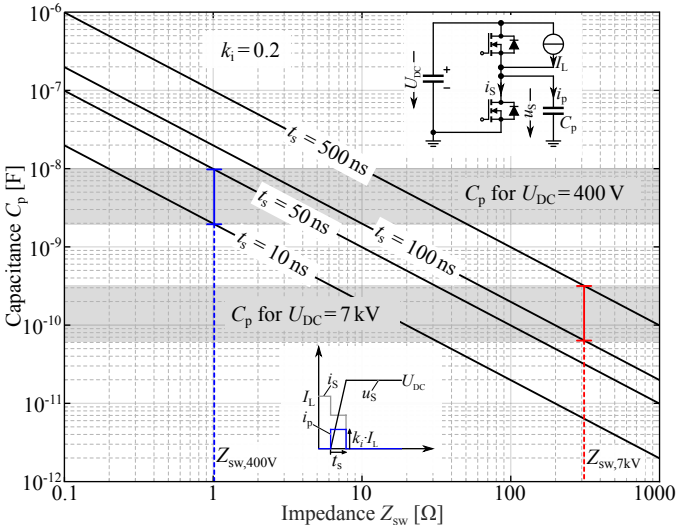

Fig. 4.8: Highest allowed parasitic capacitance C_p connected to the switch-node for a maximum capacitive current of $k_i = 20\,\%$ of the switched current I_L in dependency of the characteristic impedance Z_{sw} and the switching time t_s. A constant du/dt is assumed. The typical switching speeds ($10 \ldots 100\,\text{ns}$ for LV devices and $100 \ldots 500\,\text{ns}$ for MV SiC devices) as well as the impedances $Z_{sw,400V}$ and $Z_{sw,7kV}$, and the resulting capacitance ranges are highlighted.

to be kept very low in the range of $1 \ldots 5\,\text{nH}$, i.e. the parasitic inductances of the MOSFET packages, the DC-link capacitor, and the circuit layout have to be strictly minimized. In contrast, the allowed commutation loop inductance for the 7 kV converter at hand is in the range of $3 \ldots 15\,\mu\text{H}$. This means that the PCB and busbar inductances as well as the parasitic MOSFET package inductances (apart from the gate loop inductance, which is not affected by these considerations and should always be minimized) are relatively uncritical for this particular converter due to its high characteristic impedance or in other words due to its relatively low power considering the high input and output voltages.

A similar analysis can be conducted in order to demonstrate the impact of parasitic capacitances that are lumped into an equivalent capacitance C_p connected between the switch-node of the bridge-leg and ground, as shown in **Fig. 4.8**. Such capacitances are, besides the

nonlinear output capacitances C_{OSS} of the MOSFETs, e.g. parasitic capacitances from the MOSFET chips to the heat sink, parasitic capacitances of inductive components connected to the switch-node, and also the coupling capacitance of the high-side gate driver supply and signal transmission. If an ideal switching transition is assumed again, i.e. the DC-link voltage U_{DC} is switched within the time t_{s}, as shown in the waveforms in **Fig. 4.8**, the voltage slope across the parasitic capacitance C_{p} causes a certain current i_{p} and in case the impedance of C_{p} is in the same order of magnitude as the impedance Z_{sw}, the magnitude of i_{p} is in the same range as the switched current I_{L}. However, for a proper operation of the converter and to reduce EMI, this capacitive current should be limited to e.g. $k_{\mathrm{i}} = 20\,\%$ of the switched current, which leads to

$$i_{\mathrm{p}} = C_{\mathrm{p}} \frac{U_{\mathrm{DC}}}{t_{\mathrm{s}}} \leq k_{\mathrm{i}} \cdot I_{\mathrm{L}}. \tag{4.15}$$

By inserting (4.10) in this equation, the highest allowed parasitic capacitance C_{p}, which leads to the defined maximum admissible capacitive current, is given in dependency on the characteristic impedance Z_{sw} and the switching time t_{s} as

$$C_{\mathrm{p}} \leq \frac{k_{\mathrm{i}} \cdot t_{\mathrm{s}}}{Z_{\mathrm{sw}}}. \tag{4.16}$$

The limits for the parasitic capacitance C_{p} are shown in **Fig. 4.8**, again for the typical switching speeds of an equivalent 400 V system ($t_{\mathrm{s}} = 10\,\mathrm{ns} \ldots t_{\mathrm{s}} = 50\,\mathrm{ns}$) and the 7 kV system ($t_{\mathrm{s}} = 100\,\mathrm{ns} \ldots t_{\mathrm{s}} = 500\,\mathrm{ns}$). As can be seen (blue line), a rather high capacitance in the range of $2 \ldots 10\,\mathrm{nF}$ can be allowed for the 400 V system, and therefore parasitic capacitances are mostly uncritical for LV applications (apart from an increased CM filter effort).

However, considering the 7 kV converter (red line), the maximum allowed capacitance is only in the range between $65\,\mathrm{pF} \ldots 320\,\mathrm{pF}$, which is a factor of 30 less than in case of a 400 V converter. Consequently, it is very important to design the MV converter with the goal to minimize parasitic capacitances, whereas parasitic inductances play a minor role as shown above. E.g. for the PCB design, this means that coplanar tracks or coplanar polygons must be avoided (also due to the fact that the PCB material would hardly be able to reliably insulate the high voltages). Instead, PCB tracks on jumping potential should be separated from other potentials as far as possible in order to minimize parasitic capacitances.

4.3.2 Inductor Design

As already mentioned, the triangular current i_A flowing through the full-bridge is the sum of the currents in the inductors L_b and L_g (as shown in **Fig. 4.4(a)**), which in total has to reach a certain value I_{ZVS} at the turn-off switching instant to guarantee soft-switching of the MOSFETs. However, the sharing of the required current ripple among the two currents i_b and i_{Lg} to achieve I_{ZVS} is a free parameter, which can be optimized e.g. regarding power density and losses of the two inductors. A priori, it is not clear whether a high or a rather low current ripple in L_g leads to the smallest overall volume and losses. Therefore, optimizations of the inductors L_b and L_g regarding power density and losses have been carried out with an arbitrary sweep over the following parameters:

- peak-to-peak ripple r in L_g;
- core dimensions;
- ferrite, amorphous, and nanocrystalline core material;
- number of turns;
- litz wire / solid wire diameter;
- strand diameter,

whereby the insulation distances between the winding and the core are fixed (cf. **Section 4.3.2**).

The results of the optimization indicate that the best L_b designs consist of a ferrite core with HF litz wire windings, as expected for a pure HF AC flux. On the other hand, however, the best L_g designs utilize nanocrystalline core material and also HF litz wire windings but with a rather thick strand diameter. Due to the HF ripple and the high switching frequency, solid copper wire is subject to relatively high HF losses (mainly due to the fringing field of the air gap) and therefore inferior to HF litz wire. **Fig. 4.9(a)** shows the Pareto fronts of the optimization results for inductor L_b, whereby the labels depict the peak-to-peak current ripple r in L_g which is set between 20 % and 80 % of the peak grid current. As can be seen, the current ripple r has almost no influence on the inductor losses and volume, which is why the Pareto fronts for different ripples are very close to each other.

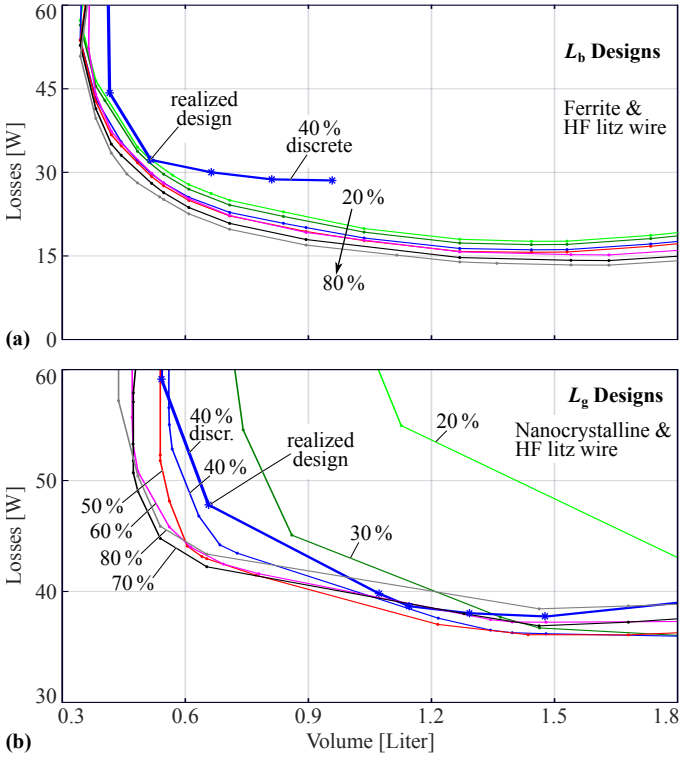

Fig. 4.9: Volume/loss optimization of the inductor L_b **(a)** and L_g **(b)** for different peak-to-peak current ripples in L_g (referenced to the peak mains current). The core size, the number of turns, the litz wire diameter, and the strand diameter are freely swept, in order to explore the theoretical limits. The curves marked with '40 % discrete' show designs with discrete available cores and litz wires for a 40 % peak-to-peak current ripple in L_g.

This can be explained by the fact that the peak current in L_b, which is given as $\hat{i}_\mathrm{b} = \frac{P}{U_\mathrm{g}} \cdot \sqrt{2} - \Delta i_\mathrm{Lg,pp}/2 + I_\mathrm{ZVS}$, decreases only from 12.9 A to 10.1 A when the ripple in the other inductor L_g is increased from 20 % to 80 %. This means that it is possible to find a good design of L_b for any current ripple $\Delta i_\mathrm{Lg,pp}$ in L_g between 20 % to 80 %, whereby designs with higher ripples in L_g are slightly beneficial.

As shown in the optimization results for inductor L_g in **Fig. 4.9(b)**, a clear trend towards more efficient and more compact designs can be

Tab. 4.3: Realized inductors L_b and L_g.

Ind.	Type	Core mat.	Core	Turns	HF litz
L_b	E-core	Ferrite N87	3xE65	3x17	270x0.071 mm
L_g	C-core	Finemet	4xF3CC-25	4x29	150x0.1 mm

seen for an increasing current ripple in L_g (also observed in [197]). From this perspective, a large current ripple in L_g would be beneficial in terms of power density and efficiency of both inductors L_b and L_g. However, a large current ripple in L_g would also result in a higher filtering effort and therefore in an increased size of the remaining input filter components C_f and L_f of the LCL-filter. E.g. a current ripple of $r > 200\,\%$ would actually mean usual TCM operation (i.e. the LC-branch would not be needed anymore), but the full triangular current ripple would then flow towards the MV grid and would have to be attenuated by $C_\mathrm{f}/L_\mathrm{f}$ or even an additional filter stage to obtain a smooth grid current. The opposite extreme, i.e. a very small current ripple of $r \leq 5\,\%$ would lead to a very high inductance value L_g and therefore to a large volume of L_g. As a trade-off, a current ripple in L_g of $r = 40\,\%$ peak-to-peak is selected, since the 40 % Pareto front shows a much better performance than the designs with 20 % and 30 % current ripple, and at the same time it is only slightly worse than the 50 % to 80 % Pareto fronts (only +15 % in volume and losses compared to the Pareto-optimal designs). With the selected ripple in L_g of $r = 40\,\%$, the inductance values of L_b and L_g can be calculated with (4.2) and (4.3). For the system at hand, the values are $L_\mathrm{b} = 1.49\,\mathrm{mH}$ and $L_\mathrm{g} = 9.55\,\mathrm{mH}$.

For the realization of the inductors L_b and L_g, discrete designs with available core shapes and HF litz wires have to be determined. Therefore, instead of a continuous optimization sweep, an optimization with available core shapes and available HF litz wires has been carried out for a ripple of $r = 40\,\%$. The results for discrete L_b and L_g designs are shown in **Fig. 4.9(a)** and **(b)**, respectively. It can be seen that the discrete designs come very close to the designs with freely swept parameters. Both of the selected designs are located in the bend of the Pareto fronts, i.e. they represent the best compromise between low volume and low losses. **Tab. 4.3** lists the parameters of the realized inductors.

Inductor Voltage Stresses

For the design of the electrical insulation of the two inductors L_b and L_g, the voltage stresses between their terminals, as well as the voltage stresses between each of their terminals and ground have to be determined in a first step. However, since the voltage stresses of L_b and L_g are equal, the analysis is only carried out for L_b. Therefore, **Figs. 4.10(a)** and **(b)** show the possible arrangements of L_b and C_b between the HF switch-node A and the LF switch-node B of the full-bridge from the *i*TCM topology shown in **Fig. 4.4(a)**. Although L_b and C_b are connected in series in both cases (forming the midpoint T), there is a significant difference in the terminal voltage stress u_T of L_b depending on whether L_b is connected to switch-node A or B. In practice, the voltage u_T will be applied between one terminal of L_b and its ferrite core, which is typically tied to ground potential. Therefore, the electrical insulation between the core and the winding has to be designed accordingly and it is important to select the configuration which leads to the lowest terminal voltage stress in order to minimize the occurring electrical fields and the insulation effort. Since L_b and C_b form an LC-filter, the voltage u_Cb across C_b is (apart from the small HF ripple) equal to the averaged PWM voltage, i.e. the grid voltage u_g (neglecting the small grid frequency voltage drop across L_g required for impressing the grid current). Consequently, the terminal voltage u_T for the configuration shown in **Fig. 4.10(a)** can easily be identified as $u_\mathrm{T} = u_\mathrm{Cb} + u_\mathrm{rec}$ and is shown in **Fig. 4.10(c)**. Since the LF bridge-leg is switched at the zero crossing of u_Cb, u_T is always positive and does not exceed the DC-link voltage of $U_\mathrm{DC} = 7\,\mathrm{kV}$. However, the terminal voltage u_T in the configuration shown in **Fig. 4.10(b)** is now the difference of the HF switch-node voltage u_SN and the line-frequency capacitor voltage u_Cb, i.e. $u_\mathrm{T} = u_\mathrm{SN} - u_\mathrm{Cb}$. As can be seen in **Fig. 4.10(d)**, u_T reaches a peak value of $U_\mathrm{DC} + \hat{u}_\mathrm{g} = 7\,\mathrm{kV} + 5.4\,\mathrm{kV} = 12.4\,\mathrm{kV}$ which is almost twice the maximum value achieved in the configuration from **Fig. 4.10(a)**. Hence, the inductor L_b must be connected to the switch-node of the HF bridge-leg in order to minimize its terminal voltage stess. Furthermore, it is directly evident from the schematic that the differential-mode (DM) voltage u_Lb does not exceed U_DC. For this reason, both the terminal and the DM voltage stresses of L_b and L_g are below or equal to $U_\mathrm{DC} = 7\,\mathrm{kV}$. In order to guarantee its functionality also in case of any undesired overvoltages, the terminal insulation and the DM insulations are designed for 15 kV.

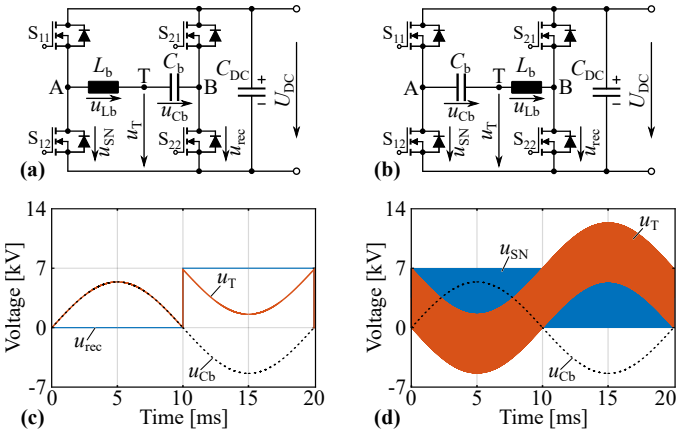

Fig. 4.10: The two possible arrangements of L_b and C_b between the HF bridge-leg (switch-node A) and the LF rectifier bridge-leg (switch-node B) in **(a)** and **(b)**, together with the respective terminal voltages u_T in **(c)** and **(d)**.

Winding Arrangement for Low Parasitic Capacitances

As shown in **Section 4.3.1**, it is very important for the converter at hand to achieve low parasitic capacitances of the magnetic components connected to the switch-nodes in order to reduce the parasitic currents and EMI during the switching transitions. Furthermore, in order to achieve soft-switching of the MOSFETs over the entire grid period, the output capacitances of the MOSFETs have to be charged and discharged in each switching transition. According to (4.1), the required ZVS current is proportional to the charge in the nonlinear parasitic output capacitances of the commutating bridge-leg. However, any additional capacitances, such as the layer-to-layer or winding-to-core capacitances of the inductors L_b and L_g connected to the switch-node also have to be charged and discharged in each switching transition, slowing down the rise and fall times. Therefore, besides the proper electrical insulation, it is also important to minimize the parasitic capacitances of the inductors. From the inductor optimization, the number of layers and the number of turns for L_b and L_g is already given. However, the arrangement of the windings within the winding window can be optimized for low parasitic capacitances. **Fig. 4.11** shows the electric field distri-

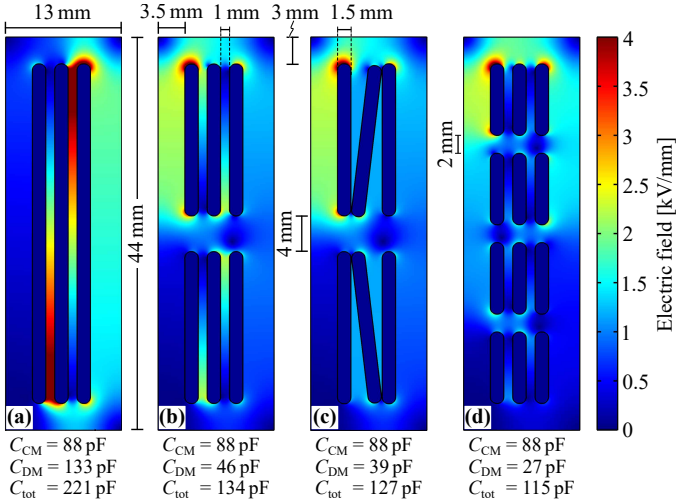

Fig. 4.11: Electric field distribution in the winding window of the inductor L_b for different winding arrangements. **(a)** Three-layer single-chamber winding; **(b)** Three-layer two-chamber winding; **(c)** Three-layer two-chamber conical winding; **(d)** Three-layer four-chamber winding.

bution (obtained from a FEM simulation) of four different winding arrangements of L_b in combination with the list of the corresponding parasitic capacitances C_{CM} (winding-to-core capacitance), C_{DM} (terminal-to-terminal capacitance), and the total capacitance $C_{tot} = C_{CM} + C_{DM}$. As can be seen, the CM capacitance C_{CM} stays constant, independently of the winding arrangement. However, with a multi-chamber arrangement (cf. **Fig. 4.11(b)-(d)**), the DM capacitance C_{DM} can be reduced by more than a factor of three compared to the single-chamber winding. However, comparing the total capacitance C_{tot} of the multi-chamber arrangements, the arrangements in **Fig. 4.11(c) & (d)** do not show significantly reduced capacitances compared to the arrangement shown in **Fig. 4.11(b)**, while being much more complicated in construction. Hence, the arrangement in **Fig. 4.11(b)** is selected for the final realization of L_b. Inductor L_g is realized with a four-layer, two-chamber winding for the same reasons. Furthermore, the isolation distances between the layers, the chambers, and to the core are given in **Fig. 4.11(b)**. The maximum electric field strength is 4 kV/mm (for 7 kV DM voltage), which is well below the 24 kV/mm breakdown field

strength of the utilized silicone in order to be able to handle overvoltages during fault conditions and to guarantee a high reliability of the MV converter.

Selection and Application of the Insulation Material

Although the selection and application of the insulation material is discussed in more detail in **Chapter 5** for the insulation of the MF MV transformer, the main reasons why an advanced insulation material is required for the insulation of L_b and L_g are briefly discussed in the following for a better readability.

Usually, epoxy resins are used for the dry-type insulation of inductors and transformers in power electronic converters. In state-of-the-art MV converters, the typical switching frequencies are in the lower kHz range due to the significant switching losses of MV IGBTs, GTOs or even hard-switched MV SiC devices [190]. However, with the new generation of 10 kV and 15 kV SiC MOSFETs combined with soft-switching techniques, switching frequencies in the range of 75 kHz are possible. Therefore, the dielectric losses $P_\mathrm{ins} \propto E^2 \cdot f_\mathrm{sw} \cdot \tan\delta$ of the insulation material start playing a role [154]. Additionally, the winding losses have to be extracted through the rather thick insulation material layer, which completely surrounds the winding. Consequently, an insulation material with a high thermal conductivity, a low dissipation factor $\tan\delta$, and a high electric breakdown field strength is required. Unfortunately, the thermal conductivity of epoxy resins is rather low. Therefore, a two-component silicone compound (containing thermally conductive particles) of type *TC-4605 HLV* from Dow Corning is used. The properties of this material are listed in **Tab. 5.3**. An additional advantage compared to epoxy resin is the mechanical flexibility of the silicone, which prevents it from cracking during the curing process.

In order to attain a cavity-free insulation, a vacuum pressure potting (VPP) process is applied. Thereby, the devolatilized silicone is pressed into the 3D-printed coil former under vacuum (not lower than 30 mbar in order to not vaporize any ingredients of the silicone). After the coil former is completely filled, the pressure is slowly increased to atmospheric pressure, compressing possible vacuum cavities. In a second step, the silicone has to be cured for several hours with a temperature of 120 °C in order to activate the adhesion to other materials. The best results regarding adhesion are achieved when the temperature is applied directly after the VPP process, although the curing itself does not

require an increased temperature. However, if the temperature is only applied after the curing at room temperature, the silicone might detach from the coil former, leading to vacuum or air cavities between coil former and silicone, which are undesired considering insulation aspects. More details on the VPP process are given in **Section 5.3.4**.

4.3.3 Dimensioning of the Capacitor C_b

The capacitor C_b in series to L_b is needed to block any LF-AC or DC current flowing through the LC-branch. Since for low frequencies C_b is quasi connected in parallel to the grid (the impedance of the inductors is negligible at the mains frequency), C_b leads to an additional reactive power consumption from the AC grid, resulting also in an asymmetric switching frequency pattern, as already mentioned. For this reason, and to minimize the volume of C_b, the capacitance value should be kept small. On the other hand, in order to achieve soft-switching, a certain minimum inductive current through the LC-branch is required. Consequently, the capacitance of C_b has to be selected sufficiently large such that the capacitor voltage ripple stays small, or in other words, the LC-resonance frequency has to be well below the switching frequency

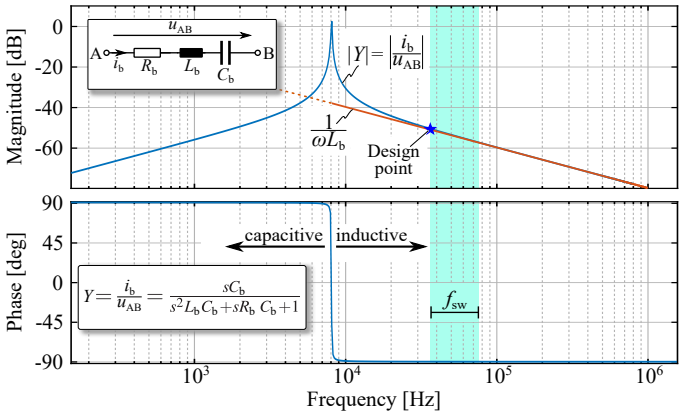

Fig. 4.12: Bode diagram of the transfer function of the LC-circuit. R_b models the series resistance of the inductor L_b. The LC-circuit has to be designed such that the effective switching frequency range is well above the resonance.

range.

Fig. 4.12 shows the Bode diagram of the LCR transfer function

$$Y = \frac{i_\mathrm{b}}{u_\mathrm{AB}} = \frac{sC_\mathrm{b}}{s^2 L_\mathrm{b} C_\mathrm{b} + sR_\mathrm{b} C_\mathrm{b} + 1}\ , \tag{4.17}$$

and the switching frequency range f_sw. It can be seen that a selection of the resonance frequency too close to the minimum effective switching frequency would lead to a deviation from a purely inductive behavior, indicated as $1/\omega L_\mathrm{b}$ in **Fig. 4.12**. This would result in a strong increase of the current amplitude for only small changes in the switching frequency. Therefore, the influence of the capacitor C_b on the maximum current amplitude $\hat{i}_\mathrm{b}$ (at the lowest switching frequency f_min) should be kept small such that $\hat{i}_\mathrm{b}$ is not changed by more than e.g. $d = 15\,\%$ with respect to I_ZVS. This translates into the condition that the relative change in the impedance $|Z|$ caused by C_b should be smaller than $d \cdot \frac{I_\mathrm{ZVS}}{\hat{i}_\mathrm{b}}$ at the lowest switching frequency f_min, i.e.

$$\frac{\omega_\mathrm{min} L_\mathrm{b} - \left(\omega_\mathrm{min} L_\mathrm{b} - \frac{1}{\omega_\mathrm{min} C_\mathrm{b}}\right)}{\omega_\mathrm{min} L_\mathrm{b}} \leq d \cdot \frac{I_\mathrm{ZVS}}{\hat{i}_\mathrm{b}}, \tag{4.18}$$

whereby $\hat{i}_\mathrm{b} = \frac{\hat{u}_\mathrm{g}}{2 f_\mathrm{min} L_\mathrm{b}} \left(1 - \frac{\hat{u}_\mathrm{g}}{U_\mathrm{DC}}\right)$ is the maximum amplidute of i_b and is obtained from (4.5) with $\sin(\omega_\mathrm{g} t) = 1$. The value C_b can now be determined by solving (4.18) for C_b:

$$C_\mathrm{b} \geq \frac{\hat{i}_\mathrm{b}}{4\pi^2 f_\mathrm{min}^2 L_\mathrm{b} I_\mathrm{ZVS} \cdot d}. \tag{4.19}$$

For the converter at hand, the minimum required capacitance is $C_\mathrm{b} \geq 242\,\mathrm{nF}$, while the (HF) rms current flowing through the LC-branch is $i_\mathrm{b,rms} = 5.3\,\mathrm{A}$. Thus, for practical reasons (sufficient current carrying capacity and appropriate voltage rating), a series connection of four 1 µF film capacitors is used, resulting in a total capacitance of $C_\mathrm{b} = 250\,\mathrm{nF}$.

4.3.4 DC-Link

Due to the fact that the system at hand is a single-phase AC/DC converter, the power fluctuation with twice the mains frequency has to be buffered in the DC-link capacitor. Especially for MV applications,

where electrolytic capacitors are not applicable due to their low voltage rating, the DC-link capacitor is one of the physically largest hardware parts. However, to keep the required volume to a minimum and to still attain a highly compact converter, a peak-to-peak DC-link voltage ripple of 10 % is selected, leading to a capacitance of $C_{\mathrm{DC}} = 16.2\,\mu\mathrm{F}$. For the mentioned practical reasons, the DC-link is realized with a series connection of six 100 µF film capacitors, whose voltages are passively balanced with high-ohmic resistors (10 MΩ) in parallel to the capacitor.

4.3.5 Semiconductors

For the design of the *i*TCM converter, it is important to determine the losses of the utilized 10 kV SiC MOSFETs (*Wolfspeed CPM3-10000-0350*). Since there is one HF and one LF bridge-leg, only the HF bridge-leg generates switching losses, while both bridge-legs generate the same conduction losses due to the same rms currents. During full-load operation, the rms current in the MOSFETs is $I_{\mathrm{FET,rms}} = 6.3\,\mathrm{A}$ which leads to $P_{\mathrm{c}} = 79.4\,\mathrm{W}$ of total conduction losses, if an on-state resistance of $R_{\mathrm{DS,on}} = 500\,\mathrm{m\Omega}$ at a junction temperature of 100 °C (datasheet value) is assumed.

In contrast to the conduction losses of the MOSFETs, the SSL have to be determined by measurements, since these values are not available from the datasheet. **Fig. 4.13** (for a better readability taken from

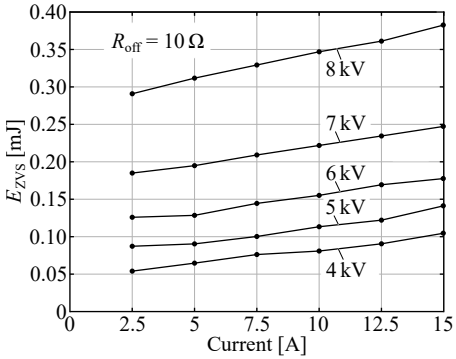

Fig. 4.13: Calorimetrically measured SSL with an external turn-off gate resistor of 10 Ω. Figure taken from **Chapter 3** and shown here for better readability.

Chapter 3 and depicted here again) shows the measured SSL of the utilized 10 kV SiC MOSFETs for different voltages and switched currents. Since the switching frequency f_{sw} and the switched current i_{sw} are varying over time during the grid period according to **Fig. 4.6**, the SSL of the MOSFETs are also time-dependent. The average SSL during the positive half-period can be calculated as

$$P_{\mathrm{sw}} = \frac{2}{T_{\mathrm{g}}} \int_0^{\frac{T_{\mathrm{g}}}{2}} f_{\mathrm{sw}}(t) \cdot E_{\mathrm{ZVS}}\left(i_{\mathrm{sw}}(t)\right) \mathrm{d}t, \tag{4.20}$$

where $T_{\mathrm{g}} = 1/f_{\mathrm{g}}$ is the length of the grid period. Evaluating (4.20) for both MOSFETs S_{11} and S_{12} employed in the HF bridge-leg leads to $P_{\mathrm{sw,S11}} = 13.1\,\mathrm{W}$ and $P_{\mathrm{sw,S12}} = 10.1\,\mathrm{W}$ and results in total switching losses of $P_{\mathrm{sw,tot}} = P_{\mathrm{sw,S11}} + P_{\mathrm{sw,S12}} = 23.2\,\mathrm{W}$.

4.3.6 LCL Input Filter Design

An important requirement of power electronic converters connected to the grid is the compliance with grid harmonic standards in order to guarantee a stable operation of all devices connected to the grid. However, up to now, existing standards such as the IEEE Std 519 [99] or the BDEW guidelines [100] do not cover frequencies higher than 2.5 kHz or 9 kHz, respectively, i.e. there are no official harmonic limits for MV converters with high switching frequencies, since typically LFTs or converters with low switching frequencies are used at MV level. Nevertheless, it is known from literature that voltages with high harmonic content cause dielectric heating and aging of insulation materials or could excite grid resonances [198, 199]. In [200], it is proposed to extend the IEEE 519 harmonic standard to higher frequencies. Hence, the LCL-filter (which is a common filter type in MV applications [58]) of the *i*TCM converter is designed such that the current harmonics stay within the limits defined in [200]. Since the inductance $L_{\mathrm{g}} = 9.55\,\mathrm{mH}$ is already defined by the maximum current ripple (cf. **Section 4.3.2**), the remaining components are L_{f}, C_{f}, and the filter damping resistor R_{d}. Due to the fact that the filter capacitance causes reactive power and results in an asymmetric switching frequency pattern over a grid period (cf. **Fig. 4.6**), a small capacitor value C_{f} is desired. If it is assumed that a reactive power of 5 % due to C_{f} is allowed, its value can be calculated according to [201] and is equal to 274 nF, whereas for practical reasons $C_{\mathrm{f}} = 250\,\mathrm{nF}$ is selected. The value of L_{f} is now

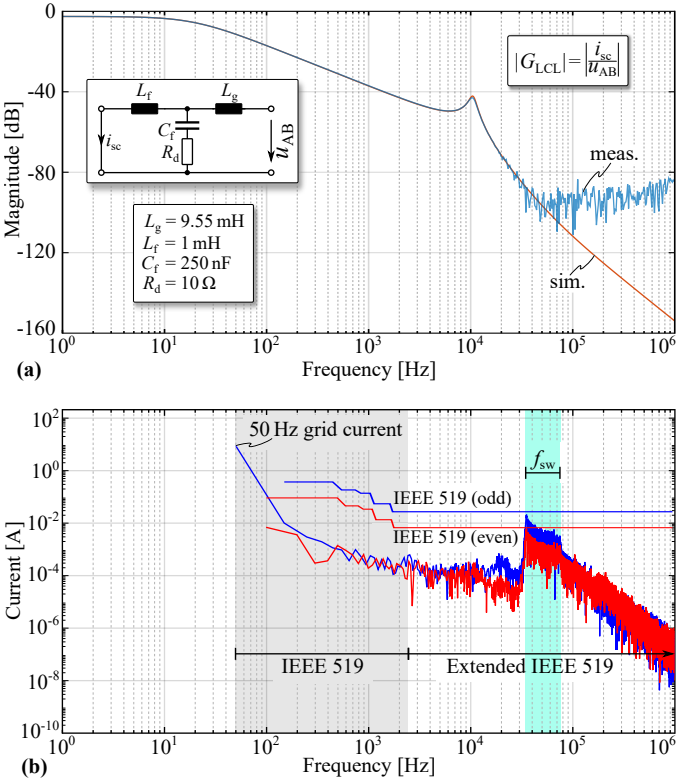

Fig. 4.14: **(a)** Simulated and measured transfer functions of the implemented LCL-filter $|G_{LCL}|$. **(b)** Extended IEEE 519 harmonic standard limits together with the grid-current spectrum of the *i*TCM converter.

varied until the current harmonics comply with the limits of the extended IEEE 519 standard, which results in $L_f = 1\,mH$. Due to the small current ripple, a core material with a high saturation flux density (such as amorphous iron) and a solid wire can be used. Thus, L_f is realized with one Metglas AMCC-4 tape-wound core and 3 layers of 21 turns with 1.2 mm solid copper wire. Since the DM voltage across L_f is below 100 V, L_f is only insulated for the terminal voltage between the winding and the core. Finally, in order to dampen the filter resonance below $-40\,dB$ (cf. **Fig. 4.14(a)**), a damping resistor of $R_d = 10\,\Omega$ is used, leading to $P_{Rd} = 7.35\,W$ of losses caused by the current ripple in

L_g. **Fig. 4.14(a)** shows the simulated and measured transfer function of the LCL-filter $|G_{LCL}|$ with shorted grid-side, i.e. the grid is assumed with zero impedance. As can be seen, the measurement and the simulation match very well apart from the fact that the utilized measurement device *Omicron Lab Bode 100* cannot measure attenuations lower than $\approx -100\,\text{dB}$. Furthermore, **Fig. 4.14(b)** shows the limits for the odd and even harmonics of the extended IEEE 519 standard together with the simulated spectrum of the grid current of the *i*TCM converter. Due to the variable switching frequency, the spectrum does not show the typical discrete harmonics but is rather blurry, while it never exceeds the extended IEEE 519 limits, as desired.

4.3.7 Connection to the MV Grid

Typically, the MV-AC distribution grid in cities is realized with MV-AC cables. From a high-frequency point of view, MV cables can be seen as practically undamped transmission lines [202]. Consequently, the cable itself is an oscillatory system with distinct resonances, depending on the length of the cable. **Fig. 4.15** shows the frequency of the first cable resonance of a 1x400 RM/35, Type *N2XS2Y* 6/10 kV cable [203] with $L' = 290\,\mu\text{H/km}$ and $C' = 550\,\text{nF/km}$. Translated into transmission line parameters, these values result in a characteristic impedance of $Z_c = 23\,\Omega$ and a propagation delay of $t_p = 6.3\,\mu\text{s}$ for an assumed cable length of 500 m. As can be seen in **Fig. 4.15**, there is a critical range of the cable length, such that the first resonance frequency of the cable is located within the switching frequency range of the *i*TCM converter. Although the harmonics of the converter are, due to the LCL-filter, only in the range of 10 mA (cf. **Fig. 4.14(b)**), it has to be ensured that there is no oscillatory interaction of the *i*TCM converter and the MV cable. In case of resonances in the cable, dielectric heating and overvoltages might cause aging and destruction of the cable insulation, as already mentioned.

Fig. 4.16(a) shows the schematic diagram of the LCL-filter and the cable, together with the transfer functions $|G_{Cable}|$ of the cable with a length of 500 m, the LCL-filter $|G_{LCL}|$ (cf. **Fig. 4.14(a)**), and the total transfer function $|G_{tot}| = \left|\frac{i_g}{u_{AB}}\right|$ from the converter voltage to the grid current, while the grid is assumed to be a short circuit. It can be seen that the first cable resonance lies within the switching frequency range of the *i*TCM converter and causes a resonance peak in the total trans-

fer function as well. As a consequence, when the switching frequency approaches the critical range $f_{\text{crit.}}$, undesired oscillations in the grid current can be observed, as shown in **Fig. 4.16(b)**. This behavior can be explained by wave reflections in the cable, since it is not terminated with its characteristic impedance Z_{c} on the input or output side.

The oscillations can e.g. be damped by another LC-filter stage, as described in [204]. However, this does not change the behavior of the cable, but only reduces the excitation, and in case several (different) converters are connected to the same MV cable, interactions between the filter stages might occur. Therefore, to completely circumvent wave reflections and oscillations independently of the cable length and other connected converters, an RC termination network (TN) is added between the LCL-filter and the MV cable, as shown in the schematic in **Fig. 4.17(a)**. Thereby, $C_{\text{t}} = 400\,\text{nF}$ acts as a blocking capacitor for line frequency currents in order to not cause undesired low-frequency losses. If now R_{t} is selected to be equal to Z_{c}, for high frequencies (where C_{t} is a quasi short circuit), the cable is terminated with its characteristic impedance $R_{\text{t}} = Z_{\text{c}}$, which prevents any wave reflections.

As can be seen in **Fig. 4.17(a)**, the transfer function of the cable with the TN is almost flat, i.e. the cable is not interfering anymore with the converter and its LCL-filter, which results in a smooth total transfer function. The grid current waveforms of the *i*TCM converter with

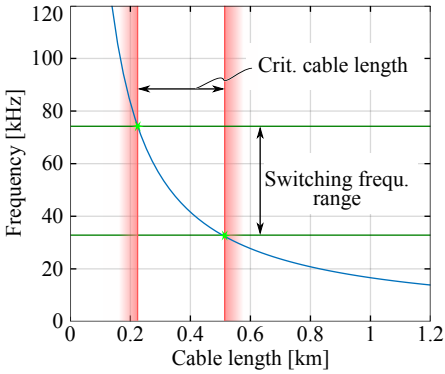

Fig. 4.15: Frequency of the first resonance peak of an MV cable depending on its length together with the switching frequency range of the *i*TCM converter.

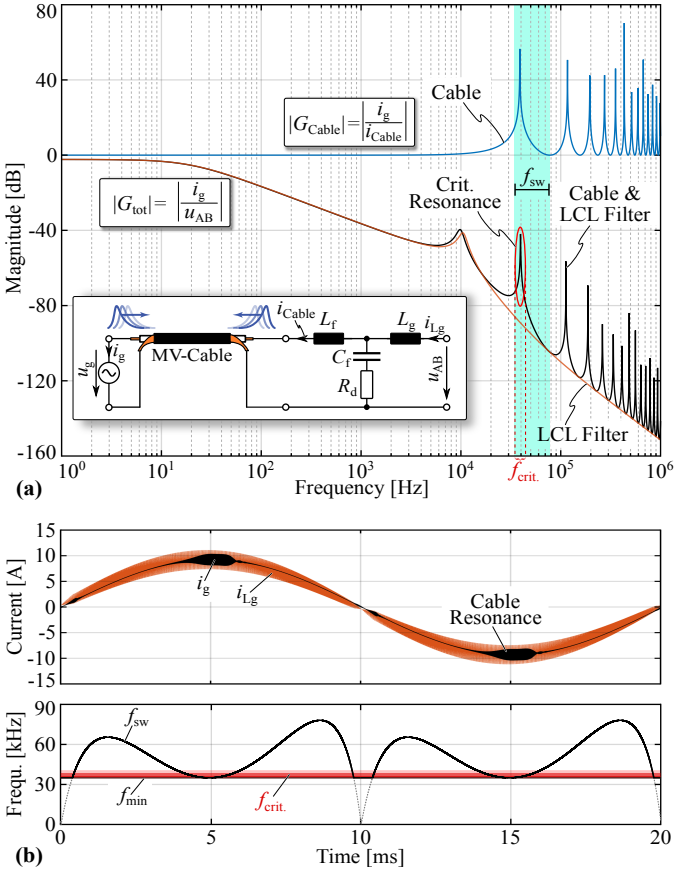

Fig. 4.16: **(a)** Transfer functions of the MV cable, the LCL-filter, and their combination, i.e. the total transfer function from the converter voltage u_{AB} to the grid current i_{g}. The first resonance peak of the cable lies within the switching frequency range of the iTCM converter, leading to oscillations in the grid current i_{g} when the switching frequency approaches the critical range, as can be seen in **(b)**. Cable parameters: $l = 500\,\mathrm{m}$, $L' = 290\,\mu\mathrm{H/km}$, $C' = 550\,\mathrm{nF/km}$.

the TN are shown in **Fig. 4.17(b)** and as expected from the transfer functions, the grid current i_{g} is smooth and free of any oscillations. As already mentioned, due to the additional capacitance C_{t}, the asymme-

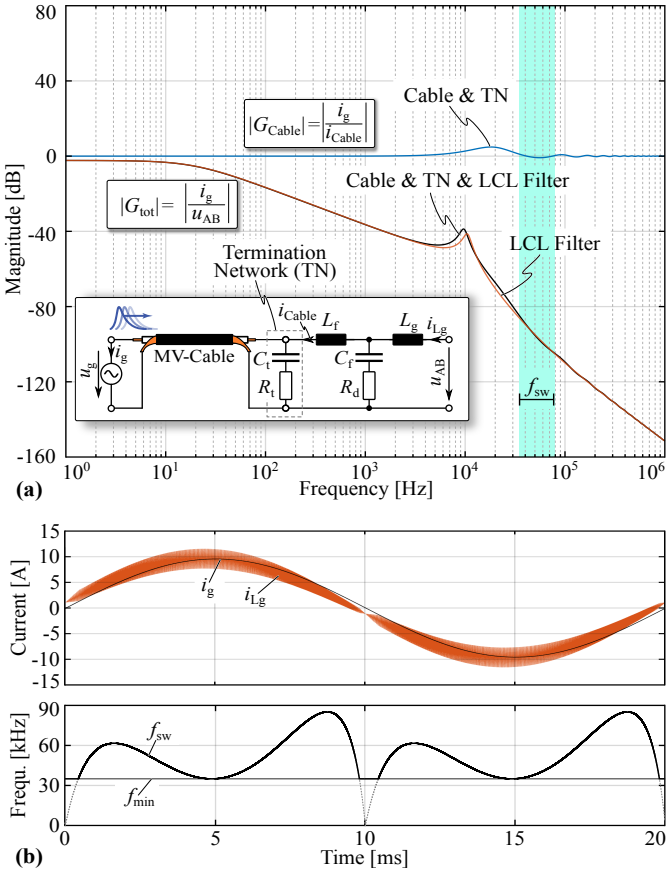

Fig. 4.17: **(a)** Transfer functions of the MV cable, the LCL-filter, and their combination in case a termination network (TN) is added between the LCL-filter and the MV cable. The TN damps the cable resonances. **(d)** The resulting grid current is now very smooth and free of oscillations. Cable parameters as for **Fig. 4.16**.

try in the switching frequency pattern is slightly more pronounced, as can be observed in **Fig. 4.17(b)**. The reader should note that the hardware demonstrated in this thesis does not contain the TN, since this is not necessary in the laboratory where the load is directly connected to the converter without an MV cable.

4.3.8 *i*TCM Hardware Prototype

For the experimental verification of the *i*TCM concept, a hardware prototype has been realized with the goal to achieve a highly compact design, even though large distances for the electrical isolation of the MV are required. These distances can be distinguished into creepage (shortest path between two conductive parts, measured along the surface of the insulation) and clearance distances (shortest distance between two conductive parts, measured through air). According to the IEC 60950-1 International Standard [130], for a sustainable operation, the required creepage distance for 7 kV is $d_{\mathrm{cr}} = 32\,\mathrm{mm}$, and the minimum clearance distance is $d_{\mathrm{cl}} = 17.5\,\mathrm{mm}$. Consequently, during the PCB layout and especially during the 3D CAD design, it has to be ensured that these distances are respected, although a highly compact design is desired.

Fig. 4.18 shows the constructed *i*TCM converter seen from its left side and its right side, respectively. It consists of a top-side PCB, which interconnects the DC-link with the HF bridge-leg, and a bottom-side PCB, which holds the LF bridge-leg as well as the filter capacitors C_{b} and C_{f}, and the inductors L_{b}, L_{g}, and L_{f}. As explained in **Section 4.3.1**, the PCB layouts are optimized for the lowest possible parasitic switch-node capacitance and as can be seen, the high-side gate driver (on 7 kV, 35...75 kHz switched potential) is separated from the low-side gate driver (GND potential) with a creepage slot in the PCB in order to break the creepage path (which increases the breakdown voltage since $d_{\mathrm{cl}} < d_{\mathrm{cr}}$). These creepage slots can also be found on the bottom PCB and in the acrylic glass side walls, which together with the top and bottom PCBs form an air channel for the cooling of the components. The necessary air flow is provided by four 70 mm fans blowing through the heat sinks of the four MOSFETs, from where the air stream continues across the inductors and capacitors, leaving the converter through a perforated acrylic plate. Since the base plates of the 10 kV SiC MOSFETs are on the respective drain potentials, the best solution for the lowest parasitic capacitance (cf. **Section 4.3.1**) is to attach the four heat sinks directly to the MOSFETs' base plates instead of grounding and isolating them with e.g. an aluminum nitride plate. Therefore, the heat sinks are also on the same potential as the drain terminal of the respective MOSFETs and have to be separated from each other and the surrounding parts such as the fans, the DC-link capacitors, and the inductors, as shown in **Fig. 4.18**. Only the heat sinks of the two high-side MOSFETs (visible in the lower picture) are on the same potential

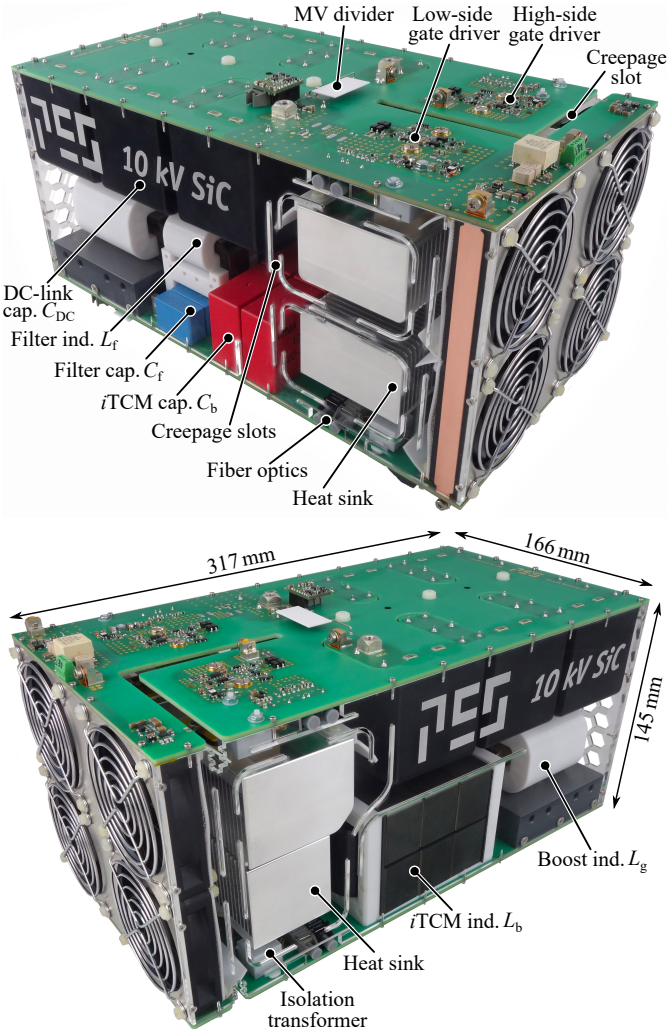

Fig. 4.18: Photos of the realized *i*TCM converter. Despite the large required isolation distances for 7 kV, a highly compact design with a power density of 3.28 kW/L (54 W/in^3) is achieved, whereby all clearance and creepage distances comply with the IEC 60950-1 International Standard [130].

U_{DC} and do not have to be separated from each other. Although the fans are separated from the heat sinks for the aforementioned reason, they are shielded from the HF electric field of the heat sinks with a steel net tied to GND in order not to disturb the fan motor electronics.

Additionally, the *i*TCM converter is equipped with Hall-effect current sensors for the measurement of i_b and i_{Lg}, as well as MV dividers for the measurement of U_{DC} and u_g. The measurement is performed on each gate driver with floating source potential and the measurement signals as well as the gate signals are transferred via optical fibers to a control PCB (with a *Texas Instruments TMS320F28335* DSP). Furthermore, the gate drivers developed in **Chapter 2** are used and feature an ultra-fast OCP, which in case of a fault reacts within 22 ns and turns off all MOSFETs safely. The ultra-compact gate driver auxiliary isolation transformers with an isolation rating of 20 kV enable a highly compact converter design.

Given the fact that the realized converter shown in **Fig. 4.18** is a 7 kV single-phase AC/DC converter, it features an unprecedented power density of 3.28 kW/L (54 W/in^3).

4.4 Experimental Setup

To test the functionality and to measure the efficiency of the realized *i*TCM converter, an appropriate experimental setup is required. Due to the bidirectionality of the converter, the power can basically be supplied either from the AC-side or the DC-side, whereby the efficiency is equal for both directions. Therefore, as shown in **Fig. 4.19**, the *i*TCM converter is supplied from the bidirectional isolated 400 V to 7 kV DC/DC converter treated in **Chapter 5**, which is fed from its

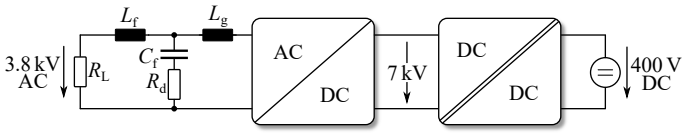

Fig. 4.19: Block diagram showing the experimental setup for the operation of the realized *i*TCM converter. For the laboratory operation, the power is fed into the 400 V DC side of the SST and dissipated in a resistive load R_L on the MV-AC side.

400 V side by two parallel 0...500 V, 0...40 A power supplies (*Regatron TopCon Quadro TC.P.16.500.400.S*). This means that for the testing of the *i*TCM converter, the complete SST (including the isolated DC/DC converter) is in LV-DC to MV-AC operation.

During the tests, the *i*TCM converter is operated in open loop (apart from a feed-forward term to compensate for the DC-link voltage ripple) in order to demonstrate the simplicity of the *i*TCM concept, i.e. no additional control is required. During operation, the currents and the HF switch-node voltage are measured with *Pearson* current transformers and *LeCroy PPE 20 kV* voltage probes, whereby the 50 Hz AC output voltage is measured with a *LeCroy HVD3605* differential voltage probe. To obtain a high measurement quality and accuracy, a *LeCroy HDO4054A* 12-bit oscilloscope is used.

One of the key performance indicators of a power electronic converter is its efficiency, which is especially important in data center applications, where energy losses directly translate into elevated operating costs. For this reason, an accurate measurement of the *i*TCM converter efficiency is essential. In the following, it is shown that an electrical efficiency measurement achieves only a low and insufficient accuracy. Thus, a calorimetric measurement of the loss components with a much higher accuracy is presented and applied to the converter at hand.

4.4.1 Electrical Efficiency Measurement Error Analysis

Typically, converter efficiencies are measured electrically by measuring the input and the output power: $\eta = \frac{P_{\text{out}}}{P_{\text{in}}}$. However, for an expected efficiency of $\eta_{\text{exp}} = 99\,\%$, already very small errors e_{p} in the input and output power measurements cause significant errors in the measured efficiency value η_{meas}. If an efficiency measurement error of $e_{\text{eff}} \leq 0.1\,\%$ is desired (i.e. for a converter efficiency of 99 %, the measured efficiency should be in the range of $98.9\,\% \ldots 99.1\,\%$), the input and output powers have to be measured with an accuracy of $e_{\text{p}} = 0.05\,\%$ each [205], as can be calculated with (4.21) and is illustrated in **Fig. 4.20 (a)**,

$$e_{\text{P}} = \frac{e_{\text{eff}}}{2 \cdot \eta_{\text{exp}} + e_{\text{eff}}} \approx \frac{e_{\text{eff}}}{2}. \tag{4.21}$$

Even a high precision power analyzer, such as the *Yokogawa WT3000*, is unable to reach this accuracy. According to the datasheet, the error

of the power analyzer is $e_{\mathrm{Y,DC}} = 0.05\,\%$ of the reading Y plus $e_{\mathrm{X,DC}} = 0.1\,\%$ of the power range X (voltage range multiplied by the current range) for DC power measurements and $e_{\mathrm{Y,AC}} = 0.02\,\%$ of the reading plus $e_{\mathrm{X,AC}} = 0.04\,\%$ of the power range for AC power measurements. However, the voltages would have to be divided by e.g. a $div = 1 : 100$ voltage divider, which is accounted with an error of $e_{\mathrm{div}} = 0.1\,\%$. Furthermore, on the AC-side, since both AC terminals are on potential, a differential voltage measurement is required, leading to an error of already $2 \cdot e_{\mathrm{div}} = 0.2\,\%$. In addition, for the same reason, the AC current would have to be measured with a current transformer which provides galvanic isolation and is accounted with $e_{\mathrm{CT}} = 0.1\,\%$. On both sides, the voltage range must be set to $X_{\mathrm{U}} = 100\,\mathrm{V}$ (due to the voltage division by a factor of 100). For the DC-side, a current range of $X_{\mathrm{I,DC}} = 5\,\mathrm{A}$ is sufficient, while the AC current has to be measured with a range of $X_{\mathrm{I,AC}} = 10\,\mathrm{A}$. These values lead to the following AC and DC power measurement errors:

$$\begin{aligned} P_{\mathrm{DC,m}} &= (U_{\mathrm{DC}} \cdot div \cdot (1 \pm e_{\mathrm{div}}) \cdot I_{\mathrm{DC}}) \\ &\quad \cdot (1 \pm e_{\mathrm{Y,DC}}) + X_{\mathrm{U}} \cdot X_{\mathrm{I,DC}} \cdot e_{\mathrm{X,DC}} \qquad (4.22) \\ e_{\mathrm{DC,m}} &= 1 - \left(\frac{P_{\mathrm{DC,m}}}{div \cdot P_{\mathrm{DC}}} \right) = \pm 0.35\,\% \qquad (4.23) \\ P_{\mathrm{AC,m}} &= (U_{\mathrm{AC}} \cdot div \cdot (1 \pm 2e_{\mathrm{div}}) \cdot I_{\mathrm{AC}} \cdot (1 \pm e_{\mathrm{CT}})) \\ &\quad \cdot (1 \pm e_{\mathrm{Y,AC}}) + X_{\mathrm{U}} \cdot X_{\mathrm{I,AC}} \cdot e_{\mathrm{X,AC}} \qquad (4.24) \\ e_{\mathrm{AC,m}} &= 1 - \left(\frac{P_{\mathrm{AC,m}}}{div \cdot P_{\mathrm{AC}}} \right) = \pm 0.48\,\%. \qquad (4.25) \end{aligned}$$

Thus, the total worst case efficiency measurement error is

$$\pm \left(|e_{\mathrm{DC,m}}| + |e_{\mathrm{AC,m}}| \right) = \pm 0.83\,\%, \qquad (4.26)$$

which for a 99 % efficient converter would lead to a measured efficiency in the range of $98.17 \ldots 99.83\,\%$. Even without the errors caused by the MV dividers and the current transformer (e.g. for a 99 % efficient 400 V system), the measurement error (only caused by the power analyzer) is $\pm 0.43\,\%$, which is totally unacceptable.

4.4.2 Calorimetric Efficiency Measurement

Due to the large measurement errors in case of an electrical efficiency measurement, a more accurate measurement method is required. Instead of measuring the input and output powers and relating them to

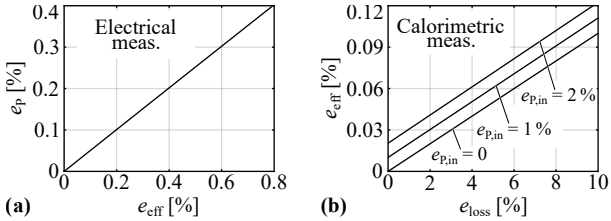

Fig. 4.20: **(a)** Allowed power measurement error e_P as a function of the desired efficiency measurement error e_eff in case of an electrical efficiency measurement. **(b)** Achieved efficiency measurement error e_eff as a function of the converter loss measurement error e_loss for different input power measurement errors $e_\mathrm{P,in}$ in case of a calorimetric efficiency measurement.

each other, the converter losses can be measured directly in a calorimetric manner, leading to a much higher accuracy. The efficiency can then be calculated by only measuring the DC input power electrically and deducing the output power from the electrical input power and the calorimetrically measured losses. **Fig. 4.20(b)** shows the achieved efficiency measurement error e_eff depending on the error of the converter loss measurement e_loss for different errors $e_\mathrm{P,in}$ in the electrical DC input power measurement. If the DC input power can be measured with an error of $e_\mathrm{P,in} = 1\,\%$, the losses of the converter need to be measured with an accuracy of $e_\mathrm{loss} = 10\,\%$ in order to achieve an efficiency error of $e_\mathrm{eff} = 0.1\,\%$.

Typically, for the calorimetric measurement of the converter losses, the converter could e.g. be operated inside a calorimeter, which measures the dissipated heat. However, the time constant of such a calorimeter to reach steady-state is in the range of several hours. Moreover, only the total converter losses can be measured and no information about the loss distribution can be given. To measure also the loss distribution among the components in an even shorter measurement time, the losses of the MOSFETs and the inductors are measured separately with calorimetric methods, as shown in **Figs. 4.21 & 4.22** and explained in the following sections. The remaining loss components, such as the auxiliary power for the gate drives, the DSP, the fans, and the filter damping resistor R_d can be measured electrically. Furthermore, the losses of the grid-side filter inductor L_f are very small and are taken from the inductor simulations, since even a large error on these small losses would not influence the accuracy of the total loss measurement

significantly. For the capacitors, it can be calculated from the dissipation factor that the losses are smaller than 1 W, and hence these losses are neglected.

Calorimetric Inductor Loss Measurement

In order to measure not only the converter efficiency, but also the loss distribution among the individual components (whereby the inductors L_b and L_g, as well as the MOSFETs are the main contributors), the inductors L_b and L_g were separated from the converter setup shown in **Fig. 4.18** and are operated outside the converter to measure the pure inductor losses. The measurement of inductor losses under real operating conditions is a difficult task, especially when a high accuracy is desired. Therefore, several calorimetric measurement methods have been developed in literature [28, 206, 207]. Thereby, steady-state measurement methods [28, 197] and transient measurement methods [206] are used. For the sake of a short measurement time, a transient measurement method is preferred in order not to dissipate the system power of 25 kW into the laboratory for several hours. Therefore, the inductors L_b and L_g are externally placed in separate oil calorimeters, i.e. thermally insulated oil tanks equipped with a stirrer (to ensure a homogeneous temperature in the oil) and an NTC temperature sensor. **Fig. 4.21(a)** gives an insight into the oil calorimeter. The silicone oil (*Bluesil Fluid 604V50* usually used for transformer insulation) fulfills two tasks in the calorimeter: On the one hand, it extracts the losses out of the core and the winding such that the inductor and the oil are at the same temperature, and on the other hand it provides electrical insulation. Due to the thermal insulation of the oil calorimeter towards the ambient, adiabatic conditions can be assumed. From calibration measurements with constant DC power injection into the inductor winding, the thermal capacitance C_Th of the calorimeter can be determined. Finally, for the measurement of the inductor losses, the oil temperature is measured during the operation of the *i*TCM converter, as shown in **Fig. 4.21(b)**. As can be seen, after a certain settling time (converter operation starts at time = 300 s), a linear temperature profile can be observed, as expected for constant inductor losses and a constant thermal capacitance C_Th. The total inductor losses can thus be determined as

$$P_\mathrm{ind} = C_\mathrm{Th} \cdot \frac{\Delta\vartheta}{\Delta\tau}. \tag{4.27}$$

As can be seen in **Fig. 4.21(b)**, the temperature slightly increases before the converter operation is started. This can be explained by the losses of the stirrer motor (6.77 W in the L_b calorimeter and 7.53 W in the L_g calorimeter) which are measured electrically and are subtracted from the calorimetrically measured losses in order to obtain the pure inductor losses.

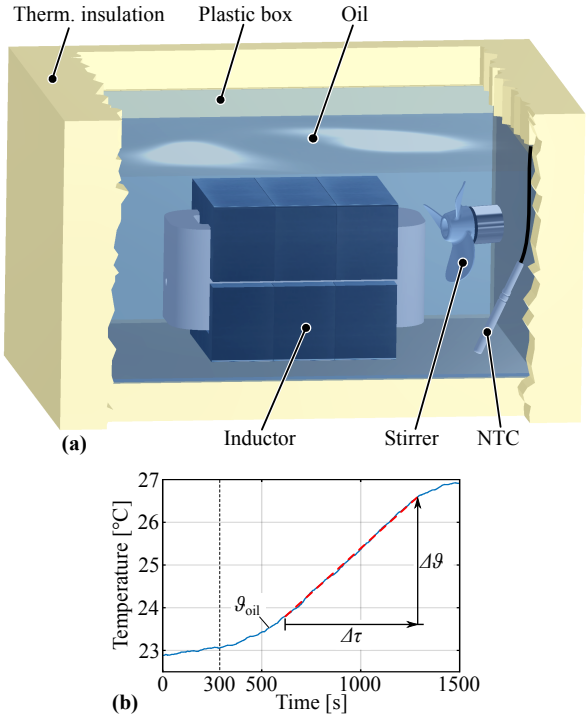

Fig. 4.21: **(a)** Calorimetric measurement setup for the determination of the losses of the MV inductors L_b and L_g. The inductors are placed in oil-filled and thermally insulated boxes and dissipate their losses into the homogeneously mixed oil whose temperature is measured via NTCs. **(b)** Measured temperature profile of the oil during full-power operation of the iTCM converter for the determination of the losses of inductor L_b. The losses are determined from the temperature rise $\Delta\vartheta/\Delta\tau$ in combination with the thermal capacitance of the entire calorimeter known from calibration measurements with constant power.

With a temperature measurement resolution of $e_{\mathrm{NTC}} = 0.1\,\mathrm{K}$ (mainly limited by EMI noise during converter operation) and a temperature difference of $\Delta\vartheta = 2.8\,\mathrm{K}$ (cf. **Fig. 4.21(b)**), the measurement error is 7.1 %, if a perfect time measurement is assumed. During the calibration with DC, no EMI noise is present and the resolution of the temperature measurement is 0.05 K. Therefore, the error in the measurement of the thermal capacitance C_{Th} is 3.5 % which leads to a total worst case measurement error of $e_{\mathrm{oil}} = 10.6\,\%$ for the oil calorimeters. The conducted experiments show that the difference between the highest and the lowest measured losses of L_{b} (which are independent of the processed power, cf. **Fig. 4.28**) diverge by 6.75 %. This value matches well with the predicted 7.1 % from above.

Calorimetric Semiconductor Loss Measurement

The loss measurement of the utilized 10 kV SiC MOSFETs has been extensively described in **Chapter 3**, where brass blocks have been used as adiabatic heat sinks with a defined thermal capacitance in order to

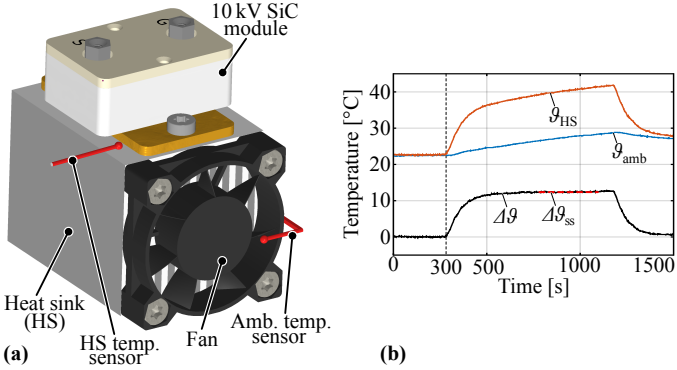

Fig. 4.22: **(a)** Calorimetric setup for the measurement of the semiconductor losses. Each of the four utilized 10 kV SiC MOSFET modules is mounted on a separate heat sink whose temperature is measured via a fiber-optic temperature measurement system (*Optocon FOTEMPMK-19"*). **(b)** Measured temperature profiles during 25 kW operation of the converter. With the measured temperature difference $\Delta\vartheta$ and the thermal resistance $R_{\mathrm{Th,HS}}$ of the heat sink (known from calibration measurements with constant power), the losses of the 10 kV SiC module can be determined.

measure the transient temperature response for the loss determination, similar to the oil calorimeter described above. However, the MOSFETs are now placed on separate and actively cooled heat sinks, as can be seen in **Fig. 4.18**. The thermal system is thus dominated by the convective cooling instead of the thermal capacitance of the heat sinks. Furthermore, the thermal time constant of the heat sinks together with the 10 kV MOSFETs is in the range of only 100 s, i.e. the time for the heat sinks to reach steady-state is approximately 10 min. For these reasons, the semiconductor losses are measured via the steady-state temperature difference $\Delta\vartheta_{\mathrm{ss}}$ between the heat sink and the ambient. **Fig. 4.22(a)** shows the basic setup with a single 10 kV module mounted on a heat sink which is actively cooled by the air flow of a fan. As already mentioned, the heat sinks in the constructed *i*TCM converter (cf. **Fig. 4.18**) are on the respective drain potential, which is why the fans are separated from the heat sink in reality. However, for the explanation of the loss measurement concept, this is not shown in the schematic drawing in **Fig. 4.22(a)**. The (switched) potentials on the heat sinks imply that the heat sink temperature measurement sensors must be galvanically isolated. Hence, a fiber optic temperature measurement system (*Optocon FOTEMPMK-19"*), which measures the temperature at the tip of up to 10 non-conductive optical fibers, is used. As shown in **Fig. 4.22(a)**, one optical fiber is placed on the heat sink and one in front of the fan for the measurement of the air temperature. The thermal resistances $R_{\mathrm{Th,HS}}$ of the four heat sinks are measured separately by injecting a constant DC-power into each MOSFET and measuring the difference between the temperature of the respective heat sink and the air temperature in front of the associated fan. Thereby, the system must be in exactly the same conditions as in case of the converter operation (e.g. the fan voltage must be kept constant and the geometry must not be changed, i.e. the side walls must remain closed and the temperature sensor position must not change). This ensures that the measured thermal resistances of the heat sinks are exactly the same during the calibration and the efficiency measurements. The reader should note that the cross-coupling between the different heat sinks has been analyzed and can be neglected.

Fig. 4.22(b) shows the measured ambient and heat sink temperature profiles ϑ_{amb} and ϑ_{HS} together with the temperature difference $\Delta\vartheta$ during the converter operation at 25 kW. The converter operation is started at time = 300 s, as can be seen from the temperature increase.

Due to the fact that the converted power is dissipated in the laboratory, the room temperature also rises slowly. However, the time constant of the heat sink is much shorter than the time constant of the room, which can be seen at time = 1200 s where the converter is turned off and the heat sink temperature decreases much faster than the ambient temperature. For this reason, the temperature difference $\Delta\vartheta$ between the heat sink and the ambient reaches a steady-state value $\Delta\vartheta_{\mathrm{ss}}$, and the losses of the semiconductor modules can be determined as

$$P_{\mathrm{semi}} = \frac{\Delta\vartheta_{\mathrm{ss}}}{R_{\mathrm{Th,HS}}}. \tag{4.28}$$

For a resolution of 0.2 K of the fiber optic temperature measurement and a steady-state temperature difference of $\Delta\vartheta_{\mathrm{ss}} = 12.4\,\mathrm{K}$, the measurement error is 3.2 %. Together with an assumed deviation of the thermal resistance of 5 %, the maximum expected error (for this operating point) is $e_{\mathrm{HS}} = 8.2\,\%$.

Calorimetric Efficiency Measurement Accuracy

In order to determine the total accuracy of the applied efficiency measurement, the errors of the individual measurement methods are weighted with the respective measured losses and are summed up to calculate the worst case error. If the following errors are assumed for the losses (L_{F}: 15 % since the losses are calculated; R_{d}: 10 % due to 5 % error of the current measurement and $R_{\mathrm{d}} \cdot I^2$; Auxiliary: 0.5 % due to low voltage, low current DC power measurement with multimeters), the total weighted loss measurement accuracy is 9 %. Combined with a converter DC input power measurement error of 2 % due to the measurement of the MV DC-link voltage, a total efficiency measurement error of 0.11 % is obtained from **Fig. 4.20(b)**.

4.5 SST Laboratory Setup

Fig. 4.23 shows the SST laboratory setup, which has been used to test the functionality of the SST and to measure its efficiency. The *i*TCM converter can be seen on the right side together with the oil calorimeters in the center to measure the losses of the inductors L_{g} and L_{b}. As indicated in **Fig. 4.19**, to test the *i*TCM converter, the SST system is transferring power from the LV-DC bus to the MV-AC

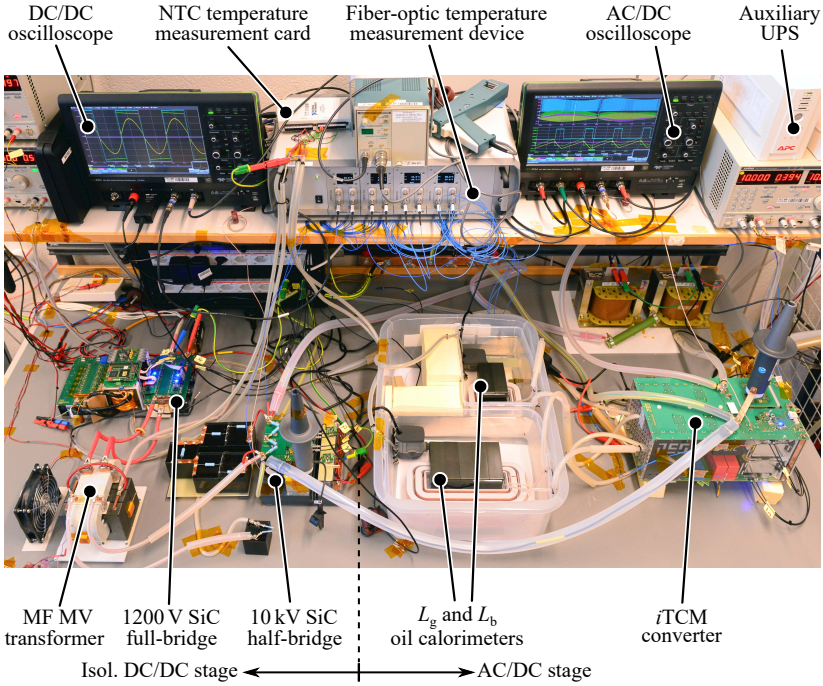

Fig. 4.23: Photograph of the 3.8 kV AC to 400 V DC SST laboratory setup with the isolated DC/DC converter on the left and the *i*TCM AC/DC converter on the right. The setup is located inside an MV cage for safety reasons and the communication between the control unit and the converters as well as the communication to the measurement devices is entirely via optical fibers.

side. The isolated DC/DC converter (cf. **Chapter 5**) on the left side provides the 7 kV DC-link voltage from the 400 V DC bus.

For safety reasons, the SST setup is located inside an MV cage without any galvanic connections between the SST and the outside of the cage, i.e. the gate signals and the fault signals of the converters as well as the communication between the PC (outside of the cage) and the measurement equipment is provided via optical fibers. Furthermore, all cables on MV potential are covered by silicone tubes to provide electrical insulation from other parts of the SST.

To guarantee a safe system shutdown in case of a power outage in the laboratory e.g. due to external factors such as other persons in the

laboratory pressing the emergency stop button, which would cut off the power, the auxiliary supplies for the gate drivers and the DSP/FPGA control unit are backed up with a UPS.

In operation, the voltage and current waveforms of the DC/DC stage and the *i*TCM AC/DC stage are monitored with separate oscilloscopes in order to have a sufficient amount of channels. Furthermore, the temperatures of the floating heat sinks and the oil inside the oil calorimeters are measured with a fiber-optic temperature measurement device and NTCs (cf. **Fig. 4.23**) for the determination of the losses of the semiconductors and the magnetic components. For the determination of the losses of the LV-side 1200 V SiC full-bridge, its heat sink temperature is measured with high-precision NTC thermistors and an analog to digital measurement card.

Since the transferred power of the SST is dissipated in a resistive load, which is also located inside the cage for safety reasons, large fans provide an airflow through to the load resistors away from the SST system in order to mitigate the temperature rise in proximity of the SST and hence to minimize the impact on the calorimetric efficiency measurements.

4.6 Experimental Results

In order to verify the proper operation of the *i*TCM converter and to determine its performance, the converter has been operated at different power levels, while the current and voltage waveforms and the efficiency have been measured. For the *i*TCM converter at hand, it is especially interesting to see whether or not soft-switching is achieved over the whole grid period in open loop operation.

4.6.1 Measured Waveforms

Fig. 4.24 shows the measured waveforms of the switch-node voltage u_{SN} of the HF bridge-leg together with the AC output voltage u_{g}, the currents i_{b}, i_{Lg}, i_{g}, and the current i_{A} flowing out of the HF switch-node A (cf. **Fig. 4.4(a)**) during full-power (25 kW) operation. As can be seen, the AC output voltage u_{g} and the AC output current i_{g} are nicely sinusoidal and in phase to each other, as desired. Furthermore, it can be observed in the envelope of i_{A}, that the switched current is almost constant at $\approx -4.5\,\mathrm{A}$ during the positive, and $\approx +4.5\,\mathrm{A}$ during

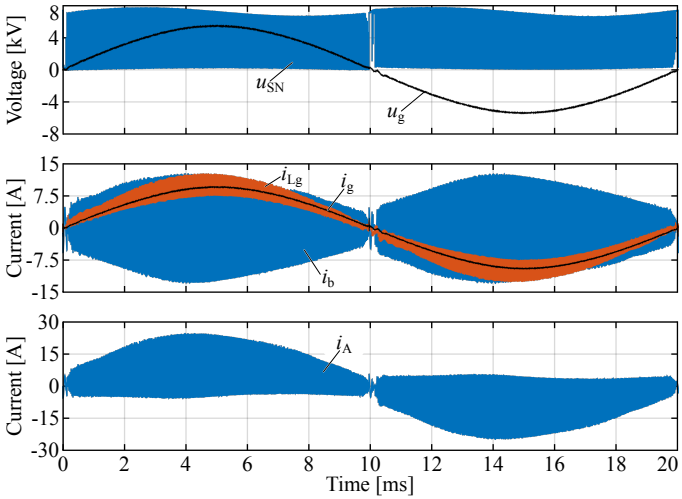

Fig. 4.24: Measured current and voltage waveforms over a full grid period during full-power (25 kW) operation of the *i*TCM converter. A smooth sinusoidal output voltage and current is achieved, while the MOSFETs are soft-switching over the full grid period, as can be seen from the current i_A flowing out of bridge-leg A and showing an almost constant turn-off value of $I_{ZVS} = 4.5\,A$.

the negative half period of the grid voltage, respectively. This means that soft-switching is achieved over the whole grid period and proves that the *i*TCM concept is working nicely, even without any feedback control.

For a better insight into the waveforms, the two most interesting points, namely the region around the peak and the zero crossing of the grid voltage, are shown in more detail in the following. The measured waveforms around the peak of the grid voltage are plotted in **Fig. 4.25**. It can be observed that the waveforms are very smooth and symmetric, which is a result of a careful design of the converter (i.e. low commutation loop inductance in the HF path and low parasitic capacitances of the inductors). Furthermore, the ZVS current $-I_{ZVS} = -4.5\,A$ proves that the converter is operated under soft-switching conditions.

The second interesting point within the grid period is the zero crossing of the grid voltage, where the LF bridge-leg commutates and the duty cycle of the HF bridge-leg changes abruptly from 1 to 0, as shown

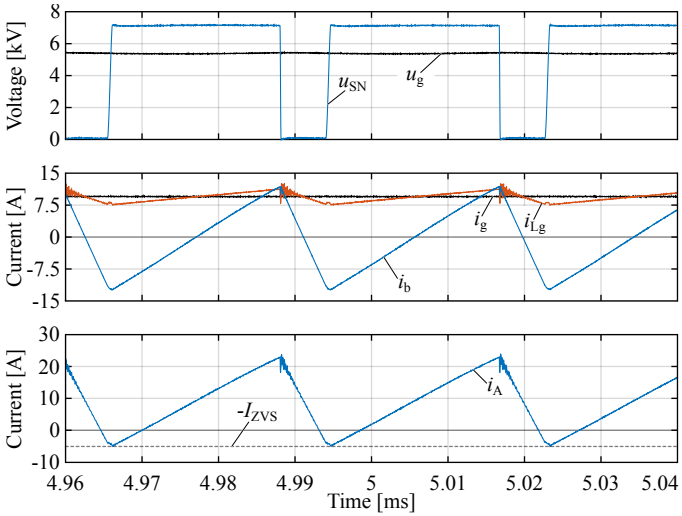

Fig. 4.25: Measured current and voltage waveforms at the peak of the grid voltage at full-power (25 kW) operation of the iTCM converter. It can be seen that both, the rising and the falling voltage transitions are soft-switched. Furthermore, the current i_A reaches a value of $-I_{ZVS} = -4.5\,A$ to guarantee soft-switching.

in **Fig. 4.26**. Thereby, it is of high importance that the commutation of the HF and the LF bridge-legs are synchronized precisely in order to avoid undesired current spikes. However, due to the different switching speeds of the HF and LF bridge-legs (the LF bridge-leg is hard-switched with a rather high gate resistance of 47 Ω in order to achieve smooth transitions), a negative current builds up in L_b, followed by an oscillation between L_b and C_b for approx. 100 ns until the HF bridge-leg starts switching again. Nevertheless, the amplitude of this oscillation is small and the grid current is not affected. As can be seen in the current i_A, apart from the ZCS transition at the time instant $t = 0\,ms$, all other switching transitions are soft-switched.

4.6.2 Efficiency Measurements

As already mentioned, the efficiency of power electronic converters operated in data centers or battery charging applications is of high im-

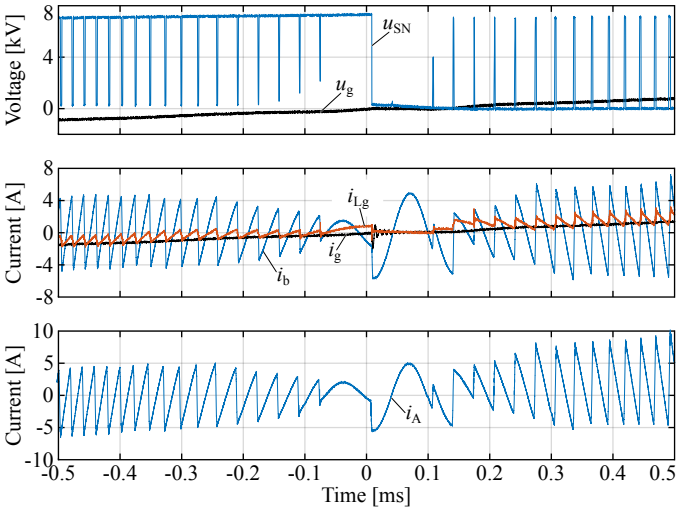

Fig. 4.26: Measured current and voltage waveforms during the zero crossing of the grid voltage at full-power (25 kW) operation of the *i*TCM converter. Both duty cycles of the HF and the LF bridge-legs are changing from 1 to 0, i.e. the local average value of the switch-node voltages change from 7 kV to 0 V. Except for the switching transition at $t = 0$ ms, all other switching transitions are soft-switched as can be seen from the current i_A.

portance due to environmental and economical aspects and it is desired that the efficiency is high for a wide power range. **Fig. 4.27** shows the calorimetrically measured efficiency curve of the *i*TCM AC/DC converter, whereby the applied calorimetric loss measurement methods have been explained in detail in **Section 4.4.2**. As can be seen, the efficiency increases with increasing power, reaching a peak efficiency of 99.1 % at full load. At 50 % load, the efficiency is still 98.8 %, making the converter also suitable for partial load operation. Comparing these values to existing 10 kV or 15 kV SiC MOSFET-based topologies [104, 109, 110, 190, 191], a significantly higher efficiency and switching frequency and thus power density is achieved by the *i*TCM converter due to ZVS.

Finally, in **Fig. 4.28** the loss distribution among the different components is shown, whereby the losses of the inductive components and the semiconductor devices have been measured calorimetrically (cf. **Section 4.4.2**), while the auxiliary and fan powers were measured electri-

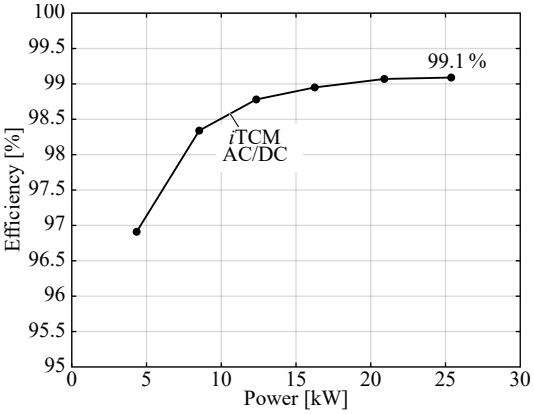

Fig. 4.27: Calorimetrically measured efficiency of the realized *i*TCM converter. A peak efficiency of 99.1 % is achieved at full load. Furthermore, also a high partial load efficiency is achieved, which makes the converter suitable for applications where it is operated under partial load conditions. The efficiency of the total SST (including the isolated DC/DC converter) is shown in **Chapter 6**.

cally and the comparably small losses of the filter inductor L_f are taken from the inductor optimization. It can be observed that (besides the constant filter damping and auxiliary losses, which include the control board and the gate drivers etc.) the losses of L_b are constant, as expected. Furthermore, at full power, the difference between the losses of the HF MOSFETs (S_{11} and S_{12}) and the LF MOSFETs (S_{21} and S_{22}), i.e. the switching losses, is 27.3 W. This is in good agreement with the 23.2 W of switching losses calculated in **Section 4.3.5** (especially considering that the HF and LF bridge losses also include conduction losses of MOSFETs with strong variations in $R_{\mathrm{DS,on}}$ from device to device). According to the calculation in **Section 4.3.5**, the total conduction losses should sum up to 79.4 W, whereby the measured conduction losses (twice the LF bridge losses) are 87.4 W. Given the fact that not all MOSFETs are on the same junction temperature, the error of 9 % between measurement and calculation is acceptable. Furthermore, for the inductor L_b, a good agreement of the measured losses (29 W in average) and the calculated losses (32.4 W, cf. **Fig. 4.9(a)**) can be noted. For L_g, the difference between the measured losses (57 W) and the calculated losses (48 W, cf. **Fig. 4.9(b)**) is slightly higher but within 16 %

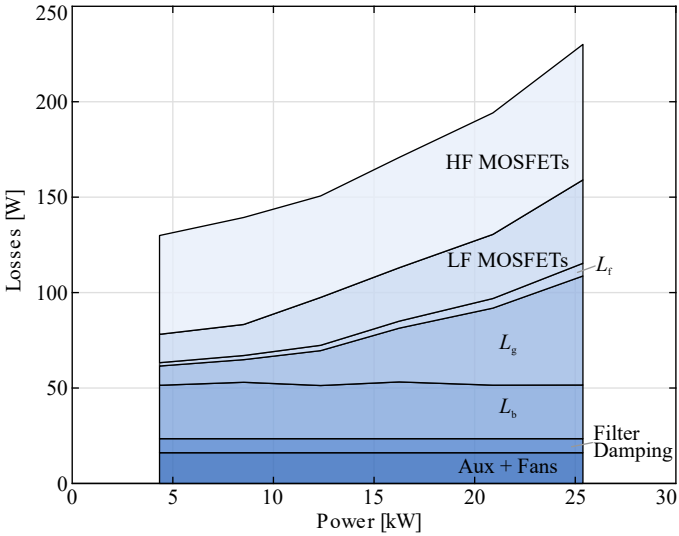

Fig. 4.28: Measured loss distribution of the *i*TCM converter in dependency of the processed power.

which is still very accurate, given that the parameter uncertainties of e.g. the core material are already in this range [208].

4.7 Summary

In this chapter, a bidirectional 25 kW, 3.8 kV AC rms to 7 kV DC PFC AC/DC converter based on the the *integrated* Triangular Current Mode (*i*TCM) concept has been developed. The *i*TCM concept is a simple method to achieve soft-switching over the entire AC grid period by adding an LC-circuit to the well-known full-bridge PWM AC/DC converter. It is demonstrated that a constant ZVS current and therewith soft-switching over the whole grid period can be achieved even in open loop operation, i.e. no current zero crossing detection, as in case of using the TCM approach, is required.

With the help of a characteristic impedance definition, the impact of parasitic inductances and capacitances on the design of MV converters is analyzed and compared to the impact on LV converters. Thereby, an elementary difference can be observed, namely that parasitic induc-

tances play a minor role for MV converters, whereas it is very important to minimize parasitic capacitances. Therefore, e.g. coplanar PCB layouts should be avoided in MV applications and the tracks should be separated as far as possible from each other to minimize parasitic capacitances.

The design of all main power components of the converter is presented, whereby the focus is set on the low-capacitive design of the MV inductors and their electrical insulation. Pareto-optimizations show that a 40 % peak-to-peak current ripple in the boost inductor is a reasonable trade-off ensuring high efficiency and high power density and requiring only moderate input filter effort. Different winding arrangements are analyzed to minimize the electric field stress and the parasitic capacitances of the inductors. Furthermore, the selection of the insulation material and the vacuum pressure potting of the windings is described.

For a proper integration of the SST into the MV-AC grid, an LCL-filter is designed in order to comply with the extrapolated IEEE 519 harmonic standard and the connection of the converter to an MV cable is analyzed. It is shown that, without further measures, oscillations due to cable resonances, which are excited by the remaining converter harmonics, would occur. These oscillations can be avoided by adding a simple RC termination network between the LCL-filter and the MV cable.

Furthermore, the performed efficiency measurement error analysis shows that electrical efficiency measurements are not suited for converter efficiencies $\geq 99\,\%$, whereas calorimetric efficiency measurement methods show much higher accuracies. Therefore, calorimetric methods for the measurement of the converter loss distribution and the efficiency are presented. The measured full-load efficiency of the realized *i*TCM converter reaches a value of 99.1 %, which in combination with a power density of $3.28\,\mathrm{kW/L}$ ($54\,\mathrm{W/in^3}$) demonstrates an unprecedented performance for an MV PFC single-phase AC/DC converter.

5

10 kV SiC-Based Isolated Bidirectional 7 kV/400 V DC/DC Converter

The power supply chain of data centers from the MV-AC utility grid down to the chip level voltage consists of many series connected power conversion stages and accordingly shows a relatively low efficiency. SSTs could improve the efficiency by substantially reducing the number of power conversion stages and/or directly interfacing the MV-AC grid to a 400 V DC bus, from where server racks with a power consumption of several tens of kilowatts could be supplied. The recent development of SiC MOSFETs with a blocking voltage of 10 kV enables the realization of a simple and hence highly reliable two-stage SST topology, consisting of an AC/DC PFC rectifier and a subsequent isolated DC/DC converter. In this context, an isolated 25 kW, 48 kHz, 7 kV to 400 V series resonant DC/DC converter based on 10 kV SiC MOSFETs is realized and tested. To achieve ZVS for all MOSFETs, a special modulation scheme to actively control the amount of the switched magnetizing current on the MV-side and the LV-side is implemented. Furthermore, the design of all main components and especially the electrical insulation of the employed MF MV transformer is discussed in detail. Calorimetric efficiency measurements show that the realized isolated DC/DC converter achieves a full-load efficiency of 99.0 %, while it features a power density of 3.8 kW/L (63 W/in^3).

5.1 Introduction

SST technology is considered as a highly interesting concept to increase the efficiency of the power supply chain from the MV-AC utility grid down to the chip voltage level in data centers by directly interfacing the MV-AC grid to a 400 V DC power distribution bus [33, 41, 42, 116]. Thereby, the number of cascaded conversion stages is substantially reduced, resulting in a lower complexity, higher reliability, higher power density, and higher efficiency of data center power supplies.

Up to the present, voltages in the 10 kV-range had to be interfaced by multi-cell converters based on ISOP-connected modules rated for a fraction of the total MV-side voltage, where each module is comprising an AC/DC [82, 92, 119, 209, 210] and an isolated DC/DC converter [30, 211, 212]. However, the recent development of 10 ... 15 kV SiC MOSFETs with outstanding switching behavior [122, 124, 190, 213] enables the construction of single-cell SSTs avoiding the series connection of several modules, and therefore resulting in a simple and reliable converter structure. Due to the reduced complexity, also a higher power density can be expected. Therefore, a 10 kV SiC MOSFET-based single-cell two-stage 25 kW, 3.8 kV single-phase AC to 400 V DC SST (cf. **Fig. 5.1**) is implemented, whereby this chapter provides a detailed analysis and experimental verification of the isolated 7 kV to 400 V DC/DC converter stage.

The efficiency goal of the SST has been set to $\eta_{\mathrm{t,SST}} = 98\,\%$. Since the *i*TCM AC/DC front end converter (cf. **Chapter 4**) achieves an efficiency of 99.1 %, the target efficiency of the isolated DC/DC converter is set to $\eta_{\mathrm{t,DCDC}} = 99.0\,\%$ at full load considering a certain margin. Furthermore, the DC/DC converter should achieve a power density of at least 3 kW/L (50 W/in^3), comparable to the power density of the *i*TCM AC/DC stage. In literature, a 15 kV SiC MOSFET-based isolated

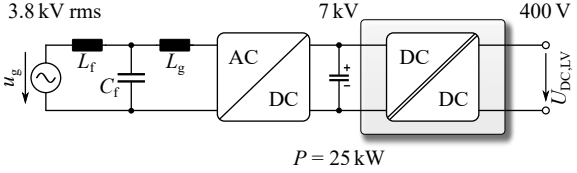

Fig. 5.1: Single-cell realization of an MV-AC to 400 V DC SST. In this chapter the isolated DC/DC converter is realized.

DC/DC converter with similar specifications (10 kV to 340 V, 20 kW) has been presented, achieving an extrapolated full-load efficiency of 97.3 % and a power density of roughly 1.5 kW/L (25 W/in^3) [214]. In contrast, considering the defined goals, the DC/DC converter at hand should generate only a third of the relative losses and should reach at least twice the power density.

To achieve such a compact converter, a relatively high switching frequency has to be selected, while to obtain the high efficiency, the switching losses have to be minimized by the operation of all MOSFETs under ZVS conditions. Since the front end PFC AC/DC stage controls the DC-link voltage, it is sufficient to realize the DC/DC converter with a fixed voltage transfer ratio and galvanic isolation. For this reason, a series resonant converter (SRC) operated at resonance frequency and therefore acting as "DC transformer", tightly coupling its input and output voltages according to the primary-side and secondary-side turns ratio, is selected [215]. Due to the significantly different rise times of the MV-side and the LV-side switch-node voltages, a special modulation scheme has to be used for the system to achieve ZVS for all MOSFETs.

Due to the combination of the high switching frequency and the high voltage stress, dielectric losses in the transformer insulation material start playing a role. It has been shown in [154] that a thermal runaway and a destruction of the transformer could occur, if epoxy resin was selected as insulation material. The reasons are the relatively high dissipation factor and the low thermal conductivity of epoxy resins, which makes them unsuitable for the insulation of MF MV transformers. Therefore, a special two component silicone compound is selected as insulation material and the vacuum pressure potting (VPP) process used to insulate the winding package is described in detail.

Section 5.2 describes the isolated DC/DC converter topology and its modulation scheme to achieve ZVS conditions over the complete power range. In **Section 5.3**, the design of all main converter components is explained in detail, with the focus on the MF transformer and its electrical insulation, as well as the MV-side and LV-side power electronic interfaces. **Section 5.4** presents the experimental setup and measurement results including the obtained voltage and current waveforms, and the calorimetrically measured efficiency and loss distribution for different power levels. Finally, a summary of the chapter is provided in **Section 5.5**.

5.2 Topology and Modulation

For the isolated DC/DC converter stage, an LLC SRC topology is selected, mainly for the reason of clamped switch voltages, the simple operation without closed-loop control, and the possibility to achieve ZVS for all semiconductors. Hence, a high switching frequency of 48 kHz can be selected, which results in a high power density. Furthermore, the SRC features sinusoidal transformer currents, which are beneficial in terms of reduced HF effects in the windings while the currents show a low rms value, which is only $\pi/\left(2\sqrt{2}\right) = 1.11$ times higher than the corresponding DC current (magnetizing current neglected). The circuit diagram of this topology is shown in **Fig. 5.2(a)**. It consists of a split DC-link and a 10 kV SiC MOSFET-based half-bridge on the MV-side, a 52 : 6 MF MV transformer providing the galvanic isolation, and a 1200 V SiC MOSFET-based full-bridge on the LV-side. The half-bridge configuration is selected due to its rather simple construction and the associated voltage division by a factor of two, which is beneficial for the MF transformer design [174]. Although the LV-side DC-link voltage is only 400 V and therefore devices with 650 V or 900 V rating could be employed, 1200 V, 25 mΩ SiC MOSFETs are used due to their outstanding performance and to keep the flexibility to adapt the SST for 800 V applications by just changing the transformer turns ratio.

5.2.1 Modulation Scheme of the SRC

As already mentioned, the main task of the DC/DC converter is to provide the galvanic isolation and the constant 7 kV/400 V voltage transfer ratio, as the DC-link voltage level is controlled to a constant value by the AC/DC front end of the SST realized in **Chapter 4**. Therefore, the SRC is operated at its resonance frequency, where it provides a quasi load-independent voltage transfer ratio and acts as a "DC transformer" [215]. Furthermore, incorporating a certain transformer magnetizing current i_μ allows the ZVS operation of all MOSFETs and hence, due to the typically low SSL, a downsizing of passive components such as the MF transformer and the DC-link capacitors is enabled by increasing the switching frequency, which is finally selected as 48 kHz considering the results of a power density/efficiency Pareto optimization (see **Section 5.3.4**).

Fig. 5.2(b) shows the simulated voltage and current waveforms together with the gate signals of all MOSFETs. For the "DC trans-

former" operating mode of the SRC, both the MV-side and the LV-side MOSFET bridges apply rectangular voltages with 50 % duty cycle to the resonant tank, i.e. the transformer's leakage inductance L_σ and the resonance capacitor C_r, resulting in sinusoidal currents on both sides of the transformer. However, in order to achieve soft-switching, the

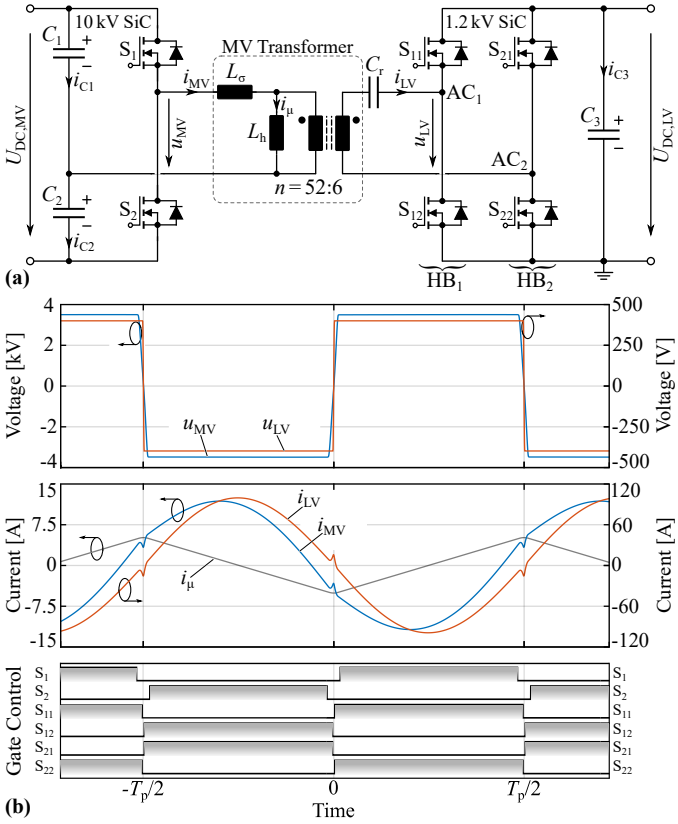

Fig. 5.2: **(a)** Circuit diagram of the SRC consisting of a 10 kV SiC MOSFET half-bridge, an MF MV transformer for the galvanic isolation and the voltage step-down, a resonance capacitor C_r, and a 1200 V SiC MOSFET full-bridge. **(b)** Simulated voltage and current waveforms of the SRC together with the corresponding gate control signals. It can be seen that the major part of the magnetizing current i_μ is switched on the MV-side.

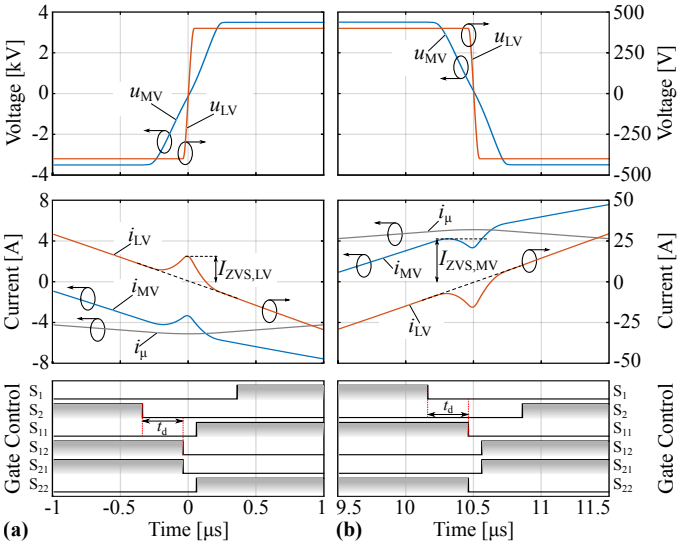

Fig. 5.3: Magnified view of the MV-side and the LV-side voltages and currents u_{MV}, i_{MV} and u_{LV}, i_{LV} during **(a)** the rising and **(b)** the falling voltage edge together with the gate control signals. Due to the much larger Q_{OSS} of the MV-side MOSFETs (relative to the corresponding current), the voltage on the MV-side u_{MV} rises/falls much slower than the LV-side voltage u_{LV}. With the phase shift t_d between the MV-side and the LV-side gate control signals, the switching transitions can be center-aligned, whereby the different rise/fall times create a current spike in the transformer which is utilized as ZVS current for the LV-side MOSFETs. The magnetizing current is used to a large extent as ZVS current for the MV-side MOSFETs.

MOSFETs must turn off a certain remaining inductive current

$$I_{ZVS} = Q_{OSS}/T_{dt}, \tag{5.1}$$

which depends on the effective output charge Q_{OSS} of the switching MOSFETs and the maximum duration of the resonant switching transition, i.e. the dead time duration T_{dt}. Since the effective output charge Q_{OSS} of the 10 kV SiC MOSFETs on the MV-side is much larger than the effective output charge of the 1200 V SiC MOSFETs on the LV-side (considering the turns ratio of the transformer and/or the corresponding current), the available transformer magnetizing current should mainly flow on the MV-side to guarantee ZVS of all MOSFETs. This can be

achieved by introducing a comparably small phase shift t_d between the MV-side and the LV-side gate control signals. **Fig. 5.3** shows a magnified view of the voltages and currents during the rising and the falling voltage edge, respectively. As can be seen, the phase shift t_d is selected such, that the MV-side bridge switches the major part of the magnetizing current i_μ. Furthermore, due to the phase shift t_d, the voltage transitions of the MV-side and the LV-side are aligned symmetrically, i.e. the much faster LV-side voltage transition is located in the middle of the MV-side voltage transition. Consequently, this leads to a certain voltage-time-area which is applied to the leakage inductance L_σ of the transformer, resulting in small current spikes on both sides of the transformer. As can be seen in **Fig. 5.3**, these current spikes lead to a reduction of the ZVS current on the MV-side, whereas on the LV-side the absolute value of the current i_LV is increased. By proper selection of the phase shift t_d, now the LV-side switches exactly at the peak of these current spikes and hence, ZVS is also enabled for the LV-side. Furthermore, it is shown in [216] that the ZVS mechanism is automatically center-aligning the voltage transitions and therefore is self-stabilizing. In practice, a compromise between the amount of (magnetizing) current switched on either side has to be found in dependency of the Q_OSS mismatch of the MV-side and the LV-side by selecting a suitable phase shift t_d. In the system at hand, it has been observed that this modulation works very well over the whole load range (0 kW to 25 kW) and is highly robust against changes in the switching frequency, the voltage level and even the phase shift t_d. For the experimental analysis $t_\mathrm{d} = 300\,\mathrm{ns}$ has been selected (cf. **Tab. 5.1**).

5.3 System Design

In the following, the design of the individual main components of the isolated DC/DC converter is described. **Tab. 5.1** shows the specifications of the SRC, together with the values of the switched currents, and the rms current stresses of the individual components as a basis for the converter design.

5.3.1 MV-Side 10 kV SiC MOSFET Half-Bridge

On the MV-side, a 10 kV SiC MOSFET-based half-bridge comprising *Wolfspeed CPM3-10000-0350* devices in combination with a split DC-

Tab. 5.1: Specifications and characteristics of the isolated DC/DC converter. MOSFET on-state resistances given for $T_\mathrm{j} = 75\,^\circ\mathrm{C}$ (MV-side) and $T_\mathrm{j} = 100\,^\circ\mathrm{C}$ (LV-side).

Parameter	**Symbol**	**Value**
Nominal power	P_N	25 kW
Switching frequency	f_sw	48 kHz
MV-side DC-link voltage	$U_\mathrm{DC,MV}$	7 kV
LV-side DC-link voltage	$U_\mathrm{DC,LV}$	400 V
MV-side DC-link capacitance	C_1, C_2	500 nF
LV-side DC-link capacitance	C_3	70 µF
Resonance capacitance	C_r	3.8 µF
Transformer leakage inductance	L_σ	195 µH
Transformer magnetizing inductance	L_h	4.1 mH
Transformer turns ratio	n	52 : 6
MV-side transformer rms current	$I_\mathrm{MV,rms}$	8.6 A
LV-side transformer rms current	$I_\mathrm{LV,rms}$	70.6 A
Nominal phase shift	t_d	300 ns
MV-side ZVS current	$I_\mathrm{ZVS,MV}$	4 A
LV-side ZVS current	$I_\mathrm{ZVS,LV}$	16 A
MV-side DC-link rms current	$I_\mathrm{C1,C2,rms}$	4.8 A
LV-side DC-link rms current	$I_\mathrm{C3,rms}$	30.9 A
MV-side switch rms current	$I_\mathrm{S,MV,rms}$	6.0 A
LV-side switch rms current	$I_\mathrm{S,LV,rms}$	50.0 A
MV-side switch resistance	$R_\mathrm{DS,on,MV}$	400 mΩ
LV-side switch resistance	$R_\mathrm{DS,on,LV}$	11.3 mΩ

link is used. For the determination of the semiconductor losses, the conduction and the switching losses are calculated in the following. With the on-state resistance and the rms current given in **Tab. 5.1**, the total conduction losses of both MOSFETs are $P_\mathrm{c,MV} = 28.8\,\mathrm{W}$ during full-load operation. Furthermore, although the MOSFETs are operated under ZVS conditions, certain SSL arise as shown in **Chapter 3**. Therefore, the calorimetrically measured SSL in **Fig. 5.4(a)**, taken from **Chapter 3** and depicted again for a better readability, are used to determine the switching losses. For a DC-link voltage of

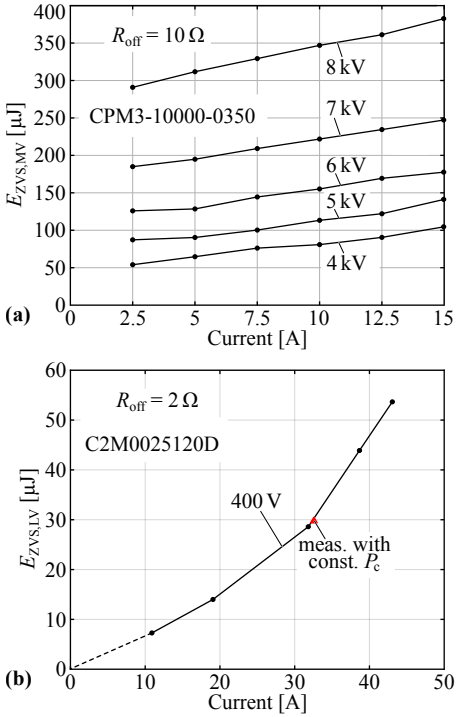

Fig. 5.4: (a) Calorimetrically measured soft-switching losses (SSL) of the 10 kV SiC MOSFETs for different DC-link voltages and currents (taken from **Chapter 3**). **(b)** Calorimetrically measured SSL of one *C2M0025120D* 1200 V SiC MOSFET for different currents and a DC-link voltage of 400 V. To verify the applied calorimetric SSL measurement method, the indicated point is measured with constant conduction losses P_c and two different switching frequencies.

$U_{DC,MV} = 7\,kV$ and a switched current of $I_{ZVS,MV} = 4\,A$, the energy loss per switching cycle and per MOSFET is $E_{ZVS,MV} = 191\,\mu J$. Therefore, the MV-side switching losses at a switching frequency of $f_{sw} = 48\,kHz$ are $P_{sw,MV} = 18.3\,W$ and together with the conduction losses, the total MV-side semiconductor losses are 47.1 W at full load.

For the realization of the MV-bridge, the goal is to achieve a highly compact design, despite the fact that large distances for the electrical isolation are necessary for voltages in the MV range. According to the

IEC 60950-1 International Standard [130], for a sustainable operation, the required creepage distance for 7 kV is $d_{cr} = 32$ mm, and the minimum clearance distance is $d_{cl} = 17.5$ mm. Therefore, during the design of the PCB-based MV-bridge, possible creepage paths have to be identified and interrupted by creepage slots, which increase the breakdown voltage since $d_{cl} < d_{cr}$.

Fig. 5.5 shows the realized MV bridge. The PCB interconnects the DC-link capacitor with the low-side and the high-side MOSFETs, whereby busbars (not visible) are used for the connection of the drain terminals (i.e. the base plates) of the MOSFETs. Since both MOSFETs are mounted on one PCB, the full (switched) DC-link voltage of $U_{DC,MV} = 7$ kV occurs between the low-side and the high-side circuits on the PCB. In order to still achieve a highly compact design despite the large required creepage distances, a creepage slot separates the high-side from the low-side circuits. Furthermore, the gate driver circuit developed in **Chapter 2** with its highly compact 20 kV-rated isolation transformers is used. These transformers are fed from driver

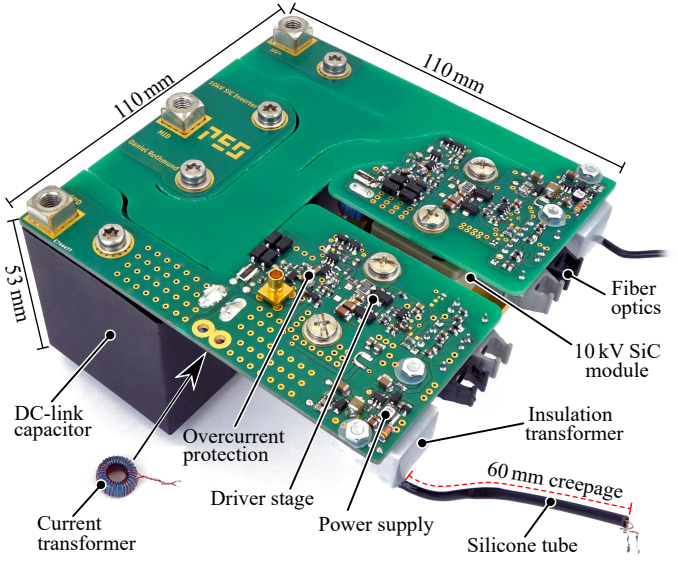

Fig. 5.5: 10 kV SiC MOSFET-based half-bridge with DC-link capacitors and gate driving circuitry including an ultra-fast OCP circuit, and 20 kV isolation voltage rated (and tested) gate driver power supplies.

circuits which are separated from the MV, whereby the required creepage distance is provided by silicone tubes that are enclosed in the insulation material of the transformers. In order to protect the 10 kV SiC MOSFETs against harmful overcurrents in case of e.g. an isolation breakdown or an operational fault, the gate drivers are equipped with the ultra-fast OCP circuit developed in **Chapter 2**, which reacts within 22 ns and safely turns off all MOSFETs in case of a fault.

The 10 kV SiC modules are directly mounted on separate heat sinks without any electrical insulation in order to achieve a low parasitic switch-node capacitance compared to the solution of grounding the heat sink and isolating it from the module with e.g. an aluminum nitride plate. However, since the base plates of the modules are not isolated (i.e. the base plates act as drain terminals), the heat sinks (not shown) are floating on the respective drain potential such that the fans have to be separated from them by a clearance distance of at least $d_{\mathrm{cl}} = 17.5\,\mathrm{mm}$, as similarly done for the *i*TCM AC/DC converter in **Chapter 4**. Although a certain part of the air flow is bypassing the heat sinks, a thermal resistance of $R_{\mathrm{th,MV}} = 0.125\,\mathrm{K/W}$ per heat sink is achieved and the expected heat sink temperature increase is less than 5 K, which is beneficial in terms of a low $R_{\mathrm{DS,on}}$ and consequently low conduction losses of the 10 kV SiC MOSFETs.

5.3.2 LV-Side 1200 V SiC MOSFET Full-Bridge

The LV-side of the isolated DC/DC converter is realized with 1200 V, 25 mΩ SiC MOSFETs *C2M0025120D* from *Wolfspeed*, since they offer a low on-state resistance and a certain flexibility for future, e.g. 800 V, applications. However, in order to handle the high current on the LV-side and to reduce the conduction losses, each switch of the LV-side full-bridge consists of three parallel-connected *C2M0025120D* MOSFETs. With the intention of a symmetric current distribution among the three parallel MOSFETs per switch, the current path from the DC-link capacitor through the bridge-legs to the AC-terminals must be symmetric for all MOSFETs. **Fig. 5.6** shows the realized layout of the full-bridge. The MOSFETs of each half-bridge are lined up between the DC-link capacitors on the left side and the AC terminals on the right side. This ensures an equal current path length through all MOSFETs and guarantees a symmetric current distribution. Furthermore, the high-side MOSFETs (HS1...HS3) and the low-side MOSFETs

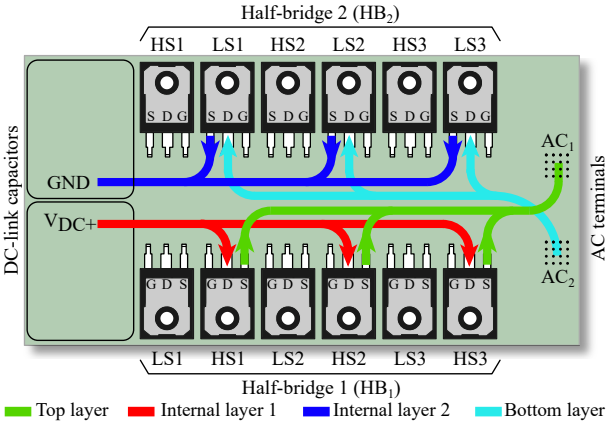

Fig. 5.6: Bottom-view of the full-bridge layout for symmetrical current path arrangement and/or equal current path lengths through the individual MOSFETs in the parallel connection. PCB current path only indicated for high-side MOSFETs of half-bridge 1 (HB_1), cf. S_{11} in **Fig. 5.2(a)**, and low-side MOSFETs of half-bridge 2 (HB_2), i.e. S_{22} in **Fig. 5.2(a)**. Each switch is composed of three parallel-connected TO247 devices.

(LS1...LS3) in each half-bridge are placed alternately in order to minimize the commutation loop inductance. Inductive switching tests show that currents of up to 100 A can be switched without oscillations or an asymmetric current distribution, as the homogeneous temperature distribution observed on thermal images of the MOSFET cooling pads prove.

For an estimation of the LV-side semiconductor losses, the conduction and the switching losses of the LV-side full-bridge are calculated. With the LV-side MOSFET rms current $I_{\mathrm{S,LV,rms}}$ and the equivalent on-state resistance $R_{\mathrm{DS,on,LV}}$ of the parallel connection of three *C2M0025120D* MOSFETs given in **Tab. 5.1** (specified for $T_{\mathrm{j}} = 100\,^{\circ}\mathrm{C}$), the conduction losses are $P_{\mathrm{c,LV}} = 113\,\mathrm{W}$.

LV-Side SSL Measurements

Similar to the MV-side MOSFETs, also the SSL of the 1200 V SiC MOSFETs are not given in the datasheet. Therefore, calorimetric SSL measurements with *C2M0025120D* MOSFETs are carried out for a drain-source voltage of 400 V and different switched currents. Thereby, an

inductor is connected to the AC terminals of the full-bridge, which is soft-switched with a duty cycle of 50 %, leading to symmetrical triangular current in the inductor. The switched current can be varied via the switching frequency or the inductance value, where the MOSFETs always turn off the peak value of the triangular current under ZVS conditions [124, 217]. Besides the conduction losses during the on-state of the MOSFETs, each turn-off event generates a certain amount of SSL in the MOSFETs. The total LV-side semiconductor losses are measured via the temperature increase of the heat sink and its thermal resistance R_{th} (similar as shown in **Section 4.4**), which is known from calibration measurements with constant DC power. In order to extract the SSL out of the total losses, at the same time the conduction losses are determined by measuring the current and the on-state voltage of the MOSFETs with a special on-state voltage measurement circuit (OVMC) [218] during operation. For these SSL measurements, the full-bridge is equipped with only one *C2M0025120D* MOSFET per switch. **Fig. 5.4(b)** shows the resulting SSL per switching cycle for a DC-link voltage of 400 V and different switched currents, measured with a turn-off gate resistor of $R_{\mathrm{off}} = 2\,\Omega$. As can be seen, the SSL increase approximately linearly with the current for low currents and start increasing disproportionally for currents beyond 20 A.

To verify the measured SSL, a different measurement method is applied. Thereby, the intention is to keep the conduction losses P_{c} constant (by keeping the peak of the triangular current and therewith the switched current i_{sw} constant) and to measure the total semiconductor losses P_{semi1} and P_{semi2} (again calorimetrically via the temperature increase and the R_{th} of the heat sink) at different switching frequencies f_{sw1} and f_{sw2} [181]. Consequently, to keep the peak current constant when the switching frequency is changed, the inductance value has to be adapted accordingly. By taking the difference between the two measured loss values, the conduction losses cancel out and the SSL for the switched current i_{sw} can be calculated as

$$E_{\mathrm{ZVS,LV}}\left(i_{\mathrm{sw}}\right) = \frac{P_{\mathrm{semi2}} - P_{\mathrm{semi1}}}{f_{\mathrm{sw2}} - f_{\mathrm{sw1}}}. \tag{5.2}$$

This method has been applied for a switched current of $i_{\mathrm{sw}} = 32.5\,\mathrm{A}$ and as can be seen in **Fig. 5.4(b)**, the obtained SSL match very well with the curve obtained with the OVMC, which proves a high accuracy of the measurement method.

With the measured SSL of the LV-side MOSFETs, the SSL during operation of the DC/DC converter can now be determined. Assuming a symmetric current distribution among the three parallel MOSFETs per switch of the full-bridge and a ZVS current of $I_{\mathrm{ZVS,LV}} = 16\,\mathrm{A}$ (cf. **Tab. 5.1**), each MOSFET turns off a current of $I_{\mathrm{ZVS,LV}}/3 = 5.33\,\mathrm{A}$. Consequently, the total LV-side switching losses of the four power switches each consisting of 3 parallel MOSFETs are

$$P_{\mathrm{sw,LV}} = 4 f_{\mathrm{sw}} \cdot 3 E_{\mathrm{ZVS}}\,(I_{\mathrm{ZVS,LV}}/3) = 1.56\,\mathrm{W}, \tag{5.3}$$

whereby the the switching loss curve in **Fig. 5.4(b)** is extrapolated towards lower currents in order to obtain the SSL value for a switched current of 5.33 A. As can be noted, the SSL of the LV-side are very low, considering the system power rating of 25 kW. However, in e.g. a DAB topology operated with conventional phase shift modulation, where the MOSFETs would be turned off at the peak of the current [219, 220], the SSL would become significant.

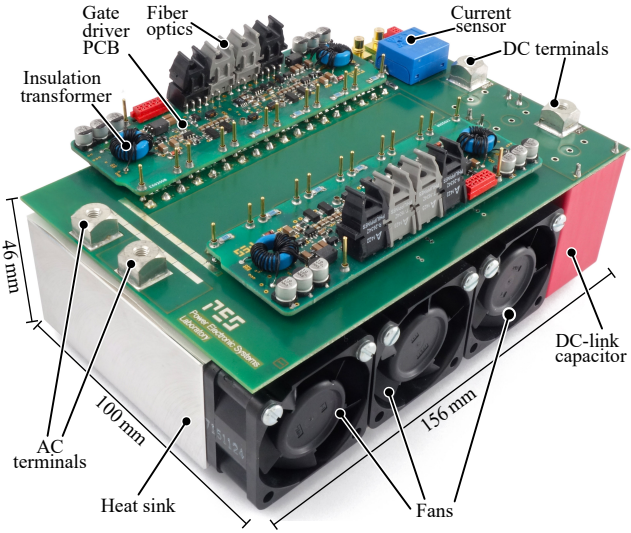

Fig. 5.7: Picture of the LV-side 1200 V SiC-based full-bridge with three parallel *C2M0025120D* MOSFETs per switch.

LV-side Full-Bridge Hardware

Fig. 5.7 shows a picture of the realized 1200 V SiC-based LV-side full-bridge. It consists of a 4-layer power PCB (140 µm outer and 105 µm inner copper thickness), which holds the MOSFETs, the DC-link capacitors, the heat sink as well as the fans, and two gate drive PCBs with isolated auxiliary supplies, each driving one half-bridge. The gate signals are received via optical fibers from a central DSP-board. Furthermore, current and voltage measurement circuits are implemented for control and monitoring purposes. As can be seen, the bridge is highly compact with dimensions of only $156 \times 100 \times 46$ mm.

5.3.3 Resonance Capacitor

As shown in **Fig. 5.2(a)**, the resonance capacitor C_r is connected in series to the LV-side winding of the transformer and it not only acts as resonance capacitor but also as DC-blocking capacitor in case the voltage applied from the LV-side full-bridge contains a small DC offset, e.g. due to incorrect switching times resulting from discretization errors in the DSP. Further reasons not to place the resonance capacitor on the MV-side are the split DC-link on the MV-side, which already takes care of the DC-blocking, and the fact that no MV-insulation of the resonance capacitor is required on the LV-side. The capacitance of C_r can be calculated via the leakage inductance of the transformer (as well as the additional stray inductance of the busbars) and the desired resonance frequency, which is equal to the switching frequency f_sw and results in $C_\mathrm{r} = 3.8\,\mu\mathrm{F}$. Care must be taken when the DC-link capacitors are comparably small and start influencing the resonance [221]. Due to the high transformer LV-side rms current of 70.6 A (cf. **Tab. 5.1**), which also flows through the resonance capacitor C_r, a low-loss capacitor with a high current rating is required. Therefore, and with the purpose of offering a high flexibility regarding the value of C_r, a parallel connection of 38 *C0G* ceramic capacitors in a 2220 package ($5.7 \times 5.0 \times 2.8$ mm) with 100 nF each and a voltage rating of 450 V is selected. With the dissipation factor of $\tan\delta = 0.05\,\%$, the capacitor losses can be determined as $P_\mathrm{Cr} = 2.17\,\mathrm{W}$ at full-load operation. The capacitor array is soldered between two copper plates for the connection to the transformer and the PCB terminal. At full-load operation of the converter, the capacitor temperature under natural convection is only 45 °C, which means that no additional cooling is required.

5.3.4 MF MV Transformer

One of the key components of the isolated DC/DC converter at hand is the MF MV transformer, which is responsible for the voltage step-down and the galvanic isolation between the MV-side and the LV-side. Although it is well-known in power electronics how to design MF transformers (for voltages below 1 kV) and it is well-known from power systems how to design the electrical insulation of MV or even HV 50/60 Hz transformers, the combination of MF and MV in a transformer is very challenging in many aspects. Only the recent development of SiC MOSFETs with blocking voltages of 10 . . . 15 kV and their outstanding soft-switching capabilities allow for the combination of switching frequencies around 50 kHz and switched voltages in the 5 . . . 10 kV range. With these conditions and the aim for a highly compact design (which directly excludes oil as insulation and cooling medium for this power level due to the required oil-expansion tank and dehydration breather), two major problems arise. Due to the MV, the insulation material layer, which encapsulates the MV winding and isolates it from the LV winding and the core, has to be designed rather thick. However, the losses of the MV winding have to be extracted by heat conduction through the insulation material, which typically features only a very low thermal conductivity. Furthermore, in a highly compact transformer, the surface area for the heat extraction is small and consequently, the cooling of the MV winding is very challenging. Secondly, due to the combination of the high switching frequency and the high switched voltage, dielectric losses inside the insulation material can lead to local hotspots, to thermal degradation and even to a thermal runaway [154]. Consequently, it is important to select a suitable insulation material and to consider the dielectric losses during the design process of the MF MV transformer.

Transformer Pareto Optimization

With the purpose of achieving a highly compact and efficient transformer, an optimization with respect to power density and efficiency is performed. For the high targeted efficiency and power density, only ferrite core material, litz wire and shell-type windings are considered. While the magnetizing inductance, the core material (BFM8) and the isolation distances are fixed, a sweep over the following parameters is carried out and the winding, the core, and the dielectric losses within the transformer operated at nominal power are determined by coupled

FEM simulations:

- operating frequency;
- core shape (U-core or E-core);
- core dimensions;
- number of layers and chambers on the MV-side;
- number of turns on the MV and the LV-side;
- litz wire diameter and number of strands;
- strand diameter.

The simulations include HF effects in the litz wire [222–224], the fringing field of the air gap [225], and the effects of the non-sinusoidal magnetic flux by calculating the core losses using the iGSE [226]. During the simulation, transformer designs which exceed a certain current

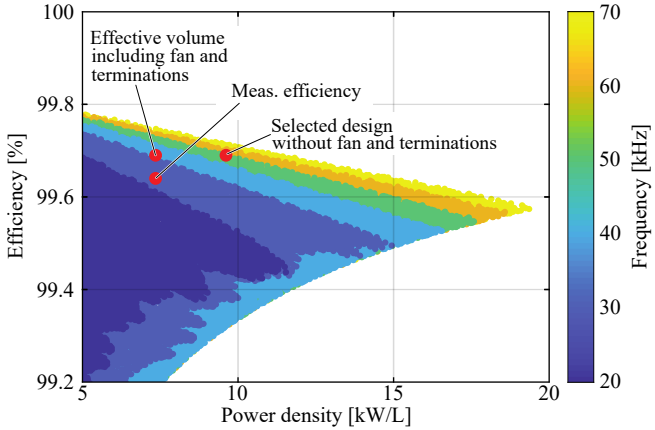

Fig. 5.8: Power density/efficiency Pareto optimization of the MF MV transformer for different operating frequencies (color-coded). The optimization does not include the volume of the fan and the terminations. Therefore, these volumes are added separately and the effective volume of the selected design is indicated in the figure. Additionally, the measured efficiency, which is slightly lower than the simulated efficiency (99.64 % compared to 99.69 %, i.e. 0.05 % difference), is shown.

Tab. 5.2: Key parameters of the realized MF MV transformer.

Parameter	**Value**
Nominal power	25 kW
Operating frequency	48 kHz
Terminal voltages	±3.5 kV/ ± 400 V
Winding	52:6 turns, litz wire, shell-type
MV litz winding	630 × 71 µm, three layers, two chambers
LV litz winding	2500 × 100 µm, single layer
Core type	U-core, BFM8 ferrite, 2500 mm^2
Air gap	2 × 1.1 mm
Insulation	4.0 mm thickness, designed for 15 kV

density in the windings, a certain core loss density, or a certain dielectric loss density in the insulation material are discarded in order to avoid designs which would cause a thermal runaway of the transformer. **Fig. 5.8** shows the results of the Pareto optimization of the transformer for different operating frequencies. As can be seen, there is a trend towards higher possible efficiencies and power densities for an increasing operating frequency. However, the efficiency gain between 50 kHz and 70 kHz is rather insignificant and a selection of a high switching frequency would also lead to an increase of the soft-switching losses and hence to a decrease of the total converter efficiency. In order to reach the DC/DC converter's full-load efficiency goal of 99.0 %, the maximum allowed transformer losses are 75 W, given the fact that the MV-side and the LV-side bridges, the resonance capacitor, the auxiliary supplies, and the fans together generate around 175 W of losses. Therefore, a design with a calculated efficiency of 99.69 % and an operating frequency of 48 kHz is selected. The selected transformer is a U-core design, which features a larger exposed area of the winding package for the forced convective cooling and an easier construction of the litz wire terminations compared to E-core designs. The selected transformer design is indicated in **Fig. 5.8**; if the volumes of the fan and the litz wire terminations are included, a slight reduction of the power density results. Furthermore, the design point of the realized transformer with its calorimetrically measured efficiency (cf. **Section 5.3.4**) is shown in the Pareto plot and as can be noted, the simulated and the measured

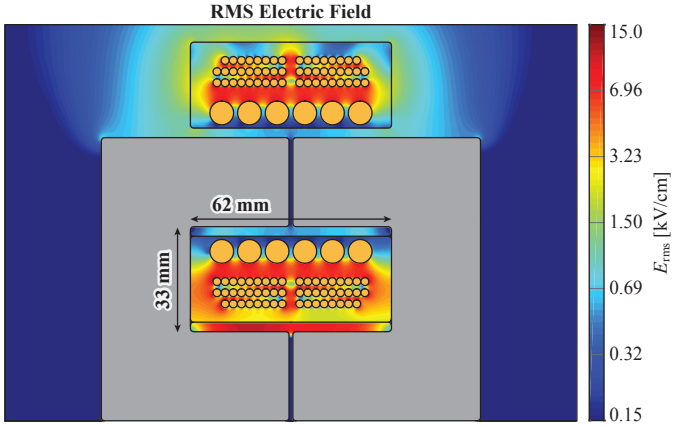

Fig. 5.9: FEM simulation of the electric field distribution (rms values) of the transformer for a $\pm 3.5\,\mathrm{kV}/400\,\mathrm{V}$ excitation.

efficiencies (99.69 % and 99.64 %, respectively) are very close, which indicates an accurate simulation as well as an accurate measurement of the transformer losses.

Tab. 5.2 lists the key parameters of the realized transformer design and as can be noted, a two-chamber winding is selected on the MV-side in order to reduce the electric field stress between the three layers of the MV winding, which increases the reliability of the electrical insulation. For a deeper analysis of the electric field strength inside the transformer winding package and the surrounding air, the result of a 2D FEM simulation is shown in **Fig. 5.9**, whereby the insulation material has been modeled with its permittivity given in **Tab. 5.3**. As can be seen, the maximum rms electric field is $15\,\mathrm{kV/cm}$ and the peak value is more than 10 times below the electric breakdown field strength of the utilized insulation material. It has to be noted that a higher electric field would lead to quadratically higher dielectric losses

$$P_{\mathrm{ins}} \propto E^2 \cdot f_{\mathrm{sw}} \cdot \tan\delta, \tag{5.4}$$

and possibly to partial discharges, which both would enhance the material's ageing process due to local hot spots and degradation. As will be shown by calorimetric measurements in **Section 5.3.4**, the dielectric losses account for a significant part of the total transformer losses and cannot be neglected as in case of MF LV transformers.

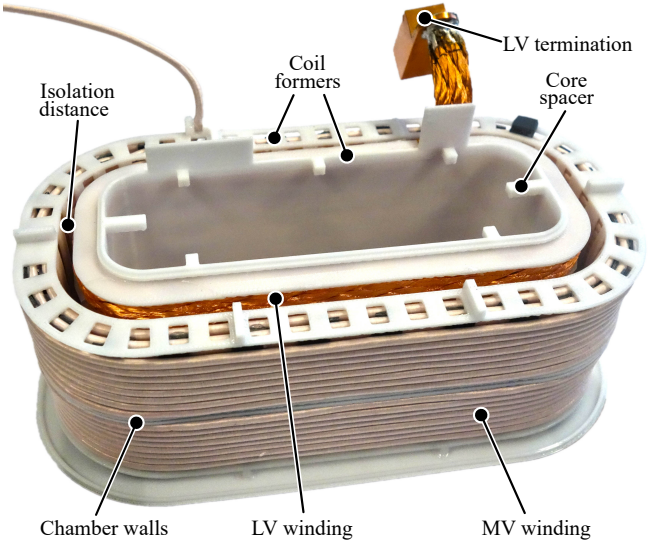

Fig. 5.10: Picture of the MV and LV transformer windings on their 3D-printed coil formers. The isolation distance between the MV and the LV windings, as well as the chamber walls separating the two MV winding chambers can be seen.

A more detailed analysis of the optimization of this MF MV transformer as well as a description of the underlying models is given in [79].

Construction of the Transformer Windings

Due to their different electric potentials, the MV and LV windings have to be isolated from each other by an electrical insulation material. In order to guarantee that the insulation material thickness between the MV and the LV windings is constant at a value of 4.0 mm, the MV and the LV windings are wound on individual 3D-printed coil formers (material: polycarbonate) and assembled concentrically, as shown in **Fig. 5.10**. For the cooling of the windings, the LV coil former is equipped with core spacers (cf. **Fig. 5.10**), which separate the core from the winding package by a certain distance and allow an air flow to pass in between. Furthermore, polypropylene spacers are used between the three layers of the MV winding in order to keep a distance of

0.8 mm between the individual layers, such that the insulation material can flow into the interspaces during the subsequent potting process. Additionally, for the monitoring of the winding temperature, several NTC temperature sensors are placed close to the LV windings. Once the windings are assembled, the HF litz wires are soldered into the intended copper terminations to guarantee a low contact resistance.

Vacuum Pressure Potting of the Transformer Windings

For the potting of the windings, the coil formers are closed with another 3D-printed part, resulting in a sealed winding package which is then filled up with the insulation material. As already mentioned, standard insulation materials such as Epoxy resins are unsuitable for MF MV applications due to their typically low thermal conductivity and/or high dielectric losses. Therefore, a two-component silicone compound (containing thermally conductive particles) of type *TC-4605 HLV* from Dow Corning is used. The properties of this material are listed in **Tab. 5.3**. An additional advantage compared to epoxy resin is the mechanical flexibility of the silicone, which prevents it from cracking during the curing.

The utilized silicone shows outstanding dielectric and thermal properties but reacts highly sensitively to amines, amides, nitriles, and alcohols etc. during the curing process. These substances might be contained e.g. in adhesives used for the mechanical fixing of the turns during the construction of the windings. When the still liquid silicone comes in contact with one of these substances, it might not cure properly, preventing it from developing its dielectric properties [227]. Therefore, the compatibility of the silicone to any adhesives or in general to any materials contained in the winding package has to be verified. It has

Tab. 5.3: Properties of the utilized silicone *Dow Corning® TC-4605 HLV*.

Property	**Value**
Dielectric strength	24 kV/mm
Dielectric constant ε_r	< 4.1 for $f > 50$ kHz
Dissipation factor $\tan\delta$	$< 0.8\,\%$ for $f > 50$ kHz
Thermal conductivity	1 W/(m K)

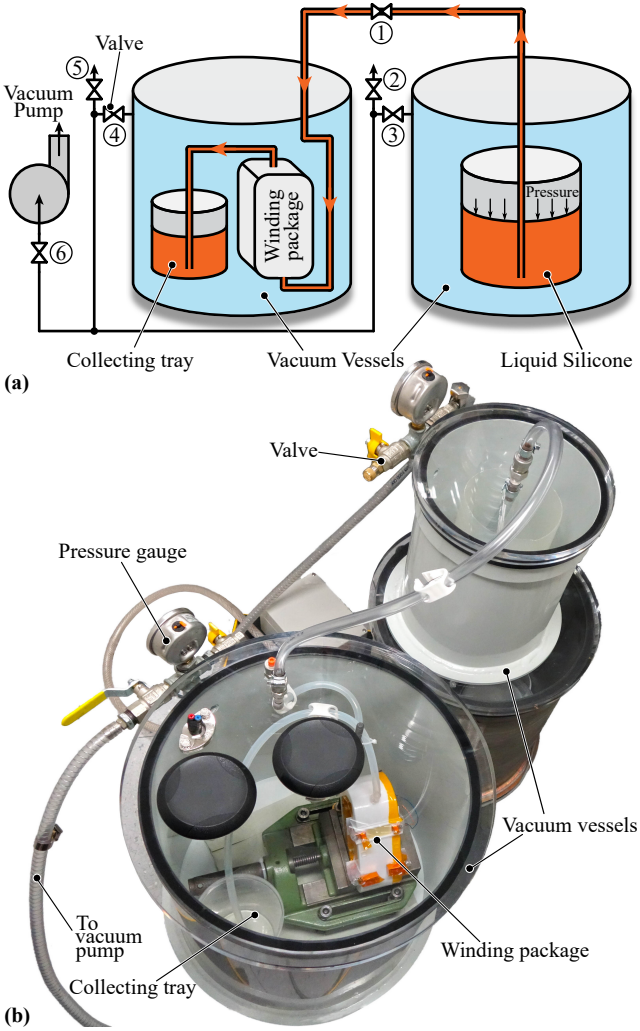

Fig. 5.11: **(a)** Schematic drawing and **(b)** picture of the silicone vacuum pressure potting (VPP) process of the transformer winding package. Both vessels are evacuated (30 mbar) to devolatilize the liquid silicone. Then, the pressure in the right vessel is increased, pressing the silicone through the tubes into the sealed winding package, from where the excessive silicone flows into a collecting tray. After the filling process, the pressure is increased to atmospheric pressure again, in order to compress possible vacuum cavities. Finally, the silicone is cured at 120 °C.

been found that e.g. cyanoacrylate-based instant adhesives and UV adhesives are unsuitable, whereas two-component instant adhesives, such as *LOCTITE 3090*, for example, have been used successfully.

To guarantee a high reliability of the MV-insulation, the insulation material must be free of cavities or other imperfections, which can lead to partial discharges. To achieve this, a vacuum pressure potting (VPP) process, as shown in **Fig. 5.11(a)**, is used. Thereby, the already mixed liquid two-component silicone and the winding package are placed in two separate vessels. With a vacuum pump, both vessels are evacuated down to a pressure of 30 mbar while valves ①, ③, ④ and ⑥ are open. Since there is no silicone yet in the collecting tray, the tubings and the sealed winding package are evacuated as well. After a certain time, when the liquid silicone is devolatilized, valves ④ and ⑥ are closed. The pressure in the right vessel is then slightly increased by shortly opening valve ②, which presses the liquid silicone into the tubings and from bottom to top through the winding package. To remove possible cavities inside the winding package, this process is not stopped before approximately 300 mL of the liquid silicone have flown through the winding package into the collecting tray. For the further steps, it is important that both ends of the tubings are located below the surface of the liquid silicone, such that no air can enter. Now, valve ① is closed and both vessels are pressurized again to atmospheric pressure, compressing possible vacuum cavities inside the winding package. Finally, the tubes entering and leaving the winding package are clamped to avoid any further flow of the silicone and the winding package is cured for several hours at a temperature of 120 °C in order to activate the adhesion of the silicone to other materials. The best results regarding adhesion are achieved when the temperature is applied directly after the VPP process, although the curing itself does not require an increased temperature. However, if the temperature is only applied after the curing at room temperature, the silicone might detach from the coil former, leading to undesired vacuum or air cavities between the coil former and the silicone. **Fig. 5.11(b)** shows a picture of the VPP setup with the two vacuum vessels and the sealed winding package. The covers of the vacuum vessels are made out of acrylic glass and each vessel is equipped with a pressure gauge to enable the monitoring of the process by eye.

Transformer Prototype

The assembled transformer consisting of the winding package and the ferrite cores is shown in **Fig. 5.12**. As can be seen, the core spacers of the winding package separate it from the core by a certain distance, forming an air channel for the forced convection cooling of both, the core and the windings. However, since the insulation between the LV winding and the inner wall of the winding package is not designed for MV but only for LV (cf. **Fig. 5.9**) and since the core spacers represent a direct creepage path between the winding package and the cores, the cores must be tied to ground potential. For this reason, a grounding bar is attached to the ferrite cores with the help of a conductive silver adhesive.

In operation, the transformer is cooled by a fan (not shown), which provides an air flow onto the cores, the winding package and through

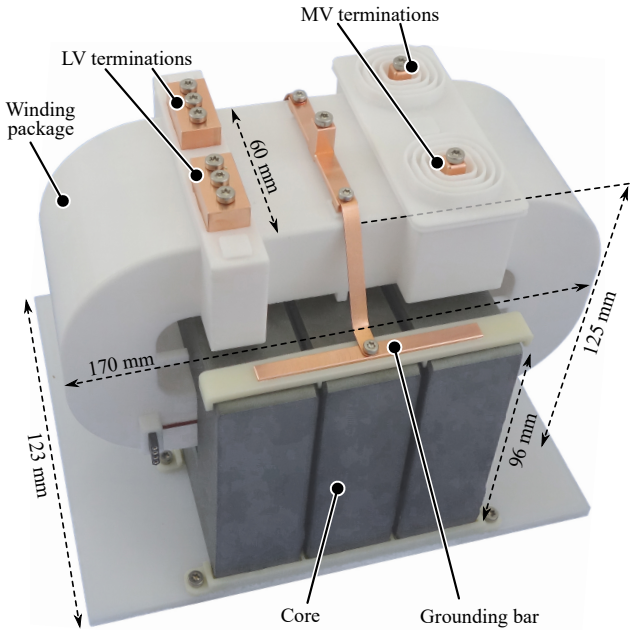

Fig. 5.12: Picture of the realized 25 kW MF MV transformer consisting of three BFM8-ferrite U-core sets and the winding package with the mounted MV-side and LV-side terminations.

the air channel in between. The dimensions of the transformer are indicated in **Fig. 5.12** and the boxed volume of the transformer itself is 2.6 L and the volume is 3.4 L when also the terminations and the fan are included. Therefore, the 25 kW MF MV transformer achieves a power density of 7.35 kW/L (including the fan and the terminations).

Transformer Measurements

To characterize the efficiency of the transformer as one of the key components of the isolated DC/DC converter at hand, electrical or calorimetric measurement methods can be applied. However, it has been shown that electrical efficiency measurements of highly efficient systems (either converters or individual power components) are inaccurate, even in case the input and output voltages and currents are DC or 50 Hz AC (cf. **Section 4.4.1**). Consequently, even larger measurement errors can be expected in case of an electric efficiency measurement of an MF MV transformer operated with switched voltages due to skews between the voltage and current measurements and the limited bandwidth of the measurement devices. Therefore, instead of electrically measuring the input and output power of the transformer to determine its efficiency, its losses are directly measured calorimetrically. With the aim of not only determining the total losses of the transformer but also the loss distribution among the windings, the core, and the insulation material, these loss components are measured independently in a highly accurate two-chamber calorimeter [228].

Fig. 5.13(a) shows the measurement setup for the determination of the winding losses. For this purpose, the LV winding of the transformer is shorted, and since the currents during the operation of the DC/DC converter are quasi-sinusoidal, a sinusoidal current with a frequency of 48 kHz (which is the operation frequency of the DC/DC converter) is impressed into the MV winding. Due to the short circuit on the LV-side, the magnetic flux in the core is nearly zero and no core losses but only winding losses $P_{\mathrm{Cu,load}}$ in the equivalent resistance R_{Cu} of both windings caused by the sinusoidal load current occur and can be measured calorimetrically for different amplitudes (i.e. different loads).

Furthermore, the circuit for the measurement of the core losses is shown in **Fig. 5.13(b)**. Thereby, the MV-side of the transformer is left open, while a rectangular voltage is applied to the LV winding, creating a triangular magnetizing current and magnetic flux with equal values as

during real operation of the DC/DC converter. Besides the actual core losses P_{core}, also the small part of the ohmic and air gap fringing-field-related winding losses $P_{\mathrm{Cu,mag}}$ generated by the magnetizing current during DC/DC operation is measured, but together with the (orthogonal) losses from the winding loss measurement with the sinusoidal load current (cf. **Fig. 5.13(a)**) add up to the correct total winding losses, i.e. $P_{\mathrm{Cu}} = P_{\mathrm{Cu,load}} + P_{\mathrm{Cu,mag}}$. Furthermore, in this arrangement, the dielectric losses in the insulation material are present as well. However, the dielectric losses are measured individually (as shown below) to separate them from the core losses.

Since the losses of ferrite material are typically strongly temperature dependent, the core temperature during the core loss measurement must be equal to the core temperature during the operation of the DC/DC converter. Due to the air channel between the winding package and

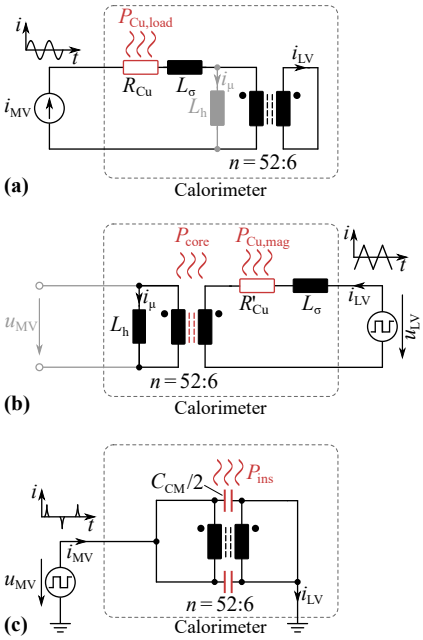

Fig. 5.13: Calorimetric measurement setups for **(a)** the winding losses, **(b)** the core losses, and **(c)** the dielectric losses P_{ins} in the insulation material of the transformer.

the ferrite cores of the transformer, their thermal coupling is extremely low. Accordingly, the core temperature and hence the core losses are not significantly influenced by the winding temperature during the converter operation. For this reason, the core temperature and therewith the core losses can be assumed as constant over the whole power range, since always the same voltage time area is applied to the transformer independently of the transferred power.

As already mentioned, due to the combination of the high voltage and the high frequency, dielectric losses occur in the insulation material. To determine these losses by measurement, the circuit in **Fig. 5.13(c)** is used. As can be seen, the transformer is shorted on both sides and grounded on the LV-side. The MV-side is excited by a rectangular voltage generated by the MV-side bridge-leg (cf. **Section 5.3.1**) with the same frequency (48 kHz), rise time (600 ns), and amplitude (±3.5 kV) as during real converter operation. Thereby, the parasitic CM capacitances C_{CM} between the MV and the LV windings are charged and discharged, which in combination with a certain dissipation factor $\tan\delta$ causes dielectric losses that are measured calorimetrically. As can be noticed, with this pure CM excitation, only the CM-component of the dielectric losses are included. However, in converter operation, there is also a differential-mode (DM) voltage across the MV winding, which causes dielectric losses in the inter-layer insulation as well. To also include these losses, the electric field FEM simulation (cf. **Fig. 5.9**) is calibrated in such a way that the pure CM insulation losses match with the measurement, before the simulation is extended to also include the DM losses.

The distribution of the calorimetrically measured transformer losses is shown in **Fig. 5.14** together with the efficiency curve over a load range from 5 kW to 30 kW. Besides the winding, core and dielectric losses, the losses caused by the fan for the cooling of the transformer are also included. As can be seen, at full load (25 kW), the measured efficiency reaches 99.64 %. Furthermore, with a loss distribution of $P_{\mathrm{Cu}} = 34.8\,\mathrm{W}$ (winding losses), $P_{\mathrm{core}} = 43.2\,\mathrm{W}$ (core losses), $P_{\mathrm{ins}} = 8.0\,\mathrm{W}$ (dielectric losses), and $P_{\mathrm{cooling}} = 5.8\,\mathrm{W}$ (cooling losses), it can be noted that the dielectric losses account for 9 % of the total transformer losses and therefore indeed have to be considered in MF MV transformer designs, especially regarding a possible thermal runaway.

If for the calorimetric transformer loss measurement the following measurement errors are assumed: 25 % for the core losses (due to the

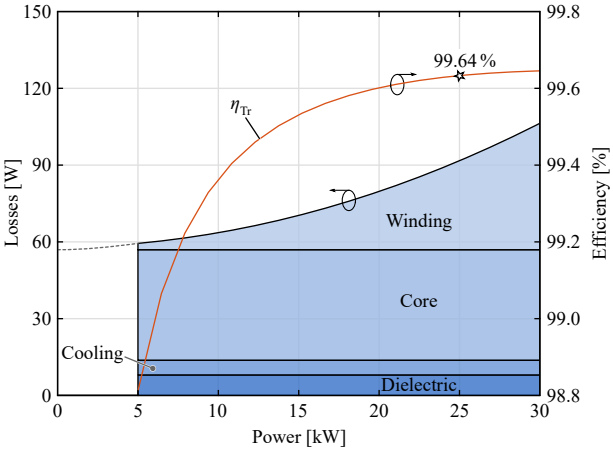

Fig. 5.14: Calorimetrically measured distribution of the transformer losses together with the transformer efficiency curve. At the rated converter power of 25 kW, the transformer efficiency reaches 99.64 %.

strong temperature dependency), 20 % for the winding losses, 40 % for the dielectric losses (since only the CM part is measured and the DM part is determined by a re-calibrated simulation), and 2 % for the cooling power, a total efficiency measurement error of ±0.08 % results for the transformer, i.e. its efficiency is in the range of 99.64 % ± 0.08 % = (99.56 % . . . 99.72 %).

5.4 Experimental Setup and Results

For the experimental verification and the efficiency evaluation of the realized DC/DC converter, an appropriate test setup is required. Due to its bidirectionality, the converter can either be supplied from the LV-side or the MV-side, whereby the transferred power is dissipated in a variable load resistor in order to be able to operate the converter at different power levels. In this case, the converter is supplied from the 400 V-side by two paralleled 0...500 V, 0...40 A power supplies (*Regatron TopCon Quadro TC.P.16.500.400.S*). During converter operation, the voltages and currents at the transformer terminals are measured especially in order to see whether or not the converter operates under ZVS conditions on both sides. For this purpose, a *LeCroy HDO4054A*

oscilloscope in combination with *Pearson* current transformers and differential voltage probes (*LeCroy HVD3605*) is used.

For the measurement of the complete system efficiency, the losses of all main power components have to be measured. As already mentioned, calorimetric measurement methods achieve a much higher accuracy compared to electrical measurement methods. Since the efficiency curve of the transformer is already characterized calorimetrically (cf. **Fig. 5.14**), the remaining main sources of losses are the 10 kV SiC MOSFETs on the MV-side and the 1200 V SiC MOSFETs on the LV-side. The power demand of the auxiliary supplies for the gate drivers and the cooling system can easily be measured electrically, whereby the relatively small losses of the resonance capacitor C_r are taken from the calculation in **Section 5.3.3**.

For the accurate measurement of the semiconductor losses, the steady-state temperature increase of their heat sinks is measured and together with the thermal resistances of the heat sinks, which are known from calibration measurements with constant power, the semiconductor losses can be determined accurately (cf. **Section 4.4.2**). While high precision NTCs are used for the measurement of the heat sink temperature on the LV-side, a fiber-optic measurement system (*Optocon FOTEMPMK-19"*), which measures the temperature at the tips of up to 10 non-conductive optical fibers, is used to determine the temperature of the floating heat sinks on the MV-side. Due to the relatively small temperature increase of the MV-side heat sinks of $\Delta\vartheta_\mathrm{ss} = 4\,\mathrm{K}$ at full-load and a resolution of 0.2 K of the fiber optic temperature measurement, the measurement error is 10 %. Together with an assumed deviation of the thermal resistance of 5 %, the maximum expected error (for the full-load operating point) is $e_\mathrm{HS,MV} = 15\,\%$. On the LV-side, however, the resolution of the NTCs used for the temperature measurement is 0.1 K and leads together with a steady-state temperature increase of 16.5 K at full-load to a measurement error of $\pm 1.2\,\%$. With an assumed deviation of the thermal resistance of $\pm 5\,\%$, the worst case error of the LV-side semiconductor loss measurement is $e_\mathrm{HS,LV} = \pm 6.2\,\%$.

5.4.1 Measured Waveforms

Fig. 5.15(a) shows the measured voltage and current waveforms at the MV-side and the LV-side transformer terminals during full-load operation (25 kW) of the DC/DC converter, together with the magne-

tizing current obtained by taking the difference between the MV-side and the transformed LV-side current. As can be seen, the waveforms are smooth and are free of any oscillations, which verifies the careful design of the converter. In **Figs. 5.15(b) & (c)**, a magnified view of

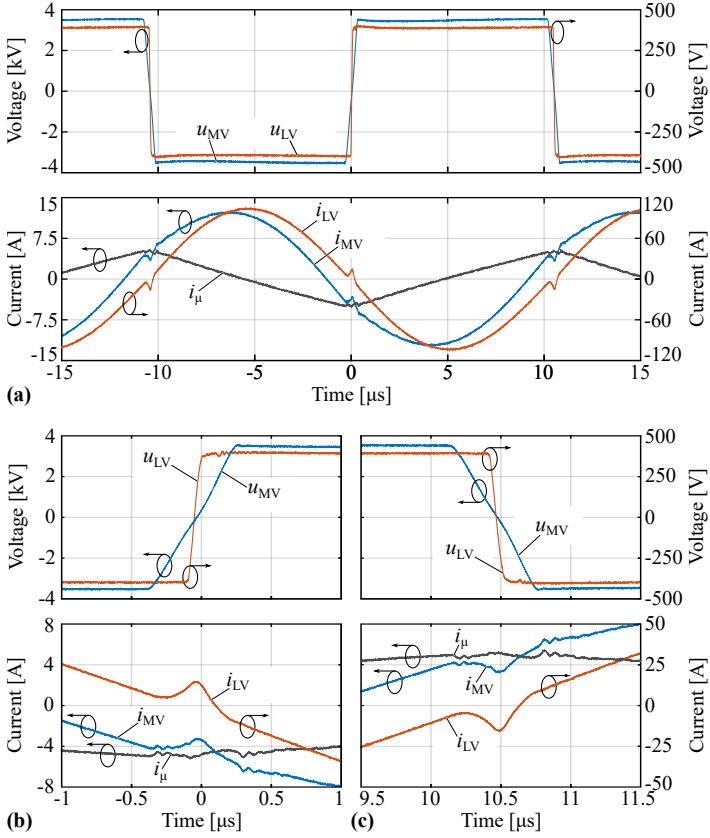

Fig. 5.15: **(a)** Measured voltage and current waveforms during 25 kW operation of the converter. The magnetizing current i_μ is determined as the difference between the MV-side current i_{MV} and the transformed LV-side current i_{LV}. **(b) & (c)** Magnified views of the voltages and currents during the rising and falling voltage transition, respectively. Practically the total magnetizing current i_μ is available for ZVS on the MV-side, whereas the current spikes are utilized for achieving ZVS on the LV-side.

the waveforms in the vicinity of the rising and falling voltage transitions is shown. It can be seen that the MV-side bridge switches almost the entire magnetizing current, whereby the LV-side bridge switches the current peak generated by the different rise/fall times of the MV-side and the LV-side voltage transitions. This means that both, the MV-side and the LV-side are operated under ZVS conditions and since the magnetizing current is load-independent, ZVS is achieved over the complete load range without a need for adjusting any parameters such as e.g. the phase shift or the switching frequency. During the measurements at different power levels, the robustness of the SRC against small changes in the switching frequency and the phase shift has been tested, especially regarding whether or not all semiconductors operate under ZVS conditions. Thereby, it has been found that the modulation is extremely robust due to its self-stabilizing effect (cf. **Section 5.2.1**), and ZVS is maintained even for changes in these parameters of up to $\pm 10\,\%$. Comparing the measured waveforms in **Fig. 5.15** to the simulated waveforms in **Figs. 5.2 & 5.3**, an almost perfect matching can be noticed.

5.4.2 Efficiency Measurements

One of the most important key characteristics of a power electronic converter is its efficiency, since the related energy losses are closely coupled to the operating costs of the converter during its lifetime. Therefore, the efficiency of the DC/DC converter is characterized for different loads between 5 kW and 25.6 kW. The calorimetrically measured efficiency curve is shown in **Fig. 5.16**. As can be seen, an efficiency of $99.0\,\%$ in the power range between 13 kW and 25 kW is achieved. This means that, in contrast to similar converters described in literature [214, 229, 230], the realized DC/DC converter not only achieves three times lower (relative) full-load losses, but is also well suited for partial load operation, e.g. in a redundant system, where two converters in parallel supply a critical load and are therefore operated at $50\,\%$ of their rated power [231]. With the given accuracy of the individual calorimetric measurements, the accuracy of the total DC/DC efficiency is $\pm 0.08\,\%$, i.e. the efficiency is between $98.92\,\%$ and $99.08\,\%$.

For a deeper analysis of the individual loss components of the DC/DC converter, **Fig. 5.17** shows the calorimetrically measured loss distribution. As can be seen, the LV-side MOSFETs and the transformer

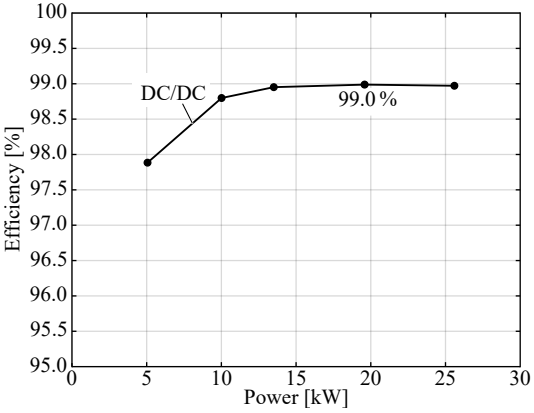

Fig. 5.16: Calorimetrically measured efficiency of the realized DC/DC converter. An efficiency of 99.0 % is achieved above 13 kW, which makes the DC/DC converter also well suited for partial load operation. The efficiency of the total SST (including the *i*TCM AC/DC converter) is shown in **Chapter 6**.

are responsible for the largest share of the losses, whereby the MV-side MOSFETs, the auxiliary supply power, and the resonance capacitor losses account for only a minor loss contribution. Whereas the transformer losses cannot be improved significantly any more (due to the given material properties), the LV-side MOSFET losses of 116 W (which match very well with the calculated losses of 113.8 W) could easily be decreased by a factor of two by replacing the 2nd generation 1200 V, 25 mΩ SiC MOSFETs with the latest 3rd generation 900 V, 11.5 mΩ SiC MOSFETs. However, even then the LV-side MOSFET conduction losses would still be significantly higher compared to the MV-side MOSFET conduction losses. To obtain equal conduction losses in both, the MV-side and the LV-side MOSFETs, the following conditions would have to be fulfilled, whereby the factor of two arises from the half-bridge/full-bridge configuration (magnetizing current neglected):

$$2R_{\mathrm{DS,on,LV}} \cdot \left(\frac{P}{U_{\mathrm{DC,LV}}}\right)^2 = R_{\mathrm{DS,on,MV}} \cdot \left(\frac{2P}{U_{\mathrm{DC,MV}}}\right)^2, \tag{5.5}$$

$$R_{\mathrm{DS,on,LV}} = 2R_{\mathrm{DS,on,MV}} \cdot \left(\frac{U_{\mathrm{DC,LV}}}{U_{\mathrm{DC,MV}}}\right)^2 = \frac{R_{\mathrm{DS,on,MV}}}{153}. \tag{5.6}$$

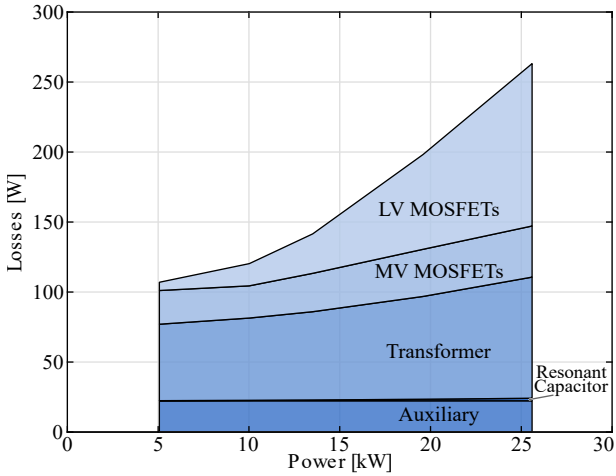

Fig. 5.17: Measured loss distribution of the DC/DC converter's main components over the power range from 5 kW to 25.6 kW.

Consequently, based on an MV-side on-state resistance of $R_{\mathrm{DS,on,MV}} = 400\,\mathrm{m\Omega}$, the LV-side on-state resistance would have to be $R_{\mathrm{DS,on,LV}} = 2.6\,\mathrm{m\Omega}$ according to (5.6) for equal MV-side and LV-side conduction losses. Such a low on-state resistance could be achieved by using e.g. 5 parallel 900 V, 11.5 mΩ SiC MOSFETs per switch. However the total SiC chip area on the LV-side would be 4.8-times higher than the total SiC chip area on the MV-side in this case. This underpins the extremely good performance of the 10 kV SiC MOSFET technology, or in other words, as long as the $R_{\mathrm{DS,on}}$ does not scale better than quadratically with the blocking voltage for the same chip area (cf. (5.6)), the MV-MOSFETs will always outperform the LV-MOSFETs. This can be explained by the fact that the SiC MOSFET channel resistance becomes much less significant compared to the SiC bulk resistance with increasing blocking voltage, therefore the total $R_{\mathrm{DS,on}}$ is closer to its theoretical limit for MOSFETs with higher breakdown voltage [189].

Furthermore, comparing the measured full-load MV-side MOSFET losses of 36.5 W to the calculated losses of 47.1 W, a significant difference can be noticed. This can be explained by the antiparallel SiC JBS diode chip (*CPW3-10000-Z020B*) contained in the 10 kV modules. With a forward voltage threshold of 1 V and a differential resistance of

300 mΩ, circuit simulations show that the JBS diode conducts a significant part of the load current during full-load converter operation with a power flow from the LV-side to the MV-side. This results in an equivalent $R_{\mathrm{DS,on}}$ of 232 mΩ and total MV-side conduction losses of 16.7 W instead of 28.8 W calculated with the $R_{\mathrm{DS,on,MV}}$ of 400 mΩ of the MOSFET chip itself. Thus, together with the MV-side switching losses of $P_{\mathrm{sw,MV}} = 18.3$ W, the total MV-side semiconductor losses sum up to 35 W, which is very close to the measured value. For a power flow from the MV-side to the LV-side, where the antiparallel JBS diodes do not conduct any current, conduction losses of 28.8 W would appear and would lead to a slight decrease ($< 0.05\,\%$) of the converter efficiency compared to a power flow from the LV-side to the MV-side.

5.5 Summary

In this chapter, the bidirectional isolated 25 kW, 48 kHz, 7 kV to 400 V DC/DC back end converter of the SST employing 10 kV SiC MOSFETs on the MV-side has been realized and tested. Due to its tight coupling of the input and output voltages and the ability to achieve ZVS in all semiconductors, an SRC topology operated at resonance frequency and therefore implementing a "DC transformer" is selected. Due to the significantly higher parasitic output capacitances C_{OSS} of the 10 kV MV-side SiC MOSFETs and the consequently much slower voltage transitions compared to the LV-side, a special modulation scheme is required. A small phase shift between the gate control signals of the MV-side and the LV-side bridge-legs is introduced, which allows an active sharing of the magnetizing current between the MV and the LV-side and therefore enables ZVS on both sides.

The design of all main power components of the DC/DC converter is presented in detail with a focus on the MF MV transformer and its electrical insulation. It is highlighted that the proper selection of the insulation material is extremely important, since a material with a low dissipation factor and a high thermal conductivity is required to avoid a thermal runaway and hence the destruction of the transformer insulation material. Therefore, a thermally highly conductive silicone compound is selected and the vacuum potting process (VPP) of the winding package is described in detail. For a deeper analysis, the distribution of the transformer losses among the core, the winding, and the insulation material is measured calorimetrically and it is found that

the dielectric losses account for 9 % of the total transformer losses and have to be considered in MF MV transformer designs. The transformer reaches a measured efficiency of 99.64 % at 25 kW transferred power.

Measurements at different power levels show that all switches are operated under ZVS and that the modulation scheme is highly robust against changes in e.g. the switching frequency and/or the phase shift. Finally, the converter efficiency is measured calorimetrically in the power range between 5 kW and 25.6 kW, achieving an efficiency of 99.0 % between 13 kW and 25.6 kW, at a power density of 3.8 kW/L (63 W/in^3, referenced to 25 kW). Due to the extremely flat efficiency curve, the realized DC/DC converter is also well suited for partial load operation. Furthermore, from the calorimetrically measured loss distribution, it can be seen that the LV-side conduction losses account for the largest part of the converter losses. Accordingly, by simply replacing the 1200 V LV-side SiC MOSFETs with latest generation 900 V SiC MOSFETs, the LV-side conduction losses could be decreased by a factor of two, resulting in a total DC/DC converter efficiency beyond 99.2 %.

Compared to 10 . . . 15 kV SiC MOSFET-based isolated DC/DC converters with similar specifications, the realized converter in this work generates three times less (relative) losses and achieves a 2.5 times higher power density.

6 Conclusion & Outlook

The conspicuous consequences of the climate change have led to an increased environmental awareness of society, industry, and politics. To limit the effects of the climate change, a significant reduction of the greenhouse gas emissions and hence a drastic decrease of the fossil fuel consumption is necessary especially in the transportation and the electricity generation sectors. On the other hand, one of the main goals of the modern society is economic growth, which is, however, closely linked to an increasing energy consumption. To enable both, a decrease of the greenhouse gas emissions and a growth of the global economy, renewable energy sources have to replace fossil fuels in the future. Accordingly, PV power and wind power generation have grown significantly in the past decade and together reached an installed capacity of 1 TW by 2018.

At the same time, to utilize the electricity generated by renewable sources, an electrification of the transportation sector is necessary. This means that passenger cars, public buses, freight trucks, and in future even ships and aircrafts have to be electrified. Furthermore, other large-scale DC-loads such as data centers are assumed to increase their (highly energy-demanding) computational power significantly over the coming years. For these reasons, a substantial increase in the consumption of electric energy can be expected in the near future and a large share of the consumed energy will be provided via LV-DC (e.g. 400 V DC) buses, e.g. for data centers and EV battery charging applications. Furthermore, on the generation-side, PV-power plants and wind turbine generators with subsequent rectifiers represent DC-sources. Accordingly, since the distribution grid is implemented as MV-AC grid, MV-AC to LV-DC conversions are required on the load-side and LV-DC to MV-AC

conversions are required on the generation-side.

In this context, SSTs are considered as a more efficient, more compact, and more flexible solution to interface an LV-DC bus to the MV-AC grid compared to the state-of-the-art solution employing an LFT and an AC/DC converter. With the goal to increase the efficiency of the power supply chain of data centers and to supply single server racks directly from the MV-AC grid, a 25 kW, 3.8 kV AC to 400 V DC SST has been realized and tested in this thesis.

In contrast to multi-cell SSTs consisting of several series-connected converter cells to interface the high voltage on the MV-side, a single-cell approach consisting of a single-cell AC/DC front end and an isolated DC/DC converter, both based on latest generation 10 kV SiC MOSFETs, has been implemented.

6.1 Results and Conclusions

The two main performance indicators for an SST are its efficiency and its power density. In **Chapter 4** and **Chapter 5**, these performance indicators are separately given for the *i*TCM AC/DC converter and the isolated DC/DC converter, respectively. To finally demonstrate the performance of the total SST system, **Fig. 6.1** shows the efficiency of both individual converters and of the total SST, i.e. the product of both efficiency curves. As can be seen, the the full-load efficiency of the 3.8 kV AC to 400 V DC SST reaches a value of 98.1 % and hence even surpasses the full-load target efficiency of $\eta_{\mathrm{SST}} = 98\,\%$.

Additionally, **Fig. 6.1** shows the achieved efficiency of the SST proposed by *Fuji Electric*, which is used as a benchmark system to compare the performance of the realized SST to an existing SST with similar specifications. As can be seen, the SST treated in this thesis shows a significantly higher efficiency over the entire power range and with its 98.1 % full-load efficiency exceeds the full-load efficiency of the *Fuji Electric SST* by 2.1 %, or in other words, generates less than half the losses. Furthermore, with the achieved power densities of $\rho_{\mathrm{AC/DC}} = 3.28\,\mathrm{kW/L}$ and $\rho_{\mathrm{DC/DC}} = 3.8\,\mathrm{kW/L}$ for the *i*TCM AC/DC stage and the isolated DC/DC converter, respectively, a total power density of $\rho_{\mathrm{SST}} = 1.76\,\mathrm{kW/L}$ results. Compared to the power density of 0.4 kW/L of the system of *Fuji Electric*, the realized SST is more than four times smaller. This shows that the single-cell approach with 10 kV SiC MOSFETs is superior to the much more complex multi-cell

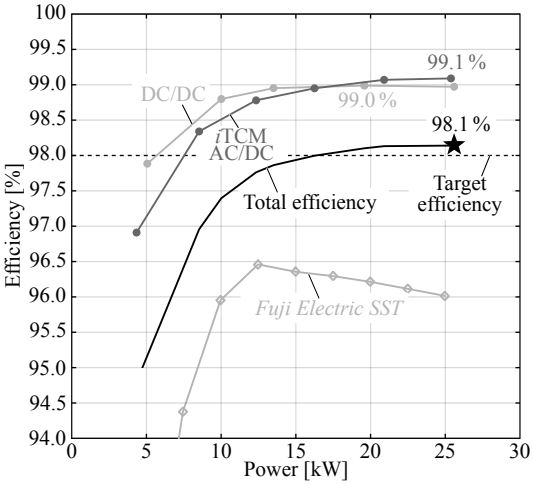

Fig. 6.1: Calorimetrically measured efficiency of the realized *i*TCM AC/DC converter and the isolated DC/DC converter as well as the total efficiency of the SST. The full-load efficiency of the SST reaches 98.1 % and thus even surpasses the full-load target value of 98 %. Additionally, the efficiency of the multi-cell SST of *Fuji Electric* [92] (used as benchmark) is given and as can be seen, the SST developed in this thesis outperforms the multi-cell approach by more than 2 % at full load, i.e. generates less than half the losses.

approach.

To achieve this unprecedented performance, many different aspects have been addressed and improved in this thesis compared to state-of-the-art solutions. Thereby, a complete technology-package for the implementation of highly efficient AC/DC and isolated DC/DC converters based on 10 kV SiC MOSFETs has been developed and the most important findings are listed in the following.

- To enable a highly compact design of MV converters of this power class, not only the main power components but also the auxiliary hardware such as the isolated gate drivers have to be realized as compact as possible. Contrary to the most prominent approach in literature, which is to isolate the auxiliary transformers of the gate drivers with air as insulation medium, a proper insulation material as well as a special transformer design, which features only one isolation barrier, are employed in order to decrease the

volume of the isolated gate drivers. Due to the very low volume of the developed isolation transformers, it is possible to integrate the entire gate driver circuit into future intelligent MV SiC modules, which allows to further improve the switching behavior of the devices due to the lower achievable gate loop inductance and at the same time significantly simplifies the design process of MV converters, since no external isolation measures are required anymore for the gate drivers. The achieved coupling capacitance of the isolation transformer is only 2.6 pF and tests have shown that it can reliably withstand a 20 kV DC voltage and the voltage stresses occurring during operation in MV AC/DC and DC/DC converters with DC-link voltages of 7 kV and switching frequencies beyond 125 kHz.

- In MV converters, so-called flashover faults (FOF) can occur e.g. due to an insulation failure of one of the switches in a bridge-leg configuration or an insulation failure in the main transformer. To protect the 10 kV SiC devices from destruction due to the resulting overcurrents, it is of high importance to provide a reliable and robust overcurrent protection (OCP) circuit which is able to withstand the extremely high voltage and current transients during an FOF and to safely turn off the device. The realized ultra-fast OCP features a reaction time of only 22 ns and it has been experimentally proven that it can safely clear a HSF and an FOF within less than 200 ns at a DC-link voltage of 7 kV.

- An analysis of the accuracy of electrical measurement methods for determining the soft-switching losses (SSL) such as the double pulse test show that large measurement errors can occur due to the limited accuracy of the measurements of the voltage and current transients during the switching process of the 10 kV SiC MOSFETs. To achieve a higher measurement accuracy, a novel calorimetric SSL measurement method has been developed, where the 10 kV SiC MOSFETs are continuously operated under soft-switching conditions while the generated losses are directly determined from the temperature increase of a brass block attached to the cooling pad of one of the devices. To split the total losses into switching losses and conduction losses, an additional switch is inserted in series to the device under test, which in combination with a special modulation scheme allows the accurate determina-

tion of the SSL. The conducted measurements show that the SSL are mainly depending on the DC-link voltage and are a factor of 30 lower compared to the HSL of the 10 kV SiC MOSFETs. Additional measurements prove that the SSL arise to a large extent purely from the charging and discharging of the nonlinear output capacitances of the MOSFET and especially of the antiparallel SiC JBS diode.

- Due to the fact that the 10 kV SiC MOSFETs show 30 times lower SSL compared to their HSL, all devices employed in the SST should be operated under ZVS conditions to achieve a higher efficiency and a higher power density. Therefore, a novel bidirectional AC/DC converter topology, which enables soft-switching over the entire AC grid period, as well as a novel modulation scheme for the isolated LLC series resonant DC/DC converter which guarantees soft-switching for all devices under all load conditions have been developed. Especially in case of the front end AC/DC converter, the application of soft-switching techniques leads to a significant increase in the achievable efficiency and power density compared to hard-switched topologies.

- A theoretical analysis has shown that there is a fundamental difference between LV converters and MV converters regarding parasitic inductances and capacitances, which leads to completely different design rules. While in LV converters parasitic inductances should be minimized, MV converters of this voltage and power class require a minimization of the parasitic capacitances of e.g. the PCB layout and the magnetic components for a proper operation.

- A detailed error analysis shows that electrical efficiency measurements feature an insufficient accuracy in case of highly efficient power electronic converters. Especially for MV converters, where the voltages have to be scaled down by means of voltage dividers in order to be in a reasonable range for standard high-precision measurement equipment, the achievable measurement accuracy is very low and therefore, calorimetric measurement methods should be employed. With the applied methods, it is possible to measure the converter efficiencies with an accuracy of $\pm 0.1\,\%$ and $\pm 0.08\,\%$ in case of the AC/DC converter and the isolated DC/DC converter, respectively. Compared to electrical measurement meth-

ods, these accuracies are roughly a factor of 10 better and at the same time, the calorimetric measurement methods allow the determination of the loss distribution among the individual power components.

- Despite the implemented LCL-filter on the AC-side of the SST, undesired oscillations might occur when the SST is connected to an MV cable. However, it has been found that a simple RC termination network between the LCL-filter and the MV cable eliminates the oscillations independently of the cable length in a quasi lossless manner.

- Due to the combination of a high switching frequency and a high switched voltage, which in this extent is only possible with MV SiC devices operated under soft-switching conditions, dielectric losses in the electrical insulation material used to insulate e.g. the MF MV transformer start playing a role and could even lead to a thermal runaway. Therefore, the insulation material has to be selected carefully with regard to a low dielectric dissipation factor and a high thermal conductivity to enable the extraction of the losses by heat conduction through the insulation material.

6.2 Future Research Areas

The main objective of this work is to present solutions for the main challenges arising during the design and realization of a 10 kV SiC-based SST. Based on the obtained results, the following topics are suggested as future research areas:

- From a grid operator's or data center operator's point of view, the reliable operation of the power supply equipment is probably the most important aspect with an even higher significance than the efficiency and/or the power density. While it is claimed that multi-cell SSTs can achieve a high reliability by incorporating redundant cells, the probability of a failure of a component within the system is much higher in the first place, since the complexity and the number of components is much higher compared to a single-cell SST. Therefore, it is not clear which of the two approaches features the highest reliability and the longest lifetime with a minimum cost of ownership. Consequently, a future

research topic could be to compare the failure probabilities of single-cell and multi-cell SSTs under consideration of the total cost of ownership.

- In case of multi-cell SSTs or multi-cell applications where a high control bandwidth and therefore a high switching frequency is required, it would be possible to apply the *i*TCM modulation individually to each of the converter cells in order to achieve soft-switching and hence to enable higher efficiencies and/or higher power densities compared to hard-switched converter cells. Furthermore, a reduction of EMI would result.

- In case of the 10 kV SiC modules utilized in this thesis, it has been found that the antiparallel SiC JBS diode is responsible for the majority of the SSL, although it never conducts any current apart from the charging/discharging current during the switching transients. By omitting this antiparallel diode and using the body diode of the MOSFET instead, a significant reduction of the SSL is expected. Due to the lack of 10 kV SiC modules with a single MOSFET chip, these measurements could not be conducted but would be an interesting future research topic.

- The switching frequency pattern of the realized *i*TCM AC/DC converter is calculated in such a way that soft-switching is achieved over the full power range. However, for power levels below full-load, the generated triangular current ripple is actually higher than required, since the switching frequency pattern is hard coded at the moment. To improve the partial load efficiency, the switching frequency pattern could be adapted to the instantaneous power level by using the measured AC current as a variable in the switching frequency function. Since the switching frequency would increase for lower power levels, the switching losses might at some point start dominating, i.e. the switching frequency could be optimized to achieve the lowest total losses.

- The intended application of the realized SST is the supply of single server racks in a data center. Therefore, many of these SSTs would be connected to the same MV-AC grid. In case of a failure of one SST, the faulty unit has to be disconnected from the MV-AC grid by means of a circuit breaker in order to not cause a short circuit. However, MV circuit breakers are typically

designed for significantly higher currents and are very large, such that the volume of the SST could be dominated by the circuit breaker. Circuit breakers could, e.g., also be realized as solid-state breakers by incorporating the same 10 kV SiC devices, which would on the other hand cause significant conduction losses and additional high costs. Therefore, future research could evaluate the different possibilities for (hybrid) MV circuit breakers for this power range regarding their cost, volume, and losses.

Since the main enabling technology for the realized SST are the 10 kV SiC MOSFETs, a further development of their current carrying capability or even a further increase of the blocking voltage will potentially unveil entirely new research fields and/or enable even higher performances in the future. However, as shown from the loss distributions of the AC/DC and the DC/DC converters, the 10 kV SiC MOSFETs are not the limiting elements to achieve even higher performances, but rather the passive components. Therefore, to fully utilize the potential of the MV SiC technology, also the performance of magnetic and dielectric materials has to be improved.

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Curriculum Vitae

Personal Information

Name	Daniel ROTHMUND
Date of birth	January 20, 1989
Nationality	German
Contact	daniel.rothmund89@gmail.com
	+41 (0)79 339 27 54

Education

2013 – 2018	Doctorate at the Power Electronic Systems Laboratory (PES), ETH Zurich
2013	Master Thesis at the Power Electronic Systems Laboratory (PES), ETH Zurich
2008 – 2013	BSc and MSc studies in Information Technology and Electrical Engineering, ETH Zurich
2000 – 2008	Fürstenberg Gymnasium, Donaueschingen, Germany
1995 – 2000	Primary School, Hausen vor Wald, Germany

Work Experience

2013 – 2018	Research Assistant at the Power Electronic Systems Laboratory (PES), ETH Zurich
2011 – 2013	Laboratory Assistant at the Institute for Biomedical Engineering, ETH Zurich
2011	Laboratory Assistant at the High Voltage Laboratory, ETH Zurich