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EMC Filtering of Three-Phase PWM Converters

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presented by
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"In this life we cannot do great things.
We can only do small things with great love."

Mother Teresa

For my father.
Para meu pai.

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I thank God for the beauty of life.

Abstract

In modern Power Electronics systems high switching frequencies are employed to increase power density, but EMC filtering components are responsible for a large volumetric occupation of the power system. In some cases the EMC filters required to fulfill EMC regulations cover more than 30% of the total system volume. In a world where space gets expensive, the volumetric reduction of the components in EMC filters is of great importance aiming for reduced dimensions. Many studies and tools regarding the EMC of power converters have been proposed for single-phase systems, but literature on three-phase systems still lacks. Therefore, the main objective of this work is to develop techniques for modeling the generation and propagation of conducted emissions in three-phase PWM converters and propose filter design procedures which effectively attenuate the propagated noise in order to meet EMC and reduce the volume of the EMC filters.

Optimizing EMC filters requires several steps to be performed, which are described here focusing on three-phase PWM converters. Electromagnetic Compatibility standards are discussed and specified according to the scope of the work. The electrical environment in which the converters are installed and tested are of great importance. These are reviewed and modeled along with the measurement instruments, cables and loads. Within this task, considerations on electrical safety are done and the impact of safety in the design of EMC filters is shown.

The modeling of the conducted emissions is highly important and is achieved here, for modern three-phase PWM converters, through simplified equivalent circuits and noise source spectra based on simulation results and/or hardware measurements. The limitations of the performed EMC oriented modeling are discussed, where it is seen that the models

can be successfully applied for the design of EMC filters. Detailed models of filter components have been studied and are employed in the computer aided design of three-phase EMC filters. In order to experimentally evaluate three-phase filter designs and the modeling of the converters, measurement tools which allow for the separate sensing of CM and DM conducted emissions have been developed. Active filtering connected to the mains has also been researched, where the implementation of a mains connected HF amplifier based active CM filter has been proposed. A study on the impact of couplings in three-phase filters has been carried out, from where guidelines are identified and winding configurations for three-phase CM inductors are proposed in order to reduce magnetic couplings between the filter components.

Finally, a discussion on the increase in power density in the last decades is carried out. It is identified that EMC filters strongly impact the overall volume of three-phase PWM converter systems. An analytical procedure is proposed to estimate the total filter volume as function of the converters' rated power and switching frequency. A discussion about the limits of power density for the considered three-phase PWM converters for state-of-the-art power semiconductors is done and optimum switching frequencies are identified.

Kurzfassung

In modernen leistungselektronischen Systemen werden hohe Schaltfrequenzen verwendet, um die Leistungsdichte zu erhöhen, jedoch nehmen die dadurch notwendigen EMV-Filterkomponenten einen grossen Anteil des Systemvolumens ein. In manchen Fällen beanspruchen die zur Erfüllung der EMV-Norm notwendigen EMV-Filter mehr als 30 % des Gesamtsystemvolumens. In einer Zeit, in der Platz zunehmend teuerer wird, ist die Volumenreduktion der EMV-Filterkomponenten hinsichtlich einer Verringerung der Systemabmessungen von grosser Bedeutung. Viele Studien und Hilfsmittel bezüglich der EMV einphasiger Leistungskonverter wurden bereits veröffentlicht, im Bereich der dreiphasigen Systeme ist allerdings noch immer ein Mangel an Literatur festzustellen. Aus diesem Grund ist das Ziel der vorliegenden Arbeit die Entwicklung von Techniken zur Modellierung der Erzeugung und Ausbreitung von leitungsgebundenen Störungen in dreiphasigen PWM Konvertern, sowie die Entwicklung von Filterentwurfsmethoden, welche zu einer effektiven Abschwächung der verbreiteten Störung führen, um die gewünschte EMV zu erreichen und das Volumen der EMV-Filter zu verringern.

Die Optimierung von EMV-Filtern erfordert die Durchführung mehrerer Schritte, welche hier mit dem Schwerpunkt auf dreiphasige PWM Konverter beschrieben werden. Im Weiteren werden EMV-Normen im Rahmen der Ausrichtung dieser Arbeit diskutiert und spezifiziert. Die elektrische Umwelt, in welcher die Konverter betrieben und getestet werden, ist von grosser Bedeutung. Diese wurde deshalb überprüft und zusammen mit den Messinstrumenten, Kabeln und Lasten modelliert. Innerhalb dieses Aufgabenteils wurde die elektrische Sicherheit berücksichtigt und der Einfluss der Sicherheitsmassnahmen auf den Entwurf des EMV-Filters aufgezeigt.

Die Modellierung der leitungsgebundenen Störungen ist sehr wichtig und wird hier für moderne dreiphasige PWM Konverter durch vereinfachte Ersatzschaltbilder und Störquellenspektren erreicht, basierend auf Simulationsergebnissen und/oder Hardwaremessungen. Die Grenzen der EMV-orientierten Modellierung werden diskutiert, wobei gezeigt wird, dass die Modelle für den Entwurf von EMV-Filtern erfolgreich angewandet werden können. Weiterhin werden detaillierte Modelle der einzelnen Filterkomponenten untersucht und in den computergestützten Entwurf für dreiphasige Filter mit einbezogen. Um den Entwurf der dreiphasigen Filter und die Modellierung des Konverters experimentell zu bewerten, werden Messhilfsmittel entwickelt, welche die getrennte Messung von leitungsgebundenen Gleichtakt- und Gegentaktstörungen erlauben. Weiters wird auch die aktive Filterung mit Netzverbindung untersucht, wobei die Implementierung eines netzkgekoppelten Hochfrequenzverstärkers auf Basis eines aktiven Gleichtaktfilters vorgeschlagen wird. Eine Untersuchung zum Einfluss der Kopplung in dreiphasigen Filtern wird durchgeführt, woraus Richtlinien identifiziert und Windungsanordnungen für dreiphasige Gleichtaktstörungsdrosseln vorgeschlagen werden, um die magnetische Kopplung innerhalb des Filters zu reduzieren.

Abschliessend wird eine Diskussion über die Erhöhung der Leistungsdichte in den letzten Jahrzehnten durchgeführt. Es wird verdeutlicht, dass die EMV-Filter einen starken Einfluss auf das Gesamtvolumen dreiphasiger PWM Konvertersysteme haben. Ein analytischer Algorithmus zur Abschätzung des Filtergesamtvolumens als Funktion der Konverterleistung und Schaltfrequenz wird vorgestellt. Eine Diskussion über die Grenzen der Leistungsdichte der betrachteten dreiphasigen PWM Konverter für moderne Leistungshalbleiter wird durchgeführt und eine optimale Schaltfrequenz vorgeschlagen.

Contents

Chapter 1

Introduction

This chapter addresses the research field in which this work is inserted. A connection between Power Electronics and Electromagnetic Compatibility is highlighted, where the origins of potential compatibility problems generated by power converters onto their environment are introduced, leading to the necessary inclusion of filters.

The design of filters for EMC of power converters is discussed here, with its corresponding major tasks. The problem is then reduced to filters for three-phase PWM converters and related works with this focus are listed. It is identified that theoretical analysis and experimental tools still lack in the literature on this subject. Therefore, the motivation for this work is clarified. Finally, an overview of the work is presented with the description of the main tasks.

1.1 Power Electronics, EMC and Filters

The first electronics patent was filed and given to Edison in 1884 [1]. Since then power electronics has evolved as a major field in electrical engineering and is making significant contributions to modern technological growth. In [2] power electronics is described as the "[...] technology associated with the efficient conversion, control and conditioning of electric power by static means from its available input form into the desired electrical output form [...]". Power electronics is interdisciplinary, covering various

different areas of electrical engineering and has found its place in modern technology, such as in heat, light and motion control, power supplies and many more fields of application. The power rating reaches from a few watts in mobile phones up to multi mega (millions) watts in gas pipeline pumps and electrochemical applications, making this field of electrical engineering extremely broad [3]. Due to the broadness of power electronics, historians can investigate innovation in this field through central components embedded in power electronics systems or the interdisciplinary knowledge growing over time [4].

Historically, the major advances in power electronics have been driven by innovations and improvements in the power electronic switching devices [5]. Highlighting the effects of breakthroughs in power device development and being able to compare the rectifier systems of very different power levels demands for a measure, which can be found by the power density, which describes the output power of a rectifier dependent on its volume.

The era of power electronics started in the late 1890's as Peter Cooper-Hewitt invented an arc lamp working with mercury vapor. He realized soon that it was conducting current only in one direction. In 1902 he filed his first patent for a working mercury arc rectifier [4]. It was continued through inventions such as vacuum tube, ignitron, phanotron, thyratron until the 1950's. Through these first controllable valves it was possible to use phase angle control where the DC voltage could be controlled from zero to its maximum. The first silicon (Si) transistor semiconductor was introduced by the Bell laboratories in 1948. Most of the modern Power Electronics inventions are traceable to this invention. The next breakthrough was also by Bell labs in 1956 inventing the thyristor, which was developed and produced industrial by General Electric in 1958 [1].

Since the beginnings of Power Electronics there was a growing need for higher frequency switching devices, since many applications benefit from higher frequencies. In the 1950's the Power Electronics development for aerospace applications created a field, where weight and size reduction were of high importance. Much of this weight is associated with the transformers, inductors or filter capacitors, which can be reduced with increased operating frequencies. Lower volume applications, which need special types or larger sizes of devices, must often wait until the research and development investment can be justified, including support from military or other interested users. Advanced development has been subsidized

by applications were performance or size reduction has a greater significance relative to cost, as in aerospace, naval and military equipment [5].

The trend in Power Electronics has been for a large increase in the power density and the dynamic technological development of the power electronic converters over the last few decades covers the complete cross section of applications and converter types. This trend is summarized in Figure 1.1 [6], where the trend line for industrial systems is differentiated from research only systems (typically, a period of 10 years is needed for the full introduction of a new concept into industry).

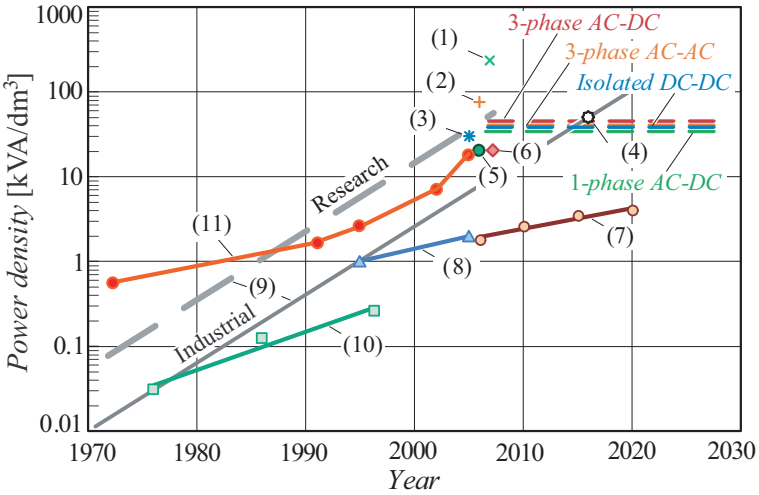


Figure 1.1: Power Density trend of commercial products and research systems [7] and Power Density Barriers as identified in [6]. Without progress in power passives and interconnection technology the barriers would result in the saturation (S-curve shape) of the future power density development of single systems; a further improvement then would have to come from splitting into partial interleaved systems. References: (1) [8]; (2) [9]; (3) [10]; (4) [11]; (5) [12]; (6) [13]; (7) [14]; (8) [15]; (9) [7]; (10) [16]; and, (11) [17].

As seen, Power Electronics industry has a major focus in the miniaturization of power converters, which is mainly driven by cost reduction demands. This means that the same functionality must be guaranteed for electronic systems built within ever smaller spaces, thus requiring electronic components with very much different characteristics to cohabit in

tightly confined areas [6, 18]. The interest and the applications for Power Electronics systems with high switching frequencies has been steadily growing in recent years [6]. This causes a more complex situation because with the steady increase in the switching frequencies, higher frequency components are prone to be observed in the electromagnetic field spectra generated by the power converters.

Aiming for cost reduction, translated into reducing raw materials utilization, more comprehensive and detailed research is being carried out in different places. The results achieved in the last decades have pushed the limits of available circuit topologies, materials, components, modulation schemes and control strategies [19, 20]. These results have also compelled design engineers to achieve a better understanding around the measures to be taken in order to assure the electromagnetic compatibility of such systems within its electrical environment and inside the system itself (self-compatibility) [21]. In this context, the interaction between Electromagnetic Compatibility (EMC) and Power Electronics plays a major role since electronic products must fulfill their respective standards and power converters are usually integrated in these. Due to characteristic trapezoidal-shaped waveforms, power converters generate electromagnetic emissions, which must be carefully evaluated if a given electronic product is to be employed, certified and commercialized in today's global market.

The harmonious cohabitation among electrical equipments and between these and human beings is technically named Electromagnetic Compatibility. In this sense, this discipline is an ecological one, which is ever more important due to increasing use of electric equipments and high frequency electronics in human activities. It is then clear that Power Electronics and its converters must be analyzed from an Electromagnetic Compatibility perspective.

Electromagnetic Compatibility as a technical field arises from the investigation of electromagnetic phenomena that has caused or might come to cause interference, either with electronic equipments or with human beings. In practice, the results of investigation in EMC has led international bodies to establish regulations, in the form of standards, which specify quality requirements for the equipments as well as test procedures and instruments. The aim of such standards is to ensure interoperability, repeatability and to achieve testing conditions that are close to the typical application.

The most internationally recognized standardization body is the In-

ternational Electrotechnical Commission – IEC. It was set up in the beginning of the XX century to deal with flourishing new electrical technologies [22]. It has now more than two hundred technical comities and working groups that work in more than 40 countries. The documents created by its comities are international and represent recommendations, thus not being mandatory. From that, they are named standards rather than legal rules. The standards are written based on voluntary consensus with the objective of setting guidelines for quality and interoperability.

Furthermore, the EMC problem is governed by Maxwell's equations in an environment that has at least two subjects, at least one electrical equipment and other electrical equipment(s) or human being(s). The complete solution of Maxwell's equations for all possible interactions is most probably not economical nor simple. Besides, there should be some level of electromagnetic fields that is able to disrupt the proper operation of the system. With this focus, EMC has been defined in [23] as

> "... a balance between the desired technical performance, the economic constraints of achieving this performance in production and operation, and the acceptability of the above constraints to the, generally non-technical, customer."

For these reasons, Electromagnetic Compatibility standardization bodies build their standards in a way to achieve EMC in a realistic and economical way.

There are international standards in all sub-fields of Electromagnetic Compatibility. These sub-fields are represented in Figure 1.2 in the form of different requirements that an electrical equipment must fulfill [24, 25]. Two major sub-fields are observed, emission and immunity. Emission is related to the electromagnetic fields generated in an equipment, which are guided through conductors (conducted emission) or air (radiated emission) and that potentially generate electromagnetic interference (EMI). Immunity is the ability of an equipment to correctly operate when submitted to electromagnetic fields, either conducted or radiated.

The high levels of switched currents and voltages are, perhaps, the main characteristic of a power converter. Due to this characteristic, power converters are known to generate high conducted emission (CE) levels [21] and this requires that a large effort is put into the proper control of these emissions in order to achieve electromagnetic compatibility. Nowadays,

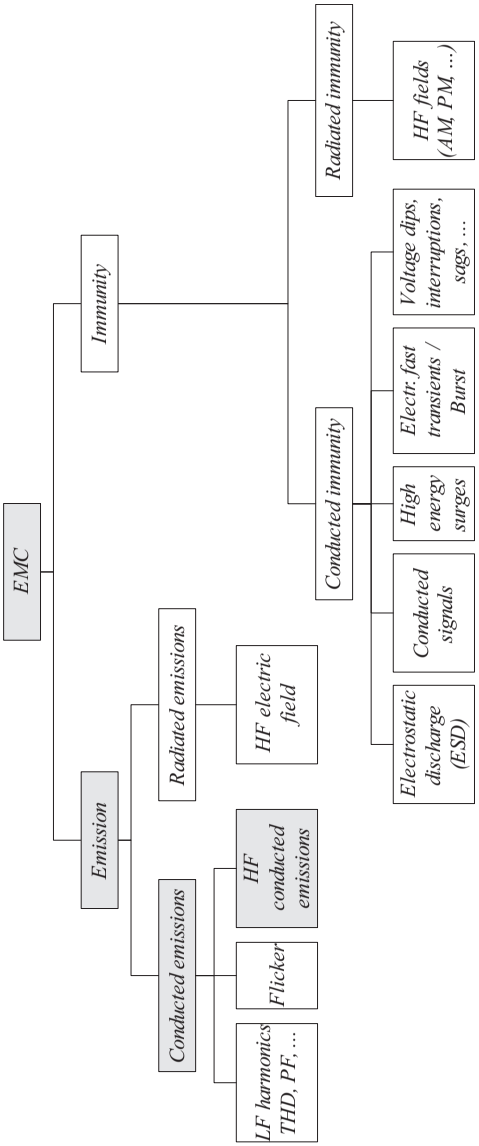


Figure 1.2: EMC requirements with sub-divisions in hierarchic placement. Highlighted are the fields that are in the scope of this work.

the frequencies employed in the carrier signals of typical power converters range from hundreds of Hz, for large power, up to some MHz, for some DC-DC converters. These frequencies, or their relevant harmonic components, lay in the ranges specified in the most referenced standards of the world for conducted emissions. With this, a large amount of the effort to construct a power converter is put into reducing the conducted emissions that propagate to the environment where the converter is placed. Although many research efforts have been put on the study of modulation schemes that lower emissions [26–31], the high frequency emissions are typically not much influenced by these techniques. Another focus of research has been on soft-switching techniques [32–38], which effectively reduce commutation speeds, thus acting only at very high frequencies and, typically, not reducing conducted emissions in large amount. All these techniques, in practice, do not avoid the necessity of employing filtering circuits, which effectively limit the propagation of electrical noise across the interconnections of the power converter to its supply or load.

Differently from radiated emissions, which are typically reduced and controlled by deployment of good layout techniques and shielding, the conducted emissions from power converters are not easily reduced [21] and, in general, there is no alternative to filtering. Filters, although essential, add cost and volume to a power converter and, thus, must be carefully designed. The extra costs and volume of EMC filters motivate the present work, which is therefore focused in providing means for the reduction of HF conducted emissions as highlighted in Figure 1.2.

Although it is still common practice to design EMC filters with try-and-error methods, more and more works [39–46] have proposed filter design procedures for application with power converters. These works typically propose filter designs that separate the EMC filters into differential mode filters and common mode ones, with reference to the configuration of the noise propagation paths. This separation allows for simpler procedures, taking advantage from the very diverse nature of the noise modes.

Further tasks in the design of EMC filters are:

i. The definition of the environment to which the equipment must be compatible. This is typically given by the electrical installation practices where the equipment is commercialized and the testing setups as specified by EMC standards.

ii. The evaluation of the attenuation that the filter must present. This

task requires knowledge about the amount of noise and characteristics of the power converter as a noise source, as well as about the EMC standards to which the equipment must comply.

iii. A filter topology/type must be chosen. This is dependent on cost and restrictions on physical dimensions, as well as in the required filtering performance.

iv. The design and/or selection of components for the chosen topology, so that it achieves the required performance. This includes not only the required emission attenuation levels, but also parameters like efficiency, thermal constraints, mechanical dimensions, reactive energy consumption, damping of resonances, reliability and electrical safety issues, among others.

v. Experimental evaluation of the achieved system performance as specified in EMC standards.

The listed tasks are discussed in this work, restricting the scope of the performed studies to EMC filters connected between three-phase PWM converters and the three-phase public mains.

1.2 Modern Three-Phase PWM Converters

High power applications like adjustable-speeds drive, uninterruptible power supplies, HVDC systems, process technology such as welding and chemical processes, battery charging for electric vehicles, power supplies for telecommunication systems, auxiliary power supplies, future More Electric Aircraft and others, require three-phase conversion of electric energy. Limiting the analysis scope to three-phase converters connected to the public mains, i.e. three-phase ac-dc converters (rectifiers) and three-phase ac-ac converters (cycloconverters and matrix converters), leads to a discussion about the quality of the input currents. Concerns with energy saving and power quality are the main reasons for standards such as IEEE-519 [47] and IEC-1000-3-2 [48], which stipulate limits for power factor and harmonic distortion for installation and equipments connected to the low-voltage energy distribution networks.

Regarding three-phase converters with low impact on the mains, Power Electronics presents basically two alternatives to these tasks: (*i*) three-

phase multi-pulse power converters, relying on passive techniques, diodes, thyristors and alike; or, (*ii*) high switching frequency three-phase PWM converters. Three-phase multi-pulse converters, for operation in the public mains, i.e., for a mains frequency of 50/60 Hz, show considerably higher volume and weight than active rectifier systems of equal power [49]. Three-phase PWM converters allow a higher controllability of the electric parameters. However, the structure of the power and control circuits is typically more complex [49, 50]. The necessity of low current distortion / high power factor and the advantage of higher power density has driven the development of modern three-phase power converters as well as of passive filters, active power filters and hybrid filters. Three-phase PWM converters are characterized by a controlled output voltage and a well controlled sinusoidal shape of the input currents and, thus, are very well suited for this application [51, 52].

Furthermore, three-phase PWM converters have increased their share in the market due to clear advantages [53] over other technologies, namely: (*i*) very high efficiency; (*ii*) robustness to mains transients; (*iii*) high power factor; (*iv*) wide range of output frequencies; (*v*) small dimensions; (*vi*) ride-through capability; (*vii*) regeneration; (*viii*) ease of implementing protection circuits, and (*ix*) excellent control features. On the other hand, PWM converters present some side effects mainly due to the pulsed waveforms with rich spectral contents and very fast transient times [54]. Thus, they typically require input filters to comply with EMC requirements.

Regarding three-phase inverters, specifically adjustable speed drives (ASDs), many research efforts have been performed leading to a vast literature [54–72] on the EMC-oriented modeling and filter design aspects for such systems. The studied systems typically comprise, as front-end converter, three-phase diode bridges (cf. Figure 1.3) or three-phase two-level boost-type rectifiers (cf. Figure 1.4) when power factor correction and regeneration are required. Thus, technical analysis on three-phase two-level boost-type rectifiers has also been performed [25, 73–76].

Even though EMC oriented modeling has been thoroughly researched for the aforementioned converters, the literature on filtering and EMC oriented modeling of more modern PWM converters still lacks. For instance, three-level boost-type rectifiers (cf. Figure 1.5 and Figure 1.6) have been proposed in the literature [77, 78] for more than a decade and there are already several applications into commercially available equipments [79],

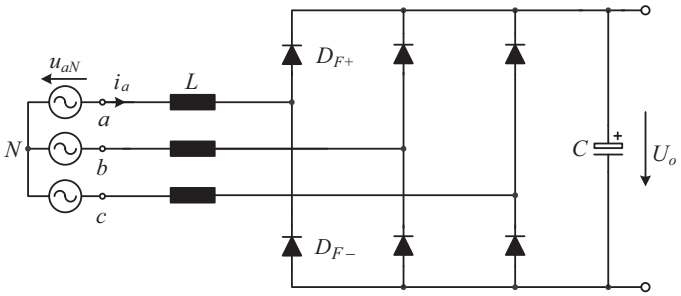


Figure 1.3: Structure of the power circuit of a three-phase diode bridge rectifier.

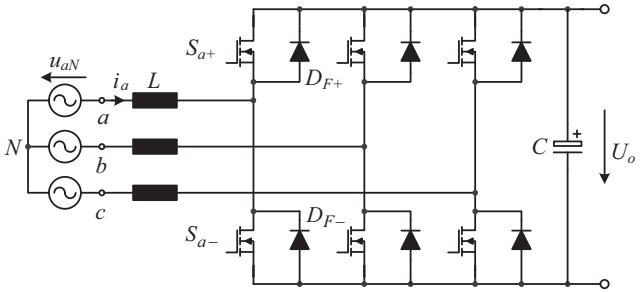


Figure 1.4: Structure of the power circuit of a three-phase two-level boost-type rectifier.

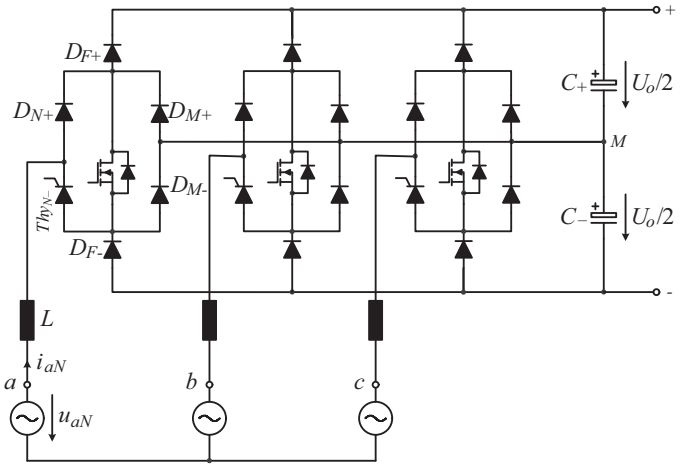


Figure 1.5: Circuit schematic of a three-phase/-switch, three-level boost-type rectifier [77].

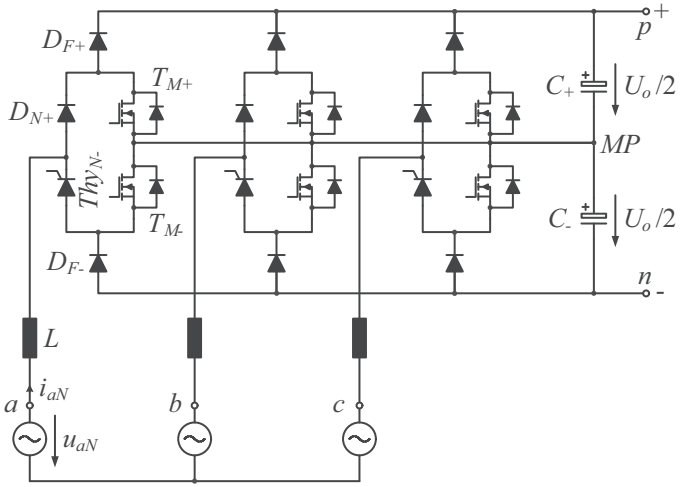


Figure 1.6: Circuit schematic of a three-phase, six-switch, three-level boost-type rectifier [78].

however have not been specifically treated in the literature regarding filtering for the fulfillment of EMC standards. This type of PWM converter finds increasing interest due to the following advantages: possibility of employing switches with reduced rated voltages, thus, lowering switching losses and increasing efficiency; reduced input inductor due to the lower voltage steps applied to these inductors, and; high controllability of the input currents. Nevertheless, these converters present high common mode voltages, which shall be properly attenuated for achieving EMC.

Other modern rectifier topologies with increasing industry application interest are the three-phase three-switch buck PWM rectifier [80, 81] and the three-phase three-switch buck PWM rectifier with integrated boost output stage [82]. The three-phase three-switch buck PWM rectifier is shown in Figure 1.7 and presents the possibility of obtaining an output voltage lower the the input voltage peak, while maintaining input currents with very high quality as main characteristic. The necessity of controlling the output voltage in an extended range, while keeping low distortion of the input currents can be fulfilled with the three-phase three-switch buck PWM rectifier with integrated boost output stage as depicted in Figure 1.8. It is observed that filtering and EMC aspects for both of these topologies has not been thoroughly researched as well. Even though the discontinuous input currents require differential mode filters with high attenuation.

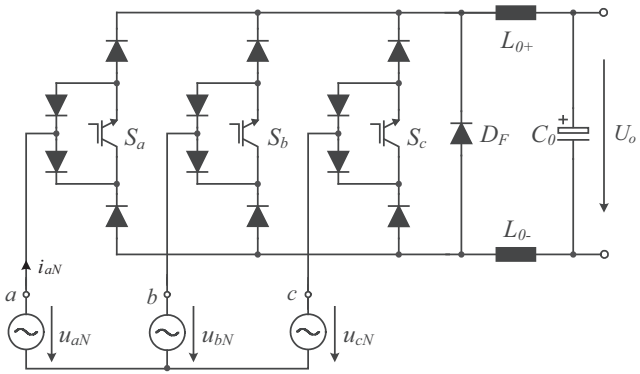


Figure 1.7: Structure of the power circuit of a three-phase three-switch buck PWM rectifier [80, 81].

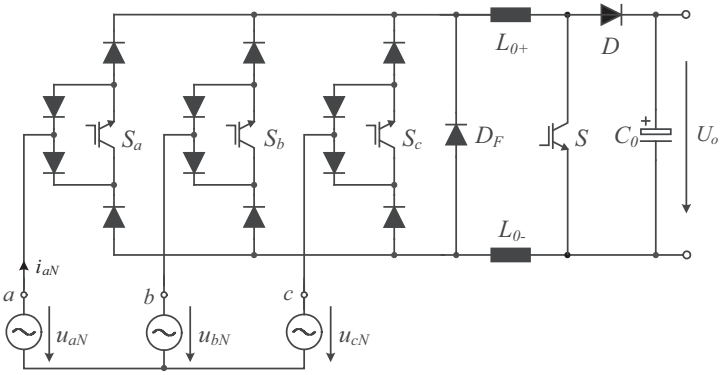


Figure 1.8: Structure of the power circuit of a three-phase three-switch buck PWM rectifier with integrated boost output stage [82].

Finally, even though matrix converters have already been integrated into commercial products [83], they have not received much attention in the research on EMC. In special Indirect and Sparse Matrix Converters [84–88] have been broadly researched in the last years due to their capability of simultaneously providing three-phase voltage amplitude and frequency transformation, while only requiring small filter components compared to conventional two-stage ac-dc-ac conversion from the back-to-back connection of voltage dc-link PWM converters, from where high efficiencies and smaller overall volumes are expected [50]. Nevertheless, very few technical papers have specifically addressed the challenges from an EMC perspective.

A timely necessity to address the challenges posed from the perspective of HF conducted emissions of the discussed modern three-phase PWM converter systems has, thus, motivated this work.

1.3 Description of the Task and Overview of the Work

The main task of this work is to enable the fulfillment of EMC standards (HF conducted emission) for systems which employ modern three-phase PWM converters. As a final goal, the computer aided design of EMC fil-

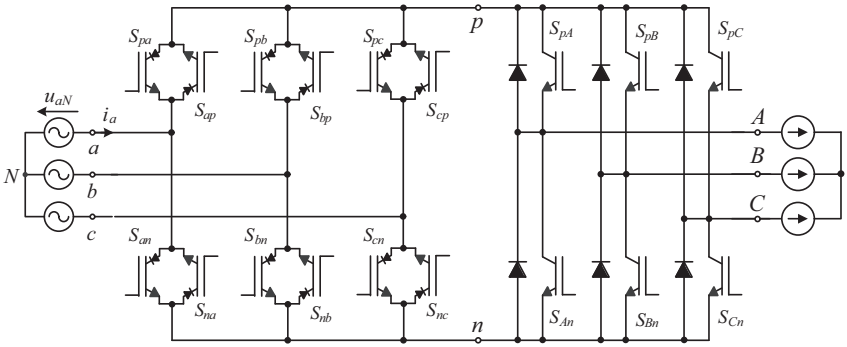


Figure 1.9: Circuit schematic of a three-phase RB-IGBT based Indirect Matrix Converter [89].

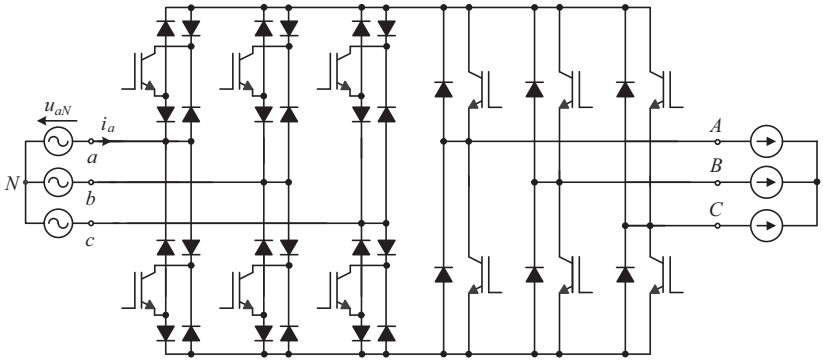
ters for such systems shall be implemented. With this, a step towards the virtual prototyping of the systems is given, which enables Power Electronics engineers to efficiently design electromagnetically compatible systems.

This task starts in Chapter 2 with the study and modeling of the environment where these systems are applied and tested. With this objective, international EMC standards are taken and their requirements are identified, the characteristics of conducted emission testing setups are modeled, electrical installation practices are discussed, safety standards are identified as presenting major requirements for EMC filters and typical loads and interconnection cables are modeled. A model of the conducted emission measurement chain is proposed, which allows for an early computation of the emission levels.

Three-phase PWM converters are modeled as noise sources in Chapter 3. The modeled converters comprise a Three-Phase Buck-Boost PWM Rectifier, Three-Phase Three-Level Boost PWM Rectifiers, and Three-Phase Sparse Matrix Converters. Different modeling techniques are employed, including simplified equivalent circuits which are able to provide trustful information for the design of EMC filters.

A review of models of passive components to be applied into EMC filters is performed in Chapter 4. A study of the volume of typical filter components is performed aiming for later minimization of overall filter volume. Regarding three-phase common mode inductors, a detailed model is presented, a method for the selection of the material for minimized volume

Very Sparse Matrix Converter



Ultra Sparse Matrix Converter

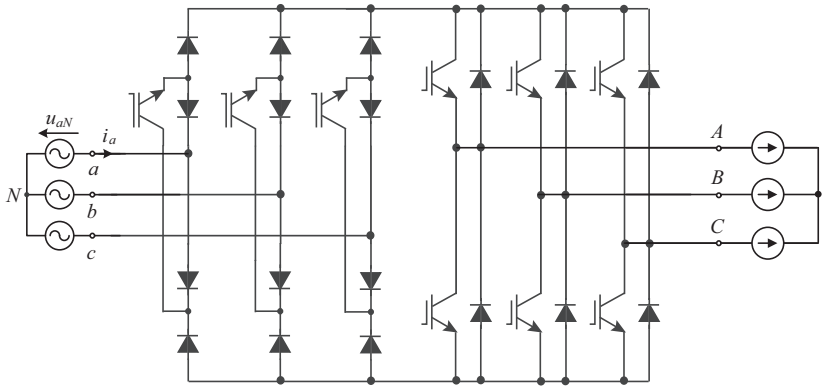


Figure 1.10: Circuit schematics of three-phase Sparse Matrix Converter topologies [88].

inductors is proposed. This chapter also reviews self-parasitic cancellation techniques, where capacitance cancellation networks for three-phase filters are proposed and the influence of parasitic effects is analyzed in detail.

Since more rational design of EMC filters takes into consideration the nature of the noise modes, Common (CM) and Differential Mode (DM), it is highly important to precisely qualify and quantify them. The separation of the noise modes in three-phase systems is analyzed in Chapter 5. Novel types of CM/DM separation networks are analyzed, which can be directly integrated into standard conducted emission test setups. This aims in facilitating the design and troubleshooting of filters for three-phase electronic equipments.

Differential mode filters are designed in Chapter 6, where design procedures are presented exemplary for Three-Phase Three-Level Boost PWM Rectifiers and Three-Phase Sparse Matrix Converters. A review on analytical methods for the computation of attenuation and impedances of the filters is done, as well as on damping of the DM filters. The advantages of multi-stage filtering are explored regarding attenuation, size and damping. A systematic procedure for the design of the DM input filter, which is based on a detailed modeling of a typical conducted emission measurement system, is presented and analyzed. Furthermore, an algorithm for the design of DM inductors is presented, which enables the computer aided design of DM filters. A volumetric optimization of the DM filter for a Three-Phase Three-Level Boost PWM Rectifier is presented, which is extended to a DM filter design algorithm that implements a minimum volume computer aided design of DM filters. The presented procedure avoids the necessity of using numerical optimization routines and allows for the analytical calculation of the filter components.

Chapter 7 describes different design procedures for CM filters for three-phase PWM converters. A common mode filter for a three-phase PWM rectifier is designed based on the parametrization of equivalent circuits by simple impedance measurements on an existing converter prototype and on a capacitive connection between the star-point of the DM input filter capacitors and the output capacitor. This chapter also proposes an implementation strategy for an HF amplifier based active CM filter for off-line converter systems. For such a system the low frequency attenuation in the feedback loop is of high importance in order to prevent amplifier saturation. However, this limits the filter's operating frequency range. Thus, critical issues and advantages for the selected approach are

identified and general requirements for a HF power amplifier to be used in active filtering are derived. Finally, a design procedure for the CM filters to be employed with a three-phase rectifier is presented, where a volumetric optimization is carried out taking into consideration different aspects related to the subject, such as electrical safety and an optimized design of the CM inductors. The design of the CM inductors is presented, which is implemented in an algorithm for the iterative search of the smallest core which simultaneously fulfills magnetic flux restrictions, minimum impedance requirement and thermal limitations.

The experimental verification for the analyzed filters demonstrate that the finally achieved HF attenuation is not only a function of the filter components themselves, but is highly dependent on the interactions between them, between them and the power section of the converters and respective interconnections. Thus, the influence of electromagnetic coupling effects are discussed in Chapter 8. A review on the existing literature on this subject is done and issues that are particular to three-phase filters studied. Practical measures to hinder coupling effects are presented, where an arrangement that reduces the effects of the equivalent series inductances for DM capacitors employed in a filter stage is proposed. Winding methods that reduce leakage inductance and/or external magnetic coupling are introduced. Finally, a study based on experimental results illustrates some of the main effects of couplings and discusses ways to improve them.

Chapter 9 discusses the increase in power density in the last decades. It is identified that this is one of the main objectives of the Power Electronics industry. Based on that, the impact of the EMC filters in the overall volume of three-phase PWM converters has been studied for converters in the range of 5 kW to 10 kW. An analytical procedure based on the volume minimization of the EMC filters is proposed to estimate the total filter volume as function of the converters' rated power and switching frequency. A discussion about the limits of power density for the considered three-phase PWM converters for state-of-the-art power semiconductors is done and optimum switching frequencies are identified. An experimental verification is carried on which validates the achieved results.

1.3.1 Publications

The results achieved during the course of this doctoral work have been published in international conferences and journals as listed below.

Publications Related to this Dissertation

This first list, enumerates the technical papers which have been directly related to the main topic of doctoral research.

1. Heldwein, M.L.; Kolar, J.W., *Winding Capacitance Cancellation for Three-Phase EMC Input Filters.* Accepted for publications in the IEEE Transactions on Power Electronics, July 2008.
2. Kolar, J.W.; Drofenik, U.; Biela, J.; Heldwein, M.L.; Ertl, H.; Friedli, T.; Round, S., *PWM Converter Power Density Barriers.* IEEJ Transactions on Industry Applications, v. 128-D, pp. 468-480, 2008.
3. ROUND, S.; Karutz, P.; Heldwein, M.L.; Kolar, J.W., *Towards a 30 kW/liter, Three-Phase Unity Power Factor Rectifier.* IEEJ Transactions on Industry Applications, v. 128-D, pp. 481-490, 2008.
4. ROUND, S.; Schafmeister, F.; Heldwein, M.L.; Pereira, E.; Serpa, L.; Kolar, J.W., *Comparison of Performance and Realization Effort of a Very Sparse Matrix Converter to a Voltage DC Link PWM Inverter with Active Front End.* IEEJ Transactions of the Institute of Electrical Engineers of Japan, v. 126-D, pp. 578-588, 2006.
5. Nussbaumer, T.; Heldwein, M.L.; Kolar, J.W., *Differential Mode Input Filter Design for a Three-Phase Buck-Type PWM Rectifier Based on Modeling of the EMC Test Receiver.* IEEE Transactions on Industrial Electronics, v. 53, pp. 1649-1661, 2006.
6. Karutz, P.; ROUND, S.; Heldwein, M.L.; Kolar, J.W., *Ultra Compact Three-phase PWM Rectifier.* In: 22nd IEEE Applied Power Electronics Conference, 2007, Anaheim (CA). Proceedings of the 22nd IEEE Applied Power Electronics Conference, 2007. v. 1. pp. 816-822.
7. Kolar, J.W.; Drofenik, U.; Biela, J.; Heldwein, M.L.; Ertl, H.; Friedli, T.; Round, S., *PWM Converter Power Density Barriers.* In: 4th Power Conversion Conference (PCC'07), 2007, Nagoya. Proceedings of the 4th Power Conversion Conference. v. CD-ROM.
8. Muesing, A.; Heldwein, M.L.; Friedli, T.; Kolar, J.W., *Steps Towards Prediction of Conducted Emission Levels of an RB-IGBT Indirect Matrix Converter.* In: 4th Power Conversion Conference (PCC'07), 2007, Nagoya. Proceedings of the 4th Power Conversion Conference, 2007. v. CD-ROM.
9. Round, S.; Karutz, P.; Heldwein, M.L.; Kolar, J.W., *Towards a 30 kW/liter, Three-Phase Unity Power Factor Rectifier.* In: 4th Power Conversion Conference (PCC'07), 2007, Nagoya. Proceedings of the 4th Power Conversion Conference, 2007. v. CD-ROM.

10. Heldwein, M.L.; Kolar, J.W., *Extending Winding Capacitance Cancellation to Three-Phase Power Filter Networks.* In: IEEE EMC Symposium 2007, 2007, Honolulu, HI. Proceedings of the IEEE EMC Symposium 2007, 2007.

11. Heldwein, M.L.; Kolar, J.W., *Design of Minimum Volume Input Filters for an Ultra Compact Three-Phase PWM Rectifier.* In: COBEP'07 - Congresso Brasileiro de Eletrônica de Potência, 2007, Blumenau. Proceedings of the 9th Brazilian Power Electronics Conference (COBEP'07), 2007. v. CD-ROM.

12. Nussbaumer, T.; Heldwein, M.L.; Kolar, J.W., *Common Mode EMC Input Filter Design for a Three-Phase Buck-Type PWM Rectifier System.* In: 21st Annual IEEE Applied Power Electronics Conference and Exposition, 2006, Dallas (TX). Proceedings of the 21st Annual IEEE Applied Power Electronics Conference and Exposition, 2006. v. 3. pp. 1617-1623.

13. Biela, J.; Wirthmueller, A.; Waespe, R.; Heldwein, M.L.; Waffenschmidt, E.; Kolar, J.W., *Passive and Active Hybrid Integrated EMI FIlters.* In: 21st Annual IEEE Applied Power Electronics Conference and Exposition, 2006, Dallas (TX). Proceedings of the 21st Annual IEEE Applied Power Electronics Conference and Exposition, 2006. v. 2. pp. 1174-1180.

14. Heldwein, M.L.; Ertl, H.; Biela, J.; Kolar, J.W., *Implementation of a Transformer-Less Common Mode Active Filter for Off-Line Converter Systems.* In: 21st Annual IEEE Applied Power Electronics Conference and Exposition, 2006, Dallas (TX). Proceedings of the 21st Annual IEEE Applied Power Electronics Conference and Exposition, 2006. v. 2. pp. 1230-1236.

15. Heldwein, M.L.; Nussbaumer, T.; Beck, F.; Kolar, J.W., *Novel Three-Phase CM/DM Conducted Emissions Separator.* In: 20th Annual IEEE Applied Power Electronics Conference and Exposition, 2005, Austin (TX). Proceedings of the 20th Annual IEEE Applied Power Electronics Conference and Exposition, 2005. v. 2. pp. 797-802.

16. ROUND, S.; Schafmeister, F.; Heldwein, M.L.; PEREIRA, E.; SERPA, L.; Kolar, J.W., *Comparison of Performance and Realization Effort of a Very Sparse Matrix Converter to a Voltage DC Link PWM Inverter with Active Front End.* In: 2005 IEEE Industry Applications Conference, 2005, Hong Kong. Conference Record of the 2005 IEEE Industry Applications Conference, 40th IAS Annual Meeting (IAS'05), 2005.

17. Heldwein, M.L.; Nussbaumer, T.; Kolar, J.W., *Differential Mode EMC Input Filter Design for Three-Phase AC-DC-AC Sparse Matrix PWM Converters.* In: 35th IEEE Power Electronics Specialists Conference, 2004, Aachen. Proceedings of the 35th IEEE Power Electronics Specialists Conference, 2004.

18. Nussbaumer, T.; Heldwein, M.L.; Kolar, J.W., *Differential Mode EMC Input Filter Design for a Three-Phase Buck-Type Unity Power Factor PWM*

Rectifier. In: 4th International Power Electronics and Motion Control Conference, 2004, Xian. Proceedings of the 4th International Power Electronics and Motion Control Conference, 2004. v. 3. pp. 1521-1526.

Further Publications

The following works have been also carried out during the doctoral studies at the ETH Zurich. However, these are not directly linked to this dissertation.

1. Nussbaumer, T.; Gong, G.; Heldwein, M.L.; Kolar, J.W., *Modeling and Robust Control of a Three-Phase Buck+Boost PWM Rectifier (VRX-4)*. IEEE Transactions on Industry Applications, v. 44, pp. 650-662, 2008.
2. Nussbaumer, T.; Heldwein, M.L.; Gong, G.; Round, S.; Kolar, J.W., *Comparison of Prediction Techniques to Compensate Time Delays Caused by Digital Control of a Three-Phase Buck-Type PWM Rectifier System*. IEEE Transactions on Industrial Electronics, v. 55, pp. 791-799, 2008.
3. Gong, G.; Heldwein, M.L.; Drofenik, U.; Kolar, J.W., *Comparative Evaluation of Three-Phase High-Power-Factor AC-DC Converter Concepts for Application in Future More Electric Aircraft*. IEEE Transactions on Industrial Electronics, v. 52, pp. 727-737, 2005.
4. Friedli, T.; Heldwein, M.L.; Giezendanner, F.; Kolar, J.W., *A High Efficiency Indirect Matrix Converter Utilizing RB-IGBTs*. In: 37th Power Electronics Specialists Conference, 2006, Jeju. Proceedings of the 37th Power Electronics Specialists Conference, 2006.
5. Mino, K.; Heldwein, M.L.; Kolar, J.W., *Ultra Compact Three-Phase Rectifier with Electronic Smoothing Inductor*. In: 20th Annual IEEE Applied Power Electronics Conference and Exposition, 2005, Austin (TX). Proceedings of the 20th Annual IEEE Applied Power Electronics Conference and Exposition, 2005. v. 1. pp. 522-528.
6. Nussbaumer, T.; Heldwein, M.L.; Gong, G.; Kolar, J.W., *Prediction Techniques Compensating Delay Times Caused by Digital Control of a Three-Phase Buck-Type PWM Rectifier System*. In: 4th International Power Electronics and Motion Control Conference, 2005, Hong Kong. Conference Record of the 2005 IEEE Industry Applications Conference, 40th IAS Annual Meeting (IAS'05), 2005.
7. Nussbaumer, T.; Gong, G.; Heldwein, M.L.; Kolar, J.W., *Control-Oriented Modeling and Robust Control of a Three-Phase Buck+Boost PWM Rectifier (VRX-4)*. In: 2005 IEEE Industry Applications Conference, 2005, Hong

Kong. Conference Record of the 2005 IEEE Industry Applications Conference, 40th IAS Annual Meeting (IAS'05), 2005.

8. Round, S.; Heldwein, M.L.; Kolar, J.W.; Hofsajer, I.; Friedrichs, P., *A SiC JFET Driver for a 5 kW, 150 kHz Three-Phase Sinusoidal-Input, Sinusoidal-Output PWM Converter.* In: 2005 IEEE Industry Applications Conference, 40th IAS Annual Meeting (IAS'05), 2005, Hong Kong. Conference Record of the 2005 IEEE Industry Applications Conference, 40th IAS Annual Meeting (IAS'05), 2005. v. CD ROM.

9. Heldwein, M.L.; Kolar, J.W., *A Novel SiC J-FET Gate Drive Circuit for Sparse Matrix Converter Applications.* In: 19th Annual IEEE Applied Power Electronics Conference and Exposition, 2004, Anaheim (CA). Proceedings of the 19th Annual IEEE Applied Power Electronics Conference and Exposition, 2004. v. 1. pp. 116-121.

10. Gong, G.; Heldwein, M.L.; Drofenik, U.; Mino, K.; Kolar, J.W., *Comparative Evaluation of Three-Phase High Power Factor AC-DC Converter Concepts for Application in Future More Electric Aircrafts.* In: 19th Annual IEEE Applied Power Electronics Conference and Exposition, 2004, Anaheim (CA). Proceedings of the 19th Annual IEEE Applied Power Electronics Conference and Exposition, 2004. v. 2. pp. 1152-1159.

Chapter 2

Conducted Emissions Environment Modeling

"Without an environment there would be no behavior at all, regardless of what genes were present." David C. Funder

2.1 Introduction

Depending on the coupling path between a noise source and a receiver/victim electromagnetic emissions are divided into radiated and conducted ones. Conducted emissions, as the name suggests, regard the emissions which are guided directly through electric conductors. These emissions flow through the components which are drawn in electrical circuit schematics, but also flow, unintentionally, through parasitic elements [24], like capacitances to ground, stray inductances, etc. Unlike radiated emissions, conducted ones are typically very difficult to avoid only through shielding and good layout practices, thus filters are usually employed to control them. Deep knowledge about the electrical environment is essential to efficiently design filters and provide the required control of these emissions. The objective of this chapter is to present mathematical models of the electrical environment typically surrounding a three-phase PWM converter. These models shall assist the design of filtering circuits for three-phase PWM converters and convey insight concerning noise propa-

gation paths.

Filters are designed so that equipment can be electromagnetically compliant [24, 39]. In practice, that is translated into controlling intra-system interference or other customer specific requirements and the fulfillment of relevant EMC standards, which specify quality levels, testing conditions, procedures and test equipments. Thus, a complete understanding of the relevant standards is required.

The electrical equipments which are in the scope of this work are to be installed in low voltage (LV) power supply systems. It is of high importance to know how these systems are configured in order to properly connect EMC filters. Above all, this is the environment where an electrical equipment operates and conducted emissions flow. A standard conducted emissions testing setup is based on usual electrical installation practices. In general, EMC standards try to define test setups which are as close as possible to the actual installation. What finally varies depending on the specific installation are the inherent impedances. Knowledge on these impedances is crucial for a successful filter design.

Another very important information regards the electrical safety standards [90, 91] that are to be observed. Among others, these standards specify the types of components, insulation practices and the amount of allowable earth leakage currents in the installation system. All these aspects have direct or indirect influence on the design and construction of an EMC filter.

All the above mentioned requirements and installation practices might vary in a large extent depending on region and application. Thus, it is strongly recommended that a study on the relevant practices, norms and standards is done prior to any filter design. Vast literature is available on these subjects and the basic notions and practices are summarized in the following sections.

From all different installation and application options, it is clear that, depending on the aimed installation practice and relevant EMC standard, the connections of an EMC input filter may vary. Even though most of the principles here presented are generally valid, the filters design procedures of this work are limited to the general practices adopted in Europe, which are specified within the respective chapters and sections.

Regarding conducted emissions requirements, EMC standards specify with details how the testing conditions and procedures shall take place.

The main objectives are to ensure interoperability, repeatability and to achieve testing conditions that are close to usual application.

EMC standards also specify the requirements for the measurement equipments which evaluate conducted emission (CE) levels. From these specifications, mathematical models of the testing equipments can be derived providing important information for successfully designing filters.

Other system parts of high importance for the modeling of propagation paths in the conducted emissions environment are:

- input and output cables, type and their disposition with respect to large earthed structures;
- loads – resistance, power converter, electrical machines;
- communication ports;
- required earthing points.

The International Electrotechnical Commission (IEC) standard requirements for conducted interference are more stringent for the mains ports than for other ports. In [92] it is stated that:

> "Conducted interference can be classified according to whether it is coupled via the mains port or via signal ports. The vast majority of CISPR and IEC based standards require testing of all phenomena on the mains port: many require immunity testing on signal ports and more tests are being proposed. CISPR 22, for instance, now requires conducted RF emissions testing on telecommunications ports.".

For this reason, communication ports are not modeled in this work. This assumes that these ports are properly insulated in the studied power electronics systems.

The modeling of power cables and earth connections is highly important to predict high and low frequency currents. Loads might define the system behavior for very low frequencies, but define HF currents as well. Thus, knowledge about all system components is typically essential. In the subsequent sections, models for the standard test setups for conducted emissions evaluation are presented. These models are subdivided according to the parts of the system to be modeled, e.g. mains impedance, test equipments, cables, machines and general loads.

2.2 Basics on Low Voltage Electricity Supply Systems

Electricity is commercially distributed through a power supply grid, which obeys standardized installation practices. These practices are internationally specified by the IEC, who defines different installation voltage classes regarding safety requirements. These classes are employed in order to determine installation practices, safety rules and other characteristics of the electrical systems and equipments. The IEC voltage classes are divided like in the following [91] classes.

Voltage classes

i. [63] ELV (Extremely low voltage installations and equipment):

- AC voltages (phase to ground) lower than 50 V or DC voltages lower than 120 V in normal indoor conditions;
- Installations with highly conductive parts, inside metallic objects, swimming pools present even lower voltage limits;
- ELV is subdivided in: SELV, PELV and FELV [91].

ii. Class LV (Standard low voltage installations and equipment):

- AC voltages lower in the range from 50 V to 1 kV or DC voltages from 120 V up to 1.5 kV.
- This is the class where this work is focused on.

iii. Class HV (High voltage installations and equipment):

- AC voltages higher than 1 kV or DC voltages above 1.5 kV.

This section intends to present the possible earthing strategies for low voltage (LV) electricity supply [93–97]. The importance of these considerations lies on the fact that the connection of EMC filters to the power grid determines the type of filter connections and configurations that are to be used.

2.2.1 Earthing Practices for Safety

From the IEC 950 [91], the purpose of the electrical safety regulation is to:

> "take all appropriate measures to ensure that electrical equipment may be placed on the market only if, having been constructed in accordance with good engineering practice in safety matters, it does not endanger the safety of persons, domestic animals or property when properly installed and maintained and used in applications for which it was made".

This is usually achieved in an electrical installation through the limitation of potential difference between different equipments. This ensures that ground-current protective devices act properly in case of faults and voltage transients due to atmospheric discharges or switched loads are limited. A third important effect is that phase voltages are balanced. Electric performance can also be enhanced through proper earthing, since low impedance paths are provided for return currents of filters and surge protective devices.

From an equipment point of view, two different earthing strategies can be applied, namely: (*i*) standard ground and (*ii*) insulated ground. Standard ground requires an extra dedicated protective conductor connected in parallel to the metallic parts that connect the equipment to the installation ground. Whereas, insulated ground configuration assumes that the electronic/electric parts are insulated from the equipment's enclosure, which is separately connected to the installation's ground. The earthing strategy causes an obvious impact in the way a power filter should be installed.

Earthing connections create current paths which allow noise signals to flow, and thus, create a problem for EMC engineers. Nevertheless, safety [98] and fault protection are the main reasons for an electrical system to include earthing [99]. Therefore, EMC is not the main concern in earthing standards.

Safety measures aim on reducing the risk of electrical shock to which human beings are exposed. A human body receives an electric shock when it is part of an electrical circuit by touching, intentionally or not, an electrical equipment or being exposed to lightning. The effects of an electric shock vary depending on a number of factors, such as body resistance,

moisture, contact resistance, altitude, temperature, electric frequency and voltage amplitudes. These effects include, in an increasing intensity scale:

i. slight perception of small current levels;

ii. surprise;

iii. reflex action ("let-go current");

iv. movement inhibition;

v. respiratory stop; and

vi. death.

The impact of lower frequencies on the human body is higher due to skin effect and higher impedances. Therefore, the current levels which cause possible damages vary, being lower for DC currents. Electrical safety standards usually specify test setups which estimate the amount of current that would flow in a human body for the case when a person touches the equipment under consideration. This current is named *earth leakage current* and it is illustrated in Figure 2.1. Based on these test setups, maximum earth leakage current levels are specified. The specified levels are usually correlated to a current level that would still not produce a reflex action, meaning that this is the highest current level at which a person releases the conductor stimulated by the shock current itself ("let-go current").

Protective earthing is therefore the practice of connecting every conductive part of an electrical installation to a common ground, commonly named *common bonding network* (CBN), to avoid the risks of unnecessarily exposing conductive parts at high voltage. With this practice, if a failure occurs and high voltage produces currents higher than the regulated ones, breakers act or fuses blow, thus protecting a possible victim. In a electrical diagram, the CBN is formed by interconnecting all metallic parts of a building (structural steel, copper tubes, etc) and the electrical installation to the ground network. The conductors that interconnect the earthing network are named *protective earth* (PE).

In order not to loose generality, product and region specific safety standards are not considered. The IEC issues international electric safety standards [90,91,98,100] which are not legal rules, but are recommended

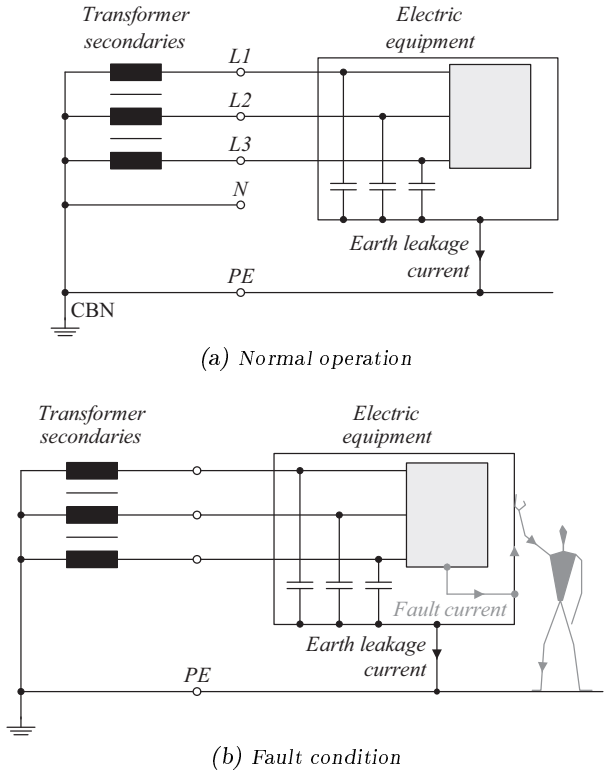


Figure 2.1: Earth leakage currents: (a) normal operation earth current, and; (b) fault condition.

by the United Nations to be adopted in the member countries. The most general requirements from these standards serve as guidelines for this work.

Three classes of equipments are specified in the IEC standards, namely:

i. Class I: equipments with conductive surfaces that might present a hazard. The surfaces shall be connected to PE, and thus, safety depends on these connections;

ii. Class II: equipments with reinforced insulation. These equipments

present no hazardous surfaces to an operator;

iii. Class III: equipments with circuits that have no voltages higher than 42.4 V.

Depending on the equipment class, the earth leakage current levels are different, as defined in Table 2.1 for non-medical equipments. In this work a maximum earth leakage current $I_{leak,max} = 3.5$ mA is assumed unless specified. This takes into account a wide range of industrial equipments making use of Power Electronics converters. This specification has a great impact on the design of CM as is seen in section 7.

Table 2.1: Maximum earth leakage current depending on equipment class for non-medical equipments.

Equipment class	*Specification*	*Maximum current*
Class II	double insulated	0.25 mA
Class I	hand-held equipments	0.75 mA
Class I	movable equipment	3.5 mA
Class I	stationary pluggable	3.5 mA
Class I	stationary, permanently connected	3.5 mA
Class I	stationary, permanently connected with a hazard label	5% of input current

Electrical safety standards specify minimum requirements for insulation in the form of distances between conductive elements presenting potentially hazardous voltage differences. This is of special interest in power filter designs, were line voltages are applied across separated inductors, different windings of CM inductors, across the line capacitors and PCB tracks. While phase voltages are applied through capacitors connected between lines and PE or line to neutral and PCB tracks. Standard IEC 60950 [91] defines the types of insulation, insulation distances and other relevant terms. Five types of insulation are defined, based on circuit function and hazard, in Table 2.2.

Table 2.2: Insulation types as defined in IEC 60950.

Insulation Type	*Definition*
Functional insulation (**F**)	Insulation required for correct operation (no explicit protection against electrical shock
Basic insulation (**B**)	Provides basic protection against shock
Supplementary insulation (**S**)	Additional insulation to **B** in order to reduce risks in case of basic insulation failure
Double insulation (**D**)	It is built with both, **B** and **S** insulation
Reinforced insulation (**R**)	Insulation equivalent to **D**, but built with a single insulation system

These insulation types define the requirements for insulation materials and distances. The way to choose to which insulation type a circuit belongs, depends on if the circuit is a *primary* (connected to the mains) or *secondary* (not connected to a primary circuit) one. A filter is typically directly connected to the mains, so it is a *primary circuit*.

Different insulation requirements are defined as functions of *working voltage*, i.e. the highest voltage applied between two parts. Working voltages are defined differently depending on the objective of the analysis, so that:

- for defining electric strength levels, the working voltage is the DC value of the applied voltage or the peak value of an AC voltage, including overshoots and ringings;
- for clearance distances, the working voltage is the rated AC mains supply voltage, and;
- for creepage distances it is the rated RMS or DC voltage, not considering short-term variations such as transients and damped ringing.

The main insulation requirements, which imply in direct impact to filter installation, components/PCB layout and components construction, are defined as:

- *Clearance distance*: the shortest physical distance, measured through the air, between two conductive parts or between one conductive part and the enclosure of an equipment.
- *Creepage distance*: the shortest physical distance, measured along the insulation surface, between two conductive parts or between one conductive part and the enclosure of an equipment.
- *electric strength test*: test though which a voltage is applied between two conductive parts and the effectiveness of insulation is proved.

Further classification is done regarding the *pollution degree* of the installation. This is according to Table 2.3.

Table 2.3: Pollution degrees as defined in IEC 60950.

Pollution degree	*Definition*
P.D. 1	Components and assemblies that are sealed (exclude moisture and dust
P.D. 2	General equipments
P.D. 3	For internal environments that are subject to conductive pollution or to dry non-conductive pollution that, due expected condensation, could conduct

Standard IEC 60950 specifies insulation requirements according to the cited criteria, so that functional insulation (**F**) is required for primary type circuits [91]. For electric strength test and working voltages the standard specifies that:

- *Working voltage* (peak) $\leq$ 184 V: Functional insulation shall be tested with a RMS voltage of 1 kV.

- 184 V $\leq$ *Working voltage* (peak) $\leq$ 354 V: Functional insulation shall be tested with a RMS voltage of 1.5 kV.

Insulation material types are also classified in IEC 60950 into four groups (I, II, IIIa and IIIb). These groups are divided according to a *comparative tracking index* (CTI). This index says that materials of group I are better insulators than those of group II and so on.

Insulation distances for primary type circuits are specified in Table 2.4 and Table 2.5.

Table 2.4: Clearance distances for functional insulation as defined in IEC 60950 for primary circuits.

Maximum working voltage (RMS) [V]	*Mains* < 150 V *Transients* < 1500 V *Pollution degree* 1 or 2 [mm]	*Pollution degree* 3 [mm]	150 V < *Mains* < 300 V *Transients* < 2500 V *Pollution degree* 1 or 2 [mm]	*Pollution degree* 3 [mm]
50	0.4	0.8	1.0	1.3
150	0.5	0.8	1.4	1.5
300	1.5	1.5	1.5	1.5
600	3.0	3.0	3.0	3.0
1000	4.2	4.2	4.2	4.2

Table 2.5: Creepage distances for functional insulation as defined in IEC 60950 for primary circuits.

RMS voltage (RMS) [V]	*Pollution degree 1* *Material group* I [mm]	II [mm]	III [mm]	*Pollution degree 2* *Material group* I [mm]	II [mm]	III [mm]	*Pollution degree 3* *Material group* I [mm]	II [mm]	III [mm]
50	use same distance from clearance			0.6	0.9	1.2	1.5	1.7	1.9
150				0.8	1.1	1.6	2.0	2.2	2.5
200				1.0	1.4	2.0	2.5	2.8	3.2
300				1.6	2.2	3.2	4.0	4.5	5.0
400				2.0	2.8	4.0	5.0	5.6	6.3

As it can be seen, safety standards requirements have a direct impact in the construction of an EMC filter and, thus, should be studied prior to the filter design and components specification.

2.2.2 LV Earthing Systems as Specified in IEC 60364

The international series of standards on electrical installations and safety IEC-60364 [100] specifies three main earthing systems, namely TN, TT and IT. The basic connections for three-phase LV systems are shown in Figure 2.2 and Figure 2.3

The TN system is divided into three different earthing strategies that are used depending on the aim of the installation and on the place. In this type of system, the secondaries of the distribution transformers are connected in a "Y" configuration (cf. Figure 2.2), but for other types of installations this might vary, depending on region and application [91].

The TN system is characterized by the following:

i. the transformer neutral is earthed;

ii. the frames of the electrical loads are connected to the neutral;

iii. is sub-divided into three parts as in Figure 2.2.

The TT system (Figure 2.3):

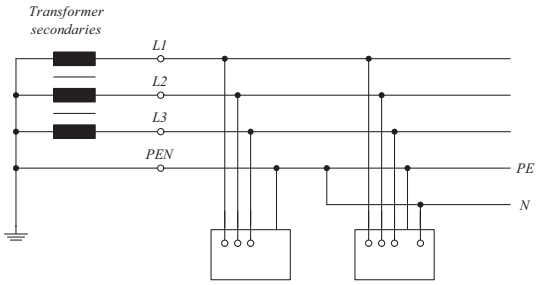
i. the transformer neutral is earthed;

ii. the frames of the electrical loads are also connected to the earth connection.

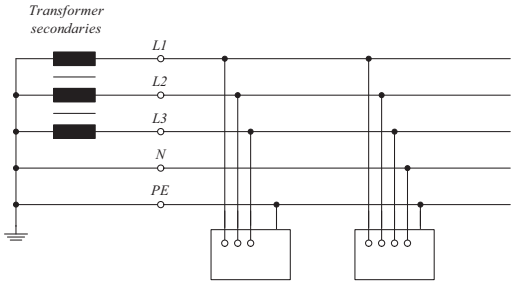
The IT system (Figure 2.3):

i. the transformer neutral is not earthed;

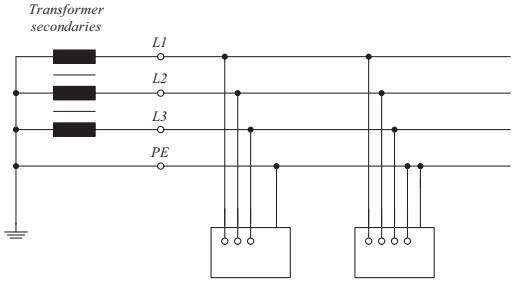
ii. the frames of the electrical loads are connected to the earth.



TN - C - S : Combined Separated Earth - Neutral



TN - S : Separated Earth - Neutral



TN - C : Combined Earth - Neutral

Figure 2.2: International standard IEC 364 basic earthing diagrams for TN configuration.

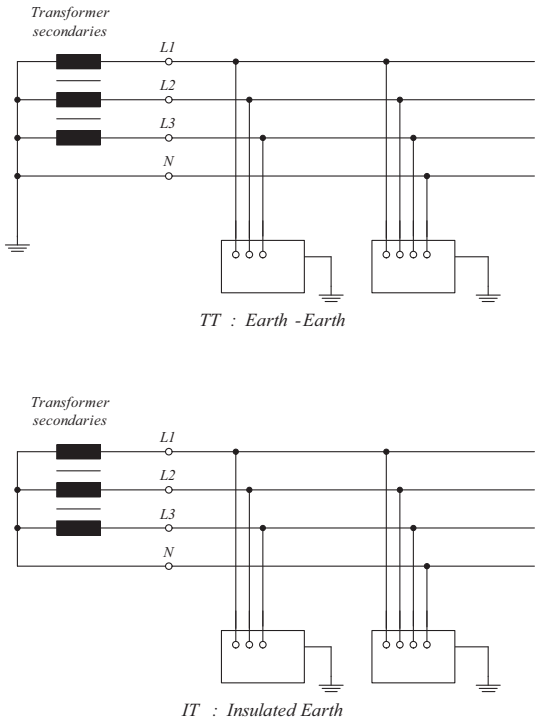


Figure 2.3: International standard IEC 364 basic earthing diagrams for TT and IT configurations.

2.2.3 The LV Earthing Systems in Japan

In order to highlight the possible differences in earthing systems, the Japanese one is introduced here. The earthing systems for low voltage installations in Japan [101, 102] are based on the TT earthing system and the basic configuration is shown in Fig. 2. There is no search for equipotentiality in this earthing strategy. Therefore, local filtering might present more advantages than a system level one. This shows the importance of knowing the characteristics of the distribution system in which the equipment under consideration is applied.

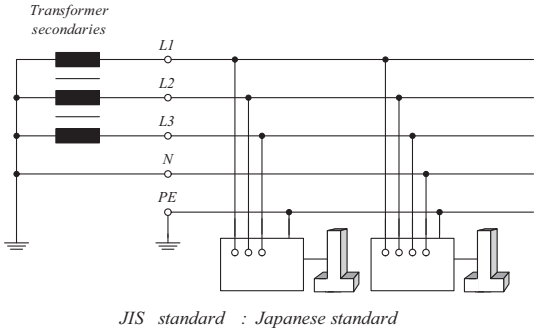


Figure 2.4: Japanese standard (JIS) basic earthing diagram.

It is also common to see in Japan systems where the ground point is not connected to the system neutral, having the earthing connection at the center point of one phase or between two phases in an open-delta configuration. This type of system is built aiming for cost reduction, but presents other requirements for filter components because the voltage from line to ground may be higher.

2.3 Standards for Conducted Emission

2.3.1 International Standards on Conducted Emissions

There are two main reasons for employing EMC input filters, namely:

i. to prevent electromagnetic interference of the considered power electronic converter with electronic systems to be present in the neighboring environment, and;

ii. to avoid a disturbance of the power converter operation by sources of electromagnetic noise in the surrounds [25, 39].

With this aim, international organizations have been constantly working on standards which have to be considered when designing the input filter of any power electronics system. These standards can be divided into civilian and military ones and further sub-divided depending on the aimed application. In this work only civilian standards [103] are considered.

With EMC standards, as for the electrical safety standards, the objective is not to loose generality. Thus, region specific EMC standards are not specifically considered. On the other hand, application specific ones are accounted for while specifying the power converter types. There is a large number of international and national institutions (e.g. CISPR, ANSI, FCC, IEC, IEEE, EIA NBS, RTCA, SAE, VDE and more) which issue standards and regulations in the field of EMC, where the IEC is the most international one.

The IEC was set up in the beginning of the XX century to deal with flourishing new electrical technologies [22]. It has now more than two hundred technical comities and working groups that work in more than 40 countries, including the USA and most of the European countries. The documents created by its comities are international and represent recommendations, thus not being mandatory. From that, they are named standards rather than legal rules. The standards are written based on voluntary consensus. The main objectives of standards is to set guidelines for quality and interoperability. Therefore, standards are the basis of regional regulation so that, in general, country or region specific rules follow them.

In 1934 the IEC, following the early EMC issues generated by the first household radios, has created a specialized committee on radio interference, the *International Special Committee on Radio Interference* – CISPR. This Committee has grown with the years and today covers many sides of EMC, being a major authority in the field and issuing standards that are used worldwide to create regional ones. Keeping a universal focus, unless specified, the EMC standards published by the CISPR are the guidelines for this work.

Some of the publications from CISRP are included in Table 2.6.

Table 2.6: Examples of CISPR standards.

Publication	Scope	Product type
CISPR 11	Limits	Industrial, scientific and medical
CISPR 12	Limits	Ignition systems in vehicles
CISPR 13	Limits	Broadcast receivers
CISPR 14	Limits	Equipments with electrical switching
CISPR 15	Limits	Lightning
CISPR 16	Measurement equipment	
CISPR 18	Limits	High voltage
CISPR 22	Limits	Data processing

There are three levels for the EMC standards published by the IEC, namely:

i. Basic EMC publications: define the involved phenomena, their terminology, safety, characterization of environments, general measuring instructions. These are product independent. An example is the IEC 60000 series.

ii. Generic EMC standards: set the basis for product specific standards and define measurement procedures and equipments. An example is CISPR 16 [104].

iii. EMC standards for family of products: specify the quality and interoperability requirements for specific equipment types or product family. Examples are CISPR 11 [105] and CISPR 22 [106].

The presented order respects an hierarchic frame and, in case a product or product family is not included in a product specific standard, the next superior level generic standard shall be applied.

In the European Union (UE), equipments shall comply with the EU's EMC Directive (EMC Directive 89/336/EEC, published in 2004, but that takes effect on July, 20, 2007) so that can be brought to the EU market. The usual way is to follow an Conformity Assessment as displayed in

Figure 2.5. Similar procedures are found all over the globe. As seen in the figure, the EU has a series of harmonized standards which cover most of the equipments in the market. The majority of EU's directive EMC harmonized standards are directly influenced by the CISPR standards. In case harmonized standards do not exist, a Technical Construction File (TCF) must be constructed as explained in [107].

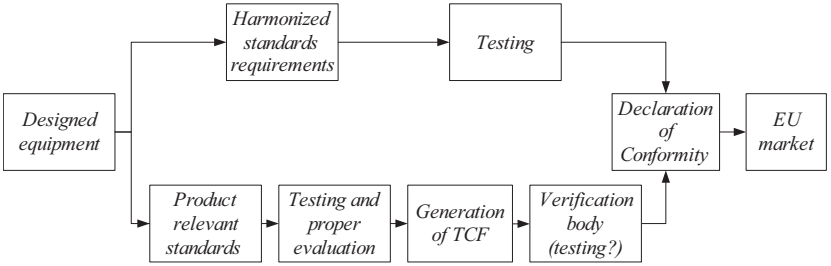


Figure 2.5: Flow diagram showing the paths for conformity assessment within the EU's EMC directive.

For the harmonized standards, the equipments are divided into two classes that depend on the environment where the application of the equipment takes place. This is illustrated in Figure 2.6, where industrial environments are divided into *light industry* and *industry*, where industry is meant for industrial environments where the power is supplied directly from the high or medium voltage distribution grid. Based on these divisions, the harmonized standards set the EMC quality requirements and test procedures to each specific equipment class.

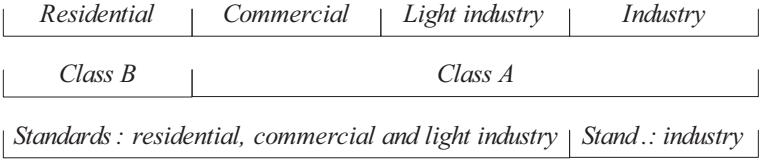


Figure 2.6: Identification of equipment classes according to EMC standards.

The Electromagnetic Compatibility of an equipment has many different aspects to be addressed. The EMC requirements for an electrical equipment are typically divided into (*i*) emissions and (*ii*) immunity. Both

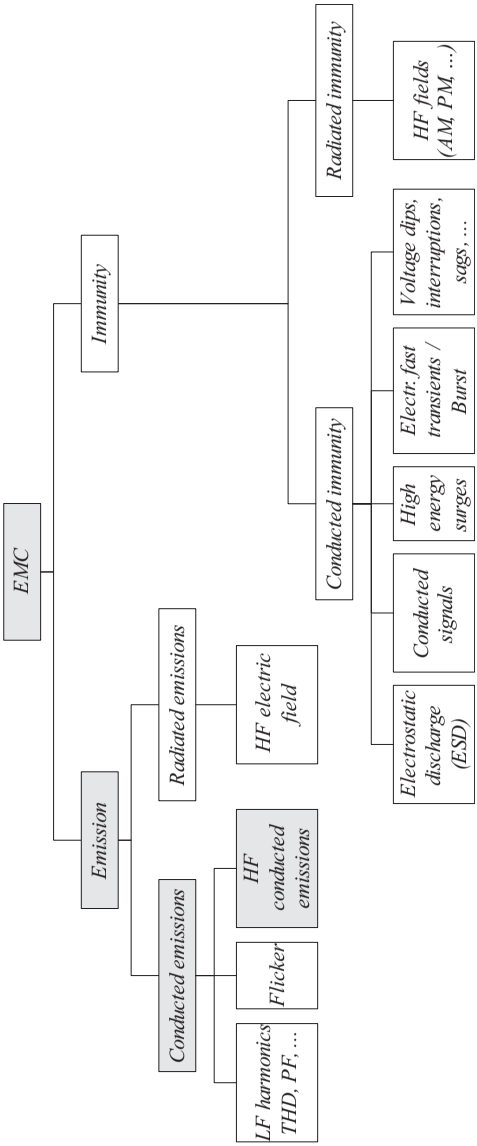


Figure 2.7: EMC requirements with sub-divisions in hierarchic displacement. Highlighted are the fields that are in the scope of this work.

are defined in the EMC standards and are typically done as shown in Figure 2.7. The diagram of Figure 2.7 shows the main divisions observed in EMC standards and highlights the fields which are within the scope of this work. It is seen that the design of filters aims mainly in fulfilling requirements that are related with high frequency conducted emissions.

Another clear division to which the EMC requirements and standards are submitted is the frequency ranges that are specifically covered. The main division regarding emissions is as depicted in Figure 2.8, where it is highlighted that the focus of this work is on conducted emissions in the 0.15 MHz to 30 MHz range.

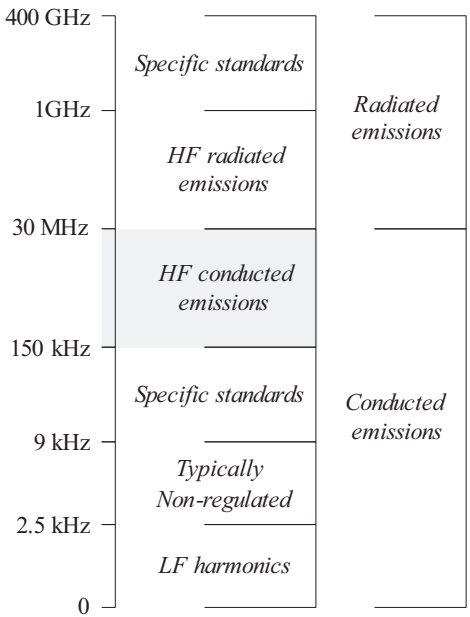


Figure 2.8: Frequency allocation of EMC requirements. Highlighted is the field that is in the scope of this work.

2.3.2 Considered Standards

As previously stated, this work is based on CISPR standards for industrial or telecommunications equipments. That means that the CE limits are set, respectively, by publications CISPR 11 [105] and CISPR 22 [106]. Common to these two standards are the allowable emission levels for equipments of classes A and B and the configuration of the measurement setup. The measurement equipment for both cases is defined in the generic standards CISPR 16 [104].

Standards for Telecommunication Equipments

General emission limits for information technology equipments are defined in CISPR 22 [106], which are identical to its American counterpart in standard FCC 15 [108, 109]. These are the employed limits for designing input filters of three-phase PWM rectifiers which operate as front-end converters in information technology (IT) power supplies.

Standards for AC Drives

The emission limits for drive systems defined in the product specific standard EN 61800-3, Tab.6 [110]. This standard sets two types of limits for industrial drives. The first limits are identical to CISPR 11 class B [105] and the second type depends on the agreement among manufacturers and the industry. This second type of limits often leads to a relaxation of the limits to the ones of CISPR 11 Class A. Therefore, in practice the limits stated in CISPR 11 are valid for AC drives as well. These limits are here employed when designing filters for direct Adjustable Speed Drives (ASD) as, for instance, AC-to-AC Sparse Matrix Converters.

2.4 Conducted Emission Limits

To understand the way limits are imposed in the CE standards, one shall be familiar with the involved dimensions. In general, conducted emissions are measured in a unit named "dBμV" which is related to a voltage through the relation,

$$1\,\mathrm{dB}\mu\mathrm{V} = 20 \cdot \log\left(\frac{1\,\mathrm{V}}{1\,\mu\mathrm{V}}\right). \tag{2.1}$$

The voltage under consideration is measured at the input of a test receiver or spectrum analyzer and is conducted through current probes or LISN circuits (cf. 2.5.1). CISPR 16 states that the input impedance of a test receiver shall be 50 Ω in the relevant frequency range. This means that the noise currents emanating from an hypothetical electrical equipment where the CE limit is $80\,\mathrm{dB}\mu\mathrm{V} = 10\,\mathrm{mV}$ shall be lower than $10\,\mathrm{mV}/50\,\Omega = 200\,\mu\mathrm{A}$. With this example it is seen that very low current amplitudes are allowed in the standards when compared to high switched currents of typical high power three-phase PWM converters, which are in the order of amperes. In practice this requires large values of attenuation for an input filter.

Two main types of limits are imposed in the relevant CISPR standards, namely: *quasi-peak* (QP) and *average* (AVG). These limits are related to the types of employed detection as explained in 2.5.2.

Different limits exist for Class A and Class B equipments and these are shown in Figure 2.9 for QP detection and in Figure 2.10 for the AVG type detector.

It is seen that Class B limits are more strict than Class A ones. The basis for that is that Class B equipments are intended for use by non-specialized operators in residential environments, thus shall be less prone

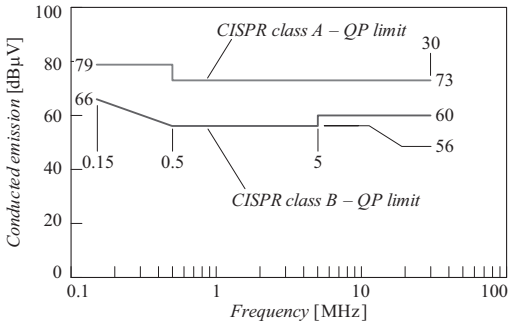


Figure 2.9: Quasi-peak limits for conducted emissions at the mains ports of Class A equipments according to CISPR Publications 11 and 22.

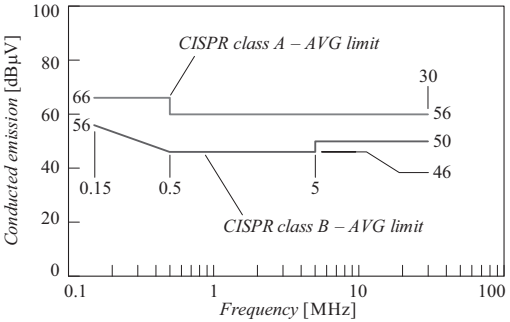


Figure 2.10: Average limits for conducted emissions at the mains ports of Class A equipments according to CISPR Publications 11 and 22.

to generate radio interference with other equipments.

2.5 Modeling of a Standard CE Test Setup

Based on CISPR Publications 11 [105] and 22 [106], there are different possibilities of assembling a test setup for CE measurements. The definition of which to use basically depends on the type of assessment that shall be carried out, on the size of the equipment to be tested and on the typical installation of the equipment. In this work, converters ranging from 5 kW to 10 kW are employed as noise sources. These converters are laboratory prototypes and therefore have no specific installation type. The sizes of such prototypes vary, but the maximum dimensions are below 40 cm. Therefore, a tabletop arrangement is suited, which is shown in Figure 2.11. This arrangement is used in most of the measurements presented here.

As seen in Figure 2.11, besides the equipment under test and its load there are other apparatus included in the testing, namely:

i. Non-conductive table.

ii. Ground planes.

iii. *Line Impedance Stabilization Networks* (LISNs), also known as *Artificial Mains Networks* (AMNs):

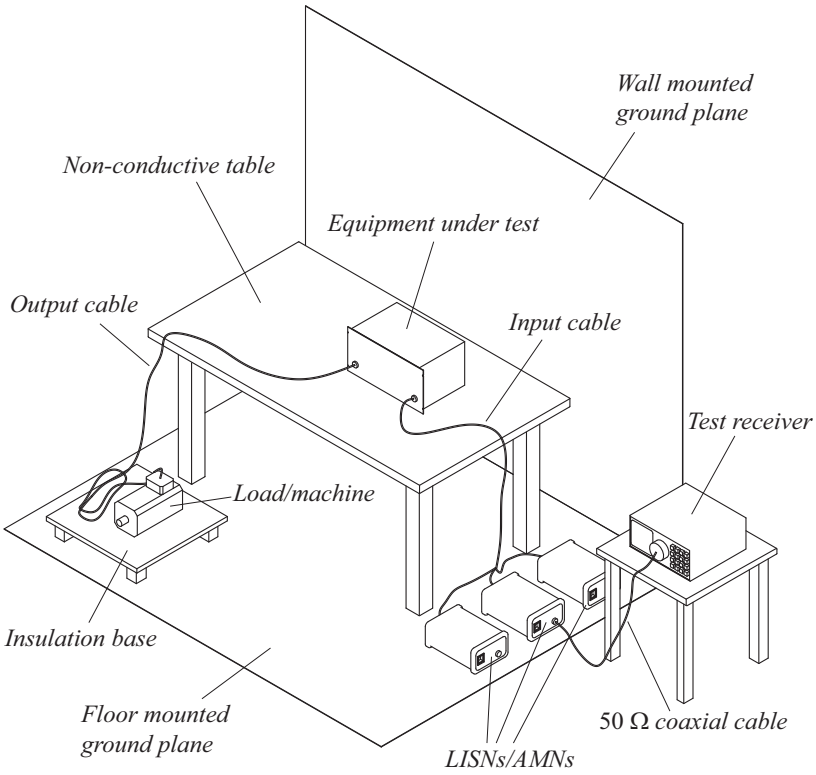


Figure 2.11: Typical CE test setup implemented in this work.

- supplying energy to the equipment under test (EUT);
- conducting HF emissions to the test receiver.

iv. A Spectrum Analyzer (SA) or Test Receiver:

- measuring HF emissions.

CISPR standards defines minimum requirements for a CE test where at least one ground plane is included in order to provide a common reference to all involved circuits. This plane is preferably a wall mounted one, but a ground mounted can also be used. Connection with the building's CBN is required for safety reasons. The minimum dimensions for the

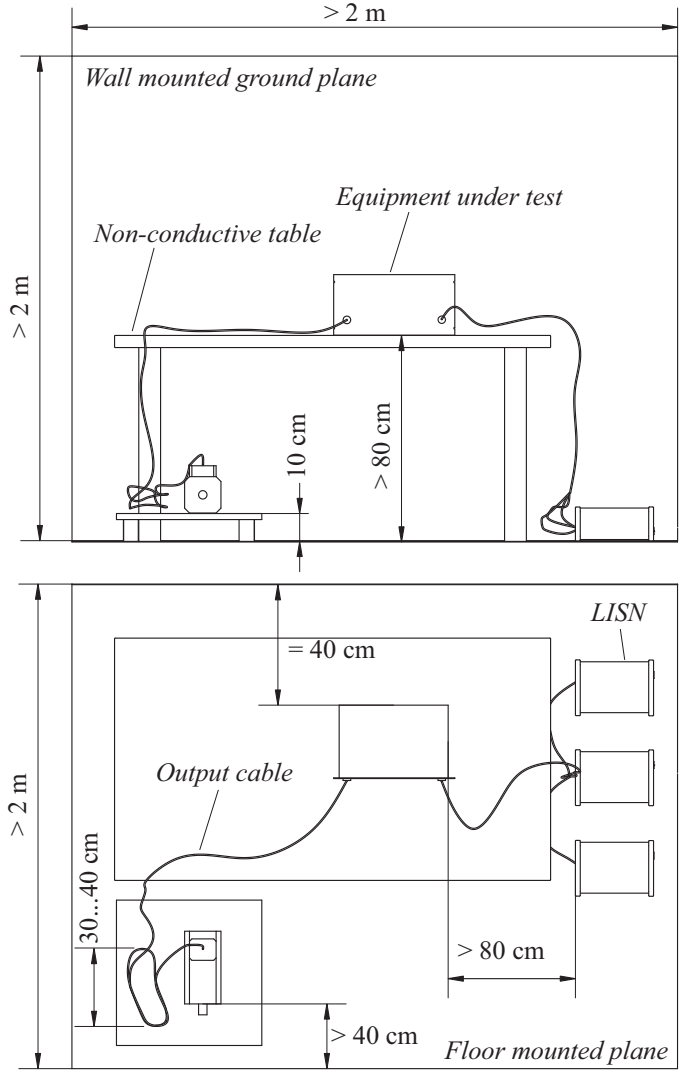


Figure 2.12: Distances in a conducted emission test setup as per CISPR requirements.

ground plane are 2 m × 2 m. The thickness of the planes is not specified in the standards, but a reasonable assumption is to calculate the skin depth δ_{150kHz} of aluminum at 150 kHz,

$$\delta_{150kHz} = \sqrt{\frac{1}{f\pi\mu_0\sigma_{Al}}} \cong 0.2\,\text{mm} \tag{2.2}$$

and use it as a basis for a low impedance plate.

It is very important to tightly connect the LISNs to the ground plane so that very low impedance connections for the ground currents regarding low and high frequencies are available. This connection is also important from an electrical safety perspective because the LISNs include large capacitors connected between phases, neutral and ground, thus producing large earth leakage currents that can be in the range of 700 mA to 1.5 A.

In the constructed laboratory, aluminum plates of 2.5 m × 2.0 m with a thickness of 2.0 mm were joined together by angel brackets spaced by less than 1 m as in CISPR 16. The planes were assembled as in Figure 2.11. Brackets were also employed to firmly bond the LISNs to the ground plane. Detailed information about the setup choice, minimum dimensions and distances can be found in the standards [105, 106] and a summary of the requirements is presented in the views of Figure 2.12. More controlled setups including shielded chambers (semi-anechoic, etc) are employed in certified EMC test houses, but are not strictly required. Nevertheless, it is advisable to place the measurement setup in an electromagnetically quiet place in order not to affect the performed measurements. Another reason is that the *floor noise* measured by a test receiver is influenced by the amount of emissions present in the mains because part of it is coupled via LISN circuits to the measuring port.

2.5.1 LISN and its Circuital Model

A *Line Impedance Stabilizing Network* (LISN), also called *Artificial Mains Network* (AMN) is specified for most of the conducted emission tests in order to guarantee the reproducibility of the measurements. It achieves that by using large filtering elements directly connected between the mains and the tested equipment. As a result, the impedance seen by the device under test is somewhat constant no matter where the electrical installation is placed. A LISN also provides good filtering from conducted emissions

coming from the mains, acting as a bidirectional filter.

The internal construction of a LISN is done so that the internal components are weakly coupled to each other. Typically, shielded chambers are provided for different inductors, which are usually wounded in an air coil providing excellent HF performance. Capacitors are also chosen aiming for good high frequency behavior. LISNs are built for various applications with different current ratings and are specified in sigle- and three-phase versions. Three single-lines LISN can also be applied in a three-phase setup, and vice-versa, since the impedances are strictly the same. Depending whether a Neutral conductor is connected or not a four-line LISN shall be applied.

A typical realization of a three-line LISN is depicted in Figure 2.13. For the CE measurement process a test receiver with 50 Ω input impedance is connected to one of the LISN output channels while the remaining two LISN ports are terminated with 50 Ω creating symmetric measurement conditions. Figure 2.13 shows that low frequency components are coupled from the equipment under test (EUT) to the power grid through inductors L_1 and L_2. The high frequency content generated by the EUT is decoupled from the grid and coupled to the test receiver and 50 Ω terminations through capacitors C_1.

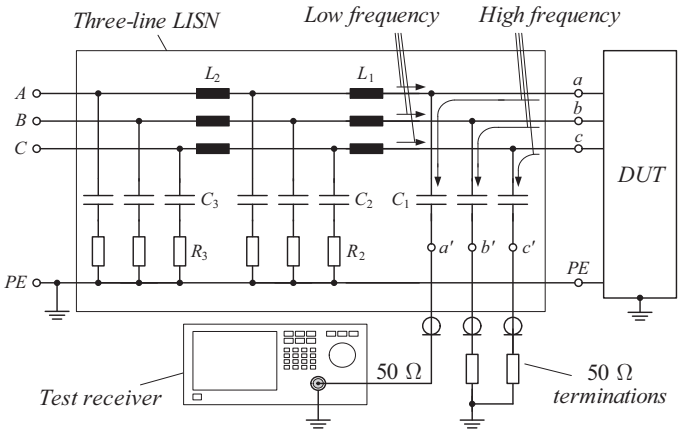


Figure 2.13: Schematics of a typical three-phase CE test setup employing a LISN illustrating the low and high frequency coupling paths.

Inspecting the circuit of Figure 2.13 the circuit of a LISN is constructed in a way that four main effects take place, namely:

- HF emissions generated by the EUT are directly coupled to a measurement test receiver;
- HF emissions coming from mains are filtered and do not influence the measurements;
- the low frequency energy from the AC power supply circulates to the EUT undisturbed, and;
- the HF impedance seen by the EUT is approximately unaffected by variations in the mains inner impedance.

The impedance curve of a LISN (the impedance seen from each phase of the EUT to PE including the test receiver's 50 Ω input impedance) is the most important characteristic and it is defined in EMC standards, specifically in CISPR 16 [104]. Different configurations are specified in different standards, but the most widespread is the 50Ω/50μH and this is here used. It is named 50Ω/50μH because it represents the impedance curve of a 50 Ω resistor in parallel with a 50 μH inductor. For this configuration, CISPR 16 suggests an equivalent circuit like in each phase of Figure 2.13 with the components specified in Table 2.7.

Table 2.7: LISN components for a 50 Ω/50 μH LISN as suggested in CISPR 16.

Component	Suggested value
L_1	50 μH
L_2	250 μH
C_1	250 nF
C_2	8 μF
C_3	1.2 μF
R_2	5 Ω
R_3	10 Ω

The LISN phase-to-ground impedance according to the parameters from Table 2.7 is compared with an ideal parallel connection of 50 Ω

with 50 μH in Figure 2.14. A $\pm$20% tolerance range around the presented curves is stated in CISPR 16. It is seen that the HF impedance from this circuits approaches the test receiver's 50 Ω.

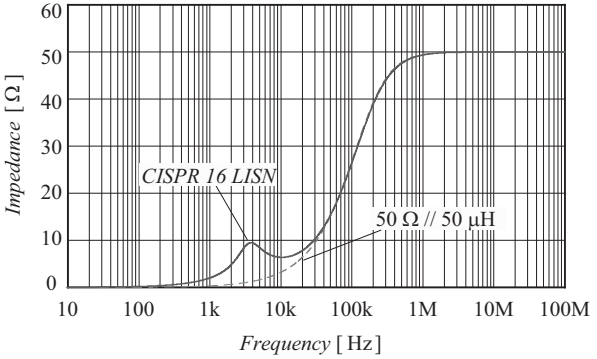


Figure 2.14: LISN impedance suggested in CISPR 16 in comparison with the impedance of an ideal parallel connection of 50 Ω with 50 μH.

Observing Figure 2.14 it is seen that the influence of L_2, C_2 and C_3 is only appreciable until 20 kHz. Therefore, a simplified mid- to high-frequency (0.15 to 30) MHz single-phase equivalent circuit of the LISN according to CISPR 16 is derived as in Figure 2.15. The voltage u_{meas} at the LISN output is applied to an EMC test receiver or appropriate spectrum analyzer. Resistor $R_{in,TR} = 50\,\Omega$ represents the input resistance of a test receiver.

The input impedance of the circuit of Figure 2.15 is defined as:

$$Z_{LISN}(s) = \frac{U_{noise}(s)}{I_{noise}(s)} = \frac{sL_{LISN}\left(sR_{in,TR}C_{LISN} + 1\right)}{s^2 C_{LISN}L_{LISN} + sR_{in,TR}C_{LISN} + 1} \tag{2.3}$$

while the transfer impedance from the measured voltage i_{meas} to the noise current i_{noise} is,

$$G_{LISN}(s) = \frac{U_{meas}(s)}{I_{noise}(s)} = \frac{C_{LISN}R_{in,TR}L_{LISN}s^2}{R_{in,TR}sC_{LISN} + 1 + s^2 C_{LISN}L_{LISN}}. \tag{2.4}$$

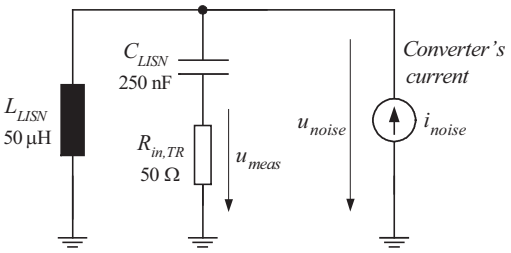


Figure 2.15: Simplified LISN high-frequency model which can be considered for determining conducted emissions through calculations or numerical simulations. The EUT is replaced by an equivalent current source i_{noise}.

Assuming, at high frequencies, an ideal decoupling from the EUT to the mains and a perfect coupling with the test receiver, which is the case for the circuit of Figure 2.13 in a simplified consideration, another simplified high frequency equivalent circuit can be obtained as illustrated in Figure 2.16. There, the input ports a, b and c of the EUT are directly connected to the input ports of the test receiver which allows all the high frequency emissions from the EUT to couple to the test receiver, while the mains ports A, B and C are separated from the EUT. Thus the LISN is considered as a direct bypass for HF currents.

Both simplified models are well suited for circuit analysis, calculations of attenuation and estimation of impedances if the relevant frequencies are high enough and the equivalent noise sources are correctly modeled. But in a complete converter simulation, where the low frequency behavior of the input supply interacts with the converter, the more complete models shall be used.

An important observation is that, due to its configuration, a LISN can not distinguish if the emissions are of common- or differential-mode nature. In fact, it represents quite different equivalent circuits for each noise mode as seen in Figure 2.17.

Based on Figure 2.16, applying superposition rules, the circuit of Figure 2.17 is obtained. It is seen that the LISN input impedances, according to noise modes are: 50 Ω for DM emissions, and; 50/3 Ω for CM emissions.

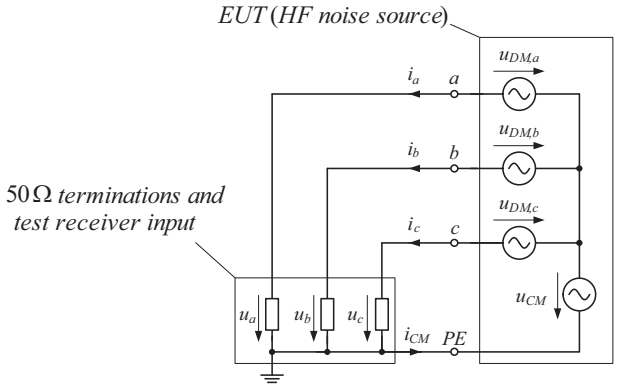


Figure 2.16: Further simplification of a LISN high-frequency equivalent "per phase" circuit. The EUT is replaced by equivalent HF noise sources split into DM $u_{DM,i}$ and CM equivalents u_{CM} and the LISN plus test receiver are simply modeled as 50 Ω resistors.

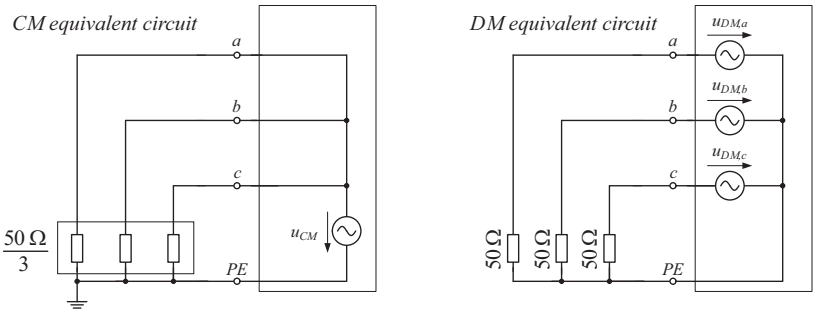


Figure 2.17: LISN high-frequency equivalent circuits for CM and DM.

2.5.2 EMC Test Receiver and its Model

EMC test receivers work like HF *spectrum analyzers*[1] (SA) specialized in accordance with the specifications stated in CISPR 16. From this perspective, conventional spectrum analyzers can be used in EMC testing

[1]Spectrum analyzer is a measurement apparatus employed to examine spectral contents of electrical signals (voltages, currents, power and other variables through proper transducers).

as long as they present features equivalent to a test receiver. The disadvantages are that, often, SAs sensitivity and dynamic range are not high enough and, depending on their input stages, they are more prone to have their input stages overloaded. Test receivers present the bandwidths, detectors and dynamic range according to CISPR standards along with high frequency and amplitude accuracies [25].

Even though modern test receivers use more and more digital signal processing through FFT calculations [111], an analog model of the measurement chain provides a good basis for a mathematical model and does not loose generality. A block diagram showing the basic functions of the frequency measurement system is depicted in Figure 2.18. The input signal (u_{meas}) of the receiver is processed according to CISPR 16 using a heterodyne technique [104], i.e. for measuring at a given frequency f the spectrum is shifted to a fixed *intermediate frequency* (IF) where band-pass filtering according to Figure 2.19 is performed. This allows analyzing a wide frequency range without changing the center (middle) frequency (MB) of the band-pass filter by properly adapting the oscillator frequency defining the frequency shift.

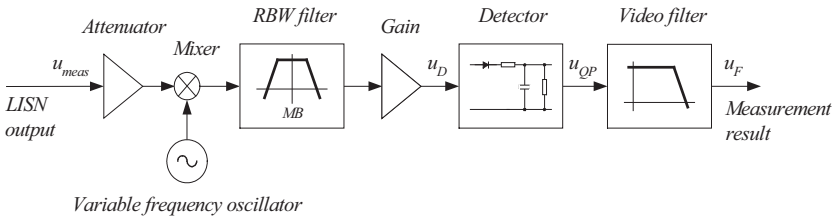


Figure 2.18: Simplified heterodyne measurement chain and QP detection model of a test receiver. Dependent on the *Oscillator* frequency the *Mixer* shifts the frequency of interest to an *Intermediate Frequency* (IF) where the measurements are performed employing a fixed-frequency band-pass filter (RBW filter) according to CISPR 16 [104].

The bandwidth of the band-pass filter (RBW filter) differs with dependency on the frequency band of interest. In CISPR 16 it is defined as $RBW = 9$ kHz at -6 dB for frequencies in the range (0.15...30) MHz as shown in Figure 2.19. Figure 2.19 also shows a simplified filter characteristic which is employed for calculation or numerical simulations of the test receiver. The fixed value MB denotes the band-pass center frequency. In

the mathematical model of the test receiver the MB is directly located at the frequency under consideration and shifted for a frequency sweep, therefore, a modeling of the oscillator and the mixer can be omitted.

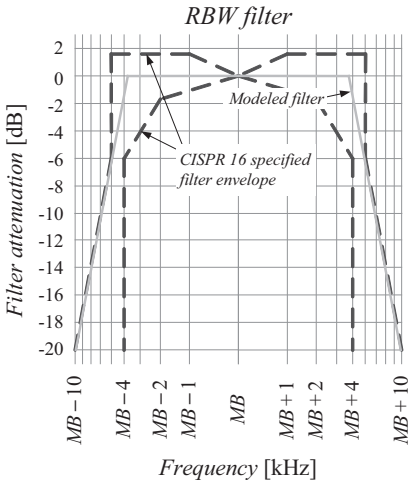


Figure 2.19: Upper and lower envelope of the characteristic of the resolution bandwidth (RBW) filter as specified in CISPR 16 and filter characteristic used when modeling the RBW filter.

As it is virtually not possible to measure the signals inside a test receiver, numerical simulations are used along with spectral calculations to illustrate the behavior of this type of equipment. An example of the effect of the RBW filter when applied to the spectrum of the measured LISN output voltage u_{meas} is shown in Figure 2.20 for a simulation of a three-phase Very Sparse Matrix Converter [112] for the point where $MB = 150$ kHz. It can be seen that the spectral components around MB (i.e. within the band-pass range) maintain their amplitude while the remaining spectral components are suppressed and therefore do not significantly contribute to the measurement result at this frequency point.

The block named *Gain* in Figure 2.18 adapts the signal level in a way that in case the input signal is formed by a single harmonic component inside the flat band-pass of RBW, the RMS value of this sine-wave results as output signal. This means that the total DC gain of the whole measurement system is $1/\sqrt{2}$.

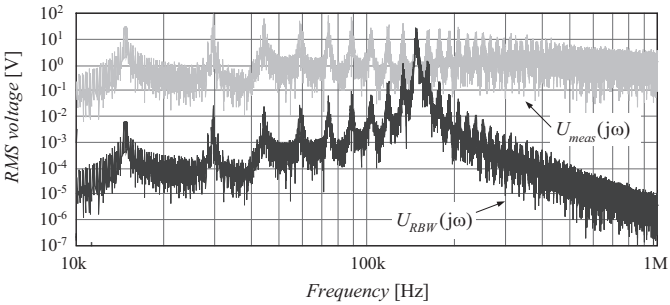


Figure 2.20: Voltage spectra at the input and at the output of the *RBW* filter for MB=150 kHz obtained from simulation results of a three-phase Very Sparse Matrix Converter [112].

The way that the signal u_D is processed in the sequence is called *detection*, performed by a block named *Detector*. This processing is further explained for different types of detectors in the following section. The final value for the measurement is obtained through the averaging of the output voltage of the QP detector what is performed in the *Video filter* which is characterized by a time constant of 160 ms for (0.15...30) MHz.

2.5.3 Detector Types and their Models

A *Detector* is a circuit that outputs a signal level which depends on specific rules. Spectrum analyzer present typically four types of detection circuits, namely:

- Peak detector;
- RMS detector;
- Average detector, and;
- Quasi-peak detector.

These detection circuits define the relation among amplitude, repetition ratio and signal shape that is applied to the measured signal. CISPR limits are defined for average and quasi-peak detectors. Peak detection can be used in a measurement process to speed up the measurements,

which are relatively time consuming. These circuits are explained in the following and, for the quasi-peak detector mathematical models are presented.

The RMS Detector

A *Root Mean Square* (RMS) Detector indicates the RMS value of the signal that is injected at its input. This is, therefore, related to the signal's power or energy. As CISPR 16 does not specify measurements with RMS detectors, these are here not considered.

The Average Detector

The *Average* (AVG) Detector is calibrated to indicate the RMS value of a pure sine wave. That is done by calibration through the injecting a single sine wave harmonic signal at its input, rectifying it, measuring the average value and multiplying it by 1.11. Therefore, a true RMS value is measured only for a pure sine wave. In case a complex waveform is injected at its input, the AVG detector evaluates it to a value which is lower than the one of a true RMS detector.

In practice, the output of the Average detector is proportional to the average value over a specified time interval of the envelope of the injected signal. An average detector characterizes waveforms of constant shape, like a square pulse. It can be used to emulate loads that are more sensitive to the average level of a noise signal, rather than to its peak value. That is the case for equipments employing long integration time constants, such as electrical indicators.

For pulse type signals, the average detector generates a level which is proportional to the duty-cycle. The basic relation for an average detection measurement of a square wave signal is given by,

$$\delta = \frac{f_S}{BW}, \tag{2.5}$$

where δ is the relation between the average value of a signal and its repetition frequency, f_S is the repetition frequency and BW is the measurement bandwidth. This means that if the repetition frequency equals the measurement bandwidth, the average detector gives the same level as a peak detector.

The Quasi-Peak Detector

The *Quasi-Peak* (QP) Detector is also specified in CISPR 16 for CE measurements. This type of detector was created to measure the annoyance of a signal. It has its origins in the way human physiology perceives annoyance and the causes date back to first experiences with public broadcasting of audio and video. It is related to the amount of noise that a person hears or sees, where the repetition rate of the annoying signal is as relevant as its amplitude. The QP detector is able to emulate this behavior.

In [113] a historical background for this type of detector is written, from where:

> "In the 1930s, a board of listeners was formed to decide what characteristics of a radio disturbance caused annoying interference, and the degree of annoyance, for listeners to radio broadcast (sound) reception. The broadcast receiver of the day received signals in the LF or MF bands, and had an IF bandwidth of between 8 kHz and 10 kHz. The desired signal was a carrier with voice or music amplitude modulation. Using a radio broadcast receiver equipped with an audio output voltmeter, the board of listeners rated the annoyance of the interference with its audio output and its particular pulse repetition frequency. Each member of the board of listeners was said to have worked independently, so that the results would be statistically useful. Out of this study came the specifications for the quasi-peak (QP) detector used in the first CISPR Radio-Noise Meter. When radio broadcasting was extended into the HF band, the frequency range of the CISPR Radio-Noise Meter was extended upward from 1605 kHz to 30 MHz. Since the later radio broadcasting services to be protected had about the same characteristics as the earlier ones, the QP detector from the early CISPR Radio-Noise Meter was retained, and did a good job predicting the interference effects of radio disturbances. CISPR Publication 1 was the specification for this radio-noise meter."

Because of the different time constants, the output of the QP detector presents a fraction of the peak value of a pulsed signal with a certain repetition frequency. This fraction increases with, both peak amplitude

and repetition rate. The *annoyance factor* is proportional to the repetition rate of an interfering signal. It is considered that the QP detection is the most suited way of evaluating possible interference because of its attribute of measuring annoyance.

An important observation is that QP detectors are well suited for measuring broadband signals, while narrowband ones are better characterized with the average detector. For this reason it is the detector used in most of the experiments and designs of this work. Besides that, the FCC only requires QP measurements for CE. As for the AVG detector, the QP output is calibrated to give the RMS value of a single frequency sine wave injected at its input.

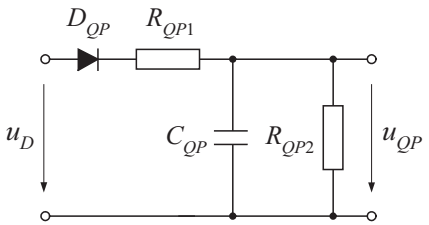


Figure 2.21: Quasi-peak (QP) detector circuit model.

The basic function of the QP detector is understood by examining the model [25, 114, 115] shown in Figure 2.21. It shows different time constants for the charging and discharging of the output capacitor C_{QP}. These charge τ_{charge} and discharge $\tau_{discharge}$ time constants are defined as,

$$\tau_{charge} = \frac{R_{QP1}R_{QP2}}{R_{QP1} + R_{QP2}}C_{QP} \tag{2.6}$$

$$\tau_{discharge} = R_{QP2}C_{QP}. \tag{2.7}$$

Considering an ideal behavior of the diode D_{QP} and ideal passive components, two linearly independent ordinary differential equations are derived, defining the time behavior of the circuit,

$$\frac{du_{QP}(t)}{dt} = \begin{cases} \frac{\tau_2-\tau_1}{\tau_1\tau_2}u_D(t) - \frac{1}{\tau_1}u_{QP}(t) & \text{if } u_D(t) \geq u_{QP}(t) \\ -\frac{1}{\tau_2}u_D(t) & \text{if } u_D(t) < u_{QP}(t). \end{cases} \tag{2.8}$$

Aiming for a calculation procedure to model the QP detector, it is required that eq. (2.8) is solved. One way to accomplish that is by considering that u_D is a piecewise linear function sampled with small time intervals. Thus, a discrete numeric solution is found by applying the derivative definition for the sampling intervals Δt and the sample is taken at $t = k\Delta t$ with $k = 0, 1, \ldots$. Discretizing eq. (2.8) leads to,

$$u_{QP}[k+1] = \begin{cases} \frac{\tau_2-\tau_1}{\tau_1\tau_2}u_D[k]\Delta t + \left(1 - \frac{\Delta t}{\tau_1}\right)u_{QP}[k] & \text{if } u_D[k] \geq u_{QP}[k] \\ \left(1 - \frac{\Delta t}{\tau_2}\right)u_{QP}[k] & \text{if } u_D[k] < u_{QP}[k], \end{cases} \tag{2.9}$$

which can be used for numeric calculations. More complex numeric integration algorithms can also be applied, but as the results are given in dB, enough precision can be achieved with eq. (2.9).

According to CISPR 16, different sets of time constants have to be considered for different frequency ranges under consideration. For the range from 0.15 MHz up to 30 MHz, the charging time constant for the QP detector is specified as $\tau_{charge} = 1$ ms, while the discharging time constant is $\tau_{discharge} = 160$ ms. An illustration of the QP detector function is shown in Figure 2.22, where the voltages at the input and output of the detector circuit for simulation results of the emissions in a three-phase Very Sparse Matrix Converter [112] are shown.

As a result of the quasi-peak detection, the measured value is larger than the RMS value of the voltage at the LISN output in case more than one harmonic component is present inside the resolution bandwidth RBW. Therefore, a filter design, not to be under dimensioned, can not be based only on the individual harmonic of higher magnitude in the RBW but has to consider the calculated QP detector output values.

Still considering the simulation results of a three-phase Very Sparse Matrix Converter [112], the QP detected averaged values $U_F(j\omega)$ resulting from the simulation model are depicted for selected frequency values in Figure 2.23 (marked by "$\times$"). Furthermore, Figure 2.23 clearly shows that

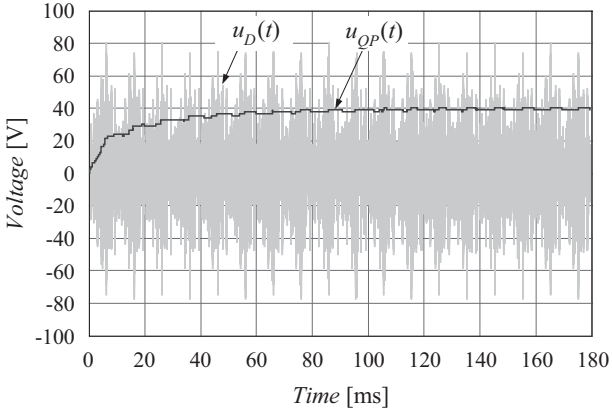


Figure 2.22: Effect of the quasi-peak detector to the voltage u_D.

the RMS amplitudes of individual harmonics of the LISN output voltage are well below the value obtained with the quasi-peak detector weighting measurement. This difference is of approximately 15 dB at 150 kHz and reduces at higher frequencies. This fact underlines the importance of proper modeling of the measurement system, i.e. a filter design procedure relying only on a LISN modeling and considering only the amplitudes of individual harmonics would not be sufficient unless large design margins are provided.

As can also be seen from Figure 2.23 the predicted quasi-peak values remain between a lower $Min_{result}(j\omega)$ and an upper limiting curve $Max_{result}(j\omega)$. The lower limit can be obtained as the square root of the sum of the squares of the RMS value of all harmonic components $U_{meas}(j\omega)$ located within the RBW as in,

$$Min_{result}(j\omega) = 20 \cdot \log \left[\frac{1}{1\,\mu\mathrm{V}} \cdot \sqrt{\sum_{f=MB-\frac{RBW}{2}}^{MB+\frac{RBW}{2}} U^2_{meas}(j\omega)} \right]. \qquad (2.10)$$

The resulting signal $Min_{result}(j\omega)$ is the equivalent RMS value and can be seen as signal showing equal spectral power at the frequency ω as

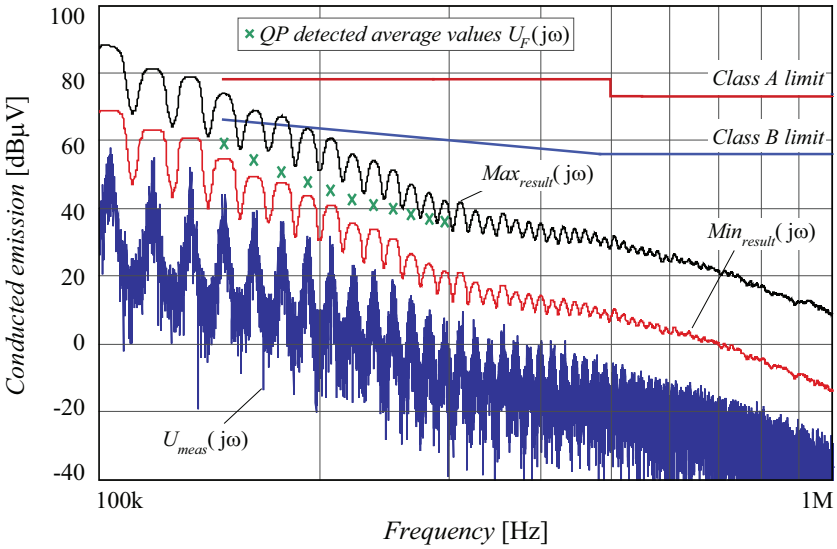


Figure 2.23: Simulation of a quasi-peak measurement compared to the spectrum of the voltage $U_{meas}(j\omega)$ at the LISN output terminals. Furthermore shown: Minimum ($Min_{result}(j\omega)$) and maximum ($Max_{result}(j\omega)$), and signal levels resulting from QP detection, and conducted emission limits according to CISPR 22, Classes A and B.

given for the original signal within the RBW.

Assuming no correlation of the individual harmonics a limiting maximum value,

$$Max_{result}(j\omega) = 20 \cdot \log \left[\frac{1}{1\,\mu\mathrm{V}} \cdot \sum_{f=MB-\frac{RBW}{2}}^{MB+\frac{RBW}{2}} U_{meas}(j\omega) \right], \qquad (2.11)$$

can be calculated by linearly adding the RMS values $U_{meas}(j\omega)$ of the spectral components within the RBW. The values of $Max_{result}(j\omega)$ can be numerically calculated with a much lower computational effort than the exact solution for a QP detector. Thus it can be employed in a sim-

plified filter design, where the full calculation of the QP measurement is neglected.

The simplified numeric calculation procedure for computing $Max_{result}(j\omega)$ is graphically depicted in Figure 2.24. This procedure, however, will result in an slightly over-dimensioned filter for some frequency range. Nevertheless, considering components variation, measurement errors and uncertainties in the modeling procedure, this can also be advantageous in a filter design procedure.

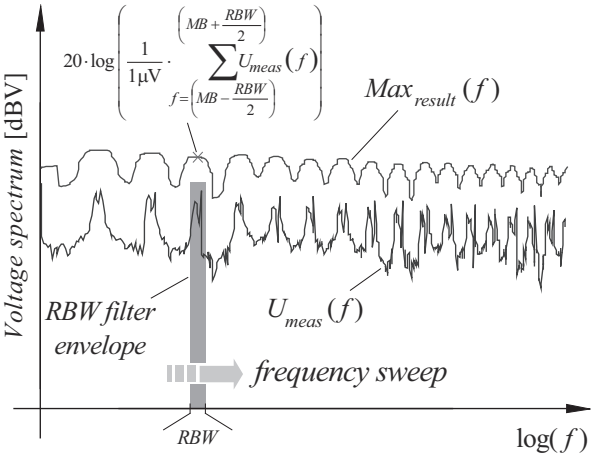


Figure 2.24: Illustration for the performed quasi-peak measurement worst case approximation where $U_{meas}(f)$ represents the input voltage of a test receiver and $Max_{result}(f)$ the maximum obtainable value for the QP measurement.

The Peak Detector

A *Peak* (PK) Detector presents a circuit configuration like the QP detector, but with a very small charging time constant and a large discharging time constant. The result is that it measures approximately the RMS value of the peak of an injected signal. It is suited for the measurement of continuous noise signals.

This detector presents a simple procedure of evaluating the magnitude of an interference. Its measurement time is very short as it charges to the peak rapidly. Figure 2.25 shows the basic behavior of the three types

of detectors which are relevant for evaluating conducted emissions. It is seen that the peak detector's output value shall be always equal or larger than the one from a QP detector. As the QP detection is very time consuming, it is common practice to use the PK detector for obtaining faster measurement times and then re-run the QP for critical points. This procedure is also described in CISPR 16.

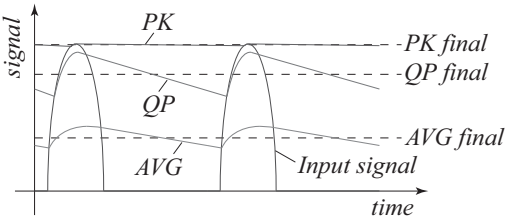


Figure 2.25: Illustration of the behavior of the different types of detection circuits.

From Figure 2.25 it is observed that if the repetition frequency of the measured signal is high enough, all final detected levels converge to the same value.

2.6 HF Modeling of Power Cables

The interconnections in a standard three-phase CE test setup are typically realized with multi-conductor power cables. The most relevant connections are the connection from the LISN to the power converter and from this to its load (resistors, electric machines, converters, etc). Cables are known to exert strong influence in the HF behavior of conducted emissions [57–59] and, thus are important portions in an accurate HF modeling procedure.

2.6.1 Modeling a Supply Cable

Supply cables are usually neglected in the literature. Probably because the parasitic components of an input cable act as filtering elements, but have a limited influence on noise when compared to input filters. In general, designing input filters and neglecting an input cable represents a safe

margin in the procedure. Nevertheless, the coupling from a noise source to its input cable might do just the opposite, increasing noise levels [59]. This happens due to different reasons, among which are:

- the highly reactive impedance of a long cable;
- the position of the cable (capacitive and magnetic couplings are present if it is placed close to a noise source), and;
- proper shielding of the noise source is not available.

Input supply cables in a three-phase setup contain at least four conductors, three for the phases and one for the protective earth. A fifth conductor for the neutral might be available as well. It is a widespread practice that these cables do not present shielding layers of any kind because the power equipments contain an input filter, which prevents further conduction of noisy currents.

Cables can be modeled through networks of lumped or distributed elements. The choice of a proper model shall be based on the relation between the length of the cable and the wavelength at the highest frequency of interest f_{max}. This leads to a wavelength λ_0 in free space of,

$$\lambda_0 = \frac{c}{f_{max}}, \tag{2.12}$$

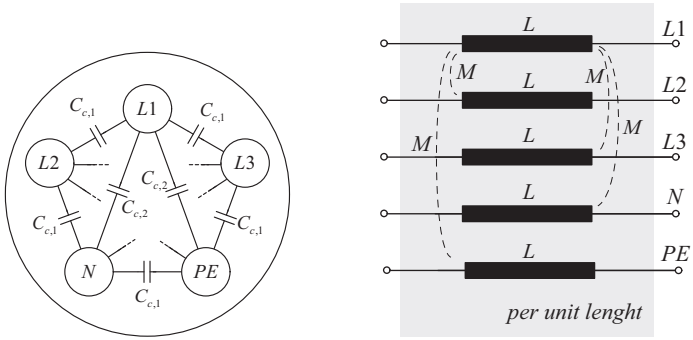
where $c \cong 2.9979 \cdot 10^8$ m/s is speed of light in free space.

For testing of conducted emissions, frequencies of up to 30 MHz are within the measurement range. The wavelength for $f_{max} = 30$ MHz is $\lambda_0 \cong 9.99$ m. Usually the conductors of a power cable are enclosed in insulation materials with relative permittivities of around 3 to 5. Therefore the wave speed is reduced three to five times and a maximum wavelength λ_0 of approximately 30 m is expected. It is recommended [24] that, to be in the safe side, distributed parameters, i.e. transmission lines models, shall be used starting from one tenth of the wavelength of interest. Therefore, the maximum cable length l_{max} for using models with lumped elements is given by,

$$l_{max} = \frac{\lambda_{max}}{10} = \frac{c \cdot \sqrt{\epsilon_{r,min}}}{f_{max} \cdot 10} = \frac{2.9979 \cdot 10^8 \,\mathrm{m/s} \cdot \sqrt{3}}{30\,\mathrm{MHz} \cdot 10} \tag{2.13}$$

$$l_{max} \cong 1.73\,\mathrm{m} \tag{2.14}$$

In the employed laboratory, a five conductors, 3 meters long unshielded cable is used for CE measurements for power converters up to 10 kW. A simplified distributed parameters model of this cable is here derived through direct impedance measurements. The assumed simplifications are the following: (*i*) a uniform distribution of, both electric and magnetic field, in the cross-section, i.e. no proximity effect; (*ii*) transverse electromagnetic wave propagation is assumed, i.e. a lossless transmission line model, and; (*iii*) no dielectric losses. The model is based on distributed "per unit length" parameters, which are shown in Figure 2.26. Self and mutual inductances between all five conductors and a capacitance matrix among all conductors are considered.



(a) *Capacitive network* (b) *Inductive network*

Figure 2.26: Input unshielded cable model: (a) Per unit length capacitive network model for the considered cable. Only two out of five $C_{c,2}$ capacitors are shown. (b) Per unit length inductive network model for the considered cable. Only the mutual couplings M of phase $L1$ are shown.

Analytical solutions for transmission line models of multi-conductor cables based on their geometry and materials are available [59, 116] only for three-conductor cables, i.e. cables for single-phase applications. This arises from the highly complex equations involved in lines with multiple

conductors. Typically, a five or more conductors cable model is achieved through computational field solvers [24] or direct impedance measurements.

Based on the model of Figure 2.26, a series of measurements were performed in order to obtain the parameters through a parameter identification routine. The different measurements were performed with an Agilent 4294A (40 Hz – 110 MHz) precision impedance analyzer, were the cable was extended with a 10 cm insulation distance from a ground plane. The measured impedances are displayed in Figure 2.27.

Aiming for the different values of series resistances, inductances and capacitances, five different measurements are performed. For the measurements, the cable has been placed on a wooden floor bent in a bundle of around 60 cm wide. The obtained values (see 2.6.2 for details) are compared with the low frequency equivalent circuit equations per-unit-length equivalent circuit of Figure 2.26 leading to five linearly independent equations, from were the parameter values are obtained. The calculated values are presented in Table 2.8.

Table 2.8: Calculated input cable parameters.

Self inductance L [μH/m]	*Mutual inductance* M [μH/m]	*Series resistance* R [mΩ/m]	*Close capacitance* $C_{c,1}$ [pF/m]	*Far capacitance* $C_{c,2}$ [pF/m]
1.32	0.60	11.9	93.7	7.47

Implementing this circuit in a computer simulation is very difficult because of the highly complex nature of the transmission line [63] formed by the five coupled lines. One way to avoid this inconvenience is to implement multi-stages which divide the cable in finite lengths, instead of the infinite characteristic of the transmission line formalism. This approach can be applied as long as each stage of the cable $l_{stage,max}$ is much smaller than the minimum wavelength. Following this rule in practice means that,

$$l_{stage,max} < \frac{\lambda_{max}}{10} \cong 2.99\,\text{m}. \tag{2.15}$$

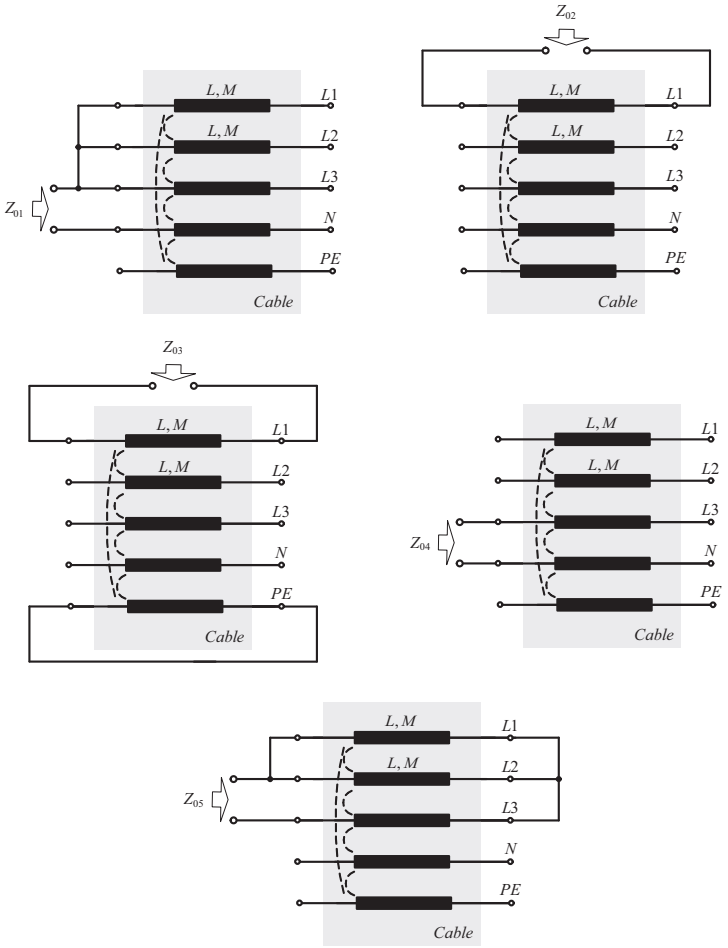


Figure 2.27: Input cable measured impedances.

As an example, a comparison between the measured impedances and a simulated four-stage ($l_{stage} \cong 0.75$ m) lumped circuit is shown in Figure 2.28, where a very good model accuracy up to 10 MHz is observed. This should be sufficient for most of the conducted emissions studies. If higher frequencies are desired, a more complex model shall be imple-

mented including proximity and skin effects as well as dielectric losses and asymmetries in the mutual inductances. On the other hand, a different installation of the cable will cause the impedances to change , so that close to perfect matching is not expected in practical applications.

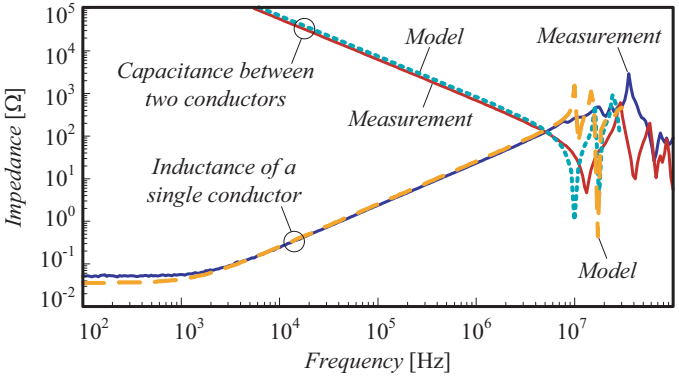


Figure 2.28: Comparison between two measured impedances in the cable and the results obtained with a four-stage lumped equivalent simulation.

2.6.2 Load Cables Modeling

The main reason to model load cables is that they typically present relevant stray capacitance values to ground, which might strongly influence the generation of CM noise. This is usually the case with the application of PWM converters in AC drives, because no output filter is used in most applications and the high frequency switched voltages are directly applied to the output cable, also named *motor cable*. For ac-to-dc converters, output filters are typically employed that prevent tangible interactions with downstream connected cables. For these reasons, this section focuses on three-phase motor cables.

Typically, the construction of modern motor cables for PWM based ac drives includes a shielding layer covering the usual four to five conductors. In practice, few exceptions to this are observed [55] when the PWM converter is directly followed by large filtering circuits or the installation still uses the cables designed for fixed frequency/voltage drives. The main objective of the shielding layer is to prevent HF electromagnetic fields

that would, otherwise, cause strong radiated emissions and possibly generate problems for EMC and signal integrity. Fulfilling radiated emissions requirements without shielding is virtually not possible [58]. An extra metallic layer for mechanical/chemical protection is also commonly found in motor cables employed in heavy industry sites [117]. With all these layers and possible different disposition of conductors, analytical models for these cables are not generally available. Again field solvers or impedance measurements are used to define a cable model. One exception is made for a symmetrical cable comprising three conductors and the shielding, which is modeled in [116].

The basic understanding for the main phenomena related to motor cables in ac drives can be introduced with Figure 2.29, where a converter provides the interface between the LV distribution grid and an electric machine through a shielded cable.

The converter is assumed to be a conventional two-level inverter with Space Vector Modulation operating with switching frequency $f_S = 1/T_S$, thus generating in an hypothetical time interval the output voltages as displayed. CM voltage arising from a front-end converter is not explicitly considered. It is seen that the line voltages applied to the cable are pulsed ones, which shall feed the machine with the required voltages. As shown if the figure, the PWM pulse pattern generates a common mode voltage u_{CM}. It is clear that, depending on the electrical characteristics of the cable and on the input impedances of the motor, oscillations are prone to happen in varying severity.

Various research studies [53, 57, 58, 116–121] have been performed to evaluate, design and understand the phenomena involved with motor cables and PWM converters. Different effects have been considered and the main focus are on the protection of the machine from high stray currents and EMC. The main motivation for these studies was the reported failures and interference problems in industrial environments after the inclusion of PWM based AC drives [53, 57, 117, 118]. A basic review based on Figure 2.29 is presented in the following.

Common Mode Currents: The PWM pulse patterns applied to a machine generate CM currents as shown in Figure 2.29. These currents are highly dependent on the cable characteristics since large capacitances to PE arise from the placement of the shielding layer and the length of the cable. The amplitudes of CM currents depend basically on the change of rate of the pulsed voltages (dv/dt), on the switching frequency (f_S),

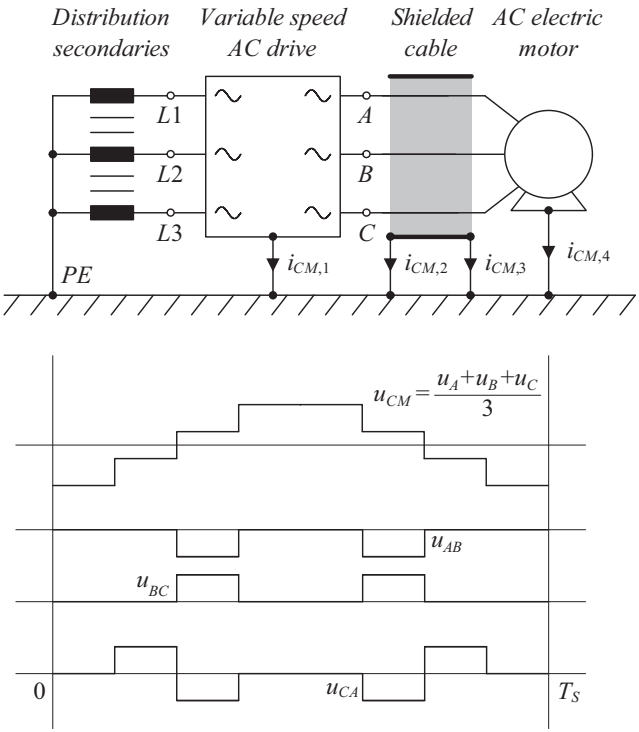


Figure 2.29: Typical three-phase PWM converter based ac drive installation and simplified output waveforms within a switching period.

on the amplitude of the pulsed voltages and on the involved impedances. This is the most important effect from an EMC modeling point of view.

For the machine, the CM currents generate [53, 57, 117, 118]:

- the deterioration of the metallic bearings through arcing currents;
- voltages induced in the shaft that, if electrically connected to other equipments, generate CM currents in these equipments, and;
- in case the motor cable includes control signals, it is very probable that the CM currents induce noise provoking malfunctions in the power converter itself [117], what could be worsen by employing non-symmetric cables.

Crosstalk: induced currents and voltages in non-shielded cables near the motor cable might generate destructive voltage stress and safety hazards [57].

Transient Standing Wave Voltage: this effect is also named reflective wave or transmission line effect. It consists in the generation of oscillations and over-voltages at the input terminals of the machine due to wave reflection [53] as shown in Figure 2.30. If the cable is long enough, the system can be modeled as a transmission line, where the characteristic impedance $Z_{0,cable}$ of the cable is mismatched with the surge (input) impedance Z_{surge} of the motor. The impedance mismatch generate waves which are reflected to the PWM converter and are summed with the following voltage pulse, generating a standing pattern and producing over-voltages. These over-voltages cause stresses in the insulation of cable and machine.

From the transmission line theory, the reflection coefficient is defined for this system as,

$$\Gamma = \frac{Z_{surge} - Z_{0,cable}}{Z_{surge} + Z_{0,cable}} \tag{2.16}$$

and the line-to-line voltage at the input of the motor $U_{motor,l-l}$ is,

$$U_{motor,l-l} = (1 + \Gamma)\, U_{AB}. \tag{2.17}$$

From eq. (2.16) it is clear that $-1 \leq \Gamma \leq 1$. This means that the motor voltage might be twice as large as the voltage applied at the output of the PWM converter.

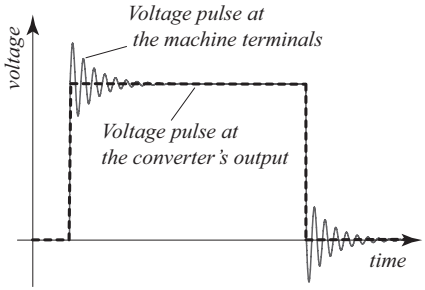


Figure 2.30: Standing wave effect.

For a full reflection ($\Gamma = 1$) to take place it is required that the wave front generated in a PWM pulse travels twice the length of the cable (l_{cable}). From this assumption it is possible to estimate a critical cable length (l_{crit}) as [57],

$$l_{crit} = \frac{vt_{rise}}{2} \tag{2.18}$$

where v is half the speed of light in vacuum and t_{rise} is the rise time of the PWM voltage pulse. Assuming $v = 150$ m/μs, Figure 2.31 presents numerical values for the minimum cable length for full wave reflection.

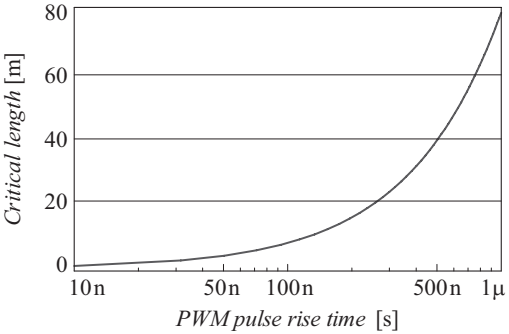


Figure 2.31: Critical cable length as a function of the rise time of PWM voltage pulses for $v = c/2 \cong 150$ m/s.

General objectives when selecting a motor cable are:

- minimize CM currents;
- minimize induced currents into the system ground;
- minimize open-circuit voltages from the motor terminals to PE;
- minimize crosstalk.

From the list above, some guidelines are derived [53, 57, 118]:

- symmetric cables to reduce external fields;
- unbroken shields are necessary to prevent radiated emissions;

- lossy dielectric materials provide damping of oscillations;
- impedance matching circuits at the machine's terminals prevent reflected voltages;
- long PWM transition times help reducing over-voltages;
- proper earthing connections are essential.

The reviewed phenomena highlight the importance of proper cable modeling in order to avoid undesired effects. In this work the main objective is to design input filters for PWM converters, thus the effects related to motor stresses and control related noise are not studied.

For the CE laboratory test setup, two cables were constructed, namely a 3 m long cable and a 30 m long cable. Both were built by employing the same cable type "Purwil EMC" rated for 450 V according to SEV standards with 2.5 mm^2 of copper area per core. The cables comprise five conductors plus shielding and are used for CE measurements for power converters up to 10 kW with rated voltages of 400 V line-to-line. The cross-section of the cable is shown in Figure 2.32.

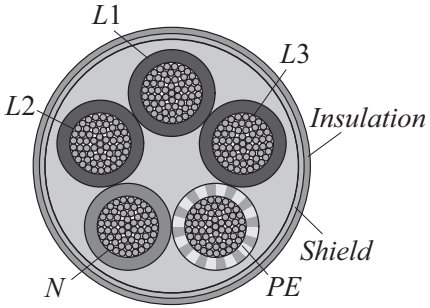
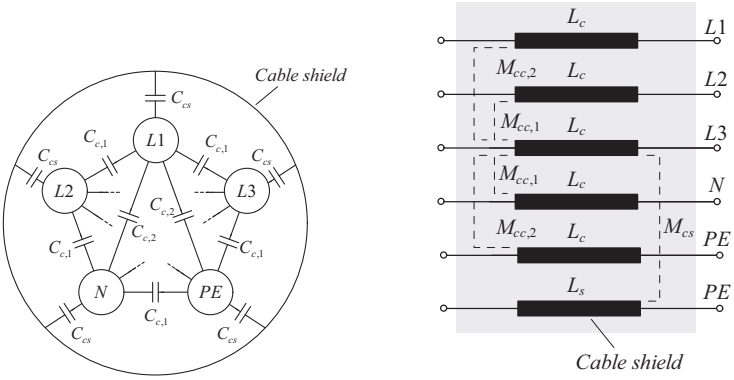


Figure 2.32: Cross section of the employed motor cables.

As for the input cable, an electrical model is obtained through impedance measurements. The model configuration is presented in Figure 2.33, where the "per unit length" inductive and capacitive networks are displayed.

Based on Figure 2.33, a lossless transmission line model of the cable is defined as in Figure 2.34.



(a) Capacitive network (b) Inductive network

Figure 2.33: Shielded motor cable model: (a) Per unit length capacitive network model for the considered cable. Only two out of five $C_{c,2}$ capacitors are shown. (b) Per unit length inductive network model for the considered cable. The mutual couplings $M_{cc,1}$, $M_{cc,2}$ and M_{cs} occur in all phases, but are here shown only for line $L3$.

Aiming for finding the parameters of Figure 2.34, a series of impedance measurements were performed in the total original cable length of $l_{cable} =$ 36 m.

The results of these impedance measurements are used to calculate the "per unit length" parameters of the cable model. The different measurements were performed with an Agilent 4294A (40 Hz – 110 MHz) precision impedance analyzer, were a 36 m long cable was extended in an insulated surface. The impedance measurements are divided into two groups, the first for evaluating the magnetic components as shown in Figure 2.35 and the second to identify the model's capacitances as in Figure 2.36.

The inductance matrix $\mathbf{L}_{cable}$ for the networks of Figure 2.35 is,

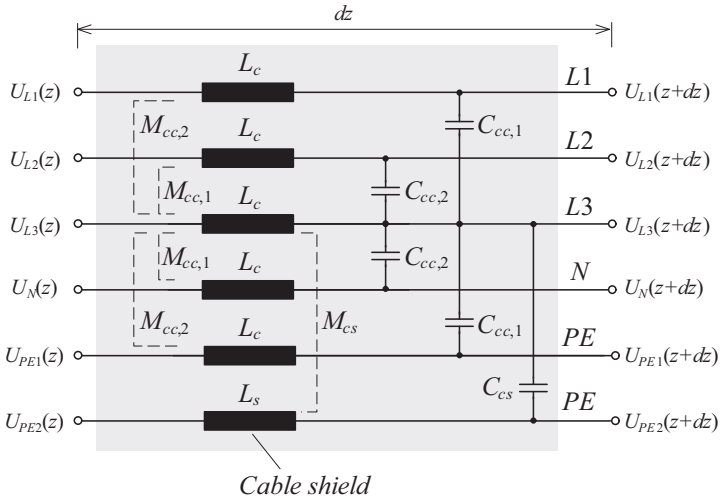


Figure 2.34: Motor cable transmission line infinitesimal ($dz \to 0$) model with the "per unit length" parameters. Couplings and capacitances are displayed only for line $L3$, but should be considered symmetrically in all lines.

$$\mathbf{L}_{cable} = \begin{bmatrix} L_{c,t} & M_{cc,1,t} & M_{cc,2,t} & M_{cc,2,t} & M_{cc,1,t} & M_{cs,t} \\ M_{cc,1,t} & L_{c,t} & M_{cc,1,t} & M_{cc,2,t} & M_{cc,2,t} & M_{cs,t} \\ M_{cc,2,t} & M_{cc,1,t} & L_{c,t} & M_{cc,1,t} & M_{cc,2,t} & M_{cs,t} \\ M_{cc,2,t} & M_{cc,2,t} & M_{cc,1,t} & L_{c,t} & M_{cc,1,t} & M_{cs,t} \\ M_{cc,1,t} & M_{cc,2,t} & M_{cc,2,t} & M_{cc,1,t} & L_{c,t} & M_{cs,t} \\ M_{cs,t} & M_{cs,t} & M_{cs,t} & M_{cs,t} & M_{cs,t} & L_{s,t} \end{bmatrix}. \tag{2.19}$$

This matrix is used to solve the identification problem posed by the different inductance measurements. As some of the involved equations are extremely long, only the final equations are directly presented as follows. Five measurement results are employed, while the sixth is only used for verification purposes.

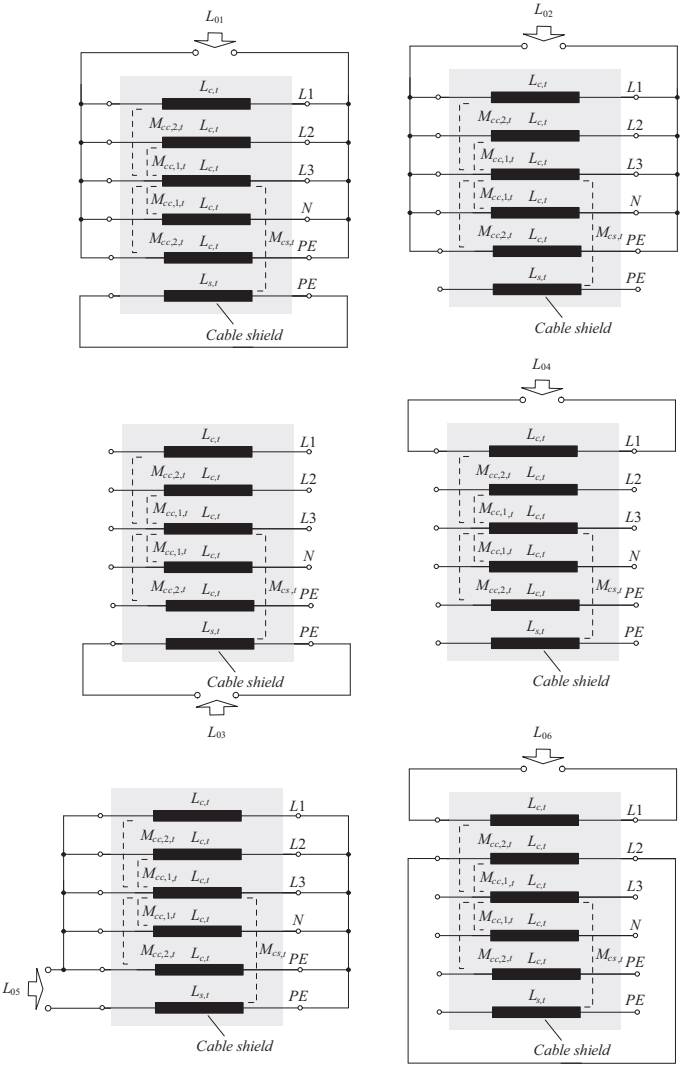


Figure 2.35: Motor cable measured inductances for the inductive network parameter identification. The t denotes the inductance values for the total cable length.

$$
\begin{aligned}
L_{c,t} &= L_{04} \\
L_{s,t} &= L_{03} \\
M_{cc,1,t} &= \sqrt{L_{04}^2 - L_{06}L_{03}} \\
M_{cc,2,t} &= \frac{5L_{02} - L_{04}}{2} - \sqrt{L_{04}^2 - L_{06}L_{03}} \\
M_{cs,t} &= \frac{L_{02} + L_{03} - L_{05}}{2}.
\end{aligned}
\tag{2.20}
$$

The measurements setups of Figure 2.36 are used for the identification of network capacitance values.

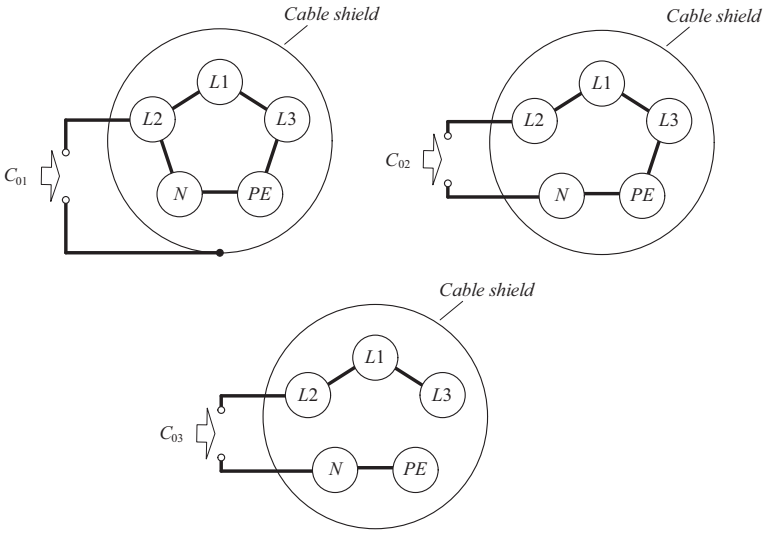


Figure 2.36: Motor cable measured impedances for the parameter identification of the capacitive network.

Again, the total capacitance values (sub-index "t") for the 36 m cable are obtained. From Figure 2.36 three linearly independent equations are derived,

$$
\begin{aligned}
C_{01} &= 5C_{cs,t} \\
C_{02} &= 2\left(C_{cc,1,t} + C_{cc,2,t}\right) + \frac{4C_{cs,t}}{5} \\
C_{03} &= 2C_{cc,1,t} + 4C_{cc,2,t} + \frac{6C_{cs,t}}{5}.
\end{aligned} \tag{2.21}
$$

Solving the system in eq. (2.21) leads to,

$$
\begin{aligned}
C_{cc,1,t} &= C_{02} - \frac{C_{03}}{2} - \frac{C_{01}}{25} \\
C_{cc,1,t} &= \frac{C_{03} - C_{02}}{2} - \frac{C_{01}}{25} \\
C_{cs,t} &= \frac{C_{01}}{5}.
\end{aligned} \tag{2.22}
$$

With this, the capacitances per meter are calculated by dividing the total capacitances by the total cable length:

$$
\begin{aligned}
C_{cc,1} &= \frac{C_{cc,1,t}}{l_{cable}} \\
C_{cc,2} &= \frac{C_{cc,2,t}}{l_{cable}} \\
C_{cs} &= \frac{C_{cs,t}}{l_{cable}},
\end{aligned} \tag{2.23}
$$

while the inductances are calculated with,

$$
\begin{aligned}
L_c &= \frac{L_{c,t}}{l_{cable}} \\
L_s &= \frac{L_{s,t}}{l_{cable}}
\end{aligned} \tag{2.24}
$$

and

$$\begin{aligned} M_{cc,1} &= \frac{M_{cc,1,t}}{l_{cable}} \\ M_{cc,2} &= \frac{M_{cc,2,t}}{l_{cable}} \\ M_{cs} &= \frac{M_{cs,t}}{l_{cable}}. \end{aligned} \tag{2.25}$$

The derived 6-lines cable transmission line model does not consider losses in the dielectric and skin effect. Series resistances are only measured for low-frequency and their measurement is straightforward. Dielectric materials are considered not to change permittivity with frequency.

The final values for all cable parameters are found in Table 2.9.

Table 2.9: Calculated input cable parameters.

Parameter	*Value*	*Unit*
Core self inductance	1.03	μH/m
Adjacent cores mutual inductance	1.00	μH/m
Non-adjacent cores mutual inductance	0.97	μH/m
Shielding self inductance	1.16	μH/m
Core-to-shield mutual inductance	1.07	μH/m
Adjacent cores capacitance	20.19	pF/m
Non-adjacent cores capacitance	2.32	pF/m
Core-to-shield capacitance	78.33	pF/m
Series resistance	6.88	mΩ/m

A circuit based on the presented model was implemented in a computer simulation by generating ten cable stages with lumped elements, instead of the distributed parameters of the transmission line model. A comparison between the measured impedances and the simulated ten-stage lumped circuit is shown in Figure 2.37. Good matching is observed validating the model for use in filter design calculations. The high frequency behavior ($>$ 10 MHz) of the cable is difficult to model due to material characteristics, skin effect and the electromagnetic environment where the cable is installed.

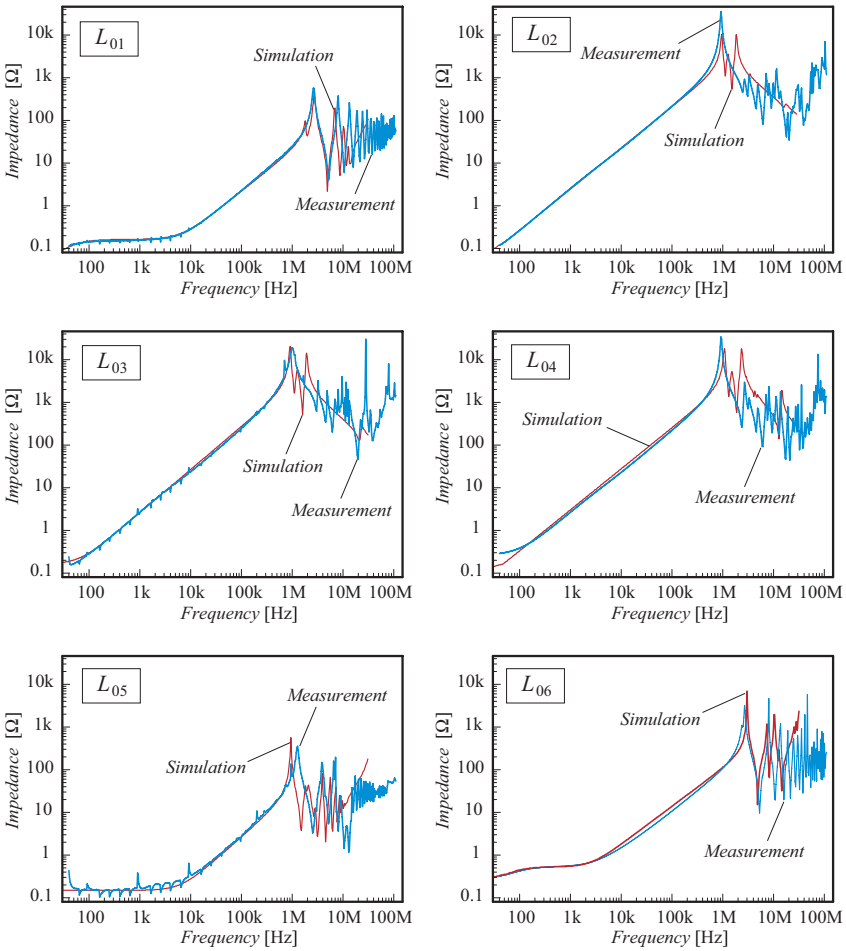


Figure 2.37: Comparison between six measured impedances in the motor cable and the results obtained with a ten-stage lumped equivalent circuit simulation.

2.7 Electric Machine Model for Conducted Emissions

Electromechanical machines are broadly employed in industry. Of special interest are the ac motors used when control over torque and speed are required in a processing industry. With the advantages of machines with higher speeds, there came the necessity of supplying voltages with variable frequency. Since the beginning of the 1900's [122], rotating converters[2] have been used to supply variable speed machines. In 1902, the first patent for a working mercury arc rectifier has been issued [123]. The first paper about an inverter appeared in 1925 [124], but is was not until the 1960's that static converters[3] supplanted rotating converters in large power industrial applications [125]. Since then, mercury arc valves have been replaced by power semiconductors (1970's) starting with low frequency static converters [123] and later on by high switching frequency PWM based converters [4].

PWM converter based ac drives have increased their share in the market due to clear advantages [53] over other technologies, namely: (*i*) very high efficiency; (*ii*) robustness to mains transients; (*iii*) high power factor; (*iv*) wide range of output frequencies; (*v*) small dimensions; (*vi*) ride-through capability; (*vii*) regeneration; (*viii*) ease of implementing protection circuits, and (*ix*) excellent control of torque and speed. Nevertheless, PWM converters present some side effects mainly due to the pulsed waveforms with rich spectral contents and very fast transient times [54].

Unlike dc motors, ac machines do not consist in a source of electrical noise alone, since commutators are not employed and arcing is not an issue in their construction. But, due to very compact designs of electrical ac motors, their windings are typically close to the chassis. This creates large distributed capacitances from the phases to the mechanical body of the machine, which for safety reasons shall be grounded. This capacitance allied with the pulsed voltages, which are applied to the machine's windings, generate common mode currents that find their way through earthing connections. Another concern is with the DM pulsed voltages applied across the windings. These voltages are fed through cables which,

[2]Converters employing an electric motor followed by a generator able to vary output frequency and voltage.

[3]Energy conversion equipment relying on electronic devices and not on electromechanical devices.

in general, do not present matched impedances with the motor's input impedances, thus generating oscillations and over-voltages as explained in Section 2.6.2. In order to properly address these effects, mathematical models for the machine shall be used [64]. These models are based on the geometric construction of the motor and vary in complexity and fidelity depending on the type of performed analysis.

As the geometrical complexity of a three-phase electric machine does not permit simple analytic models, two options are available: three dimensional simulation with EM field solvers and impedance measurements. The choice of the model shall be based on the required analysis, meaning that if detailed information about voltage and current distribution inside the machine is required, a complex 3-D model with distributed impedances is, most likely, the appropriate method. If only external currents and voltages are necessary, as it is the case for evaluating CE, lumped elements network should are sufficient [54].

In the case of a machine which is already designed using 3-D simulations, a model might be readily available and a circuital model can be created during the machine design phase. This option might prove to be efficient when the ac drive converter and the machine are designed by the same company, in a way that voltage and current stresses can be defined by design leading to an optimized configuration with low CM currents and over-voltages. At the moment, there is no reported activity in this direction in the literature. Unfortunately, the design group of a machine is usually located far away from the power converter design group. If the groups are from different companies, then the availability of a 3-D model is very limited, no to say that old machines might not even have one. For this reason, impedance measurements is the mainstream technique in motor modeling for conducted emissions [54, 60–72]. Another advantage of modeling through impedances is that thermal and electromagnetic effects can be included in the modeling in much shorter times.

The machine modeling can be divided into two parts, low frequency equivalent circuits containing where the back *emf* is in series with an equivalent inductance and, a high frequency one, called motor high frequency input impedance [61] or *surge* impedance [121].

Even though any electric machine is a complex network of distributed impedances, most of the models presented in the literature use lumped parameters. This is supported by the fact that most machines have dimensions which are inferior to 1 m, therefore much smaller than a wavelength

for 30 MHz, which is close to 10 m at free space.

A model based on the internal interconnections of a machine was proposed in [54]. Each of the phase-belts is modeled with a series inductance L_{bs} and resistance R_{bs} and a series RC connection R_{bg}, C_{bg} to the chassis. Capacitors C_{bb} connect the belt of different phases as shown in Figure 2.38. Coupling among the belts in a phase is considered as well. This network is able to model a high number of resonances and voltages across a phase/belt. The drawback of this model is that internal impedance measurements must be performed, requiring the disassembly of the machine or external access to all belt connections.

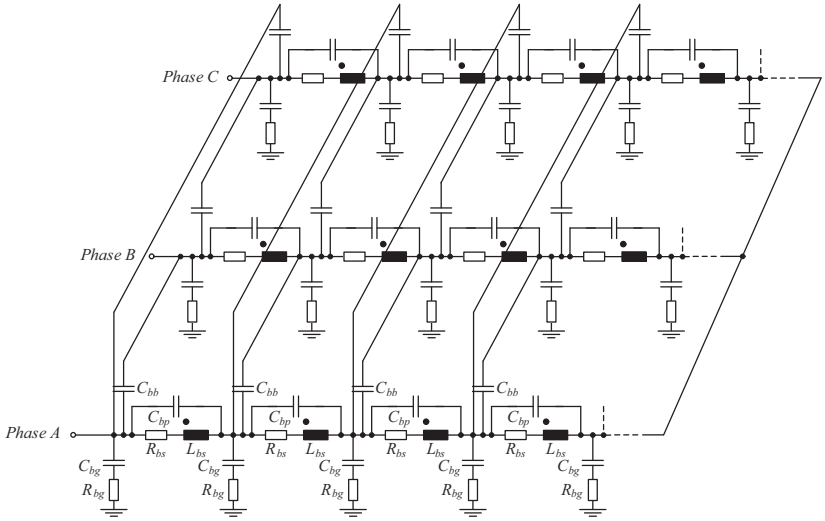


Figure 2.38: High frequency model for a three-phase motor as proposed in [54].

A simpler model is presented in [126], where circuits for the study of CM currents are proposed. Since this model is not valid for DM and it does not cope with higher order resonances it is not further considered here.

In [60, 66] the model shown in Figure 2.39 has been presented, which simplifies the model of Figure 2.38 [54]. This model shows good accuracy, even though it has no direct relation to all physical parameters of the phase-belts construction. This model is also referenced in [127], where

it is shown that it is capable of creating reproduceable curves, which match the impedance measurements of machines of different types and rated power well. It is also shown in [127] that small signal impedance measurements suffice in obtaining faithful HF impedance models. In [70] it is shown that the HF impedances are independent of the rotor position and can be derived through least-squares linear regression. Other models are presented in the literature [71,128,129] which include a higher number of circuit elements in order to model higher order resonances, skin effect and bearing currents, but these are not the main objectives of this work. As a conclusion of the literature survey, the presented models depend basically on the frequency range of interest and on the type of analysis required.

For the stated reasons, the model shown in Figure 2.39 represents the basis for the employed model, which is presented in Figure 2.40. It is seen that a series RL connection ($R_{s3} + L_{s3}$) is added in series to each phase of the previous networks. This circuit helps increasing the useful frequency range of the model by allowing a third resonance to be included as shown later in this section. Series inductances L_g are included to extend the frequency range of the CM model. The calculation of the model parameters is performed through a parameter identification routine explained in the following.

As seen in Figure 2.40, the electric machine is modeled as a four terminal network. Schematically it is displayed in Figure 2.41, from where its admittance matrix $\mathbf{Y}_{motor}$ can be defined and used for the solution of the identification problem.

A general matrix equation for the motor's admittance matrix $\mathbf{I}_{motor}$ is defined as,

$$\begin{aligned} \mathbf{I}_{motor} &= \mathbf{Y}_{motor} \cdot \mathbf{U}_{motor} \\ \begin{bmatrix} i_A \\ i_B \\ i_C \\ i_{PE} \end{bmatrix} &= \begin{bmatrix} y_{1,1} & y_{1,2} & y_{1,3} & y_{1,4} \\ y_{2,1} & y_{2,2} & y_{2,3} & y_{2,4} \\ y_{3,1} & y_{3,2} & y_{3,3} & y_{3,4} \\ y_{4,1} & y_{4,2} & y_{4,3} & y_{4,4} \end{bmatrix} \cdot \begin{bmatrix} u_A \\ u_B \\ u_C \\ u_{PE} \end{bmatrix} \end{aligned} \tag{2.26}$$

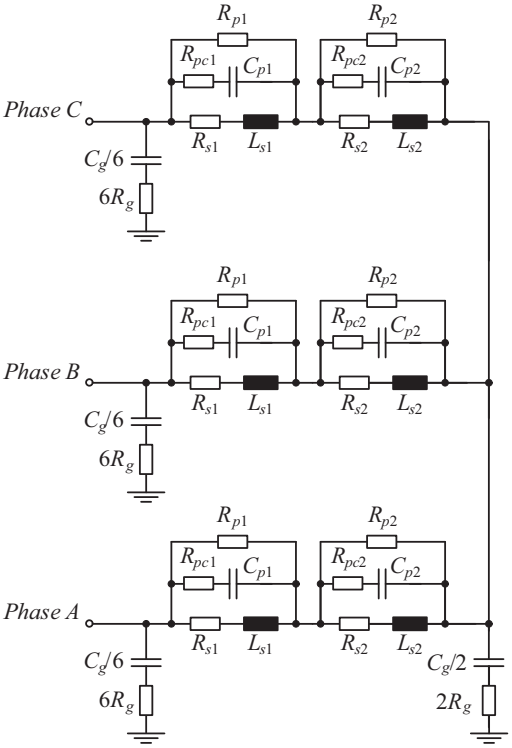


Figure 2.39: High frequency model for a three-phase motor as proposed in [60, 66].

The model shown in Figure 2.40 consists of 13 variables. For having a completely defined system, at least seven impedance measurements, in a total of seven amplitude plus seven phase curves, shall be performed. This would lead to a complex system of equations and difficult mathematical solutions. To simplify the problem, information can be retrieved from observed resonance frequencies, dominant impedances for a frequency range and circuit knowledge. Consequently, the total number of impedance measurements can be reduced. Even two impedance measurements are reported in literature [54,67] being enough for the identification. For the case at hand, more parameters are considered, thus, four impedance measurements are performed according to the test setups shown in Figure 2.42.

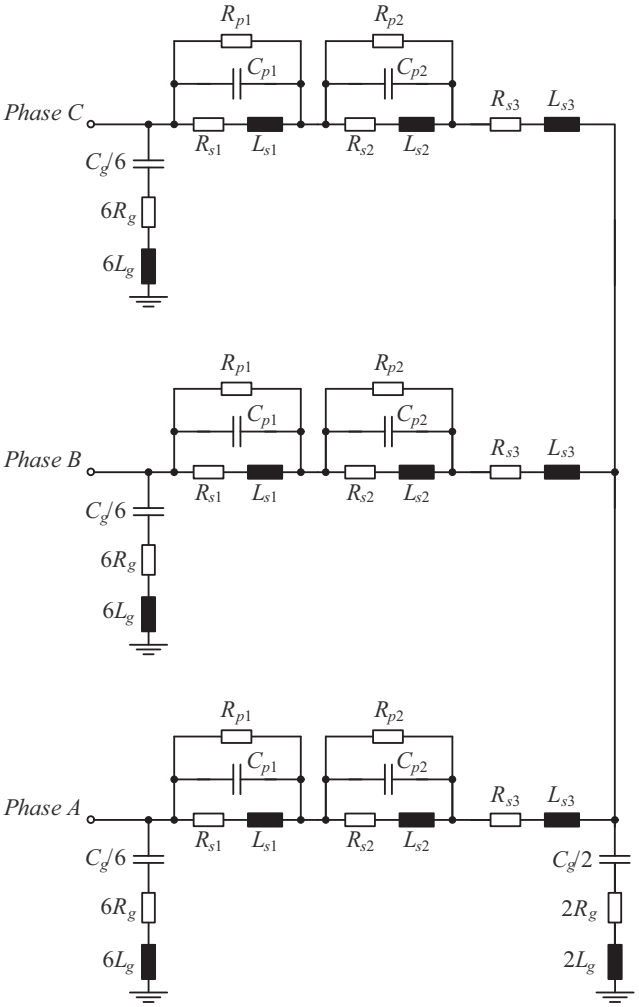


Figure 2.40: High frequency model for a three-phase motor used in this work.

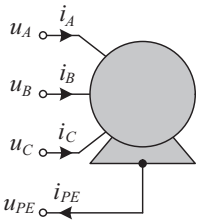


Figure 2.41: Definition of voltages and currents in the motor model.

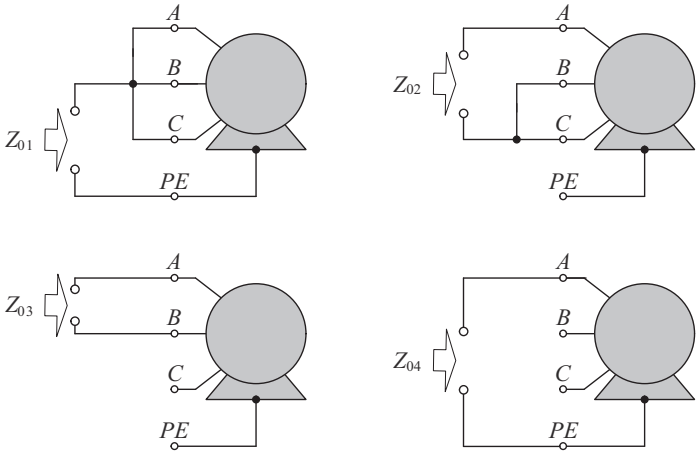


Figure 2.42: Impedance measurement setups for the identification of the motor parameters.

Solving the circuits of Figure 2.42 and considering the admittance

matrix of the circuit, it follows that,

$$Z_{01} = \frac{1}{y_{1,1} + y_{1,2} + y_{1,3} + y_{2,1} + y_{2,2} + y_{2,3} + y_{3,1} + y_{3,2} + y_{3,3}} \tag{2.27}$$

$$Z_{02} = \frac{y_{4,4}}{y_{1,1}y_{4,4} + y_{1,4}y_{4,1}} \tag{2.28}$$

$$Z_{03} = \frac{y_{3,3}y_{4,4} - y_{3,4}y_{4,3}}{y_{1,1}\left(y_{3,3}y_{4,4} - y_{3,4}y_{4,3}\right) + y_{1,3}\left(y_{4,1}y_{3,4} - y_{4,4}y_{3,1}\right) + \cdots \overline{+y_{1,4}\left(y_{4,3}y_{3,1} - y_{3,3}y_{4,1}\right)}} \tag{2.29}$$

$$Z_{04} = \frac{y_{2,2}y_{3,3} - y_{2,3}y_{3,2}}{y_{1,1}\left(y_{2,2}y_{3,3} - y_{3,2}y_{2,3}\right) + y_{1,2}\left(y_{3,1}y_{2,3} - y_{3,3}y_{2,1}\right) + \cdots \overline{+y_{1,3}\left(y_{3,2}y_{2,1} - y_{2,2}y_{3,1}\right)}}. \tag{2.30}$$

Defining the following impedances from the branch impedances of Figure 2.40 as,

$$Z_1 = R_{s1} + sL_{s1} \tag{2.31}$$

$$Z_2 = \frac{1}{\frac{1}{R_{p2}} + sC_{p2} + \frac{1}{R_{s2}+sL_{s2}}} \tag{2.32}$$

$$Z_3 = \frac{1}{\frac{1}{R_{p3}} + sC_{p3} + \frac{1}{R_{s3}+sL_{s3}}} + Z_1 \tag{2.33}$$

$$Z_4 = 6R_g + \frac{6}{sC_g} + 6sL_g. \tag{2.34}$$

The admittance matrix elements, which define the motor network, are given as,

$$y_{1,1} = \frac{3Z_2^2 + 6Z_2(Z_3 + Z_4) + 3Z_3^2 + 6Z_3Z_4 + 2Z_4^2}{3Z_4\left[Z_2^2 + Z_3^2 + Z_3Z_4 + (2Z_3 + Z_4)\right]} \tag{2.35}$$

$$y_{1,2} = \frac{-Z_4}{3\left[Z_2^2 + Z_3^2 + Z_3Z_4 + (2Z_3 + Z_4)\right]} \tag{2.36}$$

$$y_{1,3} = y_{2,1} = y_{2,3} = y_{3,1} = y_{3,2} = y_{1,2} \tag{2.37}$$

$$y_{1,4} = \frac{Z_2 + Z_3 + 4Z_4}{Z_4(Z_2 + Z_3 + Z_4)} \tag{2.38}$$

$$y_{2,2} = y_{3,3} = y_{1,1} \tag{2.39}$$

$$y_{4,1} = y_{4,2} = y_{4,3} = y_{1,4} \tag{2.40}$$

$$y_{4,4} = \frac{-3(Z_2 + Z_3 + 4Z_4)}{Z_4(Z_2 + Z_3 + Z_4)}. \tag{2.41}$$

The electric motor employed in the CE tests for the case at hand is a three-phase asynchronous machine manufactured by Otto Bartholdi AG of model HAC 145 S 08 U2/RA rated for 2 kW / 330 V / 5.37 A / $\cos\phi = 0.77$. Measuring the impedances of this machine as given in Figure 2.42 leads to the curves shown in Figure 2.43, where the frequency ranges (*LF area, HF area*) and the resonance frequencies (f_1, f_2 and f_3) are defined. These ranges and frequencies are used to acquire information on the dominant effects that define the impedances. The measurements were performed on three different configurations, exchanging the terminals A, B and C, except for Z_{01}. The shown results are an average of the three measurements, where the consideration of symmetric networks for the three phases is done throughout the identification procedure.

For the *LF area* the following variables are defined,

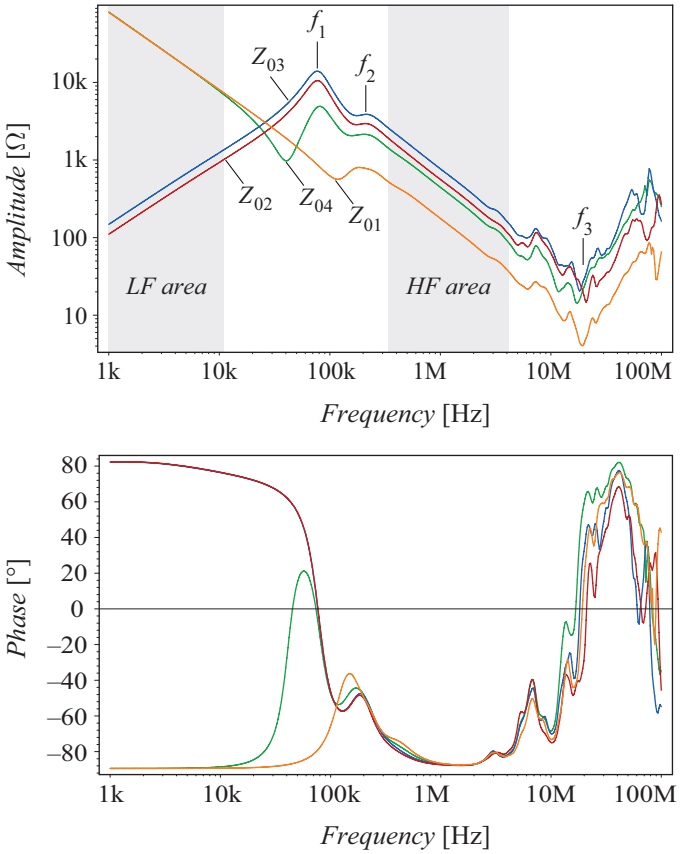


Figure 2.43: Impedance measurement results.

$$C_{LF} = \frac{1}{2\pi f\,|Z_{01}|\sin(\angle Z_{01})} \cong \frac{1}{2\pi f\,|Z_{04}|\sin(\angle Z_{04})} \tag{2.42}$$

$$L_{LF} = 2\pi f\,|Z_{02}|\sin(\angle Z_{02}) \cong \frac{8\pi f\,|Z_{03}|\sin(\angle Z_{03})}{3} \tag{2.43}$$

$$R_{LF} = |Z_{02}|\cos(\angle Z_{02}) \cong \frac{4\,|Z_{03}|\cos(\angle Z_{03})}{3}. \tag{2.44}$$

As it is observed in Figure 2.43, the impedance curves for Z_{02} and Z_{03} in the *LF area* do not increase at a 20 dB (10 times) per decade rate as expected from a pure inductance. Therefore, the impedances present a strong dependency with frequency. For this reason the variables L_{LF} and R_{LF} are curve fitted, while C_{LF} is approximately constant. These are defined as,

$$L_{LF}(f) \cong \frac{5.476\,\mathrm{H}\,\left(623.237 \cdot 10^{-6} f + 1\right)^{2.302}}{\left(37.606 \cdot 10^{-6} f + 1\right)^{2.763}} \tag{2.45}$$

$$R_{LF}(f) \cong \frac{18.807 \cdot 10^{-3}\,\Omega}{\left(988.349 \cdot 10^{-6} f + 1\right)^{0.106} \left(166.667 \cdot 10^{-9} f + 1\right)^{4.000}} \tag{2.46}$$

$$C_{LF} \cong 1.994\,\mathrm{nF}. \tag{2.47}$$

For the *HF area*, an equivalent capacitance C_{HF} can be defined as the series connection of two capacitances C_1 and C_2, which are a combination of C_{p1} and C_{p2} as shown later in this section. This capacitance is defined as,

$$C_{HF} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}}. \tag{2.48}$$

At the highest impedance peak of Z_{02}, the first resonance frequency f_1 is defined,

$$f_1 = \frac{1}{2\pi\sqrt{L_1 C_1}} \cong 76.5\,\mathrm{kHz}. \tag{2.49}$$

The second resonance frequency f_2 is defined,

$$f_2 = \frac{1}{2\pi\sqrt{L_2 C_2}} \cong 211.2\,\mathrm{kHz}. \tag{2.50}$$

Finally, the third resonance f_3 takes place at the minimum impedance measured for Z_{01},

$$f_3 = \frac{1}{2\pi\sqrt{L_3 C_3}} \cong 20.827\,\text{MHz}. \tag{2.51}$$

For frequencies much lower than f_3 the impedance measurements Z_{02} and Z_{03} are dominated by the series connection of the serial branches composed of R_{s1}, L_{s1}, R_{s2}, L_{s2}, R_{p1}, C_{p1}, R_{p2} and C_{p2}. Thus, they can be considered in a simplified network as shown in Figure 2.44.

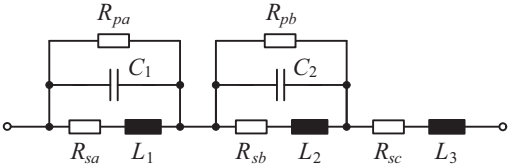


Figure 2.44: Simplified network to derive values of resistances, inductances and capacitances with Z_{02}.

Defining a total inductance as,

$$L_{total} = L_1 + L_2 \cong L_{LF}(f) \tag{2.52}$$

and observing Figure 2.44 leads to the relations:

$$C_1 = \frac{C_{HF}\left[(2\pi f_2)^2 - (2\pi f_1)^2\right]}{\left[L_{total} C_{HF}(2\pi f_2)^2 - 1\right](2\pi f_1)^2} \tag{2.53}$$

$$L_1 = \frac{L_{total} C_{HF}(2\pi f_2)^2 - 1}{C_{HF}\left[(2\pi f_2)^2 - (2\pi f_1)^2\right]} \tag{2.54}$$

$$C_2 = \frac{C_{HF}\left[(2\pi f_2)^2 - (2\pi f_1)^2\right]}{\left[L_{total} C_{HF}(2\pi f_1)^2 - 1\right](2\pi f_2)^2} \tag{2.55}$$

$$L_2 = \frac{L_{total} C_{HF}(2\pi f_1)^2 - 1}{C_{HF}\left[(2\pi f_2)^2 - (2\pi f_1)^2\right]}. \tag{2.56}$$

The value of inductance L_{total} is L_{LF}, but it is frequency dependent.

Thus, the value of the fitted function at the respective resonance frequency is chosen, so that,

$$C_1 = \frac{C_{HF}\left[(2\pi f_2)^2 - (2\pi f_1)^2\right]}{\left[L_{LF}(f_1)C_{HF}(2\pi f_2)^2 - 1\right](2\pi f_1)^2} \cong 398.6\,\mathrm{pF} \tag{2.57}$$

$$L_1 = \frac{L_{LF}(f_1)C_{HF}(2\pi f_2)^2 - 1}{C_{HF}\left[(2\pi f_2)^2 - (2\pi f_1)^2\right]} \cong 10.853\,\mathrm{mH} \tag{2.58}$$

$$C_2 = \frac{C_{HF}\left[(2\pi f_2)^2 - (2\pi f_1)^2\right]}{\left[L_{LF}(f_2)C_{HF}(2\pi f_1)^2 - 1\right](2\pi f_2)^2} \cong 762.1\,\mathrm{pF} \tag{2.59}$$

$$L_2 = \frac{L_{LF}(f_2)C_{HF}(2\pi f_1)^2 - 1}{C_{HF}\left[(2\pi f_2)^2 - (2\pi f_1)^2\right]} \cong 443.9\,\mu\mathrm{H}. \tag{2.60}$$

The total capacitance from the phases to ground can be derived for the *LF area* of measurement Z_{01}, which is,

$$C_g = C_{LF} \cong 1.994\,\mathrm{nF}. \tag{2.61}$$

At the first resonance, the parallel resistance R_{pa} of the first impedance branch dominates the impedance value of Z_{02}, while the parallel resistance R_{pb} of the second impedance branch dominates the impedance value of Z_{02} at the second resonance. This leads to the relations,

$$R_{pa} = |Z_{02}|\,(f_1) \cong 10.53\,\mathrm{k\Omega} \tag{2.62}$$

$$R_{pb} = |Z_{02}|\,(f_2) \cong 2.95\,\mathrm{k\Omega}. \tag{2.63}$$

For the evaluation of the series resistances R_{sa} and R_{sb} for the *LF area* the ratio of the inductances is used,

$$R_{sa} = R_{LF}(10\,\text{kHz})\frac{L_1}{L_1 + L_2} \cong 203.57\,\Omega \tag{2.64}$$

$$R_{sb} = R_{LF}(10\,\text{kHz})\frac{L_2}{L_1 + L_2} \cong 8.33\,\Omega. \tag{2.65}$$

At the third resonance, the impedance of Z_{02} is dominated by the series resistance R_{sc}, from where,

$$R_{sc} = |Z_{02}|\,(f_3) \cong 14.71\,\Omega. \tag{2.66}$$

Inductance L_3 can be found by the series resonant circuit composed of capacitors C_1 and C_2 and L_3, so that,

$$L_3 = \frac{1}{(2\pi f_3)^2 C_{HF}} \cong 192.13\,\text{nH}. \tag{2.67}$$

Comparing the networks of Figure 2.44 and Figure 2.40 the values of the components can be defined as,

$$R_{s1} = \frac{2}{3} R_{sa} \cong 135.71\,\Omega \tag{2.68}$$

$$L_{s1} = \frac{2}{3} L_1 \cong 7.235\,\text{mH} \tag{2.69}$$

$$R_{p1} = \frac{2}{3} R_{pa} \cong 7.02\,\text{k}\Omega \tag{2.70}$$

$$C_{p1} = \frac{3}{2} C_1 \cong 597.9\,\text{pF} \tag{2.71}$$

$$R_{s2} = \frac{2}{3} R_{sb} \cong 5.55\,\Omega \tag{2.72}$$

$$L_{s2} = \frac{2}{3} L_2 \cong 295.93\,\mu\text{H} \tag{2.73}$$

$$R_{p2} = \frac{2}{3} R_{pb} \cong 1.97\,\text{k}\Omega \tag{2.74}$$

$$C_{p2} = \frac{3}{2} C_2 \cong 1.143\,\text{nF} \tag{2.75}$$

$$R_{s3} = \frac{2}{3} R_{sc} \cong 9.81\,\Omega \tag{2.76}$$

$$L_{s3} = \frac{2}{3} L_3 \cong 128.09\,\text{nH}. \tag{2.77}$$

Based on the third resonance and the known value of C_g, the value of the inductance L_g can be found,

$$L_g = \frac{1}{(2\pi f_3)^2 C_g} \cong 29.19\,\text{nH}. \tag{2.78}$$

Finally, the value of the resistance R_g can be derived from the impedance of Z_{01} at the third resonance, leading to,

$$R_g = |Z_{01}|\,(f_3) \cong 4.0\,\Omega. \tag{2.79}$$

In practice, some of the values required corrections and the final values of the elements are presented in Table 2.10.

Table 2.10: Final values for the components of the motor model.

Component	*Value*
R_{s1}	135 Ω
L_{s1}	7.2 mH
R_{p1}	7.5 kΩ
C_{p1}	590 pF
R_{s2}	5.5 Ω
L_{s2}	495 μH
R_{p2}	2.3 $k\Omega$
C_{p2}	1.15 nF
R_{s3}	9.8 Ω
L_{s3}	128 nH
R_g	3.0 Ω
L_g	38.8 nH
C_g	2.0 nF

Based on the values of Table 2.10 and the schematics shown in Figure 2.40 the model can be compared to the measured impedances. This is done in the impedance curves shown in Figure 2.45 and Figure 2.46. These figures show the impedances obtained with the test setups presented in Figure 2.42 for, both, measurements and circuit simulation.

With the comparison done in Figure 2.45 and Figure 2.46 it is observed that the high number of structural resonances can not be completely modeled. The high frequency structural resonances can not be modeled due to the relatively low order of the machine's models (cf. Figure 2.40), while the small differences in the resonances located in the range from 100 kHz to 1 MHz can be explained with the asymmetries observed between the impedances of the three motor phases.

Regardless of the noticed differences, a very good agreement in all impedance curves is seen, which validates the use of this model for conducted emission analysis.

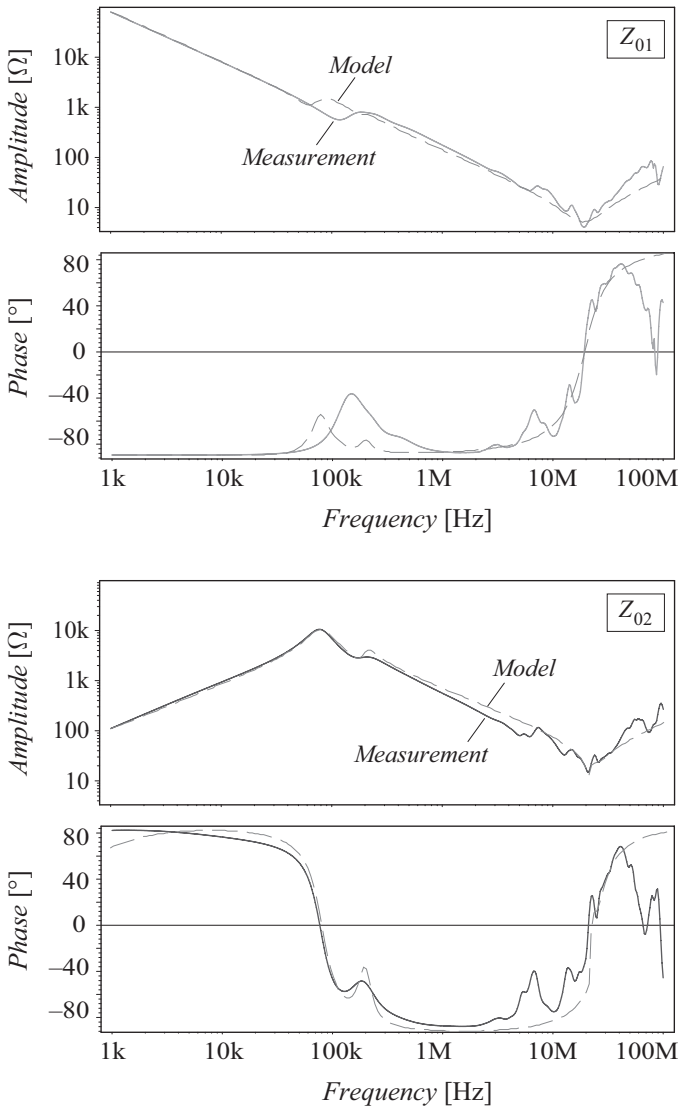


Figure 2.45: Comparison of impedance measurements Z_{01} and Z_{02} with the presented machine model.

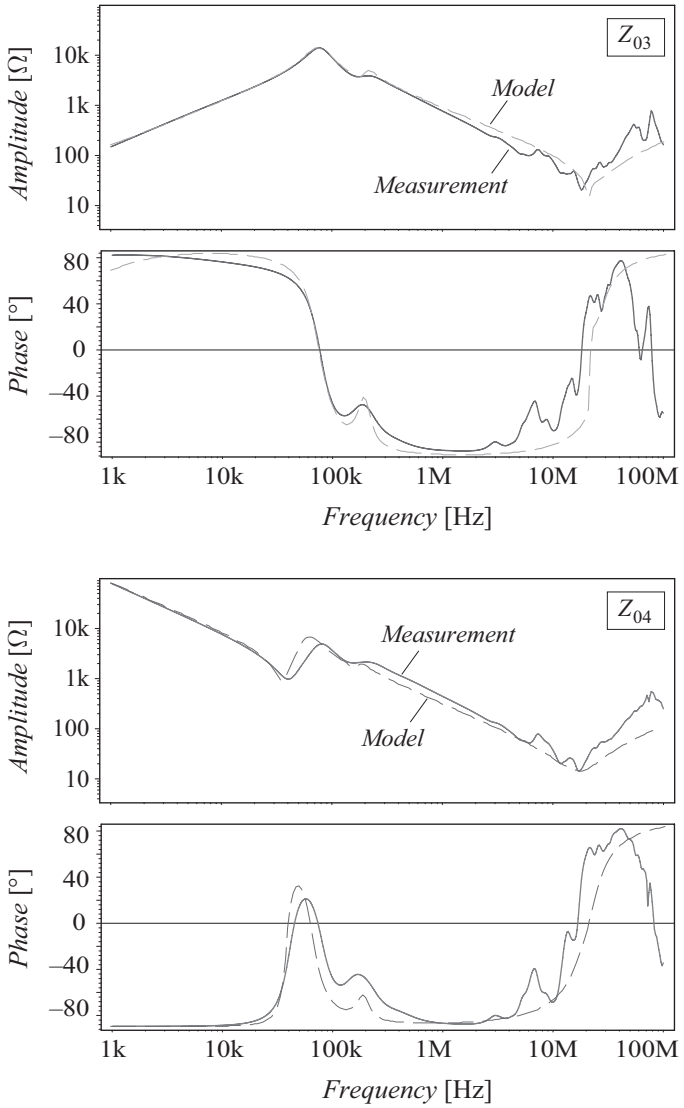


Figure 2.46: Comparison of impedance measurements Z_{03} and Z_{04} with the presented machine model.

2.8 Summary

This work focuses on the control of conducted emissions from three-phase power converters through proper HF filtering aiming for EMC. Detailed information on the electrical environment where a power filter is connected to is paramount to filter design. The requirements for the filter components and practical installations can vary in large extent due to voltage ratings, power distribution transformers connections and earthing techniques.

The scope of the work is limited to low voltage supplied systems, where earthing practices dictate specific requirements for EMC filtering. Earthing connections generate current paths through which HF electrical noise can flow and, thus creating a potential problem for EMC. Nevertheless, earthing is mandatory due to safety and fault protection reasons. Thus, the functionality problem generated by earth connections can not be solved by avoiding these connections.

The first step towards a filter design is the knowledge about its installation. The connections and voltage levels in LV power distribution systems might vary in great extent. This requires different voltage ratings for filtering components, possible asymmetries in the circuits, alternatives for installing multiple (one per equipment) or single (one per installation) filters, environmental conditions and safety requirements. Safety standards should be observed, since they imply in direct requirements for the components of a power filter. The main requirements from safety aspects are summarized as: maximum earth leakage currents, behavior during faults, insulation levels, clearance and creepage distances between conductors and components.

Equipments are tested for conducted emissions in electrical environments that are defined in EMC standards. Only civil standards are considered here. These standards clearly specify the physical disposition of measuring apparatus, ground planes, cables and the equipment under test (EUT). Interface equipments (LISN) are also defined, providing well controlled impedances and the interface between an EUT and a test receiver. Different electrical models for a standard LISN were shown, which provide different degrees of accuracy. A complete model requires more components, thus more complexity, while simplified models are appropriate for the evaluation of HF emissions in a filter design phase.

Standards also specify the type of measurements that are carried out

with an EMC test receiver. These measurements are performed with a complex system presenting results in frequency domain. Different types of detectors are used, but for conducted emission testing, peak, quasi-peak and average detectors are specified. A model for the complete frequency domain measurement chain was presented, including the non-linearities of the QP detector. In order to simplify numeric calculations in a computer, a range was proposed which covers the minimum and maximum values which can be measured with the QP detector. With this, the computational effort is reduced and safe margins are provided for a filter design.

The interconnection between the three-phase PWM converter and the LISN or power grid is typically done with a four- to five- conductors cable. This cable is of high importance for high frequencies since it may attenuate noise or generate harmful resonances with an input filter. A distributed parameters model for a five-conductor cable was presented and confirmed through comparison among several impedance measurements.

For rectifier systems, a dc load is expected to be downstream connected and this is difficult to specify before hand. Typically, long cables are not employed at the dc output. Therefore, output cables are not modeled for PWM rectifiers and specific load modeling shall be done depending on the type of load, switched, passive, pulsed and so on, connected to the rectifier's output. For the case of ac-to-ac converters used as ac motor drives, the motor cable is of high importance since it can be very long. This generates a complex impedance matrix which might be responsible for high noise currents. Cable shielding is typically employed in order to control radiated emissions. A model for a five-conductors plus shielding is presented, which is based on "per unit length" parameters obtained through a parameter identification procedure. Numeric simulations results with this model are compared with impedance measurements, where good agreement is observed to frequencies up to 30 MHz.

Electric machines represent typical loads for three-phase PWM converters. These machines are a complex network of distributed impedances and difficult to completely model. Lumped elements based models are proposed in the literature that are specific for different types of analysis, including conducted emissions generation. Based on a literature survey, a model for a 2 kW asynchronous machine is derived. The parameter identification routine is explained in detail and, again, impedance measurements are compared with simulation results demonstrating very good tuning of the parameters.

This chapter has presented the detailed modeling of the main components of a conducted emissions test setup, including LISNs, test receivers, cables and load. The modeling allows for the estimation of HF noise components generated by a PWM converter, so that the evaluation of both, filter attenuation requirements and filter performance prior to the construction of a prototype, having the potential of lowering the design costs and the required number of prototypes.

Chapter 3

Modeling of Three-Phase PWM Converters as Noise Sources

"When the river is deepest,
it makes least noise." Proverb

3.1 Introduction

Three-phase PWM converter systems are frequently employed as front-end (rectifiers) or direct conversion (matrix converters) power stages in utility interfaced systems such as power supplies for telecommunication systems, process technology and AC drive applications. They are commercially and technically attractive for presenting smaller dimensions, lower cost and improved electrical performance when compared to mains frequency switched three-phase converters, diode bridges, thyristor bridges or cycloconveters. On the other hand, PWM converters are, in general, less robust and generate voltages and currents with rich high frequency harmonic contents, thus being known sources of HF noise.

The PWM converters, for which input EMC filters are studied in this work, are:

i. Three-Phase Buck+Boost PWM Rectifiers [130];

ii. Three-Phase Three-Level Boost PWM Rectifiers [77, 131]; and,

iii. Three-Phase Sparse Matrix Converters [85, 88].

All PWM converters have in common that square-type pulses are applied to the input port of semiconductor switching devices. These square-wave pulses present time varying duty-cycles which turn the semiconductors on and off in a coherent way. This way, the required modulation pattern is applied and the desired energy transference and control are accomplished. This ensures that very low losses are inherent to the energy processing scheme and high efficiencies are observed. The side effect of this process is the generation of harmonic contents at the multiples of the switching frequency with side-bands that depend on modulation strategies and involved low-frequency waveforms. This is the basic noise generation mechanism for PWM converters.

The proper identification of the noise spectra allows, together with the determination of noise paths, for the early determination of filtering requirements and possibilities, thus, an efficient filter design work-flow. For the specific case of three-phase converters the exact analytic calculation of such spectral contents is of high complexity [132, 133] and sometimes varying upon operating conditions such as energy regeneration, low or high modulation indexes and load. Therefore, simplifications are usually performed for the determination of relevant spectra. Other methods include numerical simulation with varying degree of complexity and direct hardware measurements.

The EMC modeling of power converters based on direct hardware measurements [64, 134–137] has, over all other methods, the tremendous advantage of including all electromagnetic and thermal effects involved in the system. The obvious disadvantages of this type of modeling are the difficulties of implementing modifications and the uncertainties of not knowing exactly which mechanisms generate the observed effects. In a last step before EMC certification this method is, of course, employed and the engineering skills of the designers are required to assess the compliance of the equipment or to realize required improvements when necessary. Different techniques with varying degrees of complexity are employed in this method, such as:

- conducted emissions testing;

- identification of dominant noise modes through noise separators (see section 5);
- use of electric and/or magnetic field probes;
- impedance measurements;
- oscilloscope acquisitions;
- spectrum analyzer measurements of various variables, including zero-span mode;
- network analyzer, including measurements of insertion loss and S-parameters;
- current transducers;
- thermal measurements;
- mechanical modifications, including variations of electrical connections and shielding;
- change of components and materials;
- visual inspection and others.

Computer based simulations is another wide spread method of modeling Power Electronics systems. These simulations differ in modeling complexity, typically, proportionally with the applied efforts. Simulations aiming for EMC purposes might model a multi-physics environment involving three-dimensional electromagnetic filed solvers, heat flow dynamics, control strategies, calculations of losses and electric circuits solvers. These simulations are not yet common, since the computational effort is immense. Most of today's applications perform more than one type of simulation neglecting to some extent the couplings among different physical domains. For instance, a circuit simulator might generate the currents which are to be applied in a simplified 3-D model for finding the electric field in the surroundings of the converter, while the measured losses are used to dimension a required cooling system. Again, different complexity can be used depending on the objective of the simulation. The advantages of numerical simulations are the easiness of modifying important parameters, reduced costs and study of the effects of each part of the circuit.

The precision of a simulation relies not only on the software, but most importantly in the construction of the model.

In practice, the three approaches (analytic calculation, experiments and simulation) might be coupled together in different design stages. The proper management and coordination of these tasks, allied to practical experience, usually leads to appropriate models and subsequent EMC compliance. In the following section different examples of the application of these techniques are presented, where the main objective is to establish models that provide reliable data for the design of EMC filters for three-phase PWM converters.

In this chapter, examples of the three approaches are employed in the modeling of the aforementioned power converters, aiming for the efficient design of EMC filters.

3.2 Basics on Spectral Contents of PWM Waveforms

It is well known that periodic functions can be decomposed into other periodic functions, called *basis functions*. The basis functions are typically simpler than the original function and have the same period or sub-multiples of the original period. With this, complex signals can be decomposed into simple functions that are advantageous to work with from a mathematical perspective. Considering linear systems, the principle of superposition can be used so that the effects of each basis function can be summed in order to obtain the total response of the system. In Electrical Engineering the most used basis functions are the sinusoids leading to the Fourier transformation. This is illustrated in Figure 3.1, where it is seen that the originally distorted signal S is decomposed into five sinusoids, which are simply defined by their peak value, frequency and phase. Furthermore, the energy associated with each sinusoidal signal is well understood.

The Fourier transformation is mathematically defined with,

$$S(t) = 2c_0 + \sum_{n=1}^{\infty} |c_n| \cos\left(n\omega_0 t + \angle c_n\right), \tag{3.1}$$

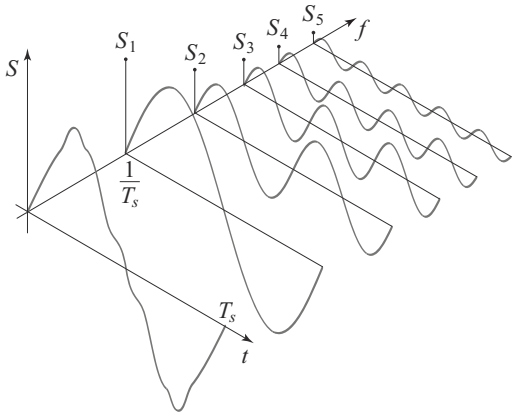


Figure 3.1: Decomposition of repetitive signal of period T_s into a sum of sinusoids with harmonic frequencies at the multiples of the fundamental frequency.

where c_n are the complex-exponential expansion coefficients considering only positive frequencies, so that their magnitude is double. The fundamental angular frequency is defined as $\omega_0 = 2\pi f$. By using Euler's identity,

$$\cos\theta = \frac{e^{j\theta} + e^{-j\theta}}{2} \tag{3.2}$$

$$\sin\theta = \frac{e^{j\theta} - e^{-j\theta}}{2j} \tag{3.3}$$

this sum of complex-exponentials returns to the sum of real and sinusoidal functions. The complex-exponential expansion coefficients are typically easier to derive than the trigonometric coefficients.

The expansion coefficients are calculated with,

$$c_n = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} S(t)e^{-j\,n\omega_0\,t}dt, \tag{3.4}$$

and, for $n = 0$ it follows that the coefficient is the average value of the signal $S(t)$ in a period,

$$c_0 = \frac{1}{T_s} \int_{t_0}^{t_0+T_s} S(t)\, dt. \tag{3.5}$$

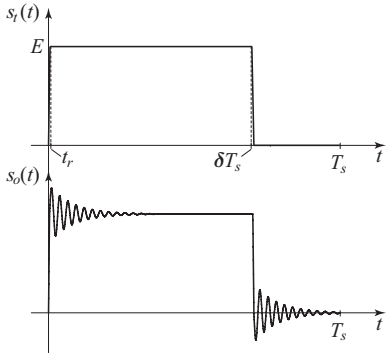


Figure 3.2: Analyzed signals.

Considering two signals, a trapezoid with constant duty-cycle and equal rise and fall times and another one with superposed oscillations, as depicted in Figure 3.2 and defined with,

$$s_t(t) = \begin{cases} \frac{E}{t_r} t, & 0 \le t \le t_r \\ E, & t_r \le t \le \delta T_s \\ \frac{E}{t_r} \left(t - \delta T_s - t_r\right), & \delta T_s \le t \le \delta T_s + t_r \\ 0, & \delta T_s + t_{rise} \le t \le T_s \end{cases} \tag{3.6}$$

and,

$$s_o(t) = \begin{cases} \frac{E}{t_r} t, & 0 \le t \le t_r \\ E + U_o e^{-\alpha t} \sin\left[2\pi f_o \left(t - t_r\right)\right], & t_r \le t \le \delta T_s \\ \frac{E}{t_r} \left(t - \delta T_s - t_r\right), & \delta T_s \le t \le \delta T_s + t_r \\ -U_o e^{-\alpha(t - \delta T_s - t_r)} \sin\left[2\pi f_o \left(t - t_r - \delta T_s\right)\right], & \delta T_s + t_r \le t \le T_s \end{cases}. \tag{3.7}$$

The expansion coefficients for these two signal are given by,

$$c_{s_t,n} = \delta E \frac{\sin(\frac{1}{2} n\omega_0 \delta\, T_s)}{\frac{1}{2} n\omega_0 \delta\, T_s} \frac{\sin(\frac{1}{2} n\omega_0 t_r)}{\frac{1}{2} n\omega_0 t_r} e^{\frac{-j\, n\, \omega_0 (\delta\, T_s + t_r)}{2}}, \tag{3.8}$$

and,

$$\begin{aligned} c_{s_o,n} = E \left[\delta\, T_s + \frac{t_r}{2}\left(e^{\frac{-j\,2n\pi\,t}{T_s}} - 1\right)\right] + \Big[j\, U_o\, \alpha \Big(-e^{-(j\,2\pi\, f_o + \alpha)[T_s(1-\delta) - t_r]} + \\ + e^{(-j\,2\pi\, f_o + \alpha)[T_s(1-\delta) - t_r]} + e^{-\delta\, T_s (j\,2\pi\, f_o + \alpha) + j\,2\pi\, t_r\, f_o - \frac{j\,2\pi\, n\, t}{T_s}} + \\ - e^{\delta\, T_s (j\,2\pi\, f_o - \alpha) - j\,2\pi\, t_r\, f_o - \frac{j\,2\pi\, n\, t}{T_s}}\Big) - 2\pi\, U_o\, f_o \Big(+e^{-(j\,2\pi\, f_o + \alpha)[T_s(1-\delta) - t_r]} + \\ + e^{(-j\,2\pi\, f_o + \alpha)[T_s(1-\delta) - t_r]} - e^{-\delta\, T_s (j\,2\pi\, f_o + \alpha) + j\,2\pi\, t_r\, f_o - \frac{j\,2\pi\, n\, t}{T_s}} + \\ - e^{\delta\, T_s (j\,2\pi\, f_o - \alpha) - j\,2\pi\, t_r\, f_o - \frac{j\,2\pi\, n\, t}{T_s}} - 2\, e^{\frac{j\,2\pi\, n\, t}{T_s} + \alpha\, t_r} + 2\Big)\Big] \frac{1}{2} \frac{1}{\alpha^2 + 4\pi^2 f_o^2}. \end{aligned} \tag{3.9}$$

Signals $s_t(t)$ and $s_o(t)$ can model to some extent the behavior of switched voltages and are very common waveforms in the study of Power Electronics systems. The signal $s_o(t)$ has the capability of modeling overvoltages and oscillations that occur during on/off transitions of turn-off semiconductor switches. However, it is seen that the calculation of the expansion coefficients leads to a complex expression that does not provide much insight into the physics of the signal. Furthermore, the coefficients employed to model the signal $s_o(t)$ typically depend strongly in the circuit topology, semiconductor characteristics, gate drivers, operating currents, voltages and temperature and parasitic elements. The actual waveforms are more complex and the calculation of Fourier expansion coefficients might be a task of formidable effort. Nevertheless, plotting the spectrum of these two signals as in Figure 3.3 shows that the influence of the oscillations happens at high frequencies and is a localized effect around the oscillation frequency f_o. Except from this effect around the oscillation frequency, the ideal trapezoid signal presents basically the same spectrum as the more complex signal. Furthermore, both spectra present envelope functions that have asymptotes that decrease at a -20 dB per frequency

decade until the frequency given by $\frac{1}{\pi\, t_r}$ and -40 dB per decade for higher frequencies. This shows the importance of the rise time in power signals. Thus, longer rise times lead to lower high frequency spectral energy and lower emissions.

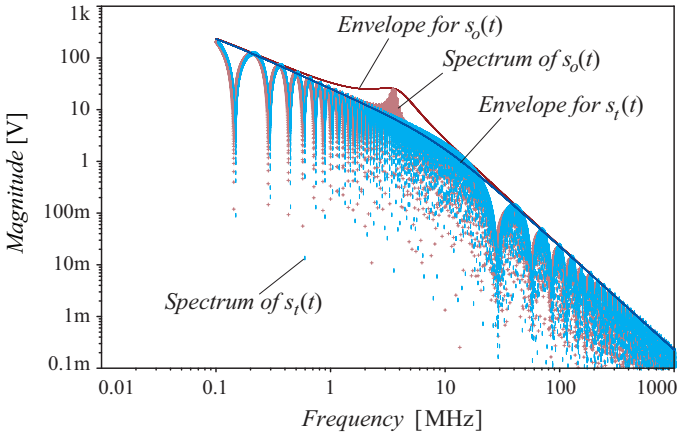


Figure 3.3: Spectra for the signals $s_t(t)$ and $s_o(t)$ with the following parameters: $T_s = 1/(100\,\text{kHz})$; $E = 400$ V; $t_r = 40$ ns; $\delta = 0.7$; $\alpha = 1.25$ MHz; $U_o = 0.3E$; $f_o = 3.6$ MHz.

For the ideal trapezoid, the envelope $\varsigma_t(f)$ is given by,

$$\varsigma_t(f) = \left| \frac{2\delta\, E}{(1+\pi\, f\, \delta\, T_s)(1+\pi\, f\, t_r)} \right|. \tag{3.10}$$

The envelope for the signal with oscillations $\varsigma_o(f)$ can not be directly determined. Thus, an empirical approximation is done, leading to,

$$\varsigma_o(f) = \left| \frac{2\delta\, E}{(1+\pi\, f\, \delta\, T_s))(1+\pi\, f\, t_r)} \frac{\omega_1(f)}{\omega_2(f)} \right|, \tag{3.11}$$

with,

$$\omega_1(f) = -2\pi \left[f_o^2 + \left(f + \frac{\sqrt{2\sqrt{(f_r\,U_o)^4 + (\frac{\alpha\, f_r\, U_o\, E}{\pi})^2} - 2(f_o\,U_o)^2}}{U_o} \right)^2 \right], \tag{3.12}$$

and

$$\omega_2(f) = 2\pi \left[f_o^2 - \left(f + \frac{\sqrt{2\sqrt{(f_r\,U_o)^4 + (\frac{\alpha\, f_r\, U_o\, E}{\pi})^2} - 2(f_o\,U_o)^2}}{U_o} \right)^2 \right]. \tag{3.13}$$

The envelope functions can be employed as worst case approximations for the spectra of the trapezoidal signals.

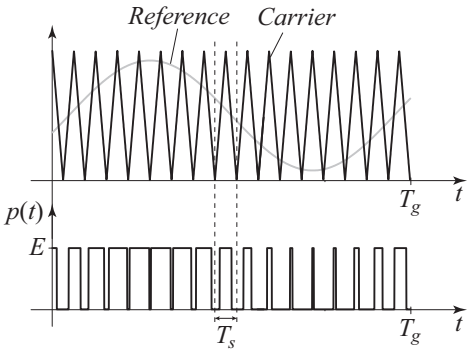


Figure 3.4: Sinusoidal PWM pulse generation patterns.

In three-phase PWM power converters, signals with constant duty cycle are typically not found. More common are pulsed signals with a duty cycle that varies as a function of the phase voltage angles. For instance, in a sinusoidal PWM modulation the pulse generation is according to Figure 3.4. For the shown case, the duty-cycle function is given by,

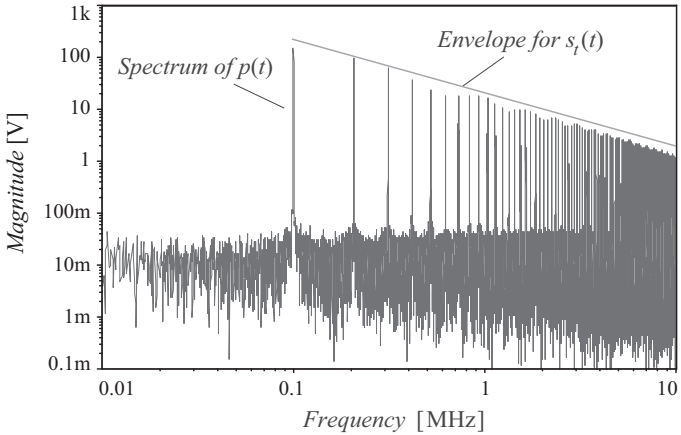


Figure 3.5: Spectrum obtained through FFT for the signal $p(t)$ with the following parameters: $T_s = 1/(100\,\text{kHz})$; $E = 400$ V; $t_r \cong 0$ s; $M = 0.7$. The envelope function $\varsigma_t(f)$ for an ideal trapezoid with constant duty-cycle $\delta = 0.7$ is also shown. The first harmonic at 100 Hz is not shown, presenting a peak value of approximately 140 V.

$$\delta(t) = \frac{1}{2}\left[1 + M\sin(2\pi\frac{1}{T_g}\,t + \phi)\right], \tag{3.14}$$

where M is the modulation index.

The function $p(t)$ can have its frequency spectrum calculated through different techniques. Employing superposition, the Fourier transformation can be applied to each of the pulses, deriving the expansion coefficients for each of them. This approach, although simple in its principle, generates extremely long expressions, since the delay between the pulses must be considered. The total number of terms, even neglecting rise and fall times and oscillations, is proportional to the ratio between the frequency $1/T_g$ and the switching frequency $1/T_s$. If more detail in the signal description is required in order to increase the frequency range where the model is valid, the number of terms in the expressions for the Fourier expansion coefficients grows accordingly. The frequency spectrum computed with Fast Fourier Transform (FFT) algorithm for the function $p(t)$ for $T_s = 1/(100\,\text{kHz})$, $E = 400$ V and $T_g = 1/(100\,\text{Hz})$ is plotted in Fig-

ure 3.5 along with the envelope function $\varsigma_t(f)$ of the ideal trapezoidal signal with a duty-cycle of 0.7, which is equal to the modulation index for $p(t)$. It is observed that the sinusoidal variation of the duty-cycle $\delta(t)$ changes the spectrum, but the peak amplitudes are still in accordance with the envelope for an ideal trapezoid with constant duty-cycle. This example shows that simple waveforms are able to produce envelopes which work as worst case approximations for more complex signals. The envelope functions are very useful for designing EMC filters, since worst case attenuation requirements and equivalent noise sources can employ them instead of the complex expansion coefficients. This approach can also be employed to other functions and is used in some of the following models.

The effect of the variation of the duty-cycle is seen in Figure 3.6, where a view around the frequency $1/T_s$ is depicted. The variation of the duty-cycle occurs with a frequency of 100 Hz. Thus, there are side-bands spaced 100 Hz from each other. It is also shown the amplitude of the harmonic calculated for the ideal trapezoid with same frequency $T_s = 1/(100\,\mathrm{kHz})$, constant duty-cycle $\delta = 0.7$ and amplitude $E = 400$ V. The amplitude of the single harmonic is higher than the peak amplitude of the sinusoidal PWM signal. By calculating the local RMS value of the spectrum of $p(t)$ at 100 kHz with,

$$H_p(100\,\mathrm{kHz}) = \sqrt{\sum_{f=99\,\mathrm{kHz}}^{101\,\mathrm{kHz}} |\mathbb{F}\{p(t)\}|^2}, \tag{3.15}$$

and neglecting the influence of other harmonics, it follows that the local RMS of $p(t)$ is lower than the harmonic value of $s_t(t)$ at 100 kHz. This situation might be very much different for other frequencies, but it explains the proximity of the envelope function to the sinusoidal PWM pattern.

State-of-the-art three-phase PWM converter typically present duty-cycles that are very complex to compute before hand. The calculations of the Fourier expansion coefficients for these are even more complex. The difficulties imposed by the calculations lead, either to the employment of numerical simulation tools, or to the direct measurement of signals or emission levels.

Numerical simulations of PWM converters in the time domain, leading to time domain waveforms which are post-processed with proper Fast Fourier Transformation algorithms are able to provide accurate spectra

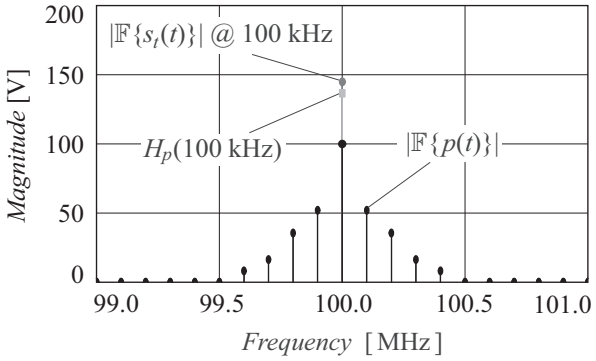


Figure 3.6: Detail around 100 kHz of the spectrum obtained through FFT for the signal $p(t)$ with the following parameters: $T_s = 1/(100\,\text{kHz})$; $E = 400$ V; $t_r \cong 0$ s; $M = 0.7$. Also shown is the harmonic value of the ideal trapezoid with same frequency $T_s = 1/(100\,\text{kHz})$, constant duty-cycle $\delta = 0.7$ and amplitude $E = 400$ V.

of relevant voltages and currents. This technique has the advantage of not requiring the construction of a prototype nor the calculation of extremely complex duty-cycles and Fourier expansion coefficients. Furthermore, the influence of different modulation schemes and operating conditions can be readily studied. Furthermore, this technique gives the condition of designing filters before a prototype is built and, thus, has the potential to shorten design time. Of course, the level of details employed in the simulations is of high importance and, ultimately are responsible for the achievable accuracy.

Another approach to estimate noise sources is the direct measurement of relevant signals in a operational prototype. This strategy has the clear advantage of including all parasitic effects of the layout and semiconductor characteristics, accounting for thermal and environmental influences. On the other hand, it has the drawback of requiring an operational prototype and measurement equipments with high frequency bandwidth and amplitude accuracy.

In the following sections, models for different three-phase PWM converters are derived for CM and/or DM. The presented models vary in complexity, modeling methodology and degree of precision. Some of the models present experimental results attesting the validity of the models

and their useful frequency range.

As an important observation, the aim of the presented models is to design input EMC filters. Thus, very large frequency ranges are not required, since the bulky components of an LC filter have their size determined by the highest attenuation demand, which is typically the lowest frequency to be filtered. This is due to two facts: (*i*) higher frequencies are ideally highly attenuated by the filter components and; (*ii*) the spectrum of typical PWM signals decreases with frequency.

3.3 CM Model of a Three-Phase Buck-Type PWM Rectifier System

The three-phase buck-type PWM rectifier (cf. Figure 3.8) has been presented in the literature [138] and is well suited for utility interfaced systems, where the rectified output voltage is required to be lower than the input voltages and the input currents are required to be of high quality [139,140]. The integration of a boost-type output stage as in [141–143] allows for higher output voltages employing the same input stage. This type of system finds its application in telecommunication energy systems or as front-end for various applications such as plasma power supplies, process technology and others. A photograph of the built prototype depicted in Figure 3.7 and the power circuit of this system is shown in Figure 3.8.

Due to the discontinuous input currents of this system [138], at least a single-stage LC differential mode (DM) input filter is obligatory, however, for full compliance to EMC standards [25, 39] the conducted differential and common mode conducted emissions (CE) propagating to the mains have to be attenuated sufficiently. For this reason, EMC input filters must be employed with this rectifier. Since the DM filter mainly defines the power density, the low-load power factor and the dynamics of the system, it is advantageous to design this filter stage in a first step, by employing either a numerical calculation procedure or using a CM/DM separator as presented in [130] for the buck-rectifier system. For the rectifier used here, the DM filter stage designed in [130] is used. Furthermore, the DM filter components influence the behavior of common mode current propagation paths and are, therefore, required for a CM modeling procedure.

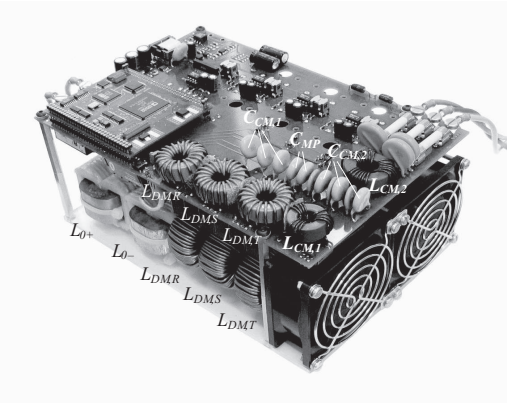


Figure 3.7: 5 kW hardware prototype including the CM filter, the DM filter, auxiliary power supply, and the DSP control board (160 mm x 240 mm x 120 mm).

In order to successfully design a CM filter, an equivalent CM noise source model is required. The objective of this section is to derive a simplified equivalent CM noise propagation model, where the relevant parasitic impedances are identified through impedance measurements. This model shall be valid for the frequency range where the main CM filter components are to be designed.

As a first step, the identification of the CM current propagation paths is required. As the CM currents circulate through parasitic distributed capacitances, which are very complex to model as distributed parameters, simplified lumped elements are used to model the main current paths. This assumption reduces the frequency range of the model validity.

The main propagation paths of the CM current are shown in Figure 3.9, which sets the basis for the identification of the filtering requirements and the analysis of the effect of the placement of the filtering elements. The paths are considered to be closed through capacitances from the components to the heatsink, which for the system at hand, is connected to the power distribution protective earth (PE). This model does not consider the different values for the stray capacitances to PE, which are due to the several possible configurations depending on the switching states of the converter. A more complete model could take more capaci-

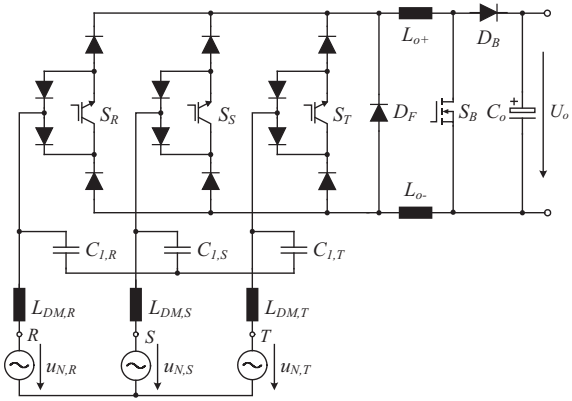


Figure 3.8: Structure of the power circuit of a three-phase three-switch buck PWM rectifier with integrated boost output stage designed for the realization of the input stage of a 5 kW telecommunications power supply module switching at $f_p = 28$ kHz. For clarity, only the DM filter components [130] which are relevant for the CM filter design ($L_{DM,i}$ and $C_{1,i}$) are shown, where $L_{DM,i}$ is the sum of all DM filter inductances of a phase.

tances into account, connecting each node of the power circuits, include the inductances of the interconnections and their mutual magnetic couplings. However, for the task of designing an input filter, the presented model should suffice.

The common mode current i_{CM} flowing through the three phases and the three DM filter inductors to the mains causes an according noise level at the supplying mains and/or LISN network, in case of the CE testing process. Assuming, due to $L_{LISN,i}$, at high frequencies an ideal decoupling of the EUT to the mains, and a perfect coupling with the test receiver, through $C_{LISN,i}$ in a simplified consideration, the equivalent high frequency circuit Figure 3.10 is obtained and only low frequency components circulate to the mains ($i_{CM,1}$).

The CM current path is closed through the parasitic capacitances (C_{MP-GND}, C_{SB-GND}, C_{Co-GND} and C_{Ro-GND}) between the PE terminal, the heatsink and the elements of the power circuit. For the CM current the three phases are lying in parallel, therefore, one third of the DM input filter inductor value becomes effective as depicted in Figure 3.10, and one third of the test receiver sensing input resistance $R_{LISN,i}$ is seen

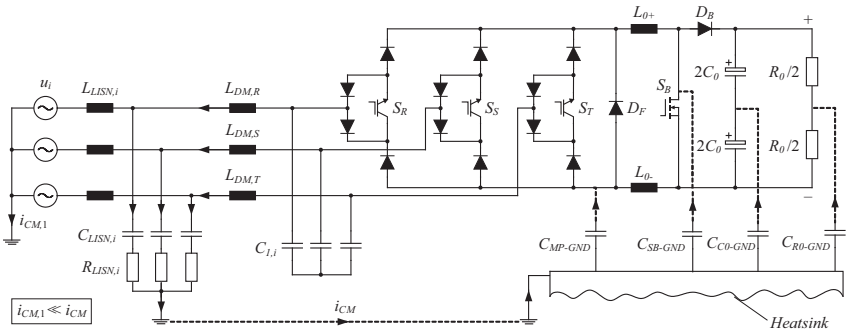


Figure 3.9: Propagation model of the common mode currents in the rectifier system used for deriving the CM noise model.

by the common mode current. The capacitance C_{MP-GND} is the lumped capacitance model for the high frequency connection between the power modules (S_R, S_S, S_T) and the heatsink. It is drawn in Figure 3.9 in the negative rail since a higher capacitance is observed at the anodes of the diodes. Capacitance C_{SB-GND} is the lumped capacitance model for the high frequency connection between the boost switches (S_B, D_B) and the heatsink. For these switches, a higher capacitance is observed at the drain of the MOSFET S_B.

Still regarding CM paths, on the DC side of the rectifier circuit, the two DC inductances $L_{o+} = L_{o-} = L_o/2$ are lying in parallel. If the capacitances from the output capacitors to ground, which are distributed parasitic capacitances, are summed into a single total capacitance C_{Co-GND}, one path with output capacitance C_0 results and this path is here modeled as a four times the capacitance of the output foil capacitors $C_{0,foil} = 220$ nF placed in parallel with the electrolytic ones. The capacitance C_{Co-GND} models the influence of the parasitic capacitive connection from the printed circuit board output traces to the heatsink. This capacitance is placed in the center point of the output foil capacitors because of the large plane in the PCB placed with this potential. The distributed capacitances from the load resistor to ground are modeled through C_{Ro-GND} from the load middle-point to ground which results in a path with $R_0/4$.

The main parasitic components of the DM filter inductors and output inductors are modeled with the parasitic capacitances C_{Ldm} and C_{Lo}.

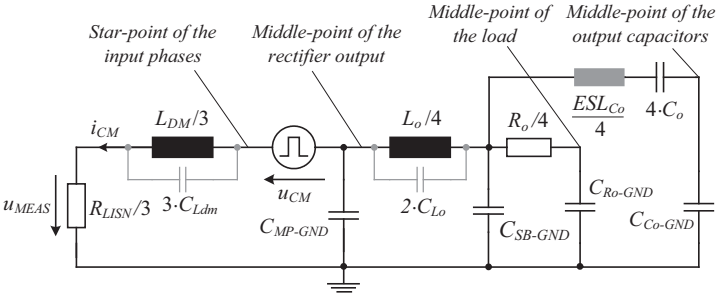


Figure 3.10: CM noise propagation model for the three-phase buck-type PWM rectifier with integrated boost output stage. Components values: $L_{DM} = 270$ μH ; $L_o = 2$ mH ; $C_0 = 750$ μF; $C_{MP-GND} = 141$ pF ; $C_{Ro-GND} = 57$ pF ; $C_{Co-GND} = 283$ pF.

The equivalent series inductance of the output foil capacitors is modeled with ESL_{Co}.

The rectifier itself is modeled as a common mode voltage source u_{CM} that drives the potential between the star-point of the rectifier input (lying at the star-point of the DM input filter capacitors, which are not relevant for the CM noise model) and the middle-point of the rectifier output.

Estimation of the Model Parameters

For the measurement and estimation of the relevant capacitances included in the CM propagation paths (C_{MP-GND}, C_{SB-GND}, C_{Co-GND} and C_{Ro-GND}), four impedance measurements are performed with an impedance analyzer Agilent 4294A, well suited for the relevant frequency range.

For evaluating C_{Ro-GND} a simple impedance measurement is carried out with disconnected power cables leading to a high frequency equivalent circuit presenting a resistor, an inductor and a capacitor is series, from which only the capacitance value is used in this design procedure and has a value of $C_{Ro-GND} = 57$ pF. The same procedure in applied to measure the impedance of the output capacitors and of the output inductors. The results for these components are displayed in Figure 3.12.

The DM filter inductors $L_{DM,i}$ are modeled as a parallel connection

of $R = 3\ \mathrm{k\Omega}$, $L = 270\,\mu\mathrm{H}$ and $C = 52\ \mathrm{pF}$.

The mathematical estimation of the capacitances C_{MP-GND}, C_{SB-GND} and C_{Co-GND} is done through two impedance measurements. For these measurements, it is considered that capacitances C_{SB-GND} and C_{Co-GND} are in parallel. This assumption is valid, since the high frequency impedance of the output capacitors is relatively small. The rectifier is disconnected from the mains and the load and the impedance Z_{Co-GND} are measured according to the setup shown in Figure 3.11, where it is seen that some diodes are shorted in order to measure a common impedance from the input side of the converter to the heatsink.

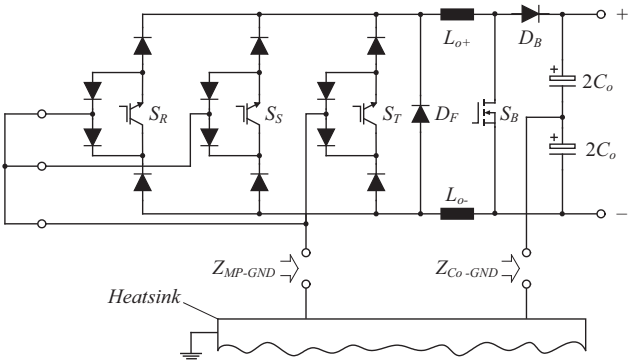


Figure 3.11: Setup for the impedance measurements performed in order to evaluate the CM noise paths within the rectifier prototype.

The results from these measurements are presented in Figure 3.12 and Figure 3.13. Simple equivalent C-L-R circuits are taken as approximation within the frequency range close to 600 kHz due to the high order observed in the impedance measurements.

By considering the two equivalent circuits (cf. Figure 3.11) resulting from each impedance measurement, two simplified equations for the two unknown parameters C_{MP-GND} and C_{Co-GND} can be derived resulting in,

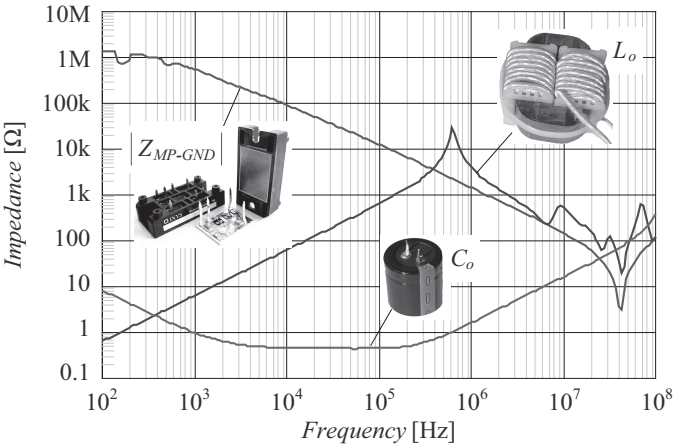


Figure 3.12: Measured impedances: output inductors L_o, output capacitors C_0 and impedance Z_{MP-GND} as defined in Figure 3.11.

$$Z_{MP-GND} \cong \frac{\frac{1}{s\,C_{MP-GND}} \cdot \left(s\frac{L_o}{4} + \frac{1}{s\,C_{Co-GND}}\right)}{\frac{1}{s\,C_{MP-GND}} + \left(s\frac{L_o}{4} + \frac{1}{s\,C_{Co-GND}}\right)} \tag{3.16}$$

$$Z_{Co-GND} \cong \frac{\frac{1}{s\,C_{Co-GND}} \cdot \left(s\frac{L_o}{4} + \frac{1}{s\,C_{MP-GND}}\right)}{\frac{1}{s\,C_{Co-GND}} + \left(s\frac{L_o}{4} + \frac{1}{s\,C_{MP-GND}}\right)}. \tag{3.17}$$

The solution for the system of equations above is not analytical and must be found numerically. Using the measurement data from Figure 3.12 and Figure 3.13 leads to $C_{Co-GND} \cong 283$ pF and $C_{MP-GND} \cong 141$ pF.

All the parameters of the equivalent circuit of Figure 3.10 are known. The remaining unknown is the CM noise source voltage spectrum for the voltage source u_{CM}.

In order to obtain the spectrum for the voltage source u_{CM}, a simplified time domain simulation of the system is performed for the circuit of Figure 3.14. The objective of the simulation is to measure voltages $u_{o+,PE}$ and $u_{o-,PE}$, so that the CM voltage can be computed with,

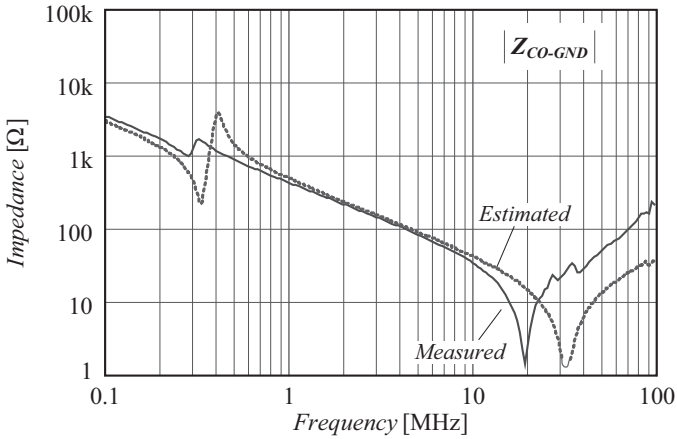


Figure 3.13: Measured and estimated impedance Z_{Co-GND} as defined in Figure 3.11.

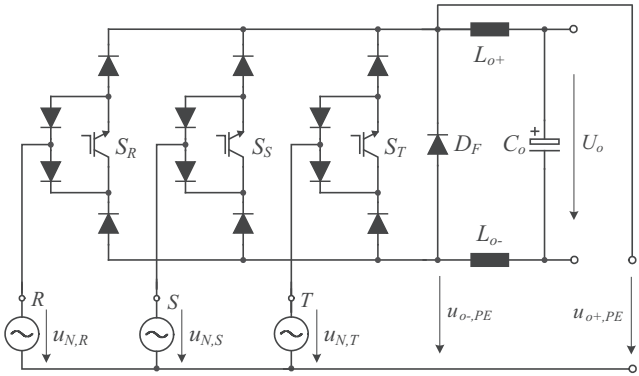


Figure 3.14: Simulated topology that is employed for the calculation of the CM voltage.

$$u_{CM} = \frac{u_{o+,PE} + u_{o-,PE}}{2}. \tag{3.18}$$

The simulated time behavior of the CM voltage is depicted in Figure 3.15. This voltage is formed by portions of the line-to-line voltages

and has a maximum high frequency peak-to-peak amplitude of approximately $U_{CM,HF,pp} = (3/\sqrt{8})\,U_{N,rms}$. With this, the CM voltage of the three-phase Buck PWM rectifier is relatively small when compared to the CM voltage in boost-type rectifiers. The counterpart of that is that the DM emissions are larger due to the discontinuous input currents.

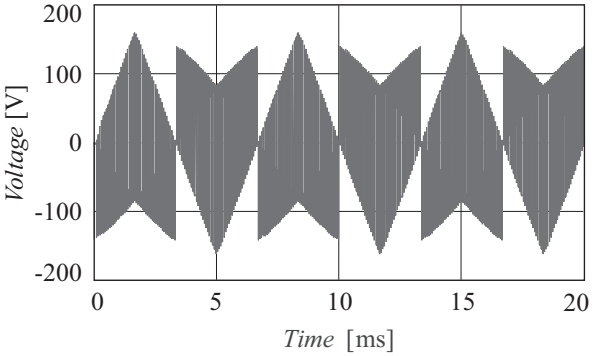


Figure 3.15: Time behavior of the CM voltage u_{CM} computed with eq. (3.18).

Computing the Fast Fourier Transform for the CM voltage leads to the spectrum presented in Figure 3.16. Experimental tests in the prototype show that, in average, the switching times are around $t_r = 200$ ns. The peak RMS voltage is approximately 45 V at the switching frequency (28 kHz) and the spectrum decays by -20 dB/decade up to $1/(\pi\, t_r) \cong 1.6$ MHz, from where -40 dB/decade follows.

In order to use the characteristics of this spectrum in a simplified way and use the experimental data regarding switching times, an envelope function is used, defined with

$$\varsigma_{U_{CM}}(f) = \left| \frac{2\delta\, E}{(1+\pi\, f\, \delta\, T_s)(1+\pi\, f\, t_r)} \right|, \tag{3.19}$$

where, $E = U_{CM,peak}/2$ V is the peak RMS CM voltage, $T_s = 1/28$ kHz is the switching period, $t_r = 200$ ns is the rise time estimated from switching loss measurements and $\delta = 0.23$ is the duty ratio, which is found from the comparison with the computed spectrum, which is also displayed in Figure 3.16.

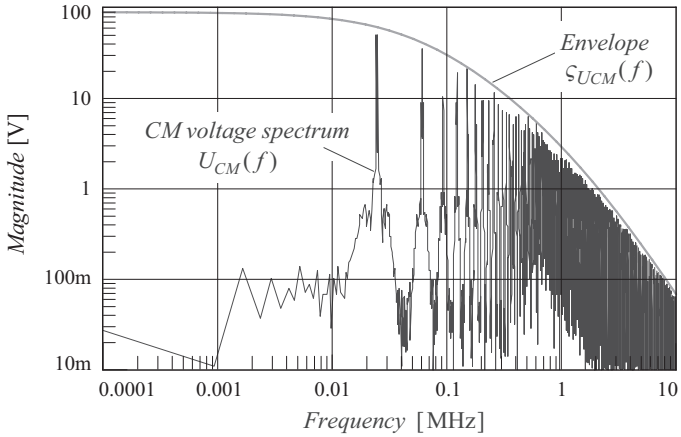


Figure 3.16: Spectrum of the common mode voltage obtained through the simplified circuit simulation. Also shown is the asymptotic curve for the employed envelope function $\varsigma_{U_{CM}}(f)$.

Model Verification

In order to verify the proposed CM propagation model, conducted emission measurements employing a HF current probe Pearson 410, presenting a nominal bandwidth of 20 MHz, measuring the sum of the three input currents. The measurement setup is shown in Figure 3.17.

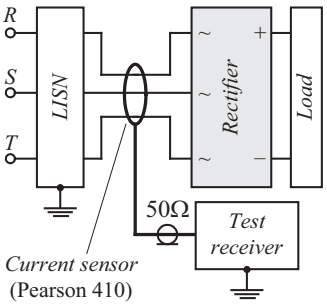


Figure 3.17: CM measurement setup: the sum of the input currents is measured with a current probe Pearson 410 in order to obtain only the CM levels.

The measured conducted emission levels are compared to estimated levels in Figure 3.18. As it can be seen, the critical frequency range for the design of the CM filter is close to 600 kHz and it is for this frequency that the input CM filter must be designed.

According to Figure 3.18, the estimated conducted emissions envelope provides a highly correlated response when compared to the measured CE levels up to approximately 4 MHz, thus, validating the modeling procedure.

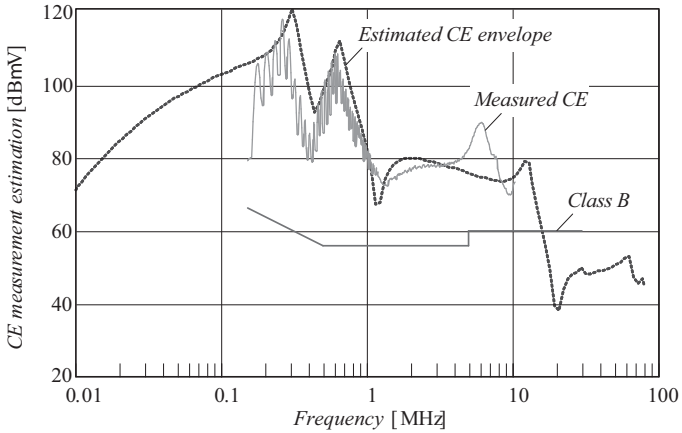


Figure 3.18: Common mode emission levels at a three-lines LISN. Shown are the measured levels and the predicted ones for a QP measurement as specified in CISPR 22.

3.4 Models for a Three-Phase Three-Level Boost PWM Rectifier

The objective of the modeling procedure presented in this section is to obtain a simplified model that allows for the design of input EMC filters for a Three-Phase Three-Level Boost PWM Rectifier as depicted in Figure 3.19 [78,131]. This rectifier has an output power of 10 kW, power density of 8 kW/dm^3, switching frequency $f_s = 400$ kHz, output voltage $U_o = 760$ V, input voltage $U_{N1} = 230$ V and is forced air-cooled. The

EMC filter for this system must be designed to fulfill EMC requirements, where an attenuation specification, based on the estimated CE levels of the rectifier, is calculated. Furthermore, the filters shall be designed taking into account the limits for CE specified for Class B information technology (IT) equipments as in CISPR 22.

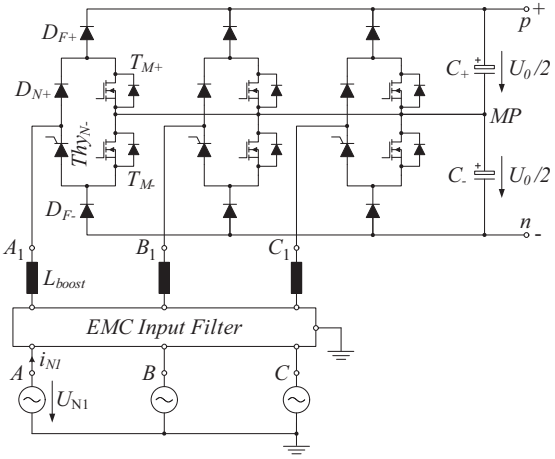


Figure 3.19: Circuit schematic of a Three-phase, Six-switch, Three-level Rectifier topology used to implement a 10 kW PWM rectifier.

The procedure starts by defining equivalent circuits used to evaluate CM and DM noise sources and to design appropriate filtering circuits. As the prime objective of the filtering circuits is to reduce emissions at frequencies typically lower than 1 MHz, the definition of very accurate models, including higher order parasitics as magnetic and capacitive couplings among components and PCB impedances, is not mandatory as long as safe margins are respected. The uncertainties in obtaining very precise simulation models, which include most of the parasitic effects observed in a prototype, also supports this practice. These parasitic impedances are critical for the filter layout and components construction, but are not essential for the input filter design. For these reasons, the circuits presented in Figure 3.20 are employed here, where the voltages u_{CM}, u_{DM}, the inductors L_{boost} and the capacitance C_g model the power converter CM and DM noise source circuits.

Capacitance C_g is a lumped representation of all stray capacitances

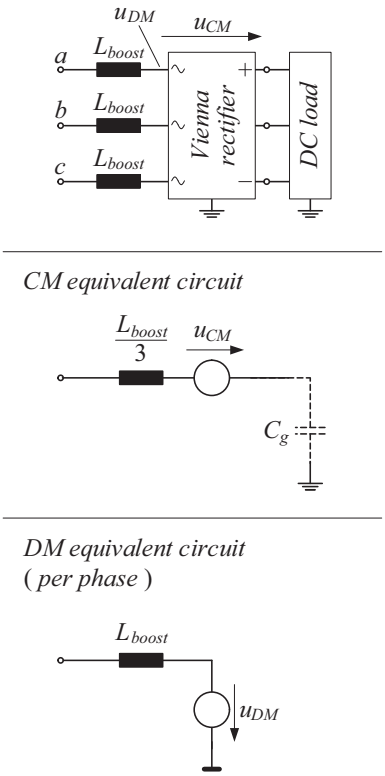


Figure 3.20: Simplified equivalent circuits for CM and DM emissions for the Three-phase, Six-switch, Three-level Rectifier.

from the power circuit and load to the protective earth (PE). Not considering load and assuming that the heatsink is bonded to PE, C_g represents mainly the capacitances from the semiconductors to the heatsink. Typically, the impedance of C_g is distributed and presents resistive and inductive portions. Thus, one capacitor at the output of the rectifier represents worst-case (lowest impedance) except from strong resonances, which are possible at frequencies other than the ones aimed with this modeling procedure. The maximum value calculated for the capacitances from the power semiconductors is around 300 pF, typical capacitances from test loads are in the range 200 pF to 2 nF.

Inductors L_{boost} model the input inductors of the rectifier, which influence CM and DM current paths. Impedance measurements of the built inductors show an inductance of approximately 30 μH and a self-resonance frequency around 8.5 MHz. The boost inductors are built with ferrite and their specification can be seen in [131].

The design of the filters is performed in the frequency domain, since the required attenuation is defined in terms of frequency and suitable impedance models for the filtering components are at hand for this domain. Therefore, the estimation of frequency spectra for DM and CM voltages and/or currents is required. A simple simulation with ideal devices presenting rise and fall times close to zero and without the inclusion of parasitic elements is able to provide spectra which are conservative, except at the frequencies close to the characteristic frequencies related to the rise and fall times due to over-voltages and oscillations. Another point, which can be neglected in this simulation, is the inclusion of the LISN circuits, once the voltage spectra do not sensibly change with the inclusion of the LISN, inner mains impedances and filter components. At last, the circuit is considered to be perfectly balanced. The simulation circuit is as in Figure 3.19, except that the EMC filter is removed and the switches are replaced by ideal ones. For the power converter at hand, the boost inductors are included in the simulation as ideal inductors, but are also seen as part of the input filters. The spectrum of the input currents changes with the inclusion of the other filter components and, for that reason, the input currents spectra are not used for the model.

For the CM design the relevant spectrum is of the voltage between the DC-link center point MP and the terminals A_1, B_1 and C_1 with the CM voltage u_{CM} given by,

$$u_{CM} = u_{MP} - \frac{u_{A1} + u_{B1} + u_{C1}}{3}. \tag{3.20}$$

The computed CM voltage is shown in Figure 3.21. It is observed that the CM voltage is formed by pulses with amplitude equal to one third of half output voltage $U_o/6$ and that at low frequencies there is a noticeable third harmonic. The frequency of the pulses is equal to the switching frequency.

A detail of the common-mode voltage shown in Figure 3.21 is seen at Figure 3.22 for the time interval between 6.5 μs and 7 μs.

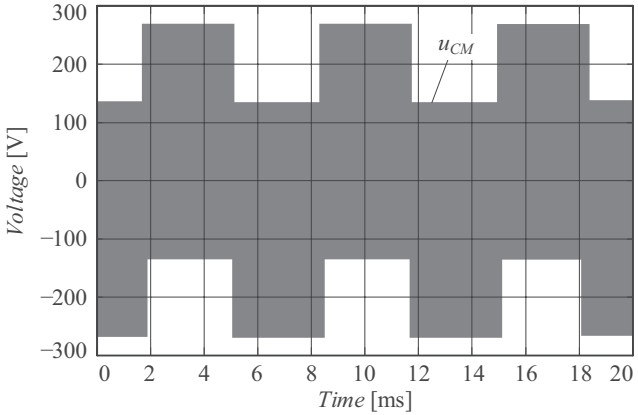


Figure 3.21: Time behavior of the common mode voltage u_{CM}. A third harmonic is clearly seen and it is produced by the injection of a third harmonic in the modulation.

Considering symmetrical spectra for the three phases, the DM filter the spectrum of interest is one of the DM voltages at terminals A_1, B_1 and C_1. The DM voltage u_{DM} is taken for phase A and is computed as,

$$u_{DM} = \frac{2}{3}u_{A1} - \frac{1}{3}u_{B1} - \frac{1}{3}u_{C1}. \tag{3.21}$$

Applying eq. (3.21) to the time domain simulation results leads to the waveform displayed in Figure 3.23. It is seen that the low frequency behavior is dominated by the harmonic at the mains frequency, which is responsible is responsible for the sinusoidal shaping of the input currents, thus, achieving a high power factor. The high frequency behavior shows pulsed voltages at the switching frequency with steps of $U_o/6$ and $U_o/3$.

The CM and DM voltage spectra are post-processed in order to obtain the signal levels that would be measured in an EMC test receiver employing QP detection. This is done with the procedure presented in section 2.5.2 and leads to the curves shown in Figure 3.24. The simulation results presented in Figure 3.24 are for nominal conditions, which, as required by the CE test specifications [106], is the worst-case emission condition for this system. This is because the fastest rise and fall times are observed for voltages and currents. These curves can then be compared

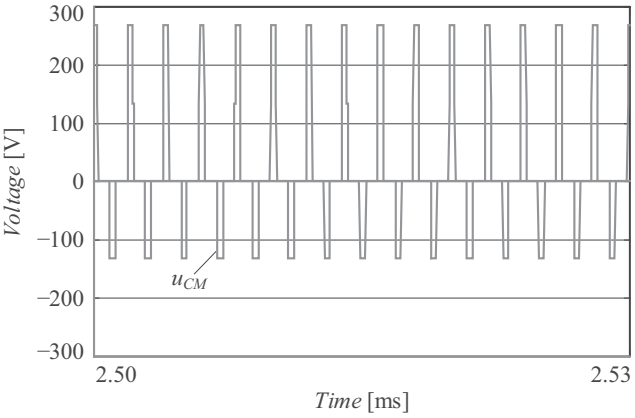


Figure 3.22: Detail of the time behavior of the common mode voltage u_{CM} for the interval 6.5 μs – 7 μs.

to the emission limits at the frequency of interest f_{int} which is 150 kHz for switching frequencies lower than 150 kHz or the switching frequency for higher frequencies. This gives the required attenuation, Att_{req}, at the frequency of interest,

$$Att_{req,CM}(f_{int}) = 20 \cdot \log\left[\frac{U_{CM}(f_{int})}{1\,\mu\text{V}}\right] - Limit_{\text{Class B}}(f_{int}) \qquad (3.22)$$

$$Att_{req,DM}(f_{int}) = 20 \cdot \log\left[\frac{U_{DM}(f_{int})}{1\,\mu\text{V}}\right] - Limit_{\text{Class B}}(f_{int}). \qquad (3.23)$$

The design must also take into account the specified CE measurement, which in this case is done with two types of detector, the quasi-peak (QP) and average (AVG), presenting both non-linear behavior. For this work, only the QP detector is considered and its behavior is modeled as proposed in section 2.5.2, by linearization. Accordingly, the voltage spectra shown in Figure 3.24 account for a maximum value for the QP measurement, which leads to slightly over dimensioned filters. However, components tolerances and other uncertainties are present in the filter and the achieved margins can be seen as an advantage.

With Figure 3.24, it is observed that, at the switching frequency $f_s =$

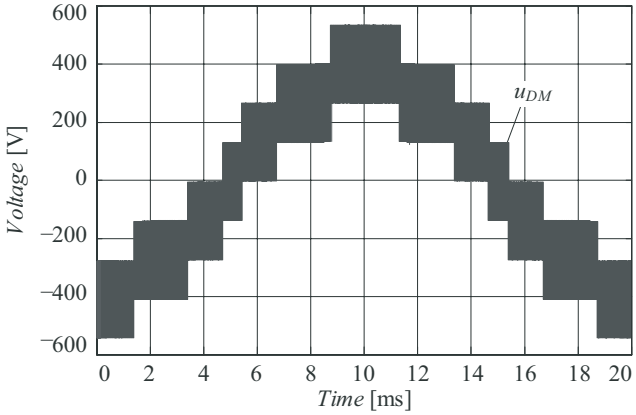


Figure 3.23: Time behavior of the differential mode voltage u_{DM}.

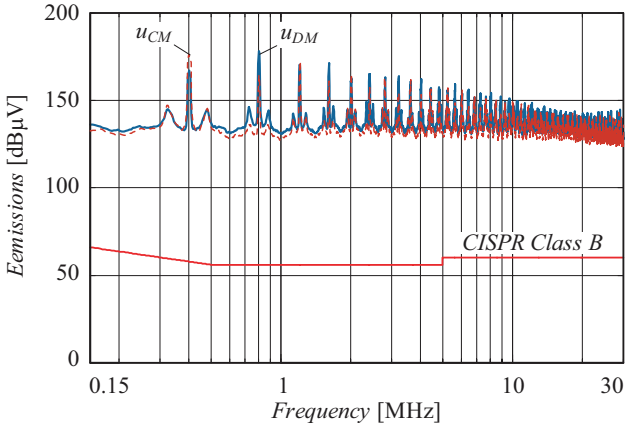


Figure 3.24: Conducted emissions predicted spectra for both voltages for the worst case QP detection (linear sum of the harmonic inside the resolution bandwidth as presented in section 2.5.2).

400 kHz, both spectra present the worst condition for the filter design task and attenuations of:

$$Att_{req,CM}(f_{int}) = -115 \text{ dB } @ \ f_{int} = f_s = 400 \text{ kHz} \tag{3.24}$$
$$Att_{req,DM}(f_{int}) = -109 \text{ dB } @ \ f_{int} = f_s = 400 \text{ kHz}, \tag{3.25}$$

are required in order to fulfill CISPR 22 Class B requirements with a 6 dB margin.

With the presented models, the design of EMC filters for the mentioned converter has been done and experimental results validate the modeling procedure. The filter design and experimental results are presented in section 6.7.

3.5 Models for Three-Phase Sparse Matrix Converters

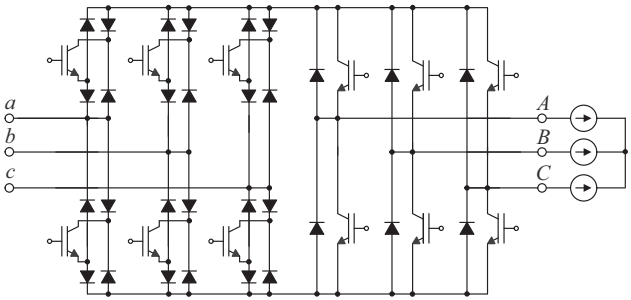
In this section, different modeling procedures for Three-phase Sparse Matrix Converters are presented. The first models are obtained with simplified equivalent circuits, whereas the more complete one is based on the modeling of all circuits that influence the conducted emissions measurement range.

3.5.1 Simplified Models

The objective of the modeling procedure presented in this section is to obtain simplified models for Three-Phase Sparse Matrix Converters as depicted in Figure 3.25 [88]. The EMC filters for this type of system must typically be designed to fulfill EMC requirements, where an attenuation specification, based on the estimated CE levels of the converter, is calculated.

A series of simplifications are done in order to keep a reasonable modeling effort, namely: (*i*) the circuits are considered symmetric regarding the three-phases, so that single-phase equivalents are used; (*ii*) the parasitics, inter-component couplings and the effects of the tolerances of the designed filter components are neglected for attenuation calculation; (*iii*) parasitics inside the power converters are neglected, except for the capacitances to ground (PE), which are responsible for CM paths and are

Very Sparse Matrix Converter



Ultra Sparse Matrix Converter

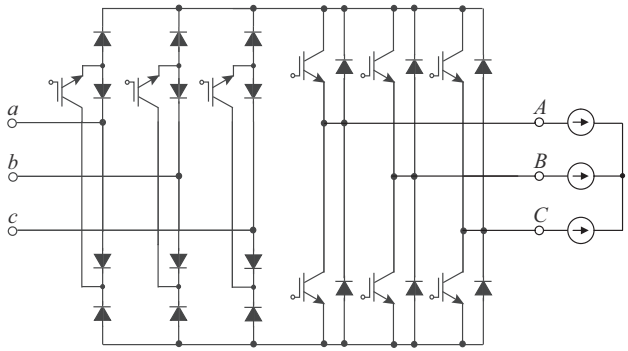


Figure 3.25: Circuit schematics of Three-phase Sparse Matrix Converter topologies.

lumped into one capacitance C_g, which represents the sum of all capacitances to PE, including the ones from a load; (*iv*) the effects of internal power supplies, control and gate drive circuits are neglected, and; (*v*) the output currents are considered free from ripple, so that current sources are considered.

Defining equivalent circuits to evaluate CM and DM noise sources as presented in Figure 3.26, lead to simplified noise source models for the converters. There, the CM voltage source u_{CM}, DM current source i_{DM}

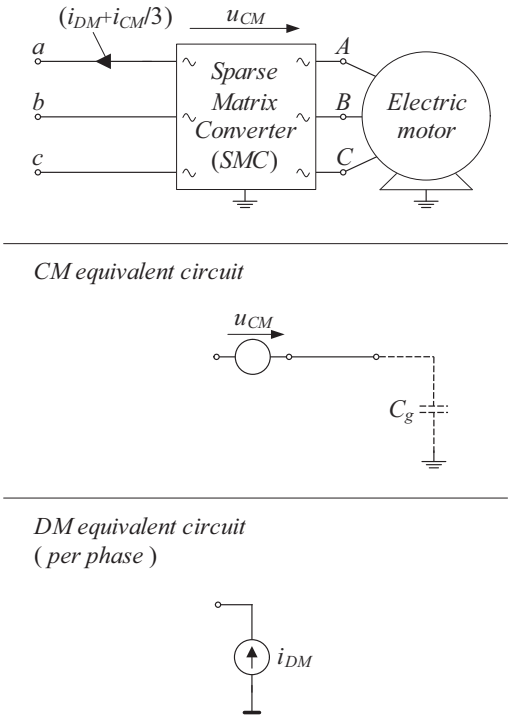


Figure 3.26: Simplified equivalent circuits for CM and DM emissions for Sparse Matrix Converters.

and the capacitance C_g model the power converter CM and DM noise source circuits. As the Sparse Matrix Converters ideally do not include passive elements in their topologies, the simplified equivalent circuits are straightforward and uncomplicated.

In order to define the CM and DM sources, the estimation of the frequency spectrum for DM voltages and currents and CM voltages is used here, where the common mode voltage is calculated from the combination of the three input and three output terminals as shown in Figure 3.26, so that,

$$u_{CM} = \frac{u_a + u_b + u_c}{3} - \frac{u_A + u_B + u_C}{3}, \tag{3.26}$$

and the differential mode currents are computed directly from the input currents as shown in Figure 3.26 as long as no common mode paths exist in the simulation circuit, so that $i_{CM} = 0$. For simplicity, the current in phase A is used so that,

$$i_{DM} = i_A. \tag{3.27}$$

A simulation of a Sparse Matrix Converter, operating with output power $S_2 = 5$ kVA, input RMS phase voltage $U_{N1} = 230$ V, mains frequency $f_1 = 50$ Hz, output frequency $f_2 = 150$ Hz and modulation index $M = 0.7$, has been performed in order to illustrate the waveforms of the CM and DM voltages at these converters. The switching frequency of the converter has been set to 10 kHz at the output stage, thus, 5 kHz at the input stage [88].

The time behavior of the CM voltage u_{CM} is presented in Figure 3.27, where it is seen that the CM voltage is formed with combinations of the input line voltages, presenting influences of both, input and output frequencies. The pulses are at the output stage switching frequency.

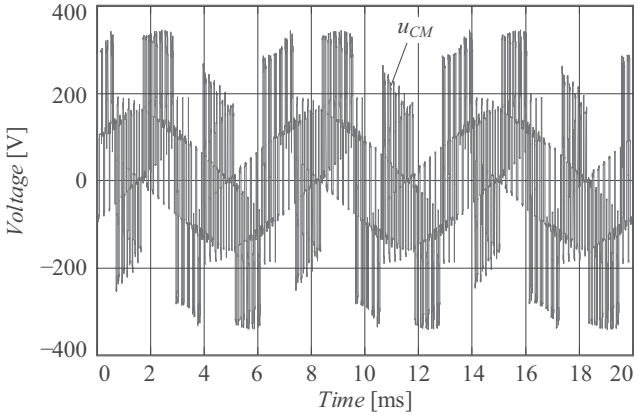


Figure 3.27: Time behavior of the common mode voltage u_{CM}.

The differential mode input current for the same simulation is depicted in Figure 3.28. It is a typical three-level PWM waveform, where the amplitude of the current pulses does not present much variation. This is because the input currents are constructed out of current blocks of the output currents that are close the their peak values. The low frequency

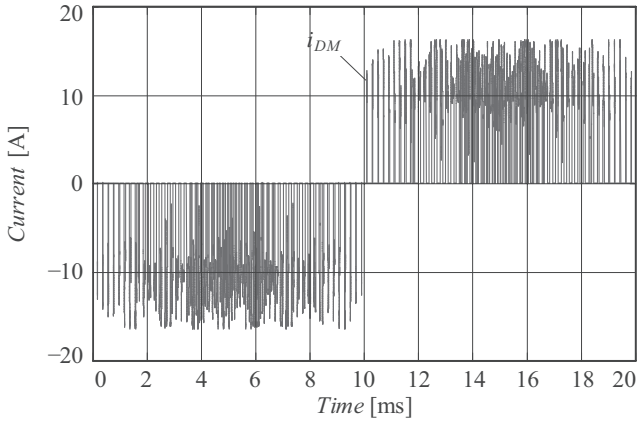


Figure 3.28: Time behavior of the differential mode current i_{DM}.

behavior shows a nearly ideal sinusoidal behavior, thus, power factor correction is obtained. The high frequency contents are due to the pulse width modulated current pulses at the output stage switching frequency.

A series of similar simulations for different modulation indexes and switching frequency has been done so that the accurate calculation of the harmonic contents of the switched voltages of the Sparse Matrix Converters can be replaced by simplified envelope functions, that depend on modulation index, switching frequency, voltage and current levels.

The empirically derived expressions for the envelope functions are given by,

$$\varsigma_{i_{DM}}(f) = \begin{cases} \frac{1}{2\sqrt{2}} \left| \frac{I_{2,peak}\, M}{1+j\,\pi\, M\, \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } f \leq f_s \\ \frac{1}{2} \left| \frac{I_{2,peak}\, M}{1+j\,\pi\, M\, \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } f_s < f \leq 6f_s \\ \frac{1}{2\sqrt{2}} \left| \frac{I_{2,peak}\, M}{1+j\,\pi\, M\, \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } 6f_s < f \end{cases}, \tag{3.28}$$

for the DM equivalent current source and by,

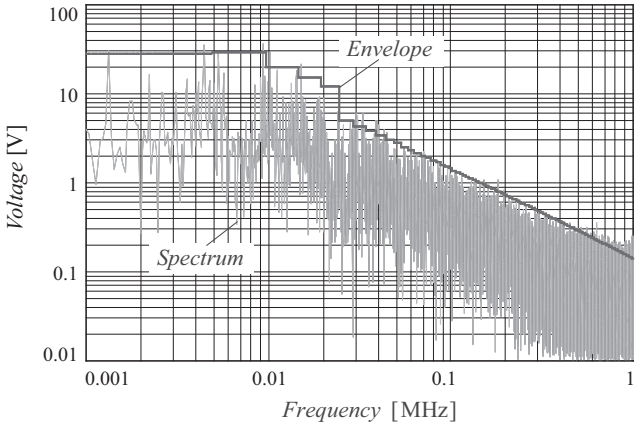


Figure 3.29: Frequency spectrum of the common mode voltage u_{CM}.

$$\varsigma_{u_{CM}}(f) = \begin{cases} \frac{1}{\sqrt{6}} \left| \frac{U_{N1}\, M}{1 + j\,\pi\, M\, \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } f \leq f_s \\ \frac{2}{\sqrt{6}} \left| \frac{U_{N1}\, M}{1 + j\,\pi\, M\, \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } f_s < f \leq 6 f_s \\ \frac{1}{\sqrt{6}} \left| \frac{U_{N1}\, M}{1 + j\,\pi\, M\, \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } 6 f_s < f \end{cases}, \tag{3.29}$$

for the CM equivalent voltage source.

In order to compare the results obtained with simulation results and with the proposed envelope functions, Figure 3.29 and Figure 3.30 show the computed spectra and envelope functions for the same simulation conditions as previously stated, to the CM voltage and DM current respectively.

The derived envelope functions have been compared with computed spectra based on other simulation results and for these different conditions the error has been smaller than 10 dB for the frequencies bellow $1/(\pi\, t_r)$. This ensures that the envelope functions can be employed in simple filter design procedures or where the conducted emission levels shall be modeled

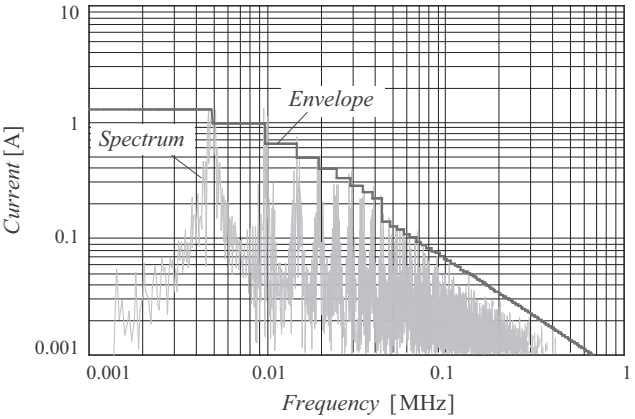


Figure 3.30: Frequency spectrum of the differential mode current i_{DM}.

as a function of the switching frequency or other converter parameters. If more precise information is required, the simulation of the power topology leads to reliable results for a limited frequency range.

3.5.2 Extending the Frequency Range of the Model

In order to illustrate the possibility of extending the useful frequency range of noise source models for the matrix converters, the procedure described below is one of the alternatives. This work has been published in [144] and represents the initial steps in order to accurately model three-phase power converters. The system of interest is a reverse blocking IGBT (RB-IGBT) based Indirect Matrix Converter (RB-IGBT IMC) as shown in Figure 3.31.

The modeling method is based on the detailed models for all EMI relevant parameters in the system. These models shall be obtained from impedance extraction computational techniques. The parasitic impedances are also included and are derived through parametric extraction. The importance of identifying and quantifying the parasitic impedances within a power converter system for EMC characterization has been highlighted in the literature [145–147]. The extraction of parasitic impedances for EMC modeling has been performed mainly for high-

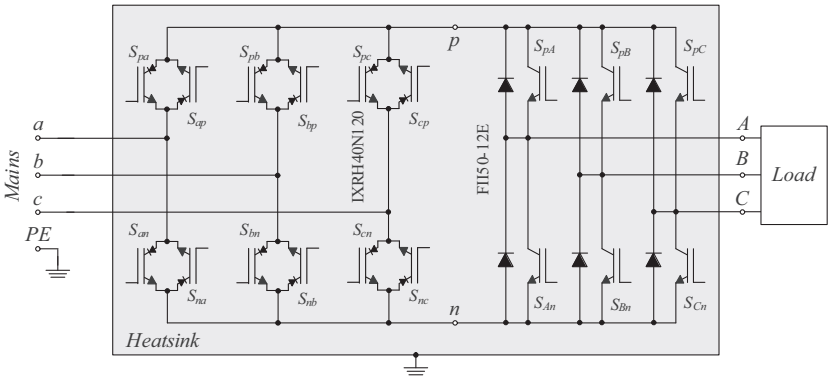


Figure 3.31: Circuit schematic of a Three-phase RB-IGBT based Indirect Matrix Converter.

speed digital electronic circuits [148,149], where operating frequencies are very high ($>$ 1 GHz). Therefore, knowledge of the parasitic impedances is mandatory for the system to function correctly. Therefore, techniques for extracting impedances from circuit layouts already exist [149]. But these techniques are either based on approximate and inaccurate expressions or require a lot of computational power. For parasitics extraction, the Partial Element Equivalent Circuit (PEEC) method emerged as a computationally effective and accurate technique. This technique can be employed in Power Electronic systems, as in [147], in order to perform the cited tasks and to use them to optimize PCB layouts before their manufacturing. Therefore, the main objective of the work is to evaluate and define mathematical tools to predict the conducted emission (CE) levels of a complex power converter system prior to the construction of a prototype.

The analyzed system employs an Indirect Matrix Converter topology with Reverse Blocking (RB)-IGBTs at the input stage and conventional IGBTs at the output, where two switches and fast recovery freewheeling diodes are included into a single power module for each output phase, respectively [89]. A block diagram of the whole converter structure is depicted in Figure 3.32, which is also used in the experimental verification of the performed simulation. This work aims at the prediction of CE measurements from a typical measurement setup, where a quasi-peak (QP) detector is employed as specified in CISPR 16. The prediction is separated

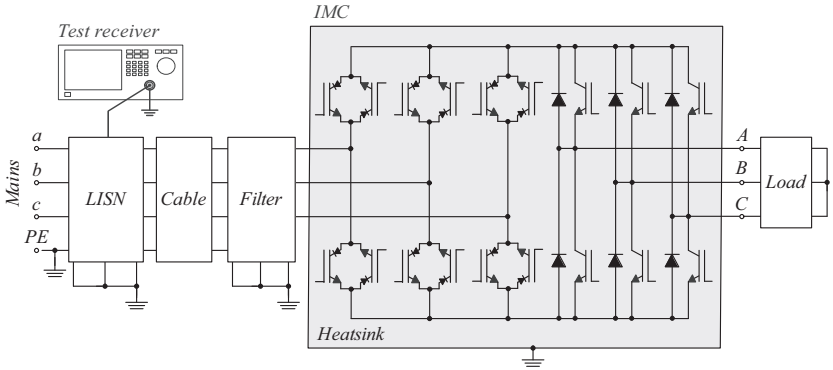


Figure 3.32: Test setup for the IMC prototype and derived model. The DM and CM emission levels are measured by a test receiver in the 50 Ω terminal resistances to ground inside the Line Impedance Stabilization Network (LISN) [104]. The source for EMI noise is the IMC.

into common mode (CM) and differential (DM) mode noise [150], since this brings important information for the design of EMC filters and, in a second step, possibility of improvement of the power circuit layout and the environment of the power components. Finally, the predicted results are compared with experimental results.

In order to remove all possible external noise sources, the load machine is replaced by a three-phase passive RL load, and the built-in auxiliary power supply was replaced by an external voltage source. Thus, the only non-modeled HF noise sources are the digital signal processing board and the internal gate drive power supplies. The latter is a self oscillating half bridge operating at a switching frequency of 80 kHz. A voltage measurement at the gate drive isolating transformers revealed a high frequency oscillation with strong components of 3.9 MHz and 7 MHz, which may influence the matching between CE simulation and measurement in this frequency range.

In order to reduce the modeling effort at these initial modeling steps, the models for the impedances of the supply cable, filter board and connection and load elements have been based in actual impedance measurements. The capacitances from the semiconductors to the grounded heatsink have been estimated also from impedance measurements. In a

later stage, the modeling of all these impedances shall be made with the aid of computational methods, so that "virtual prototyping" is achieved in its full scale.

In this study a first order behavioral IGBT model as proposed in [151] is used. The model consists of a few discrete devices and can be implemented easily in a circuit simulator. The IGBT switching edge is triggered due to changes in a time dependent conductivity. The values of the model parameters are determined by experimental measurements and subsequent fitting of the simulated behavior to the curves obtained by experiments. This IGBT model is sufficient to allow a reasonable simulation time and provides good results for the CE noise prediction. In the simulation, the IGBT model acts as a noise source and the observed voltage waveforms result from the interaction with the parasitic impedances.

The freewheeling diodes of the output stages are modeled using a detailed diode model including the diode reverse recovery effect. The model's reverse recovery time was set according to datasheet information of the employed diode. In comparison to a complex IGBT SPICE model, the diode model is simpler and appreciably does not increase the simulation time.

The layout parasitics are extracted using the Partial Equivalent Element Circuit (PEEC) method [152, 153]. In the PEEC method, a conductor is discretized into many partial elements as shown in Figure 3.33. The PEEC model creates matrices of partial inductances Lp_{ij}, partial coefficients of potential P_{ij} and node resistances R_m. From this, an equation system is generated which gives a full wave solution of the electrical field integral equation, including high frequency effects like skin and proximity effects. In general, a time-retarded simulation which considers the finite speed of electromagnetic waves is possible with the PEEC simulation method, too. To increase the calculation speed, a quasi-static model was chosen which implies an infinite fast velocity of the waves. However this is a valid approximation for the analyzed frequencies, which are lower than 30 MHz and circuit geometry layout smaller than 50 cm [154].

A Java program was developed for the PCB parasitics extraction, which is able to import PCB geometries from a Gerber file format. In the graphical user interface, one is able to set probes to arbitrary points of interest at which impedances and mutual couplings will be calculated. Furthermore, the program connects adjacent conductors and builds a mesh for the PEEC solver. The generated mesh consists of many rectangular

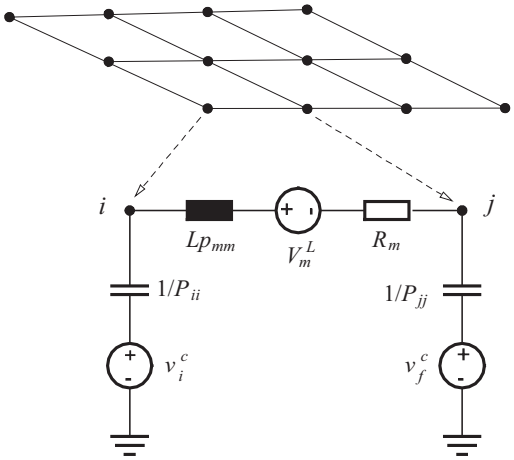


Figure 3.33: Geometry discretization and PEEC model [152]. Here, only the self term of potential and inductance are displayed. The full matrix model also contains mutual couplings of the equivalent circuit elements.

conductor cells and gives a good approximation of the actual PCB layout. The result of the PEEC calculation is an impedance matrix,

$$\mathbf{Z} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & \\ Z_{21} & Z_{22} & Z_{23} & \dots \\ Z_{31} & Z_{22} & Z_{23} & \\ & \vdots & & \ddots \end{bmatrix} \tag{3.30}$$

in which the main diagonal describes the self-impedance between two probe points and the off-diagonal elements denote the coupling between separate current paths. Due to skin- and proximity effect, the exact solution of the impedance matrix is frequency dependent $\mathbf{Z} = \mathbf{Z}(\omega)$. The frequency-dependent real part $\Re\{\mathbf{Z}(\omega)\}$ is based on the electric resistance of the copper tracks on the PCB, which can be neglected in comparison to the on-resistance of the power switches. The remaining imaginary part (i.e. the inductive or capacitive behavior) $\Im\{\mathbf{Z}(\omega)\}$ is only weakly influenced by skin- and proximity effect and can be modeled by a simple CL-network. The skin-effect is considered in the way that PEEC impedance

calculations were conducted at a high frequency (1 MHz), where the currents concentrate on the conductor edges. Dependent on the conductor geometry, the high frequency inductance shifts in the range of typically 30 % in comparison to the low freqency value.

The PCB of the IMC is modeled as a 2.5-D-geometry, that means the copper layers have no discretization in the z-direction, but the positions of the layers in the PCB layer stack are included into the model. This simplification is possible because the copper layer thickness is negligible in comparison to the width of the current path. Figure 3.34 shows three layers of the IMC power circuit, from which the impedance matrix is extracted. With the calculated values of $\mathbf{Z}$, a simulation model of the IMC is created which includes the relevant PCB track inductances and capacitances.

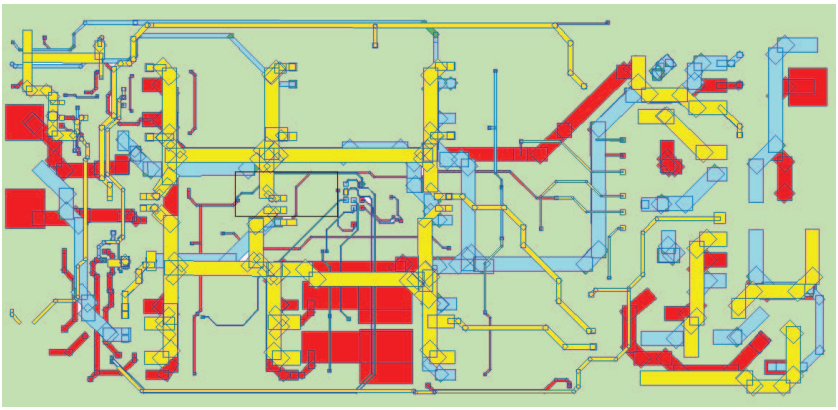


Figure 3.34: PEEC model of the three power PCB layers of the 6-layer IMC printed circuit board.

In general, inductances are only reasonable for current loops. In a switching power electronics converter, the current paths are changing due to commutation and the actual current path is determined by the switch configuration. This is incorporated in the model in such a way that partial inductances and their mutual couplings are considered for every commutation path. The total loop inductance is then determined by,

$$L_{tot} = \sum_{i,j} L_{ij} \tag{3.31}$$

where the diagonal elements L_{ii} are the self inductance terms and the off diagonal elements indicate the mutual inductance of different current paths. The determined impedance network, including the self- and mutual couplings as in eq. (3.31), defines the total loop inductance of every current path during the circuit simulation.

In order to test the performance of the simulation procedure, the standard CISPR 11 [105] was chosen for establishing the performance requirements, where the frequency range of 0.15 MHz to 30 MHz is considered for class A equipment. The voltage measured at the resistor, representing the input of a test receiver, in the simulation is used to calculate a quasi-peak maximum value $QP_{\max}(f)$. This is performed by linearly adding the values $V_h(f)$ of the spectral components positioned inside of the specified resolution bandwidth (RBW) as presented in section 2.5.2. By employing this procedure, one reduces the computational effort and the calculated emission level is slightly higher than the ones resulting from the exact calculation. The final result of the simulated CM and DM noise spectra, is depicted in Figure 3.35 along with the obtained experimental results.

The CM and DM CE levels show a very good correlation between measurement and simulation up to 5 MHz, from where it is probable that the non-modeled capacitive and magnetic coupling among the filter components becomes significant [155]. In the low frequency range 200-300 kHz, the simulated CM emission is about 5 dB higher than the measured values. It turned out that the CE spectrum is very sensitive to the load impedance to ground, which is the main CM noise path in this case. The most probable reason is the difficulty of experimentally measuring the capacitive coupling between the power semiconductors and the heatsink. Other reasons are the inter-component couplings and the influence of the gate drive, which provides various paths for HF currents. Furthermore, the models used for the cable, filter and load become less accurate for high frequencies ($>$ 5 MHz). The inclusion of the input EMC filter in the experiments increases the uncertainties of the model, as it becomes highly dependent on the modeled impedances.

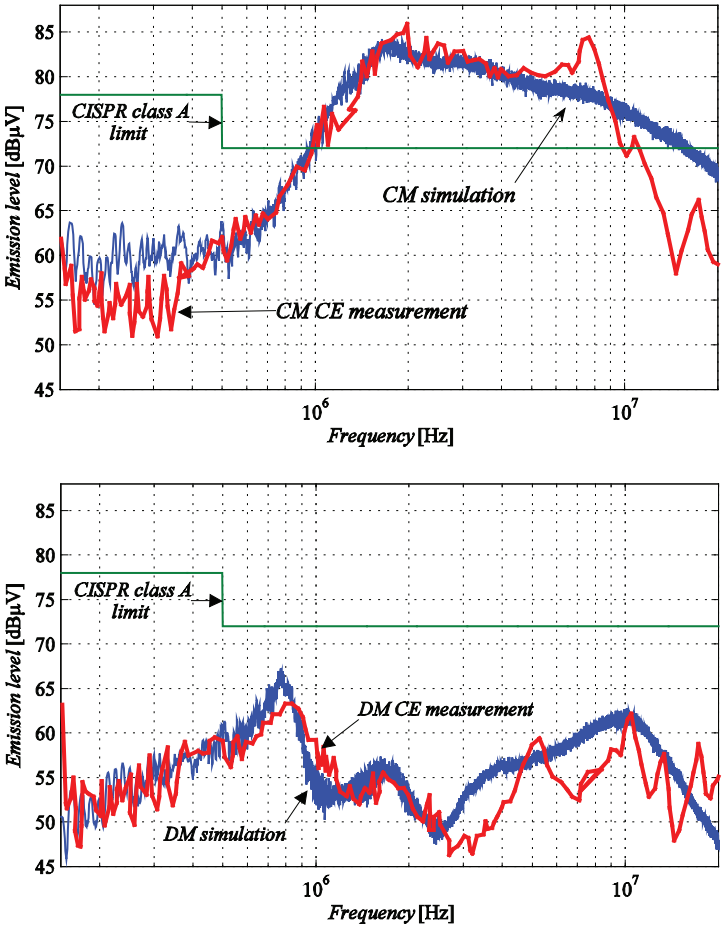


Figure 3.35: Differential and common mode noise emission levels according to measurement and simulation results.

3.6 Summary

This chapter has presented three-phase PWM converter systems as common- and differential-mode conducted emissions sources. These systems are typically employed as front-end or direct conversion converters in utility interfaced systems. The analyzed PWM converters are: Three-Phase Buck+Boost PWM Rectifier [130]; Three-Phase Three-Level Boost PWM Rectifiers [77,131]; and, Three-Phase Sparse Matrix Converters [85,88].

It has been presented that three approaches, namely: analytic calculation, experiments and simulation, can be integrated in order to obtain noise source models for the analyzed converters. The proper management and coordination of these tasks, allied to practical experience, usually leads to appropriate models and subsequent EMC compliance.

Fourier transformation is a very useful tool to analyze the frequency spectra of switched converters, but the analytical expressions can be extremely complex for the signals of three-phase PWM converters. Nevertheless, the employment of envelope functions in the the frequency domain to characterize the periodic signals has been proposed. This eases the calculation tasks and allows for the fast calculation of worst case filter attenuation requirements.

It has been suggested that numerical simulation in the time domain followed by numerical post-processing with Fast Fourier Transformation algorithms is a proper way to model PWM converters.

A model for the common mode propagation in a three-phase Buck+Boost PWM rectifier has been presented. This model is based on very simple simulations, from where CM and DM noise sources are derived. The propagation paths are modeled with the employment of equivalent impedance circuits, which are obtained from direct measurements performed in the individual components and in the power converter in order to define parasitic impedances. This model has been compared with conducted emission measurements performed with a 5 kW prototype, from where a very good correlation up to a frequency of 4 MHz is observed.

A modeling procedure is presented that allows for the design of input EMC filters for a Three-Phase Three-Level Boost PWM Rectifier has been proposed. The model is based in very simple equivalent circuits for common and differential mode. The model has been exemplary derived

for a 10 kW rectifier. The CM and DM voltage spectra, obtained from a simple numerical simulation of the system, are post-processed in order to obtain the signal levels that would be measured in an EMC test receiver. For that, the procedure presented in section 2.5.2 has been employed, leading to useful data for the design of EMC filters. The attenuation requirements for the system have been obtained and are used to design the CM and DM input filters.

Different modeling procedures for three-phase Sparse Matrix Converters have been presented. The first models are obtained with simplified equivalent circuits, similarly to the models obtained for the Three-Phase Three-Level Boost PWM Rectifier. These models are only to be employed in the design of EMC filters and do not cover the whole conducted emissions frequency range. Furthermore, envelope functions that define the highest emission levels have been proposed, leading to very simple functions for the noise sources of the models. A brief description of a more complete model is presented. This model considers the modeling of all circuits that influence the conducted emissions measurement range. Thus, it is a more complex procedure that has the potential of extending the useful frequency range of the model. The validity of the model has been shown with experimental results.

Chapter 4

EMC Filter Components

"The model principle constitutes the strongest support of the verified changes in the world." Max Scheler

4.1 Introduction

Aiming for Electromagnetic Compatibility of a high frequency switched three-phase PWM converter requires that the emissions caused by such converter are well controlled. This means that the currents generated by high switched voltages, either CM or DM, shall be adequately attenuated. In practice, this is achieved through good layout techniques, control of switching waveforms and proper low-pass filtering. Filters for the reduction of conducted emissions are built with passive elements. The basic building-blocks of filters, passive or active ones, are inductors, capacitors and resistors.

This chapter presents the most important characteristics for passive components to be used in EMC filtering of three-phase PWM converters. The major requirements for the implementation of such elements in a filter are explained.

Resistors are briefly reviewed and the main characteristics and demands are explained. Simple equivalent circuits are shown and the main application networks are presented.

A lumped model based on the physics of a capacitor is the basis for

a circuital model for such components. This model is further simplified to the classical RLC series connection, where the calculation of the ESR and ESL based on data sheet information is explained. Safety requirements that influence the types of capacitors to be employed in filters are reviewed. A study on the dependency of the volume of different technologies of filter capacitors with rated capacitance and voltage is performed, highlighting the relation volume $\times$ stored energy. From this study, a model that can be used for the minimization of the volume of filters is derived.

Filter inductors are divided into two categories, DM and CM inductors. Models are presented for both types along with experimental verification.

The operating principles of DM inductors are explained, based on the assumption of toroidal cores based inductors. Equivalent circuits are presented, showing the dependency of the equivalent circuits parameters with frequency, current and temperature. Thermal models for toroidal inductors are reviewed and a model, based on empirical considerations is derived. The calculation of parasitic capacitance, resistances and inductances is reviewed. A comparison among available core materials is performed, highlighting the major material characteristics for the filter application.

The physics of a three-phase CM inductor is explained in detail, from where equivalent circuits are derived. These equivalent circuits present dependency on the employed core material characteristics. The importance of the proper characterization of the material is highlighted and a method for the selection of the material for minimized volume inductors is proposed. The calculation of the leakage inductance is reviewed along with the related saturation issues.

Taking the parasitic elements of, both, inductors and capacitors into consideration, the high frequency performance of a filter might be severely affected. Recent research has put efforts into techniques called "parasitics cancellation", which ideally cancel the effects of parasitics. These research results have been proposed in the literature for single-phase circuits. The main networks employed in these techniques are presented. The cancellation of the equivalent series inductance of filter capacitors is reviewed and an application is experimentally tested in a three-phase filtering application.

A method for studying the impedances for CM and DM three-phase

inductive networks is proposed, which is applied in the analysis of the cancellation of parasitic parallel capacitance for, both, CM and DM inductive networks for filtering. Cancellation networks to be applied in three-phase filters are proposed along with a thorough analysis of parasitic effects that affect the performance of the capacitance cancellation networks. The possibility of asymmetrical cancellation is proposed, so that inductors applied with switching circuits do not significantly increase switching losses. An experimental implementation of these techniques proves the theoretical assumptions and highlights the practical limitations.

4.2 Resistors for High Power EMC Filtering

For simplification purposes, resistors are here considered linear time invariant elements that follow Ohm's law $i(t) = u(t)/R$, representing a proportionality constant between current and voltage in a two-port element. They dissipate electrical power. Since HF noise currents are to be minimized by a filter, dissipating their energy in resistors seems to be a good alternative. Nevertheless, high power PWM converters present high amplitude voltages and currents, which prevent the direct connection of resistors in series with high current paths or in parallel with high voltage levels. As the power in a resistor increases quadratically with current or voltage, the losses in a directly connected resistor may cause dramatic reduction of efficiency and increase in components volume. For these reason, resistors are typically employed in EMC input filters as damping elements that work on limiting the effects of strong resonances among reactive components, rather than filtering elements.

For high power PWM converters, resistors are typically connected in a way that losses are minimized. This means that the connection of resistors in series paths is done in parallel with inductors. The inductors conduct the low frequency current components. In parallel branches, the connection is done in series with capacitors, which cause a large drop for low frequency voltage components. This is shown in Figure 4.1.

Strong resonances are mainly observed close to the corner frequency of filters, thus frequencies that are much lower than the switching frequency or the range of frequencies of interest for conducted emissions. In order to implement damping networks for resonances, resistors typically present values that are not relevant for high frequency noise attenuation. The

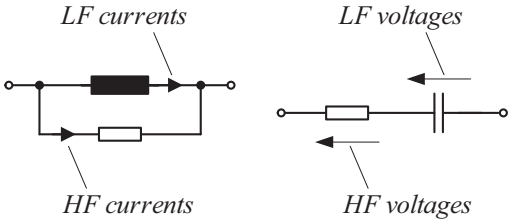


Figure 4.1: Connection of resistors in high power filtering circuits in order to reduce power dissipation.

explanation to that is that they limit the impedance of series connected capacitors and of parallel connected inductors and reduce the effect of such components in the filter's attenuation. For this reason, differently from low power applications where resistors are employed to filter conducted noise, high power input EMC filters do not profit of resistors HF impedance characteristics. Thus, the HF equivalent circuit of resistors can be, in most cases, neglected. Nevertheless, Figure 4.2 shows different models for resistors taking their characteristics into account. The values of the parasitic components can be obtained through parametric identification based on impedance measurements. It is also shown that the resistance might present dependence with frequency (f), current (I), voltage (U) and temperature (T). Depending on the objective of the analysis, very complex models including all these effects must be used. Typically, for conducted emission purposes, this is not required and a simple model can be applied.

Another application of resistors in input filters is for discharging the capacitors connected across the lines due to safety requirements. For instance, the standard for electrical safety in IT equipment IEC 60950 [91] specifies that, if the capacitors connected across the lines are larger than 100 nF, they should be discharged to a voltage lower than 60 V in less than 10 s after a supply disconnection. For this reason, resistors of large values are to be connected in parallel with such capacitors.

4.2.1 Requirements for Resistors

Extremely important functional requirements apply to resistors employed in input filters, namely: (i) power handling capability; (ii) capacity to

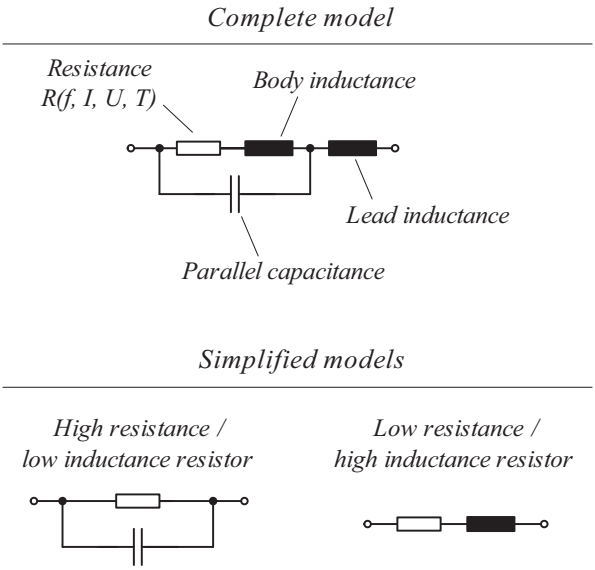


Figure 4.2: Equivalent circuits for resistors.

withstand high voltage surges, and; (*iii*) low parasitics. Added to those, other requirements, like low volume and costs, apply.

The *surge voltage* of a resistor is the maximum voltage that it can withstand for a limited period of time. Surges are not only due to electrostatic discharges or lightning, but happen when a load in parallel with the filter or a power switch is switched, or the equipment is connected and disconnected from the energy supply. Due to the highly reactive characteristics of typical EMC filters, transients are observed in all these situations. These transients shall be carefully studied in order to specify the requirement of any resistor employed in a filter.

The *rated power* is very important since losses might damage the resistors. In an input filter, the calculation of losses must be done for low frequency components as well as for high frequency ones. These losses shall be taken into account in the component specification and in the definition of the resistor's installation practice, so that interconnecting wires or printed circuit board pads and tracks are properly implemented. This is because the largest amount of heat in a resistor flows typically through

its leads due to coating and insulation higher thermal resistances.

Aiming for low volume and low parasitic effects, surface mount resistors present very good performance. They present the lowest series inductance and the smallest volume and board occupation characteristics. Special attention shall be put in the voltage and surge capability of such devices.

4.3 Capacitors for EMC Filtering

The most basic low pass-filter is a capacitor in parallel with the signal/noise source. This configuration offers an important advantage over series connected resistors or inductors, since the low frequency currents, typically responsible for the energy transfer, do not flow through the component.

Ideal capacitors provide steadily decreasing impedance with frequency, which causes a reduction in the system's HF noise voltages. Unfortunately, commercially available capacitors are not ideal. Losses in the dielectric material, due to high voltages, and on the conductive material of the leads and plates/foils, due to the circulating currents, can be modeled as resistances. Besides, the arrangement of the conductive parts comprises loops where internal and external magnetic fields are coupled and the effect of distributed inductances is observed. These effects are shown in the equivalent circuit of Figure 4.3, where the plates on both sides of the dielectric have a capacitance C with the dielectric losses being modeled in the parallel resistance R_{diel}. The ohmic losses in the conductive plates are modeled with R_{plate}. The leads present a resistance R_{lead} and an inductance L_{lead} in parallel with a capacitance C_{lead}. This is a complete model of the capacitor, based on the physical construction of the device. However, for the vast majority of the applications, a simpler model is sufficient. This model consists on the series connection of the *series equivalent resistance* (ESR), the *series equivalent inductance* (ESL) and the total capacitance (C). The ESR typically presents a strong dependency with frequency, while the capacitance varies with the applied voltage u_c. These parameters also depend on the operating temperature. The aforementioned models do not take the magnetic coupling with external components, which can be taken into account through a coupling coefficient with the ESL. A comprehensive study on the physics and technology

related aspects for capacitors is found in [156] and [157].

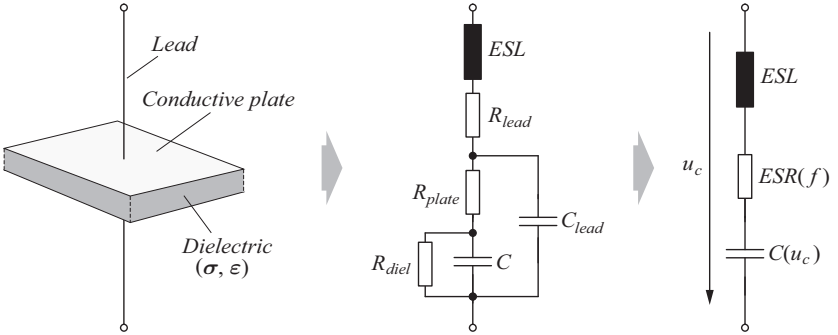


Figure 4.3: Physical model of a capacitor followed by two equivalent circuits.

The value of the parasitic components in the equivalent circuit of a capacitor show strong dependency with the technology employed in the fabrication of the device. For EMC filtering capacitors to be connected to the electrical energy distribution grid, four main technologies are available: Epoxy-filled metalized paper, metalized polyester film, polypropylene, and ceramic. The highest compactness is achieved with ceramic dielectrics, but these are only available at low capacitance values. Epoxy paper capacitors seem to be the most reliable and fire-safe because of their self-healing properties, but can be 30% to 100% larger than other technologies for the same capacitance. The large values are not available as well. Furthermoe, epoxy paper capacitors present high ESR and temperature drift. Polypropilene based capacitors present the lowest ESR and are desirable to filter very high frequency noise.

As previously mentioned, safety is a major issue for capacitors connected to the power grid. Regulatory agencies demand challenging requirements in order to approve the commercialization of such capacitors. Safety requirements for the capacitors are stated in EN 123400 [158] and divide the capacitors into two mains types: X and Y capacitors. The X capacitors are to be applied where their failure does not lead to electric shock hazard, while the Y capacitors must be applied where this risk occurs. In practice this means that X capacitors can be placed across the phases, while Y capacitors are allowed between phases and PE. This is illustrated in Figure 4.4, from where the names, X and Y, are explained.

Depending on the capacitor's surge voltage capability, the X and Y capacitors are further sub-divided as shown in Table 4.1 and Table 4.2, where U_N is the rated voltage.

Table 4.1: Sub-classes of X capacitors and their requirements.

Class	*Impulse* (1.2/50 μs)	*1000 hours test*
X1	4 kV ($C \leq 1\,\mu$F)	$1.25 \times U_N$ + 1kV/ 100ms every hour
X1	$4\,\text{kV}/\sqrt{C}$ ($C \geq 1\,\mu$F)	$1.25 \times U_N$ + 1kV/ 100ms every hour
X2	2.5 kV ($C \leq 1\,\mu$F)	$1.25 \times U_N$ + 1kV/ 100ms every hour
X2	$2.5\,\text{kV}/\sqrt{C}$ ($C \geq 1\,\mu$F)	$1.25 \times U_N$ + 1kV/ 100ms every hour
X3	None	$1.25 \times U_N$ + 1kV/ 100ms every hour

Besides X- and Y-rated capacitors, printed circuit boards can be effective capacitors. Although capacitances are of small value when compared with off-the-shelf components, they present very good behavior for high frequencies. The achievable capacitance can be estimated from,

$$C_{PCB} = \frac{\epsilon_{PCB}\, A}{d}, \tag{4.1}$$

where ϵ_{PCB} is the permittivity of the PCB insulation material, A is the total area between two layers and d is the width of the insulation layer. Taking $\epsilon_{PCB} \approx 3.6\epsilon_o$, and an insulation width of 160 μm, the capacitance per square centimeters is shown in Figure 4.5.

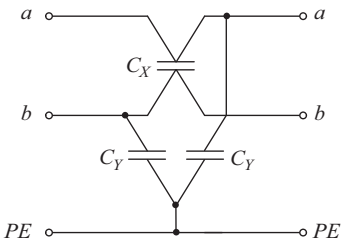


Figure 4.4: Connection of X and Y capacitors.

Table 4.2: Sub-classes of Y capacitors and their requirements.

Class	*Insulation type*	*Impulse*	*1000 hours test*
Y1	Double or reinforced	8 kV	$1.7 \times U_N$ + 1kV/ 100ms every hour
Y2	Basic or supplementary	5 kV	$1.7 \times U_N$ + 1kV/ 100ms every hour
Y3		None	$1.7 \times U_N$ + 1kV/ 100ms every hour
Y4	$\leq 250V$ $\leq 150V$	2.5 kV	$1.7 \times U_N$ + 1kV/ 100ms every hour

4.3.1 The Self-resonance of Filter Capacitors

Taking the equivalent circuit of a capacitor as in Figure 4.3, the connection of C and ESL create a series resonance that is responsible for a worsening performance of a capacitor for high frequencies. Although the final ESL depends on the physical connection of the capacitor in a filter (the total ESL depends on the closed loop in which the capacitor current flows), manufacturers measure the ESL of their capacitors for a given impedance measurement test setup. This represents a measure of quality of the components and is very important in order to estimate the attenuation provided by a capacitor at a given frequency and circuit.

Based on data sheet information [159], the self-resonance frequency $f_{o,C}$ of X rated capacitors is plotted in Figure 4.6. It is seen an exponential dependency with frequency, capacitance and rated voltage. This dependency can be modeled with the expression:

$$f_{o,C} = k_{o,1} C^{k_{o,2}} U_C^{k_{o,3}}, \tag{4.2}$$

where, for the X2 foil capacitors,

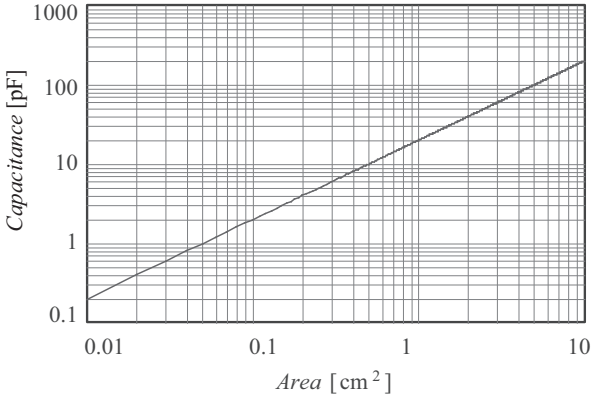


Figure 4.5: Capacitance per area for a typical PCB material.

$$k_{o,1} = 75 \cdot 10^{-6}\,\text{Hz} \tag{4.3}$$
$$k_{o,2} = -0.612 \tag{4.4}$$
$$k_{o,3} = 2.65 \tag{4.5}$$

For ceramic types, the self-resonance of the components is typically much higher than for foil capacitors due to the shorter or virtually no leads and body construction. Nevertheless, it is much more difficult to estimate the ESL for these components as it strongly depend on the employed PCB layout.

4.3.2 The Equivalent Series Resistance

The *equivalent series resistance* ESR is the resistance that if connected with an ideal capacitance leads to an equivalent impedance, which is equal to the one of the real capacitor for a given frequency. This is an important parameter, since it defines losses, and the minimum impedance of a capacitor, which occurs at the resonance frequency. Thus, the ESR damps the self-resonance, but puts a lower boundary for the impedance of a capacitor.

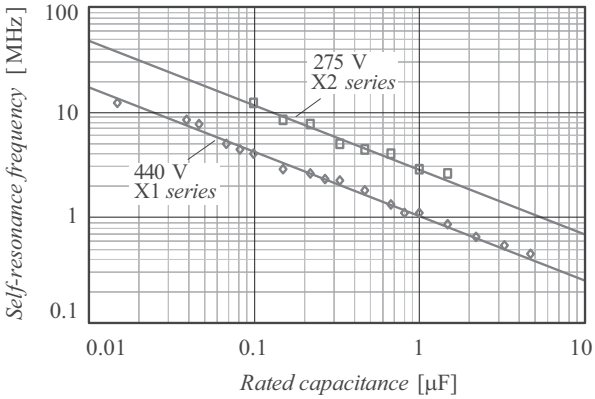


Figure 4.6: Variation of self-resonance frequency of X foil capacitors with rated capacitance and voltage.

As opposed to electrolytic capacitors, the low frequency ESR is not an important parameter for a filter capacitor. This resistance presents a strong dependency with frequency and varies with temperature as well. Typically, the ESR is not explicitly given in manufacturers data sheets. One way to estimate this resistance is by using the *dissipation factor*. This is typically given in data sheets, even though for a limited frequency range.

Considering the last equivalent circuit of Figure 4.3, it is seen that if a varying voltage is applied to the terminals of the component, the power contains a real and an imaginary parts. If the frequency of this voltage is much lower than the self-resonance, the impedance is dominated by a resistive part and a capacitive reactance. The ratio between these two impedances defines the *dissipation factor*, usually named tanδ, so that,

$$\tan\delta = \frac{ESR}{X_C} = ESR\omega C. \tag{4.6}$$

Isolating the ESR in eq. (4.6) leads to,

$$ESR(f) = \frac{\tan\delta}{2\pi f\, C}, \tag{4.7}$$

from where the ESR can be calculated given data sheet information.

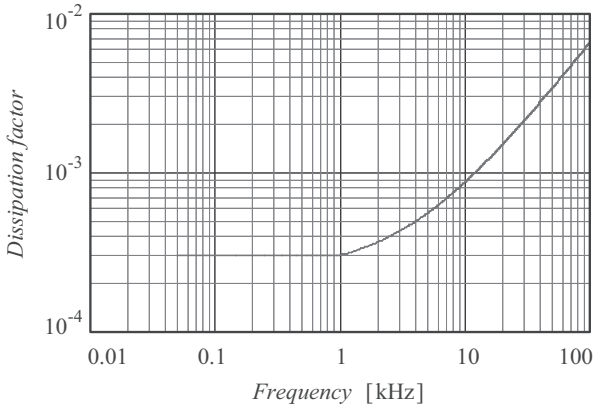


Figure 4.7: Typical dissipation factor for a foil capacitor with polypropylene dielectric [159].

Alternatively, the *quality factor* Q of a capacitor is defined as the reciprocal of the dissipation factor,

$$Q = \frac{1}{\tan\delta}. \tag{4.8}$$

The dissipation factor is not constant with frequency and care should be taken when calculating the ESR. Figure 4.7 shows the dissipation factor given in data sheet information for a foil capacitor with polypropylene dielectric. It is seen that the resistive portion of the impedance grows with frequency. This leads to the thought that the ESR increases with frequency. For a 220 nF capacitor, the ESR was calculated with the dissipation factor curve of Figure 4.7 and eq. (4.7). Examining Figure 4.8 it is observed that the ESR actually decreases with frequency until a minimum level.

4.3.3 The Volume of Filter Capacitors

The volume of foil capacitors has been discussed in [6], where a generic specific breakdown field strength E_{br} is assumed for the dielectric material. And the geometry shown in Figure 4.9 is the simplified of a foil capacitor, where the thickness of the foils is neglected.

The capacitance of the structure is given by,

$$C = \frac{\epsilon A_F}{d}. \tag{4.9}$$

The volume of the structure is,

$$Vol_C = A_F d. \tag{4.10}$$

The maximum voltage of the capacitor is defined as the electric field times the distance between the plates,

$$U_C = E_{br} d. \tag{4.11}$$

Isolating d in eq. (4.11) and replacing it in Figure 4.9 and Figure 4.10 leads to,

$$Vol_C = \frac{C U_C^2}{\epsilon E_{br}^2}. \tag{4.12}$$

Knowing that the energy in the capacitor E_c is,

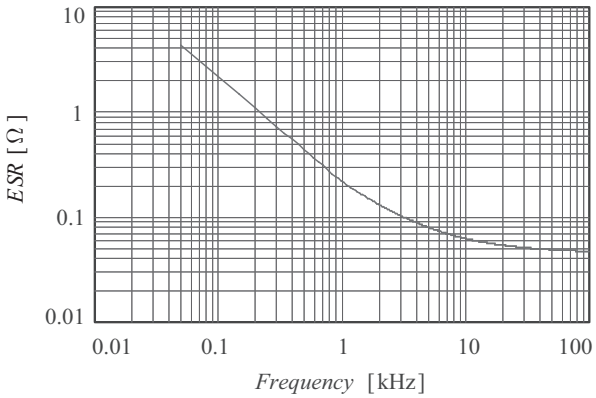


Figure 4.8: Equivalent series resistance for a 220 nF foil capacitor with polypropylene dielectric [159] for the dissipation factor of Figure 4.7.

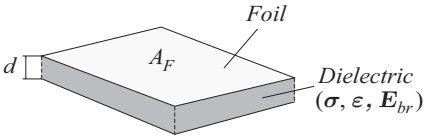


Figure 4.9: Assumed capacitor geometry for a foil capacitor.

$$E_C = \frac{CU_C^2}{2}, \tag{4.13}$$

it is seen that the volume of the foil capacitor is proportional to the capacitively stored energy. Thus, a volumetric coefficient k_C can be defined for foil capacitors, so that,

$$Vol_C = k_C E_C = k_C \frac{CU_C^2}{2}. \tag{4.14}$$

This assumptions are valid also for ceramic type capacitors or any type that the plate width can be neglected. This is not the case for electrolytic capacitors.

Although, in practice, different geometric structures are used to construct capacitors, the dependency of volume with energy is verified in practice, where the calculated volume of capacitors has been plotted in along with approximation curves. The volume of the capacitors to be used in the filters can be approximated by a curve generated by Minimum Squares regression of the volumes calculated for commercially available X type capacitors (foil [159] and ceramics [160]) as well as for ceramic capacitors rated for the Japanese mains [160].

The calculated volumetric coefficients for these capacitors are given in Table 4.3. The much smaller volumetric coefficient of the ceramic type capacitors, allows for more compact filters.

4.4 Differential Mode Inductors

A differential mode inductor is employed in three-phase EMC power filters in order to increase the high frequency impedance of series current paths, so that DM noise currents are reduced. The impedance of a DM inductor

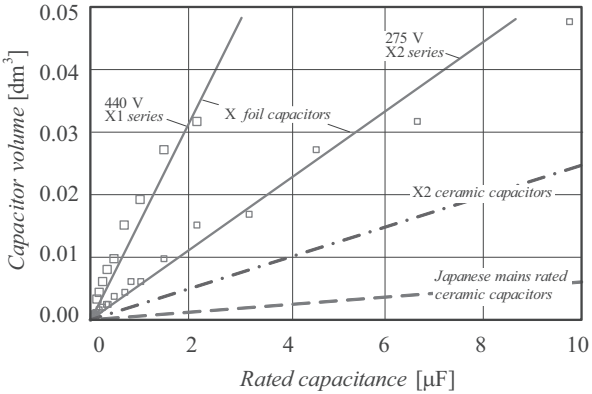


Figure 4.10: Volume and approximation curves for mains rated capacitors.

Table 4.3: Volumetric coefficient for different X capacitors technologies.

Technology	Manufacturer	*Voltage*	k_C
X2 foil	Evox-Rifa	275 V / 400 V	$46.9 \cdot 10^{-6} \frac{\mathrm{m}^3}{\mathrm{F \cdot V^2}}$
X2 ceramic	Murata	250 V	$16.4 \cdot 10^{-6} \frac{\mathrm{m}^3}{\mathrm{F \cdot V^2}}$
Jap. mains cer.	Murata	250 V	$4.07 \cdot 10^{-6} \frac{\mathrm{m}^3}{\mathrm{F \cdot V^2}}$

is its most important characteristic and is the result of the geometrical configuration of a closed current path of conductors winded onto cores of various materials employing proper insulation. In the following, the main effects that influence the impedance of a power DM inductor are introduced.

4.4.1 Self-inductance

The self-inductance is defined as the proportionality value between the rate of change of the magnetic flux linkage (Φ) with respect to the current that generates it,

$$L_s = N_L \frac{d\Phi}{di_L}, \tag{4.15}$$

where N_L is the number of turns of the employed conductor and i_L is the circulating current.

The voltage across an inductor (u_L) is given by the rate of change of the magnetic flux linkage with respect to time (t),

$$u_L = N_L \frac{d\Phi}{dt}. \tag{4.16}$$

Solving the system of differential equations formed by eq. (4.15) and eq. (4.16), leads to,

$$u_L = L_s \frac{di_L}{dt}, \tag{4.17}$$

which, by applying Fourier transformation, leads to the expression in the frequency domain,

$$X_L(j\omega) = \frac{U_L(j\omega)}{I_L(j\omega)} = j\omega L_s, \tag{4.18}$$

where X_L is the inductive reactance of the inductor and $\omega = 2\pi f$ is the angular frequency. This reactance presents a steady increase with frequency, shown in eq. (4.18) and this is typically the main effect in the impedance of an inductor.

For constructing a DM inductor, toroidal cores present some advantages, which make them the preferred ones for EMC filters. The main disadvantage of a toroidal core is that the windings are more difficult to wind than for cores which make use of coils formers, thus, requiring special winding machines or hand made windings. The most relevant advantages of these cores are:

- lowest external magnetic field, which hinders magnetic coupling with other elements in the circuit and reduces proximity effect generated losses;

- small volume because the thermal resistance is typically smaller than other core types;

- lowest core related costs, since no special mechanical post-processing is required as is opposite to cores where an air-gap is included that needs to be smoothed.

For the reasons mentioned above, only toroidal cores are considered here.

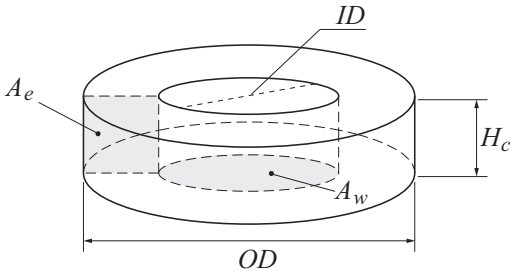


Figure 4.11: Toroidal core with relevant dimensions.

Given the geometry of a square-section toroid as shown in Figure 4.11, the self-inductance of an inductor built on a toroidal core is defined as [161]

$$L_{s,toroid} = \frac{\mu_o \mu_r N_L^2 H_c}{2\pi} \cdot \ln\left(\frac{OD}{ID}\right), \tag{4.19}$$

where $\mu_o = 4\pi 10^{-7}$ H/m is the permeability of free space and μ_r is the relative permeability of the core material.

Core manufacturers define a parameter named *inductance per turn* (A_L), which defines the initial inductance for a single turn of conductor wound on the respective core. This is a useful parameter for designing inductors. For a toroid, it is defined as

$$A_L = \frac{\mu_o \mu_r H_c}{2\pi} \cdot \ln\left(\frac{OD}{ID}\right), \tag{4.20}$$

and the inductance is alternatively given by,

$$L_{s,toroid} = A_L N_L^2. \tag{4.21}$$

Unfortunately, core materials do not present constant characteristics and this must be taken into account when modeling a DM inductor, unless an air core is applied. This is rarely the case since materials with higher relative permeability (cf. eq. (4.19)) allow for the reduction of the dimensions and/or number of turns for the same given inductance.

The main characteristic for a core (ferromagnetic) material is its relative permeability. Eddy currents, hysteresis and residual losses strongly influence the value of permeability and vary with frequency, magnetic field, temperature and aging. Typically, the effects of temperature and aging can be controlled, so that during the design of an inductor, worst case temperatures and aging are taken into account by observing data sheet information. On the other hand, varying frequency and magnetic field direct influences the instantaneous characteristics of an inductor and need to be correctly modeled. The manufacturers provide curves for the dependency of permeability with, both, frequency and magnetic field.

The magnetic field (H) in an inductor is dependent on the electromotive force ($N_L I_L$), which is generated by the circulating current in a given geometric arrangement. For the case of DM inductors for high power three-phase PWM converters, the involved low frequency currents are of high magnitude. Therefore, high peak magnetic flux is to be expected. On the other hand, the high frequency currents are expected to be small, since capacitors and/or smoothing inductors are typically connected between the filter inductors and the power converter. Thus, low core losses due to the flux density variation are typical. For this reason, high frequency core losses do not represent a main concern in the design of DM filtering inductors.

Saturation is an important phenomenon and is usually specified as a maximum flux density (B_{sat}), from where the hysteresis loop of the material is outside the linear area and the material permeability approaches that of free space. The flux density (B) is defined as,

$$B = \mu_o \mu_r H. \tag{4.22}$$

The magnetic field is given as,

$$H = \frac{N_L I_L}{l_e}, \tag{4.23}$$

where l_e is the equivalent magnetic path length of the core.

The self-inductance can be redefined as,

$$L_{s,toroid} = \frac{\mu_o \mu_r N_L^2}{l_e}, \tag{4.24}$$

Solving the equation system formed of eq. (4.22), eq. (4.23) and eq. (4.24), the following condition to avoid saturation shall be obeyed,

$$N_L I_{L,max} < \frac{l_e B_{sat}}{\mu_o \mu_r}. \tag{4.25}$$

Since the conducted emissions regulations start at 150 kHz, materials with good HF performance shall be employed. This typically reduces the choice of materials to iron powder, ferrite and amorphous materials. If low switching frequencies are used, iron alloys can also be employed, but the HF inductor's impedance would be due to core losses, rather than due to the reactive component of the impedance. If high permeability materials (ferrites or amorphous) are employed, an air gap must be included and most of the advantages of toroidal cores would fade. Besides that, iron powder materials present much higher saturation flux density than ferrites, allowing for a volume reduction. For these reasons, only iron powder materials are considered here. The main characteristics of appropriate materials for DM inductors are compared in the following.

Saturation flux density and maximum operating temperature are shown in Table 4.4 for different types of iron powder materials [162, 163] in their standard permeability value.

Table 4.4: Characteristics of iron powder materials for DM inductors.

Manufacturer	*Material*	Permeability	B_{sat}	T_{max}
Magnetics	MPP	60	0.75 T	130 °C
Magnetics	High Flux	60	1.30 T	130 °C
Magnetics	Cool Mu	60	0.90 T	130 °C
Micrometals	-26	75	1.00 T	110 °C
Micrometals	-52	75	1.00 T	110 °C

Figure 4.12 shows the magnitude of the complex permeability versus frequency of various iron powder core materials appropriate for DM induc-

tors. From Figure 4.12 it is seen that KoolMu and Molypermaloy (MPP) present the lower relative reduction of permeability with increasing frequency. Figure 4.13 shows that High Flux has the lowest permeability reduction with higher magnetic field values. MPP outperforms the other materials in the high frequency losses (cf. Figure 4.14). High Flux presents a very high saturation flux $B_{sat} = 1.3$ T, which is 30 % to 70 % higher

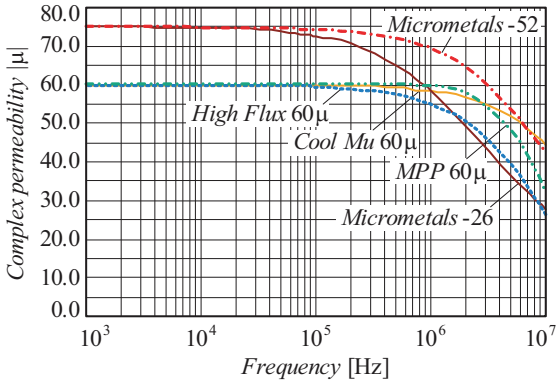


Figure 4.12: Magnitude of the complex permeability versus frequency of core materials for DM inductors [162, 163].

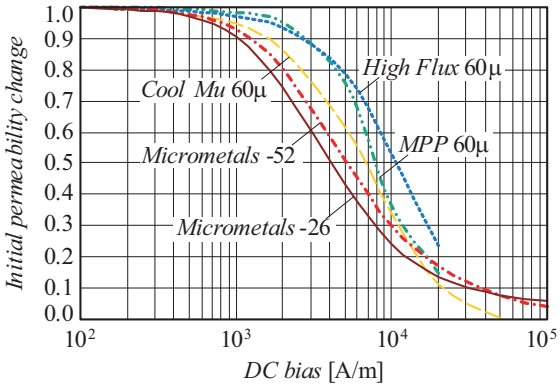


Figure 4.13: Per unit change in permeability in dependency of the dc bias of core materials for DM inductors [162, 163].

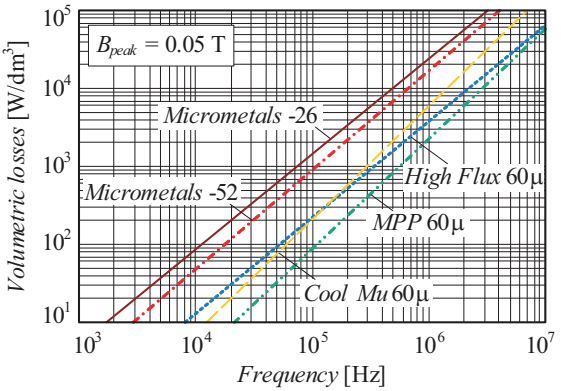


Figure 4.14: Volumetric losses in dependency of frequency for a peak flux density of 50 mT of core materials for DM inductors [162, 163].

than the others. Depending on specific situations, like large HF current ripple, special temperature requirements and costs, different materials are to be chosen. If the main concern is volume, High Flux is a very good option.

As seen in the previous figures, the permeabilities of core materials vary in great extent and a constant value for the self-inductance is not a realistic representation of the component. For this reason, the self-inductance must be redefined as,

$$L_{s,toroid}(I_L, f) = A_L N_L^2 \cdot \frac{\mu_r(I_L, f)}{\mu_r(I_L = 0\text{A}, f = 0\text{Hz})}. \tag{4.26}$$

4.4.2 Losses and Associated Resistances

The losses associated with the core and the conductors employed in an inductor can be modeled as series resistances, which add impedance to the series connected self-inductance. These are explained in the following.

Series Core Resistance

Three main effects cause losses in the core, namely: eddy currents, hysteresis and residual losses. Eddy currents are difficult to estimate and depend on the geometry of the core as well as in the material. Fortunately, the eddy current generated losses are typically very small and can be neglected [164].

Following the procedure presented in [164], the series resistance due to core losses are modeled in the following.

Hysteresis and residual losses can be modeled with the Steinmetz equation, which relates the volumetric losses (P_{vol}) in the material with frequency and flux density,

$$P_{vol} = K_c f^{\alpha} B^{\beta}, \tag{4.27}$$

where K_c, α and β are known as Steinmetz coefficients. K_c presents dependency with temperature. These coefficients are typically curve fitted from losses measurements and are optimized for certain frequency ranges.

The magnetic flux linkage is defined as the flux density through the core cross-section area,

$$\Phi = A_e B. \tag{4.28}$$

Having the inductance defined by,

$$L_{s,toroid} = N_L \frac{d\Phi}{di_L} = N_L A_e \frac{dB}{di_L}, \tag{4.29}$$

and assuming sinusoidal flux density and current,

$$B(t) = B_p \cdot \sin(2\pi\omega t) \tag{4.30}$$

$$i(t) = I_p \cdot \sin(2\pi\omega t + \phi_I), \tag{4.31}$$

the inductance is redefined as,

$$L_{s,toroid} = \frac{N_L A_e B_p}{I_p}. \tag{4.32}$$

In order to model the losses in the material, a series complex permeability ($\bar{\mu}_s$) is defined, which takes, both, reactive and active impedances of an inductor into account,

$$\bar{\mu}_s = \mu' - j\mu'', \tag{4.33}$$

so that the series impedance of an inductor ($Z_{L,core}$) due to the core material is,

$$Z_{L,core} = R_{s,core} + j\omega L_{s,toroid} = j\omega A_L N_L^2 \cdot \frac{\bar{\mu}_s}{|\bar{\mu}_{s,initial}|}, \tag{4.34}$$

from where,

$$R_{s,core} = A_L N_L^2 \cdot \frac{\omega\mu''}{|\bar{\mu}_{s,initial}|} \tag{4.35}$$

$$L_{s,toroid} = A_L N_L^2 \cdot \frac{\mu'}{|\bar{\mu}_{s,initial}|}. \tag{4.36}$$

The losses in the core are,

$$P_{core} = V_c \cdot P_{vol} = R_{s,core} \cdot \frac{I_p^2}{2}, \tag{4.37}$$

where V_c is the core volume.

Inserting eq. (4.32) into eq. (4.36) gives,

$$A_L N_L^2 \cdot \frac{\mu'}{|\bar{\mu}_{s,initial}|} = \frac{N_L A_e B_p}{I_p}, \tag{4.38}$$

from where,

$$B_p = \frac{A_L N_L \mu' I_p}{|\bar{\mu}_{s,initial}|\, A_e}. \tag{4.39}$$

Inserting eq. (4.39) into eq. (4.27) leads to,

$$P_{vol} = K_c f^{\alpha} \left(\frac{A_L N_L \mu' I_p}{|\bar{\mu}_{s,initial}| \, A_e} \right)^{\beta}. \tag{4.40}$$

Finally, substituting eq. (4.40) and eq. (4.35) in eq. (4.37) gives,

$$R_{s,core} = 2 V_c K_c f^{\alpha} I_p^{\beta-2} \left(\frac{A_L N_L \mu'}{A_e \, |\bar{\mu}_{s,initial}|} \right)^{\beta}. \tag{4.41}$$

The series resistance of an inductor due to the losses in the core can be modeled with eq. (4.41), where the large signal influence of the circulating current is taken into account and not only the small signal results arising from the measurement of the complex permeability.

Unfortunately, core manufacturers of iron powder materials do not typically provide separate measurements for both components of the complex permeability. This makes the modeling of the HF core resistance difficult. In practice this does not heavily impact the impedance of the DM inductor because the core losses are typically very small. This is due to the small HF variation of the flux density generated by the very small HF current ripple.

Series Wire Resistance

The inductors designed for HF power filtering are typically designed using a single layer. This measure ensures that the winding parasitic parallel capacitance is low and that proximity effect can be neglected. With this assumption, the resistance of the inductor's wire is dependent on skin effect and the conductor's characteristics. Furthermore, in order to profit from the increased resistance with frequency, solid round conductors are employed instead of paralleled or Litz wires.

A solid round conductor is shown in Figure 4.15 with its relevant dimensions. The dc resistance for such a wire is given by,

$$R_{w,dc} = \frac{4 l_w \rho_w}{\pi \phi_w^2}, \tag{4.42}$$

where ρ_w is the wire resistivity.

The resistivity of a conductor is dependent on temperature and for copper it is approximately,

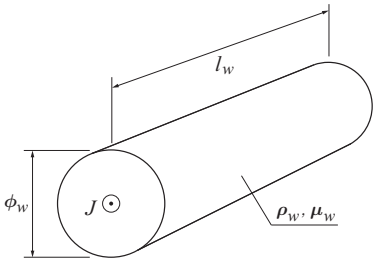


Figure 4.15: Solid round conductor with permeability μ_w and resistivity ρ_w.

$$\rho_{Cu} = 1.78 \cdot 10^{-8} \cdot (1 + 0.0039 \cdot (T - 20)) \ [\Omega \cdot \mathrm{m}], \tag{4.43}$$

with the temperature T given in °C.

For a round conductor with a diameter much larger than the skin depth, the high frequency electric and magnetic field distributions present an approximate exponential decay (cf. Figure 4.16) with the distance x from the surface of the conductor [24],

$$|J(x)| = J_s e^{-x\sqrt{\pi f \mu_w \sigma_w}}, \tag{4.44}$$

where $\sigma_w = 1/\rho_w$ is the conductor's conductivity.

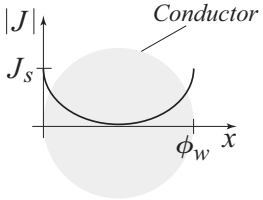


Figure 4.16: HF current distribution in a round conductor with a diameter much larger than the skin depth.

The skin depth (δ) is defined as,

$$\delta = \frac{1}{\sqrt{\pi f \mu_w \sigma_w}}. \tag{4.45}$$

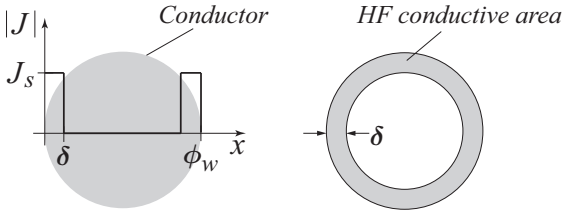


Figure 4.17: Simplified HF current distribution in a round conductor with a diameter much larger than the skin depth.

Assuming a constant current distribution up to one skin depth, the resistance for high frequencies can be calculated by reducing the conductive area as shown in Figure 4.17. And the resistance for high frequencies can be calculated by,

$$R_{w,ac} = \frac{l_w \rho_w}{\pi \left(\phi_w \delta - \delta^2\right)}, \tag{4.46}$$

where the term δ^2, being much smaller than $\phi_w \delta$ can be neglected. Thus,

$$R_{w,ac} \cong \frac{l_w \rho_w}{\pi \phi_w \delta}. \tag{4.47}$$

Replacing the definition of the dc resistance leads to,

$$R_{w,ac} = R_{w,dc} \cdot \frac{\phi_w}{4\delta}. \tag{4.48}$$

Finally, considering the definition of the skin depth,

$$R_{w,ac} = \frac{l_w}{\phi_w} \cdot \sqrt{f \cdot \frac{\mu_w}{\pi \sigma_w}}. \tag{4.49}$$

If the diameter of the round conductor is comparable to the skin depth, Maxwell equations should be solved and the AC resistance is given by [161],

$$R_{w,ac} = R_{w,dc} \cdot F_R. \tag{4.50}$$

The coefficient F_R is defined as,

$$F_R = \frac{\xi}{4\sqrt{2}} \cdot \left[\frac{\mathrm{Ber}\,(0,\xi)\,\mathrm{Bei}\,(1,\xi) + \mathrm{Ber}\,(0,\xi)\,\mathrm{Ber}\,(1,\xi)}{\mathrm{Ber}\,(1,\xi)^2 + \mathrm{Bei}\,(1,\xi)^2} + \right. \\ \left. - \frac{\mathrm{Bei}\,(0,\xi)\,\mathrm{Ber}\,(1,\xi) + \mathrm{Bei}\,(0,\xi)\,\mathrm{Bei}\,(1,\xi)}{\mathrm{Ber}\,(1,\xi)^2 + \mathrm{Bei}\,(1,\xi)^2} \right], \tag{4.51}$$

where $\mathrm{Ber}(i, var)$ and $\mathrm{Bei}(i, var)$ are Kelvin functions of order i on variable var and,

$$\xi = \frac{\phi_w}{\sqrt{2}\delta}. \tag{4.52}$$

If more than one winding layer is used in the inductor, the calculation of the AC resistance can be performed with eq. (4.53) [165]. This equation defines the AC winding resistance of a coil wound inductor with an integer number of layers (N_{layers}).

$$R_{w,ac} = R_{w,dc} \cdot A \cdot \left[\frac{e^{2A} - e^{-2A} + 2\mathrm{sin}(2A)}{e^{2A} - e^{-2A} + 2\mathrm{cos}(2A)} + \right. \\ \left. + \frac{2(N_{layers}^2 - 1)}{3} \cdot \frac{e^{A} - e^{-A} - 2\mathrm{sin}(2A)}{e^{A} + e^{-A} + 2\mathrm{cos}(2A)} \right], \tag{4.53}$$

where,

$$A = \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \cdot \frac{\sqrt{\phi_w^3}}{\delta\sqrt{d_{wires}}}, \tag{4.54}$$

with d_{wires} being the distance between two adjacent conductors.

Equation eq. (4.53) can be further simplified to [164],

$$R_{w,ac} \cong R_{w,dc} \cdot A \cdot \left[1 + \frac{2(N_{layers}^2 - 1)}{3} \right], \tag{4.55}$$

for,

$$\text{if } N_{layers} = 1 \Rightarrow f \geq \frac{\rho_w d_{wires}}{\pi \mu_w \phi_w^3} \cdot \left(\frac{4}{\pi}\right)^{\frac{3}{2}} \tag{4.56}$$

$$\text{if } N_{layers} > 1 \Rightarrow f \geq \frac{16 \rho_w d_{wires}}{\pi \mu_w \phi_w^3} \cdot \left(\frac{4}{\pi}\right)^{\frac{3}{2}}, \tag{4.57}$$

where μ_w is the permeability of the wire.

Depending on the diameter of the conductor, either eq. (4.49) or eq. (4.50) can be used to model the resistance of a round conductor in dependency of frequency. If the inductor has more than one layer, eq. (4.55) is a better option.

4.4.3 Parasitic Parallel Capacitance

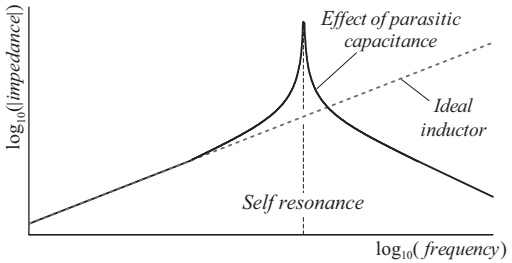


Figure 4.18: Illustration of an inductor's impedance curve showing the parallel capacitance effect on the impedance magnitude for high frequencies.

The impedance of an inductor typically presents a maximum at the so called self-resonance frequency of the component. The *self-resonance* of an inductor is the minimum frequency where the inductive reactance (X_L) equals the capacitive reactance (X_C). At this frequency a resonance occurs and the impedance reduces with frequency. This effect is modeled as a capacitor in parallel with the inductor. The observed capacitance is a consequence of the physical arrangement of the wires/turns (good conductors), core body (typically reasonable conductor) and the isolation coating/layers (dielectric). This capacitive behavior is a highly undesirable effect since it might greatly reduce the attenuation provided by a

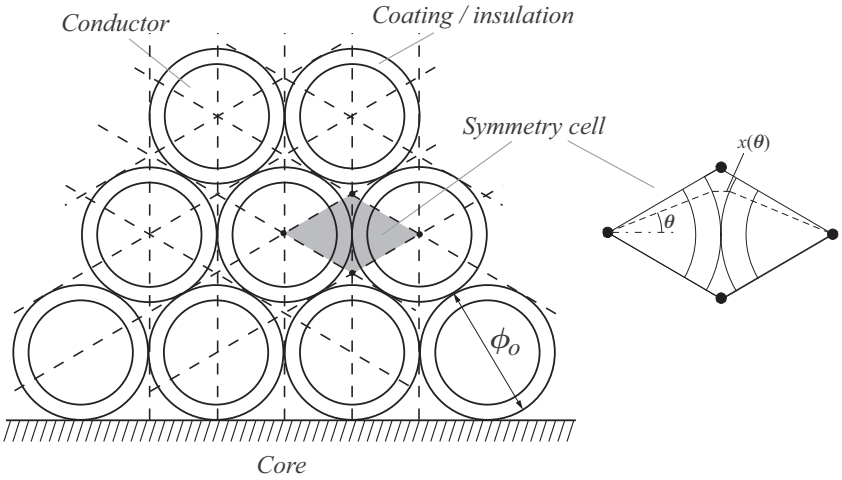


Figure 4.19: Cross-section of a multi-layer winding and symmetry cell used for the parasitic capacitance calculation.

filter at high frequencies. This effect gets worst if multiple winding layers are used in the construction of the inductor [24, 166, 167] and, as a result, inductor designs shall be limited to one or at most two layers, thus reducing available window area occupation and increasing the required total core material volume. If a planar design is used the capacitive effect is even more pronounced due to the wider conductive area in contrast with thinner dielectric distances between layers [168].

A complete modeling procedure for the calculation of the values of parasitic capacitances is presented in [166, 169], from where the main considerations are listed in the following.

The cross-section of a multi-layer winding is shown in Figure 4.19, where the symmetry lines are drawn, which are used in the calculation of the parasitic capacitance. A symmetry cell is also shown, where the simplified electric field lines are defined.

Two capacitances in series are to be considered, one of the coating of the conductors and the other from the air gap between wires. The elementary capacitance from the coating is,

$$dC = \frac{\epsilon_r \epsilon_o \phi_w}{2dr} d\theta dl, \tag{4.58}$$

and the integration of this capacitance leads to the capacitance per unit angle due to the wire coating in the symmetry cell,

$$\frac{dC_{ttc}}{d\theta} = \frac{\epsilon_r \epsilon_o l_t}{\ln\left(\frac{\phi_o}{\phi_w}\right)}, \tag{4.59}$$

For the air gap the elementary capacitance per unit angle is given by,

$$\frac{dC_g}{d\theta} = \frac{\epsilon_o l_t}{2\left(1 - \cos\theta\right)}. \tag{4.60}$$

The total capacitance for the cell is,

$$\frac{dC_{eq}}{d\theta} = \frac{dC_{ttc} dC_g}{dC_{ttc} + 2dC_g}. \tag{4.61}$$

Integrating eq. (4.61) for a angle of $\pi/6$ leads to the total turn-to-turn capacitance,

$$C_{tt} = \epsilon_o l_t \cdot \frac{2\epsilon_r \arctan\frac{(\sqrt{3}-1)\left(2\epsilon_r + \ln\frac{\phi_o}{\phi_w}\right)}{(\sqrt{3}+1)\sqrt{\left(2\epsilon_r + \ln\frac{\phi_o}{\phi_w}\right)\ln\left(\frac{\phi_o}{\phi_w}\right)}}}{\sqrt{2\epsilon_r \ln\frac{\phi_o}{\phi_w} + \left(\ln\frac{\phi_o}{\phi_w}\right)^2}}. \tag{4.62}$$

A simplified approach is proposed in [169], which leads to,

$$C_{tt} = \epsilon_o l_t \cdot \left[\frac{\epsilon_r \theta^*}{\ln\frac{\phi_o}{\phi_w}} + \cot\left(\frac{\theta^*}{2}\right) - \cot\left(\frac{\pi}{12}\right)\right], \tag{4.63}$$

with,

$$\theta^* = \arccos\left(1 - \frac{\ln\frac{\phi_o}{\phi_w}}{\epsilon_r}\right). \tag{4.64}$$

The turn-to-core capacitance is simplified to twice the value of the turn-to-turn capacitance, since the symmetry cell is approximately the

same. So that,

$$C_{tc} = 2C_{tt}. \tag{4.65}$$

The total parasitic parallel capacitance is the result of the capacitance network formed by the multiples C_{tt} and C_{tc}. For a single layer inductor, this network is shown in Figure 4.20. From where it is seen that if there is no core the capacitance is given by,

$$C_{p,air} = \frac{C_{tt}}{N_L - 1}. \tag{4.66}$$

If a conductive core is assumed, then the total parallel capacitance can be calculated by the following procedure.

For a two turns inductor,

$$C_{p,2} = 2C_{tt}. \tag{4.67}$$

For a three turns inductor,

$$C_{p,3} = \frac{3}{2}C_{tt}. \tag{4.68}$$

For a larger number of turns it follows that,

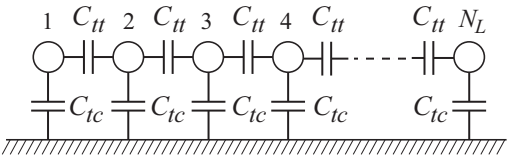


Figure 4.20: Capacitance network for a single layer inductor.

$$\begin{aligned} &\text{while } i \leq N_L \text{ do} \\ &\qquad C_{p,i} = \frac{C_{tt}}{2 + \frac{C_{tt}}{C_{p,i-2}}} + C_{tt} \\ &\qquad i = i + 1 \\ &\text{end while .} \end{aligned} \tag{4.69}$$

This sequence converges to $C_{p,N_L} \cong 1.366 C_{tt}$ for $N_L \geq 10$.

For an air core two layer inductor, assuming that the second layer has one turn less than the first and that it is winded in the opposite direction, it follows that,

$$C_{p,N_L} = 1.618 C_{tt} \text{ for } N_L \geq 10. \tag{4.70}$$

For a two layer inductor with a conductive core, assuming that the second layer has one turn less than the first and that it is winded in the opposite direction, the total parallel capacitance can be obtained with,

$$C_{p,N_L} = 1.830 C_{tt} \text{ for } N_L \geq 10. \tag{4.71}$$

For a three layers air core inductor, it is more difficult to calculate the total capacitance. However, according to [166,169] it is reduced and given by,

$$C_{p,N_L} = 0.573 C_{tt} \text{ for } N_L \geq 10. \tag{4.72}$$

The above result is somewhat controversial and seems to be based on the theoretical assumption that the inter-winding capacitances cancel each other.

The prediction achieved with the previous equations typically leads to an over-estimated capacitance, since the electric field lines assumed in the calculation are, in average, longer than the actual ones. Besides that, for toroidal cores, the wires are very close to each other in the center window, but as the outer edge of the core approaches, they spread. Thus, increasing the effective insulation distance and decreasing the turn-to-turn capacitance.

4.4.4 DM Inductor Equivalent Circuit

Based on the previously described impedances, an equivalent circuit model for a DM filter inductor can be formed. This model shall be valid for a wide frequency range and precisely describes the impedance of this type of component. A general equivalent circuit is shown in Figure 4.21, where the self-inductance and the resistance that accounts for the core losses are current and frequency dependent, while the wire resistance varies with frequency only. The parallel capacitance is approximately constant and depends basically on the geometry.

Simpler models can be used if the frequency range of interest is reduced. For instance, if the permeability of the core material is approximately constant in the frequency range of interest and core losses are expected to be small, then a constant inductance can be assumed instead.

The presented model has the limitation of not taking external couplings (magnetic and/or capacitive) into account.

In order to present the achievable results from the modeling, a comparison between models and measurements is performed for two different core materials and sizes in the following, where impedance and inductance measurements are performed with a precision impedance analyzer of model Agilent 4294A.

Applying the model from Figure 4.21 to the inductor specified in Table 4.5 generates the impedance curve presented in Figure 4.22.

It is observed a good agreement between measurement and model. A small mismatch between the self-resonance frequencies is seen, coming from uncertainties in the material's permeability and/or of the parallel capacitance calculation. The permeability published in the data sheet [162]

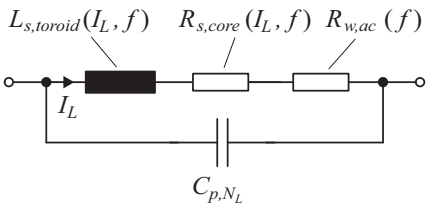


Figure 4.21: Equivalent circuit for a DM filter inductor with frequency and current dependent parameters.

Table 4.5: Specifications of inductor **01**.

Inductor number	**01**
Core	T157-52
Material	-52
Manufacturer	Micrometals
Number of turns	44
Wire diameter	1.6 mm
Core outer diameter	17.3 mm
Core inner diameter	9.65 mm
Core height	6.35 mm

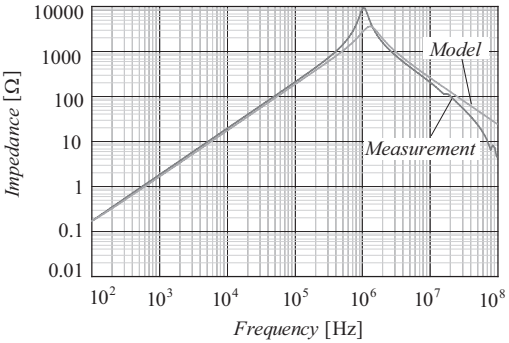


Figure 4.22: Comparison of the impedance of the modeled inductor **01** with a measurement result.

of the material -52 is used. The resistance at the resonance peak is also different, indicating that the series resistance is smaller in the measurement results. This does not turn to be a problem since the modeled impedance is smaller than the measured one, thus, being conservative for a filter design. The resonances observed at frequencies higher than 10 MHz can not be modeled with the presented equivalent circuit. For that, a complete 3-D model of the inductor would be required and the modeling effort would become much higher. For the typical switching frequencies of three-phase PWM converters, which range from 1 kHz up to some hundreds of kHz, the models here presented should suffice.

A second inductor, as specified in Table 4.6, is used to evaluate the limitations of the presented models. The impedance measurement curves for this inductor are depicted in Figure 4.23.

Good matching is observed in the curves of Figure 4.23 for frequencies below the resonance frequency. At a frequency approximately one decade lower than the self-resonance frequency, a larger value of impedances is observed in the measured inductor. This is not only due to the resonance itself, but the inductance of the measured component is higher than the inductance predicted in the model. From this observation, the magnetic

Table 4.6: Specifications of inductor **02**.

Inductor number	**02**
Core	55378-A2
Material	High Flux
Manufacturer	Magnetics
Number of turns	18
Wire diameter	0.95 mm
Core outer diameter	17.3 mm
Core inner diameter	9.65 mm
Core height	6.35 mm

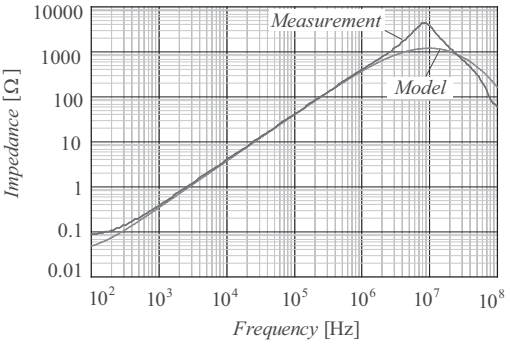


Figure 4.23: Comparison of the impedance of the modeled inductor **02** with a measurement result.

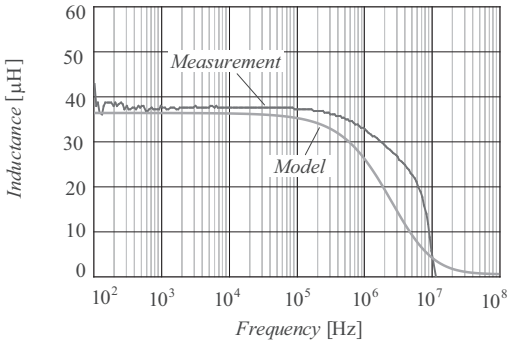


Figure 4.24: Comparison of the inductance of the modeled inductor **02** with a measurement result.

permeability curves for the material High Flux [163] seems to present lower values for high frequencies than the ones observed in the measurement. To certify that this happens, a comparison of the modeled and measured inductance for the same inductor is presented in Figure 4.24. From the inductance values it is seen that the inductance calculated with the permeability curves given in the data-sheet for material High Flux decreases earlier than expected. This highlights the importance of the input data for the model.

4.4.5 Thermal Models for Toroidal Cores

The temperature rise due to the inherent losses of a filter inductor is a major parameter when defining the core to use in a given application since magnetic and insulation materials present temperature limitations. Core materials present dependency of their characteristics with temperature. Aiming for the smallest size, consequently cheaper cores, forces a filter designer to search for the most precise thermal models.

Core manufacturers Magnetics Inc. [163] and Micrometals Inc. [162] and specialized literature [170] suggest that the expression,

$$\Delta T = \left(\frac{P_L\,[\mathrm{mW}]}{S_L\,[\mathrm{cm}^2]} \right)^{0.833}, \tag{4.73}$$

where P_L is the total inductor losses and S_L is the wounded inductor surface, provides a good approximation to the temperature rise ΔT in a core. This is a very difficult calculation since the exact calculation of the outer surface of an inductor might prove to be a challenge. The assumption for this expression is that the inductor presents a 40 % filling factor and is typically mounted on a printed circuit board. Thus, this is a special case of heat transfer based on typical boundary conditions.

The classical expression for the thermal resistance R_{th} of a body of surface S_L is given by,

$$R_{th} = \frac{1}{h_{film}\, S_L}, \tag{4.74}$$

where the film coefficient h_{film} is strongly dependent on the boundary conditions, i.e. in parameters like material characteristics, temperature, surrounding media, surface finish, distance to other bodies and air or fluid speed. The film coefficient can easily vary by orders of magnitude depending on air speed and distance to other bodies.

A more model based on eq. (4.74) is proposed in [171], where the thermal resistance R_{th} of a core is calculated with,

$$R_{th} = \frac{\Delta T}{P_L} = \frac{K_{th}}{Vol^{2/3}}, \tag{4.75}$$

where instead of the outer surface, the volume Vol of the inductor is used and a coefficient K_{th} depends on the geometry of the core and on the film coefficient for convection. Coefficient K_{th} is fairly constant for a given core family if the dimensions of the cores are proportional and the same type of convection (natural or forced air) is applied. This coefficient can be calculated with the expression,

$$K_{th} = \frac{Vol^{2/3}}{h_{film} S_L}, \tag{4.76}$$

where h_{film} is the film coefficient for the given material and convection, which typically varies from 10 W/m^2 to 25 W/m^2 for natural convection [171] and core surface temperatures around 80°C.

This method [171] shows that it is possible to relate the thermal resistance of an inductor to its volume. However, during the design phase of an inductor, the product of areas $A_e A_w$ is a more useful parameter than

the volume and a relation between product of areas and volume does exist. Therefore it should be possible to define the thermal resistance of an inductor by its product of areas.

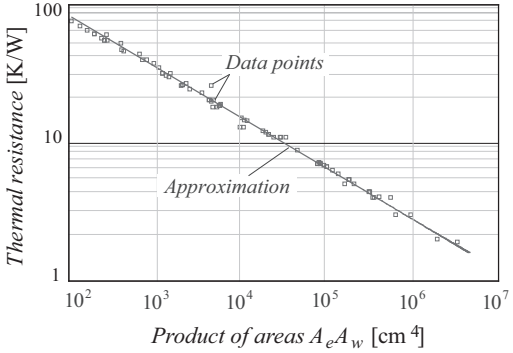


Figure 4.25: Thermal resistance of toroidal cores from different manufacturers [162, 163, 172, 173] as presented in their catalogs and proposed approximation.

In order to have a practical approach to define the thermal resistance, different toroidal core manufacturers [162, 163, 172, 173], which provide measured thermal resistances of their cores, have been researched. The result is shown in the graph of Figure 4.25, where the thermal resistance of cores from different manufacturers is plotted against the core product of areas. An exponential tendency of the data points is observed, which can be approximated by minimum squares regression to,

$$R_{th} \cong 415.17(A_e A_w \ [\text{cm}^4])^{-0.3593} \quad [\text{K/W}], \tag{4.77}$$

leading to a R-squared factor [1] of $R^2 = 0.9979$.

The model obtained with eq. (4.77) is only valid for toroidal cores typically mounted on printed circuit boards, and has the advantage of being a good approximation for the measured thermal resistance of many different cores and core manufacturers.

[1] In statistics, the coefficient of determination, R^2, is the proportion of variability in a data set that is accounted for by a statistical model. For least squares regression with a constant and linear model, R^2 equals the square of the correlation coefficient between the observed and predicted data values.

4.5 The Three-Phase CM Inductor

Due to maximum earth leakage current values imposed by safety requirements (cf. section 2.2.1), the value of capacitors that can be connected from the AC power lines to protective earth is limited. In practice, the value of such capacitors is in the nF range. In a filter which is composed of inductors and capacitors, this limitation implies that the value of the inductors should be made larger in order to compensate for the small capacitors. If separated inductors are used at each line, the same characteristics as for DM inductors apply. This means that a large peak flux density is expected, produced by the large values of the DM currents, and low permeability materials would be needed. These requirements would lead to extremely bulky inductors.

In order to prevent the large flux density generated by DM currents, engineers have been employing CM chokes since the early days of radio engineering [174, 175]. Nevertheless, it was not until 1966 that this component received the name "Common Mode Choke" [176] in the literature. In 1970, a mathematical model [175] has been presented for a two-line inductor. In 1971, a three-phase version of the CM choke has been presented [177] along with the main advantages of this type of construction for suppressing CM noise currents.

In order to avoid the saturation of a core, the same condition as presented for a DM inductor has to be respected. That is,

$$H = \frac{N_L I_L}{l_e} < \frac{B_{sat}}{\mu_o \mu_r}, \tag{4.78}$$

from where it is seen that if the magnetic field in core should be kept small.

Three ways to reduce the magnetic field in a core are possible, namely:

i. reduce the number of turns of the windings;

ii. reduce the current, and;

iii. construct the windings in a way that the fields created by each of them is opposed to the fields of the others, so that the net field is reduced.

The third possibility is explored in a three-phase CM choke constructed as illustrated in Figure 4.26.

The operating principle of a three-phase CM inductor can be understood by examining Figure 4.27. It is seen that for a CM current i_{cm} the magnetic fields generated in each of the windings ($\vec{H}_{A,cm}$, $\vec{H}_{B,cm}$ and $\vec{H}_{C,cm}$) are all on the same direction and the total net field is the scalar sum of each individual one. On the other hand, for DM currents $i_{A,dm}$, $i_{B,dm}$ and $i_{C,dm}$ where,

$$i_{A,dm} + i_{B,dm} + i_{C,dm} = 0, \tag{4.79}$$

the net flux, assuming an infinite relative permeability of the core material and the same number of turns in the windings, is given by,

$$\frac{N_L i_{A,dm}}{l_e} + \frac{N_L i_{B,dm}}{l_e} + \frac{N_L i_{C,dm}}{l_e} = \frac{N_L (i_{A,dm} + i_{B,dm} + i_{C,dm})}{l_e} = 0. \tag{4.80}$$

Is is seen that an ideal three-phase CM inductor is capable to completely eliminate the influence of the typically high DM currents. If a finite permeability is assumed, part of the magnetic field generated by the DM currents close through the surrounding media. This portion of the magnetic field is named *leakage field* and is responsible for an increase in the internal field of the inductor due to DM currents. Therefore, it needs to be taken into account when designing a CM choke.

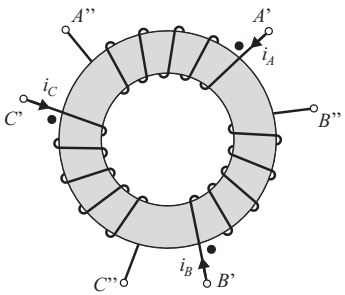


Figure 4.26: Illustration of a three-phase CM inductor.

The contributions of DM and CM fields are depicted in Figure 4.28 for the same currents as defined in Figure 4.27. It is seen that the CM generated field ($\vec{H}_{cm}$) is not significantly influenced by the non-ideal characteristic of the core material, whereas the fields due to DM currents ($\vec{H}_{A,cm}$, $\vec{H}_{B,cm}$ and $\vec{H}_{C,cm}$) do not completely cancel. Depending on the direction of the DM currents, the CM field can sum or subtract in different portions of the core.

From the CM currents shown in Figure 4.27, the magnetic field ($\vec{H}_{cm}$)

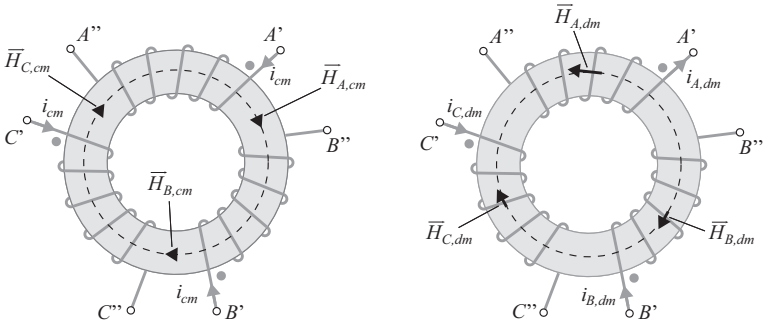


Figure 4.27: Currents and magnetic fields in an ideal three-phase CM inductor due to CM and DM currents.

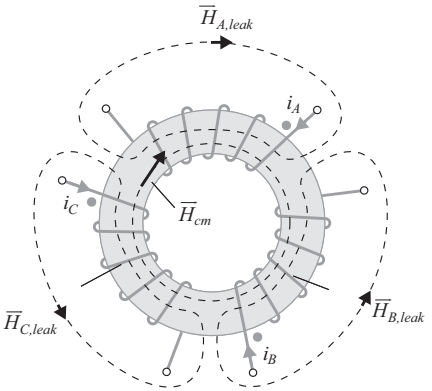


Figure 4.28: Currents and magnetic fields in a three-phase CM inductor with finite permeability.

and the magnetic flux density ($\vec{B}_{cm}$) present the distributions depicted in Figure 4.29. An exponential distribution is expected, where the space close to the inner conductors, which are more closely spaced present a higher field than the external side. The flux density is proportional to to the permeabilities and, thus, is much higher inside the core.

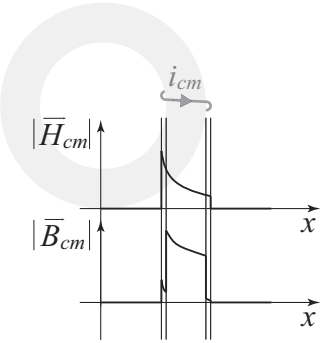


Figure 4.29: Distribution of magnetic field ($\vec{H}_{cm}$) and flux density ($\vec{B}_{cm}$) for common mode currents.

For the norm of the magnetic field, this distribution is shown with more detail in a 2-D finite element simulation result for a common mode current $I_{cm} = 1$ A in Figure 4.30. It is observed that the totality of the flux is constrained to the inner volume of the inductor. Thus, no external flux is expected to be radiated from CM currents in a CM inductor built in a toroidal core. This represents two main advantages, namely: magnetic couplings to external components are not an issue, and; radiated emissions are not relevant. This holds truth as long as the geometric symmetry of the component is preserved.

For DM currents, the norm of the magnetic field vector is presented with results of a 2-D finite element simulation preformed with instantaneous asymmetrical currents of values +2 A, -1 A and -1 A in Figure 4.31. It is observed that the field is asymmetrical, where it is high in the space between the windings with higher current difference. Unlike for the CM field, the external DM field is not ideally null. Besides that, the spatial configuration of the DM field continuously changes with time for sinusoidal currents. This allows for the external magnetic coupling with other components and generates radiated emissions. Nevertheless, the leakage

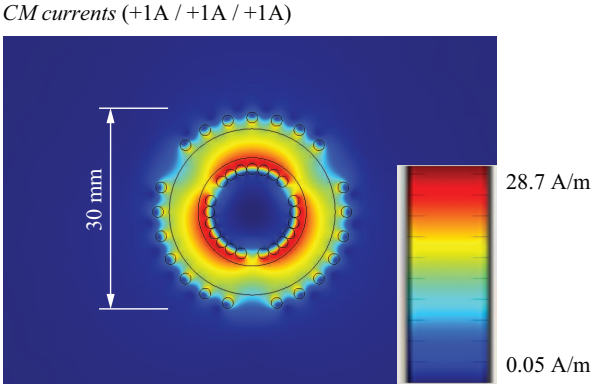


Figure 4.30: Finite elements simulation result for a three-phase CM inductor conducting three symmetrical currents. The simulation is in time domain and shows the norm of the magnetic field due to three currents of equal phase and amplitude produced in the shown windings.

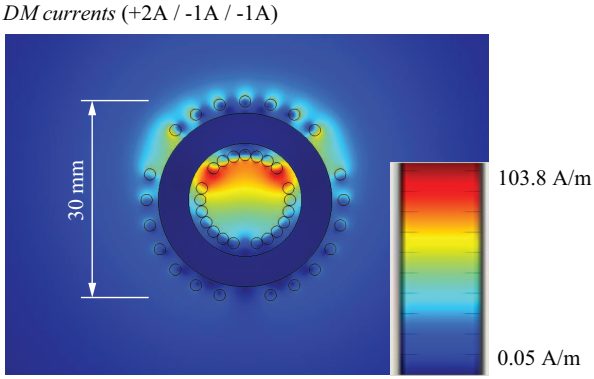


Figure 4.31: Finite elements simulation results (norm of the magnetic field) for DM currents. The simulation is in time domain and shows the norm of the magnetic field due to one current of +2 A in the uppermost winding and two currents of -1 A in the other two windings.

flux produces an inductance which is seen by DM currents. This inductance is used to filter DM noise currents [178].

The construction of a typical three-phase CM inductor is illustrated in

Figure 4.32. This construction has the advantages of using toroidal cores: lower core costs, small leakage flux and low thermal resistance. It is seen that the windings are physically spaced in order to achieve insulation, since line voltages are across them. With this measure it is possible to use magnetic wire with standard coating, reducing thermal resistance and costs if compared with high voltage insulated wires. The disadvantage of this arrangement is that the leakage flux arising from DM currents is higher than if the windings would be done close to each other.

The circuit schematics for a purely inductive and symmetrically built three-phase CM inductor is depicted in Figure 4.33. Three mutually coupled inductors reproduce the behavior previously explained from a circuit theory perspective.

From the schematic of Figure 4.33 and considering that,

$$L_A = L_B = L_C = L_{choke}, \tag{4.81}$$

it follows that,

$$\begin{bmatrix} u_A \\ u_B \\ u_C \end{bmatrix} = \begin{bmatrix} L_{choke} & M & M \\ M & L_{choke} & M \\ M & M & L_{choke} \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix}. \tag{4.82}$$

The mutual inductance is defined by,

$$M = k_{cm} \cdot L_{choke}. \tag{4.83}$$

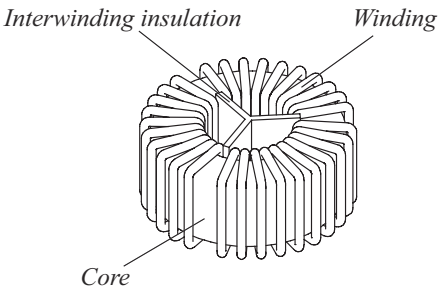


Figure 4.32: Construction of a three-phase CM inductor.

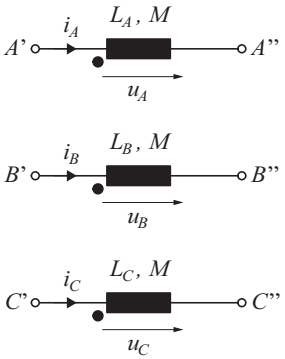


Figure 4.33: Schematic of a purely inductive three-phase CM inductor.

With these definitions, two inductances can be evaluated. The CM inductance is acting for three symmetrical currents,

$$i_A = i_B = i_C = i_{cm}, \tag{4.84}$$

thus,

$$u_A = u_B = u_C = u_{cm}, \tag{4.85}$$

and a CM inductance L_{cm} is defined as,

$$L_{cm} = \frac{u_{cm}}{di_{cm}/dt} = L_{choke} + M + M, \tag{4.86}$$

thus,

$$L_{cm} = L_{choke}\frac{1 + 2k_{cm}}{3}. \tag{4.87}$$

According to eq. (4.87) the CM inductance equals the self-inductance of a winding if a perfect coupling, that means $k_{cm} = 1$, is considered.

If three DM currents are considered,

$$i_{A,dm} + i_{B,dm} + i_{C,dm} = 0 \tag{4.88}$$

$$u_{A,dm} + u_{B,dm} + u_{C,dm} = 0, \tag{4.89}$$

it follows that,

$$\begin{bmatrix} u_{A,dm} \\ u_{B,dm} \\ u_{C,dm} \end{bmatrix} = \begin{bmatrix} L_{choke} - M & 0 & 0 \\ 0 & L_{choke} - M & 0 \\ 0 & 0 & L_{choke} - M \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_{A,dm} \\ i_{B,dm} \\ i_{C,dm} \end{bmatrix}. \tag{4.90}$$

Defining a DM inductance as the leakage inductance L_σ,

$$L_\sigma = \frac{u_{i,dm}}{di_{i,dm}/dt} = L_{choke} - M\,, \quad \text{with}\, i = A, B, C, \tag{4.91}$$

it follows that,

$$L_\sigma = L_{choke} \cdot (1 - k_{cm}). \tag{4.92}$$

If a coupling $k_{cm} = 1$ is considered, the leakage inductance given by eq. (4.92) is null. The effects of the DM inductances are not simple to model in a complete filter because of the external couplings with other components. The utilization of the DM inductances for filtering of differential mode currents might be very useful, but it should be carefully studied so that radiated emissions and deterioration of filtering performance due to external couplings do not decrease filtering performance.

From the previous analysis, the model of a CM inductor can be divided into two parts, one for symmetrical and the other for asymmetrical currents. This provides useful simplification for the following analysis.

4.5.1 Common Mode Inductance

The three-phase CM inductor can be seen as three windings in parallel and wound in the same direction for common mode currents. Therefore, as for a DM inductor, the self-inductance provided by the geometrical arrangement of the windings around a ferromagnetic core can be computed with the real part of the complex permeability μ'. However, unlike the

DM inductors, the dependency of the permeability on the CM currents is typically very small. Furthermore, the expected CM currents present low amplitudes, so that the variation of magnetic flux in the core does not create large variations in the core's permeability. For these reasons, the CM inductance is defined as,

$$L_{CM}(f) = A_L N_L^2 \cdot \frac{\mu'(f)}{\mu'(f = 0\text{Hz})}. \tag{4.93}$$

In order to profit from the low flux densities generated by CM currents, high permeability materials can be employed, so that cores with very large A_L values can be used. Thus, a low number of turns and small dimensions can be presumably achieved. Core magnetic materials for CM inductors also present a non-constant complex permeability with frequency. The proper choice of core materials leads to compact and effective inductors, with reduced parasitics.

The real part of the series complex permeability for some popular and high performance magnetic materials are shown in Figure 4.34. Two types of ferrite – N30 and T38 – [179], a nanocrystalline – VITROPERM 500F – [172, 173] and an amorphous material – MAGNAPERM – [180] are compared. It is observed that the real part of the permeability of all materials is similar in the 0.2 to 2 MHz range, but the non-ferrite materials present higher permeabilities for other frequencies.

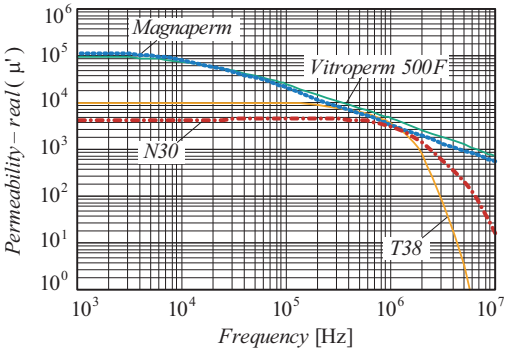


Figure 4.34: Magnitude of the real part of the relative complex permeability versus frequency of core materials for CM inductors [172, 173, 179, 180].

4.5.2 Losses and Associated Resistances

The imaginary part μ'' of the complex permeability models the small signal losses of the materials. For high permeability materials, these losses are typically higher than for the materials employed in DM inductors. The effect of the increased losses is that the total series impedance of the CM inductor is increased with a resistive part. The inductor behaves as a series RL connection, where the R part is considerable for high frequencies. Core manufacturers usually provide measurement based curves defining the imaginary part of the permeability as a function of frequency. Figure 4.35 shows the imaginary part of the permeability for the previously mentioned materials. It is seen that the imaginary part is lower for ferrites.

If flux densities that can be treated as small signal perturbations are to be expected, the ac resistance can be calculated with eq. (4.35). Thus,

$$R_{CM,core} = A_L N_L^2 \omega \cdot \frac{\mu''}{\mu''(f = 0\,\mathrm{Hz})} \tag{4.94}$$

The large signal core losses for the presented materials are shown in Figure 4.36 [172,173,179,180]. It is observed that these losses are higher for the ferrites.

From the large signal core losses, resistance can be used to model the core losse . From eq. (4.41), it follows that,

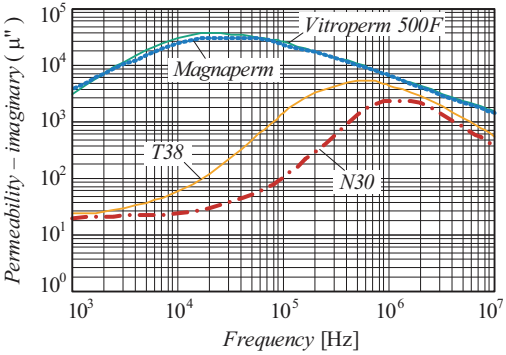


Figure 4.35: Magnitude of the imaginary part of the relative complex permeability versus frequency of core materials for CM inductors [172, 173, 179, 180].

$$R_{CM,core} = 2V_c K_c f^{\alpha} I_p^{\beta-2} \left(\frac{A_L N_L \mu'}{A_e \left| \bar{\mu}_{s,initial} \right|} \right)^{\beta}. \tag{4.95}$$

In order to compare the equivalent series resistance arising from core losses, the material VITROPERM 500 F is chosen. Three resistances are calculated, one based on eq. (4.94) taking only the imaginary part of the permeability into account and two based on eq. (4.95), considering core losses for a current of 10 mA and of 10 A. These resistances are plotted in Figure 4.37. The Steinmetz parameters for these plots are obtained from minimum squares regression of data points in the frequency range of 10 kHz up to 300 kHz. This explains why the resistance calculated with a current of 10 mA approaches the one calculated with the permeability in this frequency range. Furthermore, it is seen that an increase in this resistance is expected for higher currents. For the design of CM chokes it is sufficient to calculate the resistance with the complex permeability, since higher currents lead to higher resistances and, thus, higher attenuation of CM currents.

Core losses are usually not considered when designing CM chokes, unless very high switching frequencies are employed. Another exception is in the design of CM inductors to be placed between three-phase inverters and motors, where very large CM voltages are expected.

The losses in the wires can be calculated in the same way as for DM

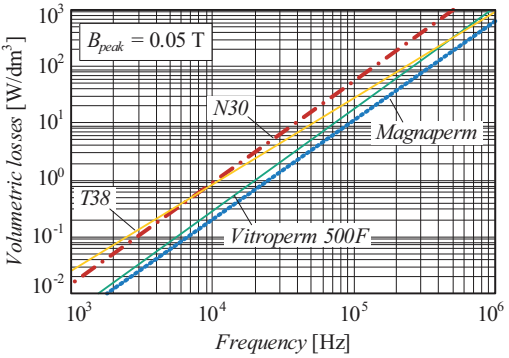


Figure 4.36: Core losses as a function of frequency and flux density of core materials for CM inductors [172, 173, 179, 180].

inductors. Thus the resistances for each of the windings can be evaluated with the same equations presented in section 4.4.2.

Material Selection for CM Inductors

The saturation flux density for the cited materials are $B_{sat,VITROPERM} = 1.2$ T, $B_{sat,MAGNAPERM} = 0.57$ T, while it is lower than 0.3 T for the ferrites. Regarding the maximum temperature for continuous operation, we have 120 °C for VITROPERM, 90 °C for MAGNAPERM and 100 °C for the ferrites.

Comparing the characteristics of the materials shown in Figure 4.34, Figure 4.35 it is observed that the highest permeability material is VITROPERM 500 F. According to Figure 4.36, core losses for MAGNAPERM are the smallest, while are higher for the ferrites.

The choice of material aiming for the smallest volume core is a complex dependency on different parameters, like temperature, currents, impedance and frequency of operation. Perhaps the most important parameter is the saturation of the core. The following analysis proposes a method to evaluate the material which leads to the smallest core dimensions.

The saturation of the core must be avoided, thus,

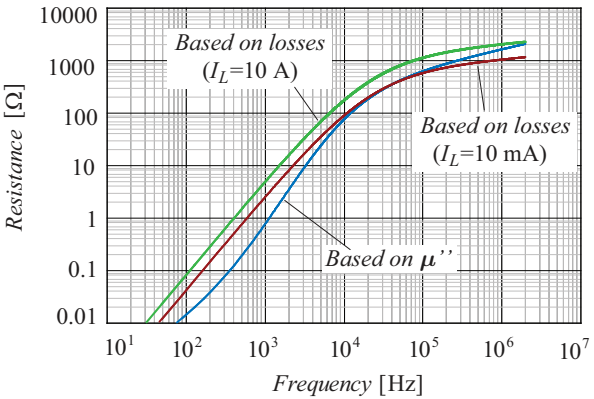


Figure 4.37: Comparison of the series resistance due to core losses for material VITROPERM 500 F, core T6000-6-L2025-W380 and windings of 7 turns.

$$N_L I_{L,max} < \frac{l_e B_{sat}}{\mu_o \mu_r}. \tag{4.96}$$

The impedance of a toroid is,

$$X_{L,toroid} = 2\pi f L_{s,toroid} = \mu_o \mu_r f N_L^2 H_c \cdot \ln\left(\frac{OD}{ID}\right), \tag{4.97}$$

from where the minimum number of turns for a given impedance and geometry is,

$$N_L = \sqrt{\frac{1}{\mu_r}} \underbrace{\sqrt{\frac{X_{L,toroid}}{\mu_o f H_c \cdot \ln\left(\frac{OD}{ID}\right)}}}_{K_1}. \tag{4.98}$$

Replacing eq. (4.98) in eq. (4.96) leads to,

$$\frac{1}{\sqrt{\mu_r}} K_1 I_{L,max} < \frac{l_e B_{sat}}{\mu_o \mu_r}. \tag{4.99}$$

Simplifying eq. (4.99) leads to,

$$\underbrace{\frac{K_1 I_{L,max} \mu_o}{l_e}}_{K_2} < \frac{B_{sat}}{\sqrt{\mu_r}}, \tag{4.100}$$

where K_2 is a constant if a fixed frequency, geometry, current and required impedance are assumed.

From eq. (4.100) it is seen that, for a fixed geometry and required impedance, the saturation condition for a CM inductor depends on the relation between two properties of the magnetic material, namely its saturation flux density and the relative permeability. In Table 4.7, this relation is calculated for the mentioned materials and given for two different frequencies. It is observed that, even though material VITROPERM 500 F presents a very high permeability, the ratio $B_{sat}/\sqrt{\mu_r}$ is the most favorable also for low frequencies. This shows that this material is supposed to allow for the smallest core size and/or number of turns for given required

impedance and CM current.

Table 4.7: Ratio $B_{sat}/\sqrt{\mu_r}$ for materials employed in CM inductors.

Material	*Ratio* $\frac{B_{sat}}{\sqrt{\mu_r}}$ @ 1 kHz	*Ratio* $\frac{B_{sat}}{\sqrt{\mu_r}}$ @ 200 kHz
N30	3.7 mT	3.5 mT
T38	2.6 mT	2.7 mT
VITROPERM 500 F	3.8 mT	7.8 mT
MAGNAPERM	1.8 mT	3.9 mT

If the most important parameter for a CM is its total volume, material VITROPERM 500 F shall be chosen . This material presents good thermal stability as well. The disadvantage is its price, which is higher than for the ferrites. If only high frequency components ($>$ 150 kHz) are present, the second best material from a volume point of view is MAGNAPERM. For large CM currents for lower frequencies the use of ferrite cores could lead to similar volumes as for VITROPERM 500 F.

4.5.3 Parasitic Parallel Capacitance

The calculation of the winding parasitic parallel capacitance for a three-phase CM inductor can be done with the same procedure present for the DM inductors. If the inter-winding capacitance can be neglected, the final parallel capacitance for CM currents is the parallel connection of the capacitances of the three windings. This is typically the case, since the windings are placed away from each other.

4.5.4 Leakage Inductance and its Saturation Issues

A prediction of the leakage inductance value is done in [178] for single-phase CM inductors. This analysis can be directly applied to three-phase inductors since the same principles apply.

Given the symmetries for the DM components shown in Figure 4.28, each of the windings can be simplified to an equivalent winding on a portion of the toroidal core. With this simplification, the inductance for an air coil is calculated by,

$$L_{air} = \mu_o N_L^2 \frac{A_e}{l_{eff}}, \tag{4.101}$$

where l_{eff} is the effective mean path length of the leakage magnetic field.

The effective mean path length of the leakage magnetic field has two portions, inside and outside the core, so that a closed path for the field lines is found. In order to simplify the analysis, the path shown in Figure 4.38 is used. From where, it follows that the mean path length is empirically defined as,

$$l_{eff} = \sqrt{\frac{1}{\sqrt{2}}\left[OD\left(\frac{\theta}{4} + 1 + \sin\frac{\theta}{2}\right)\right]^2 + \left[ID\left(\frac{\theta}{4} - 1 + \sin\frac{\theta}{2}\right)\right]^2}. \tag{4.102}$$

The equation empirically derived in [178] gives,

$$l_{eff,Nave} = l_e \sqrt{\frac{\theta}{2\pi} + \frac{1}{\pi}\sin\frac{\theta}{2}}, \tag{4.103}$$

which is valid for $\theta > \pi/6$.

Comparing eq. (4.102) and eq. (4.103) leads to the plots of Figure 4.39 for a core of dimensions $OD = 50$ mm and $ID = 35$ mm. It is seen that for angles larger than $\pi/4$ both equations present very similar results. The relative difference on these curves is observed for cores with other

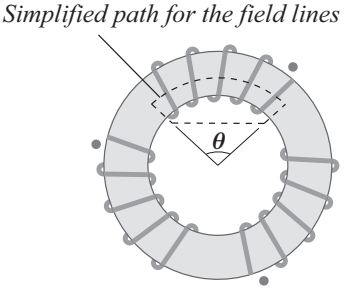


Figure 4.38: Simplified magnetic field path for the calculation of leakage inductances in a three-phase CM inductor.

dimensions as well.

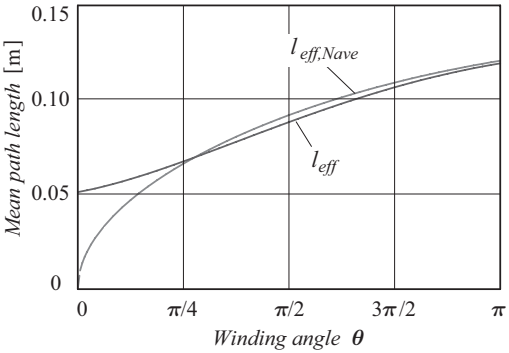


Figure 4.39: Comparison of the results of eq. (4.102) and eq. (4.103) for a core with dimensions $OD = 50$ mm and $ID = 35$ mm.

In order to model the effective permeability μ_{eff}, the winding is modeled as a wire wounded on a rod core. The effective permeability of a rod is a function of the core permeability, the rod length and the rod cross-sectional area. It can be approached for high permeability cores, with good accuracy [178], as,

$$\mu_{eff} = 2.5\Gamma^{1.45}, \tag{4.104}$$

where Γ is the ratio from the rod length to the rod diameter. And, for the case of a toroidal core with square cross-section, it is approximated as,

$$\Gamma = \frac{l_e}{2}\sqrt{\frac{\pi}{A_e}}. \tag{4.105}$$

The final value for the leakage inductance is calculated with,

$$L_\sigma = \mu_{eff} L_{air} = \mu_o \mu_{eff} N_L^2 \frac{A_e}{l_{eff}}. \tag{4.106}$$

In order to calculate the flux density in the core, the magnetic field can be evaluated with,

$$H_\sigma = \frac{N_L I_{dm}}{l_{eff}}, \tag{4.107}$$

from where,

$$B_\sigma = \mu_{eff} H_\sigma = \mu_{eff} \frac{N_L I_{dm}}{l_{eff}}. \tag{4.108}$$

Isolating the magnetic path length in eq. (4.106) and replacing it in eq. (4.108) gives,

$$B_{sigma} = \frac{L_\sigma I_{dm}}{N_L A_e}. \tag{4.109}$$

The condition for non-saturation of the core due to DM currents generated leakage flux is,

$$\frac{L_\sigma I_{dm}}{N_L A_e} < B_{sat}. \tag{4.110}$$

According to eq. (4.110) the calculation of the leakage flux density can be done with the previously estimated leakage inductance. With this, the saturation of a core can be avoided already in the design phase of the component. In [178] it is also suggested that the value of the leakage inductance can be optimized for a given DM current, so that the achieved leakage impedance helps filtering DM emissions.

4.5.5 Three-Phase CM Inductor Equivalent Circuits

The three-phase CM inductor can be modeled with two equivalent circuits, one for CM and the other for DM currents. The advantage of doing this is that the design of DM and CM can be performed separately. Thus, simpler models can be employed.

For common mode currents, assuming that the three windings are symmetrical and the core permeability is homogeneous, the impedance of the three windings are balanced and in parallel. Thus, the model for CM depicted in Figure 4.40 is a good approximation for a wide frequency range. As the magnetic field generated by the currents in all windings sums, a single inductor with the same number of turns of a single winding

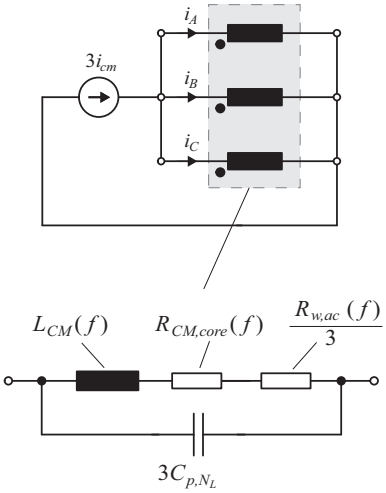


Figure 4.40: Equivalent circuits for CM of a three-phase CM inductor.

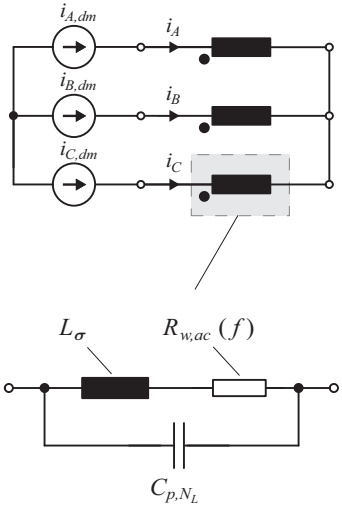


Figure 4.41: Equivalent circuits for DM of a three-phase CM inductor.

models accurately the self-inductance and core losses based resistance. The CM inductance and the resistance due to core losses are mainly dependent on the frequency, but if high flux density is expected due to high currents or large leakage flux, the permeability decreases with the associated currents. The resistance of the windings are acting in parallel, as well as the parasitic capacitances of the windings.

Differential mode currents generate leakage flux, which is not appreciably affected by the permeability of the core due to the effective magnetic path length being closed through the air. Thus, the leakage inductance is approximately constant with frequency and currents. The resistances due to losses in the wires are frequency dependent, but typically small for $f < 30$ MHz. As the leakage flux is typically small, the resistance due to core losses can be neglected. The final equivalent circuit for DM currents is shown in Figure 4.41.

In order to observe the achievable performance of the presented models, two three-phase CM inductors have been wound and the comparison from impedance measurements and the predicted models is presented in the following.

The construction specifications of the inductors are given in Table 4.8 and Table 4.9.

Table 4.8: Specifications of CM inductor **CM-01**.

Inductor number	**CM-01**
Core	T6000-6-L2025-W380
Material	VITROPERM 500 F
Manufacturer	VAC
Number of turns	10
Wire diameter	1.4 mm
Core outer diameter	27.8 mm
Core inner diameter	13.7 mm
Core height	12.7 mm

The CM impedance of inductor **CM-01** is shown in Figure 4.42 for a measurement obtained with an impedance analyzer in comparison with the impedance calculated by using the equivalent circuit of Figure 4.40.

For the CM impedance measurement, all three windings were connected in parallel. A very good correlation among the curves in the whole frequency range is given. The calculated parallel capacitance seems to be correct, since the very high frequency (>20 MHz) impedance is approximately the same. The difference in the resonance frequency is credited to differences in the permeability curves with respect to the real one. A slight difference is seen from around 30 kHz up to 500 kHz which is most probably due to differences between the complex permeability of the core and the one used in the calculations, which was curve fitted from data sheet [172]. In the impedance curves it is seen that, up to approximately 20 kHz the impedance increases at a rate of around +20 dB per decade, meaning that the core losses can be neglected in this range and that the real part of the permeability is approximately constant. From 20 kHz up to 6 MHz the impedance increases at around +10 dB per decade due to the increasing imaginary part of the permeability. This increase also shows that the real part is not very important at this frequency range. At 8 MHz the effect of the parallel capacitance starts to dominate the CM impedance, which starts to decrease at -20 dB per decade. Due to the high resistive part of the HF impedance, the resonance peak is highly damped. This is, generally, a good characteristic since strong resonances might impair the filtering performance. These curves show the importance of the correct modeling of the CM impedance of a CM inductor. If the complex permeability would be neglected, completely different curves would appear, misleading a filter design.

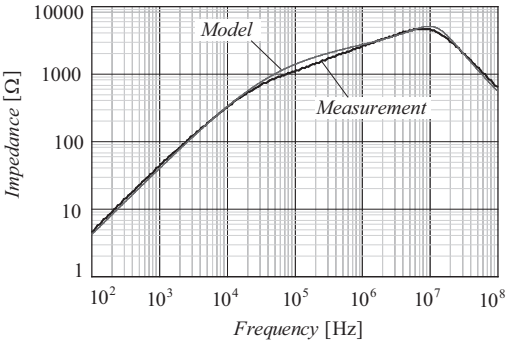


Figure 4.42: Common mode impedance curves from measurement and modeling for the inductor **CM-01**.

Table 4.9: Specifications of CM inductor **CM-02**.

Inductor number	**CM-02**
Core	B64290-L567 (2 stacked)
Material	N30
Manufacturer	EPCOS
Number of turns	8
Wire diameter	1.5 mm
Core outer diameter	30.5 mm
Core inner diameter	20.0 mm
Core height	12.5 mm (2×)

For the ferrite based inductor (**CM-02**), the impedance curves are shown in Figure 4.43. It is seen that the real part of the permeability dominates this design up to 1 MHz, and the influence of the losses is only observed at the resonance frequency. For this design, the permeability curves based model seems not to follow the impedance for frequencies higher than 1 MHz. The predicted parallel capacitance is close to the measured one, since the impedance curves for very HF are in good agreement. It is seen that CM inductors built with ferrite have a more reactive characteristic when compared to the nanocrystalline based one. The higher magnetic losses with frequency in the nanocrystalline materials might increase losses in the inductor, but it also means that the energy due to HF currents is dissipated in spite of being exchanged, leading to higher damping and resistive attenuation.

The leakage inductance of the three-phase CM inductors has been measured and is shown in Table 4.10. Errors smaller than 20% have been observed, which are considered low due to the involved simplifications. The larger inductor (**CM-02**) presents also the largest inductance even with a lower number of turns. For the measurement of the leakage inductances, two windings have been shorted, while the impedance across the terminals of the third winding has been measured. This leads to a simplified equivalent circuit where the leakage inductance of the measured winding is in series with the parallel connection of the other windings.

The previous comparison validates the presented modeling procedure for use in the design of CM inductors and filters.

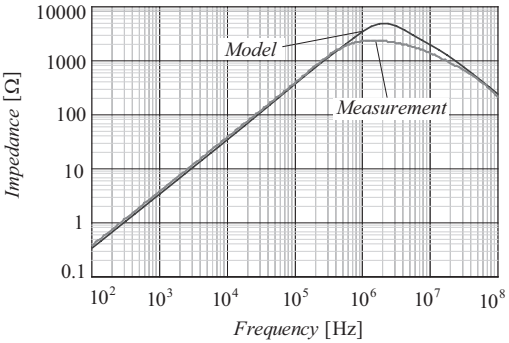


Figure 4.43: Common mode impedance curves from measurement and modeling for the inductor **CM-02**.

Table 4.10: Leakage inductances measured at 10 kHz.

Inductor number	Calculated L_σ	Measured L_σ	Relative error
CM-01	1.85 μH	1.75 μH	5.7%
CM-02	4.89 μH	4.27 μH	14.5%

4.6 Equivalence of Two-Port Networks for Parasitic Cancellation

In order to achieve simple networks, which are able to minimize the effect of parasitic elements in filter components, some networks including coupled inductors have been identified in the literature [167, 168, 181–185]. A careful analysis about these networks is able to provide helpful insight into the principles used in the parasitic cancellation techniques.

Electrical networks consisting of linear and time invariant elements are completely defined through one of their characteristic impedances (**Y**, **Z**, **T**, **h**, **s**, etc.) [186]. Therefore, if two networks present equal characteristic matrices, they are equivalent from an electrical point of view. At this section, characteristic impedance matrices **Z** are employed, allowing the study of equivalence among different networks, which are used as the basis for the cancellation of parasitic components.

A first equivalence of interest is among the networks shown in Figure 4.44, where a "T" and a "π" network are depicted. These are important building-blocks for power filters and specially interesting for studying the networks employed in parasitic cancellation techniques.

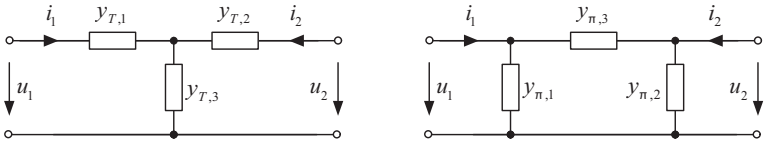


Figure 4.44: Equivalence among "T" and π networks.

The impedance matrices for the circuits of Figure 4.44 are given by:

$$\mathbf{Z}_T = \begin{bmatrix} \frac{y_{T,1}+y_{T,3}}{y_{T,1}y_{T,3}} & \frac{1}{y_{T,3}} \\ \frac{1}{y_{T,3}} & \frac{y_{T,1}+y_{T,3}}{y_{T,1}y_{T,3}} \end{bmatrix} \tag{4.111}$$

for the T-network.

And for the π-network by

$$\mathbf{Z}_\pi = \begin{bmatrix} \frac{y_{\pi,2}+y_{\pi,3}}{y_{\pi,1}y_{\pi,2}+y_{\pi,2}y_{\pi,3}+y_{\pi,3}y_{\pi,1}} & \frac{y_{\pi,3}}{y_{\pi,1}y_{\pi,2}+y_{\pi,2}y_{\pi,3}+y_{\pi,3}y_{\pi,1}} \\ \frac{y_{\pi,3}}{y_{\pi,1}y_{\pi,2}+y_{\pi,2}y_{\pi,3}+y_{\pi,3}y_{\pi,1}} & \frac{y_{\pi,1}+y_{\pi,3}}{y_{\pi,1}y_{\pi,2}+y_{\pi,2}y_{\pi,3}+y_{\pi,3}y_{\pi,1}} \end{bmatrix}. \tag{4.112}$$

If all elements of matrices $\mathbf{Z}_T$ and $\mathbf{Z}_\pi$ are the same, then the networks are equivalent.

Measuring Impedances with Parasitics Cancellation

The networks employed for canceling of parasitic elements convert the, formerly, two-terminal components to three-terminal devices. These three-terminal devices typically rely on magnetic coupling among different elements of the circuits. Therefore, a conventional impedance analyzer can not be used to directly measure such devices. Further limitation arises from the fact that the effects of parasitic cancellation techniques take place at high frequencies, where measurements are complex.

In order to avoid these limitations, network analyzers can be used to

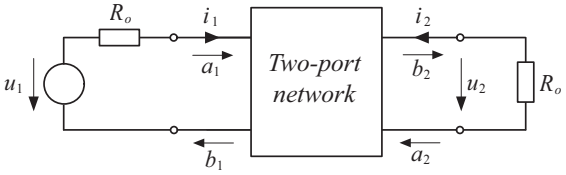


Figure 4.45: Mesurement setup for two-port networks in a network analyzer.

measure such impedances. Network analyzers measure the *S-parameters* for two-port devices. These parameters are defined in the following.

The basic measurement carried out in a Network Analyzer is shown in Figure 4.45. It is seen two currents (i_1 and i_2) and voltages (u_1 and u_2) and four waves (incident a_1, a_2 and reflected b_1, b_2).

The network analyzer measures the relation among the incident and reflected waves and converts them into variables named the S-parameters of the measured network. These parameters are defined as,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \tag{4.113}$$

and are simpler to measure than other parameters like impedances or admittances if high frequencies are involved. However, the measured parameters depend upon the source and load impedances (R_o) of the measurement setup. The voltages and currents are defined as,

$$u_1 = \sqrt{R_o} \cdot (a_1 + b_1) \tag{4.114}$$

$$u_2 = \sqrt{R_o} \cdot (a_2 + b_2) \tag{4.115}$$

$$i_1 = \frac{a_1 - b_1}{\sqrt{R_o}} \tag{4.116}$$

$$i_2 = \frac{a_2 - b_2}{\sqrt{R_o}}. \tag{4.117}$$

On the other hand, admittance and impedance matrices for a two-port network are independent from source and load impedances. The admittance matrix $\mathbf{Y}$ is the characteristic matrix for the system,

$$\begin{matrix} \mathbf{I} & = & \mathbf{Y} & \cdot & \mathbf{U} \end{matrix}$$
$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \cdot \begin{bmatrix} u_1 \\ u_2 \end{bmatrix}. \tag{4.118}$$

And the impedance matrix $\mathbf{Z}$ is defined in,

$$\begin{matrix} \mathbf{U} & = & \mathbf{Z} & \cdot & \mathbf{I} \end{matrix}$$
$$\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \tag{4.119}$$

With these relations, it is possible to transform the S-parameters into other characteristic parameters [155, 187] such as, admittances, impedances, trans-conductances, trans-impedances and so on.

Aiming for the measurement of impedances employed in parasitic cancellation, let us consider the circuits of Figure 4.44. In the case of parasitic parallel capacitance cancellation, the π-network is a proper model for the final configuration. The admittance matrix $\mathbf{Y}_\pi$ for this circuit is,

$$\mathbf{Y}_\pi = \begin{bmatrix} Y_{\pi,1} + Y_{\pi,3} & -Y_{\pi,3} \\ -Y_{\pi,3} & Y_{\pi,2} + Y_{\pi,3} \end{bmatrix}. \tag{4.120}$$

Solving the system of equations formed by eq. (4.114), eq. (4.115), eq. (4.116), eq. (4.117), eq. (4.118) leads to,

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}\, S_{21}}{R_o\, [(1 + S_{11})(1 + S_{22}) - S_{12}\, S_{21}]} \tag{4.121}$$
$$Y_{12} = \frac{-2\, S_{12}}{R_o\, [(1 + S_{11})(1 + S_{22}) - S_{12}\, S_{21}]} \tag{4.122}$$
$$Y_{21} = \frac{-2\, S_{21}}{R_o\, [(1 + S_{11})(1 + S_{22}) - S_{12}\, S_{21}]} \tag{4.123}$$
$$Y_{22} = \frac{(1 + S_{11})(1 - S_{22}) - S_{12}\, S_{21}}{R_o\, [(1 + S_{11})(1 + S_{22}) - S_{12}\, S_{21}]}. \tag{4.124}$$

From eq. (4.120), if the value of $Y_{\pi,3}$ is desired, it is sufficient to calculate Y_{12}. Therefore, $Y_{\pi,3}$ is given by,

$$Y_{\pi,3} = -Y_{12} = \frac{2\,S_{12}}{R_o\,[(1+S_{11})(1+S_{22}) - S_{12}\,S_{21}]}. \tag{4.125}$$

The case of the T-network in Figure 4.44 is a valid model for the cancellation of equivalent series inductance of filtering capacitors. In this case it is simpler to use the impedance matrix $\mathbf{Z}_T$. Solving the system of equations formed by eq. (4.114), eq. (4.115), eq. (4.116), eq. (4.117), eq. (4.119) leads to,

$$Z_{11} = \frac{R_o\,[(1+S_{11})(1-S_{22}) + S_{12}\,S_{21}]}{(1-S_{11})(1-S_{22}) - S_{12}\,S_{21}} \tag{4.126}$$

$$Z_{12} = \frac{2\,R_o\,S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}\,S_{21}} \tag{4.127}$$

$$Z_{21} = \frac{2\,R_o\,S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}\,S_{21}} \tag{4.128}$$

$$Z_{22} = \frac{R_o\,[(1-S_{11})(1+S_{22}) + S_{12}\,S_{21}]}{(1-S_{11})(1-S_{22}) - S_{12}\,S_{21}}. \tag{4.129}$$

From eq. (4.111), if the value of $1/Y_{T,3}$ is desired, it is sufficient to calculate Z_{12}. Therefore, $1/Y_{T,3}$ is given by,

$$\frac{1}{Y_{T,3}} = Z_{12} = \frac{2\,R_o\,S_{12}}{[(1+S_{11})(1+S_{22}) - S_{12}\,S_{21}]}. \tag{4.130}$$

The impedance of most of the networks employed in parasitic cancellation can be, thus, measured with eq. (4.125) and eq. (4.130). The validity of these expressions is given for the frequency range where the networks can be model as circuits with lumped elements.

Coupled Inductors for Parasitic Cancellation

Another equivalence of interest is given for the networks depicted in Figure 4.46. These are used in some of the capacitance cancellation networks, inductance cancellation networks and other types of filters.

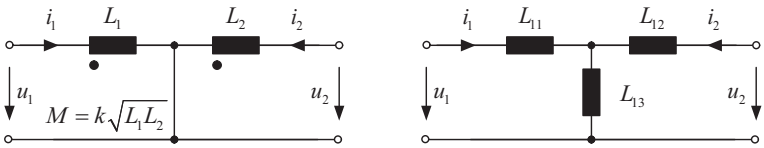


Figure 4.46: Equivalent circuits with and without magnetic coupling.

Considering the coupled inductor circuit, its impedance matrix is given by,

$$\mathbf{Z}_{coupl} = \begin{bmatrix} sL_1 & -sM \\ -sM & sL_2 \end{bmatrix} \tag{4.131}$$

The non-coupled network presents the matrix,

$$\mathbf{Z}_{non-coupl} = \begin{bmatrix} s\left(L_{11}+L_{13}\right) & sL_{13} \\ sL_{13} & s\left(L_{12}+L_{13}\right) \end{bmatrix} \tag{4.132}$$

Solving the equation given by $\mathbf{Z}_{coupl} = \mathbf{Z}_{non-coupl}$ in order to find equivalent networks results that,

$$L_{11} = L_1 + M \tag{4.133}$$
$$L_{12} = L_2 + M \tag{4.134}$$
$$L_{13} = -M \tag{4.135}$$

4.7 Inductance Cancellation for Filter Capacitors

As seen in section 4.3.1, a capacitor can be modeled with a series equivalent inductance ESL. The effect of the ESL is illustrated in Figure 4.47, where the impedance of a filter capacitor is increased for high frequencies due to the ESL. The result for the filter attenuation is that the attenuation curve changes its slope at the self-resonance frequency and an attenuation lower than expected is observed for higher frequencies. In order to avoid this harmful effect, researchers [167,181,182,188,189] have

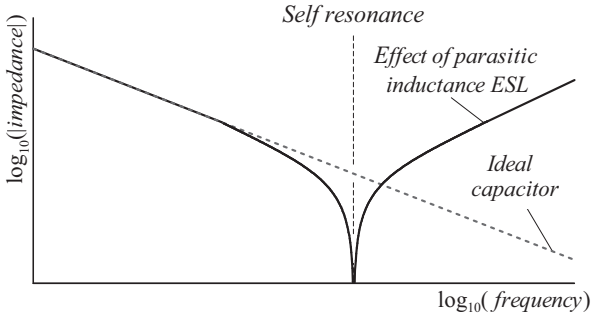


Figure 4.47: Illustration of the effect of the ESL in the impedance of a capacitor.

proposed the use of networks, which ideally eliminate the ESL. As this is a modern and important issue in filtering, a short review of the literature about this topic is done in this section.

In [181, 182, 189] the cancellation of the ESL is achieved through two main networks of coupled inductors, which are shown in Figure 4.48 along with their equivalent circuits without coupling. It is seen that the three-port networks present one port that contains a series negative inductance $-L_s$. This inductance can be ideally built with the inductance value of the ESL, effectively canceling its effect. A solution for simultaneously canceling the ESL of two capacitors, based on the same principles was proposed in [188].

Avoiding the necessity for coupled inductors, a solution was proposed in [167], which makes use of two similar capacitors and two similar inductors as in Figure 4.49.

All the aforementioned solutions have given good practical results, improving the HF performance of the studied filters.

In order to experiment the cancellation ideas in three-phase filters, a prototype was built with the application of the techniques of [181]. The filter structure of Figure 4.50 was built in order to cancel the ESL of the DM inductors. The filter is used in a 6 kW Indirect Matrix Converter [89], that means that the RMS currents expected in the coils are,

$$I_{rms} = \frac{P_2}{3U_N} = \frac{6\,\text{kW}}{3\,230\,\text{V}} \cong 8.7A. \tag{4.136}$$

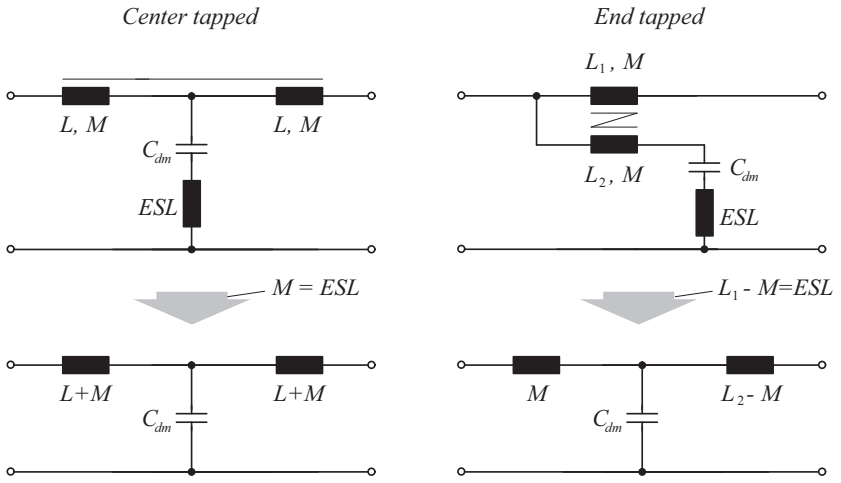


Figure 4.48: Networks of coupled inductors to achieve inductance cancellation as proposed in [181, 182, 189].

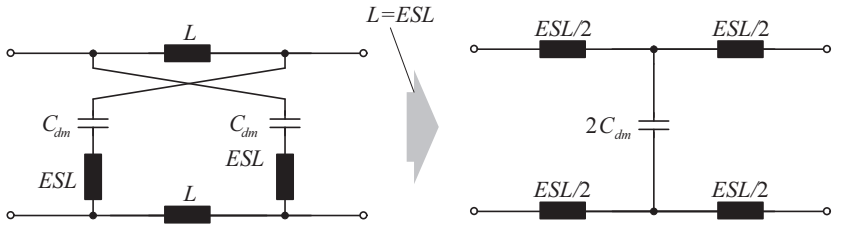


Figure 4.49: Network to achieve inductance cancellation as proposed in [167].

If the coupled inductors are to be built with tracks in the PCB, the involved PCB area would be large. In order to reduce the occupation of the coupled inductors and guarantee a well controlled temperature rise the coupled inductors were built with magnetic wires of diameter $\phi = 1.0$ mm, in the geometry shown in Figure 4.51. The dimensioning of the coil can be made in a simplified way with,

$$L_M = \mu_o \, r \, N_L^2 \left[\ln\left(\frac{8r}{R}\right) - 1.75 \right], \tag{4.137}$$

where L_M is the total inductance of a coreless coil with N_L turns for a wire of radius R.

If a very high coupling is assumed, the inductance L_M should be approximately $2 \times ESL$. The difference, in practice, can be adjusted by measuring the impedances and modifying the geometry. The measured ESL for a 2.2 μF X2 capacitor was 13 nH. The final geometry for the coupled inductors was implemented with a radius $r = 0.9$ mm, wire radius $R = 1.0$ mm and 2×2 turns.

Insertion loss measurements results from the final prototype are shown in Figure 4.52. It is seen that an improvement of approximately 20 dB is achieved for frequencies beyond 10 MHz, while the self-resonance was

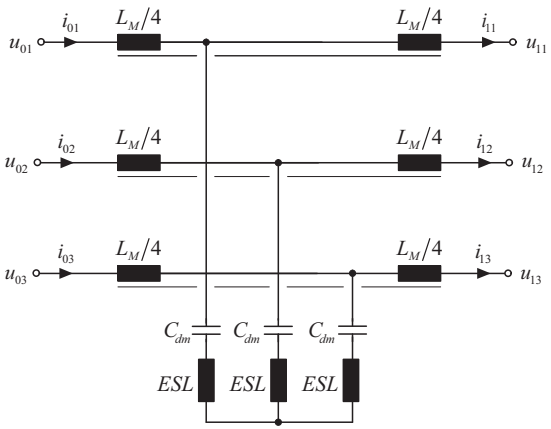


Figure 4.50: Implemented network to filter DM emissions in an 6 kW IMC, where $C_{dm} = 2.2\,\mu$F, $ESL \cong 13$ nH, $L_M \cong 26$ nH.

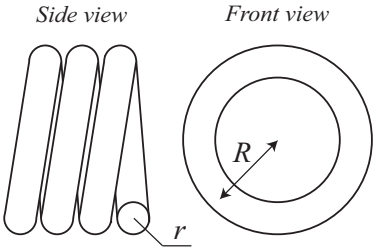


Figure 4.51: Geometry of the built coupled inductor for ESL cancellation.

shifted from 700 kHz to approximately 2 MHz. The presented results reaffirm the possible performance improvement with this technique. The 20 dB improvement has also been reported in other works [167, 181, 182].

Impedance Measurement for the Cancellation Network

In the literature, the performance of the cancellation networks are typically demonstrated with insertion loss measurements. This is due to the three-terminals of the networks. The direct measurement of the impedance would give valuable insight into the achieved results. This

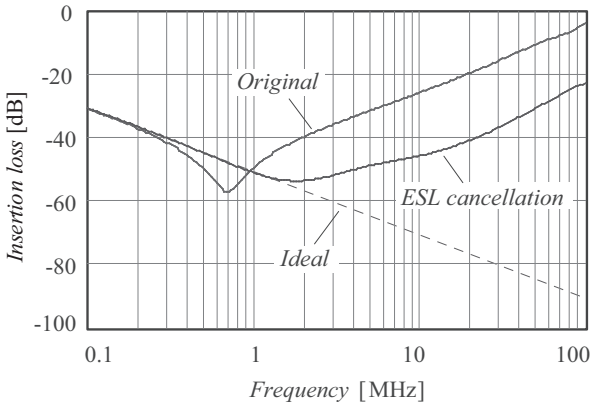


Figure 4.52: Insertion loss measurements of inductance cancellation in a three-phase DM filter for a 6 kW Indirect Matrix Converter.

can be achieved with eq. (4.130) by measuring the S-parameters of the network with a network analyzer. For the case at hand, the measurements are performed with an HP4396A.

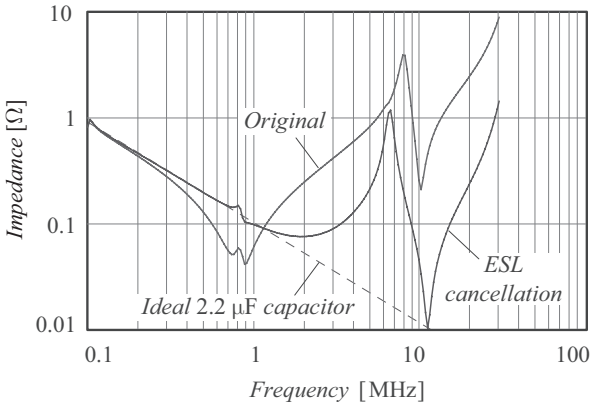


Figure 4.53: Meeasured impedances with and without the ESL cancellation network. The results are obtained from the measurement of the S-parameters.

It is observed in Figure 4.53 that the ideal impedance for the 2.2 μF capacitor is followed up to approximately 2 MHz by the circuit employing the ESL cancellation. Thus, the self-resonance frequency is shifted from $\approx$ 800 kHz to $\approx$ 2 MHz. The impedance of the capacitor from $\approx$ 10 MHz up to $\approx$ 30 MHz is reduced by one order of magnitude validating the expected cancellation effect. The strong resonances are, for the canceled ESL network, more clear. This is due to the lower involved impedances. These resonances represent the transmission line behavior of the circuit, meaning that the simple lumped elements equivalent circuit can not properly model the capacitor structure for higher frequencies.

Comparing the measurements of impedance (cf. Figure 4.53) and insertion loss Figure 4.52, it is clear that the effect of high order resonances is damped by the 50 Ω input/output impedances employed in the insertion loss measurement. This is an advantage of directly measuring the modeled impedance. The disadvantage of this method is that the four S-parameters must be measured, including the phase information.

4.8 Parallel Capacitance Cancellation

Inductors are heavy/bulky components, but are especially useful in reducing CM currents once the utilization of capacitors between lines and protective earth (PE) is limited due to earth leakage current limitations given in electric equipment safety standards (e.g. EN 60950 series). Inductors to be used in filters have been studied and theoretical models have been proposed [166, 178, 190, 191]. All of these equivalent circuit models have in common the connection of a capacitor in parallel with the inductance. The effect of this capacitance is illustrated in Figure 4.54, where it is seen that this parasitic element reduces the performance of the inductor for frequencies beyond the self-resonance.

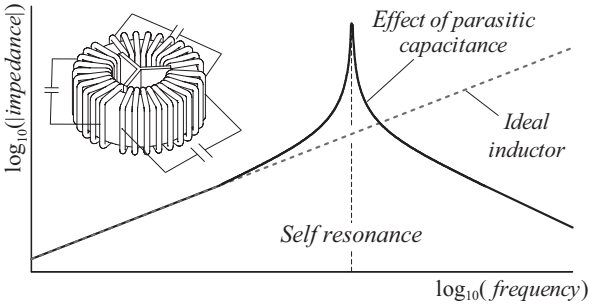


Figure 4.54: Illustration of a three-phase CM inductor with its respective CM impedance curve showing the parallel capacitance effect on the impedance magnitude for high frequencies.

To overcome the challenges imposed by parasitic elements [155] specifically in the construction of inductors, thorough research is being done to improve magnetic materials [19] and, lately, methods to reduce parasitic elements through the use of different circuit topologies in the filtering networks [168,183–185] are proposed. A term called capacitance cancellation has been created to address these techniques, which have the practical outcome of eliminating the parasitic capacitance effects observed from a perspective of CM, DM or both in a filter inside a feasible frequency range. CE are, in general, regulated up to 30 MHz, both in Europe (EN) and USA (FCC). Therefore, this is an upper bound frequency, for which a designed inductor should behave as ideal as possible.

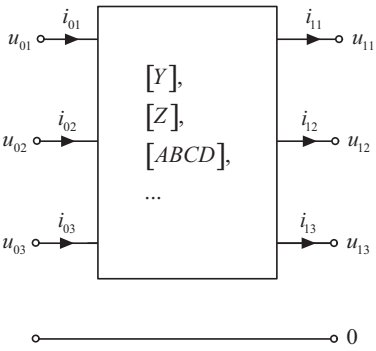
This work aims on analyzing the possibility of applying capacitance cancellation networks to three-phase power line filters, since previous literature on this subject is limited to single phase topologies, but the utility and costs of three-phase power converters are prone to justify the utilization of extra components in the filters. Due to the lack of existing tools for the analysis of three-phase networks, a procedure is presented, which uses the parameters of the networks' admittance matrices ($\mathbf{Y}$) and evaluates relevant impedances for CM and DM. The derived equations are also employed in the search for suitable capacitance cancellation networks, where some of the presented results can be extended to single-phase networks. Cancellation networks are proposed for three-phase inductive networks, where the impact for CM and DM, of the introduced components, is evaluated and the flexibility provided by three-phase networks is exploited. A basic study proposing the possibility of asymmetrical capacitance cancellation is presented. Extra measures are taken to improve the performance of such networks in the higher frequencies of the spectrum. These are based on the study of the influence of other parasitic effects, such as non-ideal coupling factors and winding resistances, which is done theoretically and experimentally as shown by experimental results.

4.8.1 The Use of Admittance Matrices to Analyze Three-Phase Networks for EMC

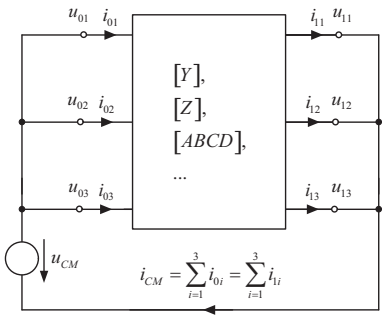
A three-phase network consisting of linear and time invariant elements, as displayed in Figure 4.55(a), is completely defined by one of its characteristic impedances ($\mathbf{Y}$, $\mathbf{Z}$, $\mathbf{T}$, $\mathbf{h}$, $\mathbf{s}$, etc) [186]. The admittance matrix $\mathbf{Y}$, as defined in

$$\begin{array}{ccc} \mathbf{I} & = & \mathbf{Y} \cdot \mathbf{U} \\ \begin{bmatrix} i_{01} \\ i_{02} \\ i_{03} \\ i_{11} \\ i_{12} \\ i_{13} \end{bmatrix} & = & \begin{bmatrix} Y_{1,1} & Y_{1,2} & Y_{1,3} & Y_{1,4} & Y_{1,5} & Y_{1,6} \\ Y_{2,1} & Y_{2,2} & Y_{2,3} & Y_{2,4} & Y_{2,5} & Y_{2,6} \\ Y_{3,1} & Y_{3,2} & Y_{3,3} & Y_{3,4} & Y_{3,5} & Y_{3,6} \\ Y_{4,1} & Y_{4,2} & Y_{4,3} & Y_{4,4} & Y_{4,5} & Y_{4,6} \\ Y_{5,1} & Y_{5,2} & Y_{5,3} & Y_{5,4} & Y_{5,5} & Y_{5,6} \\ Y_{6,1} & Y_{6,2} & Y_{6,3} & Y_{6,4} & Y_{6,5} & Y_{6,6} \end{bmatrix} \cdot \begin{bmatrix} u_{01} \\ u_{02} \\ u_{03} \\ u_{11} \\ u_{12} \\ u_{13} \end{bmatrix} \end{array} \tag{4.138}$$

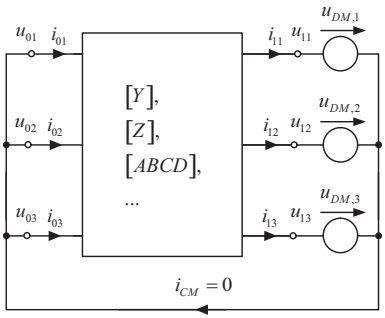
is especially useful if networks are to be connected in parallel, because the resulting matrix ($\mathbf{Y}_{res}$) of the parallel connection of two networks defined by $\mathbf{Y}_1$ and $\mathbf{Y}_2$ is the direct sum of them, $\mathbf{Y}_{res} = \mathbf{Y}_1 + \mathbf{Y}_2$. Some of the capacitance cancellation networks can be placed directly in parallel with the network of inductors and for this reason the admittance matrix is thought of being well suited for the present analysis, even though any other form could be used. The objective of this analysis is to search for equations to evaluate impedances, which are relevant for the EMC assess-



(a) General three-phase network



(b) CM impedance configuration



(c) DM impedance configuration

Figure 4.55: Network configurations used in the derivation of the relevant matrices: (a) General three-phase network; (b) Configuration used for the definition of CM impedance, and; (c) Configuration employed for the DM impedance definition.

ment in three-phase circuit networks. That is here achieved by deriving equivalent impedances from two perspectives, CM and DM, which are based on the admittance matrix of the three-phase network of interest.

Derivation of an Ideal CM Impedance

The circuit configuration presented in Figure 4.55(b) is used to define the total CM impedance (Z_{CM}) presented by the network for an ideal case, where the impedances outside the network are balanced with respect to the reference ground. From the inspection of the circuit,

$$\begin{bmatrix} i_{01} \\ i_{02} \\ i_{03} \\ i_{11} \\ i_{12} \\ i_{13} \end{bmatrix} = \begin{bmatrix} [\mathbf{Y}_{11}] & [\mathbf{Y}_{12}] \\ [\mathbf{Y}_{21}] & [\mathbf{Y}_{22}] \end{bmatrix} \cdot \begin{bmatrix} u_{CM} \\ u_{CM} \\ u_{CM} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \tag{4.139}$$

where $\mathbf{Y}_{11}, \mathbf{Y}_{12}, \mathbf{Y}_{21}$ and $\mathbf{Y}_{22}$ are the 3×3 square sub-matrices of $\mathbf{Y}$.

Simplifying eq. (4.139) leads to,

$$\begin{bmatrix} i_{01} \\ i_{02} \\ i_{03} \end{bmatrix} = [\mathbf{Y}_{11}] \cdot \begin{bmatrix} u_{CM} \\ u_{CM} \\ u_{CM} \end{bmatrix}. \tag{4.140}$$

From eq. (4.140) the individual currents are defined by

$$i_{0i} = u_{CM} \cdot \sum_{m=1}^{3} Y_{m,i}. \tag{4.141}$$

If the network is symmetric, considering the polarities presented in Figure 4.55(b), then $\mathbf{Y}_{12} = -\mathbf{Y}_{21}$ and $\mathbf{Y}_{11} = -\mathbf{Y}_{22}$ and the equivalent CM impedance Z_{CM} presented by the network can be evaluated through,

$$Z_{CM} = \frac{u_{CM}}{i_{CM}} = \frac{u_{CM}}{\sum_{i=1}^{3} i_{0i}} = \frac{u_{CM}}{\sum_{i=1}^{3} \left(u_{CM} \cdot \sum_{m=1}^{3} Y_{m,i} \right)}. \tag{4.142}$$

It is observed that the CM impedance can be calculated by the sum

of all elements of the sub-matrix $\mathbf{Y}_{11}$. Therefore,

$$Z_{CM} = \frac{1}{\sum_{i=1}^{3}\left(\sum_{m=1}^{3} Y_{m,i}\right)}. \tag{4.143}$$

Derivation of the Ideal Series DM Impedances

Again, for the derivation of ideal DM impedances for the three-phase network, the impedances outside the network are considered balanced. The circuit for this derivation is shown in Figure 4.55(c), from where it is seen that three DM voltage sources are placed in one end of the network while the currents of interest are in the other end. The idea is to find the transfer impedance from these variables assuming that the network is balanced. From the circuit configuration of Figure 4.55(c) it follows that,

$$\begin{bmatrix} i_{01} \\ i_{02} \\ i_{03} \\ i_{11} \\ i_{12} \\ i_{13} \end{bmatrix} = \begin{bmatrix} [\mathbf{Y}_{11}]\ [\mathbf{Y}_{12}] \\ [\mathbf{Y}_{21}]\ [\mathbf{Y}_{22}] \end{bmatrix} \cdot \begin{bmatrix} 0 \\ 0 \\ 0 \\ u_{DM,1} \\ u_{DM,2} \\ u_{DM,3} \end{bmatrix} \tag{4.144}$$

from where,

$$\begin{bmatrix} i_{01} \\ i_{02} \\ i_{03} \end{bmatrix} = [\mathbf{Y}_{12}] \cdot \begin{bmatrix} u_{DM,1} \\ u_{DM,2} \\ u_{DM,3} \end{bmatrix}. \tag{4.145}$$

From the definition of differential mode voltages, they must sum to zero,

$$\sum_{i=1}^{3} u_{DM,i} = 0. \tag{4.146}$$

There can be infinity possibilities for this sum to hold true. A general case is assumed, where

$$\begin{cases} u_{DM,1} = U_1 \cdot e^{j\alpha} \\ u_{DM,2} = U_2 \cdot e^{j\beta} \\ u_{DM,3} = -\left(U_1 \cdot e^{j\alpha} + U_2 \cdot e^{j\beta}\right). \end{cases} \tag{4.147}$$

Three DM impedances $Z_{DM,i}$ are defined,

$$Z_{DM,i} = \frac{u_{DM,i}}{i_{0i}}, \text{ where } i = 1..3. \tag{4.148}$$

From eq. (4.145) a general solution for the three currents is found,

$$i_{0i} = \sum_{m=4}^{6} (Y_{i,m} \cdot u_{DM,m-3}). \tag{4.149}$$

By replacing eq. (4.149) in eq. (4.148) a general solution for the three DM impedances is found,

$$Z_{DM,i} = \frac{u_{DM,i}}{\sum_{m=4}^{6} (Y_{i,m} \cdot u_{DM,m-3})}. \tag{4.150}$$

If the network under consideration is symmetric, it follows that $Y_{1,5} = Y_{1,6} = Y_{2,4} = Y_{2,6} = Y_{3,4} = Y_{3,5}$ and $Y_{1,4} = Y_{2,5} = Y_{3,6}$. Therefore, the DM impedances simplify to

$$\begin{aligned} Z_{DM,1} &= \tfrac{1}{Y_{1,4} - Y_{1,5}} \\ Z_{DM,2} &= \tfrac{1}{Y_{2,5} - Y_{2,6}} \\ Z_{DM,3} &= \tfrac{1}{Y_{3,6} - Y_{3,4}} \end{aligned} \tag{4.151}$$

and,

$$Z_{DM,1} = Z_{DM,2} = Z_{DM,3} = Z_{DM,sym}. \tag{4.152}$$

4.8.2 Capacitance Cancellation for Three-Phase Inductive Networks

The results and analysis presented in this section are based on some simplifications of the models for the inductors, namely:

i. a first order approximation, i.e. a lumped inductor in parallel with a lumped capacitor, is adopted for the equivalent circuits, which is valid in most situations up to 30 MHz;

ii. the parallel resistance is omitted since it plays negligible role in the capacitance cancellation;

iii. the influence of the series resistances is here omitted;

iv. some capacitance cancellation networks rely on the magnetic coupling between two portions of an inductor's windings, where a perfect coupling factor $k = 1$ is assumed;

v. the lead inductances are disregarded because they can be seen in series with the remaining networks, thus their connection can be performed in a second step; and,

vi. the networks have balanced impedances.

The influence of the series resistance and the reduction of the coupling factors are studied in section 4.8.6. The adopted simplifications are important in reducing the complexity of the equations and providing useful insight about the involved phenomena.

Simple capacitance cancellation techniques for single-phase systems are proposed in [184, 192], from where a summary is presented in Figure 4.56. It is seen that the equivalent networks are able to cancel the effects of the parallel connected capacitors in both cases. Techniques suitable for three-phase networks are presented in the following.

4.8.3 Capacitance Cancellation for Three-phase CM Inductors

A three-phase CM inductor can be modeled as the six-port network shown in Figure 4.57(a) and for a CM analysis the three inputs can be shortened as well as the output ports, thus the six-port device is simplified to

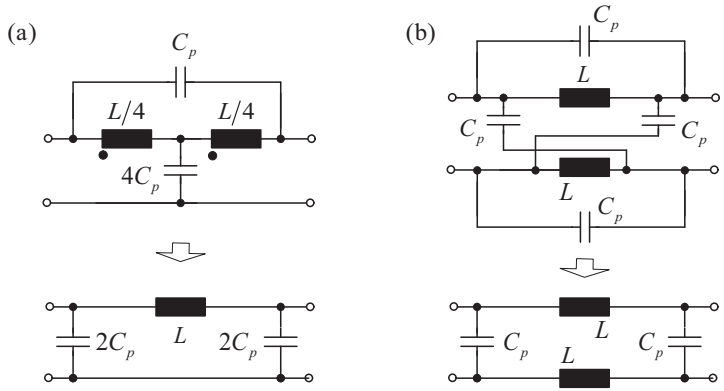


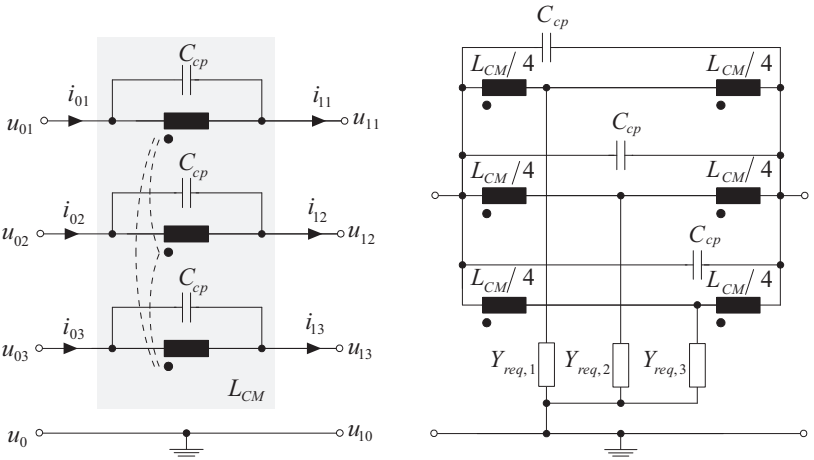
Figure 4.56: Inductor networks with capacitance cancellation as proposed in [184]; (a) cancellation relying on magnetic coupling; and, (b) cancellation for two inductors not relying on magnetic coupling.

a two-port one (cf. Figure 4.57(b)). The final aim for the capacitance cancellation is that the parallel capacitors C_{cp} disappear and an equivalent network as in Figure 4.58 results.

The admittance matrix $\mathbf{Y}_{des}$ of the circuit of Figure 4.58 is

$$\mathbf{Y}_{des} = \begin{bmatrix} \frac{3sK_cC_{cp}}{2} + \frac{s}{sL_{CM}} & -\frac{s}{sL_{CM}} \\ -\frac{s}{sL_{CM}} & \frac{3sK_cC_{cp}}{2} + \frac{s}{sL_{CM}} \end{bmatrix}. \tag{4.153}$$

The remaining analysis considers no magnetic coupling among the different windings. This assumption does not strongly influence the results, since the inter-winding magnetic coupling is reduced for high frequencies due to lowering permeability of any employed core material with increasing frequency. This consideration is on the safe side since the higher the coupling amongst the different windings the better for the capacitance cancellation. An ideal magnetic coupling $k_{cm} = 1$ between the halves of the windings of a phase is considered in order to simplify the equations, but the influence of a non-ideal coupling is studied in section 4.8.6. For a symmetric cancellation network, $Y_{req,1} = Y_{req,2} = Y_{req,3} = Y_{req}$ and the admittance matrix $\mathbf{Y}_{canc}$ for the circuit of Figure 4.57(b) is defined by:



(a) *Three-phase inductor model*

(b) *Network for finding cancellation impedances*

Figure 4.57: Three-phase CM inductor networks: (a) model of a three-phase CM inductor, and; (b) equivalent CM network aiming for finding impedances $Y_{req,i}$, with $i = 1..3$, that effectively cancel the effects of the parallel capacitors C_{cp}.

$$\mathbf{Y}_{canc} = \begin{bmatrix} Y_\alpha & -Y_\beta \\ -Y_\beta & Y_\alpha \end{bmatrix} \tag{4.154}$$

where,

$$Y_\alpha = \frac{9s^3 C_{cp} L_{CM}^2 Y_{req} + 12s^2 C_{cp} L_{CM} + 6sL_{CM} Y_{req} + 4}{sL\left(4 + 3sL_{CM} Y_{req}\right)} \tag{4.155}$$

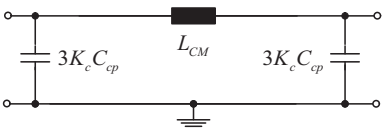


Figure 4.58: Desired final equivalent network for common mode components.

and,

$$Y_\beta = \frac{9s^3 C_{cp} L_{CM}^2 Y_{req} + 12 s^2 C_{cp} L_{CM} + 4}{sL\left(4 + 3sL_{CM} Y_{req}\right)}. \tag{4.156}$$

The capacitance cancellation is achieved when $\mathbf{Y}_{canc} = \mathbf{Y}_{des}$, from where:

$$\begin{cases} Y_{des_{1,1}} = Y_{canc_{1,1}} = Y_\alpha \\ Y_{des_{2,1}} = Y_{canc_{2,1}} = -Y_\beta. \end{cases} \tag{4.157}$$

Solving eq. (4.157) for K_c and Y_{req} leads to

$$\begin{cases} K_c = 4 \\ \frac{1}{Y_{req}} = \frac{1}{4sC_{cp}} - \frac{3sL_{CM}}{4}. \end{cases} \tag{4.158}$$

This shows that the cancellation network can be achieved with the series connection of a negative inductance with a value of $\frac{3}{4}L_{CM}$ with a capacitor of $4C_{cp}$. The final circuit is illustrated in Figure 4.59, where $C_{cc,i} = 4C_{cp}$ and $k_{cm} = 1$. This is a very useful result, since it shows that the inclusion of only three capacitors (of usually small value) is able to cancel the negative effect of the parasitic parallel capacitances.

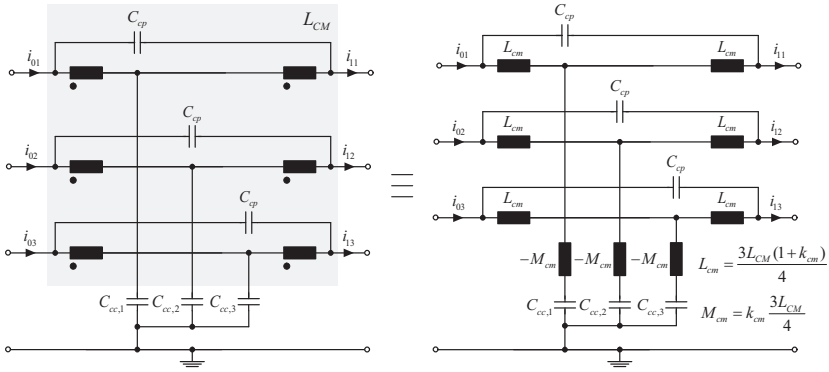


Figure 4.59: Networks that achieve the capacitance cancellation for a three-phase CM inductor (for the equivalence of these networks refer to Appendix I).

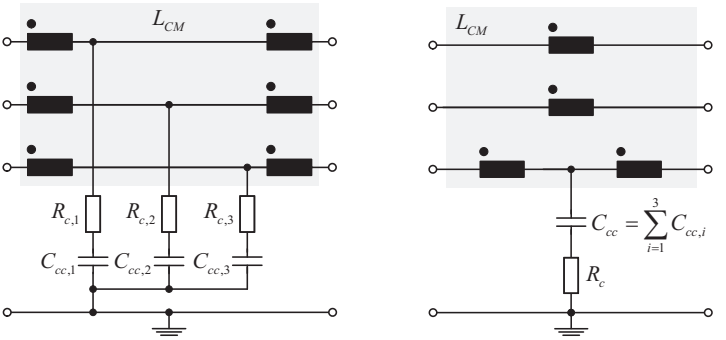
For the case that one of the admittances $Y_{req,i}$ is set to zero, for instance only $Y_{req,3} = 0$, then two capacitors of $6C_{cp}$ suffice for canceling C_{cp} as shown in

$$\begin{cases} K_c = 4 \\ \frac{1}{Y_{req}} = \frac{1}{6sC_{cp}} - \frac{3sL_{CM}}{4}. \end{cases} \tag{4.159}$$

If two admittances are set to zero, for instance only $Y_{req,1} \neq 0$, then a single capacitors of $12C_{cp}$ suffices:

$$\begin{cases} K_c = 4 \\ \frac{1}{Y_{req}} = \frac{1}{12sC_{cp}} - \frac{3sL_{CM}}{4}. \end{cases} \tag{4.160}$$

Equations eq. (4.159) and eq. (4.160) show that for the CM capacitance cancellation of an ideal three-winding CM inductor it is not required that the network cancellation is done symmetrically, thus a single capacitor connected to the center of one winding (cf. Figure 4.60(a)) might be enough. This effect can also be explained by inspecting Figure 4.60(b), where, for CM currents, the voltage is the same in all three windings if one of the following two conditions apply: *(i)* a perfect magnetic coupling between all of the windings is assumed; or, *(ii)* the terminals of the in-



(a) *Three-phase inductor model* (b) *Network for finding cancellation impedances*

Figure 4.60: Networks that provide parasitic capacitance cancellation in a three-phase CM inductor: (a) symmetrical network, where $C_{cc,i} = 4C_{cp}$, and; (b) single capacitor network.

ductors are shorted in, both input and output, what can be expected if balanced capacitors are connected in all terminals as in a conventional CM π-type filter. Thus, by considering the same voltage applied to all three phases, the voltage at the center point of any winding should be the exactly the same, therefore the connection of capacitors between any of these points and the electric ground (PE) shall provide the same effect as long as the coupling factors are high and the external impedances (connected in series with the inductors) are approximately symmetrical and balanced. This might prove useful for manufacturing reasons, since only one center point must be accessed, but attention must be paid if mixed mode noise [41,193] is pronounced in the circuit and if the coupling among the windings is low.

Proof for Neglecting Inter-Winding Couplings

In order to prove that the coupling among different windings in a three-phase CM inductor can be neglected for the analysis of the studied capacitance cancellation techniques the circuits of Figure 4.61 are used. The worst case is tested, since the most asymmetrical network is employed.

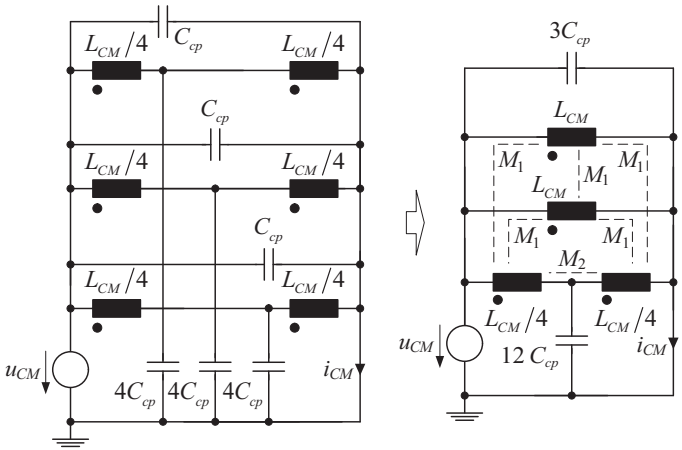


Figure 4.61: Circuits employed for analyzing the impact of the coupling among different windings in a three-phase CM inductor utilizing the proposed capacitance cancellation technique.

Defining the coupling coefficients as,

$$M_1 = k_1 \sqrt{L_{CM} \frac{L_{CM}}{4}}, \tag{4.161}$$

for the coupling inter-windings and,

$$M_2 = k_2 \sqrt{\frac{L_{CM}^2}{4^2}}, \tag{4.162}$$

for the coupling among the halves of one winding. An ideal CM impedance as,

$$Z_{CM,test} = \frac{U_{CM}}{I_{CM}}, \tag{4.163}$$

leads to the following solution for the circuit of Figure 4.61,

$$Z_{CM,test} = \frac{L_{CM}^2 C_{cp}^2 s^4 \left[k_1\left(27k_2^2 - 36k_2 + 9\right) + 18\left(1-k_2^2\right)\right] + L_{CM} C_{cp} s^2 (1-k_2)(18k_1 - 24) - 12k_1 + 16}{L_{CM} C_{cp} s^2 \left[k_1\left(9k_2^2 - 12k_2 + 3\right) + 6\left(1-k_2^2\right)\right] + k_1(2-6k_2) + 4k_2 + 4}. \tag{4.164}$$

The theoretical considerations were based on the ideal coupling among two halves of each inductor, thus,

$$k_2 = 1 \tag{4.165}$$

And eq. (4.164) is simplified to,

$$Z_{CM,test} = \frac{1}{sL_{CM}} \cdot \frac{4 - 3k_1}{2 - k_1}. \tag{4.166}$$

Equation eq. (4.166) shows that the resulting impedance depends on the coupling among different windings (k_1), but does not include any capacitive effect from the parallel capacitances. Therefore, capacitance cancellation is achieved for all possible values of k_1.

4.8.4 Capacitance Cancellation for Three-phase DM Inductors

A network composed of three DM inductors is an important building block for three-phase power filters and, unless special cores and winding techniques are used, three non-coupled inductors are applied. The simplified model for the six-port network is shown in Figure 4.62. Two ways of achieving capacitance cancellation for this network are presented in the following.

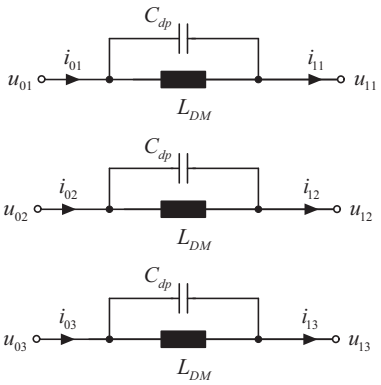
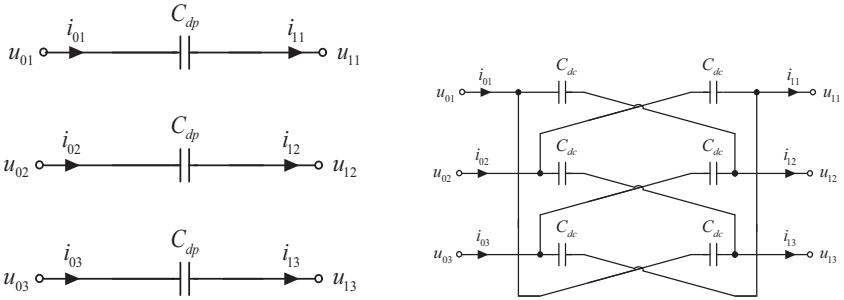


Figure 4.62: Model applied for the analysis of three DM inductors.

First Approach - No magnetic coupling required

As the capacitors and inductors are connected in parallel in the model of Figure 4.62, the inductances can be neglected in a first step because the final network admittance matrix is defined by the sum of the admittances of both circuits. The remaining network is built with the connection of capacitors C_{dp}, as displayed in Figure 4.63(a). The admittance matrix of this network $\mathbf{Y}_{con}$ is

$$\mathbf{Y}_{con} = \begin{bmatrix} sC_{dp} & 0 & 0 & -sC_{dp} & 0 & 0 \\ 0 & sC_{dp} & 0 & 0 & -sC_{dp} & 0 \\ 0 & 0 & sC_{dp} & 0 & 0 & -sC_{dp} \\ sC_{dp} & 0 & 0 & -sC_{dp} & 0 & 0 \\ 0 & sC_{dp} & 0 & 0 & -sC_{dp} & 0 \\ 0 & 0 & sC_{dp} & 0 & 0 & -sC_{dp} \end{bmatrix} \tag{4.167}$$



(a) Parallel capacitances *(b) DM cancellation network*

Figure 4.63: Capacitive networks: (a) parallel capacitances; and, (b) DM capacitive cancellation network.

If the network of Figure 4.63(b) is used for capacitance cancellation, it is left to know the value of capacitors C_{dc}. The admittance matrix $\mathbf{Y}_X$ of this network is

$$\mathbf{Y}_X = \begin{bmatrix} 2sC_{dc} & 0 & 0 & 0 & -sC_{dc} & -sC_{dc} \\ 0 & 2sC_{dc} & 0 & -sC_{dc} & 0 & -sC_{dc} \\ 0 & 0 & 2sC_{dc} & -sC_{dc} & -sC_{dc} & 0 \\ 0 & sC_{dc} & sC_{dc} & -2sC_{dc} & 0 & 0 \\ sC_{dc} & 0 & sC_{dc} & 0 & -2sC_{dc} & 0 \\ sC_{dc} & sC_{dc} & 0 & 0 & 0 & -2sC_{dc} \end{bmatrix} \tag{4.168}$$

And the final admittance matrix $\mathbf{Y}_{DM,final}$ is the sum of both $\mathbf{Y}_{DM,final} = \mathbf{Y}_{con} + \mathbf{Y}_X$. As the networks are symmetric, the DM impedances $Z_{DM,i}$ can be evaluated from eq. (4.151) and it follows that

$$Z_{DM,i} = \frac{1}{Y_{1,4} - Y_{1,6}} = \frac{1}{s(-C_{dp} + C_{dc})}, \text{ where } i = 1..3. \tag{4.169}$$

The aim of the capacitance cancellation in this case is to achieve infinite DM impedance. This is fulfilled, by inspecting eq. (4.169), if

$$C_{dp} = C_{dc} \Rightarrow Z_{DM,final,i} \rightarrow \infty. \tag{4.170}$$

An important parameter for the evaluation of the final network is the impedance observed from CM, since the DM inductors have an impact on CM currents as well. The serial CM impedance can be calculated with eq. (4.143) leading to

$$Z_{CM,final} = \frac{1}{\sum_{i,m=1}^{3} Y_{m,i}} = \frac{1}{3(2sC_{dc} + sC_{dp})}. \tag{4.171}$$

Replacing eq. (4.170) in eq. (4.171) leads to a final CM impedance of

$$Z_{CM,final} = \frac{1}{9sC_{dp}}. \tag{4.172}$$

From eq. (4.170) and eq. (4.172) it is seen that, with the inclusion of the six capacitors C_{dc}, the parallel capacitance C_{dp} is cancelled for DM currents, whereas for CM the final capacitance is increased three times in value. This is clear from the inspection of Figure 4.64, where the CM analysis can be done by connecting input and output ports respectively together and the equivalent capacitance is the sum of all capacitors.

Second Approach - Relying on magnetic couplings

If the inductors L_{DM} of Figure 4.65 are split into two halves, the same principle as used in the CM cancellation section can be used (cf. Figure 4.59) and the required admittances $Y_{req,i}$ can be derived.

The admittance matrix $\mathbf{Y}_{d,canc}$ of the network of Figure 4.65 is given by

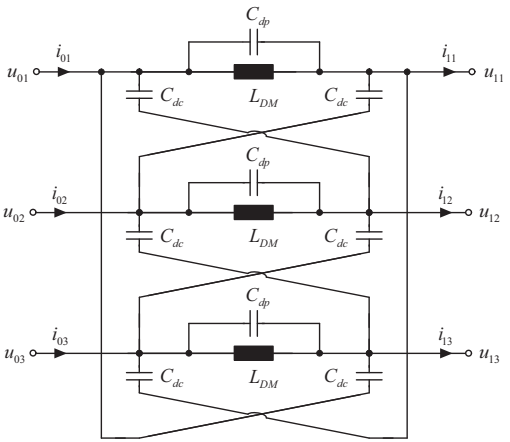


Figure 4.64: Final network for DM capacitance cancellation. The connection of capacitors C_{dc} effectively cancels the effect of C_{dp} for DM currents, not relying on magnetic couplings. For CM currents the final capacitance is increased three fold, being a drawback of this type of network.

$$\mathbf{Y}_{d,canc} = \begin{bmatrix} Y_A & -Y_B & -Y_B & -Y_A & -Y_B & -Y_B \\ -Y_B & Y_A & -Y_B & -Y_B & -Y_A & -Y_B \\ -Y_B & -Y_B & Y_A & -Y_B & -Y_B & -Y_A \\ Y_A & Y_B & Y_B & -Y_A & Y_B & Y_B \\ Y_B & Y_A & Y_B & Y_B & -Y_A & Y_B \\ Y_B & Y_B & Y_A & Y_B & Y_B & -Y_A \end{bmatrix}, \tag{4.173}$$

where:

$$Y_A = \frac{3s^2 C_{dp} L_{DM}^2 Y_{req,d} + 12 s^2 C_{dp} L_{DM} + 5 s L_{DM} Y_{req,d} + 12}{3 s L_{DM} \left(4 + s L_{DM} Y_{req,d}\right)} \tag{4.174}$$

and

$$Y_B = \frac{Y_{req,d}}{3\left(4 + s L_{DM} Y_{req,d}\right)}. \tag{4.175}$$

The only element that is desirable for the DM currents is the induc-

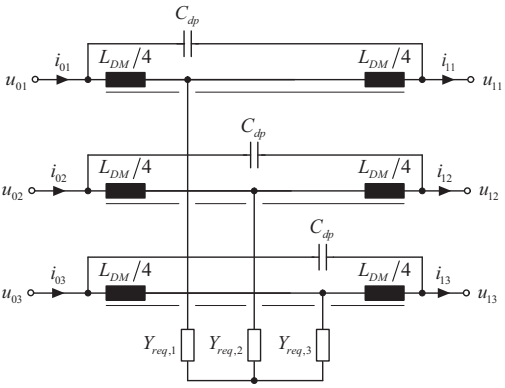


Figure 4.65: Circuit to implement capacitance cancellation for DM inductors.

tance L_{DM}, therefore the desired DM impedance $Z_{DM,canc,i}$, evaluated through eq. (4.151) and eq. (4.173), is

$$Z_{DM,canc,i} = \frac{1}{Y_{1,4} - Y_{1,6}} = \frac{1}{-Y_A - Y_B} = -\frac{1}{sL_{DM}}. \tag{4.176}$$

Solving the system of equations formed by eq. (4.173), eq. (4.174), eq. (4.175) and eq. (4.176) it follows that

$$Z_{DM,canc,i} = \frac{-1}{sL_{DM}} \rightarrow Y_{req,i} = \frac{1}{\frac{1}{4sC_p}\frac{sL_{DM}}{4}}. \tag{4.177}$$

from where,

$$C_{dy,i} = 4C_p. \tag{4.178}$$

The idea of using a network similar to the one used for the CM capacitance cancellation also works here. The final network is presented in Figure 4.66, where the capacitors $C_{dy,i}$ are added for canceling the effects of C_{dp}.

What is left is the calculation of the impedance observed by CM currents. This is calculated using eq. (4.173), eq. (4.174), eq. (4.175) and eq.

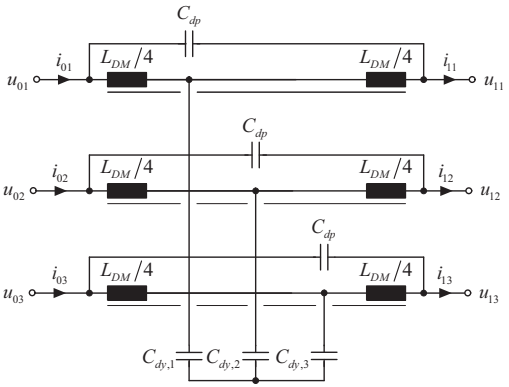


Figure 4.66: Network to achieve capacitance cancellation for DM inductors used in three-phase filters based on the magnetic coupling among two halves of each of inductors.

(4.177) into eq. (4.143), leading to

$$Z_{CM} = \frac{1}{\sum_{i,m=1}^{3} Y_{m,i}} = \frac{sL_{DM}}{(s^2 C_{dp} L_{DM} + 1)}, \tag{4.179}$$

which is the same impedance seen without the inclusion of the capacitance cancellation network, therefore this approach does not decrease the final CM impedance.

In the circuit of Figure 4.66 the capacitors $C_{dy,i}$ are connected in a Y-configuration. From the Y-Δ circuit transformation, it is clear that a Δ-connection of capacitors with one third of the value of the Y-connected capacitors is fully equivalent to the Y-configuration. Therefore, the circuit of Figure 4.67 is derived, leading to canceling capacitors $C_{d\Delta,i}$ defined as,

$$C_{d\Delta,i} = \frac{4C_p}{3}. \tag{4.180}$$

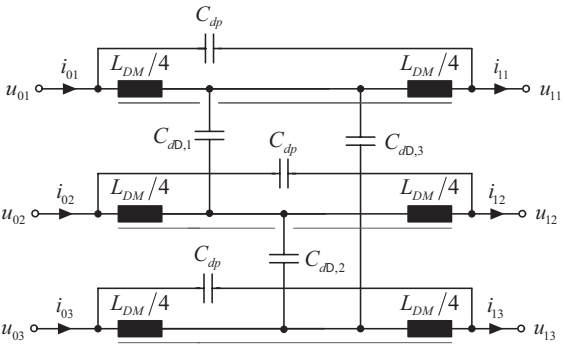


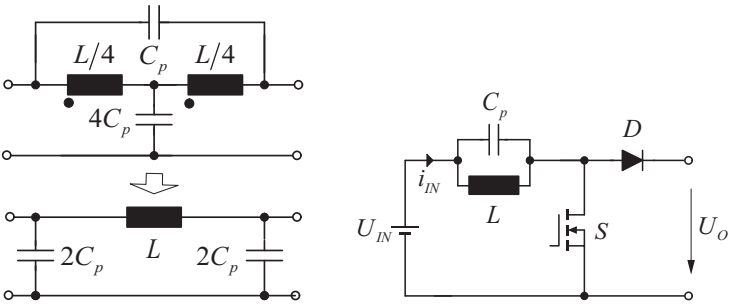
Figure 4.67: Network in Δ-configuration to achieve capacitance cancellation for DM inductors used in three-phase filters based on the magnetic coupling among two halves of each of inductors.

4.8.5 Short Discussion on Asymmetrical Cancellation

The networks presented in the previous section and in the literature [168, 183, 184] have as a characteristic that the final equivalent circuit is symmetric from the input/output impedances perspective. In these networks, the connection of the canceling elements is symmetric as in Figure 4.68(a).

For the case where an inductor is used directly at the input of a switching cell (cf. Figure 4.68(b)), the switches S_1 and S_2 will present part of the switching losses which are approximately proportional to the parallel capacitance C_p, thus this capacitance is completely unwanted. If the symmetrical capacitance cancellation networks are used, the effective parallel capacitance is increased. In fact it is doubled for the circuit in Figure 4.68(a), what means that the switching losses due to C_p would be twice as much. This would require special attention of design engineers in the use of the cancellation techniques and leads to the question: is it possible to implement a cancellation network (asymmetric [194]), which does not increase the capacitance to be switched?

To start with, the networks presented in Figure 4.69 are used, where the parameters L_1, L_2 and K are left undefined and a mutual inductance with unitary magnetic coupling factor is considered $M = \sqrt{L_1 \cdot L_2}$. The admittance matrices of the networks are used to derive the values.



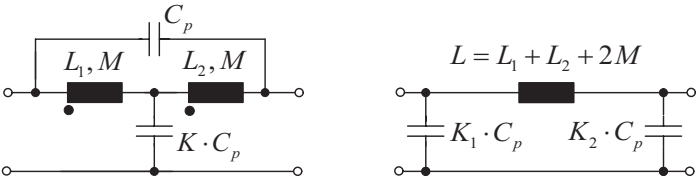
(a) *Symmetric capacitance cancellation* (b) *Switching cell with input inductor*

Figure 4.68: (a) Basic principle for symmetric capacitance cancellation and its equivalent circuit. (b) Inductor applied at the input of a switching cell, where its parasitic parallel capacitance increases switching losses in the cell.

The admittance matrix for the circuit in Figure 4.69(a) $\mathbf{Y}_C$ is

$$\mathbf{Y}_C = \begin{bmatrix} Y_{\alpha,C} & -Y_{\beta,C} \\ -Y_{\chi,C} & Y_{\delta,C} \end{bmatrix}, \tag{4.181}$$

where



(a) *Asymmetric cancellation network* (b) *Desired equivalent circuit*

Figure 4.69: Networks used to analyze the possibility of asymmetric parasitic capacitance cancellation. (a) Proposed cancellation network; and, (b) desired equivalent circuit.

$$Y_{\alpha,C} = \frac{(L_1 + L_2 + 2M)\, C_p s^2 + Y_{req} L_2 s + 1}{s\,(L_1 + L_2 + 2M)} \tag{4.182}$$

$$Y_{\beta,C} = Y_{\chi,C} = \frac{(L_1 + L_2 + 2M)\, C_p s^2 + Y_{req} M s + 1}{s\,(L_1 + L_2 + 2M)} \tag{4.183}$$

$$Y_{\delta,C} = \frac{(L_1 + L_2 + 2M)\, C_p s^2 + Y_{req} L_1 s + 1}{s\,(L_1 + L_2 + 2M)}. \tag{4.184}$$

The admittance matrix for the circuit in Figure 4.69 $\mathbf{Y}_D$ is

$$\mathbf{Y}_D = \begin{bmatrix} Y_{\alpha,D} & -Y_{\beta,D} \\ -Y_{\beta,D} & Y_{\alpha,D} \end{bmatrix}, \tag{4.185}$$

where

$$Y_{\alpha,D} = \frac{(L_1 + L_2 + 2M)\, K_1 C_p s}{L_1 + L_2 + 2M} + \frac{1}{s\,(L_1 + L_2 + 2M)} \tag{4.186}$$

$$Y_{\beta,D} = Y_{\chi,D} = \frac{-1}{s\,(L_1 + L_2 + 2M)} \tag{4.187}$$

$$Y_{\delta,D} = \frac{(L_1 + L_2 + 2M)\, K_2 C_p s}{L_1 + L_2 + 2M} + \frac{1}{s\,(L_1 + L_2 + 2M)}. \tag{4.188}$$

The capacitance cancellation is achieved when $\mathbf{Y}_C = \mathbf{Y}_D$, resulting in a system of four linearly independent equations. Solving this system leads to

$$K = \frac{K_2^2}{K_2 - 1} \tag{4.189}$$

$$K_1 = \frac{K_2}{K_2 - 1} \tag{4.190}$$

$$L_1 = (K_2 - 1)\, M \tag{4.191}$$

$$L_2 = \frac{1}{K_2 - 1} M. \tag{4.192}$$

For the design of such a network, a value is chosen for K_2 the other

parameters follow. Although, there is a theoretical lower boundary for K_2, given by $K_2 \geq 1$. This limit, in practice, means that the original parallel capacitance C_p can not be downsized from a perspective of switching losses. The total amount of capacitance $K \cdot C_p$ used in the cancellation circuit has its minimum at $K_2 = 2$ as shown in Figure 4.70, which is the case for symmetric cancellation. This means that for an asymmetric cancellation more capacitance must be used. This brings the advantage that the input capacitance $K_1 C_p$ is large, thus providing more effective filtering.

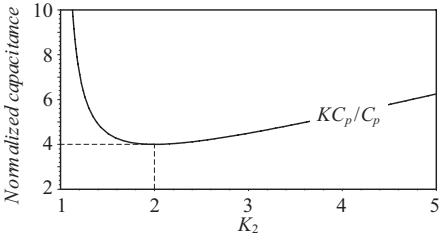


Figure 4.70: Normalized total capacitance KC_p/C_p required for the cancellation of C_p as a function of K_2.

The implementation of such a technique is more involved, since the splitting of the inductor is not done at its center point, but depends strongly in the chosen ratio K_2. Figure 4.71 illustrates how the inductance must be divided in order to achieve capacitance cancellation, where it becomes clear that if a small K_2 is desirable, the inductor shall be divided in uneven parts. The required turns ratio N_1/N_2, assuming unitary magnetic coupling, follows the line L_1/M.

4.8.6 Study on the Influence of Parasitic Elements

The previous sections have assumed close to ideal equivalent circuits, but as the high frequency behavior of the components is paramount for EMC, the influence of the main parasitic effects must be considered. For that, the circuit of Figure 4.72 is used, where the stray resistances of the windings R_σ, a non-ideal magnetic coupling k_{cm} among the halves of the windings and the stray inductance L_σ are considered.

The calculation of the CM impedance is done with equation eq. (4.141)

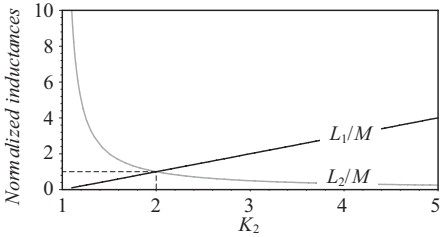


Figure 4.71: Normalized inductances and turns ratio required for the cancellation of C_p as a function of K_2.

and of the DM impedance with equation eq. (4.151), both applied to the admittance matrices of the network of Figure 4.72.

The derived CM impedance $Z_{par,CM}$ is given by,

$$Z_{par,CM}=\frac{1}{3}\,\frac{\left[6\,\pi^2 f^2 k_{cm} L_{CM} C_{cp}-6\,\pi^2 f^2 C_{cp} L_{CM}+1+\left(-16\,\pi^2 f^2 L_\sigma+8\,i R_d \pi\, f+4\,i\pi\, f R_\sigma\right)C_{cp}\right]\cdot}{36\,\pi^4 f^4 {C_{cp}}^2 {k_{cm}}^2 {L_{CM}}^2+\left[(-96\,\pi^4 f^4 L_\sigma+48\,i\pi^3 f^3 R_d)C_{cp}{}^2-6\,\pi^2 f^2 C_{cp}\right]L_{CM} k_{cm}-\ldots}$$
$$\frac{\left(3\,i\pi\, f L_{CM}+3\,i\pi\, f L_{CM} k_{cm}+2\,R_\sigma\right)\cdot}{\ldots 36\,\pi^4 f^4 {C_{cp}}^2 {L_{CM}}^2+\left[(48\,i\pi^3 f^3 R_d+48\,i\pi^3 f^3 R_\sigma-96\,\pi^4 f^4 L_\sigma)C_{cp}{}^2+6\,\pi^2 f^2 C_{cp}\right]L_{CM}-1+\ldots}$$
$$\frac{1}{\ldots\left[16\,\pi^2 f^2 {R_\sigma}^2+(32\,\pi^2 f^2 R_d+64\,i\pi^3 f^3 L_\sigma)R_\sigma\right]{C_{cp}}^2+(-8\,i R_d \pi\, f+16\,\pi^2 f^2 L_\sigma-4\,i\pi\, f R_\sigma)C_{cp}}. \tag{4.193}$$

The calculated DM impedance $Z_{par,DM}$ is,

$$Z_{par,DM}=-1/3\,\frac{\left[6\,\pi^2 f^2 k_{cm} L_{CM} C_{cp}-6\,\pi^2 f^2 C_{cp} L_{CM}+1+\left(-16\,\pi^2 f^2 L_\sigma+8\,i R_d \pi\, f+4\,i\pi\, f R_\sigma\right)C_{cp}\right]\cdot}{36\,\pi^4 f^4 {C_{cp}}^2 {k_{cm}}^2 {L_{CM}}^2+\left[(-96\,\pi^4 f^4 L_\sigma+48\,i\pi^3 f^3 R_d)C_{cp}{}^2+6\,\pi^2 f^2 C_{cp}\right]L_{CM} k_{cm}\ldots}$$
$$\frac{\left(3\,i\pi\, f L_{CM}+3\,i\pi\, f L_{CM} k_{cm}+2\,R_\sigma\right)\cdot}{-36\,\pi^4 f^4 {C_{cp}}^2 {L_{CM}}^2+\left[(48\,i\pi^3 f^3 R_d+48\,i\pi^3 f^3 R_\sigma-96\,\pi^4 f^4 L_\sigma)C_{cp}{}^2+18\,\pi^2 f^2 C_{cp}\right]L_{CM}-1+\ldots}$$
$$\frac{1}{\left[16\,\pi^2 f^2 {R_\sigma}^2+(32\,\pi^2 f^2 R_d+64\,i\pi^3 f^3 L_\sigma)R_\sigma\right]{C_{cp}}^2+(16\,\pi^2 f^2 L_\sigma-8\,i R_d \pi\, f-12\,i\pi\, f R_\sigma)C_{cp}}. \tag{4.194}$$

Due to the complexity of equations eq. (4.193) and eq. (4.194), surfaces are plotted in Figure 4.73 providing insight into the influence of the non-ideal parameters. Figure 4.73(a) shows the CM impedance as a function of frequency and the coupling factor k_{cm}, from where it is seen that the resonance frequency decreases for low values of coupling and is infinite for unitary coupling. The influence of the series resistances R_σ has the same

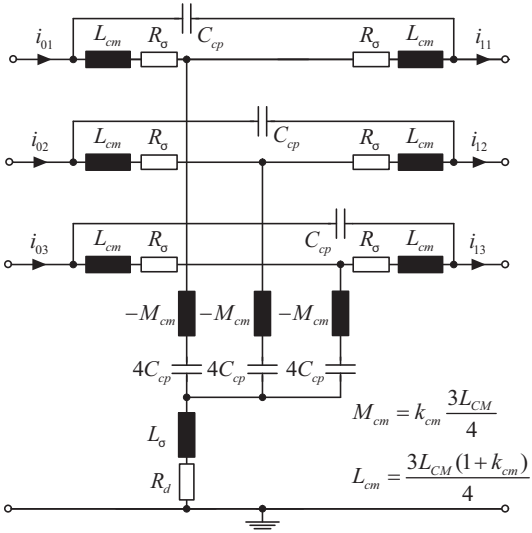


Figure 4.72: Circuit used for analyzing the influence of parasitic elements R_σ, L_σ and k_{cm} in the performance of the capacitance cancellation for a three-phase CM inductor. Damping resistor R_d is shown.

type of effect as lowering the magnetic coupling as seen in Figure 4.73.

The use of the capacitance cancellation network leads to the inclusion of L_σ, what creates resonances at frequencies higher than the original self-resonance. It produces undesired resonances in both, CM and DM, impedances and if these resonances are under 30 MHz they degrade the expected filtering performance for conducted emissions, otherwise they affect radiated emissions. These resonances can be damped with the help of a damping resistance R_d as observed in Figure 4.73(c) and Figure 4.74. The increase of the inductor's series resistance R_σ has a similar damping behavior, but it considerably lowers the capacitance cancellation effect. For the CM impedance shown in Figure 4.74(a), the lack of the capacitance cancellation networks would shift the upper corner frequency from approximately 7 MHz down to approximately 900 kHz.

Similar conclusions can be draw for the DM capacitance cancellation techniques leading to similar results.

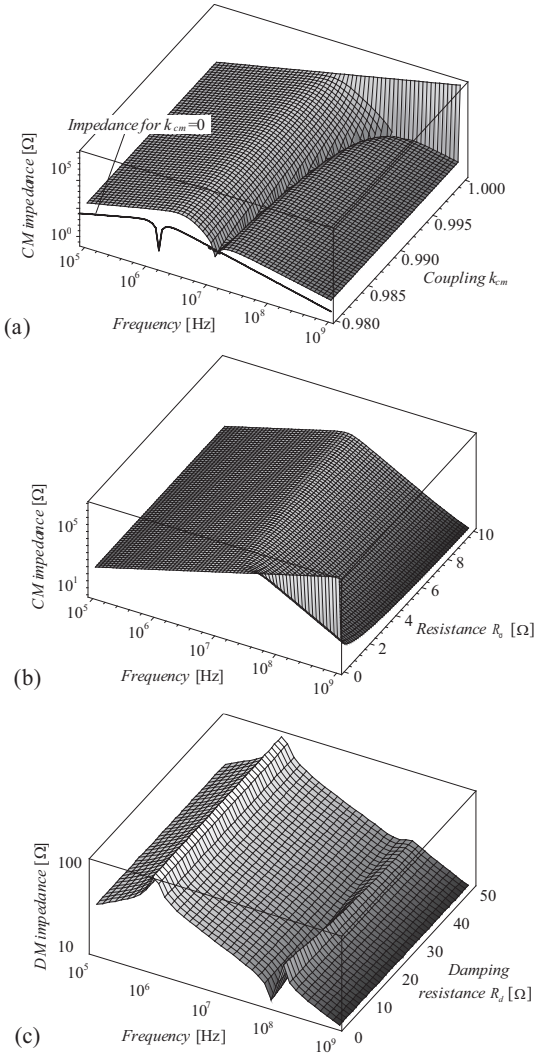
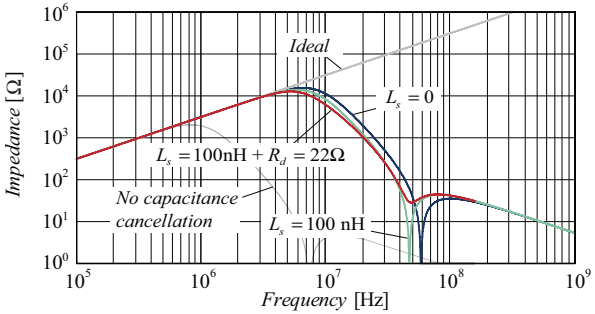
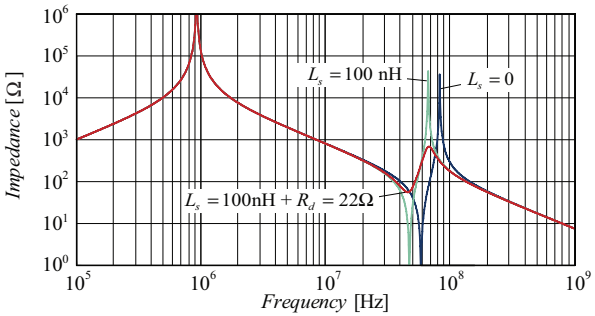


Figure 4.73: Influence of parasitic elements, where $L_{CM} = 500\ \mu$H and $C_{cp} = 10$ pF; (a) CM impedance as a function of the coupling factor k_{cm} with $R_\sigma = 0\,\Omega$ and $L_\sigma = 0$ H; (b) CM impedance as a function of the series resistance R_σ with $k_{cm} = 1$ and $L_\sigma = 0$ H, and; (c) DM impedance as a function of the damping resistance R_d with $k_{cm} = 1$, $R_\sigma = 0$ and $L_\sigma = 100$ nH.



(a) Influence on CM impedance



(b) Influence on DM impedance

Figure 4.74: Influence of L_σ in the (a) CM and (b) DM impedances and the possibility of damping by inserting a resistor R_d in series.

4.8.7 Experimental Results

Experiments are performed in order to verify the presented principles. Two filter circuits, one comprising a single LC stage DM filter and another one with a single-stage CM filter as shown in Figure 4.76, are used to verify the achievable insertion loss with the application of some of the presented techniques. The filters are built in a way that the capacitors included for capacitance cancellation $C_{canc,CM}$ and $C_{canc,DM}$ are easily removable, so that the effects of their inclusion are clearly observed. The inductors are wound such that both halves of each winding are close to each other, assuring high magnetic coupling among the inductor's halves.

This is accomplished by winding the inductors in two layers, one winding half on top of the other [184] as shown in Figure 4.75.

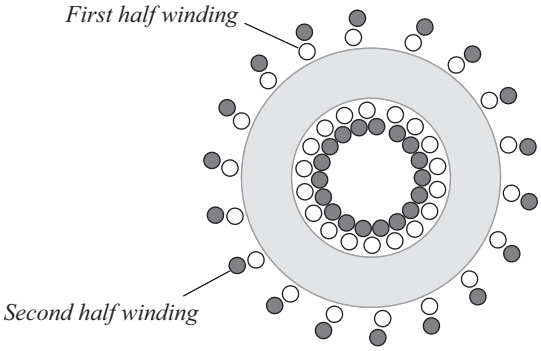


Figure 4.75: Winding arrangement for assuring high coupling among the halves of the windings.

The first measurements were performed with an impedance analyzer in order to evaluate the total parallel capacitance for each of the inductors. The parallel capacitances were measured with the technique described in [195]. For the CM inductor LCM the total measured parallel capacitance was 17.7 pF, while the capacitance for the DM inductors had an average of 52 pF within 2% variation among the three inductors L_{DM}.

A second set of experiments comprised measurements of insertion loss of the filter boards with a two-port network analyzer HP4195A. The experimental setup is as in Figure 4.77. CM insertion loss measurements are performed with the first port connected between terminals A, B and C together and PE and the second port connected from a, b and c to PE. DM insertion loss is measured with the help of two insulation transformers (input and output) from terminals A and B to terminals a and b. The insertion loss measurements are performed with both filters connected in series. Due to the limited commercially available capacitance values, only approximate values were used. This was relevant information also in order to evaluate the sensibility to the variation in capacitance.

Figure 4.78(a) shows the insertion loss measurements for CM when applying capacitance cancellation networks which employ: (*i*) upper trace – no capacitance cancellation network; (*ii*) middle trace – a single 220 pF capacitor connected to the center of one of the windings as in eq. (4.160),

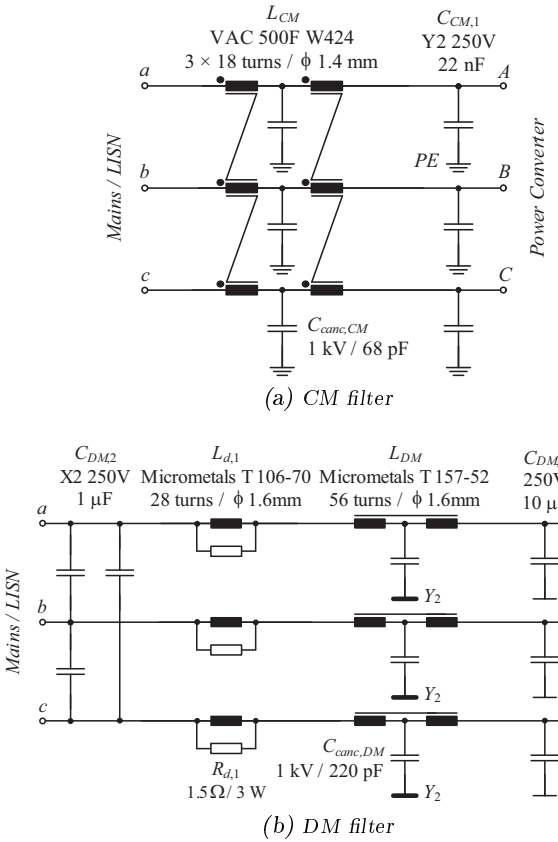
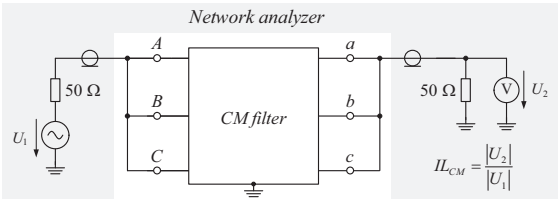


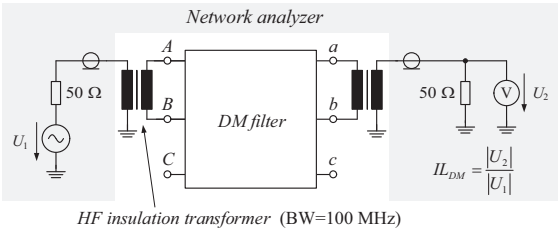
Figure 4.76: Input filter circuits employed in the testing of capacitance cancellation techniques. (a) CM filter structure employed in the experiments, and; (b) DM filter used to test the capacitance cancellation.

and; (*iii*) lower trace – three 68 pF capacitors as in eq. (4.158), each connected to each one of the windings.

The effectiveness of the capacitance cancellation networks is clearly observed since the resonance of the circuit without cancellation at approximately 2 MHz is no longer observed and an increasing gain in the insertion loss curves is seen up to 30 MHz, where a difference of more than 20 dB is seen from the configuration with three capacitors. The con-



(a) CM insertion loss measurement



(b) DM insertion loss measurement

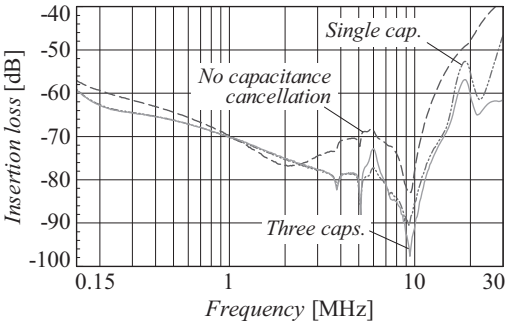
Figure 4.77: Insertion loss measurement setups for: (a) CM insertion loss; and, (b) DM insertion loss.

nection of a single capacitor is less effective due to low magnetic coupling amongst the three windings. Thus, an appreciable difference is noticed for frequencies higher than 15 MHz. The worsening in the attenuation curve beyond the resonance at 9.4 MHz is observed with and without cancellation, thus this is a point were a resonance acoours, which is not the self resonance of the inductor (2 MHz).

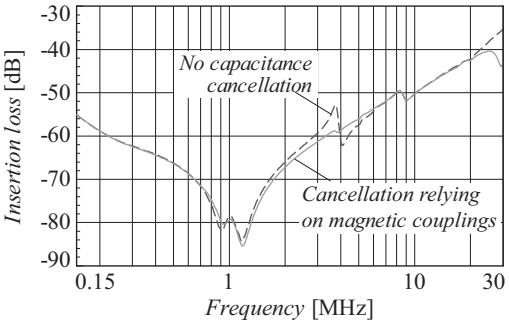
The insertion loss curves for the DM capacitance cancellation are presented in Figure 4.78(b) for a network as in Figure 4.66. It is observed that the results are not as expressive as in the CM case. A deeper analysis proves that, depending on the complete filter configuration, the cancellation of these capacitances might not improve the situation considerably. This is due to the relation between all impedances involved, for instance, of a resonance frequency. Despite that, the measurements with the DM capacitance cancellation show an improvement in very high frequencies and an appreciable reduction of the resonance peak at 4 MHz.

The improvement observed in the DM insertion loss curves is not substantial. Therefore, a measurement is performed only with the three

DM inductors, that means, removing components $C_{DM,2}$, $L_{d,1}$ and $R_{d,1}$ from the printed circuit board. The result is shown in Figure 4.79, where it is seen that the cancellation works, shifting the resonance frequency of the circuit from 1 MHz to more than 3 MHz and improving the insertion loss by 17 dB at 10 MHz.



(a) *CM insertion loss measurement*



(b) *DM insertion loss measurement*

Figure 4.78: Insertion loss measurements showing the application of capacitance cancellation in the employed three-line power filters. (a) Filter CM insertion loss illustrating the application of capacitance cancellation to a three-phase CM choke. Shown are: measurement without capacitance cancellation; with three cancellation capacitors (68 pF per winding); and, with a single one (220 pF) connected to one of the windings. (b) DM insertion loss measurement with and without capacitance cancellation to three DM inductors (220 pF per inductor).

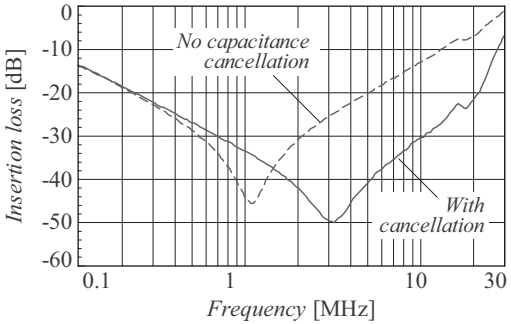
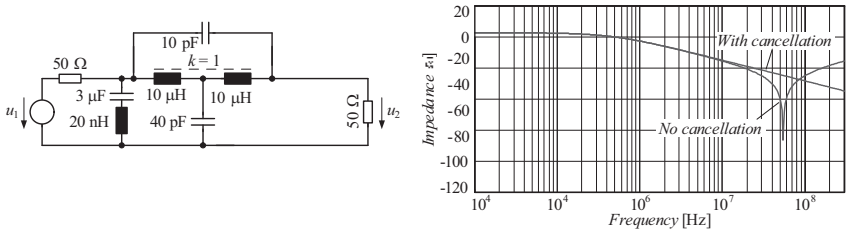


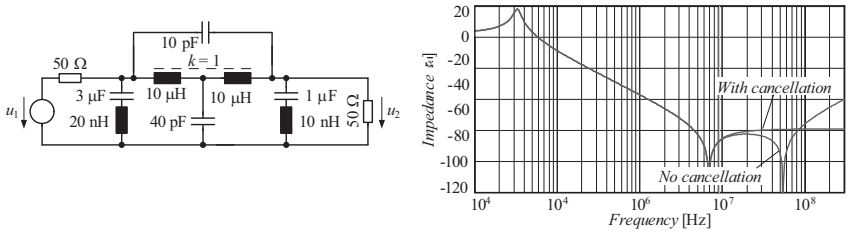
Figure 4.79: Insertion loss measurement for the DM filter when removing components $C_{DM,2}$, $L_{d,1}$ and $R_{d,1}$ from the PCB.

In order to understand the performance presented for the DM cancellation, three simple simulations are done assuming unitary coupling among the halves of the winding of the inductor, amounting for a total of 40 μH in parallel with 10 pF. The canceling capacitor is four times larger (40 pF). The simulated circuits and respective results (attenuation from u_2 to u_1) are presented in Figure 4.80. The first simulation (cf. Figure 4.80(a)) shows a simple filter configuration where a single capacitor (3 μF) with its ESL (20 nH) is employed at the input and the results show an improvement of approximately 20 dB at 30 MHz. Figure 4.80(b) a capacitor (1 μF + 10 nH) is included at the output, thus forming a π-type filter and, again, 20 dB improvement is observed. At the third simulation (cf. Figure 4.80(c)), a small amount of coupling (k = 0.05) is added between the filtering inductor and the output capacitor's ESL. It is observed that the resonances are shifted and the effect of the capacitance cancellation is only observed for higher frequencies, so that only approximately 6 dB improvement is achieved at 30 MHz. This result alerts for the fact that, depending on the complexity of the filter, the effects of capacitance cancellation might be lower than expected in practical filters and special care should be taken when designing the filter layout.

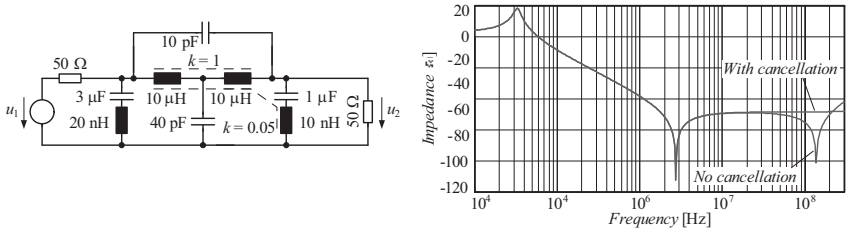
A third set of experiments utilizes a three-phase 6 kVA adjustable speed drive (ASD) prototype based on a highly compact indirect matrix converter (IMC). The converter is built with "state-of-the-art" reverse blocking IGBTs (RB-IGBT) [89] is employed as emissions source. An external filter board comprising, both DM and CM (cf. Figure 4.76), filters



(a) *LC filter.*



(b) *π-type filter.*



(c) *π-type filter with coupling from inductor to capacitor.*

Figure 4.80: Simulation circuits and results (attenuation from u_2 to u_1) for explaining the influence of coupling with external components in the performance of parasitic capacitance cancellation. (a) Simple filter employing on capacitor and the inductor with and without cancellation. (b) π-type filter, and (c) π-type circuit with coupling from the output capacitor to the inductor's winding.

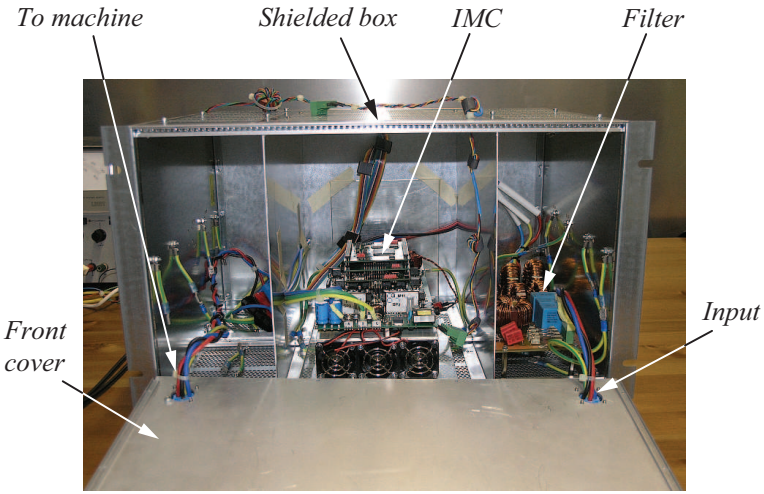


Figure 4.81: Shielded box containing the designed filter and the Indirect Matrix Converter as employed in the CE measurements.

connected in series is placed at the input of the converter.

Conducted emission measurements with the filters and the IMC supplying a 2 kVA asynchronous machine through a 3 m long shielded cable were performed with and without the inclusion of the discussed cancellation capacitors. In order to restrain HF couplings between the designed filter and the power circuits of the IMC, a shielded box with separate chambers to separately accommodate the power circuits and the input filters was built as shown in Figure 4.81.

The CE measurement results are displayed in Figure 4.82, where a three-phase CM/DM noise separator [150] is used in order to show the different contributions of the noise modes and the impact of the capacitance cancellation in each of them. The measured CM emissions are seen in Figure 4.82(a) for both versions of the filter, with and without the cancellation capacitors. Once the capacitance cancellation network is included, it is seen that the emission levels are appreciably reduced in the frequency ranges from 150 kHz to 500 kHz and from around 3 MHz to 30 MHz. However, the improvements are not as significant as in the insertion loss measurements. This is because the IMC's noise source impedance cer-

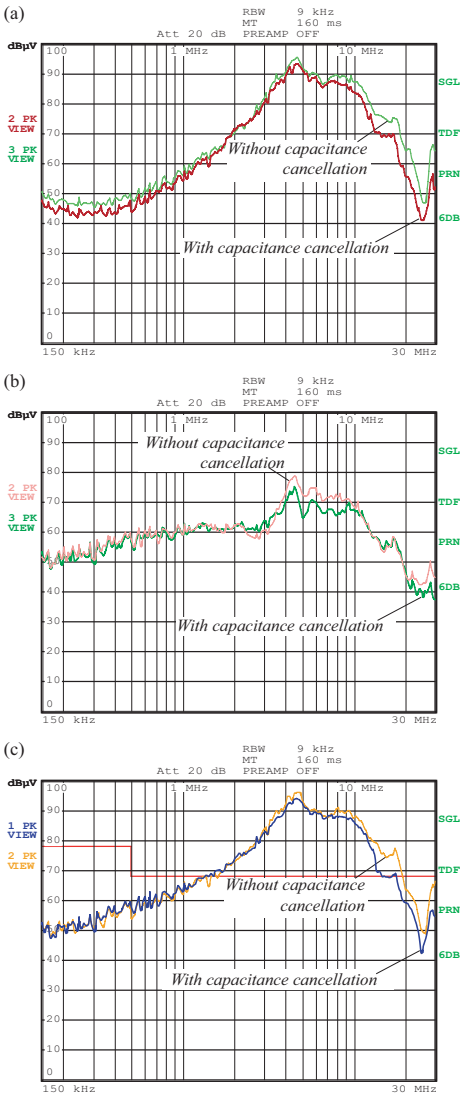


Figure 4.82: Conducted emission (CE) measurements performed in a three-phase 6 kVA ASD prototype built with an indirect matrix converter (IMC) based on RB-IGBTs. (a) CM emission levels; (b) DM emission levels, and; (c) total measured emissions.

tainly presents an impedance value which is different from the impedance used for measuring the insertion loss (50 Ω). Another probable reason is the increased series equivalent resistance for high frequencies due to higher temperatures and current ripple amplitudes when compared to the small signal insertion loss measurements. The DM emissions are depicted in Figure 4.82(b). From there it is observed that improvements are present in the frequency ranges from 4 MHz to 10 MHz and from around 20 MHz to 30 MHz. As for the CM case, the difference with the inclusion of canceling capacitors is not the same observed in the insertion loss. Finally, the total emission levels for one of the phases is shown in Figure 4.82(c), where it is seen that improvements are achieved with the inclusion of capacitance cancellation networks.

4.9 Summary

This chapter has presented models and the major issues for passive components employed in EMC filters for three-phase PWM converters.

A brief review of the application of resistors is done, highlighting the main requirements for such components. It is shown that resistors are not employed as filtering elements in high power applications due to the associated losses. They are applied as damping elements for the resonances of the reactive components. For this reason, very simple models can be used.

Safety requirements represent the main demand for filter capacitors, directly influencing their manufacturing technology. The classical model for a capacitor is reviewed, from where the calculation of the ESR and ESL based on data sheet information is explained. It is shown that, for the employed capacitor technology, the dependency of the capacitor volume is linearly dependent on its energy storage capacity and a model that can be used for the minimization of the volume of filters is derived.

Differential mode inductors are modeled, based on toroidal cores, which present clear advantages for EMC filtering. Equivalent circuits are presented, where the estimation of the equivalent circuit components is explained. Thermal models for toroidal inductors are reviewed and a model, based on empirical considerations is derived. A comparison among available core materials is performed, from where selection criteria are reviewed.

Three-phase common mode toroidal inductors are carefully studied. A lumped elements based equivalent circuit from the basic operation of these devices is explained in detail. The parameters present strong dependency on core material characteristics. A method for the selection of the material for minimized volume inductors is proposed. The calculation of the leakage inductance is reviewed along with the related saturation issues. Finally, experimental results validate the presented modeling procedure. This model can be used for the design of CM inductors.

Parasitic cancellation networks are studied. The cancellation of the equivalent series inductance of filter capacitors is reviewed and an application is experimentally tested in a three-phase filtering application.

A systematic way of evaluating impedances (CM and DM) in three-phase networks to be used in power line filtering is proposed. The alternatives provided by three-phase networks have been explored to achieve winding parasitic capacitance cancellation. Techniques have been presented for three-phase inductive networks along with a comprehensive theoretical analysis, where advantages and side-effects of the networks have been highlighted and possible improvements through damping resistances and use of different networks have been proposed. The influence of common parasitic effects was studied, from where the guidelines for a good design can be derived. The possibility of asymmetrical capacitance cancellation was proposed, which can improve the application of these techniques for switched mode power circuits. With the application of the proposed cancellation networks it is expected that cheaper inductors can be used, since the magnetic component designer is able to use a core with fully winded window. In order to prevent the elevation of the cost with capacitors it is proposed that the small capacitors are integrated into the printed circuit board whenever possible. A set if experimental results attest the presented principles and prove that the analyzed techniques allow for improvements in the performance of an EMC filter. From the experimental analyzes it is seen that the degree of improvement is dependent on the circuit structure, since different source and load impedances considerably change the influence of an inductor's parasitic capacitance. Good layout techniques, other parasitic impedance cancellation techniques and the reduction of capacitive and magnetic couplings are to be used along with the capacitance cancellation and shall allow for more compact, cheap and high performance filtering.

Chapter 5

Noise Separation for Three-Phase Systems

"There is no reason to have problems between country and country, between government and government, when there is a separation of powers." Ricardo Lagos

5.1 Introduction

Three-phase conducted emission (CE) measurements are a major issue for developing high power electronic equipment that is connected to a commercial electric grid due to EMC concerns which are reflected in international and regional product regulations. Three-phase power electronic systems, such as motor drives and high power rectifiers, must comply with these regulations. To achieve EMC compliance, electronic equipment must include filtering and/or other electromagnetic emission control strategies. The conceptualization and the dimensioning of these emission control techniques are increasingly researched and, as a result, analytical and experimental tools are developed to aid the electrical design engineers.

Proper CE measurements, such as specified in CISPR 16 [104], demand highly complex equipments, therefore expensive ones, which should be qualified for the evaluation of electromagnetic emissions. They typically include test receivers, high frequency (HF) probes, line impedance

stabilizing networks (LISNs), shielded cables, a proper electromagnetic environment and loads. Test receivers and LISNs are typically specified in relevant EMC standards, thus very useful and are employed from pre-compliance facilities in the industry to sophisticated EMC test houses. But, this combination alone does not provide information about the nature, CM or DM, of the measured emissions, meaning that the emission levels can not be discriminated in a typical CE test setup.

The qualitative and quantitative assessment of the noise modes, common (CM) and differential (DM) modes, is of great importance since the designed emission control strategy is dependent on these. The main objective of this chapter is to propose devices that can be integrated into three-phase CE standard measurement systems. Thus, allowing the separate evaluation of CM and DM emission levels. This type of device is here named the three-phase CM/DM noise separator.

Circuits that provide the discrimination of noise modes for single-phase systems have been presented in [39, 196–200] and their operating principle is based on the fact that the summing and subtracting of two sensed voltages leads to the measurement of the distinct emission values for CM and DM. Other methods that use mathematical analysis through Fast Fourier Transformation [201] are used, provided that sampling rates are adequate and phase information is correctly computed.

Focusing on the separated evaluation of CM and DM emissions in three-phase systems, some methods are proposed in the literature. The most common technique is based on current measurements [202], therefore the measurements are not performed at the outputs of a LISN. This technique relies on HF current probes, which bandwidth and precision are decisive for high quality measurements. A method for predicting CE levels without the need of a LISN and relying on numeric calculations based on wide-band hardware for data acquisition is proposed in [201], but it requires a deep knowledge and measurements on the power converter. Another technique based on HF measurements is introduced in [203], which can be used in different connection points of a system. However HF current and voltage probes, power splitters and hybrid junctions are required, which increase the complexity of the circuit and reduce its accuracy. In [44] a noise separation method for three-phase drives presenting a diode-bridge type of rectifier is proposed, being this a very particular case. This method is also based on wide-band data acquisition hardware and numeric calculations.

In order to provide a simple interface between a LISN and a test receiver in a conventional CE test setup, novel separation networks, passive and active ones, are presented here. With these networks a real-time direct measurement of DM and CM emission levels in a typical CISPR 16 specified setup [104, 141] is achieved. These networks allow for the direct measurement of CM and DM levels provided that three outputs of the LISN are accessible. The active network demands for very careful layout and large bandwidth / low noise amplifiers, which must be supplied through a very quiet power supply. The first passive solution presents all the requirements for the noise separation, being simple, robust and capable to directly measure the relevant signals. However, this network is based on HF transformers, which must present a high bandwidth and should not saturate. Besides that, parasitic elements, such as stray inductances and inter-winding capacitances, should be very well controlled; otherwise performance for high frequencies is deteriorated. Finally, networks based on transmission line transformers are proposed. With this type of transformers, high performance for HF is to be expected, as well as good impedance matching in order to fulfill strict impedance requirements, such as those of CISPR 16. With the use of TLTs, transverse electromagnetic (TEM) energy transfer mode is employed and smaller cores are utilized.

5.2 Separation of CM/DM in Three-Phase Systems

International EMC standards, such as CISPR 16, define CE test setups including a LISN, which are typically built as shown in Figure 5.1. The mains is very well filtered by the LISN components, so that it does not significantly affects the EUT. The cutoff frequencies are specified in the standards. Low frequency components are coupled from the equipment under test (EUT) to the power grid through inductors L_1 and L_2. The high frequency content generated by the EUT is decoupled from the grid and coupled to the test receiver and 50 Ω terminations through capacitors C_1. Therefore, a high frequency simplified circuit can be derived (cf. Figure 5.1), which takes into account only the HF harmonic components.

In the HF simplified circuit from Figure 5.1 the EUT is modeled as three DM voltage sources $u_{DM,a}$, $u_{DM,b}$ and $u_{DM,c}$ connected in a Y configuration in series with a CM voltage source u_{CM} and, by superposition,

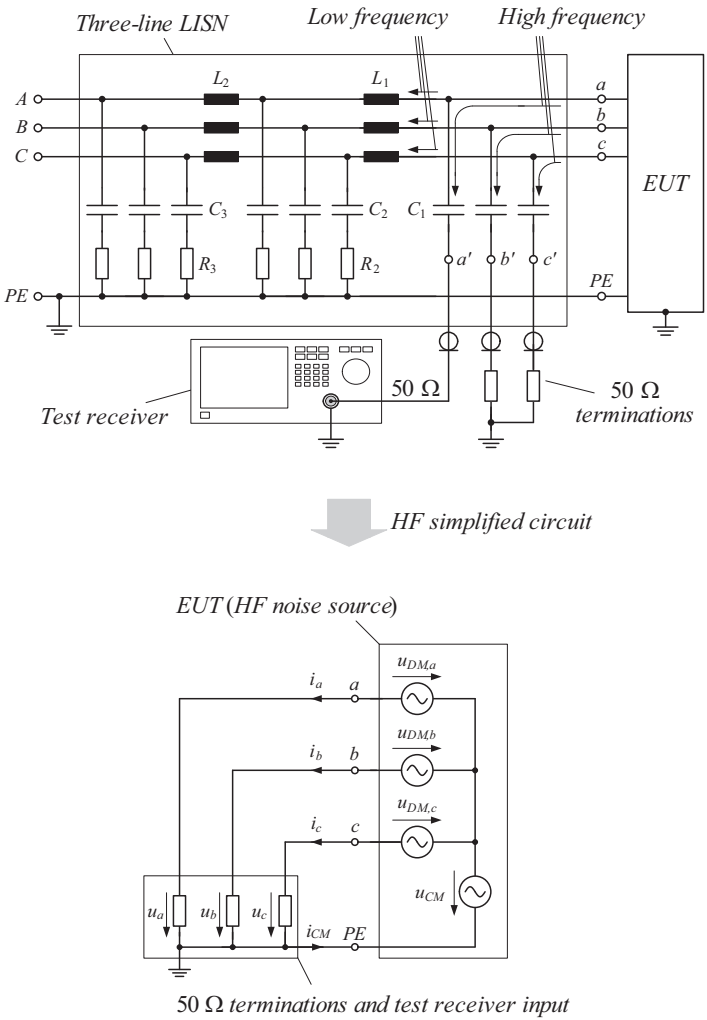


Figure 5.1: Schematics of a typical three-phase CE test setup employing a LISN illustrating the low and high frequency coupling paths and its HF equivalent simplified circuit.

the effect of each of these voltage sources is summed linearly in the 50 Ω resistors. Through mathematical calculations it is possible to properly separate the contribution of the noise sources in the sensed voltages u_a, u_b and u_c. From Figure 5.1 the following system of equations is obtained:

$$u_i = u_{DM,i} + u_{CM} \tag{5.1}$$

$$i_i = \frac{u_i}{50\,\Omega} \tag{5.2}$$

$$i_{CM} = \sum_{i=1}^{3} \frac{u_i}{50\,\Omega} \tag{5.3}$$

From the definition of DM voltages,

$$\sum_{i=1}^{3} u_{DM,i} = 0. \tag{5.4}$$

Solving the system of equations formed by eq. (5.1), eq. (5.2), eq. (5.3) and eq. (5.4) leads to the DM voltages as linear functions of the sensed voltages:

$$\begin{bmatrix} u_{DM,a} \\ u_{DM,b} \\ u_{DM,c} \end{bmatrix} = \frac{1}{3} \cdot \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \cdot \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}. \tag{5.5}$$

Whereas, the CM voltage is given by,

$$u_{CM} = \frac{1}{3} \cdot \begin{bmatrix} 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}. \tag{5.6}$$

Even though the effects of the CM and DM sources are superposed in the LISN, by sensing the three voltages at the 50 Ω terminations and performing the operations specified in equations eq. (5.5) and eq. (5.6), it is possible to access separately the different noise mode contributions.

5.3 Three-Phase CM/DM Noise Separator Based on HF Transformers

In order to practically implement the mathematical formulation given in the previous section and properly separate both noise modes using an electrical network a circuit topology based on high bandwidth transformers is proposed in Figure 5.2 [204]. In both figures the high frequency noise components are depicted by a common mode voltage source u_{CM} and three differential mode voltage sources $u_{DM,a}$, $u_{DM,b}$ and $u_{DM,c}$.

In this section, the theoretical analysis of this passive network is given for its ideal basic circuit and, in a second step, accounting for the influence of first order parasitic elements in the employed transformers.

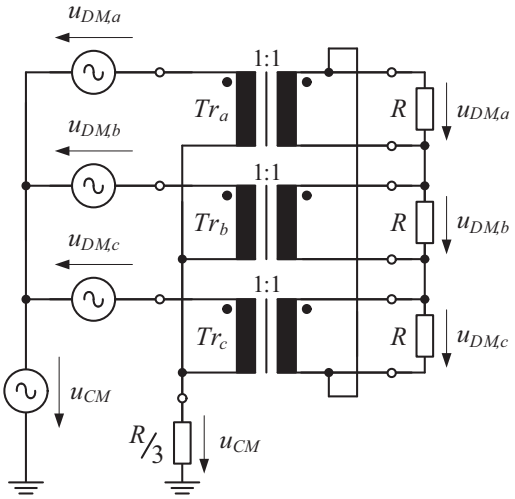


Figure 5.2: Proposed three-phase CM/DM noise separator based on HF transformers.

5.3.1 Operating Principle Analysis

The passive solution comprises of three transformers Tr_a, Tr_b and Tr_c with Y-connected primaries, Δ-connected secondary windings and one-to-one turns ratio. The primary side star-point is connected to the ground via

a resistor $R/3$ while the secondary windings are terminated by resistors R.

The mathematical analysis of the circuit helps to clarify the noise separation effect. Equations eq. (5.7) and eq. (5.8) are obtained from the circuit.

$$u_{CM} + u_{DM,i} - u_{DM,out,i} = u_{CM,out} \tag{5.7}$$

$$\sum_{i=1}^{3} u_{DM,out,i} = 0 \tag{5.8}$$

According to the definition of the differential mode voltage sources and based on the fact that the termination impedances R_a, R_b and R_c are balanced it follows that,

$$\sum_{i=1}^{3} u_{DM,i} = 0 \tag{5.9}$$

The summing of the three equations included in eq. (5.7) leads to,

$$u_{CM} = u_{CM,out} \tag{5.10}$$

By replacing eq. (5.10) in eq. (5.7) gives,

$$u_{DM} = u_{DM,out,i} \tag{5.11}$$

Based on eq. (5.10) and eq. (5.11) it is clear that the proposed network provides at its output ports the values for the differential and common mode voltages.

5.3.2 Input Impedances Calculation

Another relevant issue for the measurement setup is the value of the input impedances of the network since the CE measurements with a LISN usually specifies 50 Ω balanced sensing resistors. Since the network is symmetric the analysis of the input impedances is performed with the help of Figure 5.3 for only one of the inputs.

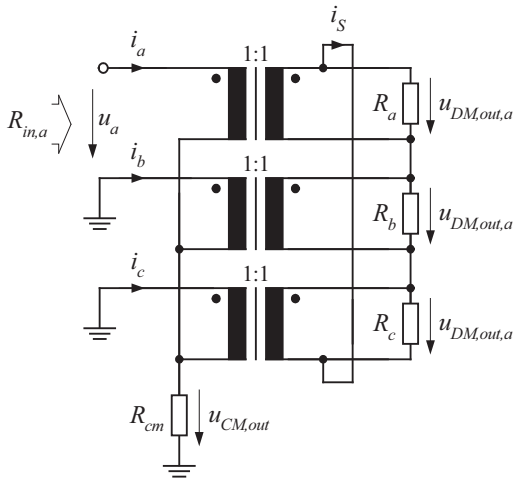


Figure 5.3: Circuit used for the calculation of the input impedances to ground (PE).

By solving the circuit equations one gets,

$$\frac{u_a}{i_a} = 9\frac{R_a R_b R_c R_{CM}}{R_a R_b R_c + R_{CM}\left[4R_b R_c + R_a\left(R_b + R_c\right)\right]} \tag{5.12}$$

In order to have a balanced circuit the resistors R_i must be made equal, so that,

$$R_a = R_b = R_c = R \tag{5.13}$$

Replacing eq. (5.13) in eq. (5.12) results in,

$$\frac{u_a}{i_a} = \frac{9}{\frac{6}{R} + \frac{1}{R_{CM}}} \tag{5.14}$$

Since the DM output ports will be sensed with the resistance R and this will be done in a test receiver with an input resistance of 50 Ω it is desirable that the input resistance present the same value, i.e. $R_{in} = R$. Solving eq. (5.14) leads to,

$$R_{CM} = \frac{R}{3} \tag{5.15}$$

Based on the presented analytical equations it is certain that the proposed network is able to perform the separation of CM and DM conducted emission levels in a standard CE measurement setup.

5.3.3 Influence of Parasitic Elements in the Noise Separation Network

The circuit shown in Figure 5.4 is employed in order to analyze the effects of the parasitic elements in the separation network physical components. Considering symmetrical components, the separation performance is mainly influenced by four major parasitic effects, namely the magnetic coupling factor (k) of the transformers, the inter-winding capac-

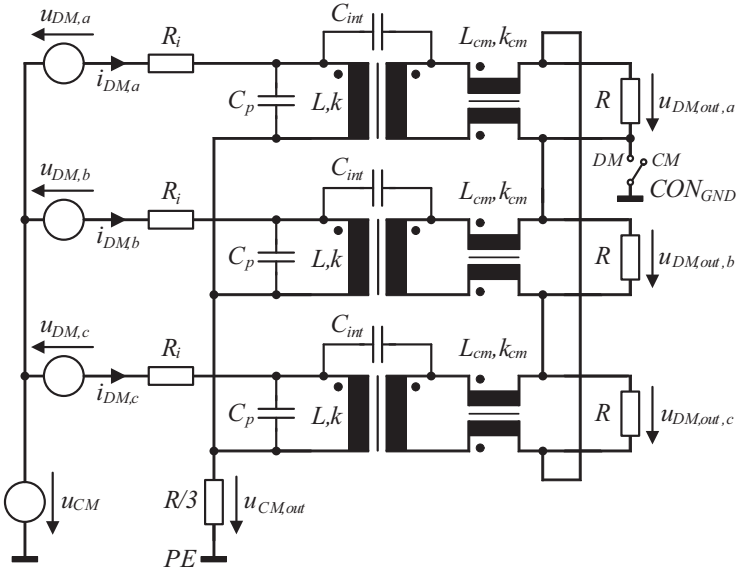


Figure 5.4: Circuit employed for the parasitic elements analysis of the three-phase CM/DM noise separator.

itance (C_{int}) and the parallel capacitance (C_p) of the transformer and the coupling factor (k_{cm}) of the output inductors (L_{cm}), which are used in order to increase the common mode rejection ratio (CMRR) for DM measurements, since for DM measurements, the connection of one of the DM outputs to PE should be made in the test receiver and this creates a path for CM currents through $CONGND$. Furthermore, the voltage sources are modeled with a definite output resistance (R_i) and the unbalances among the circuit components are neglected in a first step. For DM measurements it is considered that a connection CON_{GND} from the DM output A to PE is present. This connection is not used for the CM measurements.

The influence of parasitic elements is analyzed in the following high frequency transfer functions: (*i*) differential mode transmission ratio (DMTR); (*ii*) common mode transmission ratio (CMTR); (*iii*) differential mode rejection ratio (DMRR); (*iv*) common mode rejection ratio (CMRR). These are defined as,

$$\mathrm{DMTR} = 20\log\left(\left|\frac{U_{DM,out,A}}{U_{DM,a}}\right|\right)\Bigg|_{\substack{U_{DM,b}=U_{DM,a}\cdot e^{j\frac{2\pi}{3}} \\ U_{DM,c}=U_{DM,a}\cdot e^{-j\frac{2\pi}{3}} \\ U_{CM}=0}} \tag{5.16}$$

$$\mathrm{CMTR} = 20\log\left(\left|\frac{U_{CM,out}}{U_{CM}}\right|\right)\Bigg|_{U_{DM,a}=U_{DM,b}=U_{DM,c}=0} \tag{5.17}$$

$$\mathrm{DMRR} = 20\log\left(\left|\frac{U_{CM,out}}{U_{DM,a}}\right|\right)\Bigg|_{\substack{U_{DM,b}=U_{DM,a}\cdot e^{j\frac{2\pi}{3}} \\ U_{DM,c}=U_{DM,a}\cdot e^{-j\frac{2\pi}{3}} \\ U_{CM}=0}} \tag{5.18}$$

$$\mathrm{CMRR} = 20\log\left(\left|\frac{U_{DM,out,A}}{U_{CM}}\right|\right)\Bigg|_{U_{DM,a}=U_{DM,b}=U_{DM,c}=0} \tag{5.19}$$

Another important parameter for the separation network is the input impedance (Z_{in}) which is seen from one of the input terminal to PE. This is defined as,

$$Z_{in} = \left.\frac{U_{DM,a}}{I_{DM,a}}\right| \begin{array}{l} U_{DM,b} = U_{DM,a} \cdot e^{j\frac{2\pi}{3}} \\ U_{DM,c} = U_{DM,a} \cdot e^{-j\frac{2\pi}{3}} \\ U_{CM} = 0 \end{array} \tag{5.20}$$

As the order of the circuits is high and the resulting equations are large, only some of the results are presented here in graphical form, so that an intuitive understanding of the impact of parasitic elements can be drawn out of the analysis.

From Figure 5.5 to Figure 5.8 it is clear that parasitic elements may have a major impact in the noise separation performance. Magnetic coupling k must be very high as shown in Figure 5.5 and Figure 5.6, otherwise both, CM and DM, signals are highly attenuated in the high frequency range. In contrast, it is clear that the inter-winding capacitance C_{int} should be small so that CMRR is high as detailed in Figure 5.7. As seen in Figure 5.9 the inclusion of CM inductors L_{cm} at the DM outputs increases the CMRR, but might have a negative influence on the input impedances. The DMRR of the CM output is ideally infinite if there is no asymmetry in the circuit. Considering that one of the magnetizing inductances L of the transformers is unbalanced with respect to the other two, the dependency of DMRR can be observed in Figure 5.8, where it is clear that a large unbalance leads to a poorer DMRR.

5.3.4 Three-phase CM/DM Noise Separator Realization

In order to implement the three-phase CM/DM noise separator presented in the previous section the schematic in Figure 5.10 is used. The separator is specified to be used in a standard CISPR 16 CE test setup using a typical (50 μH + 5 Ω) // 50 Ω V-network LISN and applying input line-to-line voltages of 400 V / 50 Hz.

The noise separator is built with the network formed by the transformers Tr_a, Tr_b and Tr_c and the inductors L_a, L_b and L_c. Employing $R = 50\ \Omega$ ensures an equivalent resistance of the noise separator inputs to ground of 50 Ω and allows the measurement of the CM and DM noise voltages directly from the respective output ports. For measuring a differential mode noise voltage the corresponding output is connected to the

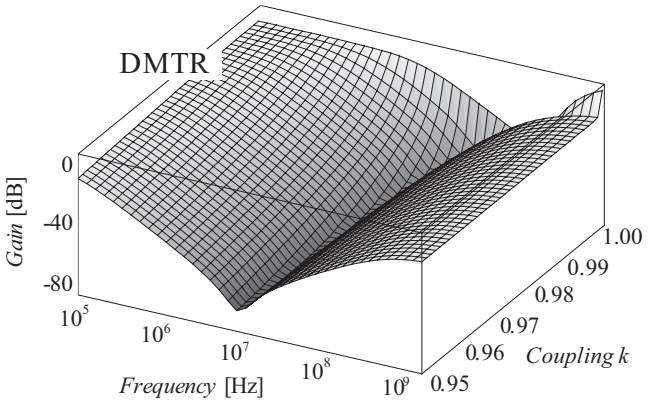


Figure 5.5: DMTR as a function of the transformers magnetic coupling showing the influence of non-idealities in the expected performance of the proposed separation network. Values if not specified: $C_p = 10$ pF, $C_{int} = 4$ pF, $L = 2$ mH, $L_{cm} = 0$, $k_{cm} = 0.99999$, $R = R_i = 50\ \Omega$.

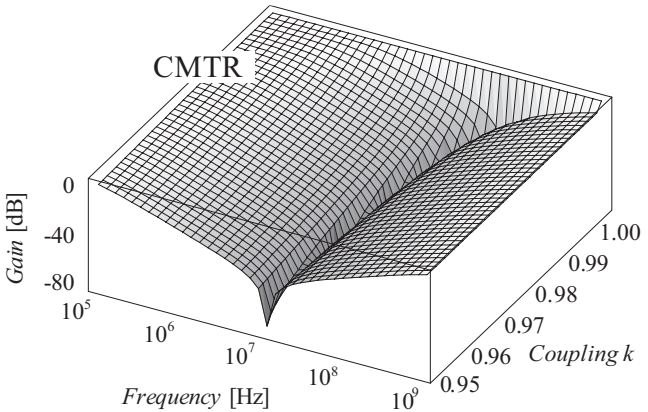


Figure 5.6: CMTR as a function of the transformers magnetic coupling showing the influence of non-idealities in the expected performance of the proposed separation network. Values if not specified: $C_p = 10$ pF, $C_{int} = 4$ pF, $L = 2$ mH, $L_{cm} = 0$, $k_{cm} = 0.99999$, $R = R_i = 50\ \Omega$.

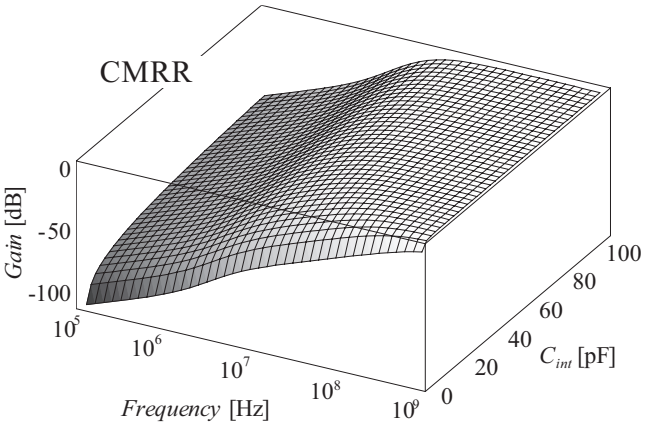


Figure 5.7: CMRR as a function of the inter-winding capacitance showing the influence of non-idealities in the expected performance of the proposed separation network. Values if not specified: $C_p = 10$ pF, $L = 2$ mH, $k = 0.9999$, $L_{cm} = 0$, $k_{cm} = 0.99999$, $R = R_i = 50\ \Omega$.

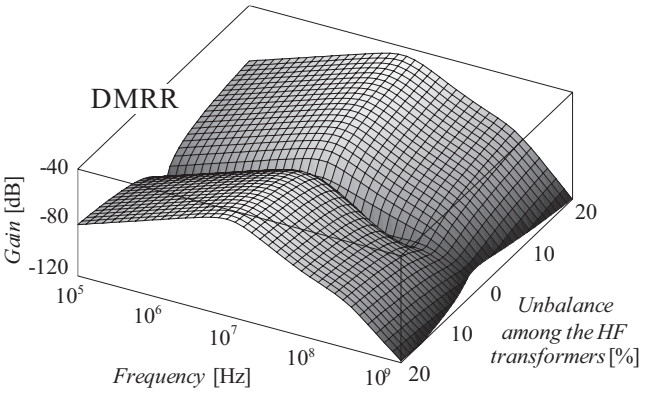


Figure 5.8: Dependency of the DMRR on the unbalance between one transformer magnetizing inductance and the other two in percent. Values used in the calculation: $C_p = 10$ pF, $C_{int} = 4$ pF, $L = 2$ mH, $k = 0.9999$, $L_{cm} = 0$, $k_{cm} = 0.99999$, $R = R_i = 50\ \Omega$.

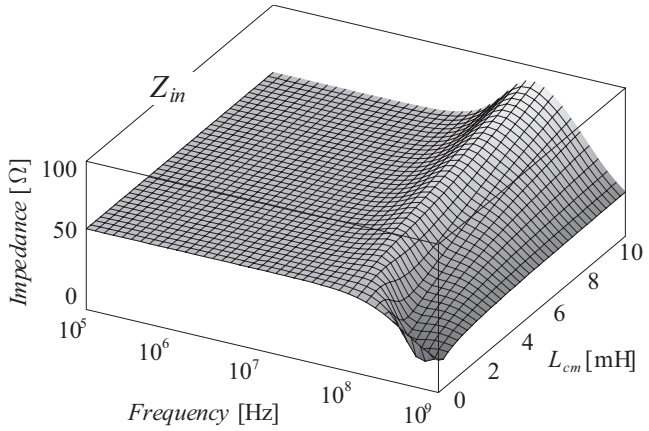


Figure 5.9: Input impedance as a function of the output CM inductance showing the influence of non-idealities in the expected performance of the proposed separation network. Values employed in the calculation: $C_p = 10$ pF, $C_{int} = 4$ pF, $L = 2$ mH, $k = 0.9999$, $L_{cm} = 0$, $k_{cm} = 0.99999$, $R = R_i = 50\ \Omega$.

input of the test receiver (input impedance of 50 Ω) after removing the explicit resistive termination.

Considering parasitic coupling capacitances of the transformers the measurement with reference to ground causes an asymmetry of the circuit which could result in a transformation of CM into DM noise. In order to achieve a higher common mode rejection ratio (CMRR), therefore common mode inductors L_a, L_b and L_c, ensuring equal impedances of the transformer output terminals against ground for high frequencies, are inserted into the differential mode outputs. A photo of a first practical realization of the three-phase CM/DM noise separator is shown in Figure 5.11.

In order to construct the transformers in the separator some requirements must be fulfilled, namely: the 50 Hz component present in the LISN output and the maximum CM signal levels should not cause the saturation of the core; leakage inductance must be small in order not to influence the gains; primary to secondary capacitance values should also be as small as possible in order to prevent CM paths to the secondary; good coupling should be guaranteed for low and high frequencies. Aiming for these

characteristics the material VITROPERM 500 F from Vacuumschmelze GmbH (VAC) was chosen, presenting a high maximum saturation flux density ($B_{\max} \cong 1.2$ T) and good high frequency characteristics. The CM chokes in the separator prototype are built with the same core material as the transformers using a smaller core (VAC 12.5x10x5-T6000-6-L2012-W498), and presenting a CM inductance around 1 mH. The transformer is built with a VAC 25x16x10-T6000-6-L2025-W380 core with 10:10 turns of twisted insulated wires. Figure 5.12 shows a calculation result for the flux density in the core for the designed transformers Tr_a, Tr_b and Tr_c when the LISN is feeding a three-phase rectifier supplying 5 kW and switching at 20 kHz. Considering only the mains frequency and a typical LISN having a coupling capacitor of $C_{coup} = 250$ nF from the power line to the test receiver input impedance $R_{in} = 50\ \Omega$ the input voltage at the LISN output terminal $V_{out,LISNpk}$ is given by

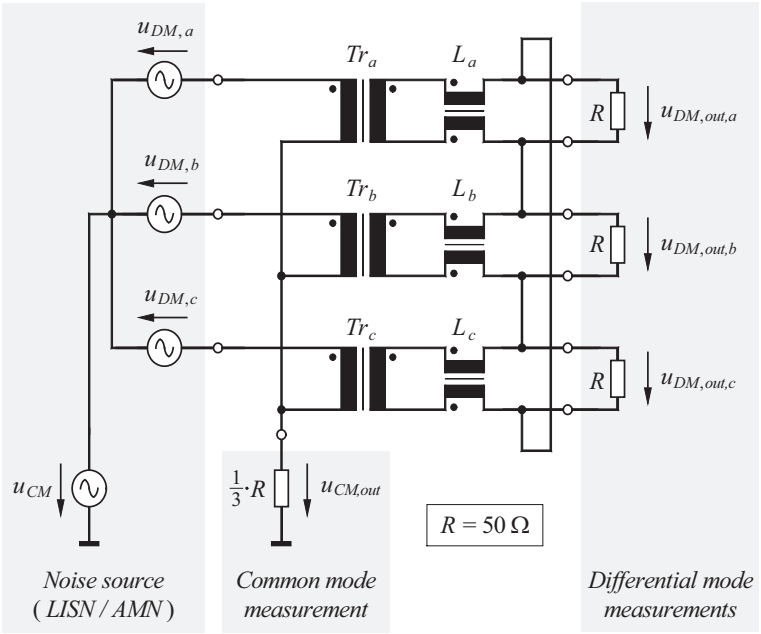


Figure 5.10: Circuit schematic of the three-phase CM/DM noise separator.

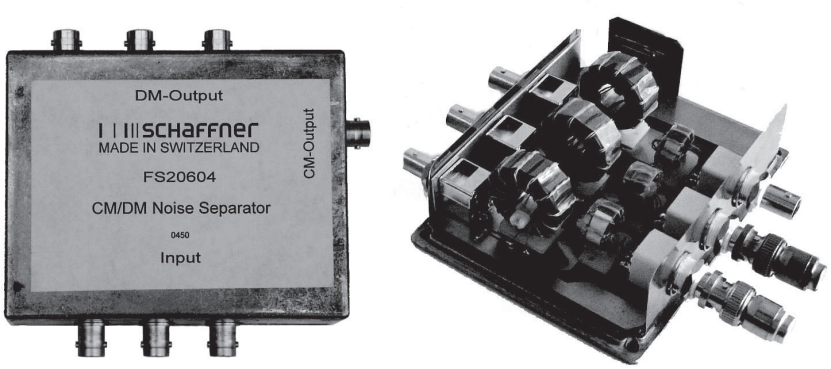


Figure 5.11: Three-phase CM/DM separator prototype photograph. Overall dimensions: 12.0x9.5x5.7 cm (4.75x3.75x2.25 in.).

$$V_{out,LISN,pk} = V_{mains,pk} \frac{R_{in}}{\sqrt{R_{in}^2 + (\frac{1}{2\pi f_{mains} C_{coup}})^2}} \tag{5.21}$$

$$= \sqrt{2}\,220\,\mathrm{V} \frac{50\,\Omega}{\sqrt{50\,\Omega^2 + (\frac{1}{2\pi 50250\,\mathrm{nF}})^2}} \cong 1.02\,\mathrm{V}. \tag{5.22}$$

The LISN employed in the CE tests has a built-in attenuator of 20 dB, leading to a gain of $G_{att} = 1/10$ times. Therefore, for the mains frequency the expected peak phase voltage $V_{in,SEP,pk}$ at the input of the noise separator is

$$V_{in,SEP,pk} = \frac{V_{out,LISN,pk}}{10} \cong 102\,\mathrm{mV}. \tag{5.23}$$

For applying the separator, a three- or four-line LISN must allow simultaneous access to all three-phase output ports. In case this is not possible, three individual single-phase LISNs could be employed. All asymmetries presented in the test circuit composed of the LISN and the noise separator will influence the measurements, especially in the higher frequency range and should be avoided.

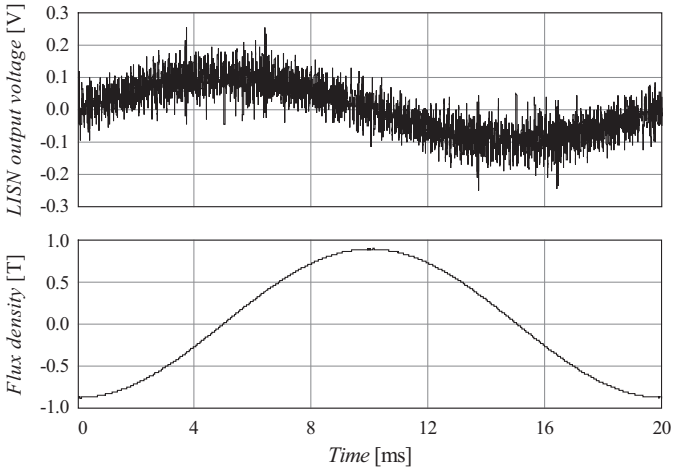


Figure 5.12: Calculated flux density in the designed transformers Tr_a, Tr_b and Tr_c, for a simulated LISN output voltage when feeding a three-phase 5 kW rectifier.

5.3.5 Experimental Evaluation

Some of the frequency response characteristics of the prototype were measured with an impedance and a network analyzer in order to evaluate the design. These measurements were performed with 50 Ω input and output impedances employing the test setups shown in Figure 5.13.

As the noise separator is intended to discriminate common and differential modes it is important to check how good the attenuation of the other noise components is, for instance, when measuring a CM signal the influence of the DM channels is needed to be known. This can be evaluated through the measurement of the differential mode rejection ratio (DMRR) of all channels and of the common mode rejection ratio (CMRR) for the DM channels. The DMRRs of the CM port are shown in Figure 5.14 and for all cases it is higher than 70 dB at 150 kHz and higher than 25 dB up to 30 MHz. These are considered to be acceptable numbers to guarantee the noise separation and are comparable with DMRR of typical measurement equipments with this bandwidth. For the measurements of DMRR and DMTR, the employed setup uses a HF transformer which presents

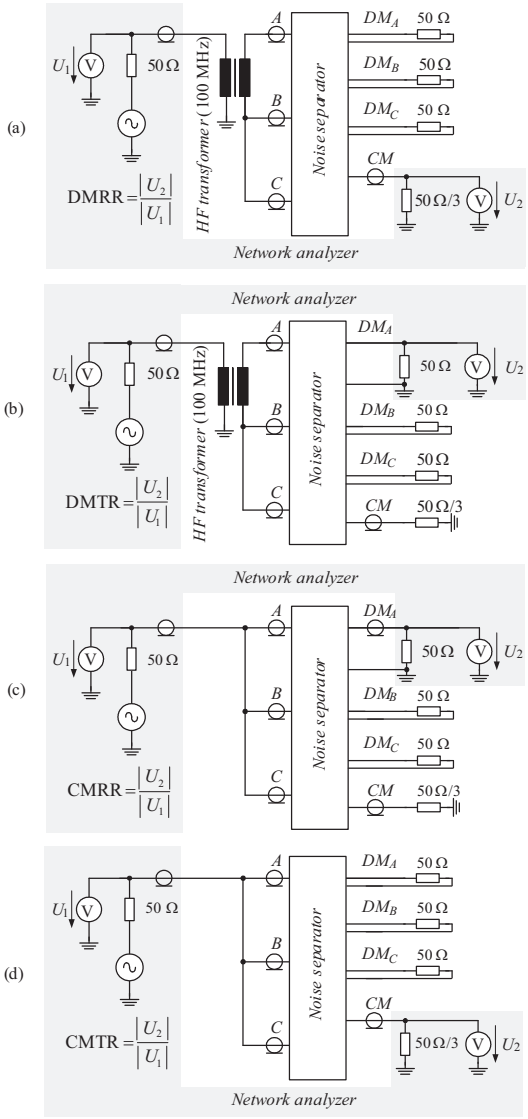


Figure 5.13: Setups used to measure: (a) DMRR – differential mode rejection ratio; (b) DMTR – differential mode transmission ratio; (c) CMRR – common mode rejection ratio, and; (d) CMTR – common mode transmission ratio.

a inter-windings capacitance of approximately 4 pF. The effects of such small capacitances generating CM currents are only to be appreciable for frequencies higher than 300 MHz, therefore, no special HF transformer connection has been employed. Furthermore, this type oof setup is common practice in the filter industry.

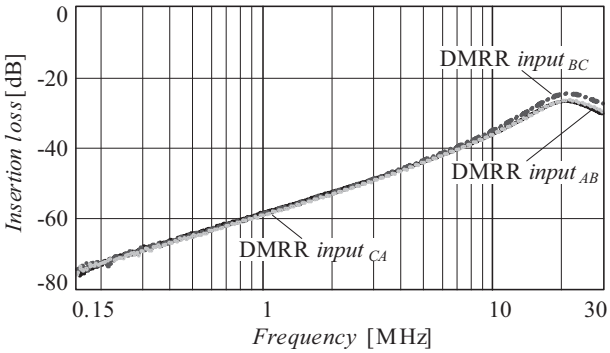


Figure 5.14: DMRR – differential mode rejection ratio.

The DMTR curves for the three DM channels are quite similar and only one is presented in Figure 5.15, where the presented -3 dB cutoff frequency is higher than 20 MHz and good symmetry amongst the channels is observed. The flat insertion loss of around -3.5 dB $\cong 2/3$ is due to the measurement setup, from where it is seen that the input voltage U_1 is applied as a line-to-line voltage and the output voltage U_2 is sensed as a phase voltage. This curves could also have been measured with the circuit of Figure 6.23.

The measured common mode rejection ratio for each of the DM output ports is presented in Figure 5.16 showing a rejection of around 50 dB in the lower frequency range and decreasing with frequency, measured around 20 dB at 10 MHz. The observed asymmetries are due to the measurement layout in combination with the layout of the prototype. Different lengths are observed, which lead to a higher CMRR in channel B. This channel is placed in the center of the printed circuit board and, therefore, presents higher symmetry. The measured asymmetries can be reduced by improving layout and test setup. Nevertheless, employing channel B for the measurements lead to reasonable results when considered that CMRR in the range of 30 dB is observed at 30 MHz.

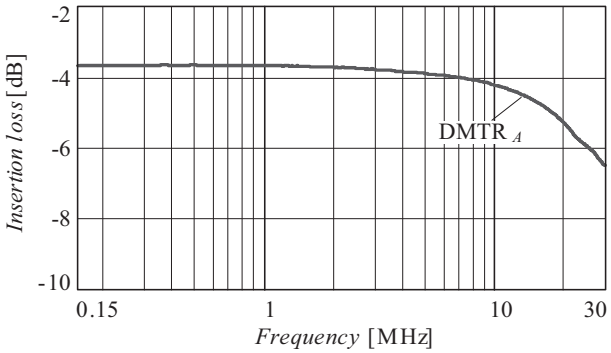


Figure 5.15: DMTR – differential mode transmission ratio.

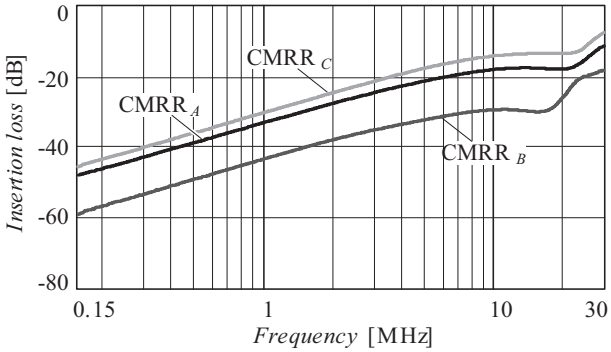


Figure 5.16: CMRR – common mode rejection ratio.

In Figure 5.17 the insertion loss between the measured CM output voltage and a CM input signal (CMTR) is plotted and a flat band up to more than 20 MHz is observed. The flat insertion loss of around -6 dB $\cong$ 1/2 is due to the measurement setup, from where it is seen that the input voltage U_1 is applied as a CM voltage and the output voltage U_2 is also sensed as a CM voltage. This flat band is enough to successfully measure CM emissions. Furthermore, modern test receivers have the built-in capability of compensating for attenuation by programming the attenuation characteristics of the interfacing device.

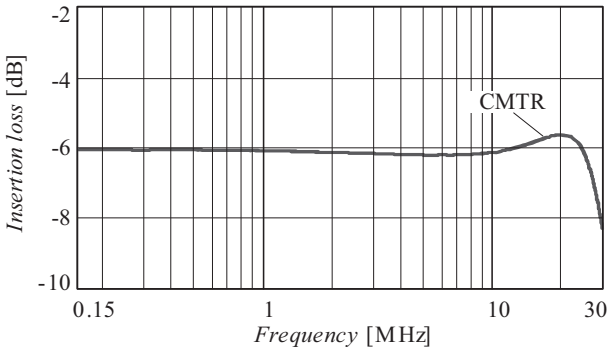


Figure 5.17: CMTR – common mode transmission ratio.

The non-idealities of the circuit also lead to imperfect input impedances, which increase with increasing frequencies leading to higher measurement results in the frequency range above 10 MHz. The impedance measured from input ports (connected together) to PE is shown in Figure 5.18, where it is seen that the input common mode impedance of the terminated separator is close to the ideal impedance, but significantly increases beyond 10 MHz. The same occurs with the measured input differential mode impedance, which is depicted in Figure 5.19).

The measured frequency characteristics show that the noise separation network performs its task very well in the frequency range up to 10 MHz. However, a better performance for higher frequencies (10 MHz $< f <$ 30 MHz) is desirable. Rejection ratios in the order of 30 dB at 30 MHz would guarantee a clear separation of the noise modes for most of the application. This could be achieved in a new implementation with a more symmetrical layout and components with improved HF performance.

Conducted emission measurements as specified in CISPR 16 were performed utilizing a setup as shown in Figure 5.20 in order to give an example for the use of the three-phase CM/DM separator. The EUT was a regenerative drive feeding a 10 kVA motor. The test conditions were as follows: input line voltages $U_{in} = 400$ V / 50 Hz; output power $P_{out} = 5$ kW. The LISN conforms with CISPR 16, is constructed to operate from 2 kHz to 30 MHz and is presented in detail in [205]. The access to all output

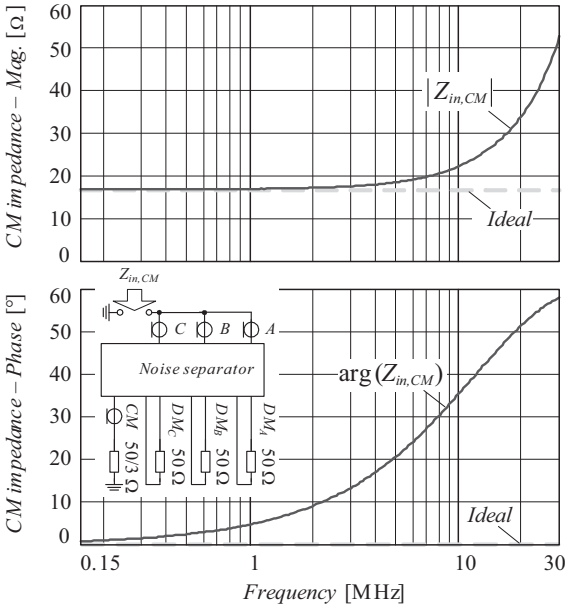


Figure 5.18: Input impedance measured from input ports (connected together) to PE. Ideal values are shown in dashed lines.

ports is available, thus guaranteeing that the three-phase CM/DM noise separator can be used.

The following conducted emission measurement results shows the acquired data for three measurements performed within the same operating conditions, one without the noise separator a second showing the measured DM emission levels sensed with the noise separator and the last presenting the measured DM emission levels.

Figure 5.21 shows the measured conducted emission levels without the noise separator. Measured emission levels sensed in one of the DM channels with the presented separation network are presented in Figure 5.22. The measurement results depicted in Figure 5.23 show the measurements performed in the CM output port. In the present CE measurement results, the upper curves show measurements performed with the quasi-peak peak detector, while the lower curves employ the average detector in the measurements as specified in CSIPR 16.

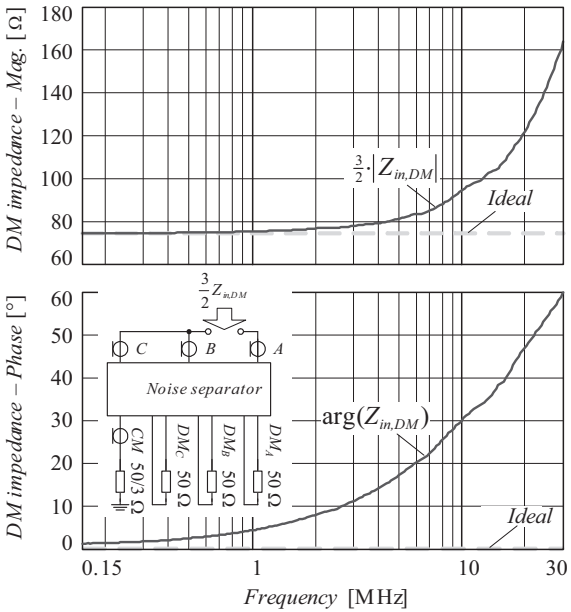


Figure 5.19: Input impedance measured between one input port and the other two ports connected together. Ideal values are shown in dashed lines.

From the measurements one can see that there is a large difference between the levels of DM and CM emissions in the lower frequency range with the DM emissions being much higher than the CM ones up to 5 MHz. This indicates the necessity of higher DM attenuation at this frequency range. It also shows how much attenuation is required and this allows an appropriate filter to be designed.

With this example, the main purpose of the three-phase CM/DM separation network, that is acquiring information for filter designs and troubleshooting of power converters, is proved through experimental results, thus confirming the theoretical analysis. It is also observed that there is still room for improvements of the rejection ratios and input impedances, which can be accomplished by employing transformer with low leakage inductance and a very symmetrical layout.

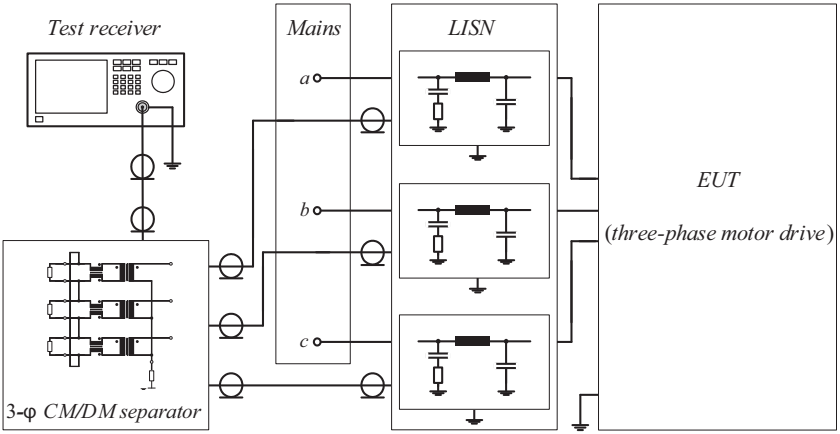


Figure 5.20: Test setup for the conducted emission measurements using the proposed three-phase CM/DM noise separation passive network.

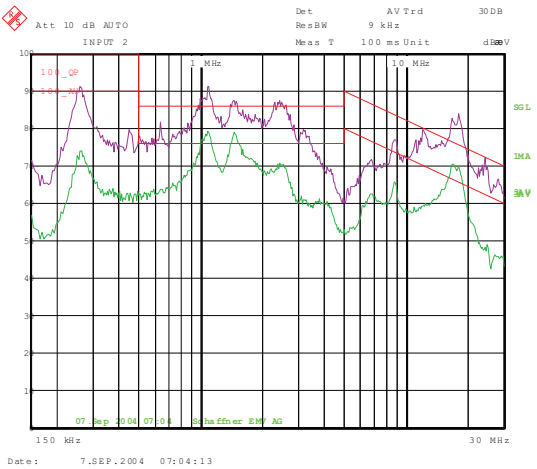


Figure 5.21: Conducted emission measurements applying directly a LISN. Axes: 0 to 100 dBμV and 150 kHz to 30 MHz.

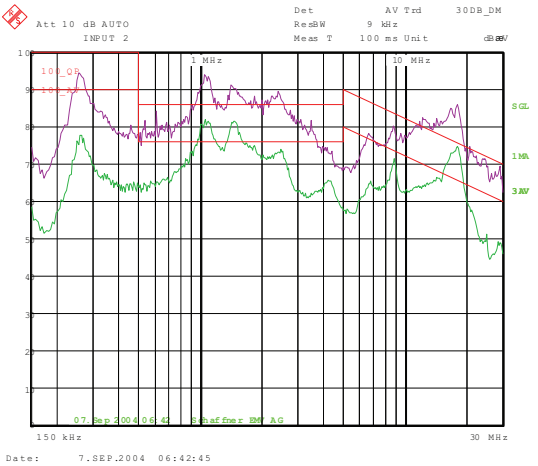


Figure 5.22: Conducted emission measurements performed in one noise separator DM output port. Axes: 0 to 100 dBμV and 150 kHz to 30 MHz.

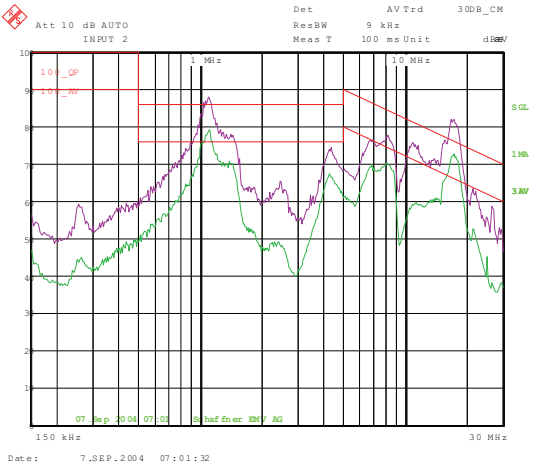


Figure 5.23: Conducted emission measurements from the noise separator CM output port. Axes: 0 to 100 dBμV and 150 kHz to 30 MHz.

5.4 Three-Phase CM/DM Noise Separator Based on Operational Amplifiers

The circuit of Figure 5.24 uses active circuit elements (operational amplifiers) in order to implement a separation network, which can effectively separate common- and differential-mode signals from the three input terminals, while presenting constant and controlled input impedances to PE of value R. The DM signals can be sensed at the output terminals DM_a, DM_b and DM_c and the CM components are available at output CM.

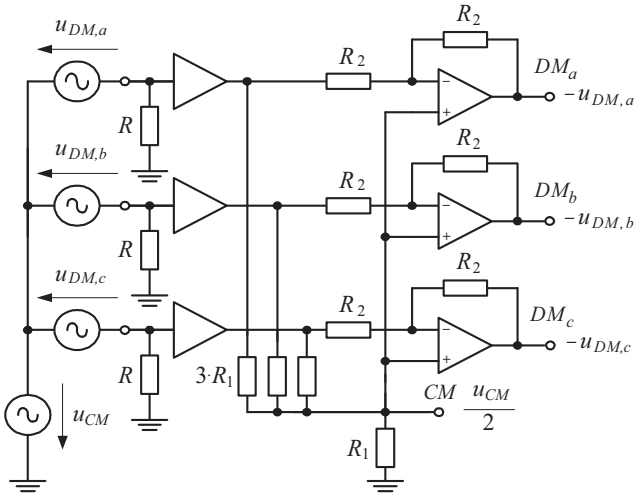


Figure 5.24: Three-phase CM/DM noise separator proposals for an active solution.

This network makes use of active circuits, thus, would require amplifiers with very large bandwidths (BW) and power supply rejection ratios (PSRR). Besides that, the active solution would require the design of a suitable amplifier power supply with isolation, thus elevating the production costs. However, this active solution is prone to provide well defined input impedances and a good control of the insertion loss allowing required adjustments to be done easily.

For the aforementioned reasons and for the sake of brevity, the analysis for the active solution is omitted and a practical implementation has not

been planned.

5.5 Three-Phase CM/DM Noise Separators Based on Transmission Line Transformers

Networks are proposed in this section, which allow for the separate assessment of CM and DM conducted emission levels and which can be integrated into a typical three-phase CE measurement system. These networks are based on transmission line transformers, thus high performance for HF is to be expected, as well as good impedance matching in order to fulfill strict impedance requirements, such as in CISPR 16. With the use of TLTs, transverse electro-magnetic (TEM) energy transfer mode is considered and small cores are utilized.

5.5.1 Three-Phase Separation Networks Based on Transmission Line Transformers

Transmission Line Transformers (TLT) are know as providing high performance in signal transmission in a wide frequency range, since the parasitic elements of the transformers are employed actively in the process and do not represent drawbacks [206, 207]. CE measurements are typically performed from 9 kHz to 30 MHz, but even 50 Hz components are to be handled by the circuit elements of a noise separator. Besides that, CE measurement standards specify input impedances, which should also be well controlled in the whole frequency range. This context makes it difficult to keep all non-idealities under control for a separator built with conventional HF transformers. Based on these facts, a CM/DM separator based on transmission line transformers for single-phase systems is successfully introduced in [208].

Novel separation networks for three-phase CE measurement systems based on TLTs are presented in the following, where each of the networks employs only three TLTs and resistors.

The network of Figure 5.25 is capable of sensing only the CM portion of signals applied to ports A, B and C, in its output u_{CM}, therefore it is hereafter named CM separator.

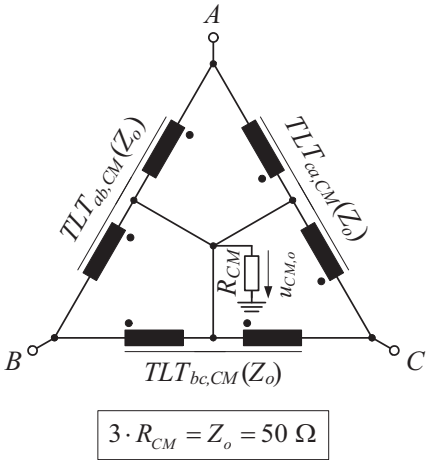


Figure 5.25: Proposed CM three-phase separation network based on TLTs.

The outputs $u_{DM,AB}$, $u_{DM,BC}$ and $u_{DM,CA}$ of the circuit presented in Figure 5.26 sense the DM line-to-line voltages of the signals applied to A, B and C. Whereas, the circuit of Figure 5.27 is ideally able to separate the DM phase-to-ground voltages in its outputs $u_{DM,A}$, $u_{DM,B}$ and $u_{DM,C}$.

The network of Figure 5.26 is used to explain the basic operating principle for the networks. Considering only $TLT_{ca,DM}$, it is assumed that: (*i*) there is no coupling between different TLTs and also not between a TLT and the signal ground; (*ii*) that the network is balanced, and; (*iii*) that the frequencies under consideration are much lower than the first resonance of the TLTs. If a signal is applied from C to A and the characteristic impedance of $TLT_{ca,DM}$ matches with the one from the load R_{DM}, it is known [24, 206] that the DM portion of this signal is transmitted to the output $u_{DM,CA}$ with a unitary gain and the CM components are suppressed on the outputs of this network. In addition, the input impedance seen from ports C to A is equal to the characteristic impedance Z_o. A comprehensive analysis for the other networks is not so evident and is given on the following.

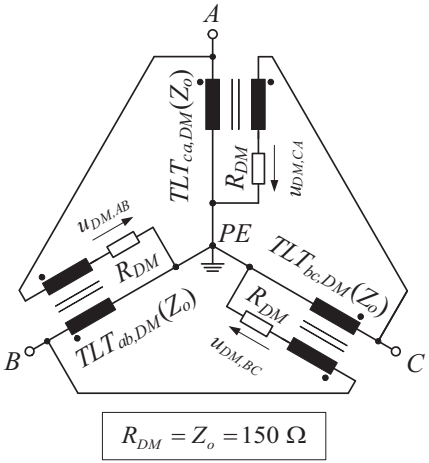


Figure 5.26: Proposed DM three-phase separation network based on TLTs and on the measurement of line voltages.

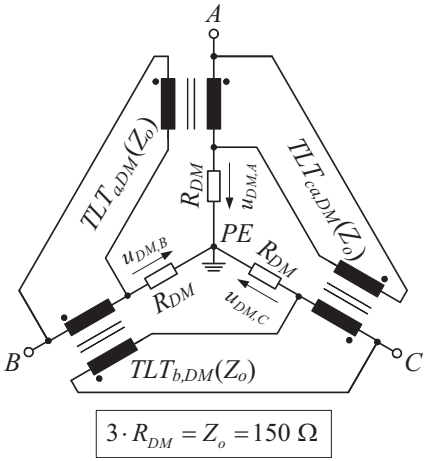


Figure 5.27: Proposed DM three-phase separation network based on TLTs and on the measurement of phase voltages.

Ideal Transfer Functions

Considering an idealized lossless transmission line, with voltages and currents as shown in Figure 5.28, inductance per unit length L_o, capacitance per unit length C_o and length l, the two-port network is characterized by,

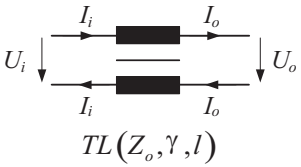


Figure 5.28: Definitions of voltages and currents for a lossless transmission line.

$$\begin{bmatrix} u_i \\ i_i \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_o \sinh(\gamma l) \\ \sinh(\gamma l)/Z_o & \cosh(\gamma l) \end{bmatrix} \cdot \begin{bmatrix} u_o \\ i_o \end{bmatrix}, \tag{5.24}$$

with,

$$Z_o = \sqrt{L_o/C_o} \tag{5.25}$$

$$\gamma = j\,2\pi f \sqrt{L_o C_o}. \tag{5.26}$$

The result from equation eq. (5.24) is obtained based on the assumption that the currents in the output terminals are equal in magnitude as shown in Figure 5.28 and this simplifies the analysis of the relevant transfer functions, which is carried out. The networks are redrawn in Figure 5.29 with the inclusion of three DM voltage sources u_i ($i = a, b, c$) and one CM source u_{CM}.

The most relevant transfer functions are defined as: (*i*) differential mode transmission ratio – DMTR (eq. (5.27)); (*ii*) common mode transmission ratio – CMTR (cf. eq. (5.28)); (*iii*) differential mode rejection ratio – DMRR (eq. (5.29)); (*iv*) common mode rejection ratio – CMRR (eq. (5.30)). Ideally, the transmission ratios should be unitary and the rejection ratios should approach infinity.

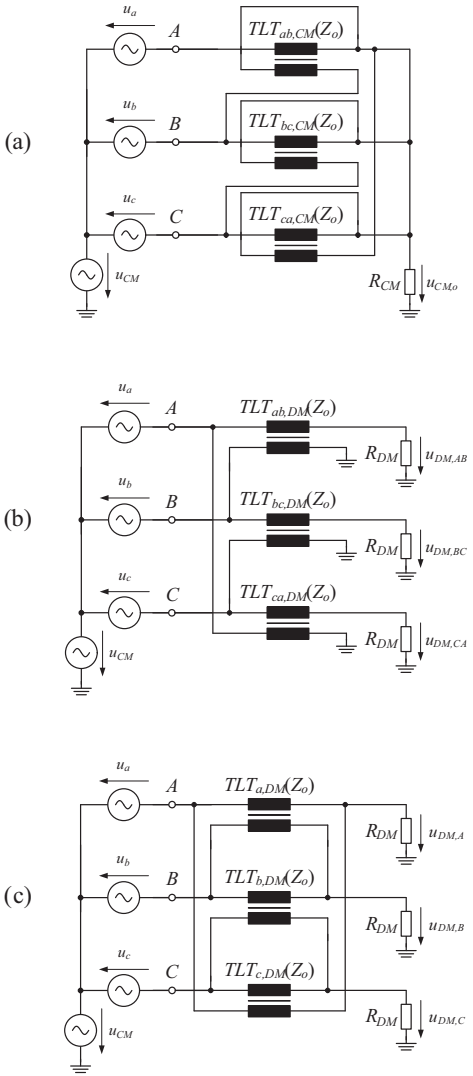


Figure 5.29: Networks utilized to perform the analytical analysis of discrimination of CM and DM voltages: (a) CM separator; (b) DM separator based on the measurement of line voltages, and; (c) DM separator based on the measurement of phase voltages.

$$\text{DMTR} = \left.\frac{u_{DM,out}}{u_a}\right|_{u_{CM}=0 \text{ and } u_a+u_b+u_c=0} \tag{5.27}$$

$$\text{CMTR} = \left.\frac{u_{CM,out}}{u_{CM}}\right|_{u_a+u_b+u_c=0} \tag{5.28}$$

$$\text{DMRR} = \left.\frac{u_{CM,out}}{u_a}\right|_{u_{CM}=0 \text{ and } u_a+u_b+u_c=0} \tag{5.29}$$

$$\text{CMRR} = \left.\frac{u_{DM,out}}{u_{CM}}\right|_{u_a+u_b+u_c=0} \tag{5.30}$$

Solving the circuit of Figure 5.29(a), for the CM separator, the main transfer functions are:

$$\text{CMTR}_{CM} = \frac{6R_{CM}\left[1+\cosh(\gamma l)\right]}{6R_{CM}\left[1+\cosh(\gamma l)\right] - Z_o \sinh(\gamma l)}, \tag{5.31}$$

and,

$$\text{DMRR}_{CM} \rightarrow -\infty. \tag{5.32}$$

From eq. (5.31) it is seen that $\text{CMTR}_{CM} \rightarrow 1$, if $R_{CM} = Zo/3$ and $f << j/(\gamma l)$. Therefore the CM separator ideally fulfills the requirements.

Deriving the transfer functions for the DM separator shown in Figure 5.29(b), leads to:

$$\text{DMTR}_{DM,line} = \frac{\sqrt{3}R_{DM}}{Z_o \sinh(\gamma l) - R_{DM}\cosh(\gamma l)}, \tag{5.33}$$

and,

$$\text{CMRR}_{DM,line} \rightarrow -\infty. \tag{5.34}$$

Following the same procedure for the DM separator for phase voltages shown in Figure 5.29(c):

$$\text{DMTR}_{DM,phase} = \frac{3R_{DM}}{3R_{DM}\cosh(\gamma l) - Z_o \sinh(\gamma l)}, \tag{5.35}$$

and,

$$\mathrm{CMRR}_{DM,phase} \to -\infty. \tag{5.36}$$

From eq. (5.34) and eq. (5.36) it is clear that both DM separators present ideally very high CMRR. The DMRR for the DM separator for line voltages $\mathrm{DMTR}_{DM,line}$ is approximately $\sqrt{3}$ if $R_{DM} = Z_o$, meaning that the line-to-line voltages are effectively sensed at the outputs of this network. Whereas, for the DM separator for phase voltages the $\mathrm{DMTR}_{DM,phase}$ approaches unity if $R_{DM} = Z_o/3$.

Ideal Input Impedances

Using the result of equation eq. (5.24) to solve the circuits depicted in Figure 5.30, Figure 5.31 and Figure 5.32 the input impedances for the relevant noise modes is derived.

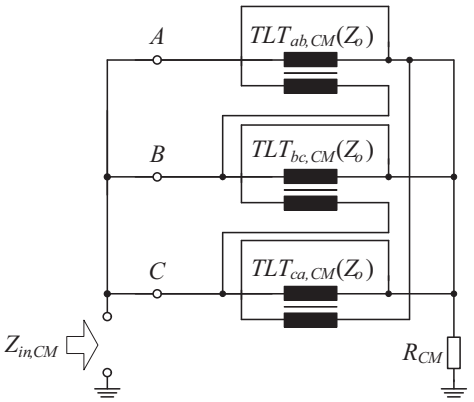


Figure 5.30: Separation network utilized to perform the derivation of the input impedances for CM and DM for the CM separator.

For the CM separator (cf. Figure 5.30), the CM input impedance is given by:

$$\mathrm{Z}_{in,CM} = \frac{1}{6} \cdot \frac{6R_{CM}\left[1 + \cosh(\gamma l)\right] - Z_o \sinh(\gamma l)}{1 + \cosh(\gamma l)}. \tag{5.37}$$

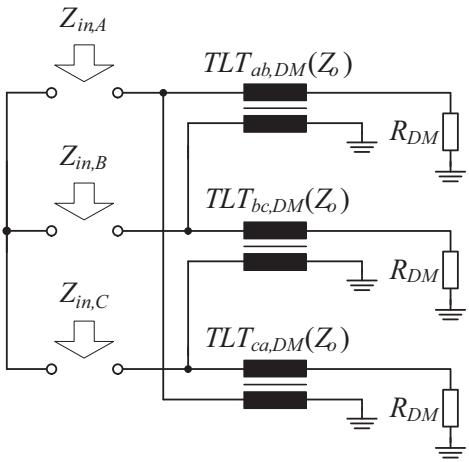


Figure 5.31: Separation network utilized to perform the derivation of the input impedances for CM and DM for the DM separator based on the measurement of line voltages. The three impedances can be solved for simultaneously and are equal if the TL transformers are balanced.

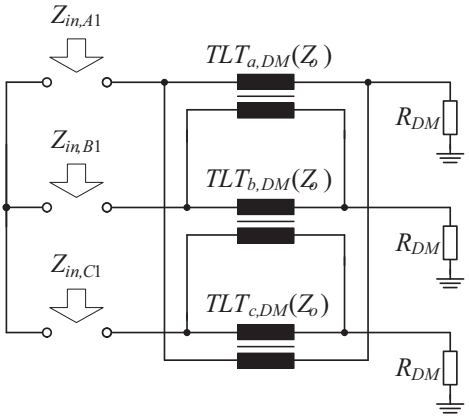


Figure 5.32: Separation network utilized to perform the derivation of the input impedances for CM and DM for the DM separator based on the measurement of phase voltages. The three impedances can be solved for simultaneously and are equal if the TL transformers are balanced.

The DM separator for line voltages (cf. Figure 5.31) presents the following DM input impedances:

$$\mathrm{Z}_{in,A} = \mathrm{Z}_{in,B} = \mathrm{Z}_{in,C} = \frac{Z_o}{3} \cdot \frac{Z_o \sinh(\gamma l) - R_{DM} \cosh(\gamma l)}{Z_o \cosh(\gamma l) - R_{DM} \sinh(\gamma l)}. \tag{5.38}$$

Finally, the DM input impedances for the DM separator for phase voltages (cf. Figure 5.32) are

$$\mathrm{Z}_{in,A1} = \mathrm{Z}_{in,B1} = \mathrm{Z}_{in,C1} = \frac{Z_o}{3} \cdot \frac{3R_{DM} \cosh(\gamma l) - Z_o \sinh(\gamma l)}{3R_{DM} \sinh(\gamma l) - Z_o \cosh(\gamma l)}. \tag{5.39}$$

Table 5.1 summarizes the ideal input impedances for the different separation networks based on the matching condition of load resistance and the characteristic impedances of the transmission line transformers.

Table 5.1: Ideal input impedances.

Input impedances	*Condition*	*Derived value*
$Z_{in,CM}$	$3\,R_{CM} = Z_o$	R_{CM}
$Z_{in,A}$, $Z_{in,B}$, $Z_{in,C}$	$R_{DM} = Z_o$	$R_{DM}/3$
$Z_{in,A1}$, $Z_{in,B1}$, $Z_{in,C1}$	$3\,R_{DM} = Z_o$	R_{DM}

Low Frequency Behavior of the DM Separator for Phase Voltages

The results obtained in the previous sections do not completely define the low frequency behavior of the DM separator for phase voltages, shown in Figure 5.29(c) as only the transmission line behavior. i.e. transverse electromagnetic mode is considered. Currents of CM nature, called even-mode currents [207], circulate from the source voltages to the load resistances reducing the CMRR of the network. These CM currents are only limited by the total even-mode impedance, which is given by the parallel

connection of the inductive impedance of the TLTs.

By using a low frequency equivalent circuit, where the transformers are modeled with a first order model only including their magnetizing L_{total} and mutual M_{total} inductances the CMRR is calculated as,

$$\mathrm{CMTR}_{DM,phase} = \frac{2R_{DM}}{2R_{DM} + j\,2\pi f(L_{total} + M_{total})}. \tag{5.40}$$

From eq. (5.40) it can be seen that the low frequency total inductance of the TLTs must be high in order to obtain high CMRR for low frequencies. Therefore, larger cores shall be employed if this network is used. For this reason this separator is not included in the following sections.

5.5.2 Performance under Non-Ideal Conditions

The analysis performed in section 5.5.1 results from the assumption that the line is treated as a two-port device and the impedances are all perfectly balanced. A more general solution is achieved by independently considering the currents and voltages in the four terminals of the transmission lines as presented in the following.

A solution for a two-conductor transmission line (cf. Figure 5.33) is here derived, which is used for the analysis of non-ideal behavior for the proposed separation networks.

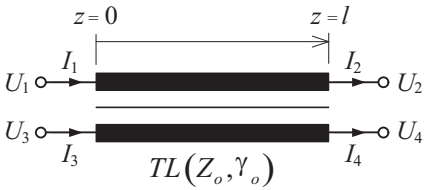


Figure 5.33: Analyzed circuit for a two-conductor transmission line.

Considering the circuit of Figure 5.34 and assuming that the voltages and currents are written in the Laplace domain, the following system of ordinary differential equations is obtained

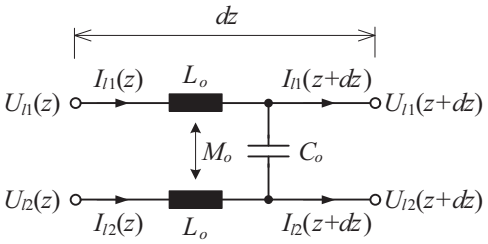


Figure 5.34: Per unit length equivalent circuit for a two-conductor transmission line.

$$\frac{\partial}{\partial z}\begin{bmatrix} U_{l1}(z) \\ U_{l2}(z) \end{bmatrix} = -s \begin{bmatrix} L_o & M_o \\ M_o & L_o \end{bmatrix} \cdot \begin{bmatrix} I_{l1}(z) \\ I_{l2}(z) \end{bmatrix}, \tag{5.41}$$

$$\frac{\partial}{\partial z}\begin{bmatrix} I_{l1}(z) \\ I_{l2}(z) \end{bmatrix} = -s \begin{bmatrix} C_o & -C_o \\ -C_o & C_o \end{bmatrix} \cdot \begin{bmatrix} U_{l1}(z) \\ U_{l2}(z) \end{bmatrix}. \tag{5.42}$$

Assuming that the currents at the beginning and at the end of the lines are,

$$\begin{aligned} I_{l1}(z=0) &= I_1 \\ I_{l1}(z=l) &= I_2 \\ I_{l2}(z=0) &= I_3 \\ I_{l2}(z=l) &= I_4, \end{aligned} \tag{5.43}$$

and that the voltages at the terminals are,

$$\begin{aligned} U_{l1}(z=0) &= U_1 \\ U_{l1}(z=l) &= U_2 \\ U_{l2}(z=0) &= U_3 \\ U_{l2}(z=l) &= U_4. \end{aligned} \tag{5.44}$$

The solution for the differential equation system is,

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} y_1 & y_2 & y_3 & y_4 \\ -y_2 & -y_1 & -y_4 & -y_3 \\ y_3 & y_4 & y_1 & y_2 \\ -y_4 & -y_3 & -y_2 & -y_1 \end{bmatrix} \cdot \begin{bmatrix} U_1 \\ U_2 \\ U_3 \\ U_4 \end{bmatrix}, \tag{5.45}$$

where,

$$y_1 = \frac{-sl\,(L_o + M_o)\,\sqrt{2C_o}\cos(\gamma_o) + \sqrt{-L_\sigma}\sin(\gamma_o)}{2sl\sqrt{L_\sigma}\,(L_o + M_o)\sin(\gamma_o)}, \tag{5.46}$$

$$y_2 = \frac{sl\,(L_o + M_o)\,\sqrt{2C_o} - \sqrt{-L_\sigma}\sin(\gamma_o)}{2sl\sqrt{L_\sigma}\,(L_o + M_o)\sin(\gamma_o)}, \tag{5.47}$$

$$y_3 = \frac{sl\,(L_o + M_o)\,\sqrt{2C_o}\cos(\gamma_o) + \sqrt{-L_\sigma}\sin(\gamma_o)}{2sl\sqrt{L_\sigma}\,(L_o + M_o)\sin(\gamma_o)}, \tag{5.48}$$

and,

$$y_4 = \frac{sl\,(L_o + M_o)\,\sqrt{2C_o} + \sqrt{-L_\sigma}\sin(\gamma_o)}{2sl\sqrt{L_\sigma}\,(L_o + M_o)\sin(\gamma_o)}, \tag{5.49}$$

with,

$$L_\sigma = L_o - M_o, \tag{5.50}$$

and,

$$\gamma_o = sl\sqrt{-2C_oL_\sigma}. \tag{5.51}$$

From this solution, it is possible to include (*i*) the low frequency behavior; (*ii*) the influence of the magnetic coupling of the TLTs; and, (*iii*) the influence of non-balanced impedances; in the performance of the separation networks.

However, the transfer functions (DMTR, CMTR, etc.) are somewhat involved if unbalanced impedances and magnetic couplings are considered. Besides that, very less insight is gained with the long equations. Therefore, for the sake of brevity these equations are not displayed here. In their place, graphs displaying the calculated curves for a given set of parameters are presented in Figure 5.35, Figure 5.36, Figure 5.37 and Fig-

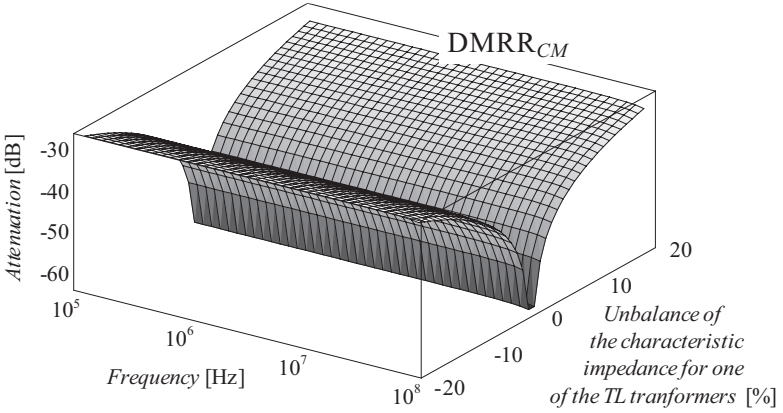


Figure 5.35: DMRR transfer function for the proposed separation networks taking into account the influence of impedance unbalance and the per unit mutual coupling of the TLTs for the CM separator as a function of frequency and unbalance of the characteristic impedance of one of the TLTs, where $R_{CM} = 50/3\ \Omega$, $L_o = 250\ \mu$H, $M_o = 0.998\, L_o$, $C_o = 145$ pF, $l = 0.2$ m.

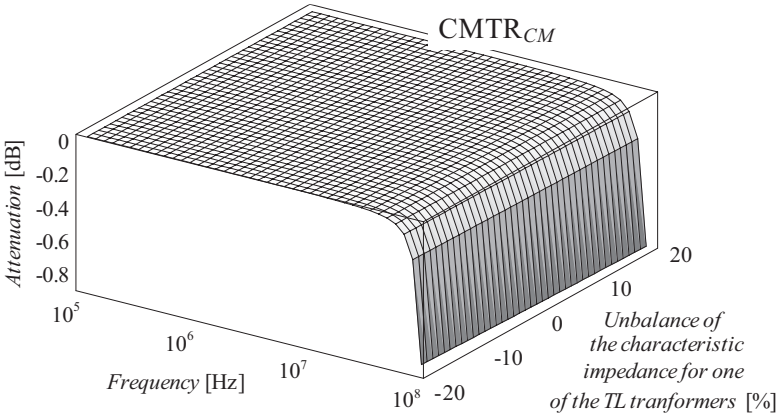


Figure 5.36: CMTR transfer function for the proposed separation networks taking into account the influence of impedance unbalance and the per unit mutual coupling of the TLTs for the CM separator as a function of frequency and unbalance of the characteristic impedance of one of the TLTs, where $R_{CM} = 50/3\ \Omega$, $L_o = 250\ \mu$H, $M_o = 0.998\, L_o$, $C_o = 145$ pF, $l = 0.2$ m.

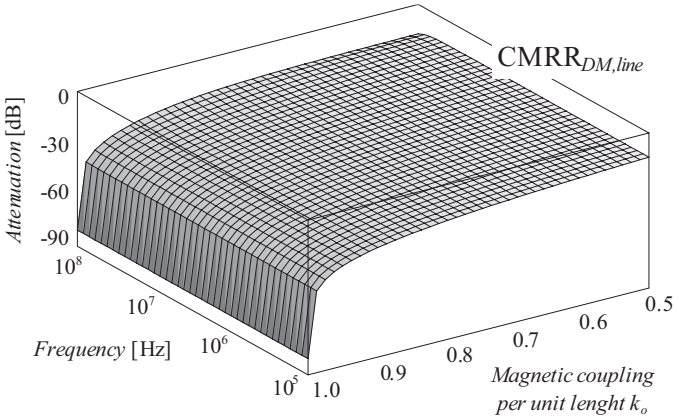


Figure 5.37: CMRR transfer function for the proposed separation networks taking into account the influence of impedance unbalance and the per unit mutual coupling of the TLTs for the DM separator for line voltages as a function of frequency and unbalance of the characteristic impedance of one of the TLTs, where $R_{DM} = 150\ \Omega$, $L_o = 542\ \mu$H, $M_o = k_o\, L_o$, $C_o = 24$ pF, $l = 0.8$ m.

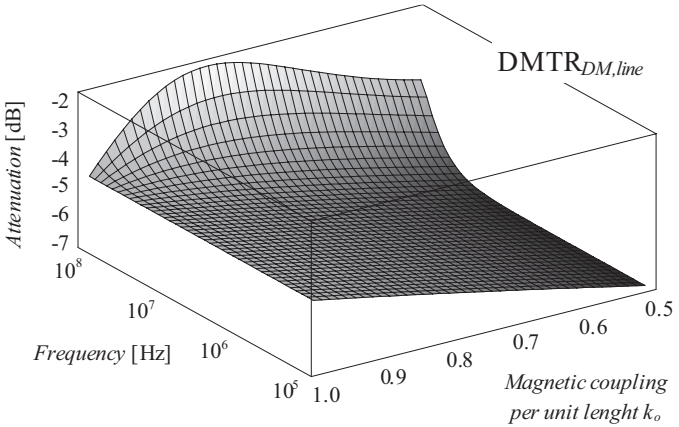


Figure 5.38: DMTR transfer function for the proposed separation networks taking into account the influence of impedance unbalance and the per unit mutual coupling of the TLTs for the DM separator for line voltages as a function of frequency and unbalance of the characteristic impedance of one of the TLTs, where $R_{DM} = 150\ \Omega$, $L_o = 542\ \mu$H, $M_o = k_o\, L_o$, $C_o = 24$ pF, $l = 0.8$ m.

ure 5.38. These plots provide valuable insight into the influence of some constructive parameters in the performance of the separation networks. It is observed that the unbalance among the TLTs affects the performance of the CM separator, while the magnetic coupling influences more the performance of the DM separator for line voltages. Typical values for the magnetic couplings are expected to be higher than $k_o > 0.985$ depending on the employed wire insulation.

5.5.3 Experimental Measurements and Performance

Aiming for the discrimination of CM and DM in three-phase CE measurements as specified in CISPR 16, prototypes were built and experimental results are presented in the following.

Transmission line transformers were built presenting characteristic impedances of 50 Ω and 150 Ω, respectively for the CM separator and for the DM separator for line voltages. The measured input impedance of one of the TLT_{CM} with a matching output resistance of 50 Ω is shown in Fig.7 along with a photograph of the built TLT. It is observed that the matching is successful and the impedance is within 10 % of its nominal value up to 60 MHz. This fulfils the requirements of CISPR 16 for the input impedance of a test receiver. The same level of performance is achieved with the TLT for the DM separator.

With the TLTs, two prototypes were built on printed circuit boards. Every trace on the PCBs had its width calculated in order to achieve the same characteristic impedances as the TLTs, therefore increasing the bandwidth of the prototypes. The input impedances for both prototypes were measured with the setups displayed in Figure 5.40 for the CM separator and in Figure 5.41 for the DM unit by using an impedance analyzer.

The input impedance measurement results are shown in Figure 5.42 for the CM separator and in Figure 5.43, where it can be seen a very good approximation between the ideal impedances and the measured ones from 150 kHz up to 30 MHz for both, CM and DM, separators.

The transfer functions were evaluated through insertion loss measurements performed with the setups presented in Figure 5.44 for the measurement of the differential mode transmission ratio for the DM separation network, Figure 5.45 for the measurement of the common mode transmission ratio for the CM separation network, Figure 5.46 for the

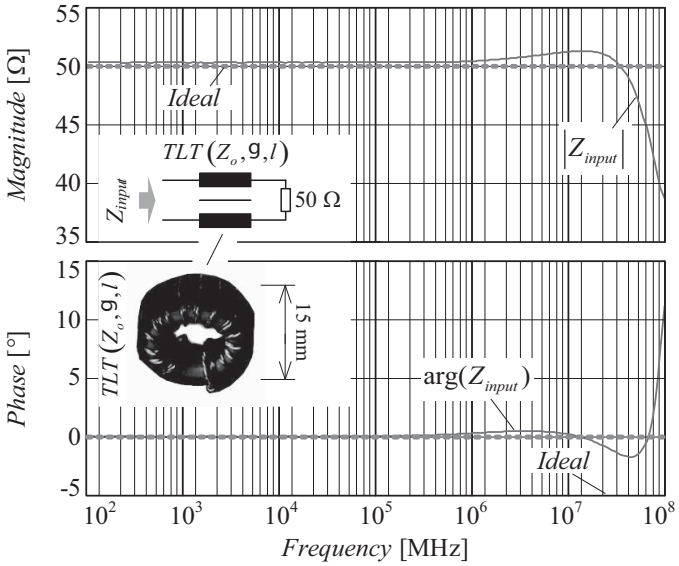


Figure 5.39: Input impedance measurement of the built TLT ($Z_o = 50\ \Omega$) when terminated with a 50 Ω SMD resistor (0805 – 1/8 W) and a photograph of the transformer with dimensions. The employed core material is Fair-Rite 43 with 16 turns of twisted magnetic wire with a diameter of 0.6 mm.

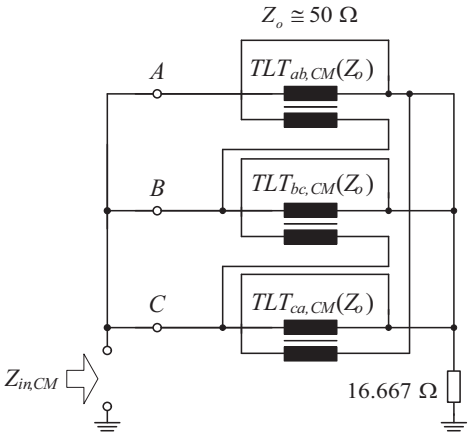


Figure 5.40: Measurement setup for the CM separator input impedance, which is measured from input ports (connected together) to PE.

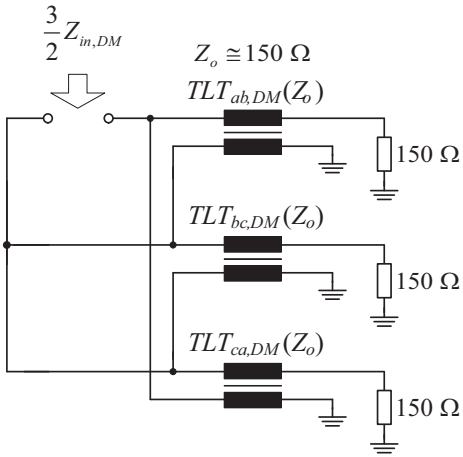


Figure 5.41: Measurement setup for the DM separator input impedance, measured between one input port and the other two ports connected together.

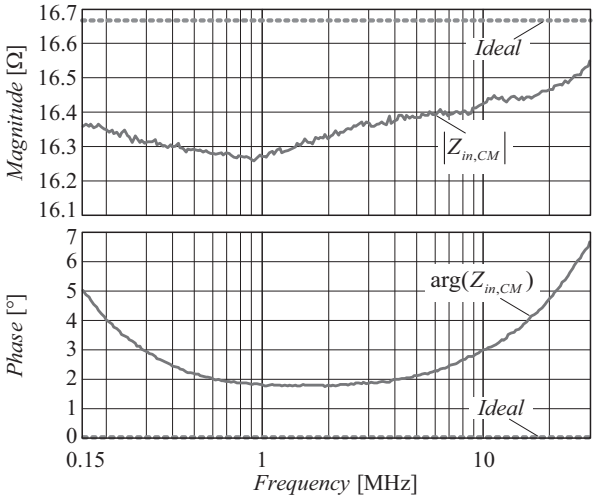


Figure 5.42: CM separator measured input impedance, measured from input ports (connected together) to PE. Ideal values are shown with dashed lines.

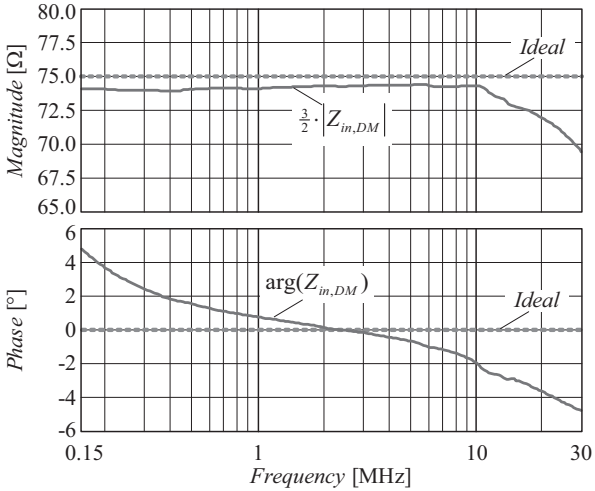


Figure 5.43: DM separator measured input impedance, measured between one input port and the other two ports connected together. Ideal values are shown with dashed lines.

measurement of the common mode rejection ratio for the DM separation network and Figure 5.47 for the measurement of the differential mode rejection ratio for the CM separation network. For the measurements of DMTR and DMRR a high frequency transformer with a bandwidth of 100 MHz was employed to isolate the ground connection of the netwrok analyzer.

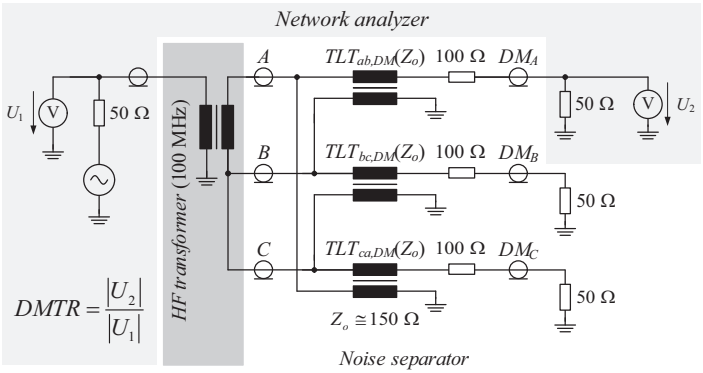


Figure 5.44: Setup employed to measure DMTR – differential mode transmission ratio. An alternative setup as shown in section 6.4.2 could also be employed.

The measurement results of the DMTR for all three ports of the DM separator are very well balanced and present a difference of less than 3 dB when compared with the ideal DMTR as shown in Figure 5.48, for the whole frequency range of interest.

The measured CMTR is displayed in Figure 5.49, where less than 1 dB deviation from the ideal CMTR is observed at 30 MHz.

The CMRR, shown in Figure 5.50 for the three DM channels, is below -40 dB up to 20 MHz and remain lower than -20 dB for the whole frequency range.

Finally, the DMRR for the three channels are below -40dB up to 30 MHz as depicted in Figure 5.51.

All the network analyzer measurements as well as the impedance measurements confirm the good high frequency behavior of the built prototypes and support the theoretical considerations.

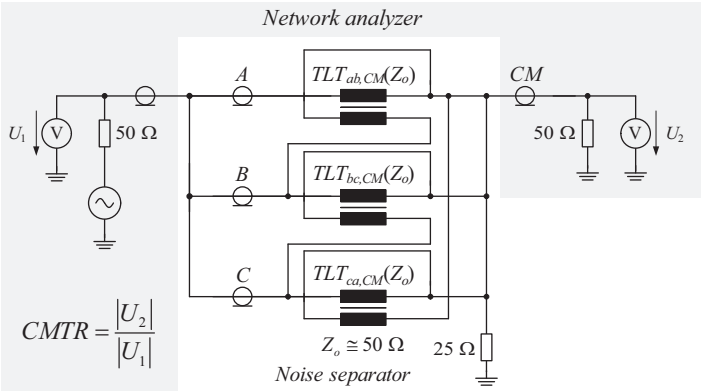


Figure 5.45: Setup employed to measure CMTR – common mode transmission ratio.

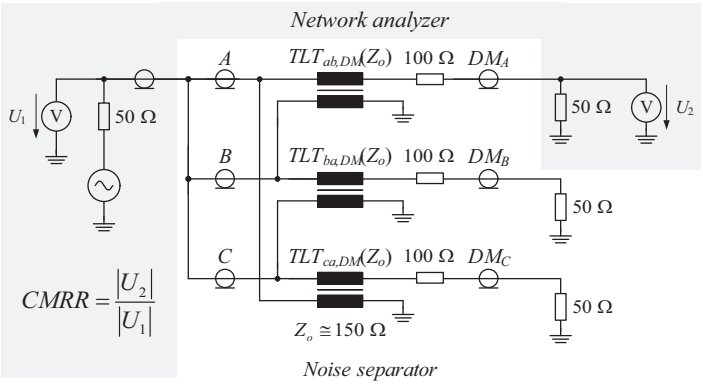


Figure 5.46: Setup employed to measure CMRR – common mode rejection ratio.

The last presented experiment was carried out with the setup presented in Figure 5.52. A three-phase rectifier employing a three-phase diode bridge supplying a 40 W Flyback converter with one of its outputs connected to protective earth (PE) and three-phase filters (CM and DM) at its input was used as equipment under test (EUT).

The prototypes of the separators were used to measure the DM and

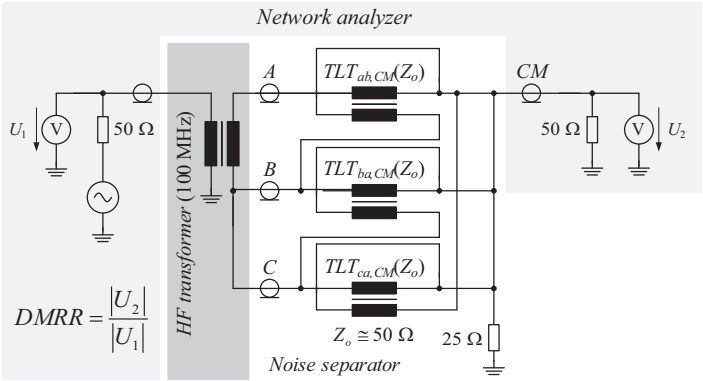


Figure 5.47: Setup employed to measure DMRR – differential mode rejection ratio. An alternative setup as shown in section 6.4.2 could also be employed.

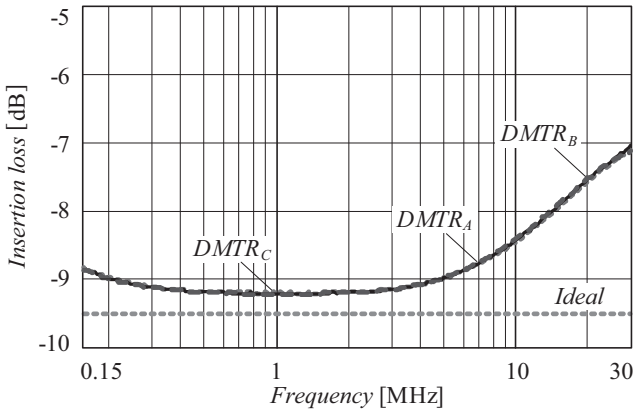


Figure 5.48: Measured frequency characteristics of the differential mode transmission ratio for the DM noise separator.

CM emission levels with a test receiver with the necessary settings for the attenuation provided by the separators. The inputs of the separators were connected to the outputs of three separated single-line LISNs. A third measurement taken directly at one of the LISNs outputs was performed in order to compare with the separated measurements.

The measurement results are presented in Figure 5.53, where it is ob-

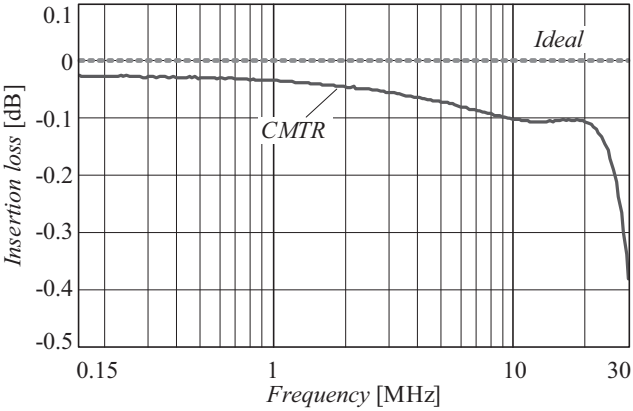


Figure 5.49: Measured frequency characteristics of the common mode transmission ratio for the CM noise separator.

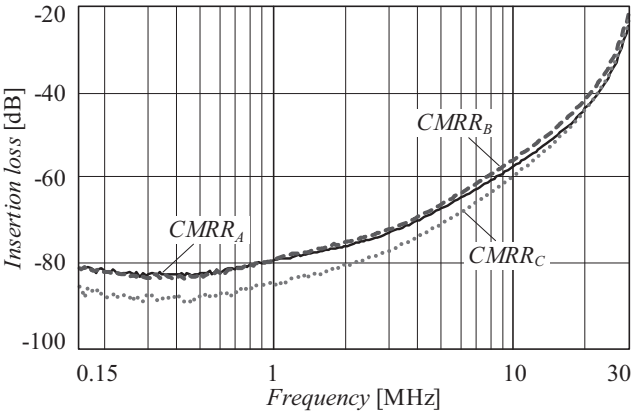


Figure 5.50: Measured frequency characteristics of the common mode rejection ratio for the DM noise separator.

served that the CM emission levels are much lower than the DM emissions in the lower frequencies, up to approximately 5 MHz, as it is to be expected. For this lower frequency range, the total noise measured directly at a LISN approaches the DM curve as expected. For higher frequencies both, CM and DM, present close values and the total emission levels are

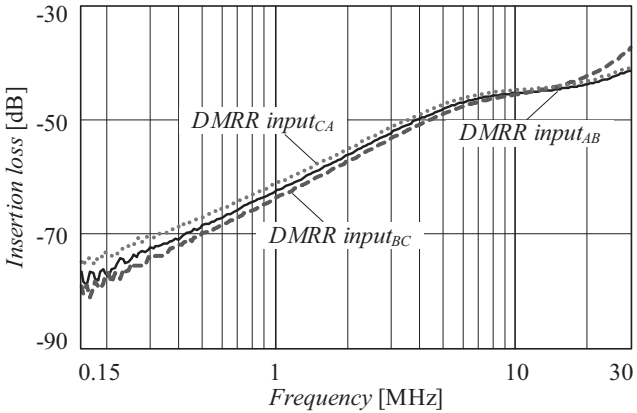


Figure 5.51: Measured frequency characteristics of the differential mode rejection ratio for the CM noise separator.

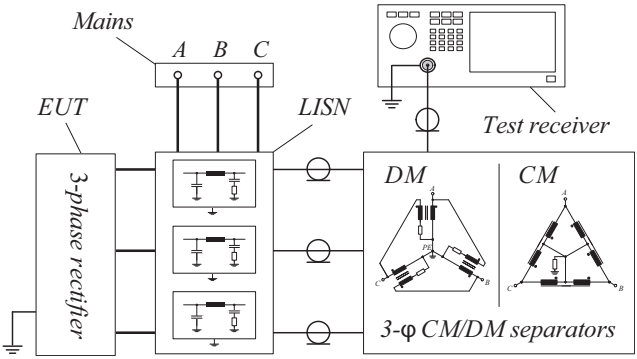


Figure 5.52: Test setup for the conducted emission measurements using the proposed three-phase CM/DM noise separation passive network.

always higher as theoretically predictable. Differences on the measurement curves are expected since it is not possible to make simultaneous measurements and the influence for high frequencies on the EUT depends on its characteristics. Besides that, the experimental results prove that the separation networks are able to effectively discriminate CM and DM emissions in a typical CE measurement setup as per CISPR 16.

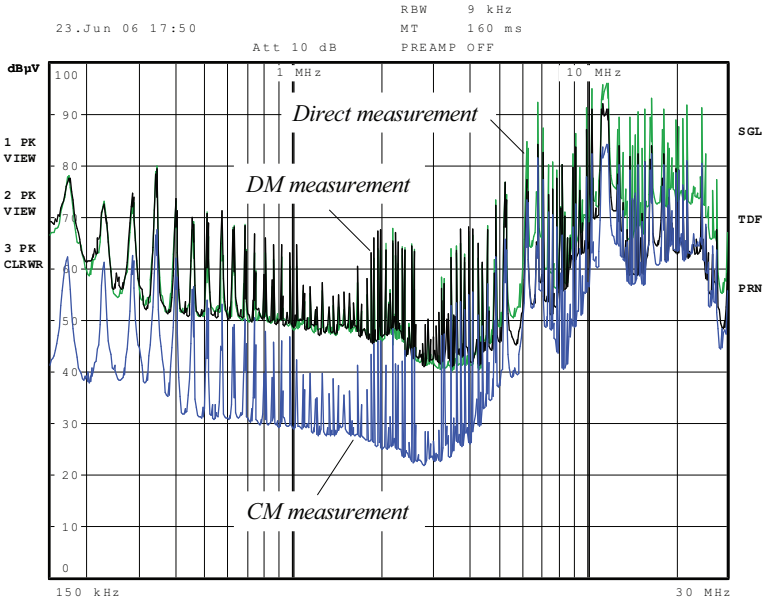


Figure 5.53: Quasi-peak measurements, as specified in CSIPR 16, performed with and without the noise separators. Axes: 0 to 100 dBmV and 150 kHz to 30 MHz. Green curve: measurement without the use of a noise separator; black curve: measurement performed in one of the DM separator output ports, and; blue curve: measurement from the noise separator CM output port.

5.6 Summary

The first part of this chapter has mathematically derived the necessary operations for the separation of common- and differential-mode signals measured at the outputs of a standard three-phase LISN. Information about the quantitative information about the noise modes can be employed to design the CM and DM stages of an EMC filter and, furthermore, can be employed to evaluate noise reduction techniques that are specific to one of the noise modes, CM or DM.

This chapter has presented novel three-phase DM/CM separation networks that are intended to be used in the evaluation of noise sources, which will help in the design and troubleshooting of electromagnetic emis-

sion control systems for electronic equipment.

The first network is an arrangement of passive components, which allows for the evaluation of CM and DM in a single unit. The operating principle and characteristics of this passive network have been discussed and experimentally verified. Conducted emission measurements were successfully performed in a three-phase electric motor drive using the separator indicating the noise levels and dominating modes. Very good measurement characteristics have been observed up to 10 MHz, from where common- and differential-mode rejection ratios begin to decrease and the equivalent input impedances start to increase beyond the boundaries specified by CISPR 16.

A second separation network that is based on the use of active circuits has been presented, but as it demands for very careful layout and large bandwidth / low noise amplifiers, which must be supplied through a very "quiet" power supply, it has not not been implemented.

This chapter has also introduced CM and DM noise separation networks for the assessment of conducted emission for EMC measurements, which are based on Transmission Line Transformers. The TLT based networks can also be easily integrated into typical CE test setups. The TLTs are specifically designed for the application, but are inexpensive small transformers. Nevertheless, high performance is achieved for a large frequency range. High rejection ratios and close to ideal transmission ratios are achieved, while the input impedances are very well matched with the requirements from CISPR 16. A study on the influence of unbalances and non-ideal coupling was carried out, which shows that these parameters must be controlled in order to achieve a good performance. The theoretical principles are presented for the different networks. Finally, experimental results verify that the proposed networks are capable of effectively separating the CM and DM emissions in a CE test setup as specified in CISPR 16, presenting acceptable common- and differential-mode rejection ratios up to 30 MHz and input impedances which are within the limits specified in CISPR 16 for a LISN.

Chapter 6

The Design of Differential-Mode Filters for Three-Phase Converters

"In life, there are no solutions. There are marching forces: create them is a must and, then, solutions follow." Antoine de Saint-Exupéry

6.1 Introduction

As power electronics converters are known to generate high conducted emission (CE) levels, efforts in research are being performed to reduce these emissions at their source, but also through line filters [21, 24, 39]. Line filters are placed at the interfaces between power grid and converters.

The demands for higher system compactness have moved Power Electronics research towards the limits of available circuit topologies, materials, components, modulation schemes and control strategies [6, 19]. Increasing switching frequencies, newly developed materials and high performance cooling systems have allowed the miniaturization of the power converters, which consequently present electromagnetic field spectra of higher frequencies confined to smaller spaces [6, 45], where one component notably influences the other if attention is not put on their physical

disposition. As electromagnetic compatibility (EMC) must obviously be guaranteed inside the system and within its environment [21], electromagnetic emissions control strategies should be employed.

For the reduction of conducted emissions (CE), filters have been designed and applied as an interface between the electrical power grid and the power electronics converters. For high performance three-phase converter systems, these input filters are typically designed based on passive components, inductors and capacitors along with resistors providing passive damping [39, 209]. Although passive cancellation circuits [210] and active filters circuits [211–214] have been lately also researched and some practical applications have been reported [213, 214], most of the power filters are still based on passive elements [24, 39, 40], where inductors play a major role in increasing series impedance for both, differential (DM) and common mode (CM) emissions, and capacitors are responsible for low parallel impedances. These passive components based filters are responsible for a significant part of the power system's volume and many efforts have been made in order to improve the performance of filter components and to develop filter topologies allowing for volume, size and costs reduction. There, multi-stage LC filters lead to more compact filters and sometimes cheaper than single-stage ones [215]. Thus, multi-stage filters are employed in the filters discussed in this chapter.

Considering Electromagnetic Compatibility, there are two main reasons for employing EMC input filters, namely: (*i*) to prevent electromagnetic interference of the considered power electronic converter with electronic systems present in the neighboring environment, and (*ii*) to avoid a disturbance of the power converter operation by sources of electromagnetic noise in the surrounds [25, 39]. With this aim, international organizations have been constantly working on standards which have to be considered when designing the EMI filter of a power electronic system.

Aiming for EMC and energy efficiency, the main requirements for input EMC filters are:

1. Fulfillment of international EMC regulations on differential mode what translates into minimum filter attenuation requirement at given frequencies;

2. Minimization of input current fundamental displacement factor;

3. Limitation of the physical size/energy stored in the filter components;

4. Sufficient passive damping causing minimum losses, in order to avoid oscillations also for no-load operation;

5. Avoidance of filter resonances at multiples of the switching frequency;

6. Minimization of the filter output impedance, in order to ensure system stability and minimize control design restrictions.

Nevertheless, critical aspects to fulfill these tasks are observed, such as:

1. Uncertainty in the mains impedance which could shift given resonant frequencies or introduce novel resonant circuits with low damping;

2. Modeling of the EMC test receiver in order to properly define the required filter attenuation in the design process;

3. Prediction of the high-frequency filter behavior which is influenced / determined by parasitics of the filter elements;

4. Low complexity and/or low component count of the filter (translating into low costs);

5. Influence of the filter on the overall system control stability.

Aiming on the design of DM filters, it is important to study calculation procedures which are suitable for today's computational resources. The calculation of the attenuation of a filter is of high importance and is studied here through the analytical solution for a ladder circuit [216], which represents the single-phase equivalent circuit for a general LC low pass filter. A general solution for the calculation of the output impedance of a ladder circuit is presented.

System control efforts are strongly influenced by the inclusion of an input filter to a PWM converter. For this reason, a section considering damping networks that reduce the peak impedance of LC filters is included. This section reviews networks which are presented in the literature and discusses a strategy to damp multi-stage filters. The results of this study show that multi-stage filters can also represent an advantage from a damping perspective.

To contribute on the design of differential mode filters, different DM filter design procedures are proposed in the following sections, which allow

for efficient designing compact EMC input filters for three-phase PWM converters.

The first design procedure is applied to a Very Sparse Matrix Converter. The filter design steps provide general guidelines being applicable to any current-source type PWM converter system. This design procedure is based on a detailed mathematical model of the EMI test receiver for measuring conducted emissions in the frequency range of 0.15...30 MHz. As verified by experimental analysis employing a novel three-phase common mode/ differential mode (CM/DM) noise separator this allows an accurate prediction of the converter behavior regarding DM emissions. Accordingly, compliance to applicable EMC standards can be ensured already in the design process what represents an important step towards a virtual prototyping of the converter system resulting in shorter total design time and/or reduced overall development costs.

A second DM filter design procedure which aims in the analytical minimization of the volume of multi-stage filters is proposed and tested in a three-phase/-level PWM rectifier unit, which is employed as a power factor correction (PFC) front-end converter in telecommunication power supplies. The EMC filter is designed to fulfill EMC requirements, where an attenuation specification, based on the estimated CE levels of the rectifier, is calculated. Furthermore, the filters are designed taking into account the limits for CE specified for Class B information technology (IT) equipments as in CISPR 22. The aim is that the designed filters are of minimum volume, present the required attenuation characteristics for the frequency range of interest and include passive damping networks, leading to reasonable efforts for the control design. The proposed procedure has its emphasis on the minimization of the total filter volume through analytical considerations, avoiding the necessity of numerical optimization calculations [44, 217]. This task is performed before a prototype is built, based on simplified frequency spectra and numerical simulation results of the rectifier and its equivalent circuits for differential mode.

Finally, the filter design procedure based on the analytical minimization of the volume of multi-stage filters is extended to a computer aided design (CAD) tool, which can be employed in different types of PWM converters and allows for a fast filter design. The CAD of DM filters represents an advantage in the design cycle of a PWM converter system design, reducing its execution time and allowing for the flexible study of filter topologies.

6.2 Attenuation Calculation for Multi-Stage Filters

Assuming perfect symmetry between all phases, a filter can be reduced to its single-phase equivalent circuit. With this, the calculation of attenuation and other filter parameters is simplified to the single-phase equivalent circuit.

There are many ways to compute the attenuation of a filter, starting from very accurate numerical simulations, through complete analytical solutions, graphical solutions and ending up in asymptotic simplified expressions.

Since EMC filtering demands the employed components up to relatively high frequencies, an accurate calculation of the attenuation of a filter should take all parasitic elements and effects into account. This can be a difficult task, since parasitic effects strongly depend on electromagnetic fields. This type of calculation is usually performed with computational tools.

The design of an input EMC filter for PWM converters is typically performed for the lowest frequency to be attenuated. Thus, the designed components shall present very low parasitic effects at this frequency. For this reason, the computation of parasitic effects can be neglected in a first filter design step. Thus, simple models for the components can be employed, allowing engineers to use analytical expressions with varying degree of accuracy.

In this section, analytical calculation procedures for the attenuation of filters are studied.

6.2.1 General Solutions for a Multi-Stage Filter

A multi-stage filter can be analyzed as a ladder circuit as depicted in Figure 6.1, where a sequence of impedances and admittances form a ladder circuit. The direct derivation of a general expression for this type of circuit is not possible. However, with the use of an iterative procedure, it is possible to compute a general rule for the calculation of the parameters of the circuit.

Applying Kirchoff's laws, the system matrix for the circuit of Figure 6.1 is given by [216],

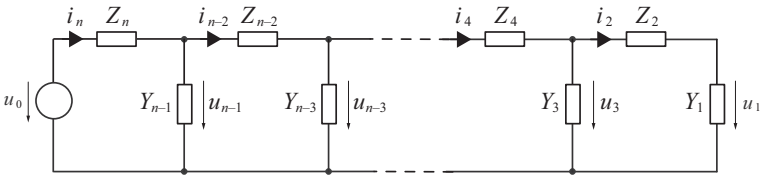


Figure 6.1: General ladder circuit.

$$\begin{bmatrix} U_0 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} Z_n & 1 & & & & & \\ -1 & Y_{n-1} & 1 & & 0 & & \\ & -1 & Z_{n-2} & 1 & & & \\ & & & & \vdots & & \\ & & & & -1 & Y_3 & 1 \\ & & 0 & & & -1 & Z_2 & 1 \\ & & & & & & -1 & Y_1 \end{bmatrix} \cdot \begin{bmatrix} I_n \\ U_{n-1} \\ I_{n-2} \\ \vdots \\ U_3 \\ I_2 \\ U_1 \end{bmatrix}. \tag{6.1}$$

From the observation of the system matrix the calculation of its determinants can be done with the following procedure,

$$\begin{aligned} & d_{-1} = 0 \\ & d_0 = 1 \\ & d_1 = Y_1 \\ & i = 2 \\ & \text{while } i \leq n \text{ do} \\ & \quad d_i = \begin{cases} Z_i\, d_{i-1} + d_{i-2}, & i = \text{even} \\ Y_i\, d_{i-1} + d_{i-2}, & i = \text{odd} \end{cases} \\ & \quad i = i + 1 \\ & \text{end do.} \end{aligned} \tag{6.2}$$

Based on eq. (6.2), any of the circuit variables can be computed with the help of the determinants. The circuit variables are voltages for the admittance branches and currents for the impedance ones. It follows, by

Cramer's rule, that the current gain Gi and the voltage gain Gu are given by,

$$Var_i = \begin{cases} GI_i = \frac{I_i}{U_0} = \frac{d_{i-1}}{d_n}, \ i = \text{even} \\ GU_i = \frac{U_i}{U_0} = \frac{d_{i-1}}{d_n}, \ i = \text{odd} \end{cases} \tag{6.3}$$

The calculation of the attenuation of the circuit can be accomplished by,

$$Var_1 = \frac{U_1}{U_0} = \frac{d_0}{d_n}. \tag{6.4}$$

This procedure is easily implemented in a computational tool, so that the calculation for any number of stages can be performed even analytically. Furthermore, other parameters can be calculated.

The input impedance of the circuit can be computed with,

$$Z_{in} = \frac{U_0}{i_n}, \tag{6.5}$$

where, from eq. (6.4),

$$i_n = U_0 \frac{d_{n-1}}{d_n}. \tag{6.6}$$

The input impedance is finally given by,

$$Z_{in} = \frac{d_n}{d_{n-1}}. \tag{6.7}$$

For the calculation of the output voltage, the calculation of the parallel impedances is required and can be performed with the following procedure,

$$
\begin{aligned}
&z_{-1} = 0 \\
&z_0 = 1 \\
&z_1 = +Y_{n-1} \\
&i = 2 \\
&\text{while } i \leq n-3 \text{ do} \\
&\quad z_i = \begin{cases} Z_{n-i}\, z_{i-1} + z_{i-2}, & i = \text{even} \\ Y_{n-i}\, z_{i-1} + z_{i-2}, & i = \text{odd} \end{cases} \\
&\quad i = i + 1 \\
&\text{end do.} \\
&z_{n-2} = \begin{cases} Z_2\, z_{n-3} + z_{i-4}, & n \geqslant 4 \\ 1, & n < 4 \end{cases}.
\end{aligned}
\tag{6.8}
$$

The output current is computed with,

$$
I_{out} = U_0 \left(\frac{z_{n-3}}{z_{n-2}} + Y_1 \right), \tag{6.9}
$$

from where the output impedance is derived,

$$
Z_{out} = \begin{cases} \frac{1}{\frac{z_{n-3}}{z_{n-2}} + Y_1}, & n > 2 \\ Z_2, & n \leq 2 \end{cases}. \tag{6.10}
$$

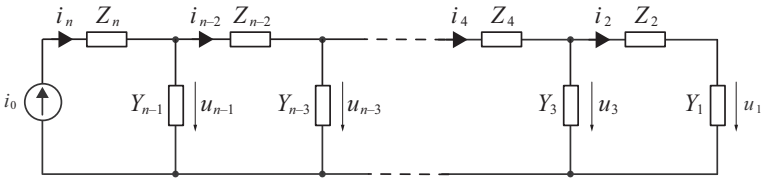


Figure 6.2: General ladder circuit supplied by a current source.

The same procedures can be applied to a circuit supplied by a current source, as in Figure 6.2. The resulting expressions and rules are strictly the same as shown for the voltage supplied circuit. This is due to the fact

that the system matrices for both circuits are similar as seen in,

$$\begin{bmatrix} I_0 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} Y_n & 1 & & & & & \\ -1 & Z_{n-1} & 1 & & 0 & & \\ & -1 & Y_{n-2} & 1 & & & \\ & & & \ddots & & & \\ & & & & -1 & Y_3 & 1 \\ & 0 & & & & -1 & Z_2 \quad 1 \\ & & & & & & -1 \quad Y_1 \end{bmatrix} \cdot \begin{bmatrix} U_n \\ I_{n-1} \\ U_{n-2} \\ \vdots \\ U_3 \\ I_2 \\ U_1 \end{bmatrix}. \tag{6.11}$$

6.2.2 Asymptotic Attenuation

As observed in the previous section, the analytical expressions that define the attenuation of multi-stage filters can be very complex even if parasitic effects are not considered. Furthermore, these equations are typically composed of polynomials of high order, having multiple roots that require numerical solutions. Thus, these expressions are not well suited for filter design. Aiming for simpler design equations, different procedures have been proposed [39, 215]. The basis for these procedures are the asymptotic lines that are observed from the polynomials of the attenuation expressions.

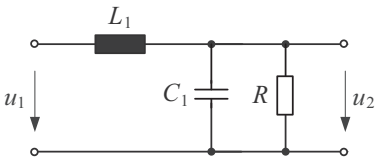


Figure 6.3: Circuit schematic of a single-stage LC filter.

Starting from a single stage LC filter as in Figure 6.3, the transfer function from input to output is defined as,

$$\frac{1}{A(s)} = \frac{U_2(s)}{U_1(s)} = \frac{1}{s^2 L_1 C_1 + s\frac{L_1}{R} + 1}. \tag{6.12}$$

The magnitude bode plot of eq. (6.12) is plotted in Figure 6.4, where

also its asymptotes are drawn. Two asymptotes are observed, one for low frequencies and a second on e for high frequencies. These asymptotes are a good approximation of the attenuation curves for frequencies that are not close to the resonance frequency $\omega_o = 1/\sqrt{L_1 C_1}$. Thus, the high frequency asymptote is valid for frequencies much higher than ω_o.

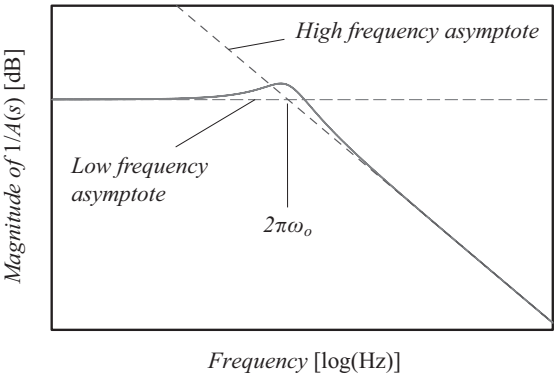


Figure 6.4: Attenuation characteristic for a single-stage LC filter. The high and low frequency asymptotes are also shown.

The high frequency asymptote can be derived directly from the attenuation expression given in eq. (6.12), where, for high frequencies, the term $s^2 L_1 C_1$ tends to be much larger than the rest of the polynomial. Thus,

$$\left|\frac{1}{A_{\text{asymptote}}(\omega)}\right| = \left|\frac{1}{A(\omega)}\right|_{\omega >> \omega_o} \cong \frac{1}{\omega^2 L_1 C_1}, \tag{6.13}$$

that is a much simpler expression than $A(s)$. Furthermore, it is essential to an EMC filter that the resonance frequency is well below the frequency range where attenuation is required to be large. This requirement validates asymptotic expressions to be employed in filter design procedures.

Assuming a multiple stage filter, it can be considered that, for frequencies that are high enough, each stage is decoupled from the surrounding ones. This assumption can be made as long as the output input impedance of a filter stage is much lower than the input impedance of the following stage. Thus,

$$\frac{1}{A_{\text{multi-stage}}(f)} \cong (2\pi f)^{2N} \prod_{i=1}^{N} (L_i\, C_i)\,, \tag{6.14}$$

where N is the number of filter stages.

This same procedure has been extended to other filter topologies in [215]. These topologies are shown in Figure 6.5 and the corresponding relations are specified in

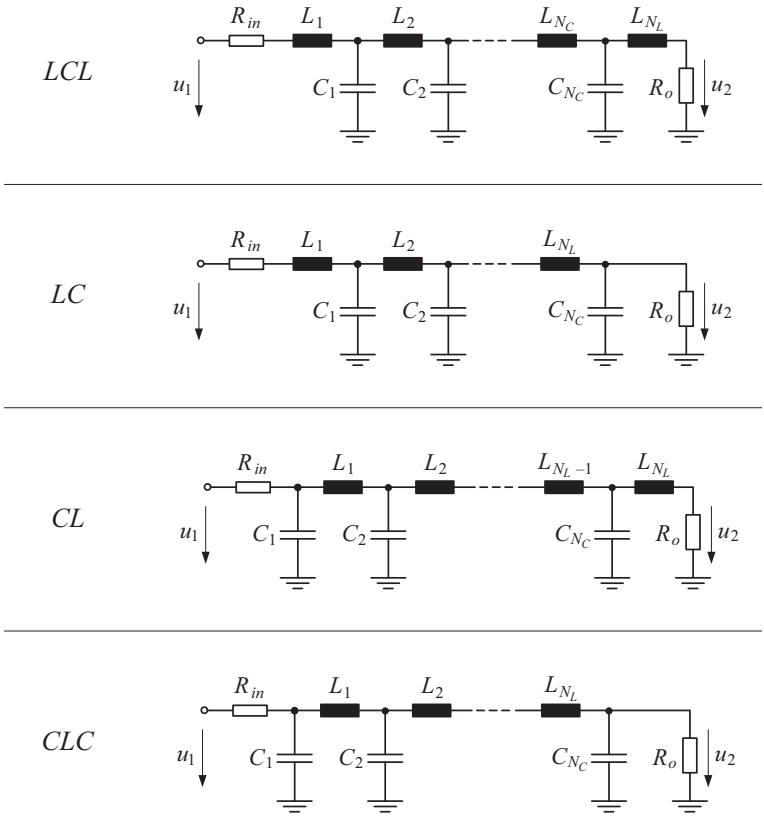


Figure 6.5: Low pass filter topologies with multiple stages composed of inductances and capacitances.

$$\frac{1}{A_{\text{general}}(f)} \cong \frac{1}{K_T}(2\pi f)^{N_L+N_C} \prod_{i=1}^{N_L} L_i \prod_{j=1}^{N_C} C_j, \tag{6.15}$$

where K_T is defined in Table 6.1 for the different filter configurations, N_L is the total number of inductors and N_C is the total number of capacitors.

Table 6.1: Coefficient K_T for different filter structures as shown in Figure 6.5 [215].

Configuration	K_T
LC	1
LCL	R_o
CL	R_o/R_{in}
CLC	$1/R_{in}$

Having the attenuation expressions a product of inductors and capacitors and the frequency to a power, one can apply the logarithm operator to eq. (6.15), so that,

$$\log\left[\frac{1}{A_{\text{general}}(f)}\right] \cong \log\left[\frac{1}{K_T}(2\pi f)^{N_L+N_C} \prod_{i=1}^{N_L} L_i \prod_{j=1}^{N_C} C_j\right]. \tag{6.16}$$

Therefore, as seen in eq. (6.17), the attenuation equation can have a parametric transformation, where new variables can be defined as in,

$$\underbrace{\log\left[\frac{1}{A_{\text{general}}(f)}\right]}_{G_{new}(f_{new})} \cong \underbrace{\left[(N_L+N_C)\log\left(\frac{2\pi}{K_T}\right)\right]}_{A} \underbrace{\log(f)}_{f_{new}} + \underbrace{\log\left[\sum_{i=1}^{N_L} L_i \sum_{j=1}^{N_C} C_j\right]}_{B}, \tag{6.17}$$

which is a linear function well suited for numerical calculations and/or optimization. With this, the calculation of the attenuation for multi-stage filters becomes simpler and appropriate for numerical calculations.

6.3 Damping Networks for Differential Mode Filters

A control problem is posed to a converter system as soon as reactive components are placed at is input. Mains impedance and input filters built with inductors and capacitors become part of the feedback system composed of a power converter and its control circuits. As part of a closed loop controlled system, their influence on the stability and dynamic responses of the system shall be analyzed.

Perhaps, the most simple way to understand this problem [218] is to model a power converter as a dynamic resistance which drains a finite and constant power P_{in} from a voltage U_{in} source supply. This is the case for most of the regulated power converters, which shall supply a controlled voltage to a load. Dynamically, though, the equivalent resistance might vary and, for this reason, it is only considered for an infinitesimal portion of the input current I_{in}, so that,

$$P_{in} = U_{in}\, I_{in} = \text{constant}, \tag{6.18}$$

from where,

$$R_{in} = \frac{dU_{in}}{dI_{in}} = -\frac{P_{in}}{I_{in}^2}, \tag{6.19}$$

which is the negative dynamic equivalent input resistance of a power converter.

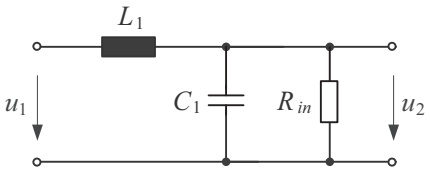


Figure 6.6: Circuit employed to analyze the effect of a negative input resistance.

The circuit shown in Figure 6.6 can be employed to analyze the impact of a negative equivalent input resistance in the behavior of a system interfaced to a power source through a purely reactive LC filter. The transfer

function from input to output for this system is,

$$G_{ideal}(s) = \frac{U_1(s)}{U_2(s)} = \frac{1}{C_1\,L_1\,s^2 + \frac{L_1}{R_{in}}s + 1}, \tag{6.20}$$

which have as poles,

$$p_1 = \frac{-\frac{L_1}{R_{in}} - \sqrt{\frac{L_1^2}{R_{in}^2} - 4C_1\,L_1}}{2C_1\,L_1} \tag{6.21}$$

$$p_2 = \frac{-\frac{L_1}{R_{in}} + \sqrt{\frac{L_1^2}{R_{in}^2} - 4C_1\,L_1}}{2C_1\,L_1}. \tag{6.22}$$

Replacing a negative value for equivalent input resistance, as it is the result in eq. (6.19), in eq. (6.21) leads to a case where the inequality,

$$\frac{L_1}{\frac{P_{in}}{I_{in}^2}} > \sqrt{\frac{L_1^2}{\left(\frac{P_{in}}{I_{in}^2}\right)^2} - 4C_1\,L_1}, \tag{6.23}$$

holds true for any positive values of the included variables. Consequently, the pole p_1 for negative input resistances is always positive and, thus, lies in the right half-plane. For this reason, this system is unstable for any positive given parameters.

Fortunately, practical inductors and capacitors present parasitic resistances and the control systems of the converters present a limited bandwidth, where the effect of negative input resistance is observed. With this, power converters can be stable systems. Even though most of the literature [42, 46, 218–222] on this subject focuses in single-phase or DC systems, the principle holds also for three-phase PWM converters.

Two approaches appear in the literature as the main streams on this subject:

i. derive simplified criteria that are sufficient for guaranteeing stability and dynamic performance based on the relation of filter output impedance and converter input impedance [42, 219–224], and;

ii. include the input filter circuits in the control oriented models, so that the complete system is considered and stability is studied based on control theory parameters [73, 74, 76, 130].

The clear advantage of the first approach is that the control matrices that model a power converter do not need to include the elements of filter circuits. Thus, simpler mathematics can be employed to judge stability and dynamic performance. The disadvantage is that, typically, the design criteria are more than sufficient. This means that the system stability is over-guaranteed and, either, excessive damping and consequent losses, or larger than necessary reactive filtering components can be the result of the design. In order to avoid the possibility of over-sized filters, the inclusion of the filter circuits in the system's control oriented models is of help. This results in more complex mathematics and parameters, where insight about the physics of the system is difficult to grasp and computational power is required. Nowadays, with the availability of advanced computational technologies, the mathematical analysis of complex systems is at hand and is, therefore, recommended if the aim of the analysis is to guarantee reduced material costs and minimized filter volume. For the explained reasons, this approach is here adopted, so that the resulting filter designs do not explicitly result from impedance criteria, but are considered to be analyzed in the system level.

Nevertheless, explicit damping networks shall be analyzed and employed in circuits. These damping networks have the objective to facilitate the control design and to avoid large oscillations during transients, such as on/off of the system, voltage surges and steep load steps. The employment of damping networks has been presented for different circuit configurations and objectives [42, 218, 219, 221, 222]. The damping networks have the objective of providing passive damping to a filter, while not increasing excessively the power dissipation as in the case of the series resistance of inductors and resistances in parallel with capacitors. Thus, the high efficiency of the switched circuits is guaranteed.

Four different filter stages including damping networks are analyzed in short. These networks are depicted in Figure 6.7, where it is seen that the low frequency series paths are through inductors of high Q and the parallel ones are through high Q capacitors, so that the low frequency currents and voltages do not generate significant losses.

The filter stage with two series capacitors (left uppermost) can also

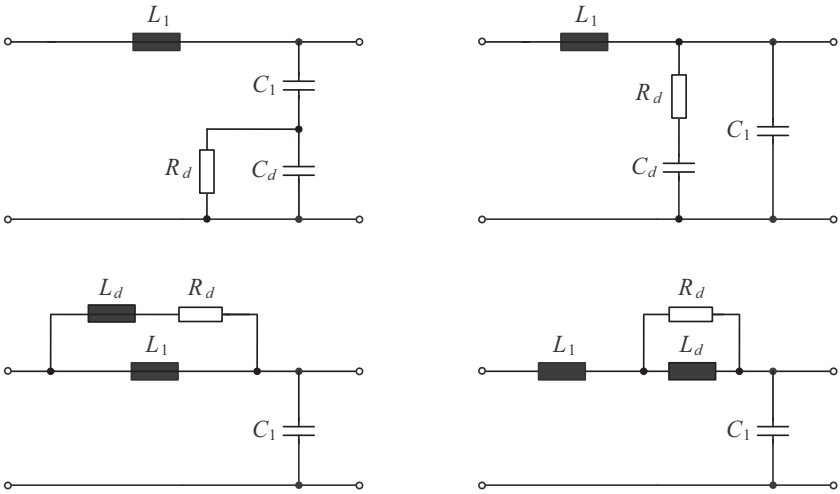


Figure 6.7: Filter stages with single resistor damping networks.

achieve passive damping and the lowest output impedance for a given high frequency attenuation, but this happens at the expense of two large sized capacitors. Capacitor C_d can be rated for lower voltage than C_1. On the other hand, C_1 must be rated for the full voltage due to safety regulations, so that a large total capacitance volume is required. Besides these, both capacitors must present low series parasitics (ESR and ESL) in order to effectively filter high frequencies.

The left-undermost filter topology employs the path formed by L_d–R_d to achieve damping. This topology is broadly employed in power converters. It is stated in [221] that good high frequency attenuation can be achieved with this circuit along with low output impedance. Nevertheless, it requires high value for the inductors L_1, L_d, since both are in parallel for high frequencies. For the same reason, the parallel parasitic capacitance of both inductors shall be minimized so that both components present high impedance for high frequencies. Furthermore, inductor L_d can be rated for lower currents, so that its size can be reduced, but inductor L_1 conducts most of the low frequency current. With its high inductance value, this is translated into a large inductor volume.

The filter stage configuration shown in the top-right side of Fig-

ure 6.7 relies in the parallel branch formed by R_d–C_d to achieve damping. The high frequency attenuation asymptote for this network is given by $1/(2\pi f\, L_1\, C_1)$, so that the filter attenuation is simple to calculate and does not strongly depend in the damping resistor. For this reason, capacitor C_d does not need to present very good high frequency characteristics. The main drawback of this structure is that a large total capacitance for low frequencies is observed, which increases the reactive power absorption and decreases the power factor for low power operation. Furthermore, if this filter stage is placed directly at the input of a power converter, increased losses due to the parallel branch R_d–C_d are expected.

The bottom-left structure in Figure 6.7 shows a damping network composed of the parallel connection of R_d–L_d. With this configuration, once again the attenuation asymptote for high frequencies is simply $1/(2\pi f\, L_1\, C_1)$. Inductor L_d is bypassed by R_d at high frequencies, so that it does not need to have its design optimized for high frequencies. In general, a lower total inductance volume is required for this topology when compared to the other one employing two inductors.

For the listed reasons, in this work, the topologies shown in the right side of Figure 6.7 are considered. The equations for the design of these filter stages leading to optimal damping are given in the following [222].

6.3.1 Filter Stage with Series RC Damping

This filter stage topology is shown in Figure 6.8. It has been studied in the literature [218,219,221,222] as one of the most advantageous topologies for this application. The main objective is to minimize the output impedance of this stage. In order to achieved this, the derivation of an optimal damping shall be accomplished. The equations employed here are according to [222].

Defining characteristic resistance R_o and frequency f_o as,

$$R_o = \sqrt{\frac{L_1}{C_1}} \tag{6.24}$$

$$f_o = \frac{1}{2\pi\sqrt{L_1 C_1}}, \tag{6.25}$$

and the ratio of the capacitors as,

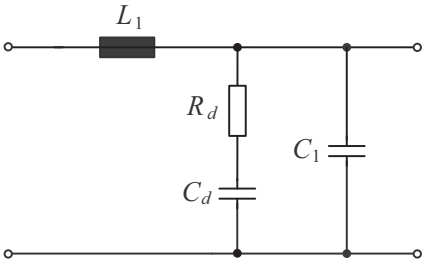


Figure 6.8: Filter stage with series RC damping network.

$$n = \frac{C_d}{C_1}, \tag{6.26}$$

it follows that the optimum resistance ratio Q_{opt} for this topology is,

$$Q_{opt} = \frac{R_{d,optimum}}{R_o} = \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}}, \tag{6.27}$$

so that, for optimum damping the damping resistance is,

$$R_d = R_o\sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}}. \tag{6.28}$$

From this result, the maximum output impedance $|Z_{out}|_{\max}$ is,

$$|Z_{out}|_{\max} = R_o\frac{\sqrt{2(2+n)}}{n}, \tag{6.29}$$

at a frequency f_{peak} of,

$$f_{peak} = \frac{2f_o}{2+n}. \tag{6.30}$$

6.3.2 Filter Stage with Parallel RL Damping

The topology with parallel RL damping network is shown in Figure 6.9. As for the previous topology, minimum output impedance is required for

given attenuation and filter elements [222].

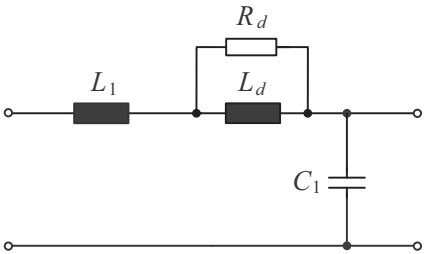


Figure 6.9: Filter stage with parallel RL damping network.

The characteristic resistance R_o and frequency f_o are defined in the same way as,

$$R_o = \sqrt{\frac{L_1}{C_1}} \tag{6.31}$$

$$f_o = \frac{1}{2\pi\sqrt{L_1 C_1}}, \tag{6.32}$$

and the ratio of the inductors as,

$$n = \frac{L_d}{L_1}, \tag{6.33}$$

it follows that the optimum resistance ratio Q_{opt} for this topology is,

$$Q_{opt} = \frac{R_{d,optimum}}{R_o} = \frac{1+n}{n}\sqrt{\frac{2(1+n)(4+n)}{(2+n)(4+3n)}}, \tag{6.34}$$

so that, for optimum damping the damping resistance is,

$$R_d = R_o \frac{1+n}{n}\sqrt{\frac{2(1+n)(4+n)}{(2+n)(4+3n)}}. \tag{6.35}$$

From this result, the maximum output impedance $|Z_{out}|_{\max}$ is,

$$|Z_{out}|_{\max} = R_o \frac{\sqrt{2(1+n)(2+n)}}{n}, \tag{6.36}$$

at a frequency f_{peak} of,

$$f_{peak} = f_o \sqrt{\frac{2+n}{2(1+n)}}. \tag{6.37}$$

6.3.3 Peaking versus Overshoot

Perhaps the most important aspect of low pass LC filters is their frequency attenuation characteristic, which can be computed with transfer functions. It is also desirable to know the damping characteristics of the filters. From control theory, the step response of a system gives information about how well the system is damped. In filter design, it is an important characteristic since it directly shows possible over-voltages due to load steps or voltage surges from the mains. The following equations can be used to derive a connection between the attenuation curve of a filter and the overshoot in a step response.

Considering a second order system with the transfer function,

$$G(s) = \frac{1}{\frac{1}{\omega_n^2}s^2 + \frac{2\zeta}{\omega_n}s + 1}, \tag{6.38}$$

the Bode magnitude plot of Figure 6.10 is typical for an undamped system. For this type of system , the peaking is defined by the resonant peak M_r and the phase margin PM of the system is [225],

$$PM = \arctan\left(\frac{2\zeta}{\sqrt{\sqrt{1+4\zeta^4} - 2\zeta^2}}\right). \tag{6.39}$$

The resonant peak amplitude can be approximately computed with,

$$M_r \cong \frac{1}{2\sin\left(\frac{PM}{2}\right)}, \tag{6.40}$$

so that it is a function of the damping ratio ζ,

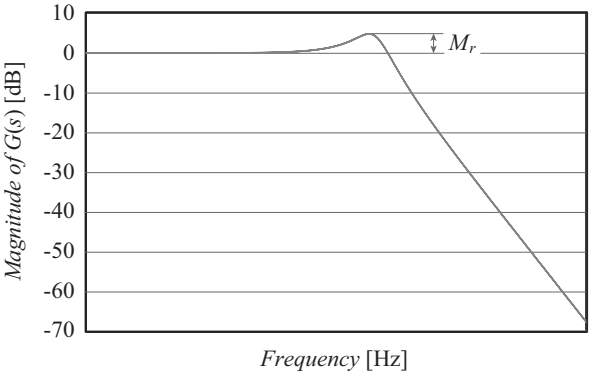


Figure 6.10: Typical magnitude bode plot for a second order system $G(s)$.

$$M_r \cong \frac{1}{2\sin\left[\arctan\left(\frac{2\zeta}{\sqrt{\sqrt{1+4\zeta^4}-2\zeta^2}}\right)\right]}, \tag{6.41}$$

Defining the following variables,

$$\omega_d = \omega_n\sqrt{1-\zeta^2} \tag{6.42}$$

$$\sigma = \omega_n\zeta, \tag{6.43}$$

the time response $y(t)$ of the system to a unit step is defined by,

$$y(t) = 1 - e^{-\sigma t}\left[\cos(\omega_d t) + \frac{\sigma}{\omega_d}\sin(\omega_d t)\right], \tag{6.44}$$

from where the behavior depicted in Figure 6.11 is observed for weekly damped systems. The overshoot amplitude is given by,

$$M_p = e^{-\frac{\pi\zeta}{\sqrt{1-\zeta^2}}}. \tag{6.45}$$

Observing eq. (6.41) and eq. (6.45) it is seen that both functions depend on the damping ratio ζ. Thus, a direct relation between overshoot

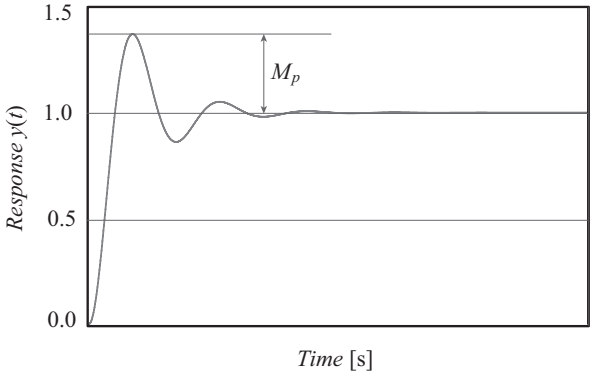


Figure 6.11: Typical time response for a second order system $G(s)$.

M_p and resonant peak M_r can be derived as,

$$\frac{1}{M_r} = -\frac{1}{2}\sin\left[\frac{1}{2}\arctan\left(2\ln(Mp)\frac{1}{\sqrt{\ln(Mp)^2+\pi^2}}\cdot \frac{\sqrt{\ln(Mp)^2+\pi^2}}{\sqrt{\left(\sqrt{\frac{5\ln(Mp)^4+2\ln(Mp)^2\pi^2+\pi^4}{\left((\ln(Mp))^2+\pi^2\right)^2}}\ln(Mp)^2+\sqrt{\frac{5\ln(Mp)^4+2\ln(Mp)^2\pi^2+\pi^4}{\left(\ln(Mp)^2+\pi^2\right)^2}}\pi^2-2(\ln(Mp))^2\right)}}\right)\right] \tag{6.46}$$

The characteristic of eq. (6.46) is plotted in Figure 6.12, from where a direct relation between the variables can be seen. It is observed that high resonant peaks lead to high overshoots.

Even though eq. (6.46) has been derived for second order systems, it can be employed to estimate overshoot in higher order systems as long as there is a pair of dominant complex conjugate imaginary poles.

6.3.4 Damping of Multi-Stage LC Filters

The previous damping networks can be applied to a filter single-stage. However, the employment of filters with multiple stages (*multi-stage filters*) is advantageous from a volume perspective for a given attenuation.

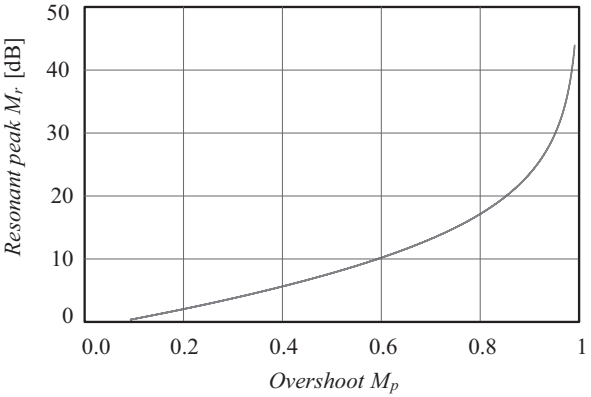


Figure 6.12: Resonant peak M_r as a function of the overshoot ratio M_p.

The basic circuit for a multi-stage filter is depicted in Figure 6.13. The asymptotic high frequency attenuation for this topology is given by,

$$\frac{1}{A_{asymp}(f)} = \frac{|U_2(f)|}{|U_1(f)|} = (2\pi f)^{2N} \prod_{i=1}^{N} (L_i\, C_i), \tag{6.47}$$

which shows that the higher the number of stages, the steeper is the attenuation slope. The result is that, for the same total inductance and capacitance, a higher attenuation can be achieved.

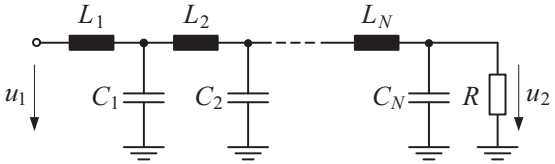


Figure 6.13: General multi-stage LC filter.

Observing the circuit of Figure 6.13 and checking the limit where $N \to \infty$, it is clear the the circuit reminds a lossless transmission line. It is common practice for a transmission line with unmatched source and load impedances to use matching circuits at both ends of the line. A broadly employed circuit is seen is Figure 6.14, where resistor R_s is added

in series with the impedance of the signal source and R_l in parallel with the impedance of a load connected at the end of the transmission line TL. This guarantees that, if the source impedance is much lower and/or the load impedance is much higher than the characteristic impedance Z_o of the line, both ends will be matched and no standing waves effect shall be observed. Of course, increasing the losses in the transmission line would have a damping effect as well, but this would not be as advantageous.

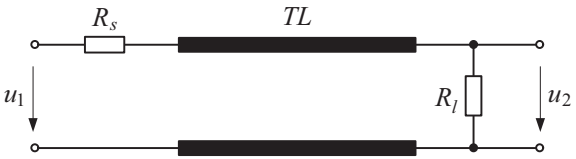


Figure 6.14: Improved matching for a transmission line.

Based on the matching strategy for a transmission line, the same technique can be extended to multi-stage filters, where only the first and last stages are to be damped. This reduces the number of components and is able to provide low output impedances.

The challenge with this strategy is to achieve optimum damping with multiple filter stages. As general expressions for such configurations are difficult to derive, a first approach is to consider that the stages are completely decoupled and design the damping networks as for a single stage with the procedure given in section 6.3. The second step is to iteratively improve the achieved damping.

In order to compare the achievable results with the employment of multi-stage filters, simulation examples are used, which provide insight into this subject and are presented in the following.

Considering the filter circuits presented in Figure 6.15, where the number of stages goes from a single one for the top circuit to a three for the lowermost one. The basic assumption that the total inductance and capacitance for the three circuits are the same is given in order to compare the structures. In a filtering application this would not be case, since the attenuation achieved with a larger number of stages shall be higher. The attenuation curves for the three circuits are shown in Figure 6.16, where this principle is illustrated.

The damping networks have been designed in order to achieve damping

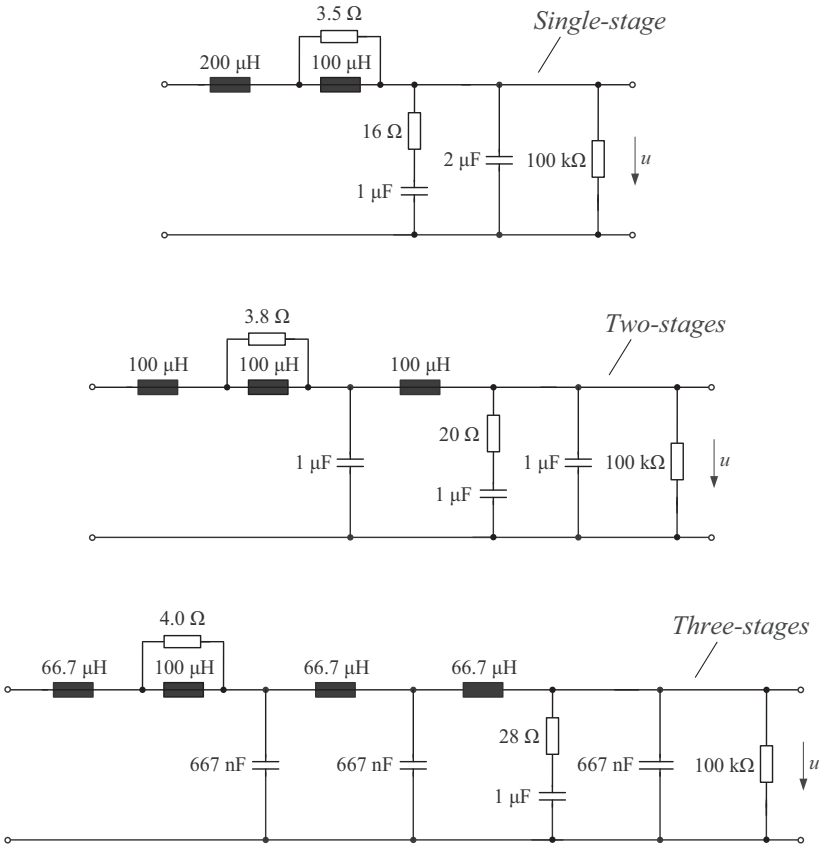


Figure 6.15: Filters with varying number of stages for a fixed amount of capacitance and inductance. Near to optimum damping is provided for all three structures.

values very close to the optimum ones for all three structures. With this, the effect of damping networks over the circuits can be understood by comparing two results. The first one is directly seen at the attenuation curves (cf. Figure 6.16). The single-stage filter shows higher peaking, thus, lower damping than the other topologies. Observing the step response of the three circuits, as shown in Figure 6.17, reveals that the overshoot for the filters with two- and three-stages is lower than for the single-stage one.

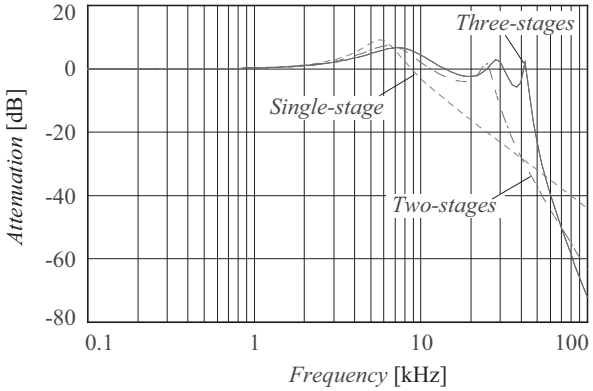


Figure 6.16: Attenuation curves for the three types of filters presented in Figure 6.15.

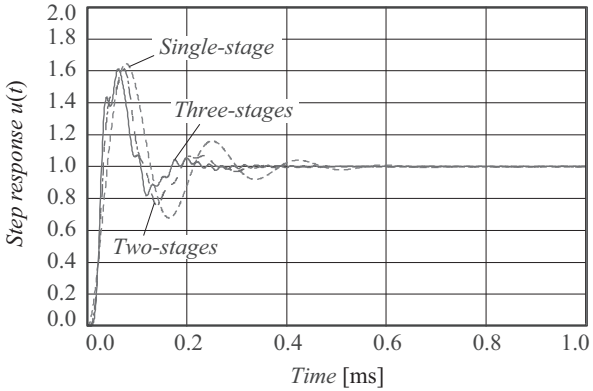


Figure 6.17: Step response for the three types of filters presented in Figure 6.15.

Furthermore, the settling time is also reduced and, for the three-stages filter it is approximately one half of the settling time for the single-stage.

6.4 Insertion Loss Measurements for Three-Phase EMC Filters

Insertion loss has been the most spread method of characterizing line filters. It is defined in [226] as:

> "1) The loss in load power due to the insertion of apparatus at some point in a transmission system. It is measured as the difference between the power received at the load before insertion of the apparatus and the power received at the load after insertion. 2) The ratio, expressed in decibels, of the power received at the load before insertion of the apparatus, to the power received at the load after insertion."

and it is a well suited method for HF measurements, were very low or very high source or load impedances are difficult to realize in practice.

The classical insertion loss measurement setup has been established in the military standard MIL-Std-220B (2000), which has been employed to measure the insertion loss in 50 Ω transmission systems, and, later in CISPR 17 for the measurement of the performance of EMC filters. The basic measurement setups are shown n Figure 6.18, where it is seen that, in theory, two measurements are required, with and without the filter inserted. The measured voltage before insertion is,

$$U_1(f) = U_s(f) \cdot \frac{R_l}{R_s + R_l}. \tag{6.48}$$

If load and source impedance are equal, then,

$$U_1(f) = \frac{U_s(f)}{2}. \tag{6.49}$$

After the insertion of the filter, a voltage which is dependent on the filter arrangement, components and the source and load impedances is measured,

$$U_2(f) = U_s(f) \cdot f(Filter, R_s, R_L). \tag{6.50}$$

The insertion loss is defined as,

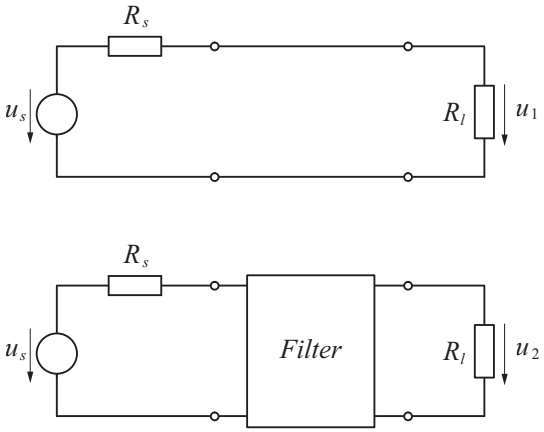


Figure 6.18: Insertion loss measurement circuits.

$$IL(f) = 20 \log \left(\frac{|U_1(f)|}{|U_2(f)|} \right), \tag{6.51}$$

thus,

$$IL(f) = 20 \log \left(\frac{|f(Filter, R_s, R_L)|}{2} \right). \tag{6.52}$$

As it is seen, the insertion loss measurement is a function of the source and load measurement impedances. Typically, insertion loss measurements are performed in 50 Ω source and load impedances. This is the most common configuration that is implemented in commercial network analyzers. This has generated long time discussions [200, 227–229], because the output impedances of power converters might be far from 50 Ω, as well as the grid impedance, which strongly varies with frequency and installation practices. Nevertheless, this is still the most common measurement parameter for commercially available line filters and proves useful in quality assurance tests or testing of models.

In order to overcome the problems arising from the dependence on the 50 Ω measurement system, different methods have been proposed. The most employed method at the moment is the employment of 0.1 Ω

/ 100 Ω source and load impedances. This method has been proposed in [228]. It is a method based in statistically measured source and load impedances and extreme-value theory, leading to more realistic prediction of the performance of a filter in a real application. The circuit proposed in [228] is shown in Figure 6.19, where it is seen that an ordinary 50 Ω test system can be employed together with special transformers to realize the 0.1 Ω / 100 Ω measurements.

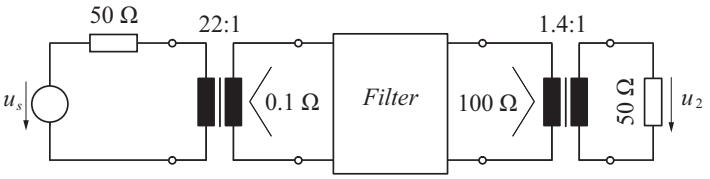


Figure 6.19: Insertion loss measurement circuits for worst-case impedances.

Different measurement setups apply to evaluate common- and differential-mode insertion loss of a filter. The test setups employed throughout this work are shown in Figure 6.20 for three-phase three-line filters, i.e. without neutral connection. It is observed that HF transformers are required in order to measure DM insertion loss. The employed transformers must present large bandwidth and low inter-winding capacitance, since very high attenuation are to be measured. In this work the 0.1 Ω / 100 Ω measurement system has not been employed because the performed insertion loss measurements have been employed only for means of comparison or to validate a model. Furthermore, 0.1 Ω / 100 Ω insertion loss curves are useful for commercially available filters, while the filters considered in this work have been specially designed for their application.

6.4.1 Alternative Method for Measuring Worst-Case Insertion Loss

The HF transformers employed in the 0.1 Ω / 100 Ω insertion loss measurement system (cf. Figure 6.19) are difficult to realize in practice due to the high turns ratio and the required large bandwidth. An alternative to this approach can be the measurement of the S-parameters of the filter under test with the conventional 50 Ω / 50 Ω insertion loss test setup (cf. Figure 6.20). In [230] it has been shown that CM and DM performance

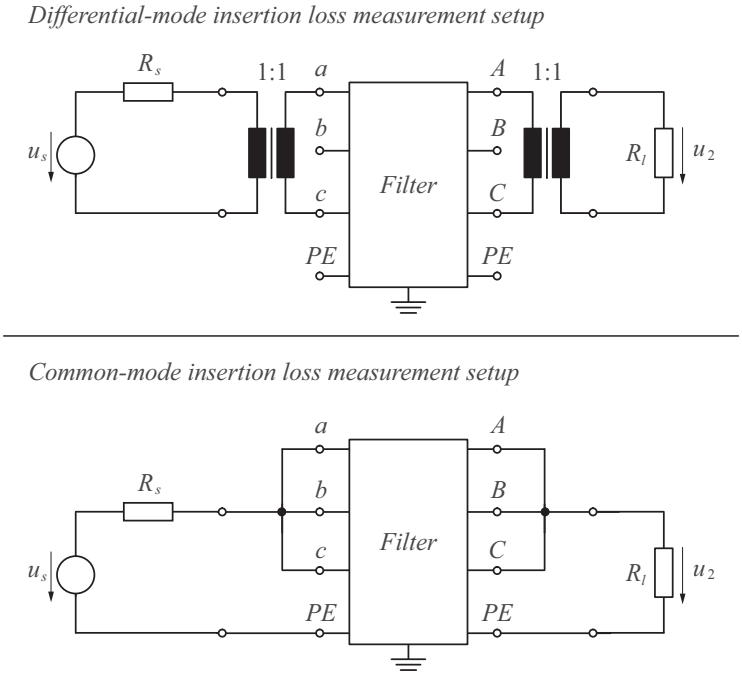


Figure 6.20: Insertion loss measurement circuits for three-phase filters.

of a filter can be characterized by the S-parameters, while in [187] the transformations from S-parameters to other characteristic matrices (Z, Y, abcd, etc) have been listed for generic impedances. These are considered here in order to find the 0.1 Ω / 100 Ω insertion loss based on 50 Ω / 50 Ω measurements of the S-parameters.

A generic two-port network is shown in Figure 6.21, where some parameters are defined, namely: two currents (i_1 and i_2) and voltages (u_1 and u_2) and four waves (incident a_1, a_2 and reflected b_1, b_2).

The network analyzer measures the relation among the incident and reflected waves and converts them into variables named the S-parameters of the measured network. These parameters are defined as,

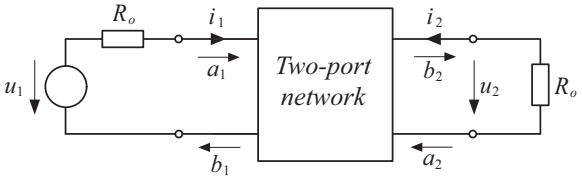


Figure 6.21: Definition of parameters for a two-port network.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \tag{6.53}$$

but the measured parameters depend upon source and load impedances of the measurement setup.

The impedance matrix $\mathbf{Z}$ for the two-port network is defined in,

$$\begin{aligned} \mathbf{U} &= \mathbf{Z} \cdot \mathbf{I} \\ \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} &= \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \end{aligned} \tag{6.54}$$

From [187], the impedance matrix coefficients can be computed with,

$$Z_{11} = \frac{R_o\,[(1+S_{11})(1-S_{22})+S_{12}S_{21}]}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \tag{6.55}$$

$$Z_{12} = \frac{2\,R_o\,S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \tag{6.56}$$

$$Z_{21} = \frac{2\,R_o\,S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \tag{6.57}$$

$$Z_{22} = \frac{R_o\,[(1-S_{11})(1+S_{22})+S_{12}S_{21}]}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}. \tag{6.58}$$

Figure 6.22 shows the two-port network inserted in a generic source and load impedance measurement system, from where the insertion loss is derived as,

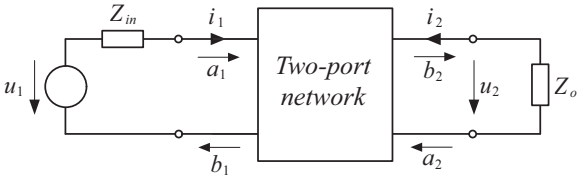


Figure 6.22: Definition of parameters for a two-port network with generic source and load impedances.

$$IL = \frac{U_2}{2\,U_1} = S_{12,final}, \tag{6.59}$$

where,

$$S_{12,final} = \frac{2\,Z_{12}\,\sqrt{R_{o1}\,R_{o2}}}{(Z_{11}+Z_{in})(Z_{22}+Z_o) - Z_{12}\,Z_{21}}, \tag{6.60}$$

with $R_{o1} = \Re\{Z_{in}\}$ and $R_{o2} = \Re\{Z_o\}$.

With these calculations, it is possible to avoid the necessity of HF transformers with non-unitary turns ratio for the measurement of the 0.1 Ω / 100 Ω insertion loss of a filter.

6.4.2 Another Discussion on the Insertion Loss Measurement for DMRR and DMTR

A setup like the one shown in Figure 6.18 for DM measurements is often employed to measure DMRR and DMTR. However, the transformers used in this configuration present parasitic inter-winding capacitances. These capacitances provide paths for CM currents to flow and, therefore, the guarantee of an excitation voltage that is free from CM depends strongly in the transformers impedances, both, desired and parasitic ones. The 0.1 Ω / 100 Ω insertion loss measurement system and the single-phase version are also not free from this problem. Nevertheless, this type of setup is employed for insertion loss measurements of CMRR and DMTR and is specified in EMC standards, such as CISPR 17 and MIL-STD-220B.

One alternative to the conventional setup is shown in the circuits of Figure 6.23, where a symmetric secondary circuit with two windings has

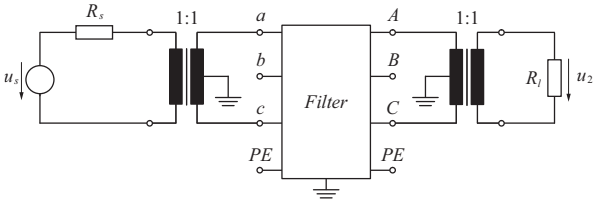


Figure 6.23: Alternative setup for the insertion loss measurement of DMTR.

its center point connected to ground. For measuring the CMRR, for instance, of a CM/DM noise separator, the only difference is that the measurement output terminals for CM would not require the output transformer, since the CM terminals would be grounded at the same potential of the measurement equipment. The drawback of this is that, for DMRR measurements, the CM signals might be reduced by the secondary side center point connected to ground.

6.5 Minimum Volume Design of Three-Phase DM Inductors

The design of the DM inductors is considerably different from that of the CM ones. The DM currents are composed of a high mains frequency component and a relatively small high frequency ripple due to the attenuation given by input inductors and capacitors. For this reason, the cross sectional area of the core A_e is mainly determined by saturation rather than by core losses. Furthermore, the high frequency losses in the winding are also comparatively small and can be neglected. The other parameter that defines the core is the required winding area A_w.

The filter inductance L_{DM} and rated current are related to the size of the inductor $A_e A_w$ (core area product) by,

$$L_{DM}\, I_{peak}\, I_{rms} = k_w J_{\max} B_{peak} A_e A_w. \tag{6.61}$$

from where, it is seen that the core material, cooling strategy are the main factors defining the maximum current density $J_{\max}$ and the maximum flux density $B_{\max}$. These are major parameters in the inductor

design, however, for a minimum volume design, these parameters must be thoroughly computed.

Two main choices for DM inductors exist, namely: high permeability materials with gapped cores or ungapped cores with controlled permeability materials. Employing gapped cores might be a difficult task due to the higher leakage flux, which might lead to coupling to other components and radiated emissions. Furthermore, ferrites present relatively low saturation flux and, thus, lead to more core volume required for a given inductance. For these reasons, only iron powder materials are considered here with toroidal cores.

The objective of this section is to propose a design procedure for minimum volume DM inductors for a given specification. This procedure must be suitable for a computational implementation and is based in an iterative process as presented in the following.

The specifications for the differential mode inductor design procedure are:

- Ambient temperature: T_{amb};
- Maximum temperature: $T_{\max}$;
- Maximum current: I_{rms};
- Frequency of interest: f_{int};
- Desired inductance at f_{int}: L_{des};
- Switching frequency: f_S;
- Peak current (or voltage) amplitude at f_S: I_s (U_s).

Design Databases

Different databases are required for iterative design of the inductors. A database containing mechanical and magnetic properties, as specified in Table 6.2, of the commercially available cores for the chosen material must be available.

The magnetic materials are modeled through approximate expressions which are obtained from curve-fitting manufacturer's catalog information.

Table 6.2: Required specifications for the database of available cores.

Parameter	*Symbol*	*Unit*
Bare outer diameter	OD_{bare}	[m]
Bare inner diameter	ID_{bare}	[m]
Bare height	H_{bare}	[m]
Outer diameter	OD	[m]
Inner diameter	ID	[m]
Core height	H	[m]
Mean magnetic path length	l_e	[m]
Core cross-sectional area	A_e	[m^2]
Thermal resistance	R_{th}	[K/W]
Core inductance per turn square	AL	[H/$turns^2$]

The expression for the magnitude of the complex permeability is here approximated as,

$$\mu_r(f) = M_1 \frac{\left(\frac{f}{M_2}+1\right)^{M_4}}{\left(\frac{f}{M_3}+1\right)^{M_5}}. \tag{6.62}$$

The coefficients for eq. (6.62) are given in Table 6.3, respectively, for some magnetic materials. The listed magnetic materials are from two manufacturers, according to:

- MPP – Magnetics;
- High Flux – Magnetics;
- Cool Mu – Magnetics;
- -26 – Micrometals;
- -52 – Micrometals;

The number following the materials's names in the following tables is the initial permeability μ_{init}.

Table 6.3: Coefficients for the complex permeability dependency on frequency for different magnetic materials.

Material	M_1	M_2	M_3	M_4	M_5
1. MPP 14	1	$1.00 \cdot 10^7$	$9.92 \cdot 10^7$	0.52903	5.01204
2. MPP 26	1	$6.95 \cdot 10^6$	$3.68 \cdot 10^7$	1.35575	6.35683
3. MPP 60	1	$4.84 \cdot 10^6$	$3.25 \cdot 10^7$	1.05366	6.73694
4. MPP 125	1	$7.52 \cdot 10^6$	$2.30 \cdot 10^7$	1.65851	6.73291
5. MPP 160	1	$7.62 \cdot 10^6$	$2.20 \cdot 10^7$	1.53103	6.94334
6. MPP 200	1	$7.89 \cdot 10^6$	$2.14 \cdot 10^7$	1.28371	7.27897
7. High Flux 14	1	$1.00 \cdot 10^7$	$9.98 \cdot 10^7$	0.38572	4.36413
8. High Flux 26	1	$1.00 \cdot 10^7$	$9.98 \cdot 10^7$	0.07413	5.04319
9. High Flux 60	1	$1.00 \cdot 10^7$	$9.64 \cdot 10^7$	0.00000	8.30268
10. High Flux 125	1	$1.00 \cdot 10^7$	$8.58 \cdot 10^7$	0.00000	17.3865
11. High Flux 160	1	$4.94 \cdot 10^6$	$5.87 \cdot 10^5$	−2.26866	−0.0871
12. Cool Mu 26	1	$1.00 \cdot 10^7$	$9.99 \cdot 10^7$	0.20540	3.00000
13. Cool Mu 60	1	$3.22 \cdot 10^7$	$1.24 \cdot 10^8$	1.22293	8.16427
14. Cool Mu 75	1	$1.47 \cdot 10^6$	$1.03 \cdot 10^8$	−0.16459	1.01451
15. Cool Mu 90	1	$7.60 \cdot 10^5$	$1.06 \cdot 10^8$	−0.11057	6.09288
16. Cool Mu 125	1	$2.19 \cdot 10^5$	$1.02 \cdot 10^8$	−0.07725	9.08545
17. -26	1	$5.74 \cdot 10^7$	$1.63 \cdot 10^6$	0.31573	0.53650
18. -52	1	$9.88 \cdot 10^7$	$1.14 \cdot 10^7$	1.68060	1.14766

For the DM inductor, the change in permeability with DC bias has an strong influence on the achieved inductance. Thus, the dependency of the permeability on the magnetic field is modeled with,

$$\mu_r(H\ [\mathrm{A/m}]) = \sqrt{\frac{a + c\,H + e\,H^2}{1 + b\,H + d\,H^2}}, \tag{6.63}$$

and a database containing the coefficients $a \ldots e$ must be available. The coefficients for the dependency of the permeability on the magnetic field for some commercially available materials are listed in Table 6.4.

Core losses can be modeled with the Steinmetz equation,

$$P_{vol} = K_c\, f^{\alpha}\, B^{\beta}, \tag{6.64}$$

Table 6.4: Coefficients for the dependency of the permeability on the magnetic field for different magnetic materials.

Mat.	a	b	c	d	e
1.	196	$-2.25\cdot10^{-5}$	$-5.19\cdot10^{-3}$	$8.48\cdot10^{-10}$	$3.70\cdot10^{-8}$
2.	676	$-4.17\cdot10^{-5}$	$-3.32\cdot10^{-2}$	$2.92\cdot10^{-9}$	$4.40\cdot10^{-7}$
3.	3600	$-9.63\cdot10^{-5}$	$-4.09\cdot10^{-1}$	$1.56\cdot10^{-8}$	$1.25\cdot10^{-5}$
4.	15625	$-2.01\cdot10^{-4}$	-3.69	$6.76\cdot10^{-8}$	$2.35\cdot10^{-4}$
5.	25600	$-2.57\cdot10^{-4}$	-7.75	$1.11\cdot10^{-7}$	$6.31\cdot10^{-4}$
6.	40000	$-3.21\cdot10^{-4}$	$-1.51\cdot10^{1}$	$1.73\cdot10^{-7}$	$1.54\cdot10^{-3}$
7.	196	$-7.64\cdot10^{-7}$	$-2.17\cdot10^{-3}$	$5.95\cdot10^{-10}$	$6.49\cdot10^{-9}$
8.	676	$-1.42\cdot10^{-6}$	$-1.39\cdot10^{-2}$	$2.05\cdot10^{-9}$	$7.71\cdot10^{-8}$
9.	3600	$-3.28\cdot10^{-6}$	$-1.71\cdot10^{-1}$	$1.09\cdot10^{-8}$	$2.19\cdot10^{-6}$
10.	15625	$-6.83\cdot10^{-6}$	-1.55	$4.74\cdot10^{-8}$	$4.12\cdot10^{-5}$
11.	25600	$-8.74\cdot10^{-6}$	-3.24	$7.77\cdot10^{-8}$	$1.11\cdot10^{-4}$
12.	676	$2.20\cdot10^{-5}$	$-1.24\cdot10^{-2}$	$6.63\cdot10^{-9}$	$7.53\cdot10^{-9}$
13.	3600	$5.08\cdot10^{-5}$	$-1.52\cdot10^{-1}$	$3.53\cdot10^{-8}$	$2.13\cdot10^{-7}$
14.	5625	$6.35\cdot10^{-5}$	$-2.98\cdot10^{-1}$	$5.52\cdot10^{-8}$	$5.21\cdot10^{-7}$
15.	8100	$7.63\cdot10^{-5}$	$-5.15\cdot10^{-1}$	$7.94\cdot10^{-8}$	$1.08\cdot10^{-6}$
16.	15625	$1.06\cdot10^{-4}$	-1.38	$1.53\cdot10^{-7}$	$4.02\cdot10^{-6}$
17.	1.009	$6.35\cdot10^{-5}$	$1.65\cdot10^{-5}$	$1.85\cdot10^{-7}$	$3.35\cdot10^{-10}$
18.	1.024	$8.43\cdot10^{-5}$	$3.10\cdot10^{-5}$	$1.22\cdot10^{-7}$	$-1.66\cdot10^{-10}$

which coefficients are given in Table 6.5 for commercially available core materials that can be employed in DM inductors.

Operation specific information about the core materials is also required for the inductor design. The most relevant parameters are listed in Table 6.6.

Finally, a database must be built for the wires with which the inductors shall be woundd with. This database can contain available wire diameters with ϕ_{ins} and without insulation ϕ_w. Conventional magnetic copper wire is considered here.

Table 6.5: Steinmetz parameters for different magnetic materials curve-fitted for the frequency range 10 kHz ... 1 MHz.

Material	K_c	α	β
MPP 14	$4.46 \cdot 10^{-2}$	1.310	2.210
MPP 26	$8.90 \cdot 10^{-3}$	1.410	2.180
MPP 60	$6.40 \cdot 10^{-3}$	1.410	2.240
MPP 125	$1.44 \cdot 10^{-2}$	1.400	2.310
MPP 160	$4.34 \cdot 10^{-3}$	1.500	2.250
MPP 200	$2.24 \cdot 10^{-3}$	1.640	2.270
High Flux 14	$3.50 \cdot 10^{-1}$	1.260	2.520
High Flux 26	$3.43 \cdot 10^{-1}$	1.250	2.550
High Flux 60	$3.39 \cdot 10^{-1}$	1.230	2.560
High Flux 125	$1.07 \cdot 10^{-1}$	1.330	2.590
High Flux 160	$1.41 \cdot 10^{-2}$	1.410	2.560
Cool Mu 26	$8.34 \cdot 10^{-3}$	1.460	2.000
Cool Mu 60	$4.17 \cdot 10^{-3}$	1.460	2.000
Cool Mu 75	$4.17 \cdot 10^{-3}$	1.460	2.000
Cool Mu 90	$4.17 \cdot 10^{-3}$	1.460	2.000
Cool Mu 125	$4.17 \cdot 10^{-3}$	1.460	2.000
Material -26	$3.20 \cdot 10^{-1}$	1.226	1.901
Material -52	$1.08 \cdot 10^{-1}$	1.274	1.880

Table 6.6: Operating parameters for different magnetic materials.

Material	*Operating temperature* T_{oper}	Saturation flux B_{sat}
MPP	130 °C	0.75 T
High Flux	130 °C	1.30 T
Cool Mu	130 °C	0.90 T
-26	110 °C	1.00 T
-52	110 °C	1.00 T

Design Initialization

A first step for the inductor design is to establish an initial maximum current density $J_{\max,0}$ and an initial maximum flux density $B_{\max,0}$. However,

these values might strongly vary depending on the involved frequencies and core size. Here, very high values are assumed, so that the maximum flux density is assumed to be the saturation flux,

$$B_{\max,0} = B_{sat}, \tag{6.65}$$

for the chosen core material and the maximum current density is set to,

$$J_{\max,0} = 2 \cdot 10^7 \,\mathrm{A/m^2}. \tag{6.66}$$

With the initial maximum current density, the maximum number of turns $N_{\max,0}$ for each of the available cores can be computed. This leads to,

$$N_{\max,0,j} = \begin{cases} 0.95\,\pi\, ID_j \sqrt{\frac{\pi\, J_{\max,0}}{4\, I_{rms}}}, & \text{if } N_{layers} = 1 \\ 0.30\,\pi I D_j^2\, \frac{J_{\max,0}}{4\, I_{rms}}, & \text{if } N_{layers} > 1 \end{cases} \tag{6.67}$$

where j is the index of the core and N_{layers} is the desirable number of layers.

The core database must be set in a way that growing impedance can be obtained with growing index j, which is defined in the range,

$$j = 1 \ldots N_{cores}, \tag{6.68}$$

where N_{cores} is the number of available cores.

With this, the maximum obtainable impedance for each of the cores can be calculated with,

$$Z_{\max,0,j} = 2\,\pi\, f\, AL\, N_{\max,0,j}^2. \tag{6.69}$$

The minimum number of turns to keep the flux density below 80% of the saturation limit at the mains frequency and below the maximum flux density at the switching frequency. Furthermore, the desired inductance value must also be achieved. Thus, three conditions for the minimum number of turns must be fulfilled,

$$N_{\min,0,j} \geqslant \frac{U_s}{2\,\pi\,f_S\,B_{\max,0}\,A_{e,j}} \tag{6.70}$$

$$N_{\min,0,j} \leqslant \frac{0.8\,B_{sat}\,L_{e,j}}{\sqrt{2}\mu_o\,\mu_r\,I_{rms}} \tag{6.71}$$

$$L_{des} \leqslant AL_j\,N^2_{\min,0,j}\,\mu_r(f_{int},\,H = \frac{\sqrt{2}\,N_{\min,0,j}I_{rms}}{l_{e,j}}) \tag{6.72}$$

The third condition, given by eq. (6.72), is re-written as,

$$L_{des} \leqslant AL_j\,N^2_{\min,0,j}\,M_1\frac{\left(\frac{f_{int}}{M_2}+1\right)^{M_4}}{\left(\frac{f_{int}}{M_3}+1\right)^{M_5}}\sqrt{\frac{a+c\,H+e\,H^2}{1+b\,H+d\,H^2}}, \tag{6.73}$$

with,

$$H = \frac{N_{\min,0,j}I_{rms}}{l_{e,j}}. \tag{6.74}$$

An analytical solution for eq. (6.73) is not obtainable, thus, a numerical solution must be found. The final $N_{\min,0,j}$ value must fulfill all three conditions.

The next step is to find the smallest core which fulfills, both, desirable impedance and maximum flux density. This can be accomplished with the algorithm below finding the core in the core database of number $N_{core,0}$.

$$
\begin{aligned}
&N_{core,0} = 0 \\
&j = 1 \\
&\text{while } j \leqslant N_{cores} \text{ do} \\
&\quad N_{core,0} = j \\
&\quad \text{if } (Z_{\max,0,j} \geqslant 2\,\pi\, f_{int}\, Z_{des}) \text{ and } (N_{\min,0,j} \leqslant N_{\max,0,j}) \\
&\qquad \text{then } j = N_{cores} + 1 \\
&\qquad \text{else } j = j + 1 \\
&\quad \text{end if} \\
&\text{end do.}
\end{aligned}
\tag{6.75}
$$

With the found core, the necessary number of turns must be found. This should fulfill the impedance and flux density requirements. The wire diameter can be determined with the following algorithm.

$$
\begin{aligned}
&S_{\min} = \frac{I_{DM,rms}}{J_{\max,0}} \\
&\phi_{\min} = \sqrt{\frac{4\,S_{\min}}{\pi}} \\
&j = 1 \\
&\text{while } j \leqslant N_{wires} \text{ do} \\
&\quad N_{wire,0} = j \\
&\quad \text{if } \phi_{\min} \leqslant \phi_{w,j} \\
&\qquad \text{then } j = N_{wires} + 1 \\
&\qquad \text{else } j = j + 1 \\
&\quad \text{end if} \\
&\text{end do,}
\end{aligned}
\tag{6.76}
$$

where $S_{\min}$ is the minimum wire section to fulfill the maximum current density, $\phi_{\min}$ is the corresponding diameter and N_{wires} is the total number

of wires in the database, which must be organized in a way that the smallest wire diameter corresponds to $j = 1$ and the diameter grows with increasing j.

The required number of turns $N_{req,0}$ can be re-calculated based on the chosen core $N_{core,0}$,

$$N_{req,0} \geqslant \frac{U_s}{2\,\pi\,f_S\,B_{\max,0}\,A_{e,N_{core,0}}} \tag{6.77}$$

$$N_{req,0} \leqslant \frac{0.8\,B_{sat}\,L_{e,N_{core,0}}}{\sqrt{2}\mu_o\,\mu_r\,I_{rms}} \tag{6.78}$$

$$L_{des} \leqslant AL_{N_{core,0}}\,N_{req,0}^2\,\mu_r(f_{int},\,H = \frac{\sqrt{2}\,N_{req,0}I_{rms}}{l_{e,N_{core,0}}}) \tag{6.79}$$

If the maximum number of turns $N_{\max,0,N_{core,0}}$ for the given core is larger than the required number of turns $N_{req,0}$, then the calculation can proceed. If this condition is not fulfilled, then the next core size should be chosen,

$$N_{core,0} = \begin{cases} N_{core,0}, & \text{if } N_{\max,0,N_{core,0}} \geqslant N_{req,0} \\ N_{core,0} + 1, & \text{if } N_{\max,0,N_{core,0}} < N_{req,0} \end{cases}. \tag{6.80}$$

In order to check if the selected core $N_{core,0}$ is able to fulfill all design requirements, the temperature rise must be computed. For this, the total power losses shall be calculated. This can be accomplished with the procedure explained in section 4.4.2 for the calculation of the equivalent resistances and core losses. The total losses are computed in two parts, the losses in the windings P_w and in the core P_c. The total inductor losses is here named $P_{total,0} = P_{w,0} + P_{c,0}$ and shall be multiplied by the core's thermal resistance in order to find the temperature rise ΔT_0,

$$\Delta T_0 = R_{th,N_{core,0}} \cdot P_{total,0}. \tag{6.81}$$

If the temperature rise is under the maximum given by $T_{\max} - T_{amb}$, then the inductor is designed. Otherwise the following iterative procedure can be implemented in order to find the smallest core size that fulfills the specifications.

Finalizing the DM Inductor Design

The iterative procedure presented in the following is implemented in order to find the smallest core size that fulfills the specifications. It employes the data from the previous section as initialization variables.

$j = 0$
while $\Delta T_j \geqslant (T_{\max} - T_{amb})$ do
  if $P_{w,j} \geqslant P_{c,j}$
    then
      $N_{wire,j+1} = N_{wire,j} + 1$
      $N_{req,j+1} = N_{req,j}$
    else
      $N_{wire,j+1} = N_{wire,j}$
      $N_{req,j+1} = N_{req,j} + 1$
  end if
  if $N_{layers} \neq 1$
    then
      $$N_{\max,j+1} = 0.4 \frac{ID^2_{N_{core,j}}}{\phi^2_{ins,N_{wire,j+1}}}$$
    else
      $$N_{\max,j+1} = 0.9 \frac{\pi\, ID_{N_{core,j}}}{\phi_{ins,N_{wire,j+1}}}$$
  end if
  if $N_{req,j+1} \leqslant N_{\max,j+1}$
    then
      calculate $P_{w,j+1}$ and $P_{c,j+1}$
      $\Delta T_j = R_{th,N_{core,j}} \cdot (P_{w,j+1} + P_{c,j+1})$
    else
      $N_{core,j+1} = N_{core,j} + 1$
      $N_{req,j+1} =$

$$
\begin{array}{l}
\max \left\{ \begin{array}{l} N_{req,j} \geqslant \frac{U_s}{2\,\pi\, f_S\, B_{\max,j}\, A_{e,N_{core,j}}} \\ N_{req,j} \geqslant \frac{0.8\, B_{sat}\, L_{e,N_{core,0}}}{\sqrt{2}\mu_o\, \mu_r\, I_{rms}} \\ L_{des} \leqslant A L_{N_{core,0}}\, N_{req,j}^2\, \mu_r(f_{int},\, H = \frac{\sqrt{2}\, N_{req,j} I_{rms}}{l_{e,N_{core,j}}}) \end{array} \right. \\
\qquad\qquad \text{calculate } P_{w,j+1} \text{ and } P_{c,j+1} \\
\qquad\qquad \Delta T_{j+1} = R_{th,N_{core,j}} \cdot (P_{w,j+1} + P_{c,j+1}) \\
\qquad \text{end if} \\
j = j + 1 \\
\text{end do.}
\end{array}
\tag{6.82}
$$

This procedure is employed throughout this work for the design of DM inductors. The models presented in section 4.4 can be employed to derive equivalent circuits which account for parasitic elements. An experimental verification for this design procedure is performed in the testing of the CM inductors and complete filters in sections 4.4 and 8.5.1.

Volume of DM Inductors

With the implementation of the iterative procedure for DM inductors, a series of designs performed in a computer is a simple task. Therefore, in order to evaluate the volume of DM inductors a series of designs has been performed with the following specification:

- Ambient temperature: $T_{amb} = 45^o$C;
- Maximum temperature: $T_{\max} = 100^o$C;
- Maximum current: $I_r = 0.5$ A $\ldots$ 20 A (equally divided in 100 points);
- Frequency of interest: $f_{int} = 150$ kHz;
- Desired inductance at f_{int}: $L_{des} = 1\ \mu$H $\ldots$ 200 μH (equally divided in 100 points).

Thus, a total of 100×100 designs have been performed per core material. In these designs, core losses have been neglected in order to obtain

the dependency of the inductors' smallest possible volume on the rated current and required inductance at 150 kHz.

From the computed volume for each of the designed inductors, a linear regression through least squares has been performed in order to fit the function,

$$Vol_L = k_L \frac{1}{2} L I_r^2, \tag{6.83}$$

to the obtained results. As an example, material High Flux with $\mu_r = 60$ has been chosen and the design results for this material are presented in Figure 6.24. It is observed a good agreement between the fitted function with $k_L = 3.95 \cdot 10^{-3}$ dm^3/J and the design points, validating the choice for this type of function.

The final values computed for the considered magnetic materials are presented in Figure 6.25, where it is seen that only four materials have volumetric coefficients lower than $5 \cdot 10^{-3}$ dm^3/J, namely: MPP with $\mu_r = 60$ and High Flux with $\mu_r = 60$, 125 and 160. The lower permeability materials are preferred since the variation of permeability with DC

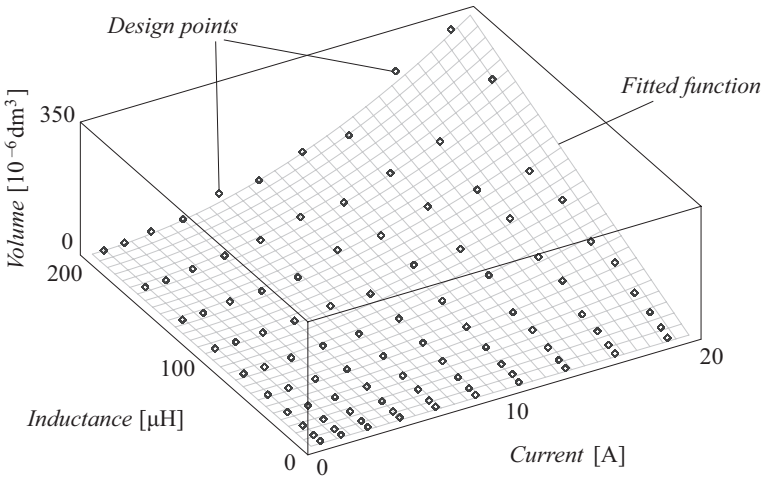


Figure 6.24: Computed volume compared with the fitting function for material High Flux with $\mu_r = 60$.

bias is reduced. For these reasons, materials MPP and High Flux, both with $\mu_r = 60$, are recommended for DM filter inductors of compact size. MPP has the advantages of lower core losses and higher thermal limits. Nevertheless, High Flux is less costly and leads to smaller inductors, thus, being generally preferred.

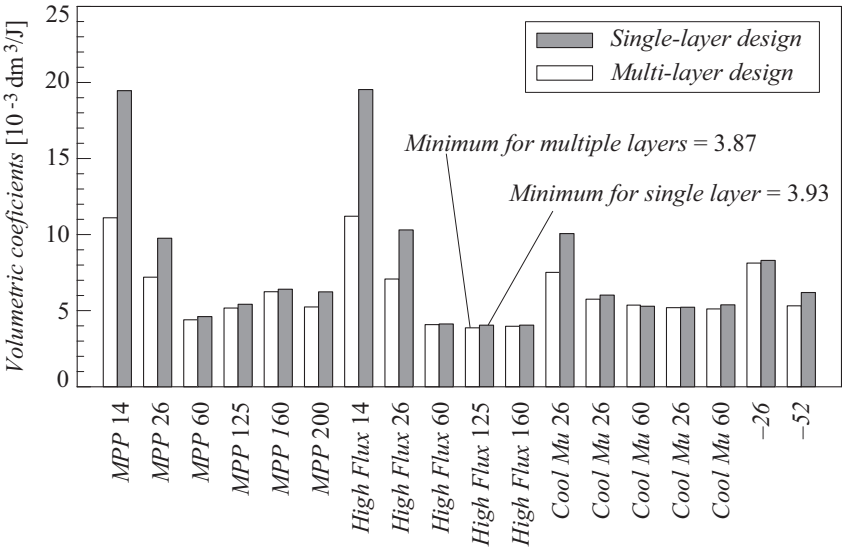


Figure 6.25: Computed volumetric coefficients for DM inductors employing the listed materials.

6.6 Input DM Filter for a Sparse Matrix Converter

In this section, the design of high performance differential mode (DM) input filter for a three-phase ac-DC-ac Very Sparse Matrix Converter (VSMC) [231] (cf. Figure 6.26) is discussed.

The filter design steps presented in section 6.6.1 provide general guidelines being applicable to any current-source type PWM converter system. The design procedure is based on a detailed mathematical model of the

test receiver for measuring conducted emissions (CE) in the frequency range of 0.15...30 MHz (cf. section 2.5). As verified by the experimental analysis shown in section 6.6.2 employing the three-phase common-/differential-mode (CM/DM) noise separator discussed in section 5.3, this allows an accurate prediction of the converter behavior regarding DM emissions. Accordingly, compliance to applicable EMC standards can be ensured already in the design process what represents an important step towards a virtual prototyping of the converter system resulting in shorter total design time and/or reduced overall development costs.

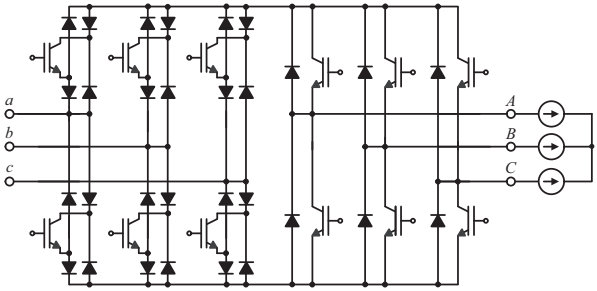


Figure 6.26: Basic structure of a three-phase ac-DC-ac Very Sparse Matrix Converter (VSMC).

6.6.1 Filter Design Procedure

Figure 6.27 illustrates the design steps in graphical form. It is seen that the design procedure is based on the estimation of the input current spectrum of the power converter. This is done because the DM currents at the input of a Matrix Converter are imposed by the given modulation and do not appreciably change with the inclusion of an input filter.

Applicable Standards and Limits for Emission

As a first step of the filter design one has to specify the admissible maximum DM conducted emission levels with reference to relevant EMC standards taking into consideration the type of equipment, the region and the environment where it will be utilized. Usually specific regulations for the

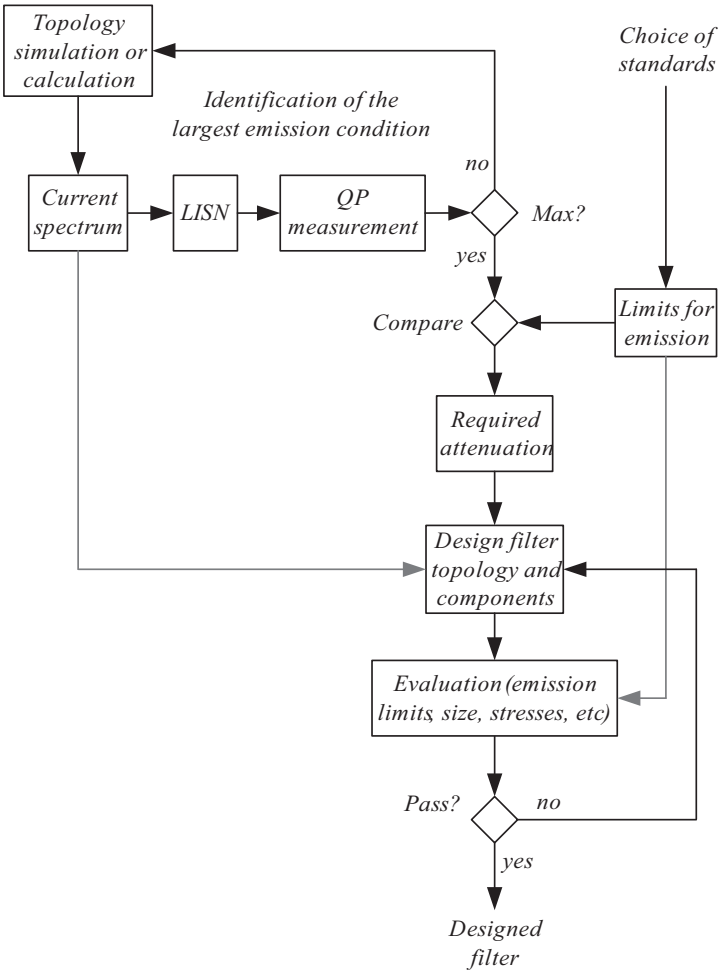


Figure 6.27: Differential mode input filter design procedure shown in graphical form.

equipment at hand are applied and in case no specific standard is available, generic standards are employed. In this procedure the focus is put on the frequency range of 0.15...30 MHz, the measurement techniques defined in CISPR 16 [104] and the emission limits for drive systems defined in EN 61800-3, Tab.6 [110] which are in the case at hand identical to CISPR 11, class B [105].

Identification of the Worst Case Operating Condition

As a basis for defining the required filter attenuation the largest emission condition in the frequency band of interest has to be identified. There, one has to analyze the input current frequency spectrum of the converter in the whole operating range, i.e. for varying modulation depth, output power, input and output frequencies and further parameters which might take influence on the spectral composition of the input current.

The DM conducted emissions for the VSMC are due to the discontinuous input currents with pulse frequency. For a Sparse Matrix Converter the following variables are taking direct influence on the high-frequency input current harmonics: (1) type of load, where for purely resistive load the highest output current ripple and/or the highest input current harmonics are observed. However, as the main application of the converter is for adjustable speed drives this is not considered further but an inductive load (sinusoidal output current) is assumed in the following; (2) modulation index (M) where the highest amplitudes of the input current harmonics are occurring around $M = 0.5$; (3) the output frequency (f_2), where the switching frequency harmonics are increasing with increasing

Table 6.7: Parameters employed in the simulation, which reflects the worst case for the conducted emissions.

Parameter	*Employed value*
Input RMS line voltages (U_1)	3×400 V
Modulation index	$M = 0.5$
Output frequency	$f_2 = 200$ Hz
Output power	$P_2 = 3.75$ kW
Current displacement angle	$\phi_2 = 30^\circ$

output frequency. Accordingly, the worst case conditions for the following digital simulations are given in Table 6.7.

The spectrum of the simulated converter input current resulting for this operating point is depicted in Figure 6.28. With zooms around the first switching frequency harmonic (cf. Figure 6.29) and at the first harmonic inside the measurement range (cf. Figure 6.30).

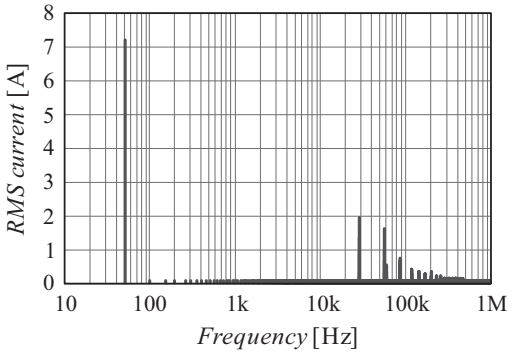


Figure 6.28: Frequency spectrum of the converter input current I_{dm}.

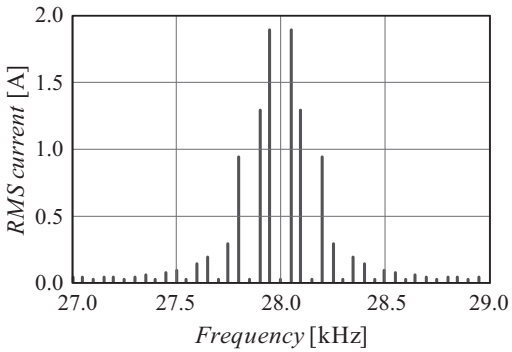


Figure 6.29: Frequency spectrum of the converter input current I_{dm} – zoom around the switching frequency at 28 kHz.

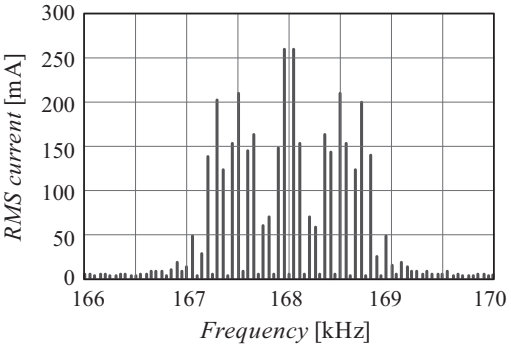


Figure 6.30: Frequency spectrum of the converter input current I_{dm} – zoom around the first switching frequency harmonic being located in the frequency range 0.15...30 MHz (at 160 kHz).

Converter Single-Phase Equivalent Circuit

Due to the phase symmetry of the converter topology and the control and the missing connection of the converter power circuit to the mains neutral the filter design can be restricted to a single-phase equivalent (cf. Figure 6.31), i.e. the converter can be replaced in the following steps by a single phase current source with a current spectrum defined by the simulated worst case operating condition.

LISN and Test Receiver

A simplified mid- to high-frequency (0.15 to 30 MHz) equivalent circuit of the LISN according to CISPR 16 is shown in Figure 6.31. The voltage u_{meas} at the LISN output is applied to an EMC test receiver or appropriate spectrum analyzer ($R_{LISN} = 50\,\Omega$ is the input resistance of the test receiver). For determining the measured voltage spectrum of u_{meas} the converter current spectrum $I_{dm}(j\omega)$ is multiplied by the LISN's transfer-function (cf. section 2.5.1).

The input signal (u_{meas}) of the receiver is processed according to CISPR 16 in a test receiver. Details on the modeling of the test receiver are given in section 2.5.2.

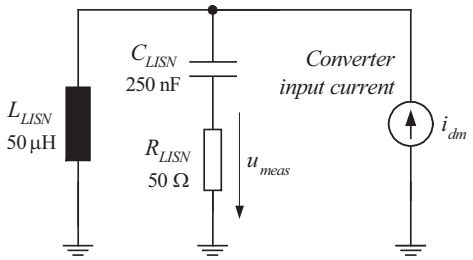


Figure 6.31: Simplified high-frequency model considered for determining the conducted emissions. The converter is replaced by a current source i_{dm}; no input filter is present. Based on the measurement results the required filter attenuation is calculated.

Calculation of Required Attenuation

Due to the low time constant the measured Video filter output voltage $u_{F,0}$ is close to the average value of $u_{QP,0}$ and in the case at hand for $MB = 150$ kHz it is,

$$u_{F,0} = u_{QP,0,avg} = 35.7\,\text{V} = 151\,\text{dB}\mu\text{V}. \tag{6.84}$$

By comparing the result to the limits specified for f = 150 kHz, the required attenuation of the input filter including a margin of 6 dB is calculated as,

$$\begin{aligned} Att_{req}\,[\text{dB}] =& U_{meas,0,150\text{kHz}}\,[\text{dB}\mu\text{V}] - Limit_{CISPR,150\text{kHz}}\,[\text{dB}\mu\text{V}] + \\ &+ Margin\,[\text{dB}\mu\text{V}] = 91\,\text{dB}. \end{aligned} \tag{6.85}$$

Selection of the Filter Components

In order to achieve the required attenuation a two-stage filter as shown in Figure 6.32 is employed where *Section 1* is formed by $C_1 - L_1 - L_{1d}$, and *Section 2* is formed by C_2 and the inner impedance of the LISN/test receiver (Z_{LISN}).

For the filter dimensioning several degrees of freedom (basically, the

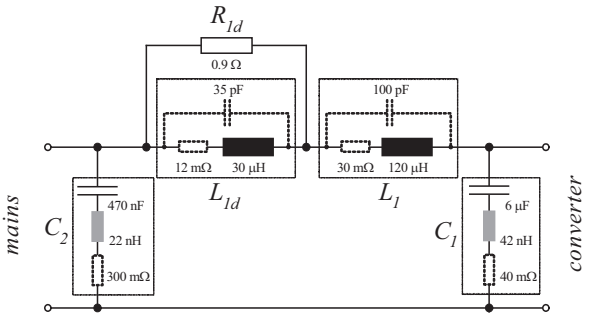


Figure 6.32: Input filter single-phase equivalent circuit providing the required attenuation including the parasitics of the inductive and capacitive elements.

positioning of cut-off frequencies and the type and extent of damping) are given and some nonlinear restrictions (like discrete available capacitance values, the maximum admissible output impedance, the maximum admissible reactive power – which defines the current consumption at no load – and maximum current and voltage stresses) have to be considered.

Furthermore, the parasitics of the filter components have to be taken into account. Therefore, the dimensioning can not be in closed form, but has to be performed recursively, starting with the determination of the ranges of the component values.

i. Capacitor C_1

   The capacitor C1 is placed directly at the rectifier input and is selected such that the voltage ripple peak-to-peak value is limited to about $\pm 5 \ldots 8$ % in order to prevent a distortion of the output voltage and to limit the voltage stress on the power semiconductors. In the case at hand this translates into $C_1 = 4 \ldots 8\,\mu$F.

ii. Inductor L_1

   Both filter sections are contributing to the required filter attenuation. For stability reasons the attenuation of *Section 1* has to be higher than that of *Section 2*, which leads to a lower cut-off frequency of *1* compared to *2* [222]. Usually, $f_{cutoff,sec1} \approx 0.1 \cdot f_{cutoff,sec2}$ is an advantageous selection, which results in an attenuation range for *Section 1* of $Att_{sec1}[\text{dB}] = 0.6 \ldots 0.7 \cdot Att_{req}[\text{dB}]$. With,

$$f_{cutoff,sec1} = \frac{150\,\text{kHz}}{\sqrt{10^{\frac{Att_{sec1}[\text{dB}]}{20}}}} = \frac{1}{2\pi\sqrt{L_1 C_1}}. \tag{6.86}$$

iii. Inductor L_{1d}

The inductor L_{1d} is normally determined by the damping ratio, $n = L_{1d}/L_1$, which should be selected only high enough in order to provide sufficient damping. A high value of n would provoke high filter output impedance which would take influence on the converter stability (for higher filter output impedances the stability of the converter control is more difficult to ensure [219, 220]). Here $n = 0.1 \ldots 0.5$ is selected and accordingly $L_{1d} = 7.6 \ldots 215\,\mu\text{H}$ is obtained.

iv. Damping Resistor R_{1d}

For an optimum damping of the filter resonance R_{1d} has to be selected according to,

$$R_{1d} = \sqrt{\frac{L_1}{C_1}}\frac{1+n}{n}\sqrt{\frac{(2+n)\cdot(4+3n)}{2\cdot(1+n)\cdot(4+n)}}, \tag{6.87}$$

which is only valid for the filter topology at hand, for other topologies details can be found in [219, 221].

v. Capacitor C_2

The second stage of the filter (*Section 2*) is formed by the capacitor C_2 in combination with the LISN/test receiver network ($R_{LISN} = 50\,\Omega$, $L_{LISN} = 50\,\mu\text{H}$, $C_{LISN} = 250$ nF and has to provide an attenuation of $Att_{sec2}[\text{dB}] = Att_{req}[\text{dB}] - Att_{sec1}[\text{dB}]$ at $MB = 150$ kHz. This directly determines the value of C_2.

vi. Optimization and Final Selection of Filter Components

After determining the ranges for all filter components as described above, a recursive optimization process has to be followed considering the following points:

- Total gain value ($U_{meas}/I_{dm} \rightarrow Att_{req}$). This transfer function has to include finally all parasitics of the inductors and capacitors. As presented in Figure 6.32, inductors are modeled including a series resistance and a parallel capacitance and capacitors

are modeled including a series resistance and a series inductance. In the case at hand the influence of the parasitics is about 1.72 dB at 150 kHz but will be more pronounced at higher frequencies.

- The maximum energy in the inductors and in the capacitor should be minimized in order to ensure a low overall filter volume, i.e.,

$$E_L = \frac{1}{2} L\, I_{max}^2 \rightarrow \min \tag{6.88}$$

$$E_C = \frac{1}{2} C\, U_{max}^2 \rightarrow \min. \tag{6.89}$$

- Losses P_{R1d} in the damping resistor should be minimized for ensuring a high efficiency of the energy conversion.

Obviously, not all design requirements can be met simultaneously, so design priorities have to be defined in accordance to the application.

Some characteristic values of the filter designed in this paper are compiled in Table 6.8.

For certain applications it could be useful to insert additional filtering elements, e.g. an input inductor which defines the filter characteristic also for large tolerances of the inner mains impedance. In order to avoid a resonance with C_2 there another damping network has to be provided.

Table 6.8: Characteristic values of the proposed filter.

Characteristic	*Value*
Input current displacement angle for nominal load	-4.3°
Power factor cosϕ for nominal load	0.997
Maximum capacitor charge of C_1	2.0 mC
Maximum inductor energy of L_1	4.4 mJ
Maximum fundamental reactive power of C_1	-165.8 VAr
Maximum fundamental reactive power of L_1	4.9 VAr
Maximum power losses of R_{1d}	300 mW

Test and Evaluation of the Design

The QP detected averaged values $U_F(j\omega)$ resulting form the simulation model are depicted for selected frequency values in Figure 6.33 (marked by $\times$). It can be seen that the resulting emission values are well below the Class B limit. At $f_{meas} = 150$ kHz the selected margin of 6 dB margin can be observed.

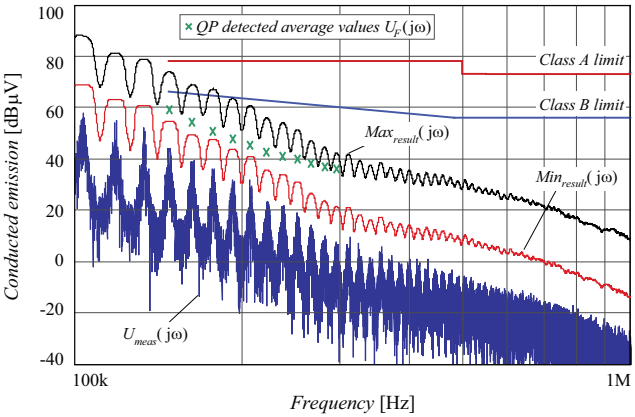


Figure 6.33: Simulation of a quasi-peak measurement compared to the spectrum of the voltage $U_{meas}(j\omega)$ at the LISN output terminals. Furthermore shown: Minimum ($Min_{result}(j\omega)$) and maximum ($Max_{result}(j\omega)$), signal levels resulting from QP detection, and conducted emission limits according to CISPR 22, Classes A and B.

Furthermore, Figure 6.33 clearly shows that amplitudes of individual harmonics of the LISN output voltage are far below the value obtained with the QP weighting measurement (approximately 15 dB at 150 kHz). This underlines the importance of a proper modeling for the measurement system. For this reason, a filter design procedure relying only on a LISN modeling and considering only the amplitudes of individual harmonics would not be sufficient unless large design margins are provided.

As can also be seen from Figure 6.33 the predicted quasi-peak values are always lying between a lower $Min_{result}(j\omega)$ and an upper limiting curve $Max_{result}(j\omega)$ as proposed in section 2.5.3.

The filter attenuation curve $I_{mains}(j\omega)/I_{dm}(j\omega)$ being present in case the VSMC is connected to the mains shows two main resonances (cf. Figure 6.34). The resonant frequencies are defined by the filter parameters in connection with the inner mains impedance, which is assumed as $L_{mains} = 50\,\mu$H in this case. It is also seen, that the parasitics of the filter elements are taking influence on the filter attenuation beyond 300 kHz.

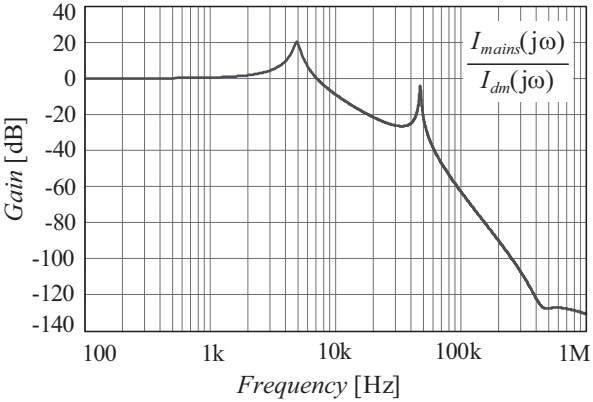


Figure 6.34: Filter frequency response – transfer function from the noise current to the LISN current.

Figure 6.35 shows that for employing the proposed input filter a sinusoidal shape of the mains current is obtained. As verified by the experimental analysis the mains current ripple in practice shows a lower value. This is due to ohmic components of the inner mains impedance and due to core losses of the inductive filter components.

6.6.2 Experimental Verification

In the following the experimental verification of the input filter design will be presented based on quasi-peak conducted emission measurements according to CISPR 11 and EN 61800-3 as described above.

For conventional EMC compliance testing DM and CM mode emissions cannot be separated. Therefore, the three-phase DM/CM noise separator presented in section 5.3 has been used in order to allow an evaluation of the DM input filter design procedure.

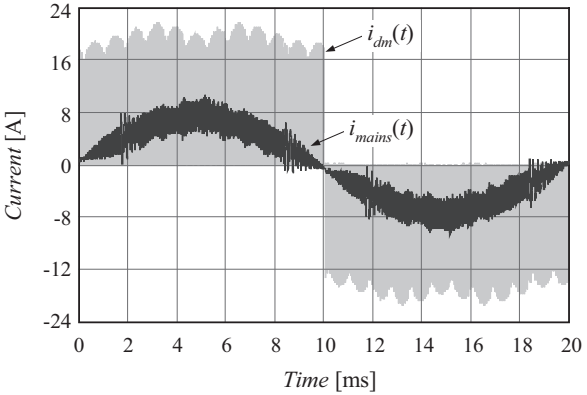


Figure 6.35: Time behavior of the converter input current $i_{dm}(t)$ compared with the calculated mains current $i_{mains}(t)$ for an inner mains impedance of $L_{mains} = 50\,\mu$H.

A verification of the input filter design described in the previous sections was carried out experimentally according to CISPR 11 using the setup shown in Figure 6.36. The measurement equipment used is listed in Table 6.9. One has to note that parasitic circuit elements (like impedances of the cables connecting the EUT and the load, impedances of the connections to safety ground, etc.) which are not shown in Figure 6.36 could take significant influence on the measurement result by forming resonant circuits for common-mode current circulation and/or coupled circuits. These must be considered by proper arrangement of LISN, EUT, cables and load.

Table 6.9: Measurement equipment employed in the test setup.

Qty.	*Equipment*	*Specification*
1	Test receiver Rohde & Schwarz - ESPI	9 kHz ... 3 GHz
2	LISN Rohde & Schwarz - ESH3-Z5	Two-lines, V-network
1	LISN Rohde & Schwarz - ESH2-Z5	Four-lines, V-network

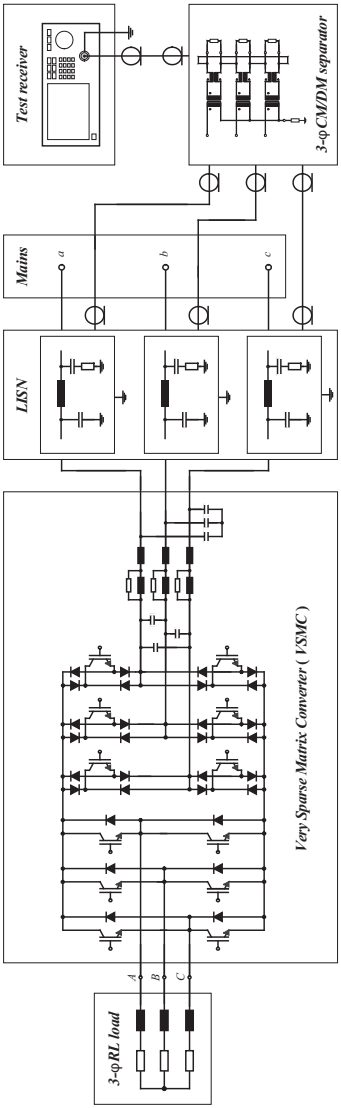


Figure 6.36: Conducted emission test setup employing the proposed three-phase CM/DM noise separator.

The specifications of the VSMC prototype are as follows:

Input (3-ϕ ac):

- Input RMS line voltages: (U_1) 3×400 V $\pm 20\%$
- Maximum input RMS phase current: $I_{1,max} = 18$ A
- Mains frequency: $f_1 = 50$ Hz
- Current displacement angle: $\phi_1 = 0°$

Output (3-ϕ ac):

- Output RMS line voltages (U_2): $3 \times 0 - 400$ V
- Maximum output power: $S_2 = 7.5$ kVA ($M = 1$)
- Output frequency: $f_2 = 0 - 200$ Hz
- Current displacement angle: $\phi_2 = 0°$ - $90°$
- Switching frequency: $f_p = 15$ kHz

Since no three-phase LISN with simultaneously accessible phase outputs was available for the tests the VSMC prototype supplying a three-phase RL star-connected load was fed via three individual LISNs (cf. Table 6.9). An analog power amplifier with low inner impedance was used for simulating the mains so that the conditions were close to the conditions assumed for simulating the system.

For analyzing the worst-case condition the modulation index was set to $M = 0.5$. The output frequency $f_2 = 200$ Hz was selected. The power consumption of the three-phase load ($R_{load} \cong 8.7\,\Omega$ in series with $L_{load} \cong 150$ mH) was measured as 3.2 kW.

The components employed in the input filter are listed in Table 6.10.

The level of the DM emissions taken from one DM output and recorded in quasi-peak detection mode is depicted in Figure 6.37. The emission level is below the limit defined by CISPR 11 class B up to 5 MHz and the levels for 150 kHz are close to the predictions.

The differences to the simulated DM noise characteristic (cf. Figure 6.33) are due to several reasons as listed in the following:

Table 6.10: Input filter components.

Qty.	*Component*	*Specification*
6	Capacitor	Evox-Rifa - PHE844 R, 1 μF / 440 Vac
3	Capacitor	Evox-Rifa - PHE840 M, 470 nF / 275 Vac
3	Inductor	Micrometals - T184-52, 41 turns / 2 mm^2
3	Inductor	Micrometals - T184-52, 12 turns / 2 mm^2
3	Resistor	0.82 / 5 W

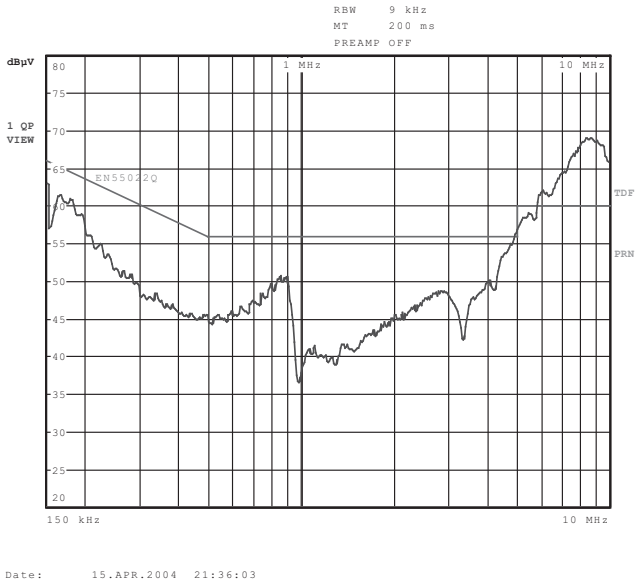


Figure 6.37: Measured conducted emission levels at a DM output of the three-phase CM/DM noise separator.

1. The CM/DM separator has a finite CM rejection ratio (CMRR) which changes with frequency and is around -40 dB @ 150 kHz. That means that in practice CM emissions ($\approx$ 80 dBμV @ 150 kHz) are taking influencing on the DM measurement. Due to the decreasing CMRR

this effect is pronounced at higher frequencies what explains the higher DM emission levels measured for frequencies higher than 5 MHz.

2. A resonance was present in the CM path at $f \approx 850$ kHz what can be seen in the increased DM levels at this frequency (again due to the limited CMRR).

3. Due to tolerances of the filter capacitances a lower filter attenuation than simulated was achieved; furthermore, the tolerances are causing an asymmetry of the filter which results in a transformation of CM into DM noise.

4. The output inductors used in the course of the test were smaller than for the simulations what leads to higher output current ripple and therefore higher input current switching frequency harmonics.

Taking all this into account the experimental result is in good correspondence with the simulations and verifies the proposed dimensioning procedure.

6.7 Minimum Volume DM Filter for a Three-Level Rectifier

The objective of this section is to design DM filters which are able to fulfill conducted emission regulations, while presenting minimum volume. Thus, filters that allow for the highest power density. The filter design procedure is proposed for a Three-Phase Three-Level Six-Switch Boost PWM Rectifier as depicted in Figure 6.38 [78, 131]. This rectifier has an output power of 10 kW, power density of 8 kW/dm^3, switching frequency $f_s = 400$ kHz, output voltage $U_o = 760$ V, input voltage $U_{N1} = 230$ V and is forced air-cooled. The EMC filter for this system must be designed to fulfill EMC requirements, where an attenuation specification, based on the estimated CE levels of the rectifier, is calculated. Furthermore, the filter shall be designed taking into account the limits for CE specified for Class B information technology (IT) equipments as in CISPR 22.

The filter design is based on the simplified models presented in section 3.4, where equivalent circuits are defined and used to evaluate CM and DM noise sources. The filter topology used for the DM design is shown

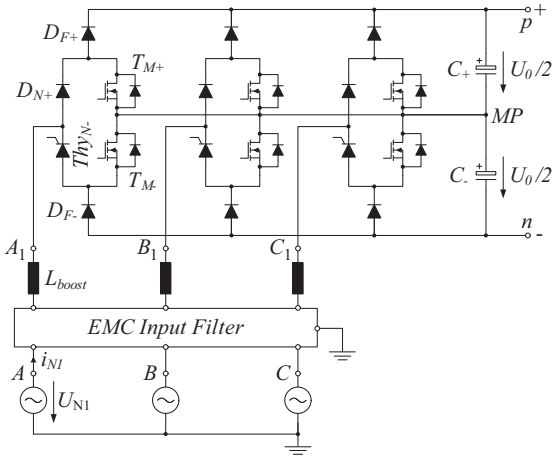
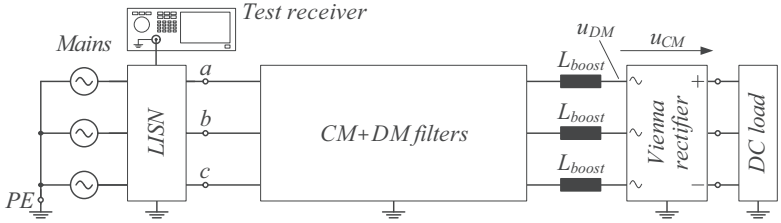


Figure 6.38: Circuit schematic of a Three-phase, Six-switch, Three-level Rectifier topology used to implement a 10 kW PWM rectifier.

as a single-phase equivalent in Figure 6.39. Three-stages are chosen based on the power level and attenuation requirements [215]. Components are chosen based on a series of requirements as given in section 4.

Besides that, the inclusion of the filter generates a displacement in the input currents. Assuming that the rectifier presents resistive behavior and that the inductors show low impedances at the line frequency, at light load the capacitive currents drained by the capacitors generate leading currents in the mains and a limit for the displacement angle constrains the maximum capacitance value. In this work, the maximum input current displacement angle is set to $\Phi_{in,\max} = 5^o$ for an output power of 10%, what means a power factor higher than 0.995.

On the other hand, capacitors $C_{DM,1}$ limit the voltage ripple at the input of the converter and a minimum amount of capacitance is required for the proper operation of the PWM converter in the sense that multiple stages of filters are employed and the voltage measurement for the control of the converter must be performed with low ripple. For this reason, the allowable voltage ripple at the input of the power converter is limited to $\Delta U_{N1,\max} \leqslant 5\%$ of the peak rated phase voltage. The input capacitors $C_{DM,1}$ can be calculated with the approximation,



DM equivalent circuit

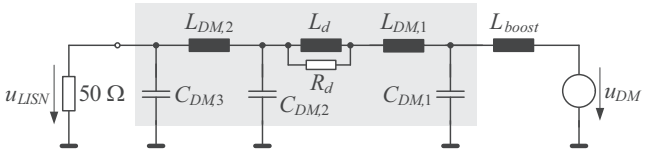


Figure 6.39: Standard test setup for conducted emission and simplified equivalent circuit for differential mode. The DM filter topology is also shown.

$$C_{DM,1} \geqslant \frac{\Delta I_{N1,\max}}{8\, f_s\, \Delta U_{N1,\max}}, \tag{6.90}$$

where $\Delta I_{N1,\max}$ is the maximum current ripple in the boost inductors. Assuming,

$$\Delta I_{N1,\max} = 0.25(\sqrt{2} I_{N1}) \cong 5.3A \tag{6.91}$$

$$\Delta U_{N1,\max} = 0.02(\sqrt{2} U_{N1}) \cong 6.5V \tag{6.92}$$

$$f_s = 400\,\text{kHz}, \tag{6.93}$$

the minimum value for the input capacitors is $C_{DM,1} \geqslant 260$ nF.

Minimum inductance for the boost inductors is required for the normal operation of the rectifier. For this design the allowable switching frequency ripple is $i_{boost,\max} = 25$ % of the peak input current $I_{N1,peak}$. High frequency losses can not be neglected and the design aims in minimizing overall losses. A calculation of the optimal point can be done [232] and is omitted here as it is not on the scope of this work. Nevertheless,

the boost inductors can be designed for,

$$L_{boost} \geqslant \frac{0.7U_o/2}{6\, f_s\, \Delta I_{N1,\max}} \cong 23\,\mu\text{H}. \tag{6.94}$$

The DM currents are composed of a large component at the mains frequency and a relatively small high frequency ripple due to the attenuation given by the boost inductors and capacitors $C_{DM,1}$. For this reason, the cross sectional area of the core A_e is determined by saturation and not by core losses. Furthermore, the high frequency losses in the winding are also comparatively small and can be neglected. The other parameter that defines the core is the required winding area A_w.

The filter inductance $L_{DM,i}$ and rated current are related to the size of the inductor $A_e A_w$ (core area product) by,

$$L_{DM,i}\, I_{N1,peak}\, I_{N1,rms} = k_w J_{\max} B_{peak} A_e A_w. \tag{6.95}$$

The volume of the filter inductor V_L is calculated with,

$$V_L = k_{geo}(A_e A_w)^{\alpha_{geo}}. \tag{6.96}$$

There, the parameters k_{geo} and α_{geo} account for the geometry of the core (toroidal, planar, etc). Assuming that a dimension grows proportionally with the other ones, α_{geo} is usually taken as $3/4$.

To choose an appropriate material for the cores the comparison of core materials done in section 4.4 for different types of iron powder materials is observed. From the comparison, material High Flux is chosen with a initial permeability of $\mu_r = 160$. The results from section 6.5 suggest that the volume of this type of inductor is proportional to its stored energy. Furthermore, the volumetric coefficient for the material High Flux with $\mu_r = 160$ is given by,

$$k_L \cong 3.95 \cdot 10^{-3} \frac{\text{m}^3}{\text{H} \cdot \text{A}^2}. \tag{6.97}$$

The volume of the capacitors to be used in the filters is approximated by a curve generated by Minimum Square fitting of the volumes calculated for commercially available X2 type capacitors (cf. section 4.3). The approximation curves along with the calculated values for discrete capac-

itors also suggest a volume dependency with the stored energy. Surface mount devices are chosen, which are rated as X2 capacitors [160], which volumetric coefficient is,

$$k_{C,X2,cer} \cong 16.4 \cdot 10^{-6} \frac{\mathrm{m}^3}{\mathrm{F} \cdot \mathrm{V}^2}. \tag{6.98}$$

Assuming that the volume of the components is directly related to their stored energy, the volumetric coefficients for inductors k_L and capacitors k_C are defined as in

$$Vol_L = k_L \, L_{DM,i} \, I_{N1}^2 \tag{6.99}$$

$$Vol_C = k_{C,X2,cer} \, C_{DM,i} \, U_{N1}^2. \tag{6.100}$$

The minimization of the volume can then be performed with the following procedure.

6.7.1 Analytical Volume Minimization of DM Filters

Two equations define the volume minimization problem, the attenuation at the frequency of interest f_{int}, that represents the main constraint, and the filter volume, which shall be minimized.

An asymptotic approximation of the attenuation Att, for frequencies much higher than the corner frequency, is used,

$$\frac{1}{Att(f_{int})} \cong (2\pi \cdot f_{int})^6 \cdot L_{boost} \cdot \prod_{i=1}^{2} L_{DM,i} \cdot \prod_{i=1}^{3} C_{DM,i}. \tag{6.101}$$

What is left to derive is the individual values for the components $L_{DM,i}$ and $C_{DM,i}$. Starting from a general filter as shown in Figure 6.40, a relation between the components can be found as in the following.

The attenuation for the multi-stage LC filter of Figure 6.40 is approximated for frequencies much higher than the cutoff frequency of the filter by,

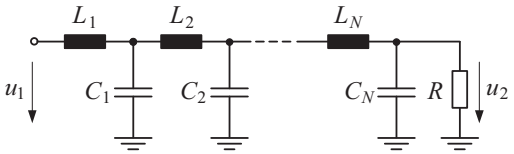


Figure 6.40: Multi-stage LC filter configuration.

$$Att\,(\omega)|_{\mathrm{HF}} = \left|\frac{U_2(\omega)}{U_1(\omega)}\right| = \frac{1}{\omega^{2N} \cdot \prod_{j=1}^{N} L_j \cdot \prod_{j=1}^{N} C_j}. \tag{6.102}$$

Assuming that the capacitors C_j are known and that a given attenuation Att_{req} is required at a frequency ω_{req}, equation eq. (6.102) can be rewritten,

$$\frac{1}{Att_{req} \cdot K_g} = \prod_{j=1}^{N} L_j, \tag{6.103}$$

where,

$$K_g = \omega_{req}^{2N} \cdot \prod_{j=1}^{N} C_j. \tag{6.104}$$

A maximum inductance L_{max} is defined as the sum of all inductors L_j,

$$L_{max} = \sum_{j=1}^{N} L_j. \tag{6.105}$$

Supposing that all inductors have the same value, then,

$$L_j = \frac{L_{max}}{N}, \tag{6.106}$$

and the attenuation is given by,

$$\frac{1}{Att_{req} \cdot K_g} = \left(\frac{L_{max}}{N}\right)^N. \tag{6.107}$$

Having the premise that one of the inductors has a different value L_{dif}, defined by,

$$L_{dif} = \frac{k_{dif} \cdot L_{max}}{N} \tag{6.108}$$

$$L_j = L_{max} \cdot \frac{N - k_{dif}}{N \cdot (N-1)}, \tag{6.109}$$

with $k_{dif} \geqslant 0$.

The attenuation equation for this new condition is,

$$\frac{1}{Att_{req} \cdot K_g} = \frac{k_{dif} \cdot (N-1)}{N - k_{dif}} \cdot \left(\frac{L_{dif} \cdot (N - k_{dif})}{K \cdot (N-1)}\right)^N. \tag{6.110}$$

Dividing equation eq. (6.110) by eq. (6.107) leads to the ratio $R(N, k_{dif})$ (cf. equation eq. (6.111)) between the attenuation obtainable for both situations, which is graphically shown in Figure 6.41.

$$R(N, k_{dif}) = k_{dif} \cdot \left(\frac{N - k_{dif}}{N-1}\right)^{N-1}. \tag{6.111}$$

Differentiating $R(N, k_{dif})$ with respect to k_{dif} leads to,

$$\frac{\partial R(N, k_{dif})}{\partial k_{dif}} = -\frac{(N-1)(k_{dif}-1)}{(k_{dif}-N)^2} \cdot \left(\frac{N - k_{dif}}{N-1}\right)^K. \tag{6.112}$$

Equating this result to zero leads to the maximum achievable attenuation,

$$\frac{\partial R(N, k_{dif})}{\partial k_{dif}} = 0 \Rightarrow k_{dif,optimum} = 1. \tag{6.113}$$

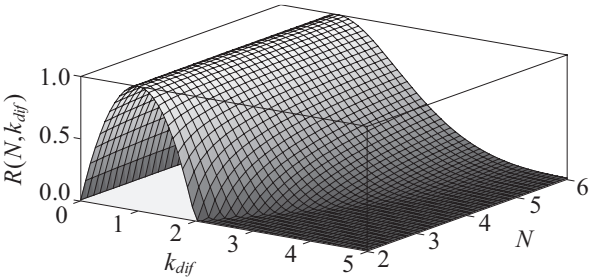


Figure 6.41: Ratio $R(N, k_{dif})$ between the attenuation obtainable with all inductors equal and the one for when a single inductor presents a different value.

As observed in equation eq. (6.113), k_{dif} equal to unity leads to the highest attenuation independent on the number of LC stages. That means that the maximum high frequency attenuation, for a given L_{max}, is achieved for equal components in all stages, since the structure of equation eq. (6.102) is the same for, both, inductances and capacitances. For the lower total inductance, each of the individual inductors have the same value $L_{DM,i} = L_{DM}$ and this is valid for the capacitors $C_{DM,i} = C_{DM}$. Thus, two variables are left to minimize the volume. The required attenuation Att_{req} equation (cf. eq. (6.101)) is simplified to,

$$\frac{1}{Att_{req}} \cong (2\pi \cdot f_{int})^6 \cdot L_{boost} \cdot L_{DM}^2 \cdot C_{DM}^3. \tag{6.114}$$

Requirements related to control issues must also be considered and, in order to provide passive damping that cause minimum losses and avoiding oscillations, RL networks are included in the choice of the topologies. Considering a damping network as shown in Figure 6.42, where the inductor $L_{DM,d}$ of the damping network has the same value as the filtering inductor L_{DM}, the number of inductors in the first filter stage is doubled and the total volume of the filter Vol_{DM} is given by,

$$Vol_{DM} = 9 \cdot (Vol_L + Vol_D) + 3 \cdot Vol_{L_{boost}}. \tag{6.115}$$

Replacing eq. (6.99) and eq. (6.100) in eq. (6.115),

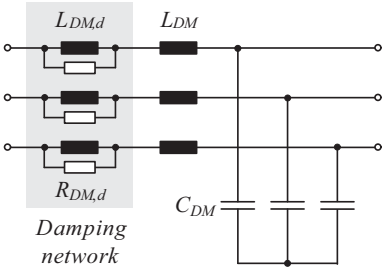


Figure 6.42: Three-phase filter stage with damping network.

$$Vol_{DM} = 9 \cdot \left(k_L \cdot L_{DM} \cdot I_{N1}^2 + k_C \cdot C_{DM} \cdot U_{N1}^2\right) + 3 \cdot Vol_{L_{boost}}. \quad (6.116)$$

Rearranging eq. (6.114) in terms of L_{DM} and replacing it in eq. (6.116),

$$Vol_{DM} = \frac{9 k_L I_{N1}^2}{(2\pi f_{\text{int}})^3 \sqrt{L_{boost} C_{DM}^3}} + 9 k_C C_{DM} U_{N1}^2 + 3 Vol_{L_{boost}} \quad (6.117)$$

The solution for a minimal volume is given for,

$$\frac{\partial Vol_{DM}}{\partial C_{DM}} = 0, \quad (6.118)$$

and the final values for the components are given by,

$$C_{DM} = \frac{I_{N1}}{4\pi \cdot f_{int} \cdot U_{N1}} \cdot \sqrt[5]{\frac{36 \cdot k_L^2 \cdot U_{N1}}{\pi \cdot f_{int} \cdot L_{boost} \cdot Att_{req} \cdot k_C^2 \cdot I_{N1}}} \quad (6.119)$$

$$L_{DM} = \frac{U_{N1}}{6\pi \cdot f_{int} \cdot I_{N1}} \cdot \sqrt[5]{\frac{36 \cdot k_C^3 \cdot U_{N1}}{\pi \cdot f_{int} \cdot L_{boost} \cdot Att_{req} \cdot k_L^3 \cdot I_{N1}}} \quad (6.120)$$

Thus, minimal volume filters can be designed based on the ratings of the components and the required filter attenuation assuming that para-

sitic elements do not strongly influence the attenuation at the frequency of interest, which is typically valid. This minimization procedure eliminates the need for a numerical optimization procedure [44,217], thus simplifying the design of minimum volume EMC filters.

6.7.2 Filter Design

The DM filter design procedure is presented in the block diagram of Figure 6.43. It is seen that after the main components are defined and respect given constraints, damping is considered and the values of the leakage inductance of CM chokes is deducted from the required inductance to design the DM inductors.

As seen in Figure 6.43, the maximum amount of capacitance C_{max} per phase is limited due to the required power factor at light load. For the case at hand the maximum input displacement angle is $\Phi_{in,\max} = 5^o$ for 10% load. From this condition and considering that the filter inductors do not notably cause current displacement it follows that,

$$C_{max} = \sum_{i=1}^{3} C_{DM,i} \leqslant \frac{3P_{\min}\Phi_{in,\max}}{2\pi\, f_N\, U_{N1}^2}, \tag{6.121}$$

from where, considering $f_N = 50$ Hz, $U_{N1} = 230$ V, $P_{\min} = 0.1 \cdot 10$ kW,

$$C_{max} \cong 5.3\,\mu\text{F}. \tag{6.122}$$

The boost inductors have the value of $L_{boost} \cong 30\,\mu$H.

From the predicted conducted emission levels computed in section 3.4, the required attenuation for the filtering circuits is,

$$Att_{req,DM,\text{dB}}(f_{int}) = -115 \text{ dB} \ @ \ f_{int} = f_s = 400 \text{ kHz}, \tag{6.123}$$

in order to fulfill CISPR 22 Class B requirements with a 6 dB margin.

From eq. (6.123), the required attenuation in absolute numbers is,

$$Att_{req} \cong 1.778 \cdot 10^{-6} \ @ \ f_{int} = f_s = 400 \text{ kHz}. \tag{6.124}$$

The rated current for the inductor is given by,

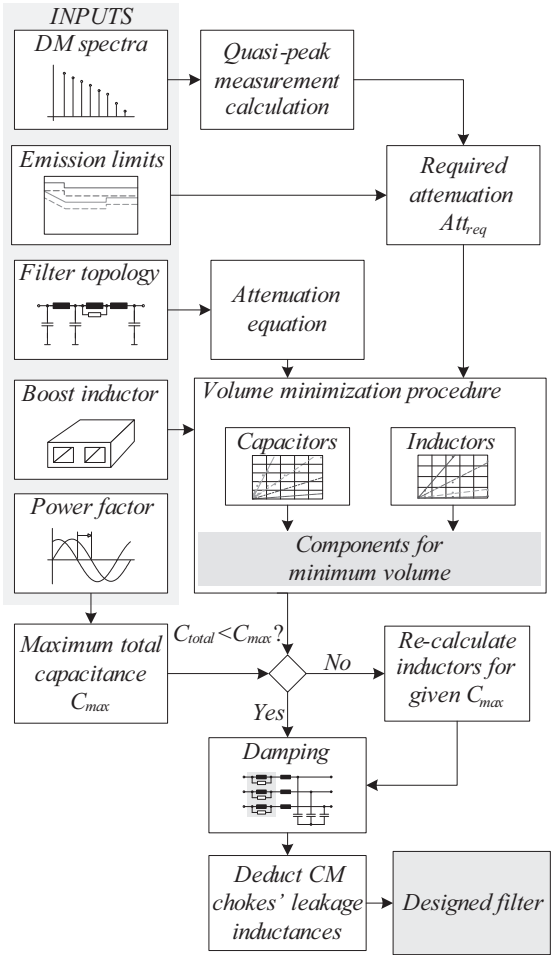


Figure 6.43: Flowchart showing the input DM filter design procedure.

$$I_{N1} = \frac{P_o}{3\,\eta\,U_{N1,\min}} = \frac{P_o}{3 \cdot 0.96 \cdot 0.8 \cdot U_{N1}} \cong 18.9\,\text{A}, \tag{6.125}$$

where $\eta = 0.96$ is the expected efficiency of the PWM converter and $U_{N1,\min} = 0.8 \cdot U_{N1}$ is the minimum input voltage.

All the required values for the calculation of the components which lead to the minimum DM filter volume are defined and plugging them into eq. (6.119) and eq. (6.120) gives,

$$C_{DM} \cong 2.57\,\mu\text{F} \tag{6.126}$$

$$L_{DM} \cong 2.10\,\mu\text{H}. \tag{6.127}$$

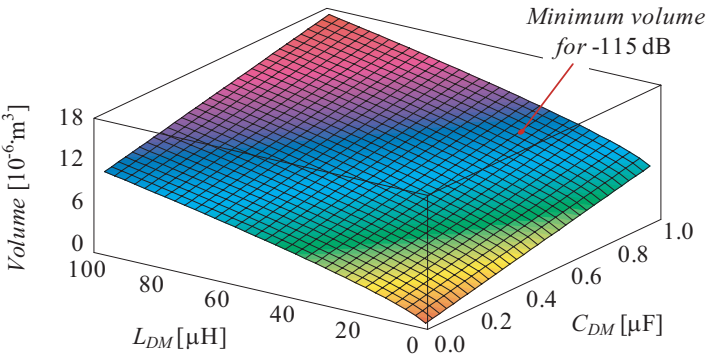
Results for the proposed volume minimization procedure are depicted in Figure 6.44. It is seen the volume and attenuation surfaces in dependency of the DM inductance L_{DM} and capacitance C_{DM}. The surfaces take into consideration a detailed model, with estimated parasitic elements (ESR, ESL, losses and parallel capacitance) as calculated in section 4.

It is seen from eq. (6.126) that the sum of three DM capacitors $3C_{DM} = 7.71\,\mu\text{F}$ is larger than the total maximum capacitance per phase $C_{\max} = 5.3\,\mu\text{F}$. For this reason, the components must be dimensioned for the largest total capacitance per phase. Dividing the total capacitance per phase by three and re-calculating L_{DM} for the required attenuation, leads to,

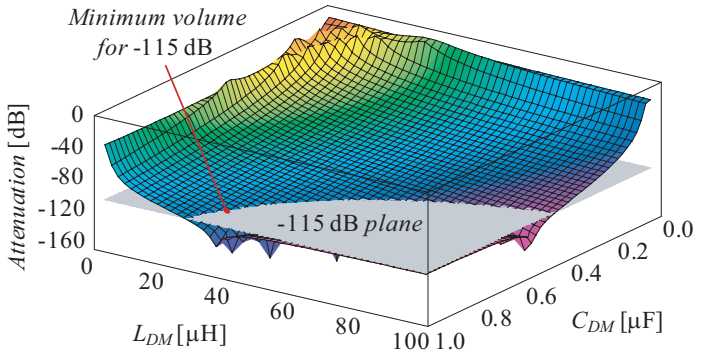
$$C_{DM} \cong 1.77\,\mu\text{F} \tag{6.128}$$

$$L_{DM} \cong 3.67\,\mu\text{H}, \tag{6.129}$$

which are employed for the implementation of the DM filter. As the obtained value for the DM capacitance is not commonly available, a different distribution of the capacitors has been employed in practice. The first filter stage has a total capacitance of $2.0\,\mu\text{F}$, while the other two stages present $1.5\,\mu\text{F}$. A worthwhile comment on the obtained result is that the inductance values are quite low and this results directly from the fact that the volumetric coefficients of foil capacitors are much lower that the



(a)



(b)

Figure 6.44: Volume and attenuation surfaces for the DM filter design with Molypermaloy cores and X2 capacitors. (a) Volume dependence on L_{DM} and C_{DM} values; (b) Attenuation at $f_s = 400$ kHz for L_{DM} and C_{DM} values and -115 dB plane (gray). Colors correspond to colors in (a).

coefficients for iron powder based DM inductors.

The DM inductors have been designed with the inductor design procedure proposed in section 4.4 leading to the specification shown in Table 6.11.

Table 6.11: Specifications for the DM inductors $L_{DM,i}$.

Parameter	*Value*
Core manufacturer	Magnetics
Core material	High Flux
Initial permeability	160
Core part number	58928-A2
Core dimensions [mm]	OD: 24.3 / ID: 13.8 / H: 9.65
Magnet wire diameter	1.5 mm
Number of turns	13
Number of layers	1
Expected losses	2.8 W
Expected temperature rise	52 °C
Maximum current	32 A
DC resistance	13.5 Ω
Parallel capacitance	2.3 pF
Inductance @ 100 Hz / 0 A	20.5 μH
Inductance @ 400 kHz / 0 A	18.2 μH
Inductance @ 400 kHz / 20 A	8.3 μH

6.7.3 Experimental Verification

The rectifiers' construction views are shown in Figure 6.45. The rectifier is designed for compactness. Thus, trade-offs among thermal, electrical, EMC and mechanical functions are required. The filter layout follows design rules to reduce interaction within filter elements and presents a straight line forward current flow. The current flows from the input terminals through the EMC filter, the current sensors and boost inductors, which links it to capacitor board. From this board the current flows through the power module into the output capacitors. In the tested ver-

sion of this system, the input filter has been placed in a separate printed circuit board in order to reduce the coupling to the power circuits.

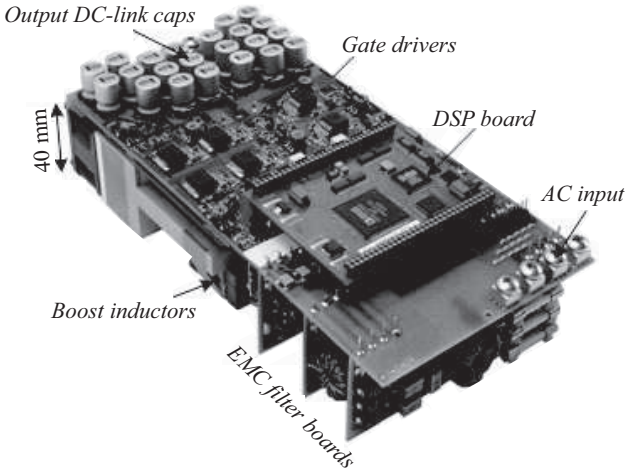


Figure 6.45: Top view of the rectifier with the EMC filter DSP board, gate drivers and electrolytic dc output capacitors.

The final filter circuit is shown in Figure 6.46, where the CM filter is also integrated in the structure. Interesting information is that the final boxed volume of the complete filter is approximately 2.4 times larger than the sum of all individual components, meaning that interconnections, air and PCB account for nearly 60% of the employed space. That leaves room for improvements through research on inter-components coupling reduction.

Due to thermal and digital processing restrictions, the switching frequency needed to be reduced to $f_s = 200$ kHz. This will be increased in a redesign of the system.

Experimental results from conducted emissions (QP) measurements, according to CISPR 22, are shown in Figure 6.47. A three-phase noise separator as in section 5 has been used in order to allow the separate evaluation of DM and CM. Figure 6.47 depicts the measured emission levels for CM and DM. For the DM emissions, the first harmonic is above

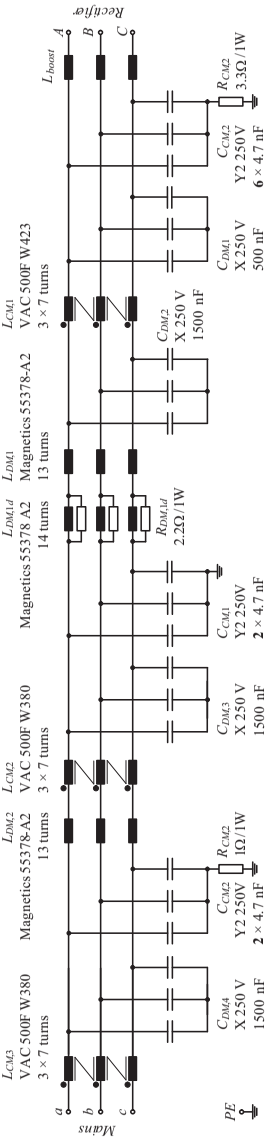


Figure 6.46: Complete circuit schematic for the designed filter with the specifications of the main components.

the designed point (400 kHz) and, thus, it is larger than predicted. These results are obtained in an open system, where no special shield was used. This explains for the worsening of the performance for higher frequencies. Nevertheless, the filter design procedure proves efficient since the components are designed for the range close to the switching frequency.

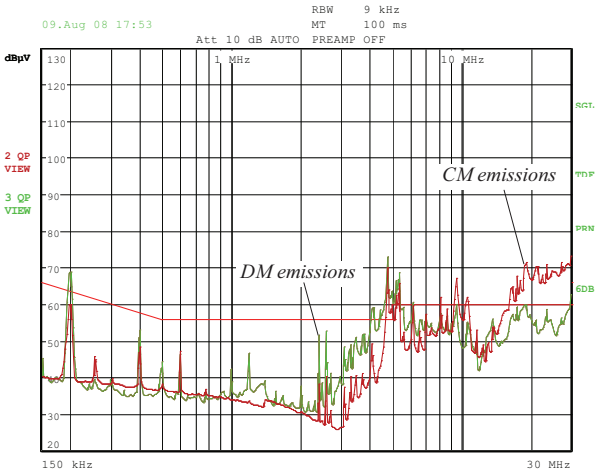


Figure 6.47: Measured CM and DM conducted emissions.

A comparison of the influence of cabling and grounding configurations in the differential mode emissions is presented in Figure 6.48. The DM emissions are shown in Figure 6.48 for two different system configurations, where the second one the interconnects are not directly shielded with copper tape around the connecting cables. It is seen that, for the same components and boards, the influence of the geometrical configuration of the interconnections and associated loops, is enormous. These effects can not be accounted for before hand in the proposed modeling, since they depend upon the 3-D geometry HF effects. This shall be the aim of future research, where parasitic modeling with field solvers are to be used in the design phase of a power system. A study on the influence of couplings in the performance of EMC filters is done in section 8.

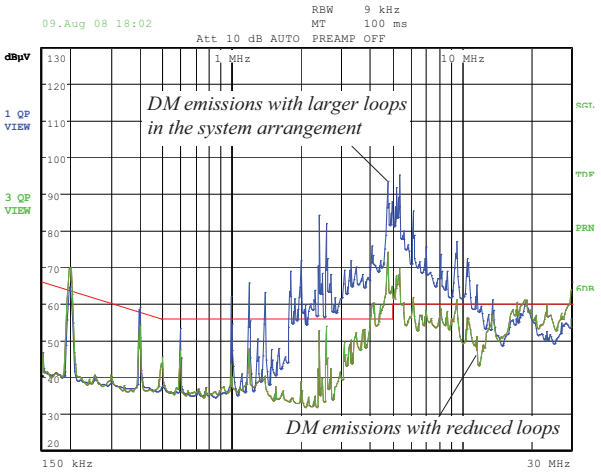


Figure 6.48: Measured DM conducted emissions.

6.8 Computer Aided Design of Three-Phase DM Filters

Aiming for shorter filter design cycles, the employment of computational resources of is great value. In order to achieve this objective, the design procedure proposed in the previous section can be extended to other PWM converter types and different filter topologies and is well suited for an algorithm. The flowchart showing the design algorithm is again depicted in Figure 6.49, where the main design tasks are specified. The implementation of this algorithm is presented in the following.

6.8.1 Required Attenuation

In order to obtain the necessary filter attenuation, the first step is to obtain the voltage or current noise source spectrum for the PWM converter. This can be computed as in section 3. For current-fed converters, the most adequate noise source model is the switched voltage at the terminals of the input inductor. Whereas, for voltage-fed type converters the most suited variables is the pulsed current at the input.

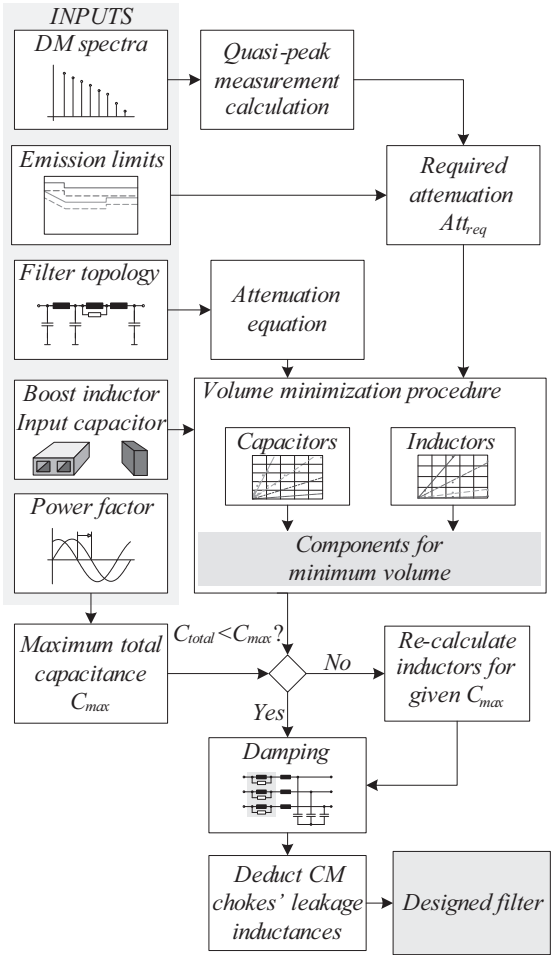


Figure 6.49: Flowchart showing the input DM filter design procedure.

Once the noise source spectrum is know, the next step is to compute the conducted emission levels for the converter without any input filter components. This is accomplished by the proper modeling of a test receiver and the relevant detection method as explained in section 2.5.2.

The requirements given by conducted emission limits are specified is EMC standards. For instance, CISPR limits for Class A or Class B equipments as shown in section 2.3. The limit curves shall be compared to the predicted emission levels at the frequency of interest f_{int}, which is 150 kHz for switching frequencies lower than 150 kHz or the switching frequency for higher frequencies. This gives the required attenuation, Att_{req}, at the frequency of interest.

6.8.2 Considered Filter Topologies

In theory, an infinite number of filter topologies exist and can be employed for low pass EMC filtering. In practice, however, a low number of topologies are typically applied. This is mainly due to two reasons, the first is costs that limit the number of components to use and, the second is the complexity associated to a large number of devices, which reduces reliability.

The principle of employing multi-stage filters in order to reduce the volume of filters finds its limits in the fact that the components need to be connected and creepage and clearance distances dictated by safety regulations need to be respected. With this, power filters are observed in practical applications limited to three or four filter stages. In [215] it has been shown that up to three filter stages can be economically advantageous for converters which require up to -100 dB attenuation and rated currents up to 20 A. For these reasons, only the topologies shown in Figure 6.50 and Figure 6.51 are considered here. Nevertheless, the procedure proposed here can be extended to other filter topologies in a straightforward way.

Figure 6.50 shows filter topologies, in their single-phase equivalent circuits, to be employed in voltage-fed PWM converters. Whereas, the topologies depicted in Figure 6.51 are considered for the design of DM filters for current-fed PWM converters. In all shown topologies the damping networks are omitted, but shall be included in the final filter circuits.

The asymptotic attenuation expressions for the considered topologies

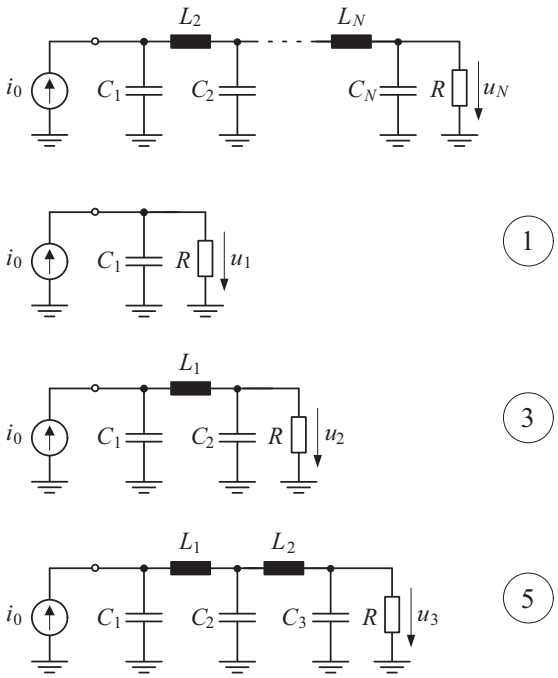


Figure 6.50: Differential mode filter topologies to be employed with voltage-fed PWM converters.

are given in Table 6.12.

The volume of the components for each of the considered filter topologies is computed with the expressions in Table 6.13. In these expressions, an extra inductor for a damping network has been considered.

6.8.3 Choice of Components

For the voltage-fed filter topologies, the input capacitors C_1 are considered to be given. This is due to the fact that these capacitors limit the voltage ripple at the converters' input and are required for the correct operation of the system. Typically, three requirements apply to these capacitors: (*i*) limit voltage ripple due to pulsed currents; (*ii*) limit voltage surges due to electrical discharges; (*iii*) limit under voltages due to large load

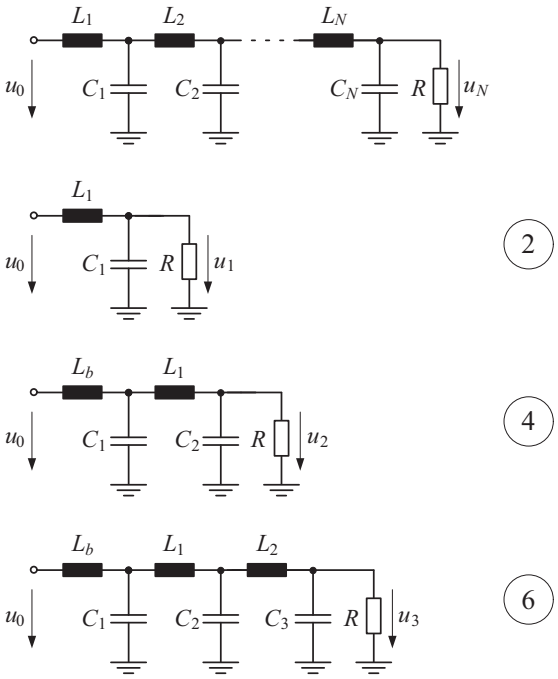


Figure 6.51: Differential mode filter topologies to be employed with current-fed PWM converters.

steps. For the current-fed topologies, the input inductors L_b are required for the proper operation of the system and are also considered to be designed to satisfy efficiency and/or current ripple demands. Furthermore, the input capacitors are also considered to be given to limit the variation of the input voltages. The exceptions to these assumptions are the filter topologies 1 and 2. Filter topology 1 presents a single capacitors and its value is chosen according to the required attenuation, while filter topology 2 has its inductor and capacitor calculated for minimum volume to achieve the required attenuation.

Following the same procedure for analytical volume minimization presented in section 6.7.1, the expressions given in Table 6.12, for the filter attenuation, and in Table 6.13, for the total volume of the components can be used. The final expressions for the filter components are summarized

Table 6.12: Asymptotic attenuation for the considered DM filter topologies.

Topology	*Attenuation*
1	$\frac{1}{2\pi f C_1}$
2	$\frac{1}{(2\pi f)^2 L_1 C_1}$
3	$\frac{1}{(2\pi f)^3 L_1 C_1 C_2}$
4	$\frac{1}{(2\pi f)^4 L_b L_1 C_1 C_2}$
5	$\frac{1}{(2\pi f)^5 L_1 L_2 C_1 C_2 C_3}$
6	$\frac{1}{(2\pi f)^6 L_b L_1 L_2 C_1 C_2 C_3}$

Table 6.13: Components' volume for the considered DM filter topologies.

Topology	*Components' Volume*
1	Vol_{C1}
2	$Vol_{C1} + Vol_{L1}$
3	$Vol_{C1} + Vol_{L1} + Vol_{C2}$
4	$Vol_{C1} + Vol_{L1} + Vol_{C2} + Vol_{Lb}$
5	$Vol_{C1} + 2\,Vol_{L1} + 2\,Vol_{C2}$
6	$Vol_{C1} + 2\,Vol_{L1} + 2\,Vol_{C2} + Vol_{Lb}$

in the following.

Filter topology 1

$$C_1 = \frac{1}{2\,\pi\,f_{int}\,Att_{req}} \tag{6.130}$$

Filter topology 2

$$L_1 = \frac{1}{2\,\pi\,f_{int}}\,\frac{U_{N1}}{I_{N1}}\,\sqrt{\frac{k_C}{2\,Att_{req}\,k_L}} \tag{6.131}$$

$$C_2 = \frac{1}{\pi\,f_{int}}\,\frac{I_{N1}}{U_{N1}}\,\sqrt{\frac{k_L}{2\,Att_{req}\,k_C}} \tag{6.132}$$

Filter topology 3

$C_1 = \text{given}$

$$L_1 = \frac{1}{4\,\pi\,f_{int}}\,\frac{U_{N1}}{I_{N1}}\,\sqrt{\frac{k_C}{\pi\,f_{int}\,Att_{req}\,k_L\,C_1}} \tag{6.133}$$

$$C_2 = \frac{1}{2\,\pi\,f_{int}}\,\frac{I_{N1}}{U_{N1}}\,\sqrt{\frac{k_L}{\pi\,f_{int}\,Att_{req}\,k_C\,C_1}} \tag{6.134}$$

Filter topology 4

$L_b = \text{given}$

$C_1 = \text{given}$

$$L_1 = \frac{1}{4\,\pi^2\,f_{int}^2}\,\frac{U_{N1}}{I_{N1}}\,\sqrt{\frac{k_C}{2\,Att_{req}\,k_L\,L_1\,C_1}} \tag{6.135}$$

$$C_2 = \frac{1}{2\,\pi^2\,f_{int}^2}\,\frac{I_{N1}}{U_{N1}}\,\sqrt{\frac{k_L}{2\,Att_{req}\,k_C\,L_1\,C_1}} \tag{6.136}$$

Filter topology 5

$C_1 = \text{given}$

$$L_1 = L_2 = \frac{1}{6\,\pi\,f_{int}}\,\frac{U_{N1}}{I_{N1}}\,\sqrt{\frac{3\,k_C}{k_L}}\,\sqrt[4]{\frac{2}{\pi\,f_{int}\,Att_{req}\,C_1}} \tag{6.137}$$

$$C_2 = C_3 = \frac{1}{4\,\pi\,f_{int}}\,\frac{I_{N1}}{U_{N1}}\,\sqrt{\frac{3\,k_L}{k_C}}\,\sqrt[4]{\frac{2}{\pi\,f_{int}\,Att_{req}\,C_1}} \tag{6.138}$$

Filter topology 6

$$L_b = \text{given}$$
$$C_1 = \text{given}$$
$$L_1 = L_2 = \frac{1}{6\,\pi\,f_{int}}\frac{U_{N1}}{I_{N1}}\sqrt{\frac{3\,k_C}{\pi\,f_{int}\,k_L}}\sqrt[4]{\frac{1}{Att_{req}\,L_1\,C_1}} \tag{6.139}$$
$$C_2 = C_3 = \frac{1}{4\,\pi\,f_{int}}\frac{I_{N1}}{U_{N1}}\sqrt{\frac{3\,k_L}{\pi\,f_{int}\,k_C}}\sqrt[4]{\frac{1}{Att_{req}\,L_1\,C_1}} \tag{6.140}$$

Once the components of a filter for minimum volume are calculated, the next step is to check if the minimum power factor for a given load is achieved. This can be specified as a maximum displacement angle $\Phi_{in,\max}$ between the input currents and phase voltages. With this value and assuming that the filter inductors do not notably cause current displacement and that power factor correction is employed, the maximum capacitance per phase can be computed with,

$$C_{max} = \sum_{i=1}^{3} C_i \leqslant \frac{3P_{\min}\Phi_{in,\max}}{2\pi\,f_N\,U_{N1}^2}, \tag{6.141}$$

where, f_N is the mains frequency, U_{N1} is the phase voltage RMS value and $P_{\min}$ is the power at which the power factor limitation is specified.

If the capacitors that have been calculated for minimum volume are larger than C_{max}, their value must be reduced to the maximum allowable. The capacitors can be equally distributed among the filter stages and the inductors shall be re-calculated based only in the required attenuation requirement. This can be accomplished with the expressions given in Table 6.14.

Having the required inductance values, the inductors shall be designed for the required current and aiming for a good high frequency performance. A winding with single layer is recommended and the inductor design procedure proposed in section 4.4 can be employed.

6.8.4 Finalizing the DM Filter Design

Damping networks can be designed once the filter topology and the components are decided. In the implemented DM filter design procedure, the damping network shown in Figure 6.52 has been chosen for the rea-

Table 6.14: Calculation of filter inductors for the case where the maximum capacitance per phase is limited.

Topology	*Attenuation*
1	Not applicable
2	$\frac{1}{(2\pi f)^2 \, Att_{req} \, C_1}$
3	$\frac{1}{(2\pi f)^3 \, Att_{req} \, C_1 \, C_2}$
4	$\frac{1}{(2\pi f)^4 \, L_b \, Att_{req} \, C_1 \, C_2}$
5	$\sqrt{\frac{1}{(2\pi f)^5 \, Att_{req} \, C_1 \, C_2 \, C_3}}$
6	$\sqrt{\frac{1}{(2\pi f)^6 \, L_b \, Att_{req} \, C_1 \, C_2 \, C_3}}$

sons stated in section 6.3. The ratio between L_{DM} and $L_{DM,d}$ is typically chosen equal to one. The unitary ratio is an advantage from a construction point of view, since only one type of inductor needs to be built/purchased for the whole DM filter circuit. Furthermore, this leads to acceptable losses in the damping resistor $R_{DM,d}$ and, from experimental results [112, 130, 131] reasonable control effort has been observed. The considerations of section 6.3 can be observed for the computation of the damping resistors $R_{DM,d}$.

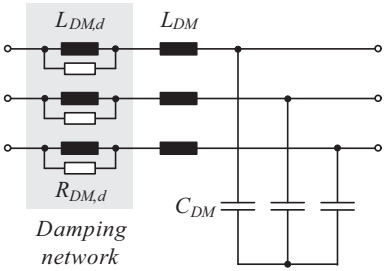


Figure 6.52: Three-phase filter stage with damping network.

The final step for the design of the DM filters is the integration with the CM filter. This integration can be performed in several ways. The inductors of both types of filters can be integrated, so that the leakage of CM inductors can be employed as part or even as the total DM inductance. Another possibility is to reduce the CM inductance by the amount of DM inductance, which is not typically done because the required CM inductance is commonly much larger than the DM inductances. The DM capacitance is increased by the CM capacitors. However, due to earth leakage current limitation, the CM capacitance is typically much smaller than the required DM capacitance and little influence is to be expected. The DM capacitance, in theory plays no role in CM filtering. Anyway, the DM filter must be constructed aiming for highly symmetrical circuits in order not to influence CM filtering performance in a counter productive way.

6.8.5 Experimental Results

As a case study, a filter has been designed and experimentally tested for a 6 kVA Indirect Matrix Converter as specified in section 3.5. The performed design and analysis for the filter is presented in the following.

The specifications for the IMC are:

- Input RMS phase voltage: $U_{N1} = 230$ V
- Minimum voltage: $U_{N1,\min} = 0.85\,U_{N1}$
- Mains frequency: $f_N = 50$ Hz
- Rated power: $P_o = 6$ kVA
- Efficiency: $\eta \cong 0.96$
- Switching frequency: $f_S = 25$ kHz
- Equipment type: CISPR Class A
- Rated modulation index: $M = 0.7$
- Minimum power factor: $PF_{\min} = 0.995$ @ $0.25\,P_o$
- Input RMS current: $I_{N1,\max} \cong 9.05$A

Employing the models of section 3.5, the following input data is computed. The predicted conducted emission levels are:

$$CE_{pred} \cong 149\,\mathrm{dB}\ @\ f_{int} = 150\,\mathrm{kHz}, \tag{6.142}$$

which are compared to the CISPR Class A limits, leading to a required attenuation of,

$$Att_{req} = ClassA_{limit} - CE_{pred} - 6\,\mathrm{dB} \cong 83\,\mathrm{dB}. \tag{6.143}$$

Material High Flux is chosen with a initial permeability of $\mu_r = 160$, which presents a volumetric coefficient of,

$$k_L \cong 3.95 \cdot 10^{-3} \frac{\mathrm{m}^3}{\mathrm{H} \cdot \mathrm{A}^2}. \tag{6.144}$$

Capacitor C_1 is chosen based on voltage ripple requirements [89] and employ 10 μF foil capacitors are employed. For the other DM filter capacitors, through-whole X2 rated capacitors are employed, which volumetric coefficient is,

$$k_C = k_{C,X2,foil} \cong 16.4 \cdot 10^{-6} \frac{\mathrm{m}^3}{\mathrm{F} \cdot \mathrm{V}^2}. \tag{6.145}$$

In order to verify the proposed CAD for DM filters, filter topology 3 has been chosen. With this, the values of the filter components can be derived from eq. (6.133) and eq. (6.134), so that:

$$C_{dm,4} = C_1 = 10\,\mu\mathrm{F} \tag{6.146}$$

$$L_{dm} = L_1 = \frac{1}{4\,\pi\,f_{int}} \frac{U_{N1}}{I_{N1}} \sqrt{\frac{k_C}{\pi\,f_{int}\,Att_{req}\,k_L\,C_1}} \cong 16.1\,\mu\mathrm{H} \tag{6.147}$$

$$C_{dm,2} = C_2 = \frac{1}{2\,\pi\,f_{int}} \frac{I_{N1}}{U_{N1}} \sqrt{\frac{k_L}{\pi\,f_{int}\,Att_{req}\,k_C\,C_1}} \cong 2.07\,\mu\mathrm{F} \tag{6.148}$$

The schematics for this filter is presented in Figure 6.53 and views of the built prototype are shown in Figure 6.54. For this filter, ESL canceling coupled inductors L_{canc} are included and this analysis is performed in

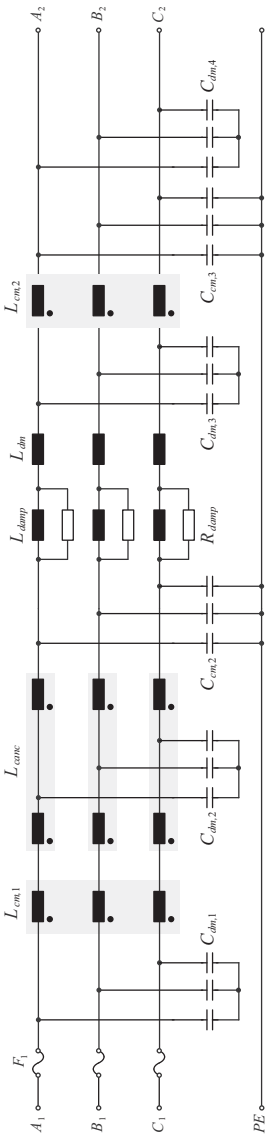


Figure 6.53: Circuit schematics of the filter designed for the Indirect Matrix Converter.

section 8.5.2. The DM capacitors $C_{dm,4}$ are placed on the power converter printed circuit board and are not shown in the photograph.

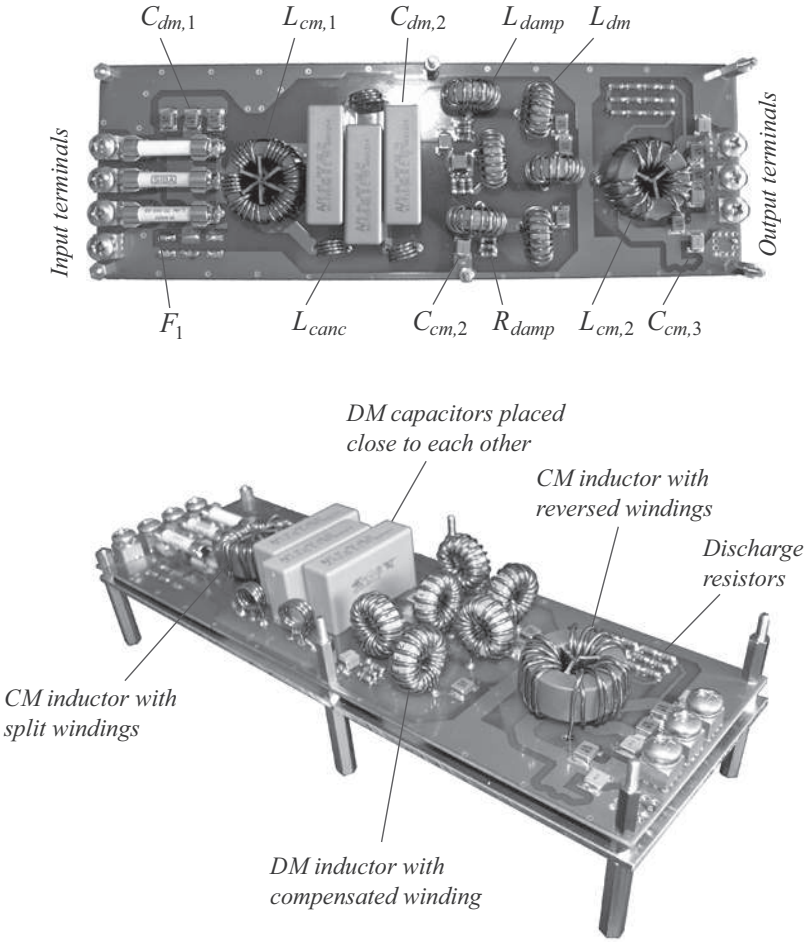


Figure 6.54: Photograph of the filter designed for the Indirect Matrix Converter.

The inductors for the filters are specified in Table 8.4. The DM inductors L_{dm} are analyzed in section 8.5.1. The CM filter is analyzed in sec-

tion 8.5.2. For the damping resistors R_{damp} three SMD resistors (MELF) of value 1.2 Ω/1 W are connected in parallel.

Table 6.15: Inductors employed in the filter for the IMC.

Inductor	*Core*	*Turns*	*Wire*
L_{dm}	55378-A2	18	ϕ 1 mm
L_{damp}	55378-A2	18	ϕ 1 mm
$L_{cm,1}$	VITROPERM W523	3×8	ϕ 1 mm
$L_{cm,2}$	VITROPERM W380	3×7	ϕ 1 mm
L_{canc}	Air (radius = 0.9 cm)	2×2	ϕ 1 mm

The DM inductor L_{dm} data is shown in Table 6.16, where it is seen that the inductance at 150 kHz is still high at the RMS current.

Table 6.16: Specifications for the DM inductor L_{dm}.

Parameter	*Value*
Core manufacturer	Magnetics
Core material	High Flux
Initial permeability	160
Core part number	55378-A2
Core dimensions [mm]	OD: 24.3 / ID: 13.8 / H: 9.65
Magnet wire diameter	1.18 mm
Number of turns	18
Number of layers	1
Expected losses	1.8 W
Expected temperature rise	54 °C
Maximum current	25 A @ 80%B_{max}
dc resistance	16.5 Ω
Parallel capacitance	2.1 pF
Inductance @ 100 Hz / 9 A	20.1 μH
Inductance @ 150 kHz / 9 A	19.2 μH
Inductance @ 150 kHz / 15 A	10.9 μH

Table 6.17: Capacitors employed in the filters for the IMC.

Capacitor	*Manufacturer*	*Specification*
$C_{dm,1}$ and $C_{dm,3}$	Murata	SMD[a] – X2 33 nF/250 V
$C_{dm,2}$	Arcotronics	TH[b] – X2 2.2 μF/250 V
$C_{dm,4}$	ICEL	TH – AC 10 μF/250 V
$C_{cm,1}$ and $C_{cm,2}$	Murata	SMD – 2 × Y2 4.7 nF/250 V
$C_{cm,3}$	Murata	SMD – 3 × Y2 4.7 nF/250 V

[a] SMD – Surface Mount Device.
[b] TH – Through hole device.

The capacitors employed in the filters are specified in Table 6.17. Capacitors $C_{dm,1}$ and $C_{dm,3}$ are small X2 SMD capacitors placed in the circuits in order to improve the high frequency performance of the filter and do not appreciably increase filter volume.

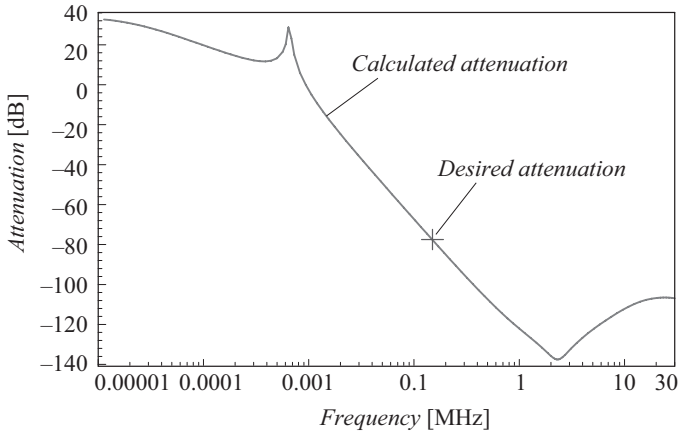


Figure 6.55: Filter attenuation for the RMS current.

The attenuation curve for the designed filter is depicted in Figure 6.55. It has been computed with the inclusion of the parasitic elements employ-

ing the equivalent circuits studied in section 4 and using the attenuation calculation procedure of section 6.2 in the circuit of the filter topology 3.

The predicted conducted emission levels for the designed filter is calculated for three-different inductance values as shown in Figure 6.56, which are calculated for currents of 0 A, 9 A and 15 A, leading to the respective values of inductance since the current increases the dc bias in the magnetic core material and, thus, lowers the permeability reducing the total inductance.

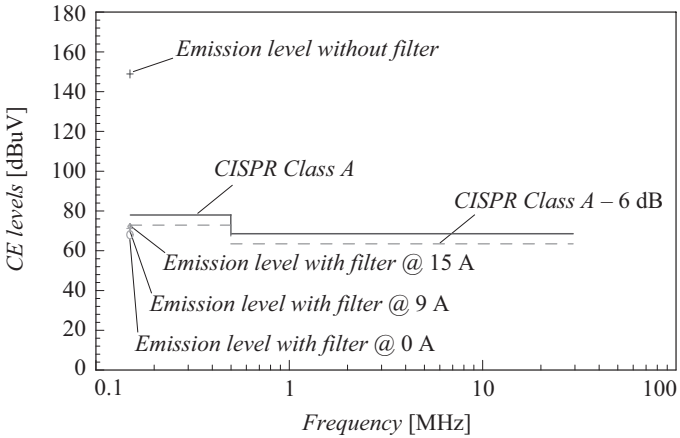


Figure 6.56: Predicted conducted emission levels with and without input filter. Three levels are shown for the emissions with filter, which are dependent on the DM inductance change with dc bias.

Conducted emission tests have been performed with the setup shown in Figure 6.57. It is seen that a three-phase CM/DM noise separator as presented in section 5 is employed in order to separately evaluate the differential mode emission levels. With this, the proposed DM filter design procedure can be tested with the IMC supplying a 2 kVA asynchronous machine through a 3 m shielded cable.

The results of the conducted emission tests are displayed in Figure 6.58. It is seen that the system fulfills the CE requirements for equipments of Class A according to CISPR 11.

Regarding differential mode conducted emissions, a large margin is observed between the DM measured levels and the Class A limit. This

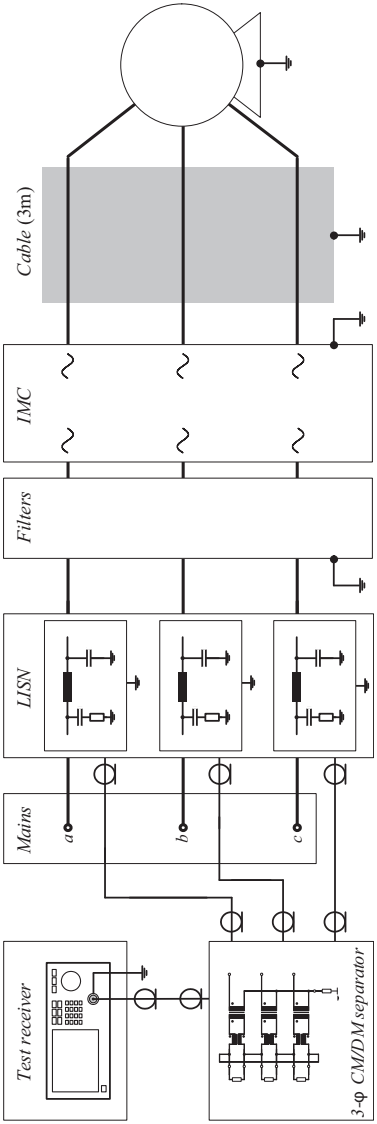


Figure 6.57: Conducted emission test setup with the designed filters and the Indirect Matrix Converter supplying a 2 kVA asynchronous machine.

is mainly because the employed machine is not heavily loaded, so that the DM emissions are lower and the inductance of the DM inductors is higher than for rated current. For higher loads, it is expected that an increase in the emissions is observed mainly for DM. Nevertheless, the filter design procedure leads to a filter which effectively reduces DM emissions to acceptable levels.

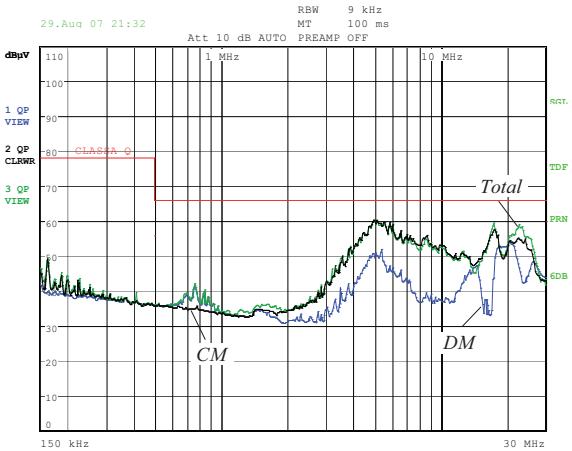


Figure 6.58: Conducted emission measurements (CM, DM and total levels) for the test setup of Figure 6.57. The complete system is placed inside a shielded box and loop areas are minimized according to section 8.5.2.

6.9 Summary

The design of DM filter is of high importance in, both, costs and performance of three-phase PWM converters. This chapter has targeted efficient design techniques that allow for low cost and high performance filters.

Multi-stage filters can be studied in their single-phase equivalent circuit as a ladder circuit and, as such, can have their attenuation and equivalent impedances calculated through algorithms. This chapter has reviewed the algorithms for attenuation and input impedance. An algorithm for the computation of output impedance has been also studied. Based on this study, design procedures can be derived to fulfill a required

filter attenuation.

Typical damping networks have been reviewed, which allow for the improvement of the transient response of filters and reduce the necessary control effort in a closed loop system comprising a three-phase PWM converter. Furthermore, a comparison between single- and multi-stage filters has been performed showing that multi-stage filters might present a beneficial effect in the DM filter implementation.

Two different DM filter design procedures have been proposed, which allow for efficient design of compact EMC input filters for three-phase PWM converters.

At first, a systematic procedure for the design of the DM input filter of a three-phase Very Sparse Matrix Converter (VSMC) has been presented which can also be applied to other three-phase current-source-type converter topologies. The procedure is based on a detailed modeling of the RF measurement system with emphasis on the EMC test receiver. Following the design approach has resulted in compliance to the considered harmonic standards (e.g. EN 61800-3) as verified by the experimental analysis of a Very Sparse Matrix Converter prototype. There, the DM noise components have been determined using a novel three-phase CM/DM noise separator.

A design procedure for the EMC filters to be employed with a three-phase rectifier unit in order to fulfill CISPR 22 Class B requirements related to conducted emissions has been also proposed. The design procedure has been explained; where a volumetric optimization has been carried out taking into consideration different aspects related to the subject, such as electrical safety, power factor and damping of resonances. The presented procedure avoids the necessity of using numerical optimization routines. The experimental verification of the proposed filter design procedure is shown, where it is identified that the system physical configuration has a large influence in the final emissions performance. These effects shall be target for future research, so that computer aided design and virtual prototyping can be fully implemented.

Aiming for shorter filter design cycles, the employment of computational resources of is great value. In order to achieve this objective, the design procedure proposed for the three-phase rectifier unit has been extended to other PWM converter types and different filter topologies. This is because the procedure is well suited as a design algorithm. As a case

study to experimentally verify the design structure, a filter has been designed and experimentally tested for a 6 kVA Indirect Matrix Converter. The performed design and analysis for the filter has been presented and experimental results have validated the performed analysis and filter design.

Chapter 7

The Design of Common-Mode Filters for Three-Phase Converters

"The greatest challenge to any thinker is stating the problem in a way that will allow a solution." Bertrand Russell

7.1 Introduction

The circulation of high frequency currents between the power lines and the protective earth conductors lead to numerous possibilities of electromagnetic interference. This noise mode is typically responsible for the larger portion of radiated emissions, which must be controlled. Input common mode filters act on reducing the CM currents flowing to the power grid, thus, decreasing radiated emissions and the possibility of EMI.

As for differential mode filters, these filters employed for two main reasons: (*i*) preventing emissions from the considered converter to interfere with neighboring equipments, and (*ii*) on the other way around, avoiding the disturbance of the converter by sources of electromagnetic noise in the surrounding environment [25, 39]. Nevertheless, these filters have their design driven mainly by international EMC standards, which put

limits to the amount of emissions that an equipment can emit. Another similarity to DM filters is that these filters typically occupy a respectable amount of space in a power converter.

Differently from DM filters, the CM filters employ relatively high inductances and low capacitance values. High inductances can be employed due to the special characteristics of the CM inductors, which can use very high permeability materials, thus achieving high impedances with limited amount of magnetic material. The small capacitances employed in a CM filter come from restrictions due to safety regulations, which limit the amount of current that can flow in such capacitors. It is observed that, even though the objectives are similar, the design of CM filters represents a quite distinct task when compared to the design on differential mode ones. Therefore, this chapter discusses detailed issues which shall be considered during the design of CM filters which are based on analytical models of the considered PWM converters, filter components and conducted emission measurement techniques.

The first part on this chapter presents the design of a CM filter for a Three-phase Buck-type PWM rectifier system. It is shown that the typical try-and-error procedure does not need to be followed for a successful CM filter design. The filter design comprises a two-stage conventional CM input filter and includes the effect of a HF connection of the star-point of the DM input filter capacitors to the output of the rectifier. Experimental results validate the realized filter and the modeling procedure.

The following section presents a study and practical implementation of an active filter employing a HF power amplifier and passive filter components to be connected to the AC power lines in order to mitigate common mode conducted emissions of PWM converter systems. The filter topology is chosen from different possibilities listed in a literature survey and studied regarding practical implementation issues, where requirements for a high frequency power amplifier to be applied in active filtering are derived. Special attention is put on the stability analysis where the challenges for the feedback loop are discussed and a simple feedback structure is proposed. Other feedback concepts are analyzed and limitations posed by stability requirements are presented. A prototype is designed and built, from which mathematical and experimental results are obtained demonstrating the potential and limitations of such a system.

The last part of this chapter presents an analytical procedure for the design of multi-stage CM filters to be included in a three-phase/-level

PWM rectifier unit in order to fulfill EMC requirements related to conducted emissions. An analytical volumetric optimization of the CM filter is performed considering constraints given by electrical safety, from where it is seen that only the CM inductors need to have their design optimized in order to achieve a small total filter volume. A procedure to design the CM inductors is presented, which is based in an iterative process implemented in software. The experimental verification of the proposed procedure is presented through CE measurements in the designed system.

7.2 Common Mode EMC Input Filter Design for a Three-Phase Buck-Type PWM Rectifier System

This section presents the CM filter design for a Three-Phase Buck-Type PWM Rectifier System as shown in Figure 7.1. This converter was modeled in section 3.3 as a CM noise source.

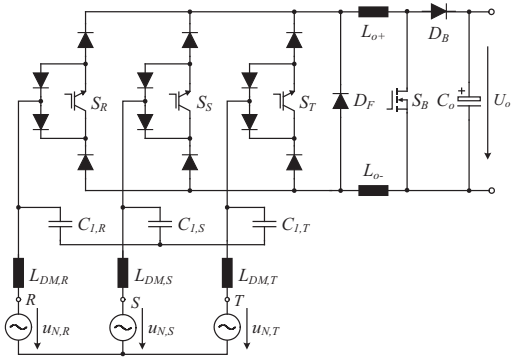


Figure 7.1: Structure of the power circuit of a Three-phase Three-Switch buck PWM rectifier with integrated boost output stage designed for the realization of the input stage of a 5 kW telecommunications power supply module switching at $f_p = 28$ kHz. For clarity, only the DM filter components [130] which are relevant for the CM filter design ($L_{DM,i}$ and $C_{1,i}$) are shown, where $L_{DM,i}$ is the sum of all DM filter inductances of a phase.

The CM filter design is, in practice, often based on a trial-and-error

and/or on the experience of the designer due to the inherently difficult prediction of the CM noise source characteristics in a complex power electronics systems [39, 233]. Accurate models for prediction have been proposed for boost-type rectifiers [234–236], where a relatively high effort is put on the numerical or mathematical modeling of the noise paths and sources. However, if a first prototype of the system is available, which can be used for the EMC evaluation, the simplified model of the CM noise propagation paths presented for this converter in section 3.3 can be used. Thus, the emission levels can be predicted with the necessary accuracy and the attenuation requirements for a CM input filter can be identified. For the case at hand the boost stage is not operating, but the parasitic capacitances of the semiconductors S_B and D_B are taken into consideration.

This work presents the tasks performed for the CM filter design and evaluation. The effect of a HF connection of the star-point of the DM input filter capacitors to the output of the rectifier is analyzed concerning its effect on the modeled CM noise paths. A two-stage conventional CM input filter is designed. The selection of the filter components aiming to achieve the filter's required attenuation is presented.

Furthermore, the insertion loss of the employed filter elements is analyzed. Finally, the compliance to CISPR 22 Class B limits is verified through CE measurements on a 5 kW prototype employing the designed CM filter.

7.2.1 Effects of a Capacitive Connection from the Input Star-Point to the Output Center-Point

To start with, the emission levels as predicted in section 3.3 are shown once again in Figure 7.2. It is noticed that, the critical emission points are the peaks close to 250 kHz and 600 kHz and, once these are lowered, the emissions at 150 kHz can become dominant.

The main purpose of the CM input filter is to hinder the common mode current propagation to the mains by providing a high impedance in the direction to the mains and/or by providing paths with low impedance around the rectifier elements, which are responsible for the generation of CM voltages so that CM noise current is circulated back internally. With this objective, an equivalent capacitor C_{MP} (cf. Figure 7.3) is placed

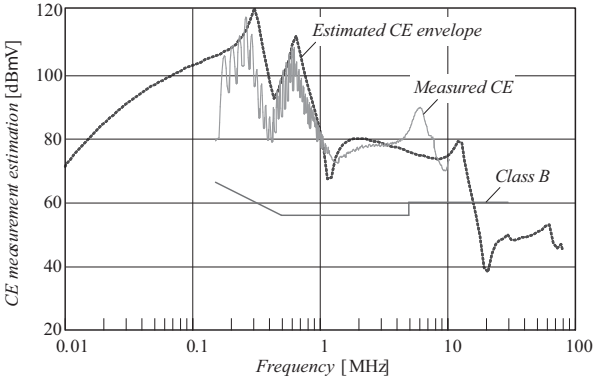


Figure 7.2: CM emission levels at a three-lines LISN. Shown are the measured levels and the predicted ones as studied in section 3.3.

between the star-point of the DM input filter capacitors and the center point of the output capacitors, allowing the HF common mode current to return in some extent to its source.

The influence of this capacitive connection in the equivalent CM circuit of Figure 7.3 is observed in Figure 7.4. It is seen that the strong resonance, originally at approximately 250 kHz can be shifted to lower frequencies. If shifted below the measurement band (150 kHz — 30 MHz), lower filtering effort is required.

In the case at hand, $C_{MP} = 20$ nF was selected in order to shift the resonance at 250 kHz (cf. Figure 7.6) to a frequency below 150 kHz. In

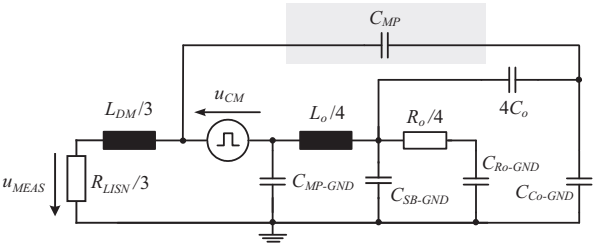


Figure 7.3: The capacitive connection from output to input creates an alternative path for the CM currents, while not increasing earth leakage currents.

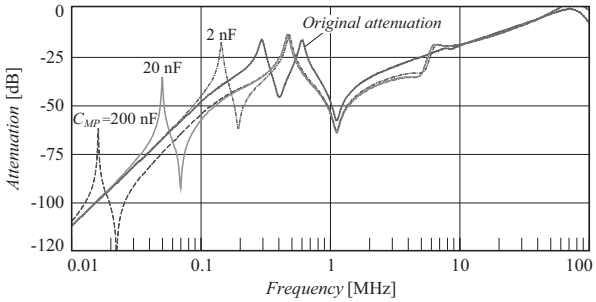


Figure 7.4: Influence of different capacitance values to the CM attenuation curves.

practice two capacitors $C_{MP}/2 = 10$ nF have been connected from the positive and negative output capacitor terminals, respectively, to the DM capacitors star-point terminal.

The effect of this connection is shown in Figure 7.6 by CM conducted emission measurements employing a current probe Pearson 410, presenting a nominal bandwidth of 20 MHz, measuring the sum of the three input currents. The measurement setup is shown in Figure 7.5.

The results of the original CM conducted emissions measurement is shown in Figure 7.6, where high emission levels are measured at 250 kHz and 600 kHz. In Figure 7.6 the measurement performed with the inclusion of C_{MP} is also presented and, as it can be noticed, the noise emission in the

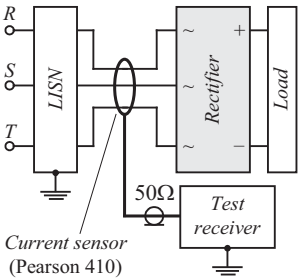


Figure 7.5: CM measurement setup: the sum of the input currents is measured with a current probe Pearson 410 in order to obtain only the CM levels.

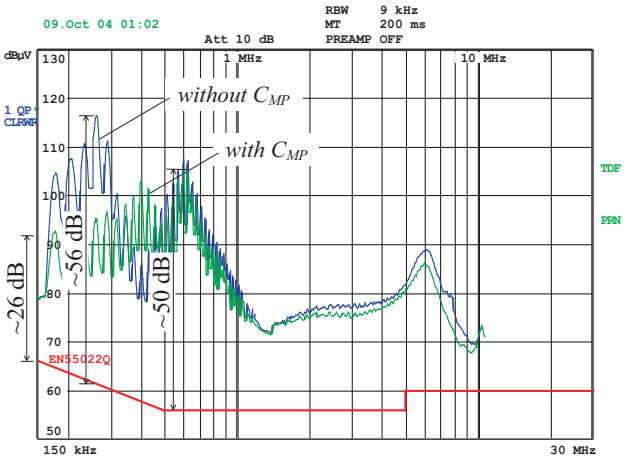


Figure 7.6: Effect of the capacitive connection (C_{MP}) from the star-point of the DM input filter capacitors to the rectifier output with $C_{MP} = 20$ nF . The sum of the input currents is measured with a current probe Pearson 410 in order to obtain only the CM signal. As the current measurement bandwidth is 20 MHz, the measurement is constrained to 10 MHz. Shown are the CE measurement without the inclusion of any CM filtering elements and after the inclusion of the capacitive connection between the input star-point and the output DC-link through C_{MP}.

lower frequency range has been reduced. The peak at 250 kHz has been shifted down to a lower frequency, sitting outside of the measurement range of interest.

Regarding the CE CM measurements, the current sensor produces an output signal of 0.05 V/A at an external 50 Ω-termination, which lies in parallel to the internal 50 Ω-termination of the sensor. This corresponds to an attenuation $G_{Pearson}$ of,

$$G_{Pearson} = 20\log(0.05) = -26\,\text{dB}. \tag{7.1}$$

The measurement at the LISN equivalent input resistance $R_{LISN}/3 = 50\,\Omega/3$ appears with a gain G_{LISN} of,

$$G_{LISN} = 20\log(50/3) = 24.4\,\text{dB}. \tag{7.2}$$

Therefore, the gain of the measurement result with the current sensor G_{total} is given by,

$$G_{total} = G_{LISN} - G_{Pearson} = 50.4\,\text{dB}. \tag{7.3}$$

Accordingly, the measurement curves are located 50.4 dB below the measurement level detected by the EMC test receiver. This gain is considered for the subsequent filter design and all conducted emission measurement graphics have this correction factor considered.

7.2.2 Two-Stage Common Mode Filter Design

For guaranteeing compliance to Class B limits, Figure 7.6 shows that the attenuation with a CM filter must be higher than -50 dB around 600 kHz and higher than -26 dB at 150 kHz. Additional margin of 6 dB is considered as suggested in CISPR 11. For reducing the total size of the CM filter the attenuation is distributed to two filter stages [215] as presented in the following.

The total capacitance $C_{CM,total} = C_{CM,1} + C_{CM,2}$ between any of the input phases and the PE is restrained by the maximum allowable earth leakage $I_{GND,rms}$ current due to IT safety regulations. The tests are performed usually with 110% of the input RMS voltage $U_{N,rms}$ and the leakage current [91] should be typically limited to $I_{GND,rms} \leqslant 3.5$ mA, even for the case where one of the phases is lost.

With the leakage current given by

$$I_{GND,rms} = 1.1\,U_{N,rms}\,2\pi 50\,\text{Hz}\,C_{CM,total}, \tag{7.4}$$

a maximum total CM capacitance per phase of $C_{CM,total} \cong 44$ nF is reached. Providing a margin and guaranteeing small footprints for the capacitors, the values of $C_{CM,1} = C_{CM,2} = 4.7$ nF are selected resulting in a total CM capacitance of 9.4 nF per phase. With two of the filter elements selected, the next step is the determination of the inductors.

As the designed filter is built with two LC stages (cf. Figure 7.8), a high slope in the attenuation is achieved. Due to this new circuit configuration, the resonance peak at 600 kHz is changed. Thus, if the filter components are selected to fulfill the attenuation requirement at 150 kHz (-32 dB), the slope provided by the multi-stage filter attenuation provides a high

attenuation at 600 kHz. For this reason, the CM filter is designed for the requirement at 150 kHz.

As the CM voltage is relatively small, the CM inductor can be built with small cores. Applying a smaller $L_{CM,1}$ and larger $L_{CM,2}$ leads to a large CM impedance at the mains side. This has the advantage of reducing the influence of the mains in the filtering performance. The total required attenuation $Att_{CM,req}$ at 150 kHz is divided into two parts, $Att_{CM,1} \cong -10dB$ and $Att_{CM,2} \cong -22dB$. With these values, the required impedances for the inductors $L_{CM,1}$ and $L_{CM,2}$ are computed for the two critical cases as

$$Z_{LCM,1,req} \cong 210\,\Omega\,@\,150\,\text{kHz} \tag{7.5}$$

$$Z_{LCM,2,req} \cong 820\,\Omega\,@\,150\,\text{kHz}. \tag{7.6}$$

With this, the filter inductors are built as specified in Table 7.1, which

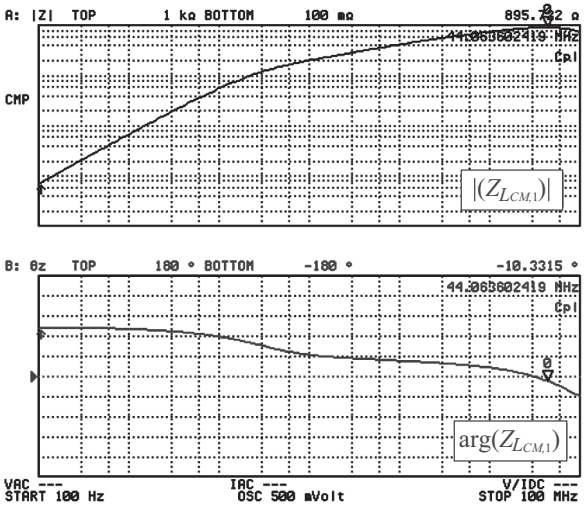


Figure 7.7: Impedance measurement for the inductor $L_{CM,1}$. A well damped high frequency behavior and a high self resonance frequency ($\approx$ 44 MHz) can be observed. The impedance at 600 kHz is measured as 490 Ω.

also presents the specifications for the capacitors in the CM filter. Passive damping through resistors is not added due to the predominantly resistive high frequency behavior of the inductors (cf. Figure 7.7) built with core material VITROPERM 500F [173]. These inductors exhibit good impedance stability for high temperatures and high power density.

Table 7.1: CM filter components.

Component	*Specification*
$C_{CM,1}$, $C_{CM,12}$	Y1 Capacitor, Epcos MKP B81123
	4.7 nF - 250 Vac
C_{MP}	Y1 Capacitor , Epcos MKP B81123
	2×10 nF - 250Vac
$L_{CM,1}$	Vaccuumschmelze VAC VITROPERM 500F W409
	N $= 3 \times 4$ turns, AWG 16
$L_{CM,2}$	Vaccuumschmelze VAC VITROPERM 500F W380
	N $= 3 \times 7$ turns, AWG 16

The effect of the addition of the filtering elements to the single-phase equivalent circuit of the final filter structure as shown in Figure 7.11 can be observed in Figure 7.9 through the plots of the transfer function $U_{MEAS}(j\omega)/U_{CM}(j\omega)$ for the different circuit configurations. The final filter configuration is able to provide the required attenuation in the complete frequency range and the peak at 600 kHz no longer exists.

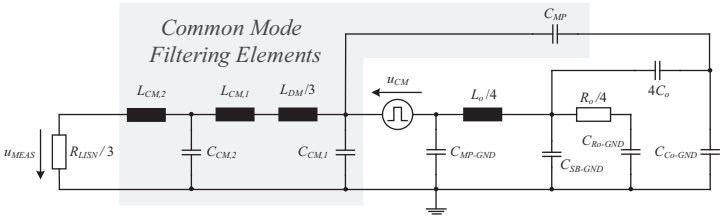


Figure 7.8: Two-stage CM filter (including the capacitive connection C_{MP} of input and output) for achieving the required attenuation of the CM emissions.

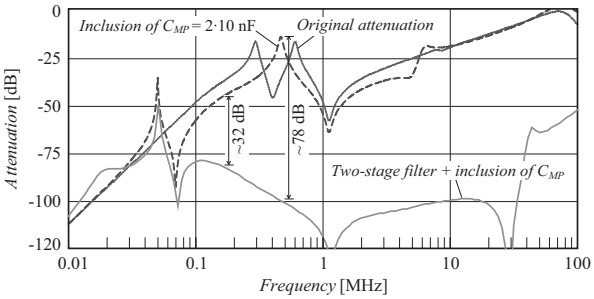


Figure 7.9: Attenuation plots. Shown are the different attenuation curves of the transfer function $U_{MEAS}(j\omega)/U_{CM}(j\omega)$ for different filter configurations, clarifying the effects of the insertion of each filtering element to the CM attenuation. The capacitance C_{MP} is included in all presented curves.

The effect of the addition of the filtering elements to the single-phase equivalent circuit of the final filter structure as shown in Figure 7.8 can be observed in Figure 7.9 through the plots of the transfer function $U_{MEAS}(j\omega)/U_{CM}(j\omega)$ for the different circuit configurations. It is observed that the final filter configuration is able to provide the required attenuation in the complete frequency range.

Employing the attenuation curves of Figure 7.9 and applying $\varsigma_{U_{CM}}(f)$, the final CE levels are estimated in Figure 7.10.

7.2.3 Experimental Verification

The final circuit schematic for the rectifier system including the CM filtering elements is shown in Figure 7.11.

With this system, Figure 7.12 shows the final result of the EMC CE measurement process performed with a four-lines 50 Ω / 50 μH LISN according to CISPR 16 [104]. The measurement is done in order to test the full compliance of the rectifier and includes both common and differential mode emissions from the 5 kW hardware prototype of the system.

The noise emissions in Figure 7.12 are mainly dominated by the DM noise emissions showing peaks at multiples of the switching frequency. Obviously, the CM noise emissions are attenuated sufficiently, and Class A is fulfilled in the frequency range 150 kHz–20 MHz. For fulfilling Class

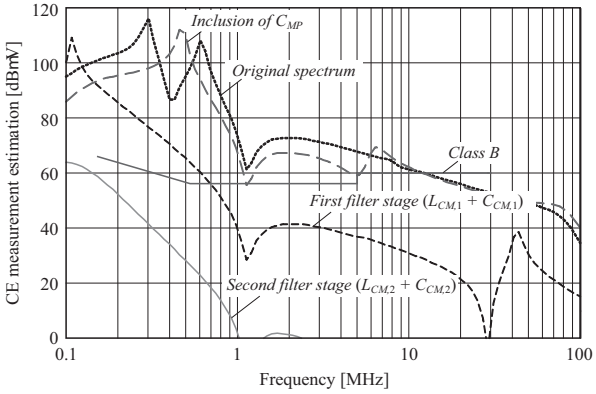


Figure 7.10: Estimated common mode conducted emission levels.

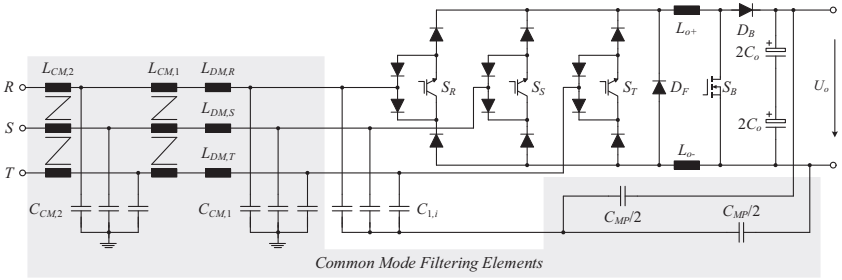


Figure 7.11: Final circuit structure for the three-phase PWM rectifier system including the designed CM input filter.

B the emission levels that increase around 10 MHz would have to be properly attenuated. This can be achieved through shielding of the EMC input filter and of the rectifier unit. Due to the superposition of the CM and DM emissions the measured curve lies slightly below the observed peaks. Furthermore, the measurement noise-floor prevents from observing the behavior beyond 400 kHz. Nevertheless, the dimensioning of the CM filter is validated.

7.3 Active Common-Mode Filtering

In modern power electronic systems, volumetric densities typically range between 1 kW/dm^3 and 3 kW/dm^3, depending on the employed technology and switching frequency. For higher power densities higher switching frequencies can be used but the EMC filtering components still occupy a large volume in the system, more than 30% in some cases. In a world where system and application space is becoming more and more expensive, the volumetric reduction of power supply components is of great importance. A proposed solution for the size reduction of EMC filters is the use of active systems [211, 237–239], commonly called active filters, instead of fully passive filters. High frequency active filters are broadly employed in signal processing, where low current and voltage levels are present. However as power levels increase, the construction of such systems becomes critical. Since wide-band amplifiers are to be used, these should be able to handle high current and voltage levels. This challenge motivates research in this field and is addressed in the following.

The scope of this work is limited to the common mode conducted

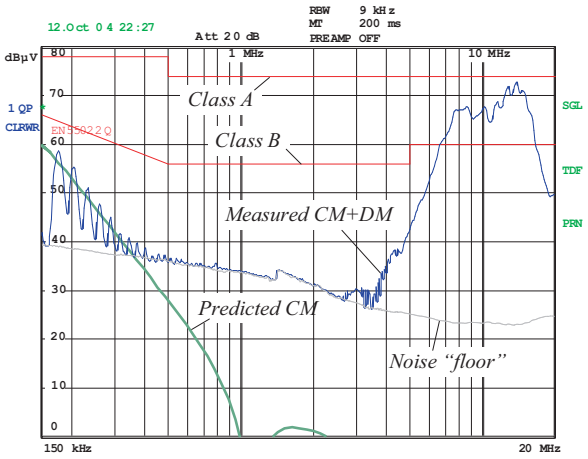


Figure 7.12: Conducted emissions measurement according to CISPR 22 of the rectifier ($U_{N,l-l,rms} = 400$ V, $U_0 = 400$ V, $P_0 = 5$ kW) including the proposed CM filter and the DM filter. This measurements were performed at the output terminals from a LISN (not with a current transducer).

emissions mainly in the frequency range from 150 kHz to 30 MHz. The connection from the EMC filter to the power circuits is on the AC mains side where a large 50 Hz or 60 Hz frequency component is present, along with its low frequency harmonic contents. In this application, the main function of the filter is the reduction of high frequency CM emissions. For that, the filters are based on linear HF power amplifiers as switched circuits currently do not provide the required operating bandwidth. The reduction of CM emissions is an important issue in all fields of electronics applications and the traditional approach is the use of Y-rated capacitors connected from lines to PE in addition to CM inductors. In most applications the size of these capacitors is limited due to safety regulations restricting the earth leakage currents, resulting in higher values of the CM filter inductors and larger filter volume, especially for high power systems. Aiming for the reduction of the total filter volume, while keeping low values of the low frequency leakage currents, an active circuit, which shapes the frequency response of a capacitor effectively increasing its value for high frequencies, is the solution presented in this section.

A practical active filter should be able to meet all relevant safety and EMC regulations, as well as high voltage surge requirements, and the filter stability should be independent from the impedances the filter is connected to. Cost is also a limiting factor and the active filter should not be more expensive than a conventional passive one.

From the potential advantages of the use of active filter circuits for reducing high frequency conducted emissions in power electronic circuits, the knowledge about the different possible structures and the design of the active EMC filter are essential. Four main types of circuits [211] are cited in the literature and shown in Figure 7.13 as simplified single-phase equivalent circuits. The classification into four circuits is based on the types of parameters employed in sensing and actuation paths. The basic strategies rely on the sensing of either current (Figure 7.13(a), [238–240] and Figure 7.13(b), [241–243]) or voltage (Figure 7.13(c), [212, 244] and Figure 7.13(d), [245–248]), and in the injection of a shunt current (Figure 7.13(b) and Figure 7.13(d)) or a series voltage (Figure 7.13(a) and Figure 7.13(c)) to the AC lines. In addition to the topologies of Figure 7.13 other active filter structures using a combination of the shown circuits can be implemented [214, 249–251]. One option is to use a current sensing feedback in combination with a voltage sensing feed-forward. Other options are to place the active filter power amplifier at the con-

verter output or at the DC-link terminals and sensing devices directly at the AC input lines or even combine two of these [251].

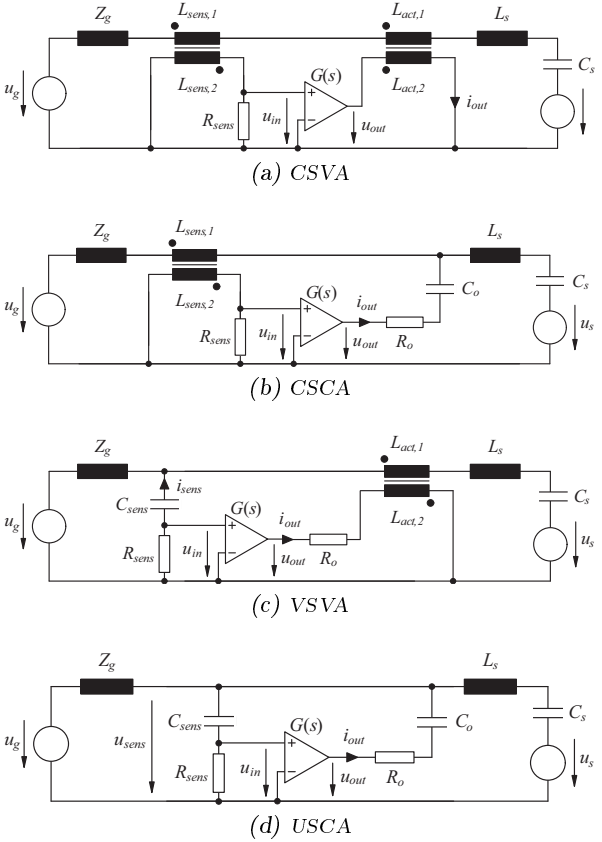


Figure 7.13: Basic active filter structures in their single phase equivalent circuits. The noise source is modeled as a voltage source in series with a capacitor C_s and an inductor L_s. The mains impedance Z_g is considered inductive. (a) 'Current Sensing / Voltage Actuation' CSVA; (b) 'Current Sensing / Current Actuation' CSCA; (c) 'Voltage Sensing / Voltage Actuation' VSVA; and, (d) 'Voltage Sensing / Current Actuation' USCA.

In this work, a filter topology to be placed directly at the AC lines of a three-phase power system is studied. It comprises a capacitive coupling ac-

tuation and a voltage sensing according to Figure 7.13(d) in a single-phase equivalent. The active filter structure is well known [245–248], therefore the emphasis is placed on the design of the feedback loop since it determines the system stability and challenges for the practical construction. It is shown that the correct placement of zeros and poles in the feedback path is of high importance [239], [245] for guaranteeing stable operation for a large range of mains and noise source impedance conditions. A theoretical basis for the determination of zeros and poles is presented, along with results obtained from a first prototype based on the described theoretical analysis.

7.3.1 Selection of Active Filter Topology and its Basic Operating Principle

By considering the circuits of Figure 7.13 one realizes that the noise source (C_s and L_s) and the power grid impedances (Z_g) are usually difficult to predict and/or control [252, 253] but should obviously be included in the stability consideration. For the topologies making use of a line current based feedback or actuation employing current transformers, it seems more difficult to decouple the system stability from the source and grid impedances. A difficult issue is that the current transformer needs a large bandwidth and the simple inclusion of an extra winding in a conventional CM inductor does not always guarantee a good high frequency magnetic coupling due to construction regarding safety regulations and the poor relative HF permeability characteristics of conventionally used materials. In addition, self resonances due the magnetic materials are to be expected as well as winding capacitances degrading the HF properties of the current transformer. The physical dimensions of a current transformer can also represent a drawback of such concepts when compared to capacitive based ones. For these reasons, the cost of a good HF current transformer must be added to the filtering system. Therefore, a topology based on capacitive sensing of the line voltage and utilizing also capacitors in the actuator stage seems to be a good choice for an active filter connected to the AC lines. The filter topology considered in this work is presented in the simplified schematic in Figure 7.14, which corresponds to the circuit in Figure 7.13(d).

This topology is comprised of two common mode inductors ($L_{CM,1}$ and $L_{CM,2}$), one coupling capacitor (C_o), a sensing path (G_{sens}) including

a low frequency attenuation network for rejection of any unwanted high amplitude low frequency components and an actuator, which is realized with a linear HF power amplifier (G_{amp}). This structure presents some advantages such as:

- The filter structure and its principle are simple, presenting a potentially high stability range, increasing the possible filter attenuation in the frequency band of interest;
- Both, sensing (G_{sens}) and output coupling (through C_o) can be performed through Y-rated capacitors;
- As the needed inductance and capacitance values decrease by the use of an active feedback, better high frequency performance is achieved than with a non-active filter, as smaller components usually present higher resonance frequencies;
- The implementation is potentially safe since the feedback sensing is done with low voltages; only a single HF power amplifier needs to be employed.

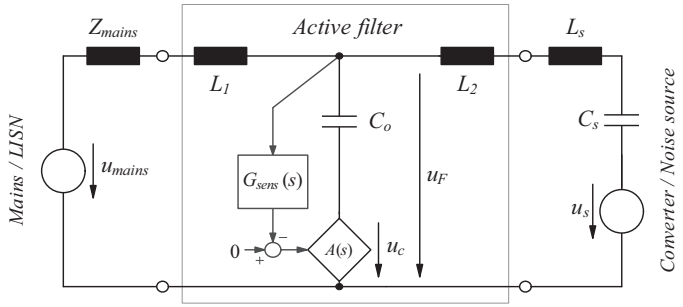


Figure 7.14: Simplified single-phase schematic showing the basic principle of the selected CM filtering system.

The use of the topology presented in Figure 7.14 has as its main advantage the use of two CM inductors and a capacitor, which are usually already present in typical CM filters, however with smaller inductance values. For the case of CM noise filtering, these components are common mode chokes and Y-capacitors, which technology are well know and do

not make the filter more expensive. Since Y-capacitors have their values limited due to the safety limitation of the allowable earth leakage currents, the main idea with this active filter topology is to use the existing values of Y-capacitors and virtually increase the capacitance by proper shaping of the feedback frequency response, thus allowing a noticeable reduction of the inductors, which are usually large, heavy and costly in high power systems.

The basic principle of the topology shown in Figure 7.14 is to increase the equivalent capacitance for high frequencies by using a feedback loop. This is illustrated in Figure 7.15 where one can see that, for the lower frequency end the original capacitance of C_o is effective, but for higher frequencies an increase in the capacitance is possible as the feedback gain increases, according to

$$Z_{act}(s) = \frac{U_{act}(s)}{I_{act}(s)} = \frac{1}{sC_o} \cdot \frac{1}{1 + G_{sens}(s)}. \tag{7.7}$$

With eq. (7.7) it can be seen that the capacitance is effectively multiplied by the gain G_{sens}. This characteristic is very important in this type of system, since the capacitance at low frequency should be kept as small as possible due to the limited earth leakage current.

The configuration for the design of the active filter regarding its attenuation is depicted in Figure 7.16, where the model of a simplified LISN is included. This configuration allows for the study of the required filter performance, with R_{lisn}, according to CISPR 16 [104], equal to 50 Ω / 3. This is because the three-lines of a LISN are in parallel for CM currents.

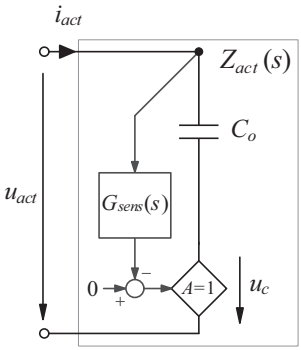
7.3.2 Stability Analysis and Feedback Structure

There are four strict requirements for the filter structure:

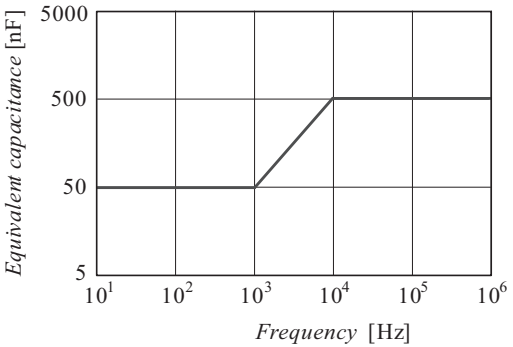
i. The attenuation of high frequencies needs to be higher than for a passive filter with the same components;

ii. The value of the capacitor (C_o) is limited due to the safety considerations (earth leakage currents);

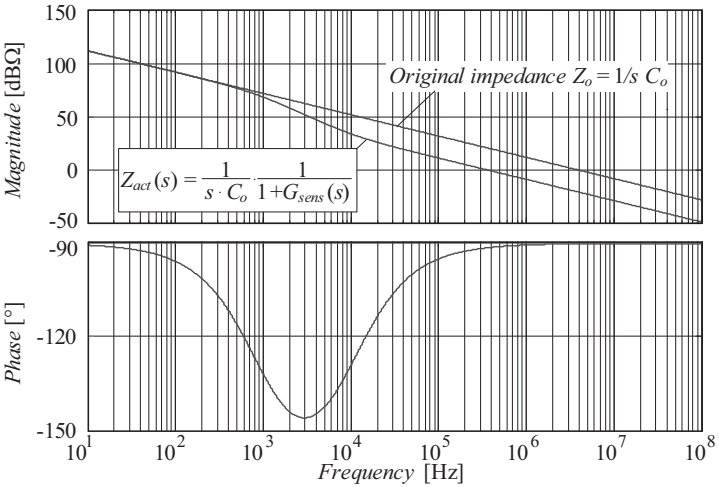
iii. The 50/60 Hz and the low frequency harmonic components present in the voltage u_F are quite large when compared with the high fre-



(a) Capacitor with voltage feedback



(b) Asymptotic capacitance increase



(c) Simulated impedance curves

Figure 7.15: Basic principle of an active filter with capacitive coupling. (a) Impedance Z_{act} of a capacitor with a voltage feedback loop; (b) equivalent capacitance is increased in the higher frequencies through the active feedback action; (c) example of impedance curves $Z_{act}(f)$ illustrating the feedback action.

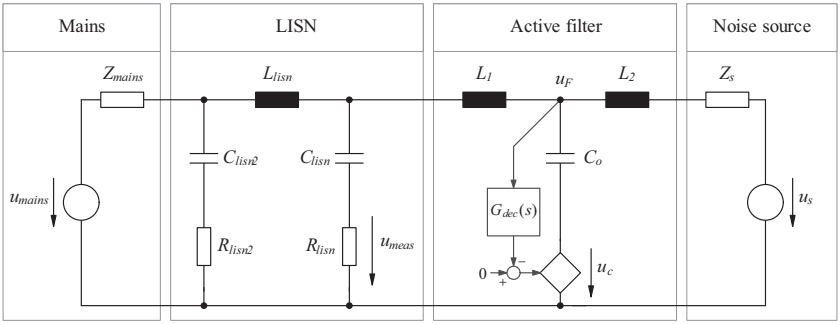


Figure 7.16: Single-phase equivalent circuit for the active filter with a LISN included.

quency components. As a requisite they must be well attenuated in the feedback loop to prevent the amplifier from saturating;

iv. The system has to be stable for a large range of noise source and mains impedances.

Once an active part is included in the topology, the natural stability achieved with only passive elements is not further guaranteed and a careful study of the stability should be carried out. The study of possible gains in the feedback loop and the sensing/control structures that lead to higher stability margins is of great importance since the 50/60 Hz component requires a high attenuation factor.

The use of Bode diagrams for the stability study is not sensible since the active filter structures do not fulfill the requirement — steadily decrease of the open loop gain and phase curves — [225] for a straightforward analysis by frequency domain plots. Thus, the root locus analysis is the tool to be used.

As a starting point for the stability analysis of the proposed active filter the circuit of Figure 7.17 is used where the reactive components consider the inductive characteristics of the mains and the mainly capacitive nature of the CM noise source. The parasitic elements of the main components, such as the resistances of inductors $L_{CM,1}$ and $L_{CM,2}$ are not explicitly shown, but as it is seen later they are crucial for the stability analysis.

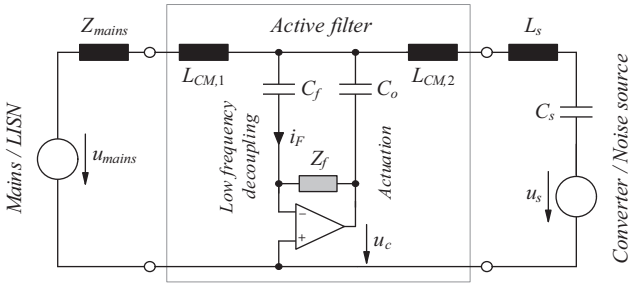


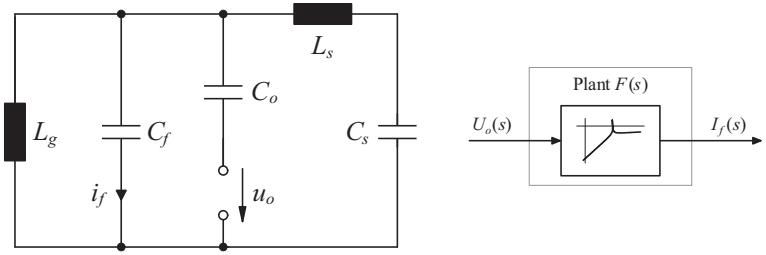
Figure 7.17: Basic single-phase equivalent circuit for the active filter including an amplifier and showing the variables of interest i_F (sensing) and u_c (actuation).

The closed loop system can have its open loop transfer function calculated by opening the loop at the output connection of the amplifier u_c. This is a logical step since the output impedance of the amplifier is typically much lower than the input impedance of the output coupling capacitor C_o. By opening the loop, short-circuiting the voltage sources and assuming that the input voltage of the operational amplifier is zero, fact that can be assumed because this voltage is much smaller than the voltage across C_f, the system can have its stability analyzed through the circuit depicted in Figure 7.17, where the impedances $L_{CM,2}$ and Z_{mains} are summed to L_g and the impedances $L_{CM,1}$ and L_{source} to L_s.

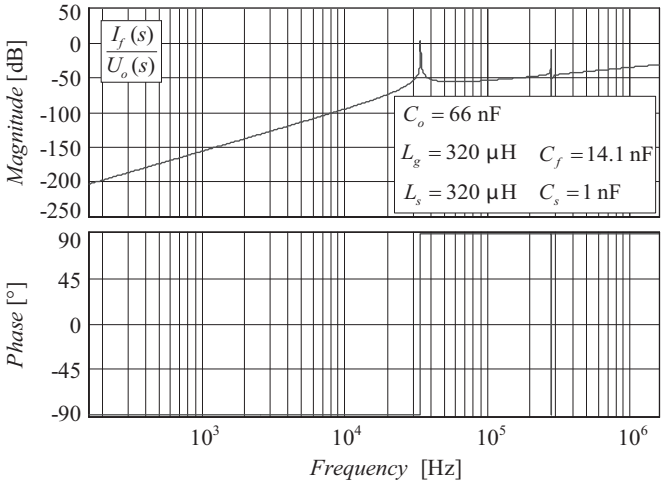
The sensing capacitance C_f is also considered, since it adds a zero and changes the positions of the poles. With these considerations, the feedback variable of interest is the current i_F, which is multiplied by the impedance Z_f for the final shaping of the feedback loop.

As an example, a Bode plot of the considered plant, for the parameters given in Figure 7.18, is shown in Figure 7.18(b). The system under consideration is a three-phase adjustable speed drive (ASD) based on a 6.8 kVA Sparse Matrix Converter (SMC), switching at a frequency of $f_P = 10/20$ kHz (input/output stage switching frequencies). The total capacitance is limited for safety reasons and the designed value is 22 nF per phase, leading to a total of 66 nF. A decrease of ten times in the former CM filter inductance of around 6 mH is desirable. Therefore, two inductors of 320 μH have been chosen. The noise source may vary depending on the nature of the load (passive, motor) and the minimum value is around 1

nF, which is measured in the SMC without load. The sensing capacitance C_f depends on all the parameters of the complete active circuit and a value of 14.1 nF is chosen.



(a) *Active filter plant*



(b) *Bode plots*

Figure 7.18: Circuit used for the stability analysis. Shown are (a) the basic circuit of the analyzed active filter plant with its transfer function and (b) an example of Bode plots for an analyzed active filter plant.

If no damping elements are considered, the root locus for the system of Figure 7.17 is plotted in Figure 7.19(a) from,

$$\frac{I_f(s)}{U_o(s)} = \frac{s^3 L_g C_f C_o (s^2 C_s L_s + 1)}{s^4 L_g L_s C_s (C_f + C_o) + s^2 \left[L_g (C_f + C_o - C_s) + L_s C_s\right] + 1}. \tag{7.8}$$

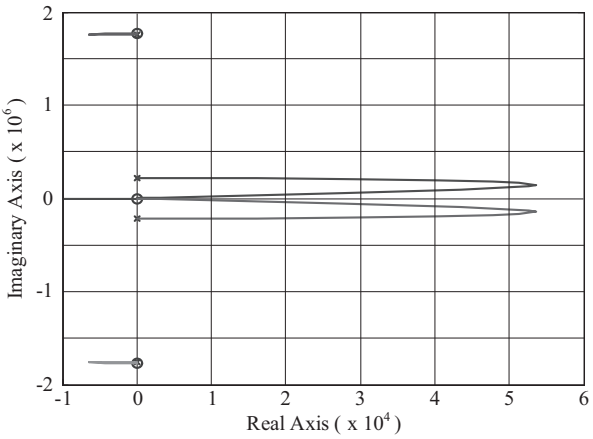
A proper modeling of the system, though requires that the resistive elements of the circuit are considered, as they move the plant singularities to the left half plane as shown in the root locus of Figure 7.19(b). Considering parasitic effects, it is feasible to employ simple feedback structures, which can properly reject the low frequency components, but have their maximum HF gain limited. The analysis of the root loci plots of Figure 7.19 shows that the plant without the inclusion of parasitic resistances would be extremely difficult to stabilize, presenting three zeros at the origin and four poles at the imaginary axis.

As previously cited, a limited supply voltage should be used for the power amplifier and it is not desirable that the closed loop system influences the circuit behavior at 50 Hz. For a single-phase system, it is necessary that the sensing network attenuates the low frequency components of the measured voltage. A value of approximately -40 dB attenuation for the 50 Hz component would imply that, for a 300 V peak in the line to ground (PE) voltage, a peak voltage of 3 V appears in the output of the power amplifier. In this case a minimum attenuation of -50 dB at 50 Hz was chosen as a starting point.

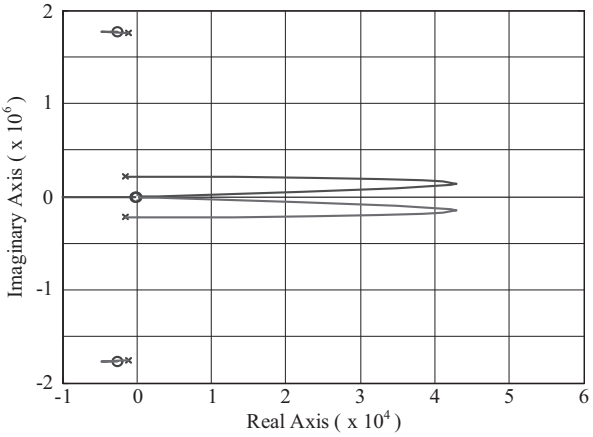
Another specification is that the high frequency gain should be practical with a low cost HF power amplifier. This specification also matches the gain limitation imposed by the plant's characteristics. The actuator for the proposed system is a linear HF power amplifier G_{amp} presenting enough bandwidth in order to allow a good performance. A good model for such amplifier is a first order low pass filter with a limited output swing due to the available supply voltage.

The most simple and desirable way to sense the voltage u_F is to use a high-pass filter. In the case at hand it is composed of two zeros, one at the origin and the other above 10 kHz. This results in a high attenuation of the 50/60 Hz component.

Poles are placed at high frequency in order to limit the high frequency gain. The final bandwidth of the feedback loop must be limited due to the power amplifier characteristics. This is achieved by placing a dominant pole at a frequency where the high frequency gain is rolled-off correctly,



(a) Root locus



(b) Changes due to resistive elements

Figure 7.19: Root locus diagrams for the active filter plant $I_f(s)/U_o(s)$ for the parameters specified in Figure 7.18. (a) Root locus for a filter plant purely reactive; (b) diagram illustrating the changes in the positions of the singularities due to the inclusion of parasitic resistive elements for the same filter plant. The parasitic resistance values are obtained from impedance measurements performed on the filtering components and on the Sparse Matrix Converter and the assumed values are shown in the three resistors depicted in Figure 7.21.

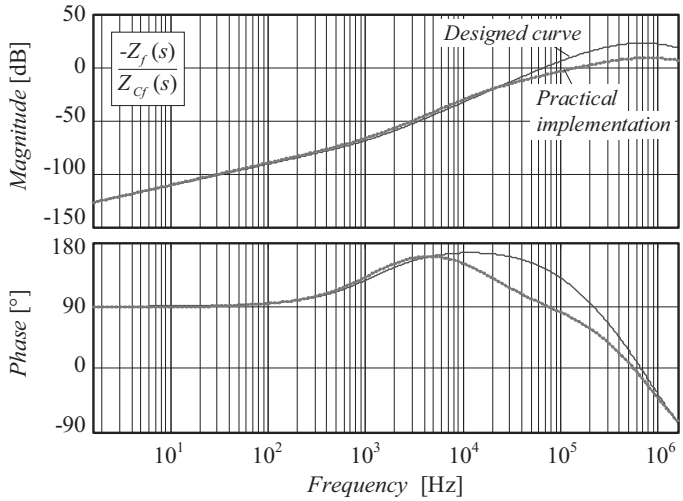


Figure 7.20: Bode diagrams for the designed feedback loop (cf. Figure 7.21). The high frequency gain for the practical implementation was lowered due a non-ideal characteristic of the HF power amplifier not accounted for in the model.

thus guaranteeing that the design is carried out with the assumption that the amplifier behaves like an ideal operational amplifier.

Defining the sensing capacitor impedance as

$$Z_{Cf}(s) = \frac{1}{s\,C_f}, \tag{7.9}$$

the designed feedback loop, $-Z_f(s)/Z_{Cf}(s) = U_c(s)/U_f(s)$, for an ideal operational amplifier can be observed in Figure 7.20. A curve for the designed loop and another curve for the actual performance of the finally implemented system are shown. The maximum slew-rate of the implemented power amplifier prevented higher gains to be applied in practice because it distorts the output signal in a way that the high frequency components are attenuated and phase-shifted non-linearly. This reduction in the HF gain limits the final achievable attenuation increase.

Considering the amplifier non-idealities as a transfer function $G_{amp}(s)$, the transfer function $U_c(s)/I_f(s)$ is given by

$$\frac{U_c(s)}{I_f(s)} = -Z_f\,\frac{G_{amp}(s)}{1+G_{amp}(s)}, \tag{7.10}$$

from where it is seen that it impacts the HF behavior of the designed active filter.

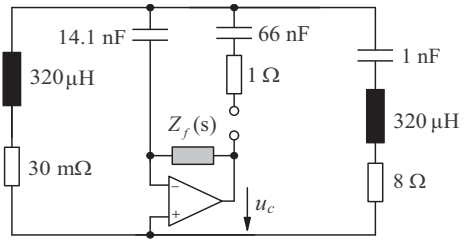


Figure 7.21: Circuit used for the transmission loop calculations and the employed transfer function $Z_f(s)$. Parasitic resistances from inductors and load have been estimated through impedance measurements and the output resistance of the amplifier is estimated through circuit simulation of the designed amplifier shown in section 7.3.3.

The final control-oriented block diagram for the circuit of Figure 7.21 of the designed system is presented in Figure 7.22, where the influence

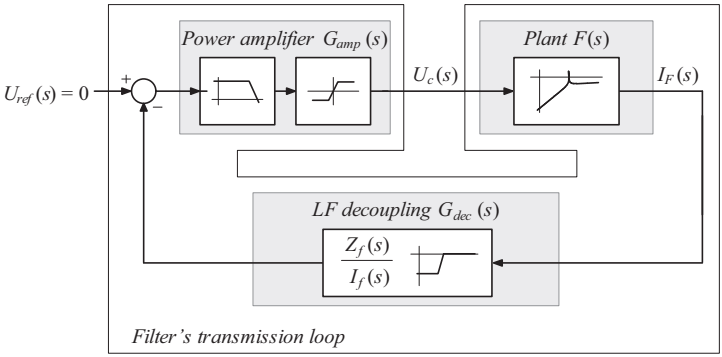


Figure 7.22: Filter's transmission loop block diagram.

of the amplifier transfer function is simplified just for the sake of clarity. This is used to obtain the final root locus diagram of the transmission loop which is plotted in Figure 7.24. Respective bode plots are presented in Figure 7.23. The inductors are modeled here as a constant inductor in series with a resistance, allowing the system stability to be analyzed with mathematical tools for linear systems. With the previously shown feedback structure, the determining part of the root locus is the region close to the origin, which includes the low frequency zeros and the dominant complex poles. The design ensures that large values of mains and noise source impedances can be employed. The final system has been successfully tested with noise source capacitances ranging from 10 pF up to 10 μF and mains-sided impedances from around 100 nH up to 12 mH measured at 1 kHz. Furthermore, the design ensures that if minimum values for the inductors $L_{CM,1}$ and $L_{CM,2}$ are employed, system stability is given for widely varying external impedances.

7.3.3 Amplifier Design

The main points in specifying the amplifier are: (*i*) DC supply voltage; (*ii*) power bandwidth, and; (*iii*) power supply rejection ratio (PSRR). Since costs are typically important, a trade-off between costs and performance is usually required as well.

To start with, the circuit of Figure 7.25 is considered, where u_s in

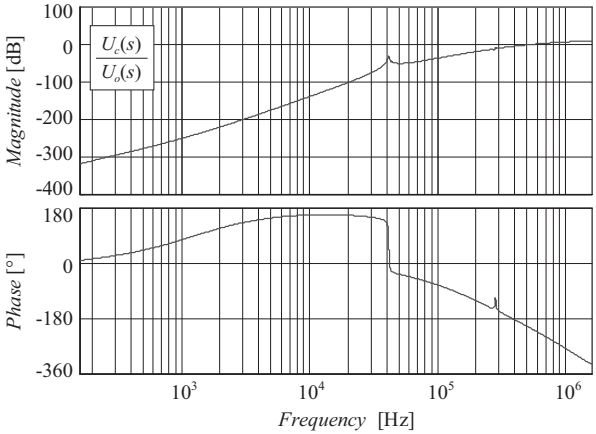


Figure 7.23: Bode plots for the modeled transmission loop including resistive elements estimated from impedance measurements and the high frequency pole modeling the power amplifier G_{amp}.

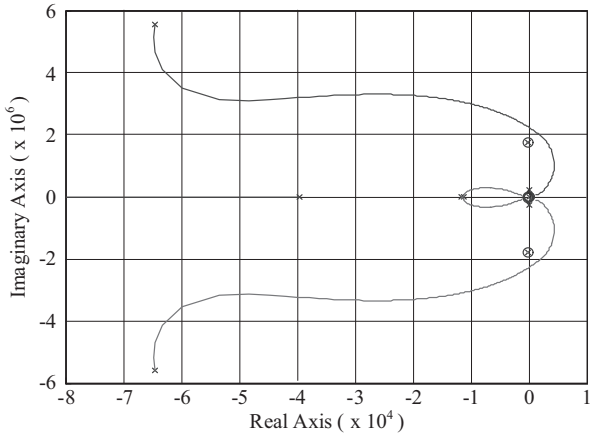


Figure 7.24: Root locus diagram for the designed system, which is shown in Figure 7.21.

series with C_s represent a noise source, inductance L_s the first filter inductor and the branch formed of C_o the filter capacitance, u_c the output voltage of the power amplifier with an output impedance R_o limited by the resistors connected at the amplifier output. The remainder of the circuit is neglected. The aim is to generate a voltage waveform at u_o capable of injecting a compensating current, which should keep the voltage at the node between L_s and C_o as close as possible to the ground potential 0 V, thus current i_g should equal zero.

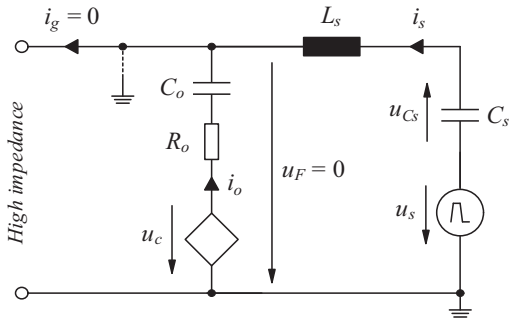


Figure 7.25: Simplified circuit for studying the requirements for a HF power amplifier to be used in active mains filtering. Noise source: u_s in series with C_s; amplifier output: u_o and output resistance R_o.

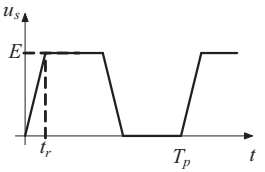


Figure 7.26: Considered waveform at the noise source.

Two simplifying assumptions are made: (*i*) a trapezoidal shape with an amplitude E and a finite rise time t_r at u_s and (*ii*) u_f equals zero (cf. Figure 7.26). From circuit inspection, the following ordinary differential equations are derived:

$$L_s \frac{di_s}{dt} = u_s - u_{Cs} \tag{7.11}$$

$$C_s \frac{du_{Cs}}{dt} = i_s \tag{7.12}$$

$$C_o \frac{du_c}{dt} = i_o + C_o R_o \frac{di_o}{dt} \tag{7.13}$$

Equations eq. (7.11) and eq. (7.12) represent the circuit branch in which the noise current i_s is generated. Assuming the initial conditions

$$i_s(0) = 0 \tag{7.14}$$

$$u_{Cs}(0) = 0, \tag{7.15}$$

the solution for i_s for the ordinary differential equations system formed by eq. (7.11) and eq. (7.12) is given by,

$$i_s(t) = C_s \frac{E}{t_r} \left[\cos\left(\frac{t}{\sqrt{L_s C_s}} \right) - 1 \right]. \tag{7.16}$$

Considering the other branch of the circuit, the circuit is characterized by equation eq. (7.13). The initial condition for this circuit is assumed as

$$i_o(0) = 0. \tag{7.17}$$

Solving eq. (7.13) for eq. (7.17) leads to,

$$\frac{du_c}{dt} = \frac{i_o(t)}{C_o \left(e^{\frac{-t}{\sqrt{C_o R_o}}} - 1 \right)}. \tag{7.18}$$

The condition which should be fulfilled is.

$$i_o(t) = -i_s(t). \tag{7.19}$$

Assuming $R_o = 0\ \Omega$, inserting eq. (7.19) into eq. (7.18) and solving the equation for du_c/dt, the output voltage of the amplifier u_o must be

able to achieve the following parameters:

$$\frac{du_{c,max}}{dt} = \frac{C_s}{C_o}\frac{E}{t_r}\frac{\cos\left(\frac{t}{\sqrt{L_s C_s}}\right)}{\left(e^{\frac{-t}{\sqrt{C_o R_o}}} - 1\right)} \tag{7.20}$$

$$u_{c,max} = \int_0^{t_r} \frac{C_s}{C_o}\frac{E}{t_r}\frac{\cos\left(\frac{t}{\sqrt{L_s C_s}}\right)}{\left(e^{\frac{-t}{\sqrt{C_o R_o}}} - 1\right)} dt. \tag{7.21}$$

Equations eq. (7.20) and eq. (7.21) define the requirements for ideal cancellation, based on the given simplifications and, with this, it is possible to evaluate the requirements for an amplifier given specific circuit parameters as shown graphically in Figure 7.27 and Figure 7.28, where the surfaces for the required DC supply voltage $V_{cc} = u_{c,max}$ are displayed for a perfect compensation of the noise source voltage. An example for maximum voltage ratio $du_{c,max}/dt$ surface is shown in Figure 7.29, translating in the requirement for the amplifier power bandwidth PBW. In Figure 7.30 the range where an ideal noise compensation can be achieved is shown, given the specified amplifier and circuit parameters.

Based on the given requirements and aiming for a prototype to be used with an "state-of-the-art" three-phase adjustable speed drive (ASD) based on a 6.8 kVA Sparse Matrix Converter, where the switching times are usually under 500 ns and the switching frequency $f_P = 10/20$ kHz, it seems to be adequate that an amplifier with a DC supply of $V_{cc} = \pm 30$ V and a power bandwidth of $PBW = 800$ kHz is employed. A discrete HF power amplifier as shown in Figure 7.31 was designed and built for a system being fed with a ± 30 V external power supply. The amplifier is built with conventional SMD components (cf. Table 7.2) and exhibits a closed loop -3dB bandwidth of approximately 1 MHz and a power bandwidth of approximately 800 kHz.

7.3.4 Practical Implementation of the Active Filter

A three-phase filter employing the presented feedback structure was built in order to test the presented mathematical models. The filter schematics

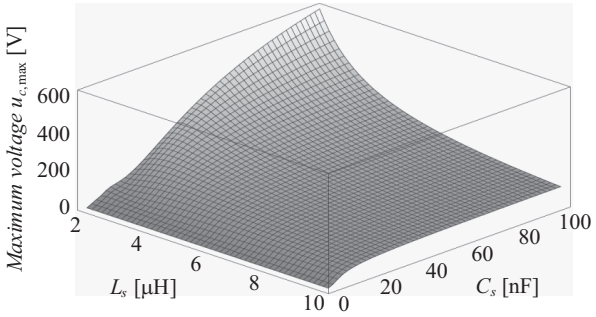


Figure 7.27: HF power amplifier requirement translated into DC supply voltage $V_{cc} = u_{c,max}$, for $C_o = 66$ nF, $R_o = 1\,\Omega$ and $E = 400$ V, where $u_{c,max}$ is shown as a function of noise source capacitance C_s and inductance L_s for ideal compensation and t_r=1 μs.

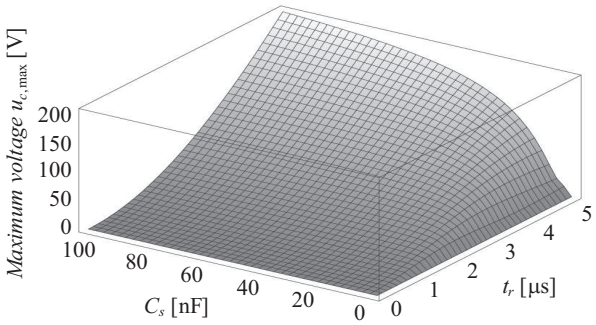


Figure 7.28: HF power amplifier requirements translated into DC supply voltage $V_{cc} = u_{c,max}$, for $C_o = 66$ nF, $R_o = 1\,\Omega$ and $E = 400$ V, where $u_{c,max}$ is a function of noise source capacitance C_s and and rise time t_r for ideal compensation and L_s=100 μH.

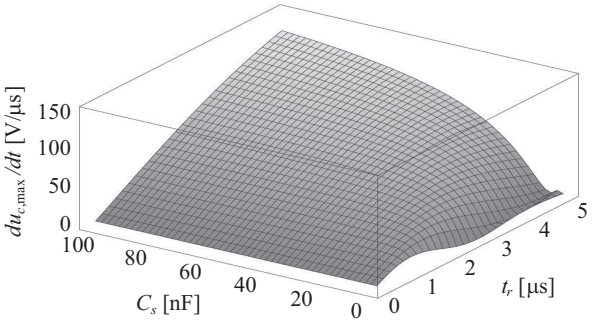


Figure 7.29: HF power amplifier requirements translated into maximum voltage change ratio $d_{uc,max}/dt$, for $C_o = 66$ nF, $R_o = 1\,\Omega$ and $E = 400$ V, where $d_{uc,max}/dt$ is a function of noise source capacitance C_s and and rise time t_r for ideal compensation and L_s=100 μH.

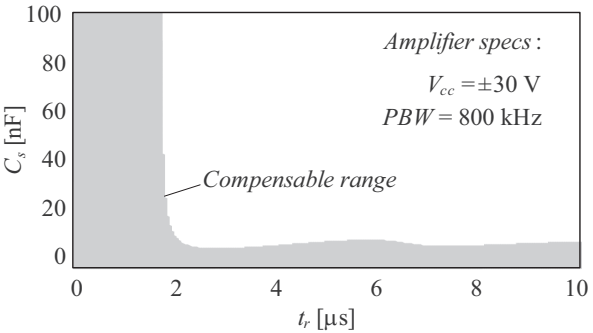


Figure 7.30: Compensable range (shaded region) valid for L_s=100 μH for an amplifier with $V_{cc} = \pm 30$ V and PBW=800 kHz.

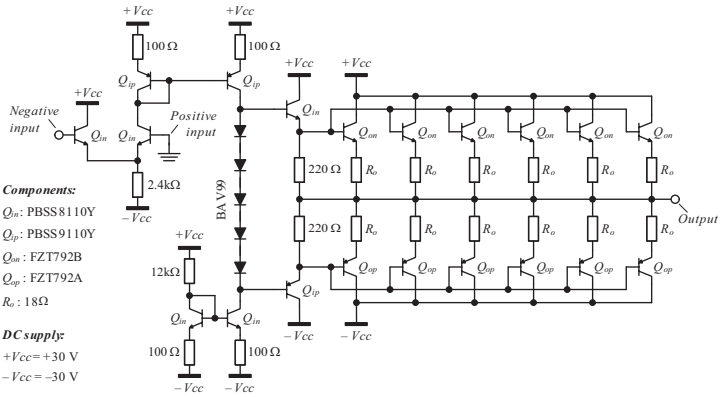


Figure 7.31: Schematic of employed linear HF power amplifier. The topology is selected aiming for low implementation costs.

are presented in Figure 7.32 and the main components are specified in Table 7.2. The filter employs inductors built with nanocrystalline cores (VAC VITROPERM 500F), which have a highly resistive behavior at high frequencies, helping to ensure high impedances at high frequencies, a well damped self-resonance and good thermal stability. The inductor models account for the complex permeability curves from the manufacturer and the parallel capacitances are modeled as described in section 4.5. The capacitor models include capacitance, equivalent series resistance (ESR) and inductance (ESL) as given in the datasheet [159].

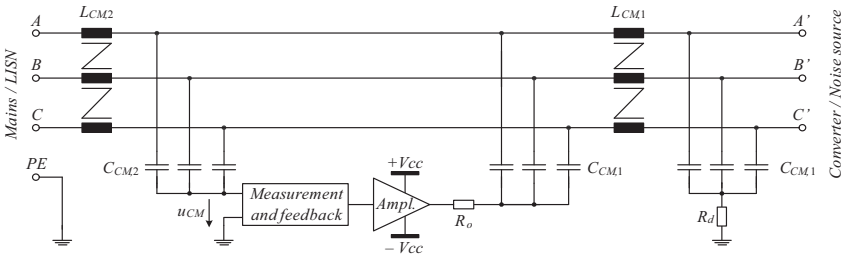


Figure 7.32: Circuit schematic for the designed filtering system. Components are specified in Table 7.2.

Table 7.2: Selected components for the active filter prototype.

Component	*Specification*
$C_{f,i}$	Y2 SMD Capacitor, Murata X7R Series GC 4.7 nF – 250 Vac
$C_{o,i}$	Y2 Capacitor , Epcos MKP B81122 22 nF – 250 Vac
$C_{CM,i}$	Y2 SMD Capacitor, Murata X7R Series GC 1 nF – 250 Vac
$L_{CM,1}$	Vaccuumschmelze VAC VITROPERM 500F T6000-6-L2012-W498 – OD(12.5) ID(10) H(5) mm N = 3 × 3 turns, ϕ 1 mm
$L_{CM,2}$	Vaccuumschmelze VAC VITROPERM 500F T6000-6-L2012-W498 – OD(12.5) ID(10) H(5) mm N = 3 × 4 turns, ϕ 1 mm

In hand of this modeling, the filter insertion loss (50 Ω input / 50 Ω output measurement) curves for the designed filter were calculated as shown in Figure 7.33, where the curve for the filter without feedback can be compared with real measurement data (indicated by crosses) and a good agreement is observed, except for a structural resonance[1] at approximately 20 MHz. Based on the modeled components two simulations were performed and their results are also presented in Figure 7.33. The first simulation, shown in the middle trace of Figure 7.33, gives the filter insertion loss in case a band-limited amplifier is used, showing that an increase in the attenuation is observed up to the amplifier's frequency limitation. The last simulation, bottom trace, is valid for an infinite bandwidth amplifier. The potential for such systems is clear and with larger amplifiers bandwidth, better performance is observed. Based on the successful simulation results a prototype based on the structure shown in Figure 7.32 was built. The prototype is rated for 10 A / 400 V / 50 Hz and a photograph is shown in Figure 7.34.

The first step in the prototype testing was to analyze the system stability under different source and load impedances. Inductors with ferrite

[1]This resonance has not been clarified in practice because of its minor effects observed in the transfer functions.

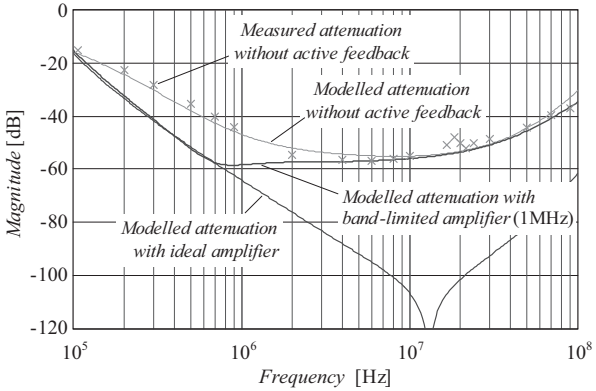


Figure 7.33: Insertion loss curves (50 Ω input / 50 Ω output measurement) for different feedback structures. The crosses represent real measurements on the built filter board with no active feedback, while the top trace shows the insertion loss for the mathematically modeled filter. The middle curve depicts the expected behavior when utilizing an active feedback, which makes use of a band-limited power amplifier, while the lower curve shows the performance with the circuit employing an infinite bandwidth amplifier.

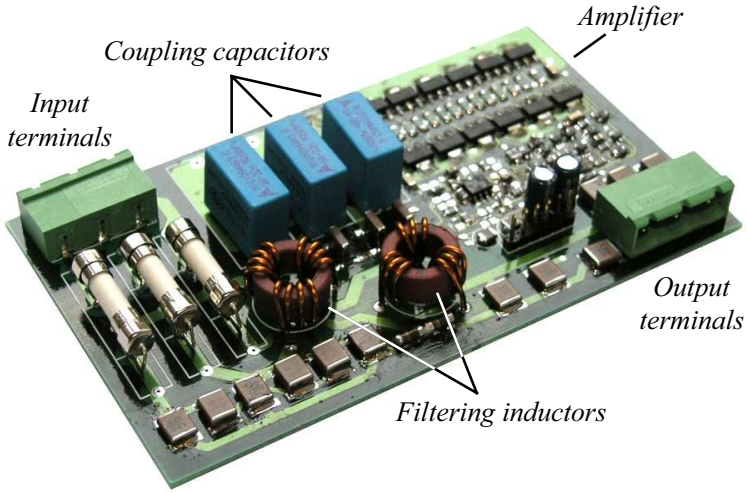


Figure 7.34: Three-phase filter prototype photograph (120 × 70 × 17 mm^3).

cores of 1 mH and 6 mH, and inductors with nanocrystalline cores of 4.2 mH and 12 mH, measured at 1 kHz, were used as artificial mains and/or source impedances. On the noise source side, capacitors in the range of 10 pF up to 10 μF were employed. Short-circuiting of the filter inputs to PE was also tested. Over this impedance range the filter operated in a stable manner. Attenuation measurements were also performed employing different source and load impedances. Figure 7.35 presents the measurement for a 8 Ω input impedance and a 50 Ω output for the filter structure with and without (C_f and $C_{o,i}$ shorted to PE) active feedback. The same measurements were repeated for a 4.2 mH source impedance and the results are presented in Figure 7.36, showing the increase in the filter attenuation in the range of 100 kHz to 1 MHz, where the amplifier bandwidth ends.

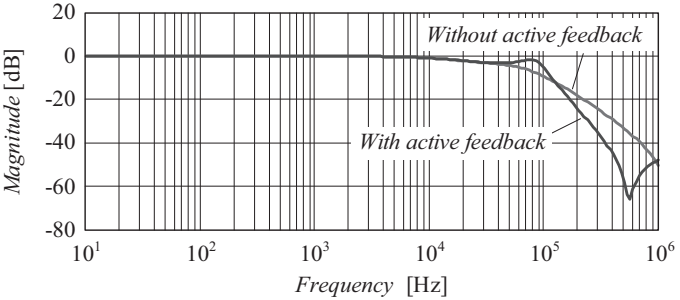


Figure 7.35: Performance for the designed filter with a source impedance of approximately 8 Ω. Measured attenuation curves for a load impedance of 50 Ω.

Another performed test made use of a square wave generator as noise source in series with a 400 pF SMD capacitor mounted on a PCB with a very small space between the capacitor and the ground plane in the back side of the PCB. As load, a four-line 50 Ω /50 μH V-network LISN was used and its output connected to an EMC test receiver. Measurements with and without filter are presented in Figure 7.37. For the measurement with the active feedback, it is demonstrated that higher attenuation is achieved up to 1 MHz. At 2 MHz a resonance in the amplifier circuit due to the distortion caused by its slew-rate limitation is seen, causing higher emission levels than those of the filter without feedback. In the higher frequency range the same conducted emission levels are seen.

The last presented test is performed with the active filter board connected at the input of an ASD built on a 6.8 kVA Sparse Matrix Converter

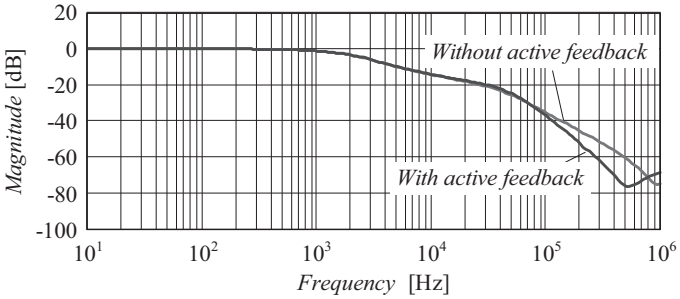


Figure 7.36: Performance of the designed filter with a source impedance of approximately 4.1 mH (measured at 1 kHz). Measured attenuation curves for a load impedance of 50 Ω.

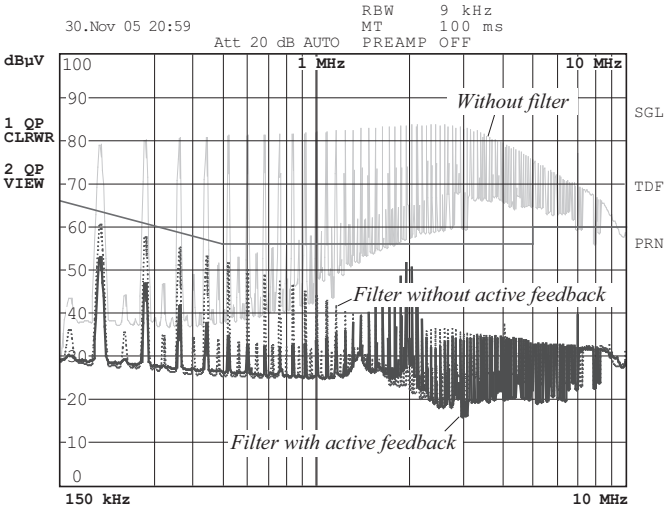


Figure 7.37: Conducted emission measurements performed employing a square wave generator switching at 40 kHz with a rise/fall time around 30 ns in series with a capacitance of approximately 400 pF. Upper trace shows the emission levels without a filter. Dashed trace shows the measurement result with no active feedback. Third trace presents the results when the proposed electronic feedback is active.

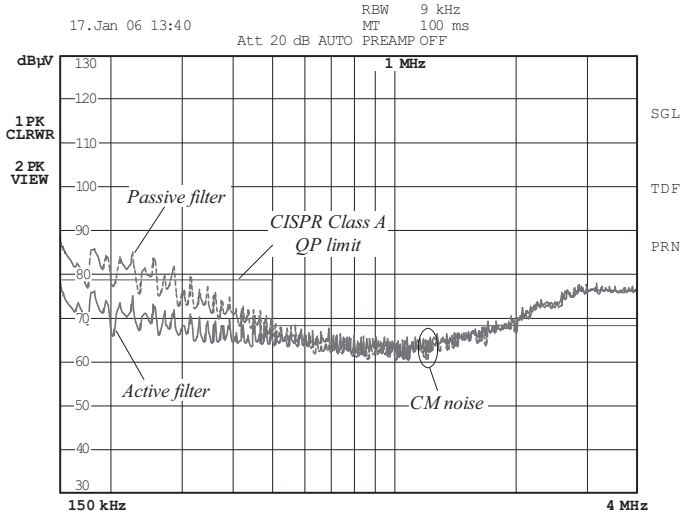


Figure 7.38: CM conducted emission measurements (acquired with the help of a three-phase CM/DM noise separator as in section 5) performed on a three-phase adjustable speed drive (ASD) based on a 6.8 kVA Sparse Matrix Converter, switching frequency $f_P = 10/20$ kHz. Dashed upper trace shows the emission levels without the active feedback. Full trace shows the measurement result with the electronic feedback active.

(SMC). The SMC board has three SMD Y-capacitors of 4.7 nF connecting each phase terminal to the PE. The load of the SMC is an RL load not connected to PE. A four-line 50 Ω /50 μH V-network LISN was used with its outputs connected to a three-phase noise separator and then to an EMC test receiver. Measurements performed with the noise separator CM output, with and without filter, are presented in Figure 7.38. For the measurement with the active feedback, it is clear that higher attenuation is achieved up to 500 kHz. In the higher frequency range the same conducted emission levels are seen, therefore the active filter does not influence this range. As a larger CM inductor is present at the input of the SMC, due to high CM voltages and for this reason lower gain in attenuation is achieved, but this proves that the active filter can be used interfacing the grid and an adjustable speed drive.

7.3.5 Low Frequency Rejection posing Limitations in Active Filter Performance

From the results presented in the previous sections it can be seen that the attenuation improvement with the designed active filter was not 40 dB as typically desired and sometimes demonstrated in some experimental applications [212,214]. It is found that when a high-pass filter is applied at the feedback loop, the HF feedback gain shall be limited in order to guarantee stability for a wide and practical range of mains impedance. To acquire an insight into the limitations to the gain in attenuation some theoretical studies are carried out in the following for different active filter structures, represented through simplified models. The mains impedance is here modeled as an inductor with a value of $L_g = 50\ \mu$H for all cases.

Voltage Sensing / Current Actuation (VSCA) Filter with Passive Damping

The circuit of Figure 7.39 is used, where the network composed of L_d and R_d provide passive damping to the circuit, thus possibly allowing for higher feedback gains. This is, of course, not practical since access to the mains impedance would be required. On the other hand it is useful in order to gain insight about the stringent requirements for the feedback design.

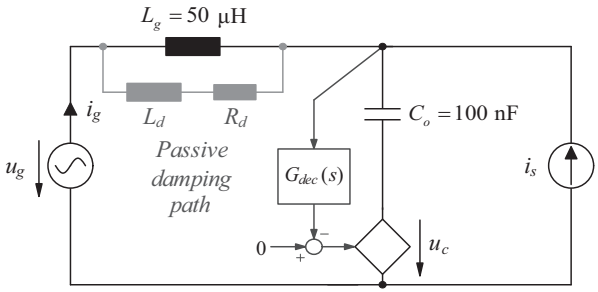


Figure 7.39: Analyzed circuit for a 'Voltage Sensing / Current Actuation' (VSCA) active filter with passive damping.

As a starting point some assumptions are made:

- The noise source is modeled as a current source i_s.
- The sensing network $G_{sens}(s)$ shall provide more than 40 dB attenuation at 50 Hz. This is achieved with a second order high pass filter defined as,

$$G_{sens}(s) = \frac{100s^2}{s^2 + 53855.9s + 1.4212 \cdot 10^9}. \tag{7.22}$$

- The HF gain in attenuation for the active filter shall be around 40 dB, when compared to a passive filter with the same components.
- The circuit should be stable.

Based on the listed requirements and on the circuit of Figure 7.39, the real part of the complex conjugated dominant poles of the open loop transfer function (OLTF) are plotted in Figure 7.40, where it is seen that only a very limited range of impedances L_d and R_d drive the real part of the dominant poles to the negative region, leading to stable operation modes. This can be interpreted as a maximum equivalent mains

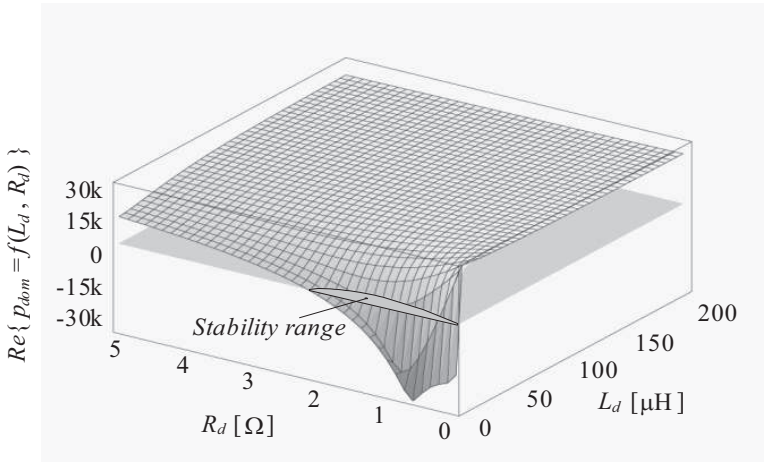


Figure 7.40: Real part of the dominant complex conjugated poles as a function of the passive damping network impedances L_d and R_d for a 'Voltage Sensing / Current Actuation' (VSCA) active filter with passive damping.

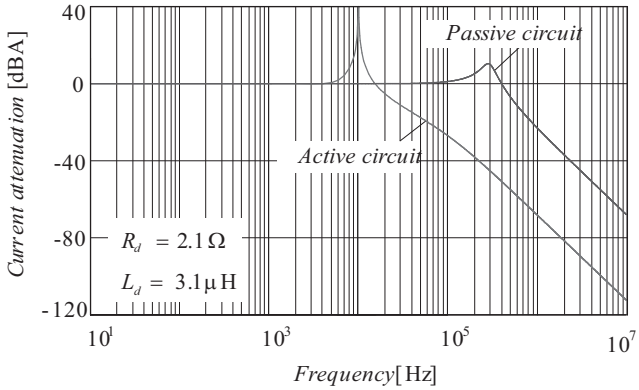


Figure 7.41: Current attenuation curves for $L_d = 3.1$ μH and $R_d = 2.1$ Ω showing a gain of 40 dB for HF from the active to the passive filter for a 'Voltage Sensing / Current Actuation' (VSCA) active filter with passive damping.

impedance in order to achieve a gain of 40 dB in attenuation with active feedback. Values for L_d and R_d inside the stable range are taken in order to plot the attenuation $I_g(s)/I_s(s)$ curves (cf. Figure 7.41), from which it is seen that the active filter achieves an attenuation around 40 dB higher than the passive one for HF.

Voltage Sensing / Current Actuation (VSCA) Filter with Active Damping

As the concept of passively damping the network impedance is impractical, the theoretical use of active damping is analyzed. An active damping loop is added to the circuit by sensing the current through capacitor C_o and feeding it back positively to the amplifier. As a drawback HF current sensing has to be implemented. The circuit of Figure 7.42 shows the basic implementation. With this scheme, however, it is not possible to guarantee to increase the attenuation by 40 dB using the active circuit instead the passive network as there might be a limit as a consequence of the stability analysis. The following assumptions are made:

- The noise source is modeled as a current source i_s.

- The feedback Gsens(s) shall provide more than 40 dB attenuation at 50 Hz. This is achieved with a second order high pass filter.
- The HF gain in attenuation for the active filter must be as large as possible.
- The circuit must be stable.

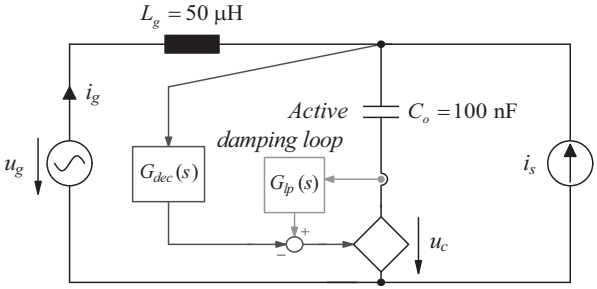


Figure 7.42: Analyzed circuit for a 'Voltage Sensing / Current Actuation' (VSCA) active filter including an active damping loop.

Since a closed-form solution can not be derived due to the large number of variables and the non-trivial form of the involved equations, numerical optimization is utilized. The objective function is the HF gain of the feedback loop and the constraints are the 50 Hz voltage rejection and the stability. This transforms the problem into a non-convex one. To solve the problem the 'Global Optimization Toolbox' of the software 'Maple 10' has been used. The four optimized variables were the corner frequencies and the gains of the feedback transfer functions G_{dec} and G_{lp}, given by:

$$G_{dec}(s) = \frac{57.38s^2}{s^2 + 54143.1s + 1.4364 \cdot 10^9}, \text{ and} \tag{7.23}$$

$$G_{lp}(s) = \frac{176}{5.0686 \cdot 10^9 s + 1}. \tag{7.24}$$

The optimization results have led to the following results. Figure 7.43 shows that the 50 Hz rejection is above the required 40 dB. The position of the closed loop poles in the complex plane (cf. Figure 7.44) demonstrate

that the system is stable. Thus both constraints are fulfilled. Through the attenuation curves (cf. Figure 7.45) it is clear that a gain in attenuation of 40 dB is not achieved. Although there is not 100% certainty that the global optimum was achieved, it is very difficult that a substantially improved solution is possible for these type of structures. Thus, for the specified problem a maximum gain of around 20 dB is to be expected. Another interesting result is the action of the active damping loop, which can be observed in the effect of the feedback loops in the impedance of the parallel circuit branch formed by u_c and C_o (cf. Figure 7.46). The impedance curve shows that a resistive section around 10 kHz is observed, which damps the final closed loop system.

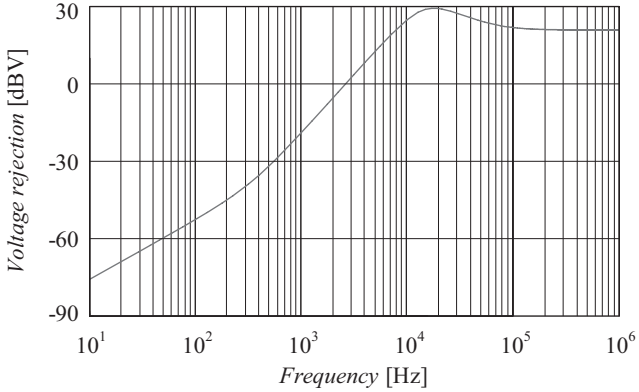


Figure 7.43: Voltage rejection/gain for the amplifier of a 'Voltage Sensing / Current Actuation' (VSCA) active filter including an active damping loop.

Other Active Filter Structures

Based on the procedure and requirements presented in section 7.3.5, similar studies have been performed for the other active filter structures.

The structure of a 'Current Sensing / Voltage Actuation' – CSVA – topology is shown in Figure 7.47. The attenuation curve results for this structure, achieved with numerical optimization are displayed in Figure 7.48.

The structure of a 'Voltage Sensing / Voltage Actuation' – VSVA – topology is shown in Figure 7.49. The attenuation curve results for

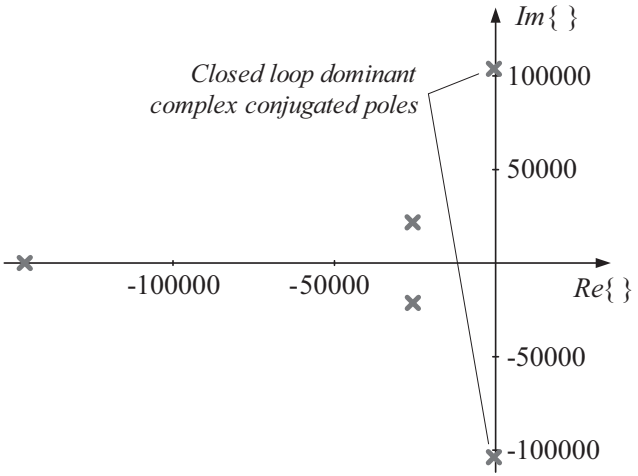


Figure 7.44: Root locus showing the position of the closed loop system poles of a 'Voltage Sensing / Current Actuation' (VSCA) active filter including an active damping loop.

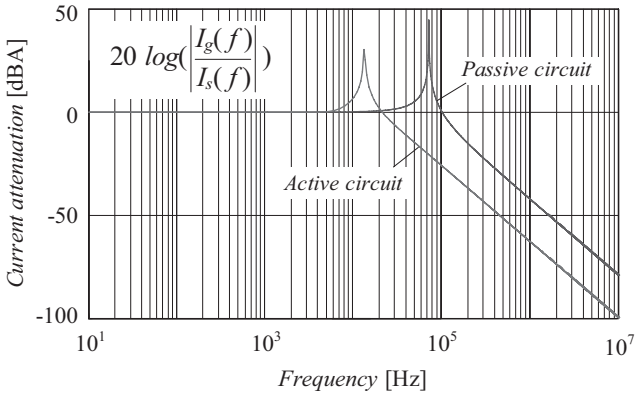


Figure 7.45: Active and passive filter current attenuation curves showing around 20 dB gain in attenuation for HF for a 'Voltage Sensing / Current Actuation' (VSCA) active filter including an active damping loop.

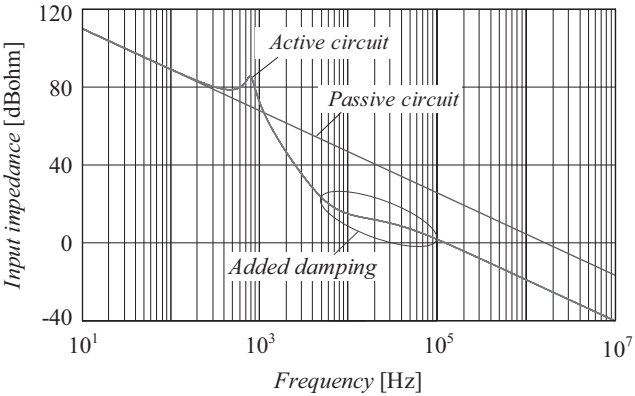


Figure 7.46: Parallel branch (u_c and C_o) impedance magnitude curves for the active and passive circuits for a 'Voltage Sensing / Current Actuation' (VSCA) active filter including an active damping loop.

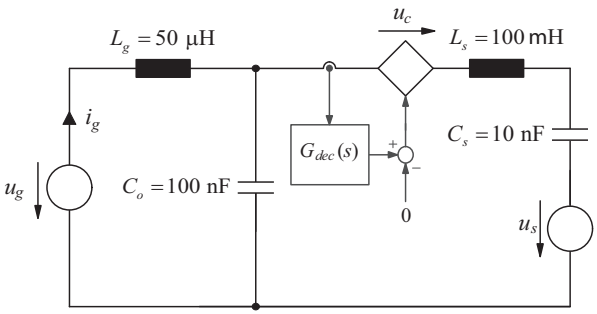


Figure 7.47: 'Current Sensing / Voltage Actuation' CSVA.

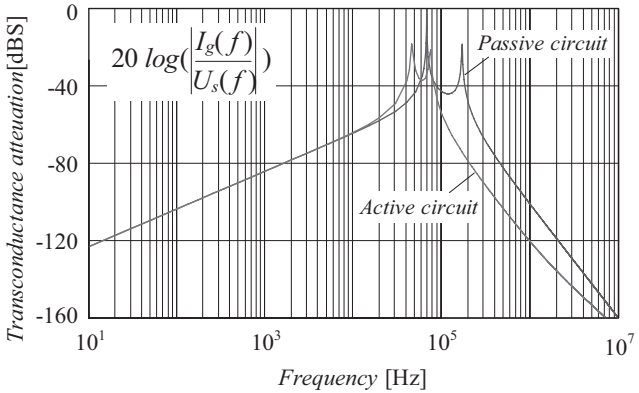


Figure 7.48: Attenuation curves for the filter structures of Figure 7.47 (CSVA) achieved with numerical optimization.

this structure, achieved with numerical optimization are displayed in Figure 7.50.

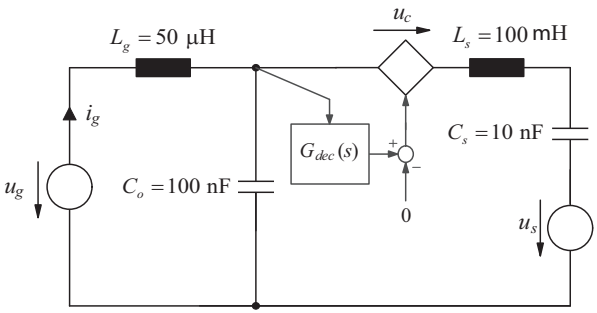


Figure 7.49: 'Voltage Sensing / Voltage Actuation' VSVA.

The structure of a 'Current Sensing / Current Actuation' – VSVA – topology is shown in Figure 7.51. The attenuation curve results for this structure, achieved with numerical optimization are displayed in Figure 7.52.

From the presented attenuation curve results, the gains in attenuation, with the application of feedback, range from 20 to 30 dB. These results

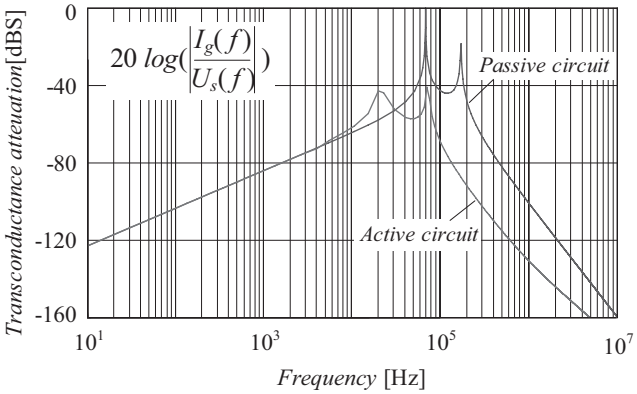


Figure 7.50: Attenuation curves for the filter structures of Figure 7.49 (VSVA) achieved with numerical optimization.

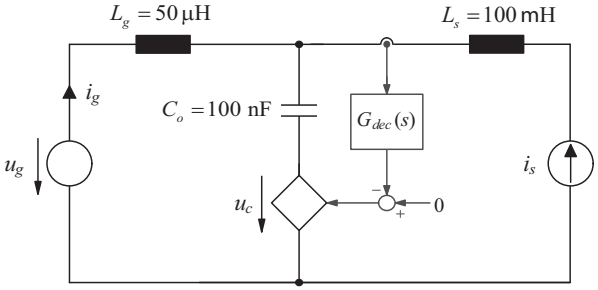


Figure 7.51: 'Current Sensing / Current Actuation' CSCA.

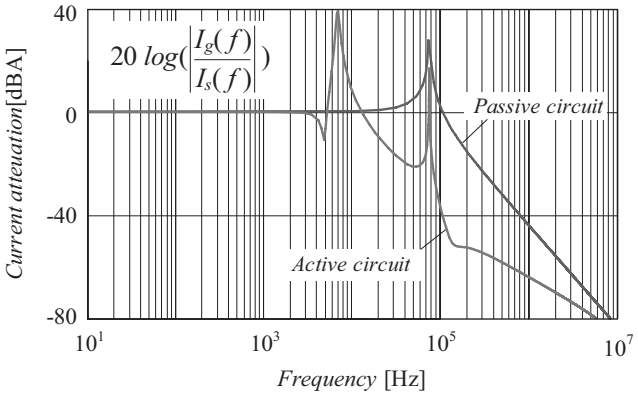


Figure 7.52: Attenuation curves for the filter structures of Figure 7.51 (CSCA) achieved with numerical optimization.

show that high attenuation enhancements are very difficult to achieve with the application of second order high-pass filters in the feedback paths. This type of structure, therefore, imposes limitations for the application of active filters connected directly to the mains. On the hand, applications where the source and load impedances are well defined and/or where such a high attenuation of low frequency components is not required, as dc supplied converters, do not suffer from the same stability restrictions and can, therefore, present more sensible performance improvements.

7.4 Minimum Volume CM Filter for a Three-Level Boost Rectifier

This section is focused in the design of CM filters which are able to fulfill conducted emission regulations and present the highest achievable power density with commercially available magnetic cores and capacitors. The filter design procedure is proposed for a Three-Phase Three-Level Six-Switch Boost PWM Rectifier as depicted in Figure 7.53 [78, 131]. This rectifier has an output power of 10 kW, power density of 8 kW/dm^3, switching frequency f_s = 400 kHz, output voltage U_o = 760 V, input voltage U_{N1} = 230 V and is forced air-cooled. The EMC filter for this

system must be designed to fulfill EMC requirements, where an attenuation specification, based on the estimated CE levels of the rectifier, is calculated. Furthermore, the filters shall be designed taking into account the limits for CE specified for Class B information technology (IT) equipments as in CISPR 22.

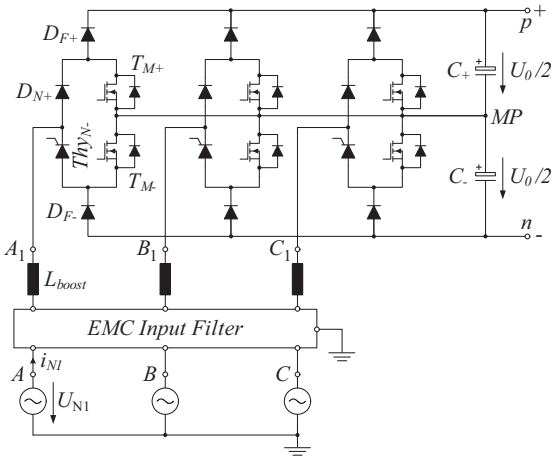


Figure 7.53: Circuit schematic of a Three-phase, Six-switch, Three-level Rectifier topology used to implement a 10 kW PWM rectifier.

7.4.1 CM Filter Topology

The CM filter design is based on the simplified models presented in section 3.4, where equivalent circuits are defined and used to evaluate CM and DM noise sources. The filter topology used for the DM design is shown as a single-phase equivalent in Figure 7.54. Three-stages are chosen based on power levels and attenuation requirements [215]. Components are chosen based on a series of requirements as given in section 4.

The first task in the CM filter design is to choose an appropriate filter topology. These filters are typically built with inductors and capacitors in a low-pass arrangement, which can have many stages and different configurations. Multi-stage filters have the potential to lower the total filter size and costs. Reference [215] defines the conditions and requirements at

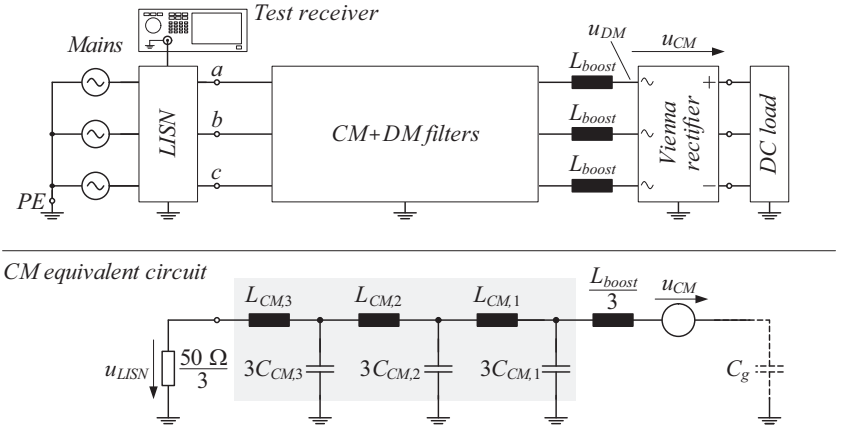


Figure 7.54: Standard test setup for conducted emission and simplified equivalent circuits for differential mode. The CM filter topology is also shown.

which each topology presents an advantage. For the case at hand, a three-stage topology is presented in Figure 7.54 in its single-phase equivalent.

Two main components are used in the CM filter, coupled inductors and capacitors. Equipment safety regulations (cf. section 2) play an important role, since they restrain *(i)* the allowable earth leakage current; *(ii)* define requirements for capacitors between an input line and PE; and, *(iii)* define insulation requirements for CM inductors and filter construction.

Earth leakage current $I_{PE,rms,\max}$ is typically limited to 3.5 mA, even for the case where one of the phases is lost. Thus, the total capacitance $C_{CM,sum} = \sum C_{CM,i}$, i=1...3, between any of the input phases and the PE is bounded to a maximum of approximately,

$$C_{CM,sum} \leqslant \frac{I_{PE,rms,\max}}{1.1 \cdot U_{N1,\max} \cdot 2\pi \cdot 50 \text{ Hz}} \cong 44 \text{ nF}. \tag{7.25}$$

Safety also requires Y2 rated capacitors. Due to these restrictions a series of Y2 ceramic capacitors [160] is chosen, which presents a maximum capacitance of 4.7 nF per SMD package, leading to compact construction and low parasitics. Since other capacitances are present in the circuit (arrestors, stray capacitances, etc.) and values present tolerances, some margin is provided so that $C_{CM,sum} = 7{\cdot}4.7 \text{ nF} = 32.9 \text{ nF}$, is to be divided

to the filter stages. According to section 6.7.1, for maximum attenuation given a minimum total capacitance, each stage shall present the same value.

The other elements of the CM filter are the coupled inductors [178]. A design methodology for the three-phase CM inductors is presented in section 7.4.2. This methodology aims in designing CM inductors with smallest dimensions and is the basis for an effective CM filter design.

7.4.2 Minimum Volume Design of Three-Phase CM Inductors

As seen in section 4.5, high permeability materials can be employed, thus, reducing the volume of the inductors. Typically, high permeability magnetic materials present a highly varying complex permeability with frequency. For this reason common mode inductors must be designed based on their required impedance at a given frequency. The real part of the permeability μ' models the reactive (inductive) impedance transfered from the core to the wires. An imaginary part μ'' models an increase in the total impedance due to core losses, so that the CM choke behaves as a series RL connection. The proper choice of core materials leads to compact and effective inductors, with reduced parasitics. This analysis is performed in section 4.5.2 and from this study, it is observed that CM inductors can be smaller by applying materials with high permeability and saturation point. Aiming for compactness and, given the results of section 4.5.2, VITROPERM 500 F [172, 173] is chosen for the CM inductors. This material presents good thermal stability as well.

The objective of this section is to propose a design procedure that allows for minimum volume CM inductors for a given specification. Therefore, an iterative procedure is presented in the following.

The minimum specifications for a successful CM inductor design are:

- Ambient temperature: T_{amb};
- Maximum temperature: $T_{\max}$;
- Maximum current (DM): $I_{DM,rms}$;
- Frequency of interest: f_{int};

- Desired impedance at f_{int}: Z_{des};
- Switching frequency: f_S;
- Peak current (or voltage) amplitude at f_S: I_s (U_s).

Design Databases

A database containing mechanical and magnetic properties, as specified in Table 7.3, of the commercially available cores for the chosen material must be available. Only toroidal cores are considered here.

Table 7.3: Required specifications for the database of available cores.

Parameter	*Symbol*	*Unit*
Bare outer diameter	OD_{bare}	[m]
Bare inner diameter	ID_{bare}	[m]
Bare height	H_{bare}	[m]
Outer diameter	OD	[m]
Inner diameter	ID	[m]
Core height	H	[m]
Mean magnetic path length	l_e	[m]
Core cross-sectional area	A_e	[m^2]
Thermal resistance	R_{th}	[K/W]
Core inductance per turn square	AL	[H/$turns^2$]

The magnetic material is modeled through approximative expressions which are obtained from curve-fitting manufacturer's information. The expression for the real part of the complex permeability is here approximated as,

$$\mu'(f) = M_1' \frac{\left(\frac{f}{M_2'} + 1\right)^{M_3'}}{\left(\frac{f}{M_4'} + 1\right)^{M_5'}}, \tag{7.26}$$

whereas the imaginary part is modeled as,

$$\mu''(f) = M_1'' \frac{\left(\frac{f}{M_2''} + 1\right)^{M_3''}}{\left(\frac{f}{M_4''} + 1\right)^{M_5''} \cdot \left(\frac{f}{M_6''} + 1\right)^{M_7''}}, \tag{7.27}$$

so that the complex permeability is given by,

$$\mu = \mu'(f) - j\,\mu''(f). \tag{7.28}$$

The coefficients for eq. (7.26) and eq. (7.27) are given in Table 7.4 and Table 7.5, respectively, for some magnetic materials.

Table 7.4: Coefficients for the real part of the complex permeability for different magnetic materials.

Material	M_1'	M_2'	M_3'	M_4'	M_5'
1. Vitroperm	$100 \cdot 10^3$	$1.00 \cdot 10^9$	$2.10 \cdot 10^4$	0.10	0.80
2. Magnaperm	$97.5 \cdot 10^3$	$1.85 \cdot 10^3$	$4.28 \cdot 10^3$	1.22	2.03
3. T38	$10.0 \cdot 10^3$	$1.90 \cdot 10^6$	$3.00 \cdot 10^7$	4.50	90.00
4. N30	$4.20 \cdot 10^3$	$1.16 \cdot 10^5$	$6.98 \cdot 10^6$	0.31	7.79

Table 7.5: Coefficients for the imaginary part of the complex permeability for different magnetic materials.

Mat.	M_1''	M_2''	M_3''	M_4''	M_5''	M_6''	M_7''
1.	405	601	2.92	$7.72 \cdot 10^3$	2.92	$9.32 \cdot 10^2$	0.66
2.	1230	871	1.78	$1.19 \cdot 10^4$	1.22	$1.19 \cdot 10^4$	1.22
3.	21.3	$3.0 \cdot 10^4$	4.65	$1.78 \cdot 10^5$	5.85	$3.09 \cdot 10^5$	0.02
4.	20.0	$3.4 \cdot 10^5$	18.5	$7.40 \cdot 10^5$	26.0	$4.00 \cdot 10^6$	-7.46

Core losses can be modeled with the Steinmetz equation,

$$P_{vol} = K_c\, f^{\alpha}\, B^{\beta}, \tag{7.29}$$

which coefficients are given in Table 7.6 for commercially available core materials for CM inductors.

Table 7.6: Steinmetz parameters for different magnetic materials.

Material	K_c [W/dm^3]	α	β
1. Vitroperm	$8.37 \cdot 10^{-6}$	1.811	2.097
2. Magnaperm	$7.77 \cdot 10^{-6}$	1.750	1.990
3. T38	$1.83 \cdot 10^{-3}$	1.528	2.644
4. N30	$1.02 \cdot 10^{-4}$	1.780	2.434

Operation specific information about the core materials is required for the design. The most relevant parameters are listed in Table 7.7.

Table 7.7: Operating parameters for different magnetic materials.

Material	*Operating temperature* T_{oper}	Saturation flux B_{sat}	Initial permeability μ_{init}
1. Vitroperm	120 °C	1.20 T	$100 \cdot 10^3$
2. Magnaperm	90 °C	0.57 T	$100 \cdot 10^3$
3. T38	100 °C	0.26 T	$10 \cdot 10^3$
4. N30	100 °C	0.24 T	$3 \cdot 10^3$

Finally, a database must be built for the wires with which the inductors shall be wound with. This database can contain available wire diameters with ϕ_{ins} and without insulation ϕ_w. Conventional magnetic copper wire is considered here.

Design Initialization

A first step for the inductor design is to establish an initial maximum current density $J_{\max,0}$ and an initial maximum flux density $B_{\max,0}$. However, these values might strongly vary depending on the involved frequencies and core size. Here, very high values are assumed, so that the maximum flux density is assumed to be the saturation flux,

$$B_{\max,0} = B_{sat}, \tag{7.30}$$

for the chosen core material and the maximum current density is set to,

$$J_{\max,0} = 2 \cdot 10^7 \,\mathrm{A/m^2}. \tag{7.31}$$

Another required information is the insulation distance d_{ins} between each of the three windings. This depends on the employed insulation technology and typically present values in the range,

$$d_{ins} = 0.5\,\mathrm{mm} \ldots 1.5\,\mathrm{mm}. \tag{7.32}$$

With the initial maximum current density, the maximum number of turns $N_{\max,0}$ for each of the available cores can be computed. This leads to,

$$N_{\max,0,j} = \begin{cases} 0.15\,\pi \left[\left(ID_j - \frac{3\,d_{ins}}{\pi} \right) \sqrt{\frac{\pi\, J_{\max,0}}{I_{DM,rms}}} \right], & \text{if } N_{layers} = 1 \\ 0.285\,\pi I D_j^2 \, \frac{J_{\max,0}}{12\, I_{DM,rms}}, & \text{if } N_{layers} > 1 \end{cases} \tag{7.33}$$

where j is the index of the core and N_{layers} is the desirable number of layers. The current density is given in [A/m^2] and the distance d_{ins} is in [m]. The core database must be set in a way that growing impedance can be obtained with growing index j, which is defined in the range,

$$j = 1 \ldots N_{cores}, \tag{7.34}$$

where N_{cores} is the number of available cores.

With this, the maximum obtainable impedance for each of the cores can be calculated with,

$$Z_{\max,0,j} = 2\,\pi\, f\, AL\, N_{\max,0,j}^2 \left| \frac{\mu(f)}{\mu_{init}} \right|. \tag{7.35}$$

The minimum number of turns to keep the flux density below the saturation limit is given by,

$$N_{\min,0,j} = \frac{U_s}{2\,\pi\, f_S\, B_{\max,0}\, A_{e,j}}. \tag{7.36}$$

The next step is to find the smallest core which fulfills, both, desirable

impedance and maximum flux density. This can be accomplished with the algorithm below finding the core in the core database of number $N_{core,0}$.

$$
\begin{aligned}
&N_{core,0} = 0 \\
&j = 1 \\
&\text{while } j \leqslant N_{cores} \text{ do} \\
&\quad N_{core,0} = j \\
&\quad \text{if } (Z_{\max,0,j} \geqslant Z_{des}) \text{ and } (N_{\min,0,j} \leqslant N_{\max,0,j}) \\
&\qquad \text{then } j = N_{cores} + 1 \\
&\qquad \text{else } j = j + 1 \\
&\quad \text{end if} \\
&\text{end do.}
\end{aligned}
\tag{7.37}
$$

With the found core, the necessary number of turns must be found. This should fulfill the impedance and flux density requirements. The wire diameter can be determined with the following algorithm,

$$
\begin{aligned}
&S_{\min} = \frac{I_{DM,rms}}{J_{\max,0}} \\
&\phi_{\min} = \sqrt{\frac{4\,S_{\min}}{\pi}} \\
&j = 1 \\
&\text{while } j \leqslant N_{wires} \text{ do} \\
&\quad N_{wire,0} = j \\
&\quad \text{if } \phi_{\min} \leqslant \phi_{w,j} \\
&\qquad \text{then } j = N_{wires} + 1 \\
&\qquad \text{else } j = j + 1 \\
&\quad \text{end if} \\
&\text{end do,}
\end{aligned}
\tag{7.38}
$$

where $S_{\min}$ is the minimum wire section to fulfill the maximum current density, $\phi_{\min}$ is the corresponding diameter, and N_{wires} is the total number of wires in the database, which must be organized in a way that the smallest wire diameter corresponds to $j = 1$ and the diameter grows with increasing j.

The required number of turns $N_{req,0}$ can be re-calculated based on the chosen core $N_{core,0}$,

$$N_{req,0} = \max\left(\sqrt{\frac{Z_{des}\,\mu_{init}}{2\,\pi\,f_{int}\,AL\,|\mu(f_{int})|}}\;,\;\frac{U_s}{2\,\pi\,f_S\,B_{\max,0}\,A_{e,N_{core,0}}}\right) \tag{7.39}$$

The maximum number of turns can be re-calculated based on the chosen wire $N_{wire,0}$ and core $N_{core,0}$,

$$N_{\max,0,N_{core,0}} = \begin{cases} 0.35\,\frac{ID^2_{N_{core,0}}}{\phi_{ins,N_{wire,0}}}, & \text{if } N_{layers} = 1 \\ \frac{0.9\left(\frac{\pi\,ID_j}{3} - d_{ins}\right)}{\phi_{ins,N_{wire,0}}}, & \text{if } N_{layers} > 1 \end{cases}. \tag{7.40}$$

If the maximum number of turns $N_{\max,0,N_{core,0}}$ for the given core is larger than the required number of turns $N_{req,0}$, then the calculation can proceed. If this condition is not fulfilled, then the next core size should be chosen,

$$N_{core,0} = \begin{cases} N_{core,0}, & \text{if } N_{\max,0,N_{core,0}} \geqslant N_{req,0} \\ N_{core,0} + 1, & \text{if } N_{\max,0,N_{core,0}} < N_{req,0} \end{cases}. \tag{7.41}$$

In order to check if the selected core $N_{core,0}$ is able to fulfill all design requirements, the temperature rise must be computed. For this, the total power losses shall be calculated. This can be accomplished with the procedure explained in section 4.5.2 for the calculation of the equivalent resistances and core losses. The total losses are computed in two parts, the losses in the windings P_w and in the core P_c. The total inductor losses is here named $P_{total,0} = P_{w,0} + P_{c,0}$ and shall be multiplied by the core's thermal resistance in order to find the temperature rise ΔT_0,

$$\Delta T_0 = R_{th,N_{core,0}} \cdot P_{total,0}. \tag{7.42}$$

If the temperature rise is under the maximum given by $T_{\max} - T_{amb}$, then the inductor is designed. Otherwise the following iterative procedure can be implemented in order to find the smallest core size that fulfills the specifications.

Finalizing the CM Inductor Design

The iterative procedure presented in the following is implemented in order to find the smallest core size that fulfills the specifications. It employes the data from the previous section as initialization variables.

$j = 0$
while $\Delta T_j \geqslant (T_{\max} - T_{amb})$ do
  if $P_{w,j} \geqslant P_{c,j}$
    then
      $N_{wire,j+1} = N_{wire,j} + 1$
      $N_{req,j+1} = N_{req,j}$
    else
      $N_{wire,j+1} = N_{wire,j}$
      $N_{req,j+1} = N_{req,j} + 1$
  end if
  if $N_{layers} \neq 1$
    then
      $$N_{\max,j+1} = 0.35 \frac{ID^2_{N_{core,j}}}{3\,\phi^2_{ins,N_{wire,j+1}}}$$
    else
      $$N_{\max,j+1} = \frac{0.9\left(\frac{\pi\, ID_{N_{core,j}}}{3} - d_{ins}\right)}{\phi_{ins,N_{wire,j+1}}}$$
  end if
  if $N_{req,j+1} \leqslant N_{\max,j+1}$
    then

$$
\begin{aligned}
&\text{calculate } P_{w,j+1} \text{ and } P_{c,j+1} \\
&\Delta T_j = R_{th,N_{core,j}} \cdot (P_{w,j+1} + P_{c,j+1}) \\
&\text{else} \\
&N_{core,j+1} = N_{core,j} + 1 \\
&N_{req,j+1} = \max\left(\sqrt{\frac{Z_{des}\,\mu_{init}}{2\,\pi\,f_{int}\,AL\,|\mu(f_{int})|}} \;,\; \frac{U_s}{2\,\pi\,f_S\,B_{\max}\,A_{e,N_{core,j+1}}} \right) \\
&\text{calculate } P_{w,j+1} \text{ and } P_{c,j+1} \\
&\Delta T_{j+1} = R_{th,N_{core,j}} \cdot (P_{w,j+1} + P_{c,j+1}) \\
&\text{end if} \\
&j = j + 1 \\
&\text{end do.}
\end{aligned}
\tag{7.43}
$$

This procedure is employed throughout this work for the design of three-phase CM inductors. The models presented in section 4.5 can be employed to derive equivalent circuits which account for parasitic elements. An experimental verification for this design procedure is performed in the testing of the CM inductors and complete filters in sections 4.5 and 7.4.3.

7.4.3 Experimental Implementation and Results

The rectifiers' construction views are shown in Figure 7.55. The rectifier is designed for compactness. Thus, trade-offs among thermal, electrical, EMC and mechanical functions are required. The filter layout follows design rules to reduce interaction within filter elements and presents a straight line forward current flow. The current flows from the input terminals through the EMC filter, the current sensors and boost inductors, which links it to capacitor board. From this board the current flows through the power module into the output capacitors. In the tested version of this system, the input filter has been placed in a separate printed circuit board in order to reduce the coupling to the power circuits.

The final filter circuit is shown in Figure 7.56, where the DM filter is also integrated in the structure.

Due to thermal and digital processing restrictions, the switching frequency needed to be reduced to $f_s = 200$ kHz. This will be increased

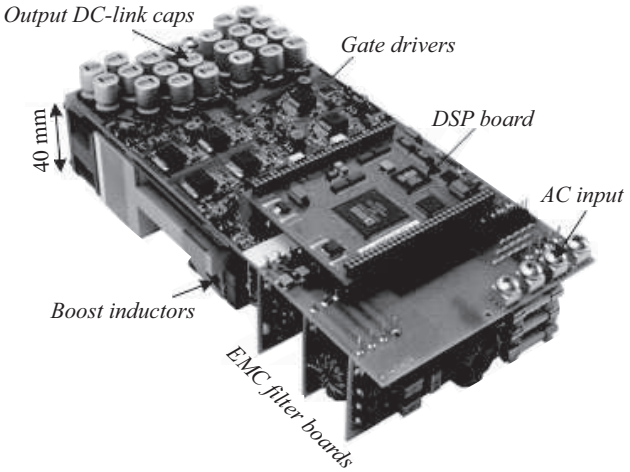


Figure 7.55: Top view on rectifier with the EMC filter DSP board, gate drivers and electrolytic dc output capacitors.

again in a redesign of the system.

From the predicted conducted emission levels computed in section 3.4, the required attenuation for the filtering circuits is,

$$Att_{req,CM,\mathrm{dB}}(f_{int}) = 121 \text{ dB} \ @ \ f_{int} = f_s = 400 \text{ kHz}, \tag{7.44}$$

in order to fulfill CISPR 22 Class B requirements with a 6 dB margin.

The value of the CM inductors among the different filter stages can, in principle, be performed in the same way as the DM inductors (cf. section 6.7.1). That means that equal inductors are to placed in all filter stages so that the total inductance is reduced and attenuation is maximized. Following this procedure leads to three CM inductors of equal value, which impedance at the frequency of interest is required to be

$$Z_{des} \cong 1.38 \text{ k}\Omega \ @ \ f_{int} = 400 \text{ kHz}, \tag{7.45}$$

which value is found through the examination of Figure 7.54. The at-

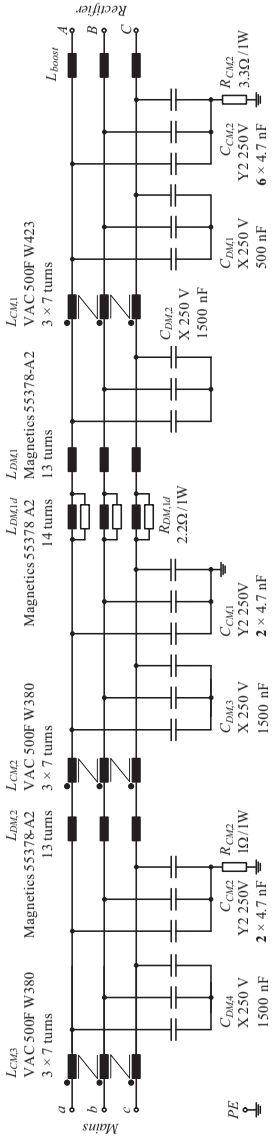


Figure 7.56: Complete circuit schematic for the designed filter with the specifications of the main components.

tenuation equation for this circuit is extremely long and for the sake of clarity it is omitted here. However, it can be numerically solved for finding this required impedance employing equal filter capacitors and assuming a purely resistive impedance for the equal inductors.

The CM inductors have been designed with the inductor design procedure proposed in section 7.4.2, where the voltage ripple at the switching frequency requires that the number of turns is increased in order to limit the flux density. The CM inductor which is at the input of the rectifier $L_{CM,1}$ must withstand a higher CM voltage and for this reason a larger core for this inductor was required. The CM voltage across this inductor can be computed from the equivalent circuit shown in Figure 7.57. The boost inductor typically presents an impedance that is much lower than $L_{CM,1}$ and $L_{CM,1}$ has an impedance which is much higher than the capacitor $3C_{CM,1}$. For these reasons, a simplified expression can be employed, which only takes the capacitances into account, as in,

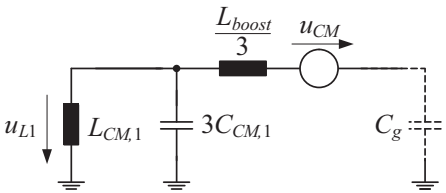


Figure 7.57: Simplified equivalent circuit for the calculation of the CM voltage across $L_{CM,1}$.

$$U_{L1} \cong U_{CM} \frac{C_g}{C_g + 3\,C_{CM,1}}. \tag{7.46}$$

For the case at hand, the peak voltage at the switching frequency is calculated as,

$$U_{CM} \cong 136.6 \text{ V} \ @ \ f_{int} = 400 \text{ kHz}. \tag{7.47}$$

A total capacitance to ground is assumed to be 2 nF as stated in section 3.4. Capacitance $C_{CM,1}$ is taken as one third of the maximum allowable capacitance per phase, so that,

$$C_{CM,1} = \frac{C_{CM,sum}}{3} = 14.6\,\text{nF}. \tag{7.48}$$

Thus, the expected peak CM voltage at the switching frequency is,

$$U_{L1} \cong 5.94\ \text{V} \ @\ f_{int} = 400\ \text{kHz}, \tag{7.49}$$

which is used for computing the flux density at the designed inductor as well as core losses.

Using the calculated required impedance Z_{des} and the peak CM voltage U_{L1}, the design algorithm leads to the inductor specification as shown in Table 7.8.

Table 7.8: Specifications for the CM inductor $L_{CM,1}$.

Parameter	*Value*
Core manufacturer	VAC
Core material	VITROPERM 500 F
Initial permeability	$\cong$ 80000
Core part number	T6000-6-L2020-W423
Core dimensions [mm]	OD: 32.7 / ID: 17.7 / H: 12.5
Magnet wire diameter	2.0 mm
Number of turns	3×8
Number of layers	1
Expected losses	3.1 W
Expected temperature rise	42 °C
Maximum DM current	94.9 A
DC resistance	3.78 mΩ
Parallel capacitance	9.75 pF
Leakage inductance	3.24 μH
Initial inductance	3.66 mH
Impedance @ 400 kHz	1481 Ω

As seen in Table 7.8 the achieved impedance of $L_{CM,1}$ is higher than Z_{des}. With this, the inductance of the other two inductors can be reduced. The CM voltage across these inductors is very low and can be neglected. With this, Table 7.9 shows the design data for $L_{CM,2}$ and $L_{CM,3}$.

Table 7.9: Specifications for the CM inductors $L_{CM,2}$ and $L_{CM,3}$.

Parameter	*Value*
Core manufacturer	VAC
Core material	VITROPERM 500 F
Initial permeability	$\cong 80000$
Core part number	T6000-6-L2025-W380
Core dimensions [mm]	OD: 27.8 / ID: 13.7 / H: 12.7
Magnet wire diameter	1.8 mm
Number of turns	3×7
Number of layers	1
Expected losses	2.8 W
Expected temperature rise	52 °C
Maximum DM current	112.9 A
DC resistance	4.20 mΩ
Parallel capacitance	5.85 pF
Leakage inductance	2.14 μH
Initial inductance	3.09 mH
Impedance @ 400 kHz	1239 Ω

Conducted emissions (QP) measurements, according to CISPR 22 have been performed in order to experimentally verify the design. These measurements are shown in Figure 7.58. A three-phase noise separator as in section 5 has been used to separately quantify DM and CM emissions. Figure 7.58 depicts the measured emission levels for CM and DM. For the DM emissions, the first harmonic is below the designed point (400 kHz) and, thus, it is larger than predicted. These results are obtained in an open system, where no special shield was used. This explains for the worsening of the performance for higher frequencies. Nevertheless, the filter design procedure proves efficient since the components are designed for the range close to the switching frequency.

A comparison of the influence of cabling and grounding configurations in the common mode emissions is presented in Figure 7.59. The CM emissions are shown in Figure 7.59 for two different system configurations. It is seen that, for the same components and boards, the influence of the geometrical configuration of the interconnections and associated loops, is

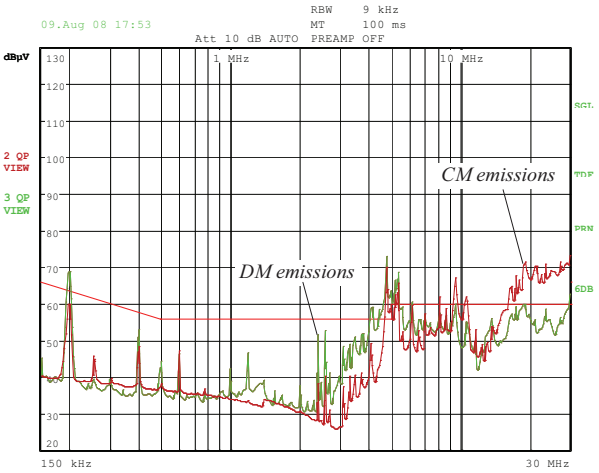


Figure 7.58: Measured CM and DM conducted emissions.

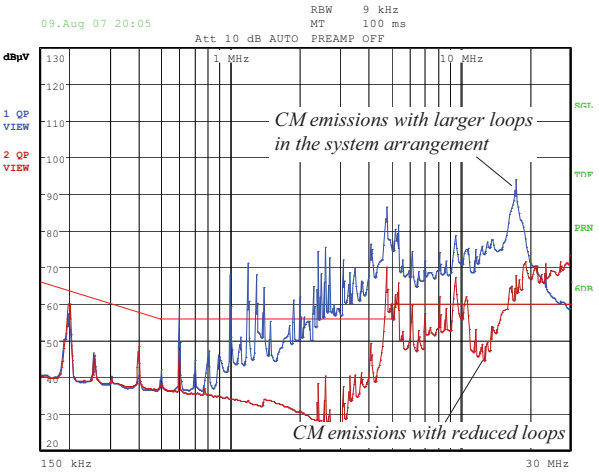


Figure 7.59: Measured CM conducted emissions.

enormous. The difference between the cases, is that the cables interconnecting the power circuit board and the filter board have been shielded and placed very close to the enclosure for the case with smaller loops.

The proposed CM filter design can be easily implemented into an algorithm, where employing modern computational resources the time spent on the design is reduced to minutes or even seconds. A first verification can be done employing detailed models for the components (cf. section 4) in a circuit simulator. Typically, this procedure leads a prototype which is very close to the final design and hardware efforts can be directed to the design of the layout, where considerations on high frequency behavior and thermal management shall be made.

7.5 Summary

The design of a CM filter for a three-phase PWM rectifier is performed based on a CM noise propagation model, which is parameterized by simple impedance measurements on an existing converter prototype. The proposed model, along with a previous CE EMC measurement, allows a sufficiently accurate prediction of the required CM filter attenuation and a straight-forward design, i.e. no complex modeling of the noise paths is required.

A capacitive connection between the star-point of the DM input filter capacitors and the output capacitor has been analyzed and additionally contributes to the attenuation of the CM noise through the modification of the noise propagation. The relevant points for a successful CM filter design have been discussed. For the case at hand, the reduction of the CM emissions from 150 kHz to 600 kHz has been identified as the most relevant range. The selection of the filtering elements is presented and their main characteristics are explained. Measurements on a hardware prototype verify the theoretical considerations and the successful common mode filter design.

This chapter has also proposed an implementation strategy for an HF amplifier based CM active filter for off-line converter systems. For such a system the low frequency (50/60 Hz) attenuation in the feedback loop is of high importance in order to prevent amplifier saturation. However, this limits the filter's operating frequency range.

A literature survey has indicated the possible filter structures, by iden-

tifying the critical issues and main advantages for the selected approach. The designed filter is based on capacitive coupling for both sensing and actuation, eliminating the need for HF transformers. General requirements for a HF power amplifier to be used in active filtering have been derived.

The active filter function has been explained in detail and a stability analysis procedure has been presented which is carried out with reference to root locus diagrams and simplified circuit models. A feedback design for the selected filter topology, which fulfills the stability requirements for the system and is characterized by a higher filter attenuation and/or smaller passive filter components, has been proposed.

The presented simulation and practical results demonstrate that this system has potential for practical use, although limitations in increasing attenuation are shown. Large attenuation for high frequencies is limited due to the highly reactive nature of the filter structure, but the use of a higher bandwidth amplifier would lead to better results. Based on the potential of this technique, other types of feedback structure have been studied in their principles. Due to stability reasons the analyzed structures are characterized by limitations in the gain of attenuation which can be achieved with an active filter having a high-pass filter in its feedback loop.

The last part of this chapter has proposed a design procedure for the EMC filters to be employed with a three-phase rectifier unit in order to fulfill CISPR 22 Class B requirements related to conducted emissions specifically regarding CM. The design procedure has been explained; where a volumetric optimization is carried out taking into consideration different aspects related to the subject, such as electrical safety and an optimized design of the CM inductors. The design of the CM inductors is based on the iterative search for the smallest core which fulfill magnetic flux restrictions, minimum impedance requirement and thermal limitations. Furthermore, the CM inductor design requires for databases with material characteristics, core and wire dimensions. The presented procedure avoids the necessity of using numerical optimization routines and allows for the analytical calculation of the filter components.

Experimental results from conducted emission measurements validate the proposed design procedure. However, the influence of the geometrical configuration of the interconnections and associated loops, is clearly seen at high frequencies. These effects can not be accounted for before hand in the proposed modeling, since they depend upon the 3-D geometry HF effects. This shall be the aim of future research, where parasitic modeling

with field solvers are to be used in the design phase of a power converter system.

Chapter 8

Coupling Issues in the Arrangement of Filter Components

"It's easy to cry 'bug' when the truth is that you've got a complex system and sometimes it takes a while to get all the components to co-exist peacefully." Doug Vargas

8.1 Introduction

Magnetic and electric fields coupling throughout the different parts of a Power Electronics system are able to generate effects that are unwanted, unpredicted and difficult to model. Such effects take place, not only between the power/switched circuits and the input filter, but between components and interconnections/cables as well. These fields are described by Maxwell equations, being highly complex solutions of the involved currents/voltages amplitudes, frequency, materials and geometries. Since simple models to describe the complex behavior of the magnetic and electric fields are typically not successful in accurately predicting conducted emission levels, this chapter does not intend to predict these levels. The main objective is to present basic models that explain the coupling mechanisms and their effects on the performance of three-phase EMC filters.

This is achieved through a basic review of the describing equations and a report of theoretical and experimental results that illustrate the effects of couplings.

A brief literature review is presented, based on reported research of single-phase filters. Literature on the couplings subject applied to three-phase filters is lacking. Thus, coupling issues that are particular to three-phase filters are studied and measures to hinder coupling effects are presented. Furthermore, the optimum arrangement for DM capacitors employed in three-phase filters is proposed.

Conventional three-phase common mode inductors have leakage, thus external, fields that propagate in all directions, thus the placement of such components is extremely important and difficult in a filter where space is restringed. The coupling mechanisms are reviewed here and practical measures to reduce the external field of three-phase CM inductors are proposed through the employment of special winding configurations.

Experimental case studies that provide insight into the effects of couplings in a complete Power Electronics system are reported. The system is composed of an Indirect Matrix Converter and different filter boards. Coupling reduction techniques are employed in such filters, so that their effects are studied. The effects of power connecting interfaces, such as the interface between the power converter and the filter board, are shown. Conclusions are made leading to important guidelines for the physical layout and arrangement of three-phase EMC filters.

8.2 Capacitive Coupling

As written in the introduction, two types of coupling exist, namely: capacitive, i.e. due to electric fields, and inductive, which is due to the magnetic fields. These effects are described by different equations. Capacitive couplings can be understood and modeled with Maxwell's first equation (integral form of Gauss's law),

$$\oint_{S(V)} \vec{E}\, d\vec{A} = \frac{Q_{enclosed}}{\epsilon}, \tag{8.1}$$

where $\vec{E}$ is the electric field vector, $d\vec{A}$ is an infinitesimal area of the surface $S(V)$ enclosing the volume V around a charge $Q_{enclosed}$ and ϵ

is the permittivity of the material. Applying this equation to solve for static electric fields allows for the calculation of capacitances between conductors. Which is the ratio between the charge q and the potential difference U between the conductors ($q = C\,U$).

Therefore, solving the Maxwell's first equation for all involved conductors and applying superposition would lead to the solution for the capacitive coupling problem. On the other hand, the geometries and materials in a power converter complicate this task enormously. In this way, only very simple geometries have an analytical solution and all others need to be solved with field solvers or direct impedance measurements.

Two capacitance concepts take different contributions into consideration, the mutual- and the self-capacitances. Mutual-capacitance is defined in a way that it is the capacitance from one conductor to another, thus, neglecting other capacitances. In this way, the mutual-capacitance C_M per unit length between two parallel conductors of radius r and separation distance d is given by [254],

$$C_M = \frac{\pi\,\epsilon}{\ln\left(\frac{d}{r}\right)}. \tag{8.2}$$

for $d << r$.

The mutual-capacitance for two parallel plates is [161],

$$C_M = \frac{\epsilon\,A}{d}, \tag{8.3}$$

where A is the total area between two layers and d is the width of the insulation layer.

For two concentric hollow conductive spheres of radii r_1 and r_2 and $r_2 > r_1$, the mutual-capacitance can be calculated as [255],

$$C_M = \frac{4\pi\epsilon}{\left(\frac{1}{r_1} - \frac{1}{r_2}\right)}. \tag{8.4}$$

It is seen in all previous expressions that the capacitance increases with the surface of the elements and decreases with the distance between them. This leads to the principle that providing large separation between two conductors reduces the capacitance and, thus, decreases the electric field coupling. This notion is truth, but has a limitation posed by the

concept of self-capacitance. This concept can be introduced by examining the mutual-capacitance between two concentric spheres in eq. (8.4) and increasing the radius of the second sphere to infinity,

$$C_S = \lim_{r_2 \to \infty} C_M = 4\pi\epsilon r_1, \tag{8.5}$$

so that the capacitance from the surface under consideration to an sphere of infinity radius is calculated. This is the self-capacitance of the inner sphere. This notion can be extended to any geometry.

The self-capacitance should be included in the circuit network so that the minimum capacitance C_{min} between two elements of self-capacitance $C_{S,1}$ and $C_{S,2}$ is,

$$C_{min} = \frac{C_{S,1}\, C_{S,2}}{C_{S,1} + C_{S,2}}, \tag{8.6}$$

and the complete capacitance network is shown in Figure 8.1.

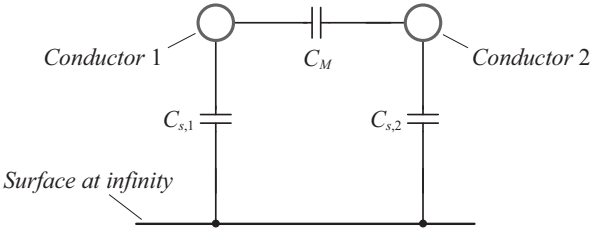


Figure 8.1: Mutual-capacitance C_M and self-capacitances $C_{s,1}$, $C_{s,2}$.

This shows that if a calculated mutual-capacitance is very low, the total capacitance might be influenced by the self-capacitance. Besides that, other conductive surfaces are typically close to the conductors and influence the final capacitance in the same way as the self-capacitance.

8.2.1 Capacitive Coupling of Noisy Signals

The mechanism of capacitively coupling noise is the same as for capacitive crosstalk analysis and can be understood by examining Figure 8.2, where u_s is the wanted or predicted voltage, Z_s is the Thevénin equivalent of the

source impedance, Z_l is the load impedance, u_n is a noise voltage which is capacitively coupled to the circuit through a stray capacitance C_n.

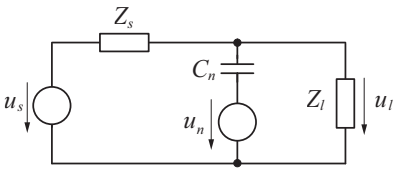


Figure 8.2: Capacitive noise coupling.

By superposition, the final voltage u_l is given by,

$$U_l(s) = U_s(s) \cdot \frac{1}{\frac{Z_s}{Z_l} + 1} + \underbrace{U_n(s) \cdot \frac{1}{\frac{1}{s\,C_n} \cdot \frac{Z_s + Z_l}{Z_s\,Z_l} + 1}}_{\text{Coupled noise}}. \tag{8.7}$$

In eq. (8.7) it is seen that the capacitively coupled noise depends on the capacitance value and on the reciprocal of the parallel impedance of the main circuit. If the parallel impedance of the main loop is small, the voltage portion due to noise is decreased and this is typically the case for power filters, where the impedance Z_l represents in most case a capacitor with low impedance for high frequencies. For this reason, capacitive coupling is typically not the most important effect in power converters.

For the case of EMC filters for PWM converters, the noise voltage is typically the same as u_s and the capacitive noise coupling is in parallel with Z_s. That is the configuration of inductors and their parasitic capacitances. Therefore, the parasitic parallel capacitance cancellation techniques presented in section 4.4.3 can be used to diminish the capacitive coupling. Capacitive coupling to other parts of the system can be reduced through shielding. Nevertheless, shielding with conductive materials of low permeability ($\mu_r \approx 1$) has limited effect against magnetic coupling.

8.3 Inductive Coupling

The other three Maxwell's equations model the behavior, effects and the generation mechanisms of magnetic fields. The peculiarity of the magnetic field is that it has no beginning or end point, meaning that it shows closed lines. Therefore, any closed circuit path is influenced by currents circulating in other conductors. Galvanic insulation, thus, does not impede interference due to magnetic fields. Maxwell's second equation explains this effect,

$$\oint_{S(V)} \vec{B}\, d\vec{A} = 0, \tag{8.8}$$

where $\vec{B}$ is the magnetic flux density vector. This equation clarifies that the total flux through the surface $d\vec{A}$ is null, thus the field lines heading inwards a volume enclosed by the surface $S(V)$ is equal to the field lines leaving this surface and the magnetic field is continuous.

Maxwell's fourth equation, describes that a magnetic field $\vec{B}$ is created by two types of currents,

$$\oint_{L(S)} \vec{B}\, d\vec{l} = \mu\, I + \epsilon\, \mu\, \frac{\partial E}{dt}. \tag{8.9}$$

The first term $\mu\, I$ is the conduction current crossing section S and the second term is the displacement current generated by the time variation of an electrical field $\vec{E}$ in the medium. Thus, any current or varying electric field generates a magnetic field.

On the other hand, time varying magnetic fields induces an electric field. This is stated in Maxwell's third equation,

$$\oint_{L(S)} \vec{E}\, d\vec{l} = -\frac{\partial \Phi}{dt}, \tag{8.10}$$

where Φ is the magnetic flux enclosed by the surface S encircled by a line $L(S)$. This equation states that the voltage induced in a closed conductive path due to the varying magnetic field is such, that the direction of the generated current creates a field in opposite direction to the original one.

From these three equations, it is clear that currents and voltages with time variation create magnetic fields that induce voltages in circuit paths.

The induced voltages depend on the enclosed surface, the magnitude of varying currents and voltages, the involved frequencies, geometries and distances. The principles of magnetic coupling are explained with these equations and the measures to reduce it can be derived.

From an electric circuits perspective, the magnetic coupling effects predicted by Maxwell's equations are modeled as *mutual inductances* M. The circuit shown in Figure 8.3 illustrates the interference from a noise source loop (i_s, L_s) in the receiver/victim loop. The voltages across the inductors are,

$$u_{Lr} = L_r \frac{di_r}{dt} + M \frac{di_s}{dt} \tag{8.11}$$

$$u_{Ls} = M \frac{di_r}{dt} + L_s \frac{di_s}{dt}. \tag{8.12}$$

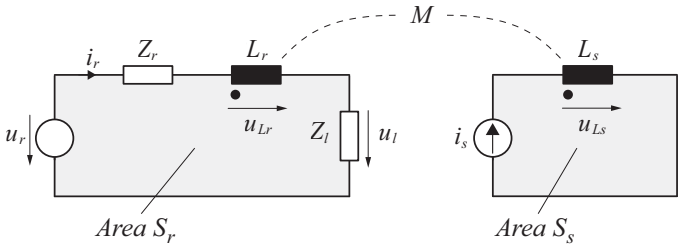


Figure 8.3: Magnetic coupling between two loops.

Applying the Laplace transform to the circuits of Figure 8.3, the load voltage is given by,

$$U_l(s) = U_r(s) \cdot \frac{Z_l}{Z_l + Z_r + s\,L_r} - I_s(s) \cdot \frac{s\,M\,Z_l}{Z_l + Z_r + s\,L_r}. \tag{8.13}$$

This equation models crosstalk between the two loops and is used for signal integrity analysis. It is observed that the load voltage depends on the source current I_s of the second loop even been both loops insulated from each other. The interference from the second loop in the load voltage depends in the relation between the mutual inductance and the series

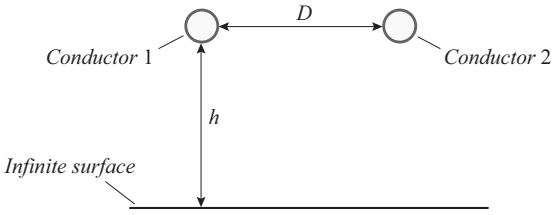


Figure 8.4: Arrangement of parallel conductors of infinite length over an infinite plane.

connection of the impedances in the receiver/victim loop. That means that the influence of magnetic couplings in filtering circuits is larger for loops with low series loop impedance. From this three measures can be taken to reduce coupling, namelly: (*i*) reduce the mutual inductance; (*ii*) reduce the source current I_s, and; (*iii*) increase the receiver/victim series loop impedance.

The mutual inductance can be generally calculated with,

$$M = \frac{1}{I_s} \int_{S_r} \vec{B}_s \, d\vec{s} = \frac{1}{I_s} \int_{S_r} \mu \vec{H}_s \, d\vec{s}, \tag{8.14}$$

where $\vec{H}_s$ is the magnetic field created by the source circuit current I_s which crosses the receiver circuit loop area S_r. The term I_s shall also appear in the magnetic field expression $\vec{H}_s$, so that the mutual inductance is only dependent on the geometric properties of both loops. Although this equation is generally valid, the analytical calculation of the mutual inductances for complex geometries and various materials is extremely difficult and field solvers or experimental measurements are applied in practice. From eq. (8.14) it is seen that the mutual inductance can be reduced by reducing the source generated magnetic field or the area which encloses the field in the receiver circuit. As the vector product $\vec{H}_s \, d\vec{s}$ depends on the direction of the involved vectors, having perpendicular vectors leads to zero mutual coupling. For circuits where the geometric placement of source and receiver circuits allows it, this is a very practical way to reduce the magnetic coupling.

Increasing the distance between the circuits is another way to reduce the magnetic field enclosed by the receiver circuit. As an example, the

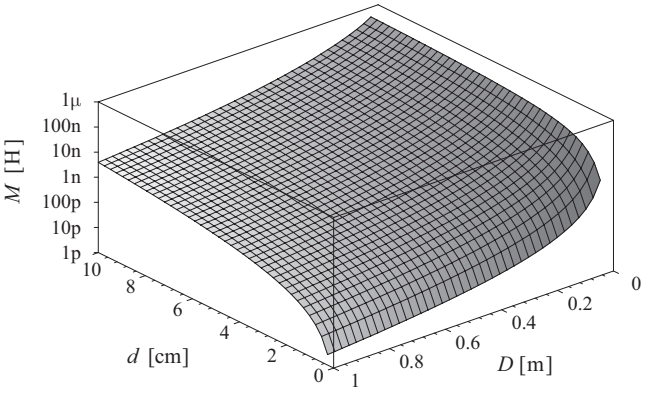


Figure 8.5: Calculation of the mutual inductance according to eq. (8.15).

configuration of Figure 8.4 presents two infinite length conductors placed at a distance d from a conductive infinite plane and apart D from each other. The return current path is through the infinite surface plane. The mutual inductance per unit length between these conductors is given by [254],

$$M = 1 \cdot 10^{-7} \cdot \ln\left(1 + \frac{4\,h^2}{D^2}\right) \tag{8.15}$$

The mutual inductance predicted in eq. (8.15) is plotted in Figure 8.5. It is seen that if the distance d, which is proportional to the loops area, is reduced, then the mutual inductance is reduced. The other way around happens for the distance between the conductors. These effects are more effective for small loop areas and this explains why loop areas in the filtering circuits shall be effectively minimized.

Other ways of reducing magnetic coupling are (*i*) the induction of eddy currents which generate fields opposed to the interfering fields, and (*ii*) deviate the otherwise enclosed field through high permeability materials. Both these measures require structures of conductive and/or high permeability materials to shield the receiver/victim circuits, being typically expensive solutions for the EMC filtering of PWM converters. Nevertheless, these are effective measures and are applied in commercially available electronic products.

8.3.1 The Effects of Magnetic Couplings Between Filter Components

The mutual inductances between filter components model the respective magnetic couplings. In a low-pass EMC filter, the inductors in the series branches can be as large as possible, while shunt branches shall present low impedances for high frequencies, employing capacitors. Thus, inductances in the parallel branches are highly unwanted. Negative inductances are high impedances for high frequencies as well, and are not desired in parallel branches either. The basic configurations shown in Figure 8.6 provide powerful tools to analyze the effects of magnetic couplings. These configurations show that, independent from the coupling direction, coupling between two series branches or between one series branch and a parallel branch result in an inductance in the parallel branch. Therefore, coupling among filter components and/or interconnecting tracks are not desired. An exception is done in some of the parasitics cancellation techniques.

A general case presents three coupled inductors. Assuming positive and negative couplings translated into positive and negative mutual inductances, the circuit of Figure 8.7 present the equivalent non-coupled network. Comparing Figure 8.7 with Figure 8.6 it is clear that the effects of the different couplings is superposed in the general network. Thus, every single magnetic coupling in a filter must be minimized. If parasitic cancellation techniques are to be employed, it is not sufficient to concentrate on each component alone, but the complete filter configuration must be considered. Of course, improvement can be achieved nevertheless, but the optimum cancellation can only be reached when all mutual couplings are considered.

A "T"-type of arrangement is found in any low-pass EMC filter, for instance as in the configuration presented in Figure 8.8. Inductors L_1 and L_2 might represent built inductors or the inductances of the interconnections. These inductors present leakage flux that magnetically couple inductors and the series equivalent inductance ESL of the parallel capacitor C_p as shown in right side of Figure 8.9. Parasitic capacitances $C_{\sigma 1}$ and $C_{\sigma 2}$ in parallel with the inductors also decrease the filtering performance for high frequencies. Examining the circuit of Figure 8.9 it is seen that the effect of the couplings in the performance of this filtering stage effectively is an increase in the ESL and an alteration in the values of inductors L_1 and L_2. If inductors L_1 and L_2 are discrete components,

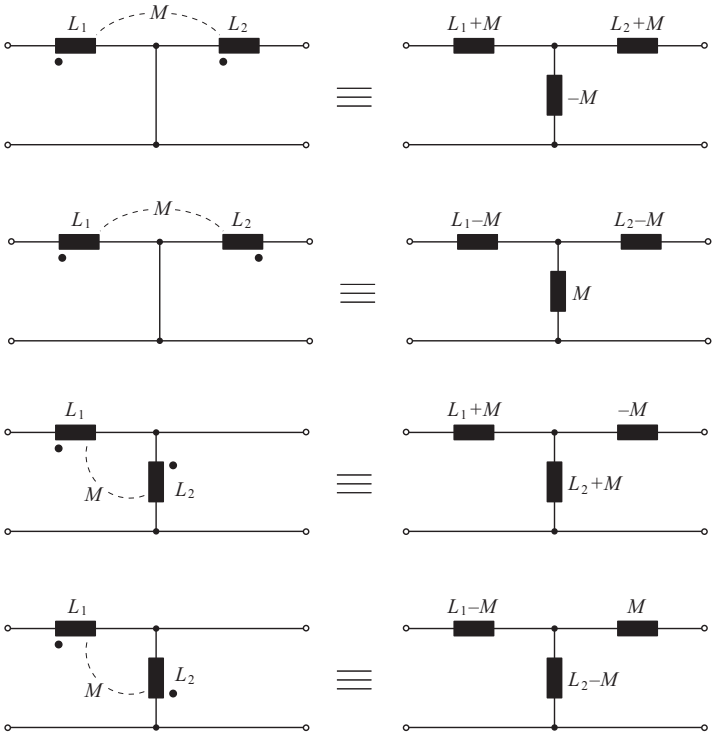


Figure 8.6: Two-port equivalent networks with two coupled inductors.

rather than PCB traces, the value of couplings M_1, M_2 and M_3 might be much larger than the original ESL [155,167].

As seen in Figure 8.9, the final values of the inductances strongly de-

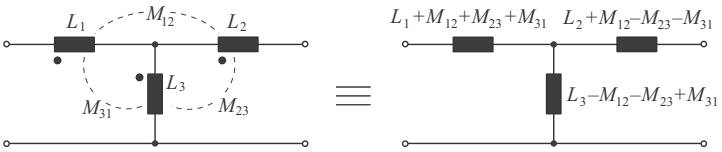


Figure 8.7: Two port equivalent networks with three coupled inductors.

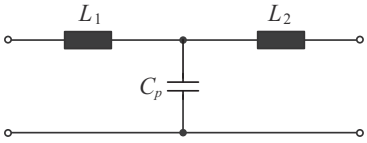


Figure 8.8: Passive "T"-network employed in low-pass EMC filtering.

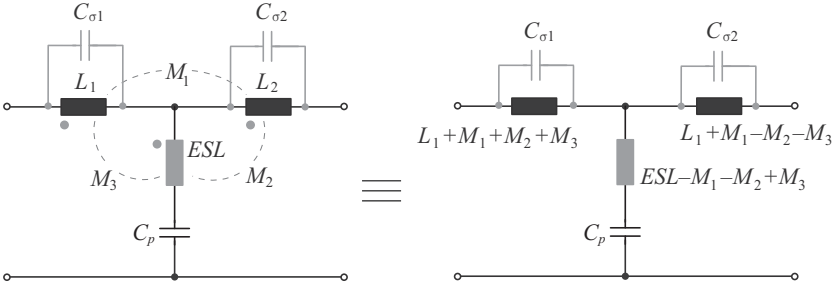


Figure 8.9: Equivalent circuits for the network of Figure 8.8 showing the reactive parasitic elements that affect filtering performance at high frequencies.

pend on all mutual inductances and their polarities. Significant couplings occur between capacitors of different filter stages as shown in the π-type filtering network of Figure 8.10. For this configuration, the values for the equivalent non-coupled inductors are given by,

$$ESL_{11} = \frac{ESL_1\, ESL_2 - M^2}{ESL_2 - M} \tag{8.16}$$

$$ESL_{22} = \frac{ESL_1\, ESL_2 - M^2}{ESL_1 - M} \tag{8.17}$$

$$L_{11} = \frac{L_1 \cdot (ESL_1\, ESL_2 - M^2)}{M\, L_1 + ESL_1\, ESL_2 - M^2}. \tag{8.18}$$

The analysis of eq. (8.16) and eq. (8.17) shows that depending of the mutual inductance the one of the equivalent series equivalent inductances might increase (unwanted effect) or decrease (wanted effect) while the opposite effect takes place in the other shunt branch's ESL. However, the

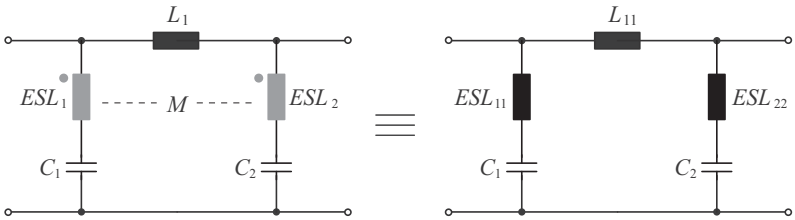


Figure 8.10: Magnetic coupling between capacitors of different filter stages.

most harmful effect occurs on the series inductance L_{11}, where the value of inductor L_1 is strongly decreased for high coupling factors. For a coupling factor equal to 1, inductor L_{11} is null. Thus, the magnetic coupling between capacitors of different filter stages worsens filtering performance.

Other magnetic couplings of interest are the ones between inductors and PCB planes, which might reduce the effective value of DM inductors because of eddy currents induced in the planes that reduce the net magnetic field of the arrangement. Although this effect might be negligible in most applications, the placement of inductors very close to PE planes increases the parasitic capacitance of the DM inductors. Summing all these effects might significantly reduce filtering performance.

Studies about the couplings in single-phase filters are presented in [127, 155, 167, 256, 257], from where the main recommendations are:

i. employ CM inductors placed with the windings turned 90° with respect to the capacitors, so that coupling is minimized with the capacitor and with the PCB traces;

ii. increase the separation between inductors and capacitors;

iii. shield the capacitors and the shields away from inductors and other shields;

iv. increase the distance between capacitors;

v. reduce the length of the pins of capacitors;

vi. reduce the loop area of interconnections;

vii. do not use ground plane under inductors;

viii. increase distances from inductor leads to ground plane;

ix. place inductors perpendicular to each other.

x. consider winding directions to achieve desired positive or negative coupling;

xi. place capacitors perpendicular to each other;

xii. consider careful layout so that coupling polarities compensate each other;

For three-phase filters, some fundamental differences are observed when compared to single-phase filters, namely: (*i*) the CM inductors are comprised of three windings, so that conventionally wound CM inductors have leakage fluxes that spread in all directions; (*ii*) the capacitors are placed in groups of three, one connected to each phase or between phases; (*iii*) the number of components and couplings is much higher and, thus, more difficult to model and reduce; and, (*iv*) there can be more differences in components, which produce asymmetries that generate noise mode conversions. Besides the listed differences, direct couplings from the PWM converter power circuits and the filter and supply cable are to be considered [258].

8.3.2 Coupling of Capacitors in a Filter Stage

In a three-phase EMC filter, capacitors are typically connected as shown in Figure 8.11.

Considering a DM current that flows from phase A and returns by phases B and C, the equivalent circuit of Figure 8.12 is derived.

Assuming that the capacitors have the same value ($C_1 = C_2 = C_3 = C$) and the equivalent series inductances as well ($ESL_1 = ESL_2 = ESL_3 = ESL$), the DM impedance for this equivalent circuit is given as,

$$Z_{dm} = \frac{s^4\,C^2\left[3ESL^2 - 2ESL(M_1+M_2+M_3) + M_1^2+M_2^2+M_3^2+2(M_1M_2+M_2M_3+M_3M_1)\right]}{2sC\left[s^2C(L-M_2+1)\right]} + \\ + \frac{2s^2C(3ESL+M_1+M_2+M_3)+3}{2sC\left[s^2C(L-M_2+1)\right]}. \tag{8.19}$$

If the layout of the capacitors is completely symmetric, then eq. (8.19) simplifies to,

$$Z_{dm}|_{\text{symmetric construction}} = \frac{3}{2sC} + \frac{3}{2}s\,ESL - \frac{3}{2}s\,M, \tag{8.20}$$

and it is clear that the original ESL of the capacitors is reduced. This reduction depends on the amount of coupling. For a coupling factor $k = 1$ the mutual inductances equal the ESL values and a perfect cancellation occurs. Of course, this is only a theoretical case. Improvement is achieved

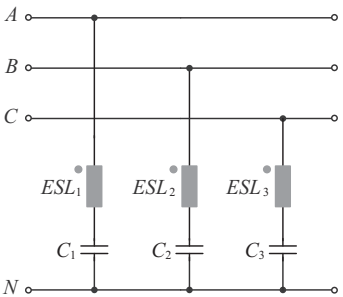


Figure 8.11: Connection of capacitors in a three-phase filter.

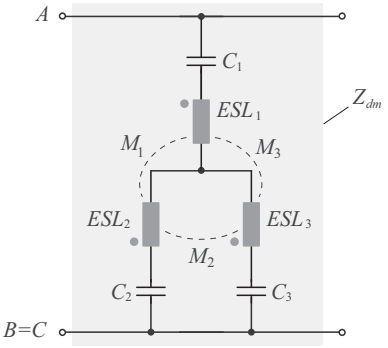


Figure 8.12: Differential mode equivalent circuit for the capacitors connected in "Y" configuration.

for the coupling polarities shown in Figure 8.11. Therefore a symmetrical construction, resulting in the correct coupling polarities is capable of improving the performance of DM capacitors. If one or more of the polarities are inverted, worsening performance occurs.

A general analysis can be made employing the networks shown in Figure 8.13. Assuming all self-inductances and mutual inductances equal, it is observed that the total inductance in each branch is lower than the original inductors without coupling. If perfect coupling applies, the total inductances are null.

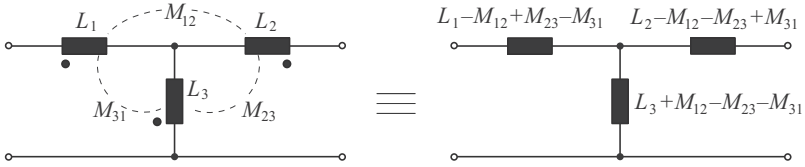


Figure 8.13: Equivalent networks with coupled inductors.

In practical cases, the capacitors can be placed in the same direction and very close together, so that coupling is increased. If the arrangement of Figure 8.14 is applied, coupling between C_1 and C_3 is smaller than the other two couplings. For this case, the DM impedance is not as improved, but it is still better than opposite polarities. The conversion from DM to CM is also an issue in non-symmetrical configurations.

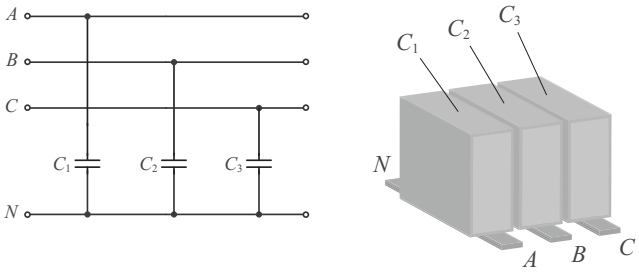


Figure 8.14: Connection and physical layout of capacitors in a three-phase filter.

8.4 Reduction of External Fields for Filtering Inductors

As seen in the previous sections, the magnetic coupling between inductors and capacitors is not desirable in filtering applications. Thus, inductive couplings must be minimized. Regarding the inductors, the external magnetic field (leakage flux) is responsible for inducing currents in other loops. Employing toroidal cores helps minimizing these external fields, but does not completely eliminate them. Different winding strategies lead to different external field configurations. For instance, if the turns of an inductor are concentrated in one region of a toroidal core, leakage flux tends to be much larger than if the turns are equally spaced and cover most of the toroid's surface.

A differential mode inductor, typically employs the winding strategy shown in Figure 8.15. It is a straightforward construction and possibly the most effective way of mechanically wind a toroid and, thus, the less costly way. Unfortunately, this construction presents a large loop area as shaded in the right side of Figure 8.15. This large area can enclose a large flux linkage and consequently present a large magnetic coupling with other components/loops.

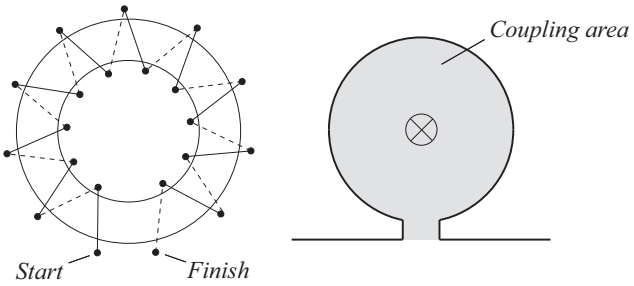


Figure 8.15: Differential mode inductor with conventional winding.

An alternative to the conventional winding strategy for DM inductors has been presented in [259]. It is described in Figure 8.16, where it is seen that, considering an uniform magnetic field with field lines that are perpendicular to the shaded surface, currents are to be induced in each half of the inductor in a way that they cancel each other. Conversely, currents

flowing in the inductor generate magnetic fields that are compensated. Thus, this winding strategy proves to be an excellent alternative to reduce the external field of DM inductors, while the winding effort and the parasitic capacitance are not significantly increased. Thermal performance is also not affected with type of windings.

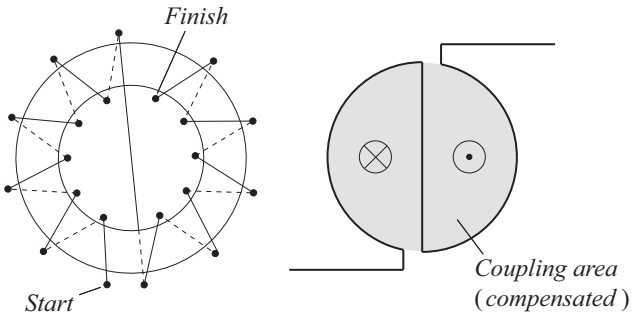


Figure 8.16: Differential mode inductor with improved winding [259].

Another winding strategy that reduces coupling to external components/loops is the reversed winding, which is used in high frequency magnetic components for communications. This strategy is shown in Figure 8.17, from where it is seen that the coupling area can be reduced. The effort in this type of winding is higher than in the other two strategies, but the main drawback of this technique is that the parasitic parallel capacitance is much increased like in a two layers wound inductor.

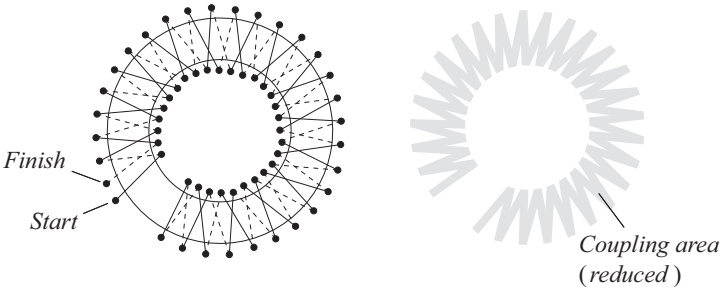


Figure 8.17: Differential mode inductor with reversed winding.

As DM inductors employed in three-phase filters are built of single inductors, no difference in winding strategy needs to be considered. Nevertheless, the placement of DM inductors in a PCB must aim for reducing coupling between the inductors. It is suggested that the inductors are placed perpendicularly and not close to each other.

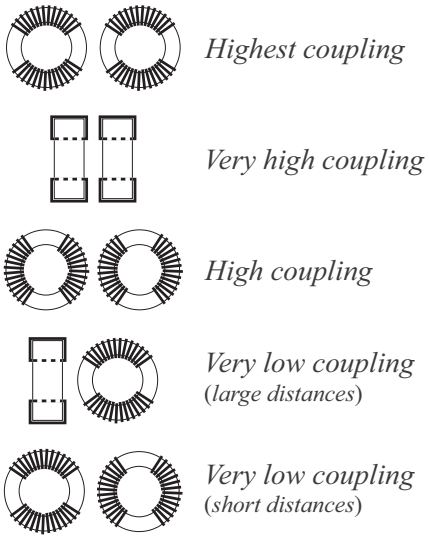


Figure 8.18: Arrangements of common mode inductors in order to reduce magnetic coupling as in [257].

Regarding common mode inductors, studies have been carried out [155,167,257] which suggest arrangements with low coupling. These studies are done for single-phase CM inductors and the results are summarized in Figure 8.18, from where it is seen that perpendicular arrangements present better performance.

The problem in three-phase CM inductors is that there are three windings in a single core and perpendicular arrangements are not possible. A conventionally wound three-phase CM inductor is depicted in Figure 8.19.

The magnetic field due to CM currents is very well contained in the toroidal core as shown with the simulation result in Figure 8.20. The norm of the magnetic field, is shown with detail in this 2-D finite element simulation for a common mode current $I_{cm} = 1$ A. Ideally, no external

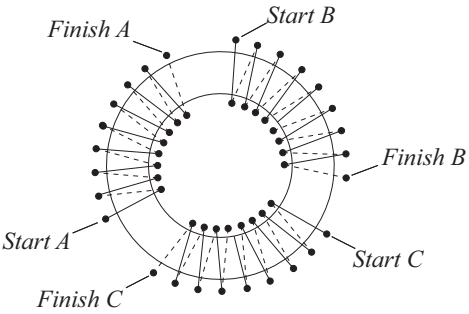


Figure 8.19: Three-phase common mode inductor with conventional windings.

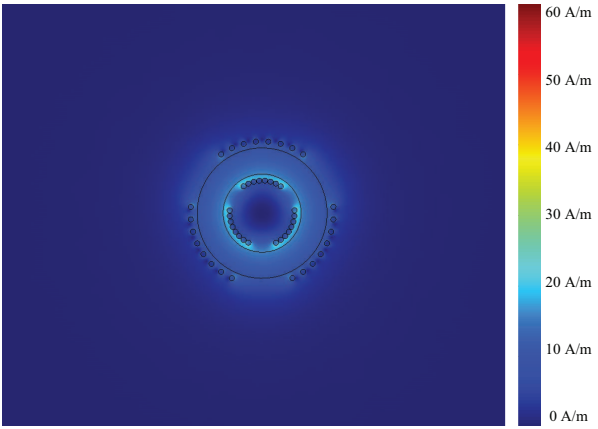


Figure 8.20: Finite elements simulation result for a three-phase CM inductor conducting three symmetrical currents. The simulation result shows the norm of the magnetic field due to three currents of equal phase and amplitude ($\cong$ 1 A) produced in the shown windings.

flux is expected to be radiated from CM currents in a CM inductor built in this way as long as the geometric symmetry of the component is preserved. The core dimensions for this simulation are OD = 25 mm and ID = 15 mm; the wires are of diameter $\phi = 1$ mm and are distant 0.6 mm from the core.

For DM currents, the norm of the magnetic field vector is presented with results of a 2-D finite element simulation preformed with instantaneous asymmetrical currents of values +1 A, -0.5 A and -0.5 A in Figure 8.21. Unlike for the CM field, the external DM field is not ideally null for a non-ferromagnetic core material. Besides that, the spatial configuration of the DM field continuously changes with time for alternating currents. This allows for the external magnetic coupling with other components not mattering its position.

In order to reduce the external field in a three-phase CM inductor, two methods can be applied. The first is to increase the coupling between the windings. The second is to reduce the loop area. The easiest way to achieve both measures would be to twist the three windings together and wind them around the toroidal core. This would demand that the wires are very well insulated and this insulation must withstand high temperatures. This can not be achieved with conventional magnetic wires. Employing special insulation (thicker) would drastically decrease the window occupation and complicating the heat removal. This would lead to larger and more costly inductors.

A new idea is to wind the inductor conventionally, but include properly insulated wires of very small cross-section. This is presented in Figure 8.22. The small section wires are to be wound in parallel with the larger wires, but very close to the other two windings, so that the loop area coupling to external fields is reduced and coupling among different windings is increased. Employing small section wires would guarantee that the current distribution at low frequencies leads to small currents in the small wires. At high frequencies this distribution would become more even and the coupling between the windings of different phases would be high. The main drawback of this solution is that again the window occupation is reduced due to extra wires with thick insulation. Besides that, winding is complex and more expensive, requiring two types of wires. Furthermore, the thermal performance would still be somewhat worsened.

Another technique is to use reversed windings as proposed in Figure 8.23. This follows the same principles as for the DM inductors. Half

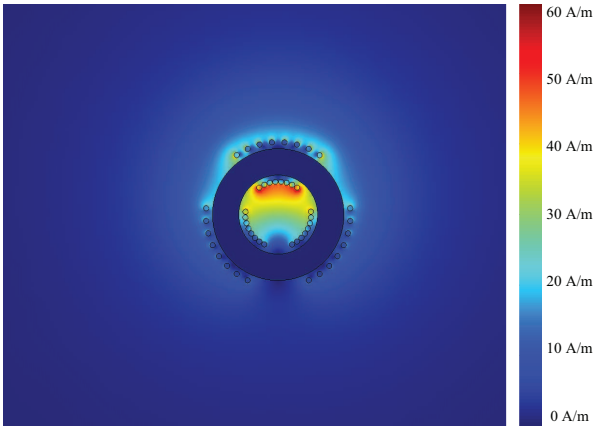


Figure 8.21: Finite elements simulation results (norm of the magnetic field) for DM currents. The simulation is on time domain and shows the norm of the magnetic field due to one current of +1 A in the uppermost winding and two of -0.5 A in the other two windings.

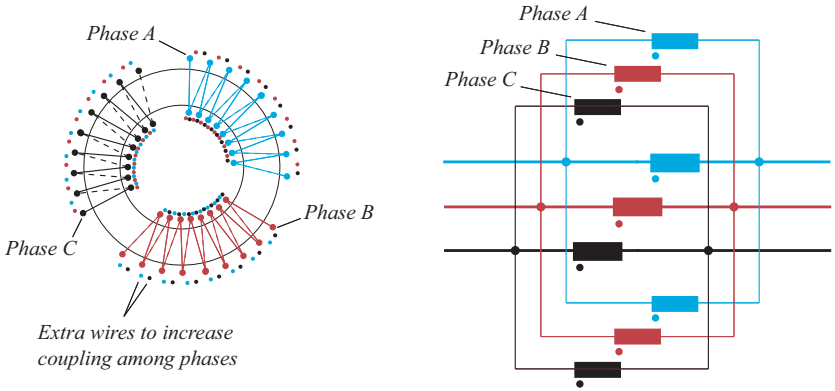


Figure 8.22: Three-phase common mode inductor with extra wires. The smaller, extra wires are wound in parallel with the larger cross section wires, but these connections are not shown in the drawing.

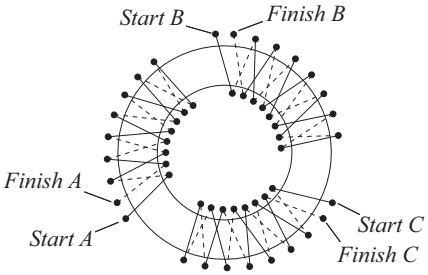


Figure 8.23: Three-phase common mode inductor with reversed windings.

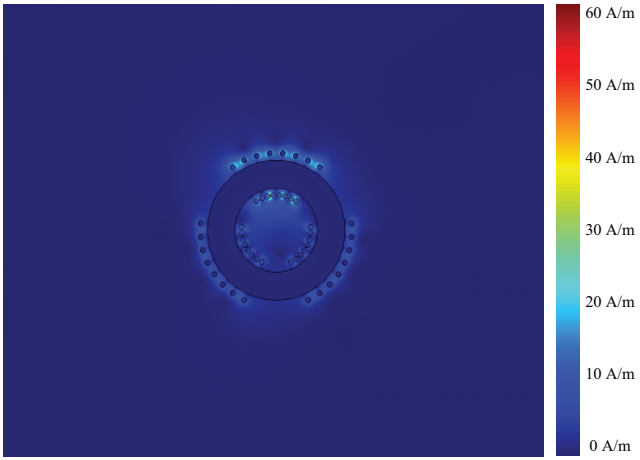


Figure 8.24: Finite elements simulation results (norm of the magnetic field) for DM currents in a CM inductor employing reversed windings. The simulation is on time domain and shows the norm of the magnetic field due to one current of +1 A in the uppermost winding and two of -0.5 A in the other two windings.

of the turns of each winding are wound in one direction and then returns to close to the starting point. This ensures that the loop area coupling to external fields is highly decreased. Each turn follows another with the currents flowing in exactly opposite directions, ensuring low radiated external fields.

For the CM inductor with reversed windings, the norm of the magnetic field vector due to DM currents is presented with results of a 2-D finite element simulation preformed with instantaneous asymmetrical currents of values +1 A, -0.5 A and -0.5 A in Figure 8.24. It is seen that the external DM field is much lower than with the conventional windings. This results in lower magnetic coupling to other filtering components. This type of winding arrangement employs conventional magnetic wires and, in principle, does not reduce window occupation. The drawbacks are that the windings are more difficult to realize and, most important, the parasitic parallel capacitance is significantly increased. The self-leakage inductance is somewhat reduced.

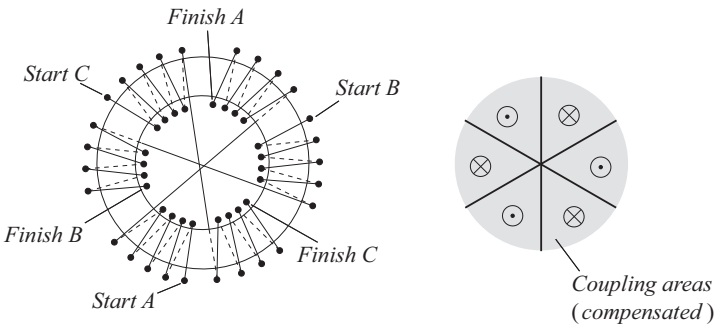


Figure 8.25: Three-phase common mode inductor with interleaved windings.

In order to avoid the increase of the parallel capacitance, a new technique is proposed. This technique is based on the separation and interleaving of the windings. In theory each phase winding can be split in many partial windings that are interleaved with partial windings of the other phases. A practical approach is to split each winding in two as presented in Figure 8.25.

This winding strategy is based on two principles: (i) the areas of coupling to external fields are compensated in the same way as in the DM

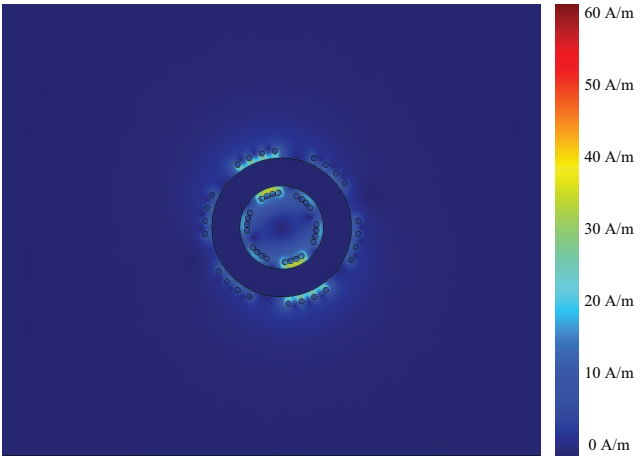


Figure 8.26: Finite elements simulation results (norm of the magnetic field) for DM currents in a CM inductor with split windings (two). The simulation is in time domain and shows the norm of the magnetic field due to one current of +1 A in the uppermost winding and two of -0.5 A in the other two windings.

inductor with two winding directions, and; (*ii*) the effective distance between different phase windings is reduced, increasing the coupling between them. Thus, besides compensating external fields, the self-leakage inductance is effectively decreased. A FEM simulation result for this type of windings is shown in Figure 8.26 for the same conditions as for the CM inductors employing conventional and reversed windings. It is seen that the external field is reduced when compared to the conventional windings, but larger than with the reversed windings. Thus a reduction of couplings with other components can also be achieved with this winding technique. If further reduction is necessary, the windings can be split into more partial windings. This technique slightly reduces the window occupation, since more insulation barriers are required between the now split windings. Splitting into two partial windings seems to be a good compromise. The parallel parasitic capacitance is approximately the same as for conventional windings, having the possibility of even reducing it depending in the number of partial windings and insulation distances. The windings are more complex due to the crossing of wires in the center, which requires insulation. This can be overcome by making the connec-

tion between partial windings directly in the PCB. Thermal performance should not be appreciably affected by this technique.

Based on the presented 2-D FEM simulations, the numerical integration of the magnetic energy density leads to the total stored energy for each of the configurations. This calculated energy is proportional to the inductances. The energy is here calculated for two cases: (*i*) the total energy in the complete simulation environment and; (*ii*) the energy stored in the air surrounding the core and windings. The energy stored in the air is related to the magnetic coupling with external components/loops, while the difference between the total energy and the energy stored in the air is related with the self-leakage inductance. The calculated values are presented in Table 8.1. The absolute values are not important in this analysis, but the relative values provide insight into the coupling and self-leakage inductances for the different techniques.

Table 8.1: Calculated stored energy with the winding techniques for three-phase CM inductors based on FEM simulations.

Winding technique	*Total stored energy* $W_{mag,tot}$	*Air stored energy* $W_{mag,air}$
Conventional	$8.439 \cdot 10^{-7}$ J/m^3	$3.521 \cdot 10^{-7}$ J/m^3
Reversed	$2.457 \cdot 10^{-7}$ J/m^3	$4.181 \cdot 10^{-8}$ J/m^3
Split	$9.956 \cdot 10^{-8}$ J/m^3	$6.305 \cdot 10^{-8}$ J/m^3

Observing the results of Table 8.1 it is seen that the lowest total energy is achieved with the split windings, while the lowest stored energy in the air is obtained with the reversed windings. Both special winding strategies are able to reduce both energies (total and air), thus reducing external couplings and self-leakage inductance. A strong reduction of the self-leakage inductance is achieved with the split windings and this elects this type of winding for applications where the DM currents are very high, allowing the core material to work in a lower portion of the hysteresis curve.

A comparison between the techniques is summarized in Table 8.2. It is seen that the reversed and split windings present significant advantages and certainly can find application areas that justify the higher costs.

Table 8.2: Comparison of different winding techniques for three-phase CM inductors.

Winding technique	Conventional	Extra wires	Reversed	Split
Winding effort	++	−−	+	+−
Cooling	++	−	++	++
Cost	++	−−	+	+
External coupling	−−	++	++	+
Self-leakage	−−	++	−	+
Parasitic capacitance	+−	−	−−	+−

8.5 Experimental Analysis

The effects of magnetic coupling are investigated in this section, through the experimental analysis of different filters and components. The efficacy of coupling cancellation techniques employed in the filter inductors are analyzed.

8.5.1 Inductors with Coupling Reduction

In order to experimentally verify the effects of the external coupling reduction techniques for filtering inductors, the components specified in Table 8.3 have been built.

Table 8.3: Analyzed inductors for external coupling reduction techniques.

Mode	*Core*	*Manufacturer*	*Turns*	*Wire diameter*
DM	55378-A2	Magnetics	18	1 mm
CM	VITROPERM W380	VAC	3 × 7	1 mm
CM	VITROPERM W523	VAC	3 × 8	1 mm

Two DM inductors have been built with the specifications of the upper inductor in Table 8.3. The first one with a conventional winding,

while the second inductor employs the compensated winding proposed in [259]. The impedance of both inductors has been measured with a Precision Impedance Analyzer (Agilent 4294A) and these measurements are shown in Figure 8.27. It is seen that the inductors present quite similar impedance curves. The conventionally wound inductor presents a slightly lower impedance beyond the self-resonance frequency ($\cong$ 22 MHz), but this effect is negligible. This demonstrates that the compensated winding technique does not strongly influence the self impedance of the DM inductor.

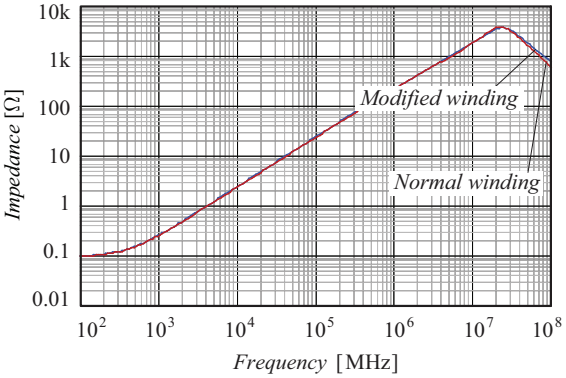


Figure 8.27: Measured impedance for the two DM inductors, one employing conventional winding and the other employing the winding technique presented in [259].

These inductors have been connected to one of the terminals of a 2.2 μF X2 capacitor with a distance of approximately 10 mm, forming an "Γ"-shaped low-pass filter. The components have been mounted on a PCB (same for all arrangements). The insertion loss of this filter has been measured with a network analyzer and the result is presented in Figure 8.29. Three measurements are shown: the first employs the conventional inductor mounted with a distance of 2 mm of the PCB; in the second, the inductor with modified (compensated) winding has been mounted 7 mm apart from the PCB; and, the third employs the modified inductor at a distance of 2 mm from the PCB. It is observed that the modified inductor is capable of reducing the coupling with the capacitor in both configurations, but when placed at a larger distance from the PCB, the gain is

reduced in the frequency range from 1 MHz to 6 MHz. This shows the importance of connecting inductor with short leads and that the special winding is effective in reducing magnetic coupling between DM inductors and capacitors.

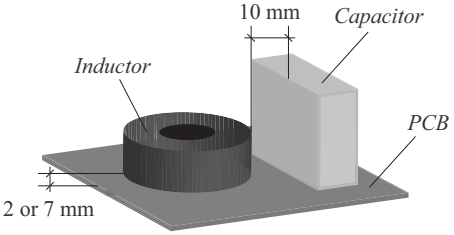


Figure 8.28: Setup for measuring the coupling from the DM inductors to a DM X2 capacitor.

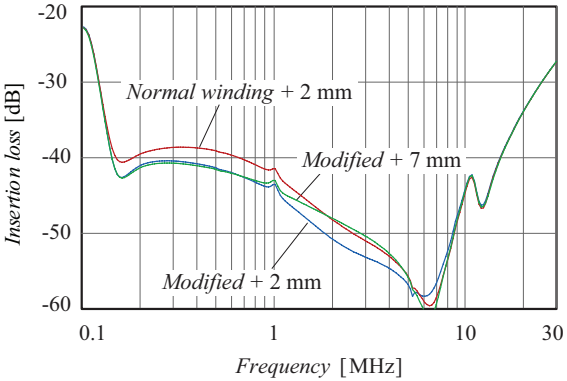


Figure 8.29: Comparison of the insertion loss for the two different DM inductors winding strategies and a 2.2 μF X2 capacitor illustrating the magnetic coupling among these components.

The three-phase CM inductors of Table 8.3 have been measured regarding their CM impedance by connecting the three windings in parallel. In order to measure the leakage inductance the windings have been connected in series so that only DM currents circulate. These measurements have been performed with the impedance analyzer.

Two versions of the larger CM inductor (VITROPERM W380) have been built, one employing reversed windings and another with conventional windings. The measured CM impedance curves of these components are presented in Figure 8.30. It is seen that the inductor with reversed windings presents a much larger parallel parasitic capacitance and consequently a lower self-resonance frequency ($\cong$ 3.6 MHz instead of $\cong$ 8.7 MHz). This reduces the CM impedance of the inductor with reversed windings more than three times ($\cong 600\,\Omega$ instead of $\cong 2\,k\Omega$) at 30 MHz.

The results of the leakage inductance measurements for the two inductors built with VITROPERM W380 are shown in Figure 8.31, from where it is observed that the leakage inductance is reduced by approximately 15 %. The leakage inductances have been measured by connecting two windings in anti-series and dividing the result by two.

Two units of the smaller CM inductor (VITROPERM W523) have been built, the first employing conventional windings and the second with split windings (two partial windings per phase). The measured CM impedance curves of these components are presented in Figure 8.32. With these configurations the inductor employing split windings presents a smaller parasitic capacitance, leading to a slightly higher self-resonance frequency. Thus, higher impedance for frequencies higher than 10 MHz are observed.

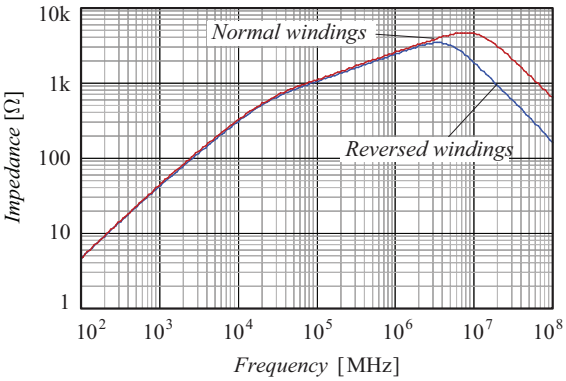


Figure 8.30: Measured CM impedance for the two inductors wound with the W380 core, one employing reversed windings and the other with conventional windings.

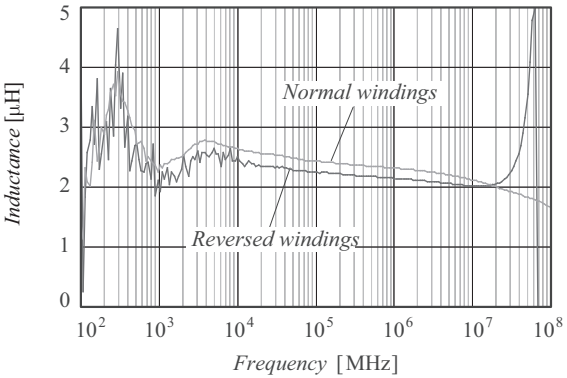


Figure 8.31: Measured leakage inductance for the two inductors wound with the W380 core, one employing reversed windings and the other with conventional windings.

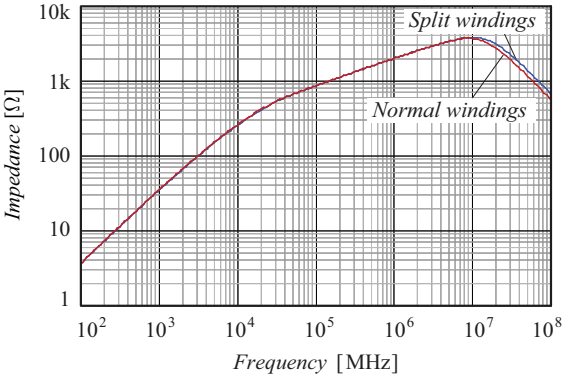


Figure 8.32: Measured CM impedance for the two inductors wound with the W523 core, one employing split windings and the other with conventional windings.

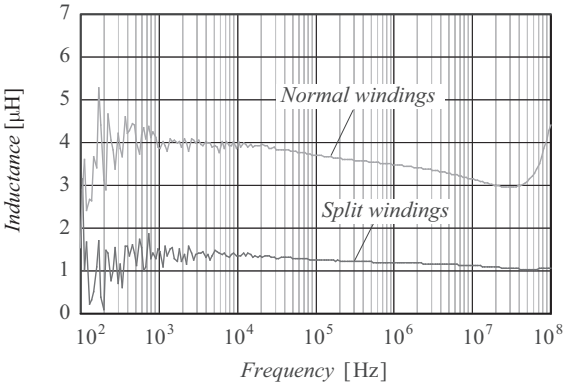


Figure 8.33: Measured leakage inductance for the two inductors wound with the W523 core, one employing split windings and the other with conventional windings.

The leakage inductance of the CM inductors constructed with VITROPERM W523 has been measured as well. The measured leakage inductances are shown in Figure 8.33. The leakage inductance of the inductor with conventional windings is higher than the leakage inductance measured in the VITROPERM W380 inductor because of the higher number of turns and larger internal diameter. The leakage inductance is remarkably reduced with the split windings by a factor of approximately three, demonstrating the efficacy of such arrangement.

In order to compare the three winding strategies, a third sample of the inductor with VITROPERM W523 has been built. A PCB with the circuit shown in Figure 8.34 has been constructed and the DM insertion loss from terminals A_1 and N to terminals A_2 and N measured. The PCB presents the same layout for the three configurations. In all cases, the winding of L_{cm} of phase A, or half of it, was placed close to the capacitor C_A as shown in Figure 8.35. The three DM capacitors have been placed very close to each other and the inductor L_{cm} has been placed in a distance of 1 mm from the most external capacitor (C_A). The DM capacitors C_A, C_B and C_C are 2.2 μF X2 capacitors from Arcotronics [260].

The insertion loss measurement results are presented in Figure 8.36. Three measurements are shown: the first employs the conventional CM inductor; the second with the CM inductor split windings, and; the third

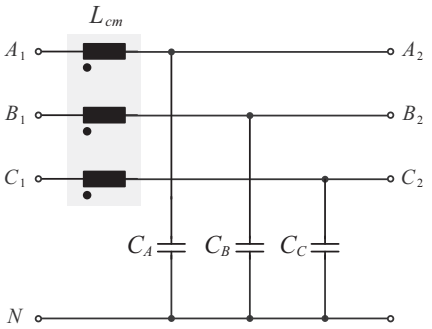


Figure 8.34: Schematics for the measurement of the insertion loss to analyze different CM inductors' winding strategies.

employing reversed windings. It is observed that the filter mounted with the conventionally wound inductor presents the worst performance, except at frequencies higher than 10 MHz, were the inductor with reversed windings certainly presents higher parallel parasitic capacitance. In the frequency range from 200 kHz up to 10 MHz, the inductor with reversed windings presents a slightly better performance. This can be for two reasons, the leakage inductance is higher than for the split windings inductor and the coupling is possibly slightly smaller. These measurements show only the tendencies of such circuits, but it is seen that, even with the highest leakage inductance, the inductor with conventional windings shows the worst performance already at the low frequency end (100 kHz). By changing the source and load impedances (insertion loss is measured with a 50 Ω input / 50 Ω output system) the influence of coupling can be greatly affected.

8.5.2 Experimental Analysis of Three-Phase Filters

In this section experiments with two types of three-phase PWM converters are carried out in order to study the influence of coupling on the performance of three-phase filters. The employed converters have been introduced in section 3.5 (Indirect Matrix Converter – IMC) and section 3.4 (Three-phase/-level boost PWM "Vienna" Rectifier – VR). The filters have been designed with the design procedure presented in section 6.8.

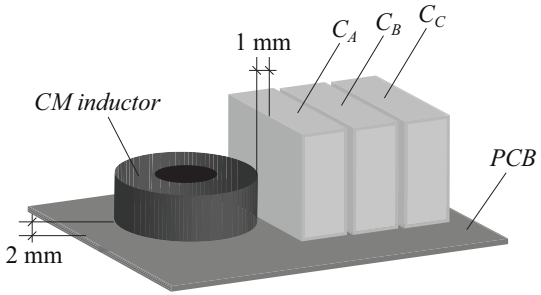


Figure 8.35: Setup for measuring the coupling from the CM inductors to three DM X2 capacitors.

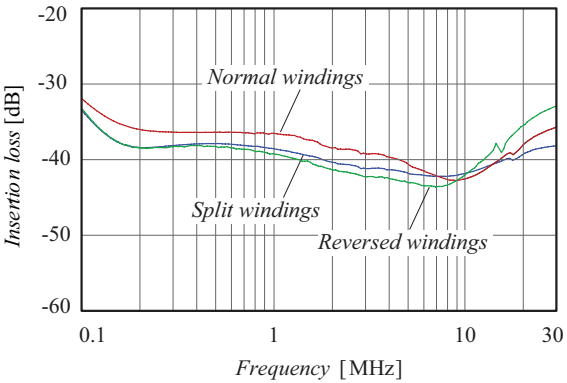


Figure 8.36: Comparison of the insertion loss for the three different CM inductors winding strategies and a 2.2 μF X2 capacitor illustrating the magnetic coupling among these components.

IMC Filter Analysis

Two filters have been constructed for the 6 kVA Indirect Matrix Converter, both presenting the same PCB dimensions. The PCBs present four layers in order to improve the layout and to reduce the area of potential coupling loops [258]. For this reason, a lower number of layers has not been considered here.

For both filters, the specification of the components are kept strictly the same. Therefore, the differences are only on the employed winding strategies of the inductors, both CM and DM, and the second prototype (*Filter 2*) employs ESL cancellation inductors L_{canc} as specified in section 4.7.

The schematics for both filters are presented in Figure 8.37 and a photograph of *Filter 2* is shown in Figure 8.38. In *Filter 1* the components are placed in the same positions, but the ESL canceling coupled inductors L_{canc} are not included. Discharge resistors (four MELF 220 kΩ in series) are placed in parallel with $C_{dm,4}$, but are not included in the schematics. Furthermore, the DM capacitors $C_{dm,4}$ are placed in the power converter printed circuit board and are not shown in the photograph.

The inductors for the filters are specified in Table 8.4. It is seen that the DM inductors L_{dm} are the same as tested in section 8.5.1. The same holds true for the CM inductors. For the damping resistors R_{damp} three SMD resistors (MELF) of value 1.2 Ω/1 W are connected in parallel.

Table 8.4: Inductors employed in the filters for the IMC.

Inductor	*Core*	*Turns*	*Wire*
L_{dm}	55378-A2	18	ϕ 1 mm
L_{damp}	55378-A2	18	ϕ 1 mm
$L_{cm,1}$	VITROPERM W523	3×8	ϕ 1 mm
$L_{cm,2}$	VITROPERM W380	3×7	ϕ 1 mm
L_{canc}	Air (radius = 0.9 cm)	2×2	ϕ 1 mm

The capacitors employed in the filters are specified in Table 8.5. Capacitors $C_{cm,1}$ are not employed in *Filter 2*, while in *Filter 1* these are used to study the effects of having capacitors connected between lines and

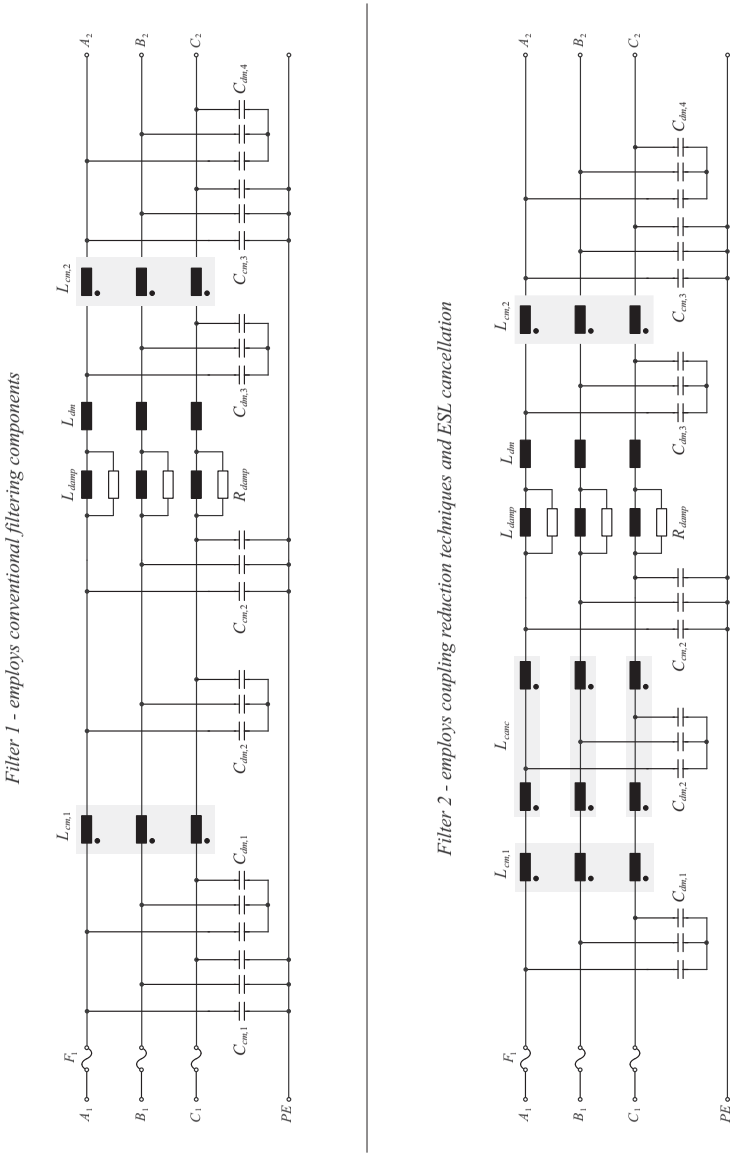


Figure 8.37: Circuit schematics of the filters designed for the Indirect Matrix Converter.

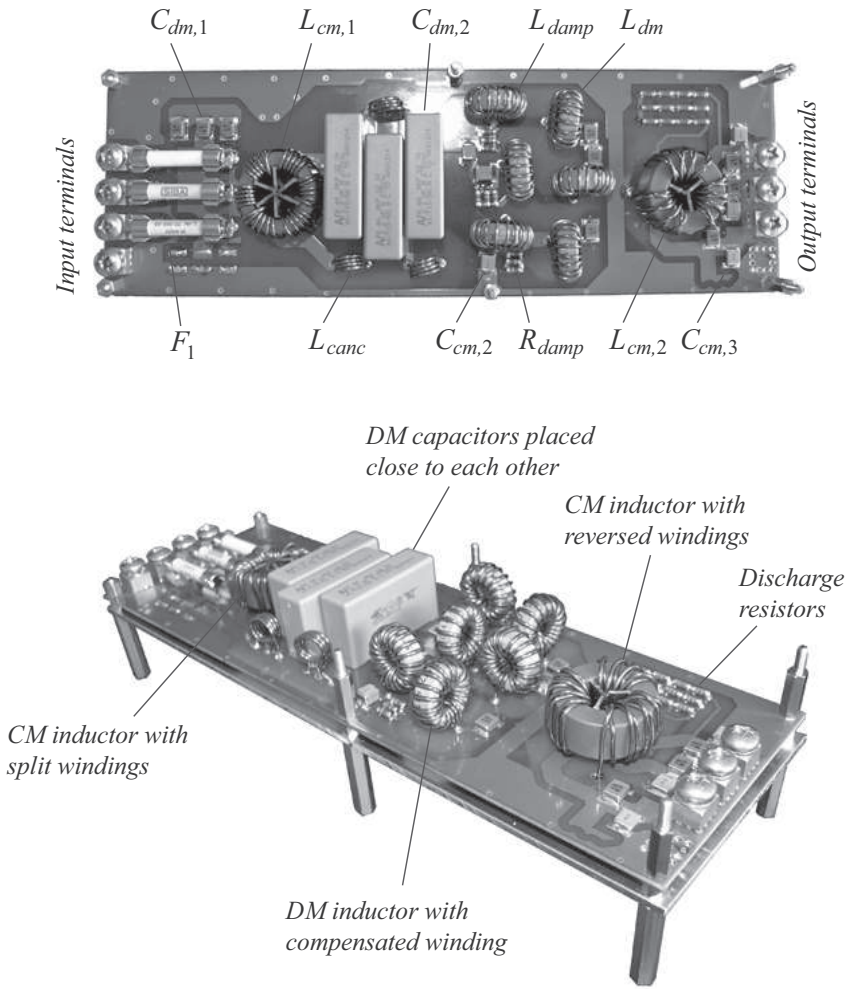


Figure 8.38: Photograph of the filter designed for the Indirect Matrix Converter employing inductors with coupling reduction techniques.

Table 8.5: Capacitors employed in the filters for the IMC.

Capacitor	*Manufacturer*	*Specification*
$C_{dm,1}$ and $C_{dm,3}$	Murata	SMD[a] – X2 33 nF/250 V
$C_{dm,2}$	Arcotronics	TH[b] – X2 2.2 μF/250 V
$C_{dm,4}$	ICEL	TH – AC 10 μF/250 V
$C_{cm,1}$ and $C_{cm,2}$	Murata	SMD – 2 × Y2 4.7 nF/250 V
$C_{cm,3}$	Murata	SMD – 3 × Y2 4.7 nF/250 V

[a] SMD – Surface Mount Device.

[b] TH – Through hole device.

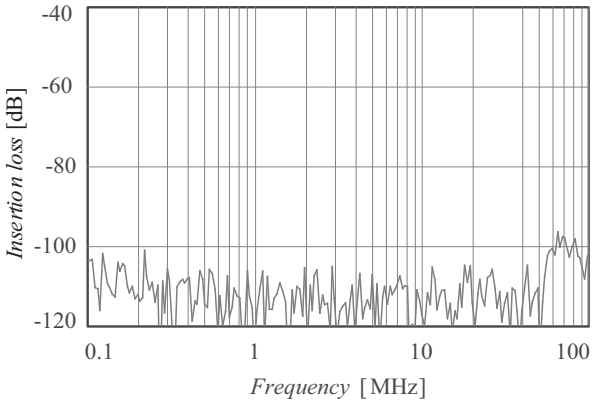


Figure 8.39: Bottom of scale for common mode insertion loss measurements.

PE at the mains side of the filters.

Insertion loss measurements performed as in section 6.4.1 show the performance of the built three-phase filters and are employed here in order to study the effects of different phenomena.

The first series of insertion loss measurements are performed for CM signals. The measurement noise floor is shown in Figure 8.39, where it is seen that it is below or very close to −100 dB up to 100 MHz.

The first studied effect is the inclusion of capacitors $C_{cm,1}$ connected from lines to PE at the mains side of the filters. Only part of the CM

filter is considered along with the LISN as displayed in Figure 8.40.

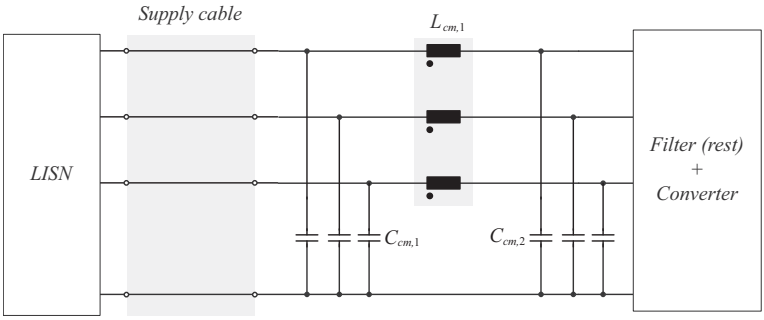


Figure 8.40: Influence of capacitors $C_{cm,1}$ on the attenuation of a three-phase filter.

Considering a single-phase CM equivalent circuit and a magnetic coupling with the input CM current i_{CM}, the circuit of Figure 8.41 is derived.

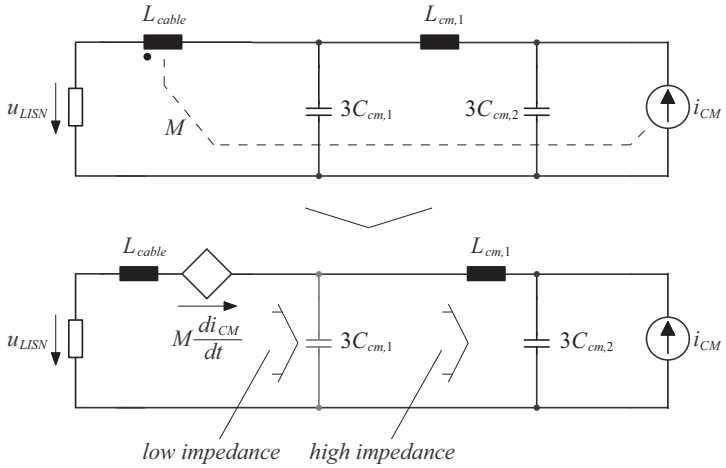


Figure 8.41: Influence of capacitors $C_{cm,1}$ at the attenuation of a three-phase filter.

At a first glance, capacitor $C_{cm,1}$ is placed in parallel with the LISN input terminals and cable impedance and should provide an effective current

divider and, thus, increase filter attenuation for high frequencies. However, the coupling with the CM current modeled by the mutual inductance M has the effect of introducing an induced voltage that is proportional to the mutual inductance and the derivative of the current i_{CM} in series with the CM impedance of the supply cable as shown in Figure 8.41. For high frequencies, in case capacitors $C_{cm,1}$ are included in the circuit, this induced voltage finds as only impedance, the inductance of the supply cable, which is typically low. On the other hand, excluding capacitors $C_{cm,1}$ puts the impedance of the CM inductor $L_{cm,1}$ in series with the induced voltage. These two situations explain the reasons that capacitors connected to PE at the supply-side of a CM filter might worsen filtering performance. It is also clear that the problem is not a resonance between these capacitors and other elements, like the inductances of the cable. In order to illustrate this effect, Figure 8.42 presents simulation results for the circuit of Figure 8.41. It is observed that even with a mutual inductance that is 1/100 of the cable inductance, the influence of the coupling is severe. Thus, the exclusion of capacitors $C_{cm,1}$ improves substantially the attenuation for high frequencies.

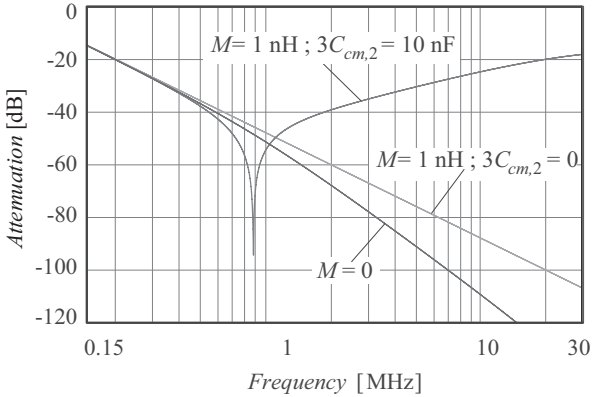


Figure 8.42: Attenuation curves U_{LISN}/I_{CM} showing the influence of magnetic coupling and Y-capacitors $C_{cm,1}$ for different components' values. Not changed are: $L_{cable} = 100$ nH, $L_{cm,1} = 10$ mH, $3C_{cm,2} = 10$ nF and $R_{LISN} = 50/3\ \Omega$.

Nevertheless, if the coupling area between the LISN terminals and the input of the filter is very small, this effect is small and the capacitors might

present a beneficial effect. Special attention must be put on the layout and arrangement of the filter board and the supply terminals of the equipment. Figure 8.43 presents insertion loss measurements of *Filter 1* with and without $C_{cm,1}$. These measurements are without the supply cable and the measurement leads are made very short with BNC connectors. As a result, even without the loop areas of the supply cable, it is seen that magnetic coupling affects strongly the high frequency performance of the filter. If the photograph (cf. Figure 8.38) of the filter is observed, it is seen that the input fuses have a distance to the PCB which is very difficult to reduce, contributing for increasing the CM loop area between capacitors $C_{cm,1}$ and the input terminals.

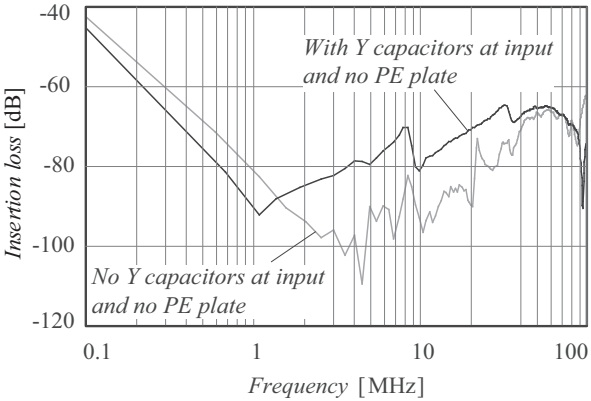


Figure 8.43: Common mode insertion loss measurement for *Filter 1*. Two measurements are shown: the first including the mains sided Y capacitors $C_{cm,1}$ and the second without these capacitors.

As a result of this study, capacitors $C_{cm,1}$, which are not included in *Filter 2*, have been removed from *Filter 1* as well. With this a direct comparison of the filters is possible.

In order to study the effect of a metal plate connected to PE and placed below the filters, the CM insertion loss of *Filter 2* has been measured for three different separation distances, namely: 30 mm, 14 mm and 6 mm. The metal plate is shown below the filter board in Figure 8.38, where it is seen that it is connected to the PE plane in the PCB through six metal poles. The size of these metallic connections has been varied to

adjust to the three listed distances. The measured results are displayed in Figure 8.44. It is seen that the shorter the distance, the better is the high frequency attenuation. This is due to two main effects: the main effect is most probably due to the reduced loop areas between PCB, components and the PE conductors (PCB traces, PCB planes, metal poles and plate). With this, the high frequency current distribution is better, so that loop inductances are smaller and generated magnetic fields are reduced in a shorter distance. A second and also beneficial effect is the increase of the capacitance from the lines to PE. This shows the importance of a good high frequency layout for the filters, where 40 dB at 30 MHz can be gained by just reducing loop areas.

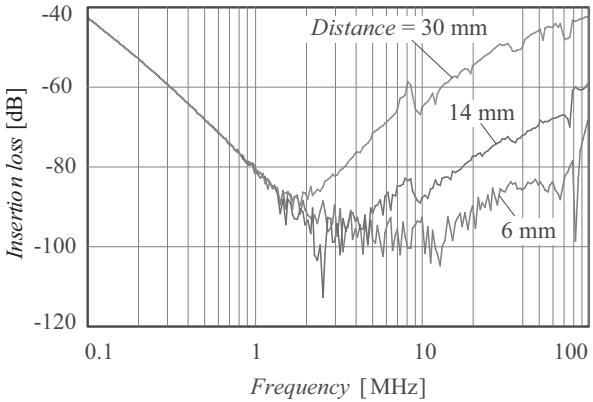


Figure 8.44: Common mode insertion loss measurement for *Filter 2*, excluding the mains sided Y capacitors $C_{cm,1}$. The filter is placed over a solid conductive plate connected to PE at the different shown distances.

A separation distance of 6 mm has been used in both filters, so that a proper comparison of the achieved results is possible.

In order to compare the effectiveness of the coupling reduction techniques applied to CM and DM inductors, the CM insertion loss of both filters with similar configurations has been measured. The measurement results are presented in Figure 8.45. It is observed that the board with coupling reduction techniques presents better performance at high frequencies, starting from 4 MHz. This shows the effectiveness of the employed winding strategies.

Comparing the CM insertion loss measurement results for frequencies higher than 30 MHz (maximum frequency for conducted emissions testing) show that an improvement of more than 10 dB is achieved at 30 MHz. This improvement is observed up to 100 MHz. Thus, suggesting that the employed coupling reduction techniques might have a beneficial impact in the radiated emissions, where the main radiation sources are CM currents [24].

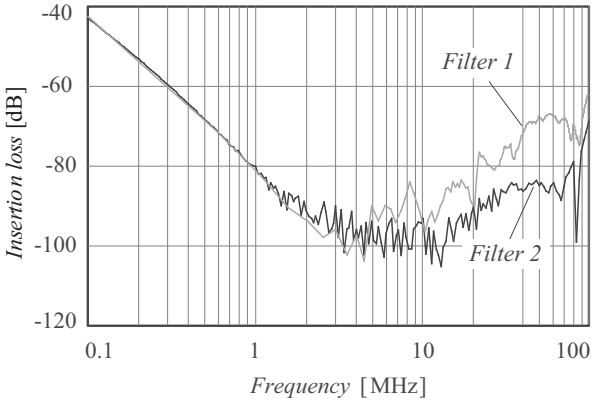


Figure 8.45: Common mode insertion loss measurement for both filters. The mains sided Y capacitors $C_{cm,1}$ are excluded and a metallic plate connected to PE is included at a distance of 6 mm from the printed circuit boards.

Differential mode insertion loss measurements have been performed for the same filter configurations in order to study the impact of the coupling reduction techniques in the DM attenuation. These results are shown in Figure 8.46. Unfortunately, the employed measurement insulation transformers limits the insertion loss measurement range for high frequencies. With this, the measurement floor is too high already from 2 MHz on and a comparison of the DM insertion loss of the filters can not be done for higher frequencies. This comparison is performed latter in this section through conducted emission measurements.

Nevertheless, from the comparison of the measurements depicted in Figure 8.46, it is seen that the filter employing coupling reduction (*Filter 2*) presents higher insertion loss in the frequency range from 200 kHz to 600 kHz. This observation suggests that the employed coupling reduction

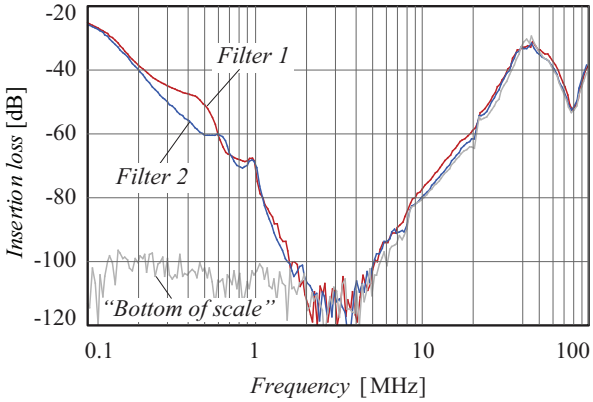


Figure 8.46: Differential mode insertion loss measurement for both filters. Also shown is the insertion loss measurement floor – "bottom of scale".

winding techniques have a beneficial impact also for differential mode conducted emissions, improving noise attenuation performance.

Another technique that might help in the DM attenuation is the use of the ESL cancellation coupled inductors in *Filter 2*. The effects of these inductors are only observed beyond the self-resonance of the DM capacitors $C_{dm,2}$, which is around 1.1 MHz. Thus, the improvement observed in the DM insertion loss measurements, which is for frequencies lower than 600 kHz, must be due to the coupling reduction strategies.

Quasi-peak conducted emission measurements with the filters and the IMC supplying a 2 kVA asynchronous machine through a 3 m long shielded cable were performed with both filters and different configurations. In order to restrain HF couplings between the designed filter and the power circuits of the IMC, a shielded box with separate chambers to separately accommodate the power circuit and the input filter was built as shown in Figure 8.47. The filter boards have been connected through metallic poles to the box in six different places as shown in Figure 8.38. Furthermore, the heatsink of the Indirect Matrix Converter has been also connected to the shielded box through conductive copper tapes, assuring a good high frequency bonding.

In order to separately observe the effects of CM and DM emissions, a three-phase CM/DM noise separator [150] has been employed in some

measurements.

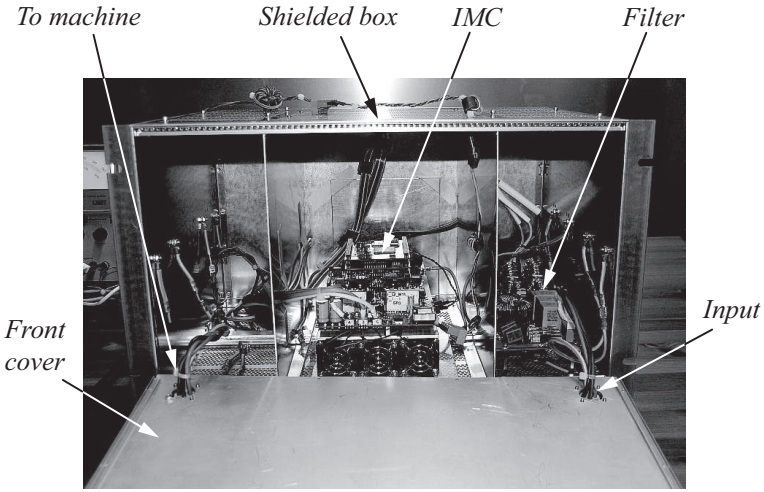


Figure 8.47: Shielded box containing filter and Indirect Matrix Converter as employed in the CE measurements.

The first conducted emission tests have been performed in order to, once again, observe the effects of the mains sided Y capacitors $C_{cm,1}$. Figure 8.48 shows the CE levels for *Filter 1* with $C_{cm,1}$ included, while Figure 8.49 presents the results for the same configuration, but without these capacitors. Both configurations have been optimized from a loop area point of view. This means that the CM and DM loop between the IMC and the filter board have been minimized at the most. Furthermore, the loop area between the mains sided filter terminals and the supply cable have been minimized as well, where conductive copper tape has been employed around the connecting cables.

Regarding common mode emissions, it is observed that the inclusion of capacitors $C_{cm,1}$ causes an increase of the CM emissions already at 300 kHz. The increase is observed in the frequency range from 300 kHz up to approximately 5 MHz. Thus, increasing CM and total emissions. Beyond 5MHz the effects of these capacitors can not be clearly seen and other parasitic effects dominate the filter attenuation.

Differential mode emissions, however, show a slight increase in the

frequency ranges from 700 kHz to 900 kHz and 2 MHz up to 10 MHz. Again, for high frequencies, very small influence is noticed. Summing up the effects of CM and DM, the total measured conducted emission levels are reduced with the exclusion of the mains sided Y capacitors.

The first conducted emission measurements with *Filter 2* are done in order to evaluate the effects of different coupling loop areas, namely: the influence of the shielded box and the influence of the area between the IMC input terminal and the filter board, that means the connection between the power converter and the EMC input filters.

Figure 8.50 shows the CE levels for the case when the front cover of the shielded box is opened. It is seen that for the whole measurement frequency range, the levels are higher than for the other configurations shown in Figure 8.51 and Figure 8.52. Is special it is seen that a steep increase in the emissions is observed from 1 MHz up to 4 MHz. Thus, the shielded box reduces coupling from the power and filtering circuits to the supply cable and LISN circuits. With this configuration, the CISPR 11 Class A limit is crossed by more than 20 dB.

Closing the front cover of the shielded box and employing simple cables, which are placed close to each other and close to the wall of the shielded box, to connect the power converter board to the input filter board, leads to the measurement levels shown in Figure 8.51. Better results are achieved, strongly reducing CM and DM levels in the whole frequency range. A noticeable improvement occurs in the frequency range from 1 MHz to 10 MHz. Unfortunately, this measure is not enough to bring the total emission level below the Class A QP limit.

In order to improve the filtering performance, twisted cables have been employed to connect the IMC to the EMC filter board. Furthermore, these twisted cables have been shielded with conductive copper tape, so that the loop area of this connection is strongly reduced. The final results are displayed in Figure 8.52. It is observed that the CM and DM emissions between 3 MHz and 6 MHz are reduced while some alterations occur at frequencies higher than 10 MHz. With these measurements, it is seen that the effects of these considerably large loop areas are mostly noticed in the frequency range from 300 kHz to 10 MHz. Higher frequencies seem to be not so much affected. Thus, the parasitics of the components, including the coupling between them, might be dominant effects at these frequencies.

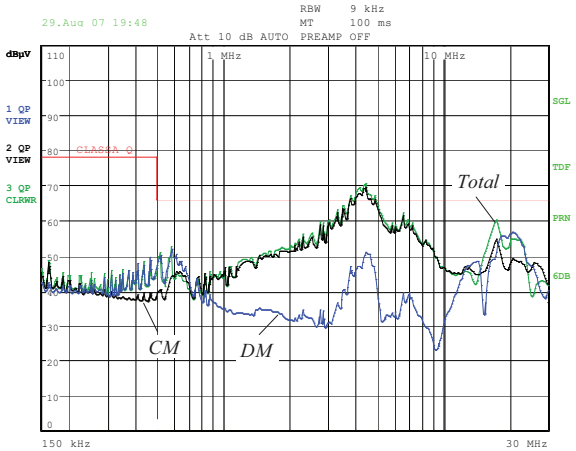


Figure 8.48: Conducted emission measurements (CM, DM and total levels) with *Filter 1* including the mains sided Y capacitors $C_{cm,1}$. The complete system is inside the shielded box.

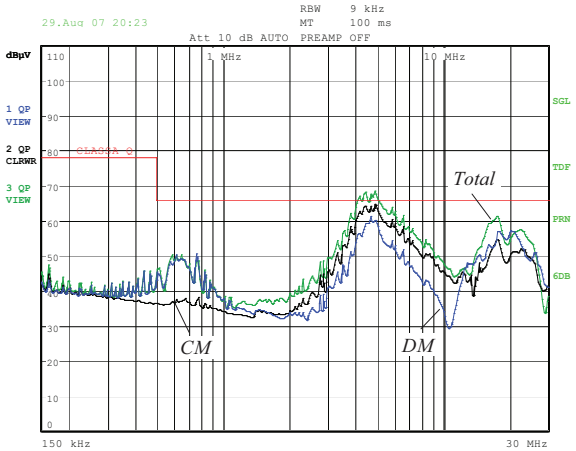


Figure 8.49: Conducted emission measurements (CM, DM and total levels) with *Filter 1* excluding the mains sided Y capacitors $C_{cm,1}$. The complete system is placed inside the shielded box.

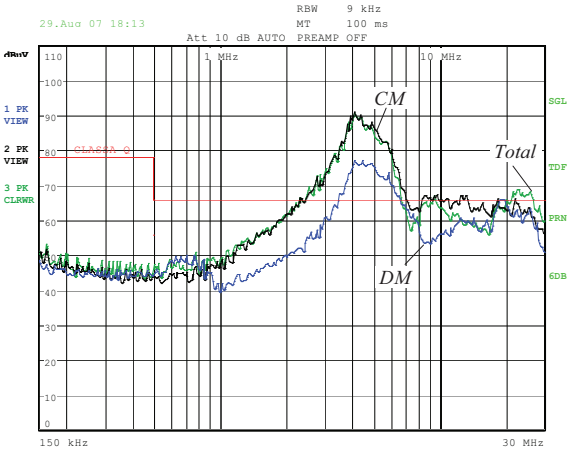


Figure 8.50: Conducted emission measurements (CM, DM and total levels) with *Filter 2*. The door of the shielded box is opened.

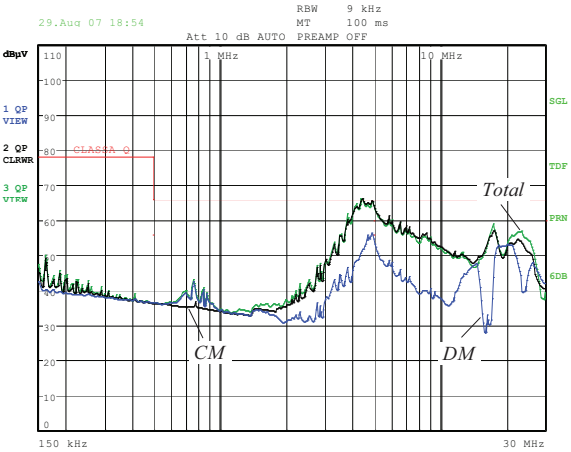


Figure 8.51: Conducted emission measurements (CM, DM and total levels) with Filter 2. The complete system is placed inside the shielded box.

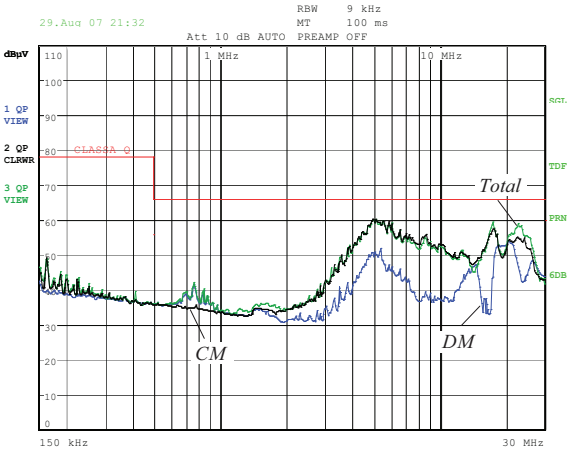


Figure 8.52: Conducted emission measurements (CM, DM and total levels) with Filter 2 with a reduced loop between the Indirect Matrix Converter and the filter board. The complete system is placed inside the shielded box.

The measurements results for *Filter 2* shown in Figure 8.52 have been performed for a similar configuration as the results shown for *Filter 1* in Figure 8.49. It is observed the setup with the second filter, which employs *ESL* cancellation and coupling reduction techniques, presents a better performance, being able to fulfill CISPR 11 Class A QP limits with a 6 dB margin in the whole frequency range. Thus, the validity of the presented techniques is demonstrated in a practical application.

8.6 Summary

The effects of magnetic and electric fields coupling throughout the different parts of a three-phase power system comprising a power converter and an EMC filter have been here explored due to the lacking literature on this specific subject. Basic models that explain the coupling mechanisms and their effects on the performance of three-phase EMC filters have been proposed and a basic review of the describing equations has been done.

The mechanisms of capacitive noise coupling in three-phase EMC filters has been briefly described in this chapter. It has been shown that the

main capacitive connections are due to parasitic capacitances of employed filtering inductors. These effects can be reduced by employing capacitance cancellation techniques as proposed in section 4.8.2. It has been explained that special attention must be taken regarding not only two conductive surfaces, but also with surfaces that are in the vicinity of the components.

The effects of magnetic couplings between filtering components has been introduced with a brief literature review, based on reported research of single-phase filters. Magnetic coupling issues that are particular to three-phase filters have been studied and practical measures to hinder coupling effects presented. The arrangement for DM capacitors employed in a filter stage of a three-phase filter has been studied and an arrangement that reduces the effects of the equivalent series inductances of these capacitors has been proposed, based on the correct coupling direction between such capacitors and a short distance between them.

As conventional three-phase CM inductors have leakage, thus external, fields that propagate in all directions, the placement of such components is extremely important and difficult in a filter where space occupation is limited. The coupling mechanisms of these fields have been reviewed and practical measures to reduce the external field of three-phase CM inductors are proposed through the employment of special winding configurations. The impact of such winding techniques on the impedance of the inductors is evaluated through measurements and finite elements simulation results.

A system employing a three-phase AC-AC Indirect Matrix Converter as noise source and input filters has been constructed and tested. This case study is reported showing the importance of keeping small interconnection loop areas in the whole system. Two filter boards have been built based on a four layers PCB, one based on conventional components and another employing the presented coupling reduction and ESL cancellation techniques. A comparison between these filters is made and the effectiveness of the employed strategies is demonstrated. Conclusions are made leading to important guidelines for the physical layout and arrangement of three-phase EMC filters.

Chapter 9

Influence of EMC Filters in Power Density

"Perhaps no variable brings the problems of being alive so vividly and clearly before the analyst's eye as does size." Gregory Bateson

9.1 Introduction

Power Electronics high power converters are used in the most different types of industry, supplying stable and reliable DC or AC energy to equipments, motors, batteries, etc. These converters must present a few very important characteristics, namely: (*i*) high power conversion efficiency; (*ii*) small volume; (*iii*) high reliability; (*iv*) safety to the users, and; (*v*) electromagnetic compatibility. High efficiency and small volume are commons aims among end users and manufacturers, while the other aims can be seen as end user requirements. These aims were treated differently since the first inventions in the field, but lately they are translated into national and international standards.

Power conversion efficiency η is defined as the ratio of power available at the output of a power converter in relation to the total consumed power at its input,

$$\eta = \frac{P_o}{P_{total,input}} \cdot 100\% \ , \tag{9.1}$$

and is commonly named efficiency.

The efficiency is usually defined for the nominal output rated power and it is a very important measure of the performance of a power converter. It can be considered for the study of the speed of change in the Power Electronics technology, but as it can be seen in Figure 9.1 it is naturally saturating close to its theoretical maximum at 100% and depending on the employed semiconductor technology it can be completely different. Since the 1920's there have been rectifiers with very high efficiency. For this reason it is very difficult to use this figure of merit (FOM) to evaluate the evolution of the power converters. This has been the opinion shown in [261, 262].

Another interpretation is that the technology has entered into the upper part of the efficiency S-curve and very small advancements are to be seen in the future. This can be seen with the trend-line traced in Figure 9.1 for the switch mode power converters, which are the latest addition (1970's) to the Power Electronics technologies and represent the "state-of-the-art" at the moment. For either of these reasons, the use of efficiency as a FOM to evaluate the late technology does not seem to lead to useful results.

For the explained reason, other FOM is desirable. The power converters are usually rated for the amount of power which they are able to supply and this is named "rated power". Thus, a very useful quantity is the power density of the converter, which is defined as the ratio between the rated output power P_o and the total volume of the system Vol,

$$\rho = \frac{P_o}{Vol} \ [\mathrm{W/dm^3}]. \tag{9.2}$$

Power density seems to be still increasing quite rapidly depending on the application. This can be observed in Figure 9.2, where all the data points collected in this work are shown. From the graph it is clear that a lot of progress has happened in the late years and this seems to provide useful insight into the technology change of power converters over time. For this reason it is the parameter used throughout this work to address the change in the Power Electronics technology.

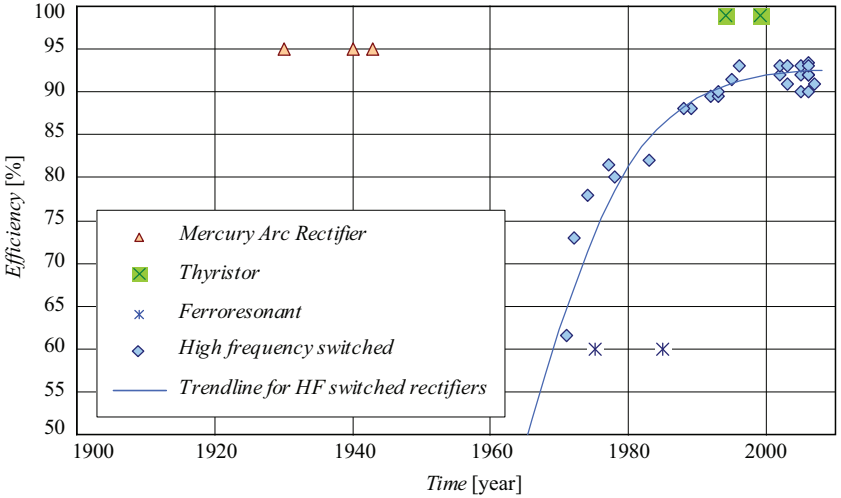


Figure 9.1: Evolution of the power conversion efficiency for different semiconductor technologies.

The measurement of the evolution of power density over time is here performed through the collection of data acquired from books, magazines, scientific journals, manufacturers' homepages, product catalogs, articles published in the World Wide Web and personal communication (e-mail) with industry personnel.

The graph shown in Figure 9.2 shows the calculated power density for the complete data collection as a function of time. Through the observation of this picture it is seen that power density continues to increase and an exponential trend can be traced. It is also possible to conclude that two major periods have occurred, where considerable improvement has happened. The first has taken place in the 1940's and 1950's and this is synchronized with the mature technological state of mercury arc rectifiers, which was the second technology used for the construction of power converters. The second period has been happening since the 1990's until today and this is coincident with the use of high switching frequencies enabled by the use of power transistors (BJT's, MOSFET's and IGBT's). Still another improvement is observed in the 1970's with the employment of semiconductor built thyristors and diodes, but this improvement is not

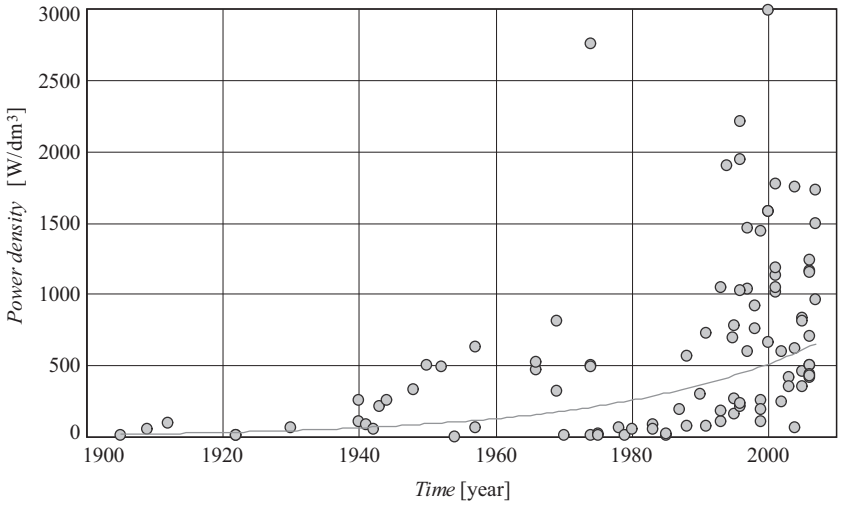


Figure 9.2: Change in power density expressed in watts per liter over time for the gathered data. An exponential trend line based on the measured points is shown.

as clear as the other two previously cited. In Figure 9.2 no distinction is made regarding the application and employed technology. Therefore, a clear picture of the complete evolution of Power Electronics is not observed and a distinction is performed in the following presented results.

Two classes of equipment are analyzed, namely inverters and rectifiers. The results which are presented here for inverters are based on the literature. Nevertheless, the power density evolution is closely related with the one of the analyzed rectifiers.

In Figure 9.3 the power density evolution for inverters is shown. These results have been published in [261, 262] and in [15] and show that an exponential growth has been happening since the early 1970's which was enabled by the use of high frequency switched converters. Such equipments make use of ever improving power semiconductors and it is also observed in [261, 262] that the continuous improvement of semiconductor technology must endure if this exponential growth is to be continued.

The power rectifiers are here divided in two groups depending on their rated output power. This is done because the employed technology can

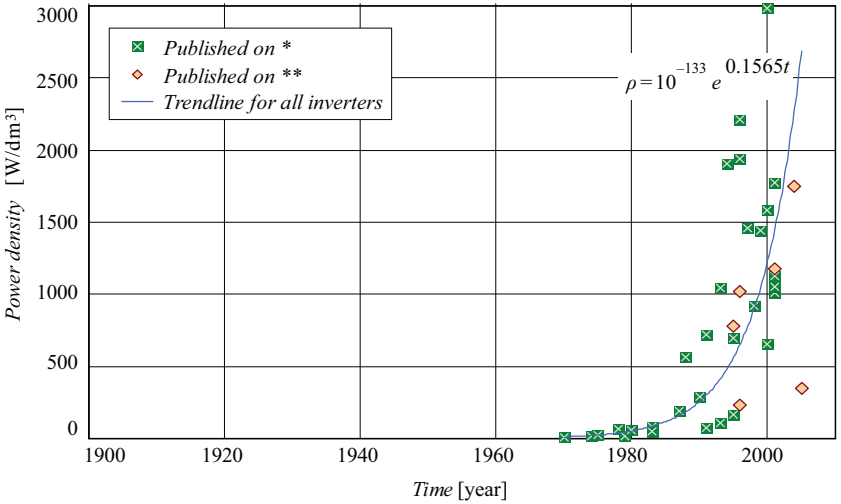


Figure 9.3: Change in power density for inverters as published in * [261, 262] and ** [15]. An exponential trend line based on the measured points is shown.

be quite different for both groups. The first group comprises the rectifiers with a rated power from 100 kW up to 10 MW. The second group encompasses the rectifiers from 1 kW to 100 kW. Other power ratings are observed in practice, but would require a much larger effort in the collection of data. Rectifiers with more than 10 MW are rare and their construction is quite complex, thus it is not easy to evaluate their power density. For the low power range, the amount of equipment is immense, since it comprises most of the power supplies for household appliances, personal computers, laptops and so on. These are very competitive markets, where not large differences are seen among different manufacturers and not so much research results are published. The high power rectifiers are a good measure for the whole Power Electronics field since they are among the equipments with high aggregated value. Therefore "state-of-the-art" technology is to be expected in such systems. Special focus is placed on DC power supplies for telecommunication systems, which demand high performance due to stringent international standards in the field.

For the rectifiers of lower power ratings (1 to 10 kW), the measured

power density points are presented for the different employed technologies, namely: (*i*) Mercury Arc Rectifiers, including all types of vacuum valve tubes; (*ii*) Synchronous mechanical rectifiers, which are based on a rotary arrangement with AC and DC electric motors, and; (*iii*) Thyristors, diodes and GTOs representing the semiconductor based rectifiers which are switched with low frequency; and, (*v*) another class is included, which is called MOSFET, but represents all types of power transistors (BJTs, IGBTs, and MOSFETs) switched at high frequencies, usually higher than 2 kHz. The transistors were invented in the late 1950's and 1960's, but were only incorporated in products later on. The collected data for these rectifiers is presented in Figure 9.4 for the different switch technologies. It is seen that very little progress is observed until the 1990's, when high research efforts were applied in order to achieve better circuits, semiconductor based switches, magnetic materials and capacitors, besides the employment of digital processors [19]. For this reason, two tendency curves are shown in Figure 9.4, one shows the exponential fitted curve for the complete data set and another curve approximates the rapid growth observed on the high frequency switched converters. The use of high switching frequencies has enabled the reduction of passive components volume (transformers, inductors and capacitors) and is the main factor for the current exponential increase in the power density. Research oriented prototypes are typically preceding products five to ten years [261, 262] and, based on these, it is expected that the exponential growth in power density for this class of rectifiers continues. However, it is very difficult to predict for how long since it depends on a number of different enabling technologies, such as materials, circuits and scientific understanding.

Two of the main factors that influence the power density of power converters are the cooling system and the passive components, where the EMC filters are responsible for a substantial part [13, 263]. Increase in the power density is possible, in principle, with an increase of switching frequency or an increase in the operating temperature of the power semiconductors. Higher switching frequencies (smaller passive components), however, lead to higher switching losses (larger cooling systems). Therefore, a compromise exists, in which a Power Electronics engineer must find an optimum.

This chapter aims in the evaluation of the influence of the EMC filters on the power density of three-phase PWM converters. In order to achieve this objective, two topologies are chosen, namely: a three-phase AC-DC-

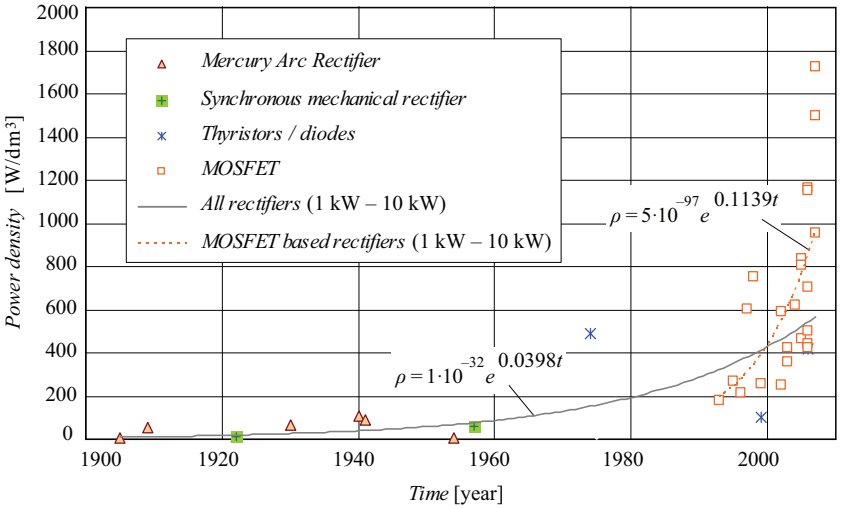


Figure 9.4: Evolution of power density over time for power rectifiers rated from 1 kW to 100 kW. Two exponentially fitted curves are shown: one for all (full line) collected points and another for the lately introduced high frequency switched mode rectifiers (dashed).

AC Sparse Matrix Converter (SMC) and a three-phase PFC Vienna Rectifier. The design of the EMC filters for these topologies is performed in order to obtain minimum volume filters based on the filter design practices employed in this work. The calculated filters present a minimum limitation for the achievable power density of the power converters and consequently are of high importance in the course of the design of power converters. This procedure is presented in the following sections, starting by the dimensioning of the filter components, explaining the filter design procedure for both converters, presenting the obtained results and comparing them with built prototypes.

9.2 Volume Estimation of Filter Components

In order to evaluate the impact of EMC filters on the power density of three-phase PWM converters, the volume of the employed filtering com-

ponents must be known. For analyzing the maximum achievable power density figures, the volume of such components must be the smallest possible. Thus, this section discusses on the design of the filter components assuming necessary simplifications, so that the volume of the components can be predicted beforehand and that the achieved volume is close to the smallest possible with today's commercially available materials and components.

9.2.1 Volume Estimation for CM Inductors

To estimate the volume of CM inductors, a model must be derived. This model is proposed in the following and is based on a series of designs as performed in section 7.4.2. A series of inductors are designed with the following assumptions:

- possible asymmetries, parasitic capacitances and the effect of the tolerances are neglected;
- ambient temperature equals 45°C and the maximum temperature rise is 60°C;
- a single winding layer is allowed in order to reduce parasitics;
- iterative choice of the maximum flux density B_{max} and current density J_{max} is performed;
- discrete values determined by the limited choice of cores and wire diameters are approximated by continuous functions.

For the design of the CM choke a maximum window factor of 0.28 is considered. The design takes into consideration the variation of the complex permeability of the cores as well as the total losses, where the maximum temperature rise is limited to 75 °C.

Based on these design guidelines, a series of inductor designs is conducted for different frequencies and current ratings. In order to simplify the analysis, only material VITROPERM 500 F is considered here. Furthermore, only the cores commercially available from VAC [172, 173] are employed, leading to ten different sizes of inductors (cf. Figure 9.5).

In Figure 9.5 the dependency of the volume of an inductor on its product of areas $A_e A_w$ is depicted along with the core volume for two

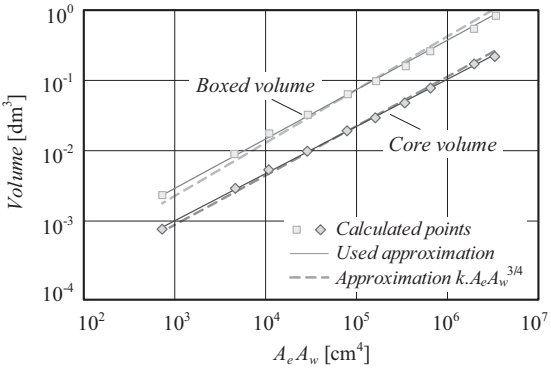


Figure 9.5: Dependency of an inductor's boxed and core volume on area product $A_e A_w$ of the used material.

types of core coatings, namely epoxy coated cores and cores with a plastic enclosure. This dependency is usually considered with a power of 3/4, but for the case at hand a lower factor is employed leading to closer approximations. With this, the volume of the filter inductor Vol_{Lcm} is calculated with,

$$Vol_{Lcm} = k_{geo}(A_e A_w)^{\alpha_{geo}}, \tag{9.3}$$

with,

$$k_{geo} \cong 10.776 \cdot 10^{-2}\,[\mathrm{dm}^3] \tag{9.4}$$

$$\alpha_{geo} \cong 0.7052, \tag{9.5}$$

for the cores with a plastic enclosure.

From the results obtained in the performed designs, approximative functions can be empirically found for the two main design parameters, namely: the maximum current density J_{max} and the maximum flux density B_{max} as functions of the core product of areas $A_e A_w$ and switching frequency f_s, respectively.

The obtained curve for the maximum current density J_{max} is presented in Figure 9.6, where it is seen that the current density is a function of

the product of areas, where larger inductors require lower current density. This seems logical since the relation between the outer surface and the volume of the toroidal inductors is more favorable for small cores. Therefore, the relative thermal resistance of small inductors shall be smaller than the one of large inductors. This can also be explained by observing the distance between the hottest spot and the outer surface, which is smaller for small inductors.

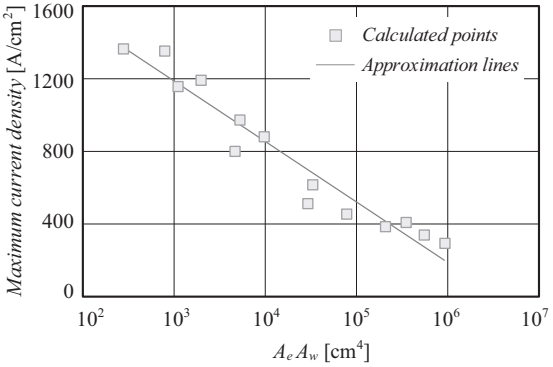


Figure 9.6: Maximum current density as a function of the area product.

The maximum flux density B_{max} is plotted as a function of the switching frequency f_s in Figure 9.7. It is observed that the employed maximum flux density is assumed to be determined by the saturation flux B_{sat} for low switching frequencies, but if the switching frequency increases the flux density is reduced and, thus, keeps core losses under controlled values. The core losses are simply computed with the peak harmonic at the switching frequency and using the Steinmetz equation. This simplification is necessary in order to achieve a time efficient algorithm for the volume calculation. In a precise design, this would have to be specially considered if the switching frequency is very high (» 100 kHz). The core losses are designed to be lower than 20 % of the total losses.

Considering all available cores and evaluating the maximum impedance they can provide for each of the design points leads to the smallest inductor volume for a given impedance. Finally, based on these considerations and on the material's complex permeability curves an equation for the maximum achievable CM choke impedance Z_{choke} for a given

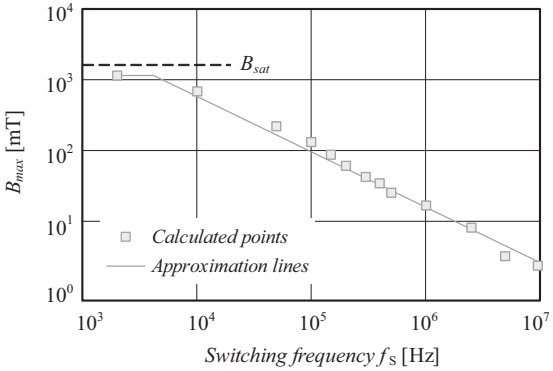


Figure 9.7: Maximum flux density as a function of the switching frequency.

product of areas and switching frequency is empirically derived,

$$Z_{choke}(f_{int}) \cong 10^{2.243-2\cdot\log(I_{N1})+0.181\cdot\log(|\mu(f_{int})|\cdot f_{int})\cdot\log(A_e A_w)}, \qquad (9.6)$$

from where, given the inductor's RMS current I_{N1}, the frequency of interest f_{int} and the required product of areas $A_e A_w$, the desired CM inductor impedance Z_{choke} can be found. As an example, Figure 9.8 shows the calculated impedance at $f_{int} = 150$ kHz and $I_{N1} = 15$ A as a function of area product for two core types.

Equation eq. (9.6) presents an R-squared value higher than 0.939 for frequencies in the range 150 kHz $\leqslant f_{int} \leqslant$ 10 MHz, when compared with the calculated values. Solving eq. (9.6) for the product of areas leads to the core size and its volume can be calculated with the help of eq. (9.3). This approach is useful in an optimization procedure where a minimum total volume for the filters and power converter are searched.

9.2.2 Volume Estimation for DM Inductors

The design of the DM inductors is considerably different to that of CM ones. The differential mode currents are composed of a high amplitude mains frequency component and a relatively small high frequency ripple due to the attenuation given by the boost inductors and capacitors

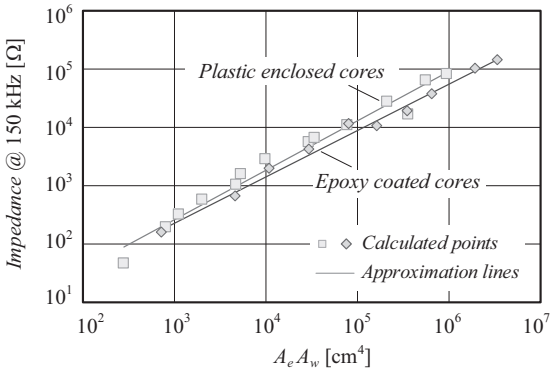


Figure 9.8: Impedance at $f_{int} = 150$ kHz and 15 A (RMS) as a function of the area product for two core types namely, epoxy coated cores and cores with a plastic enclosure employing VITROPERM 500 F.

$C_{DM,1}$. For this reason, the cross sectional area of the core A_e is determined mainly by saturation and not by core losses. Furthermore, the high frequency losses in the winding are also comparatively small and can be neglected. The other parameter that defines the core is the required winding area A_w.

The filter inductance $L_{DM,i}$ and rated current are related to the size of the required core area product by,

$$L_{DM,i}\, I_{N1,peak}\, I_{N1,rms} = k_w J_{\max} B_{peak} A_e A_w. \tag{9.7}$$

The volume of the filter inductor Vol_{Ldm} is calculated with,

$$Vol_{Ldm} = k_{geo}(A_e A_w)^{\alpha_{geo}}, \tag{9.8}$$

where, the parameters k_{geo} and α_{geo} account for the geometry of the core (toroidal, planar, etc). Assuming that a dimension grows proportionally with the other ones, α_{geo} is tipicaly taken as $3/4$.

A series of designs is performed aiming for a characterization of the volume of the DM inductors related to their rated current and inductance. The resulting designs are shown in Figure 9.9,

Figure 9.9 suggests that the volume of this type of inductor is propor-

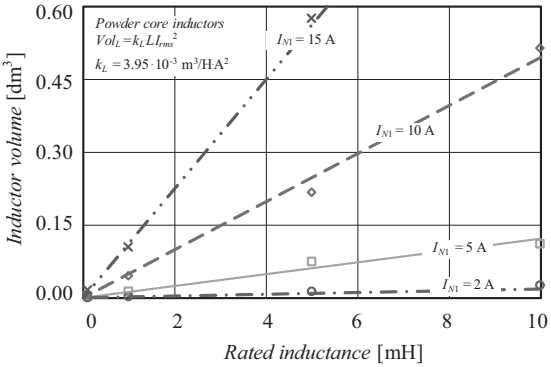


Figure 9.9: Volume of filter inductors employing High Flux toroidal cores in dependency of current and inductance value. Also shown is the volumetric coefficient for these inductors.

tional to its stored energy, so that,

$$Vol_{L,i} = k_L \cdot L_{DM,i} \cdot I_{N1}^2 \tag{9.9}$$

9.2.3 Volume Estimation for Filter Capacitors

CM Capacitors

Equipment safety regulations play an important role, since they restrain the allowable earth leakage current, define requirements for capacitors between an input line and PE, and; define insulation requirements for CM inductors and filter construction.

Earth leakage current $I_{PE,rms,\max}$ is typically limited to 3.5 mA, especially for the case where one of the phases is lost. Thus, the total capacitance $C_{CM,sum} = \sum C_{CM,i}$, i=1...3, between any of the input phases and the PE is bounded to a maximum of approximately,

$$C_{CM,sum} \leqslant \frac{I_{PE,rms,\max}}{1.1 \cdot U_{N1,\max} \cdot 2\pi \cdot 50 \text{ Hz}} \cong 44 \text{ nF}. \tag{9.10}$$

This is a very low value and, therefore, for minimum volume CM filters, the maximum amount of capacitors from phase to PE must be employed.

With this, the only degrees of freedoms are the type of capacitor and how to distribute the total amount between the filter stages.

Safety requires Y2-rated capacitors for connections between phase and PE. Due to these restrictions a series of Y2 ceramic capacitors [160] is chosen, which presents a maximum capacitance of 4.7 nF per SMD package, leading to compact construction and low parasitics. The volume of each SMD unit of this series is approximately $Vol_{Ccm,unit} \cong 52 \cdot 10^{-9}$ m^3. Since other capacitances are present in the circuit (arrestors, stray capacitances, etc) and values present tolerances, some margin is provided so that $C_{CM,sum} = 8 \cdot 4.7$ nF= 37.6 nF, is to be divided into three CM filter stages. According to section 6.7.1, for a maximum attenuation given a minimum total capacitance, each stage shall present the same value. With this,

$$C_{CM,i} = \frac{C_{CM,sum}}{3}. \tag{9.11}$$

Employing eight units of Y2 SMD capacitors per phase leads to a total volume for CM capacitors of,

$$Vol_{Ccm,total} = 8\, Vol_{Ccm,unit} \cong 0.47 \cdot 10^{-6}\,\mathrm{m}^3. \tag{9.12}$$

DM Capacitors

The volume of the capacitors to be used in the filters can be approximated by a curve generated by Minimum Squares regression of the volumes calculated for commercially available X type capacitors (foil [159] and ceramics [160]) as well as for ceramic capacitors rated for the Japanese mains [160]. The computed volume of X-rated capacitors has been plotted in along with approximation curves in Figure 9.10.

Assuming that the volume of the components is directly related to their stored energy, the volume of DM capacitors is defined as in,

$$Vol_{C,i} = k_C \cdot C_{DM,i} \cdot U_{N1}^2. \tag{9.13}$$

The calculated volumetric coefficients for these capacitors are given in Table 9.1. It is observed the much smaller volumetric coefficient for the ceramic type of capacitors, allowing for more compact filters.

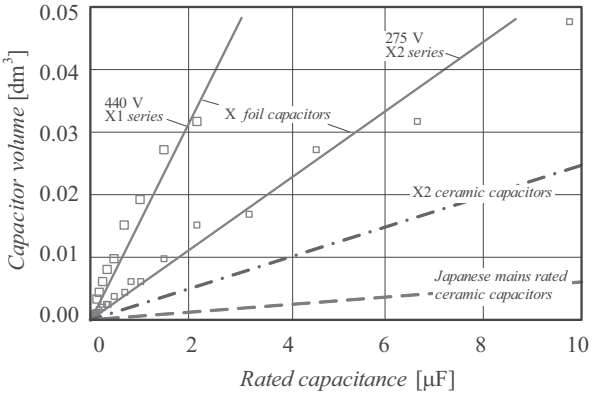


Figure 9.10: Volume and approximation curves for mains rated capacitors.

Table 9.1: Volumetric coefficient for different X capacitor technologies.

Technology	Manufacturer	*Voltage*	k_C
X2 foil	Evox-Rifa	275 V / 400 V	$46.9 \cdot 10^{-6}\ \frac{\mathrm{m}^3}{\mathrm{F \cdot V^2}}$
X2 ceramic	Murata	250 V	$16.4 \cdot 10^{-6}\ \frac{\mathrm{m}^3}{\mathrm{F \cdot V^2}}$
Jap. mains cer.	Murata	250 V	$4.07 \cdot 10^{-6}\ \frac{\mathrm{m}^3}{\mathrm{F \cdot V^2}}$

9.3 Design Procedure for the EMC Filters

The power converter topologies which are considered for this study are presented in Figure 9.11 and Figure 9.12, along with simplified equivalent circuits used for the filter design calculations, where the LISN circuits are replaced by 50 Ω resistors representing the input sensing resistance of a test receiver. It is shown in Figure 9.11 that two-stage filters are considered for a Sparse Matrix Converter (SMC) and in Figure 9.12 three-stage filters are considered for the Vienna Rectifier. For the SMC an output CM choke is included, since the CM voltage at the input terminals of the electric motor must be limited due to CM currents which might cause damage otherwise. The output cable and the machine usually present a high capacitance value to PE when compared to the capacitance between

semiconductors and cooling system. Therefore, for simplicity reasons, this is the only capacitance considered for the SMC filters. The first DM capacitors $C_{DM,1}$ are chosen in order to limit the high frequency ripple of the input voltages of the SMC to $\pm 7.5\%$ of the peak input RMS voltage. For the Vienna rectifier the boost inductors L_{boost} are also considered as part of the filters, although their design is done based on the limitation of the input current ripple to 10% of the peak current and the used materials are high performance ferrites.

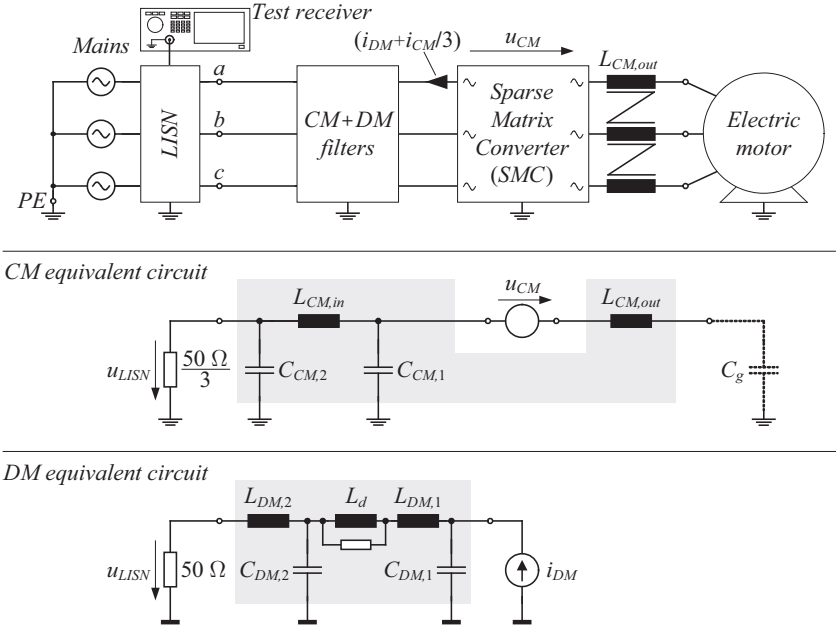


Figure 9.11: Considered converter, filter topologies and simplified equivalent circuits for a Sparse Matrix Converter.

The starting point for the filter design is the estimation of the frequency spectrum for DM voltages and currents and CM voltages, which is compared to the desired limits at the frequency of interest $f = \omega/(2\pi)$, which is 150 kHz for switching frequencies lower than 150 kHz or the switching frequency for higher frequencies. This leads to a required attenuation Att_{req} at the frequency of interest.

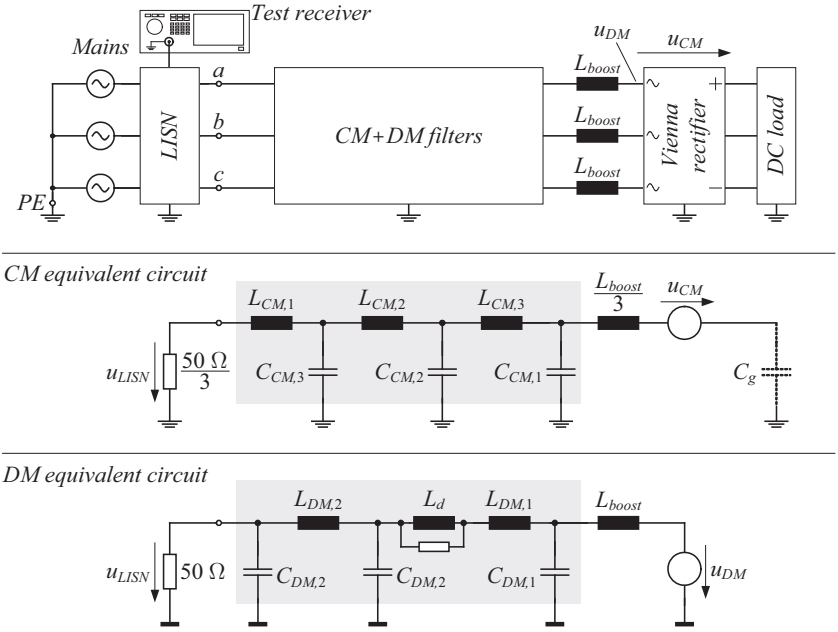


Figure 9.12: Considered converter, filter topologies and simplified equivalent circuits for a Vienna Rectifier.

The EMC filters are based on the design of high performance differential mode and common mode filters, which lead to the fulfillment of the conducted emissions (CE) requirements for Class B equipments in the frequency range of 150 kHz to 30 MHz from CISPR 11 [105]. The limits taken into consideration for all designs here performed is actually 6 dB lower as displayed in Figure 9.13.

The design is based on the calculation of filter component values which lead to minimum volume filters based on a series of constraints as explained in the previous sections.

A series of simplifications are done in order to keep a reasonable calculation effort, namely:

i. accurate calculation of the harmonic contents of the switched voltages of the power converters is replaced by simplified envelopes, which are

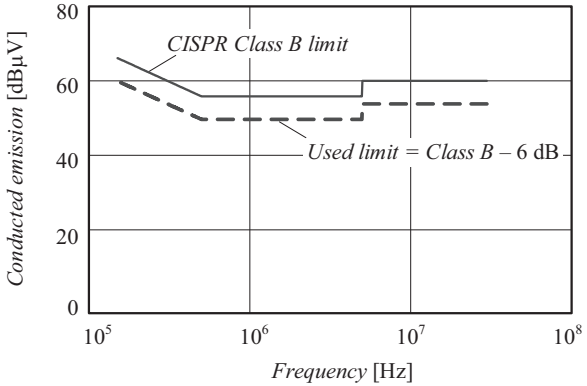


Figure 9.13: Conducted emissions limit used in this work equals the CISPR class B minus 6 dB.

functions of topology, modulation index and switching frequency, and which do not consider the influence of parasitics and rise and fall times. Furthermore,

ii. the circuits are considered symmetric regarding the three-phases, so that single-phase equivalents are used;

iii. parasitics, inter-component couplings and the effects of the tolerances of the designed filter components are neglected for attenuation calculation;

iv. parasitics inside the power converters are neglected, except for the capacitances to ground (PE), which are responsible for CM paths and are lumped into one capacitance C_g which is summed to any load capacitances to PE;

v. effects of internal power supplies and gate drive circuits are neglected;

vi. values of components and cores are linearized.

The empirically derived expressions (cf. 3.5) for the envelope functions for the Sparse Matrix Converter are given by,

$$\varsigma_{i_{DM,SMC}}(f) = \begin{cases} \frac{1}{2\sqrt{2}} \left| \frac{I_{2,peak}\, M}{1+j\,\pi\, M \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } f \leq f_s \\ \frac{1}{2} \left| \frac{I_{2,peak}\, M}{1+j\,\pi\, M \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } f_s < f \leq 6f_s \\ \frac{1}{2\sqrt{2}} \left| \frac{I_{2,peak}\, M}{1+j\,\pi\, M \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } 6f_s < f \end{cases}, \tag{9.14}$$

for the DM equivalent current source and by,

$$\varsigma_{u_{CM,SMC}}(f) = \begin{cases} \frac{1}{\sqrt{6}} \left| \frac{U_{N1}\, M}{1+j\,\pi\, M \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } f \leq f_s \\ \frac{2}{\sqrt{6}} \left| \frac{U_{N1}\, M}{1+j\,\pi\, M \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } f_s < f \leq 6f_s \\ \frac{1}{\sqrt{6}} \left| \frac{U_{N1}\, M}{1+j\,\pi\, M \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } 6f_s < f \end{cases}, \tag{9.15}$$

for the CM equivalent voltage source.

The envelope functions (cf. 3.4) for the Vienna Rectifier are defined by,

$$\varsigma_{u_{DM,VR}}(f) = \begin{cases} \left| \frac{U_o\, M}{1+j\,\pi\, M \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } f \leq f_s \\ \frac{2}{\sqrt{6}} \left| \frac{U_o\, M}{1+j\,\pi\, M \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } f_s < f \leq 6f_s \\ \frac{1}{\sqrt{6}} \left| \frac{I_{2,peak}\, M}{1+j\,\pi\, M \mathrm{ceil}\left(\frac{f}{f_s}\right)} \right|, & \text{if } 6f_s < f \end{cases}, \tag{9.16}$$

for the DM equivalent voltage source and by,

$$\varsigma_{u_{CM,VR}}(f) = \begin{cases} 2\sqrt{2}\left|\frac{U_o\, M}{1+j\,\pi\, M\mathrm{ceil}\left(\frac{f}{f_s}\right)}\right|, & \text{if } f \le f_s \\ 4\sqrt{2}\left|\frac{U_o\, M}{1+j\,\pi\, M\mathrm{ceil}\left(\frac{f}{f_s}\right)}\right|, & \text{if } f_s < f \le 6f_s \\ \frac{3}{\sqrt{2}}\left|\frac{U_o\, M}{1+j\,\pi\, M\mathrm{ceil}\left(\frac{f}{f_s}\right)}\right|, & \text{if } 6f_s < f \end{cases}, \tag{9.17}$$

for the CM equivalent voltage source.

DM Filter Design

In order to guarantee that the designed filters are of minimum volume the desired component values can be derived as functions of two equations, namely the required attenuation at a given frequency and the total volume, which is to be minimized. Here, the main assumptions are: (*i*) the inductors are designed for their low frequency RMS current; (*ii*) the parasitics of the components do not influence the attenuation at the relevant frequency; and, (*iii*) the boost inductor is not included in the analysis and has its value defined by current ripple requirements.

In order to simplify the problem the asymptotic approximation of the attenuation *Att* is used for a LC filter, which leads to an equation of this type,

$$Att(\omega) = \frac{1}{\omega^{2\cdot N} \cdot \prod_{j=1}^{N} L_j \cdot \prod_{j=1}^{N} C_j}. \tag{9.18}$$

It has been proven in section 6.7.1 that, for the smallest total inductance, each of the individual inductors must have the same value and the same is valid for the capacitors. Based on that, only two variables are left to minimize the volume. Let us consider only the case of a single LC stage, which shows the basic principle of minimizing a filter's volume. The required attenuation Att_{req} equation can be further simplified to,

$$Att_{req} = \frac{k_{att}}{L \cdot C}, \tag{9.19}$$

where,

$$k_{att} = \frac{1}{\omega^2}. \tag{9.20}$$

The second equation for the minimization problem is the total volume of the filter, which is the sum of the volume of the inductor with the one of the capacitor,

$$Vol_{filt} = Vol_L + Vol_C. \tag{9.21}$$

It can be assumed the volume of this type of components is directly related to their stored energy, so that volumetric coefficients for inductors k_L and capacitors k_C are defined by the relation between the volumes of such components to their rated storage energy,

$$Vol_L = k_L \cdot L \cdot I_{nom}^2 \tag{9.22}$$

$$Vol_C = k_C \cdot C \cdot U_{nom}^2 \tag{9.23}$$

It follows that,

$$Vol_{filt} = k_L \cdot L \cdot I_{nom}^2 + k_C \cdot C \cdot U_{nom}^2. \tag{9.24}$$

Isolating L leads to,

$$Vol_{filt} = k_L \cdot L \cdot I_{nom}^2 + k_C \cdot \frac{k_{att}}{L \cdot Att_{req}} \cdot U_{nom}^2. \tag{9.25}$$

By differentiating eq. (9.25) with respect to L the minimum volume point can be found and the values for the components are finally defined by,

$$L = \frac{U_{nom}}{\omega \cdot I_{nom}} \sqrt{\frac{k_C}{k_L \cdot Att_{req}}} \tag{9.26}$$

$$C = \frac{I_{nom}}{\omega \cdot U_{nom}} \sqrt{\frac{k_L}{k_C \cdot Att_{req}}}. \tag{9.27}$$

The same procedure can be extended to multi-stage filters. Thus, minimal volume filters can be designed based on the ratings of the components and their volumetric coefficients.

Requirements related to control issues must be considered. In order to provide sufficient passive damping causing minimum losses and avoiding oscillations, also for no-load operation, RL networks are included in the choice of the topologies. These networks are used for damping resonant frequencies introduced by the filter components and the uncertainties in the mains impedance, which could shift given resonances or introduce new resonant circuits with low damping. For simplicity reasons the influence of the RL damping networks in the attenuation is neglected and the inductors L_d are considered to have the same volume as inductors $L_{DM,1}$.

Regarding the DM spectra of emissions, the SMC is considered as a current source i_{DM} (Fig.2(a)), while the Vienna Rectifier is treated as a voltage source u_{DM} due to their inherent shaping of the currents and voltages waveforms.

CM Filter Design

For the design of the CM filters the converters are considered as voltage sources u_{CM}, which are dependent on modulation, input and output voltages and switching frequencies. The CM filter of the SMC is split into an output CM choke and a two-stage CM filter at the input. The aim of the output choke is to keep the CM RMS voltage at the input terminals of the motor lower than 15 V for any switching frequency and capacitances to ground C_g. The remaining components are responsible for providing the total required attenuation.

Two types of components are considered for the CM filters: ceramic capacitors which are Y2-rated [160] and CM chokes which are designed based on toroidal nanocrystalline cores VITROPERM 500F [173], which are "state-of-the-art" in their classes. An earth leakage current limitation of 3.5 mA is considered and this bounds the total capacitance per phase to approximately 40 nF at 50 Hz, which is reduced to 30 nF per phase and evenly distributed among the filter stages.

9.4 Sparse Matrix Converters Power Density Limits

With the given volume minimization procedures for CM and DM filters the impact of the filter volume in the maximum achievable power density as a function of the switching frequency is calculated and an optimum frequency can be estimated, aiming for maximizing overall power density.

An Indirect Matrix Converter topology is assumed, where the power semiconductors are considered to be formed by four SiC JFETs rated for 1200 V, 6 A and having a channel resistance of 0.5 Ω. These are considered in order to reduce switching losses to the minimum allowed with state-of-the-art semiconductors [264]. The calculated power losses as a function of switching frequency are shown in Figure 9.14.

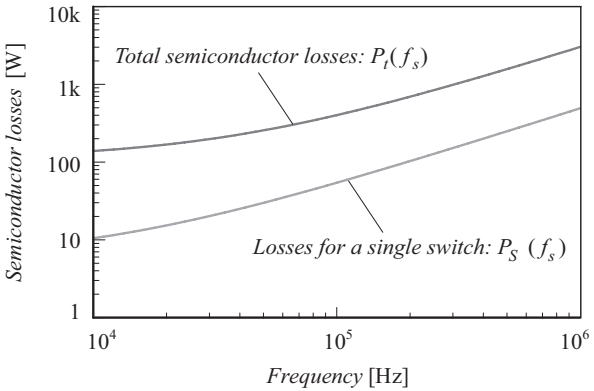


Figure 9.14: Calculated semiconductor losses for a 5 kVA IMC with SiC JFETs.

The total losses and the thermal limits for the SiC JFETs define a required thermal resistance for the cooling system. This is computed here with the total thermal resistance between the heatsink and the ambient $R_{th,sa}$,

$$R_{th,sa}(f_s) \leqslant \frac{T_j - T_a}{P_t(f_s)} - \frac{P_S(f_s)\, R_{th,jc}}{P_t(f_s)} - R_{th,cs}, \tag{9.28}$$

where T_j is the maximum allowable junction temperature, T_a is the am-

bient temperature, $R_{th,jc}$ is the thermal resistance between junction and case for the paralleled JFETs and $R_{th,cs}$ is the thermal resistance between the JFETs' case and the heatsink.

The parameters adopted in this calculation are:

$$T_j = 125\,^{\circ}\mathrm{C}$$
$$T_a = 45\,^{\circ}\mathrm{C}$$
$$R_{th,jc} = 1.2\,\mathrm{K/W}.$$

Assuming that the thermal resistance between the semiconductors and the heatsink can be neglected, i.e. $R_{th,cs} = 0\,\mathrm{K/W}$, the required thermal resistance for the cooling system of the IMC is estimated as in Figure 9.15.

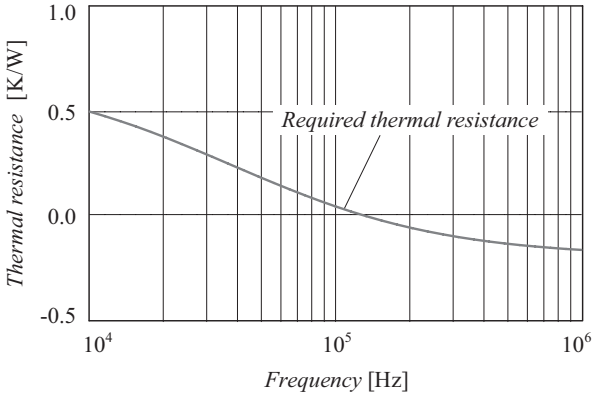


Figure 9.15: Maximum thermal resistance required for the cooling system for the SiC JFET based IMC.

Figure 9.15 shows that switching frequencies higher than approximately 120 kHz are not practical for the given set of semiconductors, since negative thermal resistances are required. That means that active cooling would have to be employed for this condition.

From the required thermal resistance, it is possible to estimate the volume for an optimized forced air cooling systems based on [265]. For the calculations, a coefficient $CSPI = 25\ \mathrm{W/K^{-1}liter^{-1}}$ [265] is used, leading to a total volume of the cooling system Vol_{hs} given by,

$$Vol_{hs}(f_s) \geqslant \frac{1}{CSPI \cdot R_{th,sa}(f_s)}. \tag{9.29}$$

The volume of the various filter components can be derived as functions of the converter ratings, switching frequency and total capacitance to ground C_g. This is of high importance since optimum switching frequencies can be chosen minimizing the total converter volume.

The design of the input CM inductor is dependent on the output CM inductor as well. It is here considered that the output CM inductor keeps the CM voltage across the load machine below $U_{out,\max} = 15$ V RMS. With this, the required impedance for the output CM inductor can be estimated with,

$$Z_{Lcm,out}(f_s) \geqslant \frac{U_p(f_s)}{2\,\pi\,f_s\,C_g\,\sqrt{2}\,U_{out,\max)}}, \tag{9.30}$$

where $U_p(f_s)$ is the first harmonic peak voltage at the switching frequency.

The input CM inductor can have its required impedance estimated based on the required attenuation to achieve compliance with CISPR 11 Class B limits. This leads to an inductor with the volume presented in Figure 9.16, where it is observed that the design of the inductor is divided

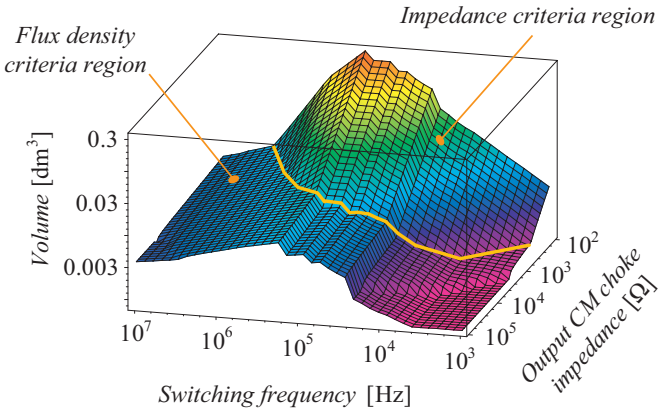


Figure 9.16: Volume of the input CM inductor $L_{CM,1}$ as a function of the

in two regions. In the first region the inductor is designed according to the required impedance only and, for the frequency range from 150 kHz to approximately 1 MHz and low output CM choke impedance, this leads to a fast decrease characteristic ($\cong -20$ dB/decade) regarding higher switching frequencies and the increase of the output inductor impedance. Whereas, in the second region, the volume of the inductor is defined by the maximum flux density allowed in order to keep core losses under control. It is seen that in the second region, for frequencies above 150 kHz, the volume of the inductor presents a slower reduction of the volume with increasing switching frequency and output inductor impedance. This characteristic prevents a large reduction of the volume of the components of CM filters with frequency and identifies that the performance of the state-of-the-art core materials for CM inductors must improve if higher switching frequencies are to be employed in three-phase PWM converters.

The total volume of the components of the EMC filters for a 5 kVA Indirect Matrix Converter is displayed in Figure 9.17 along with the contributions of the DM and CM filter volumes as well as the volume of the first DM capacitors $C_{DM,1}$ for a specific value of capacitance to ground of $C_g = 20$ nF. The volume of an optimized cooling system is also included, which is based on the previous considerations, from where an optimum switching frequency can be derived.

From Figure 9.17 it is observed that the DM filters dominate the filters volume for lower switching frequencies and that the CM filters volume are highly dependent on the capacitance to ground. The increased volume of the CM filter for low switching frequencies in Figure 9.17 is a result of the lower required output CM choke, resulting in the increase of the input sided components. This happens because the choke which is placed between the Matrix Converter and its load has the function to prevent high RMS CM currents to flow in the load, and for low switching frequencies the output choke has a very small value and the filtering effort must be taken by the input filter alone. An increased total volume is seen at 150 kHz due to the CE requirements and the necessity of filtering low order switching frequency harmonics. Furthermore, the total volumes of the DM and CM filters for the Sparse Matrix Converter implemented and analyzed in section 8.5.2 are shown as the implemented filters. It is observed that the DM filter is approximately 29% larger than the prediction and that the CM filter is 14% smaller. These figures are within the expected variation range, since many simplifying assumptions have been taken.

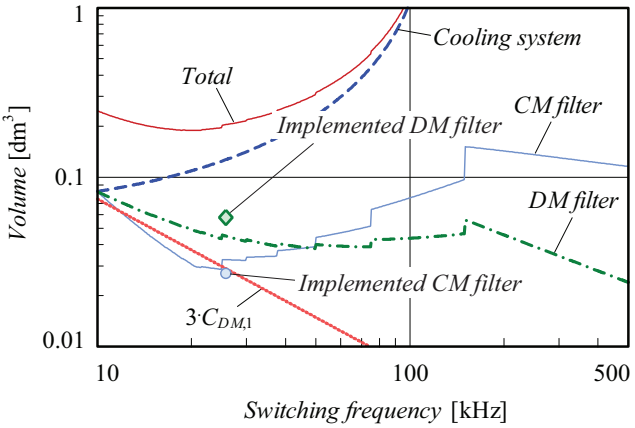


Figure 9.17: The total and partial volumes of the EMC filters for an IMC rated for 230 V RMS phase voltage, modulation index $M = 0.7$, mains frequency 50 Hz, output power $S_2 = 5$ kVA and X2-rated ceramic capacitors for a capacitance to ground $C_g = 20$ nF.

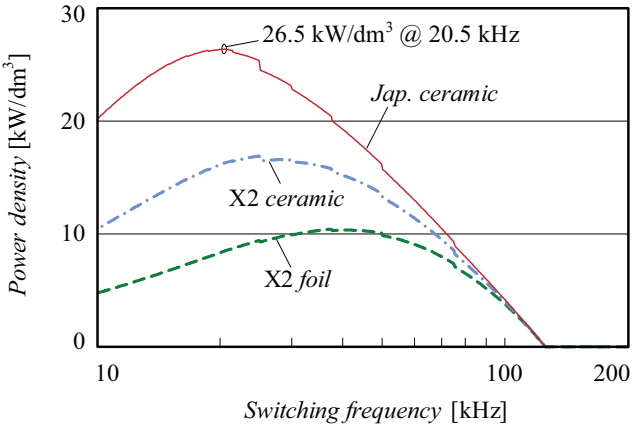


Figure 9.18: Power density limits for three different capacitor technologies as a function of the switching frequency considering only the EMC for a 5 kVA Sparse Matrix Converter.

Taking the results shown in Figure 9.17 it is possible to derive power density limit curves as a function of the switching frequency. This is done in Figure 9.18 for three different capacitor technologies. Since the power semiconductor losses reduce the achievable power density for higher switching frequencies, it is seen that a power density limit of 26.5 kW/liter is achieved with ceramic capacitors rated for the Japanese mains at a switching frequency of 20 kHz. This frequency is around 26 kHz and 41 kHz for the other capacitor technologies, but at much lower power densities. This shows the importance of the improvement of passive components technology for increasing power density.

9.5 Vienna Rectifier Power Density Limits

The same type of calculations are made for a 10 kW Vienna rectifier leading to the results discussed in the following.

Considering the empirically approximated voltage spectra envelopes, the conducted emissions requirements for CISPR 22 Class B and design procedures presented in the previous sections, all filter parameters can be defined as a function of the switching frequency f_s and of the total capacitance C_g to PE.

The first design step for the CM filter is to equally distribute the CM inductors among the stages in the same way that the Y-capacitors are distributed. If this is done, the required impedance for inductors $L_{CM,i}$ with $i = 1..3$ is given by the surface shown in Figure 9.19. It is seen that the required impedances are highly dependent on the capacitance to PE C_g. The characteristic of the curve changes completely for capacitance values higher or lower than some nanofarads. If C_g is much lower than 1 nF, then the impedance increases up to 150 kHz and then decreases. For high values of capacitance, the required impedances are very high for low switching frequencies and drops off rapidly with higher frequencies. This characteristics show the importance of the correct estimation of the stray capacitances in a PWM converter.

However, the first inductor is typically subjected to higher HF voltage amplitudes. This leads to larger $L_{CM,1}$, so that the second and third inductors can be smaller in volume and, most of the times, in impedance as well.

Following the aforementioned considerations leads to the total volume

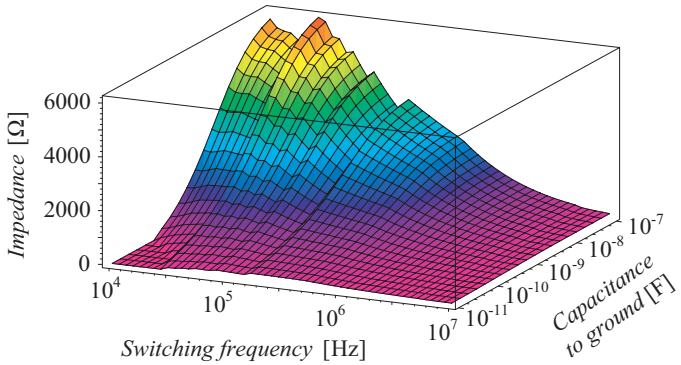


Figure 9.19: Required impedance for the CM inductors $L_{CM,i}$, with $i = 1..3$, if these are equally distributed among three LC stages.

of the CM filter components as shown in Figure 9.20.

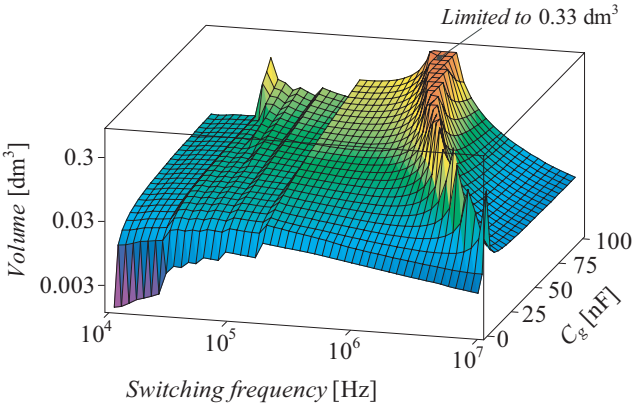


Figure 9.20: CM filter volume in dependency of C_g and f_s.

It is observed in Figure 9.20 that for capacitances C_g lower than approximately 20 nF, the volume of the CM filter increases for switching frequencies up to 150 kHz. This is expected, since the order of the harmonic components which are to be filtered decrease with f_s, and at 150 kHz the first harmonic would have to be filtered. It is seen that small

values of capacitance to PE strongly help to reduce the CM emissions. Another observation is made on the peak which goes from 10 MHz to 1 MHz with increasing value of capacitance C_g. This peak is due to a resonance between the boost inductors and C_g, which is responsible for the strong increase in the voltage across the first CM inductor $L_{CM,1}$ and a consequent enlargement of this inductor.

The total volume of the differential mode filter is shown in Figure 9.21 as a function of the converter's modulation index M and of the switching frequency f_s.

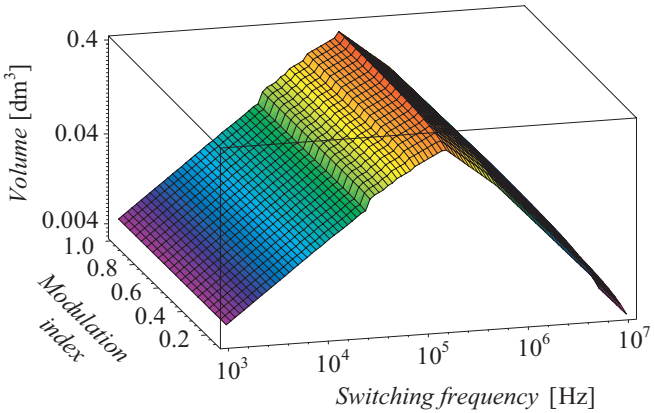


Figure 9.21: Estimated volume for the DM filter components for the 10 kW Vienna Rectifier excluding the input DM capacitors $C_{DM,1}$ and the boost inductors L_{boost}.

Figure 9.21 shows that the maximum volume of these components is found at 150 kHz, which is the frequency where the conducted emission regulations start, so that if the switching frequency is equal to 150 kHz, the first harmonic of the switching frequency must be filtered. For frequencies beyond 150 kHz the volume of the filter components starts to decrease with a ratio of approximately -20 dB per decade. It is observed that, in order to achieve the same volume as for a 20 kHz switching frequency, a higher frequency must be chosen higher than approximately 800 kHz. It is also observed in Figure 9.21 that the volume of the filters does not significantly change with modulation index.

For the designed rectifier [131], a custom designed power module is

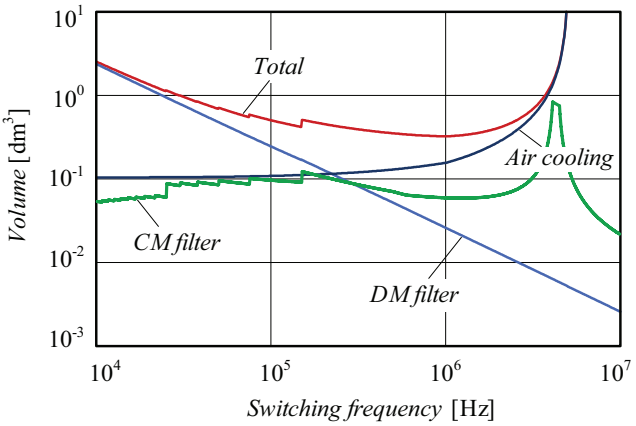


Figure 9.22: Volume curves for a Vienna Rectifier rated for 230 V RMS phase voltage, 800 V output voltage, output power $P_2 = 10$ kW. Shown are the total and partial volumes of the EMC filters and cooling system for X2-rated ceramic capacitors and $C_g = 2$ nF.

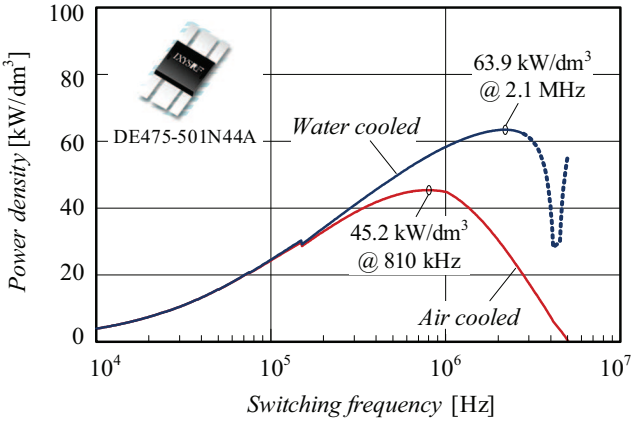


Figure 9.23: Power density limits for two different cooling strategies as a function of the switching frequency considering filters and cooling system of a 10 kW Vienna Rectifier rated for 230 V RMS phase voltage, 800 V output voltage, output power $P_2 = 10$ kW.

employed. The calculated power losses as a function of switching frequency define a required thermal resistance for the cooling system. Based on that, the volume for an optimized forced air cooling systems is estimated [265]. The calculations for the volume of cooling systems are included, based on the considerations of [265]. For the forced air cooling system $CSPI = 25\ \mathrm{W/K^{-1}dm^{-3}}$ is considered. For the water cooled system the dimensions as in [266] are considered. The losses are estimated for a IXYS DE475-501N44A RF MOSFET and 4 paralleled Cree SiC Schottky Diodes (6 A / 600 V) [13] leading to a required thermal resistance from heatsink to ambient in order to limit the junction temperatures to 125°C for an ambient temperature of 45°C. A total capacitance to ground of $C_g = 2$ nF is considered. The DM capacitors are X2-rated ceramics. In Figure 9.22 it is seen that CM filter and cooling system volumes are the main contributors for the total volume and the minimum volume is achieved for a switching frequency around 800 kHz for an air cooled system.

The achievable power densities are presented in Figure 9.23, where it is seen that a water cooled system is capable of further increasing the power density for a frequency of approximately 2 MHz. The curve which shows the power density with water cooling is dashed beyond 1.5 MHz because there is no available information about the feasibility of such small thermal resistances (< 0.1 K/W) given the size of the employed power module. Such low thermal resistances are required if higher frequencies are used and the curve for an air cooled system is shown up to 3 MHz, from where a negative thermal resistance would be required. This means that the semiconductor losses and the thermal resistances which are internal to the power module are physically limiting the possible heat removal with such cooling systems. As a conclusion from such an estimation, it is clear that the main limiting factors for increasing the power density are the materials available for the inductors, the losses generated by the power semiconductors and the available packaging technology.

Considering another set of more conventional power semiconductors (CoolMOS 600 V, 47 A C3 and Cree SiC Schottky Diodes 600 V, 6 A), an analysis is performed for junction temperatures up to 125°C and an ambient temperature of 45°C. A total capacitance to ground of $C_g = 2$ nF is considered. The DM capacitors are X2-rated ceramics. The estimated volumes are depicted in Figure 9.24(a). It is seen that the DM filter (mainly the boost inductors) dominates the volume for low frequencies, whereas

the CM is larger for higher switching frequencies. The increase in the switching losses is responsible for the large increase of the cooling system at high frequencies until it limits the feasibility of the rectifier for requiring negative thermal resistances. Figure 9.24(b) presents the calculated power densities, for just the EMI filter and cooling system also for a water cooled system. A water cooled system is capable of further increasing the power density for high switching frequencies. For an air cooled system the higher power density is calculated as 39.9 kW/dm^3 for $f_s = 540$ kHz.

For this system, the implementation presented in section 6.7 has been carried out and the final volumes for the EMC filters are also included in Figure 9.24. A comparison with the predicted volumes can be made leading to an error of 37% for the DM filter components and 22% for the CM ones. This is considered within the expected range arising from all simplifications made in the prediction procedure. An interesting aspect is that the final boxed volume of the complete filter is approximately 2.4 times larger than the sum of all individual components, meaning that interconnections, air and PCB account for nearly 60% of the employed space. That leaves room for improvements through further research on inter-components coupling reduction, materials and packaging.

9.6 Summary

This chapter has discussed the increase in power density in Power Electronics Systems as one of the main characteristics of such systems. Based on that, the impact of the EMC filters in the achievable power density of three-phase PWM converters has been studied for converters in the range of 5 kW to 10 kW.

A design procedure for the EMC filters has been proposed in order to fulfill CISPR 11 Class B requirements related to conducted emissions for two types of PWM converters, a Sparse Matrix Converter and a three-level/-phase six-switch boost-type rectifier. The design procedure is explained; where a volumetric optimization is carried out taking into consideration different aspects related to the subject, such as electrical safety, power factor and damping of resonances. The presented procedure allows for the analytical calculation of the total filter volume as function of the rated power and switching frequency, therefore helping in the early determination of the optimum switching frequency for a given rectifier specifi-

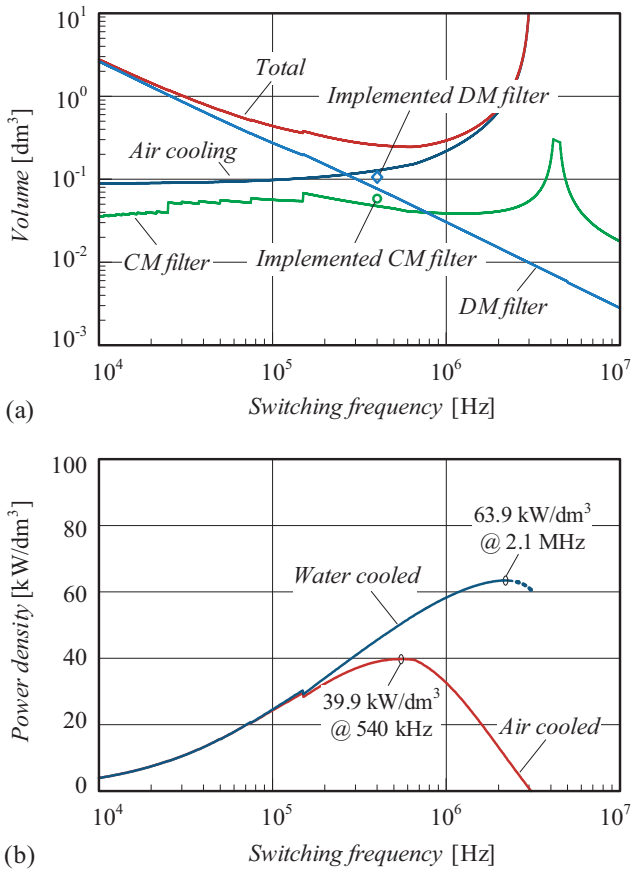


Figure 9.24: EMC filters and cooling system; (a) estimated volume, with the final volume for the designed filters shown, and (b) power density in dependence of the switching frequency. The influence of the volumes of the CM and DM filter components, including the boost inductors and of the forced air cooling devices (fans and heatsink) is observed in the curves. The curves are generated for a total capacitance to ground of 2 nF. A curve for a possible water cooled system is added.

cation. A discussion about the limits of power density for the considered three-phase PWM converters for state-of-the-art power semiconductors is done and optimum switching frequency are identified for an optimized forced air-cooled system and for an water cooled three-level/-phase six-switch boost-type rectifier.

The experimental verification of the proposed filter design procedure is limited to two examples, one for each PWM converter. A total error in the volume prediction of 37% (VR) / 29% (SMC) for the DM filter components and 22% (VR) / 14% (SMC) for the CM ones has been observed. This is considered within the expected range arising from all simplifications made in the prediction procedure.

The performed study shows the importance of optimizing the construction of Power Electronics Systems and highlights some important points for the further increase in power density. Research efforts are required in the fields of magnetic materials, capacitors technology, packaging and integration of the components, while the effects of the 3-D geometries must be considered in order not to influence filtering performance.

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