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Closed-Loop IGBT Gate Drive and Current Balancing Concepts

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*For my parents
Ursula and Fredy*

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Kurzfassung

IGBT Leistungshalbleiter finden aufgrund ihrer hohen Spannungsfestigkeit von bis zu 6.5 kV und ihrer hohen Stromtragfähigkeit von bis zu 3.6 kA eine breite industrielle Anwendung im Nieder- und Mittelspannungsbereich, wie z.B. bei der Netzeinspeisung erneuerbarer Energien, in drehzahlvariablen Antriebssystemen oder bei unterbrechungsfreien Stromversorgungen.

Die schnellen Schalttransienten moderner IGBTs ermöglichen die Realisierung von Umrichtersystemen mit hoher Effizienz und geringem Bauvolumen. Dabei stellen die hohen Strom- und Spannungsänderungsraten bzw. die daraus resultierenden elektromagnetischen Störaussendungen eine Belastung sowohl für die Halbleiter und die Last als auch für die in der Umgebung angeordnete Ansteuer- und Signalelektronik dar, und beeinträchtigen somit die Zuverlässigkeit und Lebensdauer des Gesamtsystems.

Nach einer kurzen Einführung in das charakteristische Schaltverhalten des IGBTs bei induktiver Last in Kapitel 2, wird in Kapitel 3 der dabei entstehende Zielkonflikt zwischen geringen Schaltverlusten und Schaltverzögerungszeiten, Überströmen und Überspannungen als auch leitungsgebundener und abgestrahlter elektromagnetischer Störaussendungen bei konventioneller, resistiver Ansteuerung von IGBTs aufgezeigt.

Ausgehend von einer Untersuchung aktueller Implementierungen zur Beeinflussung und Optimierung des IGBT Schaltverhaltens in Kapitel 4, wird in Kapitel 5 eine IGBT Ansteuerschaltung mit einer hochdynamischen Regelung der Strom- und Spannungsänderungsraten, di_C/dt und dv_{CE}/dt , unter Verwendung eines einzelnen analogen PI-Reglers vorgeschlagen. Dieses neue Regelungskonzept ermöglicht ein definiertes Schaltverhalten des IGBTs entsprechend vorgegebener Sollwerte weitgehend unabhängig von dessen Nichtlinearitäten und Parameterabhängigkeiten. Diese Grundvoraussetzung erlaubt es, das Schaltverhalten hinsichtlich der Schaltverluste und der elektromagnetischen Störaussendungen zu optimieren und somit den vorherrschenden Zielkonflikt bei konventioneller Ansteuerung weitestgehend zu entschärfen. Im Zuge einer Stabilitätsanalyse, welche auf regelungstechnischen Modellen der Ansteuerschaltung und des IGBTs basiert, werden für verschiedene IGBT Module der 1.2 kV Klasse mit Nennstromwerten von 400 – 450 A die Grenzen des vorgeschlagenen Regelungskonzepts aufgezeigt.

In Kapitel 6 wird das Konzept der di_C/dt und dv_{CE}/dt Regelung in eine vollwertige Ansteuerschaltung für IGBTs in Brücken-zweigstrukturen, wie z.B. für den Wechselrichterbetrieb benötigt, überführt. Dabei wird neben der Verhinderung eines Brückenschlusses mittels gegenseitiger Verriegelung der Ansteuerungen der Brücken-zweigtransistoren die Totzeit und somit die Ausgangsspannungsverzerrung minimiert. Die fortwährende Überwachung und sichere Abschaltung verschiedener Arten von lastseitigen Kurzschlüssen runden die Überlegungen zur Ansteuerschaltung ab.

Eine weitere dezentrale Regelungsmöglichkeit, welche die symmetrische Stromaufteilung zwischen parallelgeschalteten IGBT Modulen mittels durch die Ansteuerschaltung dynamisch und individuell angepasster Ein- und Ausschaltzeiten sicherstellt, wird in Kapitel 7 vorgestellt. Damit kann die sonst zur Einhaltung einer Sicherheitsmarge für Asymmetrien erforderliche Herabsetzung der Stromausnutzung der IGBTs bei Parallelschaltung entfallen bzw. die maximal mögliche Ausnutzung der Halbleiter sichergestellt werden.

Die im Zuge dieser Arbeit vorgeschlagenen Regelkonzepte wurden jeweils in Prototypen der Ansteuerschaltungen realisiert und mittels Doppelpulsverfahren an einem Prüfaufbau experimentell verifiziert.

In Kapitel 8 wird die Arbeit mit einer Zusammenfassung abgeschlossen und ein Ausblick auf zukünftige Forschungsthemen im Bereich der in dieser Arbeit vorgeschlagenen Ansteuerkonzepte gegeben.

Abstract

IGBT power semiconductors are widely employed in industrial low- and medium voltage applications, e.g. in systems feeding renewable energies into the mains, in variable speed drive systems or uninterruptible power supplies, because of their high voltage blocking capability of up to 6.5 kV and high current-carrying capacity of up to 3.6 kA.

The fast switching transients of modern IGBTs enable an implementation of converter systems with high efficiency and small physical volume. In this context, the fast rates of current and voltage changes, and the resulting electromagnetic emissions respectively, are causing stresses on the semiconductors, the load, and the surrounding control and signaling electronics as well. Hence, they negatively impact the reliability and lifetime of the overall system.

After shortly introducing the characteristic switching behavior of the IGBT with an inductive load in Chapter 2, the trade-off between low switching losses and switching delay times, overcurrents and overvoltages, as well as conducted and radiated electromagnetic emissions, which arises with conventional resistive IGBT gate drive circuits, is illustrated in Chapter 3.

Based on the investigation of state-of-the-art gate driver implementations, which enable a control and an optimization of the IGBTs switching behavior, shown in Chapter 4, an IGBT gate drive concept comprising a highly dynamic closed-loop control of the current and voltage time derivatives, i.e. di_C/dt and dv_{CE}/dt , and using only a single analog PI-controller is proposed in Chapter 5. This novel control concept enables a defined switching behavior of the IGBT according to preset reference values largely independent of its nonlinearities and parameter dependencies. Furthermore, it allows to optimize the switching behavior concerning switching losses and electromagnetic emissions, and to consequently mitigate the predominant trade-off which exists with conventional gate drive circuits. In the course of a stability analysis the limits of the proposed control concept are determined for different IGBT modules in the 1.2 kV class with current ratings of 400 – 450 A on the basis of control oriented models of the gate driver and the IGBT.

In Chapter 6, the concept of the di_C/dt and dv_{CE}/dt control is incorporated in a complete gate driver for IGBTs in bridge leg configurations, as e.g. needed for inverter operation. Apart from the prevention of a shoot-through, the dead-time and, thus, the output voltage distortion are thereby minimized by reciprocal interlocking of the bridge leg

transistors' gate drivers. A continuous monitoring and the safe turn-off of different types of short circuits of the load complete the gate driver.

Another local control method, which ensures a symmetric current balancing between IGBT modules connected in parallel by means of dynamically adapting the individual turn-on and turn-off times, is presented in Chapter 7. Thereby, the derating of the IGBTs' current-carrying capacity for parallel connection, otherwise required to maintain a safety margin for asymmetries, can be omitted and, accordingly, the maximum possible utilization of the semiconductors is ensured.

The control concepts presented in the course of this work have been implemented into gate driver prototypes and have been verified experimentally in a test setup by means of double pulse tests.

In Chapter 8, this thesis concludes with a summary and gives an outlook on subjects of future research related to the different gate drive concepts presented in the course of this thesis.

1

Introduction

DUE to the steadily increasing demand for electrical energy all over the world [1], highly efficient and ultra-compact power electronic converter systems, which exhibit a high degree of reliability, are of major importance in nearly all industrial areas [2, 3]. This asks for sustained improvements with regard to the converter topologies, the modulation and control schemes, the passive components, the packaging and the level of integration, and especially the power semiconductors and their associated driving circuits [2, 4, 5].

Nowadays, the Insulated-Gate Bipolar Transistor (IGBT) is typically the power semiconductor of choice for medium-frequency power electronic converters with power ratings from few Kilowatts up to several Megawatts [6]. Its popularity results from the high voltage blocking capability of up to 6.5 kV and its high current-carrying capacity of up to 3.6 kA in combination with comparably low switching, conduction, blocking, and gate drive losses. Figure 1.1 gives an overview on today's application areas of the main semiconductor technologies, i.e. thyristors, IGBTs, MOSFETs, and emerging wide-bandgap power semiconductors based on Silicon Carbide (SiC) or Gallium Nitride (GaN), with respect to the converter's power rating and switching frequency.

The range of the voltage and current ratings of today's IGBTs, cf. Figure 1.2 (a), covers many industries and, thus, IGBTs are widely employed in a great variety of applications. As shown in Figure 1.2 (c), typical fields of application are propulsion converters for traction or industrial variable speed drive systems, the feed-in of renewable energies such as wind power generators or industrial PV grid-tie inverters, or UPS systems to name a few. Depending on the voltage and current rating of the semiconductors, different packages, e.g. discrete devices

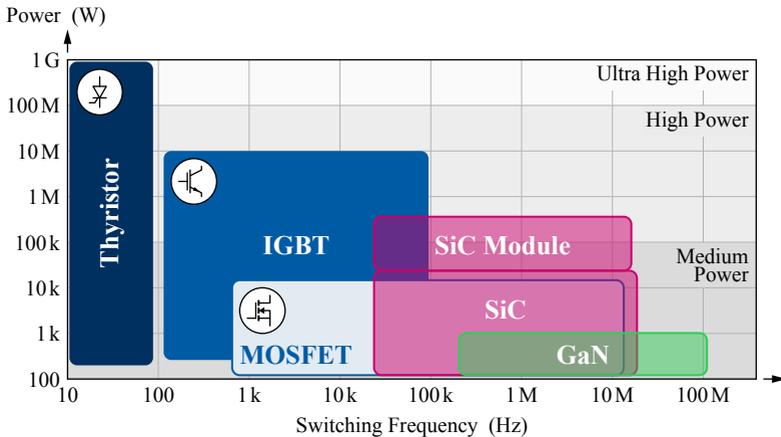


Figure 1.1: (a) Typical application areas of the main semiconductor technologies with respect to the converter power rating and the switching frequency [6].

or modules, are commercially available as exemplary illustrated in Figure 1.2 (b).

In order to attain high efficiency, attempts are made to minimize the switching losses which in many cases significantly contribute to the overall converter losses [8]. As will be detailed in Chapter 2 of this thesis, the dynamic switching behavior of the IGBT and, accordingly, the switching losses can be influenced by the current injected into the gate terminal of the IGBT by means of the gate driver (GD). As a basic principle, low switching losses are achieved by means of fast switching with short intervals of linear operation, i.e. with a short overlap of high voltage and current [9, 10]. In return, the associated fast current and voltage transients are increasing the stresses on the semiconductors and the load due to switching overvoltages or overcurrents, and are negatively impacting the environment due to EMI. This trade-off between slow and fast switching is described in Chapter 3.

In the conventional case of employing a passive push-pull GD, the switching speed of an IGBT is defined by the gate resistor [11, 12]. This resistor needs to be selected in such a way that the aforementioned stresses, which are resulting from the fast rates of current and voltage changes, never exceed the admissible limits. Thereby, all possible op-

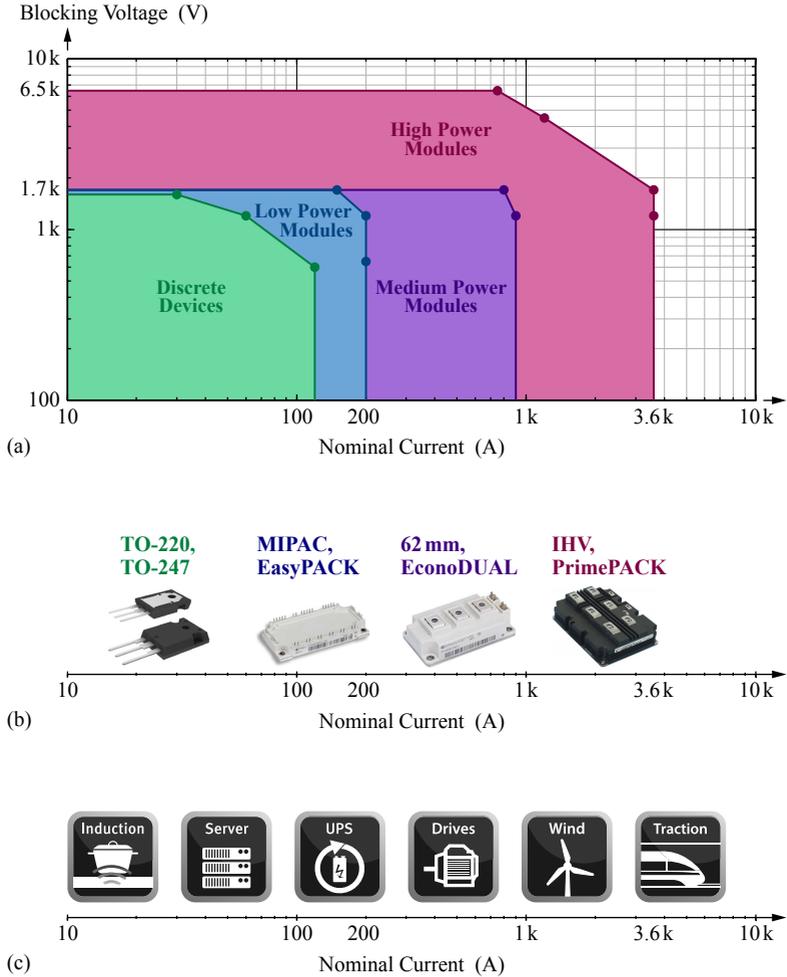


Figure 1.2: (a) Typical maximum voltage / current ratings of today's IGBTs (dots) and subdivision based on packaging; (b) examples of corresponding packages; (c) typical related applications [7].

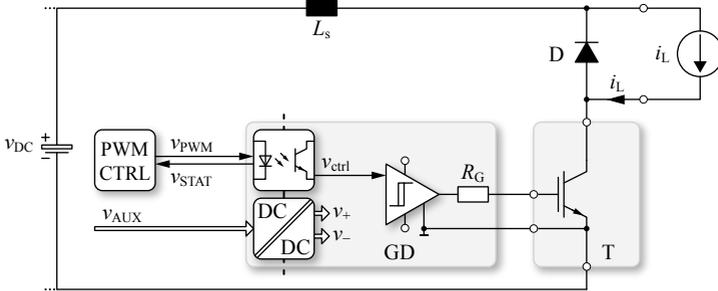


Figure 1.3: Chopper configuration, i.e. series connection of an IGBT and a Free-Wheeling Diode (FWD) to a voltage DC-link with an inductive load; for controlling the IGBT an isolated resistive push-pull GD is employed. The circuit structure is characteristic e.g. for AC/DC PFC rectifiers or unidirectional DC/DC converters such as the conventional buck or boost converters.

erating conditions need to be taken into account, i.e. the worst case conditions of ambient and semiconductor junction temperatures, and the potential levels of the load current and the DC-link voltage must be considered. Accordingly, in normal operation, only a compromise in terms of switching losses, semiconductor overvoltages / overcurrents and EMI is attained and the room for further improvements by means of a passive GD is very limited.

In contrast and as a motivation of this thesis, by means of (dynamically) adapting the gate voltage or current of the IGBT to the actual state of the converter system and the IGBT, the potential for optimizing the switching behavior is significantly increased. In Chapter 4, state-of-the-art gate drive concepts, which enable a control of the current and voltage switching trajectories, are reviewed and their individual advantages and disadvantages are analyzed.

After identifying the limits of state-of-the-art gate drive concepts, in Chapter 5 a high-bandwidth (up to 34.3 MHz) closed-loop di_C/dt and dv_{CE}/dt GD is proposed for chopper configurations, cf. Figure 1.3, which enables a defined switching behavior of the IGBT at inductive load switching, largely independent of its parameter variations and nonlinearities. Furthermore, the proposed gate drive concept is also analyzed regarding stability and is verified experimentally.

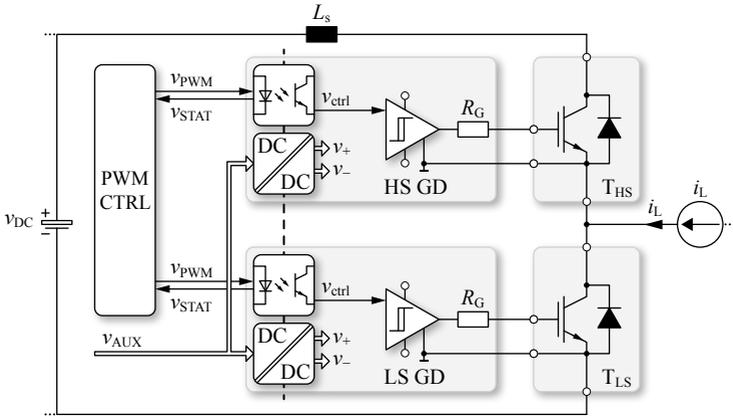


Figure 1.4: Bridge leg arrangement and associated GDs of two IGBT / diode cells connected to an inductive load.

However, in addition to the attainment of a defined, i.e. optimized, and secure switching behavior of the IGBT for all operating conditions, additional challenging GD tasks have to be accomplished for IGBT / diode cells arranged in bridge leg configurations, cf. Figure 1.4, as described in Chapter 6. There, a simultaneous turn-on of both transistors must strictly be avoided, though, the output voltage delay and distortion must be kept minimal. In addition, overall system reliability is gained by means of a short circuit proof output. The proposed closed-loop di_C/dt and dv_{CE}/dt GD is, hence, extended in Chapter 6 in order to fulfill the critical tasks arising at bridge leg configurations and thereby to increase its application area.

Another local control method, which ensures a symmetric current distribution between IGBT modules connected in parallel by means of dynamically adapting the turn-on and turn-off times on the GD, is presented in Chapter 7. Thereby, the conventional derating of the IGBTs' current-carrying capacity at parallel connection can be omitted and the maximum possible utilization of the semiconductors is ensured.

This thesis concludes with a summary and gives an outlook on subjects of future research related to the different presented gate drive concepts.

2

IGBT Switching Behavior for Inductive Load

THIS chapter introduces the basic characteristics of an IGBT and presents appropriate equivalent circuits in order to explain the static and dynamic behavior of the device. Subsequently, its characteristic switching transients occurring at clamped inductive load (hard) switching are described for a buck converter topology. In doing so, the relations between the GD and the corresponding current and voltage waveforms are derived based on the IGBT's equivalent circuit. Furthermore, the effects caused by the stored charges of the power semiconductors, i.e. the diode's reverse recovery current and the IGBT's tail current, as well as the parasitic inductance in the commutation loop are discussed.

2.1 IGBT Equivalent Circuit

The IGBT is a bipolar power semiconductor which is formed by integration of a Bipolar Junction Transistor (BJT) and a gate side Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). A corresponding equivalent circuit is shown in Figure 2.1 (a) [11]. This combination allows to exploit synergies of the two semiconductor technologies, i.e. the high-impedance and low-loss gate control of the MOSFET as well as the low forward voltage drop of the BJT.

The static (DC) characteristics of the IGBT can be described based on the equivalent circuit neglecting the capacitances, cf. Figure 2.1 (b). There, the drain current of the gate-side MOSFET equals the base

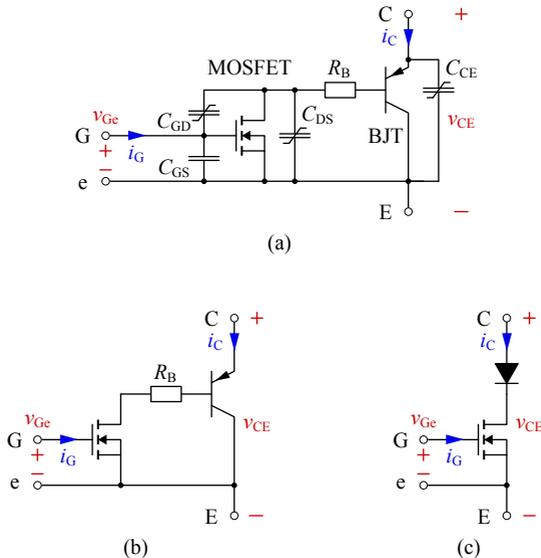


Figure 2.1: (a) Equivalent circuit of the IGBT consisting of a n-channel MOSFET and a pnp BJT. (b) Equivalent circuit for stationary operation and (c) simplified equivalent circuit at saturation [9, 11, 13, 14].

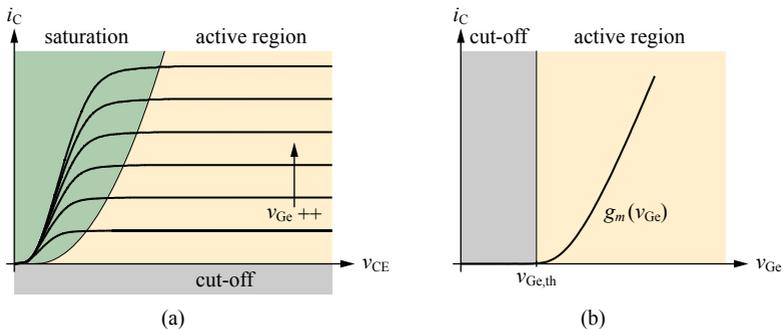


Figure 2.2: (a) Typical IGBT output characteristic. (b) Typical IGBT transfer characteristic determining the transconductance $g_m(v_{ge})$.

current of the BJT, which is why the static behavior of the IGBT is dominated by the MOSFET. The corresponding output characteristic and the transconductance of the IGBT are shown in Figure 2.2 and can be divided into three different regions of operation.

- ▶ **Cut-off** ($v_{Ge} < v_{Ge,th}$)
The MOSFET is turned-off and, hence, no collector current flows.
- ▶ **Active Region** ($v_{Ge} \geq v_{Ge,th}$, $v_{CE} \geq v_{Ge} - v_{Ge,th}$)
The gate voltage controls the drain current of the MOSFET in its active region and it also regulates the collector current via the BJT's current gain, accordingly.
- ▶ **Saturation** ($v_{Ge} \geq v_{Ge,th}$, $v_{CE} < v_{Ge} - v_{Ge,th}$)
Below $v_{CE} \approx 0.6 \dots 0.7 \text{ V}$ the BJT is blocking. Above this voltage, the BJT conducts and, since the MOSFET stays in the ohmic region, i_C increases in dependency of v_{CE} and v_{Ge} .

The transfer characteristic for cut-off and for the active region can be described in accordance to a MOSFET [13–15],

$$i_C = \begin{cases} 0 & v_{Ge} < v_{Ge,th} \\ \frac{1}{1-\alpha_{BJT}} \cdot \frac{K}{2} \cdot (v_{Ge} - v_{Ge,th})^2 & v_{Ge} \geq v_{Ge,th}, v_{CE} \geq v_{Ge} - v_{Ge,th}, \end{cases} \quad (2.1)$$

at which α_{BJT} equals the current gain factor of the BJT and

$$K = \mu_n \cdot C'_{ox} \cdot \frac{w}{l} \quad (2.2)$$

is a transconductance parameter of the MOSFET. μ_n denominates the mobility of the electrons, C'_{ox} corresponds to the capacitance per area of the gate oxide, w is the width, and l is the length of the channel. Finally, for the sake of simplicity, the IGBT's transconductance is typically linearized and the collector current can be expressed as

$$i_C = g_{m,s} \cdot (v_{Ge} - v_{Ge,th}), \quad (2.3)$$

where $g_{m,s}$ relates to the IGBT's linearized transconductance

$$g_{m,s} = \frac{di_C}{dv_{Ge}}. \quad (2.4)$$

In saturation, the equivalent circuit of Figure 2.1 (c) can be assumed and the forward voltage drop of the IGBT can be calculated as

$$v_{\text{CE,sat}} = v_f + r_{\text{D}}(v_{\text{Ge}}) \cdot i_{\text{C}}. \quad (2.5)$$

Here, v_f corresponds to the base voltage drop of the BJT and/or the minimal forward voltage drop of the IGBT and r_{D} is the equivalent linearized on-state resistance.

2.2 Equivalent Circuit for the Switching Transients

The buck converter represents the most simple power electronics converter topology at which hard switching occurs and, accordingly, serves as a basis for the subsequent investigations. Figure 2.3 shows the equivalent circuit at hard switching using the most widespread resistive push-pull GD, which provides either a positive or a (typically) negative GD output voltage, $v_{\text{G}} = v_+$ or $v_{\text{G}} = v_-$. The DC-link voltage v_{DC} and the load current i_{L} , which represents the current impressed by the inductance of the buck converter's LC -output filter, are assumed constant within the period of the switching transients. All the parasitic inductances in the commutation loop, i.e. in the DC-link, the busbars and the IGBT / diode module, are concentrated in the stray inductance L_{s} . Any inductance in the gate loop is neglected for the sake of limiting the complexity.

The IGBT is represented by the terminal capacitances C_{GE} , C_{GC} , and C_{CE} according to Figure 2.1 which in datasheets are typically defined by specification of the following capacitance values,

$$C_{\text{ies}} = C_{\text{GE}} + C_{\text{GC}} \quad (2.6)$$

$$C_{\text{oes}} = C_{\text{GC}} + C_{\text{CE}} \quad (2.7)$$

$$C_{\text{res}} = C_{\text{GC}}. \quad (2.8)$$

The transconductance is modelled according to (2.3).

2.3 Switching Behavior

In the following, the dynamic switching behavior of the IGBT at diode-clamped inductive load is reviewed based on the equivalent circuit of Figure 2.3 for the turn-on and the turn-off transients.

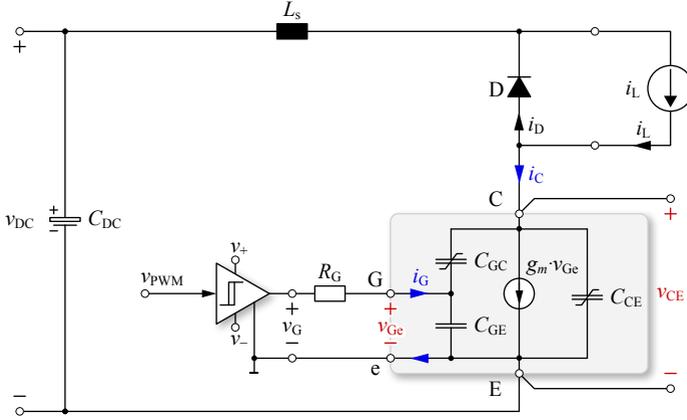


Figure 2.3: Equivalent circuit for diode-clamped inductive load (hard) switching of an IGBT using a resistive push-pull GD. L_s represents the sum of the parasitic inductances of the DC-link, the busbars and the IGBT module, i.e. the commutation loop inductance.

2.3.1 Turn-on

The turn-on describes the commutation of the load current i_L from the complementary freewheeling diode to the IGBT, which is being turned-on, and the transition of the blocking of the DC-link voltage from the IGBT to the diode.

The schematic waveforms of the IGBT at turn-on, i.e. the currents and voltages in the power and in the gate driving path, are shown in Figure 2.4. In this figure, the progress of the operating point in the IGBT output characteristic and in the transfer characteristic is shown as well. The turn-on is subdivided into the characteristic intervals I – VI, represented by the equivalent circuits and current paths shown in Figure 2.5, which are described in the subsequent paragraphs.

I: Off-state ($t < t_0$)

Before being turned-on, it is assumed that the IGBT is completely turned-off and the gate is discharged to the negative gate drive voltage, i.e. $v_{Ge} = v_G = v_-$ and $i_G = 0$. Thereby, the IGBT is not carrying current, i.e. $i_C = 0$, and blocking the full DC-link voltage, i.e. $v_{CE} = v_{DC}$, as shown in Figure 2.4; the impressed load current is freewheeling

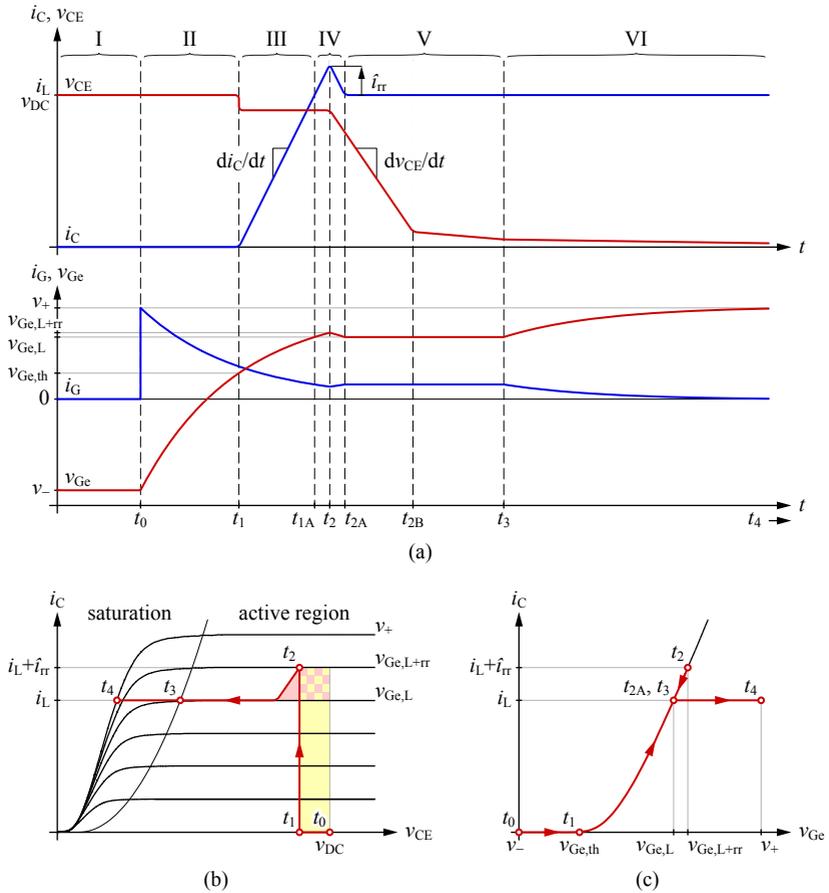


Figure 2.4: Diode-clamped inductive load switching behavior of an IGBT at turn-on. (a) Schematic voltage and current waveforms subdivided into the intervals I – VI. Progress of the operating point (b) in the output characteristic and (c) in the transfer characteristic of the active region.

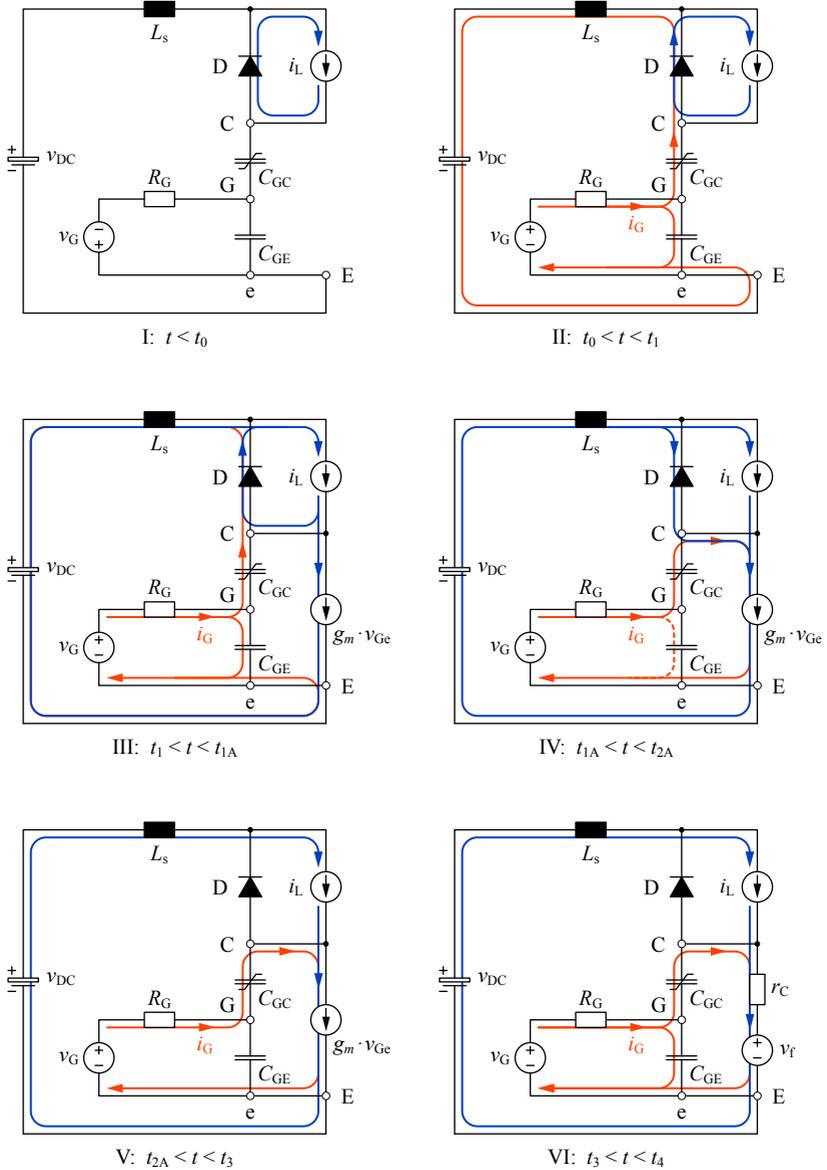


Figure 2.5: Equivalent circuits with associated current paths valid during the different intervals at turn-on, cf. Figure 2.4.

in the complementary diode, cf. Figure 2.5. The forward voltage drop of the diode during conduction and the leakage current of the IGBT in the blocking state are neglected here.

At $t = t_0$, the turn-on is initiated, i.e. the GD sets its output voltage v_G to the constant positive voltage v_+ .

II: Gate charge delay ($t_0 < t < t_1$)

Applying a voltage step from $v_G = v_-$ to $v_G = v_+$ at $t = t_0$ initiates a charging of the IGBT's input capacitance $C_{ies} = C_{GE} + C_{GC}$, i.e. the gate capacitance C_{GE} is charged while the Miller capacitance C_{GC} is discharged. This is due to the clamping of the collector potential to the positive DC-link rail by the freewheeling diode.

Using a resistive GD, this process describes the charging of a RC -circuit and, accordingly, the gate voltage v_{Ge} rises starting from v_- ,

$$v_{Ge}(t) = v_- + \Delta v_G \cdot \left(1 - e^{-(t-t_0)/\tau_{G,S}}\right). \quad (2.9)$$

There,

$$\Delta v_G = v_+ - v_- \quad (2.10)$$

equals the difference between the positive and the negative gate drive output voltages and

$$\tau_{G,S} = R_G \cdot C_{ies} = R_G \cdot (C_{GE} + C_{GC,S}) \approx R_G \cdot C_{GE} \quad (2.11)$$

corresponds to the time constant of the charging process for large values of v_{CE} where the Miller capacitance is significantly smaller than C_{GE} as will be shown in Figure 4.5 (b). Accordingly, it can be approximated by a small value denominated $C_{GC,S}$ as shown in Figure 2.7, and is, thus, neglected here. While the gate voltage rises, the gate current first performs a step to its maximum value and then starts to decay,

$$i_G(t) = \frac{v_+ - v_{Ge}(t)}{R_G} = \frac{\Delta v_G}{R_G} \cdot e^{-(t-t_0)/\tau_{G,S}}. \quad (2.12)$$

The IGBT is blocking as long as v_{Ge} stays below the threshold voltage $v_{Ge,th}$. The turn-on gate charge delay, i.e. the time from initiating the turn-on until the gate voltage reaches $v_{Ge,th}$, can be calculated for the resistive GD as

$$t_{d,gc} = t_1 - t_0 = \tau_{G,S} \cdot \ln \left(\frac{\Delta v_G}{v_+ - v_{Ge,th}} \right). \quad (2.13)$$

As soon as v_{Ge} reaches $v_{\text{Ge,th}}$, the IGBT starts to conduct current according to its transfer and output characteristics.

III: Current rise ($t_1 < t < t_{1A}$)

The charging of the gate as described in interval II continues, i.e. (2.9) and (2.12) remain valid for v_{Ge} and i_{G} , respectively. Since v_{Ge} is now above $v_{\text{Ge,th}}$, the load currents starts to commutate from the freewheeling diode to the IGBT. The collector current is basically defined according to the static transfer characteristic (2.3),

$$i_{\text{C}}(t) = g_{m,s} \cdot (v_{\text{Ge}}(t) - v_{\text{Ge,th}}), \quad (2.14)$$

since the IGBT remains in the active region as shown in Figure 2.4. By differentiating (2.14), the rate of current rise of i_{C} can be calculated as a function of the rate of rise of the gate voltage or the gate current and the input capacitance,

$$\frac{di_{\text{C}}}{dt} = g_{m,s} \cdot \frac{dv_{\text{Ge}}}{dt} = g_{m,s} \cdot \frac{i_{\text{G}}}{C_{\text{ies}}} \approx g_{m,s} \cdot \frac{i_{\text{G}}}{C_{\text{GE}}}. \quad (2.15)$$

Accordingly, the current in the freewheeling diode i_{D} decays at the negative rate of increase of the collector current,

$$\frac{di_{\text{D}}}{dt} = -\frac{di_{\text{C}}}{dt}. \quad (2.16)$$

Since the freewheeling diode keeps conducting current within this interval, the collector potential is clamped to the upper DC-link rail. In order to achieve the desired rate of collector current rise, a voltage drop needs to be applied to the parasitic inductance in the commutation loop and, hence, the voltage over the IGBT is reduced,

$$v_{\text{CE}} = v_{\text{DC}} - L_s \cdot \frac{di_{\text{C}}}{dt}. \quad (2.17)$$

When the collector current reaches the level of the load current i_{L} , the gate voltage according to (2.14) is

$$(v_{\text{Ge}})_{i_{\text{C}}=i_{\text{L}}} = v_{\text{Ge,L}} = v_{\text{Ge,th}} + \frac{i_{\text{L}}}{g_{m,s}}. \quad (2.18)$$

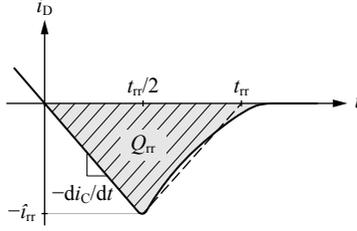


Figure 2.6: Schematic current waveform of a Si-diode during turn-off with a defined rate of change $di_D/dt = -di_C/dt$, assuming a symmetrical triangular-shaped reverse recovery behavior [16]. Q_{rr} equals the diode's stored reverse recovery charge.

IV: Reverse recovery of diode ($t_{1A} < t < t_{2A}$)

At $t = t_{1A}$, the current of the freewheeling diode becomes negative and the diode's charge carriers (stored charge Q_{rr}) are actively removed while the collector current keeps rising. This so called reverse recovery effect is illustrated in Figure 2.6. If a symmetrical triangular-shaped reverse recovery behavior is assumed [16], the reverse recovery charge can be expressed as a function of the reverse recovery time t_{rr} and the peak reverse recovery current \hat{i}_{rr} ,

$$Q_{rr}(T_j) = \frac{t_{rr} \cdot \hat{i}_{rr}}{2}. \quad (2.19)$$

In turn, the peak reverse recovery current can be expressed in dependency of di_C/dt and the reverse recovery time,

$$\hat{i}_{rr} = \frac{t_{rr}}{2} \cdot \frac{di_C}{dt}, \quad (2.20)$$

and the reverse recovery time can be calculated as a function of Q_{rr} and di_C/dt by combining (2.19) and (2.20), which yields

$$t_{rr} = 2 \cdot \sqrt{\frac{Q_{rr}}{di_C/dt}}. \quad (2.21)$$

Finally, the peak reverse recovery current can be calculated as a function of Q_{rr} and di_C/dt by equating (2.20) and using (2.21),

$$\hat{i}_{rr} = \sqrt{Q_{rr} \cdot \frac{di_C}{dt}}. \quad (2.22)$$

As soon as i_C reaches the sum of the load current and the peak reverse recovery current, the diode gains voltage blocking capability and, thus, the IGBT's collector-emitter voltage starts to decay. At that moment, corresponding to (2.14) the gate voltage reaches

$$(v_{Ge})_{i_C=i_L+\hat{i}_{rr}} = v_{Ge,L+rr} = v_{Ge,th} + \frac{i_L + \hat{i}_{rr}}{g_{m,s}}. \quad (2.23)$$

V: Voltage decay ($t_{2A} < t < t_3$)

After the collector current reaches $i_L + \hat{i}_{rr}$, it decays back to the level of the load current, cf. Figure 2.6 and Figure 2.4. Since the IGBT remains in the active operating region and the collector current is basically constant, the gate voltage stays clamped to $v_{Ge,L}$ and corresponds to the value given in (2.18). This constant level of the gate voltage during turn-on and, as will be shown later, also during turn-off is the so-called Miller plateau. Even in the case of employing a resistive GD a constant gate current results in this interval,

$$i_G = \frac{v_+ - v_{Ge,L}}{R_G}. \quad (2.24)$$

Hence, the gate current only discharges C_{GC} and leads to a decay of the collector-emitter voltage,

$$\frac{dv_{CE}}{dt} = -\frac{dv_{GC}}{dt} = -\frac{i_G}{C_{GC,S}}. \quad (2.25)$$

In practice, the Miller capacitance C_{GC} shows a non-linear dependency on the voltage v_{CE} as shown in Figure 2.7. For high values of v_{CE} , the Miller capacitance can be approximated by a small capacitance value $C_{GC,S}$. As soon as v_{CE} reaches values close to v_{Ge} , i.e. at $t = t_{2B}$, C_{GC} increases strongly and dv_{CE}/dt becomes very small. Accordingly, the steep voltage slope does not continue but the Miller capacitance is still discharged with the same gate current and the IGBT remains in the active region of operation. For low values of v_{CE} , the Miller capacitance can be approximated by $C_{GC,L}$ as shown in Figure 2.7.

VI: Gate charge ($t_3 < t < t_4$)

Once the IGBT crosses the boundary from the active region to saturation at $t = t_3$, the gate is no longer clamped and the GD continues the

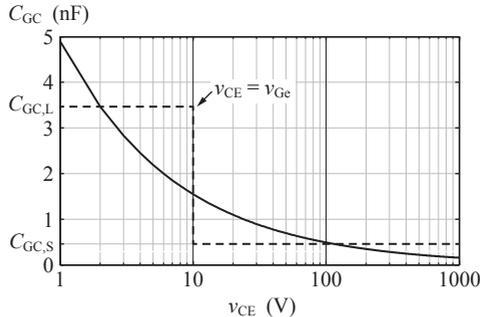


Figure 2.7: Typical voltage dependency of the IGBT’s Miller capacitance C_{GC} (solid line) according to (B.2) and a corresponding approximation (dashed line) with a small capacitance $C_{GC,S}$ for high values of v_{CE} and a large capacitance $C_{GC,L}$ for low values of v_{CE} , respectively [16].

RC -charging of the IGBT’s input capacitance (cf. interval II), starting from $v_{Ge} = v_{Ge,L}$. Now, the time constant is larger than in interval II,

$$\tau_{G,L} = R_G \cdot (C_{Ge} + C_{GC,L}), \quad (2.26)$$

because of the larger Miller capacitance for low values of v_{CE} . In this interval, the forward voltage drop of the IGBT finally reaches the low on-state voltage level while conducting the load current; the complementary freewheeling diode blocks the full DC-link voltage.

2.3.2 Turn-off

The turn-off describes the commutation of the load current i_L from the IGBT to the complementary freewheeling diode and basically reverses the transients occurring during turn-on except for the reverse recovery behavior.

The schematic waveforms of the IGBT at turn-off, i.e. the currents and voltages in the power and in the gate driving path, are shown in Figure 2.8 in a similar way as for the turn-on. In this figure, the progress of the operating point in the output characteristic and in the transfer characteristic is shown as well. The turn-off is subdivided into the intervals VII – XII, which can be represented by the equivalent circuits and current paths shown in Figure 2.9 and are described in the following paragraphs.

VII: On-state ($t < t_5$)

Before turn-off, it is assumed that the IGBT is completely turned-on and the gate is charged to the positive gate drive output voltage, i.e. $v_{Ge} = v_G = v_+$ and $i_G = 0$; the IGBT is carrying the load current, i.e. $i_C = i_L$, and the forward voltage drop is low, i.e. $v_{CE} = (v_{CE,sat})_{i_C=i_L}$, as shown in Figure 2.8. The complementary freewheeling diode is blocking the DC-link voltage and is not carrying any current (a leakage current in the blocking state of the freewheeling diode is neglected here).

At $t = t_5$, the turn-off is initiated, i.e. the GD sets its output voltage v_G to v_- , which is typically negative in order to prevent a parasitic turn-on in the off-state for large values of dv_{CE}/dt as caused by the switching of the complementary transistor in bridge leg configurations, as will be explained in Section 6.1.1.

VIII: Gate discharge delay ($t_5 < t < t_6$)

The mathematical description is similar than for the turn-on interval VI; the IGBT's input capacitance is discharged and the gate voltage becomes

$$v_{Ge}(t) = v_+ - \Delta v_G \cdot \left(1 - e^{-(t-t_5)/\tau_{G,L}}\right). \quad (2.27)$$

While the gate voltage decays, the gate current first performs a step to its maximum negative value and then reduces its amplitude,

$$i_G(t) = \frac{v_- - v_{Ge}(t)}{R_G} = -\frac{\Delta v_G}{R_G} \cdot e^{-(t-t_5)/\tau_{G,L}}. \quad (2.28)$$

At $t = t_6$, the gate voltage reaches the minimum value in order to carry the load current, $v_{Ge,L}$, and the IGBT enters the active region, i.e. the gate voltage gets clamped. This interval determines the turn-off gate discharge delay. For a resistive GD we have

$$t_{d,gd} = t_6 - t_5 = \tau_{G,L} \cdot \ln \left(\frac{\Delta v_G}{v_{Ge,L} - v_-} \right). \quad (2.29)$$

IX: Voltage rise ($t_6 < t < t_7$)

While the gate voltage remains clamped,

$$v_{Ge} = v_{Ge,L}, \quad (2.30)$$

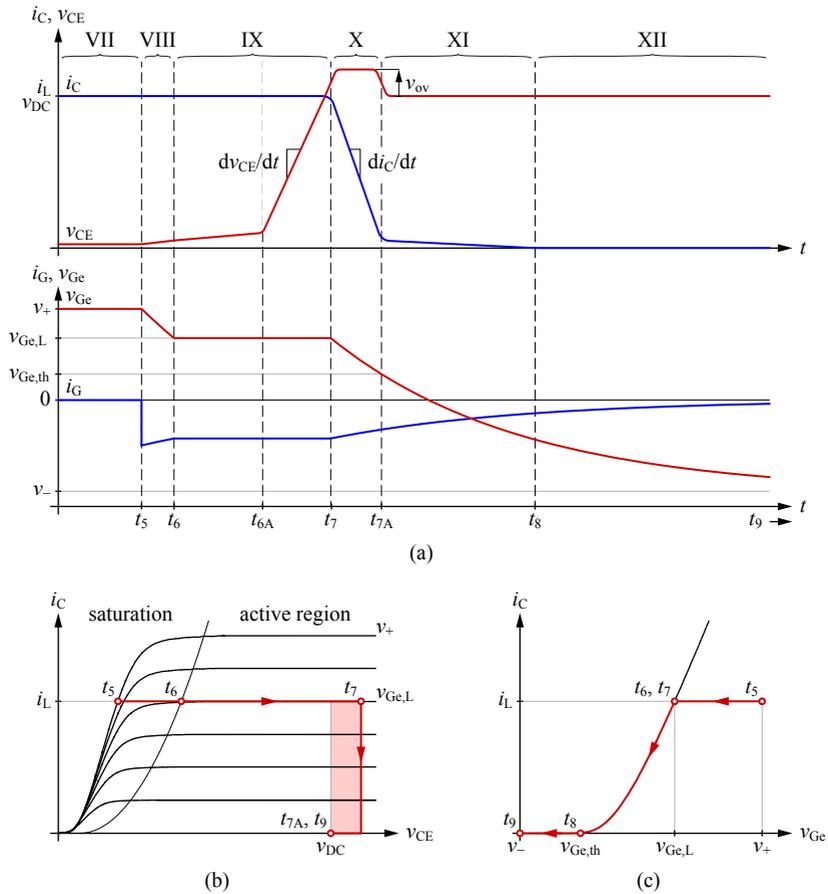


Figure 2.8: Diode-clamped inductive load switching behavior of an IGBT at turn-off. (a) Schematic voltage and current waveforms subdivided into the intervals VII – XII. Progress of the operating point (b) in the output characteristic and (c) in the transfer characteristic of the active region.

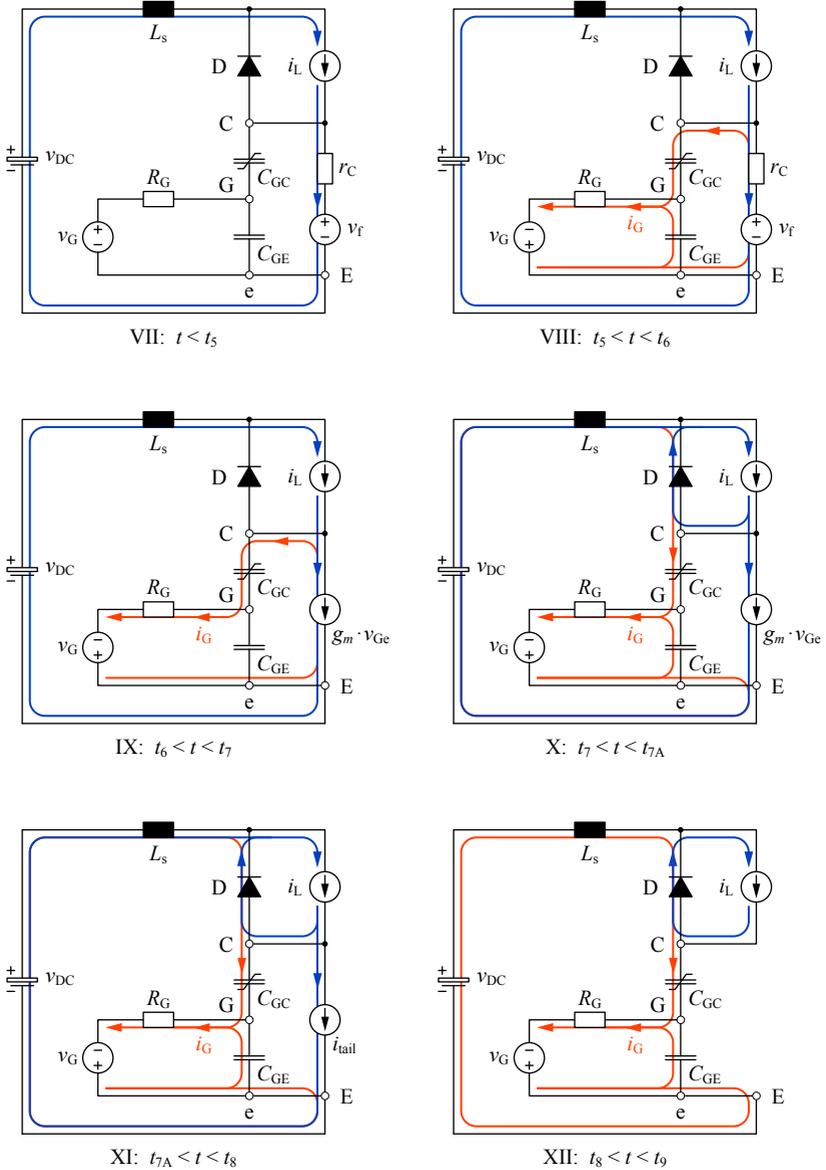


Figure 2.9: Equivalent circuits with associated current paths valid during the different intervals at turn-off, cf. Figure 2.8.

even in the case of employing a resistive GD the gate current stays constant,

$$i_G = \frac{v_- - v_{Ge,L}}{R_G}, \quad (2.31)$$

and charges the Miller capacitance $C_{GC,L}$ which is comparably large for low values of v_{CE} , cf. Figure 2.7. Accordingly the collector-emitter voltage rises only very slowly. As soon as v_{CE} reaches v_{Ge} , C_{GC} steeply decreases in value and, hence, the collector-emitter voltage starts to rise fast. Prior to that, the second portion of the turn-off delay is caused in this interval which can be calculated as

$$t_{d,GC} = t_{6A} - t_6 = \underbrace{((v_{CE,sat})_{i_L} - v_{Ge,L})}_{\Delta v_{CE,L}} \cdot \frac{C_{GC,L}}{i_G}. \quad (2.32)$$

From $t = t_{6A}$ on, $v_{CE} \geq v_{Ge}$ is valid and the Miller capacitance can be approximated as $C_{GC,S}$. This is where the characteristic voltage slope at turn-off begins. The rise of v_{CE} can be calculated similar to interval IV,

$$\frac{dv_{CE}}{dt} = -\frac{dv_{GC}}{dt} = -\frac{i_G}{C_{GC,S}}, \quad (2.33)$$

which is positive here since i_G is negative at turn-off.

X: Current decay ($t_7 < t < t_{7A}$)

As soon as v_{CE} reaches the value of the DC-link voltage, the free-wheeling diode is forward biased and therefore able to conduct current. Hence, the load current starts to commute from the IGBT to the diode and, thus, the gate voltage is no longer clamped, i.e. C_{ies} is discharged, similar to interval VIII, starting at the gate voltage $v_{Ge} = v_{Ge,L}$. Here, the time constant is again small, i.e. $\tau_{G,S}$.

The collector current is defined corresponding to the IGBT's static transfer characteristic,

$$i_C(t) = g_{m,s} \cdot (v_{Ge}(t) - v_{Ge,th}), \quad (2.34)$$

and the rate of change can be found as a function of the gate voltage or the gate current by differentiating (2.34),

$$\frac{di_C}{dt} = g_{m,s} \cdot \frac{dv_{Ge}}{dt} = g_{m,s} \cdot \frac{i_G}{C_{ies}} \approx g_{m,s} \cdot \frac{i_G}{C_{GE}}. \quad (2.35)$$

In order to achieve the desired decrease of collector current over time, a voltage drop needs to be present across the parasitic inductance in the commutation loop and, hence, the voltage occurring over the IGBT exceeds the DC-link voltage,

$$v_{\text{CE}} = v_{\text{DC}} - L_s \cdot \frac{di_{\text{C}}}{dt} = v_{\text{DC}} + v_{\text{ov}}, \quad (2.36)$$

as di_{C}/dt is negative at turn-off.

XI: Tail current ($t_{7\text{A}} < t < t_8$)

At $t = t_{7\text{A}}$, the gate voltage still decreases but the collector current reaches the level of the tail current i_{tail} and therefore cannot be actively reduced further and /or influenced by means of the GD. The remaining charge carriers are actively removed since positive DC-link voltage is applied to the IGBT; furthermore, the stored charge is decreased by recombination. This effect highly depends on the IGBT's technology (PT, NPT, Trench-Gate Field-Stop) and the charge carrier lifetime, and varies with the junction temperature $T_{\text{j,T}}$, with the amplitude and the shape of the collector current during the conduction state, and with the duration of the turn-off switching transient [17–19].

XII: Gate discharge ($t_8 < t < t_9$)

While the tail current decays and also thereafter, the gate voltage decreases until v_{G_e} reaches v_- . A gate voltage far below the threshold value in off-state enables to prevent a parasitic turn-on of the IGBT in off-state, cf. Section 6.1.1. Now, the freewheeling diode is carrying the load current, and the IGBT is blocking the full DC-link voltage and is ready to be turned-on again.

3

Switching Trajectory Definition Trade-off

IN the previous chapter, the characteristic voltage and current intervals have been identified for hard turn-on and turn-off, and the characteristic quantities of the IGBT waveforms have been derived for a conventional resistive GD. Based on these findings, the trade-off at selecting the value of the gate resistor is illustrated and summarized in this chapter. First, the waveforms for switching using a small and a large gate resistor are compared to each other and, subsequently, their differences are explained in detail.

Figure 3.1 shows the measured waveforms as well as the calculated switching loss energies $E_{\text{on}}/E_{\text{off}}$ of an IGBT at hard switching by means of a resistive GD for small (1) and large (2) values of the gate resistor. The voltages and currents are in accordance to the typical waveforms described in the last chapter and, hence, consolidate the considerations made. This graphical comparison now allows to identify the individual differences for the two values of the gate resistor, which are explained subsequently.

According to Chapter 2, a reduction of the gate resistor leads to higher absolute values of the gate current i_G in all intervals of the switching operation. This results in a faster charging/discharging of the gate as well as in faster switching transients, i.e. higher absolute values of di_C/dt as per (2.15) and (2.35) and dv_{CE}/dt according to (2.25) and (2.33). In the following, the consequences of slow or fast switching are discussed in terms of switching losses, switching delay times, SOA operation and EMI.

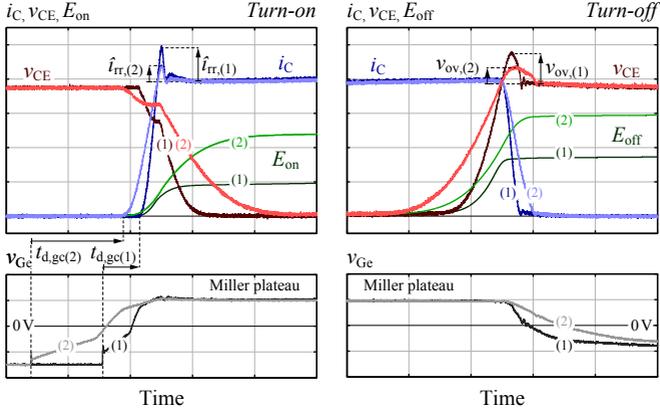


Figure 3.1: Measured current and voltage waveforms at hard switching by means of a conventional resistive GD during turn-on and turn-off using a small (1) or a large (2) gate resistor $R_{G,\text{on/off}}$. Remark: The final part of the turn-on interval where v_{G_e} reaches v_+ is not shown; also the initial part of the turn-off interval is not depicted.

3.1 Switching Losses

The energy losses during turn-on and turn-off, which are resulting from the temporary overlap of comparably large values of collector-emitter voltage v_{CE} and collector current i_C , highly depend on the switching waveforms.

On the basis of the schematic voltage and current waveforms derived in Chapter 2, the switching loss energies can be calculated. For reasons of clarity, this is made in Appendix A. As a result, the turn-on energy loss can be calculated according to (A.12),

$$\begin{aligned}
 E_{\text{on}} = & \underbrace{\frac{i_L \cdot v_{\text{DC}}}{2} \cdot \left(\frac{i_L}{|di_C/dt|} + \frac{v_{\text{DC}}}{|dv_{\text{CE}}/dt|} \cdot (1 - \sigma_s)^2 \right)}_{\text{Loss due to limited rates of } i_C / v_{\text{CE}} \text{ change}} + \\
 & \underbrace{\left(i_L \cdot \sqrt{\frac{Q_{\text{rr}}}{|di_C/dt|}} + Q_{\text{rr}} \right) \cdot v_{\text{DC}} \cdot (1 - \sigma_s)}_{\text{Loss due to reverse recovery effect}} - \underbrace{\frac{1}{2} \cdot L_s \cdot i_L^2}_{\text{Energy to } L_s}, \quad (3.1)
 \end{aligned}$$

and the turn-off loss results as (A.22),

$$E_{\text{off}} = \underbrace{\frac{i_L \cdot v_{\text{DC}}}{2} \cdot \left(\frac{v_{\text{DC}}}{|dv_{\text{CE}}/dt|} \cdot (1 + \sigma_s)^2 + \frac{i_L}{|di_C/dt|} \right)}_{\text{Loss due to limited rates of } i_C / v_{\text{CE}} \text{ change}} + \underbrace{v_{\text{DC}} \cdot Q_t}_{\text{Tail current loss}} + \underbrace{\frac{1}{2} \cdot L_s \cdot i_L^2}_{\text{Energy from } L_s}. \quad (3.2)$$

Thereby,

$$\sigma_s = \frac{L_s \cdot |di_C/dt|}{v_{\text{DC}}} \quad (3.3)$$

is a positive definite factor which describes the ratio between the voltage across the stray inductance L_s and the DC-link voltage during the rise time and fall time of the collector current ($\sigma_s \leq 1$ at turn-on), Q_{rr} equals the stored reverse recovery charge of the freewheeling diode, and Q_t equals the charge of the IGBT extracted by the tail current.

Both switching energy loss components are mainly resulting from the limited rates of i_C and v_{CE} change. Using a low-ohmic gate resistor enables to increase di_C/dt as well as dv_{CE}/dt and, hence, to decrease the corresponding contributions to the total switching energies, cf. Figure 3.1. The saving of energy losses due to the stray inductance L_s at turn-on is compensated at turn-off and therefore L_s does not contribute to the overall switching losses; but, via σ_s , an increased value of L_s mainly redistributes the losses from turn-on to turn-off and limits the switching speed.

As a result, from the switching losses' point of view the gate resistor should be selected as small as possible. It must only be considered that because of the (parasitic) inductance in the gate loop L_{gl} a minimum gate resistance $R_{\text{G,min}}$ has to be provided in order to ensure at least critical damping of the LC -gate driving path [12],

$$R_{\text{G,min}} = 2 \cdot \sqrt{\frac{L_{\text{gl}}}{C_{\text{ies}}}}. \quad (3.4)$$

3.2 Switching Delay Times

The switching delays indicate the time intervals from triggering a turn-on / turn-off to the decrease / increase of v_{CE} to half the DC-link voltage,

cf. Figure 2.4 and Figure 2.8. In practice, these delay times should be kept as low as possible since they introduce a phase shift between the PWM control signal and the generated output voltage waveform which in turn could reduce the phase margin and the bandwidth of a superordinate control.

For a resistive GD, the turn-on delay equals the sum of the gate charge delay (2.13), the current rise time (A.3), and half the voltage fall time (A.7) assuming $L_s = 0$ and $Q_{rr} = 0$ for limiting the complexity. In sum, the turn-on delay results as

$$t_{d,on} = \tau_{G,S} \cdot \ln \left(\frac{\Delta v_G}{v_+ - v_{Ge,th}} \right) + \frac{i_L}{|di_C/dt|} + \frac{v_{DC}}{2 \cdot |dv_{CE}/dt|}. \quad (3.5)$$

The turn-off delay originates from discharging the gate to the level of the Miller-plateau (2.29), from charging the (large) Miller-capacitance $C_{GC,L}$ to the level of the gate voltage as per (2.32), and from half the voltage rise time (A.16) where a smaller value of the Miller capacitance $C_{GC,S}$ is considered (see Figure 2.7); furthermore, $L_s = 0$ is assumed for limiting the complexity. As a result, the turn-off delay can be expressed as

$$t_{d,off} = \tau_{G,L} \cdot \ln \left(\frac{\Delta v_G}{v_{Ge,L} - v_-} \right) + \underbrace{\left((v_{CE,sat})_{i_L} - v_{Ge,L} \right)}_{\Delta v_{CE,L}} \cdot \frac{C_{GC,L}}{i_G} + \frac{v_{DC}}{2 \cdot |dv_{CE}/dt|}. \quad (3.6)$$

In consideration of (2.11) and (2.26), using a small gate resistor leads to a decrease of the gate charge/discharge delays, increases the absolute values of di_C/dt and dv_{CE}/dt , and is finally also beneficial in terms of short switching delay times.

As has been shown so far, fast switching is beneficial in terms of low switching losses and short switching delay times. On the other hand, as will be detailed in the next two sections, fast switching transients negatively impact the SOA operation of the IGBT and EMI of a power electronics converter.

3.3 Safe Operating Area (SOA)

Employing a low ohmic gate resistor is beneficial concerning switching losses and switching delay times. However, fast rates of current change

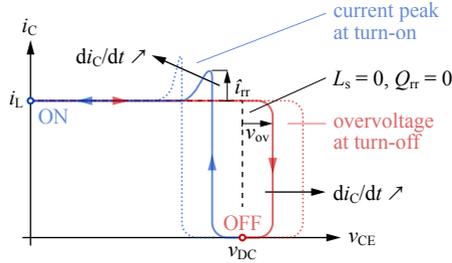


Figure 3.2: Schematic IGBT trajectory at hard switching considering the turn-off overvoltage v_{ov} and the peak reverse recovery current \hat{i}_{rr} for low di_C/dt (solid) and high di_C/dt (dotted). The dashed line represents the trajectory for an ideal commutation loop ($L_s = 0$) and no reverse recovery charge ($Q_{rr} = 0$).

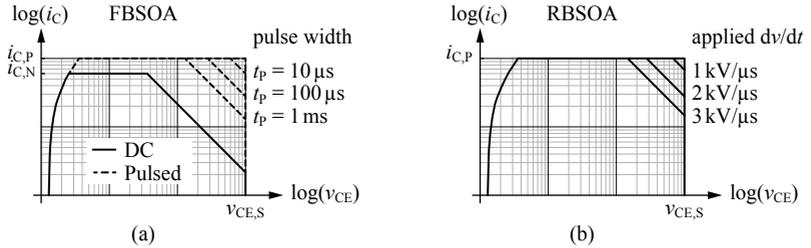


Figure 3.3: Typical safe operating areas (SOAs) of an IGBT [16]. (a) Forward Bias SOA (FBSOA) valid at turn-on with thermal limitation; (b) Reverse Bias SOA (RBSOA) valid at turn-off with dv_{CE}/dt restriction to prevent a dynamic latch-up.

are causing an increased peak reverse recovery current at turn-on

$$\hat{i}_{rr} = \sqrt{Q_{rr} \cdot \frac{di_C}{dt}} \quad (3.7)$$

and higher switching overvoltage

$$v_{ov} = L_s \cdot |di_C/dt| \quad (3.8)$$

at turn-off. Furthermore, the high di_C/dt may also lead to a diode snap-off overvoltage [20]. The corresponding trajectory of the IGBT is visualized in Figure 3.2 for low and high values of di_C/dt . In consideration of this trajectory, in order to comply with the SOA of the IGBT, cf.

Figure 3.3, it is obvious that the peak collector current $i_{C,\text{pk}} = i_L + \hat{i}_{\text{rr}}$ must stay within the FBSOA at turn-on and the peak collector-emitter voltage $v_{\text{CE},\text{pk}} = v_{\text{DC}} + v_{\text{ov}}$ must remain inside the RBSOA at turn-off. It is important to note that thereby the voltage across the IGBT chip is higher than the voltage at the module's power terminals, as the voltage drop across the parasitic inductance of the IGBT module adds to the voltage measured at the power terminals.

Accordingly, the switching speed must typically be decreased by means of a larger gate resistor in order to maintain a SOA switching of the IGBT for all possible operating conditions, e.g. for the whole range of i_L , v_{DC} and $T_{\text{j,T}}$ which results in an increase of the switching losses and switching delay times.

3.4 Electromagnetic Interference (EMI)

Switched-mode power converters are causing EMI as a result of the high frequency (HF) discontinuous current and voltage profiles with short switching transition times, i.e. fast rates of the semiconductors' current and voltage changes, di_C/dt and dv_{CE}/dt , respectively. Fig. 3.4 shows a schematic overview of a typical power electronic converter system which interfaces a three-phase electrical machine / generator to a three-phase grid.

Conducted EMI is resulting from the fast voltage changes of the switching nodes, i.e. the dv_{CE}/dt of the IGBTs, needed for the generation of a specific output voltage or current by means of PWM. Differential-Mode (DM) noise propagates between the grid / machine phases, the semiconductors, and the DC-link. Common-Mode (CM) noise is propagating via the parasitic capacitances C_p , C_b shown in Figure 3.4, i.e. the capacitances from the switching nodes, the busbars or the PCB tracks, and the cabling as well as the load to ground. Figure 3.5 depicts the CM current measurement in an IGBT half-bridge module's parasitic capacitance C_p , which is directly proportional to the rate of the output voltage and / or the IGBTs' collector-emitter voltage changes dv_{CE}/dt .

Furthermore, the fast changes of the currents in the commutation loops and in magnetic components are causing radiated EMI.

As a consequence, EMI filters and elaborate shielding techniques, which attenuate and / or limit the conducted and radiated EMI, need to be included in power electronic converters in order to comply with

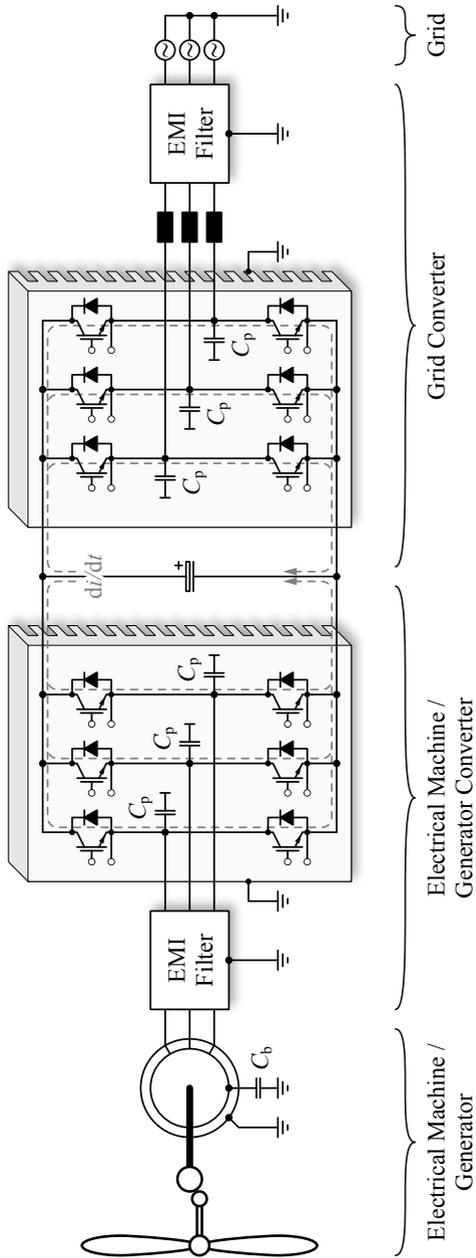


Figure 3.4: Typical application example of a three-phase power electronics converter interfacing a three-phase electrical machine / generator to a three-phase grid.

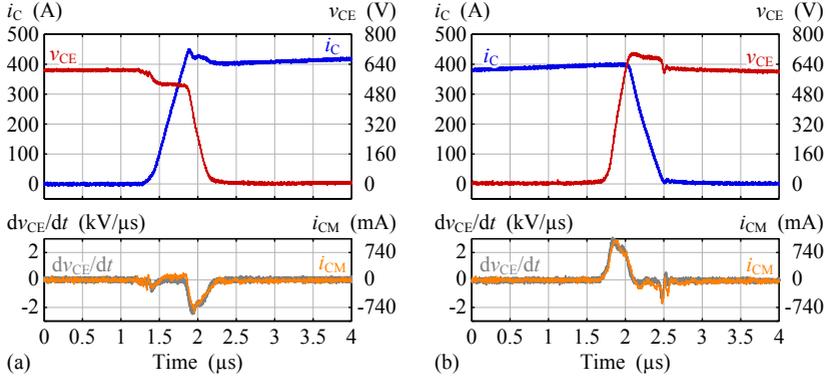


Figure 3.5: Measurement of CM current i_{CM} in C_P of a half-bridge IGBT module during (a) turn-on and (b) turn-off of the low-side IGBT.

EMI standards. Another reason for providing EMI filters is the attenuation of the inverter-induced HF currents in the bearings of an electrical machine [21] and to prevent cable-reflection induced terminal overvoltages [22]. Furthermore, the breakdown voltage of insulation materials decays with increasing frequency [23], which is why EMI filters might be necessary for maintaining the insulation voltage of e.g. a transformer winding.

In order to highlight the impact of fast switching transients in terms of EMI, the relation between the PWM current and voltage waveforms over time and the corresponding spectral components in the frequency domain are briefly reviewed in the following.

Figure 3.6 shows a typical rectangular PWM reference signal $v_{S,\text{ref}}(t)$ and the corresponding trapezoidal converter output waveform $v_S(t)$, whereby the increase and decrease of voltage are assumed as linear with defined switching transitions times t_{Ti} . In Figure 3.6, v_S is shown for fast ($i = 1$) or slow ($i = 2$) switching. By means of Fourier transform, the spectral amplitudes of the periodic switching reference signal $v_{S,\text{ref}}$ can be expressed for the harmonic rank n as [24, 25]

$$\hat{v}_{S,\text{ref}}(n \cdot f_S) = 2 \cdot v_{\text{pk,pk}} \cdot D \cdot \frac{\sin(\pi \cdot n \cdot D)}{\pi \cdot n \cdot D}, \quad (3.9)$$

where $v_{\text{pk,pk}}$ equals the peak-to-peak value and $D = t_P/T_S$ corresponds to the duty-cycle of $v_{S,\text{ref}}$. The trapezoidal switching signal v_S can be obtained by convolution of $v_{S,\text{ref}}$ and a single rectangular pulse with an

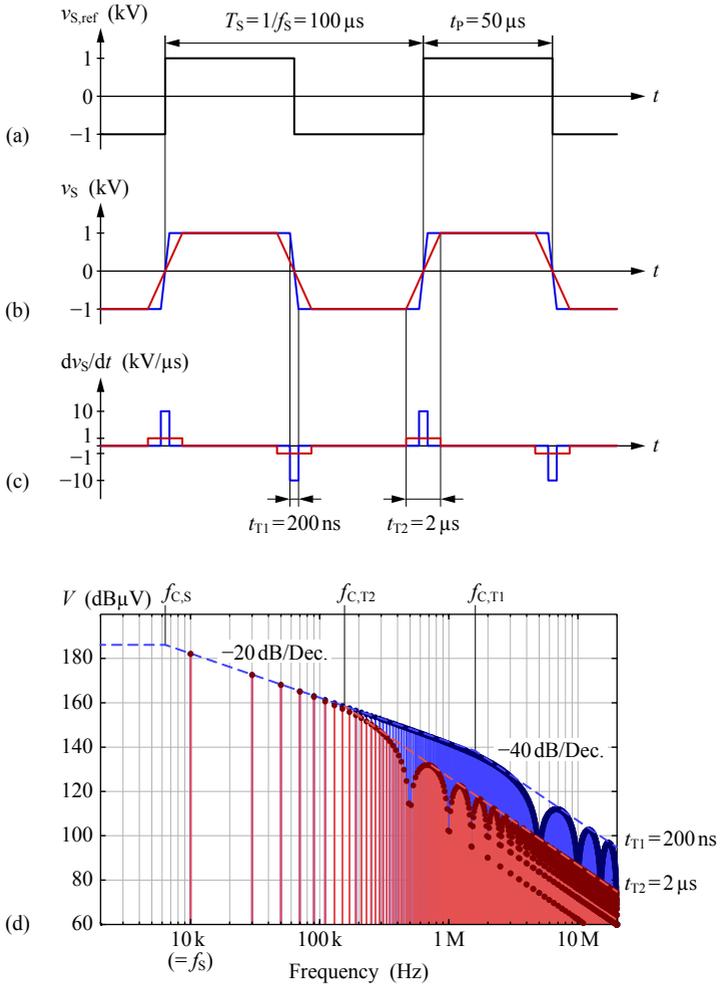


Figure 3.6: (a) Rectangular PWM reference signal $v_{S,ref}$; (b) corresponding trapezoidal output waveform v_S with fast (1) or slow (2) switching times; (c) corresponding time derivative dv_S/dt ; (d) Related amplitude spectrum (bars) and spectral envelopes (dashed lines).

amplitude of $1/t_{Ti}$ and a width of t_{Ti} . As the convolution in the time-domain corresponds to a multiplication in the frequency domain, the spectral amplitudes of the switching signal can be calculated as [24, 25]

$$\hat{v}_S(n \cdot f_S) = \underbrace{2 \cdot v_{pk,pk} \cdot D \cdot \frac{\sin(\pi \cdot n \cdot D)}{\pi \cdot n \cdot D}}_{\text{Spectral components of the rectangular waveform}} \cdot \underbrace{\frac{\sin(\pi \cdot n \cdot t_{Ti}/T_S)}{\pi \cdot n \cdot t_{Ti}/T_S}}_{\text{reduction due to limited rates of change in the transition intervals}}, \quad (3.10)$$

where the switching time is given by

$$t_{Ti} = \frac{v_{pk,pk}}{|dv_S/dt|}. \quad (3.11)$$

The corresponding corner frequencies of the spectral envelope of (3.10) can be expressed for the two $\sin(x)/x$ -functions as

$$f_{C,S} = \frac{1}{\pi \cdot t_P}, \quad (3.12)$$

$$f_{C,Ti} = \frac{1}{\pi \cdot t_{Ti}}. \quad (3.13)$$

Figure 3.6 (d) illustrates the amplitude spectrum of v_S and the spectral envelopes with the appropriate corner frequencies. Starting at the switching frequency, the amplitude decays linearly with frequency, i.e. by -20 dB/dec. in the log-log diagram. For frequency components beyond the corner frequency $f_{C,Ti}$, which is basically defined by the transition time t_{Ti} , the amplitude decays proportional to the square of the frequency and, hence, by -40 dB/dec.

Slow switching is accordingly a means for reducing the HF components of the noise spectrum. In order to comply with the EMI standards and to maintain a safe operation of the load, i.e. to prevent overvoltages, bearing currents, or stress on insulation materials, it could, hence, become necessary to decrease the switching speed by enlarging the gate resistor from this point of view. However, the switching loss and the switching delay times are increased thereby.

3.5 Summary

The selection of a specific gate resistor involves an inevitable trade-off between switching losses, output voltage distortion, EMI, and stresses

R_G	Advantages
small	Low switching losses E_{sw} Low switching delay times $t_{d,on/off}$ High noise immunity to dv_{CE}/dt
large	Low conducted and radiated EMI Low turn-off overvoltage v_{ov} Low peak reverse recovery current \hat{i}_{tr} Slow diode snap-off, no oscillations

Table 3.1: Switching trajectory definition trade-off, i.e. advantages, for a small and a large value of the gate resistor R_G .

on the semiconductors and the load. Table 3.1 summarizes the corresponding advantages of using either a small or a large value of the gate resistor.

In practice, on the one hand the gate resistor is selected as small as possible to achieve low switching losses and a minimal distortion of the output voltage / current by means of low switching delay times. On the other hand, the gate resistor must be selected sufficiently large in order to never exceed the SOA for all possible operating conditions, i.e. for the whole range of the junction temperature, the load current and the DC-link voltage; furthermore, the damping of the gate loop needs to be maintained. In addition, a lower limit of the gate resistor may also be required in order to ensure compliance with EMI standards. Accordingly, the room for optimizations is very limited with this basic type of GD.

In order to break through the limitations of this significant trade-off and to extend the possibilities for optimizing the switching behavior, a GD is needed which allows to independently adjust the rates of di_C/dt and dv_{CE}/dt , i.e. which decouples the current and the voltage slopes. This allows to separately optimize the different intervals of the switching operation in terms of switching losses, SOA operation and EMI and, hence, leads to an improved switching behavior of the IGBT.

Prior to proposing the closed-loop GD developed in the course of this thesis, in the next chapter, state-of-the-art implementations of such gate drive concepts are illustrated and reviewed.

4

State-of-the-Art Gate Drive Concepts

As has been shown in the previous chapter, an individual control of the IGBT's current and voltage slopes is needed for optimizing the switching trajectories in terms of switching losses, SOA operation (peak reverse recovery current of the complementary freewheeling diode and IGBT / diode turn-off overvoltages), switching delay times, and EMI.

Substantial research work concerning gate drive concepts, which enable a control of the current and voltage switching trajectories at inductive load (hard) switching, has already been published in numerous scientific journals and conferences.

In this chapter, the essential ideas and operating principles of state-of-the-art IGBT gate drive concepts are described and their individual advantages, disadvantages and limitations are identified. The gate drive concepts can be classified into passive, open-loop and closed-loop types. An according graphical overview is shown in Figure 4.1.

The passive concepts are pure feed-forward GDs, i.e. the GD's output is predefined and not actively changed during switching. The open-loop GDs are able to adjust their output, e.g. the gate resistor, the gate current, or the gate voltage, to different (constant) values for each characteristic interval of a switching transient, i.e. the gate charge / discharge delay interval, the current slope and the voltage slope, though without dynamic feedback of the IGBT status. The last category are closed-loop GDs, where the GD's output voltage or current is dynamically controlled in dependency of control reference signals and feedback signals of the IGBT's voltage and / or current.

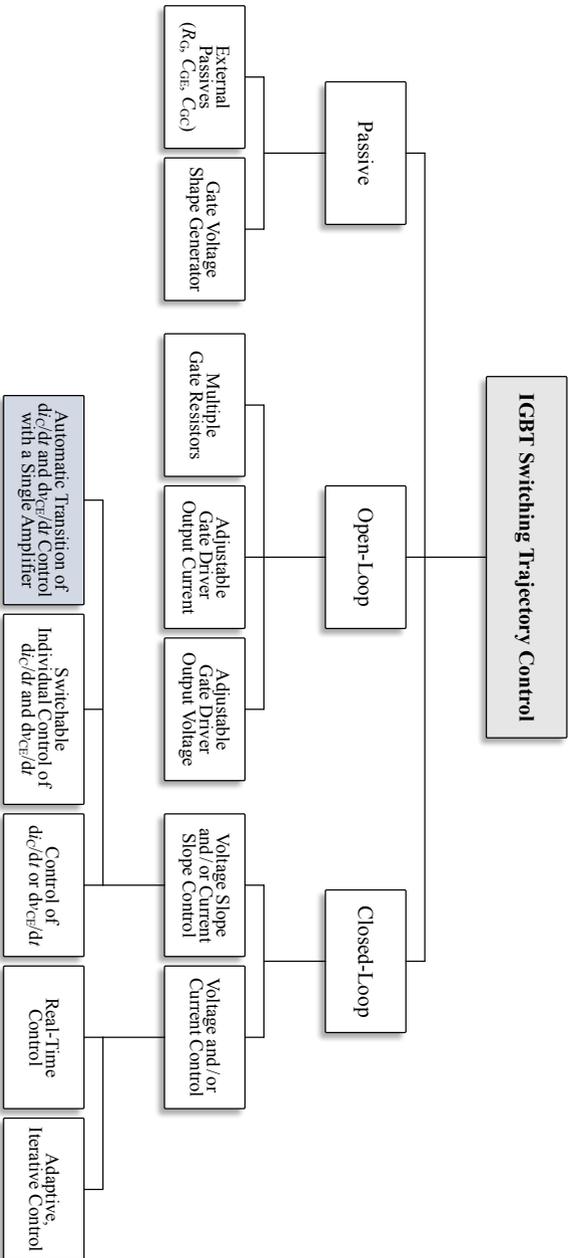


Figure 4.1: Classification of gate drive concepts which enable a shaping of the IGBT's switching trajectory at hard turn-on or turn-off. The proposed closed-loop di/dt and dv/dt control concept of this thesis, which employs a single analog amplifier and features a seamless automatic transition from di/dt to dv/dt control at turn-on and vice versa at turn-off, is highlighted.

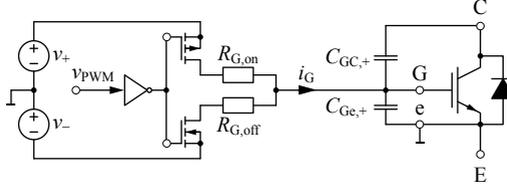


Figure 4.2: Basic push-pull resistive GD extended by external passives, i.e. individual gate resistors $R_{G,on}$, $R_{G,off}$, and additional gate-emitter capacitance $C_{Ge,+}$ and gate-collector capacitance $C_{GC,+}$.

4.1 Passive Gate Drive Concepts

4.1.1 External Passives

The current and voltage slopes can individually be adjusted by extending the basic push-pull GD circuit of Figure 2.3 by means of additional external components as shown in Figure 4.2:

Individual gate resistors $R_{G,on}$, $R_{G,off}$ for turn-on and turn-off with corresponding diodes allow to independently tune the switching behavior at turn-on and turn-off with a marginal hardware effort. One of the series diodes is not essentially required and even both diodes can be omitted if the GD features an output stage with individual transistors connected to the gate drive circuit supply rails [12], cf. Figure 4.2.

External gate capacitance $C_{Ge,+}$ adds to the IGBT's internal gate capacitance and thus slows down the di_C/dt as per (2.15) and (2.35) without affecting the dv_{CE}/dt [12]. While this suppresses the crosstalk [26], the switching delay times and gate drive losses are increased due to the larger IGBT input capacitance.

External Miller capacitance $C_{GC,+}$ adds to the IGBT's internal capacitance and reduces the absolute value of dv_{CE}/dt according to (2.25) and (2.33) without influencing di_C/dt substantially [12]. The downside of this method is that the external capacitor must provide a voltage rating as high as the blocking voltage of the IGBT. In addition, this approach increases the risk of a cross conduction fault in bridge leg configurations of IGBTs [9].

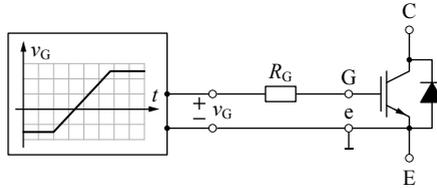


Figure 4.3: Schematic representation of the feed-forward gate voltage shape generator [27].

4.1.2 Gate Voltage Shape Generator

A possible solution to avoid the above mentioned disadvantages of adding external passives is the feed-forward gate voltage shape generator presented in [27], cf. Figure 4.3. This GD is basically applying a passively generated voltage slope via a gate resistor to the gate terminals of the IGBT during turn-on. The di_C/dt is then defined by the specific slope of the applied gate voltage in combination with the IGBT's transconductance. In the interval of the IGBT's collector-emitter voltage slope the gate current increases due to the IGBT's constant gate-emitter voltage at the Miller-plateau, i.e. while the gate output voltage still rises a significant voltage drop occurs across the gate resistor. Hence, the gate current and the dv_{CE}/dt can be controlled by means of the gate resistor to some extent. With this concept, the controllability of the voltage slope is limited and, in normal operation, an application is only possible for the turn-on transients.

4.2 Open-Loop Gate Drive Concepts

An individual control of the gate current and thus of the IGBT can also be achieved through an active GD, e.g. via employing switchable or adjustable gate resistors [12, 28–32], gate current sources / sinks [13, 28, 33–43] or gate voltages [44]. A schematic overview of such gate drive concepts is depicted in Figure 4.4.

The basic idea thereby is to subdivide the switching transients into characteristic intervals such as a delay interval, the current slope, and the voltage slope interval, etc., whereby a specific gate resistor, gate current, or gate voltage is selected for each interval in order to independently control the IGBT. For all topologies the control of the output

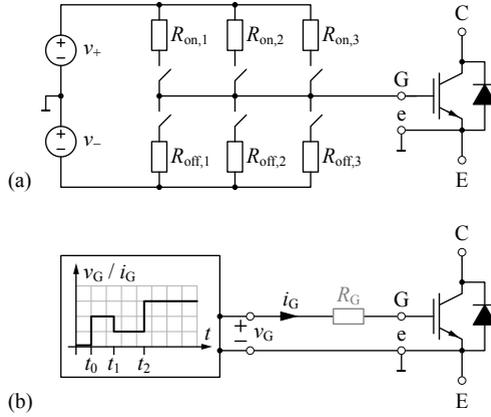


Figure 4.4: GD with adjustable output stage implemented by (a) switchable gate resistors or (b) a switchable gate voltage or gate current source featuring discrete resistances / voltage / current levels.

stage can either be based on a fixed profile [13, 28, 39, 43], an operating point dependent transition [29, 30, 41] or an event / level feedback of the switching transients [29, 31–35, 37, 38, 40, 42, 44].

4.2.1 Limitations

The practical implementation of the GD has to restrict the di_C/dt and dv_{CE}/dt to specific limits for all possible operating conditions such as varying junction temperature $T_{j,T}$, load current i_L or DC-link voltage v_{DC} , and is thus selected considering the worst case. In the following, the impacts of the different parameters are discussed.

Junction Temperature $T_{j,T}$ The IGBT's transconductance $g_{m,s}$ decreases as the junction temperature increases, cf. Figure 4.5 (a), and so does $|di_C/dt|$, cf. (2.15) and (2.35).

Accordingly, the GD must be designed considering the lowest possible value of $T_{j,T}$. At nominal operating conditions, i.e. at high values of $T_{j,T}$, however, this leads to a switching of the IGBT which is slower than actually necessary.

Load Current i_L The impact of the load current i_L is twofold. On the one hand, $g_{m,s}$ increases with the level of i_L , cf. Figure 4.5 (a),

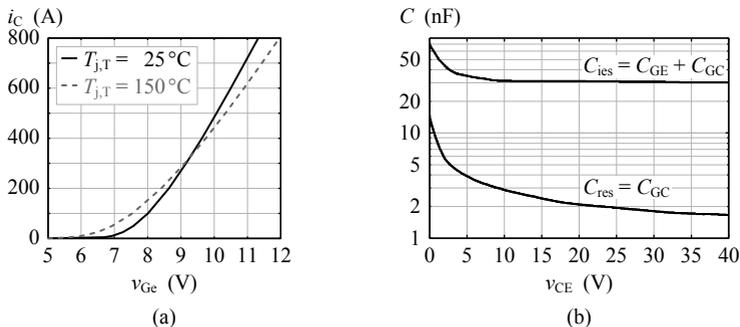


Figure 4.5: (a) Nonlinear IGBT transconductance g_m (Infineon FF450R12KE4) in dependency of the junction temperature $T_{j,T}$ and (b) nonlinear differential (small-signal) capacitances C_{res} and C_{ies} (Semikron SKM 500 GA 123 D) depending on v_{CE} measured at $v_{Ge} = 0\text{ V}$ and $f = 1\text{ MHz}$.

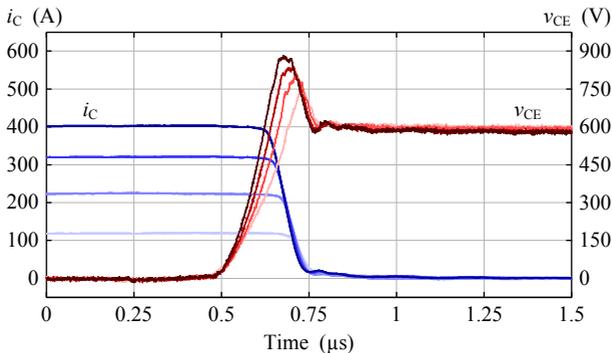


Figure 4.6: Measured turn-off waveforms of a trench-gate field-stop IGBT module (Infineon FF450R12KE4) at hard switching for different values of the load current i_L ($R_G \approx 1\ \Omega$).

and, hence, $|di_C/dt|$ increases as well if a constant gate current i_G is assumed, cf. (2.15) and (2.35). On the other hand, i_L has a significant impact on the gate current of a resistive GD. This is explained by the fact that the level of the Miller plateau $v_{Ge,L}$ increases with i_L and, thus, the absolute value of the gate current and, accordingly, the $|dv_{CE}/dt|$ at turn-on decreases, cf. (2.24) and (2.25), but increases at turn-off, cf. (2.31) and (2.33).

In addition, due to the increased level of the Miller plateau, the maximum value of the gate current during the turn-off current slope and, thus, $|di_C/dt|$ also increases with i_L . Figure 4.6 experimentally verifies the faster voltage and current slopes towards higher levels of i_L for the turn-off case.

As a result, the GD must be designed concerning $|di_C/dt|$ considering the maximum level of the load current. In addition, concerning $|dv_{CE}/dt|$ a resistive GD must be designed for the minimum level of i_L at turn-on and for the maximum level of i_L at turn-off. Again, at nominal values of i_L the IGBT is switching slower than allowed.

DC-Link Voltage The Miller capacitance C_{GC} decreases while the collector-emitter voltages rises, cf. Figure 4.5 (b), and, hence, $|dv_{CE}/dt|$ increases, cf. (2.25) and (2.33).

Since the GD must be designed for the maximum admissible value of v_{DC} , the IGBT switches slower than tolerable while v_{CE} is below this value, i.e. most of the time.

Gate Voltage As has been explained, $g_{m,s}$ and $|di_C/dt|$ are increasing with the load current but also with the gate voltage, respectively, cf. Figure 4.5 (a). In practice, the gate capacitance C_{GE} shows a nonlinear characteristic for gate voltages below the threshold voltage [12] but can be assumed constant during the current slope. This gate voltage dependency hence only impacts the switching delay times.

In summary, the described parameter dependencies and nonlinearities prevent to attain the maximum possible values of $|di_C/dt|$ and $|dv_{CE}/dt|$ in nominal operation. This results in higher switching losses than actually possible.

4.2.2 Intrinsic IGBT Effects

In addition to these dependencies of the switching trajectories on the operating conditions, the di_C/dt at turn-off of trench-gate field-stop IGBTs is sensitive to a desaturation of the semiconductor [17, 45, 46]. A lower gate current and/or a higher gate resistance results in a slower voltage slope at turn-off. Thereby, the stored charge in the drift region of the IGBT is partly extracted which finally results in a faster

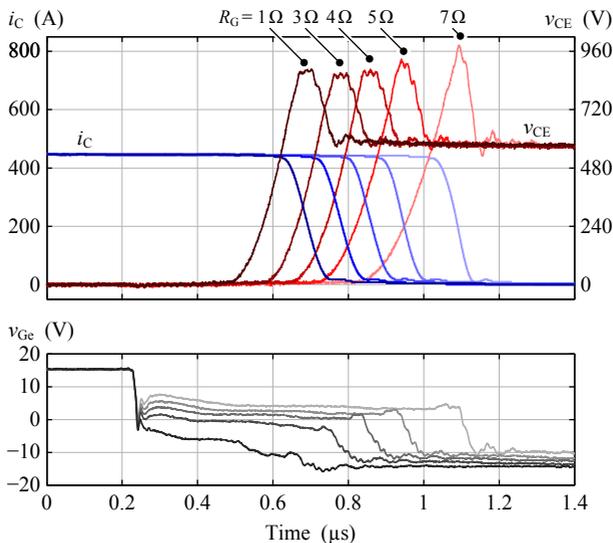


Figure 4.7: Measured turn-off waveforms of a trench-gate field-stop IGBT module (Infineon FF450R12KE4) at hard switching for different values of the gate resistor $R_G \approx \{1\ \Omega, 3\ \Omega, 4\ \Omega, 5\ \Omega, 7\ \Omega\}$.

di_C/dt . This is unexpected and typically unwanted, as it is causing higher switching overvoltage (cf. Figure 4.7, $R_G = 7\ \Omega$), and makes it extremely difficult if not impossible for an open-loop gate drive concept to switch the IGBT along a desired switching trajectory.

4.2.3 Summary

Missing compensation of the IGBT's nonlinearities as well as remaining dependencies on the load and temperature conditions are a main drawback of all passive and open-loop control concepts. With an open-loop approach, accurately defined and constant current and voltage slopes can thus hardly be obtained in all operating points. As a result, the switching transients are always tuned to not exceed the limits for di_C/dt and dv_{CE}/dt in the worst case and thus the switching behavior at nominal operation is compromised. For that reason, closed-loop concepts with negative feedback are applied to achieve a more precise and, hence, optimized control of the IGBT's switching trajectories.

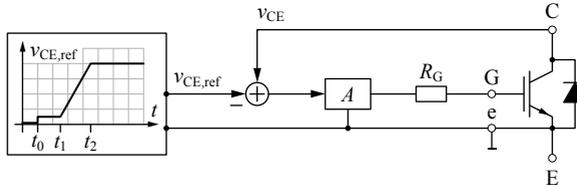


Figure 4.8: Simplified analog closed-loop v_{CE} control with a reference voltage profile $v_{CE,ref}$.

4.3 Closed-Loop Gate Drive Concepts

Compensation of the IGBT's nonlinearities as well as operating point and temperature dependencies is advantageously achieved by closed-loop control. In the following, first, concepts providing closed-loop control of the IGBT's collector current and / or the collector-emitter voltage are reviewed. Thereafter, topologies which directly control di_C/dt and / or dv_{CE}/dt are discussed.

4.3.1 Voltage and / or Current Control

A sophisticated closed-loop analog v_{CE} control topology as schematically shown in Figure 4.8 was proposed and investigated in [47–52]. A similar approach could also be followed for an i_C control. If a combination of voltage and current control is needed, the generation of both reference signals by analog circuits will be involved and hardly feasible due to their mutual dependency and the dependency on the operating point, e.g. the temporal variation of the state transition (current / voltage slope) or the value of the load current.

The handling of a combined i_C and v_{CE} control becomes only feasible by means of a digital approach as developed in [53–58] and schematically depicted in Figure 4.9. In doing so, all main state variables (i_C , v_{CE} and v_{Ge}) are sampled and processed in a digital control unit which calculates the actual state of the IGBT, adjusts the reference profiles to the actual operating point, and, finally, controls the gate current in order to attain the desired switching trajectories.

Due to the relatively large delay times of Digital-to-Analog Converters (DACs) and Analog-to-Digital Converters (ADCs) of 55 nanoseconds [57] or even 100 to 200 nanoseconds [53] in the signal paths, a

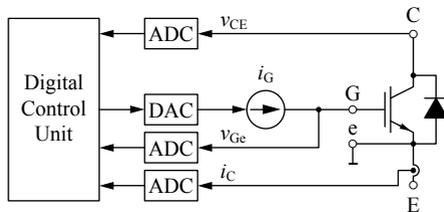


Figure 4.9: Digital GD unit comprising a microcontroller (e.g. FPGA), Analog-to-Digital Converters (ADCs) for measuring the IGBT’s state variables and a Digital-to-Analog Converter (DAC) for providing the reference signal for the controlled gate current source.

real-time approach is only promising for IGBT switching transients not faster than approx. 2 microseconds. Iterative, adaptive and system parameter dependent approaches are therefore typically applied to overcome this problem [53–56, 58]. In turn, their main downside is the lack of accurate control in case of significant changes in the converter’s system state between subsequent switching operations. In addition, the limited bandwidth of high current sensors and the highly dynamic reference and feedback signals are limiting the performance and accuracy of any i_C and v_{CE} control concept. Furthermore, the cost of high-speed DACs and ADCs is comparably high.

4.3.2 Voltage Slope and / or Current Slope Control

A very simple implementation and high performance in terms of analog control bandwidth is achieved by means of analog closed-loop di_C/dt and dv_{CE}/dt control [59–62], cf. Figure 4.10, due to constant reference value(s), simple control amplifier stages and passive measurement circuits providing high analog control bandwidth.

Different implementations of only di_C/dt control [9, 63–65], di_C/dt control at turn-on [14, 66] and dv_{CE}/dt control at turn-off [14], or individual solutions for current or voltage slope control during turn-on or turn-off [67, 68] have been proposed in the literature. A complete solution of turn-on and turn-off di_C/dt and dv_{CE}/dt control was presented in [61, 62]. However, due to the implementation with a large number of bipolar transistors and the need for detection and selection of the active control loop, cf. Figure 4.10, the performance was limited to current and voltage rates of change of 200 A/ μ s and 1 kV/ μ s, respectively.

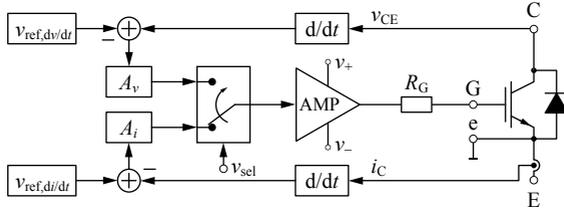


Figure 4.10: Schematic analog closed-loop di_C/dt and dv_{CE}/dt control concept where the transition between the current and the voltage slope control has to be actively detected and triggered via v_{sel} .

4.4 Summary

Passive gate drive concepts are inexpensive and simple to implement but their impact on di_C/dt and dv_{CE}/dt is limited, i.e. a specific adjustment is only feasible to a certain extent. Accordingly, the switching delay times and switching trajectories remain a non-optimal compromise in terms of switching losses, semiconductor overvoltages and EMI.

Open-loop gate drive concepts enable to adapt the gate current for the different intervals of the switching transients. This also implies a more complex and expensive hardware implementation. To achieve the desired switching behavior in each interval, a very fast and accurate detection of the different intervals and also a quick switching of the output stage is needed, here.

The main drawback of both, the passive and the open-loop concepts is their lack for compensation of the IGBT's nonlinearities as well as operating point and temperature dependencies, i.e. the switching behavior must be tuned for the worst case conditions and, thus, in nominal operation the maximum permissible switching speed is not achieved.

Basically, only closed-loop concepts offer the potential to enable a specifically defined switching behavior of the IGBT. For fast switching transients in the sub-microsecond range, concepts which directly control the slopes are beneficial in terms of control performance and cost. This is due to constant and easy to generate reference signals without dependency on the operating point, i.e. the DC-link voltage, the load current, or the junction temperature. In addition, the measurement of di_C/dt and dv_{CE}/dt can be performed with very fast and inexpensive passive sensing circuits. State-of-the-art concepts are, unfortunately, either only working in specific intervals of the switching trajectories, or

need to detect and select the respectively active control loop.

In order to overcome those limitations, in the next chapter, a highly dynamic analog closed-loop di_C/dt and dv_{CE}/dt gate drive concept with a seamless automatic transition from di_C/dt to dv_{CE}/dt control at turn-on and vice versa at turn-off is proposed.

5

New Closed-Loop di/dt and dv/dt Gate Drive Concept

IN this chapter a high-bandwidth closed-loop di_C/dt and dv_{CE}/dt gate drive concept is proposed. As has been shown in the previous chapter, the control of the IGBT's collector current and collector-emitter voltage time derivatives has advantages over the control of the IGBT's current and voltage. This is explained by constant reference signals, which are independent of the operating point and can thus be generated with minimum effort, and simple measurement and control circuits.

5.1 Conceptual Description and Operating Principle

In order to explain the basic idea of the proposed closed-loop GD, first the hard switching of an IGBT is briefly reviewed. The typical current and voltage waveforms for inductive load switching are shown in Figure 5.1. Thereby, the intervals with current and voltage changes always appear in direct sequence and / or without overlap at both turn-on and turn-off. As a consequence, ideally, dv_{CE}/dt is zero during the collector current change and di_C/dt is zero during the collector-emitter voltage change. This fact actually permits the utilization of a combined di_C/dt and dv_{CE}/dt closed-loop control, i.e. both control loops are closed simultaneously via a single PI-controller, where in contrast to [61, 62] no active selection of the control loop is required. Therefore, an automatic and extremely fast transition from the current to the voltage slope control and vice versa occurs, and the PI-controller always controls the

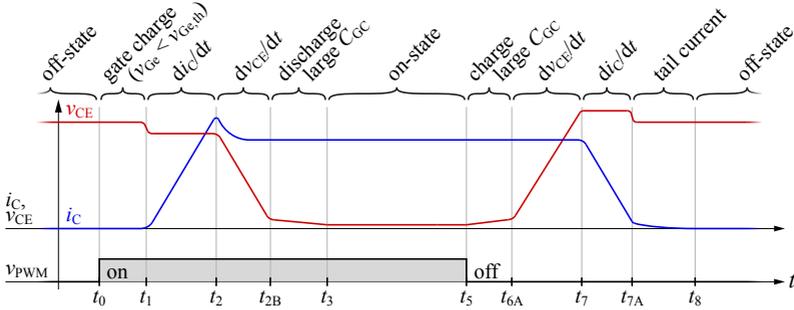


Figure 5.1: Schematic current (i_C) and voltage (v_{CE}) waveforms at hard switching during turn-on and turn-off subdivided into characteristic intervals, cf. Figure 2.4 and Figure 2.8. v_{PWM} corresponds to the PWM control command input.

variable which is changing over time.

However, a single exception must be considered. In the turn-on interval $t_2 \dots t_{2B}$, where i_C is reduced after the diode's peak reverse recovery current, cf. Figure 5.1, di_C/dt is not zero during the voltage slope, different to the original assumption. For that reason, a clipping circuit preventing this unwanted negative di_C/dt feedback during the turn-on voltage slope will be presented in Section 5.3.4.

The block diagram for the proposed combined closed-loop current and voltage slope control is depicted in Figure 5.2. There, the input reference signal $v_{ref,d/dt}$, that is set once at the beginning of every switching operation, is kept at a constant value for the complete switching process and defines in combination with the feedback gains k_I and k_V the set-points for both control variables,

$$\left(\frac{di_C}{dt} \right)_{ref} = \frac{v_{ref,d/dt}}{k_I}, \quad (5.1)$$

$$\left(\frac{dv_{CE}}{dt} \right)_{ref} = -\frac{v_{ref,d/dt}}{k_V}. \quad (5.2)$$

Accordingly, a turn-on, at which di_C/dt is positive and dv_{CE}/dt negative, is initiated by setting $v_{ref,d/dt}$ to a constant positive value which is amplified and integrated by the PI-controller to charge the IGBT's gate. Applying a negative value at $v_{ref,d/dt}$ initiates a turn-off. In order to adjust the current and voltage slopes individually for turn-on and

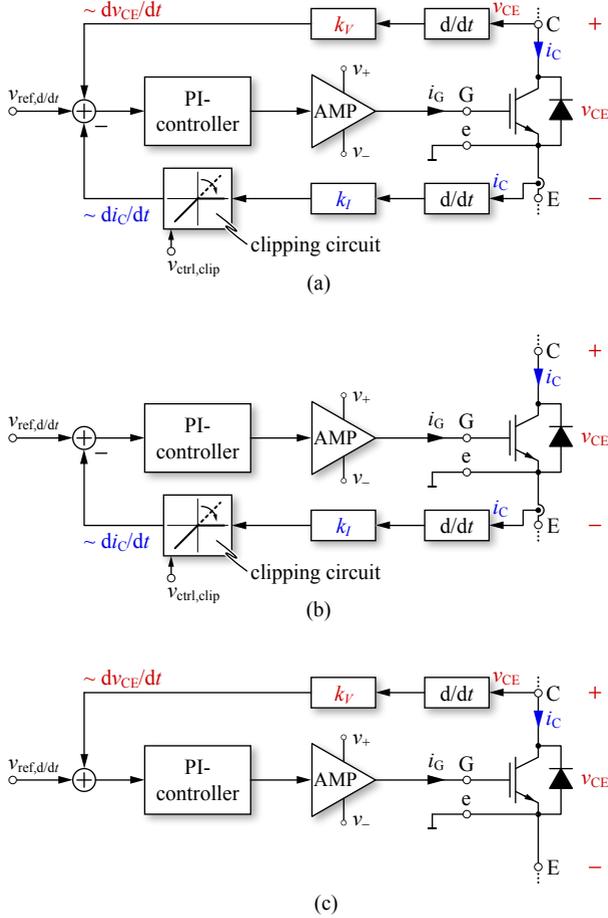


Figure 5.2: (a) Block diagram of the proposed closed-loop IGBT GD featuring di_C/dt and dv_{CE}/dt control with a single input reference signal $v_{ref,d/dt}$, continuously active feedbacks of di_C/dt and dv_{CE}/dt with individual gains k_I and k_V , a clipping circuit, a single PI-controller, and an output amplifier. Signal $v_{ref,d/dt}$: reference value for the current and voltage slope control; $v_{ctrl,clip}$: control command for the clipping circuit. (b) Circuit representation for the current slope control where dv_{CE}/dt is assumed to be zero and (c) for the voltage slope control where di_C/dt is assumed to be zero.

turn-off, the absolute values of the reference voltage $v_{\text{ref},d/dt}$ and also the feedback gains k_I and k_V may be selected differently for turn-on and turn-off.

Since the dynamic feedbacks of di_C/dt and dv_{CE}/dt are only active during the current and voltage slopes, the PI-controller is not able to control the IGBT during the turn-on interval $t_0 \dots t_1$ and during the turn-off interval $t_5 \dots t_{6A}$, cf. Figure 5.1. This missing feedback typically results in too high absolute values of the gate current at the interval transition point t_1 at turn-on and at t_{6A} at turn-off and, thus, leads to an overshoot of the di_C/dt at turn-on and the dv_{CE}/dt at turn-off, respectively. A solution acting prior to a current or voltage slope feedback is, hence, presented in the following.

5.1.1 Extension by Gate Current Control

If the gate current, that mainly defines the current and voltage slopes as per (2.15), (2.25), (2.33), and (2.35), is actively controlled in the turn-on and turn-off delay intervals, the aforementioned overshoots can be prevented. Such a gate current control can be implemented into the proposed closed-loop gate drive concept without changing the current and voltage slope control part as depicted in Figure 5.3.

The corresponding sequence diagram for the reference and control signals of the combined i_G , di_C/dt and dv_{CE}/dt control is shown in Figure 5.4. A switching operation is initiated by setting the reference signals for the current and voltage slopes $v_{\text{ref},d/dt}$ and for the gate current v_{ref,i_G} to the desired values and by simultaneously activating the gate current control via the control signal of the multiplexer v_{ctrl,i_G} . Subsequently, the gate current control must be deactivated by means of toggling the multiplexer at the beginning of the current rise at turn-on or at the voltage rise at turn-off. This point in time can be assumed to occur with a defined time delay after the initiation of the switching operation, or can be derived from reaching a predefined gate-emitter voltage level or from a certain level of active current or voltage slope feedback (implemented in the hardware prototype).

In addition, it's even possible to employ a 2-step gate current reference at turn-on and turn-off, where first a high gate current is selected to minimize the gate charge / discharge delay times, $t_{d,gc}$ and $t_{d,gd}$, and thereafter a lower gate current amplitude is programmed to avoid the aforementioned overshoots.

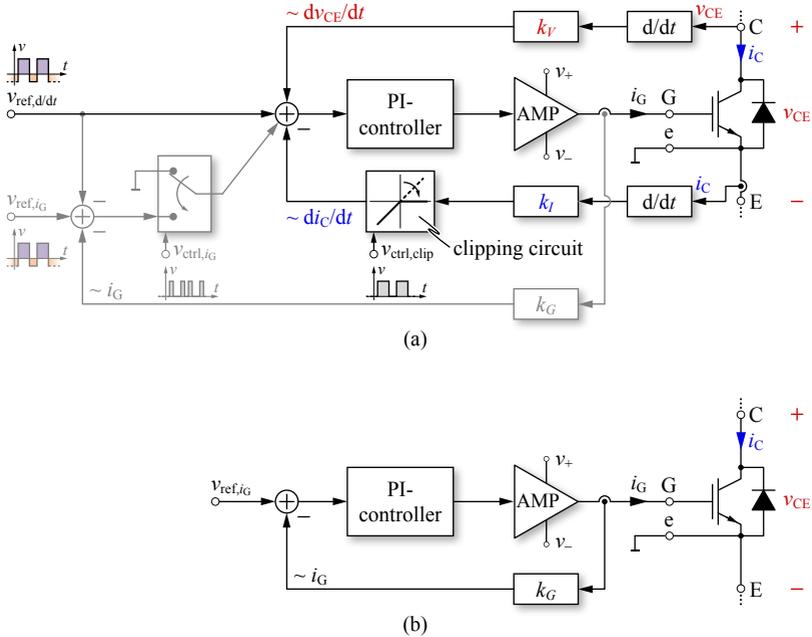


Figure 5.3: (a) Block diagram of the proposed combined closed-loop current slope and voltage slope control (shown in black), cf. Figure 5.2, extended by an additional gate current control (shown in gray) that is used to define the gate current during the turn-on and turn-off delay intervals as described in section 5.1.1. Signal $v_{ref,d/dt}$: reference value for the current and voltage slope control; $v_{ctrl,clip}$: control command for the clipping circuit; v_{ref,i_G} : reference value for the gate current control; v_{ctrl,i_G} : control command for the gate current control. (b) Block diagram of the gate current control, i.e. when v_{ctrl,i_G} is set to logic high and when di_C/dt and dv_{CE}/dt are assumed to be zero.

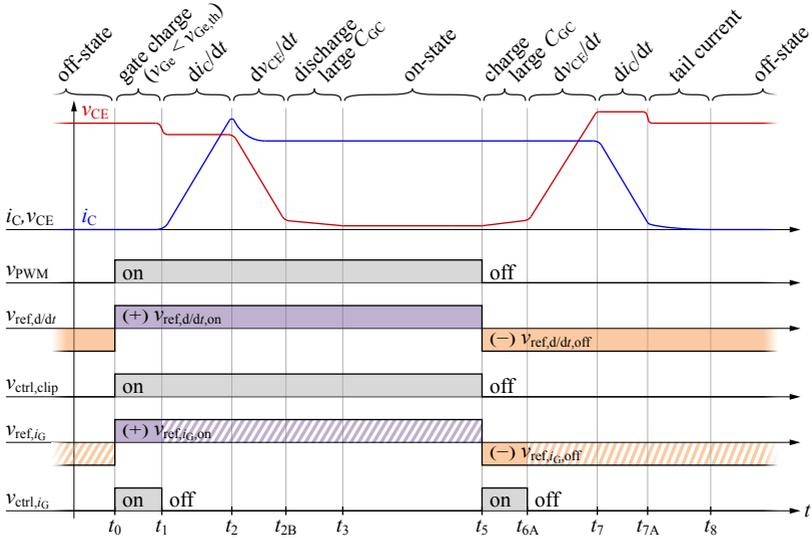


Figure 5.4: Sequence diagram for the closed-loop control of i_G , di_C/dt and dv_{CE}/dt during turn-on and turn-off. Signal v_{PWM} : PWM control command input; $v_{ref,d/dt}$: reference value for the current and voltage slope control; $v_{ctrl,clip}$: control command for the clipping circuit; v_{ref,i_G} : reference value for the gate current control; v_{ctrl,i_G} : control command for the gate current control.

The circuit diagram and a realized prototype of the proposed closed-loop GD will be shown in Section 5.3 and Section 5.4, respectively. However, first the stability and the sensitivity to changes of parameters of the proposed closed-loop switching trajectory control are verified with respect to different IGBT modules in the next section. This allows to predict the control performance and to analyze the stability and robustness of the concept.

5.2 Control-Oriented Modeling and Stability Analysis

A key issue of any closed-loop control is system stability. Based on models of the proposed GD and the IGBT, which are derived and described in this section, the stability and robustness analysis of the proposed closed-loop di_C/dt and dv_{CE}/dt switching trajectory control will be performed.

5.2.1 Model of the Closed-Loop Gate Driver

The PI-controller of the proposed GD, cf. Figure 5.3 (a), is implemented using a high-bandwidth operational amplifier, cf. Section 5.3. Its transfer function is given by

$$G_{OP}(s) = \frac{A_{DC,OP}}{s \frac{A_{DC,OP}}{2\pi f_{T,OP}} + 1}, \quad (5.3)$$

where $A_{DC,OP}$ denominates the DC-gain and $f_{T,OP}$ corresponds to the transit frequency. As the amplifier is wired in a non-inverting configuration, the transfer function of the PI-controller becomes

$$G_{PI}(s) = \frac{G_{OP}(sK_P + K_I)}{s(G_{OP} + K_P) + K_I}, \quad (5.4)$$

where K_P denominates the (ideal) proportional gain and K_I defines the (ideal) integral part $K_I s^{-1}$. The output amplifier, that is used to provide the needed output current, can be modeled as low-pass filter with a corner frequency at $f_{c,AMP}$, i.e.

$$G_{AMP}(s) = \frac{1}{s \frac{1}{2\pi f_{c,AMP}} + 1}. \quad (5.5)$$

A dv_{CE}/dt feedback signal with positive sign is needed for the voltage slope control since the IGBT shows an inverting characteristic from the gate voltage to the collector-emitter voltage. This is provided by means of an RC -high-pass filter,

$$H_{V,HP}(s) = k_V \frac{s}{sk_V + 1}, \quad (5.6)$$

Parameter	Value
$A_{DC,OP}$	100 dB
$f_{T,OP}$	350 MHz
$f_{c,AMP}$	100 MHz
k_V	1 ns
k_I	1 nH

Table 5.1: Parameter values of the closed-loop gate drive circuit.

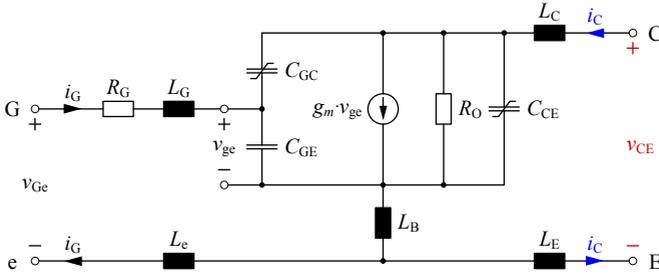


Figure 5.5: Simplified IGBT model valid in the active region including parasitic inductances of the bond wires and /or the electrical terminals.

where the time constant equals the dv_{CE}/dt feedback gain k_V and specifies the corner frequency $f_{c,V} = \frac{1}{2\pi k_V}$ of the high-pass filter.

The voltage drop across a parasitic inductance in the main current path is utilized for generating a di_C/dt proportional feedback signal,

$$H_{I,HP}(s) = k_I s. \quad (5.7)$$

The corresponding parameters of the amplifiers and feedback signals, which are used for the hardware implementation in Section 5.3, are summarized in Table 5.1.

5.2.2 Control-Oriented IGBT Model

For the IGBT a small-signal model valid in the active operating region as used in [49, 50, 65, 69–72] and shown in Figure 5.5 can be employed for the investigation of the closed-loop di_C/dt and dv_{CE}/dt switching trajectory control.

On the basis of this IGBT model, the transfer functions from the gate voltage $V_{Ge}(s)$ to the collector-emitter voltage $V_{CE}(s)$ and to the collector current $I_C(s)$ can be derived. However, the resulting transfer functions depend on the operating conditions given by the external circuitry, which in this case is the equivalent circuit for the inductive load switching, cf. Figure 2.3. Since the operating conditions for the voltage and the current slope are different, the IGBT's transfer functions for both slopes are derived separately in the following.

Interval of dv_{CE}/dt Control

For the voltage slope, i_C is impressed by the inductive load, cf. Figure 2.3, and is therefore assumed to be constant. Accordingly, the transfer function from the gate voltage to the collector-emitter voltage can be calculated based on Figure 5.5 as

$$G_V(s) = \frac{V_{CE}(s)}{V_{Ge}(s)} = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}, \quad (5.8)$$

with the coefficients

$$\begin{aligned} a_0 &= -g_m R_O \\ a_1 &= R_O C_{GC} \\ a_2 &= L_B (C_{GE} + C_{GC}(1 + g_m R_O)) \\ a_3 &= L_B R_O C_t \\ b_0 &= 1 \\ b_1 &= R_O (C_{GC} + C_{CE}) + R_G (C_{GE} + C_{GC}(1 + g_m R_O)) \\ b_2 &= R_O R_G C_t + (L_{Ge} + L_B)(C_{GE} + C_{GC}(1 + g_m R_O)) \\ b_3 &= R_O C_t (L_{Ge} + L_B) \\ C_t &= C_{GE} C_{GC} + C_{GE} C_{CE} + C_{GC} C_{CE}, \end{aligned} \quad (5.9)$$

which is in accordance with [49, 50] and is given here for the sake of completeness and easier reference. The inductances in the gate path can be joined according to $L_{Ge} = L_G + L_e$.

Interval of di_C/dt Control

For the current slope, v_{CE} is clamped by the diode to the DC-link, cf. Figure 2.3, and is thus assumed to be constant. Accordingly, the

transfer function from the gate voltage to the collector current can be derived based on Figure 5.5 as

$$G_I = \frac{I_C}{V_{Ge}} = \frac{c_3 s^3 + c_2 s^2 + c_1 s + c_0}{d_4 s^4 + d_3 s^3 + d_2 s^2 + d_1 s + d_0}, \quad (5.10)$$

with the coefficients

$$\begin{aligned} c_0 &= g_m R_O \\ c_1 &= -R_O C_{GC} \\ c_2 &= -L_B (C_{GE} + C_{GC}(1 + g_m R_O)) \\ c_3 &= -L_B R_O C_t \\ d_0 &= R_O \\ d_1 &= L_{CE} + L_B(1 + g_m R_O) + R_G R_O (C_{GE} + C_{GC}) \\ d_2 &= R_G (L_{CE} + L_B) (C_{GE} + C_{GC}(1 + g_m R_O)) \\ &\quad + R_O (C_{GE}(L_B + L_{Ge}) + C_{GC}(L_{CE} + L_{Ge})) \\ &\quad + C_{CE}(L_{CE} + L_B) \\ d_3 &= R_G R_O C_t (L_{CE} + L_B) \\ &\quad + L_t (C_{GE} + C_{GC}(1 + g_m R_O)) \\ d_4 &= L_t R_O C_t \\ C_t &= C_{GE} C_{GC} + C_{GE} C_{CE} + C_{GC} C_{CE} \\ L_t &= L_{CE} L_{Ge} + L_{CE} L_B + L_{Ge} L_B, \end{aligned} \quad (5.11)$$

where the inductances in the power- and gate paths can be joined according to $L_{CE} = L_C + L_E$ and $L_{Ge} = L_G + L_e$.

5.2.3 Closed-Loop Transfer Functions

The derived transfer functions for the GD and the IGBT are defining the block diagrams representing the voltage- and current slope control depicted in Figure 5.6. Accordingly, the open-loop transfer functions from the reference signal $V_{ref,d/dt}$ to the voltage and current time derivative values are given by

$$\begin{aligned} G_{V,OL}(s) &= \frac{V_{dv/dt}(s)}{V_{ref,d/dt}(s)} \\ &= G_{PI}(s) \cdot G_{AMP}(s) \cdot G_V(s) \cdot H_{V,HP}(s), \end{aligned} \quad (5.12)$$

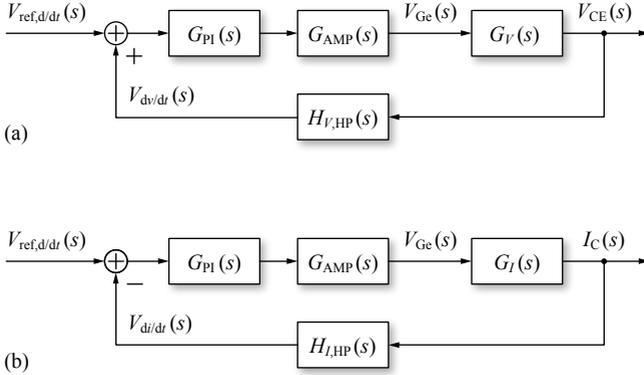


Figure 5.6: Block diagram representation of the (a) closed-loop voltage- and (b) closed-loop current slope control. G_{PI} corresponds to the PI-controller, G_{AMP} to the output amplifier, G_V and G_I to the small signal transfer functions of the IGBT, and $H_{V,HP}$ and $H_{I,HP}$ to the high-pass feedbacks according to equations (5.3) to (5.11).

$$\begin{aligned}
 G_{I,OL}(s) &= \frac{V_{di/dt}(s)}{V_{ref,d/dt}(s)} \\
 &= G_{PI}(s) \cdot G_{AMP}(s) \cdot G_I(s) \cdot H_{I,HP}(s).
 \end{aligned} \tag{5.13}$$

Finally, the corresponding closed-loop transfer functions for the voltage and current slope control based on positive $V_{dv/dt}$ and negative $V_{di/dt}$ feedback can be derived,

$$G_{V,CL}(s) = \frac{G_{V,OL}(s)}{1 - G_{V,OL}(s)}, \tag{5.14}$$

$$G_{I,CL}(s) = \frac{G_{I,OL}(s)}{1 + G_{I,OL}(s)}. \tag{5.15}$$

5.2.4 Stability Analysis

A fundamental property of the proposed closed-loop GD is the common PI-control amplifier for the di_C/dt and dv_{CE}/dt control loops, that is controlling the current and voltage slopes subsequently and individually, since they appear in direct sequence without overlap at hard switching.

	K_P	K_I
IGBT (A)	3.75	$12.9 \cdot 10^7 \text{ s}^{-1}$
IGBT (B)*	1.34	$8.57 \cdot 10^7 \text{ s}^{-1}$
IGBT (C)	5.93	$14.5 \cdot 10^7 \text{ s}^{-1}$

Table 5.2: PI-controller parameters for the closed-loop control of the IGBT modules' (A), (B)* and (C) high-side IGBT.

This temporal separation allows to independently investigate the closed-loop di_C/dt and dv_{CE}/dt control, i.e. $G_{V,CL}(s)$ and $G_{I,CL}(s)$, under the condition of identical PI-controller parameters for both control loops.

Closed-Loop Transfer Functions

In order to determine the closed-loop transfer functions (5.14) and (5.15), the parasitic inductances and the small-signal IGBT model parameters related to Figure 5.5 must be known. In appendix B, a detailed derivation of these model parameters is given for three IGBT modules from different manufacturers. All considered IGBTs feature a voltage blocking capability of 1.2 kV and a current rating of 400 – 450 A. As will be shown, the parasitic inductances of the IGBT modules are key parameters regarding the closed-loop controllability.

dv_{CE}/dt control By means of the IGBT parameters, the closed-loop transfer functions (5.14) and (5.15) can be evaluated in dependency of the controller parameters. In a first step, the PI-controller was adjusted individually for each of the three IGBT modules in order to achieve a dv_{CE}/dt control without overshoot in the step response. The controller gains K_P and K_I for the different modules are given in Table 5.2 and the corresponding Bode diagrams and step responses of the closed-loop dv_{CE}/dt control are depicted in Figure 5.7.

As can be observed, the control of the IGBT modules with larger gate loop inductance $L_{gl,HS} = L_G + L_e$, cf. Figure B.3, demands for higher K_P and K_I values of the controller, in order to achieve the desired step response, and exhibits a lower closed-loop control bandwidth, f_c . This behavior results due to the implementation of the PI-controller with an operational amplifier with limited gain-bandwidth product. A higher controller gain, that is needed at larger gate loop inductance,

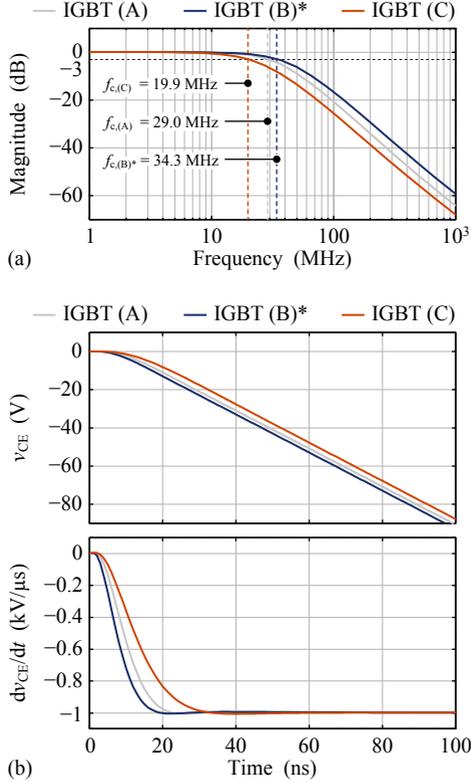


Figure 5.7: (a) Bode diagram of the closed-loop dv_{CE}/dt control for the IGBT modules (A), (B)* and (C) and (b) step responses of v_{CE} and dv_{CE}/dt for a dv_{CE}/dt reference value step from 0 to -1 kV/ μ s with the PI controller parameters given in Table 5.2 and the IGBT parameters provided in Table B.1.

reduces the control bandwidth, and in addition leads to an increased applied gate voltage amplitude. Since in practice the output voltages of the operational amplifier and the output amplifier are limited to the supply voltages, v_+ and v_- , i.e. $\pm 15\text{ V}$, another (non-linear) reduction of the control dynamics may occur. For the sake of simplicity, this effect is not considered here.

di_C/dt control The proposed gate drive concept employs only a single control amplifier, thus the PI-controller for the di_C/dt control must be the same as for the dv_{CE}/dt control, however, the control loops are different in both cases. On the basis of the optimized dv_{CE}/dt control, the closed-loop transfer functions for the current slope control, $G_{I,CL}$, can be evaluated. The corresponding Bode diagrams and step responses of the di_C/dt control are depicted in Figure 5.8.

Since the controller is optimized for the dv_{CE}/dt control, an unsatisfactory performance of the di_C/dt control results, that is close to or even beyond the stability limit as can be seen in Figure 5.8. In the following, two different solutions to overcome the problem of having only one PI-controller, that is used to implement two different control tasks, are presented. On the one hand, the controller can be optimized for the more sensitive, i.e. less stable, control loop. In the present case, this would mean to adjust the PI-controller for the di_C/dt loop. Thereby, an optimal current slope control could be achieved with the drawback that the control bandwidth of the voltage slope control would be below its optimal value. On the other hand, a degree of freedom is to add an external gate- or Miller capacitance close to the IGBT chip, whereby the effective values for C_{GE} and C_{GC} are then defined by the sum of the IGBT's internal and the external capacitance values. Since i_C is controlled via the gate voltage and v_{CE} depends on the Miller capacitance's voltage, adding additional capacitance acts as low-pass filter for the corresponding loop. In the present case, the PI-controller could be adjusted for a fast dv_{CE}/dt control and the di_C/dt control loop could be adapted by means of additional gate capacitance to get a desired control behavior.

The performance of the closed-loop di_C/dt control with additional gate capacitance, which has been tuned by means of evaluating and optimizing the closed-loop transfer functions, is depicted in Figure 5.9. Since the two control loops are subsequently active for inductive switching, adding gate capacitance does not directly impact the voltage slope

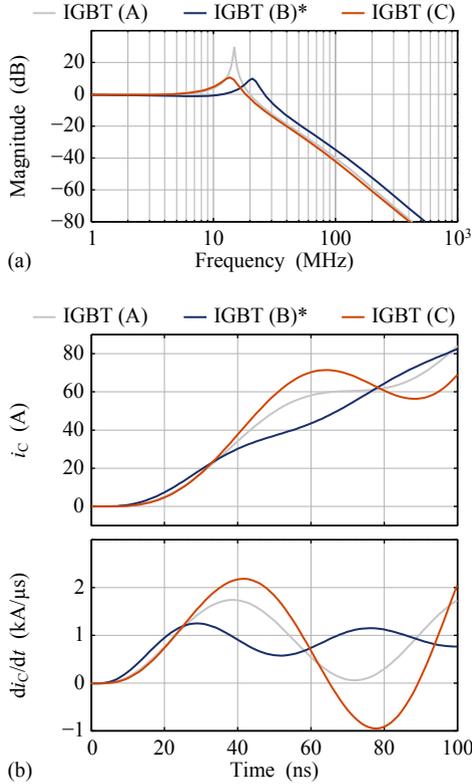


Figure 5.8: (a) Bode diagram of the closed-loop di_C/dt control for the IGBT modules (A), (B)* and (C) and (b) step responses of i_C and di_C/dt for a di_C/dt reference value step from 0 to 1 kA/ μ s with the PI controller parameters given in Table 5.2 and the IGBT parameters provided in Table B.1.

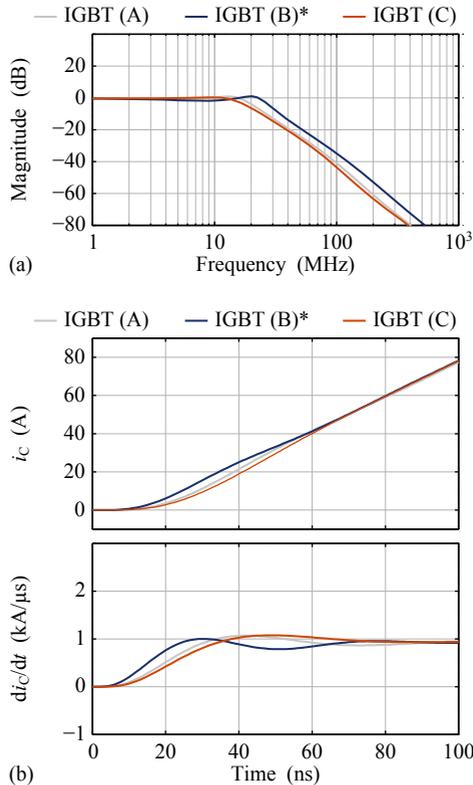


Figure 5.9: (a) Bode diagram of the closed-loop di_C/dt control for the IGBT modules (A), (B)* and (C) and (b) step responses of i_C and di_C/dt for a di_C/dt reference value step from 0 to 1 kA/ μ s with the PI controller parameters given in Table 5.2, the IGBT parameters provided in Table B.1, and additional external gate-emitter capacitances, i.e. $C_{GE,(A),ext.} = 143$ nF, $C_{GE,(B)*,ext.} = 38$ nF and $C_{GE,(C),ext.} = 230$ nF.

control. The disadvantages of this solution are the increased gate drive charge and the difficulty to insert a capacitor close to the chip in practice.

Parameter Variations

A verification of the control's robustness can be performed by investigating the impact of IGBT and controller parameter variations. According to Nyquist's stability criterion, in the case at hand the stability of the closed-loop system is given, if all poles of the corresponding open-loop transfer function are located in the open-left s -half plane.

To investigate the sensitivity of the controller, the root-locus plots of the dv_{CE}/dt control loop for increasing the PI-controllers' proportional gain (K_P) up to 4-times the nominal value are depicted in Figure 5.10. It can be seen for all IGBT modules, that the controls are approaching the stability limit for the maximum values of K_P . From the controller's side, there should accordingly not be a concern regarding stability, since in practice the PI-controller's gain is properly adjusted initially and then kept constant.

For the robustness analysis of the control with respect to the IGBT's parameters, root-locus plots of the dv_{CE}/dt control loop for reduced Miller capacitance, cf. Figure 5.11, and of the di_C/dt control loop for increased transconductance, cf. Figure 5.12, are evaluated. Reducing the Miller capacitance down to 25 % of the nominal value as worst case assumption for high values of v_{CE} leads to a shifting of the pivotal poles of the dv_{CE}/dt control towards the right s -half plane, but the system is still stable.

For the di_C/dt loop, the dominant poles are also shifted towards the right s -half plane for an increase of g_m by a factor of 4, and therewith the system gets close to instability. Since this high value of g_m exceeds the specified values in the data sheets by far, no stability issues are to be expected in practice.

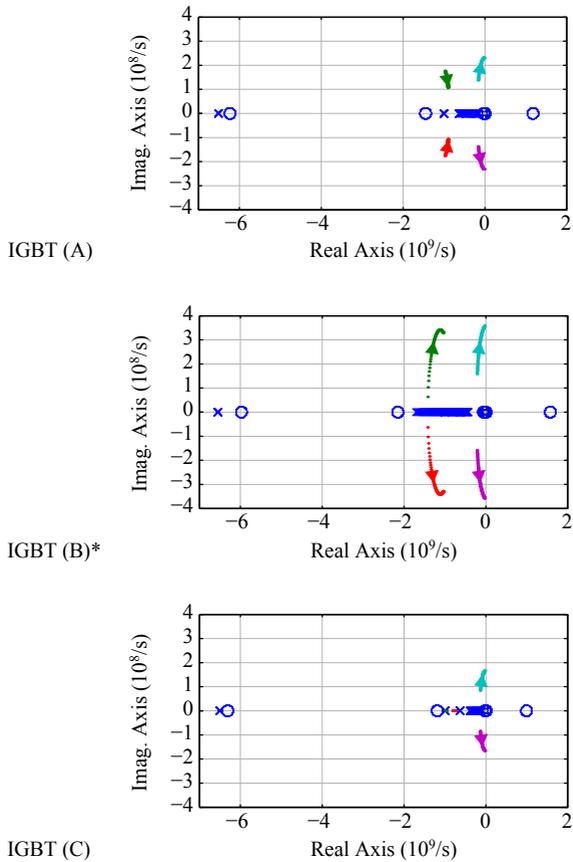


Figure 5.10: Root locus plots of the dv_{CE}/dt control for increasing the PI-controller's proportional gain (K_P) from nominal value, cf. Table 5.2, up to 4-times the nominal value.

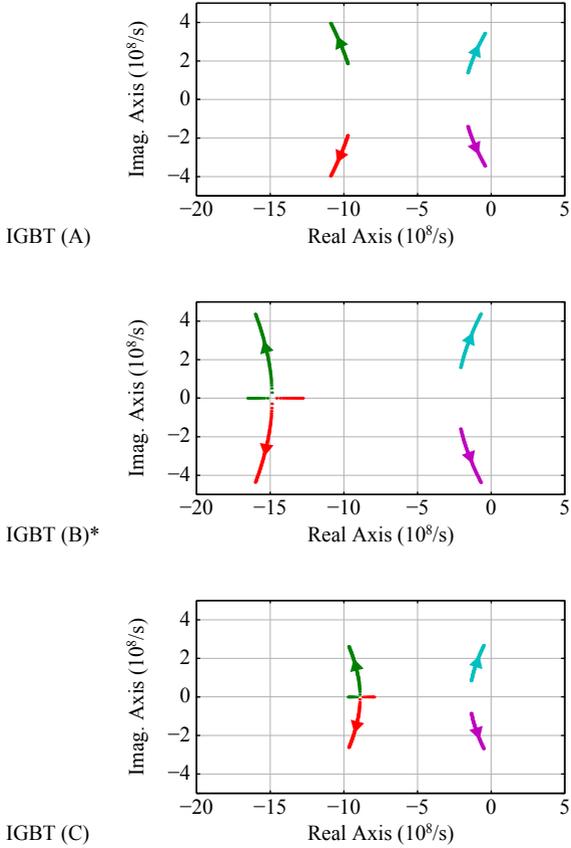


Figure 5.11: Root locus plots (poles only) of the dv_{CE}/dt control related to Fig. 5.7 for a decrease of the IGBT’s Miller capacitance C_{GC} from nominal value, cf. Table B.1, down to 25 % of the nominal value.

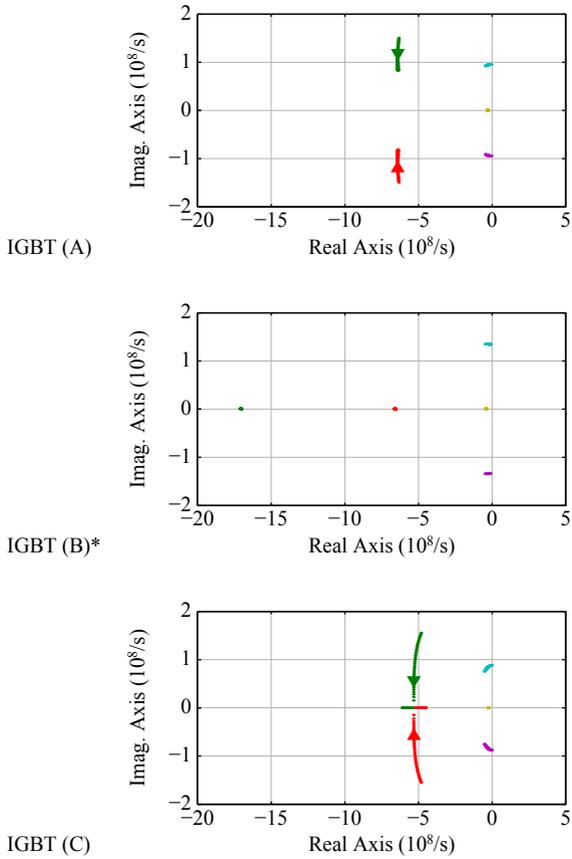


Figure 5.12: Root locus plots (poles only) of the di_C/dt control related to Fig. 5.9 for an increase of the IGBT's transconductance g_m from nominal value, cf. Table B.1, up to 4-times nominal value.

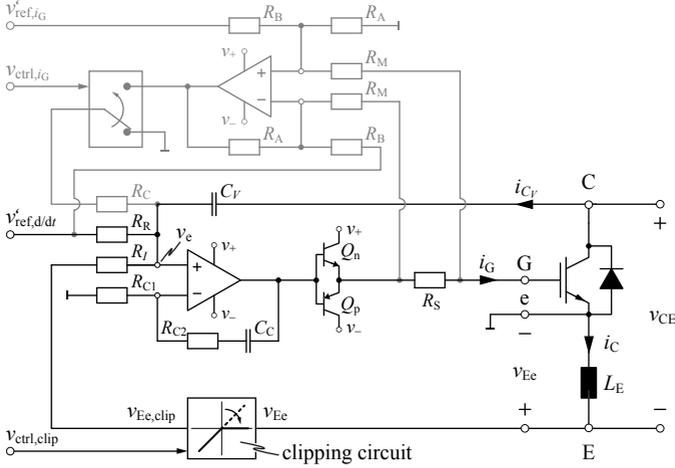


Figure 5.13: Circuit diagram of the proposed closed-loop di_C/dt and dv_{CE}/dt GD (shown in black) with a clipping circuit to block a negative di_C/dt feedback at turn-on as proposed in Section 5.3.4 including the gate current control (shown in gray).

5.3 Hardware Implementation

According to Figure 5.3, the implementation of the proposed closed-loop GD relies on di_C/dt , dv_{CE}/dt , and i_G feedback signals, the determination of the control error, a PI-controller and a highly dynamic and powerful output amplifier stage. The circuit diagram of the GD is presented in Figure 5.13 and will be discussed in the following.

5.3.1 Measurement Circuits

The measurement of the time derivative signals di_C/dt and dv_{CE}/dt features a duality. Feedback proportional to di_C/dt is derived as voltage drop across an inductance in the load current path, e.g. the emitter's parasitic bond wire inductance L_E as shown in Figure 5.13. The current of a capacitor connected in parallel to the voltage path, i.e. to the IGBT's collector terminal, is used as feedback signal proportional to dv_{CE}/dt . In practice, depending on the accuracy needs of the control, the tolerances of the parasitic inductance and the sensing capacitance could either be taken into account by selecting slightly lower di_C/dt

and/or dv_{CE}/dt set-points or be compensated by means of measurement and calibration of the sensing circuitry.

Neglecting any parasitic inductance in the auxiliary emitter connection and assuming a (+)-input voltage v_e of the operational amplifier being comparably small with regard to v_{CE} , the two feedback signals can be expressed as

$$v_{Ee} \approx -L_E \cdot di_C/dt, \quad (5.16)$$

$$i_{C_V} \approx C_V \cdot dv_{CE}/dt. \quad (5.17)$$

The gate current i_G can be measured as voltage drop across a very small, e.g. 100 m Ω , shunt resistor R_S in the gate current path.

5.3.2 Control Error Determination

For the determination of the control error v_e , i.e. for summing up the reference and the negative feedback signals, a passive network consisting of R_C , R_R , R_I and C_V can be employed as depicted in Figure 5.13. Thereby, the capacitor C_V of the dv_{CE}/dt feedback path acts as a low-pass filter for the reference, the di_C/dt and the gate current control signals. If this time constant, which in practice is typically in the nanosecond range, would be too high for a particular case, a buffer amplifier could be inserted to decouple the capacitor of the voltage slope feedback. For the determination of the gate current control error, an operational amplifier wired as multi-port subtractor can be employed, cf. Figure 5.13 (shown in gray).

Interval of Current and Voltage Slope Control

During the control of the current and voltage slopes the gate current control is turned-off via setting v_{ctrl,i_G} to logic low. In order to make the practical implementation of the control error signal generation as easy as possible, $R_C = R_R$ can be selected without giving up a significant degree of freedom. In that case the control error signal becomes

$$v_e \approx \underbrace{v'_{ref,d/dt} \cdot \frac{R_I}{R_R + 2R_I}}_{v_{ref,d/dt}} - \underbrace{L_E \cdot \frac{R_R}{R_R + 2R_I}}_{k_I} \cdot di_C/dt + C_V \cdot \underbrace{\frac{R_R \cdot R_I}{R_R + 2R_I}}_{k_V} \cdot dv_{CE}/dt. \quad (5.18)$$

This is in accordance with Figure 5.3, i.e. the control error equals the sum of the control reference signal and the current and voltage slope feedbacks with individual feedback gains.

Interval of Gate Current Control

In the interval of the gate current control, the d/dt -control reference signal $v'_{\text{ref},d/dt}$ must be cancelled out. This is achieved by setting $R_A/R_B = R_C/R_R$. Since the gate current control is only active in the turn-on and turn-off gate charge/discharge intervals, the di_C/dt and dv_{CE}/dt feedbacks are assumed to be zero. Under the consistent assumption of $R_C = R_R$ the control error signal during the gate current control becomes

$$v_e \approx \underbrace{v'_{\text{ref},i_G} \cdot \frac{R_I}{R_R + 2R_I}}_{v_{\text{ref},i_G}} - \underbrace{\frac{R_S \cdot R_A}{R_M} \cdot \frac{R_I}{R_R + 2R_I}}_{k_G} \cdot i_G \quad (5.19)$$

and is also in accordance with Figure 5.3.

5.3.3 Control Amplifier and Buffer Stage

The PI-controller can be implemented by means of a fast operational amplifier as shown in Figure 5.13, where the (ideal) gains result as

$$K_P = 1 + R_{C2}/R_{C1}, \quad (5.20)$$

$$K_I = 1/(R_{C1} \cdot C_C). \quad (5.21)$$

As output buffer amplifier, a push-pull emitter-follower (Q_n, Q_p) can be used to provide the high analog bandwidth and the needed current gain. In doing so, the parallel connection of lower current rated bipolar transistors is beneficial compared to using single devices in terms of current gain (typ. $h_{\text{FE}} > 100$) and analog bandwidth ($f_T > 100$ MHz). In addition, the operational amplifier must be able to operate at ± 15 V, feature a high bandwidth and provide comparably high current source and sink capabilities.

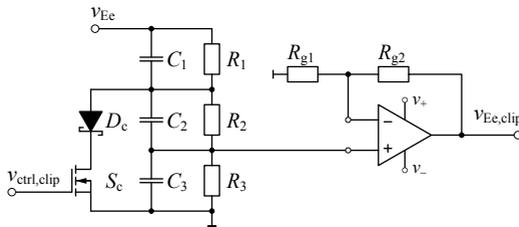


Figure 5.14: Schematic of the clipping circuit to restrict negative di_C/dt feedback during turn-on; S_c is closed for the whole turn-on interval.

5.3.4 Clipping of Negative di_C/dt Feedback at Turn-On

Ideally, the intervals of the current and voltage slopes at hard switching are not overlapping as has been illustrated in Section 5.1, which actually enables the proposed di_C/dt and dv_{CE}/dt control with simultaneously closed but subsequently active feedback loops. However, at turn-on the collector current i_C is decreasing after the peak reverse recovery current \hat{i}_{rr} , whereby the collector-emitter voltage already starts falling simultaneously. In order to attain an accurate control of dv_{CE}/dt in this interval, any negative di_C/dt feedback signal must be inhibited or, at least, be strongly attenuated.

This can be achieved by inserting the proposed clipping circuit shown in Figure 5.14 into the di_C/dt feedback path. In doing so, the switch S_c must be closed during the entire turn-on transients as shown in Figure 5.4 and Figure 5.15. The positive voltage of v_{Ee} , which occurs for a current decay, is thus restricted to the forward voltage drop of the diode D_c multiplied by the dividing ratio of the compensated voltage divider ($R_2||C_2$, $R_3||C_3$). In contrast, the negative voltage of v_{Ee} during current rise is not clipped since D_c blocks in this case. At turn-off, the clipping circuit is disabled, i.e. S_c is left open, and no clipping takes place. A schematic diagram of the corresponding trigger and feedback signals is shown in Figure 5.15.

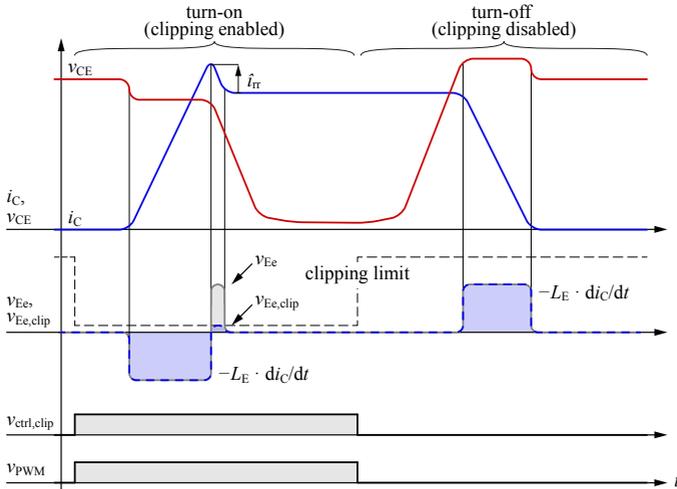


Figure 5.15: Schematic waveforms and according control signals of the clipping circuit at turn-on and turn-off.

5.4 Experimental Verification

5.4.1 Hardware Prototype

A prototype of the proposed closed-loop GD was developed, cf. Figure 5.16, that contains all described measurement and control circuits, in order to experimentally verify the closed-loop gate drive concept. The setting of the control reference signals and the multiplexers are triggered by a finite state machine running at 100 MHz implemented in a Complex Programmable Logic Device (CPLD) on the GD.

In the following, experimental results using the developed GD prototype are presented. All measurements are based on double-pulse tests and an experimental test setup consisting of a DC-link capacitor (up to 1 kV, 320 μ F), different half-bridge IGBT modules in the 1.2 kV class with current ratings of 300 – 450 A, an air-core inductor (53 μ H) as inductive load and a low inductance busbar interconnecting all components.

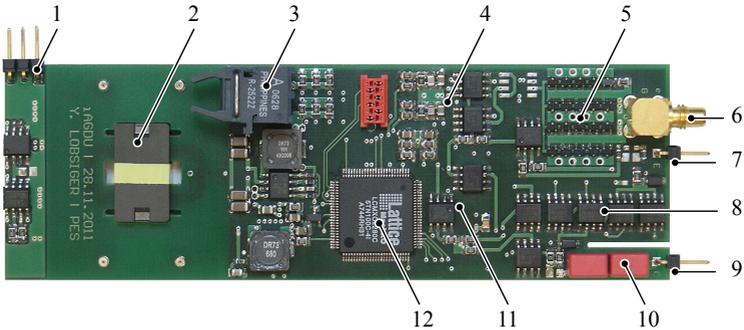


Figure 5.16: Prototype of the proposed closed-loop di_C/dt , dv_{CE}/dt , and i_G GD; dimensions of the PCB: 40 mm x 124 mm and / or 1.6 in x 4.9 in. 1: Power supply terminal; 2: isolation transformer; 3: optical link for PWM-in; 4: i_G control section; 5: output stage; 6: gate drive output; 7: power emitter connection terminal and di_C/dt feedback; 8: edge detection comparators; 9: collector connection terminal; 10: dv_{CE}/dt feedback; 11: di_C/dt and dv_{CE}/dt control section; 12: CPLD.

5.4.2 Independent Control of di_C/dt and dv_{CE}/dt

In a first series of measurements, the independent control of di_C/dt and dv_{CE}/dt of IGBT module (B)*, cf. appendix B, to individual set-point values is investigated for the a specific operating point, i.e. $v_{DC} = 600$ V and $i_L = 450$ A.

Fig. 5.17 shows the waveforms at the turn-on and turn-off transients for a variation of the di_C/dt set-point values and Fig. 5.18 shows the waveforms for a variation of the dv_{CE}/dt set-point values. Setting the different individual references of di_C/dt and dv_{CE}/dt was carried out by adjusting the feedback gains k_I and k_V , cf. Figure 5.3 (a), and (5.1) or (5.2), respectively. Based on these measurements, the possibility of an independent control of di_C/dt and dv_{CE}/dt to individual set-point values is experimentally verified. In practice, this enables a defined switching behavior of the IGBT inside the SOA and the direct implementation of a desired trade-off between switching losses and EMI.

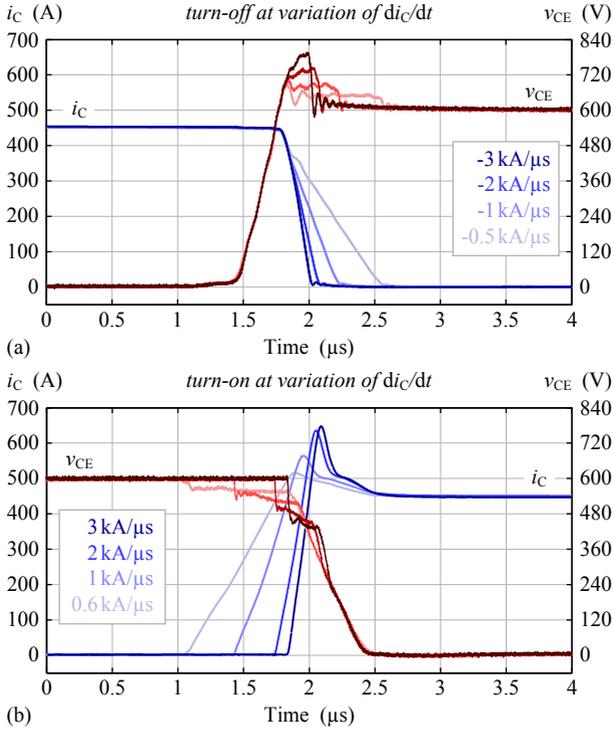


Figure 5.17: Measurement results at closed-loop switching of IGBT (B)* for different di_C/dt reference values. Variation of di_C/dt at (a) turn-off with $dv_{CE}/dt_{ref} = 2 \text{ kV}/\mu\text{s}$ and (b) turn-on with $dv_{CE}/dt_{ref} = -1 \text{ kV}/\mu\text{s}$.

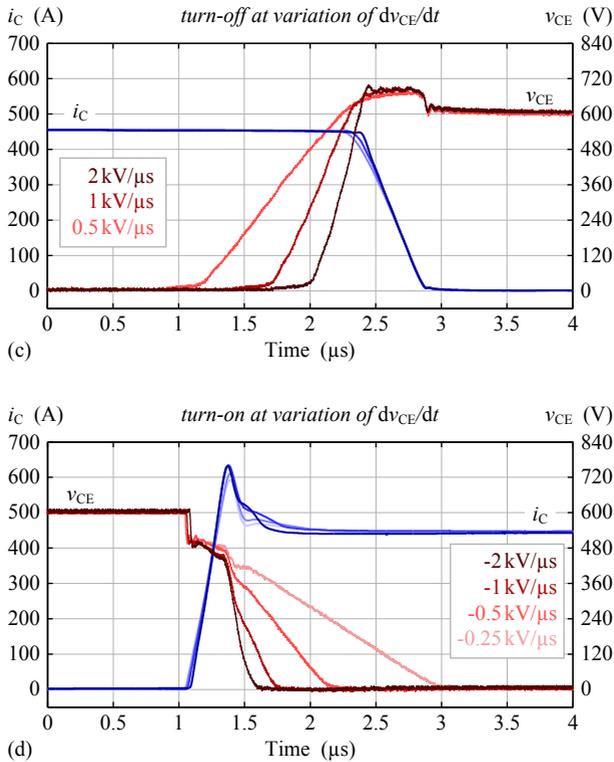


Figure 5.18: Measurement results at closed-loop switching of IGBT (B)* for different dv_{CE}/dt reference values. Variation of dv_{CE}/dt at (a) turn-off with $di_C/dt_{ref} = -1 \text{ kA}/\mu\text{s}$ and (b) turn-on with $di_C/dt_{ref} = 2 \text{ kA}/\mu\text{s}$.

5.4.3 Load Current Compensation

In a next step, the natural closed-loop compensation of changes in the operating point, i.e. the load current level, is investigated and the natural transition from the voltage to the current slope control during turn-on and vice versa during turn-off is illustrated.

In Figure 5.19 the turn-off and turn-on waveforms for different load current levels are depicted. In both cases the GD applies higher gate voltages v_{Ge} to the IGBT during the voltage slope for higher load current levels. This is in fact needed for achieving the desired dv_{CE}/dt , cf. Figure 2.4. Furthermore, it is evident that, independent of the load current level, the gate voltage performs a step exactly at the transition point between the voltage and the current slope without any actively triggered change in the GD, i.e. the claimed natural transition between the current and voltage control is working as intended during turn-off as well as during turn-on. Another benefit of the proposed gate drive concept is the very fast drop of the gate voltage to the negative gate drive voltage, v_- , as soon as the collector current reaches the tail current level during turn-off.

5.4.4 Comparison to Resistive Gate Driver

In order to comprehensively illustrate the benefits of the proposed closed-loop GD regarding switching losses, a comparison to a passive, i.e. resistive GD is provided in the following. For the experimental analysis the low-side switch of a 1.2 kV, 300 A IGBT half-bridge module (Infineon FF300R12MS4) in EconoDUAL housing has been selected, in order to additionally verify the GD for a different type of semiconductor and/or housing.

In a first measurement series, the gate resistors of the passive GD were adjusted for a maximum di_C/dt of ca. $\mp 2 \text{ kA}/\mu\text{s}$ for turn-off and turn-on. Thereby, a dv_{CE}/dt of roughly $\pm 1 \text{ kV}/\mu\text{s}$ results, cf. Figure 5.20 (a). The same values for di_C/dt and dv_{CE}/dt have been set with the closed-loop GD, cf. Figure 5.20 (b). For both GDs, similar current slopes and accordingly similar diode peak reverse recovery currents, turn-off overvoltages, and also switching losses result. Accordingly, if di_C/dt and dv_{CE}/dt of the closed-loop GD are set to exactly what a passive GD provides, no significant gain concerning switching losses is achieved.

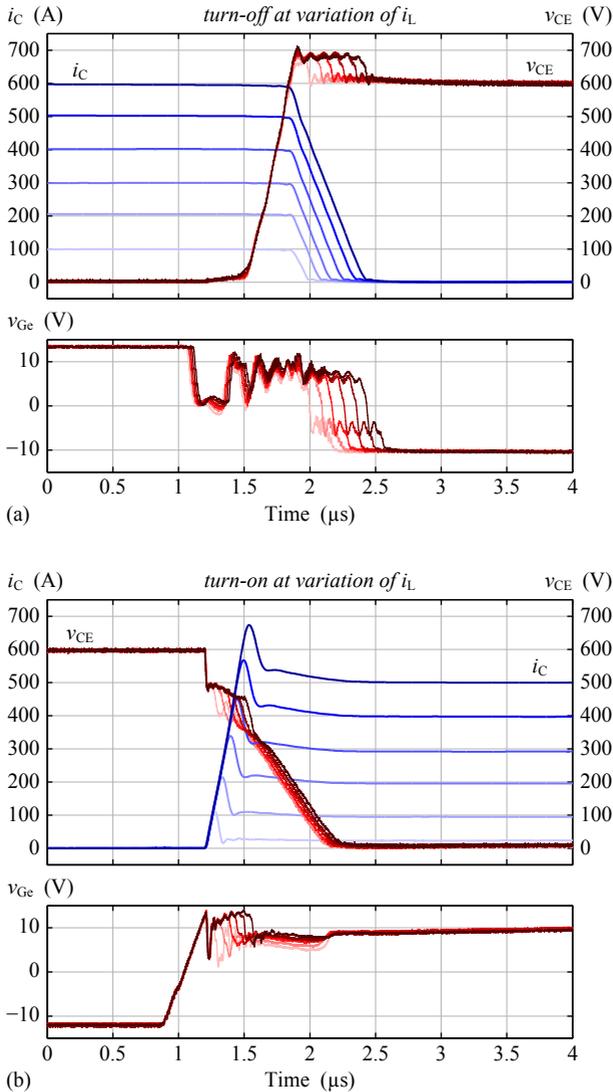


Figure 5.19: Measured waveforms at hard switching for different levels of the load current. (a) Turn-off at $dv_{CE}/dt_{ref} = 2 \text{ kV}/\mu\text{s}$ and $di_C/dt_{ref} = -1 \text{ kA}/\mu\text{s}$; (b) turn-on at $di_C/dt_{ref} = 2 \text{ kA}/\mu\text{s}$ and $dv_{CE}/dt_{ref} = -0.5 \text{ kV}/\mu\text{s}$.

In a next measurement series, the gate resistors of the passive GD were adjusted for a maximum di_C/dt of ca. $\mp 1 \text{ kA}/\mu\text{s}$. Thereby, a dv_{CE}/dt of roughly $\pm 0.5 \text{ kV}/\mu\text{s}$ results, cf. Figure 5.21 (a). The same di_C/dt was set with the closed-loop GD, however, contrary to the resistive GD, the dv_{CE}/dt can be selected independent of the di_C/dt and has been set to $\pm 2 \text{ kV}/\mu\text{s}$ in this case, cf. Figure 5.21 (b). For both GDs, similar current slopes and accordingly similar diode peak reverse recovery currents and turn-off overvoltages result. However, due to the faster voltage slope, the switching losses of the closed-loop GD are about halved in comparison to the resistive GD. Therefore, the ability of setting di_C/dt and dv_{CE}/dt individually from each other enables a significant reduction of the switching losses in cases, where the gate resistors of a passive GD cannot be reduced due to restrictions of SOA operation or EMI.

5.4.5 Control of Different IGBT Modules

The stability analysis performed in this chapter, cf. Section 5.2, showed that the bandwidth and also the stability of the closed-loop control highly depend on the parasitic inductance in the gate loop, i.e. a low inductance in the gate loop is beneficial for a fast and stable control. In order to verify this aspect, in the following an experimental comparison of the closed-loop control of three IGBT modules in the 1.2 kV, 400 – 450 A class from different manufacturers, i.e. modules (A), (B)*, and (C) shown in appendix B, is performed.

Fig. 5.22 shows the closed-loop control of the IGBT modules at turn-on for a variation of the load current i_L . In accordance with the stability analysis of Section 5.2, IGBT module (B)* shows the most accurately controlled current and voltage values. Slight oscillations are observable for module (A) and the controllability of module (C) is most demanding due to the high gate loop inductance. This result is in accordance with the expected behavior, i.e. for larger gate loop inductance L_{gl} a high PI-controller gain must be selected to achieve a fast control, which in turn causes a less accurate and / or less stable control.

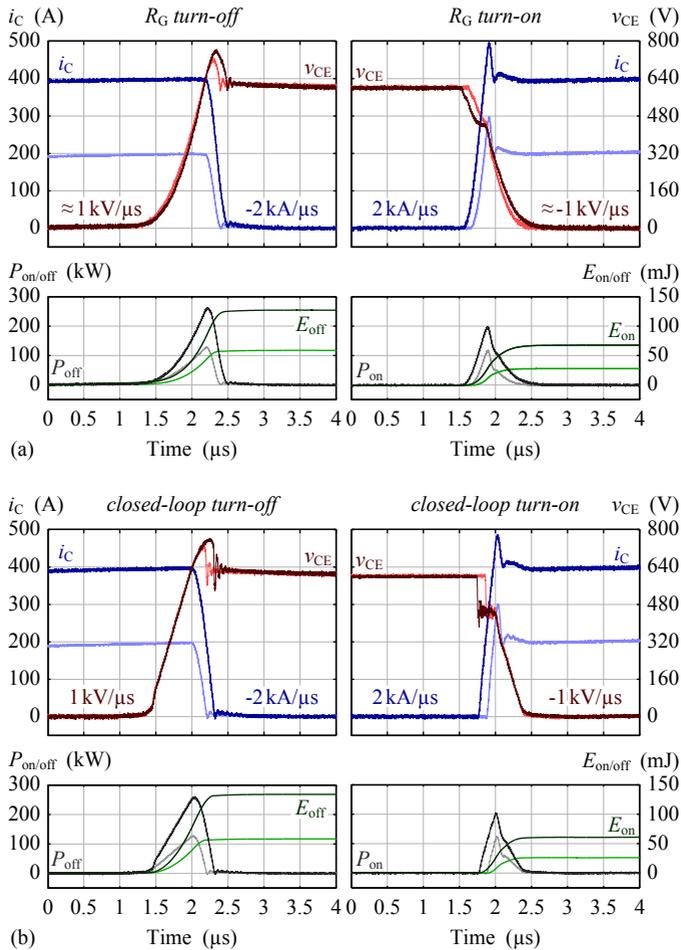


Figure 5.20: Experimental comparison of the turn-off and turn-on voltage and current waveforms and switching losses for (a) a resistive GD and (b) the proposed closed-loop GD.

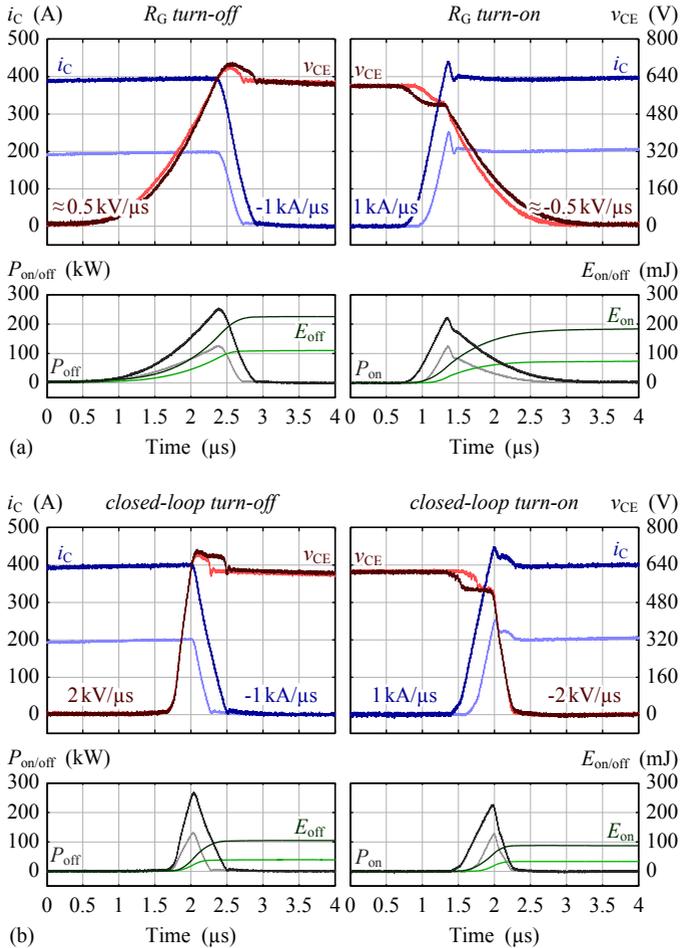


Figure 5.21: Experimental comparison of the turn-off and turn-on voltage and current waveforms and switching losses for (a) a resistive GD and (b) the proposed closed-loop GD.

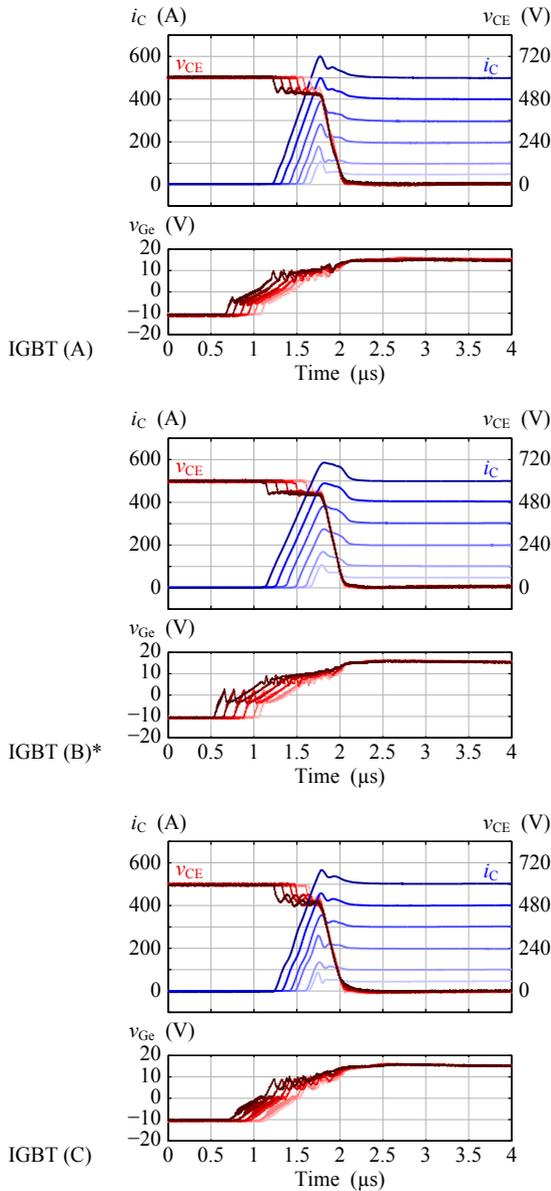


Figure 5.22: Measured closed-loop controlled turn-on waveforms at $1 \text{ kA}/\mu\text{s}$, $-2 \text{ kV}/\mu\text{s}$ of the IGBT modules (A), (B)* and (C).

5.4.6 Closed-Loop Control Using SiC Diodes

In a last series of measurements, the proposed closed-loop GD was also tested in combination with the low-side switch of a 1.2 kV, 300 A IGBT half-bridge module in EconoDUAL housing containing SiC-diodes (Infineon FF300R12MS4F_ENG), and compared to an IGBT half-bridge module in the identical housing comprising conventional Si-diodes (Infineon FF300R12MS4). The corresponding measurement results are shown in Figure 5.23.

It can be summarized, that the control is accurate and stable for both the conventional module as well as for the module equipped with SiC-diodes. At the IGBT's turn-off transients, absolutely no difference is noticed between the two modules. During the IGBT's turn-on, as expected, the SiC diode does not show any reverse recovery effect, but its abrupt blocking excites a small ringing between the commutation loop stray inductance and the parasitic capacitance of the diode.

5.5 Summary

In this chapter, a closed-loop IGBT GD providing independent di_C/dt and dv_{CE}/dt control was presented and analyzed in terms of control stability. Furthermore, a possible hardware implementation was shown and a corresponding prototype was realized. By means of this prototype, the gate drive concept successfully passed various experimental verifications using several different IGBT modules.

The GD permits to adjust the current and voltage slopes according to set-point values largely independent of nonlinearities or parameter variations of the IGBT and the load. Therewith, a degree of freedom for the converter design is gained, which allows to ensure an operation in the SOA and a defined trade-off between switching losses and EMI independent of the load current level, the DC-link voltage or the junction temperature of the employed IGBTs. By means of using only simple passive measurements for the generation of the feedback signals and a single operational amplifier as PI-controller, high analog control bandwidth is achieved enabling the application of a closed-loop GD even for switching times in the sub-microsecond range.

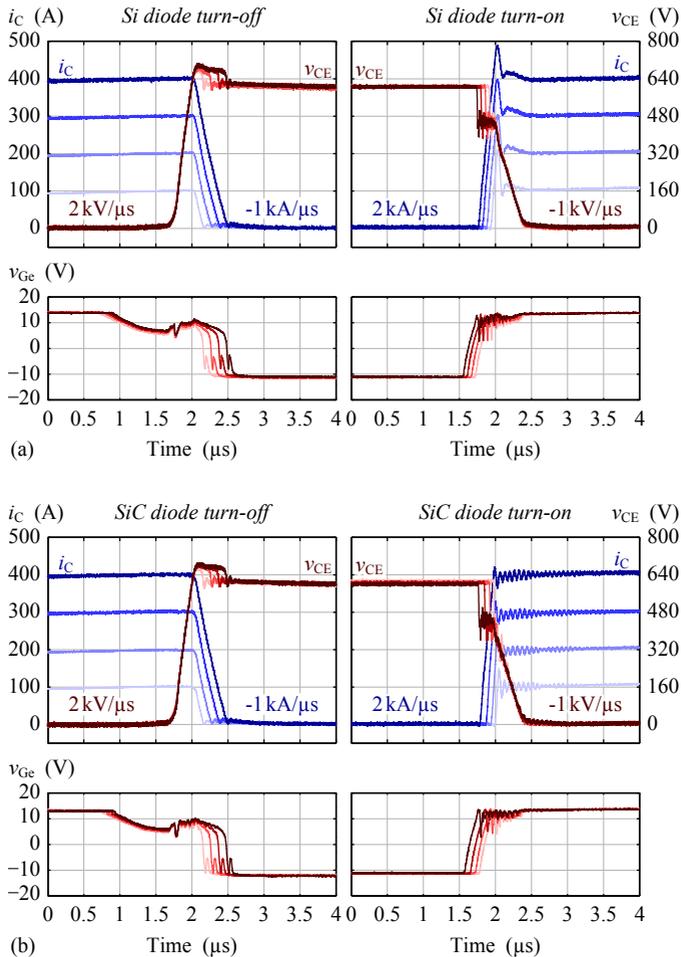


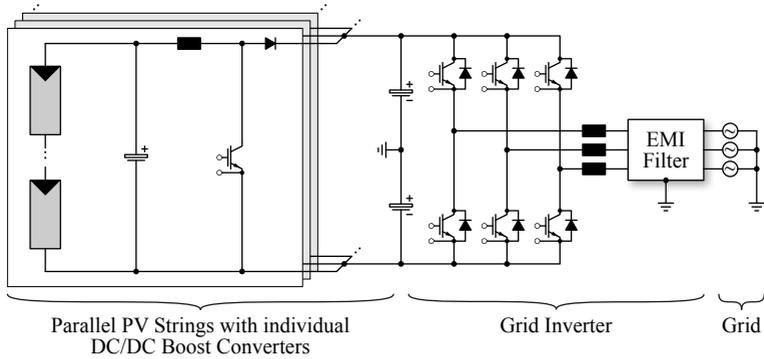
Figure 5.23: Measurement results for (a) the conventional Si-diode Si-IGBT module and (b) the SiC-diode Si-IGBT module. Turn-off at $-1 \text{ kA}/\mu\text{s}$, $2 \text{ kV}/\mu\text{s}$ and turn-on at $2 \text{ kA}/\mu\text{s}$, $-1 \text{ kV}/\mu\text{s}$.

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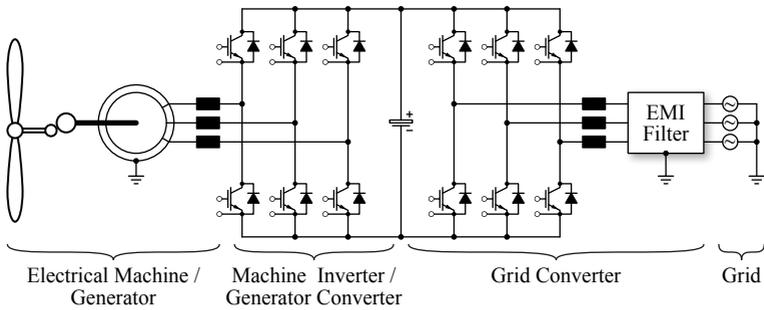
Closed-Loop Gate Driver for Bridge Leg Configurations

IN the previous chapter, a highly dynamic closed-loop IGBT gate drive concept was proposed which enables an individual control of di_C/dt and dv_{CE}/dt at hard switching. This allows to ensure a defined trade-off between switching losses and EMI, and a maximum utilisation of the current-carrying capacity and voltage blocking capability within the SOA of the IGBT. So far, this concept was proposed and investigated in the context of a chopper configuration, i.e. the connection of an IGBT and a freewheeling diode to a voltage DC-link with an inductive load/source connected in between the two semiconductors, cf. Figure 2.3. Typical application examples of this type of interconnection of semiconductors and a load are AC/DC PFC rectifiers or unidirectional DC/DC converters such as the conventional buck or boost converters, cf. Figure 6.1 (a).

In a multitude of industrial applications, e.g. for variable speed drive systems, or for the control and interfacing of renewable energy sources such as wind or solar power to the mains (cf. Figure 6.1), however, single- or multi-phase bridge leg configurations of the semiconductors are required in order to also allow a phase shift of the AC output voltages and currents. Thereby, two complementary IGBTs with anti-parallel freewheeling diodes are connected across a DC-link for feeding an inductive, i.e. current impressing, load according to the corresponding equivalent circuit depicted in Figure 6.2. An interlocking of the two complementary IGBTs is inevitable for shoot-through prevention and is typically ensured by a preset dead-time t_d between the individual PWM signals [12].



(a)



(b)

Figure 6.1: Typical application examples of inductive load switching IGBTs in chopper and bridge leg configuration [3]. (a) String boost converters for industrial PV applications (representing the chopper configuration) and three-phase DC/AC grid-tie inverter. (b) Three-phase two-level voltage source inverters in back-to-back configuration as AC/AC converter for wind-turbine generators or drive applications.

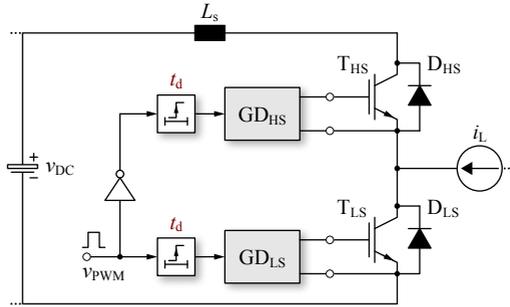


Figure 6.2: Application of IGBTs T_{LS} and T_{HS} with anti-parallel freewheeling diodes D_{LS} and D_{HS} in a bridge leg configuration. An interlocking of the IGBTs is typically ensured by delaying the turn-on PWM commands by a preset dead-time t_d [12].

In contrast to GDs for chopper configurations, i.e. only one IGBT and a complementary diode as used e.g. in buck or boost converters, the needed functionalities of a GD for IGBTs in bridge leg configuration are manifold as shown in the overview diagram of Figure 6.3. In addition to switching the IGBT along a defined voltage / current trajectory, the GD must suppress crosstalk from the switching of the complementary semiconductor [12,26,73,74], needs to detect and safely turn-off different types of short circuits (SCs) [75–79], has to provide an appropriate status feedback for a reliable overall converter operation, and should minimize the interlock dead-time in order to maintain short delays and undistorted volt-seconds at the bridge leg’s output terminal [73,80–85].

Over the last two decades, substantial work on concepts and circuits for optimizing the IGBT’s switching behavior with regard to switching losses and EMI has been carried out and published in literature as summarized in Chapter 4. Though the best performance regarding the shaping of the IGBT’s switching trajectories is attained with closed-loop gate drive topologies, nearly all such concepts have been investigated and tested for chopper circuits only. However, due to the coupling of the two IGBTs in a bridge leg configuration concerning voltage and current ($v_{CE,LS} + v_{CE,HS} = v_{DC}$, neglecting the commutation loop inductance; $i_{C,LS} - i_{C,HS} = i_L$, neglecting parasitic capacitive currents), special care must be taken when extending such a GD with additional feedback circuits into a closed-loop gate drive concept for bridge leg configurations.

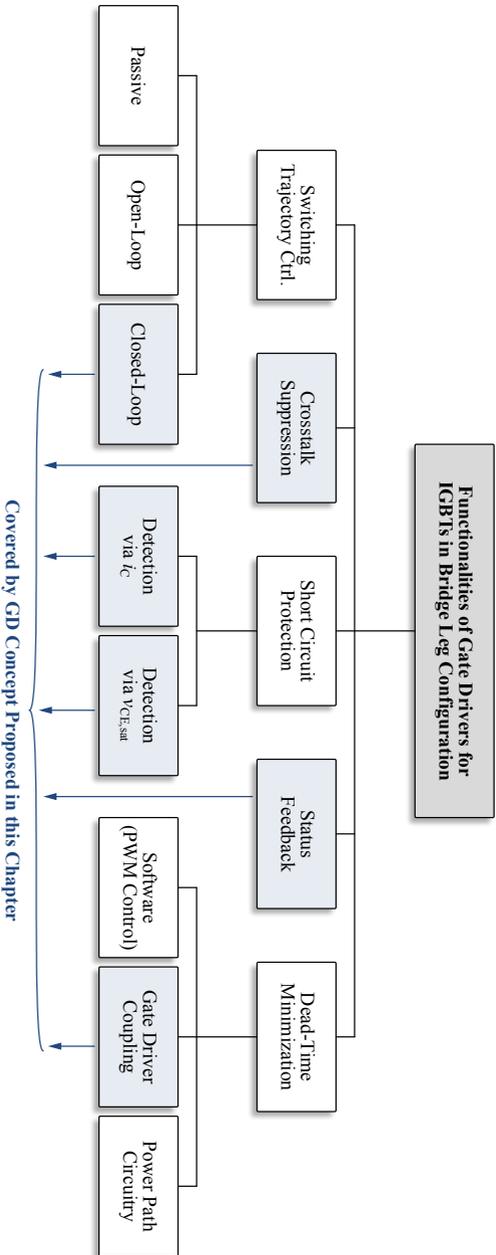


Figure 6.3: Overview diagram of the main requirements for GDs for IGBTs in bridge leg configuration and associated implementation possibilities. The gate drive concept proposed in this chapter covers the highlighted tasks and implementations.

In this chapter, the closed-loop GD proposed for IGBTs in chopper configurations, cf. Chapter 5, is extended for IGBTs in bridge leg configuration in order to provide the needed functionality according to Figure 6.3. Based on an analysis of the characteristic turn-on and turn-off switching transitions under normal operation, in Section 6.1.2 auxiliary circuits are added to prevent crosstalk and to guarantee a robust switching. In order to ensure a safe operation at minimal interlock dead-time between the two complementary power transistors (delay time between a turn-off and the complementary turn-on command) a reciprocal interlocking and active dead-time minimization is proposed in Section 6.2. Subsequently, SC detection and turn-off methods for different types of SCs and corresponding extensions of the closed-loop GD are described in Section 6.3. Section 6.4 then gives an overview of the final closed-loop bridge leg IGBT gate drive concept proposed in this thesis. A comprehensive experimental verification is finally presented in Section 6.5 by means of a hardware demonstrator employing a 1.2 kV, 300 A half bridge IGBT module. The chapter concludes with a summary of the main functionalities of the proposed GD and gives an outlook on potential applications.

6.1 Closed-Loop Gate Driving in Normal Operation

The bridge leg arrangement of two IGBT / diode cells allows, in contrast to a chopper configuration, to actively connect the output either to the positive (+) or to the negative (-) rail of the DC-link irrespective of the direction of the load current i_L by means of turning-on either the high-side or the low-side IGBT. At a transition from (+) to (-) or vice versa, the conducting IGBT is turned-off first and the complementary IGBT is turned-on thereafter considering a dead-time in order to prevent a cross-conduction current or transient short circuit of the DC-link.

The resulting current paths in the bridge leg before, during and after the different possible switching transitions, i.e. from (+) to (-) and (-) to (+) output voltage, are illustrated in Figure 6.4 and Figure 6.5 for a positive and negative direction of the load current i_L . The corresponding waveforms of the high-side and low-side semiconductors are shown as well. Based on this overview and due to symmetry considerations two basic types of switching transitions can be distinguished.

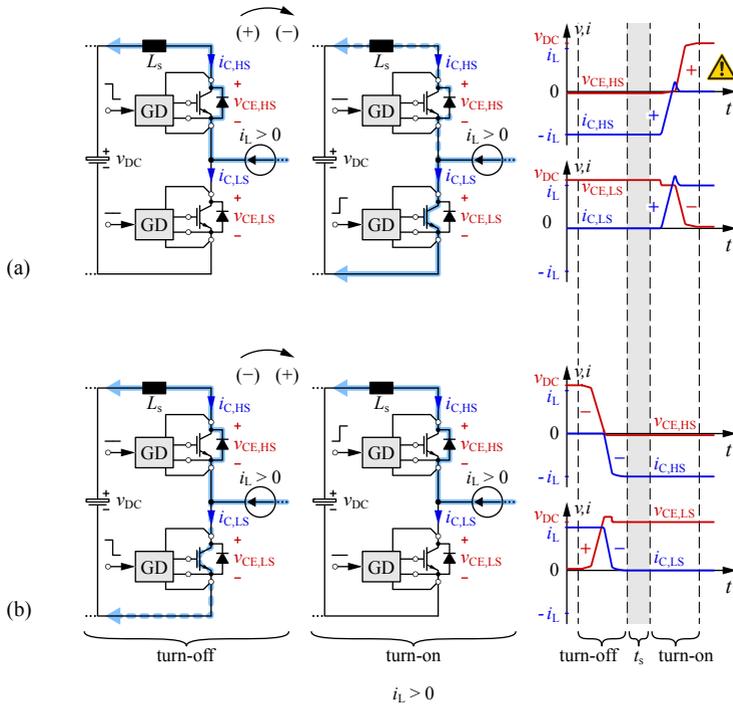


Figure 6.4: Current paths and corresponding schematic waveforms of the IGBT/diode currents ($i_{C,LS/HS}$) and voltages ($v_{CE,LS/HS}$) at the switching transients of a bridge leg for positive load current i_L . (a) transition from positive (+) to negative (-) output voltage; (b) transition from (-) to (+) output.

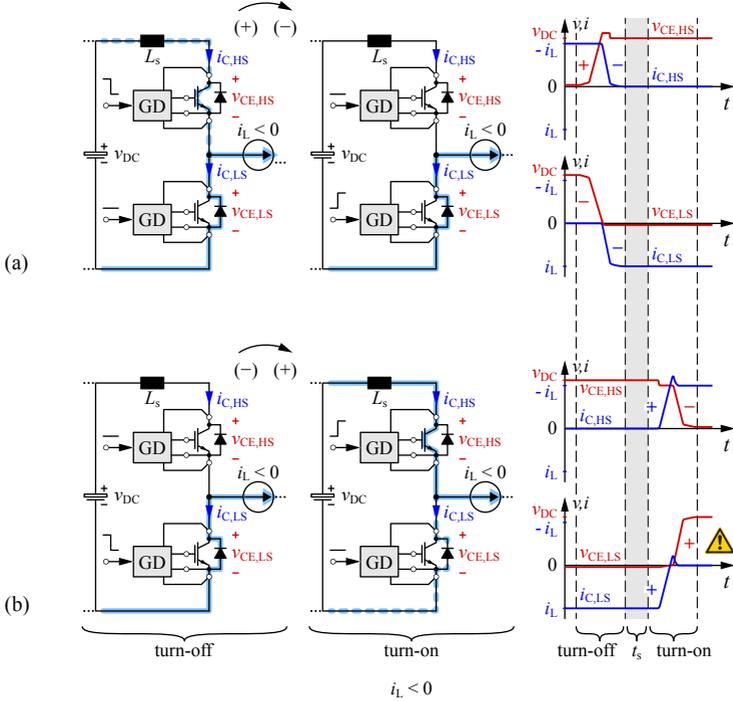


Figure 6.5: Current paths and corresponding schematic waveforms of the IGBT/diode currents ($i_{C,LS/HS}$) and voltages ($v_{CE,LS/HS}$) at the switching transients of a bridge leg for negative load current i_L . (a) transition from positive (+) to negative (-) output voltage; (b) transition from (-) to (+) output.

Switching Transition Type (A) corresponds to Figure 6.4 (a) and Figure 6.5 (b), where the diode is conducting before the antiparallel IGBT is turned-off. Accordingly, this IGBT is turning-off soft, i.e. at zero current, and the load current only commutates as soon as the complementary IGBT is turned-on.

Switching Transition Type (B) corresponds to Figure 6.4 (b) and Figure 6.5 (a), where the IGBT is conducting before being turned-off. At its turn-off, the current commutates to the diode of the complementary IGBT which performs, subsequently, a soft turn-on.

6.1.1 Crosstalk

In practice, however, the (hard) switching of an IGBT / diode cell in a bridge leg always affects the complementary (turned-off) cell because of their direct coupling, i.e. because the sum of their voltages always equals the DC-link voltage minus the voltage drop across the stray inductance,

$$v_{CE,LS} + v_{CE,HS} = v_{DC} - L_s \cdot \frac{di_{C,LS/HS}}{dt}, \quad (6.1)$$

and their difference in current levels is always equal to the load current,

$$i_{C,LS} - i_{C,HS} = i_L. \quad (6.2)$$

This is especially a problem for fast dv_{CE}/dt transients, cf. Figure 6.6 (a). Here, the voltage slope at turn-on of the high-side transistor causes a capacitive current in the Miller capacitance of the complementary IGBT which leads to a charging of C_{GE} of the low-side switch (crosstalk) [73, 86]. As a result, the low-side IGBT in Figure 6.6 (a) might temporarily be turned-on which causes an unwanted current across the DC-link and leads to additional switching losses or even a short circuit. In practice, this crosstalk is suppressed by different means [26, 74, 86] as listed below.

Gate Capacitance Additional gate capacitance absorbs the charge injected due to the Miller current and reduces the rate of gate charging. However, this capacitance also reduces the di_C/dt during switching in normal operation, cf. (2.15) or (2.35), and is, thus, often not desired.

6.1. Closed-Loop Gate Driving in Normal Operation

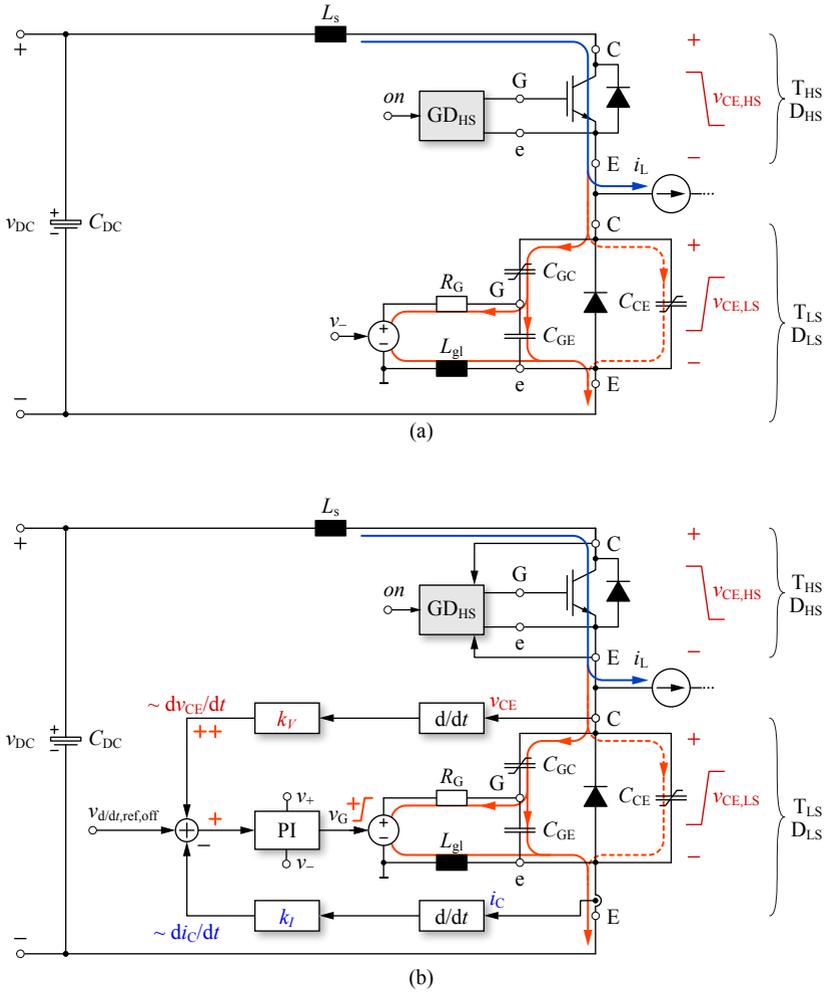


Figure 6.6: Current paths for switching transition type (A) according to Figure 6.5 (b), i.e. during the voltage decay at hard turn-on of T_{HS} once the current has already commutated from D_{LS} to T_{HS} (diode reverse recovery current of D_{LS} neglected). Situation for (a) a resistive GD and (b) the proposed closed-loop GD.

Gate Drive Impedance The lower the gate loop impedance, i.e. R_G and L_{Ge} , the larger the share of the Miller current, which is absorbed by the GD. In practice, hence, R_G is typically shorted in off-state by means of an additional transistor. Such type of circuitry is known as Miller clamping [12].

Negative Gate Drive Output Voltage As the Miller clamping is limited by the internal gate resistance and inductance of the IGBT module, a negative gate drive output voltage in the turn-off state can be used to increase the gap to the threshold voltage and to prevent a parasitic turn-on [12].

As has been shown in Chapter 5, the proposed closed-loop GD also asks for a very small gate loop inductance for attaining a high control bandwidth, uses only a very low-ohmic gate resistor for the gate current measurement, and is beneficially operated with a negative gate drive turn-off output voltage. From this point of view, the prerequisites for a safe and robust operation concerning crosstalk and / or cross-conduction are given. In contrast to a passive GD, however, the closed-loop GD comprises additional feedback loops acting on the gate, i.e. a positive dv_{CE}/dt feedback and a negative di_C/dt feedback, which may increase the risk of a parasitic turn-on of a turned-off IGBT as described in the following.

As depicted in Figure 6.6 (b) for switching transition type (A), e.g. Figure 6.5 (b), in addition to the gate charging by the Miller current at the fast rise of v_{CE} , the positive dv_{CE}/dt feedback of the closed-loop GD may lead to an increase of the gate drive output voltage v_G via the PI-controller and, hence, to a parasitic turn-on of T_{LS} . This is the case if the absolute values of the positive and negative dv_{CE}/dt references of both GDs in the bridge leg are different, or could be caused by tolerances of the individual reference signals and the feedback gains. If e.g. the slope of $v_{CE,LS}$, which is defined by the GD and switching of the HS IGBT, would be higher than the reference value set for the LS IGBT for turn-off, the LS GD would apply a positive gate voltage in order to slow down the switching process. Due to the negative feedback of di_C/dt , the change of current has no impact via the GD, here.

At switching transition type (B), e.g. Figure 6.5 (a), the negative dv_{CE}/dt across the turned-off IGBT T_{LS} leads to a Miller current in opposite direction than shown in Figure 6.6 (b) and causes a discharging of the gate. Hence, a clamping of the gate to the negative gate drive

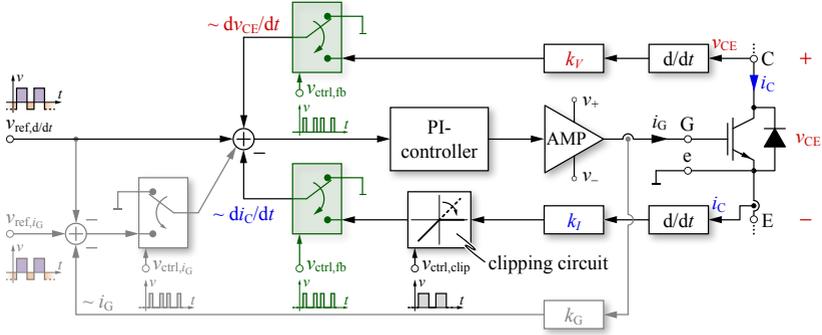


Figure 6.7: Extension of the block diagram of the closed-loop GD for chopper circuits, cf. Figure 5.3, in order to ensure applicability for bridge leg circuits with additional switches to temporarily disable the dv_{CE}/dt and the di_C/dt feedbacks. Please refer to Section 5.3 for the corresponding hardware implementation.

output voltage level might be needed to protect the gate from exceeding the negative limit. Due to the positive feedback of dv_{CE}/dt , here, the voltage step has no impact via the feedback of the GD. On the other hand, while the current decays, the negative di_C/dt feedback of the closed-loop GD may lead to an increase of the gate drive output voltage v_G via the PI-controller and, hence, to a turn-on of the IGBT. At this point in time, however, the turning-off IGBT T_{HS} is already blocking the full DC-link voltage and therefore, fortunately, a parasitic turn-on of T_{LS} would not lead to a cross-conduction.

6.1.2 Extensions of the GD for Bridge Leg Applications

As a consequence of the foregoing considerations, at least the dv_{CE}/dt feedback of the closed-loop GD must be disabled as soon as the IGBT enters the blocking state in order to maintain a safe operation of the IGBT. As will be shown in Section 6.3, a disabling of the di_C/dt feedback is needed as well to safely turn-off a particular type of short circuit. In practice, as illustrated in Figure 6.7, the deactivation of the di_C/dt and dv_{CE}/dt feedback signals can be implemented by means of high-speed (video) multiplexers.

For this purpose, the point in time at which the IGBT reaches blocking ability needs to be detected with an additional circuitry. Measuring the collector current or the collector-emitter voltage is not sufficient [82] since a transistor can either be in the on-state or in the off-state without current flow, e.g. when the antiparallel diode is conducting. A very simple solution for an IGBT is to test whether the gate voltage v_{Ge} is on a level below the threshold voltage $v_{Ge,th}$, equal to testing the absence of a base current for a BJT [82].

6.2 Interlocking and Dead-Time Minimization

Shoot-through, i.e. the simultaneous conduction of both transistors in a bridge leg, has to be strictly prevented. If this would not be the case the high currents resulting for cross-conduction would cause high switching losses and would potentially lead to switching trajectories leaving the IGBTs' SOA or to a thermal destruction of the power semiconductors.

A very simple and common solution to ensure an interlocking of the two complementary IGBTs is to insert a dead-time t_d between the turn-off and turn-on commands of the upper and lower IGBTs [12], cf. Figure 6.2. This is typically done in the PWM controller by delaying the particular turn-on commands of each transistor by a fixed time interval $t_d \gg t_{d,off} - t_{d,on}$ as shown in Figure 6.8 (c). The determination of t_d must consider the maximum possible delay $t_{d,off}$ until the conducting IGBT reaches the blocking state and the minimum possible delay $t_{d,on}$ until the blocking IGBT starts conducting for all operating conditions, i.e. considering the variations of the level and the sign of the load current, the DC-link voltage or the junction temperature, as proposed in [87]. In addition, a safety margin is typically added to guarantee a safe operation.

In the dead-time interval, i.e. if neither one nor the other IGBT is turned-on, the output voltage of the bridge leg v_{out} is only defined by the direction of the load current i_L as shown in Figure 6.8 (a,b). As a result, the volt-seconds of the output voltage are not in accordance to the reference profile $v_{out,ref}$ and /or an output voltage distortion $v_{out,err}$ occurs which depends on the direction of the load current i_L . This error

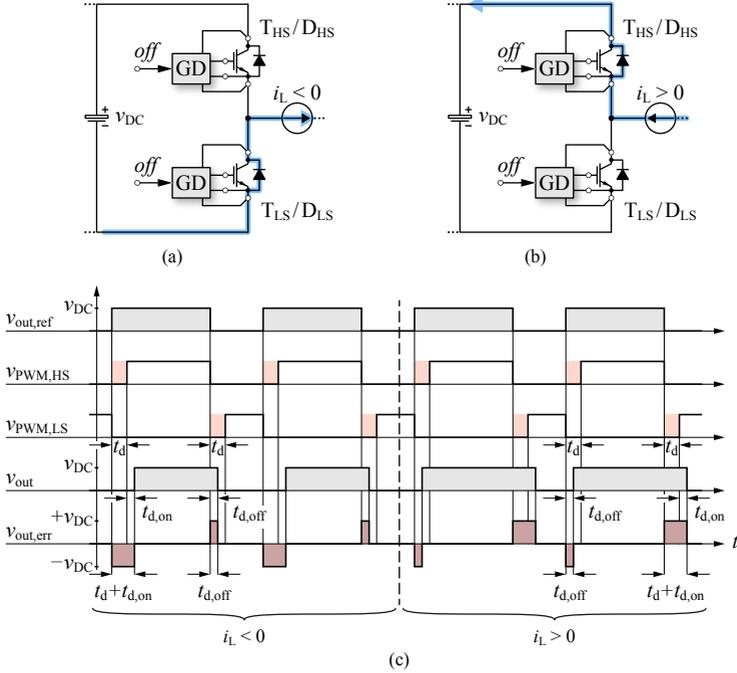


Figure 6.8: Current paths in the dead-time interval, i.e. both IGBTs are in the blocking state, for (a) negative and (b) positive direction of the load current. (c) Output voltage reference $v_{out,ref}$, corresponding switching signals $v_{PWM,HS}$ and $v_{PWM,LS}$, resulting output voltage v_{out} in dependency of the direction of the load current, output voltage error $v_{out,err}$, dead-time t_d , turn-on delay $t_{d,on}$, and turn-off delay $t_{d,off}$.

can be averaged over a switching period T_s ,

$$\bar{v}_{out,err} = \begin{cases} +v_{DC} \cdot \frac{t_d + t_{d,on} - t_{d,off}}{T_s} & i_L > 0 \\ -v_{DC} \cdot \frac{t_d + t_{d,on} - t_{d,off}}{T_s} & i_L < 0, \end{cases} \quad (6.3)$$

whereby the absolute value within a switching period T_s is equal for both signs of i_L . This dependency of switching delay on the direction of the load current can also be observed in Figure 6.8 (c). Even though the error of a single pulse is small, the accumulated errors affect the generated output voltage fundamental especially for higher switching frequencies and could e.g. lead to a distorted current waveform and

torque pulsations if supplying an electrical machine [88], or could cause the saturation of a transformer. For these reasons the output voltage distortion must eventually be compensated [88–93].

In order to potentially avoid this compensation and/or to minimize the output voltage distortion, the dead-time t_d should ideally be adapted to the actual switching condition. According concepts have already been proposed (cf. Figure 6.3), and are illustrated in Figure 6.9 and briefly discussed in the following.

A first possibility is to insert a diode in series to the low-side switch and to make a connection to the gate terminal of the high-side transistor [80, 81] as shown in Figure 6.9 (a). In high-power applications, however, the additional losses evoked in this diode are typically unwanted and a defined turn-off behavior of T_{HS} is not possible. Another option is to implement a reciprocal (two-way) interlocking of the two GDs [73, 82–85] according to Figure 6.9 (b) whereby the blocking ability or the conduction state of the semiconductors is detected and communicated between the GDs. Thereby, a turn-on is triggered as soon as the complementary IGBT obtained blocking ability, i.e. the turn-on delay is adapted to the turn-off time. A last method is to measure the load current and to adapt the switching times of the two IGBTs in a central PWM controller according to predefined delay times [88–93] as depicted in Figure 6.9 (c).

6.2.1 Reciprocal Interlocking of Closed-Loop Gate Driver

Given that the closed-loop GD is already equipped with an off-state detector, cf. Section 6.1.2, which is needed to trigger the deactivation of the dv_{CE}/dt and di_C/dt feedback signals at entering the blocking state, a reciprocal interlocking can simply be implemented as shown in Figure 6.9 (b) by only adding two signal isolators in between both GDs of a bridge leg. In addition, this circuit provides a redundancy to the interlocking by means of dead-times and thus also allows to apply directly inverted PWM gate signals to the low-side and high-side GDs, i.e. the number of gate signals, that need to be generated and distributed from the main PWM control unit, can be halved in case a simultaneous turn-off state of both transistors is not needed at e.g. startup.

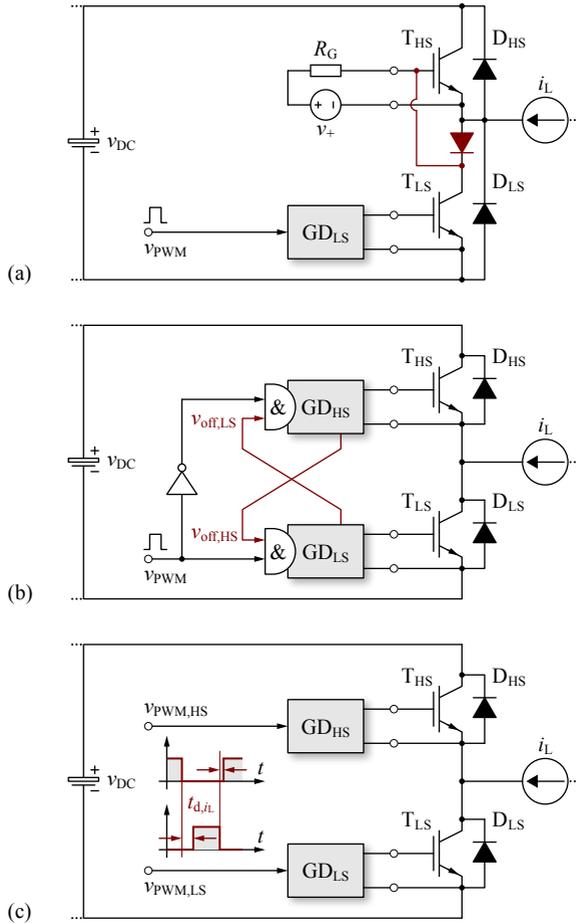


Figure 6.9: Overview of shoot through prevention and dead-time minimization techniques. (a) Passive circuitry in the power path and connection to the gate enabling a self triggered high-side IGBT; (b) reciprocal interlocking of the IGBTs via signal coupling of the GDs; (c) individual PWM signals with dead-times t_{d,i_L} online controlled in software according to the measured load current i_L .

6.3 Short Circuit Detection and Turn-off

At normal operation of the proposed closed-loop GD, a safe switching of the IGBTs in a bridge leg is guaranteed through reciprocal interlocking of the complementary transistors and by means of a robust di_C/dt and dv_{CE}/dt control of the switching transients, as explained previously. Nevertheless, a failure of e.g. a GD, an IGBT, or the load could at any time lead to a SC of the output terminal to either the (+) or the (-) DC-link rail with a specific SC impedance Z_{SC} . Similar as for a conventional (passive) GD, the closed-loop GD thus also needs to provide a fast SC detection and a safe turn-off for the different types of SCs, in order to attain a robust and reliable overall system operation.

Remark: The discussion on the SCs and the according extensions of the GD are directly applicable also for the closed-loop GD presented in Chapter 5 for chopper circuits.

6.3.1 Basic Types of Short Circuit

In terms of gate driving there exist two basic types of IGBT SCs [79], whereby SC type I corresponds to a turn-on of a turned-off IGBT into an existing SC impedance Z_{SC} at the output terminal of the bridge leg. The characteristic current paths for this type of SC are depicted in Figure 6.10.

At the SC type II the IGBT is already in the on-state and is carrying the load current i_L when the SC occurs at the output terminal. The corresponding turn-off sequence and the current paths are shown in Figure 6.11.

For a third category, SC type III described in [78, 79], the direction of the load current is negative, i.e. the anti-parallel diode of T_{UT} would conduct the load current before the SC occurs. Considering the required modifications of the GD SC type III is equivalent to SC type II.

Independent of the type of the SC, its impedance Z_{SC} can basically feature an arbitrary value, which mainly depends on the location and source for the SC.

6.3.2 Short Circuit Type I Detection and Turn-off

At SC type I with a low SC impedance Z_{SC} and assuming a small inductance of the commutation loop L_s the IGBT's collector-emitter voltage remains close to the DC-link voltage during the interval of current rise.

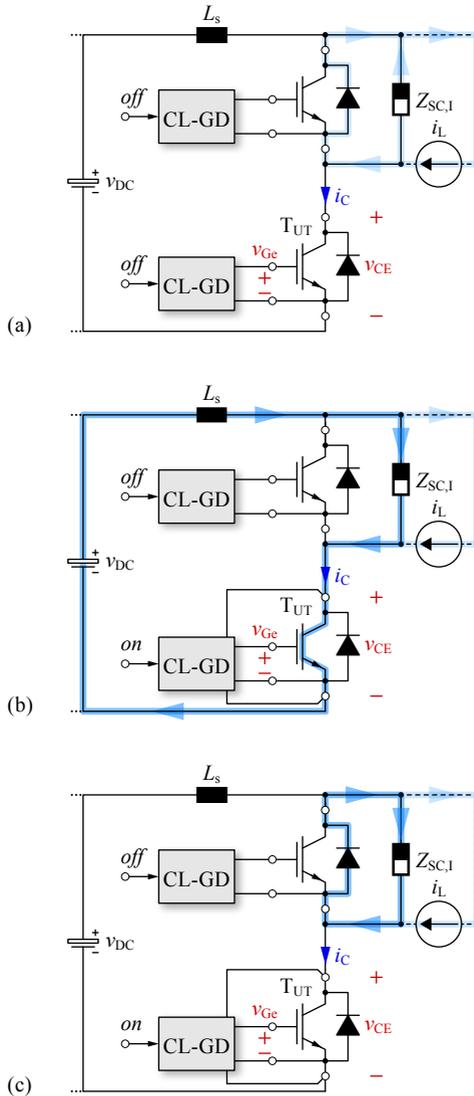


Figure 6.10: Switching state sequence and current paths for SC type I, i.e. a Hard Switching Failure (HSF). (a) The SC impedance Z_{SC} is already present prior to the turn-on of T_{UT} . (b) T_{UT} is turned-on and, hence, closes the SC current path. (c) The GD of T_{UT} detects the SC and turns T_{UT} off. The SC current remains free-wheeling in the complementary diode.

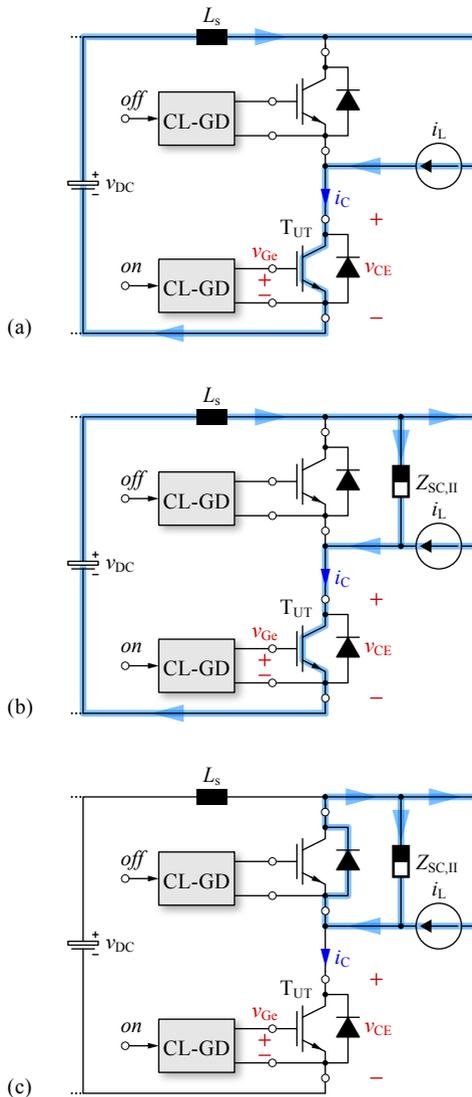


Figure 6.11: Switching state sequence and current paths for SC type II, i.e. a Failure Under Load (FUL). (a) T_{UT} is carrying the load current i_L . (b) The SC occurs at the output terminal causing a SC current in addition to i_L . (c) The GD of T_{UT} detects the SC and turns-off T_{UT} off. The SC and the load current are free-wheeling in the complementary diode.

For the proposed GD this corresponds to the case of a conventional hard turn-on at nominal operation, i.e. the rate of rise of the collector current, di_C/dt , is actively controlled to its reference value by the closed-loop control. As soon as the SC overcurrent level is detected, the IGBT can be turned-off by changing the control reference signal $v_{\text{ref},d/dt}$ from the positive to a negative value. Accordingly, i_C is reduced at a constant rate by means of closed-loop control. In case of a high SC impedance Z_{SC} , the detection and turn-off is similar to the SC type II, cf. Section 6.3.3.

Detection Circuits

In order to ensure a fast detection of SCs of type I various direct or indirect methods of i_C measurement have already been suggested [76,94] or are proposed in this thesis, cf. Figure 6.12, and are summarized in the following. Due to the short transients at turn-on an AC current measurement is sufficient here in case a full demagnetization of the current sensor can be ensured.

Shunt Resistor Using a shunt resistor to measure i_C is a simple and high-bandwidth solution, cf. Figure 6.12 (a). For large currents (e.g. $\gg 10$ A) the main drawback of the shunt is the linear increase of losses in dependency of the nominal current, assuming a constant level of the sensor output voltage at nominal current.

Sense IGBT A sense IGBT splits the collector current with a defined ratio whereby the small (sense) current i_{se} is measured with a shunt, cf. Figure 6.12 (b). This type of IGBT, however, is today very rare and expensive.

Gate Voltage or Gate Charge An indirect measurement of i_C can be performed by means of analyzing the gate voltage or the gate charge, as for a SC of type I no Miller plateau exists [95, 96] and the gate charge is reduced [97].

Rogowski Coil The Rogowski coil consists of a coil without magnetic core which encloses the conductor carrying the current to be measured. According to the law of induction, the voltage across the coil terminals is proportional to the time derivative of the current,

$$v_{\text{rog}} = M \cdot \frac{di_C}{dt}, \quad (6.4)$$

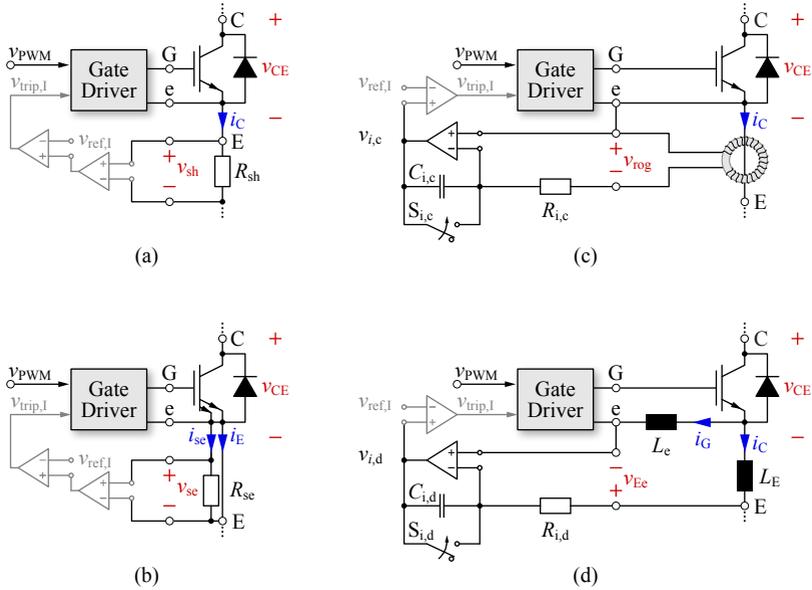


Figure 6.12: Overview of i_C measurement concepts and according detection/prevention of SC type I. (a) Shunt resistor; (b) sense IGBT and shunt resistor; (c) Rogowski coil and integrator; (d) parasitic voltage drop across emitter inductance and integrator.

where M describes the mutual inductance of the Rogowski coil and the conductor [98]. By means of a passive or active integrator, which should be resettable in order to limit the influence of parasitic offset voltages, the collector current during the switching transients can finally be derived,

$$v_{i,c} = i_C \cdot \frac{M}{R_{i,c} \cdot C_{i,c}}, \quad (6.5)$$

as shown in Figure 6.12 (c). The main challenge of the Rogowski coil is the insertion of a wound or PCB-integrated coil into the commutation loop without adding stray inductance or violating the creepage distances [99].

Bond Wire Inductance The voltage occurring between the power emitter and the auxiliary emitter terminals, i.e. across the para-

sitic inductances L_E and L_e , is mainly proportional to the derivative of the collector current,

$$v_{Ee} = -L_E \cdot \frac{di_C}{dt} + L_e \cdot \frac{di_G}{dt} \approx -L_E \cdot \frac{di_C}{dt}, \quad (6.6)$$

if the comparably small gate current is neglected. This voltage is already utilized as di_C/dt feedback signal for the closed-loop control. Accordingly, using a passive integrator [32] or a resettable active integrator the collector current during the switching transients can be derived similarly to the Rogowski coil, cf. Figure 6.12 (d),

$$v_{i,d} \approx i_C \cdot \frac{L_E}{R_{i,d} \cdot C_{i,d}}. \quad (6.7)$$

The main advantage of this concept is that the stray inductance is unchanged and no additional lossy or expensive sensing element is needed. Utilizing the already existing v_{Ee} measurement on the GD, this approach of SC type I detection was implemented with a resettable active integrator in the GD at hand, cf. Figure 6.12 (d).

6.3.3 Short Circuit Type II Detection and Turn-off

At SC type II, contrary to SC type I, the IGBT is already in the on-state and carrying the load current at the moment when the SC occurs. Accordingly, the IGBT is fully saturated and v_{CE} remains at a comparably low value. The SC current rises until the IGBT starts to desaturate and the collector-emitter voltage starts to increase which in turn causes a current in the Miller capacitance. As shown in Figure 6.6, this leads to a charging of the gate which again results in an increase of the SC current via the IGBT's transconductance. Accordingly, a gate clamping circuit, i.e. a diode connected from the gate to the positive gate drive supply voltage or a bidirectional Z-diode connected between gate and kelvin emitter is mandatory to limit the SC current [100].

Detection Circuits

The increase of v_{CE} at the occurrence of the SC type II is typically utilized to detect this kind of SC, whereby the on-state voltage $v_{CE,sat}$ can only be monitored once the dynamic processes of the IGBT's turn-on transient are completed, i.e. typically several microseconds after the

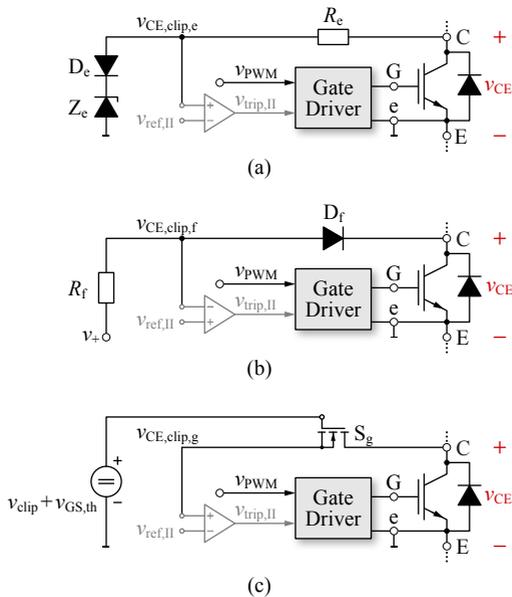


Figure 6.13: Overview of v_{CE} clipping circuits to measure v_{CE} in on-state with high accuracy and to detect a SC of type II. (a) High-ohmic forward-bias resistor and limiting Z-diode [101]; (b) high-voltage diode and forward-bias resistor [101]; (c) self-triggered auxiliary high-voltage transistor in parallel to the IGBT [102].

turn-on command. A fast and precise detection of v_{CE} which shows values of a few volts in the on-state cannot be performed by a simple resistive divider directly connected between collector and emitter due to the very low signal amplitude and the sensitivity to noise resulting for the required large dividing ratio. This is why different clipping circuits have been proposed in the literature, cf. Figure 6.13, which are summarized in the following.

Resistor + Z-diode Clipping by a Z-diode Z_e , diode D_e , and a high-ohmic resistor R_e was proposed in [101], cf. Figure 6.13 (a). The advantage of this circuit is that no high-voltage semiconductor is needed, however, the disadvantage is the low bandwidth due to the relatively slow charging / discharging of the parasitic capacitance of Z_e via R_e . D_e is needed to ensure an unipolar voltage clipping.

Diode A high-voltage diode D_f can be used to clip collector-emitter voltages above the positive gate drive supply voltage v_+ as proposed in [101] and shown in a simplified way in Figure 6.13 (b). Compared to the solution with the Z-diode this circuit is very fast since the resistance of the series resistor R_f is comparably low. The voltage drop caused by the diode can be compensated by an additional diode and a resistor [101]. As this circuit is fast and simple, and does not need a transistor, this SC type II detection method was implemented for the closed-loop GD at hand.

Transistor An auxiliary transistor S_g connected in parallel to the IGBT, which is only turned-on during the on-state of the IGBT, can be used to measure v_{CE} with high precision. An elegant solution with a self-triggered control signal was analyzed in [102] and is shown in Figure 6.13 (c). The drawback of this solution is the need for an active semiconductor with the same blocking capability as the IGBT.

Turn-off

Even though SC type II (or a SC of type I with large SC impedance) can be detected with a comparably low hardware effort, the turn-off by means of the proposed closed-loop GD is not straight forward as will be explained subsequently.

At SC type II, i_C and v_{CE} are rising / falling simultaneously, however, the basic principle of the proposed closed-loop GD was derived on the basis of subsequent changes of the collector current and the collector-emitter voltage as explained in Section 5.1. Accordingly, a closed-loop turn-off at SC type II is not possible. However, a SC II may be turned-off similar to a conventional GD. There, a short circuit is turned-off using a relatively high-ohmic turn-off gate resistor, i.e. a small negative gate current, in order to ensure a slow decay of the collector current and, hence, avoid an overvoltage exceeding the SOA [103]. By means of disabling the di_C/dt and dv_{CE}/dt feedbacks in on-state, i.e. via the inhibition switches introduced in Figure 6.7, a SC type II can safely be turned-off through the gate current controller of the proposed GD. In doing so and relating to Figure 6.7, the gate current control is activated via v_{ctrl, i_G} and a small negative value is set as reference signal v_{ref, i_G} for the gate current at SC type II turn-off.

6.4 Final Closed-Loop Gate Driver

The complete block diagram of the proposed closed-loop GD of Figure 6.7, extended for a safe and robust handling of SCs of type I and II and including an interlocking of the complementary transistors, is depicted in Figure 6.14.

6.4.1 Closed-Loop Control of Switching Behavior

The subordinate (inner) high-bandwidth analog control ensures a defined and optimized switching behavior of the IGBT by means of closed-loop di_C/dt , dv_{CE}/dt , and i_G control according to the detailed block diagram shown in Figure 6.7 and the explanations in Chapter 5.

6.4.2 Central Control and Protection

In a superordinate (outer) digital controller, i.e. a Finite State Machine (FSM) implemented in a CPLD / FPGA, the control and reference signals for the closed-loop controller are generated on the basis of the input command of the main PWM controller and the edge detectors indicating a current or voltage rise. In addition, also the reciprocal interlocking of the two complementary transistors in a bridge leg, which minimizes the distortion of the output voltage and prevents a shoot-through, is implemented, here.

Employing the feedback signals v_{CE} and v_{Ee} , which are also used for the closed-loop control, the collector current during the switching transients is derived by active integration of v_{Ee} , cf. Figure 6.12 (d), and the on-state collector-emitter voltage is measured by means of the v_{CE} clipping circuit presented in Figure 6.13 (b). These measured state variables of the IGBT are then used to detect the different types of short circuit by means of comparators and to initiate the SC turn-off.

6.4.3 Online Measurement and Health Monitoring

Optionally, the measurement signals of i_C after the switching transients and v_{CE} in on-state can be sampled by individual ADCs. On that basis, an online monitoring and analysis of the health state of the IGBT, i.e. an estimation of the junction temperature or of a lift-off of bond wires, can be performed in the digital controller by comparison to a

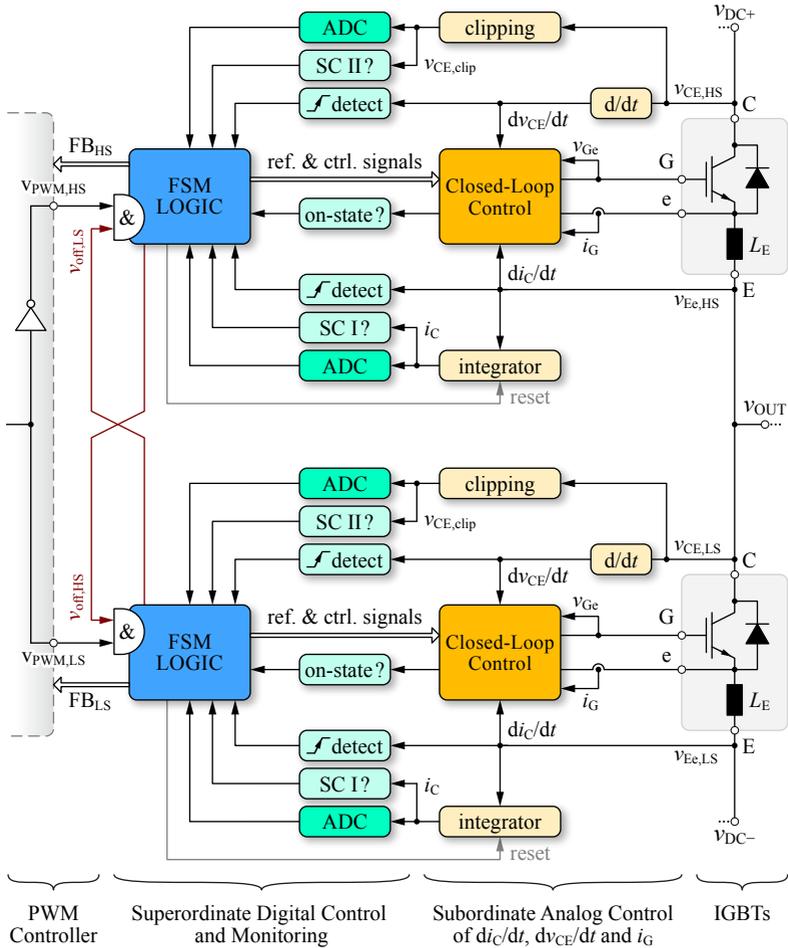


Figure 6.14: Implementation-oriented block diagram of the proposed closed-loop bridge leg IGBT GD.

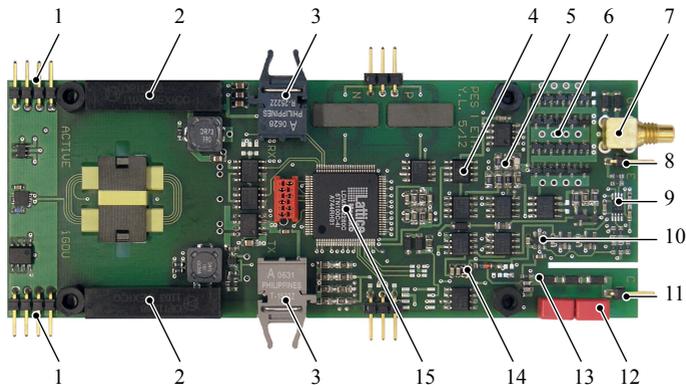


Figure 6.15: Prototype of the proposed closed-loop di_C/dt , dv_{CE}/dt , and i_G bridge leg IGBT GD; dimensions of the PCB: 50 mm x 133.3 mm and / or 1.97 in x 5.25 in. 1: Power supply, PWM-in, and fault-out terminals; 2: optocouplers for PWM-in and fault-out signals; 3: optical links for IGBT interlocking; 4: i_G control section; 5: di_C/dt and dv_{CE}/dt control section; 6: output stage; 7: gate drive output; 8: power emitter connection terminal and di_C/dt feedback; 9: i_C measurement; 10: SC I detector; 11: collector connection terminal; 12: dv_{CE}/dt feedback; 13: v_{CE} clipping circuit; 14: SC II detector; 15: CPLD.

reference output characteristics [104]. In this case, the simple 'ok' / 'not-ok' status feedback to the main PWM controller can be extended by an online status report of the IGBT, which allows an early detection of over temperature or failures of the system and enables to perform a system maintenance prior to a failure.

6.5 Experimental Verification

A hardware prototype of the proposed closed-loop di_C/dt , dv_{CE}/dt , and i_G GD was developed, cf. Figure 6.15, that basically implements all the measurement and control circuits described in Chapter 5 and Chapter 6 of this thesis. The finite state machine (FSM) is implemented in a CPLD (type LCMXO2280C-5TN100C from Lattice) running at a clock frequency of 100 MHz in order to generate the desired trigger and reference signals for the closed-loop control and to handle e.g. the deactivation of the feedback signals or the detection of the dif-

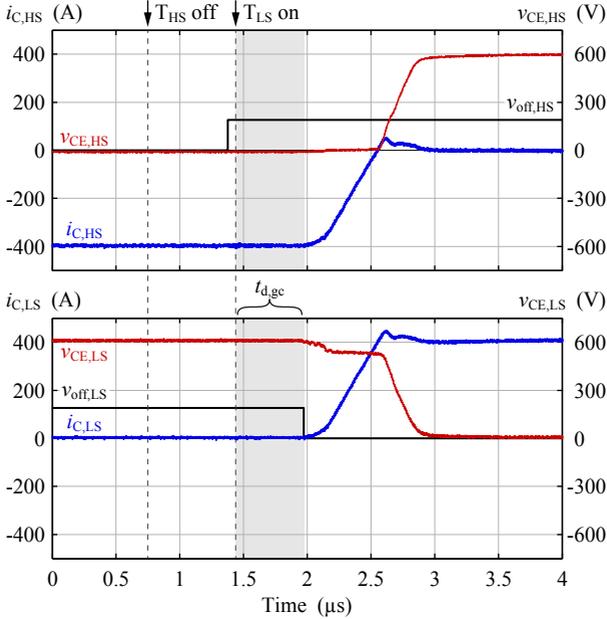


Figure 6.16: Measurements at closed-loop control of the switching transition type (A), i.e. a soft (zero current and zero voltage) turn-off of T_{HS} is followed by a hard turn-on of T_{LS} .

ferent types of SCs. A 1.2 kV, 300 A bridge leg IGBT module (Infineon FF300R12MS4) in an EconoDUAL housing was selected as semiconductor arrangement to be switched. The test setup was completed by an air-core pulse inductor (53 μH) as inductive load and a low-inductance busbar interconnecting all the components.

6.5.1 Normal Operation

In order to experimentally verify the safe switching in normal operation, double pulse tests were performed employing two GD prototypes for driving both IGBTs in the bridge leg of the test setup. Due to the mentioned symmetry considerations of the low-side and high-side switches, each of the two different switching transition types (A) and (B), cf. Section 6.1, are only shown once in the following. The measured current and voltage waveforms are depicted in Figure 6.16 for switching

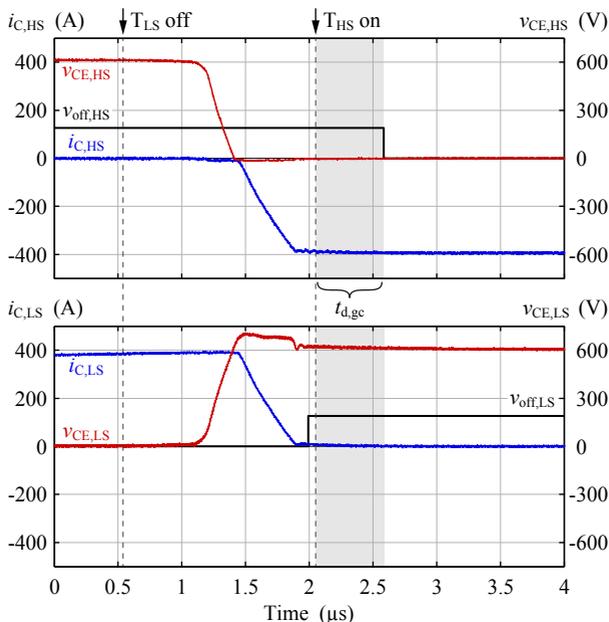


Figure 6.17: Measurements at closed-loop control of the switching transition type (B), i.e. a hard turn-off of T_{LS} is followed by a soft (zero current and zero voltage) turn-on of T_{HS} .

transition type (A) and in Figure 6.17 for type (B). The absolute value of the di_C/dt reference was set to $1 \text{ kA}/\mu\text{s}$ and the absolute value of the dv_{CE}/dt reference was set to $2 \text{ kV}/\mu\text{s}$. As can be seen, the waveforms are exactly as expected according to Section 6.1. A robust operation of the closed-loop di_C/dt and dv_{CE}/dt IGBT GD is enabled by disabling the feedback signals in the off-state and by the interlocking circuit.

6.5.2 Short Circuit

The two basic types of SCs of the load were experimentally verified according to the proposal in Section 6.3. Figure 6.18 depicts the current and voltage waveforms for the SC type I. Thereby, the IGBT T_{UT} to be tested was turned-on while the complementary IGBT of the bridge leg was already in the on-state. The di_C/dt reference signal was set to $1 \text{ kA}/\mu\text{s}$. Once the SC is detected by the SC type I detector, cf.

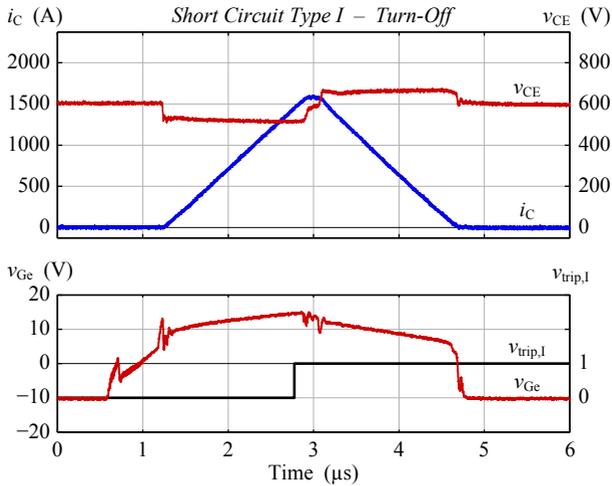


Figure 6.18: Measured current and voltage waveforms and SC detection trip signal $v_{trip,I}$ at occurrence and during turning-off a SC of type I.

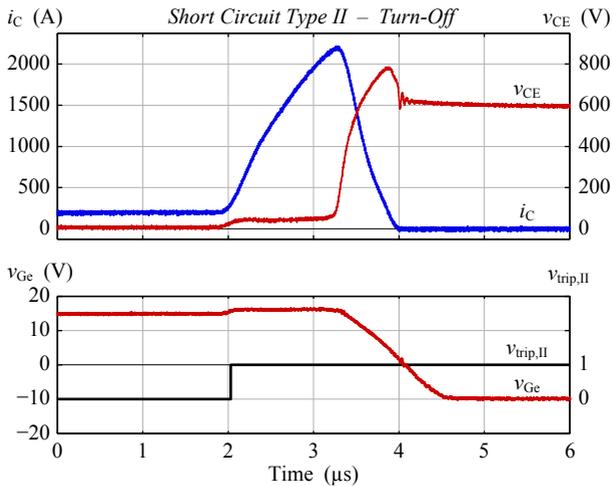


Figure 6.19: Measured current and voltage waveforms and SC detection trip signal $v_{trip,II}$ at occurrence and during turning-off a SC of type II.

Figure 6.12 (d), a safe turn-off with a di_C/dt reference of $-1\text{ kA}/\mu\text{s}$ is initiated. The waveforms for the SC type II are shown in Figure 6.19. T_{UT} is conducting a load current i_L of ca. 200 A, when a SC is initiated by a fast turn-on of the complementary IGBT. The desaturation detection circuit, cf. Figure 6.13 (b), detects the SC which subsequently is turned-off safely by disabling the di_C/dt and dv_{CE}/dt feedback signals and by using the gate current controller at a reference current of -3 A . Based on the measurement results, it can be summarized that the proposed closed-loop GD is able to detect and securely turn-off the two basic types of SCs of the load.

6.6 Summary

In this chapter, the closed-loop di_C/dt and dv_{CE}/dt gate drive concept proposed in Chapter 5 for chopper configurations was extended to IGBTs in bridge leg configuration. A safe and robust switching at normal operation and for short circuit conditions is ensured, and by reciprocal interlocking of the complementary IGBTs, the interlock dead-time and accordingly the output voltage distortion is minimized.

This extension enables an application of the proposed gate drive concept in numerous industrial systems such as variable speed drives, renewable energy systems or UPS applications. Therewith, a degree of freedom in the converter design is gained, which allows to ensure a defined trade-off between switching losses and EMI independent of the load current level, the DC-link voltage or the junction temperature of the power semiconductors. Furthermore, the closed-loop gate control allows to combine IGBTs from different manufacturers for the realization of a converter system without requirement of tuning gate resistors as typically required for conventional gate drive circuits. Accordingly, manufacturing and /or maintenance costs are reduced and a widespread application of power electronic converters in industry and renewable energy systems is supported.

7

Current Balancing of Parallel Connected IGBTs

In today's power electronic converters operating at currents up to few kA and voltages up to several kV, i.e. with power ratings in the range of few Kilowatts up to several Megawatts, IGBT modules are typically employed [6], cf. Figure 1.1.

The increasing power demand of modern inverters and rectifiers results in higher currents and voltages; currents up to tens of kA and voltages up to tens of kV are required, which exceed the ratings of single IGBT semiconductors currently available, cf. Figure 1.2. Accordingly, multiple IGBT modules must be connected in parallel or in series for providing the requested current or voltage ratings.

Depending on the geometrical arrangement and the parasitic inductances of interconnections of the series or parallel connected IGBTs, an unbalanced current or voltage distribution may occur. Furthermore, an unsymmetric loading could be caused by parameter variations of the semiconductors, as well as tolerances and different delay times of the GDs. Therefore, the IGBT modules are generally derated, which results in an increased number of devices and volume, and also in higher cost. Accordingly, active current balancing concepts are highly advantageous.

In this chapter, first, the most promising state-of-the-art current balancing concept, i.e. the centralized delay time compensator [94, 105–107], is reviewed. Thereafter, a novel decentralized delay time control approach is proposed, which overcomes the main disadvantages of the centralized concept. Different control topologies and ways how to detect a current imbalance in the simplest way are illustrated. Subsequently, an experimental verification of the proposed concept by double pulse

tests of 4 parallel connected IGBTs is performed. A review of the static and thermal current balancing concludes this chapter.

7.1 State-of-the-Art Current Balancing

7.1.1 Introduction

For IGBT modules connected in parallel, several factors may cause a dynamic and static unbalanced current distribution and could result in overcurrents or even unwanted system failures. Substantially, these factors can be related to the electrical and thermal interconnection of the IGBTs with the busbar and the heat sink, to parameter variations of the semiconductors, and to tolerances and different delay times in the gate driving circuits. In Figure 7.2, a schematic overview of these main influencing factors is shown.

A symmetric electrical layout of the parallel connected IGBTs and the DC-link, i.e. identical inductances in the commutation loop, is a key prerequisite to attain balanced currents in the dynamic case [108]. To attain a static current balancing and thermal stability, IGBTs with a positive temperature coefficient, i.e. a crossover-point in the output characteristics well below the nominal current, should be used and mounted on a common heat sink [109, 110].

Even if these requirements are met, the typical current distribution for parallel connected IGBTs without dedicated means for current balancing may exhibit a significant imbalance, cf. Figure 7.1. This current imbalance is mainly caused by the inevitable and different delay times

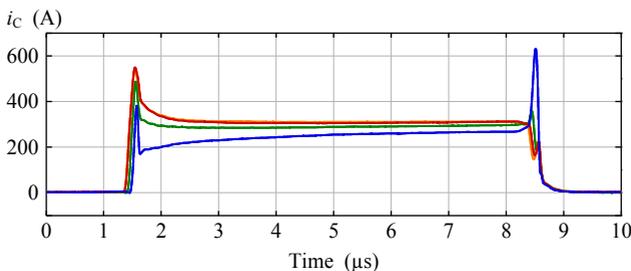


Figure 7.1: Typical current distribution for parallel connected IGBTs without dedicated means for balancing the currents.

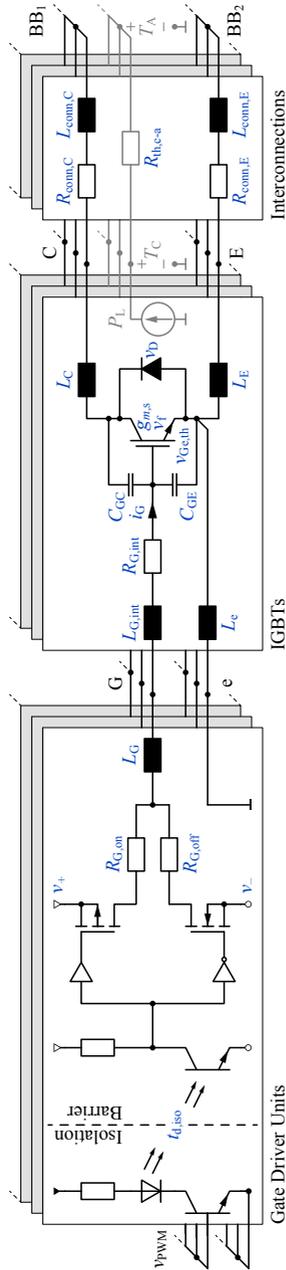


Figure 7.2: Overview of the main causes of an unbalanced current distribution of parallel connected IGBT modules, subdivided into the GDs, the IGBTs, and the electrical and thermal interconnections.

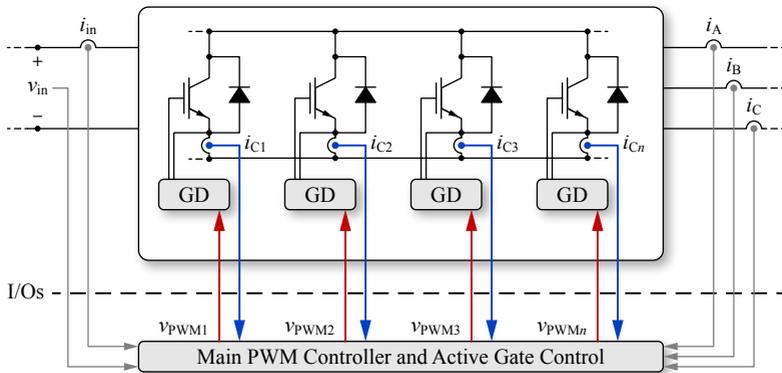


Figure 7.3: Parallel connected IGBT modules used as single switch of a power electronic converter, where the individual gate signals v_{PWMi} are controlled by a centralized active gate control unit. The control is based on measurements related to the currents in the individual devices and ensures a balanced current distribution.

of the signal isolators of the individual GDs and the tolerances of the IGBTs ($R_{G,int/ext}$ and $v_{Ge,th}$) which basically also introduce a delay time [111]. By preselecting and matching the IGBT modules, by using GDs with extremely tight tolerances of the delay skews, and by tuning the gate resistors, a balanced current distribution can be attained [112].

7.1.2 Centralized Delay Time Compensation

In order to avoid the costly and elaborate preselection and tuning process, previous works show that the dynamic current balancing of parallel connected IGBTs is beneficially attained by a delay time compensation, i.e. an active control of the individual PWM control signals [94, 105–107]. Thereby, the inevitable delay skews of the GDs and the tolerances of the IGBTs and the gate driving paths are compensated. A schematic overview of such centralized active gate control is illustrated in Figure 7.3.

Operating Principle

In a central digital control platform the information on the actual switching times of the IGBTs are derived, e.g. by means of measuring

the currents [94, 105, 106] or the corresponding time derivatives [107]. On the basis of the measured switching times, the centralized control unit (FPGA / CPLD) iteratively adjusts the turn-on and turn-off times of the individual PWM signals for each IGBT to ensure a simultaneous switching and, hence, a dynamically-balanced current sharing.

Disadvantages

The main disadvantage of this solution is the extensive bidirectional interface between the main PWM controller and the IGBTs / GDs, which leads to a bulky wiring in the converter cabinet and asks for large I/O-capacity of the PWM controller. For each IGBT an individual current sensing circuitry, which must provide an isolation level as high as the voltage of the DC-link, and a dedicated PWM control signal are needed. In addition, changing the number of IGBT modules is elaborate since the software and the hardware need to be modified.

In the following, a novel delay time compensation is proposed, where the control of the switching times is performed decentralized, i.e. implemented directly on the GD units.

7.2 Decentralized Active Gate Control

7.2.1 Introduction

The basic idea to overcome the extensive bidirectional interface of a central delay time compensator is to distribute the control of the switching times directly to the (intelligent) GDs, which then need to be equipped with a small digital controller (FPGA / CPLD).

A schematic overview of this approach, where GDs are comprising the so called Decentralized Active Gate Control (DAGC), is illustrated in Figure 7.4. Thereby, all GDs share a common PWM control signal. Each GD adapts its delay times based on measurements related to the own collector current and a reference signal from a neighboring GD, which contains the information on the switching time, in order to ensure a balanced current distribution. Accordingly, the needed current sensing circuitry must not provide any isolation and no feedback to the main PWM controller is needed. The interface between neighboring GDs, i.e. the transmission of the reference signal, must only provide a low isolation voltage due to the parallel connection of the IGBTs.

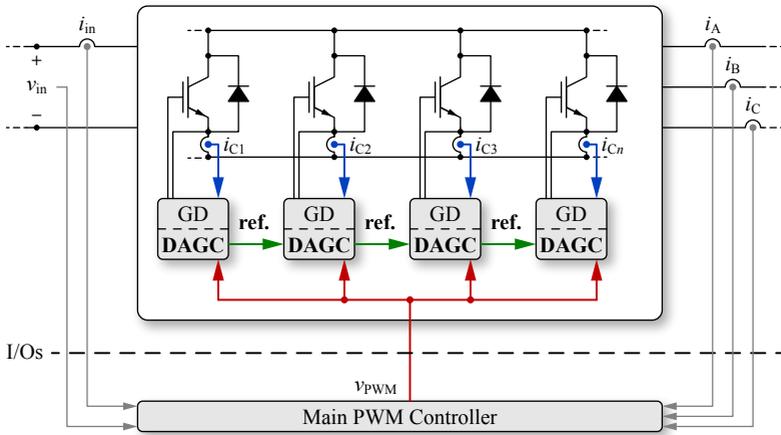


Figure 7.4: Parallel connected IGBT modules used as single switch of a power electronic converter, sharing a common gate signal v_{PWM} . Each GD contains DAGC and adapts its switching times, based on a measurement related to the collector current and a reference signal from a neighboring GD, in order to ensure a balanced current distribution.

Prior to the investigation how this reference signal can be defined and how it can be transmitted between neighboring GDs, possible decentralized control topologies are investigated subsequently.

7.2.2 Control Topologies

In contrast to a centralized approach, where the information on all switching times can be used to calculate the optimal individual switching delays, a different control topology must be used, here.

Master-Slave

A first possibility of the control topology is to transmit the reference signal, which contains the informations needed to adapt the switching times, of the first (master) IGBT to all neighboring (slave) IGBTs, cf. Figure 7.5 (a). This concept is known as master-slave topology. Thereby, the master GD delays its gate signal to a preset value and the slave GDs adapt their delay times to attain switching times identical to

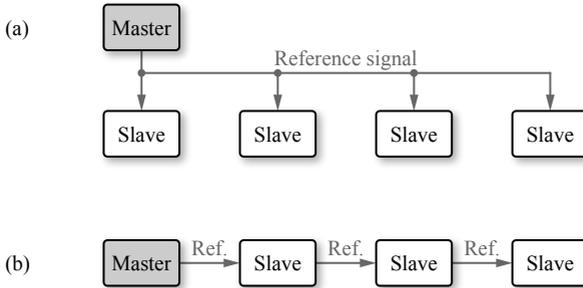


Figure 7.5: Possible control topologies for the implementation of the DAGC. (a) Master-Slave; (b) Daisy Chain.

the master IGBT. If this control is maintained, a simultaneous switching of the IGBTs can be ensured.

Daisy Chain

Another possibility is to only distribute the reference signals between neighboring GDs, cf. Figure 7.5 (b). This concept is denominated as daisy chain topology. Here, the master IGBT again switches with a constat delay and its neighbor, i.e. the first slave, adapts its switching times to the master. This slave IGBT is again the master for the second slave IGBT and so on, i.e. after few iteration cycles, a simultaneous switching of the IGBTs can be ensured as well.

Control Dynamics

A simulation of the development of the switching times was performed in order to compare the dynamic and static control performance of the two different control topologies. The simulation model considers distributed delay time compensators with independent clocks which, accordingly, leads to individual sampling-jitter of the PWM control signal and of the detection of the switching times. In case a delayed switching is detected, i.e. the switching times are not detected within the same sampling interval, the delay time is adapted in increments of the sampling rate. The attained results are illustrated in Figure 7.6.

As expected, the master-slave control topology leads to faster control dynamics, i.e. a lower number of cycles i is needed to reach the

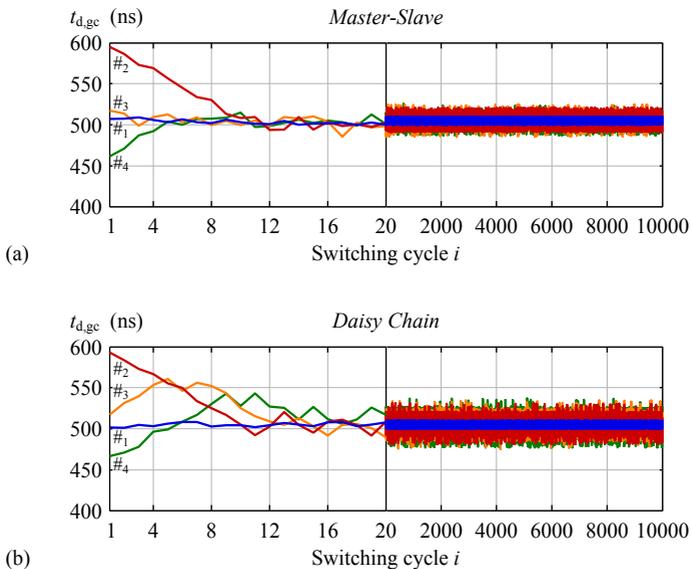


Figure 7.6: Simulation of the control response for (a) the master-slave and (b) the daisy chain control topology for a sampling rate of $T_{\text{dagc}} = 1/f_{\text{clk}} = 10$ ns.

appropriate switching delays, and to a smaller absolute deviation between the switching times of all IGBTs. However, by increasing the sampling frequency, a similar static deviation can be attained with the decentralized approach.

7.2.3 Measures for the Current Imbalance

In order to adapt the switching delays, a measure to quantitatively determine the current imbalance is needed. A first possibility is to detect the switching times t_i of the IGBTs by current level comparators [94] or by detecting an increase/decrease of the current [107], cf. Figure 7.7 (a). Another possibility is to evaluate the amplitudes after the turn-on switching transients [105], where a smaller amplitude corresponds to a later switching time, cf. Figure 7.7 (b).

Especially with a decentralized delay time compensator, significant advantages of the amplitude information over the time information in

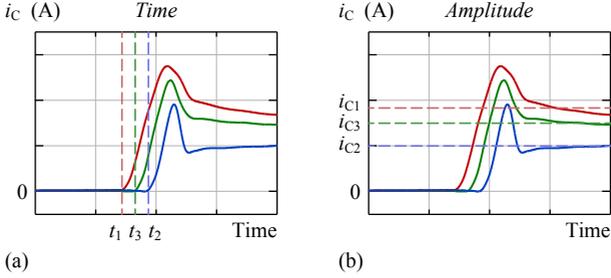


Figure 7.7: Possible measures in order to detect a current imbalance. (a) individual points in time (edges) t_i of increasing current or (b) individual current amplitudes i_{C_i} sampled after the switching transients.

terms of control accuracy, hardware implementation and flexibility exist. On the one hand, due to the limited clock frequency of the digital controller, the resolution in time is typically significantly lower compared to the resolution of the sampling of the current amplitude by an ADC, i.e. a current imbalance can be detected and controlled more precisely on the basis of amplitude information. On the other hand, the propagation of the switching time between the GDs is very time critical, since the GDs do not share a common clock, i.e. each GD needs to measure the switching time differences individually. Due to transient voltage drops across the parasitic emitter inductances of the IGBTs, the interface for the transmission of the reference signal must provide a galvanic isolation of typically up to 100 V. This is why pulse transformers typically need to be employed for distributing the switching instant, in order to maintain a short and defined transmission delay. In contrast, the current amplitude sampled after the turn-on transients is not time-critical and can be transmitted via an isolated digital bus between neighboring GDs, whereby either optical or magnetic transducers can be employed.

In addition, the transmission of a digital signal offers the possibility of either using the master-slave or the daisy chain control topology by only a small software modification, i.e. either the input reference signal is directly forwarded (master-slave) or the own measurement is transmitted (daisy chain).

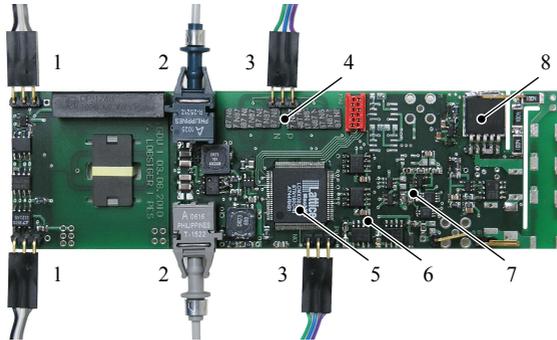


Figure 7.8: Developed GD containing the DAGC functionality. 1: power supply and gate signal connectors (in/out); 2: optical links for current amplitude transmission (in/out); 3: electrical links for current edge transmission (in/out); 4: signal isolation transformers for edge transmission; 5: CPLD; 6: current edge detection; 7: current measurement; 8: output stage.

7.2.4 Experimental Verification

Gate Driver Prototype

An isolated GD was developed, cf. Figure 7.8, which contains the DAGC functionality, i.e. a digital control unit (CPLD), a current measurement circuit based on the IGBT's emitter voltage difference, cf. Figure 6.12 (d), including an edge detection, and communication interfaces to transmit both switching times and sampled current amplitudes between neighboring GDs.

Hardware Setup

In order to verify the proposed decentralized delay time compensator, a test setup consisting of a DC-link capacitor C_{DC} (up to 1 kV, 1.6 mF), 5 parallel connected Infineon IGBT half-bridge modules (FF450R12KE4, 1.2 kV, 450 A) driven by the developed GDs, an air-core pulse inductor L_P (53 μ H) and a symmetric low inductance busbar interconnecting all components was implemented. Its schematic and corresponding hardware setup are depicted in Figure 7.9. With this setup, double or multiple pulse tests for up to 5 parallel connected IGBT modules can be performed to measure and analyze the current sharing during turn-on and turn-off switching transients. In order to measure the currents of all

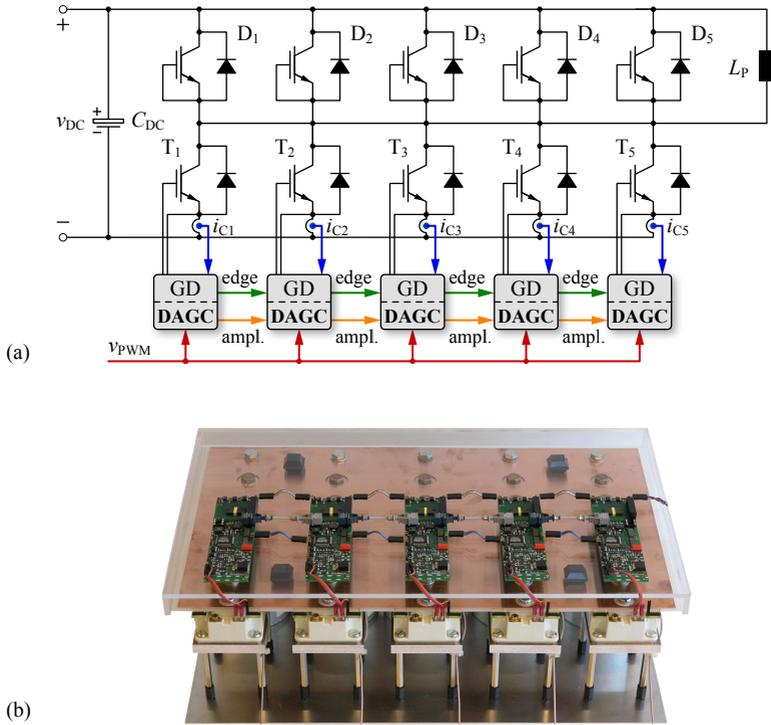


Figure 7.9: Test setup for the experimental verification of the DAGC at diode clamped inductive load switching. (a) Circuit diagram and (b) implemented hardware setup.

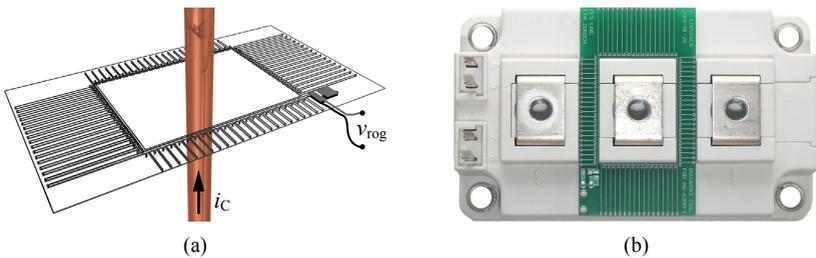


Figure 7.10: PCB-integrated Rogowski coil. (a) 3D-drawing of the coil; (b) assembly of IGBT module and Rogowski coil.

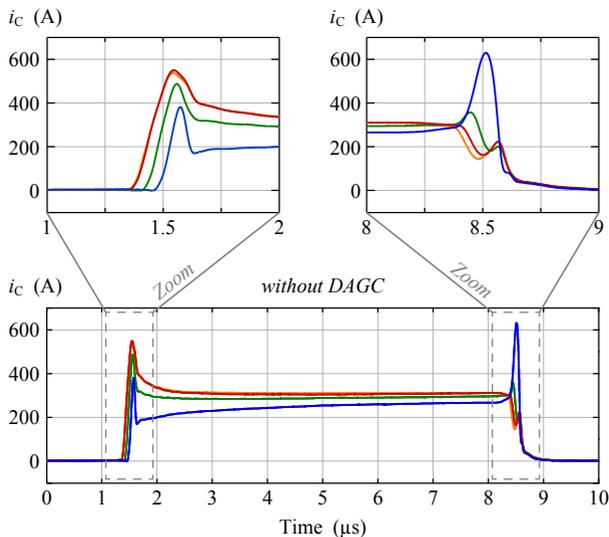


Figure 7.11: Measured IGBT currents without delay time compensation (with PWM delays of $t_{\text{delay}(1,2,3,4)} = 100 \text{ ns}, 0 \text{ ns}, 20 \text{ ns}, 50 \text{ ns}$).

IGBTs without changing the main power circuit, PCB integrated Rogowski coils, as illustrated in Figure 7.10 and described in Section 6.3.2, have been employed in the hardware setup.

Measurement Results

The current distribution of 4 parallel connected IGBT modules was measured for hard turn-on and turn-off switching transients in a double pulse test to demonstrate the performance of the decentralized delay time control. The gate signal delays of all 4 IGBTs have been adjusted to constantly $t_{\text{delay}(1,2,3,4)} = 100 \text{ ns}, 0 \text{ ns}, 20 \text{ ns}, 50 \text{ ns}$ representing the delay skews of optical signal isolators. A sequence of 20 pulses was performed after which the current sharing has been measured.

Without DAGC, the constant gate signal delays are not compensated, thus an unbalanced current distribution as shown in Figure 7.11 results. The IGBT, which turns off last, is exposed to an excessive current stress due to the impressed load current.

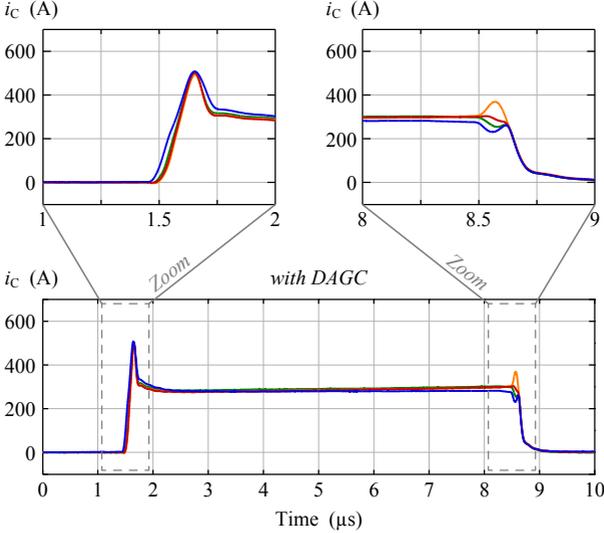


Figure 7.12: Measured IGBT currents with DAGC based on amplitude control (with PWM delays of $t_{\text{delay}(1,2,3,4)} = 100 \text{ ns}, 0 \text{ ns}, 20 \text{ ns}, 50 \text{ ns}$).

With DAGC ($f_{\text{clk}} = 100 \text{ MHz}$) based on the amplitude control, the delays of the gate signals are compensated by the digital control units. As a consequence, the current distribution is transiently and statically almost completely balanced for all 4 IGBT modules as depicted in Figure 7.12. In case a control based on the time information was used instead of the amplitude, a similar current distribution was achieved.

It has to be mentioned, that due to the individual clocks of the control units and the sampling jitter of the PWM gate signal inputs, the decentralized switching time control is a continuous process, where the delay times for all IGBTs may vary individually around the optimal average delays. This can result in temporary slightly less balanced currents than shown in Figure 7.12. In order to minimize this effect, the clock frequency f_{clk} of the CPLD could be increased.

In summary, it is not possible to maintain an absolutely perfect current balance. In the following, hence, the static and thermal balancing of the currents is reviewed.

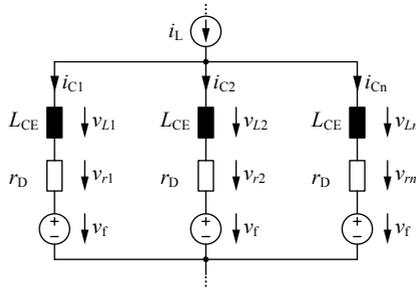


Figure 7.13: Equivalent circuit of n parallel connected IGBTs for investigating the static current balancing, i.e. valid after the turn-on switching transients with different initial currents $i_{Cj,0}$ also flowing in the corresponding parasitic inductances L_{CE} .

7.3 Static Current Balancing

In the static case, the currents of the parallel connected IGBTs will be evenly balanced under the assumption of identical on-state characteristics of the IGBTs including the temperature dependencies. In order to understand how the static case is attained after the turn-on switching transients, a simple equivalent circuit of the parallel connected IGBTs, cf. Figure 7.13, is employed. There, v_f corresponds to the forward voltage drop, r_D to the differential on-state resistance, and L_{CE} to the parasitic inductance of the IGBT modules. Due to the extremely low inductance busbar, any contribution of the busbar to the parasitic inductances is neglected.

After a non-optimal turn-on of n IGBTs, i.e. with unbalanced individual collector currents $i_{Cj,0}$ after the switching transients, the voltages across the individual inductances can be specified as

$$\sum_{j=1}^n v_{Lj}(t) = 0, \quad (7.1)$$

$$v_{Lj}(t) + v_{rj}(t) + v_f = v_{CE} \quad j \in [1, n] \quad (7.2)$$

if the load current i_L is assumed to remain constant. Accordingly, the voltage drops across the individual inductances, which basically define

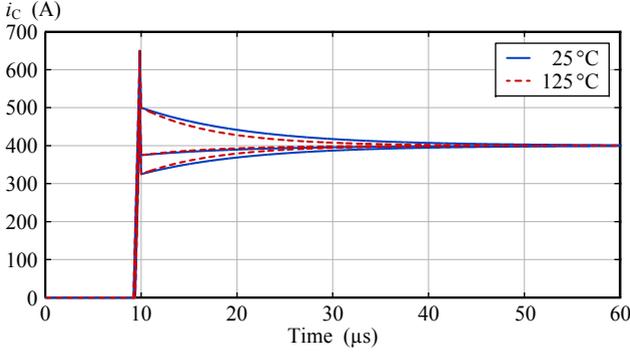


Figure 7.14: Current waveforms at static current balancing of 3 IGBTs according to (7.4) with IGBT parameters of the Infineon power module FF450R12KE4: $r_D(25^\circ\text{C}) = 1.75\text{ m}\Omega$, $r_D(125^\circ\text{C}) = 2.56\text{ m}\Omega$, $v_f(25^\circ\text{C}) = 0.95\text{ V}$, $v_f(125^\circ\text{C}) = 0.83\text{ V}$, $L_{CE} = 20\text{ nH}$. Accordingly, $\tau_b(25^\circ\text{C}) = 11.4\text{ }\mu\text{s}$ and $\tau_b(125^\circ\text{C}) = 7.8\text{ }\mu\text{s}$.

the changes of the individual currents, become

$$v_{Lj}(t) = \left(\frac{i_L}{n} - i_{Cj}(t) \right) \cdot r_D = L_{CE} \cdot \frac{di_{Cj}(t)}{dt} \quad j \in [1, n]. \quad (7.3)$$

As a result, the individual currents can be calculated as

$$i_{Cj}(t) = \frac{i_L}{n} + \left(i_{Cj,0} - \frac{i_L}{n} \right) \cdot e^{-t/\tau_b} \quad j \in [1, n], \quad (7.4)$$

$$\tau_b = \frac{L_{CE}}{r_D}, \quad (7.5)$$

i.e. the static case is approached via an exponential decay with the balancing time constant τ_b . The corresponding waveforms are illustrated in Figure 7.14 for the cases of low and high junction temperatures. The static case is reached quicker at higher junction temperature where an increased value of r_D reduces τ_b .

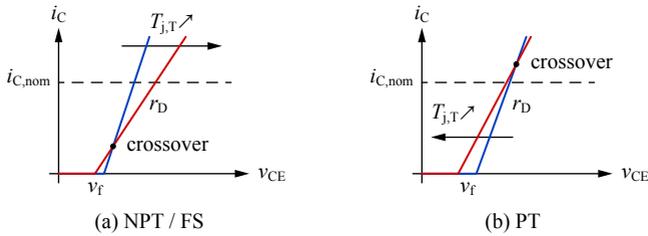


Figure 7.15: Typical output characteristics of (a) NPT / Field-Stop IGBTs (positive temperature coefficient) and (b) PT IGBTs (negative temperature coefficient) for low (blue) or high (red) values of the junction temperature [110].

7.4 Thermal Current Balancing

In case of identical junction temperatures of the parallel connected IGBTs, evenly balanced currents are attained in the static case. Over time, however, slight switching loss differences or uneven thermal resistances $R_{th,c-a}$ from case to ambient may lead to different junction temperatures of the semiconductors. In order to maintain a thermally stable current balancing, it is, hence, important that the IGBTs feature a positive temperature coefficient, i.e. a crossover point of the on-state voltage / current characteristics well below the nominal current value, cf. Figure 7.15. Thereby, the forward voltage drop increases with the junction temperature. As a result, the static on-state current of a hotter IGBT will stay below the average current and the conduction losses are reduced, leading to a decay of the temperature and a thermal stabilization.

The same prerequisite applies for the parallel connection of the diodes. Even though the crossover point of many diodes is close to or even above the nominal current, it is possible to fabricate diodes with positive temperature coefficient [113].

In an experiment, the IGBT / diode modules of the test setup, cf. Figure 7.9 (b), have been preheated to largely different temperatures in the range of 35 – 125 °C as illustrated in Figure 7.16. This was done in order to analyze the impact of excessive junction temperature differences on the static current balancing and also to test the proposed dynamic current balancing concept in this case.

The corresponding waveforms are illustrated in Figure 7.17. First of

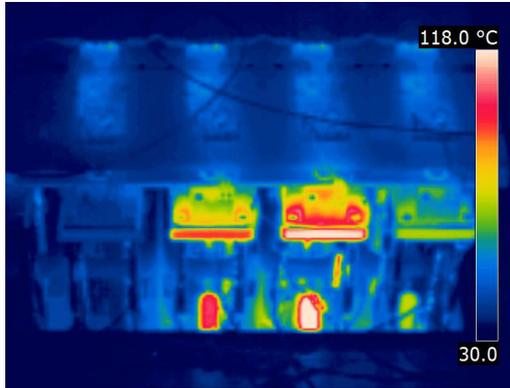


Figure 7.16: Temperature distribution of the preheated IGBTs' base plates.

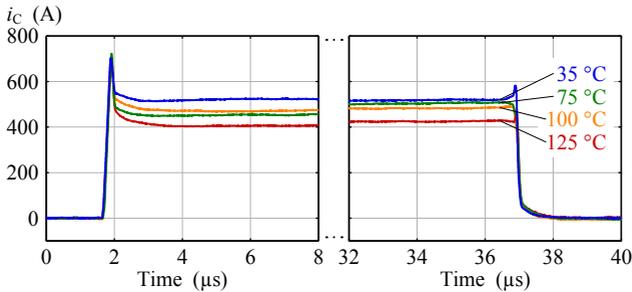


Figure 7.17: Current distribution for different junction temperatures defined by preheating of the IGBT / diode modules, cf. Figure 7.16.

all, even in this practically unrealistic case, a dynamic current balancing is attained by the proposed decentralized control concept. In addition, no surprisingly high current imbalance can be discovered, i.e. no significant current stress occurs, and the static balancing is consistent with the output characteristics of the IGBT. Accordingly, in a realistic case of similar thermal resistances to the heat sink, i.e. at a thermal imbalance of e.g. $10\text{ }^{\circ}\text{C}$, only a negligible static current imbalance will be observed.

7.5 Summary

In this chapter, the modular DAGC concept for balancing the currents of parallel connected IGBT modules is presented. The GDs adjust the switching times to achieve a dynamic current balancing by means of the implemented measurement and communication capability. Thanks to the modular concept, adding or removing IGBTs to and from the parallel connection is very simple since no changes in the GDs' hardware and software have to be performed. By means of employing IGBTs with a positive temperature coefficient, also a static and thermal balancing is maintained.

8

Conclusion and Outlook

8.1 Summary and Conclusion

In the presented work, a highly dynamic closed-loop IGBT GD providing independent control of di_C/dt and dv_{CE}/dt at clamped inductive load switching is proposed and investigated. The concept permits to adjust the current and voltage slopes according to reference values largely independent of nonlinearities or parameter variations of the IGBT. Therewith, a degree of freedom for the converter design is gained, which allows to ensure an operation in the SOA and a defined trade-off between switching losses and EMI independent of the load current level, the junction temperature or the DC-link voltage. A minimization of the switching delay times is achieved via the implemented gate current control loop.

By means of using only simple passive measurement circuits for the generation of the feedback signals and a single operational amplifier wired as PI-controller, a high analog control bandwidth of up to 34.3 MHz is achieved, which enables the application of the proposed closed-loop GD even for switching times in the sub-microsecond range.

For IGBTs arranged in bridge leg configurations, i.e. for rectifier or inverter operation, apart from the prevention of a shoot-through, the dead-time and, accordingly, the output voltage distortion are minimized by reciprocal interlocking of the complementary transistors. A continuous monitoring and the safe turn-off of short circuits of the load complete the GD.

Furthermore, the closed-loop gate control allows to combine IGBTs from different manufacturers for the realization of a converter system

without requirement of tuning gate resistors as typically required for conventional gate drive circuits. Accordingly, manufacturing and/or maintenance costs are reduced and a widespread application of power electronic converters in industry and renewable energy systems is supported.

In addition, a (local) control concept, which ensures a symmetric current balancing of IGBT modules connected in parallel by means of dynamically adapting the switching times on the GDs, is proposed and verified. Thereby, the conventional derating of the IGBTs' current-carrying capacity for parallel connection can be omitted and/or the maximum possible utilization of the semiconductors can be maintained.

The gate drive concepts presented in the course of this work have been implemented into GD prototypes and have been verified experimentally for 5 different IGBT modules in the 1.2kV class with current ratings of 300 – 450 A in different test setups by means of double pulse tests.

In contrast to related work presented in this area so far, even though a very simple and cost-efficient hardware implementation of the control is attained, the proposed gate drive concept maintains a full control of the IGBT over the complete switching process and provides a higher control bandwidth.

8.2 Outlook

8.2.1 Online Monitoring and Health State Analysis

Based on the implemented measurement circuits of the IGBT's terminal parameters i_C and v_{CE} , cf. Figure 6.14, an online monitoring and health state analysis of the IGBT could be performed [104]. In doing so, the collector current and the appropriate collector-emitter forward voltage drop could be sampled by individual ADCs after the switching transients and could subsequently be processed in the digital controller for specific evaluation purposes.

On the one hand, the output characteristic of an IGBT, i.e. the relation between the collector current and the collector-emitter voltage drop in on-state, depends on the junction temperature $T_{j,T}$ [114]. Accordingly, this relation could also be utilized as a measure to estimate $T_{j,T}$. On the other hand, the effects of ageing caused by the thermo-mechanical stress, i.e. a gradual bond-wire lift off, lead to an increase

of the differential on-state resistance [115], which could be detected by evaluating and comparing the IGBT's terminal characteristics to its initial and/or data sheet values.

As a result, the conventional 'OK' / 'Not-OK' feedback of the GD to the main PWM controller could be replaced by a comprehensive digital status feedback of the IGBT's parameters (i_C , v_{CE} , $T_{j,T}$, health indicator, etc.). This in turn would allow an early detection of an over temperature, aging or other failures, and enable to extend the lifetime and reliability of the converter by bringing forward maintenance of the system prior to a failure.

8.2.2 Integration of Gate Driver and IGBT

As has been detailed in this thesis, low parasitic inductances are a key prerequisite for attaining a fast and precise closed-loop control of the IGBT's switching trajectories. Unfortunately, conventional power modules exhibit rather large parasitic inductances in the power and especially in the gate driving paths.

A significant reduction of the parasitic inductances can e.g. be attained by means of embedding the semiconductor chips into a PCB [116]. This technology allows to interconnect the semiconductor chips and the DC-link as well as the GDs and the IGBTs with minimum possible inductances.

Accordingly, switching overvoltages of the IGBT / diode cells can be kept to a minimum and faster switching may become permissible. In addition, the control bandwidth of the proposed closed-loop gate drive concept could be further increased and an application at even shorter switching times and faster rates of di_C/dt and dv_{CE}/dt would become feasible.

8.3 Future Trends

Over the last decades, the performance of integrated circuits such as digital signal processors and analog-to-digital signal transducers has steadily improved [117, 118]. If this trend is maintained by the manufacturers in the long term, FPGAs as well as ADCs and DACs will become faster, cheaper and even more energy efficient over the next decades.

Following this performance evolution, the implementation of a real-time fully digital closed-loop GD [57], cf. Figure 4.9, will also become feasible for switching transients in the sub-microsecond range. The advantages of such a digital GD over the proposed composite digital/analog solution are twofold. On the one hand, the versatility of a digital controller allows to adapt the PI-controller relating to the particular control loop and, hence, to provide maximum overall control bandwidth and stability. On the other hand, if e.g. S-shaped instead of linear reference signals for the control of i_C and v_{CE} over time would be used, which could easily be calculated and generated in dependency of the operating point by fast digital signal processors, an additional -20 dB/dec. decay of the EMI noise spectrum would result at high frequencies [119, 120]. As a consequence, the trade-off between switching losses and EMI could be improved even more.

Currently, however, the costs of a fully digital control platform are up to 100 € [56], which is significantly higher than the cost-effective implementation with a single analog PI-controller. In addition, the high analog control bandwidth of up to 34.3 MHz of the closed-loop gate drive concept proposed in this thesis, cf. Section 5.2.4, cannot be reached by real-time digital implementations today.

Appendices

A

Switching Loss Calculation

ANALYTICAL expressions for the energy losses, which occur at diode-clamped inductive load switching in the IGBT, are derived in this chapter. The calculations are based on the typical waveforms of i_C and v_{CE} which are shown in Figure 2.4 for turn-on and in Figure 2.8 for turn-off, respectively.

In order to simplify the considerations, piecewise linear current and voltage slopes are assumed. To indicate the signs of the specific parts of the switching energies at first sight, the following equations are expressed as functions of the absolute values of di_C/dt and dv_{CE}/dt , since in any case at turn-on di_C/dt is positive and dv_{CE}/dt is negative and vice versa at turn-off.

A similar analysis was carried out in [9, 10], however, the loss components during the voltage slopes as well as the loss related to the tail current have been omitted and only a very simple assumption has been made for the loss caused by the reverse recovery effect.

A.1 Turn-on

The main parts of the switching losses during turn-on are generated in the intervals III – V of the switching operation, cf. Figure 2.4. Different loss shares, which are caused during the current slope, $E_{on,di/dt}$, during the voltage slope, $E_{on,dv/dt}$, and due to the reverse recovery effect, $E_{on,irr}$, are evaluated in the following and will finally be summed up for the calculation of the total energy loss at turn-on,

$$E_{on} = E_{on,di/dt} + E_{on,dv/dt} + E_{on,irr}. \quad (\text{A.1})$$

A.1.1 Current Slope Related Loss

The energy loss for the interval (t_1, t_{1A}) characterized by increasing collector current can be expressed as

$$E_{\text{on},di/dt} = \frac{i_L \cdot (v_{\text{DC}} - L_s \cdot |di_C/dt|)}{2} \cdot (t_{1A} - t_1). \quad (\text{A.2})$$

The corresponding time duration is given by

$$t_{1A} - t_1 = \frac{i_L}{|di_C/dt|}, \quad (\text{A.3})$$

and can be inserted in (A.2) whereby the energy loss can be calculated as a function of di_C/dt ,

$$E_{\text{on},di/dt} = \frac{i_L \cdot v_{\text{DC}}}{2} \cdot \frac{i_L}{|di_C/dt|} - \frac{1}{2} \cdot L_s \cdot i_L^2. \quad (\text{A.4})$$

The first term equals the switching energy loss for the case of $L_s = 0$ and the second term indicates the energy which is stored in the (parasitic) commutation loop inductance L_s in t_{1A} .

A.1.2 Voltage Slope Related Loss

If a constant current $i_C = i_L$ is assumed during the voltage slope interval (t_2, t_{2B}) , i.e. the reverse recovery current is neglected for a moment, the energy loss during the voltage slope becomes

$$E_{\text{on},dv/dt} = \frac{i_L \cdot v_{\text{DC}} \cdot (1 - \sigma_s)}{2} \cdot (t_{2B} - t_2). \quad (\text{A.5})$$

Thereby, σ_s is a positive definite factor [9] which describes the ratio between the voltage across the commutation loop inductance and the DC-link voltage for rising or falling collector current ($\sigma_s \leq 1$ at turn-on),

$$\sigma_s = \frac{L_s \cdot |di_C/dt|}{v_{\text{DC}}}. \quad (\text{A.6})$$

By substituting the voltage fall time

$$t_{2B} - t_2 = \frac{v_{\text{DC}} \cdot (1 - \sigma_s)}{|dv_{\text{CE}}/dt|} \quad (\text{A.7})$$

in (A.5), the energy loss during the voltage slope can be expressed as a function of dv_{CE}/dt ,

$$E_{\text{on},dv/dt} = \frac{i_L \cdot v_{\text{DC}}}{2} \cdot \frac{v_{\text{DC}}}{|dv_{CE}/dt|} \cdot (1 - \sigma_s)^2. \quad (\text{A.8})$$

A.1.3 Diode Reverse Recovery Related Loss

For the calculation of the energy loss caused by the reverse recovery effect of the complementary diode it is assumed that the interval of the reverse recovery current decay is very short in comparison to the voltage slope interval ($t_{2B} - t_2 \gg t_{2A} - t_2$), i.e. the collector-emitter voltage basically remains at the level of $v_{\text{DC}} \cdot (1 - \sigma_s)$ within the time interval where the reverse recovery effect occurs. Under this assumption, the loss caused by the reverse recovery charge Q_{rr} can be calculated as

$$E_{\text{on},irr} = i_L \cdot v_{\text{DC}} \cdot (1 - \sigma_s) \cdot (t_2 - t_{1A}) + Q_{\text{rr}} \cdot v_{\text{DC}} \cdot (1 - \sigma_s). \quad (\text{A.9})$$

The first addend describes the losses related to the load current in the additional switching time caused by the reverse recovery effect. The second addend indicates the losses of the reverse recovery charge itself. On the basis of (2.21) and referring to Figure 2.4, this additional turn-on switching time can be expressed as

$$t_2 - t_{1A} = \frac{t_{\text{rr}}}{2} = \sqrt{\frac{Q_{\text{rr}}}{|di_C/dt|}}. \quad (\text{A.10})$$

Together with (A.9) this enables to derive the energy loss caused by the reverse recovery current in dependency of di_C/dt ,

$$E_{\text{on},irr} = \left(i_L \cdot \sqrt{\frac{Q_{\text{rr}}}{|di_C/dt|}} + Q_{\text{rr}} \right) \cdot v_{\text{DC}} \cdot (1 - \sigma_s). \quad (\text{A.11})$$

A.1.4 Summary

The total energy loss during turn-on can be calculated according to (A.1), i.e. by summing up (A.4), (A.8) and (A.11),

$$\begin{aligned}
 E_{\text{on}} = & \underbrace{\frac{i_{\text{L}} \cdot v_{\text{DC}}}{2} \cdot \left(\frac{i_{\text{L}}}{|di_{\text{C}}/dt|} + \frac{v_{\text{DC}}}{|dv_{\text{CE}}/dt|} \cdot (1 - \sigma_{\text{s}})^2 \right)}_{\text{Loss due to limited rates of } i_{\text{C}} / v_{\text{CE}} \text{ change}} + \\
 & \underbrace{\left(i_{\text{L}} \cdot \sqrt{\frac{Q_{\text{rr}}}{|di_{\text{C}}/dt|}} + Q_{\text{rr}} \right) \cdot v_{\text{DC}} \cdot (1 - \sigma_{\text{s}})}_{\text{Loss due to reverse recovery effect}} - \underbrace{\frac{1}{2} \cdot L_{\text{s}} \cdot i_{\text{L}}^2}_{\text{Energy to } L_{\text{s}}}. \tag{A.12}
 \end{aligned}$$

Thereby, on the one hand the limited rates of i_{C} and v_{CE} change as well as the reverse recovery charge of the freewheeling diode contribute to the energy loss. On the other hand, the stray inductance reduces the total turn-on energy loss as it absorbs a part of the DC-link voltage while being charged to the level of the load current. As will be shown in the next section, this gain of course is lost again during turn-off and does, hence, in sum not contribute to the overall switching losses, cf. Section A.3.

A.2 Turn-off

The main parts of the switching losses at turn-off are occurring during the intervals IX – XI of the switching operation, cf. Figure 2.8. The amount of the dynamic losses in the saturation region (interval VIII) and in the active region for large values of C_{GC} (t_6 , $t_{6\text{A}}$) is typically small in relation to the total switching losses for hard switched IGBTs and is, thus, neglected in the context of a simplification, here.

In sum, the total energy losses at turn-off can accordingly be calculated by adding the loss shares during the voltage slope, $E_{\text{off},dv/dt}$, during the current slope, $E_{\text{off},di/dt}$, and the loss component caused by the tail current, $E_{\text{off},\text{tail}}$,

$$E_{\text{off}} = E_{\text{off},dv/dt} + E_{\text{off},di/dt} + E_{\text{off},\text{tail}}. \tag{A.13}$$

A.2.1 Voltage Slope Related Loss

Assuming $i_C = i_L$ while v_{CE} rises, the energy loss during the voltage slope is given by

$$E_{\text{off},dv/dt} = \frac{i_L \cdot (v_{\text{DC}} + v_{\text{ov}})}{2} \cdot (t_7 - t_{6A}), \quad (\text{A.14})$$

where v_{ov} equals the the turn-off overvoltage which can be expressed by using (A.6) as

$$v_{\text{ov}} = L_s \cdot |di_C/dt| = v_{\text{DC}} \cdot \sigma_s. \quad (\text{A.15})$$

By calculating the time duration of this interval

$$t_7 - t_{6A} = \frac{v_{\text{DC}} + v_{\text{ov}}}{|dv_{\text{CE}}/dt|} \quad (\text{A.16})$$

and combining it with (A.14) and (A.15), the energy loss during the voltage rise can be described as a function of dv_{CE}/dt ,

$$E_{\text{off},dv/dt} = \frac{i_L \cdot v_{\text{DC}}}{2} \cdot \frac{v_{\text{DC}}}{|dv_{\text{CE}}/dt|} \cdot (1 + \sigma_s)^2. \quad (\text{A.17})$$

A.2.2 Current Slope Related Loss

If v_{CE} is assumed constant during the decay of the collector current, the resulting energy loss is

$$E_{\text{off},di/dt} = \frac{i_L \cdot (v_{\text{DC}} + v_{\text{ov}})}{2} \cdot (t_{7A} - t_7), \quad (\text{A.18})$$

and the corresponding time duration is

$$t_{7A} - t_7 = \frac{i_L}{|di_C/dt|}. \quad (\text{A.19})$$

By combining (A.18), (A.19) and (A.15), the energy loss during the current slope can also be calculated in dependency of di_C/dt ,

$$E_{\text{off},di/dt} = \frac{i_L \cdot v_{\text{DC}}}{2} \cdot \frac{i_L}{|di_C/dt|} + \frac{1}{2} \cdot L_s \cdot i_L^2. \quad (\text{A.20})$$

Here, the first term corresponds the switching energy loss for the case of $L_s = 0$ and the second term indicates the energy loss caused by the (parasitic) commutation loop inductance L_s .

A.2.3 Tail Current Related Loss

The energy loss caused by the extraction of the IGBT's stored charge Q_t via the tail current can be expressed as

$$E_{\text{off,tail}} = v_{\text{DC}} \cdot \int_{t_{\tau A}}^{t_s} i_C(t) dt = v_{\text{DC}} \cdot Q_t. \quad (\text{A.21})$$

The extracted charge Q_t depends on the IGBT's charge carrier lifetime and typically varies with the junction temperature $T_{j,T}$, with the duration of the turn-off switching transient, and with the amplitude and the shape of the collector-current during the conduction state [17–19].

A.2.4 Summary

The energy loss at turn-off can be calculated according to (A.13), i.e. by adding (A.17), (A.20) and (A.21),

$$E_{\text{off}} = \underbrace{\frac{i_L \cdot v_{\text{DC}}}{2} \cdot \left(\frac{v_{\text{DC}}}{|dv_{\text{CE}}/dt|} \cdot (1 + \sigma_s)^2 + \frac{i_L}{|di_C/dt|} \right)}_{\text{Loss due to limited rates of } i_C / v_{\text{CE}} \text{ change}} + \underbrace{v_{\text{DC}} \cdot Q_t}_{\text{Tail current loss}} + \underbrace{\frac{1}{2} \cdot L_s \cdot i_L^2}_{\text{Energy from } L_s}. \quad (\text{A.22})$$

In addition to the losses related to the limited rates of i_C and v_{CE} change as well as related to the tail current, the energy stored in the stray inductance contributes to the total energy loss at turn-off.

A.3 Total Energy Loss

For the sake of completeness, the total switching energy loss during turn-on and turn-off, E_{sw} , can be calculated as the sum of the turn-on energy E_{on} , (A.12), and the turn-off energy E_{off} , (A.22). In order to derive an informative and compact expression, identical absolute values of di_C/dt and dv_{CE}/dt are assumed for turn-on and for turn-off, here.

Hence,

$$\begin{aligned}
 E_{\text{sw}} = & \underbrace{i_{\text{L}} \cdot v_{\text{DC}} \cdot \left(\frac{i_{\text{L}}}{|di_{\text{C}}/dt|} + \frac{v_{\text{DC}}}{|dv_{\text{CE}}/dt|} \cdot (1 + \sigma_{\text{s}}^2) \right)}_{\text{Loss due to limited rates of } i_{\text{C}} / v_{\text{CE}} \text{ change}} + \\
 & \underbrace{\left(i_{\text{L}} \cdot \sqrt{\frac{Q_{\text{rr}}}{|di_{\text{C}}/dt|}} + Q_{\text{rr}} \right) \cdot v_{\text{DC}} \cdot (1 - \sigma_{\text{s}})}_{\text{Loss due to reverse recovery effect}} + \underbrace{v_{\text{DC}} \cdot Q_{\text{t}}}_{\text{Tail current loss}} \quad (\text{A.23})
 \end{aligned}$$

results. The reduction of the losses due to the parasitic stray inductance at turn-on is compensated by equal losses at turn-off, i.e. the two loss components are canceling out each other.

B

IGBT Module Parasitics and Model Parameters

IN order to perform a stability analysis of the proposed di_C/dt and dv_{CE}/dt closed-loop GD, the parameters of the small-signal IGBT model, cf. Figure 5.5, and their variations must be known. For that reason, in this chapter the parasitic inductances of three IGBT modules from different manufacturers are investigated and compared with each other. The remaining model parameters of the modules are subsequently extracted from the IGBTs' datasheets.

B.1 Parasitic Inductances

Parasitic inductances of an IGBT module are in general undesired. On the one hand, the total inductance in the power path L_{pp} contributes to the parasitic inductance L_s of the commutation loop, which is causing an overvoltage at the IGBT's turn-off transients, cf. Figure 3.1, and should thus typically be minimized by the manufacturers [121]. On the other hand, as shown in this thesis, the inductance in the gate loop L_{gl} is negatively affecting the achievable control bandwidth of the closed-loop IGBT GD, cf. Section 5.2.4.

Source of the IGBT module's parasitic inductances is the mechanical setup, which is consisting of the screw terminals for the power connections, the gate drive terminals and the internal wiring, e.g. via bond wires. Three IGBT half-bridge modules from different manufacturers in the 1.2 kV class with current ratings of 400-450 A (all in 62 mm housing) have been disassembled, in order to illustrate and compare their

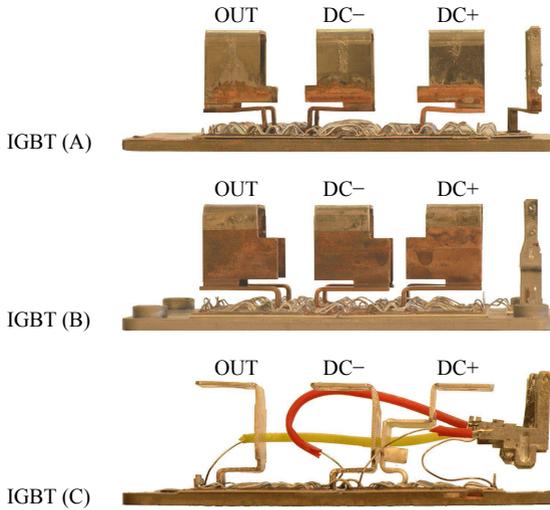


Figure B.1: Side view with visible construction of the screw terminals for the power connections of the disassembled half-bridge IGBT modules of manufacturers (A) - (C).

mechanical setups and parasitic inductances.

Figure B.1 depicts the construction of the IGBT module’s power terminals, which are a main reason for the parasitic inductance L_{pp} . It’s apparent that the DC+ and DC– terminals of modules (A) and (B) are located side by side, whereas a coplanar, i.e. low-inductance, layout is employed for module (C). According to the measured inductance values depicted in Figure B.3, module (C) exhibits the lowest value of L_{pp} as a result of its coplanar layout and module (A) shows the largest value of L_{pp} due to the parallel layout with large geometric distance.

The module’s internal gate and auxiliary emitter wirings are highlighted in Figure B.2 in order to compare the different manufacturing approaches. Bond wires are employed for modules (A) and (B) to interconnect the gate drive terminals and the IGBT chips resulting in similar values of the gate loop inductances, cf. Figure B.3. Module (C) uses, in addition to the bond wires, silicon insulated cables for the connection from the module terminals to the baseplate, what results in additional wiring loops and thus increased gate loop inductances.

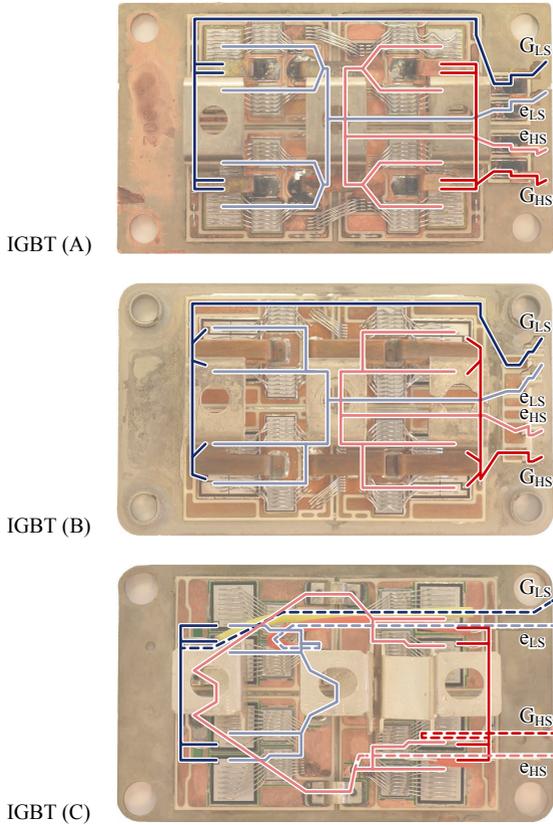


Figure B.2: Top view of the IGBT modules (A) - (C) with highlighted gate and auxiliary emitter connections (solid: bond wire connections; dashed: silicon insulated cabling).

Since the gate drive terminals are located next to the high-side IGBT and diode chips, the gate loop of the low-side IGBT is spatially more extended than the one for the high-side device as depicted in Figure B.2. Accordingly, for all three modules larger values result for the measured low-side gate loop inductances $L_{g1,LS}$ than for the high-side inductances $L_{g1,HS}$ as shown in Figure B.3. In order to investigate and experimentally verify the impact of reduced parasitic gate loop inductance on the closed-loop control, the high-side gate drive terminals of module

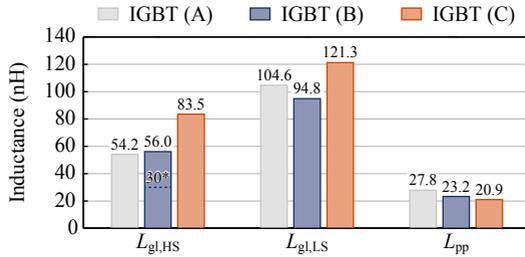


Figure B.3: Measured parasitic inductances of the three IGBT modules (A), (B) and (C), cf. Figure B.1 and Figure B.2. The gate loop inductance was measured between the gate and the auxiliary emitter terminals of the high-side ($L_{g1,HS}$) and the low-side ($L_{g1,LS}$) IGBT and the power path inductances were measured from the DC+ to the DC- connector with a straight connection for closing the measurement loop. A lower gate loop inductance $L_{g1,HS}$ of module (B) was achieved by bypassing the gate drive terminals, cf. Figure B.4.

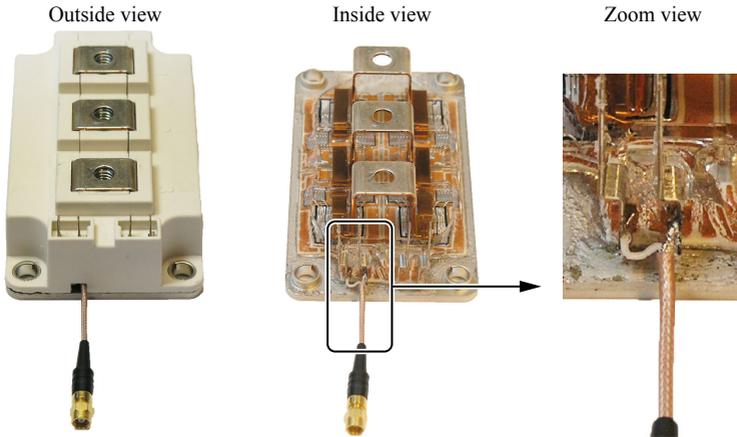


Figure B.4: Modified IGBT module (B) by means of a (low-inductance) coaxial connection soldered to the foot ends of the high-side gate terminals on the DBC, denominated as module (B)*. Bypassing the actual gate terminals by this measure reduces the gate-loop inductance by 26 nH and / or 46 % for the high-side.

(B) have been bypassed by a low-inductance coaxial connection, cf. Figure B.4. Therewith, $L_{\text{gl,HS}}$ of module (B) was reduced by 26 nH and / or 46 % as illustrated in Figure B.3. This modified module is denominated as module (B)* in this thesis ($L_{\text{gl,LS}}$ is not modified, as only the high-side switch is operated and only the freewheeling diode of the low-side switch is utilized).

B.2 Small-Signal IGBT Model Parameters

The remaining parameters of the IGBT model are derived from the IGBT's data sheets and are summarized in Table B.1. The values for the transconductance g_m at a current of $i_C = 200$ A, the gate capacitance

$$C_{\text{GE}} = C_{\text{ies}} - C_{\text{res}} \quad (\text{B.1})$$

and the Miller capacitance

$$C_{\text{GC}}(v_{\text{CE}}) \approx C_{\text{GC,ref}} \sqrt{\frac{v_{\text{CE,ref}}}{v_{\text{CE}}}} \quad (\text{B.2})$$

at a voltage of $v_{\text{CE}} = 300$ V can directly be extracted and calculated. The output capacitance

$$C_{\text{CE}} = C_{\text{oes}} - C_{\text{res}} \quad (\text{B.3})$$

is assumed to be smaller by a factor of 10 than C_{GC} . R_O is typically not specified in the data sheet, thus a typical value for an 1.2 kV, 400 A IGBT [69] is used. R_G and L_E have been measured with an impedance analyzer. The measured gate loop inductance, $L_{\text{gl,HS}}$, cf. Figure B.3, is assumed to be equally split to L_G and L_e . L_B is typically very small in modules with auxiliary emitter terminal and / or can hardly be measured, and was therefore estimated. Assuming that the inductance of the power path is split into two equal parts for the high and the low side IGBT,

$$L_C \approx L_{\text{pp}}/2 - L_B - L_E \quad (\text{B.4})$$

is used to calculate L_C .

	<i>IGBT (A)</i>	<i>IGBT (B)*</i>	<i>IGBT (C)</i>
g_m (S)	200	200	200
R_G (Ω)	2	2.05	1.62
L_B (nH)	1	1	1
L_E (nH)	2.1	3.85	3.2
L_C (nH)	11	6.75	6.25
L_G (nH)	27.1	15	41.7
L_e (nH)	27.1	15	41.7
C_{GE} (nF)	34.9	26.9	23
C_{GC} (nF)	0.61	0.32	0.87
C_{CE} (nF)	0.06	0.03	0.09
R_O (Ω)	50	50	50

Table B.1: Parameter values of the high-side IGBTs (A), (B)* and (C). Operating point: $v_{CE} = 300$ V, $i_C = 200$ A.

Nomenclature

Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
AUX	Auxiliary
BJT	Bipolar Junction Transistor
C	IGBT collector terminal
CM	Common-Mode
CPLD	Complex Programmable Logic Device
CTRL	Control
D	Diode
DAC	Digital-to-Analog Converter
DAGC	Decentralized Active Gate Control
DBC	Direct Bonded Copper
DC	Direct Current
DM	Differential-Mode
DOI	Digital Object Identifier
E	IGBT power emitter terminal
e	IGBT auxiliary emitter terminal
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FB	Feedback
FBSOA	Forward Bias Safe Operating Area
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
FUL	Failure Under Load
FWD	Freewheeling Diode
G	IGBT gate terminal
GaN	Gallium Nitride
GD	Gate Driver
HF	High Frequency
HS	High-Side
HSF	Hard Switching Failure
IGBT	Insulated-Gate Bipolar Transistor
LS	Low-Side
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NPT	Non-Punch Through

OP-AMP	Operational Amplifier
PCB	Printed Circuit Board
PFC	Power Factor Correction
PI	Proportional-Integral
PT	Punch Through
PV	Photovoltaics
PWM	Pulse-Width Modulation
RBSOA	Reverse Bias Safe Operating Area
SC	Short Circuit
SiC	Silicon Carbide
SOA	Safe Operating Area
STAT	Status
T	Transistor
UPS	Uninterruptible Power Supply

Physical Properties

General

C_{DC}	DC-link capacitance
D	Duty cycle
f_c	Corner frequency
f_s	Switching frequency
f_T	Transit frequency
h_{FE}	Current gain of a bipolar transistor
i_L	Load current
L_P	Load pulse inductor
L_s	Stray inductance of the commutation loop
$R_{th,c-a}$	Case-to-ambient thermal resistance
t	Time
$t_{d,gc}$	Turn-on gate charge delay time
$t_{d,GC}$	Charging time of $C_{GC,L}$ at turn-off
$t_{d,gd}$	Turn-off gate discharge delay time
$t_{d,on}$	Turn-on delay time
$t_{d,off}$	Turn-off delay time
t_s	Dead-time interval in which none of the two IGBTs of a bridge leg are turned-on
T_s	Switching period
v_{DC}	DC-link voltage

v_{out}	Bridge leg output voltage
$v_{\text{out,ref}}$	Bridge leg output voltage reference
$\bar{v}_{\text{out,err}}$	Averaged bridge leg output voltage error within T_s
v_{PWM}	PWM control command input
$v_S(t)$	PWM signal with defined rise / fall times
σ_s	Ratio between voltage drop across L_s and voltage v_{DC} during the current slope
$\tau_{\text{G,S}}$	Gate (dis)charging time constant for $C_{\text{GC,S}}$
$\tau_{\text{G,L}}$	Gate (dis)charging time constant for $C_{\text{GC,L}}$

IGBT

C_{CE}	Collector-emitter capacitance
C_{GC}	Gate-collector capacitance
$C_{\text{GC,S}}$	Gate-collector capacitance approximation valid for $v_{\text{CE}} \geq v_{\text{Ge}}$
$C_{\text{GC,L}}$	Gate-collector capacitance approximation valid for $v_{\text{CE}} < v_{\text{Ge}}$
C_{GE}	Gate-emitter capacitance
C_{ies}	Input capacitance, output shorted
$C_{\text{o es}}$	Output capacitance, input shorted
C_{res}	Reverse transfer / Miller capacitance
di_{C}/dt	Collector current time derivative
dv_{CE}/dt	Collector-emitter voltage time derivative
E_{off}	Turn-off switching energy loss
$E_{\text{off,di/dt}}$	Turn-off loss at current slope
$E_{\text{off,dv/dt}}$	Turn-off loss at voltage slope
$E_{\text{off,tail}}$	Turn-off loss caused by the tail current
E_{on}	Turn-on switching energy loss
$E_{\text{on,di/dt}}$	Turn-on loss at current slope
$E_{\text{on,dv/dt}}$	Turn-on loss at voltage slope
$E_{\text{on,irr}}$	Turn-on loss caused by the reverse recovery effect
E_{sw}	Turn-on + turn-off switching energy loss
$g_{m,s}$	Linearized transconductance
$i_{\text{C}}(t)$	Collector current
$i_{\text{C,N}}$	Maximum continuous collector current
$i_{\text{C,P}}$	Maximum repetitive pulsed collector current
$i_{\text{G}}(t)$	Gate current
K	Transconductance parameter of internal MOSFET

L_B	Common emitter inductance
L_C	Collector inductance
L_E	Emitter inductance
L_e	Auxiliary emitter inductance
L_G	Gate inductance
L_{gl}	Total gate loop inductance of the IGBT
L_{pp}	Total power path inductance of the IGBT module
Q_G	Gate charge
Q_t	Stored charge extracted by the tail current
r_D	Linearized collector-emitter on-state resistance
R_O	Output / Early resistance
$T_{j,T}$	Junction temperature
$v_{CE}(t)$	Collector-emitter voltage
$v_{CE,S}$	Maximum collector-emitter voltage
v_f	Collector-emitter forward voltage at linearization
$v_{Ge}(t)$	Gate-emitter voltage
$v_{Ge,L}$	Min. gate-emitter voltage at current i_L
$v_{Ge,L+rr}$	Min. gate-emitter voltage at current $i_L + \hat{i}_{rr}$
$v_{Ge,th}$	Gate-emitter threshold voltage
v_{ov}	Collector-emitter turn-off overvoltage
α_{BJT}	Current gain of the IGBT's internal BJT
τ_b	Current balancing time constant

Diode

di_D/dt	Anode-cathode current time derivative
i_D	Anode-cathode current
\hat{i}_{rr}	Peak reverse recovery current
Q_{rr}	Stored reverse recovery charge
$T_{j,D}$	Junction temperature
t_{rr}	Reverse recovery time
v_D	Diode forward voltage

Gate Driver

$G_{AMP}(s)$	Transfer function of the output amplifier
$G_{I,CL}(s)$	Closed-loop transfer function for di_C/dt control
$G_{I,OL}(s)$	Open-loop transfer function for di_C/dt control

$G_{OP}(s)$	Transfer function of the operational amplifier
$G_{PI}(s)$	Transfer function of the PI-controller
$G_{V,CL}(s)$	Closed-loop transfer function for dv_{CE}/dt control
$G_{V,OL}(s)$	Open-loop transfer function for dv_{CE}/dt control
$H_{I,HP}(s)$	Transfer function of the di_C/dt feedback
$H_{V,HP}(s)$	Transfer function of the dv_{CE}/dt feedback
k_G	Feedback gain of i_G
K_I	Integral part of the PI-controller
k_I	Feedback gain of di_C/dt
K_P	Proportional gain of the PI-controller
k_V	Feedback gain of dv_{CE}/dt
R_G	Gate resistor
$R_{G,min}$	Minimum gate resistor to attain critical damping
t_d	Interlocking dead-time
$t_{d,iso}$	Delay time of signal isolator
$v_{ctrl,clip}$	Control signal for the clipping circuit
$v_{ctrl,fb}$	Control signal for the feedback circuits
v_{ctrl,i_G}	Control signal for the i_G control
$v_{off,HS}$	Off-state signal of high-side IGBT gate driver
$v_{off,LS}$	Off-state signal of low-side IGBT gate driver
$v_{ref,d/dt}$	Reference signal for the di_C/dt and dv_{CE}/dt control
v_{ref,i_G}	Reference signal for the i_G control
$v_{trip,I/II}$	Short circuit type I/II detection trip signal
v_+	Positive gate drive voltage
v_-	Negative gate drive voltage
Δv_G	Difference between positive and negative gate drive voltages

List of Publications

Different parts of the research findings presented in this dissertation and of other research projects carried out in parallel have already been published or will be published in international scientific journals, conference proceedings, tutorials, workshops, technical magazines and / or have been protected by multi-national patents. The publications and patents developed in the course of this Ph.D. thesis are listed below.

Journal Papers

- ▶ Y. Lobsiger and J. W. Kolar, “Closed-loop di/dt and dv/dt gate driver for IGBTs in bridge leg configurations,” submitted for publication in *IEEE Trans. Power Electron.*
- ▶ Y. Lobsiger and J. W. Kolar, “Closed-loop di/dt and dv/dt IGBT gate driver,” *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3402–3417, Jun. 2015. DOI: [10.1109/TPEL.2014.2332811](https://doi.org/10.1109/TPEL.2014.2332811)

Conference Papers

- ▶ Y. Lobsiger, G. Ortiz, D. Bortis, and J. W. Kolar, “Concept and experimental evaluation of a novel DC–100 MHz wireless oscilloscope,” in *Proc. of the Int. Power Electron. Conf. (IPEC - ECCE Asia)*, Hiroshima, Japan, May 2014, pp. 1309–1316. DOI: [10.1109/IPEC.2014.6869755](https://doi.org/10.1109/IPEC.2014.6869755)
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