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Next-Generation Ultra-Compact/Efficient Data-Center Power Supply Modules

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presented by

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I am the way, and the truth, and the life;
no one comes to the Father except through Me.
– Jesus Christ (John 14:6)

Ich bin der Weg, und die Wahrheit, und das Leben;
niemand kommt zum Vater als nur durch mich.
– Jesus Christus (Johannes 14:6)

Eu sou o caminho, e a verdade, e a vida;
ninguém vem ao Pai senão por mim.
– Jesus Cristo (João 14:6)

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Gustavo Knabben

Abstract

The increasingly-electric future requires next-generation power supplies that are compact, efficient, low-cost, and ultra-reliable, even across mains failures, to power mission-critical electrified processes. Hold-up time requirements and the demand for ultra-high power density and minimum production costs, in particular, drive the need for DC/DC power converters with (i) a wide input voltage range, to reduce the size of the hold-up capacitor, (ii) soft-switching over the full input-voltage and load ranges, to achieve low losses that facilitate a compact realization, and (iii) complete PCB-integration for low-cost manufacturing. Wide-bandgap power semiconductors, with excellent on-resistance properties and low switching and reverse-recovery losses, come along these requirements toward the conceptualization of next-generation power-supply modules, but cannot alone catapult state-of-the-art converter technology to the performance baseline of future automotive, automated manufacturing and hyperscale data-center applications. Instead, the combination of wide-bandgap devices with proper converter topology, control and magnetics design has proven to be the real enabler of power supplies for the increasingly-electric future.

This thesis makes a case for the combination of these three features (wide-bandgap devices, proper topology/control and advanced magnetics) as the keys for paving the way toward next-generation power-supply modules. Therefore, a suitable low-complexity circuit topology with improved control scheme that operates across a wide-input-voltage range with complete soft-switching is identified, which switches efficiently at higher frequencies and high output currents with PCB-integrated magnetics, improving significantly power density compared to state-of-the-art designs. This topology embeds a sophisticated PCB-integrated matrix transformer that has a single path for the magnetic flux, ensuring equal flux linkage of parallel-connected secondary windings despite possible geometric PCB-layout asymmetries or reluctance imbalances. The so-called *snake-core* transformer avoids the emergence of circulating currents between parallel-connected secondary windings and guarantees proper operation of parallel-connected, magnetically-coupled converter modules.

The benefits of the proposed topology, control scheme and transformer design are validated by three fabricated 300 V-430 V-input, 12 V-output DC/DC hardware demonstrators. The converters utilize an LLC-based control scheme for complete soft-switching and the snake-core transformer to divide the output current with a balanced flux among multiple secondary windings. First, a 3 kW DC/DC series-resonant converter achieves 350 $\mathrm{W/in^3}$ (21.4 $\mathrm{kW/dm^3}$)

power density and 94 % peak efficiency, validating control and transformer operation. Then, a second hardware prototype with 1.5 kW showcases a peak efficiency close to 96 % and a power density of 337 W/in^3 (20.6 kW/dm^3), with full PCB-integration and zero-voltage switching even down to zero load. Finally, the third demonstrator—a magnetically-coupled, input-parallel/output-parallel, two-1.5 kW-module DC/DC converter—achieves a peak efficiency of nearly 97 % and a power density of 345 W/in^3 (21.1 kW/dm^3) with ideal current sharing among modules and stable operation, important characteristics enabled by the novel snake-core transformer. Detailed loss models are derived for every converter's component and the measurement results are in excellent agreement with the calculated values. These loss models are used to identify improvements to further boost efficiency, the most important of which is the minimization of delay times in synchronous rectification with either synchronous rectifier ICs embedded into the power-device's package or, at a minimum, Kelvin-source connections on high-current MOSFETs.

The results accomplished in this thesis indicate the necessity of careful topology/control selection and advanced-magnetics design for enabling WBG-based industrial power supplies that will outperform state-of-the-art solutions and catapult them to the next-generation performance standards. None of these features—be it WBG devices, wide-gain-range resonant converters, or advanced PCB-integrated magnetics—will alone enable next-generation power-supply modules, but the thoughtful combination of these technologies and their careful application to the particular application, with emphasis to high-frequency PCB magnetics and soft-switching topologies, which enable compact and cost-effective converters with competitive efficiencies.

Kurzfassung

Die zunehmende Elektrifizierung verschiedenster technischer Bereiche erfordert bereits heute, und insbesondere in Zukunft, Stromversorgungen, die immer kompakter, effizienter, kostengünstiger und zuverlässiger werden. Letzteres ist von besonderer Bedeutung für leistungselektronische Systeme, welche als Stromversorgungen ausfallskritischer elektrischer Prozesse eingesetzt werden, da die Energieversorgung auch im Falle eines kurzzeitigen Netzausfalls nicht unterbrochen werden darf. Insbesondere die Anforderungen an die Überbrückungszeit, sowie die Forderung nach ultrahoher Leistungsdichte und minimalen Produktionskosten, erfordern Gleichspannungswandler mit (i) einem weiten Eingangsspannungsbereich, um die Größe des Überbrückungskondensators zu reduzieren, (ii) einer effizienten Ansteuerung der Halbleiter über den gesamten Eingangsspannungs- und Lastbereich, um die Verluste zu minimieren, was wiederum eine kompakte Realisierung ermöglicht, und (iii) einer vollständigen PCB-Integration der Wicklungen der magnetischen Komponenten, was in einer kostengünstigen Fertigung resultiert. Auch wenn in den letzten Jahren dank der Entwicklung immer besserer Wide-Bandgap Halbleitertechnologien grosse Fortschritte bezüglich der Optimierung des Schaltverhaltens von elektrisch gesteuerten Schaltern erreicht wurden, so ist dies dennoch nicht genug, um die zuvor erwähnten Anforderungen an künftige leistungselektronische Systeme optimal zu erfüllen. Dies kann nur mit einer Kombination aus einer optimalen Schaltungstopologie, den neuesten Halbleitertechnologien, einer ausgefeilten Steuerung, sowie optimal entworfenen magnetischen Komponenten erreicht werden.

In dieser Arbeit werden die oben genannten Punkte zuerst einzeln analysiert und optimiert, um anschliessend die gewonnenen Erkenntnisse zu kombinieren und den Weg zu Gleichspannungswandlern der nächsten Generation zu ebnen. Im Detail wird auf diesem Weg zuerst eine geeignete Schaltungstopologie mit geringer Komplexität und einem verbesserten Steuerungsschema entwickelt, welche einen weiten Eingangsspannungsbereich abdecken und dabei die Halbleiter trotzdem weitestgehend verlustfrei schalten kann. Dies erlaubt einen effizienten Betrieb auch bei sehr hohen Frequenzen und hohen Ausgangsströmen, wodurch das Volumen der PCB-integrierten magnetischen Komponenten reduziert, und die Leistungsdichte des gesamten Systems, im Vergleich zum heutigen Standard, erheblich verbessert wird. Diese Topologie verwendet einen neuartigen PCB-integrierten Matrixtransformator, der dem magnetischen Fluss nur einen einzigen Pfad bietet und dadurch eine perfekte Symmetrierung der sekundärseitigen Ausgangsspannungen garantiert, auch wenn aufgrund möglicher geometrischer Asymmetrien in den PCB-

integrierten Wicklungen in einem konventionellen Matrix Transformator unterschiedliche sekundärseitige Spannungen resultieren würden. Entsprechend vermeidet der sogenannte Snake-Core-Transformator aufgrund seines internen Aufbaus das Auftreten von Kreisströmen zwischen den parallel geschalteten Sekundärwicklungen und garantiert so auch einen symmetrischen und effizienten Betrieb im Falle mehrerer parallelgeschalteter, magnetisch gekoppelter Wandlermodule.

Die Vorteile der verwendeten Topologie, des entwickelten Steuerschemas und des Snake-Core-Transformators, gegenüber konventionellen Ansätzen, werden mittels drei DC/DC-Hardware-Prototypen mit einer Eingangsspannung von 300 V bis 430 V, einer Ausgangsspannung von 12 V und einer maximalen Ausgangsleistung von 3 kW validiert. Die Wandler verwenden dabei ein Steuerschema, welches auf demjenigen des bekannten LLC-Resonanzkonverters basiert, jedoch, im Gegensatz zu herkömmlichen Steuerverfahren, über den gesamten Eingangsspannungs- und Ausgangsleistungsbereich weiches Schalten der Halbleiter garantiert. Des Weiteren erlaubt es der Snake-Core-Transformator, den hohen Ausgangsstrom, dank des identischen magnetischen Flusses in allen Wicklungen, gleichmässig auf mehrere Sekundärwicklungen aufzuteilen, wodurch die sekundärseitige Synchrongleichrichtung des Ausgangsstroms erheblich erleichtert wird.

Der erste Hardwareprototyp, ein galvanisch getrennter Serienresonanzwandler, liefert eine maximale Ausgangsleistung von 3 kW bei einer Leistungsdichte von 350 $\mathrm{W/in^3}$ (21.4 $\mathrm{kW/dm^3}$) und einem maximalen Wirkungsgrad von 94 %. Diese Hardware wurde primär für die Validierung des Steuerschemas sowie des reibungslosen Betriebs des Snake-Core-Transformators entwickelt. Der zweite Hardwareprototyp liefert eine maximale Ausgangsleistung von 1.5 kW und weist einen maximalen Wirkungsgrad von fast 96 % bei einer Leistungsdichte von 337 $\mathrm{W/in^3}$ (20.6 $\mathrm{kW/dm^3}$) auf. Bei diesem Prototypen wurden erstmals die Wicklungen aller magnetischen Komponenten in die Leiterplatte (PCB) integriert und dank einer Erweiterung des Steuerschemas können die Halbleiter auch ohne Last am Ausgang weich geschaltet werden, was die Effizienz im Niedriglastbetrieb verbessert. Der dritte Demonstrator besteht aus zwei magnetisch gekoppelten 1.5 kW Modulen, welche sowohl eingangsseitig als auch ausgangsseitig parallelgeschaltet sind. Dieser Prototyp erreicht einen maximalen Wirkungsgrad von nahe 97 % bei einer Leistungsdichte von 345 $\mathrm{W/in^3}$ (21.1 $\mathrm{kW/dm^3}$). Dabei teilt sich der Ausgangsstrom ohne aktive Symmetrierungsregelung perfekt symmetrisch auf beide Module auf, wodurch ein äusserst effizienter und stabiler Betrieb des Konverters resultiert, was nur dank des neuartigen Snake-Core-Transformators möglich ist.

Die Messresultate der Hardwareprototypen stimmen hervorragend mit den zuvor hergeleiteten Verlustmodellen der verschiedenen Leistungskomponenten überein, weshalb diese Verlustmodelle anschliessend verwendet werden, um mögliche weitere Verbesserungen bezüglich Effizienz der Systeme zu identifizieren. Einer der wichtigsten Punkte, welche in zukünftigen Wandlern die Effizienz noch weiter steigern könnte, ist, die Verzögerungszeit der sekundärseitigen Synchrongleichrichter zu minimieren, da die hohen sekundärseitigen Ströme, in Kombination mit dem Vorwärtsspannungsabfall der antiparallelen Diode der MOSFETs, zu hohen Leitverlusten während der Stromnulldurchgänge führen. Dies ist mit heutigen Halbleitern schwierig, könnte jedoch in Zukunft mit im Halbleiterchip integrierten Synchrongleichrichter-Steuer-ICs erheblich verbessert werden. Alternativ würden nur schon dedizierte Anschlüsse im Gehäuse der Schalter (Kelvin-Kontakte) für die Messung der Drain-Source Spannung über den MOSFETs das Problem entschärfen.

Die in dieser Arbeit erzielten Ergebnisse zeigen klar, dass es nicht reicht, nur eine einzelne Komponente eines kompletten Systems zu verbessern, da die Zusammenhänge zwischen dem Design-Space und dem Performance-Space extrem komplex und oft nicht bis ins letzte Detail analysierbar sind. Sprich, gibt es eine technologische Neuerung/Verbesserung für eine Komponente (z. B. die Entwicklung der Wide-Bandgap Halbleitertechnologie), ist es nicht ausreichend diese Technologie direkt in bestehende Systeme einzubauen, da ihr volles Potential so bei weitem nicht ausgenutzt wird. Um die neuen Möglichkeiten voll auszuschöpfen muss das gesamte System, vom Konzept über die Schaltungstopologie bis zur Optimierung der einzelnen Komponenten, von Grund auf neu analysiert werden. Nur so ist es möglich, neue, effiziente, kompakte und vor allem wettbewerbsfähige Wandler für verschiedene Anwendungen zu entwickeln.

Abbreviations

3-D	Three-Dimensional
AC	Alternating Current
BCM	Boundary Conduction Mode
CCM	Continuous Conduction Mode
CNC	Computerized Numerical Control
CPU	Central Processing Unit
CT	Current Transformer
Cu	Copper
DAB	Dual Active Bridge
DCM	Discontinuous Conduction Mode
DSAB	Double-Stacked Active Bridge
DC	Direct Current
DCX	Direct Current Transformer
EV	Electric Vehicle
Fe	Iron/Ferrite
FEM	Finite Element Method
FHA	Fundamental Harmonic Approximation
GaN	Gallium Nitride
HEMT	High-Electron-Mobility Transistor
HV	High Voltage
IC	Integrated Circuit
ICT	Information and Communication Technology
IP	Input Parallel
IS	Input Series
IT	Information Technology
LC	Inductor-Capacitor
LDO	Low Drop Out
LLC	Inductor-Inductor-Capacitor
LV	Low Voltage
MCU	Microcontroller Unit
MMF	Magnetomotive Force
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OP	Output Parallel
OS	Output Series
PCB	Printed Circuit Board
PE	Protective Earth
PSFB	Phase-Shifted Full-Bridge

PSU	Power Supply Unit
PWM	Pulse-Width Modulation
RMS	Root Mean Square
SCT	Snake-Core Transformer
Si	Silicon
SiC	Silicon Carbide
SR	Synchronous Rectifier/Rectification
UAV	Unmanned Aerial Vehicles
WBG	Wide Bandgap
ZCD	Zero-Current Detection
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Contents

1 Introduction

After centuries of curiosity around electrical phenomena—with ancient Egyptians already aware of shocks from electric fish even 2750 years before Christ [1]—and a rather slow progress in electrical science, the late 19th century would be marked by the greatest development in electrical engineering that the world had ever seen. Well-known names as Bell, Edison, Tesla, Westinghouse and many others [2] would turn electricity from a scientific curiosity into an essential tool for modern life—and use inventions/discoveries from Volta, Ampère, Faraday, Ohm and Maxwell (among other great scientists) to drive the way we handle energy in our current days. Since then, electric power usage continues to grow rapidly in a contemporary world reliant on electricity for its prime source of energy [3].

Three main areas could be pointed out when discussing the increasingly-electric future, also illustrated in Fig. 1.1:

- **Sustainable Transportation:** as all-electric ships, more-electric aircraft and electric heavy-duty vehicles start to become reality along with the on-going electrification of automobiles and the established railway industry [4–6];
- **Automated Manufacturing:** with electricity as the primary source of energy driving different kinds of robots, CNC systems and automated processes in very efficient and reliable production lines [7, 8]; and
- **Information Processing:** as digital data drives the current society in all spheres imaginable, not only in the day-by-day use of gadgets, but also in the so called Industry 4.0 [9], with server systems and data centers being the brains of what is now named as the Information Age [10].

(a) (b) (c)

Fig. 1.1: Non-exhaustive examples for the three main areas of electrification of the increasingly-electric future: (a) transportation, here illustrated by the EV Tesla Model S, (b) automated manufacturing, with different kinds of electronically-controlled machines here represented by a collaborative robot from ABB, and (c) information processing, for instance, the hyperscale data centers from Google. Images from the public domain.

In the midst of this very exciting context, power electronics plays a key role in designing supply systems to cope with the ultra-demanding specifications required by the aforementioned areas of electrification. These supplies may, for example, drive servo systems, charge EV batteries or energize IT systems, and the low-voltage output must deliver hundreds of amperes of current while the system still excels in performance [7, 8], achieving:

- **High power density:** with real estate at a premium and supply cabinets already consuming space otherwise available for functional equipment;
- **High efficiency:** with supplies rarely operating at full load and heat generation in cabinets driving cooling needs; and
- **Low cost:** with low initial and/or installation costs as the critical metric for adoption.

Besides the ultra-demanding performance, such power supplies must also be reliable and fulfil hold-up time criteria. This is particularly important for the data industry, but not less critical in the other fields of electrification, as mere moments of power supply downtime potentially translate to costly hours of downtime for the plant. Therefore, the design of a next-generation power supply module that fulfils the demanding specifications of the increasingly-electric future is a challenging task for the industry that requires attention.

1.1 Challenges in Designing Next-Generation Power Supply Modules

From all three fields of electrification mentioned, power supply units (PSU) for information and communication technology (ICT) have the most demanding requirements. It is therefore reasonable to take server and data-center PSUs as benchmarks to address challenges and derive key specifications for this next-generation power supply module. For the general PSU of Fig. 1.2(a), commercially-available solutions are galvanically-isolated and typically designed for an output power (P_o) between 2 kW and 3 kW, a low-output voltage (V_o) of 12 V, and a single-phase-mains AC input voltage (v_{in}) of 180-270 V at 47-63 Hz [11–13]. Although some hyperscale data centers have adopted the 48 V bus architecture [14–16], 12 V power supplies still dominate industrial applications, specially now that 380 V/400 V DC distribution and direct conversion to 12 V is being considered [17–19]. The PSU form factor in these applications is standardized to one-unit height (1U—44 mm) and to 72 mm width (with exceptions diverging only by few millimeters)—see Fig. 1.3. The length depends on the rated power and ultimately defines the supply's power density, which is linked to its efficiency: if striving for 80-PLUS-Titanium performance [20] (96 % efficiency at 50 % load), typical power densities in off-the-shelf products vary between 60 W/in^3 (3.7 kW/dm^3) and 70 W/in^3 (4.3 kW/dm^3) [11, 12]. On the other hand, supplies certified for lower efficiencies achieve higher power densities, for instance up to 75 W/in^3 (4.6 kW/dm^3) in 80-PLUS-Platinum certificates (94 % efficiency at 50 % load) [13].

The low-voltage output in these high-reliability supplies must bridge short mains faults and, with a complete mains failure, hold-up V_o long enough for a safe shutdown of the digital and physical systems (see Fig. 1.2(b)). This is so critical for continuous line operation that batteries are sometimes added to commercially-available industrial power supplies in this class to extend hold-up time [8]. When batteries are not installed, two stages of conversion is the typically-adopted solution, as the required energy for holding-up V_o is stored in the DC-link capacitor (C_{dc}). The hold-up time requirement could also be met with additional converters, for example with (i) a partial-power pre-regulation converter and a fixed-voltage-ratio DC/DC converter [21], (ii) a hold-up time extension circuit [22], or (iii) a reverse-feeding concept [23]. Each of these solutions adds complexity, size and cost in the form of an additional power stage. Instead, the combination of a low-volume C_{dc} and a wide-input-voltage-range DC/DC converter offers the most cost-effective and low-complexity solution to meet the hold-up time requirement, and is

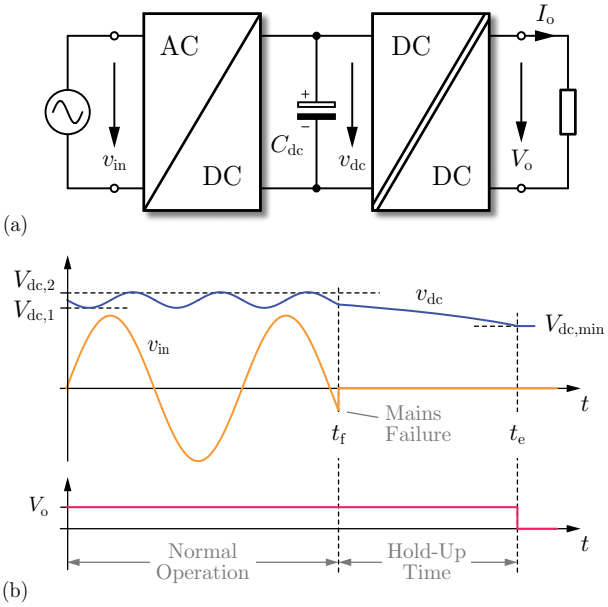

Fig. 1.2: (a) Industrial power supply block diagram to convert the AC-mains voltage to a low-voltage/high-current DC output. The capacitance of the DC-link capacitor (C_{dc}) is mainly determined by the hold-up time requirements during fault conditions, as shown in (b).

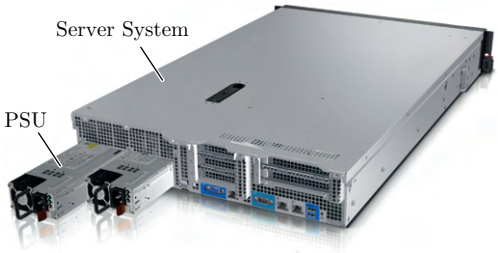

Fig. 1.3: Lenovo ThinkSystem® server solution from the rear-side perspective, with highlight to the two available power supply units (PSUs) for a 1+1 redundancy scheme.

assumed here as the most promising approach to catapult state-of-the-art PSUs to the performance baseline of the next generation.

An ambitious industry- and academia-relevant target is to aim for a high-density 3 kW supply with 100 W/in^3 (6.10 kW/dm^3) that fulfils the 80-PLUS-Titanium efficiency standard (see Fig. 1.4(a)). For this power density, a volume of 491 cm^3 must be partitioned between all power supply elements, including AC/DC and DC/DC stages, DC-link capacitor, AC connector and cooling fan. Both connector and fan (ideal for this power range [24], see Appendix A) already account for 16 % of the total available volume. Furthermore, taking a typical specific capacitance of 267 µF/in^3 (for box-volume, ultra-compact, 450 V electrolytic capacitors, e.g. *450USK1000MEFCSN35X55*), C_{dc} = 1 mF would occupy additional 14 % of the allotted volume, leaving the remainder 70 % to be equally shared between AC/DC and DC/DC stages (see Fig. 1.4(b,c)), and requiring 300 W/in^3 (18.3 kW/dm^3) designs for both.

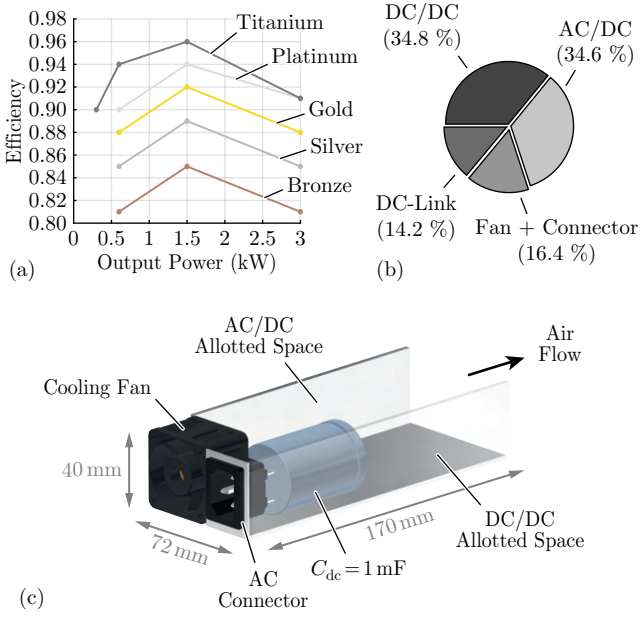

Fig. 1.4: (a) Efficiency standards of the voluntary certification program 80-PLUS launched in 2004 to promote efficient energy use in computer PSUs [20]. (b,c) Proposed volume partitioning of a 3kW PSU with 100 W/in^3 (6.10 kW/dm^3) to benchmark the next-generation power module.

This 1 mF DC-link capacitor would provide $t_e - t_f = 10$ ms of hold-up time at 80 % load ($P_o = 2.4$ kW), calculated from:

$$t_e - t_f = \frac{\eta_{dc} C_{dc}}{2P_o} \left(V_{dc,1}^2 - V_{dc,min}^2 \right), \tag{1.1}$$

fulfilling one typical hold-up-time requirement of highly-compact server PSUs. $\eta_{dc} = 0.96$ is the DC/DC expected efficiency at 80 % load, $V_{dc,min} = 300$ V is the minimum allowed DC-link voltage (selected as a good compromise between the remaining stored energy and DC/DC controllability), and $V_{dc,1}$ is calculated from the $C_{dc} = 1$ mF voltage ripple:

$$V_{dc,2} - V_{dc,1} = \frac{P_o}{2\pi f \eta_{dc} C_{dc} \frac{V_{dc,2}+V_{dc,1}}{2}}, \tag{1.2}$$

assuming $(V_{dc,2} + V_{dc,1})/2 = 400$ V as the nominal DC-link voltage and $f = 47$ Hz as the worst-case v_{in} frequency. Finally, with all these constraints and assumptions considered, the DC/DC converter would need to operate from $V_{dc,min} = 300$ V to $V_{dc,2} = 430$ V, a wide-input-voltage range. This input range is taken as a requirement, knowing that the required PSU power density will not be achieved if additional capacitance is added to narrow this range.

Ultimately, with power-density prescribing such a high switching frequency that soft-switching is required, and initial costs driving the need of full PCB integration (including magnetics), the major design challenge to be addressed is the topology and control of an isolated, soft-switching, PCB-integrated, wide-voltage-range-input, low-voltage-output DC/DC converter which simultaneously meets the efficiency *and* power-density specifications. The efficiency of this converter should be high enough that the PSU is certified as 80-PLUS-Titanium. A converter with such high-demanding prescriptions cannot be found in commercially-available supplies and is titled here as the next-generation DC/DC power supply module, whose specifications are summarized in Tab. 1.1. With the main challenges addressed and key specifications identified, we move to the analysis of state-of-the-art solutions and to the definition of the thesis's contribution and scope.

1.2 State of the Art of DC/DC Power Supply Modules

Literature offers a broad range of solutions concerning DC/DC power modules. The challenges addressed in Section 1.1 and the design constraints of Tab. 1.1

Tab. 1.1: Design specifications of the isolated, soft-switching, PCB-integrated DC/DC power module for next-generation PSUs.

Full-load output power (P_o)	3 kW
Output voltage (V_o)	12 V
Input voltage range ($V_{dc,min}$-$V_{dc,2}$)	300 V-430 V
Full-load output current (I_o)	250 A
Power density	300 W/in^3 (18.3 kW/dm^3)
Efficiency at 1.5 kW	> 0.96
Galvanically isolated	Yes
Soft-switching	Yes
PCB-integrated	Yes

help to narrow down this range and to get more specific with the literature review, culminating in the selection of:

- **Isolated** over non-isolated topologies,
- **Regulated** over fixed-ratio converters,
- **Wide** over narrow input-voltage ranges,
- **Simple** over complex control schemes,
- **PCB** over litz-wire magnetics, and
- **Soft** over hard switching.

Following the survey conducted by [25], where potential topology candidates are sorted out according to the aforementioned categories, two big groups are identified as suitable:

- **Buck-based topologies:** essentially the full-bridge DC/DC converter, the dual-active-bridge (DAB) converter, or topological derivations. These isolated topologies support a wide-input-voltage range, but are hard-switched (over at least part of the regime) and therefore have low efficiency [26–29]. Moreover, due to the lack of soft-switching, these converters require voltage-clamping circuits to avoid voltage overshoots across semiconductor devices (in case of high output current/low output voltage [27]), or passive snubbers further decreasing

efficiency, or active snubbers increasing their complexity, or additional resonant networks. They also suffer from currents with high harmonic content and increased conduction losses.

- **LLC-based topologies:** resonant converters with two, three or more resonant-tank elements, and the LLC combination as the most popular choice. These isolated converters are soft-switched, have low-harmonic-distortion currents and have high efficiencies even at high switching frequencies, but are limited by a narrow input voltage range [30–35] that, in this application, would result in an unreasonably-large DC-link capacitor to meet hold-up specifications. At the extreme of narrow input voltage ranges, DC transformers ("DCX") with a fixed voltage conversion ratio require a full additional pre-regulation stage or, at a minimum, a differential-power pre-regulation stage [21].

With these two topological groups in mind, a survey of published converters near the design specifications of Tab. 1.1 is conducted and compiled in Tab. 1.2. Three soft-switched, PCB-integrated and 12 V-output converters (see Fig. 1.5) stand out from all researched designs with unprecedented power densities and/or efficiencies, suggesting that soft-switching and PCB-integration are indeed key technologies to enable high-density and efficient DC/DC power modules. Moreover, at least two of these three converters take advantage of wide-bandgap (WBG) power semiconductors in their designs, in particular gallium nitride (GaN), indicating that GaN devices—with excellent specific R_{on} and zero reverse-recovery losses [36, 37]—are essential to increasing switching frequency and achieving higher power densities (see Fig. 1.6).

(a) (b) (c)

Fig. 1.5: Examples of PCB-integrated, soft-switched, 12 V-output DC/DC power modules with unprecedented efficiency and/or power density: (a) LLC with matrix transformer from CPES / Virginia Tech [32], (b) double-clamp ZVS from VICOR Corporation [38], and (c) PSFB with current injection from Rompower Energy Systems [39].

Tab. 1.2: Survey of published converters near the design specifications of Tab. 1.1. Efficiency is given at nominal load ($1.0P_o$) and 50 % of nominal load ($0.5P_o$).

Ref.	Topology	Full ZVS	v_{dc}	V_o / I_o	Power Density	Eff. ($1.0P_o$)	Eff. ($0.5P_o$)	PCB-int.
[30, 31]	LLC	Yes	380 V	12 V / 83 A	700 W/in^3	96.5 %	97.1 %	Yes
[32]	LLC	Yes	380 V	12 V / 67 A	900 W/in^3	97.2 %	97.6 %	Yes
[33]	LLC	Yes	200 V-420 V	12 V / 83 A	—	91.2 %	96.0 %	No
[33]	PSFB	No	200 V-420 V	12 V / 83 A	—	92.4 %	96.0 %	No
[41]	PSFB	Yes	270 V	22 V / 68 A	—	93.2 %	96.0 %	No
[42]	PSFB	Yes	230 V-430 V	14 V / 150 A	170 W/in^3	95.0 %	96.0 %	Yes
[39, 43]	PSFB	Yes	330 V-420 V	12 V / 83 A	300 W/in^{3**}	97.8 %*	99.1 %*	Yes
[38, 44]	Double-clamp	Yes	180 V-420 V	12 V / 33 A	826 W/in^{3***}	93.0 %	93.5 %	Yes
[29]	Half-bridge	No	150 V-400 V	12 V / 167 A	—	91.8 %	94.7 %	No
[27]	DAB	No	240 V-450 V	12 V / 182 A	25 W/in^3	93.5 %	95.0 %	No
[28]	DSAB	No	350 V-410 V	12 V / 25 A	$\approx$ 20 W/in^3	95.9 %	97.0 %	Yes

*Driving losses not included

**Apparently not including auxiliary circuits and control

***Package without external-required passives and heat sink

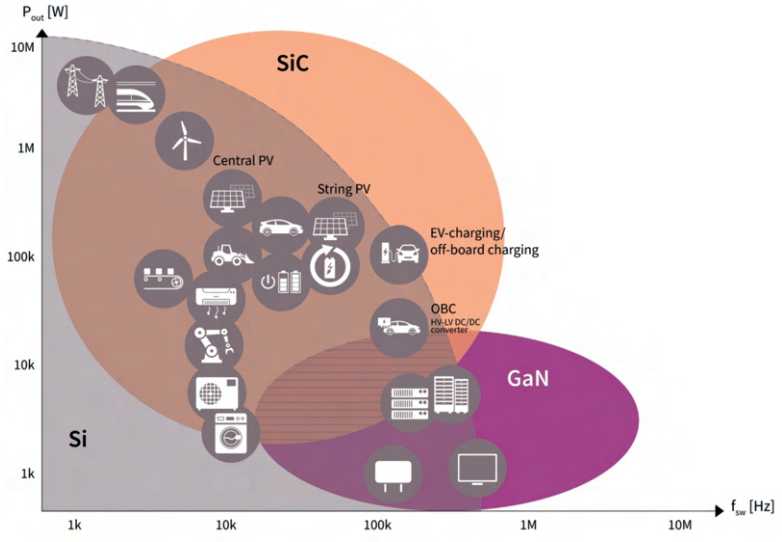

Fig. 1.6: Power-*versus*-frequency map of suitable semiconductor technologies in selected power-electronics applications, with GaN devices particularly enabling switching-frequency increase by one order of magnitude in kW-range server and data-center power supplies [40].

The CPES/Virginia Tech LLC power module [32] (see Fig. 1.5(a)) reaches 900 W/in^3 and a peak efficiency of 97.6 %, but operates with fixed input voltage and, therefore, does not qualify as a wide-voltage-range converter. The ultra-compact double-clamp *DCM4623xD2J13Do7yz* power module from VICOR Corporation [38] (see Fig. 1.5(b)) has very high power density with a wide-voltage-range controllability, but has a maximum efficiency of only 93 %. Finally, the ultra-efficient phase-shifted-full-bridge (PSFB) power module from Rompower Energy Systems [39] (see Fig. 1.5(c)) achieves an unprecedented 99.1 % peak efficiency with a wide-input-voltage range (without considering driving losses of switching elements [43]), but has limited power density and requires module scaling to reach the desired 3 kW output, which further reduces power density with additional interfacing PCBs and connectors [45]. Although power density could be traded off with efficiency here, this 99 %-efficient converter uses Rompower current-injection technology, which is legally protected [46–49] and adds significant complexity to the

control scheme (with additional voltage, current and temperature measurements [43]).

Indeed, upon reviewing the literature, there is no prior art that meets the demanding specifications of this next-generation DC/DC power module as specified in Tab. 1.1. In particular, wide-input-voltage range, complete soft-switching, and high-current 12 V output with PCB-integrated magnetics are rarely found together. Adding the low-complexity-control-scheme requirement makes the conceptualization, design and implementation of this next-generation DC/DC power module very challenging—but also appropriate to be investigated in the scope of this PhD thesis.

1.3 Aims and Contributions

The goal of this work is to conceptualize, design, model, and fabricate a cost-effective power supply module that meets the demanding specifications of high-reliability industrial applications while maximizing efficiency and power density (Tab. 1.1). More specifically, this wide-range-input, low-voltage-output DC/DC converter has to be isolated, soft-switching, PCB-integrated and regulated by a simple control scheme, a combination that has not been realized previously in the literature.

To achieve these difficult specifications, we leverage GaN power semiconductors to push the switching frequency up by an order of magnitude and improve power density. These high switching frequencies, though, introduce new design challenges to be addressed: firstly, high-frequency magnetics that are cost-effective, efficient, and small are required, for which innovations in PCB integration are proposed and validated. Secondly, a proper topology and control scheme must be selected to achieve soft-switching, low RMS-to-average current ratios, controllability, and a wide-input-voltage range, for which we combine the controllability of buck-based converters and the efficiency of soft-switched LLC topologies. Tab. 1.3 shows the impact of each design choice in the general power-module performance. Ultimately, we seek to prove that the design of a next-generation DC/DC power module is only possible by the *combination* of WBG power semiconductors with advanced PCB-integrated magnetics and proper topology/control.

Tab. 1.3: Key characteristics and technologies that, if combined, will potentially enable reliable, cost-effective, compact and efficient next-generation DC/DC power modules.

Goal	Means
Reliability & safety	Voltage regulation
	Hold-up time
	Low-complexity system
	Galvanic isolation
Low cost	PCB-integrated magnetics
	Low-complexity system
High power density	High switching frequency
	PCB-integrated magnetics
High efficiency	WBG power semiconductors
	Soft switching
	Proper topology & control

1.4 List of Publications

Key insights presented in this thesis have been published in international scientific journals, conference proceedings, or presented at workshops. The publications created as part of this thesis, or in the scope of related projects, are listed below in reverse-chronological order.

1.4.1 Journal Papers

- **G. C. Knabben**, G. Zulauf, J. Schäfer, J. W. Kolar, M. J. Kasper, , J. Azurza Anderson, G. Deboy, "Conceptualization and analysis of a next-generation ultra-compact 1.5-kW PCB-integrated wide-input-voltage-range 12V-output industrial DC/DC converter module," *Electronics* **2021**, 10, 2158. DOI: 10.3390/electronics10172158, [PDF].

- D. Neumayr, **G. C. Knabben**, E. Varescon, D. Bortis and J. W. Kolar, "Comparative evaluation of a full- and partial-power processing active power buffer for ultracompact single-phase DC/AC converter systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 2, pp. 1994-2013, 2021. DOI: 10.1109/JESTPE.2020.2987937, [PDF].

1.4.2 Conference Papers

- **G. C. Knabben**, J. Schäfer, J. W. Kolar, G. Zulauf, M. J. Kasper and G. Deboy, "Wide-input-voltage-range 3 kW DC-DC converter with hybrid LLC & boundary / discontinuous mode control," in *Proc. of IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2020. DOI: 10.1109/APEC39645.2020.9124410, [PDF].

- M. J. Kasper, L. Peluso, G. Deboy, **G. Knabben**, T. Guillod and J. W. Kolar, "Ultra-high power density server supplies employing GaN power semiconductors and PCB-integrated magnetics," in *Proc. of International Conference on Integrated Power Electronics Systems (CIPS)*, March 2020. DOI: not available, [PDF].

- **G. C. Knabben**, J. Schäfer, L. Peluso, J. W. Kolar, M. J. Kasper and G. Deboy, "New PCB winding "snake-core" matrix transformer for ultra-compact wide DC input voltage range hybrid B+DCM resonant server power supply," in *Proc. of IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Nov 2018. DOI: 10.1109/PEAC.2018.8590430, [PDF].

  Best-Presenter-at-the-Session Award

- **G. C. Knabben**, D. Neumayr and J. W. Kolar, "Constant duty cycle sinusoidal output inverter with sine amplitude modulated high frequency link," in *Proc. of IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018. DOI: 10.1109/APEC.2018.8341372, [PDF].

1.4.3 Workshops and Seminars

- **G. C. Knabben**, J. Schäfer, J. W. Kolar, M. J. Kasper, and G. Deboy, "Key enablers for ultra-compact server power supplies," presented at *TechTalks at Infineon Technologies Austria AG*, Villach, Austria, Oct 2020. DOI: not available, [PDF].

1.5 Thesis Outline

According to the goals and contributions mentioned above, the content of the thesis is divided into five main chapters and conclusions. All the chapters can be read independently, since the interdependencies have been reduced to the strict minimum.

- **Chapter 2** identifies a suitable low-complexity circuit topology and control scheme that operates across the wide-input-voltage range with complete soft-switching, implementing a new hybrid wide-input-range LLC control for a topology that includes a full-bridge primary and a matrix transformer for multiple high-current outputs. With this topology, the converter can operate efficiently at higher frequencies and high output currents with PCB-integrated magnetics, significantly improving power density compared to state-of-the-art designs.

- **Chapter 3** introduces the "Snake-Core" Transformer, a PCB-integrated matrix transformer that has a single path for the magnetic flux, ensuring equal flux linkage of parallel-connected secondary windings despite possible geometric PCB-layout asymmetries or reluctance imbalances. This approach avoids the emergence of circulating currents between parallel-connected secondary windings and guarantees, at the same time, equal secondary-side voltages in power supplies with multiple isolated outputs.

- **Chapter 4** demonstrates a wide-input-voltage-range, 370 V-430 V-to-12 V, 3 kW DC/DC series-resonant converter that validates the control method and transformer design discussed in Chapter 2 and Chapter 3. The converter achieves 350 W/in^3 (21.4 kW/dm^3) power density and 94 % peak efficiency while operating from 300 V to 430 V input voltage and from 10 % to full load. An improved design additionally utilizes the magnetizing inductance for boost operation and a performance comparison is finally explored for comparing the improved design with the presented hardware demonstrator and with conventional LLC converters.

- **Chapter 5** presents the conceptualization, design, modelling, fabrication, and characterization of a 1.5 kW, 12 V-output DC/DC converter for industrial power supplies that is required to operate across a wide 300 V–430 V input voltage range. The converter achieves close to 96 % peak efficiency with a power density of 337 W/in^3 (20.6 kW/dm^3), excellent matching to the derived loss models, and zero-voltage switching even down to zero load. The loss models are used to identify improvements to further boost efficiency, the most important of which is the minimization of delay times in synchronous rectification.

- **Chapter 6** demonstrates a 12 V-output, 300 V–430 V-input DC/DC power module that takes advantage of the the loss models and effi-

ciency analysis developed in Chapter 5 to improve efficiency at all load levels. This 1.5 kW hardware prototype eliminates nearly 25 % of converter losses for a peak efficiency of nearly 97 % with a power density of 308 W/in^3 (18.8 kW/dm^3). Two 1.5 kW modules are then paralleled to achieve 3 kW output power at 12 V and 345 W/in^3 (21.1 kW/dm^3) with ideal current sharing between the secondary outputs and no drop in efficiency from a single module.

- **Chapter 7** concludes the thesis and briefly summarizes the main contributions and key findings. In addition, an outlook on possible future research is provided.

2

Topology & Control for Compact and Efficient DC/DC Power Supply Modules

Chapter Abstract

Proper topology and control-scheme selection is crucial for designing high-performance converters. In this chapter, a suitable topology for an isolated, wide-voltage-range-input, high-current-output DC/DC converter is conceptualized. First, state-of-the-art topologies are analysed and compared. Three candidates are considered for the application: the full-bridge converter, the dual-active-bridge converter, and the LLC converter. Because of its soft-switching properties, low-harmonic currents and synchronous rectification, the LLC converter with center-tap rectifier and matrix transformer is chosen as the most promising topology to fulfil the high-demanding requirements. The remainder of the chapter analyses alternative control strategies to overcome the issue of controllability in LLC converters, making them suitable for wide-input-voltage-range applications while still efficient. Two main techniques are described as key to extend the LLC converter gain range and keep high efficiency: a proper selection of the resonant inductor, and the synergetic control of frequency and phase-shift.

2.1 Introduction

A key power conversion stage in a broad range of emerging applications is a kW-scale, high-step-down-ratio DC/DC converter with a 12 V output. In electric vehicles, for example, this stage converts the high-voltage battery output, which typically varies between 250 V and 450 V, to 12 V for chassis

electronics [50]. In data centers, the output of a mains-connected PFC rectifier is converted to supply the 12 V distribution bus, with nominal input voltage near 400 V and fault operation required down to 300 V [51]. Similar specifications are also required in industrial automated manufacturing [52]. These diverse applications feature common demands for this 12 V DC/DC converter: exceptional power density, high efficiency and a wide-input-voltage range, beside other key specifications (see Tab. 1.1).

Previous approaches to meet the given requirements are limited by the tradeoff between high efficiency and wide-input-voltage range: LLC-based, soft-switched designs achieve high efficiency within a narrow input-voltage range [30–35] while buck-based topologies are lossy but can achieve the required range [26–29]. A design that combines the best features of both approaches is, however, mandatory in order to comply with the design specifications of Tab. 1.1, where we require high efficiency despite the large full-power output current and a tightly-regulated output voltage throughout the wide-input-voltage range.

2.2 Topology Selection

The topology challenges are driven by the combination of wide-input-voltage range (needed for hold-up time requirements) and high performance, as discussed in Section 1.2. We seek a low-complexity topology and control scheme, which eliminates approaches such as (i) DCX transformers, which require pre-regulation to fix the input voltage to the DC/DC module [21], (ii) additional hold-up time extensions circuits, which require a full additional converter module [22], and (iii) reverse-feeding for hold-up time, which adds significant control complexity to the DC/DC module [23]. Instead, the aim is to use a topology that can be controlled—with minimal complexity—across a wide gain range, and that maintains soft-switching throughout the full load and voltage ranges.

2.2.1 Topology Options

The full-bridge DC/DC converter with phase-shift control (see Fig. 2.1) [33, 39, 41–43, 53–63] is an isolated topology typically selected in applications where controllability throughout wide-voltage ranges is required. This converter consists of a full-bridge arrangement of power semiconductors that switches with high frequency and phase-shift modulation (between the bridge legs), imposing a square-voltage waveform across the primary side of the trans-

former that can have its duty cycle adjusted. The resulting AC-voltage on the transformer's secondary side is rectified and applied to an output LC network that filters the modulated waveform and builds up the output DC voltage. The main advantages of this topology are full transformer usage with positive and negative excitation, output-current-control capability through the output inductor, fixed-frequency operation for optimal component design, and wide-range controllability with phase-shift modulation. These advantages come with the cost of multiple elements in the high-output-current path (particularly the output inductor), square current waveforms with high harmonic content (see Appendix B), and hard-switching. Alternatively, the secondary-side diode bridge could be replaced by the current-doubler topology of Fig. 2.2(a) [64], leading to lower semiconductor count and splitting the high output current into two inductors (for lower conductions losses).

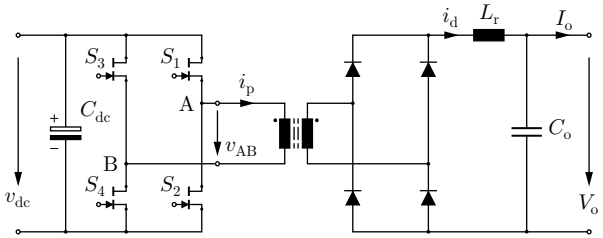

Fig. 2.1: Phase-shifted-full-bridge (PSFB) DC/DC converter with galvanic isolation and passive secondary-side rectification. A phase shift between the two bridge legs controls the energy transfer in this topology.

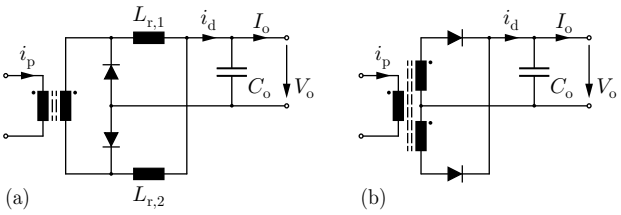

Fig. 2.2: Current-doubler (a) and center-tap (b) circuits as alternative output switching stages to, respectively, the full-bridge and the LLC topologies.

Another potential topology is the dual-active-bridge (DAB) converter (see Fig. 2.3) [27, 28, 65–74], which achieves higher efficiencies in high-output-current applications as the inductor is placed on the high-voltage side (where currents are smaller and less conduction losses are expected), and zero-voltage switching (ZVS) is achieved in all semiconductors for at least part of the operating range. It also offers fixed-frequency operation and tight output-voltage regulation throughout a wide-input-voltage range, with phase-shift control between the active bridges. As a topological disadvantage, the devices' turn-off happens typically with high currents, resulting in larger switching losses when compared to topologies with both zero-voltage and zero-current switching (ZVS and ZCS). Furthermore, the triangular shape of the currents contains harmonics that, though not as large as in the full-bridge topology (see Appendix B), lead to conduction losses—specially in the transformer windings, where losses are frequency-dependent. Due to the two active bridges, a more elaborated gating with signal isolators is also required, adding complexity to the overall system.

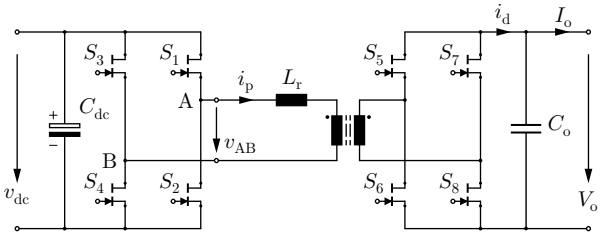

Fig. 2.3: Dual-active-bridge (DAB) converter with galvanic isolation. This converter is typically controlled by applying a phase-shift between the two active bridges.

As a third option, LLC topologies (see Fig. 2.4) [30–33, 75–83] are capable of converting energy with very low harmonic content (cf. Appendix B) and ZVS throughout the full load range. Moreover, due to the sinusoidal shape of the currents, secondary-side semiconductors switch with ZCS and primary-side devices with very low currents (just the minimum for ZVS), making this topology the most efficient choice for high-output-current applications. Further improvements in efficiency and simplicity can be achieved by replacing the diode-bridge rectifier stage with the center-tap circuit of Fig. 2.2(b) [84] for a lower semiconductor count and lower conduction losses. The main drawback of LLC converters, however, lies in their control method. To keep the desired sinewave shape for ZCS and low-harmonic currents, the energy

transfer is controlled by means of frequency modulation, which makes the topology inefficient for wide-voltage-range applications.

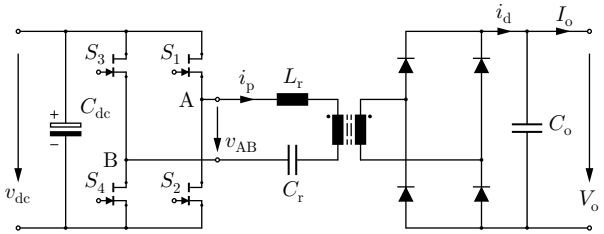

Fig. 2.4: LLC resonant converter with galvanic isolation and passive secondary-side rectification. The energy transfer in this converter is controlled by frequency modulation of the primary-side full-bridge.

As discussed in Section 1.2, and recalled in Section 2.1, the challenge is to combine the controllability of buck-based converters, which enables a wide-input-voltage range, with the high efficiency of LLC-based resonant topologies, that feature low-harmonic currents and soft-switching (ZVS and ZCS) across the full load and voltage ranges. As a first step toward this goal, we seek to derive a topology that is LLC-based and can handle high output currents, benefiting from the soft-switching properties and low-harmonic currents of LLC converters. Next, alternative control approaches that can handle wide-input-voltage ranges are proposed, culminating in the derivation of an efficient LLC-based topology with wide-voltage-range controllability.

2.2.2 Conceptualization

A key component of next-generation DC/DC power supply modules is the PCB-integrated transformer, which must handle high output currents while still being compact and efficient. With the winding-geometry parameters of a generic PCB transformer shown in Fig. 2.5(a), the current density in the secondary winding can be calculated (cf. Appendix C) as:

$$J_{pk} = \frac{\pi N_s I_o}{2A_w}, \tag{2.1}$$

while the flux density in the core is:

$$B_{pk} = \frac{V_o}{4N_s f_s A_c}. \tag{2.2}$$

According to Ohm's law and Steinmetz's equation [85], these two parameters can be directly related to winding ($P_{v,w}$) and core ($P_{v,c}$) volumetric losses:

$$P_{v,w} = \frac{J_{pk}^2}{2\sigma} \tag{2.3}$$

$$P_{v,c} = k_c f_s^{\alpha} B_{pk}^{\beta}, \tag{2.4}$$

showing that winding and core losses are proportional to J_{pk}^2 and B_{pk}^2 [1], respectively. It becomes clear from the equations that a high-current, low-voltage output will potentially lead to higher winding losses against core losses. Adding the requirement of PCB integration, with low winding cross-sectional areas (A_w), makes the design of such a transformer very challenging. The formulas also reveal that the secondary-winding number of turns (N_s) is a key parameter that can be tweaked to rebalance core and winding losses for an optimized overall transformer loss. But with the challenging requirements of this design ($V_o = 12\,V$, $I_o = 250\,A$), N_s must be reduced to the strict minimum of a single turn ($N_s = 1$), not yet being optimal.

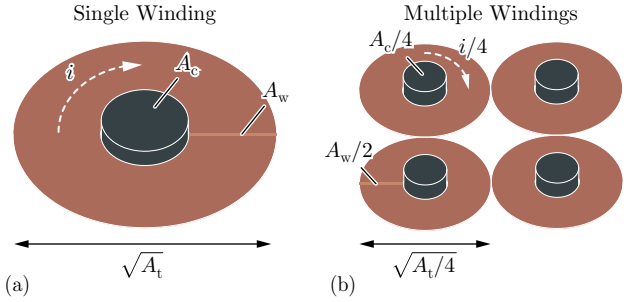

Fig. 2.5: (a) Illustrative scheme of a PCB-integrated, single-turn secondary-side winding with A_w window area, A_c core cross-section area, A_t total footprint area, and current i. (b) Winding-loss minimization at the expense of increased core loss by means of a multi-output (matrix) structure with paralleled windings that reduces the current density for the shown arrangement by a factor of 2 for a fixed total footprint area A_t and fixed current i.

To further improve the balance of core and winding losses, the high output current is divided among multiple windings and rectifiers, with in-

[1] Assuming a typical $\beta = 2$ for core materials in this application.

spiration drawn from matrix transformers used in state-of-the-art LLC designs [30–32]. As shown in Fig. 2.6, the utilization of four identical sub-transformers ($T_1 - T_4$)—with primary windings connected in series and single-turn secondary windings connected in parallel—allows to split the output current among four secondary stages and to have only one primary-side connection to the high-voltage switching stage. The optimal number of sub-transformers is selected to balance the copper and core losses. We eliminate the choices with an odd number of secondary windings, which would yield an asymmetrical structure, a complex core shape, or unnecessarily-higher core losses. 1 or 2 sub-transformers does not sufficiently reduce copper losses, while 8 sub-transformers would yield a complicated core structure with potentially higher core losses. Therefore, for the particular constraints of this design—and especially around PCB integration, which limits the available copper thickness—a proper copper-to-core loss ratio is achieved with 4 sub-transformers, as validated later with experimental results. This multi-output, matrix structure with 4 paralleled outputs reduces the copper loss by a factor of 4 over a single output with the same footprint area (A_t), as the current density reduces by a factor of 2 (see Fig. 2.5(b)). Ultimately, the optimal A_w-to-A_c ratio between winding window area and core cross-sectional area must be selected based on a Pareto-optimization from copper and core loss models, which is developed and detailed later in this thesis.

For the remainder elements of the topology in Fig. 2.6, a center-tapped rectifying stage is selected for the secondary side, a circuit that features a low semiconductor count, zero-voltage and zero-current switching, and no high-current output inductor. Attached to each single-turn secondary winding, synchronous rectifiers with power MOSFETs ($S_{5x} - S_{6x}$, $x = [a, b, c, d]$) and close-connected output capacitors (C_o) are chosen to avoid diode voltage drops, reduce commutation loops and minimize termination losses. Since the transformer secondary windings are directly connected to C_o (voltage source characteristic), the series-connected primary windings must be excited by a current source, whose waveform should be sinusoidal in order to minimize losses from harmonics (see Appendix B). These sinusoidal currents are generated by a resonant-tank network, which is excited with a rectangular voltage from the primary-side full-bridge ($S_1 - S_4$). GaN devices are chosen for the realization of $S_1 - S_4$, with excellent specific R_{on} and low switching losses and/or zero reverse-recovery losses [36, 37]. Relative to the half-bridge topology, the full-bridge has half of the primary-side current for a given power (with a tank excitation of $\pm v_{dc}$, rather than $\pm \frac{1}{2} v_{dc}$ for the half-bridge), and an additional control variable in the phase-shift between the two bridge legs,

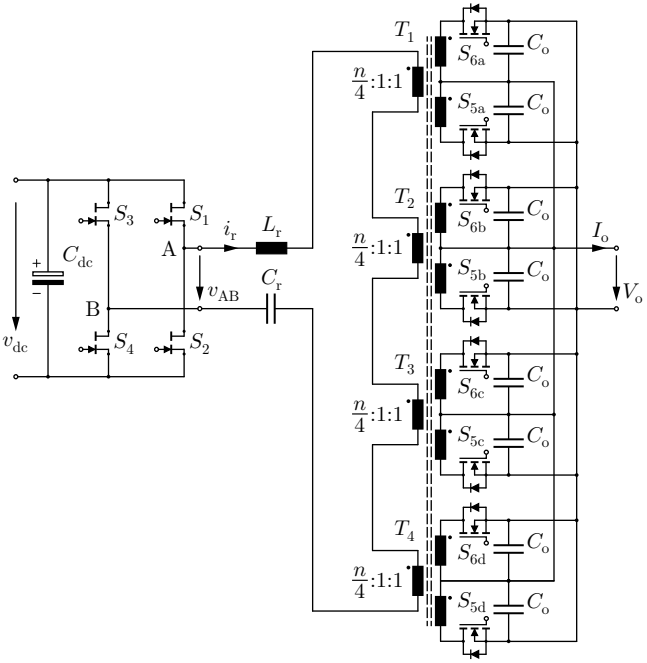

Fig. 2.6: Power circuit of the proposed DC/DC converter featuring GaN devices for the primary-side full-bridge, power MOSFETs operating as synchronous rectifiers on the secondary-side, and a series-input, paralleled-output, center-tapped matrix transformer.

during which a variable-length voltage of 0 V can be applied to the tank. This added flexibility of two available control variables (frequency and phase-shift) will be leverage to extend the gain range of the converter without increasing largely the switching frequency as in state-of-the-art solutions.

2.3 Improving the Controllability of LLC Resonant Converters

As mentioned earlier in this chapter, the challenge of LLC converters for wide-input-voltage ranges lies in their control method. Hence, some alternatives to extend their gain range will be analysed in this section, in particular (i) the

use of an external-to-the-transformer resonant inductor (L_r), with higher inductance than in state-of-the-art designs, and (ii) the synergetic control of both full-bridge's frequency and phase-shift.

2.3.1 Gain Analysis

Before moving to the investigation of alternative control schemes, this subsection briefly discusses the derivation of the topology gain. Knowing the gain characteristic of a converter is essential for designing the control method, as it describes the output-to-input voltage ratio ($\frac{V_o}{v_{dc}}$) as a function of the control variable. In state-of-the-art LLC converters, the control variable that allows gain changing is the switching frequency (f_s) of the primary-side switching stage. This comes directly from the gain characteristic of such converters, as frequency modulates how much energy the resonant tank can deliver.

For the selected topology of Fig. 2.6, the simplified circuit of Fig. 2.7 is derived. Here, the full-bridge was replaced by a sinusoidal voltage source with the fundamental frequency of v_{AB}, and the output stage was replaced by a resistance (R_p). This is only possible by means of the fundamental-harmonic-approximation (FHA) [86], an extensively-used tool in LLC converter designs to simplify the gain analysis. The FHA essentially assumes that the resonant tank—which has a high quality factor (Q)—works as a band pass filter and is capable of rejecting all harmonics of the square-voltage excitation except the fundamental component (to which the tank is tuned), allowing a simplified frequency-domain analysis of the circuit. With this method applied to the circuit of Fig. 2.7, straightforward equations can be derived, and the gain (normalized by the transformer turns ratio, n) has a comprehensive analytical solution [84]:

$$\frac{nV_o}{v_{dc}} = \frac{(m-1)\left(\frac{f_s}{f_r}\right)^2}{\sqrt{\left[m\left(\frac{f_s}{f_r}\right)^2 - 1\right]^2 + Q^2(m-1)^2\left(\frac{f_s}{f_r}\right)^2\left[\left(\frac{f_s}{f_r}\right)^2 - 1\right]^2}} \tag{2.5}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.6}$$

$$m = 1 + \frac{L_m}{L_r} \tag{2.7}$$

$$Q = \frac{Z_r}{R_p} \tag{2.8}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{2.9}$$

$$R_p = \frac{8n^2}{\pi^2}\frac{V_o^2}{P_o}. \tag{2.10}$$

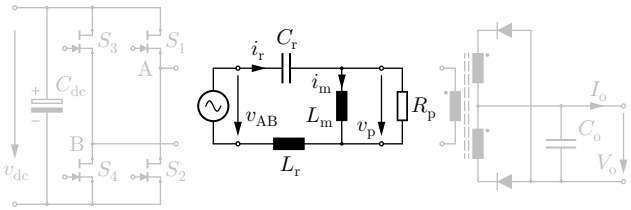

Fig. 2.7: Simplified version of the selected topology of Fig. 2.6, using the fundamental-harmonic-approximation (FHA) to capture the fundamental component of switched waveforms.

Each parameter in the gain equation relates to a particular design constraint: the transformer turns ratio, n, defines the operation mode for the converter (buck, boost, or both), L_m restricts the maximum gain, L_r defines the selectivity of the tank [87] (cf. Section 2.3.2) and therefore the required switching frequency range for a given gain, and C_r is used to tune the desired resonant frequency. Each of these parameters, though, also has constraints on its selected value: n must be a multiple of the number of output stages (sub-transformers) for symmetry, L_r must be optimized for low volume, C_r must have a withstand voltage that is achievable with commercially-available capacitors, and L_m should be large to minimize the magnetizing current and the associated conduction losses.

A generic example of this gain curve is shown in Fig. 2.8, where the big deficiency of the FHA is highlighted. Although FHA provides a straightforward method for calculating the gain, the accuracy drops when the switching frequency moves away from the resonant frequency, as the current/voltage waveforms become more nonsinusoidal. The calculation of the exact solution, on the other hand, is very exhaustive, and requires an extensive LLC-mode

analysis and the solving of several differential equations by numerical methods [88, 89]. Ultimately, both approaches shall be used: the FHA for a first, quick and worst-case design of the tank parameters, and the calculation of the exact solution (preferably by circuit simulation) for analyzing the practical gain behaviour.

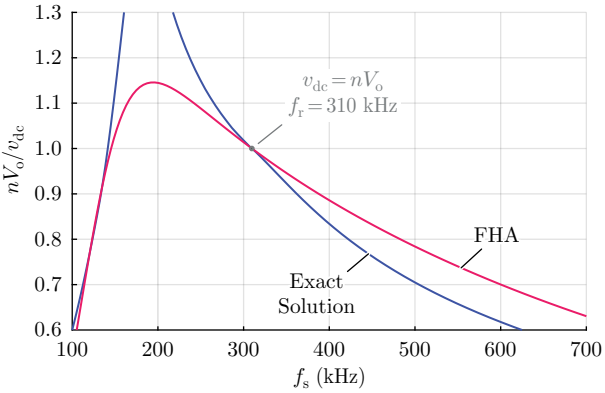

Fig. 2.8: Graphical description of a generic output-to-input conversion ratio (normalized by the transformer turns ratio n) as a function of the switching frequency (control variable). The exact solution, obtained through circuit simulation, is compared to the fundamental-harmonic-approximation (FHA), where we see that the the FHA captures the correct monotonic behavior of the gain function, though not exactly. Parameters: $n = 32$, $L_r = 24\,\mu H$, $C_r = 11\,nF$, $L_m = 110\,\mu H$, $f_r = 310\,kHz$, $R_p = 80\,\Omega$.

2.3.2 Resonant-Inductor Selection

The selection of the resonant tank parameters is critical in designing LLC converters, specially the design of the series resonant elements L_r and C_r, which define the tank's resonant frequency (f_r) and characteristic impedance (Z_r) according to (2.6) and (2.9). These two parameters, together with R_p and L_m, determine the tank's input impedance (Z_{in}), which is the impedance seen from the full-bridge switching stage that regulates the power flow. Fig. 2.9(a) shows a typical plot of Z_{in} relative to the switching frequency (here with high L_m for simplicity). For a particular load condition (fixed R_p), the characteristic impedance (Z_r) defines the shape of Z_{in}: the higher the Z_r, the higher the quality factor (see (2.8)), and the more selective the tank becomes. From (2.6)

and (2.9), one can write that:

$$Z_r = 2\pi f_r L_r, \tag{2.11}$$

revealing that, for a given resonant frequency, L_r is the parameter to adjust when a higher selectivity is desired (see Fig. 2.9(b)). A resonant tank with high selectivity (or more narrow passband) is capable of letting the fundamental component pass while rejecting other harmonics, but it also allows to increase rapidly the input impedance with small switching-frequency changes. Thus, by having a design with large L_r, the resonant-tank impedance can be widely adjusted with a narrow f_s range.

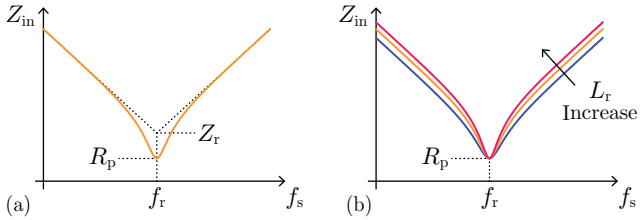

Fig. 2.9: (a) Resonant-tank input impedance as a function of the full-bridge switching frequency. (b) Impact of L_r in the selectivity of the tank: higher L_r values yield higher attenuation of current harmonics.

The input impedance (Z_{in}) depends on the resonant-tank parameters and so does the converter's gain ($\frac{nV_o}{v_{dc}}$). Fig. 2.10 illustrates typical LLC gain-curves and the impact of parameter sweeping on their shape (now including L_m). Fig. 2.10(a) shows that larger L_r values contribute to narrowing the switching-frequency operating range for the same targeted gain range, which results in lower switching losses and higher controllability at the cost of a larger inductor volume and a smaller peak gain. To correct for the peak gain, one can adjust the magnetizing inductance (L_m) until the desired maximum gain is achieved, as shows Fig. 2.10(b). Therefore, by combining these two parameters (L_r and L_m), the gain bandwidth can be narrowed (with higher L_r), and, at the same time, the maximum desired gain can be achieved (with lower L_m), as shows Fig. 2.10(c). Despite the drawback of increased component volume and larger magnetizing currents, the use of a larger resonant inductance (L_r) is a first, essential step toward higher controllability of LLC converters, as this choice avoids increasing the switching frequency excessively when dealing with wide-input-voltage ranges.

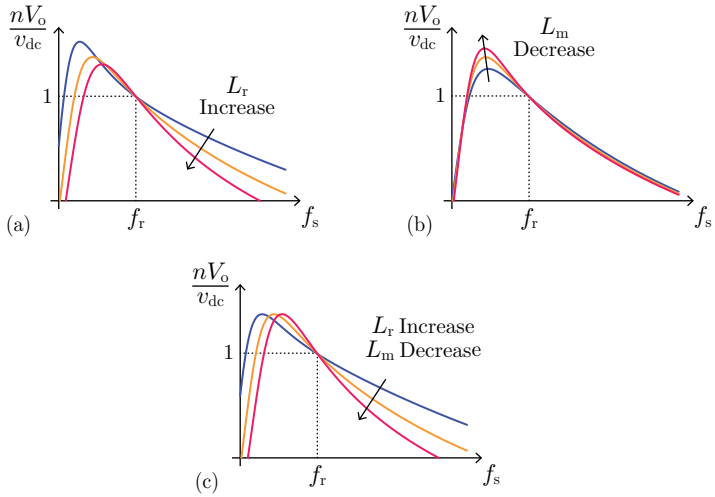

Fig. 2.10: Gain curves of three LLC designs generated by sweeping (a) the resonant inductance (L_r) only, (b) the magnetizing inductance (L_m) only, and (c) both together when aiming for the same peak gain. C_r was adjusted in each case according to (2.6) for keeping f_r constant. By selecting large L_r values, the converter's gain can be widely adjusted with a narrow f_s range.

2.3.3 Frequency/Phase-Shift Synergetic Control

Increasing the resonant-inductance value is not always a suitable option to improve controllability of LLC resonant converters, specially when the typically-low leakage inductance of PCB-integrated transformers is the only available resource. In such designs, with low L_r, the switching frequency must be significantly increased to keep the output voltage regulated across the wide-input-voltage range, yielding higher switching and frequency-related conduction losses. This becomes particularly critical for light load operation, as showcases the generic gain plot of Fig. 2.11, where f_s must be increased by *one order of magnitude* before a significant gain change is achieved.

As a promising alternative solution, the additional phase-shift control—enabled by a full-bridge switching stage—helps extending the LLC converter gain range beyond what is possible with frequency modulation only, widening the voltage controllability of such converters even for low-L_r designs. This section will therefore investigate alternative ways of modulating the resonant current using the synergy between frequency and phase-shift control, aiming

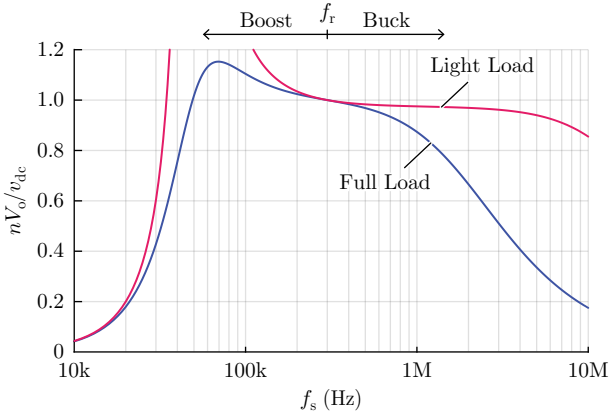

Fig. 2.11: Generic gain plot of a low-L_r LLC design at full- and light-load conditions. At light load, the switching frequency must be increased by at least one order of magnitude before the gain finally starts to drop. Parameters: $n = 24$, $L_r = 4\,\mu H$, $C_r = 70\,nF$, $L_m = 150\,\mu H$, $f_r = 300\,kHz$, $R_{p,full} = 44.8\,\Omega$, $R_{p,light} = 448\,\Omega$.

to extend the converter's gain without having to increase f_s by orders of magnitude.

Resonant-Current Modulation

As already mentioned, state-of-the-art LLC designs utilize frequency modulation to control the current that flows through the resonant tank. For the circuit of Fig. 2.12(a)—with neglected magnetizing inductance for a first, simplified analysis—typical waveforms are shown in Fig. 2.12(b). The full-bridge voltage v_{AB}, with 50 % duty-cycle and frequency control, excites the tank from the left-hand side, while the transformer-primary-side voltage v_p clamps the tank's right-hand side to $\pm nV_o$. The result is a second-order oscillation of i_r and v_r, which is described by the circuit differential equations:

$$v_{AB} - v_p = v_r + L_r C_r \frac{d^2 v_r}{dt^2} \tag{2.12}$$

$$i_r = C_r \frac{dv_r}{dt}, \tag{2.13}$$

and their time-domain solution:

$$\begin{aligned} v_{\mathrm{r}}(t_{\mathrm{i}}) =& -\left[v_{\mathrm{AB}} - v_{\mathrm{p}} - v_{\mathrm{r}}(t_{\mathrm{i\text{-}1}})\right]\cos\left[2\pi f_{\mathrm{r}}(t_{\mathrm{i}} - t_{\mathrm{i\text{-}1}})\right] + \\ &+ i_{\mathrm{r}}(t_{\mathrm{i\text{-}1}})\sin\left[2\pi f_{\mathrm{r}}(t_{\mathrm{i}} - t_{\mathrm{i\text{-}1}})\right]Z_{\mathrm{r}} + v_{\mathrm{AB}} - v_{\mathrm{p}} \\ i_{\mathrm{r}}(t_{\mathrm{i}}) =& \frac{v_{\mathrm{AB}} - v_{\mathrm{p}} - v_{\mathrm{r}}(t_{\mathrm{i\text{-}1}})}{Z_{\mathrm{r}}}\sin\left[2\pi f_{\mathrm{r}}(t_{\mathrm{i}} - t_{\mathrm{i\text{-}1}})\right] + \\ &+ i_{\mathrm{r}}(t_{\mathrm{i\text{-}1}})\cos\left[2\pi f_{\mathrm{r}}(t_{\mathrm{i}} - t_{\mathrm{i\text{-}1}})\right]. \end{aligned} \tag{2.14}$$

Solving these equations for each switching state ($t_{\mathrm{i}} - t_{\mathrm{i\text{-}1}}$ with $i = 1, 2, 3, 4$) allows to reconstruct i_{r} and v_{r} for a full switching period. For the particular case of Fig. 2.12(b), the resonant current (i_{r}) evolves continually with either positive or negative values, but never stays at zero, indicating that the converter operates in continuous conduction mode (CCM). Under this operating mode, f_{s} is the only variable to be adjusted for shaping i_{r}, as all other quantities in (2.14) are fixed by design. The flexibility comes, however, when a phase-shift (ϕ) between the full-bridge legs is introduced, which allows controlling the duty-cycle:

$$d = \frac{\phi}{2\pi} \tag{2.15}$$

of v_{AB}—and thus the shape of i_{r}—without necessarily adjusting f_{s}. Two new operation modes are enabled by this type of control, shown together with CCM in Fig. 2.13. Discontinuous conduction mode (DCM) takes place when the duty-cycle of v_{AB} is reduced to the point where i_{r} reaches zero and stays at zero (see Fig. 2.13(d)), as it cannot go negative due to the blocking of the output-rectifier diodes. With DCM, a maximum switching frequency can be established while the output voltage is still fully regulated, solving the problem of indefinitely increasing f_{s} for bucking the output voltage (see Fig. 2.13(a)). The second mode is the operation at the boundary of CCM and DCM (see Fig. 2.13(c)), for which both v_{AB}'s frequency and duty-cycle are adjusted simultaneously to keep the operation under what is called boundary conduction mode (BCM).

The boundary and continuous conduction modes differ essentially on the shape of the tank excitation voltage v_{AB} (cf. Fig. 2.13(b-c)). BCM controls the full-bridge such that v_{AB} assumes 0 V for a certain time before i_{r} crosses zero, allowing the combination of frequency and phase-shift modulations. CCM, however, generates only positive and negative v_{dc}, limiting the output regulation to frequency control. The additional 0 V interval allows BCM to have a larger conversion-ratio range for the same switching frequency

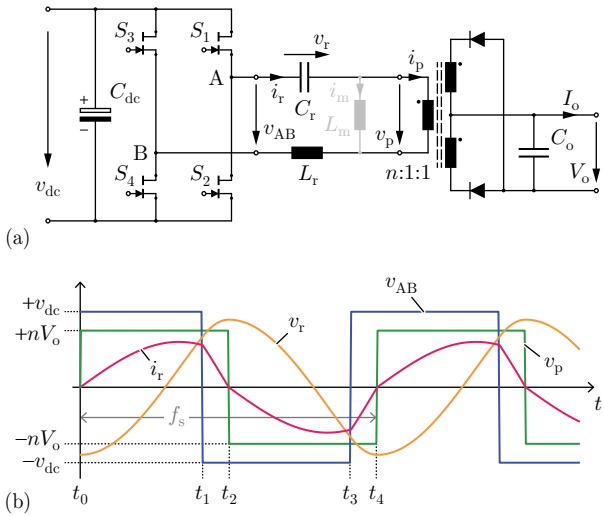

Fig. 2.12: (a) Simplified resonant-converter circuit and (b) typical waveforms.

relative to CCM, as now the resonant gain depends also on the duty cycle d of v_{AB}. If d equals 0.5 ($\phi = \pi$), v_{AB} assumes a square shape and CCM operation takes place. Both modes have, by definition, the same gain near the resonant frequency f_r, which is also the highest achievable gain in this case. To reach lower gains, both BCM and CCM have to increase the switching frequency. In BCM, however, the same gain can be achieved by switching at a lower frequency, as reveals Fig. 2.13(a). BCM control therefore extends the allowable input voltage range relative to CCM and benefits from lower switching losses and conduction losses in frequency-related resistances. As a disadvantage, BCM requires a zero-current-detector circuit that increases the system's complexity. Ultimately, the choice between CCM or BCM has to be made for each system in particular, trading off switching losses and circuit complexity.

Analysis Including the Magnetizing Inductance

In applications where the converter operates mostly with v_{dc} far from $V_{dc,min}$, as in Fig. 1.2(b), having a high L_m might not be the optimal choice. By setting the lowest input voltage at the resonant frequency (gain of 1 in Fig. 2.13(a)), the converter can only operate in buck mode. As resonant converters are most effi-

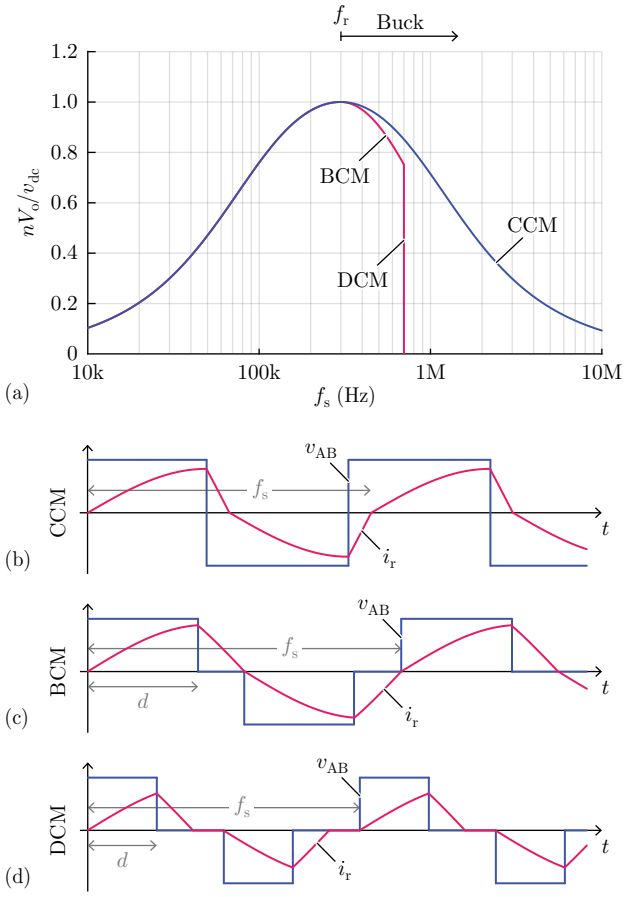

Fig. 2.13: Series-resonant-converter gain (a) and respective waveforms (b-d) for the three analysed modulation schemes: (b) continuous (CCM), (c) boundary (BCM), and (d) discontinuous (DCM) conduction modes. Parameters: $n = 24$, $L_r = 8\,\mu H$, $C_r = 35\,nF$, $L_m = \infty$, $f_r = 300\,kHz$, $R_p = 44.8\,\Omega$.

cient switching at the resonant frequency, the buck-only operation maximizes efficiency at the minimum v_{dc}, which occurs only during the infrequent fault operation. In the nominal operating range tough, the switching frequency is relatively high and DCM—where one of the half-bridges is hard-switched—is used extensively, potentially resulting in steep efficiency degradation at light loads. Therefore, for this particular application, a design would have higher efficiency if f_s was closer to the L_r-C_r resonant frequency (f_r) in the nominal v_{dc} range; that is, if the gain of 1 operating point ($\frac{nV_o}{v_{dc}} = 1$) was selected nearer the nominal range. Fault operation would then operate in a boost mode, which requires a proper L_m selection and CCM.

The introduction of L_m as a design parameter alters the nature of the resonant tank, which becomes a third-order oscillator. The new circuit (LLC converter) is shown in Fig. 2.14(a) together with typical waveforms in Fig. 2.14(b) for operation with $f_s > f_r$. For this modified circuit, the set of differential equations that describes the resonant-tank oscillation must be extended to also accommodate the magnetizing current (i_m) as a state variable:

$$v_{AB} - v_p = v_r + L_r C_r \frac{d^2 v_r}{dt^2} \tag{2.16}$$

$$i_r = C_r \frac{dv_r}{dt} \tag{2.17}$$

$$v_p = L_m \frac{di_m}{dt}, \tag{2.18}$$

which extends the time-domain solution into a new form as well:

$$\begin{aligned} v_r(t_i) =& -\left[v_{AB} - v_p - v_r(t_{i\text{-}1})\right] \cos\left[2\pi f_r (t_i - t_{i\text{-}1})\right] + \\ &+ i_r(t_{i\text{-}1}) \sin\left[2\pi f_r (t_i - t_{i\text{-}1})\right] Z_r + v_{AB} - v_p \\ i_r(t_i) =& \frac{v_{AB} - v_p - v_r(t_{i\text{-}1})}{Z_r} \sin\left[2\pi f_r (t_i - t_{i\text{-}1})\right] + \\ &+ i_r(t_{i\text{-}1}) \cos\left[2\pi f_r (t_i - t_{i\text{-}1})\right] \\ i_m(t_i) =& \frac{v_p (t_i - t_{i\text{-}1})}{L_m} + i_m(t_{i\text{-}1}). \end{aligned} \tag{2.19}$$

The introduction of L_m as a design parameter does not significantly change the operation above f_r, as the converter still behaves as a series-resonant converter with i_r and v_r largely decoupled from i_m. This conveniently allows to operate the converter in either CCM, BCM or DCM for $f_s > f_r$. For the desired boost mode, however, where the converter operates with $f_s < f_r$, the shape of the resonant waveforms change considerably, as shows Fig. 2.15. The

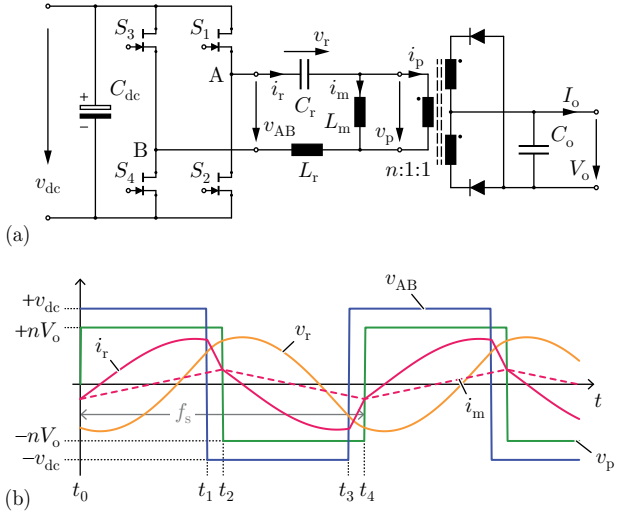

Fig. 2.14: (a) Simplified LLC converter circuit and (b) typical waveforms for operation above the resonant frequency ($f_s > f_r$).

converter still operates in CCM from the primary-side point of view, as i_r never stays at zero after crossing the x-axis, but the secondary-side currents become discontinuous after i_r hits i_m due to the blocking of the output-rectifier diodes. At this point, with $i_r = i_m$ and $i_p = 0$, $L_r + L_m$ resonates with C_r and "Open"-mode (or O-mode) takes place, during which v_p does not have a defined value ($\pm nV_o$) but is the result of the resonance between $L_r + L_m$ and C_r. The converter equations (2.16)-(2.18) have no longer a closed-form solution in this mode, as the boundary conditions yield a transcendental equation—with i_m partially linear and partially sinusoidal within a half switching period (see Fig. 2.15)—that relies on numerical methods to be solved [88]. Despite the difficulty of having an analytical solution with O-mode, which is circumvented by circuit simulation, a close look at Fig. 2.15 reveals that O-mode is the key for boost operation, as C_r stores energy during this mode and transfers energy to L_r in the subsequent mode ("positive"-mode, or P-mode) and thus to the output, resulting in a boost-like operation with $v_{dc} < nV_o$. In boost mode, the gain is increased by lowering f_s, but this comes with the cost of extending O-mode against P-mode, which increases circulating currents for the same output power and reduces efficiency. That is also why BCM and DCM are not

used for boost operation, as they would further extend O-mode unnecessarily. Instead, CCM control is selected as the only reasonable option for boost operation.

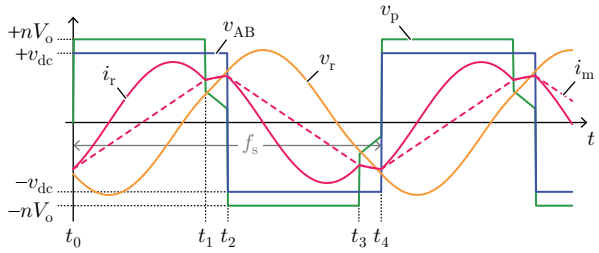

Fig. 2.15: Typical LLC converter waveforms for operation below the resonant frequency ($f_s < f_r$).

Fig. 2.16 shows the gain-curve and mode-waveforms for the proposed control scheme: a combination of CCM, BCM and DCM modes and a design with finite magnetizing inductance that allows boost and buck operation for the ultimate goal of setting the nominal operating range close to the efficient gain-of-1 point. All the control methods introduced and qualitatively discussed is this section will be further explored and validated with experimental measurements in the chapters to come.

2.4 Summary

This chapter revisited state-of-the-art topologies suitable for an isolated, wide-voltage-range-input, high-current-output DC/DC converter that has to fulfil high-demanding performance specifications. Three principal topologies were analysed as promising candidates: the full-bridge converter, the dual-active-bridge converter, and the LLC converter. After contrasting advantages and drawbacks of each individual topology, the LLC resonant converter with center-tap synchronous rectifier and matrix transformer was selected as the most suitable one for the application at hand. However, as LLC converters are most efficient as fixed-ratio converters, alternative control schemes have been proposed to extend the gain-range of the selected topology, which will be demonstrated experimentally in the chapters to come.

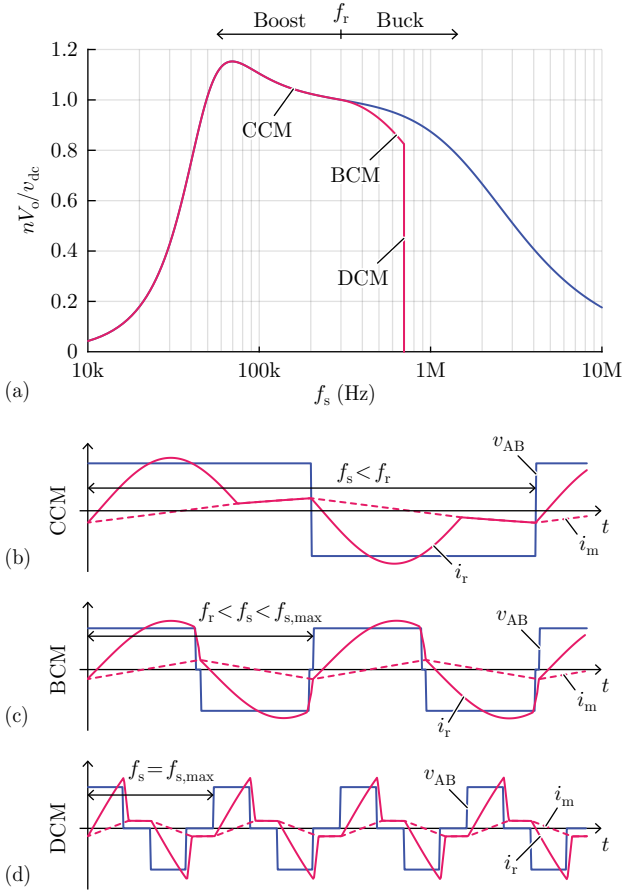

Fig. 2.16: LLC converter gain (a) and respective waveforms (b-d) for the three analysed modulation schemes: (b) continuous (CCM), (c) boundary (BCM), and (d) discontinuous (DCM) conduction modes. Parameters: $n = 24$, $L_r = 4\,\mu H$, $C_r = 70\,nF$, $L_m = 150\,\mu H$, $f_r = 300\,kHz$, $f_{s,max} = 700\,kHz$, $R_p = 44.8\,\Omega$

3
”Snake-Core” Transformer

Chapter Abstract

An improved PCB-winding matrix transformer is introduced in this chapter, which provides a single path for the magnetic flux to flow within the core and therefore ensures an even flux linkage of the parallel-connected secondary windings. This so-called ”snake-core” matrix transformer avoids the emergence of circulating currents among the secondary windings and, at the same time, guarantees equal secondary-side voltages in power supplies with multiple isolated outputs. The design of the snake-core transformer is analysed in detail and validated by finite-element-method simulations and experimental measurements. Moreover, a comprehensive mathematical analysis of circulating currents in matrix transformers explains their origin and proves the effectiveness of the snake core in mitigating such parasitics. Thus, the design of the primary windings in PCB-winding matrix transformers is significantly simplified as a perfect symmetry among these windings is no longer required.

3.1 Introduction

As electricity consumption grows rapidly worldwide in various electrification fields—most notably in data centers and server systems due to the high data volume being processed in the cloud during the last years [90]—power supply systems with high efficiency, high power density and low realization costs are in demand. Despite recent efforts on changing the common 12 V data-center bus architecture to 48 V, or to even 400 V, and to integrate the final voltage regulator module (VRM) in the CPU motherboards [19], the majority of solutions still relies on two-stage 180 V-270 V AC input to 12 V DC output power conversion with power densities up to 70 $\mathrm{W/in^3}$ [12]. For next-generation PSUs, an increase in power density to at least 100 $\mathrm{W/in^3}$ is

demanded while still being able to handle the typically wide-input-voltage range and the large output currents of such converter systems (see Section 1.1 for further details). Therefore, the DC/DC converter stage of next-generation power supplies should comply with the exemplary set of specifications given in Tab. 1.1.

Although numerous galvanic-isolated DC/DC converter concepts for data centers have been proposed in literature [25, 30, 91, 92], the most promising approaches take advantage of winding-integrated PCB magnetics and resonant converter topologies, achieving exceptional performances in terms of power density and efficiency in particular designs [32]. By series connecting the transformer's primary windings and parallel connecting the corresponding secondary windings, i.e., by employing a so-called matrix transformer (cf. Fig. 3.1, recalling Fig. 2.6), the large output current can be distributed among several secondary windings and a larger characteristic impedance $Z_c = V_o/I_o$ per winding results. Less sensitivity to the stray inductance of the current path and lower overvoltages across the synchronous rectifiers are therefore achieved [93], allowing the selection of semiconductors with lower breakdown voltages and better R_{on} properties. However, in state-of-the-art PCB-winding matrix transformers, the sub-transformers T_1–T_4 (see Fig. 3.1) are magnetically connected in parallel, whereby multiple paths for the magnetic flux are provided, potentially resulting in asymmetric flux distribution among core limbs. Thus, from an unbalanced flux distribution, different voltages are induced in each secondary winding, leading to undesired inter-winding circulating currents and increased conduction losses.

In order to design an efficient PCB-integrated transformer and to overcome the circulating currents issue, we introduce in this chapter the "snake-core" transformer [94], a PCB-integrated matrix transformer whose core ensures equal magnetic-flux linkages in all windings and therefore equal induced voltages in parallel-connected secondary windings. A detailed mathematical analysis of both this transformer concept and the prior art is provided, which explains why circulating currents emerge in conventional matrix transformers, but not in the snake-core transformer. Experimental results finally validate the proposed magnetic-core concept and its benefits.

3.2 Transformer Concept and Analysis

Section 2.2.2 introduced the selected topology for the next-generation DC/DC power module, which includes a multiple-output transformer structure with 4 sub-transformers to overcome the challenge of high output currents. In this

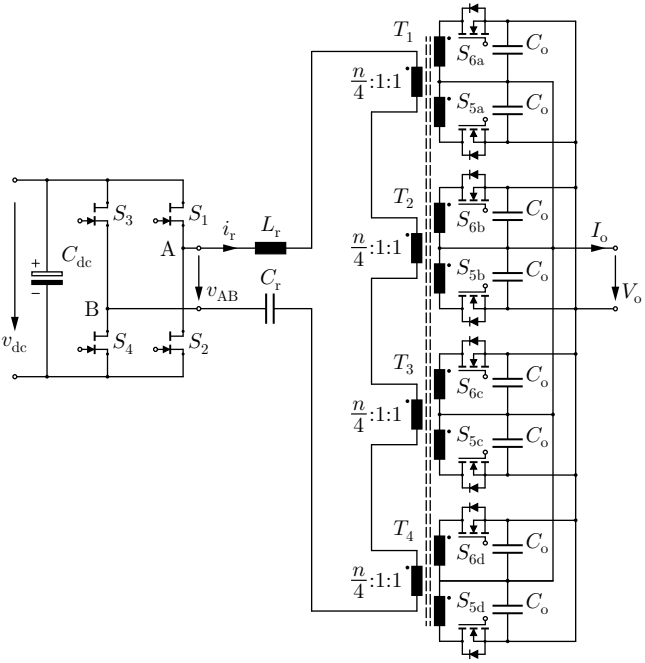

Fig. 3.1: Power circuit of the proposed DC/DC converter featuring GaN devices for the primary-side full-bridge, power MOSFETs operating as synchronous rectifiers on the secondary-side, and a series-input, paralleled-output, center-tapped matrix transformer.

section, we walk through the design and analysis of this PCB-integrated transformer and propose a single-path magnetic connection of the sub-transformers with the snake core.

3.2.1 Transformer Implementation

The proposed transformer is implemented in a 4-layer PCB, where the middle layers are assigned to the series-connected primary turns and the top and bottom layers to the parallel-connected secondary windings. In order to minimize the termination losses and to increase the power density of the converter, the switches of the synchronous rectifiers (S_{5x}, S_{6x}) and the output capacitors (C_o) are directly integrated onto the secondary windings, as

schematically depicted in Fig. 3.2. The coplanar arrangement of the primary- and secondary-side currents theoretically cancels the vertical magnetic field components within the windings and leads to low AC-to-DC resistance ratios. Even for high switching frequencies, a current distribution close to the DC current density is achieved. The PCB copper thickness should be chosen smaller than the skin depth:

$$\delta = \frac{1}{\sqrt{\pi f_s \sigma_{Cu} \mu_{Cu}}}, \tag{3.1}$$

calculated for the maximum switching frequency (f_s) that the system operates, in order to avoid skin effects due to horizontal magnetic field components. σ_{Cu} is the copper conductivity and μ_{Cu} is the copper permeability.

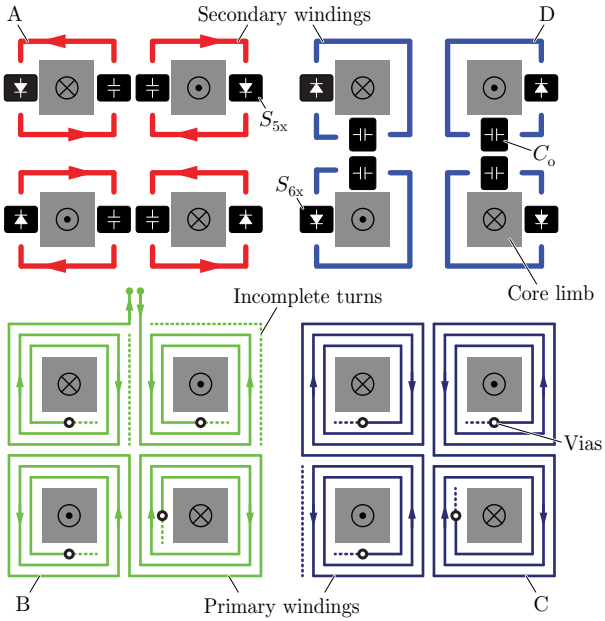

Fig. 3.2: Schematics of the proposed 4-layer PCB-winding matrix transformer with the middle layers (B,C) dedicated to the series-connected primary windings and the top (A) and bottom (D) layers implementing the parallel-connected secondary windings. The switches (S_{5x} – S_{6x}) as well as the output capacitors (C_o) are directly integrated into the windings to improve power density and reduce commutation loops.

In state-of-the-art, PCB-integrated matrix transformers, the required close magnetic coupling of the primary and the secondary windings is usually achieved using core geometries similar to Fig. 3.3(a), where two ferrite plates (core yokes) are placed above and underneath the PCB windings in order to magnetically connect the (four) core limbs. Assuming open circuits in all secondary windings and a symmetric core geometry, the structure can be represented by the reluctance model of Fig. 3.3(b). $N_{px} i_p$ (x = [1, 2, 3, 4]) refers to the generated magnetomotive force (MMF) of the primary windings, ϕ_x to the magnetic flux flowing in each core limb, and $\mathcal{R}_1 - \mathcal{R}_3$ to the reluctances of the magnetic paths given the symmetry of the core. If $N_{p1} = N_{p2} = N_{p3} = N_{p4}$, the symmetry of the transformer yields the same flux linkage in each core limb, whereby identical voltages are induced in each secondary winding. However, due to PCB routing limitations, some turns of the primary windings might be incomplete, as for instance indicated by the dashed lines in Fig. 3.2, creating discrepancies between the MMFs generated in the limbs and therefore inducing different voltages in the secondary windings.

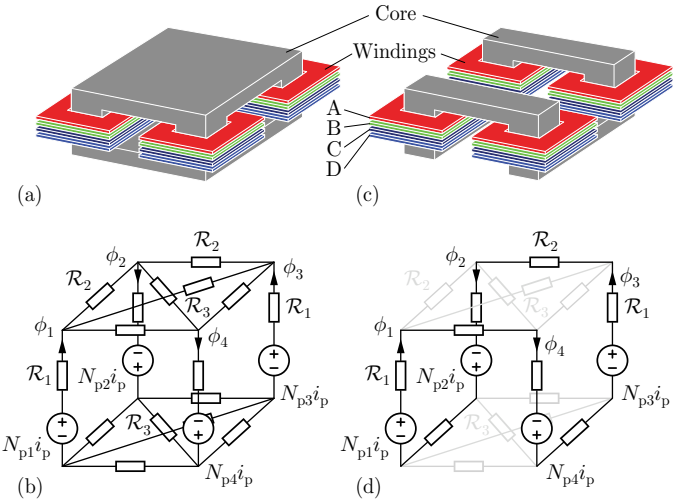

Fig. 3.3: (a) State-of-the-art core arrangement whose magnetic circuit (b) shows the possibility of unequal flux distribution across the corners of the cube, causing undesired circulating currents within the secondary windings due to unequal induced voltages. (c) Proposed snake-core arrangement to avoid flux splitting and therefore circulating currents; only one path for the magnetic flux is provided, as highlighted in the equivalent magnetic circuit (d). Labels A,B,C,D are referenced from Fig. 3.2.

In order to better understand the statement, a winding arrangement according to $N_{p1} > N_{p2} = N_{p4} > N_{p3}$ is assumed. In this particular case, the MMF generated within limbs 2 and 4 are equal (same current and same number of turns) and the reluctance model of Fig. 3.3(b) can be replaced by the circuit shown in Fig. 3.4(a), where the limbs with the same MMF are connected in parallel and the diagonal yoke reluctances are neglected for the sake of simplicity. The circuit can be further simplified to the one shown in Fig. 3.4(b), where it can be seen that $\phi_1 > \phi_3$ applies. Basically, the fluxes can be equated as $\phi_1 > \phi_2 = \phi_4 > \phi_3$ and therefore different voltages are induced in the secondary windings N_{s1} and N_{s3} (single turns), according to $v_{sx} = -\mathrm{d}\phi_x/\mathrm{d}t$. As all secondary windings are effectively connected in parallel, the different induced voltages create circulating currents among the windings (cf. Fig. 3.4(c)), which potentially affect the transformer conduction losses.

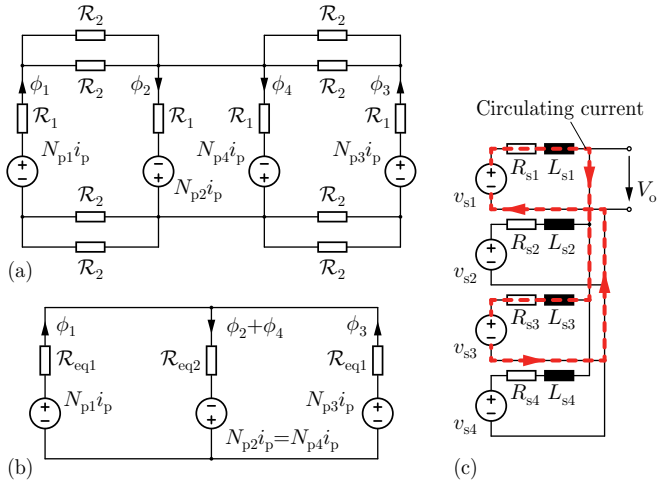

Fig. 3.4: (a) Equivalent and (b) simplified circuits of the reluctance model of Fig. 3.3(b) for $N_{p2} = N_{p4}$. (c) Example of a circulating current generated between the parallel-connected secondary windings of the transformer due to different induced voltages in the corresponding windings. For the sake of simplicity, the rectifier diodes present in the actual secondary-side circuits are omitted.

Aiming to overcome the aforementioned issue, a new core design named as ”snake core” is proposed, where the top and the bottom core-yokes are divided into two pieces in such a way that the four sub-transformers $T_1 - T_4$ are magnetically-connected in series, whereby only one path for the magnetic

flux is provided (cf. Fig. 3.3(c)). The equivalent reluctance model is shown in Fig. 3.3(d) and is similar to the magnetic circuit of Fig. 3.3(b), however unequal flux splitting in the circuit nodes is now impossible as only a single magnetic path is provided. Hence, $\phi_1 = \phi_2 = \phi_3 = \phi_4$ always applies, leading to equal induced voltages in all secondary windings and therefore no circulating currents. The snake-core transformer also benefits power supplies with several individual isolated outputs, as each secondary winding inherently experiences the same flux linkage, yielding identical output voltages.

The snake-core matrix transformer should be designed based on the specifications of the next-generation DC/DC power module summarized in Tab. 1.1. The idea behind the design is to optimize the copper-core loss balance for a given transformer volume. Copper loss is considered to be the winding DC-resistance loss corrected by the R_{ac}/R_{dc} frequency dependency, which could be even neglected in a rough calculation, as the excellent coupling in PCB winding transformers significantly minimizes skin and proximity effects. Core loss is computed by solving the General Steinmetz Equation. The minimum loss value is then selected by changing the core-limb area (A_c) while keeping the whole transformer area (A_t) constant, thus inversely changing the winding cross-sectional area (A_w)—see Fig. 2.5 for reference. The loss modelling follows well-known equations from the literature [85, 95] and will be further detailed in Chapter 5 accompanied with loss measurements. For now, we will limit the analysis to a general electromagnetic characterization of the snake-core transformer by means of finite-element methods and a mathematical operation analysis.

3.2.2 Finite-Element-Method (FEM) Simulations

The operation of the proposed transformer was validated by FEM simulations that were performed using the geometry of Fig. 3.5(a). Two basic simplifications were done intending to facilitate the design of the simulation model, i.e., concentric copper rings are utilized for representing the primary turns, and only Secondary 1 is assumed to carry current (zero current in the Secondary 2, as given for a half switching cycle in regular operation). The first approach, the concentric-rings approach, does not precisely model the spiral primary winding shape, but still gives a satisfying approximation of the conduction losses and field interactions. The second approach, where we set zero current in the Secondary 2 and force full sinusoidal current in the Secondary 1, avoids modelling the currents in their inconvenient rectified shape and allows a simplified frequency-domain FEM simulation.

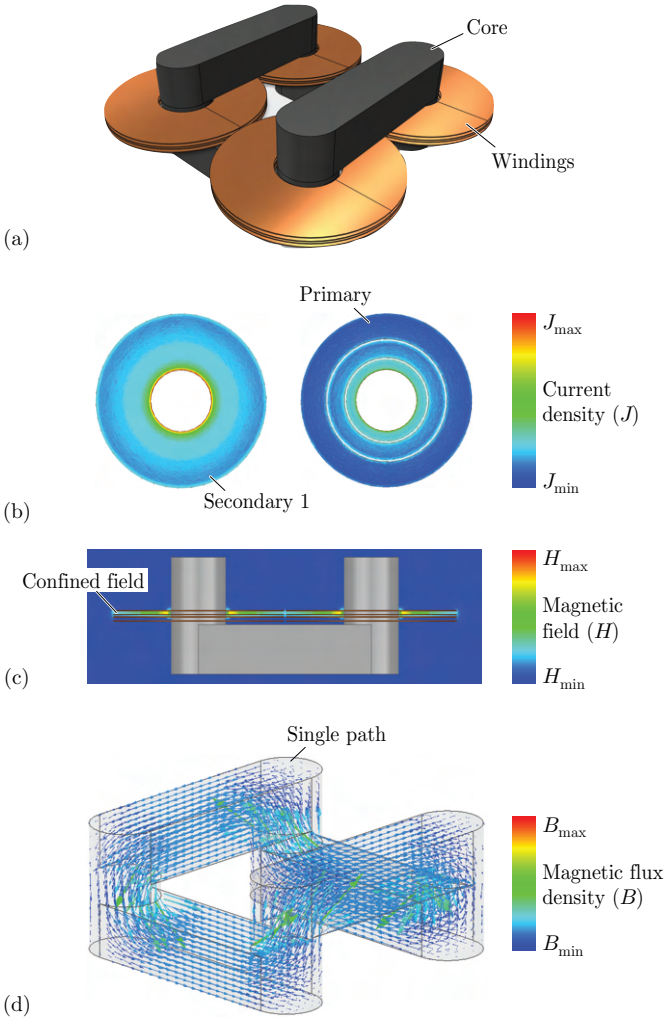

Fig. 3.5: (a) FEM-simulated transformer geometry with sinusoidal-current excitation. (b) Current density (J) in the series connected primary windings and in one of the secondary windings (Secondary 1). (c) Magnetic field (H) in the vicinity of the windings. (d) Magnetic flux density (B) confined within the core. For simplifying the simulation without loosing generality, the primary windings were considered as concentric rings and the secondary-side current flows within Secondary 1 only.

Fig. 3.5(b) shows that the vertical components of the magnetic field (H) generated by the primary and secondary windings cancel each other due to the coplanar winding arrangement. Consequently, no eddy currents are induced along the windings and a current distribution close to the DC current density is achieved in all windings. The benefits of the coplanar arrangement can also be seen in how H is distributed within the windings' vicinity, i.e., the field is almost completely confined in between the PCB layers (see Fig. 3.5(c)), which also reduces radiated electromagnetic interference. The circular shape of the turns is particularly chosen for avoiding sharp corners of the current path, which would increase the conduction losses due to the increased current densities around these corners. The benefit of the snake-core arrangement can be seen in Fig. 3.5(d), where the high-permeability core confines all magnetic-flux-density (B) lines and provides one single path for the flux to flow and penetrate the windings, which fundamentally imposes equal voltage induction in all windings (assuming equal numbers of turns).

A second FEM simulation was performed to analyse alternative winding stackups and qualitatively compare losses. Fig. 3.6(a) shows the reference design with 2 layers dedicated for the primary winding ("HV1" and "HV2") and another 2 layers for the center-taped secondary windings ("LV1" and "LV2"). An alternative layer stackup with 6 instead of 4 PCB layers is proposed in Fig. 3.6(b), where two additional LV layers are added in parallel to the former ones to increase the secondary-winding available copper. This approach reduces the copper losses by 7 %, but requires additional through-hole vias for paralleling the LV layers that end up reducing the primary-winding available copper. To further improve the layout, we distribute the vias along the outer border of the windings where less primary current flows. This arrangement is shown in Fig. 3.6(c), which dissipates 3 % less losses for a total 10 % loss reduction in from the 4-layer stackup. Finally, Fig. 3.6(d) showcases that an 8-layer PCB-winding design, with 2 HV layers and 6 interleaved LV layers, further improves losses by only 3 %. It becomes evident from the simulations that the marginal reduction in winding losses does not pay off the substantial complexity increase of approaches (b-d), based on which we choose the 4-layer structure (a) as the appropriate winding design for the snake-core transformer, and straightforwardly reduce losses on secondary windings by increasing the top and bottom layers' thickness with copper foils in later implementations.

To conclude the transformer analysis, we further investigate the capability of the snake-core transformer in mitigating circulating currents and compare it with the state-of-the-art core. Thus, a detailed mathematical model of the circulating currents issue is introduced in the next sub-section, leading to a

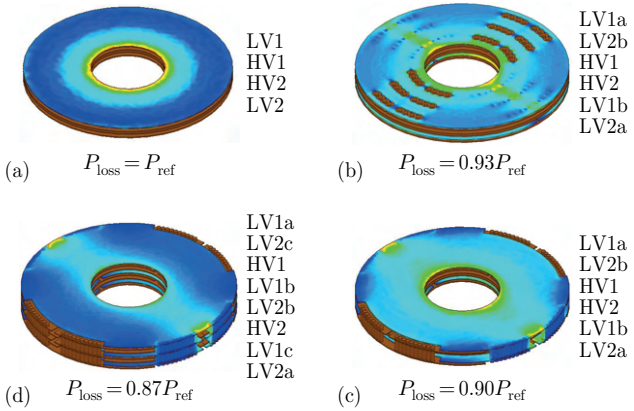

Fig. 3.6: FEM-simulated transformer windings—primary (”HV”) and secondary (”LV”)—in four potential implementations: (a) 4-layer PCB, (b) 6-layer PCB with vias at the middle of the winding, (c) 6-layer PCB with vias at the borders, and (d) 8-layer PCB with vias at the borders. Copper losses are compared with reference to the 4-layer design of (a).

deeper understanding of how such currents originate and to which design parameters are they dependent.

3.2.3 Circulating-Currents Analysis

To confirm the statement that circulating currents emerge among the parallel connected secondary windings of the state-of-the-art matrix transformer, we analyse the reluctance model of Fig. 3.3(b) considering secondary windings as well. The cube shape of the reluctance model is however simplified into the circuit shown in Fig. 3.7, in which the yoke reluctances are neglected and only the limb reluctances are considered. This simplification reduces the complexity of the analysis and corresponds to an insertion of air gaps in the transformer limbs—a common practice in resonant converters where a comparably small magnetizing inductance is required to support ZVS. The simplified circuit also allows to investigate the impact of air-gap insertion on the magnitude of circulating currents.

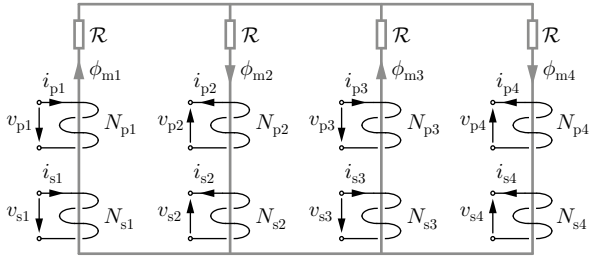

Fig. 3.7: Particular case of the general matrix-transformer reluctance model shown in Fig. 3.3(b) where air gaps are inserted in the core limbs to reduce the magnetizing inductance and support ZVS.

A solution for the circuit of Fig. 3.7 is derived in Section C.2 (Appendix C) and given by:

$$\begin{bmatrix} \mathbf{V_P} \\ \mathbf{V_S} \end{bmatrix} = \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} \mathbf{N_P}\left(\mathbf{\Phi}_{\sigma\mathbf{P}} + \mathbf{\Phi_m}\right) \\ \mathbf{N_S}\left(\mathbf{\Phi}_{\sigma\mathbf{S}} + \mathbf{\Phi_m}\right) \end{bmatrix}, \tag{3.2}$$

where:

$$\mathbf{V_P} = \begin{bmatrix} v_{p1} & v_{p2} & v_{p3} & v_{p4} \end{bmatrix}^{\mathrm{T}} \tag{3.3}$$

$$\mathbf{V_S} = \begin{bmatrix} v_{s1} & v_{s2} & v_{s3} & v_{s4} \end{bmatrix}^{\mathrm{T}} \tag{3.4}$$

are the windings' voltages,

$$\mathbf{N_P} = \begin{bmatrix} N_{p1} & 0 & 0 & 0 \\ 0 & N_{p2} & 0 & 0 \\ 0 & 0 & N_{p3} & 0 \\ 0 & 0 & 0 & N_{p4} \end{bmatrix} \tag{3.5}$$

$$\mathbf{N_S} = \begin{bmatrix} N_{s1} & 0 & 0 & 0 \\ 0 & N_{s2} & 0 & 0 \\ 0 & 0 & N_{s3} & 0 \\ 0 & 0 & 0 & N_{s4} \end{bmatrix} \tag{3.6}$$

are the windings' number of turns,

$$\mathbf{\Phi_m} = \begin{bmatrix} \phi_{m1} \\ \phi_{m2} \\ \phi_{m3} \\ \phi_{m4} \end{bmatrix} = \boldsymbol{\mathcal{P}}_\mathbf{m}\left(\mathbf{N_P I_P} + \mathbf{N_S I_S}\right) \tag{3.7}$$

is the flux distribution inside the magnetic core,

$$\boldsymbol{\mathcal{P}}_{\mathbf{m}} = \frac{1}{4\mathcal{R}} \begin{bmatrix} 3 & 1 & -1 & 1 \\ 1 & 3 & 1 & -1 \\ -1 & 1 & 3 & 1 \\ 1 & -1 & 1 & 3 \end{bmatrix} \tag{3.8}$$

is the magnetic permeance of the core,

$$\mathbf{I_P} = \begin{bmatrix} i_{\mathrm{p}1} & i_{\mathrm{p}2} & i_{\mathrm{p}3} & i_{\mathrm{p}4} \end{bmatrix}^{\mathrm{T}} \tag{3.9}$$

$$\mathbf{I_S} = \begin{bmatrix} i_{\mathrm{s}1} & i_{\mathrm{s}2} & i_{\mathrm{s}3} & i_{\mathrm{s}4} \end{bmatrix}^{\mathrm{T}} \tag{3.10}$$

are the windings' currents,

$$\boldsymbol{\Phi}_{\boldsymbol{\sigma}\mathbf{P}} = \mathbf{N}_{\mathbf{P}}^{-1} \mathbf{L}_{\boldsymbol{\sigma}\mathbf{P}} \mathbf{I_P} \tag{3.11}$$

$$\boldsymbol{\Phi}_{\boldsymbol{\sigma}\mathbf{S}} = \mathbf{N}_{\mathbf{S}}^{-1} \mathbf{L}_{\boldsymbol{\sigma}\mathbf{S}} \mathbf{I_S} \tag{3.12}$$

are the primary- and secondary-winding fluxes that leak the core, and

$$\mathbf{L}_{\boldsymbol{\sigma}\mathbf{P}} = \begin{bmatrix} L_{\sigma\mathrm{p}1} & 0 & 0 & 0 \\ 0 & L_{\sigma\mathrm{p}2} & 0 & 0 \\ 0 & 0 & L_{\sigma\mathrm{p}3} & 0 \\ 0 & 0 & 0 & L_{\sigma\mathrm{p}4} \end{bmatrix} \tag{3.13}$$

$$\tag{3.14}$$

and

$$\mathbf{L}_{\boldsymbol{\sigma}\mathbf{S}} = \begin{bmatrix} L_{\sigma\mathrm{s}1} & 0 & 0 & 0 \\ 0 & L_{\sigma\mathrm{s}2} & 0 & 0 \\ 0 & 0 & L_{\sigma\mathrm{s}3} & 0 \\ 0 & 0 & 0 & L_{\sigma\mathrm{s}4} \end{bmatrix}. \tag{3.15}$$

are the leakage inductances of each winding. These equations can be simplified by the application of boundary conditions, which reduce the general problem to a specific problem. The first set of boundary conditions account for the connection of the primary windings in series and the secondary windings in parallel, yielding:

$$v_{\mathrm{p}1} + v_{\mathrm{p}2} + v_{\mathrm{p}3} + v_{\mathrm{p}4} = v_{\mathrm{p}} \tag{3.16}$$

$$i_{\mathrm{p}1} = i_{\mathrm{p}2} = i_{\mathrm{p}3} = i_{\mathrm{p}4} = i_{\mathrm{p}} \tag{3.17}$$

$$v_{\mathrm{s}1} = v_{\mathrm{s}2} = v_{\mathrm{s}3} = v_{\mathrm{s}4} = v_{\mathrm{s}} \tag{3.18}$$

$$i_{\mathrm{s}1} + i_{\mathrm{s}2} + i_{\mathrm{s}3} + i_{\mathrm{s}4} = i_{\mathrm{s}}. \tag{3.19}$$

The second boundary condition is derived by inspecting Fig. 3.7, where it becomes clear that $\phi_{m1} - \phi_{m2} + \phi_{m3} - \phi_{m4} = 0$, allowing to write that:

$$i_{s1} - i_{s2} + i_{s3} - i_{s4} = 0 \tag{3.20}$$

if we assume equal secondary-side stray inductances (see Section C.2.3). These boundary conditions applied to the transformer equations ultimately lead to an expression for calculating the circulating currents among parallel-connected secondary windings in a zero-load condition:

$$\frac{\mathrm{d}i_{sx}}{\mathrm{d}t} = \frac{v_s - \frac{N_s N_{pex}}{\mathcal{R}} \frac{\mathrm{d}i_p}{\mathrm{d}t}}{L_{\sigma s} + \frac{N_s^2}{\mathcal{R}}}, \tag{3.21}$$

with $x = [1, 2, 3, 4]$.

In light of equation (3.21), circulating currents essentially result from the difference between the parallel output voltage (v_s) and the induced voltage in each secondary winding, which is calculated by multiplying the primary-side current with the correspondent mutual inductance ($M_x \frac{\mathrm{d}i_p}{\mathrm{d}t}$, with $M_x = \frac{N_s N_{pex}}{\mathcal{R}}$). If the primary windings do not contain asymmetries ($N_{pe1} = N_{pe2} = N_{pe3} = N_{pe4} = N_{pc}$, see Section C.2.3 for further details), no voltage difference will result and no circulating currents will flow. The magnitude of these currents is limited by the secondary-winding self inductance L_s, which corresponds to the sum of the winding leakage inductance $L_{\sigma s}$ and the magnetizing inductance L_{ms} seen from the secondary winding ($L_s = L_{\sigma s} + L_{ms}$, with $L_{ms} = \frac{N_s^2}{\mathcal{R}}$). Hence, the better the transformer coupling is, the more influence the core inductance on the circulating currents has. Due to the close coupling of the primary and secondary windings in PCB transformers, the leakage inductance is very small and the secondary self-inductance is considered to be the magnetizing inductance only. For high-μ cores (low-reluctance cores), the magnetizing inductance is high and the circulating currents are negligible. However, a transformer with air gaps faces a linear increase in the reluctance with respect to the air gap length. In LLC converters, for example, the magnetizing current supports the boost operation and air gaps in the transformer core are required. Typical values for the core reluctance in LLC transformers are 10 to 50 times the value of the core reluctance without air gap. This represents a reduction of 10 to 50 times in the core inductance and, therefore, an increase in the circulating currents by the same factor, making them no longer negligible.

Likewise, the matrix-transformer equations could be solved for the snake-core case (see Fig. 3.8), for which a different permeance matrix:

$$\boldsymbol{\mathcal{P}}_{\mathbf{m}} = \frac{1}{4\mathcal{R}} \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix} \tag{3.22}$$

and a different flux condition ($\phi_{\mathrm{m1}} = \phi_{\mathrm{m2}} = \phi_{\mathrm{m3}} = \phi_{\mathrm{m4}}$) must be considered (see Section C.2.3 for the complete analysis). The result with zero load is:

$$i_{\mathrm{s1}} = i_{\mathrm{s2}} = i_{\mathrm{s3}} = i_{\mathrm{s4}} = 0, \tag{3.23}$$

which shows that circulating currents for the snake-core matrix transformer are fundamentally equal to zero.

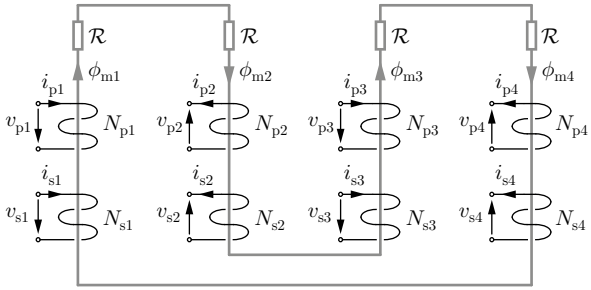

Fig. 3.8: The planar representation of the snake-core-transformer reluctance model of Fig. 3.3(d) with air gaps inserted in the limbs and/or in the yokes to reduce the magnetizing inductance and support ZVS.

3.3 Experimental Results

Though the snake-core transformer is validated as part of converter prototypes in the chapters to come, an intermediate hardware prototype was fabricated for the characterization of the snake-core transformer alone. This hardware prototype is shown in Fig. 3.9, with the designed primary- and secondary-winding layouts ($n = 24$) depicted in Fig. 3.9(a) including footprints for the secondary-side synchronous rectifiers and corresponding gate-drive circuits. The core was manufactured by machining off-the-shelf ferrite blocks and

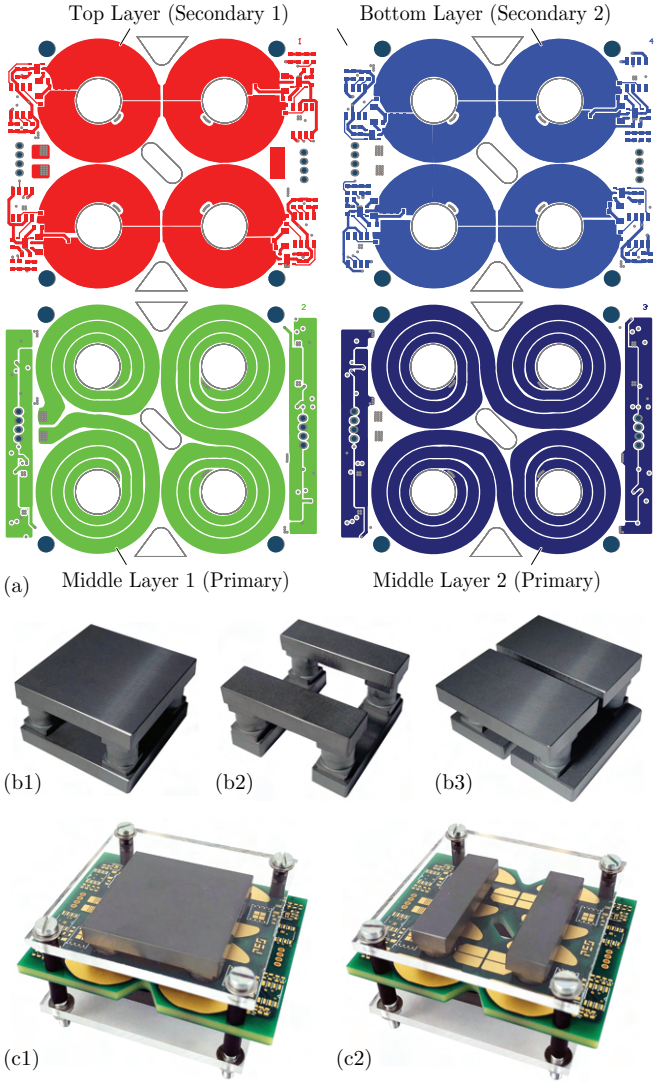

Fig. 3.9: (a) PCB design of the proposed transformer exhibiting the high- and low-voltage-windings implementation. The core can be arranged either in the state-of-the-art form (b1) or using the snake core (b2,b3), and the top and bottom yokes of the snake-core arrangement might be chosen larger (b3) in order to reduce core losses. (c) Final transformer assembling, measuring 65 mm x 51 mm x 24 mm.

plates using a linear precision saw with a diamond blade. Two magnetic core geometries were chosen for comparison purposes: the state-of-the-art core arrangement with top and bottom plates and four core limbs in between (see Fig. 3.9(b1)), and the proposed snake-core arrangement (see Fig. 3.9(b2)). The snake core can also be assembled in such a way that larger top and bottom plates are used and therefore lower core losses result (see Fig. 3.9(b3)). The fully assembled state-of-the-art and snake-core matrix-transformer designs are shown in Fig. 3.9(c1) and Fig. 3.9(c2), respectively.

An open-circuit test was conducted on both transformer designs to validate the assumption that equal induced voltages occur in each secondary winding if the snake core is used. By coupling the series-connected primary windings to a 300 V-peak/300 kHz sinusoidal-voltage supply, the open-circuit-secondary-winding voltages (v_{sx}, x = [1, 2, 3, 4]) can be measured for the state-of-the-art (conventional) core and the snake core. The test circuit is shown in Fig. 3.10(a), where a function generator excites a power amplifier that applies the desired voltage v_p to the primary winding. A capacitor C_2 is connected in parallel to the primary winding to resonate with the magnetizing inductance (L_m) and further amplify the current i_p that feeds the transformer. Additionally, the capacitor C_1 blocks DC currents and avoids transformer saturation.

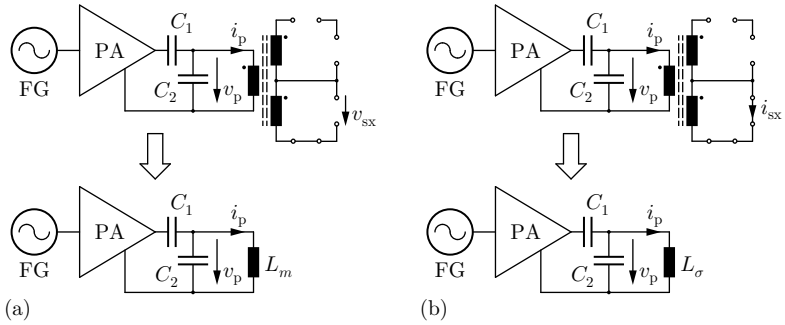

Fig. 3.10: (a) Open-circuit test whose setup utilizes a function generator (FG) to generate a 300 kHz sinusoidal voltage that is amplified by a power amplifier (PA) and applied to the series-connected primary windings of the transformer. The parallel capacitor (C_2) and the magnetizing inductance (L_m) form a resonator that amplifies the current i_p, while the series capacitor (C_1) blocks DC current and avoids saturation. (b) Transformer short-circuit test analogous to (a) tough with the leakage inductance (L_σ) resonating with C_2.

The results are shown in Fig. 3.11, in which $v_{p,conv}/v_{p,snake}$, $i_{p,conv}/i_{p,snake}$ and $v_{sx,conv}/v_{sx,snake}$ (x = [1, 2, 3, 4]) refer to the transformer primary voltage, primary current and secondary voltages of the conventional and the proposed cores, respectively. Despite the efforts in designing the PCB primary windings as symmetric as possible (see Fig. 3.9(a)), the measurements reveal that the turns are still not perfectly distributed around the core limbs, as different voltages are induced in each secondary winding for the state-of-the-art transformer. However, as expected, the proposed snake-core arrangement provides equal flux distribution among the secondary windings and the induced voltages are the same. This approach not only avoids the emergence of circulating currents among the parallel-connected secondary windings, but also provides a solution for equalizing the voltages in power supplies with several individual isolated outputs. Thus, regardless of a possible asymmetry in the distribution of the primary turns within the transformer, the snake core ensures identical induced voltages in the secondary windings, whereby not only higher efficiency results, but also the design of such PCB winding-integrated transformers is considerably simplified. The open-circuit test was also used to measure the core losses and compare them to the previously calculated and FEM-simulated results (see Tab. 3.1). The calculated values are revisited in Chapter 5, where the loss models are significantly improved and a satisfying accuracy is achieved.

Tab. 3.1: Snake-core-matrix-transformer performance based on calculated, FEM-simulated and measured results. The transformer measures 50 mm by 50 mm, with 51 mm^2 magnetic core cross-sectional area, N49 magnetic material and 105 mm PCB copper thickness. Parameters: P_o = 3 kW, V_o = 12 V, n = 24.5, $f_{s,min}$ = 300 kHz, $f_{s,max}$ = 700 kHz, T = 100 °C.

Performance	**Calc.**	**FEM**	**Meas.**
Total loss (P_{total})	37.7 W	40.7 W	43.4 W
Copper loss (P_{Cu})	34.8 W	39.2 W	41.6 W
Core loss (P_{Fe})	2.9 W	1.5 W	1.8 W

The short-circuit test was also applied to the snake-core transformer in order to assess the copper losses and its thermal performance. The test circuit is very similar to the one for open circuit (see Fig. 3.10(b)), though now the equivalent inductance that models the transformer is the total leakage inductance (L_σ). The results are summarized in Tab. 3.1 and compared to the estimated values based on loss models and Finite Element Method (FEM)

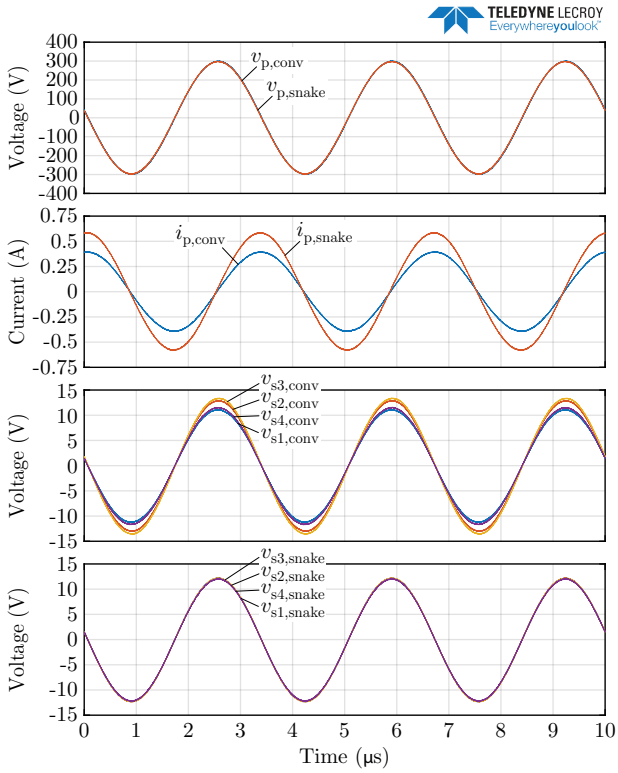

Fig. 3.11: Open-circuit test using the state-of-the-art (conventional) or the proposed snake-core approach. For the same primary voltage excitation ($v_{p,conv}/v_{p,snake}$), the conventional-core transformer (see Fig. 3.9(c1)) shows different induced voltages in the secondary windings ($v_{sx,conv}$, $x = [1, 2, 3, 4]$) caused by asymmetries in the primary-winding layout or different remaining airgaps in the magnetic circuit, while the proposed snake core (see Fig. 3.9(c2)) keeps the voltages equal ($v_{sx,snake}$). The magnetizing currents ($i_{p,conv}/i_{p,snake}$) of the cores are slightly different due to their different geometries and thus different magnetizing inductances.

simulations. The thermal time-constant of PCB winding transformers is small and a few seconds of short circuit measurement with the nominal input current is sufficient to heat up the windings' surface up to 100 ℃ (see Fig. 3.12). A good thermal management in such a design is therefore essential, and means for extracting heat out of the windings must be implemented, e.g., attaching aluminium heat sinks with an interface material to the PCB surfaces where the copper is intentionally exposed.

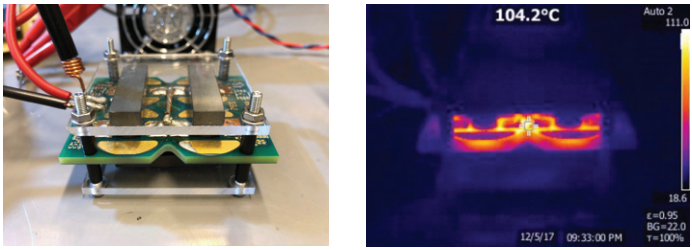

Fig. 3.12: Thermal analysis of the snake-core transformer assessing the source of heat for the correct positioning of the cooling system.

Lastly, the circulating currents for the state-of-the-art core with parallel-connected secondary windings were investigated considering an additional insertion of a 0.32 mm-length air gap in each core limb. Again, connecting the series-connected primary windings to a 300 V-peak/300 kHz sinusoidal-voltage, the parallel-connected-secondary-winding currents were measured and compared. The experiment was performed with the same primary-side excitation voltage ($v_{\mathrm{p,not}}/v_{\mathrm{p,gap}}$), which results in the same secondary-side induced voltage ($v_{\mathrm{s,not}}/v_{\mathrm{s,gap}}$). As shown in Fig. 3.13, the circulating currents with inserted air gap ($i_{\mathrm{sx,gap}}$, x = $[1, 2, 3, 4]$) are larger than in case of no air gap ($i_{\mathrm{sx,not}}$) and follow the increase of the magnetizing current (i_{p}), as expected according to (3.21). Considering now the peak value of the magnetizing current referred to each secondary-side winding $i_{\mathrm{msx}} = i_{\mathrm{mp}} \frac{n}{4} = 23.2$ A (cf. Fig. 3.1 with $n = 24$), the ratio between the magnetizing current and the circulating current for this particular transformer design is $i_{\mathrm{sx,gap}}/i_{\mathrm{ms}}$ =2.3 %. This value would be even higher in practice, since the current probe and the wire loops used for measuring the circulating currents add significant stray impedances, which reduce the real values that those currents can achieve. In case of a LLC converter where the magnetizing current might be as large as the load current in boost operation, the apparently small ratio of 2.3 % would represent a significant absolute value of circulating currents. It is also

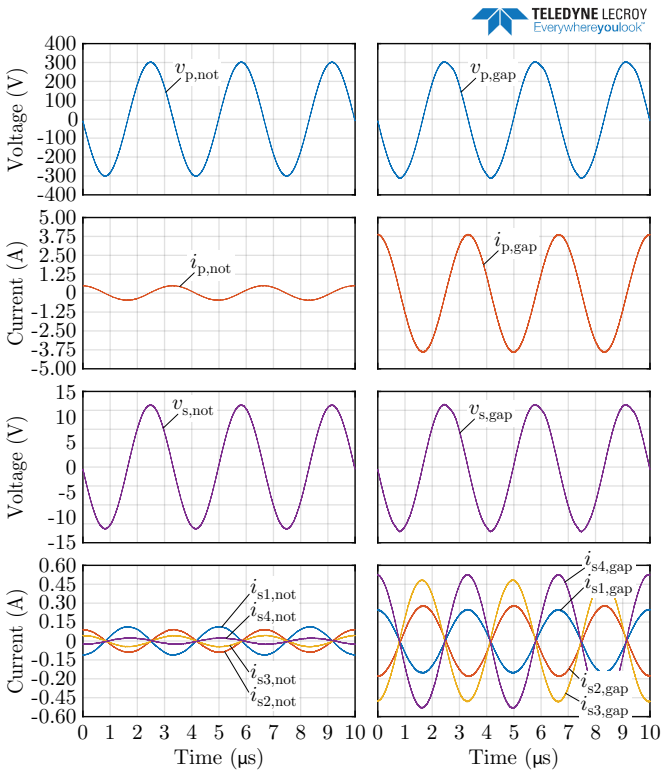

Fig. 3.13: Measurements of circulating currents for the state-of-the-art core (see Fig. 3.9(c1)) with the secondary windings connected in parallel. Two cases were analysed: with (”gap”) and without (”not”) the insertion of a 0.32 mm-length air gap in each core limb. For the same primary-voltage excitation ($v_{p,not}/v_{p,gap}$), both cases present the same secondary voltages ($v_{s,not}/v_{s,gap}$), but highly different magnetizing currents ($i_{p,not}/i_{p,gap}$) and circulating currents ($i_{sx,not}/i_{sx,gap}$, x = [1, 2, 3, 4]).

important to mention that the PCB layout was realized trying to achieve the highest possible symmetry among the sub-transformer primary windings and any further asymmetry would again increase the magnitude of these currents. Moreover, the circulating currents are independent of the converter load condition and can lead to significant efficiency reduction in partial load operation. Consequently, the proposed snake-core transformer represents a simple and cost-effective approach to ultimately eliminate circulating currents in matrix transformers.

3.4 Summary

A PCB-integrated transformer with a special core structure is introduced in this chapter as a promising solution to fulfil the high-demanding requirements of next-generation power supplies regarding efficiency, power density and cost. The proposed snake-core matrix transformer equally distributes the high output current in multiple secondary windings and yields low conduction losses as the coplanar arrangement of the primary and secondary windings minimizes their AC-to-DC resistance ratios. Moreover, the proposed snake core avoids the emergence of circulating currents between parallel-connected secondary windings regardless of possible asymmetries in the layout of the series-connected primary windings. The snake core therefore facilitates the overall design of PCB-winding matrix transformers, as perfect primary-winding symmetry isn't necessary, and represents a simple and cost-effective approach to ultimately eliminate circulating currents in matrix transformers.

4

LC Resonant Converter with Boundary/Discontinuous-Conduction-Mode Control

Chapter Abstract

This chapter demonstrates a wide-input-voltage-range, 370 V-430 V-to-12 V, 3 kW DC/DC series-resonant converter that validates the control method and transformer design discussed in previous chapters. The employed boundary/discontinuous-conduction-mode control scheme extends the input-voltage range over conventional LLC techniques, and the "snake-core" matrix transformer achieves ideal parallel-connected secondary voltage balance. The converter achieves 350 W/in^3 (21.4 kW/dm^3) power density and 94 % peak efficiency while operating from 300 V to 430 V input voltage and from 10 % to full load. An improved design additionally utilizes the magnetizing inductance for boost operation in order to optimize the operating conditions of the converter system and to increase the overall efficiency. A performance comparison is finally conducted for comparing the improved design with the presented hardware demonstrator and with conventional LLC converters.

4.1 Introduction

This chapter validates the control, magnetics, and topological schemes for a converter to support both wide-input-voltage and high-output-current requirements. Specifically, the series-resonant converter with boundary/discontinuous-conduction-mode control (B/DCM-LC) operates from 300 V-430 V and from zero to 250 A output current. The hardware prototype (see Fig. 4.1(a)) achieves a high power density of 350 W/in^3 and an efficiency

of 94 %, validating the control method and transformer design introduced in previous chapters. For the challenging design constraints of Tab. 1.1 though, with an efficiency target beyond 96 %, a circuit-level modification to improve efficiency is further explored and described in detail in this chapter.

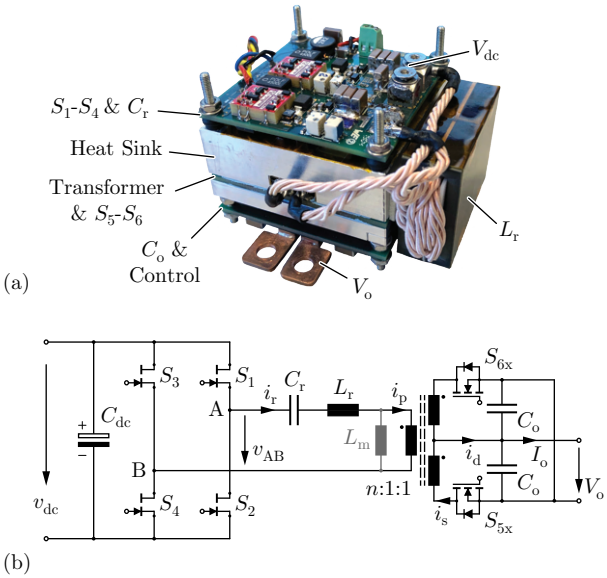

Fig. 4.1: (a) Implemented 3 kW hardware prototype of the B/DCM-LC converter measuring 66 mm by 51 mm by 41 mm (350 W/in^3). (b) Simplified power circuit (generalized single-secondary circuit shown) of the hardware prototype (see Fig. 2.6 for the complete topology), with the transformer implemented as snake-core matrix transformer (cf. Chapter 3) with 4 parallel-connected synchronous rectifier stages.

4.2 Hardware Prototype

4.2.1 Overview

The hardware prototype of Fig. 4.1 comprises a series-resonant converter with a full-bridge and a matrix transformer. The large output current (250 A) is split between four center-tapped, parallel-connected secondary windings, as introduced in Chapter 3, where a "snake-core" transformer (SCT) that

overcomes the problem of flux imbalance in paralleled secondary windings is demonstrated. The resonant-tank elements are designed following the guidelines of Section 2.3.1, with their values shown in Tab. 4.1. Unlike conventional LLC converters, the hardware prototype is operated as a step-down converter only, which is why the magnetizing current—and therefore the magnetizing inductance L_m of the SCT—is not used for the converter operation at all. Hence, L_m is chosen large, minimizing the circulating magnetizing current and the associated additional conduction losses.

Tab. 4.1: Key design parameters of the B/DCM-LC resonant converter.

Parameter	Value
n	24
L_r	8 µH
C_r	35 µF

The converter is operated with the boundary/discontinuous-conduction-mode control technique (B/DCM) introduced in Chapter 2 [94, 96]. At most load and input-voltage levels (see Fig. 4.2(a)), the converter is operated in boundary conduction mode (BCM), where the full-bridge switching frequency (f_s) is modulated based on required output power and the phase-shift between the bridge-legs (ϕ) is varied to operate exactly at the discontinuous (DCM) and continuous conduction mode (CCM) boundary. In BCM, the transformer current is nearly sinusoidal (see Fig. 4.2(b)), which reduces AC-related winding losses and peak currents, and the full-bridge and synchronous rectifier (SR) power switches operate under ZVS. At low output power, very high f_s would be required to maintain BCM, leading to high frequency-related losses in the magnetic components and gate-drives, whereby the converter is instead operated in DCM at a fixed, maximum f_s under phase-shift control (cf. Fig. 4.1(c)). In DCM, one half-bridge leg switches with ZVS while the other operates under zero-current-switching (ZCS) conditions. Relative to conventional CCM control techniques of LLC converters, the additional degree of freedom due to the variable duty cycle of v_AB extends the allowable input voltage range, achieves ZVS over a wide load range, and decreases the harmonic content of the currents in the circuit. Nevertheless, as pointed out in Chapter 2, it is important to verify if BCM has indeed advantages over CCM for the particular design at hand. Otherwise, additional measurement circuits required for BCM operation will add unnecessary volume and complexity to the system.

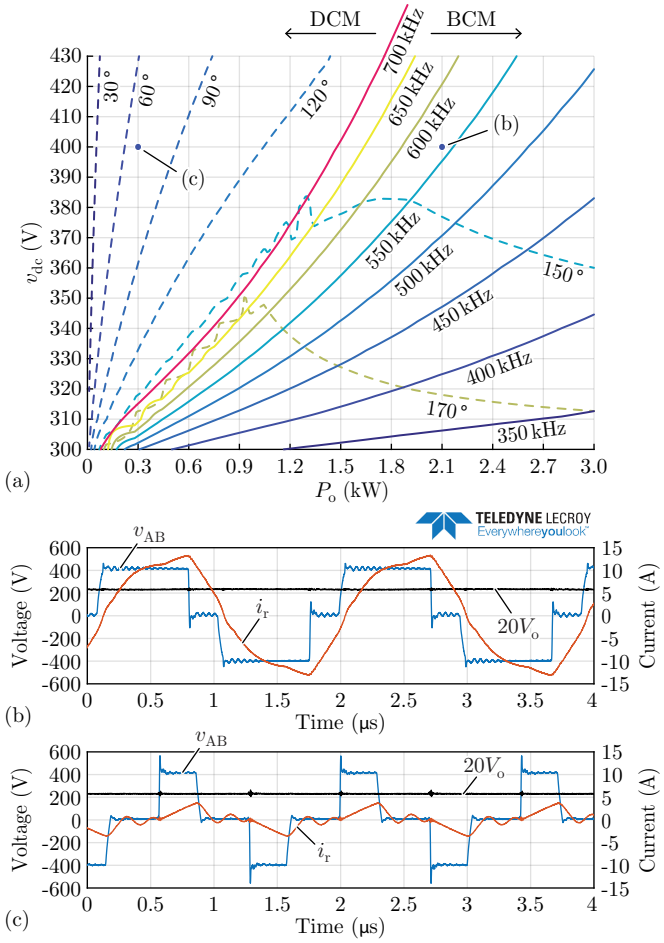

Fig. 4.2: (a) Voltage/Output-Power map of all hardware-prototype operating points and their respective f_s and ϕ control values. (b) Key measured waveforms under BCM operation at 70 % load and 400 V_{dc} (notation from Fig. 4.1(b)), cf. operating point (b) indicated in (a). (c) Key measured waveforms under DCM operation at 10 % load and 400 V_{dc}, cf. operating point (c) indicated in (a).

4.2.2 BCM *versus* CCM

The boundary and continuous conduction modes differ essentially on the shape of the tank excitation voltage v_{AB}. BCM controls the full-bridge such that v_{AB} assumes 0 V for a certain time before i_r crosses zero, allowing the combination of frequency and duty cycle modulations. CCM, however, generates only positive and negative values of v_{AB} ($\pm v_{dc}$), limiting the output regulation to frequency control. The additional 0 V interval allows BCM to have a larger conversion-ratio range for the same switching frequency relative to CCM, as now the resonant gain (with $L_m \rightarrow \infty$):

$$\frac{nV_o}{v_{dc}} = \frac{\frac{f_s}{f_r}}{\sqrt{\left(\frac{f_s}{f_r}\right)^2 + Q^2\left[\left(\frac{f_s}{f_r}\right)^2 - 1\right]^2}} \sin(\pi d) \tag{4.1}$$

depends also on the duty cycle d of v_{AB}, which is generated by the application of a phase-shift $\phi = 2\pi d$ between the full-bridge legs. If d equals 0.5 ($\phi = \pi$), v_{AB} assumes a square shape and CCM operation takes place. In this particular case, $\sin(\pi d)$ equals 1 and (4.1) relies on f_s as its only control variable.

Recalling Section 2.3.1, the quality factor (Q) is load-dependent and can be written as $Q = \frac{Z_r}{R_p}$, where $Z_r = \sqrt{\frac{L_r}{C_r}}$ is the tank characteristic impedance and $R_p = \frac{8n^2}{\pi^2}\frac{V_o^2}{P_o}$ is the equivalent load resistance seen from the primary side, which depends on both output load (P_o) and transformer turns-ratio (n). Fig. 4.3(a) plots the gain-*versus*-frequency characteristic of the hardware prototype for both BCM and CCM at full-power (dashed lines). Both modes have, by definition, the same gain near the resonant frequency ($f_r = \frac{1}{2\pi\sqrt{L_r C_r}} = 300\,\text{kHz}$). In this situation, $\frac{nV_o}{v_{dc}}$ equals 1 and the turns ratio is set according to the lowest input voltage required (cf. Tab. 1.1): $V_{dc,min} = 300\,\text{V}$, $V_o = 12\,\text{V} \rightarrow n = 25$. At any higher input voltage, both BCM and CCM have to increase the switching frequency in order to keep the output at 12 V. In BCM, however, the same gain can be achieved by switching at a lower frequency (see dashed lines in Fig. 4.3(a)). BCM control therefore extends the allowable input voltage range relative to CCM and benefits from lower switching losses and conduction losses in frequency-related resistances.

As i_r is far from having a sinusoidal shape for frequencies higher than f_r (see waveforms in Fig. 4.3(b)), the FHA used to derive (4.1) is not accurate enough for comparing gain plots with circuit-simulation results. The exact

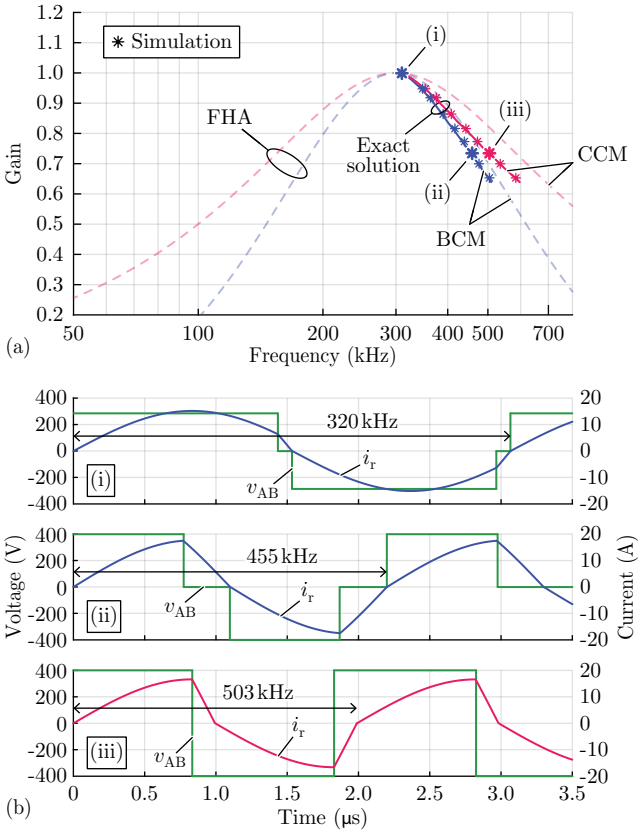

Fig. 4.3: (a) Resonant-tank gain-*versus*-frequency plots using the FHA solution of (4.1) and the exact solution of (4.2) at full-power. (b) Particular time-domain waveforms are shown to highlight the frequency deviation between BCM and CCM: (i) at $\frac{nV_o}{v_{dc}} = 1$, both BCM and CCM switch with $f_s \approx 320\,\text{kHz}$; while at $\frac{nV_o}{v_{dc}} = 0.735$, (ii) BCM switches with $f_s = 455\,\text{kHz}$ and (iii) CCM with $f_s = 503\,\text{kHz}$.

solution is found solving the 2nd-order, resonant-tank equations:

$$\begin{aligned} v_{\mathrm{r}} = &- (v_{\mathrm{AB}} - nV_{\mathrm{o}} - V_{\mathrm{r},0}) \cos(2\pi f_{\mathrm{r}} t) + \\ &+ I_{\mathrm{r},0} \sin(2\pi f_{\mathrm{r}} t) Z_{\mathrm{r}} + v_{\mathrm{AB}}(t) - nV_{\mathrm{o}} \\ i_{\mathrm{r}} = &\frac{v_{\mathrm{AB}} - nV_{\mathrm{o}} - V_{\mathrm{r},0}}{Z_{\mathrm{r}}} \sin(2\pi f_{\mathrm{r}} t) + I_{\mathrm{r},0} \cos(2\pi f_{\mathrm{r}} t), \end{aligned} \tag{4.2}$$

for each different v_{AB} excitation over one switching period. Fig. 4.3(a) shows, in solid lines, the exact solution of the gain-*versus*-frequency plot for both BCM and CCM. The accuracy is compared and validated by circuit-simulation data displayed on the top of these lines and three different operating points are chosen for comparison purposes. Near the resonant frequency of the tank ($v_{\mathrm{dc}} = 300\,\mathrm{V}$, $f_{\mathrm{s}} = 320\,\mathrm{kHz}$), both BCM and CCM achieve the same gain by switching at the same frequency. That does not hold true for lower gain values though, as the curves of BCM and CCM start to move away from each other. If we analyse v_{AB} and i_{r} at $\frac{nV_{\mathrm{o}}}{v_{\mathrm{dc}}} = 0.735$ (waveforms (ii) and (iii) in Fig. 4.3(b)), BCM achieves the same gain switching 50 kHz slower than CCM due to the lower $\frac{\mathrm{d}i_{\mathrm{r}}}{\mathrm{d}t}$ of BCM during the zero-volt interval of v_{AB}. This puts CCM at a disadvantage, setting the preference for BCM as the converter's modulation scheme.

4.2.3 Implementation of the Proposed Control Scheme

The B/DCM modulation scheme was implemented for the hardware prototype of Fig. 4.1 using a small, low-cost 32-pin ST Arm Cortex M4 microcontroller and external logic-gate ICs embedded in 2-by-2 mm SOT packages. The logic circuit, shown in Fig. 4.4, operates based on the zero-crossing of the resonant current (i_{r}) captured by two comparator circuits with 10 mΩ shunt resistors connected to the clamped potentials $v_{\mathrm{dc}}+$ and $v_{\mathrm{dc}}-$ for switching noise reduction. When the current is above the defined threshold value $|I_{\mathrm{th}}|$ (adjusted by the potentiometers in Fig. 4.4(a)), the normally-high zero-current-detection signals ZCD_{H} and ZCD_{L} become low, indicating current conduction on the converter's secondary-side (see Fig. 4.5). This happens for both $+I_{\mathrm{th}}$ and $-I_{\mathrm{th}}$ respectively to the positive and negative half-cycles of i_{r}. Thus, ZCD_{H} and ZCD_{L} are used to generate the turn-on and turn-off signals for the secondary-side MOSFETs ($S_{5\mathrm{x}}$,$S_{6\mathrm{x}}$), as they are switched only when the ZCD circuit detects current flowing toward the secondary side. Fig. 4.4(c) shows the logic circuit that generates $S_{5\mathrm{x}}$ and $S_{6\mathrm{x}}$, where two set-reset latches are used to avoid signal bouncing that could be introduced by noise during the ZCD_{H} and ZCD_{L} transitions.

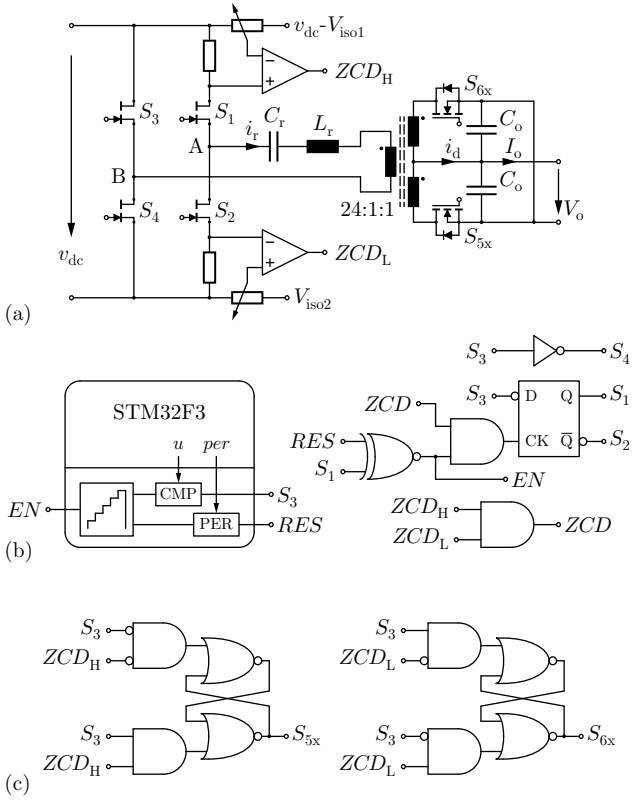

Fig. 4.4: (a) Zero-current-detection (ZCD) circuits implemented with 10 mΩ shunt resistors, precision potentiometers and large-bandwidth comparators to generate the ZCD_H and ZCD_L signals for the B/DCM control logic. (b) MCU and external logic gates that generate the switching signals $S_1 - S_4$. (c) SR latch circuits to avoid S_{5x}/S_{6x} signal bouncing.

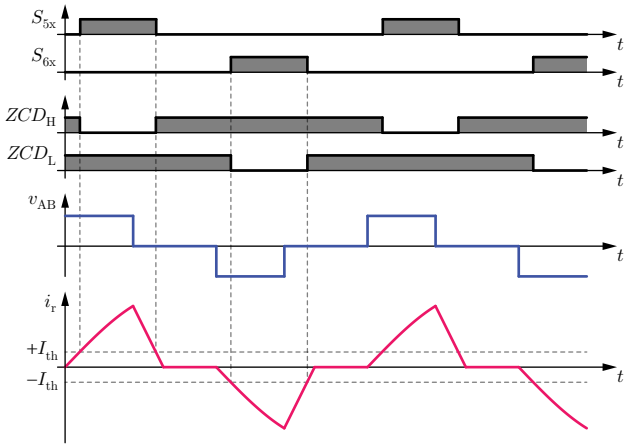

Fig. 4.5: Generation of S_{5x} and S_{6x} from the zero-current-detection signals ZCD_H and ZCD_L, which indicate current conduction above or below the defined threshold values $+I_{th}$ and $-I_{th}$.

Fig. 4.4(b) shows the implemented logic that generates the full-bridge PWM signals ($S_1 - S_4$). In DCM mode (see Fig. 4.6(a)), the period of the MCU internal timer (*per*)—which toggles S_1 and S_2—is set to the maximum switching frequency selected by design. The current is therefore controlled by the bridge-legs phase-shift only, which is adjusted by the control variable u and the toggling of S_3/S_4. The ZCD_H/ZCD_L signals are combined into one single ZCD signal, whose rising edge also defines the commutation of S_1 and S_2. In DCM, however, ZCD's rising edge happens before the end of the minimum period *per*, so the timer continues to count and i_r reaches zero before the end of the half-period. For higher output loads though, u is increased by the control algorithm to provide more current to the output. For the particular case of Fig. 4.6(b), u approaches *per* and ZCD becomes high only after the end of the period, forcing the logic circuit to disable the MCU counter (through the *EN* pin) and to toggle S_1 and S_2 later, once zero-i_r is detected. This scenario shows the transition from DCM operation to BCM, where now both frequency and phase-shift are modulated. If more power is demanded, u is further increased, reaching *per* in the case of Fig. 4.6(c). Here, *per* is not a fixed value any more, but assumes the same value of u, and both

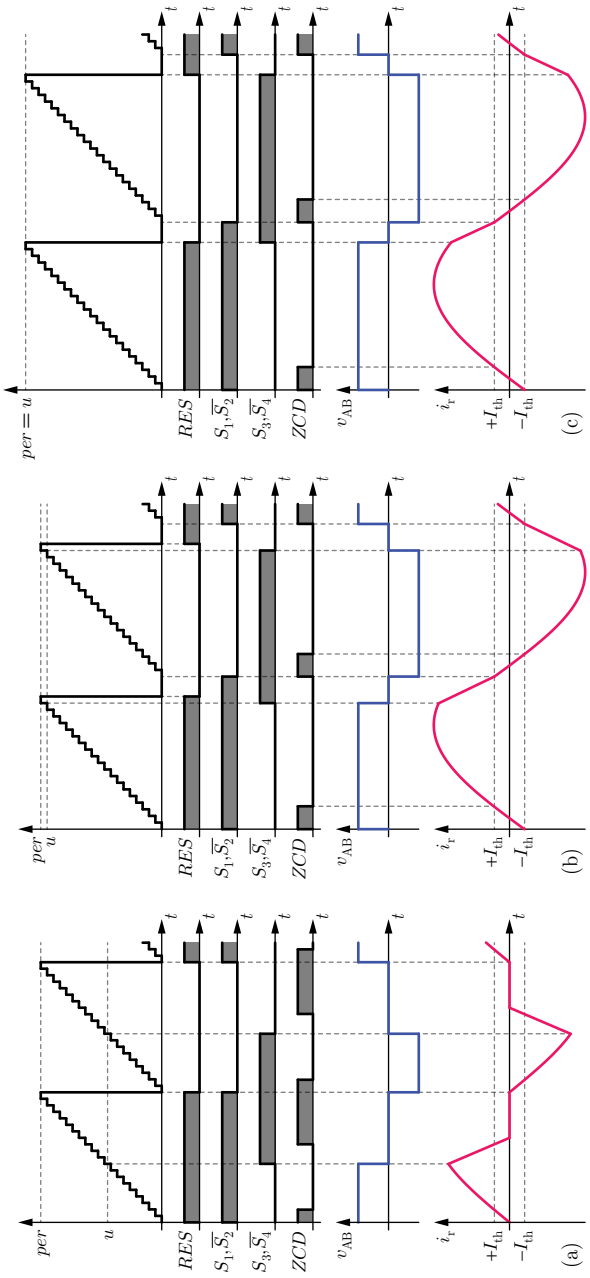

Fig. 4.6: Key waveforms and signals for the implemented control logic under DCM operation (a), BCM operation (c), and in the transition between the two modes (b).

increase together as higher currents are demanded, operating toward lower switching frequencies.

Alternatively to the ZCD circuit of Fig. 4.4(a) is the current transformer (CT) of Fig. 4.7. The key advantage of the CT over the former approach is the reduction of the current that flows through the shunt, allowing the selection of higher resistances while losses are still kept low. A larger shunt resistor improves the signal-to-noise ratio and ultimately avoids wrong switching caused by the inevitable common-mode noise of switching converters. Thus, after encountering control issues due to the low noise immunity of the ZCD circuit of Fig. 4.4(a), the CT prototype of Fig. 4.8(a) was designed to replace it and improve the signal-to-noise ratio. This current transformer is implemented on a 10-layer PCB with 2 layers for the primary-side winding (where i_r flows, cf. Fig. 4.8(b)), 6 layers for the secondary-side winding (30 turns in total, 5 turns per layer, cf. Fig. 4.8(d)) and 2 shielding layers to protect the secondary-windings from switching-noise coupling (see Fig. 4.8(c)). A 10 Ω burden resistor/shunt is connected to the secondary-winding, where the voltage is measured and compared to the threshold value for the generation of ZCD_H and ZCD_L. Voltage isolators are not needed for the CT approach thanks to its inherent galvanic isolation, yielding a very compact and efficient design with total losses less than 1 W.

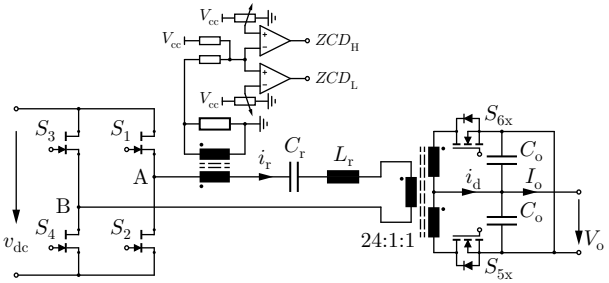

Fig. 4.7: Alternative zero-current detector comprising a current transformer, two high-precision potentiometers and two high-bandwidth comparators.

Fig. 4.9 showcases measured waveforms of the PCB-integrated CT under operation. The voltage across the shunt resistor (v_shunt)—an image of the resonant current (i_r)—has very low noise despite the positioning of the CT close to the converter's switching node, yielding precise zero-crossing detection and adequate signalling for the secondary-side synchronous rectifiers (S_{5x},S_{6x}), as shown in the bottom pane of Fig. 4.9.

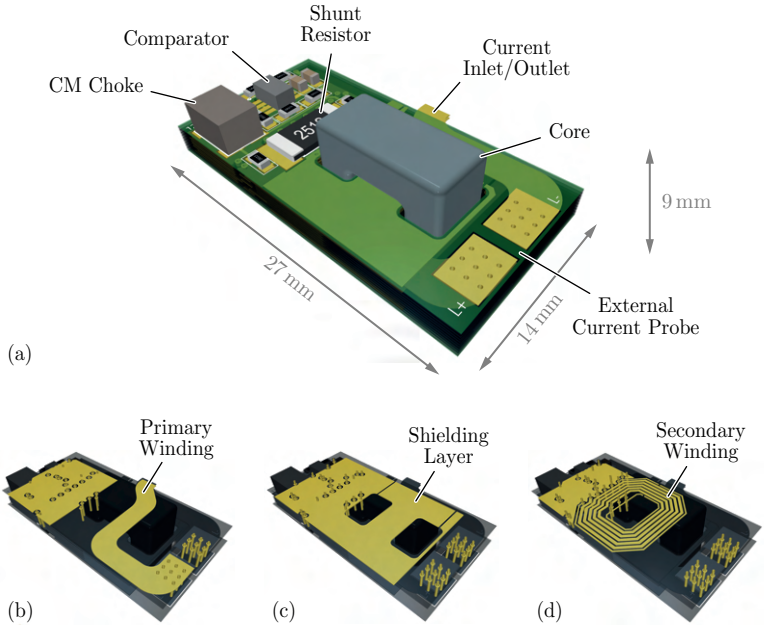

Fig. 4.8: (a) PCB-integrated current transformer (CT) for detecting i_r zero crossing. (b-d) Selected internal layers of the 10-layer-PCB design for exemplification: (b) primary winding (2 layers in total), (b) shielding layers between primary and secondary windings (2 layers in total), and (c) secondary winding (6 layers in total). Pads $L+$ and $L-$ allow the insertion of an external current probe.

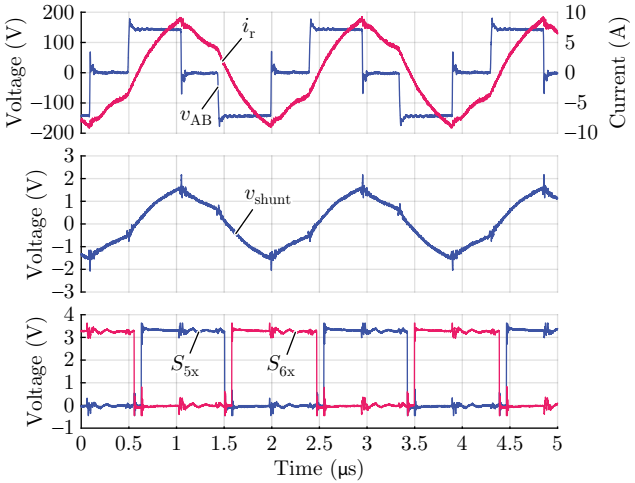

Fig. 4.9: Measured zero-current-detection (ZCD) signals (bottom pane) generated from the comparison of the shunt voltage (middle pane) with the threshold values $+I_{th}$ and $-I_{th}$. The shunt voltage (v_{shunt}) results from the transformation of i_r through the PCB-integrated CT of Fig. 4.8(a). The primary current i_r is measured using an external current probe.

4.2.4 Experimental Performance

The hardware prototype of Fig. 4.1(a) was characterized across the wide-V_{dc} range from 10 % load to the full 3 kW output power. Measured efficiencies for the implemented converter are reported in Fig. 4.10 (key components specified in Tab. 4.2 and design details shown in Fig. 4.11(a-d)), with a maximum of 94 % near 50 % load and the minimum V_{dc}. The converter power density is 350 W/in^3, with 16 % of the volume dedicated to the resonant inductor (L_r) and 41 % consumed by the snake-core matrix transformer.

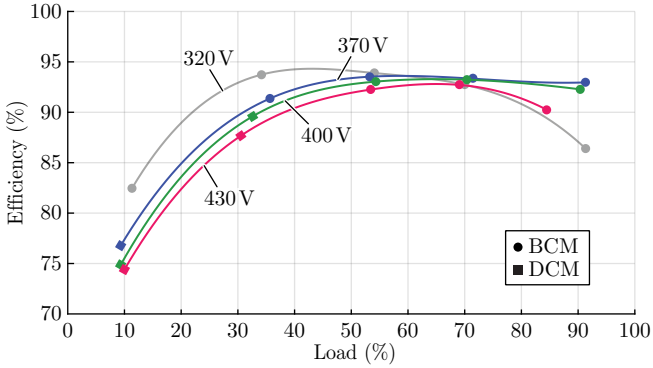

Fig. 4.10: Measured DC/DC efficiency over input voltage V_{dc} and load variation (prototype of Fig. 4.1(a)).

This converter achieves high power density and validates the control technique and transformer design with reasonably efficient operation across wide V_{dc} and load ranges. In the hardware converter, though, there is significant self-heating in the GaN HEMTs at high output power, degrading efficiency due to increased R_{on} at high junction temperatures and lack of soft-switching at light load. Additionally, the SR body diodes conduct for a significant portion of the on-time (approximately one-sixth of the switching period), increasing losses in these MOSFETs by a factor of 3 compared to an ideal synchronous rectification. In a first approximation, diode losses increase linearly with output power ($P_{diode} \approx V_F I_{avg}$), reducing efficiency across all load levels. Moreover, the converter's cube-shape is not optimal for PCB designs, as limited surface is available for heat extraction, which requires bulky aluminum heat sinks that occupy significant space. The converter is also placed in an unfavorable position, at the back of the PSU case, being the last element to receive cold air from the front side (cf. Fig. 4.11(e)).

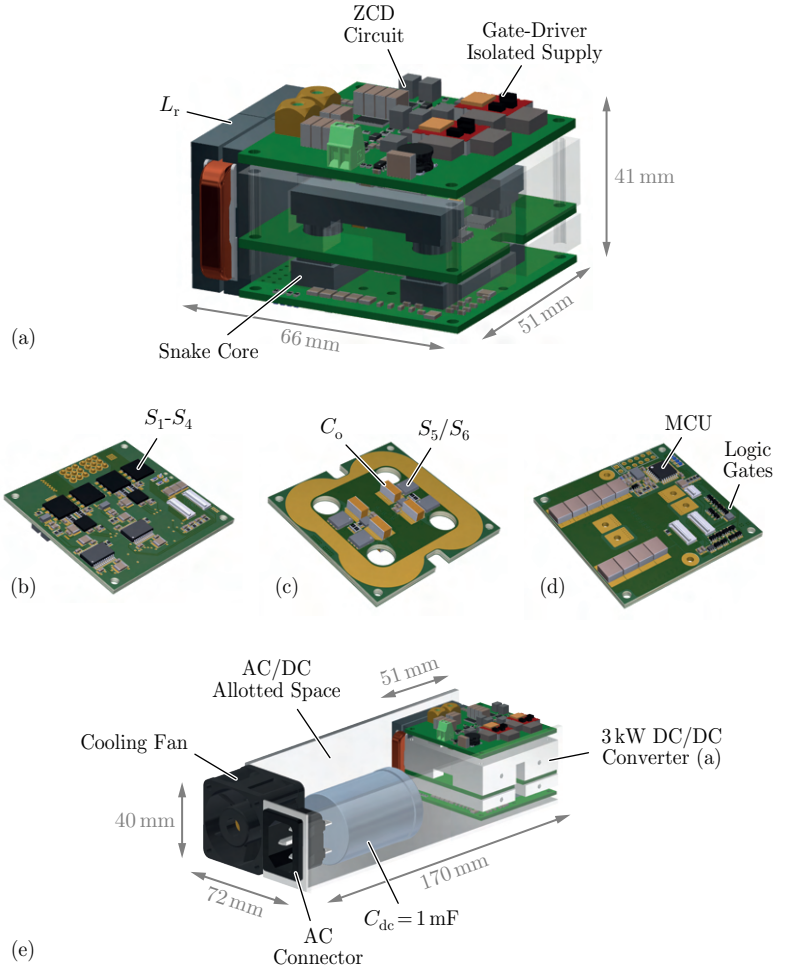

Fig. 4.11: (a) 3-D-model of the B/DCM converter with transparent heat sink to show the details of the snake-core transformer. Highlight on the three designed PCBs: (b) full-bridge switching stage, (c) matrix transformer and synchronous rectifiers, and (d) output and control. (e) Virtual placement of the converter inside the PSU case (see Section 1.1 for details on the PSU volume partitioning).

Tab. 4.2: Key components of the hardware prototype of Fig. 4.1(a).

Parameter	Value
S_1-S_4	CoolGaN (GaN) 600 V, IGLD60R070D1
	70 mΩ ($R_{ds(on)}$), 41 nC @ 400 V (Q_{oss})
S_5-S_6	OptiMOS (Si) 40 V, BSC007N04LS6
	0.7 mΩ ($R_{ds(on)}$), 103 nC @ 20 V (Q_{oss})
Transformer	Snake-core transformer
	PCB windings, 4-layers, N49 core, no airgap
Res. inductor	8 µH, 16 A peak current
	Litz wire, 6 turns, N49 core, 2 mm airgap
Res. capacitor	13x 2.7 nF, 450 V, C0G
	CGA4J4C0G2W272J125AA

The next-iteration design must therefore improve the GaN HEMT thermal design and the SR trigger control to increase efficiency across all operating modes. An improved converter design with a flat instead of a cube form-factor is also critical to enhance heat extraction. Then, soft-switching in all semiconductor devices and throughout the entire load and voltage ranges is required to reduce losses at light load. Finally, based on the findings and measurements of the hardware prototype, a circuit-level modification is proposed to support the required loss reduction and to improve the operating conditions of the converter in the nominal input voltage range. The expected performance improvements of the new design are explored in the remainder of the chapter.

4.3 Design Improvements

4.3.1 Additional Degree of Freedom

A reconsideration of the circuit design and control scheme is needed to increase the converter efficiency. By setting the lowest input voltage at the resonant frequency (gain of 1 in Fig. 4.3(a)), the converter can only operate in a ”buck” mode. As resonant converters are most efficient switching at the resonant frequency, the buck-only operation of the current hardware prototype maximizes efficiency at the minimum V_{dc} (as seen experimentally in Fig. 4.10 for 320 V_{dc}), which occurs only during the infrequent fault operation.

In the nominal operating range for this application (V_{dc} = 370 V-430 V, see Fig. 1.2), the switching frequency is relatively high and DCM—where one of the half-bridges is hard-switched—is used extensively, resulting in the steep degradation of efficiency at light load seen in Fig. 4.10.

Intuitively, a design would have higher efficiency if f_s was closer to the L_r-C_r resonant frequency (f_r) in the nominal V_{dc} range; that is, if the gain of 1 operating point ($\frac{nV_o}{v_{dc}} = 1$) was selected nearer the 370–430 V_{dc} range. Fault operation would then operate in a "boost" mode, which requires a finite magnetizing inductance (L_m) and LLC-style operation in this boost regime [89]. Considering L_m as an additional design parameter, the gain transfer function of (4.1) is expanded based on (2.5), giving:

$$\frac{nV_o}{v_{dc}} = \frac{(m-1)\left(\frac{f_s}{f_r}\right)^2}{\sqrt{\left[m\left(\frac{f_s}{f_r}\right)^2 - 1\right]^2 + Q^2(m-1)^2\left(\frac{f_s}{f_r}\right)^2\left[\left(\frac{f_s}{f_r}\right)^2 - 1\right]^2}} \sin(\pi d), \qquad (4.3)$$

where $m = 1 + \frac{L_m}{L_r}$ represents the ratio between L_r and L_m. As the magnetizing inductance becomes much larger than L_r ($L_m \to \infty$), (4.3) collapses to (4.1).

Fig. 4.12(a) plots the gain function (4.3) for three different selections of L_m. The reduction of the magnetizing inductance L_m allows for boost-mode operation, with gains above unity. Here, in addition to the aforementioned BCM and DCM control schemes used to operate the current hardware prototype (cf. Fig. 4.2), CCM is introduced for switching frequencies below the resonant frequency of 300 kHz. Typical waveforms of the three operating modes are shown in Fig. 4.12(b,c,d). If the converter requires boost-mode operation, the control imposes a square-wave v_{AB} voltage with $f_s < f_r$, as shown in Fig. 4.12(b), and gains above 1 can be achieved. On the other hand, BCM control is used in buck-mode operation for $f_r < f_s < f_{s,max}$ up to a maximum switching frequency ($f_{s,max}$) defined by design (see Fig. 4.12(c)). For $f_s = f_{s,max}$, DCM applies and the switching frequency is fixed while the duty cycle of v_{AB} is changed to control the power flow (cf. Fig. 4.12(d)).

DCM should only be used at light load conditions, as i_r is no longer sinusoidal and high losses result for high output-power values (P_o). For this reason, it would be reasonable to select the design with L_m = 53 µH instead of 89 µH in Fig. 4.12(a), as a lower step-down gain at the transition between BCM and DCM is achieved, extending BCM operation to lower P_o values. However, the design with L_m = 53 µH requires twice as much resonance inductance L_r for keeping the maximum boost gain at 1.2, increasing the volume of this component accordingly. Furthermore, a smaller L_m yields larger magnetizing

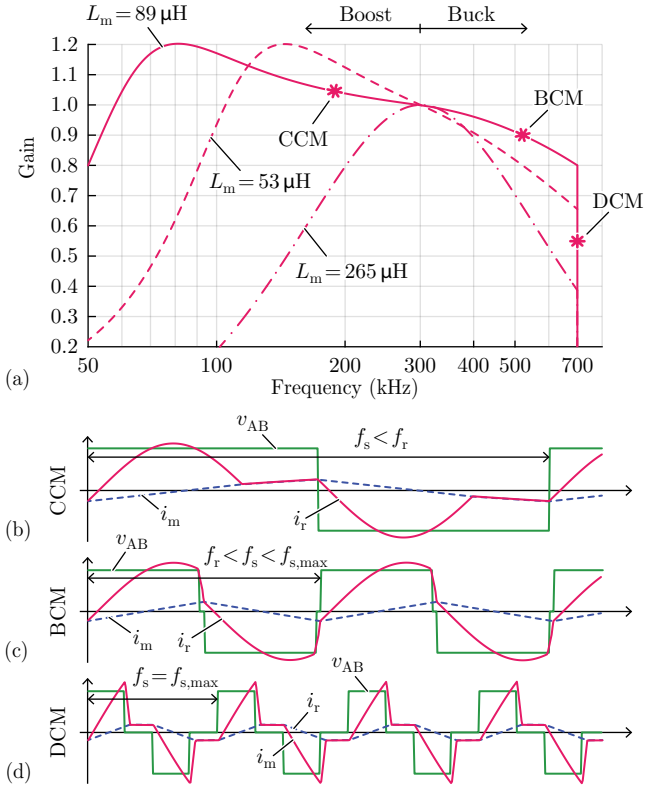

Fig. 4.12: (a) Plot of the gain function (4.3) for different L_m values. Design parameters for $L_m = 89\,\mu H$ and $256\,\mu H$ are detailed in Tab. 4.3. For $L_m = 53\,\mu H$: $nV_o = 360\,V$, $L_r = 7.4\,\mu H$ and $C_r = 38\,nF$. Three operating modes are highlighted in (a) with corresponding time-domain waveforms ($L_m = 89\,\mu H$): (b) CCM for boost operation ($f_s < f_r$), and (c) BCM ($f_r < f_s < f_{s,max}$) and (d) DCM ($f_s = f_{s,max}$) for buck operation.

currents (i_m), which, on the one hand, increase conduction losses, but, on the other hand, support ZVS at light loads. The magnetizing inductance as a free design parameter therefore introduces a tradeoff in the converter design, but nevertheless efficiency improvements are expected, as the new degree of freedom of L_m allows to shift the converter's nominal operating region closer to the most-efficient gain-of-1 operating point. The extent of these improvements will be assessed in the following.

4.3.2 Design Considerations

In order to confirm the benefits of the proposed enhanced control scheme, a performance comparison between the current hardware prototype, the next-iteration design and common LLC designs must be conducted. To accomplish this comparison, the performance across the v_{dc} and load ranges for all these three designs is evaluated: (i) the buck-only prototype of Section 4.2 ("B/DCM"), (ii) a design with B/DCM control in the nominal range and CCM control during fault conditions ("Hybrid"), and (iii) an CCM-only design without B/DCM control ("LLC"). The B/DCM design operates only with the waveforms that are shown in Fig. 4.12(c,d), while the LLC design is mostly characterized by the waveforms of Fig. 4.12(b). The Hybrid control, however, benefits from all three operating modes in Fig. 4.12(b,c,d). These designs must operate down to 300 V_{dc} but the efficiency is optimized for operation in the nominal v_{dc} range.

To shift the nominal operating range closer to the resonant frequency and consequently optimize efficiency, nV_o must properly selected such that $\frac{nV_o}{v_{dc}} = 1$ for a v_{dc} near or within the nominal range. The Hybrid design places nV_o just below the nominal range minimum (360 V_{dc}) and maximizes the $m-1$ ratio, L_m/L_r, and the tank quality factor, Q, to achieve the required gain at 300 V_{dc}. These design choices force the Hybrid control to operate in buck mode across the nominal input range ($v_{dc} > 360$ V), and to enter boost mode only in case of a mains fault—taking advantage of the B/DCM-control benefits described in Section 4.2. Following the efficiency-optimal design guidelines in [89], the LLC design places nV_o at 420 V_{dc} and solves for the maximum $(m-1)Q$ product that can maintain regulation down to 300 V_{dc}. The values for each design, including the first-generation prototype, are listed in Tab. 4.3, and the gain characteristics for each tank are compared in Fig. 4.13(a).

Relative to the LLC, the Hybrid design needs much lower boost gain and extends the regulation capability at $f_s > f_r$, resulting in a higher $(m-1)Q$ figure-of-merit and lower circulating currents. The LLC design follows the

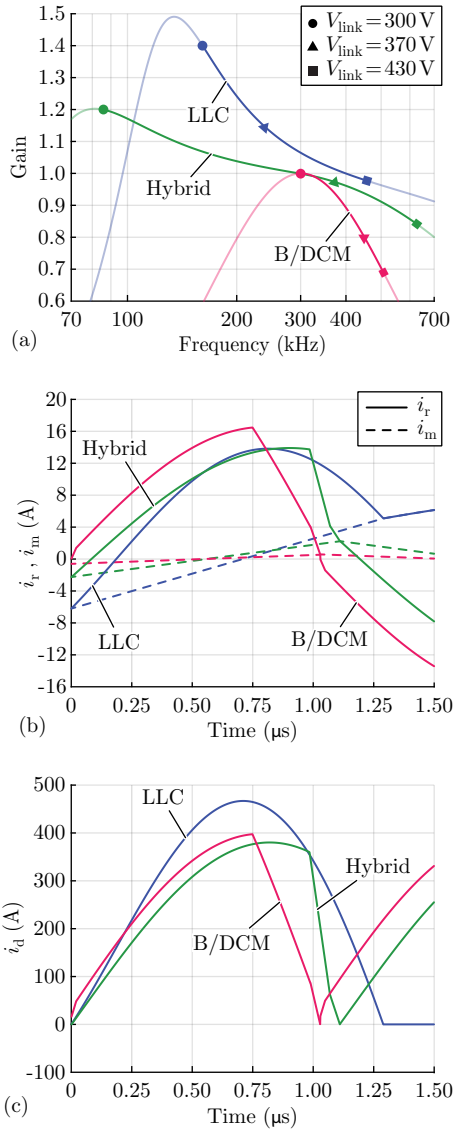

Fig. 4.13: Operating characteristics for the three proposed designs at $P_{\text{o}} = 3\,\text{kW}$ (cf. Tab. 4.3). (a) Voltage gain. (b) Predicted resonant-tank current (i_{r}) and magnetizing current (i_{m}) at $400\,\text{V}_{\text{dc}}$. (c) Predicted secondary-side rectified current (i_{d}) at $400\,\text{V}_{\text{dc}}$.

Tab. 4.3: Key specifications for compared designs.

Parameter	B/DCM	Hybrid	LLC
f_r	300 kHz	300 kHz	400 kHz
$f_{s,min}$	300 kHz	75 kHz	75 kHz
$f_{s,max}$	700 kHz	700 kHz	700 kHz
nV_o	300 V	360 V	420 V
L_r	8 µH	3.7 µH	4.4 µH
C_r	35 nF	76 nF	36 nF
L_m	265 µH	89 µH	48 µH

design guidelines of [89], where we must tradeoff conduction losses with a lower magnetizing inductance and the width of achievable gain. An efficiency-maximized design yields the LLC gain curve of Fig. 4.13(a). A comparison between current waveforms at the nominal v_{dc} and full output power are shown in Fig. 4.13(b,c). The small magnetizing inductance in the LLC (needed for high boost gain) results in higher primary-side RMS currents for the same output power, increasing conduction losses in the transformer primary windings and full-bridge power devices. The LLC design has also higher secondary-side RMS currents due to a zero-current interval during the "Open"-mode (O-mode—discontinuous conduction on the secondary side [89]), which increases the peak value of that current to compensate for the 0 A interval (cf. Fig. 4.13(c)), leading to higher conduction losses in the SR MOSFETs.

Relative to the B/DCM, the Hybrid design operates closer to the gain-of-1 operating point and has currents with lower peak-to-average ratios. Furthermore, the magnetizing current is larger relative to B/DCM, improving primary-side ZVS at light load at the expense of slightly-higher conduction losses. The Hybrid design therefore has the potential to outperform both other designs, but a loss analysis is required to confirm this claim and benchmark the achievable efficiency, which is performed below.

4.3.3 Analysis Techniques & Loss Models

To compare the three designs across the full range of v_{dc} and output power, the steady-state waveforms are numerically calculated at each operating point and first-order models are used to estimate the key loss mechanisms, assuming a fixed volume for magnetics and ideal synchronous rectification (i.e. zero body diode conduction). For each design and at each v_{dc}-load operating point,

there is a unique set of operating conditions that satisfy periodic steady-state conditions. Unfortunately, with a finite magnetizing inductance and the inclusion of a DCM mode (or O-mode in case of LLC), there are no analytical solutions and the sinusoidal approximation is inaccurate for much of our operating range [88]. Numerical techniques are therefore used to find the state variables in steady-state operation, and the full current and voltage waveforms for the converter are then known.

With the full current and voltage waveforms synthesized, power dissipation in the key components is estimated with first-order loss models. In the primary-side GaN HEMTs, conduction losses ($i^2 R_{\text{on}}$) with R_{on} equal to the datasheet value at 100 ℃) and hard-switching losses are included, and any soft-switching losses from resonantly charging and discharging the parasitic output capacitance (C_{oss}) are ignored. At 500 kHz, the worst-case error from ignoring these soft-switching losses is around 0.75 W per device [97]. To include hard-switching losses, it has to be considered that the first switching transition per half-cycle will be soft-switched (see Fig. 4.3(b)) if the load current is sufficiently high, and this assumption is made for the full operating space. The hard-switched losses that occur from partial ZVS are calculated using the method in [98], with the current at the switching transition known from the numerical synthesis.

The resonant inductor can be integrated into the same snake-core structure used for the transformer in this design [94], which will be used here to simplify the calculations. To do this, the nearly-perfect interleaving between the primary and secondary windings will need to be reduced, which will increase the AC resistance. To calculate conduction losses in the resonant inductor and transformer, an AC resistance factor of $\frac{R_{\text{AC}}}{R_{\text{DC}}} = 1.1$ is used beyond the DC resistance of the windings. Core losses are calculated using the Generalized Steinmetz fitting [99] based on the maximum magnetizing current, and losses in the resonant capacitor (C_{r}) can be comfortably ignored.

Because they operate under ZVS conditions, the secondary-side synchronous rectifier device losses are assumed to only include conduction losses. In this model, perfect synchronous rectification is assumed, or zero diode conduction time. Accordingly, a fast, reliable sensing and driving circuit is critical to mitigating any additional losses that occur from diode conduction.

4.3.4 Performance Comparison

Fig. 4.14 shows the calculated converter losses for the prototype converter (B/DCM, cf. Fig. 4.1(a)) and the two potential design improvements (Hybrid

and LLC). The B/DCM converter achieves the lowest losses at input voltages that only occur during fault events for this application, and both the Hybrid and B/DCM design outperform the conventional LLC in the nominal input voltage range (green, shaded area). At 400 V_{dc} and 3 kW output power, the LLC dissipates 81 W, the Hybrid design dissipates 70 W, and the B/DCM design has 78 W of predicted losses. The required inductance values are more than 50 % lower in the Hybrid design than in the B/DCM design, further improving efficiency for a fixed-volume magnetics design or power density for a fixed-loss design.

Fig. 4.15 shows the calculated efficiencies for the three aforementioned designs. It again proves that the Hybrid design is the best choice to improve efficiency at the nominal-input-voltage range (highlighted in blue). These efficiencies must be carefully analysed, though, as they are not directly comparable with the measured efficiencies of Fig. 4.10 due to the simplistic modelling approach conducted. Nevertheless, they serve as adequate and insightful indicators if used to compare one design against the other, as they all were submitted to the same modeling approach. For any LLC design, there exists a fundamental tradeoff between nominal efficiency and gain range [33], whereas with the B/DCM control, the Hybrid design can use a lower gain range. The higher circulating currents, shown at one operating point in Fig. 4.13(b), increase losses throughout the operating region and this analysis confirms the mutual exclusivity of high efficiency and wide voltage range for conventional LLCs. Based on the analysis here, the Hybrid design is necessary to reach higher efficiencies in the nominal voltage range.

4.3.5 Next-Iteration Hardware Prototype

The results presented in this section confirm the potential of the Hybrid design to outperform the compared ones, as intuitively justified throughout the section and verified by the loss analysis. Therefore, based on the Hybrid-design performance and the improvements described in Section 4.2.4, the next-iteration hardware prototype will consist of two identical modules of 1.5 kW each, which are then connected in a parallel-input parallel-output (IPOP) configuration. Fig. 4.16 anticipates how the two 1.5 kW modules should be placed inside the PSU case, with the remainder volume dedicated to the DC-link capacitor (C_{dc}), cooling fan, AC connector and AC/DC stage, as previously detailed in Section 1.1. This modular approach significantly enhances the converter's thermal management relative to the first-iteration prototype of Fig. 4.1(a). Furthermore, a power density of 300 W/in^3 is targeted, which is less

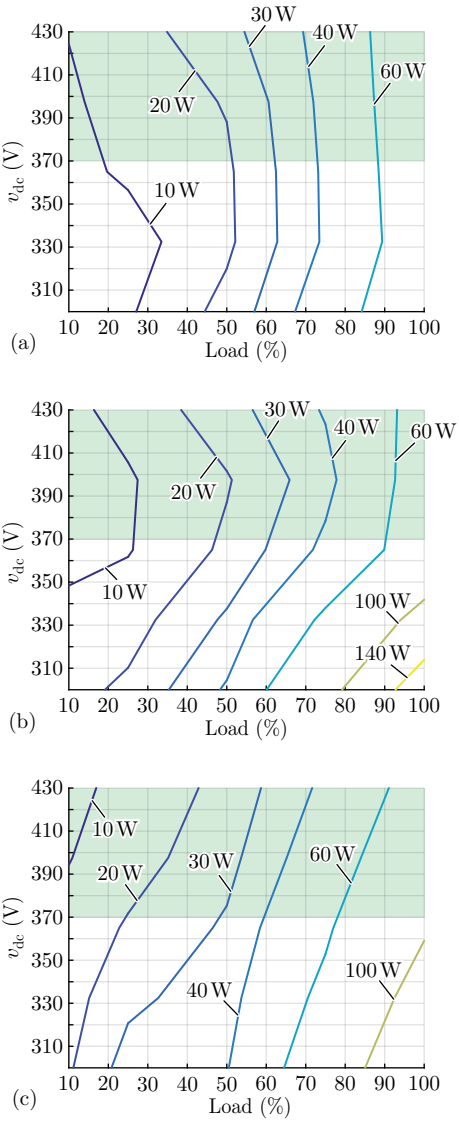

Fig. 4.14: Modeled losses at all v_{dc}-P_o operating points for: (a) the currently realized B/DCM design (cf. prototype shown in Fig. 4.1(a)), (b) the Hybrid control scheme, and (c) the efficiency-optimized traditional LLC design. The Hybrid design is the most efficient for the nominal operating conditions (highlighted in green).

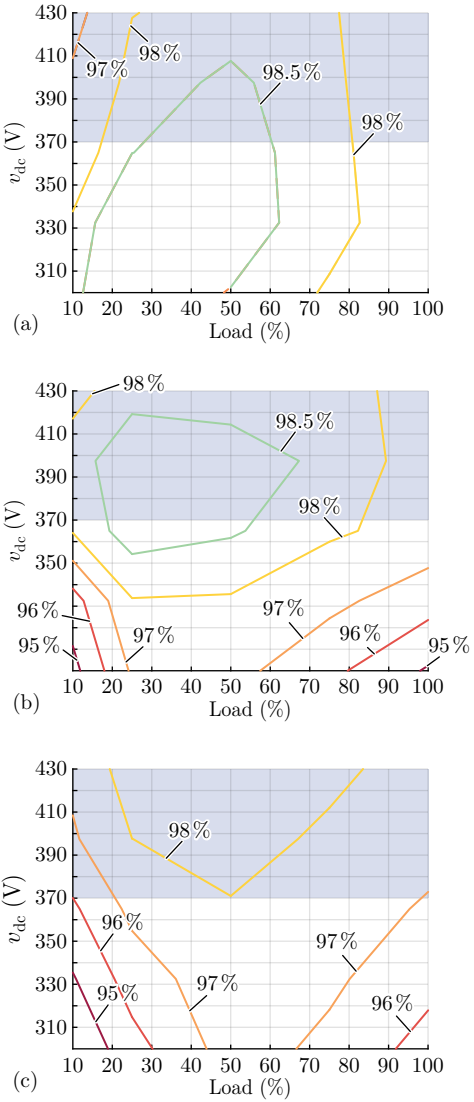

Fig. 4.15: Calculated efficiencies at all v_{dc}-P_o operating points for: (a) the currently realized B/DCM design (cf. prototype shown in Fig. 4.1(a)), (b) the Hybrid control scheme, and (c) the efficiency-optimized traditional LLC design. The Hybrid design is the most efficient for the nominal operating conditions (highlighted in blue).

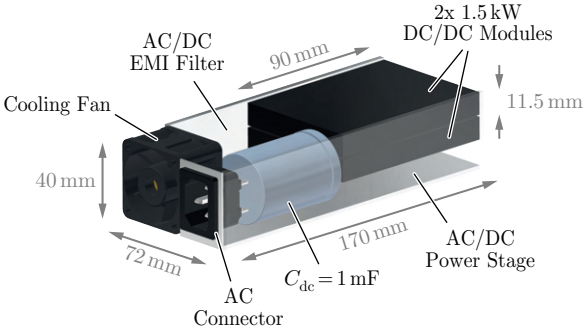

Fig. 4.16: PSU volume partitioning following the guidelines of Section 1.1 with two IPOP-connected 1.5 kW modules comprising the the DC/DC stage for enhanced thermal management and easier PCB integration.

than the current hardware, but still fulfils Tab. 1.1 specifications. The goal with these improvements and the relaxed power density—that are implemented and described in the next chapter—is to finally achieve the high efficiency demanded from next-generation DC/DC power modules (cf. Tab. 1.1).

4.4 Summary

A hardware prototype of a wide-input-voltage-range 370 V-430 V-to-12 V, 3 kW DC/DC converter is described, which employs B/DCM control and achieves high power density (350 W/in^3) but requires improvements to increase the efficiency beyond the measured 94 %. For this reason, predicted losses for three circuit and control combinations are compared, and the highest efficiency for an improved Hybrid design that utilizes both LLC and B/DCM control schemes is found. A detailed and comprehensive analysis on resonant-tank transfer functions and predicted time-domain current waveforms gives reasoning for the reported higher performance of the Hybrid control. In summary, the converter design takes advantage of the Hybrid-control benefits, and higher efficiencies at a power density of 300 W/in^3 are expected for the next-iteration hardware prototype that is analysed in detail in the next chapter.

5

LLC Resonant Converter with Continuous/Discontinuous-Conduction-Mode Control

Chapter Abstract

This chapter presents the conceptualization, design, modelling, fabrication, and experimental characterization of a 1.5 kW, 12 V-output DC/DC converter for industrial power supplies that is required to operate across a wide 300 V–430 V input voltage range. This module utilizes the continuous/discontinuous-conduction-mode control scheme applied to a LLC converter for complete soft-switching and a snake-core transformer to divide the output current with a balanced flux among multiple secondary windings. Detailed loss models are derived for every component in the converter. The converter achieves close to 96 % peak efficiency with a power density of 337 W/in^3 (20.6 kW/dm^3), excellent matching to the derived loss models, and zero-voltage switching even down to zero load. The loss models are used to identify improvements to further boost efficiency, the most important of which is the minimization of delay times in synchronous rectification.

5.1 Introduction

In previous chapters, key aspects regarding topology, control and magnetics were laid down as foundations for the conceptualization of a next-generation DC/DC power converter module that copes with the challenging demands of the increasingly-electric future. These aspects were used in Chapter 4 for the design of a wide-input-voltage-range, 400 V-to-12 V, 3 kW DC/DC series-resonant converter that validates the control method

and transformer design introduced earlier. This hardware prototype employs boundary/discontinuous-conduction-mode (B/DCM) control and achieves high power density (350 W/in^3), but requires improvements to increase the efficiency beyond the measured 94 %. For this reason, predicted losses for three circuit and control combinations were compared, and the highest efficiency for an improved Hybrid design that operates in both boost and buck modes was found. Therefore, based on the Hybrid-design performance and the proposed improvements described in Section 4.2.4, the next-iteration hardware prototype will consist of two identical modules of 1.5 kW each, which are then connected in a parallel-input parallel-output configuration to reach the desired 3 kW output power. This modular approach significantly enhances the converter's thermal management relative to the first-iteration prototype of Chapter 4 and is easier to PCB-integrate. Power density is also relaxed for this next-iteration hardware and targeted to 300 W/in^3, which still fulfils Tab. 1.1 specifications and allows efficiency improvements to achieving the goal of 96 % and beyond.

5.2 Converter Design

First, the design of the DC/DC converter module is detailed, which has the topology shown in Fig. 5.1 (adapted from the generic topology of Fig. 2.6), with the secondary split into four paralleled outputs to reduce the output current stress imposed on a single secondary winding and rectifier stage, and the inductor sitting inbetween the sub-transformers to equally share the winding parasitic-capacitance seen from the full-bridge stage. Before moving to the two most challenging passive components: the PCB-integrated transformer and primary inductor, both of which must achieve ultra-high copper utilization within the constraints of PCB fabrication methods, the gain range and controllability are analysed. The copper utilization is so critical to the converter performance that intermediate test setups are built to validate the analytical approach and optimization procedures. Finally, the capacitor and power-semiconductor selection is detailed to complete the design analysis of this demanding wide-input-voltage range, high-output-current, PCB-integrated DC/DC converter.

5.2.1 Topology, Gain Analysis, and Control

As discussed in Chapter 2, the challenge is to combine the controllability of buck-based converters, which enables a wide-input-voltage range, with the

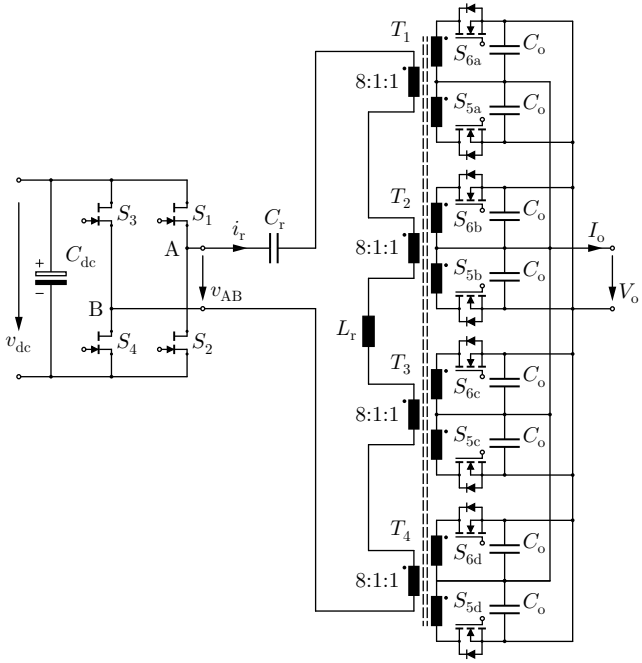

Fig. 5.1: Power circuit of the proposed DC/DC converter featuring GaN devices for the primary-side full-bridge, Si power MOSFETs operating as synchronous rectifiers on the secondary-side, and a series-input, paralleled-output, center-tapped matrix transformer.

high efficiency of LLC-based resonant topologies that feature soft-switching (ZVS and ZCS) across the full load and voltage ranges.

Topology

The topology challenges are driven by the combination of wide-input-voltage range (needed for hold-up time requirements) and complete soft-switching. A low-complexity topology and control scheme needs to be developed, which eliminates approaches such as (i) DCX transformers, which require pre-regulation to fix the input voltage to the DC/DC module [21], (ii) additional hold-up time extensions circuits, which require a full additional converter module [22], and (iii) reverse-feeding for hold-up time, which adds significant

control complexity to the DC/DC module [23]. Instead, a soft-switched LLC approach is aimed that can be controlled—with minimal complexity—across a wide gain range while maintaining soft-switching, and inspiration is drawn from matrix transformers used in server power supplies (e.g., [30]) to divide the high output current among multiple windings and rectifiers.

A full-bridge topology, as shown in Fig. 5.1, is chosen to excite the primary-side resonant tank. Relative to the half-bridge topology, the full-bridge has half of the primary-side current for a given power (with a tank excitation of $\pm v_{dc}$, rather than $\pm\frac{1}{2}v_{dc}$ for the half-bridge) and an additional control variable in the phase-shift between the two bridge legs, during which a variable-length voltage of 0 V can be applied to the tank. A center-tapped synchronous rectifier is selected for the secondary side, a topology that features a low semiconductor count, zero-voltage-switching, and no high-current output inductor. The equivalent circuit is shown in Fig. 5.2 (recalled from Fig. 2.7), including the LLC tank (C_r, L_r, and L_m), the reflected, equivalent load resistance (R_p), and the fundamental of the tank excitation (v_{AB}). The proposed converter's footprint, introduced in Section 4.3.5 (see Fig. 4.16), is partitioned according to Fig. 5.3, where the matrix transformer with integrated synchronous rectifiers and output capacitors is preliminary built as a square block that sets the converter's width (w) and height (h). The PCB inductor should also be square and therefore, together with the primary-side semiconductors and control circuitry, defines the footprint's length (l).

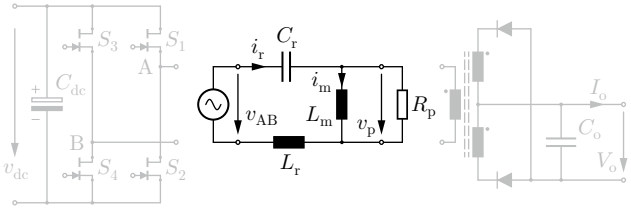

Fig. 5.2: Simplified version of Fig. 5.1 using the fundamental harmonic approximation (FHA) to capture the fundamental components of switched waveforms.

Gain

For LLC converters, the fundamental harmonic approximation (FHA) is typically used [88, 89] to describe the gain, or the output-to-input voltage ratio (v_p/v_{AB}), as a function of the control variable: switching frequency (f_s).

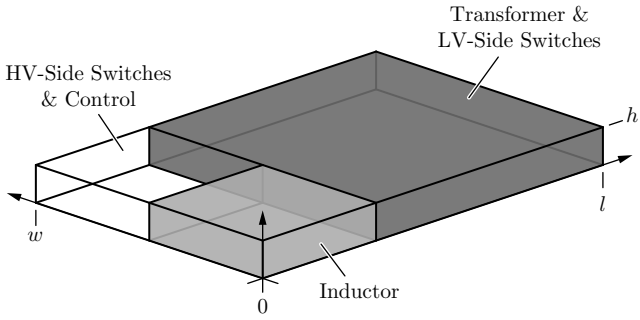

Fig. 5.3: Proposed layout with matrix transformer, synchronous rectifiers and output capacitors as the main block defining the converter's width (w) and height (h), and the PCB inductor and primary-side full-bridge fixing the footprint's length (l).

The gain as a function of switching frequency (normalized by the transformer turns ratio, n) is shown in Fig. 5.4, where the FHA is compared to the exact solution obtained through circuit simulation for the proposed design parameters. The FHA is used primarily for the design of the unity gain point and to assess the gain in the boost region, with margin implicit because the actual gain under boost conditions is always higher than that predicted by the FHA (as shown in Fig. 5.4). For a detailed mathematical description of the LLC gain under FHA, please refer to Section 2.3.1.

Recalling Section 2.3.1, each resonant-tank parameter relates to a particular design constraint: the transformer turns ratio, n, defines the operation mode for the converter (buck, boost, or both), L_m restricts the maximum gain, L_r defines the selectivity of the tank and therefore the required switching frequency range for a given gain, and C_r is used to tune the desired resonant frequency. Each of these parameters, though, also has constraints on its selected value: n must be an integer multiple of the number of output stages (secondary transformers) for symmetry, L_r must be optimized for low volume, C_r must have a withstand voltage that is achievable with commercially-available capacitors, and L_m should be large to minimize the magnetizing current and the associated conduction losses.

It is known from Section 4.3 that a combination of buck and boost modes will be required to achieve, simultaneously, high efficiency and a wide-input-voltage range, and the nominal input voltage of $v_\mathrm{dc} = 400\,\mathrm{V}$ is placed close to the resonant frequency, where $f_\mathrm{s} = f_\mathrm{r}$ and $nV_\mathrm{o}/v_\mathrm{dc} = 1$ (see Fig. 5.4). This results in $n = v_\mathrm{dc}/V_\mathrm{o} = 400\,\mathrm{V}/12\,\mathrm{V} = 33.33$, with $n = 32$ chosen for

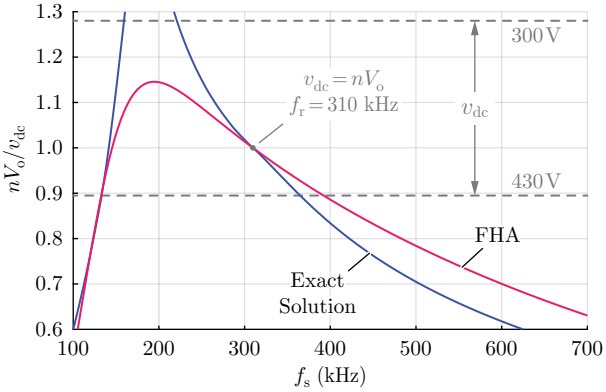

Fig. 5.4: Graphical description of the output-to-input conversion ratio (normalized by the transformer turns ratio n) as a function of the switching frequency (control variable). The exact solution, obtained through circuit simulation, is compared to the fundamental harmonic approximation (FHA), where it can be seen that the the FHA captures the correct monotonic behavior of the gain function. For the given v_{dc} range (300 V–430 V) and the parameters selected in this section, the converter operates from 210 kHz to 350 kHz.

a symmetric design of the matrix transformer ($nV_o = 384$ V). From here, following the guidelines of Section 2.3.2, $L_r = 24$ µH is selected to compromise between inductor volume and the maximum operating frequency at light load (with the inductor design detailed later in this section), mandating $L_m = 110$ µH to achieve the maximum gain at the minimum input voltage of $v_{dc} = 300$ V. A resonant frequency of 310 kHz is selected to balance the demanding efficiency and power density metrics of Tab. 1.1, which results in $C_r = 11$ nF. Differently from the hardware prototype of Chapter 4, this design achieves full ZVS at all load and input-voltage conditions, a requirement to approach the required metrics—a hard-switching half-bridge employing *IGLD60R070D1* GaN HEMTs at $v_{dc} = 400$ V and 310 kHz would generate switching losses of one third of the allowable losses in the *complete DC/DC converter* for 96 % efficiency at 50 % load!

Control

Finally, returning to the goal of a simplicity of control that approaches that of buck-based converters, a hybrid control loop and scheme is proposed

(shown in Fig. 5.5(a)). Variable switching-frequency and phase-shift control in continuous and discontinuous conduction modes is implemented based on a comparison between the measured output voltage and requested output voltage, with the gain monotonic above the peak frequency around 200 kHz (see Fig. 5.4). Here, CCM is chosen over BCM due to the proximity of the nominal operation to the resonant frequency, where BCM and CCM have similar performance (see Section 4.2.2 for design tradeoffs between BCM and CCM). An off-the-shelf gate-driver IC with an embedded dead-time generator drives the GaN full-bridge ($g_1 - g_4$) with the corresponding PWM signals from the MCU ($s_1 - s_4$). A digital PI controller (C_{PI}) drives the sensed output voltage (V_{o}) to the reference value ($V_{\mathrm{o}}{}^*$) by adjusting the period of the MCU timer to trigger $s_1 - s_4$. When the control variable (u) has a lower value than the minimum user-defined switching period (per), the control leaves continuous conduction mode (CCM, Fig. 5.5(b)) and enters discontinuous conduction mode (DCM, Fig. 5.5(c)), where the frequency is now fixed and a phase shift between s_1/s_2 and s_3/s_4 is introduced. This simple control scheme achieves the wide-input-voltage range and complete ZVS with only an isolated low-voltage measurement, a 12 V-to-3.3 V auxiliary supply, a hardware-implemented dead-time generator, and the 32-pin ST Arm Cortex M4 as the MCU.

5.2.2 PCB-Integrated Transformer

With the topology, control techniques, and gain range determined, the passive components need to be designed next. With 125 A at the 12 V output and the automated manufacturing requirement for full PCB integration, the multi-output transformer requires an ultra-low AC-to-DC resistance ratio ($R_{\mathrm{ac}}/R_{\mathrm{dc}}$), high copper area within the constraints of the PCB geometry, and a tight, compact layout with the synchronous rectifier. The multi-output matrix transformer approach for high-current, low-voltage outputs is known from server power supplies (e.g., [32]), but does not achieve ideal flux balancing among multiple paralleled outputs [94,96]. Accordingly, the novel snake-core transformer concept introduced in Chapter 3 is utilized for implementing a compact, low-loss and balanced transformer that achieves perfect current sharing among one or many modules (as showcased later in Chapter 6).

Any multi-output transformer, including the snake-core transformer, with four sub-transformers (see Fig. 5.1) benefits more from the PCB integration if built with side symmetry, i.e., in a squared shape, as already assumed in Fig. 5.3. This allows compactness of PCB windings and the shortest path for the magnetic flux (lower core losses). The transformer's side length and

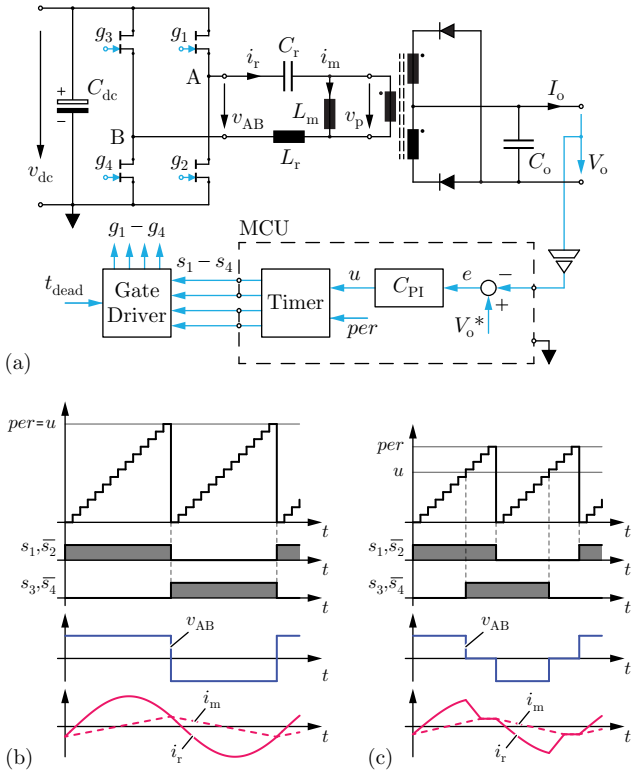

Fig. 5.5: (a) Proposed control topology for the DC/DC converter, with output-voltage regulation by variable frequency using only an isolated low-voltage measurement and a low-cost, 32-pin ST Arm Cortex M4 as the MCU. (b) Continuous conduction mode (CCM) operation, where the digital PI controller adjusts the period of the MCU timer to trigger $s_1 - s_4$. (c) When the control variable (u) is lower than the minimum (user-defined) switching period (per), the converter enters discontinuous conduction mode (DCM), with a fixed frequency and a variable phase-shift to control the output voltage to the reference value (V_o*).

height follow the power-module dimensions w and h (see Fig. 5.3), which should by no means extrapolate the dimensions of the targeted PSU form factor (see Fig. 4.16 and find more details in Section 1.1).

Winding Optimization and Losses

Firstly, the number of turns for the secondary winding (N_s) and the number of sub-transformers in the matrix structure are optimized, recalling Section 2.2.2. With the high output current requirement, a single turn ($N_s = 1$) is selected for each secondary-side winding, with winding losses minimized against core losses, though not yet optimally balanced. Therefore, the number of sub-transformers is selected to balance the copper and core losses. Choices with an odd number of secondary windings, which would yield an asymmetrical structure, a complex core shape, or much higher core losses are not considered. 1 or 2 sub-transformers results in much higher copper losses, while 8 sub-transformers would yield a complicated core structure with high core losses. Therefore, for the particular constraints of this design—and especially around PCB integration, which limits the available copper thickness—a proper copper-to-core loss ratio is achieved with 4 sub-transformers, as shown later with experimental results. This multi-output, matrix structure with 4 paralleled outputs reduces the copper loss by a factor of 4 over a single output with the same footprint area, as the current density reduces by a factor of 2 (see Section 2.2.2 for further details). Ultimately, the optimal A_w-to-A_c ratio between winding window area and core cross-section area must be selected based on a Pareto-optimization from copper and core loss models, which are developed and detailed later in this section.

The high-current outputs must then be tightly-integrated into the remainder of the converter design. The transformer configuration, layer stackup, and secondary-side layout is detailed in Fig. 5.6 and Fig. 5.7. In Fig. 5.6, a cutaway 3-D view shows the secondary-side semiconductors directly on top of the low-voltage windings ("LV Wind") for low termination losses, an adjacent output capacitance (C_o) to minimize the commutation loop, and the full-bridge excitation input and chain through L_r to the high-voltage winding ("HV Wind"). The core configuration is shown in Fig. 5.7(a), with the losses and design detailed in the next sub-section. Fig. 5.7(b) shows the vertical stackup and Fig. 5.7(c) shows the layer-by-layer copper for the 10-layer, 2.4 mm PCB that can be fabricated using standard processes, including the low-voltage, high-current layers of TL/L2 and L9/BL, the high-voltage layers of L5/L6, and the shielding layers of L3 and L8.

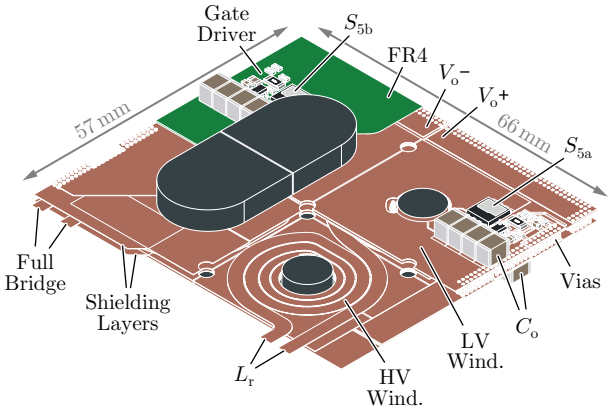

Fig. 5.6: The 3-D view of the snake-core matrix transformer with cutaway view of the PCB-integrated windings. The secondary-side semiconductors and output capacitors are placed directly above the low-voltage windings for low termination losses and minimization of commutation loops.

The shielding layers (connected to v_{dc}-) are included to minimize the capacitance between the high-voltage and low-voltage sides of the transformer and to confine the full-bridge high-frequency noise within the DC/DC-converter circuit. These shielding layers, however, add common-mode capacitance that appears between the high-voltage excitation and high-voltage ground, or, analysing the AC-equivalent circuit of Fig. 5.8, add to the C_{oss} of the high-voltage switches. In order to reduce this undesired parasitic capacitance, layers L4 and L7 have been removed from the transformer's layout (see the schematic representation in Fig. 5.8), increasing the distance (d) between L5/L6 and L3/L8 and therefore reducing $C_{pri\text{-}shi}$ according to:

$$C_{pri\text{-}shi} = 2\epsilon_r\epsilon_0\frac{A}{d}, \tag{5.1}$$

with ϵ_0 being the air permittivity. From the winding area (A) and the relative permittivity of FR4 ($\epsilon_r = 4.5$), we calculate $C_{pri\text{-}shi} = 550\,\text{pF}$ and measure $C_{pri\text{-}shi} = 554\,\text{pF}$ (with the bridge-legs shorted together, measured to high-voltage ground). Despite the removal of layers L4/L7, this is still a significant contribution to the C_{oss} of the selected high-voltage GaN switches and must be included in the ZVS and loss analyses.

The primary-side winding is then designed with the configuration shown in Fig. 5.7(c), with high-voltage windings around each core leg for high cou-

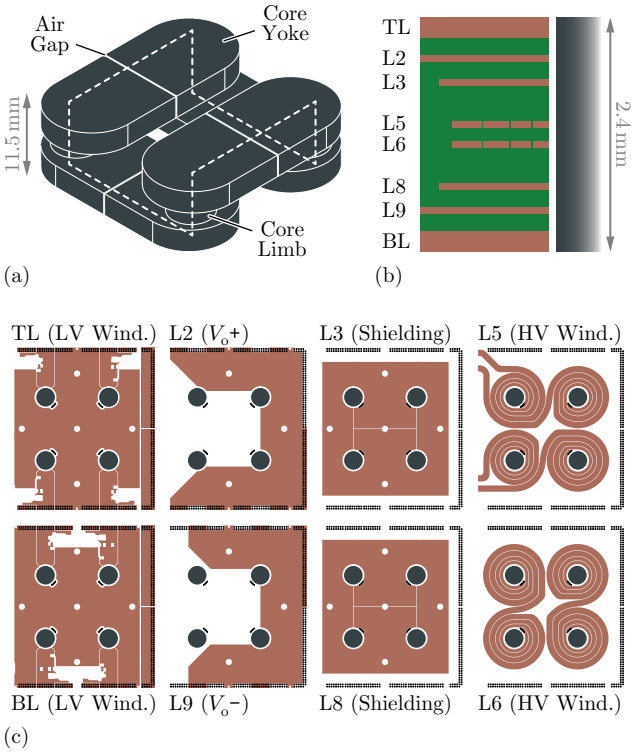

Fig. 5.7: (a) Snake core with the single path for magnetic flux highlighted with white dashed lines. (b) PCB layer stackup from the top (TL) to bottom layer (BL), with copper and isolation thicknesses proportional to the final design. (c) Layer-by-layer copper of the 10-layer layout, with layers L4/L7 empty to reduce parasitic capacitance.

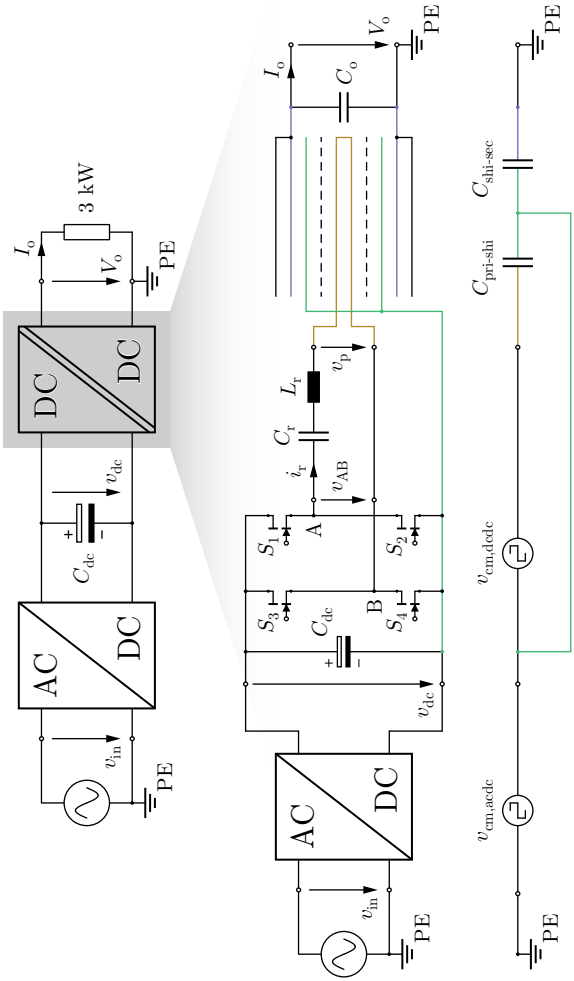

Fig. 5.8: Schematic representation of the DC/DC converter with special emphasis to the transformer's layer stackup for identifying key parasitic capacitances and deriving an AC-equivalent common-mode circuit. Two PCB layers (L4/L7) from the 10-layer design were removed to reduce $C_{\text{pri-shi}}$ and avoid further increase of the switches' C_{oss} parasitic capacitance.

pling and a balanced flux (design detailed in Chapter 3 [94]). The total DC resistance of each multi-turn winding is:

$$R = \frac{2\pi}{\sigma_{\mathrm{Cu}} h_{\mathrm{Cu}}} \sum_{i=0}^{k-1} \frac{1}{\ln\left(\frac{r_{\mathrm{i+1}}}{r_{\mathrm{i}}}\right)}, \tag{5.2}$$

with the optimal turn radii (see Fig. 5.9(a)), adapted from [32]) as:

$$r_{\mathrm{i}} = \sqrt[k]{r_0^{\mathrm{k-i}} r_{\mathrm{k}}^{\mathrm{i}}}, \tag{5.3}$$

where k is the number of turns per layer and per sub-transformer in the matrix structure. This optimized design is implemented for the high-voltage side windings to achieve the turns ratio (with $N_{\mathrm{s}} = 1$) of $n = 32$ selected in Section 5.2.1, which leads to $k = 4$: 32 turns implemented in 2 PCB layers and wound around the 4 core limbs (4 sub-transformers, $T_1 - T_4$ in Fig. 5.1).

With the winding a critical driver of efficiency and losses, a test setup is built to validate the spiral radii optimization and expected winding resistances. An impedance analyzer in the circuit of Fig. 5.9(c) measures the transformer impedance (Z_{p}) across frequency from the primary-side terminals with short-circuited secondary-side windings for two layer configurations: (i) both primary (HV) and secondary-side (LV) windings are built with the standard 2 oz copper thickness of 70 µm and (ii) 270 µm LV windings for reduced conduction losses. The results (shown as AC-to-DC resistance ratio) are reported in Fig. 5.9(b), with the theoretical approach well-validated by the experimental results. The measured $R_{\mathrm{ac}}/R_{\mathrm{dc}}$ values across frequency are modeled by empirical linear functions (dashed lines) for later use in the winding resistance calculation.

With this same test setup, the calculated resistances of the primary and secondary windings are compared to the measured values in Tab. 5.1. Across the complete operating range of frequency, the predicted current-weighted sum of the primary and secondary resistance ($R_{\mathrm{prim}}+n^2 R_{\mathrm{sec}}$) is within 2 % of the measured value, indicating precise loss models for the windings that correctly describe the implemented PCB-integrated transformer and the frequency-dependent effects. The resistance of layers L2 and L9—that connect all sub-transformers in parallel (see Fig. 5.7(c))—was obtained by FEM simulations with an error between measured and FEM-calculated values under 2 % (cf. Tab. 5.1). With the winding optimized and the loss model validated, the transformer core design and loss optimization comes next.

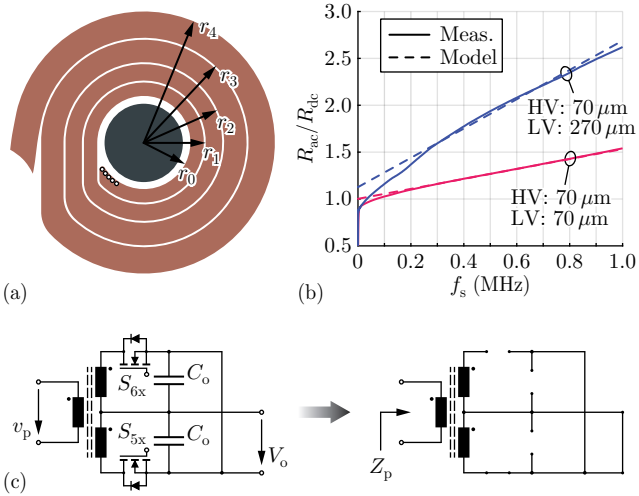

Fig. 5.9: (a) Radii calculated from (5.3) for minimizing winding resistance. (b) Transformer AC-to-DC resistance ratio across frequency—measured as shown in (c)—with secondary-side short-circuited for two copper-thickness arrangements: 70 µm primary (HV) and 70 µm secondary-side (LV) windings, or 70 µm HV and 270 µm LV windings (with 0.2 mm copper foils soldered onto the 70 µm LV windings for experimental results). (c) Measurement technique for transformer resistance measurements, with measurement opens and shorts highlighted at right.

Tab. 5.1: Comparison between predicted and measured winding losses for the PCB-integrated transformer. Copper-thickness arrangement: 70 µm primary (HV) and 270 µm secondary (LV) windings with 10 % tolerance. All parameters at $T = 25$ °C.

	Freq. (kHz)	$R_{\mathbf{calc}}$ **(mΩ)**	$R_{\mathbf{meas}}$ **(mΩ)**	**Error (%)**
R_{prim}	DC	244.2	256.5	−4.8
R_{sec}	DC	0.2085	0.2166	−3.7
$R_{\text{prim}} + n^2 R_{\text{sec}}$	300	755.2	758.0	−0.4
$R_{\text{prim}} + n^2 R_{\text{sec}}$	500	892.5	906.6	−1.6
$R_{\text{prim}} + n^2 R_{\text{sec}}$	700	1030	1027	0.3
$R_{\text{L2+L9}}$	DC	0.03622	0.03554	1.9

Core Optimization and Losses

The matrix transformer is implemented with the snake-core proposed in Chapter 3, where the winding configuration—with a single, deterministic flux path through the high-permeability ferrite (TDK N49)—guarantees well-balanced flux among the paralleled secondary windings. The core configuration is shown in Fig. 5.7(a), with cylindrical through-PCB limbs to avoid current crowding on windings due to sharp edges, low-profile yokes following components' height, and total required air gap distributed among core yokes, calculated as:

$$l_g = \frac{\mu_o A_{c,yoke}}{n^2 L_m}. \tag{5.4}$$

The core is built with different cross-sectional areas for the yokes and for the through-PCB limbs (see Tab. 5.2), with $A_{c,limb}$ selected to optimize core and winding losses for a fixed total transformer area (A_t)—Pareto optimization shown later in this section—and $A_{c,yoke}$ made as large as the combination of A_t and the specified converter height would allow. We recall that $L_m = 110\,\mu H$ and $n = 32$ were selected in Section 5.2 to meet the gain and voltage range specifications, yielding a total air gap of $l_g = 0.83\,mm$.

Tab. 5.2: Design characteristics of the optimized transformer and inductor.

	Transformer	**Inductor**
Winding width	8.6 mm	2.2 mm
Limb area ($A_{c,limb}$)	48 mm^2	36 mm^2
Yoke area* ($A_{c,yoke}$)	71 mm^2	149 mm^2
Air-gap length (l_g)	0.83 mm	0.33 mm

*at the air gap

Eddy-current losses and hysteresis losses are included in the core loss model. The flux density in the transformer core at a given operating point is given by (2.2), with the yoke and limb flux densities considered separately as their cross-sectional areas are different (see Tab. 5.2), resulting in $B_{limb} = 196\,mT$ and $B_{yoke} = 143\,mT$. The losses in each piece of the snake core are then summed for the total core losses. With the flux density known, the eddy current losses are then:

$$P_{eddy} = V_c \frac{\pi f_s^2 \hat{B}^2 A_c}{4\rho}, \tag{5.5}$$

with $\rho = 17\,\mathrm{m}\,\Omega$ being the N49-ferrite resistivity, and V_c the volume of each transformer piece. Hysteresis loss (P_hyst) also scales with V_c and is modeled as a function (P_v) of frequency (f_s), flux density ($\hat{B}$) and temperature (T):

$$P_\mathrm{hyst} = V_\mathrm{c} P_\mathrm{v} \tag{5.6}$$

$$P_\mathrm{v} = f(f_\mathrm{s}, \hat{B}, T) \tag{5.7}$$

based on the manufacturer's loss data (see Fig. 5.10). Although the flux is triangular, modeling the hysteresis loss from a sinusoidal excitation is used as a reasonable and simplifying approximation [100, 101].

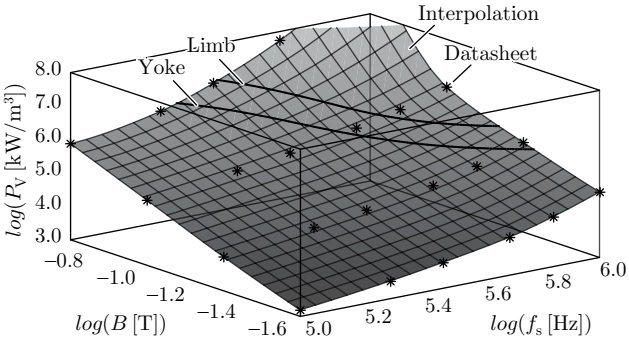

Fig. 5.10: N49-ferrite hysteresis losses (volumetric) as a function of flux density and frequency (axes in log scale). Stars are datasheet-given values, which are interpolated as inputs into continuous loss models. The frequency-dependent limb and yoke fluxes are calculated using (2.2) and shown with black lines on the top of the interpolation surface, indicating that core losses will decrease at higher operating frequencies due to the lower flux density.

To validate the model and the manufacturer's measurements, measured core losses with varying flux amplitude are recorded in a calorimetric chamber fixed at 35 ℃ using the methodology outlined in [102] (which has a maximum loss error of less than 0.5 W). The chamber—or ambient—temperature vary from application to application (can be even cooler in data-center racks with air-conditioning or water cooling), so the key metric considered here is the temperature on the core's surface, monitored to correctly calculate losses using the derived models. The comparison is detailed in Tab. 5.3, with the measurements matching the calculation within 10 % across all measured operating points. With the core loss model validated, a Pareto optimization between transformer footprint area and losses is performed next.

Tab. 5.3: Comparison between predicted and calorimetrically-measured core losses for the PCB-integrated transformer.

	#1	**#2**	**#3**	**#4**
$B_{\mathbf{limb}}$ (T)	0.156	0.166	0.176	0.149
$B_{\mathbf{yoke}}$ (T)	0.113	0.121	0.129	0.148
$T_{\mathbf{core}}$ (°C)	85.9	92.4	103	105
$P_{\mathbf{hyst,limb,calc}}$ (W)	1.01	1.64	2.77	1.73
$P_{\mathbf{hyst,yoke,calc}}$ (W)	3.99	5.67	8.99	17.1
$P_{\mathbf{eddy,limb,calc}}$ (W)	0.0033	0.0038	0.0043	0.0057
$P_{\mathbf{eddy,yoke,calc}}$ (W)	0.0344	0.0391	0.0442	0.0581
$P_{\mathbf{total,calc}}$ (W)	5.04	7.45	11.8	18.9
$P_{\mathbf{total,meas}}$ (W)	4.61	6.91	10.7	17.5
Error (%)	9.3	7.8	10.3	8.0

Pareto Optimization

For the transformer shape of Fig. 5.3, the total footprint area can be increased or decreased with an associated improvement or penalty on losses. Further, the area allocated to copper and magnetic core trades off winding and core losses, and a Pareto optimization is performed to select the loss-optimal design for each candidate footprint. The core design tradeoff between total transformer losses and footprint area is shown in Fig. 5.11(a) for nominal load and Fig. 5.11(b) for 50 % load. The designs that form the Pareto front shift materially between the two load conditions, with the selected design (footprint area of 26.4 cm^2 and full load losses of 29.2 W) representing a Pareto-optimal design at full load and a sub-optimal design at 50 % load. This indicates that the transformer design is one knob that can be tweaked to optimize for efficiency at different load conditions. Here we proceed with the Pareto-optimal design at the nominal load condition—as the whole system was designed considering full-load metrics as a first (conservative) design constraint—with the selected design marked in Fig. 5.11(a,b) and detailed in Tab. 5.2. Later in this chapter, though, it is shown that selecting the optimal transformer at 50 % load improves losses at light load and changes the shape of the efficiency curve.

The implemented core and copper layers for the PCB-integrated, snake-core transformer are shown in Fig. 5.7(a,c), respectively. With the transformer

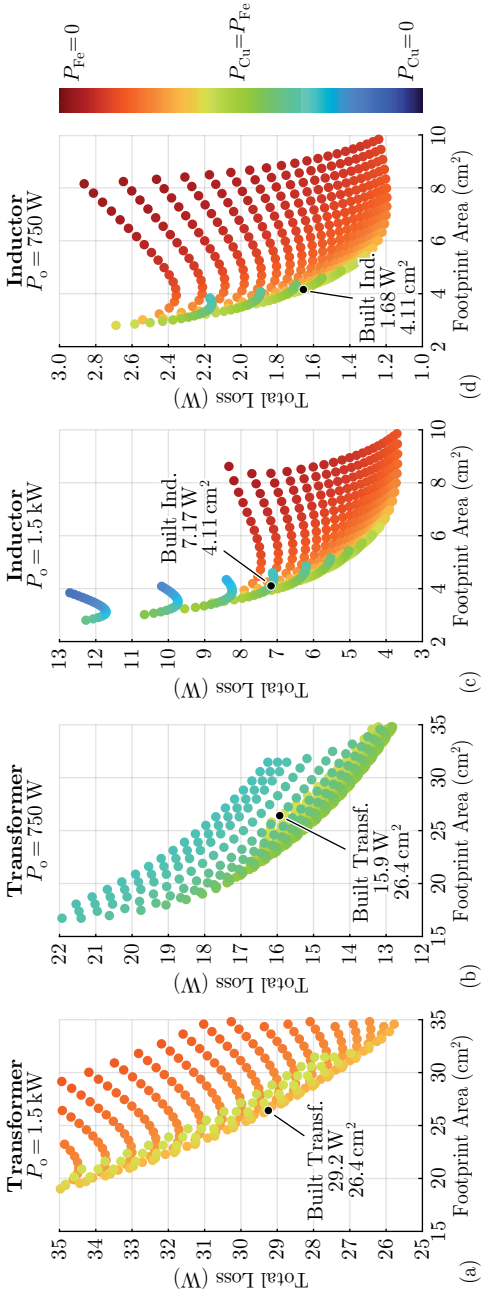

Fig. 5.11: Pareto optimizations between total loss—sum of copper (P_{Cu}) and core (P_{Fe}) losses—and footprint area (directly related to volume) of the PCB-integrated (a,b) transformer and (c,d) inductor for (a,c) nominal and (b,d) 50 % load. The design spaces were defined by sweeping core radius and winding width values for each of the two components to tradeoff the winding and core area. Selected designs that were Pareto-optimized for nominal load (P_o = 1.5 kW) are shown as black dots, with the design characteristics of Tab. 5.2. Note that the Pareto-optimal designs are constant between full and 50 % load for the inductor but change significantly for the transformer, as transformer core losses are load independent.

loss models proposed and validated, the design and loss modeling for the PCB-integrated resonant inductor (L_r) is discussed next.

5.2.3 PCB-Integrated Inductor

Much like the transformer designed, optimized, and characterized in Section 5.2.2, the primary-side inductor must be PCB-integrated for compactness, manufacturability, and cost-effectiveness—but this comes with the penalty of increased losses relative to litz-wire inductors in the desired frequency range (100 kHz–1 MHz) [103]. This integration penalty—which is based on the lower fill factor, worse copper utilization (R_{ac}/R_{dc} ratio), and other geometric constraints of PCBs relative to litz wire—can be mitigated through the compensating fringing-field concept (CFFC) introduced in [87], where skin and proximity effects in a PCB-based inductor are minimized by using the otherwise-parasitic fringing fields caused by the air gap in the magnetic core.

The loss models detailed in this section for the transformer can be reused and combined with the fringing-field effects of [87] to arrive at the complete winding and core losses for the primary-side inductor, which is then Pareto-optimized for the selected value of $L_r = 24\,\mu H$ (driven by the desired gain ratio, as discussed in Section 5.2.1) between footprint area (directly related to volume) and total inductor losses. This optimization is shown in Fig. 5.11(c) for nominal load and Fig. 5.11(d) for 50 % load, where it turns out that, unlike the PCB-integrated transformer, the Pareto-front analysis is load-independent, with the map merely shifted down on the loss axis between nominal load and 50 % load. A footprint area of $4.11\,cm^2$ is selected for a primary-side inductor loss of 7.2 W at full load and 1.7 W at 50 % load. This selection represents a good tradeoff between inductor footprint area and full-load losses—with enough space left for primary-side components and control circuitry (see Fig. 5.3), and the inductor already contributing to 12 % of total losses for a hypothetical full-load efficiency of 96 %.

The complete inductor, as implemented, is shown in Fig. 5.12(a), with a final footprint area slightly larger than the one Pareto-optimized to accommodate thermal interfaces [87]. Fig. 5.12(b) shows the implemented layer-by-layer copper of the 10-layer PCB design. The selected design is marked in Fig. 5.11(c,d) and detailed in Tab. 5.2.

It should be noted that some LLC converters utilize the leakage inductance of the transformer as the auxiliary inductance, but this approach (i) is not feasible with the required inductance of 24 µH and a PCB-integrated transformer, which has very high coupling (and accordingly low leakage

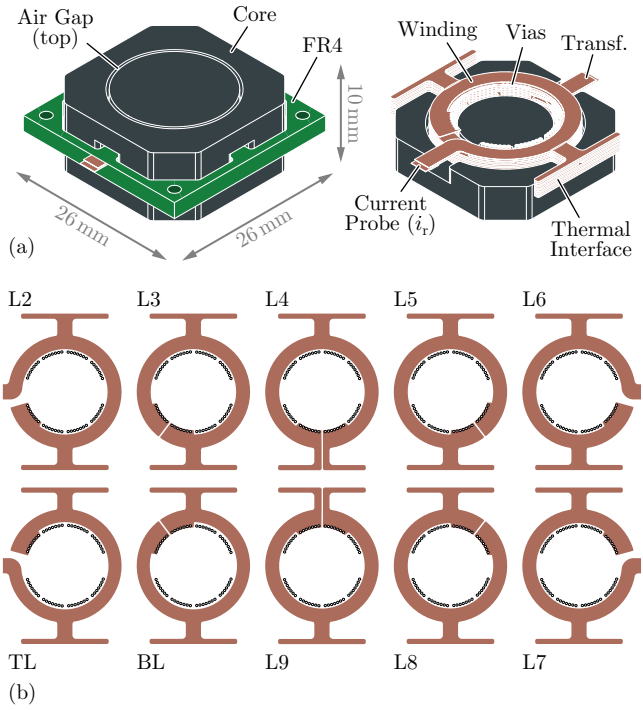

Fig. 5.12: (a) The 3-D view of the primary-side inductor (L_r) with PCB-integrated windings schematically shown with cutaways. Winding heat is transferred by thermal interfaces to adjacent surfaces that can be thermally coupled to heat sinks for cooling. Following [87], air gaps are strategically placed above and underneath the windings to improve current distribution and boost efficiency. (b) Layer-by-layer copper of the 10-layer stackup.

inductance), (ii) would make the benefits of the fringing-field approach [87] difficult to achieve, and (iii) prevents the Pareto-optimization of the resonant inductor alone, leading to higher losses.

5.2.4 Capacitor and Power-Semiconductor Selection

With the control, topology, and PCB-integrated magnetics designs finalized, the selection of the input, resonant, and output capacitors and the primary- and secondary-side power semiconductors follows. The loss contributions to the detailed model are outlined in the power semiconductor sections, while calculations indicate that the losses from all of the capacitors are negligible.

Output Capacitor Selection

With four secondary-side sub-transformers and two windings per sub-transformer, the sheer quantity of output capacitors (eight groups) make their selection critical to the design of the converter. An analytical solution may be derived for the voltage ripple specification based on the converter parameters and the required output capacitance, as:

$$\Delta v_\mathrm{o} = \frac{P_\mathrm{o}}{C_\mathrm{o} V_\mathrm{o}} \left\{ \frac{1}{2 f_\mathrm{s}} \cos\left[\sin^{-1}\left(\frac{2 f_\mathrm{s}}{\pi f_\mathrm{r}} \right) \right] + \frac{1}{\pi f_\mathrm{r}} \sin^{-1}\left(\frac{2 f_\mathrm{s}}{\pi f_\mathrm{r}} \right) - \frac{1}{2 f_\mathrm{r}} \right\}. \tag{5.8}$$

With the output ripple specified as under 2 % in the worst-case, a total output capacitance of 640 µF is selected, implemented as $4x$ 20 µF capacitors per group (*C4532X7R1C336M250KC* @ 12 V). This gives a worst-case full-power ripple of $\Delta v_\mathrm{o} = 194\,\mathrm{mV}$ ($f_\mathrm{s} = 210\,\mathrm{kHz}$, $v_\mathrm{dc} = 300\,\mathrm{V}$, $P_\mathrm{o} = 1.5\,\mathrm{kW}$) and a ripple of $\Delta v_\mathrm{o} = 66.3\,\mathrm{mV}$ at nominal operation ($f_\mathrm{s} = 310\,\mathrm{kHz}$, $v_\mathrm{dc} = 400\,\mathrm{V}$, $P_\mathrm{o} = 1.5\,\mathrm{kW}$).

Input Capacitor Selection

No analytical solution for calculating the input voltage ripple exists (the equation is transcendental), so the input capacitor value is selected from circuit simulations as $C_\mathrm{dc} = 1\,\mu\mathrm{F}$. Four capacitors, each with $C_\mathrm{dc} = 0.28\,\mu\mathrm{F}$ at 400 V, are selected to achieve this capacitance (*C5750X7T2W105K250KA*).

Resonant Capacitor Selection

As detailed in Section 5.2.1, the resonant capacitance is selected as $C_\mathrm{r} = 11\,\mathrm{nF}$ from the gain analysis. The resonant capacitor is implemented as 5 paralleled C0G capacitors, each contributing 2.2 nF (*CGA4F4C0G2W222J085AA*).

Primary-Side Semiconductors

The high-voltage power semiconductors must block up to the maximum input voltage of $v_{dc} = 430\,V$, and incur losses from conduction, resonant soft-switching, body-diode conduction, and gating, with the hard-switching contributions of Q_{oss} and VI overlap eliminated by achieving ZVS across the complete load and voltage ranges and by a fast-turn-off gate drive. To minimize the remaining loss contributions, the 600 V GaN HEMT *IGLD60R070D1* are selected, with 70 mΩ nominal on-resistance and, like all GaN HEMTs, zero reverse-recovery losses. For the primary-side semiconductor modeling, the junction temperature is estimated based on load condition, with a linear spacing between 60 °C (full load) and 40 °C (10 % load). From here, the losses are straightforwardly calculated and the breakdown is reported later in this chapter. *UCC21225A* gate drivers are used with bootstrap power supplies, common-mode chokes to reduce noise on these supplies, and a series capacitor to introduce a negative gate drive voltage.

Secondary-Side Semiconductors

The low-voltage switching stage incurs high currents and therefore must rectify synchronously, underscoring its importance to the total losses of the converter. The devices must withstand $2V_o = 24\,V$; accordingly, the 40 V Si MOSFET *TPW48004PL* is selected, with a nominal on-resistance of 0.65 mΩ. The semiconductor junction temperature is again modeled based on load condition, with a linear spacing between 90 °C (full load) and 50 °C (10 % load). As will be analyzed in depth when searching for further improvements later in this chapter, minimizing the delay of the synchronous turn-on is critical to minimizing secondary-side losses, and a dedicated synchronous rectifier IC (*NCP4306*) is used to drive the MOSFETs based on a direct v_{ds} measurement. This stage is supplied by the output voltage to fully decouple the primary and secondary sides of the converter. Again, these MOSFETs are operated under ZVS and ZCS (a natural condition of synchronous rectification) and therefore only incur conduction, body-diode, and gating losses, the contributions of which are detailed in the next section.

5.3 Hardware Prototype

The design detailed in Section 5.2 is fabricated as a 1.5 kW hardware demonstrator, and is shown in Fig. 5.13(a) with the summary of the final design values and implementations given in Tab. 5.4. The DC/DC converter measures 96 mm

Tab. 5.4: Key design values and implementation for components in the 1.5 kW hardware demonstrator of Fig. 5.13.

Parameter	Design Value	Implementation
$S_{1\text{-}4}$	—	600 V, 70 mΩ GaN HEMT *IGLD60R070D1*
$S_{1\text{-}4}$ gate drivers	—	*UCC21225A*, bootstrap
$S_{5,6}$	—	40 V, 0.65 mΩ Si MOSFET *TPW48004PL*
$S_{5,6}$ gate drivers	—	*NCP4306* and *UCC27511A*, $v_{\text{gate}} = 6\,\text{V}$
L_r	24 µH	PCB-integrated, CFFC [87]
C_dc	1 µF	4× 0.28 µF *C5750X7T2W105K250KA*
C_out	640 µF	32× 20 µF *C4532X7R1C336M250KC*
C_r	11 nF	5× 2.2 nF *CGA4F4C0G2W222J085AA*

by 66 mm by 11.5 mm, with the high-voltage switching cell highlighted in the top-right of Fig. 5.13(a), the snake-core transformer in the center of the converter, and the high-current, low-voltage output to V_o in the bottom-left. This converter includes the detailed layouts of the PCB snake-core transformer (Fig. 5.7(c)) and the PCB inductor L_r (Fig. 5.12(b)), and is virtually placed inside the PSU case according to Fig. 5.13(b).

Key operating waveforms are captured at nominal (Fig. 5.14) and 50 % (Fig. 5.15) load, indicating correct operation of both the high-voltage and low-voltage sides of the converter for a well-regulated output voltage of $V_\text{o} = 12\,\text{V}$. These measured waveforms show excellent agreement with circuit-simulation results, validating the model that is used as a waveform generator for the loss models. The selected control scheme maintains sinusoidal currents through the resonant network (shown with the i_r waveform captures) to minimize harmonic losses and simplify the frequency-dependent effects in the design, and soft-switching is achieved across the entire load range. The synchronous rectifier gate driver signals are shown in the bottom pane (g_5, g_6), where the correct operation of the circuit with a simple zero-crossing detector—but an unmistakable (albeit short) time at the end of each conduction cycle (see the third pane, $v_{\text{s},5}$ and $v_{\text{s},6}$) where the paralleled body-diodes conduct rather than the MOSFETs is verified. The effect of this timing mismatch sets a loss minimum for the high-current rectification, the effects of which are investigated more deeply in the next section.

The measured DC/DC efficiency, from $v_\text{dc} = 300\,\text{V}$ and $v_\text{dc} = 400\,\text{V}$ to $V_\text{o} = 12\,\text{V}$, for the hardware demonstrator across output power is shown in

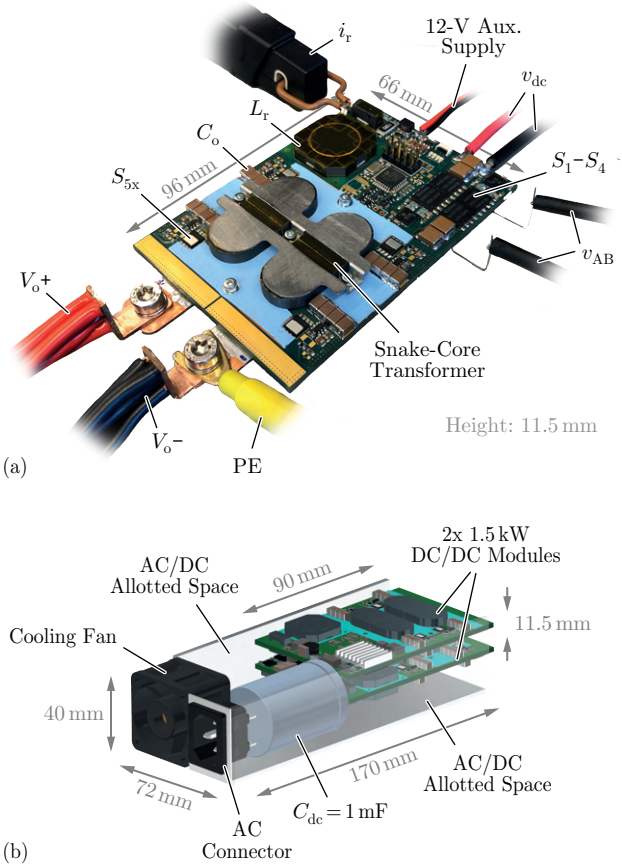

Fig. 5.13: (a) The 1.5 kW hardware demonstrator of the DC/DC resonant converter, measuring 96 mm × 66 mm × 11.5 mm. Key components and measurement devices are highlighted, with key values and implementations given in Tab. 5.4. (b) Virtual placement of two 1.5 kW modules inside the PSU case as previously proposed in Fig. 4.16 (check Section 1.1 for details on the PSU volume partitioning).

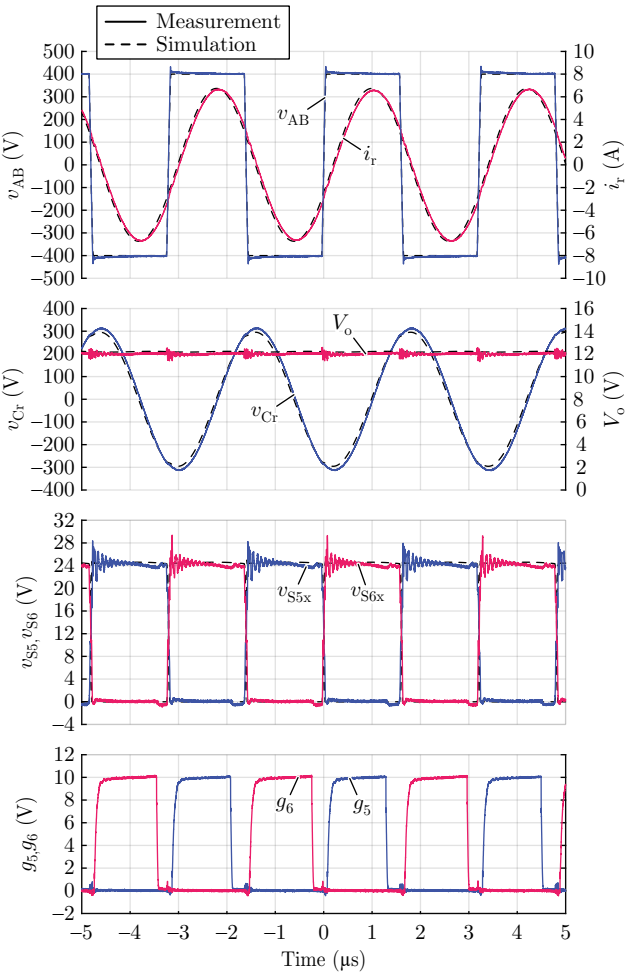

Fig. 5.14: Key operating waveforms captured at *nominal load*, demonstrating good agreement with circuit-simulation data (shown as dashed lines). Output voltage (V_o) is regulated at 12 V by controlling the switching frequency of v_{AB}. The sinusoidal shape of i_r minimizes harmonic losses, and synchronous rectification supports both ZVS and ZCS of the LV-side switches (drain-to-source voltages v_{S5x}/v_{S6x} commute naturally at zero current) and reduces body-diode losses by conducting most of the current through the MOSFET channel (gate signals g_5/g_6 are commanded after and before switching actions).

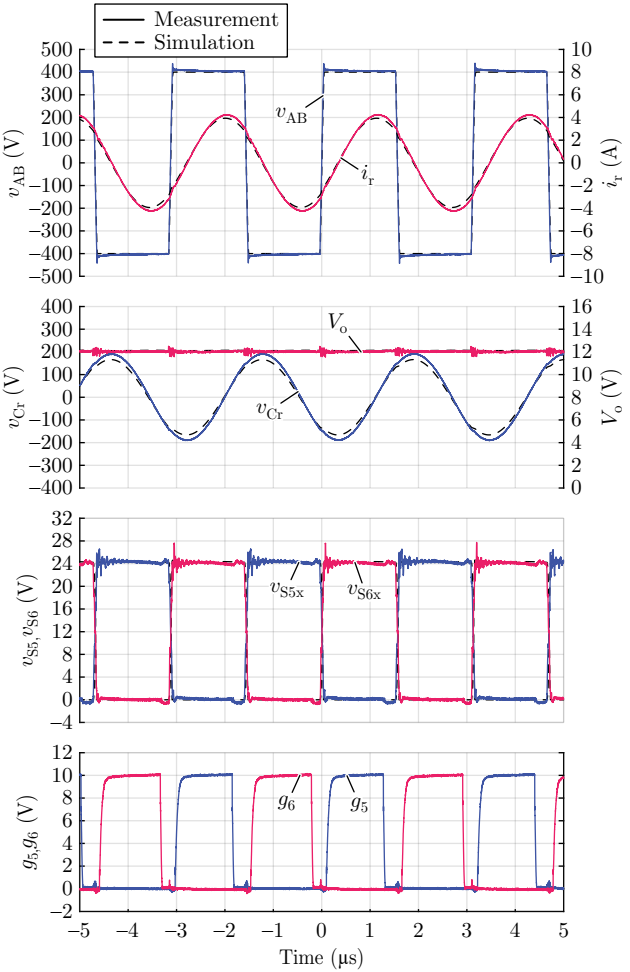

Fig. 5.15: Key operating waveforms captured at 50 % *load*, demonstrating good agreement with circuit-simulation data (shown as dashed lines). Output voltage (V_o) is regulated at 12 V by controlling the switching frequency of v_{AB}. The sinusoidal shape of i_r minimizes harmonic losses, and synchronous rectification supports both ZVS and ZCS of the LV-side switches (drain-to-source voltages v_{S5x}/v_{S6x} commute naturally at zero current) and reduces body-diode losses by conducting most of the current through the MOSFET channel (gate signals g_5/g_6 are commanded after and before switching actions).

Fig. 5.16. The module delivers a flat and high efficiency above around 40 % of nominal load for v_{dc} = 400 V, with a maximum just below 96 % efficiency near 1 kW of output power. The detailed loss models developed for each component in Section 5.2 predict the complete converter efficiency quite accurately, with minute differences across most of the load range and less than 5 % of the loss not captured by the model at the largest variation between calculation and measurement (at nominal load). These component-level loss models, further, support a detailed breakdown of the losses that are shown for nominal and 50 % load in Fig. 5.17.

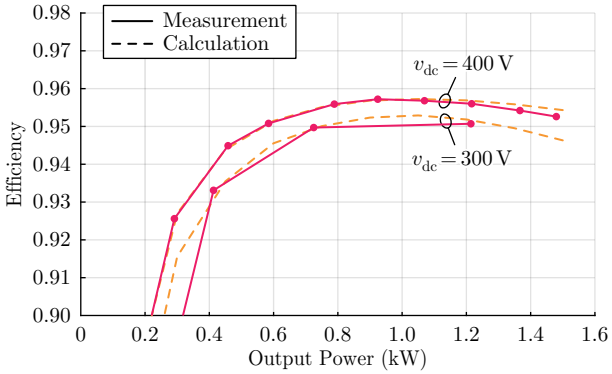

Fig. 5.16: DC/DC calculated and electrically-measured efficiencies from input (v_{dc} = 300 V, 400 V) to output (V_o = 12 V) at different load conditions, including all loss components.

At full load (Fig. 5.17(a)), the transformer accounts for over 40 % of the total losses, with the inductor, high-voltage logic, and GaN devices bringing the high-voltage losses to about 60 % of the total converter dissipation. The low-voltage loss breakdown, however, highlights the challenges of high-current outputs with high power density (and therefore high switching frequency). Firstly, the low-voltage tracks contribute 10 % of the losses alone, even with a careful design to maximize the copper and copper utilization in this path. Similarly, the synchronous rectifier diode alone accounts for 16.5 % of total converter losses, despite conducting for less than 10 % of the on-time! At high switching frequencies and high output currents, the speed of the sensing, control, and gating of the synchronous rectifier switches is a major performance driver, and the next section analyses efficiency limits as this delay decreases.

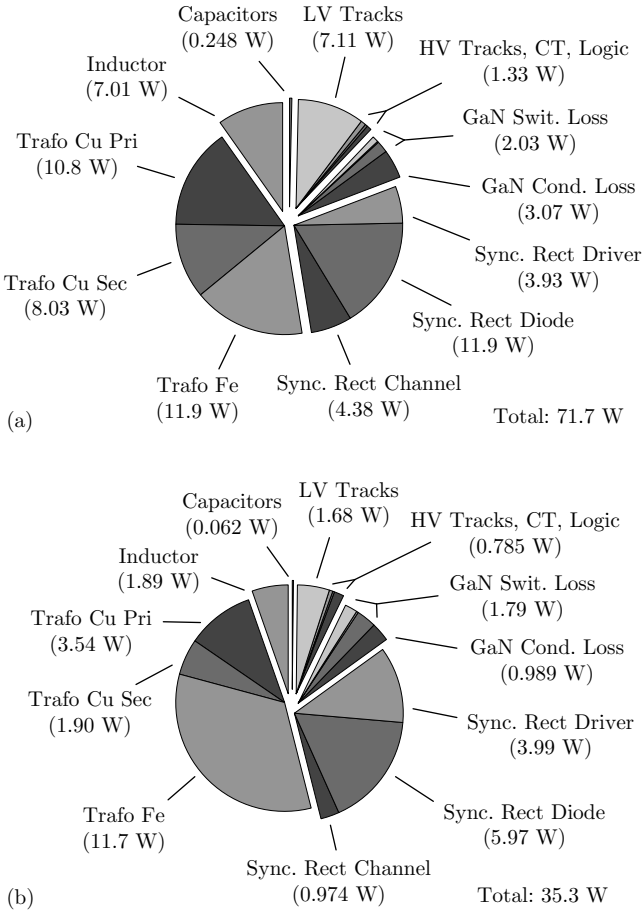

Fig. 5.17: (a) Full- and (b) 50 %-load loss budgets for the DC/DC converter with $v_{dc} = 400\,V$ and $V_o = 12\,V$. Transformer, synchronous rectifiers and HV-side components/PCB tracks represent the three groups of loss contributors. Transformer losses account for 43 % and 49 % of the total losses at full and 50 % load, respectively. Synchronous rectification is the second element with highest loss, achieving nearly 30 % of the total losses in both load conditions.

At 50 % load (Fig. 5.17(b)), as expected, the current-independent (or nearly current-independent) losses represent a larger fraction of the total loss budget, including the transformer core losses (1/3 of total losses), the GaN switching losses, and the synchronous rectifier gating losses. The synchronous rectifier diode losses remain at around 1/6 of the total losses, with these VI losses simply related to the ratio of the forward drop to the output voltage and the percent of the period in which the diode conducts.

A thermal image of the converter at nominal load and nearly steady-state is shown in Fig. 5.18. A small fan was used to blow air on the surface of the converter (air speed of approximately 1 m/s) and keep the temperature within limits. The high-current output results in a relatively-hot low-voltage side of the converter—with losses from the transformer winding, transformer core, low-voltage tracks, and synchronous rectifier—but the maximum temperature remains below 71 °C. The hottest components are the gate drivers for the synchronous rectifier switches, which each dissipates around 0.5 W in a small package that is located in a hot environment. In a commercial application, heat sinks should be installed to conduct heat from the hot surfaces of the transformer windings either onto a cooling plate or into air.

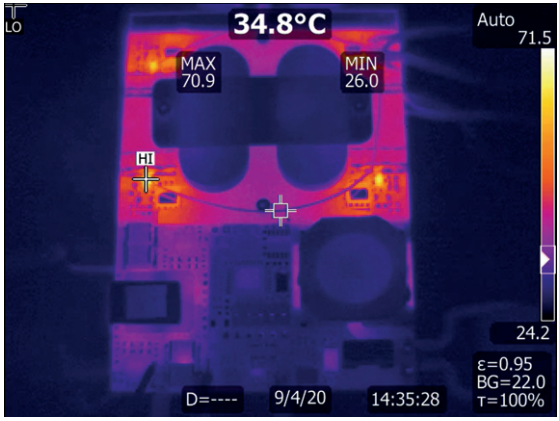

Fig. 5.18: Thermal image of the converter at steady-state and $P_o = 1.5\,\text{kW}$ with forced cooling. The hottest component (71 °C) is the gate driver for the synchronous rectifier switches, which each dissipate around 0.5 W.

In this section, simplified control techniques, novel PCB-integrated passive components, and detailed loss optimizations were combined to showcase an

efficient, power-dense, and wide-input-voltage-range DC/DC converter for industrial power supplies with stringent hold-up time and manufacturability requirements. This module achieves a flat efficiency curve with a peak of nearly 96 % and a power density of 337 $\mathrm{W/in^3}$ with (i) only PCB-integrated magnetic components, (ii) soft-switching across the entirety of the operating envelope, and (iii) a wide-input-voltage range that achieves the hold-up time requirements while minimizing the volume of the DC-link bulk capacitor. However, the detailed loss models developed in this section and the converter's loss budgets reveal that losses can be still reduced, especially that from the transformer core and synchronous rectifiers. These loss improvements will be explored in the next section, and the most significant efficiency barriers of the hardware will be identified.

5.4 Efficiency Barriers

The detailed loss models derived in the previous section permit component- and converter-level optimizations, and these extensive models are now leveraged to identify the barriers to higher efficiency that may be overcome with a next-generation module. These improvements are evaluated in two distinct categories—firstly, the operating parameters and converter design approaches, which may be optimized by the power electronics engineer, are evaluated. Secondly, key component advances that could improve efficiency are analyzed, improvements that will likely be considered as *inputs* to the power electronics design.

Firstly, the selections of transformer turns ratio, switching frequency, and primary-side bridge configuration are revisited. The transformer turns ratio determines the required gain range but also drives losses, as its selection defines whether the converter nominally operates near resonance or away from resonance. Fig. 5.19 confirms that $n = 32$ is the optimal choice for efficiency across load, with lower turn counts especially penalized as the load is increased through higher conduction losses. The nominal switching frequency, characterized by the tank resonant frequency, can also be optimized across load range, as shown in Fig. 5.20, where it turns out that increasing the resonant frequency to $f_\mathrm{r} = 500\,\mathrm{kHz}$ can eliminate around 10 % of the losses at 50 % load. These models, though, exclude the extra losses incurred by the non-idealities in synchronous rectification timing, when the body diode conducts, and $f_\mathrm{r} = 300\,\mathrm{kHz}$ remains the ideal nominal switching frequency when these losses are included. Finally, a half-bridge decreases the number of semiconductors relative to a full-bridge, accruing gains in both

area and number of devices in the conduction path, but the full-bridge has a more flexible control scheme (CCM and DCM operation are both possible, as shown in Fig. 5.5) and less primary-side current. The half-bridge efficiency is marginally higher at light load, as shown in Fig. 5.21, but the full-bridge outperforms on an efficiency basis above around 75 % load and improves the control scheme. In all three cases, the converter-scale improvements tap out at around 96 % peak DC/DC efficiency. Component-level improvements will therefore be explored to further push down losses.

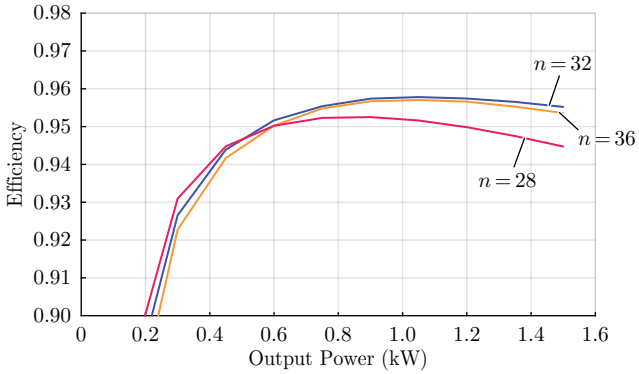

Fig. 5.19: Calculated efficiencies at $v_{dc} = 400$ V and $V_o = 12$ V, highlighting the optimal choice for turns ratio ($n = 32$).

As detailed in Fig. 5.17, the transformer and synchronous rectifier are the primary loss drivers across the load range, and are accordingly the components which first should be analyzed concerning loss reduction. Firstly, the transformer cross-sectional area can be increased in the limbs and yokes to lower the core losses at the expense of increased winding losses (with a fixed total volume). This benefit is shown in Fig. 5.22, which highlights the Pareto front for 50 % load, recalling from Fig. 5.11(b) that the selected transformer was optimized at nominal load and was sub-optimal at light load. This design change increases the peak efficiency at light load, where core losses dominate over conduction-related losses, by up to 1 %, as shown with the case labeled (i) in Fig. 5.23(a).

Even larger gains can be realized in the synchronous rectifier; replacing the low-voltage MOSFETs with the new 40 V MOSFET from Infineon, *IQE013N04LM6*, reduces the driver losses by 5×, from nearly 4 W to 0.8 W, by dropping the gate driver voltage from 12 V to 6 V with a low-drop-out

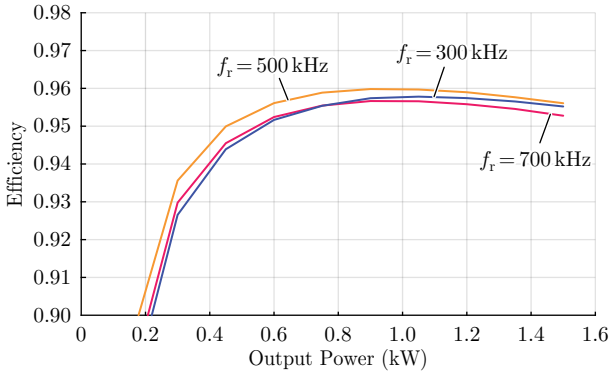

Fig. 5.20: Calculated efficiencies at $v_{dc} = 400\,\text{V}$ and $V_o = 12\,\text{V}$, highlighting the optimal choice for the resonant frequency ($f_r = 500\,\text{kHz}$). Due to the non-ideal synchronous rectification, body-diode conduction losses increase at higher frequencies (practical behavior not captured by the loss models), which actually makes $f_r = 300\,\text{kHz}$ the best choice to maximize efficiency.

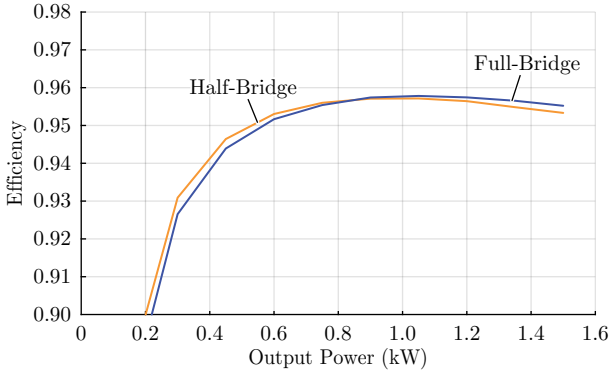

Fig. 5.21: Calculated efficiencies at $v_{dc} = 400\,\text{V}$ and $V_o = 12\,\text{V}$, highlighting that a HV half-bridge switching-stage (that prevents DCM operation) does not improve efficiency over the full-bridge, even though n is cut by half.

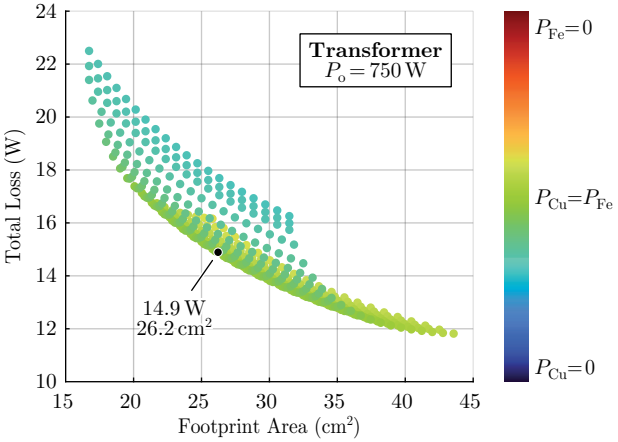

Fig. 5.22: Transformer Pareto front optimized at 50 % load by increasing limb and yoke cross-sectional areas according to case (i) of Fig. 5.23(a), which shows that 8.11 W/6.59 W of core/winding losses is optimal on Fig. 5.23(b).

regulator (LDO) and requiring a lower gating charge. The LDO efficiency is given by the output-to-input voltage ratio ($\eta = \frac{V_{gate}}{V_{drive}}$), while gate losses are calculated as the total gate charge multiplied by the gate voltage and the switching frequency ($P_{gate} = f_s C_{gate} V_{gate}^2$), both expressions leading to:

$$P_{drive} = f_s C_{gate} V_{drive} V_{gate}. \tag{5.9}$$

Thus, a reduction in driving losses is possible even for a poor 50 %-efficiency 12 V-to-6 V LDO regulation, and the improvement is shown as case (ii) in Fig. 5.23(a).

Further efficiency improvements can be achieved by reducing the conduction time of the synchronous-rectifier body diode. In synchronous rectification, the MOSFET is switched ideally with zero voltage and zero current, a condition that is typically identified by measuring the MOSFET's drain-to-source voltage (v_{ds}) with dedicated gate-driver ICs. The turn-on event is easily detected by the relatively large body-diode voltage drop that appears across the switch after a full commutation. The turn-off-event detection, however, suffers from the low v_{ds} voltage that results from the selection of low-R_{on} switches in high-output-current applications. In such cases, the drain-to-source voltage is a combination of the voltage across the on-resistance and the voltage from the parasitic inductance of the MOSFET's package (L_{ds}),

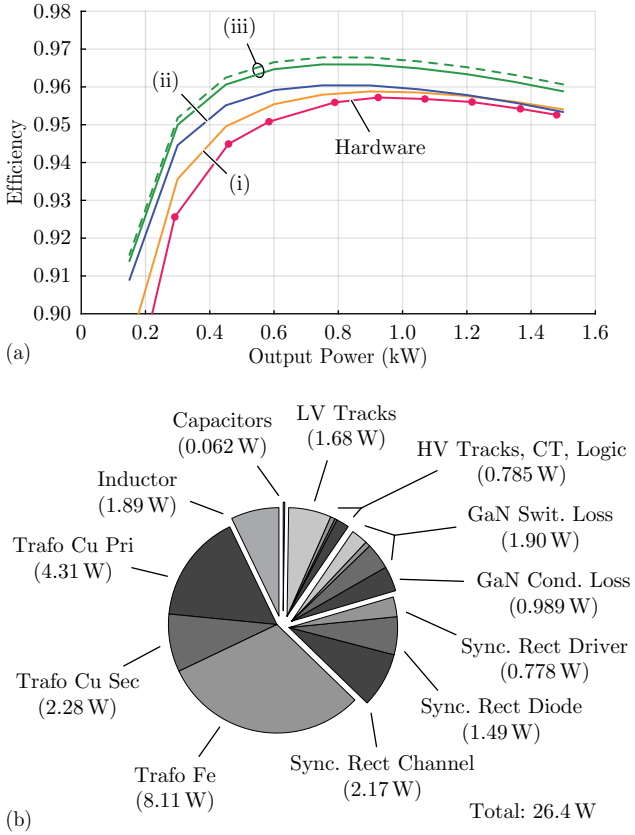

Fig. 5.23: (a) Calculated efficiencies (i,ii,iii) as result of a series of improvements for comparison with the prototype's measured efficiency ("Hardware"): (i) larger limb and yoke cross-sectional areas for reduced core losses; (ii) new LV-side switch (*IQE013N04LM6*) with lower gate charge and triggered by a lower gate voltage using an LDO (6 V instead of 12 V); and (iii) 50 % lower body-diode conduction time (dashed line shows the ideal case of no body-diode conduction). (b) Loss budget of case (iii) at 50 % load.

equated (for a sinusoidal drain current i_d) as:

$$v_\mathrm{ds} = R_\mathrm{on} i_\mathrm{d} - L_\mathrm{ds} \frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t} \tag{5.10}$$

$$= R_\mathrm{on} I_\mathrm{d,pk} \sin(2\pi f_\mathrm{s} t) - 2\pi f_\mathrm{s} t L_\mathrm{ds} I_\mathrm{d,pk} \cos(2\pi f_\mathrm{s} t). \tag{5.11}$$

The turn-off is commanded when the drain-to-source voltage reaches zero ($v_\mathrm{ds} = 0$), yielding:

$$t_\mathrm{d} = \frac{L_\mathrm{ds}}{R_\mathrm{on}}, \tag{5.12}$$

here assuming that $\tan(2\pi f_\mathrm{s} t) \approx 2\pi f_\mathrm{s} t$ for relatively low t values. This key formula shows that the turn-off event happens t_d seconds before the current reaches zero, and gets worse for larger parasitic inductances or lower on-resistances. During the time between the premature turn-off event and the actual rectifier commutation at zero current, the MOSFET body diode conducts the high output current and generates significant additional losses to the system. These losses are calculated averaging the sinusoidal current that flows through the body diodes during t_d within one switching period:

$$I_\mathrm{d,avg} = \frac{1}{T_\mathrm{s}} \int_0^{t_\mathrm{d}} I_\mathrm{d,pk} \sin(2\pi f_\mathrm{s} t)\, \mathrm{d}t = I_\mathrm{d,pk} \pi f_\mathrm{s}^2 t_\mathrm{d}^2, \tag{5.13}$$

with $\sin(2\pi f_\mathrm{s} t) \approx 2\pi f_\mathrm{s} t$. This equation combined with (B.8) leads to a formula for calculating the total body-diode losses:

$$P_\mathrm{diode} = \frac{P_\mathrm{o} V_\mathrm{diode}}{V_\mathrm{o}} (\pi f_\mathrm{s} t_\mathrm{d})^2 . \tag{5.14}$$

The formula reveals that low-output-voltage, high-frequency conversion yields higher body-diode losses; and t_d is the parameter to minimize in order to reduce these losses. Therefore, cutting this time by half pushes the efficiency—in combination with the other two improvements—over 96.5 %, as shown by case (iii) in Fig. 5.23(a). This reduction in conduction time could be achieved, for instance, by adaptive synchronous rectification that increases the MOSFET's on-time until no diode voltage drop is detected after turn-off. Close-to-ideal synchronous rectification, though, is difficult to achieve at high switching frequencies with existing discrete components; speeding the sense and actuation might require either integrated synchronous-rectifier ICs

or, at a minimum, Kelvin-source connections on high-current MOSFETs to support direct v_{ds} measurements.

The loss breakdown at 50 % load with the three proposed improvements is shown in Fig. 5.23(b), with the total losses reduced from 35.3 W (cf. Fig. 5.17(b)) to 26.4 W, driven by reductions in transformer core losses (3.6 W), synchronous-rectifier gate-driver losses (3.2 W), and synchronous-rectifier body-diode losses (4.5 W). With these key module-level improvements characterized and identified—and, indeed, improvements identified that can eliminate 26 % of the total converter losses—a design of an improved 1.5 kW module to be fabricated and experimentally characterized in the next chapter is identified. This improved demonstrator is finally combined with the snake-core transformer concept to achieve ideal current sharing with two paralleled modules for a total output power of 3 kW.

5.5 Summary

This chapter conceptualizes, analyses and demonstrates a 1.5 kW, 12 V-output DC/DC converter module for industrial applications. This converter reaches nearly 96 % peak efficiency with a power density over 300 W/in^3 (18.3 kW/dm^3) while fulfilling the application-specific requirements: complete PCB integration, soft-switching over the entire operating range, and a wide-input-voltage range from 300 V to 430 V. This demonstrator met the key requirements, but further component- and converter-level improvements were subsequently identified using the detailed loss models derived in the design optimization stage. These improvements are implemented in the next chapter, including expanding the snake-core-transformer core area and improving the synchronous rectifier speed and device selection.

6

Input-Parallel/Output-Parallel Association of LLC Resonant Converters

Chapter Abstract

This chapter demonstrates a 12 V-output, 300 V–430 V-input DC/DC power supply module that takes advantage of the the loss models and efficiency analysis developed in the last chapter to improve efficiency at all load levels. This 1.5 kW hardware prototype eliminates nearly 25 % of converter losses for a peak efficiency of nearly 97 % with a power density of 308 W/in^3 (18.8 kW/dm^3). Two 1.5 kW modules are then paralleled to achieve 3 kW output power at 12 V and 345 W/in^3 (21.1 kW/dm^3) with ideal current sharing between the secondary outputs and no drop in efficiency from a single module. The ideal current sharing is an important characteristic enabled by the snake-core transformer, and flux measurements are presented in this chapter to highlight the enhanced performance of this approach compared to state-of-the-art solutions.

6.1 Introduction

The previous chapter focused on the conceptualization, design, modelling, fabrication and characterization of a 1.5 kW, 12 V-output DC/DC converter for industrial power supplies that is required to operate across a wide 300 V–430 V input voltage range. This converter reaches nearly 96 % peak efficiency with a power density of 337 W/in^3 (20.6 kW/dm^3) and meets the key requirements of complete PCB integration and soft-switching over the entire operating range; but further component- and converter-level improvements were sub-

sequently identified using the detailed loss models derived in the design optimization stage. In this chapter, therefore, this improved hardware prototype is implemented and characterized, which includes expanding the snake-core cross-sectional area and improving the synchronous rectifier speed and device selection. Moreover, to reach the desired 3 kW output power, two 1.5 kW converter modules are connected in input-parallel/output-parallel configuration and ideal current sharing among the secondary outputs with two paralleled modules is demonstrated, a critical characteristic for high-current outputs that is uniquely enabled by the snake-core architecture.

6.2 Next-Generation DC/DC Module

Firstly, a next-generation DC/DC converter module is fabricated with the critical changes proposed in Section 5.4 to improve efficiency. The updated module includes, with references to Fig. 5.1 and a component summary in Tab. 6.1:

- New LV-side switches ($S_{5,6}$), with *IQE013N04LM6* featuring lower gate charge and driven by a 6 V gate voltage (supplied by an LDO) rather than a 12 V gate voltage;
- An updated rectifier integrated circuit (*SRK2001A*) with adaptive turn-off, which reduces the body-diode conduction time by up to 25 %; and
- Larger transformer limb (65 mm^2) and yoke (93 mm^2) cross-sectional areas (see Tab. 5.2 for previous values), which lowers core losses but also slightly reduces power density through a larger core height.

This updated converter is shown as "Module 1" in Fig. 6.1, and measures 89.5 mm × 66.0 mm × 13.5 mm, for an 8.6 % reduction in power density to 308 W/in^3. This minor reduction in power density, though, accompanies a large increase in efficiency across the load range, as shown in Fig. 6.2: at 10 % load, the efficiency increases from 87.2 % to 92.3 %, and at 50 % load, total converter losses are reduced by the predicted 26 % for an efficiency increase from 95.6 % to 96.7 % (see Fig. 6.3 for a detailed loss budget). The major improvements at 50 % load involve 5 W transformer-core-loss reduction with a slight 0.8 W increase in winding losses, 3.2 W gate-loss reduction of the synchronous rectifiers with 1.1 W increase in R_{on}-related losses, and 2 W body-diode loss improvement (compare Fig. 6.3 with Fig. 5.17(b)).

Tab. 6.1: Key design values and implementation for components in the *Improved* 1.5 kW hardware demonstrator of Fig. 6.1.

Parameter	Design Value	Implementation
$S_{1\text{-}4}$	—	600 V, 70 mΩ GaN HEMT *IGLD60R070D1*
$S_{\mathbf{1\text{-}4}}$ gate drivers	—	*UCC21225A*
$S_{\mathbf{5,6}}$	—	40 V, 1.35 mΩ Si MOSFET *IQE013N04LM6*
$S_{\mathbf{5,6}}$ gate drivers	—	*SRK2001A* and *1EDN7511B*, $v_{\text{gate}} = 6$ V
$L_{\mathbf{r}}$	24 µH	PCB-integrated, CFFC [87]
$C_{\mathbf{dc}}$	1 µF	4× 0.28 µF *C5750X7T2W105K250KA*
$C_{\mathbf{out}}$	640 µF	32× 20 µF *C4532X7R1C336M250KC*
$C_{\mathbf{r}}$	11 nF	5× 2.2 nF *C3216C0G2J222J115AA*

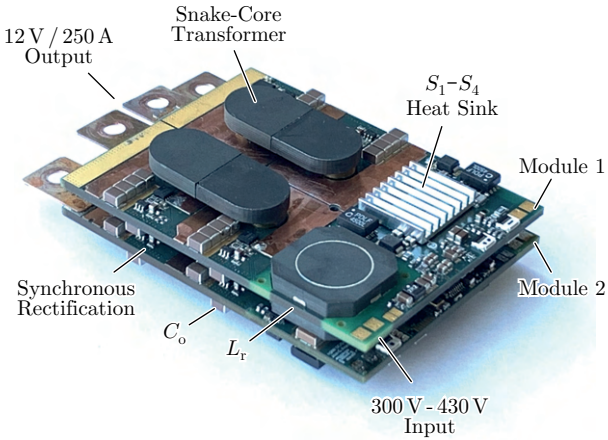

Fig. 6.1: Next-generation DC/DC module (key values and implementations given in Tab. 6.1), measuring 89.5 mm × 66.0 mm × 13.5 mm (308 W/in^3), shown with two 1.5 kW modules combined in an input-parallel output-parallel (IPOP) configuration to reach 3 kW output power at 250 A of output current and measuring 89.5 mm × 66.0 mm × 24.1 mm (345 W/in^3). The snake-core transformer enables ideal current sharing between the phases and modules with reduced core losses from the single flux path and shared transformer core between the two modules.

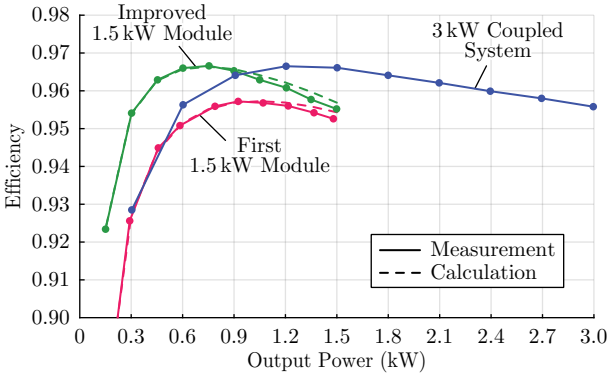

Fig. 6.2: DC/DC electrically-measured and calculated efficiencies from input (v_{dc} = 400 V) to output (V_o = 12 V) at different load conditions, including all loss components. The improved DC/DC converter module achieves higher efficiency than the original module at all load conditions, and the paralleled 3 kW converter achieves higher efficiency from reduced core losses at power levels below 1.5 kW.

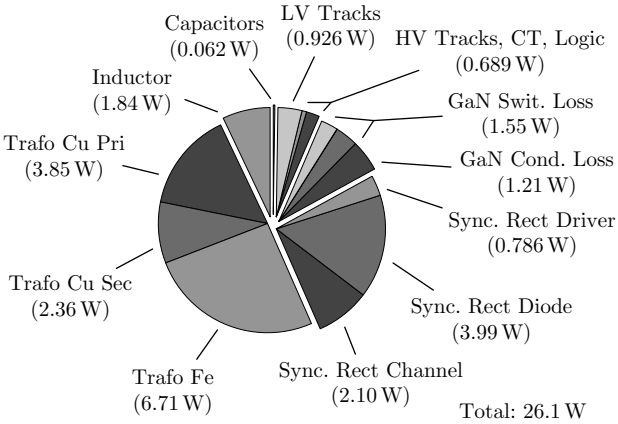

Fig. 6.3: Experimental loss budget at 50 % load of the "Improved 1.5 kW Module" of Fig. 6.2 ("Module 1" in Fig. 6.1), with v_{dc} = 400 V and V_o = 12 V, confirming the expected performance improvements calculated in Fig. 5.23(b).

6.3 Paralleled DC/DC Modules

With the improvements identified in Section 5.4 demonstrated in hardware for a significant increase in overall efficiency, two modules are now coupled to highlight one key benefit of the snake-core transformer—improved current sharing—and reach 3 kW of output power, demonstrating a path to higher output powers and currents with the modular approach.

The modules could be coupled in four configurations, with the input connections configured as "input series" (IS) or "input parallel" (IP) and the outputs independently configured as "output series" (OS) or "output parallel" (OP). The output series configurations (ISOS and IPOS) are not preferred for high-output-current applications, as each module would need to be configured to half of the total output voltage and therefore each module would need to provide the full output current. An input-series-output-parallel (ISOP) configuration features natural current sharing [104], at the expense of higher input currents per module and, for this application, switches rated to the awkward and non-commercial voltage level of 300 V.

In this application, the input-parallel-output-parallel (IPOP) module coupling is preferred, with simple scaling at the expense of complications in power sharing, where even minor mismatches in resonant tank impedance leads to poor current sharing between modules [105, 106]. Fig. 6.4(a) shows the parallel connection of two resonant-tank circuits and reveals that power sharing is essentially determined by the input impedance of each resonant tank. Once there is a mismatch between modules' impedances—easily occurring due to component tolerances that shift the tank's resonant frequency cf. Fig. 6.4(b)—poor current sharing between modules will inevitably exist.

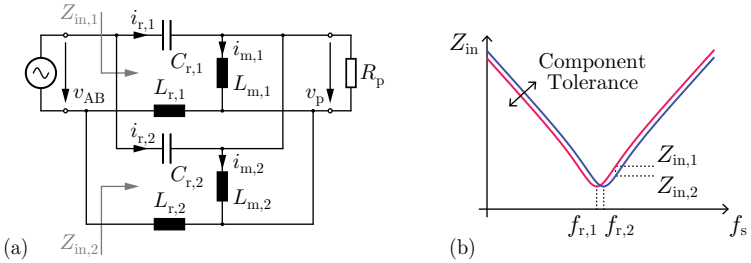

Fig. 6.4: (a) Parallel connection of resonant tanks with the input impedance (Z_{in}) as the key parameter that determines power sharing. (b) Direct impact of component tolerances on the input impedance through resonant-frequency (f_{r}) shifting.

To work around this fundamental problem, which is especially pernicious at high output currents, a few concepts can be considered. Firstly, digital or analog output current controllers that force equal power sharing through modulation are possible, but require additional sensing circuits, control loops, and computational power and complexity. In [83, 107], coupled inductors are used to force equal current sharing, but these cannot be arbitrarily modularized and cannot benefit from the compensating fringing-field approach used here [87] to realize high-efficiency PCB inductors. Finally, the resonant capacitors or inductors can be electrically connected [105, 106, 108], which achieves good power balancing with a simple implementation but does not improve the power density or core losses.

The proposed snake-core transformer, however, helps solving the power-sharing issue that bedevils IPOP modularity. The two-module topology is shown in Fig. 6.5, highlighting the direct magnetic coupling through a single flux path between the two modules. With a single flux path, the snake core forces the same induced voltage in all secondary windings regardless of how the modules share the current on the primary side, providing proper balancing of the output currents. Moreover, given the high precision with which the proposed PCB-integrated inductor can be designed, component tolerances are reduced to the strict minimum, naturally balancing the currents on the primary-side as well. The capacitor connection proposed in [105, 108] could be additionally applied if tolerances are not low enough, which together with the snake-core transformer would provide the best power-sharing results among state-of-the-art solutions [106].

This single flux path—the critical innovation of the snake-core—can be visualized through an equivalent circuit model of the magnetic reluctance, shown in Fig. 6.6 for a conventional matrix transformer (Fig. 6.6(a)) and for the snake-core transformer (Fig. 6.6(b))—here omitting the top and bottom diagonal reluctances for simplicity. With a high-permeability core, the snake-core transformer can be modeled with a single flux path through each winding, so mismatches in the number of turns or core reluctances cannot affect the current sharing between phases or modules. With the matrix transformer, alternatively, additional flux paths exist across the core yokes, so even small mismatches (in turns or reluctance) can result in current imbalances, and, potentially, lead to operational instability.

The benefits of the snake-core transformer, and by association the reluctance model, are validated *in situ* by artificially unbalancing the reluctance of a conventional matrix transformer with the addition of 50 % more air gap in one core limb—a total 12.5 % air-gap increase. This additional air gap un-

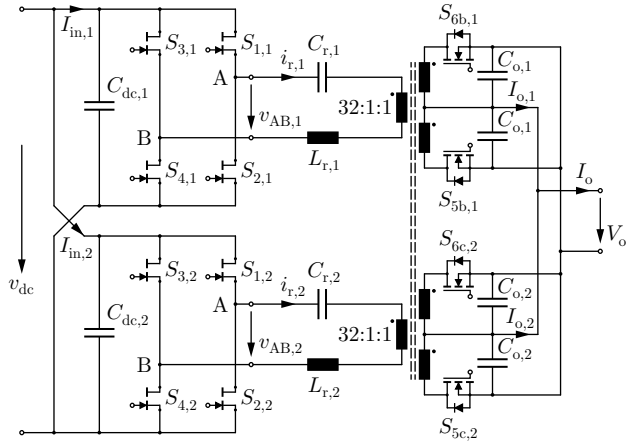

Fig. 6.5: Simplified power circuit of the proposed input-parallel output-parallel (IPOP) combined DC/DC converter, with the snake-core transformer shared for a single flux path between the two modules that results in ideal current sharing, lower core losses, and improved power density. The converter utilizes *IGLD60R070D1* GaN HEMT devices for the primary-side full-bridge and the updated *IQE013N04LM6* Si power MOSFETs operating as synchronous rectifiers on the secondary-side.

balances the flux distribution of the conventional core, which according to Section C.2.3 is calculated as:

$$\begin{bmatrix}\phi_{\mathrm{m1}}\\ \phi_{\mathrm{m2}}\\ \phi_{\mathrm{m3}}\\ \phi_{\mathrm{m4}}\end{bmatrix} = \frac{1}{4\mathcal{R}}\begin{bmatrix}3 & 1 & -1 & 1\\ 1 & 4 & 1.5 & -1.5\\ -1 & 1.5 & 4 & 1.5\\ 1 & -1.5 & 1.5 & 4\end{bmatrix}\begin{bmatrix}N_{\mathrm{p}}i_{\mathrm{p}} + N_{\mathrm{s}}i_{\mathrm{s1}}\\ N_{\mathrm{p}}i_{\mathrm{p}} + N_{\mathrm{s}}i_{\mathrm{s2}}\\ N_{\mathrm{p}}i_{\mathrm{p}} + N_{\mathrm{s}}i_{\mathrm{s3}}\\ N_{\mathrm{p}}i_{\mathrm{p}} + N_{\mathrm{s}}i_{\mathrm{s4}}\end{bmatrix}, \tag{6.1}$$

with $r = 1.5$ replaced in (C.76) for 50 % more reluctance in Limb 1. On the one hand, flux imbalance leads to circulating currents among the parallel-connected secondary windings, as indicates (C.87):

$$i'_{\mathrm{s1}} = -i'_{\mathrm{s3}} = \frac{v_{\mathrm{s}}}{5L_{\sigma\mathrm{s}} + 2\frac{N_{\mathrm{s}}^2}{\mathcal{R}}} \tag{6.2}$$

$$i'_{\mathrm{s2}} = -i'_{\mathrm{s4}} = 0, \tag{6.3}$$

but they can also lead, on the other hand, to instabilities and low-performance system operation. The snake-core transformer, however, fundamentally solves

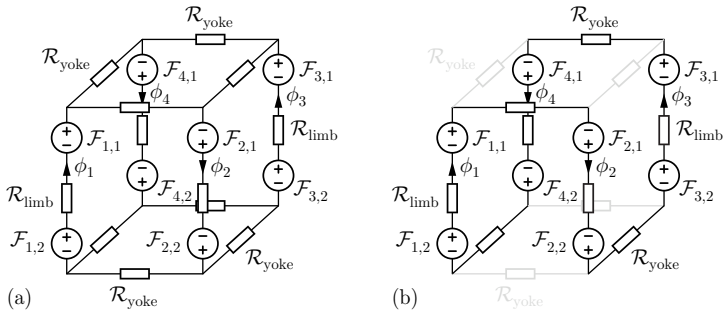

Fig. 6.6: Magnetic circuits for (a) a conventional matrix transformer and (b) the proposed snake-core transformer, with the magnetomotive forces of the windings ($\mathcal{F}$) and core reluctances ($\mathcal{R}$) highlighted, assuming the permeability of the core is sufficiently high to ignore reluctance paths through the air. The snake-core transformer has only a single path for the magnetic flux, guaranteeing identical flux through every winding and resulting in ideal current sharing. The conventional matrix transformer has multiple flux paths, and small turns or reluctance mismatches therefore result in poor current sharing and, potentially, operation instability.

the issues of reluctance imbalance and/or winding asymmetries, as all reluctances and windings are magnetically arranged in series by the single flux path and no flux imbalance exists (cf. (C.89)). Therefore, in the flux measurement of Fig. 6.7(a), the snake-core transformer maintains ideal current sharing between the phases and modules with the same flux penetrating all windings, while in Fig. 6.7(b,c), a traditional matrix transformer is tested, resulting in poor current sharing (especially during and near switching transitions) and signs of instability even before the artificial air gap is added. In real-world conditions, then, with variations in core materials and PCB manufacturing processes inevitable, the snake-core transformer uniquely provides a straightforward and reliable path to module coupling for high-current outputs.

The two paralleled modules are implemented in Fig. 6.1, with the transformer core shared for higher power density and reduced core losses. The hardware measures 89.5 mm × 66.0 mm × 24.1 mm and achieves a power density of 345 W/in^3, which is 12 % higher than that of a single module (308 W/in^3). The measured efficiency for this combined 3 kW DC/DC converter is given in Fig. 6.2 as the "3 kW Coupled System", with the expected gains in efficiency from reduced core losses boosting the 1.5 kW efficiency by

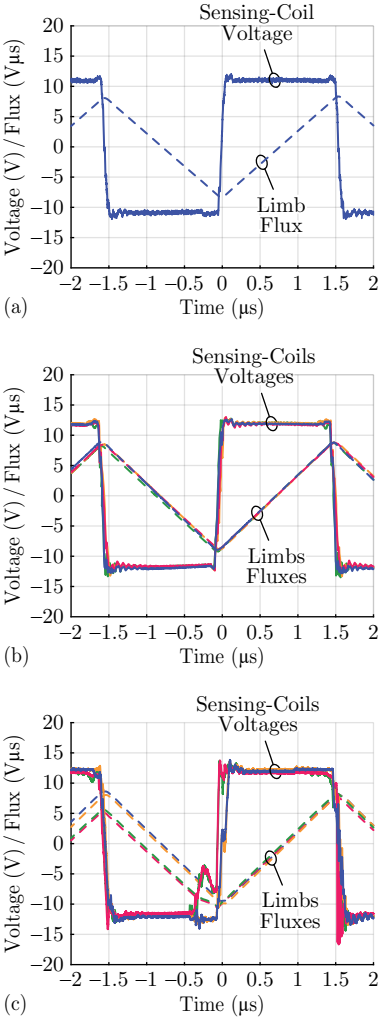

Fig. 6.7: Measured induced voltages and limb fluxes—with 3-turns sensing coils wound around the core limbs—for (a) the proposed snake-core transformer, and for the conventional matrix transformer with (b) balanced and (c) unbalanced reluctances, through the addition of an larger air gap in one leg. Output power is 40 % load for all test conditions.

half percentage point at light load. The paralleled converter reaches nearly 97 % peak efficiency and outputs 250 A at 12 V for 3 kW output power.

Measurements on power sharing were also conducted based on the following definitions:

$$\sigma_{\mathrm{Po}} = \left| \frac{2\left(I_{\mathrm{o},1} - I_{\mathrm{o},2}\right)}{I_{\mathrm{o},1} + I_{\mathrm{o},2}} \right| \tag{6.4}$$

$$\sigma_{\mathrm{Pin}} = \left| \frac{2\left(I_{\mathrm{in},1} - I_{\mathrm{in},2}\right)}{I_{\mathrm{in},1} + I_{\mathrm{in},2}} \right| \tag{6.5}$$

$$\sigma_{\mathrm{Ir,rms}} = \left| \frac{2\left(I_{\mathrm{r},1,\mathrm{rms}} - I_{\mathrm{r},2,\mathrm{rms}}\right)}{I_{\mathrm{r},1,\mathrm{rms}} + I_{\mathrm{r},2,\mathrm{rms}}} \right|, \tag{6.6}$$

whereby the differences between input power (P_{in}), output power (P_{out}) and resonant-current amplitude ($I_{\mathrm{r,rms}}$) of each module are calculated and compiled in Tab. 6.2 for two different scenarios: (i) two independent modules with two completely decoupled snake cores, and (ii) the two modules magnetically coupled by one single snake core. The benefits of magnetic coupling are evident from the error results, which show that power sharing is improved throughout the converter. Parallel connection of two (or more) LLC converter modules is therefore enabled by the combination of the snake-core transformer, for equal flux and output-current sharing, and PCB-integrated inductors, with high manufacturing precision and low tolerances, paving the way toward next-generation power supply modules.

Tab. 6.2: Power-sharing error at 50 % load for parallel-connected modules with and without magnetic coupling.

Coupling	σ_{Po}	σ_{Pin}	$\sigma_{\mathrm{Ir,rms}}$
No	9.38 %	7.32 %	1.72 %
Yes	0.64 %	4.91 %	0.89 %

6.4 Summary

Key component- and converter-level improvements were identified in the previous chapter using the detailed loss models derived in the design optimization stage. These improvements have been implemented in this chapter, including expanding the snake-core-transformer core area and improving the

synchronous-rectifier speed and device selection, and eliminate 25 % of the total converter losses in a second-generation demonstrator that achieves nearly 97 % peak efficiency. Additionally, the benefits of the proposed snake-core transformer are showcased by paralleling two DC/DC modules with ideal current sharing among the secondary outputs for 3 kW total output power with an improvement in efficiency over a single module and a power density of 345 W/in^3 (21.1 kW/dm^3). This hardware prototype accomplishes all design specifications defined in Tab. 1.1 and opens the way toward next-generation industrial power supplies.

7 Conclusion and Outlook

7.1 Paving the Way Toward Next-Generation Power Supplies

Compact, reliable, cost-effective and efficient power supplies are critical to unlocking the electrification of the future, including power for new forms of (i) sustainable transportation, such as e.g. unmanned aerial vehicles (UAVs), more-electric aircraft and electric vehicles (EVs) developing rapidly, (ii) automated manufacturing, with CNC systems, automated machines and collaborative robotics dominating future industry, and (iii) information processing, with hyperscale data centers, 5G telecommunication and Industry 4.0 establishing the Information Age. These next-generation industrial power supplies must be realized under a challenging set of specifications, including long hold-up times that result in DC/DC-converter stages with wide-input-voltage ranges, output-voltage regulation with galvanic isolation, and high output currents at low voltages. Moreover, the strict requirements on power density and cost mandate high switching frequencies with soft-switching and complete PCB-integration (including magnetics), which potentially reduce the efficiency and increase the complexity of such supplies.

In the last couple of years, the dominating idea was that wide-band-gap (WBG) power semiconductors are the key enablers of smaller, faster and more efficient next-generation power electronics; with some publishers even portraying galium nitride (GaN) and silicon carbide (SiC) as "superheroes" [109]. Indeed, as [110] explains, they are largely doing so, but only in conjunction with improved magnetics and integrated circuits, better packaging, and more sophisticated circuit design and control. Fortunately, the necessity of advanced magnetics, proper topology and control to fulfil the challenging

specifications of next-generation supplies (cf. Tab. 1.1) was identified at the very beginning of this thesis, which directed the research efforts toward the investigation of soft-switched topologies, PCB-integrated magnetics and low-complexity control schemes that benefit the most from the enhanced switching characteristics of WBG devices.

Therefore, on the way toward the conceptualization of this next-generation power supply module—with focus given to the DC/DC stage in the scope of this work—the hypothesis relied on the combination of WBG power semiconductors (particularly GaN), high-efficiency LLC-based topologies, and improved PCB-integrated matrix transformers to accomplish the demanding requirements. The result was the conceptualization, design, modeling and fabrication of an isolated, regulated, 3 kW, 370 V-430 V-input, 12 V-output DC/DC power supply module with 97 % peak efficiency, 345 W/in^3 power density and full PCB integration for facilitated manufacturability and low production costs. This converter has no prior art in literature and was enabled by the topology, control and transformer design proposed in this thesis, with specific contributions and key findings detailed in the following.

7.2 Main Contributions and Key Findings

The most important contributions of the thesis are described in Chapter 2 and Chapter 3, where topology selection, control analysis and transformer design lay down the foundation for the excellent performance achieved by the hardware demonstrators. First, the proposed frequency and phase-shift synergetic control applied to the LLC converter, with minimized magnetizing current and external-to-the-transformer resonant inductor, extends the input-voltage range beyond that of state-of-the-art LLC designs and guarantees soft-switching throughout the full load and voltage ranges. This topology and control scheme, that includes a full-bridge primary and a matrix transformer for multiple high-current outputs, operates efficiently at higher frequencies and high output currents with PCB-integrated magnetics, improving significantly power density compared to state-of-the-art designs. The second key contribution is the snake-core transformer, a PCB-integrated matrix transformer that has a single path for the magnetic flux, ensuring equal flux linkage of parallel-connected secondary windings despite possible geometric PCB-layout asymmetries or reluctance imbalances. This approach avoids the emergence of circulating currents between parallel-connected secondary windings and guarantees, at the same time, equal secondary-side voltages in

power supplies with multiple (individual) isolated outputs or superior results in parallel-connected, magnetically-coupled modules.

The benefits of the proposed topology, control scheme and transformer design are validated by three fabricated 370 V-430 V-input, 12 V-output DC/DC hardware demonstrators, shown in Fig. 7.1 with their efficiency curves. Chapter 4 showcases a 3 kW DC/DC series-resonant converter (see Fig. 7.1(a)) that achieves 350 W/in^3 (21.4 kW/dm^3) power density and 93 % peak efficiency at 400 V input, with validated control and transformer operation. Chapter 5 presents a 1.5 kW DC/DC power converter module (see Fig. 7.1(b)) that achieves close to 96 % peak efficiency and a power density of 337 W/in^3 (20.6 kW/dm^3), with full PCB-integration and zero-voltage switching even down to zero load. Chapter 6 finally demonstrates a magnetically-coupled, input-parallel/output-parallel, 3 kW DC/DC converter (see Fig. 7.1(c)) that achieves a peak efficiency of nearly 97 % and a power density of 345 W/in^3 (21.1 kW/dm^3), with ideal current sharing among modules and stable operation.

Interestingly enough, though all three hardware demonstrators take advantage of WBG semiconductors for the primary-side full-bridge, they all have different loss performances, an indicator that WBG devices alone cannot push efficiency to the baseline of next-generation power-supply modules. Much more important is the combination of these high-frequency devices with proper topology, control and magnetics design and selection. This becomes evident by the design evolution of the three fabricated demonstrators, where efficiency gets significantly higher for nearly the same power density as improvements on topology, control and magnetics are implemented. The first hardware prototype, though compact and functional, suffers from efficiency degradation toward low loads due to hard-switching, and generally higher losses from partial PCB-integration (additional wires and copper bars) and sub-optimal thermal management. This is significantly improved in the second hardware demonstrator, where a topological/control upgrade utilizes the magnetizing inductance to operate the system around the resonant frequency and support soft-switching throughout the entire load and input voltage ranges; and full PCB-integration on a single board (including transformer, resonant inductor and circuit connections) minimizes termination losses and enhances heat extraction. Even higher efficiencies are achieved with further improvements in design and control for the third prototype, where synchronous rectification is updated with a more sophisticated gate driver and a lower gate voltage; and the snake-core transformer is optimized for partial load and used to couple two IPOP modules to reach higher output

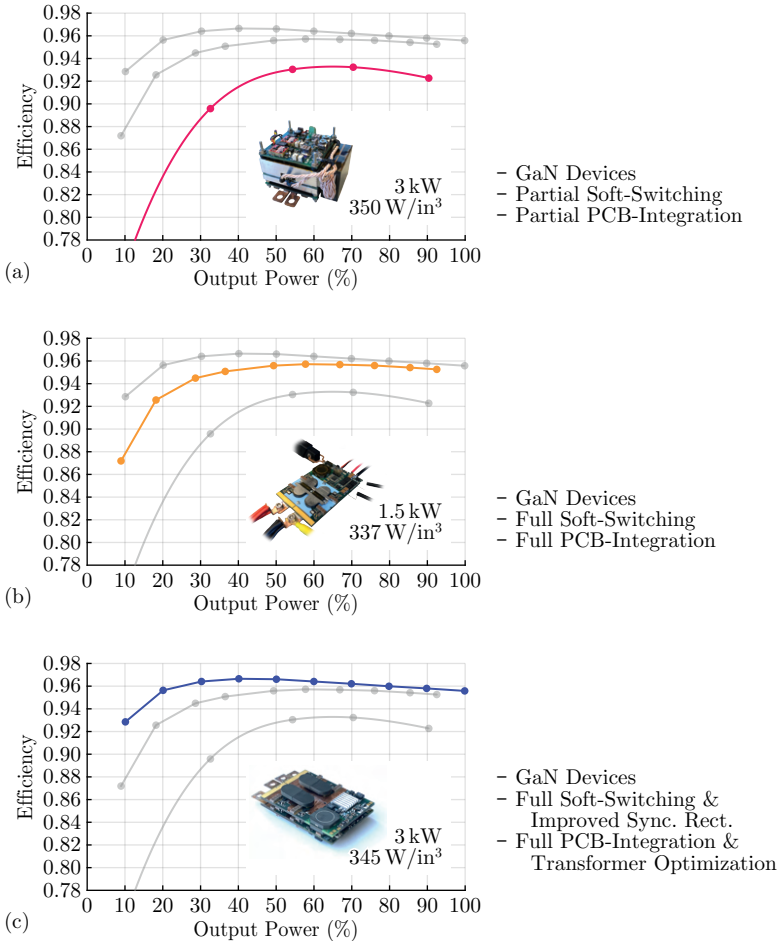

Fig. 7.1: The three hardware demonstrators conceptualized, designed and fabricated in the framework of this thesis, with 370 V-430 V input voltage, 12 V output voltage and nearly 350 W/in^3 (21.4 kW/dm^3) power density. Efficiencies are measured at 400 V input and shown for each of the three converters: the hardware prototypes of Chapter 4 (a), Chapter 5 (b), and Chapter 6 (c). Though all converters benefit from WBG semiconductors, the key enablers of performance enhancement are improvements on topology, control and magnetics.

powers with ideal output-current sharing, improved power density and lower core losses.

In conclusion, the results accomplished in this thesis indicate the necessity of careful topology/control selection and advanced-magnetics design for enabling WBG-based industrial power supplies that will outperform state-of-the-art solutions and catapult them to the next-generation performance standards. None of these features—be WBG devices, wide-gain-range resonant converters, or advanced PCB-integrated magnetics—will alone enable next-generation power-supply modules, but the thoughtful combination of these technologies and their careful application to the particular application, with emphasis to high-frequency PCB magnetics and soft-switching topologies, which enable compact and cost-effective converters with competitive efficiencies.

7.3 Outlook and Future Research

To keep pushing transportation, automated manufacturing and information and communication technology toward its increasingly-electric future, and especially enable the Industry 4.0, power supplies that feature a wide-input-voltage range, soft-switching, full PCB-integration, high efficiency, high power density, and high output currents are required. This work highlights key innovations—with experimental demonstrations—that unlock these critical requirements, with particular emphasis on alternative control schemes to extend the gain range of resonant converters, and on the snake-core transformer to support modular power scaling with ideal current sharing.

The research opportunities on these topics, however, go way beyond what was investigated in the framework of this thesis. First, the introduced control concepts should be evaluated for different sets of specifications, in order to identify their applicability and assess their performance in each particular case. Second, the analyses on the snake-core transformer should be extended to include the impacts on current balancing and system stability when three or more power supply modules are coupled. Finally, the bottleneck of synchronous rectification must be circumvented if higher power densities are targeted, as switching frequency cannot be increased above 500 kHz for the implemented prototype without penalizing efficiency with higher SR body-diode conduction losses. Close-to-ideal synchronous rectification, though, is difficult to achieve at high switching frequencies with existing discrete components; speeding the sensing and actuation might require either integrated synchronous rectifier ICs or, at a minimum, Kelvin-source connections on

high-current MOSFETs to support direct v_{ds} measurements for precise turn off.

Appendices

A

Power-Supply-Unit Heat Extraction

Chapter Abstract

This Appendix expands Chapter 1 on the discussion about PSU volume partitioning, as cooling becomes a major issue when striving for higher power densities. For the targeted 3 kW, 100 W/in^3 power supply, the cooling fan occupies nearly 10 % of the total available volume. Nevertheless, the analysis in this appendix proves that natural convection cooling is not enough for dissipating all supply's expected losses, and ultimately shows that the chosen fan was properly selected for keeping the temperature inside the PSU within reasonable limits.

A.1 Natural Convection Cooling

Thermal management of power supply units (PSUs) is an essential design step that guarantees proper conversion operation, shapes power density, and even influences conversion efficiency. For the targeted 3 kW PSU with 100 W/in^3 power density and 80-PLUS-Titanium efficiency, it first should be analyzed if heat transfer by natural convection and irradiation is enough to keeping the internal PSU temperature within reasonable limits. Therefore, assuming a typical thermal conductivity (λ) of 13 W/(K m^2) for natural convection and irradiation, an ambient temperature (T_a) of 25 ℃, a maximum PSU temperature (T_p) of 50 ℃, and considering the PSU form-factor dimensions shown in Fig. 1.4(c)—for 438 cm^2 of total surface area (A)—, a natural power dissipation (P_n) of 14.2 W results, according to:

$$P_n = \lambda A \left(T_p - T_a\right). \tag{A.1}$$

This is far from what is required considering, for example, a total full-load efficiency of $\eta = 94\,\%$ for a 96 %-efficient DC/DC stage and a 98 %-efficient

AC/DC stage. For these assumed efficiencies and $P_o = 3\,\text{kW}$, the cooling concept should dissipate near 180 W of losses according to:

$$P_l = P_o \left(\frac{1}{\eta} - 1 \right), \tag{A.2}$$

which is not achieved by natural convection cooling even if an absurd temperature of 300 ℃ would be allowed inside the supply's cabinet. Thus, forced cooling is required for the supply at hand, which is discussed in the next section.

A.2 Forced Convection Cooling

Forced convection cooling in server and data-center PSUs is typically realized by a fan that blows cold air from the facility into the supply's cabinet and forces the hot air to leave its interior together with the energy that is being dissipated. As the air particles move inside the cabinet, they hit hot component surfaces and devices' heat sinks, absorbing energy and heating up from the original ambient temperature (T_a) to the temperature at the air-flow exit (T_p). For a volume of air V with specific heat capacity c and density ρ, the absorbed energy can be calculated as:

$$E = \rho c V \left(T_p - T_a \right), \tag{A.3}$$

from which the power (P_f) that is dissipated can be calculated if a given air-flow rate ($\frac{dV}{dt}$) is maintained inside the PSU:

$$P_f = \frac{dE}{dt} = \rho c \frac{dV}{dt} \left(T_p - T_a \right). \tag{A.4}$$

Air-flow tests were performed with the generic PSU of Fig. A.1(a) in order to determine the expected air speed of a 5 W axial fan [24] that is typically employed in server supplies of this class. This general supply has a very compact component placement and the same dimensions of the targeted $100\,\text{W/in}^3$ form factor (see Fig. 1.4(c)), so it can be assumed that the air resistance approaches that of the targeted PSU. The fan is operated at full power and a plastic air duct is used to homogenize the air flow and improve measurement results. The air speed is measured using the *TSI Velocicalc 9535* air-velocity meter, whose probe was positioned at six different locations at the end of the duct, according to Fig. A.1(b). An average air speed of 1.9 m/s was measured

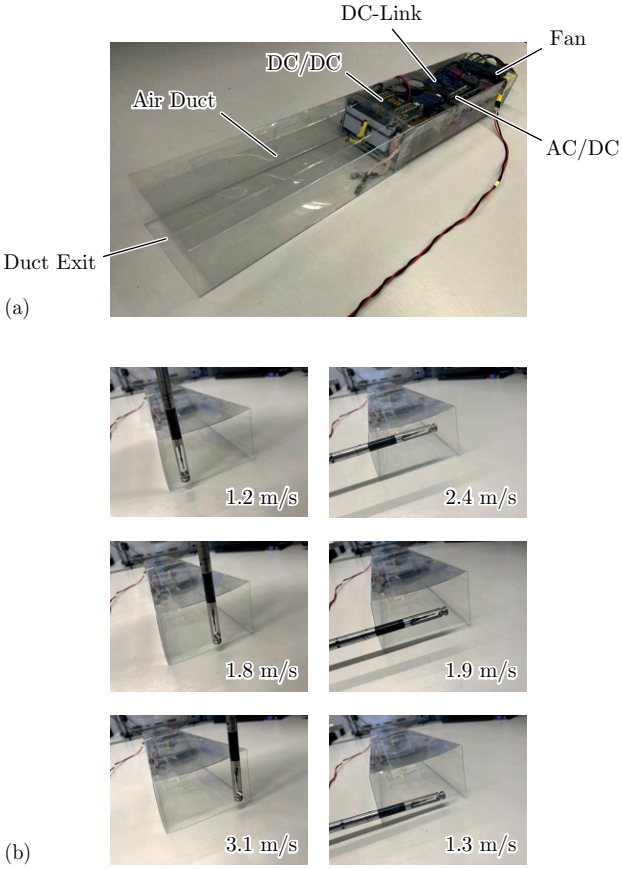

Fig. A.1: (a) Implemented setup for measuring the air speed of a 5 W axial fan that pushes air through the compactly-arranged components of a 3 kW, 100 W/in^3 power supply. The air speed was measured at six different locations at the exit of the attached air duct (b) for a homogeneous measurement.

at the air-duct exit, which has a cross-sectional area of $31\,\mathrm{cm}^2$ and thus gives $5.9\,\mathrm{dm}^3/\mathrm{s}$ of average air-flow rate.

Once the air-flow rate is determined, this value is applied to (A.4) together with $T_\mathrm{a} = 25\,^\circ\mathrm{C}$ and $P_\mathrm{f} = 180\,\mathrm{W}$ (cf. Section A.1), resulting in an estimate of $50\,^\circ\mathrm{C}$ for the maximum air temperature inside the PSU. This is a reasonable temperature value that confirms the selected fan as a proper choice.

B

Harmonic Analysis of Current Waveforms

Chapter Abstract

This Appendix expands Chapter 2 and introduces the RMS-to-average ratio as a simple but useful mathematical tool to compare different topologies in regard to their current shapes and expected conduction losses. It is seen from the analysis that resonant converters with sinusoidal current waveforms prevail over converters with triangular or square currents in regard to less conduction losses for the same transferred power.

B.1 Introduction

The frequency-domain representation of a particular steady state/periodic waveform consists of a sinewave in the same frequency of the original waveform (fundamental frequency) and an infinite number of sinewaves with frequency multiples of the fundamental frequency (harmonics). This transformation from the time domain into the frequency domain—known as the Fourier analysis—helps identifying the harmonic content of a particular current waveform and analyzing its impact in conduction losses that arise from, e.g., a transformer winding with frequency-dependent resistance.

Alternatively to the Fourier analysis, the harmonic content of a waveform could also be identified, in a more simplistic approach, by the calculation of the RMS-to-average ratio. This quantity indicates how higher is the RMS value of a particular current waveform to the average value of this waveform rectified. As the average value of the rectified waveform in DC/DC converters is typically analogous to the load's power, and the RMS currents give a glimpse

of conduction losses, this indicator helps analysing which topology generates the lowest conduction losses for the same transferred power.

B.2 Calculating the RMS-to-Average Ratios of Different Current Waveforms

A typical current waveform in various DC/DC-converter topologies has the generic square shape and harmonic content of Fig. B.1(a)—where d is the duty cycle, f_s is the switching frequency, and I_{pk} is the peak current. The RMS value of a current with this shape can be calculated as:

$$I_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\phi} I_{pk}^2 \, d\theta} = \sqrt{\frac{\phi}{\pi}} I_{pk}, \tag{B.1}$$

while the average value of the current rectified is calculated as:

$$|i|_{avg} = \frac{1}{\pi}\int_0^{\phi} I_{pk} \, d\theta = \frac{\phi}{\pi} I_{pk}, \tag{B.2}$$

with $\theta = 2\pi f_s t$, $\phi = 2\pi d$ and $d = [0, 0.5]$. Thus, the RMS-to-average ratio can be determined by the division of these two quantities:

$$\frac{I_{rms}}{|i|_{avg}} = \frac{1}{\sqrt{2d}}. \tag{B.3}$$

Therefore, assuming a typical duty cycle of 0.25, the RMS-to-average ratio for the generic current waveform of Fig. B.1(a) is 1.41, which indicates that RMS currents are 41 % higher than their ideal value of one. Ultimately, different waveforms can be compared in light of this number in order to find the one closest to ideal, which will implicate in the lowest conduction losses.

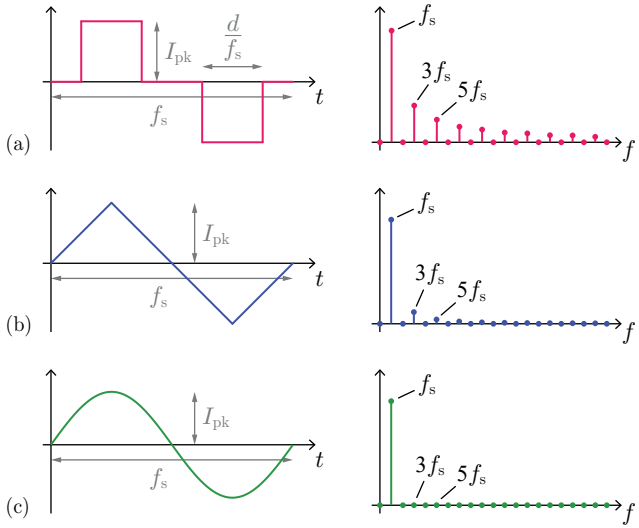

Fig. B.1: Time- and frequency-domain representations of three key current waveforms: (a) square, (b) triangular and (c) sinusoidal.

Now for the triangular waveform of Fig. B.1(b), the RMS-to-average ratio is calculated as:

$$I_{\text{rms}} = \sqrt{\frac{2}{\pi}\int_0^{\pi/2}\left(\frac{2I_{\text{pk}}}{\pi}\theta\right)^2 \,\mathrm{d}\theta} = \frac{1}{\sqrt{3}}I_{\text{pk}} \tag{B.4}$$

$$|i|_{\text{avg}} = \frac{2}{\pi}\int_0^{\pi/2}\frac{2I_{\text{pk}}}{\pi}\theta \,\mathrm{d}\theta = \frac{1}{2}I_{\text{pk}} \tag{B.5}$$

$$\frac{I_{\text{rms}}}{|i|_{\text{avg}}} = \frac{2}{\sqrt{3}} = 1.15 \tag{B.6}$$

resulting in only 15 %-higher RMS currents from the ideal value, which is consistent with the low harmonic content of this waveform.

Finally, for the sinewave of Fig. B.1(c), that consists of the fundamental component only, the RMS-to-average ratio is determined as:

$$I_{\text{rms}} = \sqrt{\frac{1}{\pi}\int_0^{\pi} \left(I_{\text{pk}} \sin\theta\right)^2 \, \mathrm{d}\theta} = \frac{1}{\sqrt{2}} I_{\text{pk}} \tag{B.7}$$

$$|i|_{\text{avg}} = \frac{1}{\pi}\int_0^{\pi} I_{\text{pk}} \sin\theta \, \mathrm{d}\theta = \frac{2}{\pi} I_{\text{pk}} \tag{B.8}$$

$$\frac{I_{\text{rms}}}{|i|_{\text{avg}}} = \frac{\pi}{2\sqrt{2}} = 1.11, \tag{B.9}$$

which is the lowest RMS-to-average ratio from the three shapes analysed. This result indicates that resonant DC/DC converters have the potential to achieve the lowest conduction losses among its counterparts (see Tab. B.1).

Tab. B.1: Comparison of the RMS-to-average current ratios for the three key current waveforms displayed in Fig. B.1.

Waveform shape	$I_{\text{rms}}/\lvert i\rvert_{\text{avg}}$
Square ($d = 0.25$)	1.41
Triangular	1.15
Sinusoidal	1.11

C Matrix-Transformer Essentials

Chapter Abstract

This Appendix extends Chapter 3 and gives special emphasis to the mathematical modeling of matrix transformers. First, a key formula for calculating the current density of a general transformer winding with rectified sinusoidal currents that supply a DC output is derived. Next, a formula for calculating the flux density of the transformer core with square-voltage excitation is derived. Finally, the mathematical background behind the matrix-transformer operation is introduced, including the voltage-current transformer equation, particular cases of the matrix structure for different air-gap positioning, and a detailed analysis on the emergence of circulating currents among the parallel-connected secondary windings. This analysis provides good insight into the (i) origin of circulating currents in state-of-the-art matrix transformers, (ii) the magnitude of such currents, and (iii) how the snake-core transformer fundamentally mitigates them.

C.1 Calculation of Current and Flux Densities

Two essential metrics in transformer design are the current density of a winding (J) and the flux density (B) in the magnetic core, which represent, respectively, the amount of current (i) and magnetic flux (ϕ) per unit area:

$$J = \frac{i}{A} \qquad [\mathrm{A/m^2}] \tag{C.1}$$

$$B = \frac{\phi}{A} \qquad [\mathrm{T}]. \tag{C.2}$$

In resonant converters, the sinusoidal or quasi-sinusoidal waveforms are rectified and filtered, by the output diode stage and capacitor, to supply the

load with a DC current. Thus, recalling (B.8) from Appendix B, the output DC current can be calculated as the average value of a rectified sinewave, resulting in:

$$I_o = |i|_{avg} = \frac{1}{\pi}\int_0^{\pi} I_{pk} \sin\theta \, d\theta = \frac{2}{\pi} I_{pk}, \tag{C.3}$$

where I_o is a function of the sinewave peak value (I_{pk}). Therefore, the current-density peak value in a transformer winding with sinusoidal currents can be calculated as:

$$J_{pk} = \frac{\pi N_s I_o}{2A_w}, \tag{C.4}$$

where N_s is the secondary-winding number of turns and A_w the secondary-winding cross-sectional area.

As the output rectifier stage consists of a diode bridge and a capacitor filter, the output voltage is directly applied to the secondary winding of the transformer, which is clamped to $+V_o$ and $-V_o$ at each half period. Thus, a square voltage waveform is applied to the transformer, which generates a magnetic flux that has a triangular shape according to Faraday's law of induction:

$$v_s = N_s \frac{d\phi}{dt}, \tag{C.5}$$

allowing to rewrite this equation as:

$$V_o = N_s \frac{\Delta\phi}{\Delta t}. \tag{C.6}$$

From (C.2), we replace $\Delta\phi$ with $A_c \Delta B$, where ΔB is the peak-to-peak value of the triangular flux density, and A_c the magnetic-core cross-sectional area, giving:

$$V_o = N_s \frac{2B_{pk} A_c}{\Delta t}, \tag{C.7}$$

where $\Delta B = 2B_{pk}$, and B_{pk} is the flux-density peak value. Furthermore, as the flux grows linearly for half switching period and decreases linearly for the subsequent half period, Δt can be equated as:

$$\Delta t = \frac{T_s}{2} = \frac{1}{2f_s}, \tag{C.8}$$

leading to a comprehensive formula for the flux density in the magnetic core:

$$B_{\mathrm{pk}} = \frac{V_{\mathrm{o}}}{4N_{\mathrm{s}} f_{\mathrm{s}} A_{\mathrm{c}}}. \tag{C.9}$$

C.2 Matrix-Transformer Fundamental Equations

This section expands Chapter 3 and provides a comprehensive mathematical model for describing the matrix-transformer operation. This model is subsequently leveraged to analyse the origin of circulating currents in state-of-the-art matrix transformers and to show that the snake-core transformer fundamentally mitigates such currents.

C.2.1 General Model

The matrix transformer with four sub-transformers and two windings per sub-transformer can be described by the reluctance model of Fig. C.1, adapted from Fig. 3.3(b). This generic representation captures sufficient properties for a comprehensive mathematical analysis of the transformer's operation, with the leakage fluxes omitted in the figure but considered in the model.

The windings are essentially characterized by their voltages and currents:

$$\mathbf{V_P} = \begin{bmatrix} v_{\mathrm{p1}} & v_{\mathrm{p2}} & v_{\mathrm{p3}} & v_{\mathrm{p4}} \end{bmatrix}^{\mathrm{T}} \tag{C.10}$$

$$\mathbf{V_S} = \begin{bmatrix} v_{\mathrm{s1}} & v_{\mathrm{s2}} & v_{\mathrm{s3}} & v_{\mathrm{s4}} \end{bmatrix}^{\mathrm{T}} \tag{C.11}$$

$$\mathbf{I_P} = \begin{bmatrix} i_{\mathrm{p1}} & i_{\mathrm{p2}} & i_{\mathrm{p3}} & i_{\mathrm{p4}} \end{bmatrix}^{\mathrm{T}} \tag{C.12}$$

$$\mathbf{I_S} = \begin{bmatrix} i_{\mathrm{s1}} & i_{\mathrm{s2}} & i_{\mathrm{s3}} & i_{\mathrm{s4}} \end{bmatrix}^{\mathrm{T}}, \tag{C.13}$$

their number of turns:

$$\mathbf{N_P} = \begin{bmatrix} N_{\mathrm{p1}} & 0 & 0 & 0 \\ 0 & N_{\mathrm{p2}} & 0 & 0 \\ 0 & 0 & N_{\mathrm{p3}} & 0 \\ 0 & 0 & 0 & N_{\mathrm{p4}} \end{bmatrix} \tag{C.14}$$

$$\mathbf{N_S} = \begin{bmatrix} N_{\mathrm{s1}} & 0 & 0 & 0 \\ 0 & N_{\mathrm{s2}} & 0 & 0 \\ 0 & 0 & N_{\mathrm{s3}} & 0 \\ 0 & 0 & 0 & N_{\mathrm{s4}} \end{bmatrix}, \tag{C.15}$$

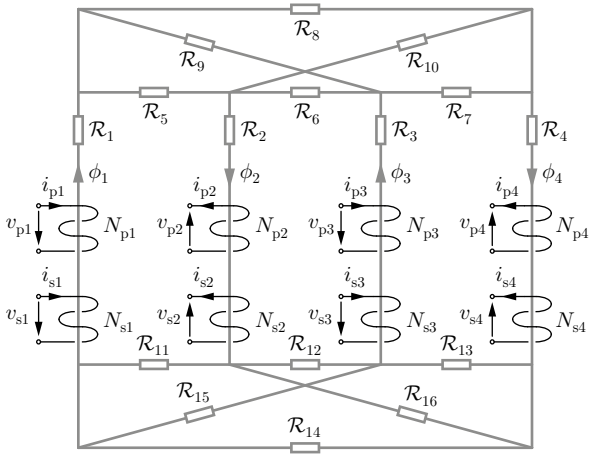

Fig. C.1: The planar view of the matrix-transformer reluctance model shown in Fig. 3.3(b), with four sub-transformers and two windings per sub-transformer. Here omitted are the leakage fluxes, which will nevertheless be consider in the model.

and the fluxes that penetrate them:

$$\boldsymbol{\Phi} = \begin{bmatrix} \phi_1 & \phi_2 & \phi_3 & \phi_4 \end{bmatrix}^{\mathrm{T}}, \tag{C.16}$$

while the properties of the medium where the windings are inserted are captured by the permeance matrix:

$$\boldsymbol{\mathcal{P}} = \boldsymbol{\mathcal{R}}^{-1} = \begin{bmatrix} \mathcal{R}_{11} & \mathcal{R}_{12} & \mathcal{R}_{13} & \mathcal{R}_{14} \\ \mathcal{R}_{21} & \mathcal{R}_{22} & \mathcal{R}_{23} & \mathcal{R}_{24} \\ \mathcal{R}_{31} & \mathcal{R}_{32} & \mathcal{R}_{33} & \mathcal{R}_{34} \\ \mathcal{R}_{41} & \mathcal{R}_{42} & \mathcal{R}_{43} & \mathcal{R}_{44} \end{bmatrix}^{-1} \tag{C.17}$$

that describes the ability of the medium to conduct magnetic flux. Permeance is the inverse of reluctance, thus the permeance matrix ($\boldsymbol{\mathcal{P}}$) is the inverse of the reluctance matrix ($\boldsymbol{\mathcal{R}}$), with $\mathcal{R}_{ij} = \mathcal{R}_{ji}$ by reciprocity [110, 111]. Reluctance ($\mathcal{R}$), that gives name to the model, is a property of the medium that acts against the magnetic-flux propagation and depends on the length (l), cross-sectional area (A) and permeability (μ) of the medium where the flux flows, calculated as:

$$\mathcal{R} = \frac{l}{\mu A}. \tag{C.18}$$

Based on these definitions and on Fig. C.1, the reluctance model can be solved for the fluxes that penetrate the windings as:

$$\boldsymbol{\Phi} = \boldsymbol{\mathcal{P}} \left(\mathbf{N_P} \mathbf{I_P} + \mathbf{N_S} \mathbf{I_S} \right) . \tag{C.19}$$

The permeance matrix $\boldsymbol{\mathcal{P}}$ is a generic representation of the medium and includes both the magnetic-core and the leakage reluctances. The fluxes in (C.19) are assumed to link all turns of a winding and are thus written as linkage fluxes:

$$\begin{aligned} \boldsymbol{\Psi_P} &= \mathbf{N_P} \boldsymbol{\Phi} && \text{(C.20)} \\ &= \mathbf{N_P} \boldsymbol{\mathcal{P}} \mathbf{N_P} \mathbf{I_P} + \mathbf{N_P} \boldsymbol{\mathcal{P}} \mathbf{N_S} \mathbf{I_S} && \text{(C.21)} \\ &= \mathbf{L_P} \mathbf{I_P} + \mathbf{M} \mathbf{I_S} && \text{(C.22)} \end{aligned}$$

$$\begin{aligned} \boldsymbol{\Psi_S} &= \mathbf{N_S} \boldsymbol{\Phi} && \text{(C.23)} \\ &= \mathbf{N_S} \boldsymbol{\mathcal{P}} \mathbf{N_P} \mathbf{I_P} + \mathbf{N_S} \boldsymbol{\mathcal{P}} \mathbf{N_S} \mathbf{I_S} && \text{(C.24)} \\ &= \mathbf{M} \mathbf{I_P} + \mathbf{L_S} \mathbf{I_S} . && \text{(C.25)} \end{aligned}$$

Finally, by applying Faraday's law, the celebrated transformer equation that relates voltages and currents with the self ($\mathbf{L_P}$,$\mathbf{L_S}$) and mutual ($\mathbf{M}$) inductances of the windings is found:

$$\begin{bmatrix} \mathbf{V_P} \\ \mathbf{V_S} \end{bmatrix} = \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} \boldsymbol{\Psi_P} \\ \boldsymbol{\Psi_S} \end{bmatrix} = \begin{bmatrix} \mathbf{N_P} \\ \mathbf{N_S} \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}t} \boldsymbol{\Phi} = \begin{bmatrix} \mathbf{L_P} & \mathbf{M} \\ \mathbf{M} & \mathbf{L_S} \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} \mathbf{I_P} \\ \mathbf{I_S} \end{bmatrix} . \tag{C.26}$$

This representation fully captures the effect of inductive coupling among the electrical ports and is a straightforward model to be used in circuit simulations.

While the inductance matrix is an useful mathematical tool, it does not provide a clear physical description of the transformer [110]. To overcome this issue, we first assume that the core magnetization flux and the winding leakage flux are two independent fluxes—a reasonable assumption for high-permeability cores as the one in question, where the vast majority of the magnetic-field lines is found inside the core that links the windings (see Fig. 3.5(d)). We then describe these two fluxes in two different ways: the core flux-path by the reluctance model of Fig. C.1, which allows proper air-gap positioning and core-loss calculation, and the leakage flux-path as leakage inductances associated to each individual winding [85, 112]. With this assumptions at hand, a comprehensive model for the the matrix transformer is

achieved and given by:

$$\begin{bmatrix}\mathbf{V_P}\\ \mathbf{V_S}\end{bmatrix} = \frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}\mathbf{N_P}\left(\boldsymbol{\Phi}_{\sigma\mathbf{P}} + \boldsymbol{\Phi}_{\mathbf{m}}\right)\\ \mathbf{N_S}\left(\boldsymbol{\Phi}_{\sigma\mathbf{S}} + \boldsymbol{\Phi}_{\mathbf{m}}\right)\end{bmatrix} \tag{C.27}$$

$$\boldsymbol{\Phi}_{\sigma\mathbf{P}} = \mathbf{N_P}^{-1}\mathbf{L}_{\sigma\mathbf{P}}\mathbf{I_P} \tag{C.28}$$

$$\boldsymbol{\Phi}_{\sigma\mathbf{S}} = \mathbf{N_S}^{-1}\mathbf{L}_{\sigma\mathbf{S}}\mathbf{I_S} \tag{C.29}$$

$$\boldsymbol{\Phi}_{\mathbf{m}} = \boldsymbol{\mathcal{P}}_{\mathbf{m}}\left(\mathbf{N_P}\mathbf{I_P} + \mathbf{N_S}\mathbf{I_S}\right), \tag{C.30}$$

where $\boldsymbol{\Phi}_{\mathbf{m}}$ and $\boldsymbol{\mathcal{P}}_{\mathbf{m}}$ are, respectively, the flux inside the magnetic core and the permeance of the core, $\boldsymbol{\Phi}_{\sigma\mathbf{P}}$ and $\boldsymbol{\Phi}_{\sigma\mathbf{S}}$ are the primary- and secondary-winding fluxes that leak the core, and $\mathbf{L}_{\sigma\mathbf{P}}$ and $\mathbf{L}_{\sigma\mathbf{S}}$ are the leakage inductances of each winding:

$$\mathbf{L}_{\sigma\mathbf{P}} = \begin{bmatrix} L_{\sigma\mathrm{p}1} & 0 & 0 & 0\\ 0 & L_{\sigma\mathrm{p}2} & 0 & 0\\ 0 & 0 & L_{\sigma\mathrm{p}3} & 0\\ 0 & 0 & 0 & L_{\sigma\mathrm{p}4}\end{bmatrix} \tag{C.31}$$

$$\mathbf{L}_{\sigma\mathbf{S}} = \begin{bmatrix} L_{\sigma\mathrm{s}1} & 0 & 0 & 0\\ 0 & L_{\sigma\mathrm{s}2} & 0 & 0\\ 0 & 0 & L_{\sigma\mathrm{s}3} & 0\\ 0 & 0 & 0 & L_{\sigma\mathrm{s}4}\end{bmatrix}. \tag{C.32}$$

C.2.2 Particular Cases

From the general matrix transformer of Fig. C.1, three particular cases of importance can be derived depending on the air-gap insertion. Air gaps are commonly used in resonant converters to increase the magnetizing current and support ZVS. As equation (C.18) indicates, air-gap reluctances dominate over high-permeability core reluctances (with core permeability typically $1000-10000$ times larger than that of air), resulting in the circuit of Fig. C.2(a) for air gaps symmetrically placed in the limbs, or the circuit of Fig. C.2(b) if air gaps are positioned in the yokes, or even the circuit of Fig. C.2(c) for the snake-core transformer (regardless if air gaps are in the limbs or in the yokes).

These simplified circuits can be expressed as permeance matrices ($\boldsymbol{\mathcal{P}}_{\mathbf{m}}$) for a complete mathematical representation of the transformer. For the circuit

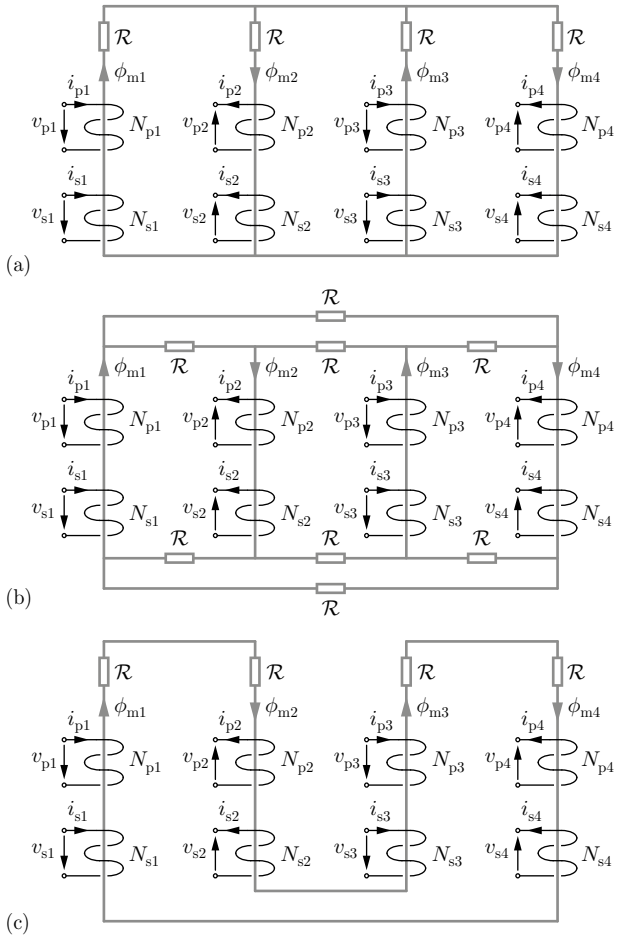

Fig. C.2: Three particular cases of the general matrix-transformer reluctance model shown in Fig. C.1 where air gaps are inserted in the core paths to reduce the magnetizing inductance and support ZVS. (a) Air gaps in the core limbs. (b) Air gaps in the core yokes. (c) Snake-core arrangement with air gaps in the limbs and/or in the yokes.

of Fig. C.2(a), the permeance matrix is calculated as:

$$\boldsymbol{\mathcal{P}}_{\mathbf{m}} = \frac{1}{4\mathcal{R}} \begin{bmatrix} 3 & 1 & -1 & 1 \\ 1 & 3 & 1 & -1 \\ -1 & 1 & 3 & 1 \\ 1 & -1 & 1 & 3 \end{bmatrix}, \tag{C.33}$$

whereas for the circuit of Fig. C.2(b), the permeance is described as:

$$\boldsymbol{\mathcal{P}}_{\mathbf{m}} = \frac{1}{2\mathcal{R}} \begin{bmatrix} 2 & 1 & 0 & 1 \\ 1 & 2 & 1 & 0 \\ 0 & 1 & 2 & 1 \\ 1 & 0 & 1 & 2 \end{bmatrix}. \tag{C.34}$$

For the snake-core transformer though, the reluctance model is significantly simplified (see Fig. C.2(c)), leading to a permeance matrix of ones:

$$\boldsymbol{\mathcal{P}}_{\mathbf{m}} = \frac{1}{4\mathcal{R}} \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix}. \tag{C.35}$$

In a more generic description, the permeance matrix can be written for the case of different reluctance values [113]. Thus, in case of air gaps in the core limbs with reluctances $\mathcal{R}_1 - \mathcal{R}_4$, the model of Fig. C.2(a) is described as:

$$\boldsymbol{\mathcal{P}}_{\mathbf{m}} = \mathcal{R}_{\mathrm{p}} \begin{bmatrix} \left(\frac{1}{\mathcal{R}_{\mathrm{p}}} - \frac{1}{\mathcal{R}_1}\right)\frac{1}{\mathcal{R}_1} & \frac{1}{\mathcal{R}_1\mathcal{R}_2} & -\frac{1}{\mathcal{R}_1\mathcal{R}_3} & \frac{1}{\mathcal{R}_1\mathcal{R}_4} \\ \frac{1}{\mathcal{R}_2\mathcal{R}_1} & \left(\frac{1}{\mathcal{R}_{\mathrm{p}}} - \frac{1}{\mathcal{R}_2}\right)\frac{1}{\mathcal{R}_2} & \frac{1}{\mathcal{R}_2\mathcal{R}_3} & -\frac{1}{\mathcal{R}_2\mathcal{R}_4} \\ -\frac{1}{\mathcal{R}_3\mathcal{R}_1} & \frac{1}{\mathcal{R}_3\mathcal{R}_2} & \left(\frac{1}{\mathcal{R}_{\mathrm{p}}} - \frac{1}{\mathcal{R}_3}\right)\frac{1}{\mathcal{R}_3} & \frac{1}{\mathcal{R}_3\mathcal{R}_4} \\ \frac{1}{\mathcal{R}_4\mathcal{R}_1} & -\frac{1}{\mathcal{R}_4\mathcal{R}_2} & \frac{1}{\mathcal{R}_4\mathcal{R}_3} & \left(\frac{1}{\mathcal{R}_{\mathrm{p}}} - \frac{1}{\mathcal{R}_4}\right)\frac{1}{\mathcal{R}_4} \end{bmatrix}, \tag{C.36}$$

where:

$$\mathcal{R}_{\mathrm{p}} = \frac{1}{\frac{1}{\mathcal{R}_1} + \frac{1}{\mathcal{R}_2} + \frac{1}{\mathcal{R}_3} + \frac{1}{\mathcal{R}_4}}, \tag{C.37}$$

which indicates that imbalances in air-gap reluctances lead to flux imbalances. For the snake-core transformer though, air-gap-reluctance imbalances do not

affect the flux at each winding separately due to the unique flux path (see Fig. C.2(c)), which is also confirmed by its permeance matrix:

$$\boldsymbol{\mathcal{P}}_{\mathbf{m}} = \frac{1}{\mathcal{R}_{\mathrm{s}}} \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix}, \tag{C.38}$$

where:

$$\mathcal{R}_{\mathrm{s}} = \mathcal{R}_1 + \mathcal{R}_2 + \mathcal{R}_3 + \mathcal{R}_4. \tag{C.39}$$

Flux imbalances ultimately lead to circulating currents in the parallel-connected secondary windings of a matrix transformer. As these currents potentially yield conduction losses, it is convenient to analyse their emergence from a mathematical point of view. Such analysis is conducted in the next sub-section.

C.2.3 Circulating Currents

Circulating currents arise in the matrix-transformer structure because of the parallel-connected secondary windings. As Fig. C.1 indicates, different limb fluxes ($\boldsymbol{\Phi}$) lead to different secondary-side induced voltages ($\mathbf{V_S}$) and, therefore, circulating currents among the parallel-connected secondary windings, which are limited only by whatever impedance exists in-between the windings. Thus, as flux imbalance is the key originator of such currents, we can conclude that they ultimately emerge from permeance matrices ($\boldsymbol{\mathcal{P}}$) with unbalanced reluctances, from asymmetrical number of turns ($\mathbf{N_P}$,$\mathbf{N_S}$), or from both, as indicates equation (C.19). First, the discussion is focused on the emergence of circulating currents due to asymmetries in the primary number of turns ($\mathbf{N_P}$), as symmetrical primary windings are harder to be fabricated compared to symmetrical secondary windings or symmetrical core structures (see "incomplete turns" in Fig. 3.2). Once this is settled, the discussion is extended to reluctance imbalance and its impact on circulating currents.

Primary-Winding Asymmetries

The analysis starts with the general reluctance model of Fig. C.1, further simplified into the circuit of Fig. C.2(a), in which the yoke reluctances are neglected and only the limb reluctances are considered. This simplification reduces the complexity of the analysis and corresponds to the insertion of

air gaps in the transformer limbs—a common practice in resonant converters where a comparably small magnetizing inductance is required to support ZVS. The simplified circuit also allows to investigate the impact of air-gap insertion on the magnitude of the circulating currents.

From Section C.2.1, and specifically from equation (C.27), the total flux linking each primary (ϕ_{px}) and secondary (ϕ_{sx}) winding, with x = [1, 2, 3, 4], can be equated as:

$$\phi_{\mathrm{px}} = \phi_{\sigma\mathrm{px}} + \phi_{\mathrm{mx}} \tag{C.40}$$

$$\phi_{\mathrm{sx}} = \phi_{\sigma\mathrm{sx}} + \phi_{\mathrm{mx}}, \tag{C.41}$$

where ϕ_{mx} denotes the flux in each transformer limb (see Fig. C.2(a)) and $\phi_{\sigma\mathrm{px}}$ and $\phi_{\sigma\mathrm{sx}}$ correspond to the flux which leaks from each winding. From the flux equations, one can derive equations for the voltage in each winding, recalling (C.27):

$$v_{\mathrm{px}} = L_{\sigma\mathrm{px}} i'_{\mathrm{px}} + N_{\mathrm{px}} \phi'_{\mathrm{mx}} \tag{C.42}$$

$$v_{\mathrm{sx}} = L_{\sigma\mathrm{sx}} i'_{\mathrm{sx}} + N_{\mathrm{sx}} \phi'_{\mathrm{mx}}, \tag{C.43}$$

where $i' = \frac{\mathrm{d}i}{\mathrm{d}t}$, $\phi' = \frac{\mathrm{d}\phi}{\mathrm{d}t}$ and the leakage flux is represented by the winding leakage inductance times the time-derivative of the winding current. The core-limb fluxes ϕ_{mx} depend on the magnetic-circuit geometry and can be derived by solving the reluctance circuit of Fig. C.2(a) (see equation (C.33)), which gives:

$$\begin{bmatrix} \phi_{\mathrm{m1}} \\ \phi_{\mathrm{m2}} \\ \phi_{\mathrm{m3}} \\ \phi_{\mathrm{m4}} \end{bmatrix} = \frac{1}{4\mathcal{R}} \begin{bmatrix} 3 & 1 & -1 & 1 \\ 1 & 3 & 1 & -1 \\ -1 & 1 & 3 & 1 \\ 1 & -1 & 1 & 3 \end{bmatrix} \begin{bmatrix} N_{\mathrm{p1}} i_{\mathrm{p1}} + N_{\mathrm{s1}} i_{\mathrm{s1}} \\ N_{\mathrm{p2}} i_{\mathrm{p2}} + N_{\mathrm{s2}} i_{\mathrm{s2}} \\ N_{\mathrm{p3}} i_{\mathrm{p3}} + N_{\mathrm{s3}} i_{\mathrm{s3}} \\ N_{\mathrm{p4}} i_{\mathrm{p4}} + N_{\mathrm{s4}} i_{\mathrm{s4}} \end{bmatrix}. \tag{C.44}$$

As one might realize, the limb fluxes are dependent on both primary and secondary magnetomotive forces of each core limb ($N_{\mathrm{p1}} i_{\mathrm{p1}} + N_{\mathrm{s1}} i_{\mathrm{s1}}$), which again indicates that winding asymmetries contribute to unbalanced flux distribution. In order to solve this system of equations, (C.42) and (C.43) are

re-written in the form of (C.27)-(C.30), that is:

$$\begin{bmatrix} v_{\mathrm{p1}} \\ v_{\mathrm{p2}} \\ v_{\mathrm{p3}} \\ v_{\mathrm{p4}} \end{bmatrix} = \begin{bmatrix} L_{\sigma\mathrm{p1}} & 0 & 0 & 0 \\ 0 & L_{\sigma\mathrm{p2}} & 0 & 0 \\ 0 & 0 & L_{\sigma\mathrm{p3}} & 0 \\ 0 & 0 & 0 & L_{\sigma\mathrm{p4}} \end{bmatrix} \begin{bmatrix} i'_{\mathrm{p1}} \\ i'_{\mathrm{p2}} \\ i'_{\mathrm{p3}} \\ i'_{\mathrm{p4}} \end{bmatrix} + \begin{bmatrix} N_{\mathrm{p1}} & 0 & 0 & 0 \\ 0 & N_{\mathrm{p2}} & 0 & 0 \\ 0 & 0 & N_{\mathrm{p3}} & 0 \\ 0 & 0 & 0 & N_{\mathrm{p4}} \end{bmatrix} \begin{bmatrix} \phi'_{\mathrm{m1}} \\ \phi'_{\mathrm{m2}} \\ \phi'_{\mathrm{m3}} \\ \phi'_{\mathrm{m4}} \end{bmatrix} \tag{C.45}$$

$$\begin{bmatrix} v_{\mathrm{s1}} \\ v_{\mathrm{s2}} \\ v_{\mathrm{s3}} \\ v_{\mathrm{s4}} \end{bmatrix} = \begin{bmatrix} L_{\sigma\mathrm{s1}} & 0 & 0 & 0 \\ 0 & L_{\sigma\mathrm{s2}} & 0 & 0 \\ 0 & 0 & L_{\sigma\mathrm{s3}} & 0 \\ 0 & 0 & 0 & L_{\sigma\mathrm{s4}} \end{bmatrix} \begin{bmatrix} i'_{\mathrm{s1}} \\ i'_{\mathrm{s2}} \\ i'_{\mathrm{s3}} \\ i'_{\mathrm{s4}} \end{bmatrix} + \begin{bmatrix} N_{\mathrm{s1}} & 0 & 0 & 0 \\ 0 & N_{\mathrm{s2}} & 0 & 0 \\ 0 & 0 & N_{\mathrm{s3}} & 0 \\ 0 & 0 & 0 & N_{\mathrm{s4}} \end{bmatrix} \begin{bmatrix} \phi'_{\mathrm{m1}} \\ \phi'_{\mathrm{m2}} \\ \phi'_{\mathrm{m3}} \\ \phi'_{\mathrm{m4}} \end{bmatrix}. \tag{C.46}$$

Boundary conditions must now be established in order to reduce the general problem to a specific problem. The series-connected primary windings are wound in such a way that the primary current (i_{p}) generates fluxes ϕ_{m1} and ϕ_{m3} that point upward in Fig. C.2(a), and negative fluxes ϕ_{m2} and ϕ_{m4} that point downward. As these windings are connected in series, one can write that:

$$v_{\mathrm{p1}} + v_{\mathrm{p2}} + v_{\mathrm{p3}} + v_{\mathrm{p4}} = v_{\mathrm{p}} \tag{C.47}$$

$$i_{\mathrm{p1}} = i_{\mathrm{p2}} = i_{\mathrm{p3}} = i_{\mathrm{p4}} = i_{\mathrm{p}}. \tag{C.48}$$

Furthermore, seeking to analyse the impact of asymmetric primary turns in the flux distribution and circulating currents, they are modelled as common and differential quantities, which will help simplifying the equations, giving:

$$\begin{aligned} N_{\mathrm{p1}} &= N_{\mathrm{pc}} + N_{\mathrm{pd1}} \\ N_{\mathrm{p2}} &= N_{\mathrm{pc}} + N_{\mathrm{pd2}} \\ N_{\mathrm{p3}} &= N_{\mathrm{pc}} + N_{\mathrm{pd3}} \\ N_{\mathrm{p4}} &= N_{\mathrm{pc}} + N_{\mathrm{pd4}}, \end{aligned} \tag{C.49}$$

where all differential quantities sum up to zero:

$$N_{\mathrm{pd1}} + N_{\mathrm{pd2}} + N_{\mathrm{pd3}} + N_{\mathrm{pd4}} = 0. \tag{C.50}$$

The single-turn secondary windings are much easier to be symmetrically designed and their number of turns are considered here to be equal:

$$N_{\mathrm{s1}} = N_{\mathrm{s2}} = N_{\mathrm{s3}} = N_{\mathrm{s4}} = N_{\mathrm{s}} = 1. \tag{C.51}$$

The flux equation in (C.44) can now be re-written considering the above-mentioned constrains:

$$\begin{aligned}
\phi_{\mathrm{m1}} &= \frac{N_{\mathrm{pe1}}}{\mathcal{R}} i_{\mathrm{p}} + \frac{N_{\mathrm{s}}}{4\mathcal{R}} \left(3i_{\mathrm{s1}} + i_{\mathrm{s2}} - i_{\mathrm{s3}} + i_{\mathrm{s4}}\right) \\
\phi_{\mathrm{m2}} &= \frac{N_{\mathrm{pe2}}}{\mathcal{R}} i_{\mathrm{p}} + \frac{N_{\mathrm{s}}}{4\mathcal{R}} \left(i_{\mathrm{s1}} + 3i_{\mathrm{s2}} + i_{\mathrm{s3}} - i_{\mathrm{s4}}\right) \\
\phi_{\mathrm{m3}} &= \frac{N_{\mathrm{pe3}}}{\mathcal{R}} i_{\mathrm{p}} + \frac{N_{\mathrm{s}}}{4\mathcal{R}} \left(-i_{\mathrm{s1}} + i_{\mathrm{s2}} + 3i_{\mathrm{s3}} + i_{\mathrm{s4}}\right) \\
\phi_{\mathrm{m4}} &= \frac{N_{\mathrm{pe4}}}{\mathcal{R}} i_{\mathrm{p}} + \frac{N_{\mathrm{s}}}{4\mathcal{R}} \left(i_{\mathrm{s1}} - i_{\mathrm{s2}} + i_{\mathrm{s3}} + 3i_{\mathrm{s4}}\right),
\end{aligned} \tag{C.52}$$

where N_{pex} refers to the primary equivalent number of turns and is calculated according to:

$$\begin{aligned}
N_{\mathrm{pe1}} &= N_{\mathrm{pc}} + \frac{N_{\mathrm{pd1}} - N_{\mathrm{pd3}}}{2} \\
N_{\mathrm{pe2}} &= N_{\mathrm{pc}} + \frac{N_{\mathrm{pd2}} - N_{\mathrm{pd4}}}{2} \\
N_{\mathrm{pe3}} &= N_{\mathrm{pc}} - \frac{N_{\mathrm{pd1}} - N_{\mathrm{pd3}}}{2} \\
N_{\mathrm{pe4}} &= N_{\mathrm{pc}} - \frac{N_{\mathrm{pd2}} - N_{\mathrm{pd4}}}{2}.
\end{aligned} \tag{C.53}$$

Considering now these derivations for a real transformer design, the open-circuit test could be applied to determine the primary equivalent number of turns N_{pex} and the core reluctance $\mathcal{R}$ based on open-circuit measurements. In this case, the secondary-side currents i_{sx} are zero and the secondary-side open-circuit voltages $v_{\mathrm{sx}}^{\mathrm{oc}}$ are measured. Hence, (C.45) and (C.46) can be written as:

$$\begin{aligned}
v_{\mathrm{p1}}^{\mathrm{oc}} &= \frac{\left(N_{\mathrm{pc}} + N_{\mathrm{pd1}}\right) N_{\mathrm{pe1}}}{\mathcal{R}} i_{\mathrm{p}}^{\mathrm{oc\prime}} & v_{\mathrm{s1}}^{\mathrm{oc}} &= \frac{N_{\mathrm{s}} N_{\mathrm{pe1}}}{\mathcal{R}} i_{\mathrm{p}}^{\mathrm{oc\prime}} \\
v_{\mathrm{p2}}^{\mathrm{oc}} &= \frac{\left(N_{\mathrm{pc}} + N_{\mathrm{pd2}}\right) N_{\mathrm{pe2}}}{\mathcal{R}} i_{\mathrm{p}}^{\mathrm{oc\prime}} & v_{\mathrm{s2}}^{\mathrm{oc}} &= \frac{N_{\mathrm{s}} N_{\mathrm{pe2}}}{\mathcal{R}} i_{\mathrm{p}}^{\mathrm{oc\prime}} \\
v_{\mathrm{p3}}^{\mathrm{oc}} &= \frac{\left(N_{\mathrm{pc}} + N_{\mathrm{pd3}}\right) N_{\mathrm{pe3}}}{\mathcal{R}} i_{\mathrm{p}}^{\mathrm{oc\prime}} & v_{\mathrm{s3}}^{\mathrm{oc}} &= \frac{N_{\mathrm{s}} N_{\mathrm{pe3}}}{\mathcal{R}} i_{\mathrm{p}}^{\mathrm{oc\prime}} \\
v_{\mathrm{p4}}^{\mathrm{oc}} &= \frac{\left(N_{\mathrm{pc}} + N_{\mathrm{pd4}}\right) N_{\mathrm{pe4}}}{\mathcal{R}} i_{\mathrm{p}}^{\mathrm{oc\prime}} & v_{\mathrm{s4}}^{\mathrm{oc}} &= \frac{N_{\mathrm{s}} N_{\mathrm{pe4}}}{\mathcal{R}} i_{\mathrm{p}}^{\mathrm{oc\prime}},
\end{aligned} \tag{C.54}$$

where the primary leakage inductances were neglected as the magnetizing inductance dominates in open-circuit measurements. We now apply constraints

(C.47) and (C.48) to the primary-winding voltages of (C.54), yielding:

$$\frac{v_{\mathrm{p}}^{\mathrm{oc}}}{i_{\mathrm{p}}^{\mathrm{oc}\prime}}\mathcal{R} = 4N_{\mathrm{pc}}^2 + \frac{\left(N_{\mathrm{pd1}} - N_{\mathrm{pd3}}\right)^2}{2} + \frac{\left(N_{\mathrm{pd2}} - N_{\mathrm{pd4}}\right)^2}{2}. \tag{C.55}$$

The subtraction of $v_{\mathrm{s1}}^{\mathrm{oc}}$ from $v_{\mathrm{s3}}^{\mathrm{oc}}$ and $v_{\mathrm{s2}}^{\mathrm{oc}}$ from $v_{\mathrm{s4}}^{\mathrm{oc}}$ in (C.54) gives:

$$N_{\mathrm{pd1}} - N_{\mathrm{pd3}} = \frac{\mathcal{R}}{N_{\mathrm{s}} i_{\mathrm{p}}^{\mathrm{oc}\prime}} \left(v_{\mathrm{s1}}^{\mathrm{oc}} - v_{\mathrm{s3}}^{\mathrm{oc}}\right) \tag{C.56}$$

$$N_{\mathrm{pd2}} - N_{\mathrm{pd4}} = \frac{\mathcal{R}}{N_{\mathrm{s}} i_{\mathrm{p}}^{\mathrm{oc}\prime}} \left(v_{\mathrm{s2}}^{\mathrm{oc}} - v_{\mathrm{s4}}^{\mathrm{oc}}\right), \tag{C.57}$$

while an expression for N_{pc} is found by equating $v_{\mathrm{s1}}^{\mathrm{oc}} + v_{\mathrm{s2}}^{\mathrm{oc}} + v_{\mathrm{s3}}^{\mathrm{oc}} + v_{\mathrm{s4}}^{\mathrm{oc}}$, which leads to:

$$N_{\mathrm{pc}} = \frac{\mathcal{R}}{4N_{\mathrm{s}} i_{\mathrm{p}}^{\mathrm{oc}\prime}} \left(v_{\mathrm{s1}}^{\mathrm{oc}} + v_{\mathrm{s2}}^{\mathrm{oc}} + v_{\mathrm{s3}}^{\mathrm{oc}} + v_{\mathrm{s4}}^{\mathrm{oc}}\right). \tag{C.58}$$

Finally, by substituting (C.56), (C.57) and (C.58) in (C.55), an expression for calculating the reluctance is found:

$$\mathcal{R} = \frac{2N_{\mathrm{s}}^2 v_{\mathrm{p}}^{\mathrm{oc}} i_{\mathrm{p}}^{\mathrm{oc}\prime}}{\left(v_{\mathrm{s1}}^{\mathrm{oc}} - v_{\mathrm{s3}}^{\mathrm{oc}}\right)^2 + \left(v_{\mathrm{s2}}^{\mathrm{oc}} - v_{\mathrm{s4}}^{\mathrm{oc}}\right)^2 + \frac{\left(v_{\mathrm{s1}}^{\mathrm{oc}} + v_{\mathrm{s2}}^{\mathrm{oc}} + v_{\mathrm{s3}}^{\mathrm{oc}} + v_{\mathrm{s4}}^{\mathrm{oc}}\right)^2}{2}}. \tag{C.59}$$

Therefore, the open-circuit test can very well characterize the transformer model and even describe winding asymmetries. By exciting the series connected primary windings with an alternating voltage source ($v_{\mathrm{p}}^{\mathrm{oc}}$,$f$) and by measuring the primary-side magnetizing current ($i_{\mathrm{p}}^{\mathrm{oc}}$) and secondary-side open-circuit voltages ($v_{\mathrm{s1}}^{\mathrm{oc}}$,$v_{\mathrm{s2}}^{\mathrm{oc}}$,$v_{\mathrm{s3}}^{\mathrm{oc}}$,$v_{\mathrm{s4}}^{\mathrm{oc}}$), $\mathcal{R}$ and N_{pex} may be calculated using (C.59), (C.58), (C.57), (C.56) and (C.53), respectively.

As a final step, it is possible to derive expressions for calculating the circulating currents when connecting the secondary windings in parallel. Two new constraints are applied for this parallel-connected condition:

$$v_{\mathrm{s1}} = v_{\mathrm{s2}} = v_{\mathrm{s3}} = v_{\mathrm{s4}} = v_{\mathrm{s}} \tag{C.60}$$

$$i_{\mathrm{s1}} + i_{\mathrm{s2}} + i_{\mathrm{s3}} + i_{\mathrm{s4}} = i_{\mathrm{s}}. \tag{C.61}$$

These constraints, however, do not simplify the model in a comprehensive level, and one extra constraint is proposed. By substituting (C.60) in (C.46):

$$\begin{aligned} v_{\mathrm{s}} &= L_{\sigma \mathrm{s}1} i'_{\mathrm{s}1} + N_{\mathrm{s}} \phi'_{\mathrm{m}1} \\ v_{\mathrm{s}} &= L_{\sigma \mathrm{s}2} i'_{\mathrm{s}2} + N_{\mathrm{s}} \phi'_{\mathrm{m}2} \\ v_{\mathrm{s}} &= L_{\sigma \mathrm{s}3} i'_{\mathrm{s}3} + N_{\mathrm{s}} \phi'_{\mathrm{m}3} \\ v_{\mathrm{s}} &= L_{\sigma \mathrm{s}4} i'_{\mathrm{s}4} + N_{\mathrm{s}} \phi'_{\mathrm{m}4}, \end{aligned} \tag{C.62}$$

isolating the fluxes in each equation, and summing them up according to $\phi_{\mathrm{m}1} - \phi_{\mathrm{m}2} + \phi_{\mathrm{m}3} - \phi_{\mathrm{m}4} = 0$ (see Fig. C.2(a)), it is possible to write that:

$$L_{\sigma \mathrm{s}1} i_{\mathrm{s}1} - L_{\sigma \mathrm{s}2} i_{\mathrm{s}2} + L_{\sigma \mathrm{s}3} i_{\mathrm{s}3} - L_{\sigma \mathrm{s}4} i_{\mathrm{s}4} = 0. \tag{C.63}$$

Here, it is clear that the circulating currents show a linear dependency on the leakage inductances. With reasonable approximation, a symmetric secondary-side circuit might be considered, i.e., $L_{\sigma \mathrm{s}1} = L_{\sigma \mathrm{s}2} = L_{\sigma \mathrm{s}3} = L_{\sigma \mathrm{s}4} = L_{\sigma \mathrm{s}}$, and a new constrain is found:

$$i_{\mathrm{s}1} - i_{\mathrm{s}2} + i_{\mathrm{s}3} - i_{\mathrm{s}4} = 0, \tag{C.64}$$

which together with the previous constraint (C.61) and zero-load condition ($i_{\mathrm{s}} = 0$) leads to:

$$\begin{aligned} i_{\mathrm{s}1} &= -i_{\mathrm{s}3} \\ i_{\mathrm{s}2} &= -i_{\mathrm{s}4}, \end{aligned} \tag{C.65}$$

representing a particular case of the parallel-connected secondary-side circuit where the stray impedances of each winding are assumed to be equal. Applying now (C.65) in (C.52) and substituting the result in (C.62) allows to find a comprehensive expression for the circulating currents with paralleled secondary windings and zero load:

$$i'_{\mathrm{sx}} = \frac{v_{\mathrm{s}} - \frac{N_{\mathrm{s}} N_{\mathrm{pex}}}{\mathcal{R}} i'_{\mathrm{p}}}{L_{\sigma \mathrm{s}} + \frac{N_{\mathrm{s}}^2}{\mathcal{R}}}, \tag{C.66}$$

where $\mathrm{x} = [1, 2, 3, 4]$.

Hence, the circulating currents essentially result from the difference between the parallel output voltage (v_{s}) and the induced voltage in each secondary winding, which is calculated by multiplying the primary-side current with the correspondent mutual inductance ($M_{\mathrm{x}} i'_{\mathrm{p}}$, with $M_{\mathrm{x}} = \frac{N_{\mathrm{s}} N_{\mathrm{pex}}}{\mathcal{R}}$). If the

primary windings do not contain asymmetries ($N_{\text{pe1}} = N_{\text{pe2}} = N_{\text{pe3}} = N_{\text{pe4}} = N_{\text{pc}}$), no voltage difference will result and no circulating currents will flow. The magnitude of these currents is limited by the secondary-winding self inductance L_{s}, which corresponds to the sum of the winding leakage inductance $L_{\sigma\text{s}}$ and the magnetizing inductance L_{ms} seen from the secondary winding ($L_{\text{s}} = L_{\sigma\text{s}} + L_{\text{ms}}$, with $L_{\text{ms}} = \frac{N_s^2}{\mathcal{R}}$). Hence, the better the transformer coupling is, the more influence the core inductance on the circulating currents has. Due to the close coupling of the primary and secondary windings in PCB transformers, the leakage inductance is very small and the secondary self-inductance is considered to be the magnetizing inductance only. For high-μ cores (low-reluctance cores), the magnetizing inductance is high and the circulating currents are negligible. However, a transformer with air gaps faces a linear increase in the reluctance with respect to the air gap length. In LLC converters, for example, the magnetizing current supports the boost operation and air gaps in the transformer core are required. Typical values for the core reluctance in LLC transformers are 10 to 50 times the value of the core reluctance without air gap. This represents a reduction of 10 to 50 times in the core inductance and, therefore, an increase in the circulating currents by the same factor, making them no longer negligible.

Equation (C.66) could be further improved including the winding resistance that models the secondary-winding losses. If the waveforms are sinusoidal, the expressions can be written in the complex form with their RMS or peak values and the resistance corresponds to the real part of the winding impedance:

$$I_{\text{sx}} = \frac{V_{\text{s}} - 2\pi f_{\text{s}} \frac{N_{\text{s}} N_{\text{pex}}}{\mathcal{R}} I_{\text{p}}}{R_{\text{s}} + j2\pi f_{\text{s}} \left(L_{\sigma\text{s}} + \frac{N_s^2}{\mathcal{R}} \right)}. \tag{C.67}$$

Likewise, the circulating currents could be now calculated for the case of the snake-core matrix transformer (see Fig. C.2(c)). The analysis is changed from the very beginning and a new flux equation must be considered based on the permeance matrix (C.35) of the snake core:

$$\begin{bmatrix} \phi_{\text{m1}} \\ \phi_{\text{m2}} \\ \phi_{\text{m3}} \\ \phi_{\text{m4}} \end{bmatrix} = \frac{1}{4\mathcal{R}} \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} N_{\text{p1}} i_{\text{p1}} + N_{\text{s1}} i_{\text{s1}} \\ N_{\text{p2}} i_{\text{p2}} + N_{\text{s2}} i_{\text{s2}} \\ N_{\text{p3}} i_{\text{p3}} + N_{\text{s3}} i_{\text{s3}} \\ N_{\text{p4}} i_{\text{p4}} + N_{\text{s4}} i_{\text{s4}} \end{bmatrix} \tag{C.68}$$

If all steps previously established were now repeated, one would find that the differential components of the primary-winding number or turns (N_{pdx})

cancel each other in the flux equations, leading to $N_{\mathrm{pex}} = N_{\mathrm{pc}}$ and:

$$\begin{aligned}
\phi_{\mathrm{m1}} &= \frac{N_{\mathrm{pc}}}{\mathcal{R}} i_{\mathrm{p}} + \frac{N_{\mathrm{s}}}{4\mathcal{R}} \left(i_{\mathrm{s1}} + i_{\mathrm{s2}} + i_{\mathrm{s3}} + i_{\mathrm{s4}}\right) \\
\phi_{\mathrm{m2}} &= \frac{N_{\mathrm{pc}}}{\mathcal{R}} i_{\mathrm{p}} + \frac{N_{\mathrm{s}}}{4\mathcal{R}} \left(i_{\mathrm{s1}} + i_{\mathrm{s2}} + i_{\mathrm{s3}} + i_{\mathrm{s4}}\right) \\
\phi_{\mathrm{m3}} &= \frac{N_{\mathrm{pc}}}{\mathcal{R}} i_{\mathrm{p}} + \frac{N_{\mathrm{s}}}{4\mathcal{R}} \left(i_{\mathrm{s1}} + i_{\mathrm{s2}} + i_{\mathrm{s3}} + i_{\mathrm{s4}}\right) \\
\phi_{\mathrm{m4}} &= \frac{N_{\mathrm{pc}}}{\mathcal{R}} i_{\mathrm{p}} + \frac{N_{\mathrm{s}}}{4\mathcal{R}} \left(i_{\mathrm{s1}} + i_{\mathrm{s2}} + i_{\mathrm{s3}} + i_{\mathrm{s4}}\right).
\end{aligned} \tag{C.69}$$

Also a simplified formula for the reluctance calculation based on the open-circuit measurement is found:

$$\mathcal{R} = \frac{4N_{\mathrm{s}}^2 v_{\mathrm{p}}^{\mathrm{oc}} i_{\mathrm{p}}^{\mathrm{oc}\prime}}{\left(v_{\mathrm{s1}}^{\mathrm{oc}} + v_{\mathrm{s2}}^{\mathrm{oc}} + v_{\mathrm{s3}}^{\mathrm{oc}} + v_{\mathrm{s4}}^{\mathrm{oc}}\right)^2}. \tag{C.70}$$

Moreover, the limb-fluxes in the snake core are always equal ($\phi_{\mathrm{m1}} = \phi_{\mathrm{m2}} = \phi_{\mathrm{m3}} = \phi_{\mathrm{m4}}$, see Fig. C.2(c)), which allows to use the boundary conditions in (C.62), of paralleled secondary windings, and write that:

$$L_{\sigma \mathrm{s1}} i_{\mathrm{s1}} = L_{\sigma \mathrm{s2}} i_{\mathrm{s2}} = L_{\sigma \mathrm{s3}} i_{\mathrm{s3}} = L_{\sigma \mathrm{s4}} i_{\mathrm{s4}}. \tag{C.71}$$

If we again assume a symmetric secondary-side circuit with $L_{\sigma \mathrm{s1}} = L_{\sigma \mathrm{s2}} = L_{\sigma \mathrm{s3}} = L_{\sigma \mathrm{s4}} = L_{\sigma \mathrm{s}}$, a special constraint for the snake-core transformer with equal secondary-side stray inductances is found:

$$i_{\mathrm{s1}} = i_{\mathrm{s2}} = i_{\mathrm{s3}} = i_{\mathrm{s4}}, \tag{C.72}$$

which combined with (C.61) and zero load ($i_{\mathrm{s}} = 0$) proves that the circulating currents in the snake-core transformer are fundamentally zero:

$$i_{\mathrm{s1}} = i_{\mathrm{s2}} = i_{\mathrm{s3}} = i_{\mathrm{s4}} = 0. \tag{C.73}$$

Reluctance Imbalance

Before closing this Appendix, it should be investigated how a potential imbalance on the core reluctances generally affects the core's flux distribution and, consequently, the circulating currents. The main analysis remains the same, though now the more generic reluctance matrix (C.36) is used to simulate the case where Limb 1 has larger/smaller air gap than limbs 2,3 and 4. By

defining a reference reluctance $\mathcal{R}$, it is possible to write the air-gap reluctances ($\mathcal{R}_1 - \mathcal{R}_4$) as functions of $\mathcal{R}$ for this hypothetical case:

$$\mathcal{R}_1 = r\mathcal{R} \tag{C.74}$$

$$\mathcal{R}_2 = \mathcal{R}_3 = \mathcal{R}_4 = \mathcal{R}, \tag{C.75}$$

where $r = [0, \infty]$ sets how larger or smaller is $\mathcal{R}_1$ in comparison to the other limb reluctances. Replacing (C.74) and (C.75) in (C.36) gives the permeance matrix for this particular case, which is used to write the flux equation:

$$\begin{bmatrix} \phi_{m1} \\ \phi_{m2} \\ \phi_{m3} \\ \phi_{m4} \end{bmatrix} = \frac{1}{(3r+1)\mathcal{R}} \begin{bmatrix} 3 & 1 & -1 & 1 \\ 1 & (2r+1) & r & -r \\ -1 & r & (2r+1) & r \\ 1 & -r & r & (2r+1) \end{bmatrix} \begin{bmatrix} N_p i_p + N_s i_{s1} \\ N_p i_p + N_s i_{s2} \\ N_p i_p + N_s i_{s3} \\ N_p i_p + N_s i_{s4} \end{bmatrix}, \tag{C.76}$$

where symmetrical primary and secondary windings:

$$N_{p1} = N_{p2} = N_{p3} = N_{p4} = N_p \tag{C.77}$$

$$N_{s1} = N_{s2} = N_{s3} = N_{s4} = N_s \tag{C.78}$$

and series-connected primary windings:

$$i_{p1} = i_{p2} = i_{p3} = i_{p4} = i_p. \tag{C.79}$$

are considered. Applying now constraint (C.65), of parallel-connected secondary windings at zero load, a simplified set of flux equations for the unbalanced-reluctance problem is found:

$$\begin{aligned} \phi_{m1} &= \frac{N_p}{\mathcal{R}} \frac{4}{3r+1} i_p + \frac{N_s}{\mathcal{R}} \frac{4}{3r+1} i_{s1} \\ \phi_{m2} &= \frac{N_p}{\mathcal{R}} \frac{2\,(r+1)}{3r+1} i_p + \frac{N_s}{\mathcal{R}} \left(\frac{1-r}{3r+1} i_{s1} + i_{s2} \right) \\ \phi_{m3} &= \frac{N_p}{\mathcal{R}} \frac{4r}{3r+1} i_p + \frac{N_s}{\mathcal{R}} \frac{2\,(r+1)}{3r+1} i_{s3} \\ \phi_{m4} &= \frac{N_p}{\mathcal{R}} \frac{2\,(r+1)}{3r+1} i_p + \frac{N_s}{\mathcal{R}} \left(\frac{1-r}{3r+1} i_{s1} + i_{s4} \right). \end{aligned} \tag{C.80}$$

From these flux equations and recalling (C.62) with $L_{\sigma s1} = L_{\sigma s2} = L_{\sigma s3} = L_{\sigma s4} = L_{\sigma s}$, we can write formulas for calculating the circulating currents:

$$i'_{s1} = \frac{v_s - \frac{4}{3r+1}\frac{N_s N_p}{\mathcal{R}} i'_p}{L_{\sigma s} + \frac{4}{3r+1}\frac{N_s^2}{\mathcal{R}}} \tag{C.81}$$

$$i'_{s2} = \frac{v_s - \frac{2(r+1)}{3r+1}\frac{N_s N_p}{\mathcal{R}} i'_p - \frac{1-r}{3r+1}\frac{N_s^2}{\mathcal{R}} i'_{s1}}{L_{\sigma s} + \frac{N_s^2}{\mathcal{R}}} \tag{C.82}$$

$$i'_{s3} = \frac{v_s - \frac{4r}{3r+1}\frac{N_s N_p}{\mathcal{R}} i'_p}{L_{\sigma s} + \frac{2(r+1)}{3r+1}\frac{N_s^2}{\mathcal{R}}} \tag{C.83}$$

$$i'_{s4} = \frac{v_s - \frac{2(r+1)}{3r+1}\frac{N_s N_p}{\mathcal{R}} i'_p - \frac{1-r}{3r+1}\frac{N_s^2}{\mathcal{R}} i'_{s1}}{L_{\sigma s} + \frac{N_s^2}{\mathcal{R}}}, \tag{C.84}$$

We immediately note that i'_{s2} and i'_{s4} are identical, which together with constraint (C.65) discloses that:

$$i_{s2} = i_{s4} = 0, \tag{C.85}$$

and thus no currents circulate in secondary-windings 2 and 4. That does not hold true for secondary windings 1 and 3 though. If we apply $i_{s1} = -i_{s3}$ to (C.81) and (C.83), the following formula is found:

$$\frac{N_s N_p}{\mathcal{R}} i'_p = \frac{(3r+1)\, L_{\sigma s} + (r+3)\, \frac{N_s^2}{\mathcal{R}}}{2\,(r+1)\, L_{\sigma s} + 4\frac{N_s^2}{\mathcal{R}}} v_s, \tag{C.86}$$

which substituted back in (C.81) or (C.83) leads to the final set of equations that calculate the circulating currents in case of reluctance imbalance:

$$i'_{s1} = -i'_{s3} = \frac{(r-1)\, v_s}{(r+1)\, L_{\sigma s} + 2\frac{N_s^2}{\mathcal{R}}} \tag{C.87}$$

$$i'_{s2} = -i'_{s4} = 0. \tag{C.88}$$

Therefore, if $r = 1$ ($\mathcal{R}_1 = \mathcal{R}_2 = \mathcal{R}_3 = \mathcal{R}_4$), the core has a symmetrical structure and no circulating currents emerge. However, any additional air gap introduced in one of the limbs that unbalances the core's reluctance structure will lead to circulating currents and losses.

Interestingly enough, the snake-core transformer does not suffer from asymmetrical core reluctances, as the magnetic circuit is equivalent to the

series-connection of all reluctances (see (C.38)), and thus results in the following flux equation:

$$\begin{bmatrix} \phi_{\mathrm{m1}} \\ \phi_{\mathrm{m2}} \\ \phi_{\mathrm{m3}} \\ \phi_{\mathrm{m4}} \end{bmatrix} = \frac{1}{4\mathcal{R}_{\mathrm{s}}} \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} N_{\mathrm{p}} i_{\mathrm{p}} + N_{\mathrm{s}} i_{\mathrm{s1}} \\ N_{\mathrm{p}} i_{\mathrm{p}} + N_{\mathrm{s}} i_{\mathrm{s2}} \\ N_{\mathrm{p}} i_{\mathrm{p}} + N_{\mathrm{s}} i_{\mathrm{s3}} \\ N_{\mathrm{p}} i_{\mathrm{p}} + N_{\mathrm{s}} i_{\mathrm{s4}} \end{bmatrix} \tag{C.89}$$

with:

$$\mathcal{R}_{\mathrm{s}} = \mathcal{R}_1 + \mathcal{R}_2 + \mathcal{R}_3 + \mathcal{R}_4 = (r+3)\,\mathcal{R}. \tag{C.90}$$

The similarity of this equation with (C.68) is obvious, leading to the same result achieved in (C.73):

$$i_{\mathrm{s1}} = i_{\mathrm{s2}} = i_{\mathrm{s3}} = i_{\mathrm{s4}} = 0, \tag{C.91}$$

which again makes of the snake core the ideal choice for PCB-integrated matrix transformers.

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