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Bidirectional Galvanically Isolated 25 kW 50 kHz 5 kV/700 V Si-SiC SuperCascode/Si-IGBT DC-DC Converter

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presented by
DANIEL AGGELER
Dipl. El. Ing. ETH Zurich
born 22. April 1981
citizen of Mels-Weisstannen, Switzerland

accepted on the recommendation of
Prof. Dr. Johann W. Kolar, examiner
Prof. Dr. Hans-Peter Nee, co-examiner

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Abstract

In order to reduce the emission of greenhouse gases and replace the limited energy sources like coal, oil or uranium, the number of renewable energy sources is constantly growing. This development results in a rising number of distributed power plants, which are principally subject to substantial energy fluctuations.

For the purpose of easy connection of the new energy sources to the grid and improvement of the power quality by harmonic filtering, voltage sag correction and highly dynamic control of the power flow new power electronic systems - so called *solid-state transformers (SST)* - are required. These interconnecting devices would enable full control of magnitude and direction of real power flow and reactive power generation and could replace not controllable, voluminous and heavy line frequency transformers. Based on such devices a *smart grid* comparable to the Internet, where a plug and play connection of sources and loads, distributed energy uploads and downloads and energy routing for transferring energy from the producer to the consumer, is possible.

Conventional interconnecting systems based on a back-to-back (BTB) converter and slow IGBT/IGCT devices consist of ac-dc/dc-ac converters and two line frequency transformers, which provide galvanic isolation as well as voltage level adaption and have a large volume and weight. In order to decrease the volume/weight of the conventional system and reduce the raw material consumption new topologies (SST) are in the focus of today's power electronics system investigations and developments.

So as to build the basis for minimizing the overall size of the SST which is in particular determined by the passive components and the heat sink, it is important to show, that a high switching frequency combined

with high efficiency is possible. Recent semiconductor materials as SiC, GaAs, GaN or diamond are characterized by a wide band gap and feature low conduction state voltage drop at high blocking voltage capability and marginal switching losses. These excellent device characteristics offer the possibility to achieve switching frequencies of several kHz at high blocking capabilities of several kV and/or to realize highly compact and highly efficient dc-dc converters with a medium voltage level input.

This research work investigates the application of SiC power semiconductors in form of a Si-SiC JFET SuperCascode to realize a bidirectional, galvanically isolated 25 kW/50 kHz 5 kV-700 V dc-dc converter. The main focus of the thesis is the analysis and modeling of the dynamic and the static behavior of the Si-SiC cascode as well as of the Si-SiC SuperCascode and the high frequency medium voltage transformer. With using simplified analytical models, simulation circuits and measurements of different experimental setups and of a converter prototype, the switching behavior of the SuperCascode, which is influenced by parasitic characteristics of each single power semiconductor, and wiring inductances and coupling capacitances, is investigated in particular.

Kurzfassung

Die Verwendung von erneuerbaren Energiequellen in den Bereichen Strom, Wärme und Kälte sowie Verkehr wird weltweit kontinuierlich gefördert, um einerseits den Ausstoss von Treibhausgasen zu reduzieren und andererseits auch die begrenzten Ressourcen an fossilen Energieträgern wie Kohle, Öl oder Uran zu schützen und zu ersetzen. Diese Entwicklung führt zu zahlreichen verteilten Energieerzeugunsanlagen, welche beträchliche Schwankungen des Energieangebotes aufweisen.

Um nun diesen neuen, umweltschonenden Energiequellen einen einfachen Zugang zum Energieversorgungsnetz zu garantieren, und dazu eine verbesserte Netzqualität durch Filterung von Oberschwingungen, Regelung von Spannungseinbrüchen und schnelle dynamische Regelung des Leistungsflusses zu gewährleisten, sind neue leistungselektronische Systeme - sogenannte *solid-state transformers (SST)* - notwendig. Diese Verbindungs-/Kupplungseinheiten (SST) erlauben die vollständige Regelung des Aussteuergrades wie auch eine Kontrolle der Richtung des Wirkleistungsflusses und/oder Blindleistungserzeugung und ersetzen nicht regelbare, voluminöse und schwere Netztransformatoren. Basierend auf diesen neuartigen leistungselektronischen Systemen (SST) wird es möglich ein sogenanntes intelligentes Netz - *smart grid* - zu realisieren, welches vergleichbar ist mit dem Internet, wo eine sofort betriebsbereite Verbindung von Quellen und Lasten erlaubt, verteilte Energien einzuspeisen und zu beziehen und vorhandene Energien geschickt gebündelt werden, um vom Erzeuger direkt zum Verbraucher geleitet zu werden.

Das herkömmliche Energiesystem besteht aus direkt aufeinanderfolgenden Topologien (BTB) von ac-dc/dc-ac Stromrichtern, langsam schaltenden IGBT/IGCT Halbleiterelementen und zwei netzfrequenten Transformatoren hohen Gewichtes und Bauvolumens, welche für die galvanis-

che Trennung wie auch für die Spannungsanpassung notwendig sind. Um das Volumen/Gewicht des herkömmlichen Gesamtsystemes und den Verbrauch an magnetischem Rohmaterial zu reduzieren, werden neue Stromrichtertopologien (SST) verstärkt erforscht und analysiert.

Um die Grundlage für eine Minimierung der insbesondere durch passive Komponenten und die Kühlvorrichtung bestimmten Baugrösse eines SST zu schaffen, ist es hier wichtig zu zeigen, dass eine hohe Schaltfrequenz bei hohem Wirkungsgrad möglich ist. Neueste Halbleitermaterialien wie SiC, GaAs, GaN oder Diamant, sind durch eine grosse Bandlücke charakterisiert und weisen auch bei hoher Sperrspannungsfestigkeit geringen Durchlassspannungsabfall und sehr niedrige Schaltverluste auf. Dies bietet die Möglichkeit bei Sperrspannungsfestigkeiten von mehreren kV Schaltfrequenzen von mehreren kHz und damit z.B. hochkompakte und hocheffiziente dc-dc Konverter mit Mittelspannungseingang zu realisieren.

In dieser Forschungsarbeit wird die Anwendung von SiC Leistungshalbleitern in Form einer Si-SiC JFET SuperKaskode zur Realisierung eines bidirektionalen, galvanisch getrennten 25 kW/50 kHz 5 kV-700 V dc-dc Konverters untersucht. Der Schwerpunkt liegt dabei auf der Analyse und Modellierung des dynamischen sowie statischen Verhaltens der Si-SiC Kaskode wie auch der Si-SiC SuperKaskode und des Hochfrequenz-Mittelspannungstransformators. Mittels vereinfachter analytischer Modelle, Simulationen und Messungen an Versuchsaufbauten und einem Prototyp des Konverters wird insbesondere das Schaltverhalten der SuperKaskode unter Einfluss parasitärer Eigenschaften der einzelnen Leistungshalbleiter, Verdrahtungsinduktivitäten und Koppelkapazitäten untersucht.

Notation

Principle Notation

x	lower case letters denote time-varying parameters x
$\hat{x}$	peak value of x
$\overline{x}$	average value of x
X	root mean square value of x

Symbols

C	capacitance
C_{DG}	drain-gate capacitance
C_{DGa}	'artificial' (additional) drain-gate capacitance
$C_{D,AVi}$	i-th barrier layer capacitance of the avalanche diode
C_{DS}	drain-source capacitance
$C_{eq,D,AVi}$	equivalent $C_{D,AVi}$
C_{GS}	gate-source capacitance
C_{iss}	input capacitance
$C_{iss(eq)}$	equivalent input capacitance
C_{rss}	reverse transfer capacitance
C_{oss}	output capacitance
D	drain
DC	duty cycle

D_{AVi}	i-th avalanche (balancing) diode
D_{GS}	gate-source diode
E_{off}	turn off energy losses
E_g	energy bandgap
E_{on}	turn on energy losses
E_{rrD}	diode reverse recovery energy losses
E_C	stored capacitor energy
E_c	critical electric field
f_s	switching frequency
G	gate
G_{Ji}	i-th SiC JFET gate potential
I_D	drain current
I_{DSS}	drain-source leakage current
I_{revD}	reverse (freewheeling) drain current
I_G	gate current
L_{load}	load inductor
$L_{\sigma,parasitic}$	parasitic stray inductance
m_{scalin}	linear scaling of mass
m_{int}	mass resulting by interpolation
N	number of single semiconductor devices
n_i	intrinsic carrier concentration
n	transformer turns ratio
P_c	conduction losses
P_{cD}	anti parallel diode conduction losses
P_{sw}	switching losses
P_{rrD}	reverse recovery diode losses
P_n	nominal power
$R_{DS(on)}$	drain-source on-resistance
$R_{D(on)}$	diode on-resistance
$R_{th(j-c)}$	thermal resistance from junction to case
R	resistance
R_{damp}	damping resistance
R_G	external gate resistor
S	source

S_x	switch of x type
V_1	HV side dc-link voltage
V_2	LV side dc-link voltage
V_{DS}	drain-source voltage
V_{aval}	avalanche voltage
V_{p-off}	pinch-off voltage
V_{GS}	gate source voltage
V_{th}	threshold voltage
$V_{(BR),DSS}$	drain-source breakdown voltage
V_{scalin}	linear scaling of volume
V_{int}	volume resulting by interpolation
v_{sat}	electron saturation velocity
V_C	capacitor voltage
V_{dc}	dc-link voltage
V_D	drain potential
v_{FD}	diode forward voltage
V_G	gate driver voltage
V_M	Miller level
V_R	reverse Zener diode voltage
ϵ_r	relative permittivity
μ_n	electron mobility
λ	thermal conductivity

Subscripts

C	Si-SiC Cascode
i	i-th element
J,Ji	SiC JFET, i-th SiC JFET
$Ji-M$	i-th SiC JFET to MOSFET
M,Mi	MOSFET, i-th MOSFET
m	number m of series connected balancing diodes
n	number n of cascaded elements
SC	Si-SiC SuperCascode

M^s	single MOSFET
CL	current limitation

Abbreviations

ac	alternating current
AVG	average
BTB System	back-to-back system
BJT	bipolar junction transistor
DAB	dual active bridge
dc	direct current
EMI	electro magnetic interference
EMC	electro magnetic compatibility
FET	field-effect transistor
GaAs	gallium arsenide
GaN	gallium nitride
GTO	gate turn-off thyristor
HF	high frequency
HV	high voltage
IGBT	insulated gate bipolar transistor
IGCT	integrated gate commutated thyristor
JFET	junction FET
MOSFET	metal oxide semiconductor FET
NMSiSiCSC	novel modified Si SiC SuperCascode
ppm	parts per million
RMS	root mean square
Si	silicon
SiC	silicon carbide
SST	solid-state transformer
ZVS	zero voltage switching

Contents

Chapter 1

Introduction

1.1 Motivation

Since the end of the 20^{th} century the global energy demand has increased tremendously due to higher living standards and fast industrialization of countries with emerging economies. Most of the required energy is generated from fossil fuels. The utilization of renewable energy sources is

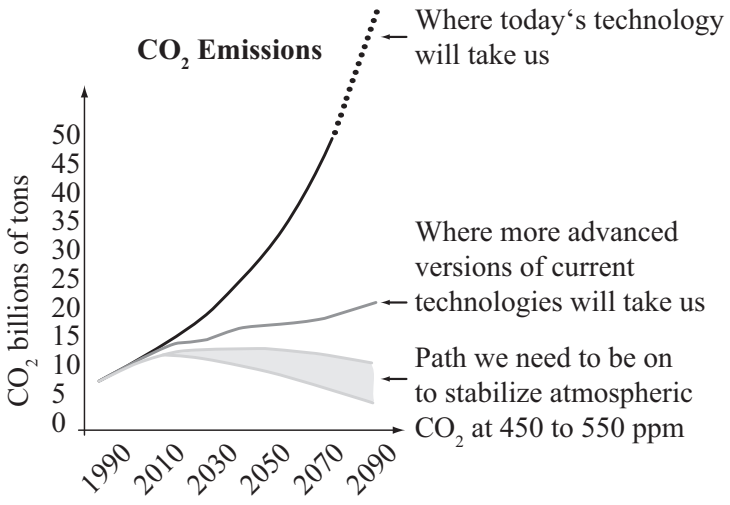

Figure 1.1: A dramatic departure is required to reduce CO_2 emissions (Source: Merrill Lynch/PNM resources) [1].

advancing but still limited by higher costs and therefore not significantly contributing to the global energy generation.

The consequence is an immense consumption on limited energy sources e.g. coal, oil or uranium and furthermore a corresponding environmental pollution problem. International committees and research groups discuss scenarios for a reduction of the pollution and/or a replacement of fossil fuels in the energy generation processes.

The greenhouse gases are representative for environmental pollution and the most well known one is carbon dioxide, CO_2. In [1] the CO_2 emissions today and in future are analyzed for today's energy generation technology and for advanced versions of the current technologies. The dramatical increase of CO_2 emissions which would result for continued utilization of current technologies is illustrated in Figure 1.1. Even with an advanced version of today's technologies the CO_2 emissions will not be stabilized at 450 ppm to 550 ppm but the rate of increase would be much slower.

Bose et al. [3] described the importance of advanced technologies like power electronics, which includes power semiconductor devices, converters, machines, drives and control. This technology combined with a wide range of renewable energy applications would possibly stabilize the CO_2 emission. A possible road map of renewable energy utilization is discussed and analyzed in [2]. There it is shown (Figure 1.2), that the annual electricity production based on photovoltaics is increasing significantly, but

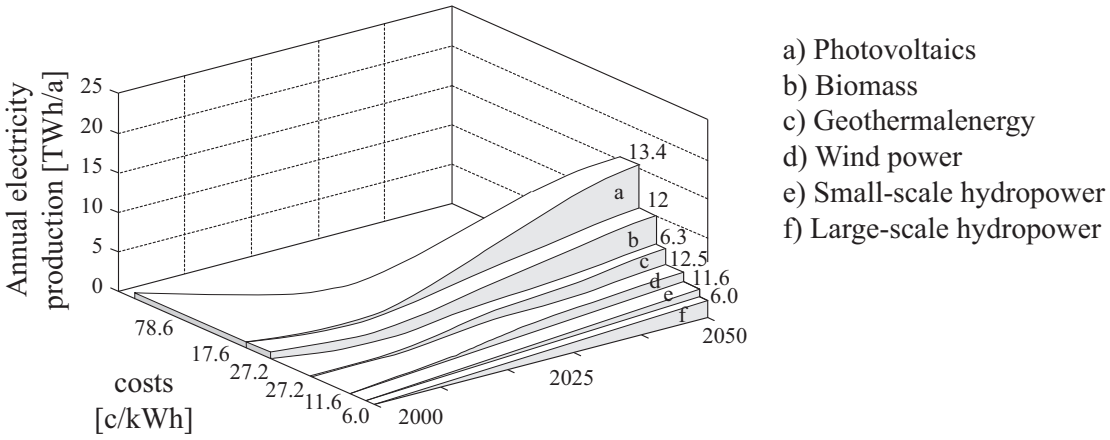

Figure 1.2: Development over time of electricity production from renewable energy sources [2].

is almost constant for small and large-scale hydro power respectively. Furthermore, the costs are decreasing because of a strongly increasing renewable energy market.

Global projects are now supporting the use of renewable energy and plans are developed to minimize the environmental pollution in future. DESERTEC Foundation [4] is just one of those clean tech projects, where in future solar energy will be used for electric power generation. In future, the number of renewable sources and the amount of generated energy, by clean technology, will grow continuously. This development will result in a rising number of distributed power plants, which are in principal showing substantial energy fluctuations. In order to easily connect the new energy sources to the grid and to improve the power quality by harmonic filtering, voltage sag correction and highly dynamic control of the power flow new power electronic systems, so called intelligent *universal/solid-state transformers (SST)*, are required. These interconnecting devices will enable full control of magnitude and direction of real and reactive power flow and will partly replace not controllable, bulky and heavy line frequency transformers. Based on such intelligent systems a *smart grid* (cf. Figure 1.3) comparable to the Internet, where a 'plug and play' connection of sources and loads, distributed energy uploads and downloads and energy routing for transferring energy from the producer to the consumer, is possible.

Accordingly, today's hierarchical power system will be replaced in

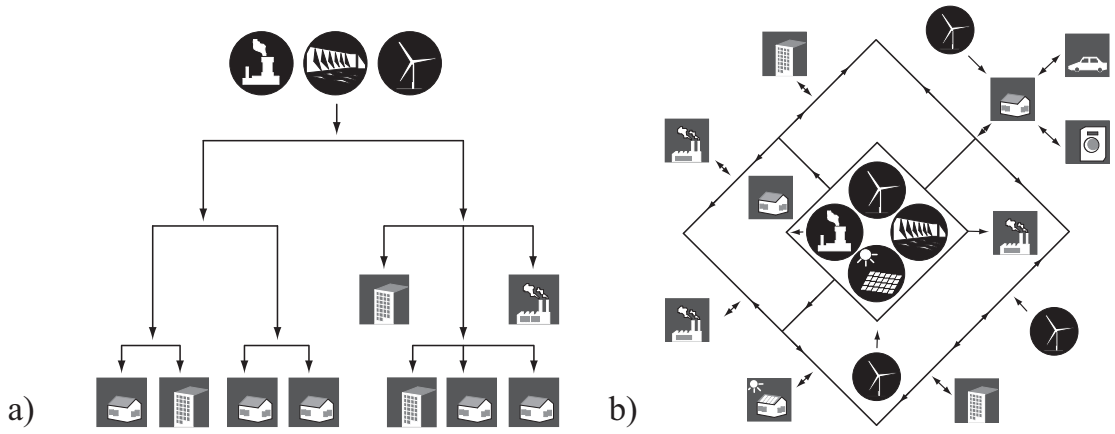

Figure 1.3: ABB's vision of the power system of the future: (a) today's hierarchical power system and (b) future fully realized smart grid (Source: ABB white paper) [5].

future with a smart grid system [6], due to the distributed power generation of several renewable sources. The power generation with renewable energy sources is in most cases not continuous and e.g. depending on the weather condition. Feeding the produced energy into a distribution system, influences the overall energy flow. Therefore, it is a challenge to control and keep the energy flow between sources and loads balanced. To solve the problem of power flow balancing back-to-back (BTB) systems, also known as loop controllers, have been investigated.

The conventional BTB system is discussed in the following, with an example power distribution system of Japan. The disadvantages of the conventional BTB system are briefly evaluated and new topologies for next-generation BTB systems are introduced.

1.2 BTB Systems

Todays power distribution system in Japan has radial feeders forming no loop as shown in Figure 1.4 for a 6.6 kV distribution system having two feeders from a distribution transformer. If the distributed power generators are installed concentrated on one of the feeders (feeder 2 in Figure 1.4), regulating voltage on both feeders within an acceptable range becomes difficult. Therefore, the above mentioned BTB systems have been investigated and the dotted lines in Figure 1.4 illustrate, where the BTB system would be installed.

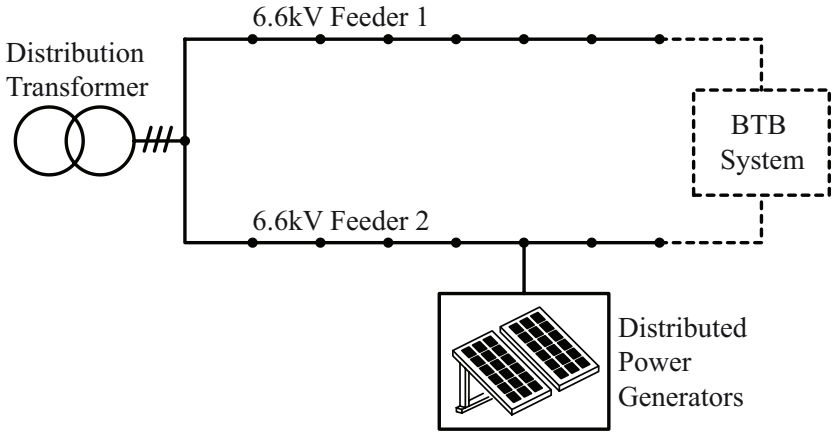

Figure 1.4: A 6.6 kV distribution system in Japan having two feeders.

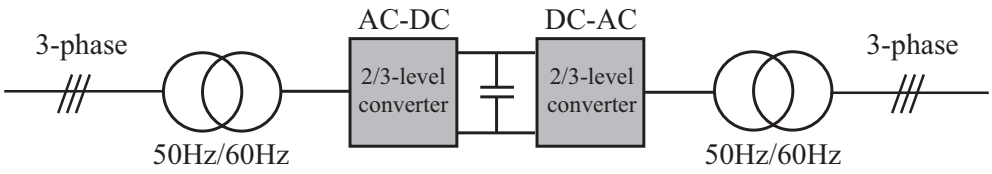

Figure 1.5: Conventional BTB system.

1.2.1 Conventional Bidirectional BTB Systems

In Figure 1.5 a circuit configuration of a BTB system is shown, which is presented in [7]. The line-frequency (50 Hz or 60 Hz) transformers play an important role in stepping down/up the voltage and in ensuring galvanic isolation between the two feeders. Especially, galvanic isolation is desirable to prevent a zero-sequence current circulating between the two feeders. However, one 6.6 kV, 1 MW transformer weighs approximately 4000 kg, and may be too heavy to be mounted on an electric pole. Accordingly, the solution with the transformers results in a large volume of the conversion system. Furthermore, the costs are quite high due to rising prices of raw materials.

1.2.2 Next-Generation BTB/SST Systems

In order to decrease the volume/weight of the BTB systems and reduce the raw material consumption new topologies [8–10], which replace the line-frequency transformers by medium/high frequency (HF) and medium/high voltage (HV) transformers, have been proposed. These proposals are based on IGBT devices which however limit the feasible switching frequencies and the voltage level of the converter systems. In order to overcome these limits, new converter systems (cf. Figure 1.6) are under investigation, which require power semiconductor switches with high blocking capability ($3\,\mathrm{kV}<V_{(BR),DSS}$) and very low switching losses enabling high switching frequencies ($25\,\mathrm{kHz}<f_s$). Such power semiconductor devices enable a much higher power density and a significantly better system dynamics/bandwidth. Due to the high operating frequency, the volume and the weight of the passive components are reduced considerably compared to the line-frequency transformers of the conventional system.

In Figure 1.6 three different topologies are shown, for realizing a solid-state transformer system based on HF and HV single-phase transformers. All concepts comprise a rectifier/inverter stage and a HF/HV dc-dc converter. In topology a) a two-level single-phase inverter/rec- tifier stage and a two-level dc-dc converter are combined in a converter cell. In order

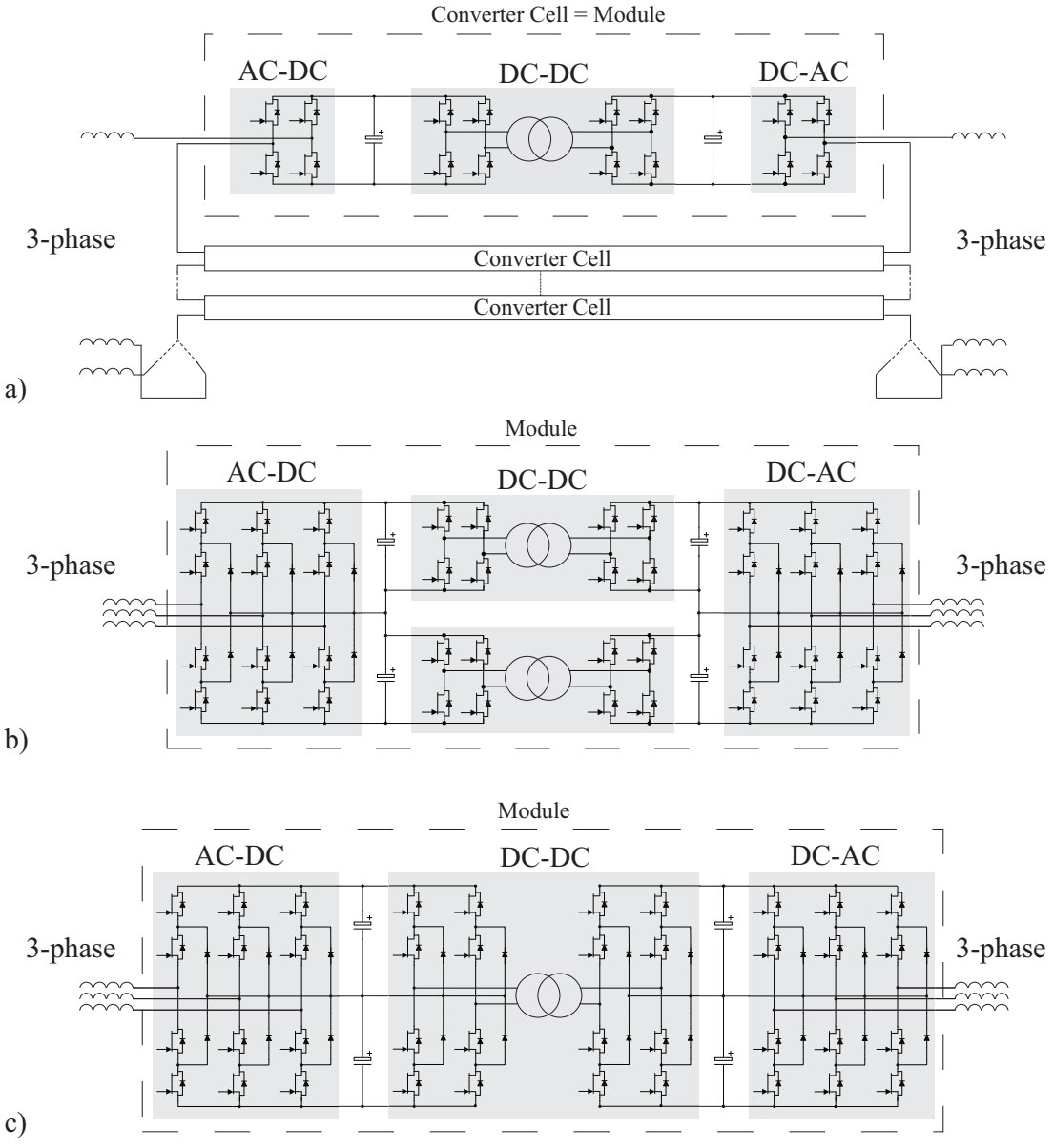

Figure 1.6: Future solid-state transformers: (a) single-phase modular converter cells, (b) three-level converter/inverter and two-level dc-dc converter and (c) three-level topology system.

to reduce the required blocking voltage of the semiconductors, several cells are connected in series. Furthermore, the three converter branches are star connected. With this concept SSTs for medium voltage level applications (11-35kV) can be realized. Based on HV/HF switches also a direct three-phase topology as shown in Figure 1.6 b) and c) could be used for ac voltages up to 10kV. Due to the reduced number of required switches the system costs are reduced and the reliability increases. There, a three-level boost rectifier/inverter stage is applied, which allows higher operating voltages than a two-level concept. In topology b) the dc-link is split into two equal voltages, so that a series connection of two two-level dc-dc converter as in topology a) is possible. There, the balancing of the two dc voltages is possible by proper control of the ac-dc stage. In topology c) three-level branches are utilized also in the dc-dc converter so that a single dc-dc converter cell is sufficient.

A key element of all topologies described above is the HF/HV dc-dc converter, which enables a significant volume reduction of SSTs compared to line-frequency concepts. Within the dc-dc converter the key components are the HF/HV switches. Therefore, the available HV semiconductor devices based on the current Si technology and HF/HV transformer are evaluated in the following. Moreover, recently investigated and developed switches based on wide band gap semiconductor material are summarized. It should be mentioned that only switches based on the SiC (representative in this thesis for wide band gap materials) are considered.

The requirements for HF/HV semiconductor devices to be employed in next-generation/SST systems and thus in general in future high power electronics systems, can be summarized with

$$\begin{aligned} 3\,\mathrm{kV} &< V_{(BR),DSS} \\ 25\,\mathrm{kHz} &< f_s. \end{aligned} \tag{1.1}$$

In addition, the devices should be available in a compact package in order to minimize the influence of parasitics.

The main focus of this thesis is to develop and investigate a HF/HV switch based on SiC technology which fulfills the specifications given in Eq. (1.1). Therefore, first of all the state-of-the-art in Si and SiC semiconductor technology is investigated and evaluated.

1.3 HF/HV Semiconductors

The following analysis and discussion of the state-of-the-art of power semiconductor devices distinguishes Si and SiC semiconductor technology.

1.3.1 Si Based Semiconductors

High voltage semiconductors play a major role in high power systems, especially in the area of power transmission and distribution and for industrial applications. The main development of power devices [11], [12] has always been focused on increasing the power ratings while improving the overall device performance in terms of losses, robustness, controllability and reliable behavior under normal and fault conditions. Figure 1.7 illustrates the power level of commercially available power semiconductors (MOSFET, IGBT, IGCT and GTO). In the megawatt range, it can be clearly seen, that three types of active switching devices are dominant; the IGCT, the IGBT and the GTO. Currently, the maximum blocking

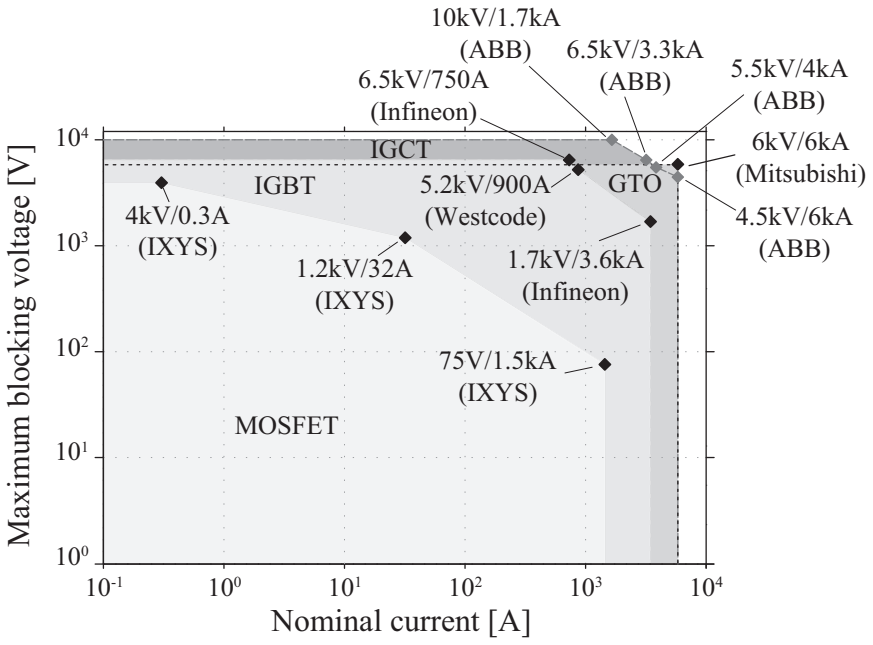

Figure 1.7: Power level of different commercially available semiconductor devices based on Si technology.

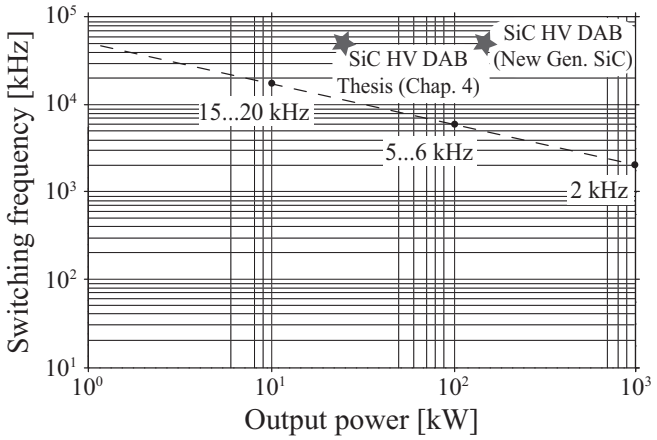

Figure 1.8: Typical switching frequencies of industrial systems employing Si power semiconductors in dependency of the power load.

voltage level of an IGCTs is 10 kV [13] and the highest current rating, with reduced blocking voltage, of an IGCT wafer is 6 kA [14]. The IGCT is the further development of the GTO thyristor and shows improved turn-off behavior. Mitsubishi [15] provides the highest power rating GTO devices at present, with nominal ratings of 6 kV/6 kA. The IGBT technology covers a large area of applications, from low power level up to megawatt systems. At this stage various voltage and current ratings of IGBT devices/modules are available, e.g. 6.5 kV/750 A or 1.7 kV/3.6 kA from Infineon [16] or 5.2 kV/900 A from Westcode [17].

In conventional BTB system high power IGBT modules, IGCT or GTO devices are required. Since these devices are based on bipolar technology, the switching speed is limited and the switching losses are higher (e.g. due to the tail current), what limits the converter efficiency and increases the costs for cooling. Part of the switching speed limitation is caused by the parasitic elements of the power modules packaging as has been shown in [18]. There, standard 4.5 kV IGBT chips for traction applications are mounted in a special low inductive housing, which allows significantly faster switching transitions than possible with standard high power modules. Due to the high switching losses at high operating frequency, especially at higher power levels, the operating frequency usually decreases with increasing voltage/power level (cf. Figure 1.8). Therefore with reference to the semiconductor requirements given in Eq. (1.1) IGCTs and GTOs are not further considered. Single IGBT and MOSFET devices with a small and/or compact package and high blocking

voltage capability up to 3 kV are available from only few manufacturers (cf. Table 1.1). However, also these semiconductors are thermally limited to switching frequencies significantly lower than 25 kHz.

The state-of-the-art analysis on Si based semiconductors (2010) shows, that there is currently no single device, nor a compact module which would offer a combined high blocking voltage capability and fast switching speed as required according to Eq. (1.1).

Series Connected Devices

The series connection of fast low-voltage power semiconductors results also in a high blocking voltage three terminal switch (gate, drain and source) and therefore offers another possibility to fulfill the semiconductor requirements of future SSTs. There are two basic series configurations well known in power electronics application; On the one side, a series connection where each power semiconductor is controlled by a single gate drive/auxiliary circuit (galvanically isolated) as illustrated in Figure 1.9 (a). On the other side, only the switch connected to the source could be directly controlled with a gate drive circuit and the upper semiconductors are indirectly controlled with an auxiliary circuit as shown in Figure 1.9 (b).

The main challenge of a series connection is the voltage distribution across the single switches which is influenced by semiconductor tolerances and parasitic layout inductances and capacitances. Furthermore, the $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ behavior reaches high values with an increased nominal voltage and should be limited with suitable circuits to acceptable values. The series connection of several devices offers the required semiconductor characteristics defined in Eq. (1.1) and is therefore further considered in Section 3.1.

	$V_{(BR),DSS}$	I_D	$E_{off}@I_D$	typ. $R_{th(j-c)}$
IXEL40N400	4 kV	40 A	220 mJ	0.33 K/w
QIS4506002	4.5 kV	60 A	170 mJ	0.1 K/w
IXTF1N400	4 kV	0.7 A	-	0.78 K/w

Table 1.1: Data sheet values of commercially available Si-based HV semiconductors.

1.3.2 SiC Based Semiconductors

Wide band gap power devices as e.g. SiC offer significant benefits compared to Si semiconductor devices. In contrast to bipolar devices, unipolar devices basically show a significantly better switching performance since only majority carriers are used for current conduction. Furthermore, the devices enable also high blocking voltages, high switching frequencies and high operation temperature to name only a few of the advantageous SiC material characteristics [21]. Some of the main physical properties which allocate SiC as a favorable power device material are compiled in Table 1.2 [22, 23].

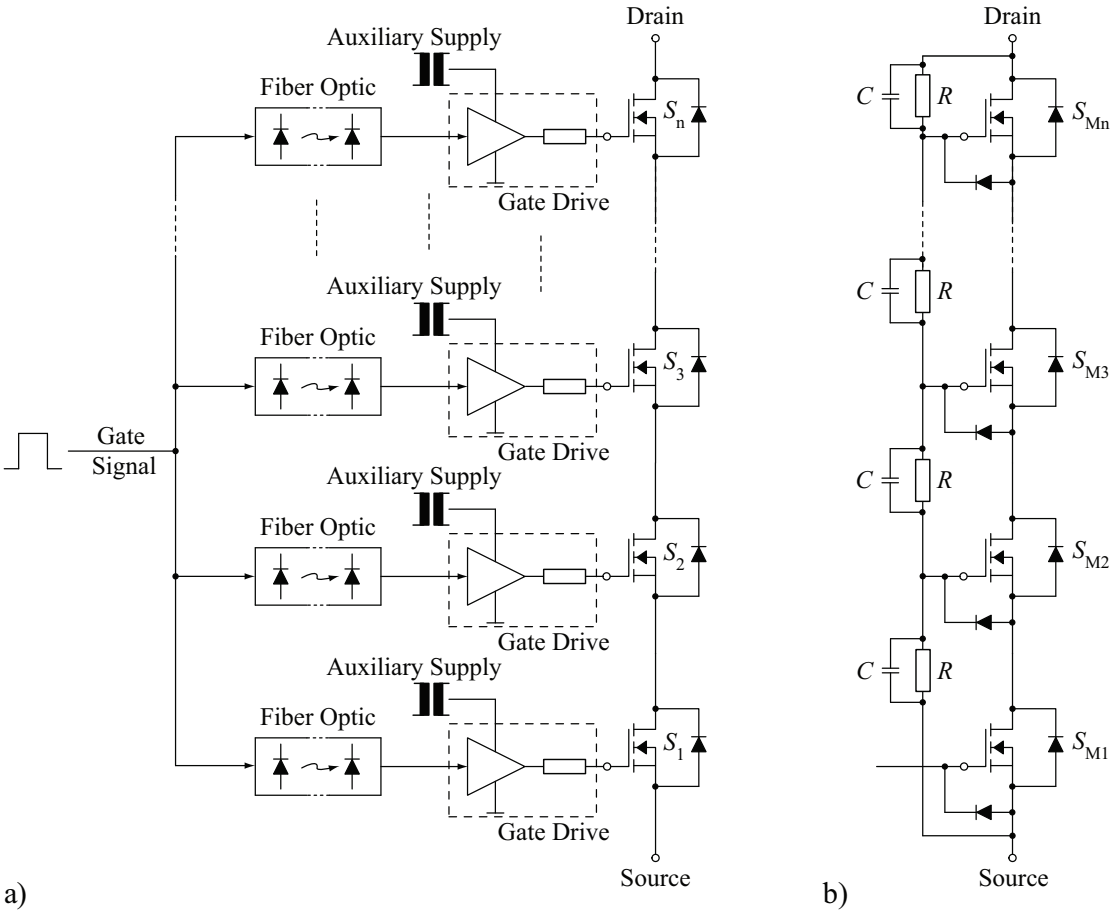

Figure 1.9: Power semiconductor devices connected in series: (a) each power switch is controlled with an individual gate unit [19] and (b) only the bottom transistor is directly controlled with a gate unit and the upper switches are indirectly controlled by an auxiliary circuit [20].

	Units	Si	4H-SiC
E_g	eV	1.1	3.26
n_i	cm^{-3}	$1.5 \cdot 10^{10}$	$8.2 \cdot 10^{-9}$
ϵ_r	-	11.8	10
μ_n	$^{cm^2}/_{(Vs)}$	1500	900
E_c	$^{MV}/_{cm}$	0.3	2.0
v_{sat}	$^{cm}/_{s}$	$1 \cdot 10^7$	$2 \cdot 10^7$
λ	$^{W}/_{(cmK)}$	1.5	4.5

Table 1.2: Physical properties of silicon and 4H silicon carbide materials [22, 23].

Over the last ten years, intensive research was performed to meet the technological challenges on the material side but also to improve the manufacturing process in order to finally produce commercial SiC power devices [24, 25]. Nevertheless, the market introduction of SiC switches was postponed several times and only the SiC Schottky diodes have been established in the market. In Table 1.3 SiC power device manufacturers and their currently available commercial products (online status) and research activities, partially in collaboration with research groups, are listed. It can be observed, that silicon carbide unipolar turn-off power devices were launched in 2009 with the SiC JFET and SiC MOSFET as main devices.

The state-of-the-art evaluation of SiC devices (status 2010) shows, that there is also no single device commercially available which combines the semiconductor requirements for future high power electronic systems (cf. Eq. (1.1)). However, recently few research activities concerning a single device were published as listed in Table 1.3 describing a 10 kV SiC MOSFET and a 6.5 kV SiC JFET. Nonetheless, as for the Si power devices, the attractive alternative of series connected power devices has to be taken into account to achieve a high blocking voltage in combination with high frequency operation.

Series stacked HV configurations

Based on the normally-on SiC JFET from SiCED an elegant and attractive perspective with a stacked high voltage switch for future high power applications is proposed in [26, 27]. The approach of a series connection

Manufacturer	Commercially Available/Research Activities(R&D)
CREE [28]	***Schottky diode (JBS):*** 600 V up to 20 A TO-220, 1.2 kV up to 20 A TO-220 1.7 kV/10 A and 25 A chip ***MOSFET:*** 1.2 kV/20 A TO-247/D^2Pak [29] (R&D) 10 kV/10 A HV package [30] (R&D)
Infineon [16]	***Schottky diode (JBS):*** 600 V up to 16 A DPak/D^2Pak/TO-220 1.2 kV up to 15 A TO-220 1.2 kV/600 A Si IGBT module
SiCED [31]	***Schottky diode (JBS):*** 1.2 kV/50 A ***VJFET (normally-on):*** 1.2 kV/20 A (released 2009) 1.2 kV/5 A and 20 A TO-220 [32, 33] (R&D) 6.5 kV HV package [34] (R&D)
Semisouth [35]	***Schottky diode (JBS):*** 1.2 kV up to 10 A TO-220, 1.2 kV up to 30 A TO-247 ***JFET (normally-off):*** 1.2 kV/ 100/63 mΩ TO-247, 1.7 kV/ 550 mΩ TO-247 ***JFET (normally-on):*** 1.2 kV/ 85 mΩ TO-247
TranSiC [36]	***Bipolar junction transistor:*** 1.2 kV/6 A and 20 A, 1.2 kV/6 A and 20 A
Rohm [37]	***Schottky diode (JBS):*** 600 V/10 A ***SiC power module:*** 1.2 kV/100 A (samples) ***SiC Trench MOSFET and DMOS:*** 300 V/300 A, 600 V/5 A up to 20 A (R&D)
Powerex [38]	***MOSFET:***(released 10/2009) 1.2 kV/100 A module (QJD1210006, QJD1210007)
GE [39]	***MOSFET:*** 1.2 kV/15 A and 30 A TO-268 [40] (R&D)
Mitsubishi [15]	R&D activities

Table 1.3: Overview of SiC device manufacturers, their offered products and research activities (R&D) respectively (Status 2010).

of JFETs is based on the well known cascode circuit [41] a combination of a low-voltage MOSFET and a normally-on SiC JFET.

This special configuration is able to reach high blocking voltages and features excellent dynamic performance and/or very fast switching behavior. However, the highest reported dynamic voltage and current measurements are only 1.2 kV/5 A although the HV stacked switch was rated to 8 kV/10 A. Above 1.2 kV there are only simulation results presented and no conclusive results regarding the static and especially the dynamic behavior of the stacked switch are reported.

Also, with the SiC MOSFET power device it would be possible to build a high voltage switch based on series connection. As for the Si technology the stacked HV switch configuration shown in Figure 1.9 b) could be used. However, due to the technical challenges of the SiC MOSFET concerning the channel mobility and the long-term reliability of the gate oxide [42,43] and the limited availability of device samples, the focus of this thesis is on the cascaded (stacked) switch approach based on the SiC JFETs which is analyzed in detail in Chapter 2 and Chapter 3. As illustrated in Figure 1.8 the performance of the stacked switch, based on wide band gap material, is well above the trend line of Si-based systems.

1.4 HV/HF Transformers

Besides the HV/HF power semiconductor switch, the design of the integrated HV/HF transformer is the other key element of next-generation and future SST systems. Due to the high operating frequencies the HF losses in the windings must be limited by a careful design, so that a high efficiency and volume of the transformer is achieved. The volume and weight reduction, as a result of high switching frequency can be estimated with applying transformer scaling laws [44]. Assuming sinusoidal current and voltage waveforms and constant current density and magnetic flux density we have for the transformer volume and weight[1]

$$V_{scalin}[dm^3] \sim \frac{1}{f^{0.75}}, \qquad m_{scalin}[kg] \sim \frac{1}{f^{0.75}}. \tag{1.2}$$

[1]Note: The transformer volume and weight trend line is valid and confirmed by various prototypes in the presented operating frequency range. However, at very high switching frequencies the thermal behavior (HF losses) will require an increase of volume and/or weight.

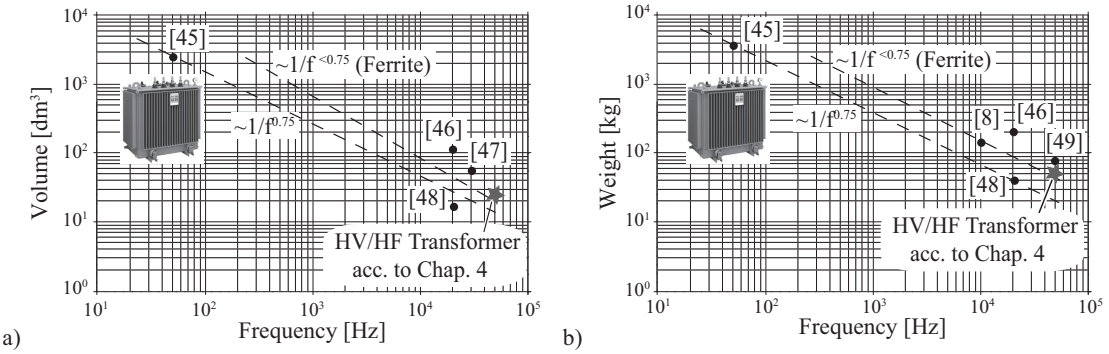

Figure 1.10: Trend line, based on 1 MVA power level, for (a) volume and (b) weight versus operating frequency,indicating the HF transformer performance (cf. Chapter 4).

In Figure 1.10, different HF transformer designs from various publications [8, 45–49] are summarized with volume, weight and operating frequency. Based on a line-frequency 1 MVA transformer (steel-iron core), the HF transformers (ferrite material) have been scaled up to the same power level. The trend line for ferrite material which allows a lower flux density compared to silicon steel is calculated by interpolation.

As illustrated in Figure 1.10, the transformer design of this thesis is located well on the trend line of transformers employing ferrite magnetic cores. The transformer design and realization are discussed and analyzed in detail in Chapter 4 and Chapter 5.

1.5 Challenges

For the development of a cascaded ultra fast high voltage switch based on SiC material and the design of a HF/HV transformer different challenges have to be addressed on the technical and safety side. The main challenges are:

- Investigation of the single SiC JFET device characteristics and the dynamic behavior of several cascaded switches, where only very limited electrical data and experimental measurements were available. Furthermore, in the early stage, SiC device tolerances (due to manufacturing tolerances) imposed an additional challenge related to the series connection of power semiconductors.

- Design and realization of a compact setup of discrete series connected high voltage devices. A major design task is to guarantee proper isolation and enough creepage distance to avoid electrical flashover.

- Control of the symmetric voltage distribution over the series connected SiC JFETs by only passive means.

- Measurement of low voltages at a reference potential of several kV or measurements of different voltages at the same time with different reference potentials which are needed for detailed investigations of inner potentials of the stacked switch.

- Design of the HF/HV transformer that withstands the electrical and thermal stresses.

- Integration of the well defined leakage inductance into the transformer, which is required to define the power transfer of the DAB converter.

- Design and construction of an overall compact demonstrator including the HF/HV transformer.

1.6 Outline of the Thesis

The goal of this research work is the application of SiC semiconductor devices in terms of a cascaded SiC HF/HV switch to realize a bidirectional, galvanically isolated 25 kW 50 kHz 5 kV/700 V dc-dc converter. The focus is on the dynamic and static evaluation of the stacked switch as well as on the design of a simulation model. In particular, the switching behavior of the SiC HF/HV switch, which is influenced by parasitic characteristics of the single semiconductor devices and coupling capacitances as well as the dynamic voltage distribution are investigated using simplified analytical models, simulation models and measurements on experimental setups and on a converter prototype.

After the introduction (**Chapter 1**), where the background and motivation of the thesis is discussed, **Chapter 2** explains the basic operation principle of the Si-SiC cascode. The normally-off characteristic of the

Si-SiC cascode is discussed, SPICE simulation models and the experimental switching behavior are analyzed. The $\mathrm{d}v/\mathrm{d}t$ behavior of the basic switch configuration and of the stacked HV switch, are discussed and novel $\mathrm{d}v/\mathrm{d}t$ control methods are proposed. Lastly, the power losses of the Si-SiC cascode switch are calculated based on experimental measurement results.

Chapter 3 presents the development and investigation of the Si MOSFET/SiC JFET SuperCascode (stacked SiC HF/HV switch). Different operating conditions (static/dynamic operation, inductive/resistive load, low/high load current, room/high temperature operation) are experimentally tested and compared to SPICE simulations and analytical calculations. The passive control mechanism of the stacked switch configuration is analyzed in detail and main influencing factors are evaluated. Switching loss measurement are performed and energy loss functions are determined. Finally, the avalanche capability of the novel switch is discussed based on simulation results.

In **Chapter 4** the specifications and the electrical design of the bidirectional 25 kW 50kHz dc-dc converter based on the Si-SiC SuperCascode is presented. A complete power loss analysis, of the active as well as of the passive elements is elaborated.

Chapter 5 describes the realization of the converter prototype and the achieved experimental results. The dc-dc converter operates with phase-shift modulation and a switching frequency of 50 kHz.

Finally, **Chapter 6** summarizes the achieved results and discusses future prospects of Si MOSFET/SiC JFET SuperCascode switches.

1.7 Scientific Contributions

The main contributions of this thesis are summarized in the following. Most of these results have been published at international conferences or in IEEE Transactions as listed in Section 6.2.

- A novel $\mathrm{d}v/\mathrm{d}t$ limitation methods for the Si-SiC MOSFET/JFET cascode are proposed. Based on this new concepts the outstanding performance of SiC devices can be fully utilized for realizing hard commutated switches as required e.g. on the PFC rectifier stage of telecom power supply modules.

- An ultra fast, high voltage switch based on SiC material is investigated, including novel auxiliary circuits, which are required for proper operation and voltage sharing of the cascaded devices. The dynamic and static behavior of the HV switch is evaluated in detail and verified with experimental measurements.

- Design, development and construction of a HF/HV transformer which integrates a well defined leakage inductance for future applications of SST.

- First discrete realization of a complete SiC high voltage switch, denominated as Si-SiC SuperCascode, which is mainly passively controlled by balancing diodes and verification of the excellent transient switching behavior at a nominal voltage of 5 kV with switching times less than 100 ns. Furthermore, testing of the HF/HV SiC switch in continuous mode operation in a medium voltage DAB dc-dc converter.

Chapter 2

Si-SiC Cascode Switch

In 1920, the cascode topology was invented to handle the Miller effect in triode amplifiers [50] and after the invention of the transistors in 1947, in common-emitter transistor amplifiers. The earliest reference to a cascode topology using transistors was found so far in a paper from 1960 entitled "Analysis of the transistor cascode configuration" [51]. The composite pair, another cascode configuration known as the Baliga-Pair, i.e. of a normally-on and normally-off power semiconductor was invented by Baliga in 1982 [52]. The development and the investigations of the wide band gap materials in an extension of the cascode topology in 1997 [53]. This concept of a multi-stage switch and/or Si-SiC SuperCascode (cf. Chapter 3) is further investigated in this thesis.

2.1 Si-SiC Cascode Configuration

As the evaluation of current semiconductor power switches and the requirements on the future semiconductor devices shows (cf. Section 1.3), power switches, based on wide band gap materials, provide attractive electrical characteristics for an operation at high power levels and at high operating frequencies. In particular, the normally-on SiC JFET (SiCED, [31]) offers very fast transient behavior, with a blocking voltage of 1200 V. The experimental evaluation of the SiC JFET performance [54, 55] in comparison to state-of-the-art MOSFETs/IGBTs, clearly identifies the

JFET as an alternative switch in various applications (e.g. photovoltaic converter topologies, [56]). However, the normally-on behavior of the SiC JFET prevented fully acceptance for industry applications [57, 58] so far, although improved gate drive circuits have been developed [59–63].

A normally-off behavior can be achieved by using the normally-on device in a cascode configuration [41] where a low-voltage normally-off MOSFET is connected in series with the 1200 V SiC JFET, as presented in Figure 2.1, without compromising the excellent characteristics of the SiC device [64]. A number of research groups investigated the cascode configuration in an optimized single package. There, the low-voltage MOSFET chip and the SiC JFET chip are mostly packaged in an ISOPLUS $i4^{TM}$ [65] or in customized packages as e.g. in an EasyPack 2B power module [66]. This thesis analyzes the Si-SiC cascode and performs the experimental measurements with discrete devices. The same approach is used for the stacked HV switch described in Chapter 3.

2.1.1 Low-Voltage Si MOSFET

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) [67] is a voltage controlled device and is used in the cascode configuration for changing the normally-on characteristic of the SiC JFET into a normally-off characteristic of the Si-SiC cascode. The MOSFET semiconductor material could be either Si or SiC. A SiC MOSFET would have to be selected if the specifications require operation at high temperature [68]. In this case also the package has to be able to withstand high temperatures. As high temperature packages are currently not available the utilization of a SiC MOSFET and/or the realization of a SiC-SiC cascode is not considered further.

A tremendous diversity of low-voltage Si MOSFET is available on the market, which could be used in the cascode topology. But not each Si MOSFET influences the dynamic switching behavior in the same way, as will be discussed in Section 2.5 and Section 2.6. Therefore, the selection of the low-voltage MOSFET could be optimized with respect to switching behavior, power losses, minimal influence of parasitic inductances or costs.

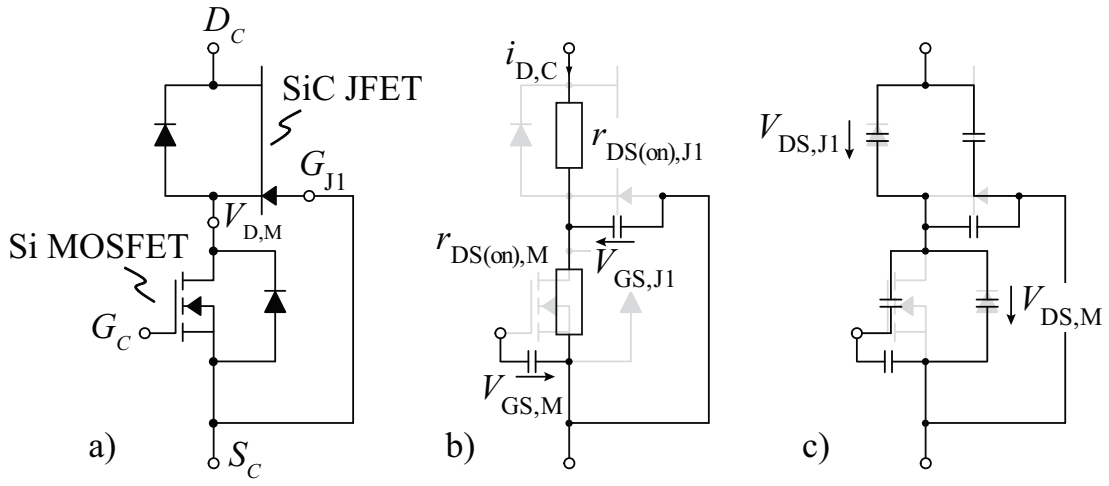

Figure 2.1: Low-voltage Si MOSFET SiC JFET cascode: (a) cascode switch topology, (b) equivalent circuit for conduction mode ($V_{GS,M} > V_{th}$) and (c) for blocking mode ($V_{GS,M} < V_{th}$).

2.1.2 SiC JFET

The Junction Field Effect Transistor (JFET) [67] like the MOSFET is a voltage controlled device and is utilized in the cascode configuration, to block the high voltage. The JFETs evaluated and investigated in this thesis, are manufactured and developed by SiCED [31] and are characterized as a normally-on, vertical JFETs with lateral channel. This structure combines the advantages of two previous developed vertical JFET structures [23] (trade-off between extremely low on-resistance against large drain-gate 'Miller' capacitance) and provides reverse current flow capability by the integrated body diode. The SiC JFET voltage and current rating is 1200 V/5 A. The device is available in a standard TO-220 package and the integrated die size is 2.4 mm by 2.4 mm. Additional basic characteristics (determined by SiCED) of the SiC JFETs employed in the test setups are listed in the Appendix A.

It is important to note that the first generation of SiC JFETs showed a large variation in the pinch-off voltages, ranging from -9.4 V to -23.9 V. With respect to these device tolerances, developing a cascaded switch is especially challenging as will be discussed in Chapter 3. However, in the meantime the fabrication and production processes of SiC devices could be improved and the considered variation of the device characteristics is nowadays not existing any more. In addition, also the maximal blocking

voltage level, previously varying from 1.25 kV to 1.86 kV, is well defined in the meantime.

2.2 Basic Operation Principle (Static)

Based on the composite topology of the Si-SiC cascode, the operation is depending on the normally-off MOSFET transistor and on the normally-on JFET transistor characteristics. Only the low-voltage MOSFET is actively controlled, whereas the SiC JFET is passively controlled by the MOSFET drain-source voltage. In the following, the three steady state conditions, namely conduction, blocking and reverse conduction mode of the Si-SiC cascode are analyzed. The equivalent circuits of the conduction and blocking mode are shown in Figures 2.1 (b) and (c).

Conduction Mode

In the on-state of the Si-SiC cascode, a positive gate-source voltage ($v_{GS,M} > V_{th,M}$) is applied to the low-voltage MOSFET. Thus, the MOSFET channel is conducting and behaves like an ohmic resistor. Resulting is a voltage drop across the on-resistance of

$$v_{DS,M} = i_{D,C} \cdot R_{DS(on),M}. \tag{2.1}$$

The SiC JFET gate-source voltage is the negative drain-source voltage of the low-voltage MOSFET,

$$v_{GS,J1} = -v_{DS,M} < 0\,\mathrm{V}, \tag{2.2}$$

because the gate of the SiC JFET G_{J1} is connected to the source of the MOSFET. Accordingly, the gate-source voltage of the JFET is controlled by the drain-source voltage of the MOSFET and depending on the MOSFET conduction state and/or on the drain current $i_{D,C}$ and the on-resistance of the MOSFET $R_{DS(on),M}$. Considering the wide variety of available low-voltage MOSFETs, optimized MOSFETs with very low on-resistance can be applied. Due to the limited current capability of todays SiC JFET devices, the resulting gate-source voltage of the SiC JFET is then,

$$v_{GS,J1} \approx 0\,\mathrm{V}. \tag{2.3}$$

Due to the normally-on behavior of the SiC JFET, the channel is conducting and behaves like the MOSFET as an ohmic resistor. Therefore, the total drain-source voltage of the Si-SiC cascode in conduction mode is calculated to

$$v_{DS,C} = i_{D,C} \cdot (R_{DS(on),M} + R_{DS(on),J1}). \tag{2.4}$$

Blocking Mode

In the blocking state a negative gate-source voltage is applied to the MOSFET ($v_{GS,M} < V_{th,M}$). The drain potential of the MOSFET $v_{D,M}$ increases up to the SiC JFET pinch-off voltage $V_{p-off,J1}$. Thus, the drain-source voltage of the low-voltage MOSFET is equal to the pinch-off voltage of the SiC JFET

$$v_{DS,M} = -v_{GS,J1} = V_{p-off,J1}. \tag{2.5}$$

The SiC JFET channel is completely depleted and the high voltage of the Si-SiC cascode switch occurs across the SiC JFET as desired.

$$V_{DS,M} << V_{DS,J1} \approx V_{DS,C} \tag{2.6}$$

Reverse Conduction - Freewheeling Mode

The third state of the Si-SiC cascode is the reverse conduction mode. The low-voltage MOSFET is able, due to its internal structure, to conduct the freewheeling current $i_{revD,C}$ through the parasitic anti parallel diode, whereas the on-resistance $R_{D(on)}$ and the forward voltage drop v_{FD} of the diode have to be considered, but also through the MOSFET channel if a positive gate voltage is applied. Therefore, the gate-source voltage of the SiC JFET is depending on the conducting device (MOSFET channel, anti parallel diode). Hence, $v_{GS,J1}$ can be expressed with

$$v_{GS,J1} = \begin{cases} i_{revD,C} \cdot R_{DS(on),M} & \text{if, } V_{GS,M} \geq V_{th,M} \\ i_{revD,C} \cdot R_{D(on),M} + v_{FD,M} & \text{if, } V_{GS,M} < V_{th,M}. \end{cases} \tag{2.7}$$

In Eq. (2.7) the case of a high reverse current $i_{revD,C}$ is not considered, where in case of $v_{GS,M} \geq V_{th,M}$ also the diode is conducting due to a high voltage drop across the MOSFET channel.

However, the SiC JFET is always turned-on during freewheeling operation ($v_{GS,J1} > 0V$) an acts as a simple resistor. The turn-on of the SiC JFET body diode is unlikely, due to the high forward voltage $v_{FD,J1}$ of about 2.8 V. The freewheeling current will flow through the JFET channel and the conduction losses are only caused by the $R_{DS(on),J1}$ of the JFET. Therefore, the SiC JFET channel is conducting if the following condition is fulfilled

$$R_{DS(on),J1} \cdot i_{revD,C} < v_{FD,J1} \approx 2.8\,\mathrm{V}. \tag{2.8}$$

If the voltage drop across the SiC JFET channel exceeds $v_{FD,J1}$ the body diode is starting to participate in the current conduction, but carrier lifetime in SiC devices is very short and therefore only small recovery current can be observed.

The Si-SiC cascode freewheeling operation offers considerable advantages compared to existing silicon solutions. The internal body diode of a low-voltage (30 V to 50 V) MOSFET is characterized by a small reverse recovery charge and/or short recovery time in contrast to high voltage silicon MOSFETs [69].

2.3 SiC JFET SPICE Simulation Model

An accurate and physics/behavioral based SPICE model of the SiC JFET semiconductor is required and greatly useful for power electronic circuit simulations. Especially, in case of composite circuits (Si-SiC cascode / Si-SiC SuperCascode) the application of SPICE models are favored due to following reasons:

- The dynamic behavior of series connected semiconductor devices depends strongly on parasitic capacitances defined by the structure of the transistor. Accordingly, the experimental circuit will change the dynamic behavior with connecting e.g. voltage measurement probes with finite input capacitances. The simulation circuit allows the analysis of voltages without influence on the measured circuit.

- Various currents and voltages can be observed easily, simultaneously and without time deskew during the simulation run.

- Accurate simulation models are important for developing new power circuits, because they provide: a fast overview about the basic and advanced operation principle; cost-savings as no hardware has to be built for understanding e.g. the dynamic behavior; high safety concerning the power/voltage ratings in laboratories and a fast way to change parts of the power circuit or just component values e.g. of a snubber circuit.

- A compact design of converter prototypes leads to high power density, but limits the space and complicates the access to important measurement points during the experimental analysis of power converters. A SPICE simulation run can clarify in advance most of the critical operating points. Afterwards in the experimental analysis of the prototype, these measurement points can be considered.

Currently, various SiC JFET SPICE models are published and verified with experimental measurements. Depending on different characteristics, i.e physical semiconductor design and packaging different SPICE models are resulting. In relation to the semiconductor power switch investigated in this thesis only the SPICE models of normally-on SiC JFETs in a TO-220 packaged and manufactured by SiCED are considered.

Wang et al. [70] published a SPICE model which is based on static and dynamic characterization of a 1.2 kV, 5 A 4H-SiC power JFET from SiCED. The SPICE model parameters (intrinsic and extrinsic parameters) are extracted from experimental measurements. Reasonably good agreement is obtained between the modeled and experimental results. SiCED [71] developed different SPICE models (Symetrix platform) based on experimental measurements of a 1200 V/400 mΩ JFET and a 1200 V/ 100 mΩ JFET. The SPICE models are described by an empirical function using voltage controlled current sources. The output characteristics of both SPICE models are shown in Figure 2.2. Obviously, the characteristics are different in the ohmic region as also in the saturation region. Therefore, it has to be considered that the SPICE model from Wang has been developed in 2006 and the model from SiCED in 2009. During that time, various development and growing processes of SiC wafers have been improved and therefore the SiC JFET dies have changed their basic characteristics. The characteristic behavior of the SiC JFET body diode is provided by the SiCED model. Even the possibility of reverse current flow through the JFET channel ($v_{GS,J1}$= 0 V) is considered. The Wang

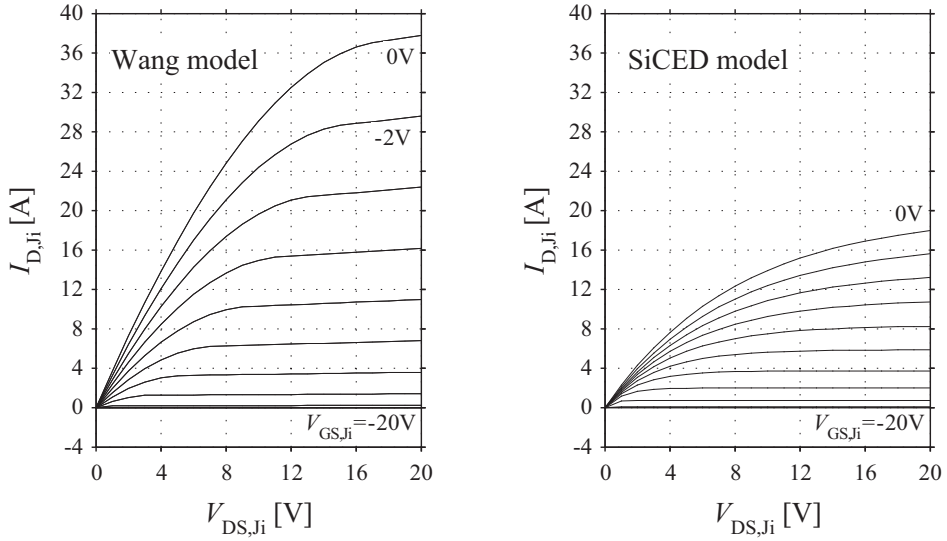

Figure 2.2: Output characteristics of the SPICE SiC JFET models: Intrinsic model from Wang (V_{p-off}=-17.36 V) and empirical model from SiCED (V_{p-off}=-19 V).

model assumes ideal reverse current conduction of the body diode.

Numerous transient simulation runs of the SPICE SiC JFET models have shown, that they are working properly, when included into the power circuit as a single device and controlled directly by the gate of the SiC JFET. However, simulation circuits built with several series connected devices result in numerical instabilities with the SiCED model. Therefore, the Wang SPICE model has been selected for the Si-SiC cascode and the Si-SiC SuperCascode simulations, although the SiCED SPICE model represents more accurate the latest SiC JFET generation. In the following section further differences concerning the dynamic behavior of the SPICE models are evaluated and compared with experimental measurements.

MOSFET SPICE model

Most manufacturers of Si low-voltage MOSFETs provide accurate and stable SPICE models. For the low-voltage MOSFETs used in all the experimental prototypes and experimental setups in this thesis, SPICE models are available from the corresponding manufacturers homepage.

2.4 Experimental Setup and Measurements

An experimental setup shown in Figure 2.3 has been built for the Si-SiC MOSFET/JFET cascode to investigate the fast transient switching behavior and to analyze the switching losses. The experimental tests have been performed with a buck topology. Therefore, the setup consists of capacitors stabilizing the dc-link voltage, a half bridge consisting of a Si-SiC MOSFET/JFET cascode and a SiC diode and a standard MOSFET gate drive circuit. Due to high dc-link voltage, the transfer of the gate signal is realized with a fiber optic transmitter/receiver. Furthermore, an auxiliary power supply is accommodated on the board feeding both, gate driver and the fiber optic receiver.

The transient behavior of the Si-SiC cascode, measured with the experimental setup shown in Figure 2.3, is presented in Figure 2.4. At the beginning of the turn-on transient, the load current is commutating from the SiC diode to the Si-SiC cascode. The Si-SiC cascode current $i_{D,C}$ shows a capacitive current peak which rises to a peak value of 17 A, while the blocking voltage decreases. The drain-source voltage $v_{DS,C}$ de-

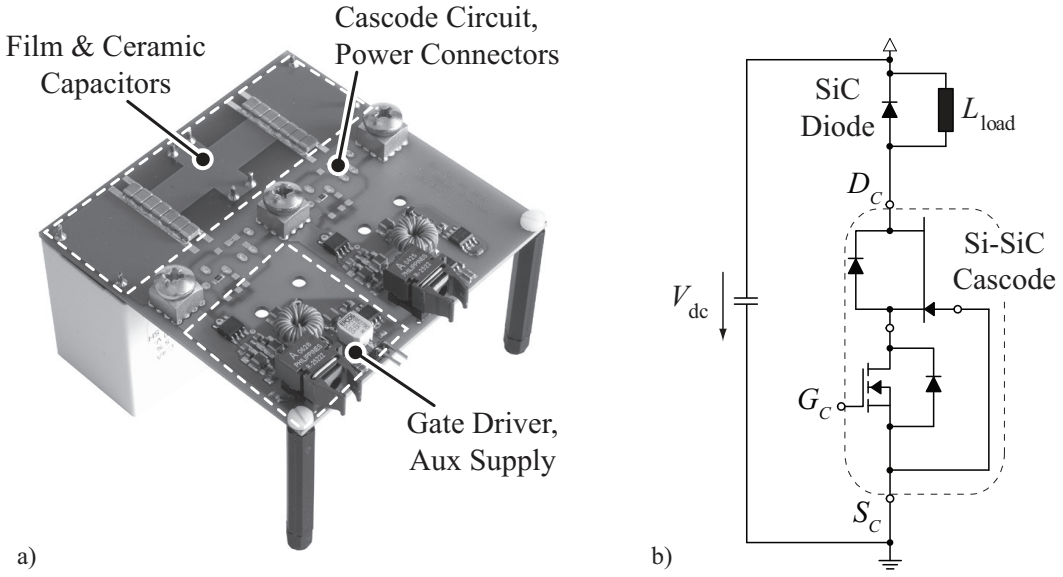

Figure 2.3: (a) Experimental setup to investigate the dynamic switching behavior of the Si-SiC cascode. (b) Schematic of the experimental circuit (buck topology).

creases very fast with a voltage slop of $\mathrm{d}v/\mathrm{d}t = 45\,\mathrm{kV}/\mu\mathrm{s}$[1]. The turn-off transient at a current level of 11 A is characterized by almost a perfect current and voltage waveforms during the commutation. The voltage rate of change is slightly lower than at turn-on, but still reaches $\mathrm{d}v/\mathrm{d}t$ values up to $40\,\mathrm{kV}/\mu\mathrm{s}$. The detailed transient behavior of the Si-SiC cascode is evaluated and discussed in Section 2.5.

In Figure 2.5 the time behavior of the Si-SiC cascode drain-source voltage $v_{DS,C}$ at turn-on and turn-off is shown for different load currents. The load current i_L is varied from 1.8 A to 9 A. At turn-on, the voltage rate of change in time is independent of the load current and the same $\mathrm{d}v/\mathrm{d}t$ values are resulting for all the measurements. The turn-off transient shows, that the $\mathrm{d}v/\mathrm{d}t$ is determined by the load current and the parasitic capacitances. Therefore, the $\mathrm{d}v/\mathrm{d}t$ values of $21\,\mathrm{kV}/\mu\mathrm{s}$ at low load current and goes up to $37\,\mathrm{kV}/\mu\mathrm{s}$ at increased load current.

[1] **Note:** $\mathrm{d}v/\mathrm{d}t$ denotes the voltage variation in the time interval from 90 % to 10 % of the applied dc-link voltage V_{dc}.

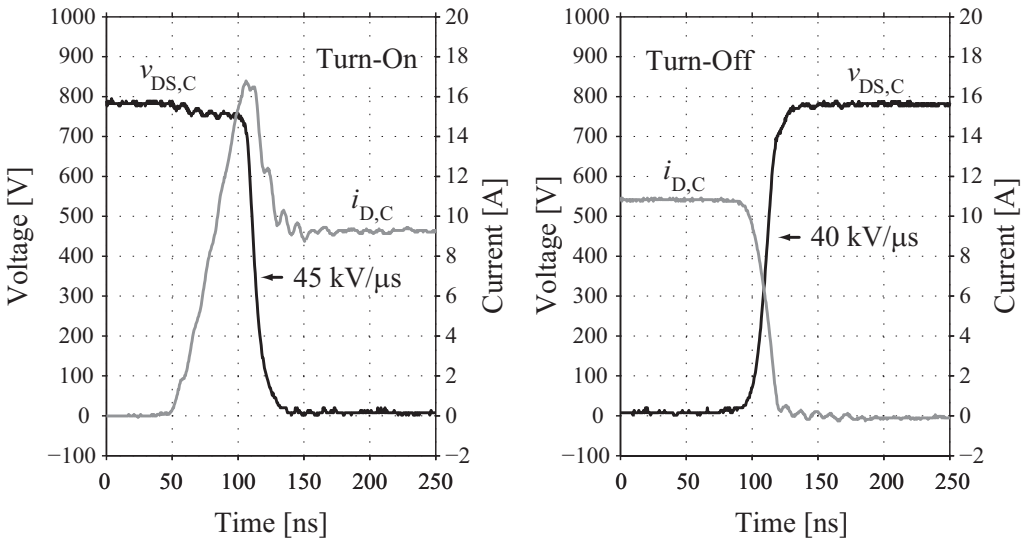

Figure 2.4: Switching behavior of the Si-SiC MOSFET (IRLR024N)/JFET cascode at $V_{dc} = 800\,\mathrm{V}$/ $i_{D,C} = 9\,\mathrm{A}/11\,\mathrm{A}$. Proper hard switching behavior at turn-on and turn-off (where the parasitic output capacitance of the switch takes effect on the voltage time behavior).

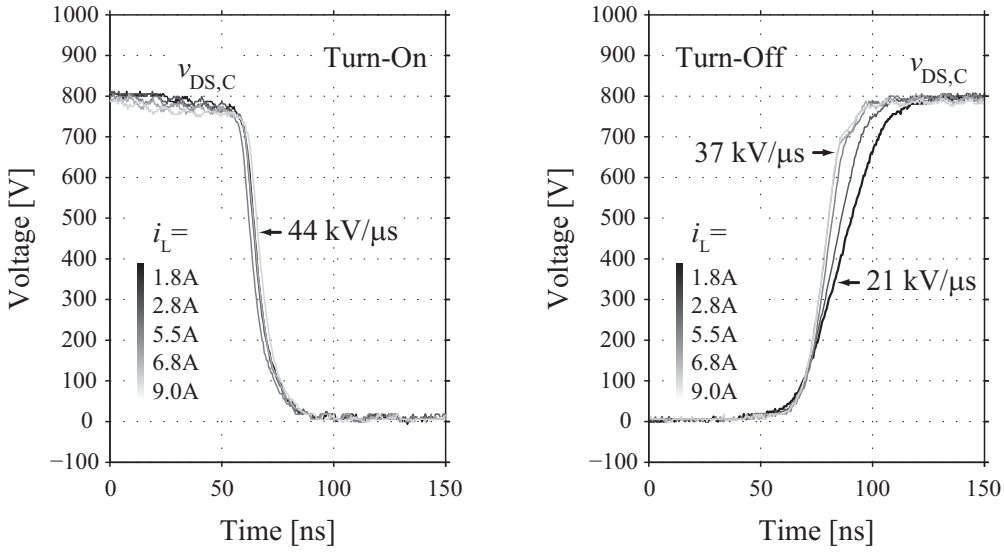

Figure 2.5: Measurement result of the Si-SiC cascode at $V_{dc} = 800\,\mathrm{V}$ and different load currents i_L for turn-on and turn-off.

2.5 Si-SiC Cascode dv/dt Control

As a result of extremely fast voltage edges and corresponding high di/dt values, resulting for hard switching of the Si-SiC cascode (cf. Figure 2.4), the effort for ensuring a low-inductive layout avoiding switching-related overvoltages is increasing. In [72] overvoltages are occurring due to parasitic and not avoidable module and layout inductances (cf. Figure 2.6). Furthermore, a controllability of the voltage rise time in switching transients of the Si-SiC cascode is valuable concerning EMI/EMC filtering [73]. Especially in drive systems, transients with hard commutation reaching values of up to $45\,^{\mathrm{kV}}/_{\mu\mathrm{s}}$, could lead to EMC problems and to earth currents (bearing currents) due to parasitic capacitive coupling between stator and rotor. Therefore, dv/dt control methods for the Si-SiC MOSFET/JFET cascode have been investigated.

2.5.1 Conventional dv/dt Limitation Techniques

For currently, frequently used semiconductors as Si MOSFETs and IGBTs, several techniques [74] to reduce and control the dv/dt at fast switching edges are well known as shown in Figure 2.7. The most simple and applied dv/dt control method is the external gate resistor $R_{G,M}$,

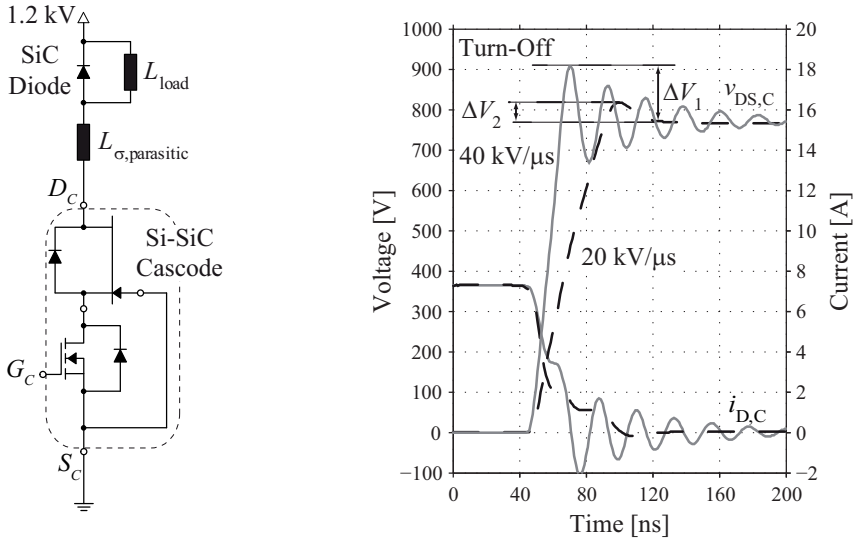

Figure 2.6: Simulation result of the Si MOSFET (IRLR024N)/SiC JFET cascode with an assumed unfavorable layout ($L_{\sigma,parasitic}$). The solid line illustrates the fast switching behavior of the conventional cascode topology. With the novel methods (cf. 2.5.2) a reduced $\mathrm{d}v/\mathrm{d}t$ is achievable, which also leads to a reduced $\mathrm{d}i/\mathrm{d}t$ and therefore, also the overvoltage is reduced $\Delta V_2 \ll \Delta V_1$ (dashed line).

where the optimal resistance value is selected based on the switching behavior of the corresponding semiconductor. In [75] a new active gate control method is presented, which allows to control the $\mathrm{d}v/\mathrm{d}t$ at turn-off by acting directly on the input gate voltage shape (2-or 3-step gate voltage). A more complex active gate control method is published in [76], where an additional external (artifical) Miller capacitance is electronically adjusted to the effective gate-drain capacitance. Finally, an advanced method is introduced in [77], where the current of the external Miller capacitance is electronically controlled and at the same time the optimal control for minimal switching losses is calculated.

Most of these $\mathrm{d}v/\mathrm{d}t$ limitation methods are based on the Miller effect of an increased input capacitance at the switching events. For each turn-on and turn-off switching the gate-source and the drain-source capacitance has to be charged and discharged. Applying the considered conventional $\mathrm{d}v/\mathrm{d}t$ limitation techniques to the Si-SiC cascode doesn't result in the desired behavior of reducing the fast switching voltage edges. The reason is the series connection of the low-voltage Si MOSFET and

the SiC JFET. The conventional methods only influence the behavior of the actively controlled low-voltage Si MOSFET as analyzed in the following.

Si-SiC Cascode

To investigate the influence of the conventional methods on the Si-SiC cascode configuration, a simulation setup (cf. schematic of the experimental setup in Figure 2.3) with $Simplorer^{TM}$ is implemented. There, standard SPICE models supplied by the manufacturers are used for the low-voltage MOSFET [78] and the freewheeling SiC Diode [28]. The SPICE model applied for the SiC JFET is discussed in Section 2.3.

The SPICE simulation is performed with the standard dv/dt control method, i.e. different gate resistors $R_{G,M} = 15\,\Omega$ and $R_{G,M} = 3\,\Omega$. It should be noted that similar simulation results could also be achieved with a 2 or 3-step voltage or an additional drain-gate capacitor $C_{DGa,M}$ (artificial increase of the Miller capacitance) of the low-voltage Si MOSFET.

The conventional techniques influence only the turn-on and turn-off behavior of the low-voltage Si MOSFET as demonstrated in Figure 2.8 with SPICE simulation results. Illustrated are the turn-on and turn-off

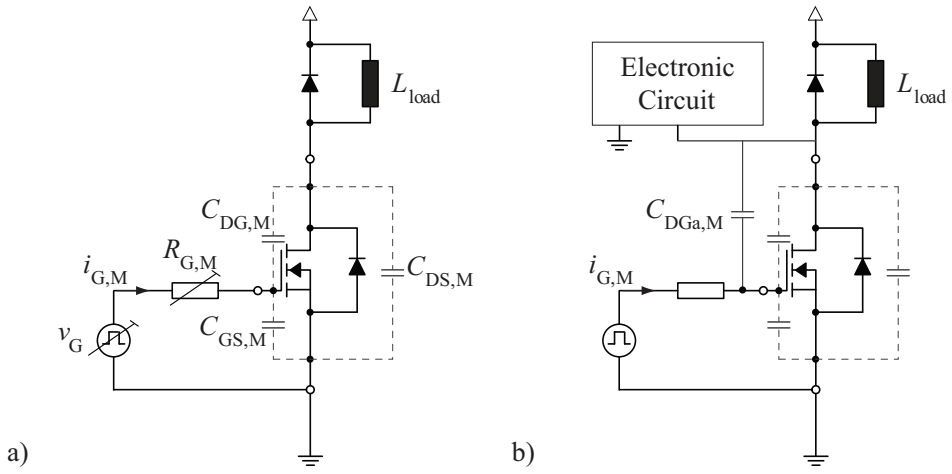

Figure 2.7: Frequently used dv/dt limitation methods for MOSFET and IGBT switches; (a) Varying gate resistor and 2- or 3-step controlled gate voltage. (b) Additional drain-source capacitor $C_{DGa,M}$ causing an increased negative Miller feedback.

switching behavior at load currents of 4 A (hard turn-on switching) and 7.5 A (turn-off transient) for two different low-voltage MOSFETs specified in Table 2.1. The MOSFET type *IRLR024N* is characterized by low capacitance values of several hundred pF and the MOSFET *IRF2804* exhibits an extremely low on-resistance of $2\,m\Omega$. Depending on the MOSFET capacitance values (C_{iss}, C_{oss} and C_{rss}) and the gate resistance $R_{G,M}$ the charge and discharge behavior of $C_{iss,M}$ is drastically influenced as can be observed by the gate-source voltage $v_{GS,M}$. Also the MOSFET drain-source voltage is strongly influenced as expected and well known in power electronic circuits. However, there is only a marginal change in $\mathrm{d}v/\mathrm{d}t$ behavior of the Si-SiC cascode.

The standard/conventional methods, to control the $\mathrm{d}v/\mathrm{d}t$ value of the Si-SiC cascode, influence the drain-source voltage edge of the JFET insignificantly as illustrated in the third simulation result. The impact of the different gate resistors is the starting time of the rise and fall event of the drain-source voltage $v_{DS,J1}$. In this case the delay times (t_{on}, t_{off}) can be controlled by the conventional techniques, but the $\mathrm{d}v/\mathrm{d}t$ of the drain-source voltage is not influenced, independent of the MOSFET type and the applied conventional techniques.

Si Low-Voltage MOSFET - Optimal Si-SiC Cascode

In order to identify an optimal MOSFET for the Si-SiC cascode, two MOSFETs as given in Table 2.1 are analyzed. The MOSFET's maximal voltage ratings of 55 V/40 V are suitable for the Si-SiC cascode configuration and should not be lower than 35 V. Otherwise, the MOSFET is probably running into avalanche mode, which should be avoided in repet-

	IRLR024N (M1)	***IRF2804*** (M2)
$V_{(BR),DSS}$	55 V	40 V
$I_D@T_c = 25\,°\mathrm{C}$	17 A	75 A
$R_{DS(on)}@V_{GS,M} = 10\,\mathrm{V}$	$65\,\mathrm{m}\Omega@I_D = 10\,\mathrm{A}$	$2\,\mathrm{m}\Omega@I_D = 75\,\mathrm{A}$
$C_{iss}@V_{DS,M} = 0$	680 pF	7800 pF
$C_{oss}@V_{DS,M} = 0$	480 pF	5000 pF
$C_{rss}@V_{DS,M} = 0$	230 pF	2100 pF

Table 2.1: Main characteristics of the selected low-voltage MOSFETs from International Rectifier.

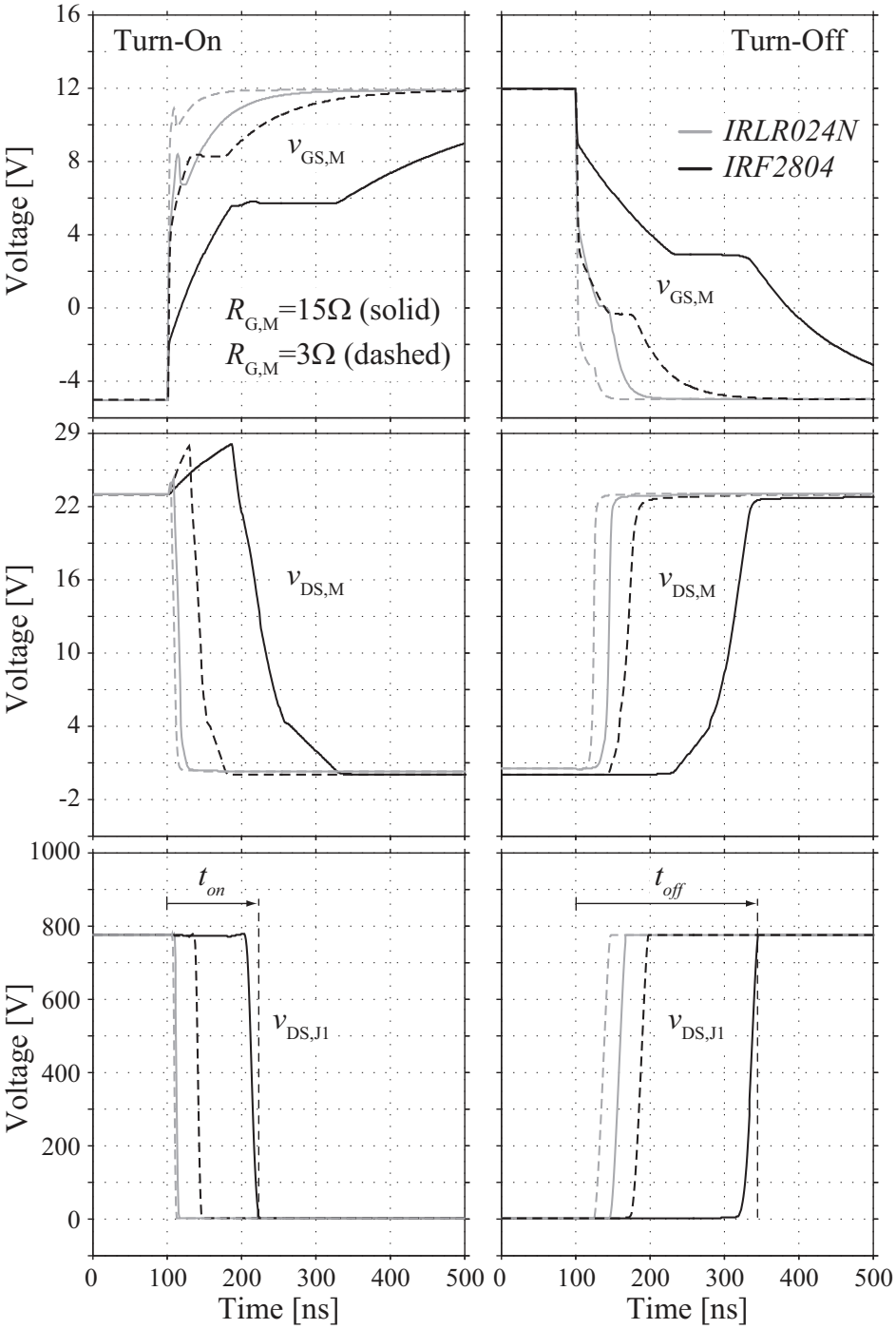

Figure 2.8: Si-SiC cascode simulation results using conventional dv/dt limitation techniques with different gate resistors (3 Ω dashed line, 15 Ω solid line). The voltage rate of change of the Si-SiC cascode is not controllable with conventional methods as illustrated by the equal dv/dt of the corresponding SiC JFET drain-source voltages.

itive operation. The current rating of MOSFET *IRLR024N* 17 A@25 °C is much smaller than of MOSFET *IRF2804* 75 A@25 °C. Resulting is a smaller die size and therefore a larger on-resistance of 65 mΩ compared to MOSFET *IRF2804*. In contrast, the capacitance values of MOSFET *IRF2804* are larger than those of MOSFET *IRLR024N* and result in unfavorably long turn-on and turn-off switching times (cf. Figure 2.8) and/or significantly delay times (t_{on},t_{off}) before the main switching action of the Si-SiC cascode takes place. Accordingly, the switching losses are higher than for the MOSFET *IRLR024N*. In addition, the reverse recovery losses of the corresponding anti parallel body diodes must be taken into account of an optimal design. The following equations express in general the power losses which occur in MOSFET devices, where $i \in (1, 2)$ indicate $M1$ and $M2$:

MOSFET and diode conduction losses:

$$P_{c,Mi} = I^2_{D(rms),Mi} \cdot R_{DS(on),Mi} \tag{2.9}$$

$$P_{cD,Mi} = V_{FD,Mi} \cdot I_{revD(avg),Mi} + R_{D(on),Mi} \cdot I^2_{revD(rms),Mi} \tag{2.10}$$

Switching and reverse recovery losses:

$$P_{sw,Mi} = f_S \cdot (E_{on,Mi} + E_{off,Mi}) \tag{2.11}$$

$$P_{rrD,Mi} = f_S \cdot E_{rrD,Mi} \tag{2.12}$$

In applications with ultra high operating frequencies the switching losses are preferably minimized and the switching times should be as short as possible. Accordingly, a MOSFET type corresponding to $M1$ is preferably selected. Furthermore, taking into consideration the current rating of todays SiC devices and their relatively large on-resistance of $R_{DS(on),J} \approx 0.3\,\Omega$ compared to low-voltage MOSFETs supports the choice of MOSFET type $M1$. Therefore, the favored MOSFET towards an optimal cascode configuration results in a somewhat larger on-resistance but lower switching losses.

2.5.2 Novel dv/dt Limitation Methods

For the Si-SiC cascode topology novel methods to control the dv/dt are investigated. Resulting are two concepts to slow down the very fast voltages edges at turn-on as well as at turn-off. In Figure 2.9 the novel

topologies for the cascode configuration to control the dv/dt behavior are shown. On the one hand, the idea of the novel topology is based on the conventional technique of a MOSFET/IGBT to reduce the dv/dt values with an additional capacitor $C_{DG,C}$ from the JFET drain to the MOSFET gate and/or with increasing the input capacitance (cf. Figure 2.9 (a)). On the other hand, an RC-Circuit (R_{damp},$C_{DGa,J1}$) is increasing the input capacitance of the SiC JFET and the additional gate resistor $R_{GS,J1-M}$ slows down the turn-on behavior of the JFET (cf. Figure 2.9 (b)). Both novel dv/dt control methods are analyzed in detail and verified with experimental measurements in the following.

Drain-Gate Capacitor $C_{DG,C}$ (Concept A)

The additional capacitor $C_{DG,C}$ is connected between the MOSFET gate and the JFET drain or the Si-SiC cascode drain. The effect of this capacitor is the same as for a single discrete switch; the negative feedback of the Miller capacitance is increased and therefore it takes longer to complete the dynamic switching for an equal current provided by the gate driver. Therefore, the dv/dt controlling concept with the additional drain gate capacitor $C_{DG,C}$ is based on the conventional method of the MOSFET.

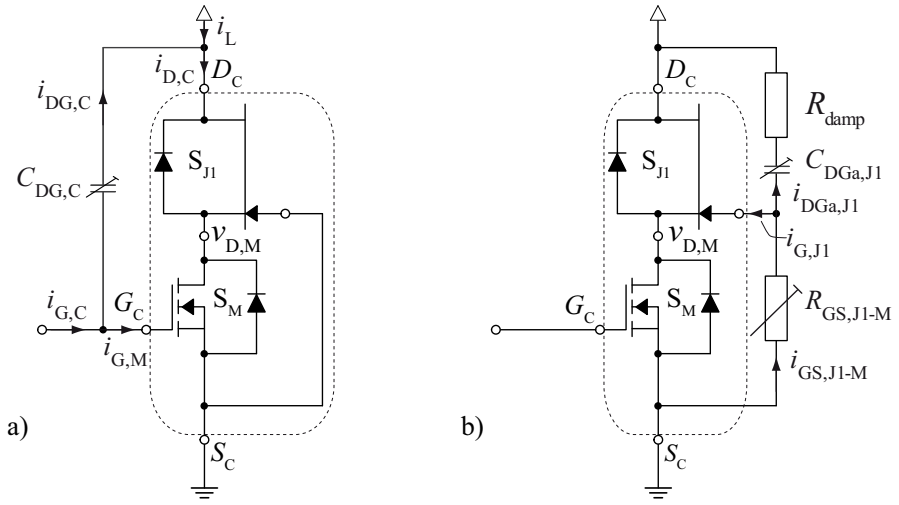

Figure 2.9: The novel dv/dt control concepts for the SiC MOSFET/JFET cascode; (a) Additional drain-gate capacitance resulting in an increased negative feedback to the MOSFET gate. (b) The RC-circuit between drain-gate of the SiC JFET and the external JFET gate resistance.

For a single MOSFET device [79], the total equivalent input capacitance $C_{iss,M}$ seen from the gate-source junction during the on/off transition can be expressed with

$$\begin{aligned} i_{G,M^s} &= (C_{GS,M} + (1 + G_M) \cdot C_{DG,M}) \cdot \frac{d(v_{GS,M})}{dt} \\ &= C_{iss,M} \cdot \frac{dv_{GS,M}}{dt}. \end{aligned} \tag{2.13}$$

The term $(1 + G_M)$ is called *Miller Effect* and describes a capacitive feedback between the output and the input of the single MOSFET device. The gain G_M of the low-voltage MOSFET is given as

$$G_M = -\frac{d(v_{DS,M})}{d(v_{GS,M})}. \tag{2.14}$$

Regarding the novel $\mathrm{d}v/\mathrm{d}t$ concept with the additional drain-gate capacitor (cf. Figure 2.9 (a)), the cascode gate current $i_{G,C}$ is calculated to

$$\begin{aligned} i_{G,C} &= i_{G,M} + i_{DG,C} \\ &= i_{G,M} + C_{DG,C}\Big(- \frac{d(v_{GS,M} - v_{DS,C})}{dt}\Big). \end{aligned} \tag{2.15}$$

It has to be noticed, that the MOSFET gate current $i_{G,M}$ in the cascode topology is different from the gate current i_{G,M^s} for a single MOSFET device. The detailed operating principle to control the $\mathrm{d}v/\mathrm{d}t$ of the drain-source voltage $v_{DS,C}$ is explained with experimental switching waveforms in four time intervals T_1 to T_4. The experimentally determined turn-on and turn-off behavior of the Si-SiC cascode is presented in Figure 2.10. The dashed lines show the simulated voltage and current waveforms, which match very well the experimental results (solid lines).

Interval T_1: During T_1 a positive voltage is applied to the MOSFET gate-source terminals and the corresponding capacitance $C_{GS,M}$ is charged. This result in a marginal increase of the MOSFET drain source-voltage. As long as $v_{GS,M} < V_{th,M} \approx 4\,\mathrm{V(max)}$, $i_{D,C}$ remains zero. Once $v_{GS,M}$ reaches $V_{th,M}$, the MOSFET starts to conduct. While the drain current $i_{D,C}$ is increasing, the drain-source voltage starts to decrease slightly and then stops abruptly. The cascode switch, mainly represented

by the high voltage blocking device of the SiC JFET, is still turned off and the behavior is comparable to a single MOSFET device.

Interval T_2: At the beginning of T_2 the gate-source voltage reaches the Miller plateau, where the drain current is equal to the load current and the freewheeling diode stops conduction. The MOSFET drain-source voltage $v_{DS,M}$ remains at a voltage level which herein is called cascode Miller level $V_{M,C}$. This cascode Miller level is kept almost constant until the SiC JFET drain-source voltage $v_{DS,J1}$ is decreased to the on-state voltage. The cascode Miller level of $V_{M,C} \approx 16\,\mathrm{V}$ is depending on the cascode drain current $i_{D,C}$. Assuming, that $v_{GS,M}$ and $v_{DS,M}$ keep the constant voltage level (cf. Figure 2.10 (a) and (b)), the resulting voltage rate of change results in

$$\frac{d(v_{GS,M})}{dt} = \frac{d(v_{DG,M})}{dt} = 0. \tag{2.16}$$

Therefore, during time period T_2 the MOSFET gate current $i_{G,M}$ is zero and the cascode drain current can be approximatively calculated to

$$\begin{aligned} i_{D,C} &= i_{G,C} + i_L \\ &= i_{DG,C} + i_L. \end{aligned} \tag{2.17}$$

The drain-gate capacitive current $i_{DG,C}$ is defined by the applied voltage across the gate resistor $R_{G,C}$ to

$$i_{DG,C} = \frac{v_G - v_{GS,M}}{R_{G,C}} = C_{DG,C} \cdot \frac{d(v_{DS,J1})}{dt}. \tag{2.18}$$

It must be noted here, that the parasitic gate inductance is neglected in Eq. (2.18), due to the optimized layout of the experimental setup.

The SiC JFET drain-source voltage $v_{DS,J1}$ decreases linearly and the fall time t_f can be calculated with the gate current $i_{G,C}$ which is limited by the gate resistor to

$$t_f = \frac{C_{DG,C} \cdot \Delta v_{DS,J1} \cdot R_{G,C}}{V_G - v_{GS,M}} = 114\,\mathrm{ns}. \tag{2.19}$$

With a gate drive voltage of $V_G = 12\,\mathrm{V}$, a fall time of 114 ns is resulting. Approximately, this value is also resulting experimentally as demon-

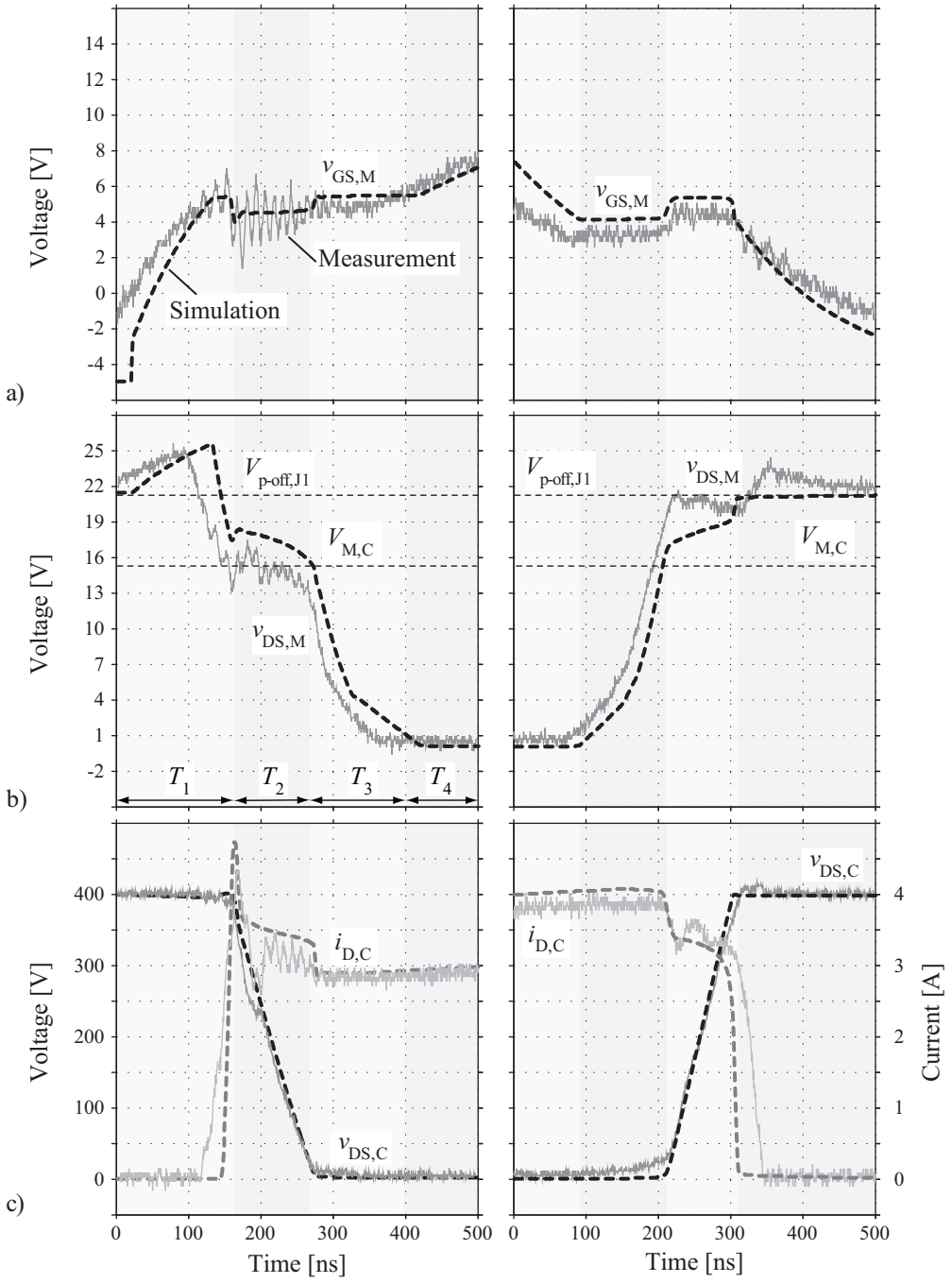

Figure 2.10: Measurement (solid) and simulation (dashed) results of the Si-SiC cascode illustrating the influence of the additional capacitor $C_{DGa,C}$ @400 V/3 A(turn-on) and 4 A(turn-off). MOSFET gate-source voltage $v_{GS,M}$ (a), MOSFET drain-source voltage $v_{DS,M}$ (b), cascode drain-source voltage $v_{DS,C}$ and cascode drain current $i_{D,C}$ are shown (c). Measurement and simulation parameters: MOSFET type *IRF2804*, $C_{DG,C} = 100\,\text{pF}$, $R_{G,C} = 20\,\Omega$.

strated in Figure 2.10 (c). The cascode Miller level $V_{M,C}$ is depending on the load current i_L and the capacitive drain-gate current $i_{DG,C}$. Thus, $V_{M,C}$ is decreasing with a larger drain current $i_{D,C}$ and increasing with a lower drain current. Responsible for the drain current depending cascode Miller level is the JFET characteristics, which has to open the channel to conduct the drain current and consequently the gate-source voltage of the JFET ($v_{DS,M} = v_{GS,J1}$) is forced to decrease. At the end of interval T_2, the fast drop of $i_{D,C}$ (cf. Figure 2.10 (c)) indicates the completed discharge of capacitor $C_{DG,C}$ ($i_{DG,C} = 0$).

Interval T_3: During interval T_3, the voltage across the SiC JFET is equal to the voltage drop caused by the on-resistances of the JFET and MOSFET channels. The gate-source voltage keeps still at the Miller plateau as now the MOSFET drain-source voltage decreases to zero.

Interval T_4: The cascode switch is now completely in conduction mode and therefore the gate-source voltage is increasing to the nominal gate drive voltage v_G. Furthermore the inductive load current increases in dependence of the load voltage and the inductance value.

The main interval to limit the dv/dt is time interval T_2. There, only the gate drive limited current $i_{DG,C}$ is flowing through the capacitor $C_{DG,C}$ and therefore the length of T_2 is controllable. It is important to note, that conventional dv/dt techniques are applicable in combination with the additional drain-gate capacitor.

At turn-off, the dv/dt control behavior is almost equal and analog as described in detail for the turn-on transient. First, $v_{GS,M}$ decreases and therefore $v_{DS,M}$ is driven into blocking state. The cascode drain current is still flowing through the MOSFET and JFET channels until the MOSFET drain-source voltage is between the cascode Miller level $V_{M,C}$ and the SiC JFET pinch-off voltage $V_{p-off,J1}$. In fact, the SiC JFET gate-source voltage $v_{GS,J1}$ touches shortly the pinch-off voltage level and immediately afterwards, the cascode drain current drops and the voltage $v_{DS,J1}$ increases. The JFET channel is not pinched-off completely and the load current is still flowing in both channels. The rate of change of $v_{DS,J1}$ is mainly controlled by the drain-gate current $i_{DG,C}$ through the additional capacitor $C_{DG,C}$. Assuming, that $i_{G,M}$ is zero and the voltages applied to the MOSFET ($v_{GS,M}$ and $v_{DS,M}$) are nearly constant, the

voltage variation over time can be calculated to

$$\begin{aligned}\frac{d(v_{DS,J1})}{dt} &= -i_{DG,C} \cdot \frac{1}{C_{DG,C}} \\ &= \frac{v_G - v_{GS,M}}{R_{G,C}} \cdot \frac{1}{C_{DG,C}}.\end{aligned} \tag{2.20}$$

Due to the nearly constant current $i_{DG,C}$, the slope of the voltage change is linear and thus well controllable with the novel configuration. Finally, the total dc-link voltage occurs across the SiC JFET and the cascode drain current decreases fast to zero. Both devices, low-voltage MOSFET and high voltage SiC JFET, are now in blocking mode.

RC-Circuit and JFET Gate Resistor $R_{GS,J1-M}$ (Concept B)

An alternative concept to control the dv/dt behavior of the Si-SiC cascode employs an *RC*-circuit and an additional resistor $R_{GS,J1-M}$. The idea of this configuration is to affect the drain-gate capacitance of the high voltage device, which mainly determines the dv/dt characteristic of the Si-SiC cascode. The detailed evaluation of the dynamic behavior is described based on the experimental measurement presented in Figure 2.11. The turn-on and turn-off transitions are subdivided into five time intervals T_1 to T_5.

Interval T_1: Interval T_1 is analogous to the first control method with the additional drain-gate capacitor $C_{DG,C}$. The gate-source voltage is applied and the MOSFET gate-source capacitor is charged until the Miller level is reached. It should be noted, that the level of the MOSFET drain-source voltage is above the pinch-off voltage of the JFET $V_{p-off,J1}$. The discussion of this characteristic Si-SiC cascode over voltage effect is shifted to the analysis of the discussion of the turn-off behavior.

Interval T_2: The gate-source voltage of the MOSFET is equal to the Miller level, while the drain-source voltage of the MOSFET and the gate-source voltage of the SiC JFET are decreasing rapidly simultaneously, hence

$$-\frac{d(v_{DS,M})}{dt} = -\frac{d(-v_{GS,J1})}{dt}. \tag{2.21}$$

The drain-source voltage of the JFET remains at the same voltage

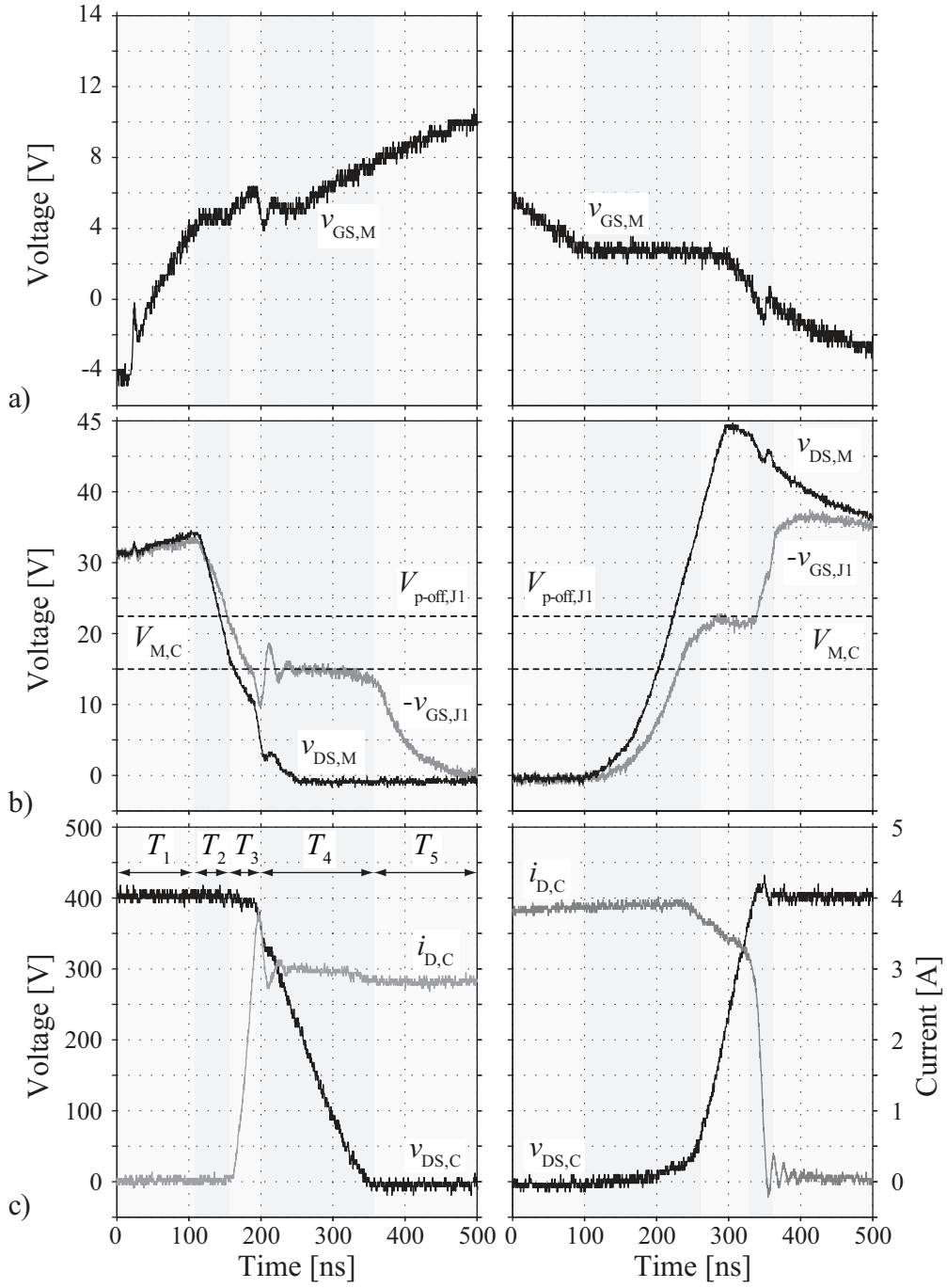

Figure 2.11: Measurement results of the Si-SiC cascode illustrating the influence of the *RC*-circuit and the JFET gate resistor $R_{GS,J1-M}$ @400 V/3 A(turn-on) and 4 A(turn-off). MOSFET gate-source voltage $v_{GS,M}$ (a), MOSFET drain-source voltage $v_{DS,M}$ and JFET gate-source voltage (b), cascode drain-source voltage $v_{DS,C}$ and the cascode drain current $i_{D,C}$ are illustrated (c). Measurement parameters: MOSFET type *IRF2804*, $R_{damp} = 100\,\Omega$, $C_{DGa,J1} = 100\,\text{pF}$, $R_{GS,J1-M} = 47\,\Omega$ and $R_{G,C} = 20\,\Omega$.

level as shown in the measurement (cf. Figure 2.11 (c)).

Interval T_3: At the beginning of T_3, $v_{GS,J1}$ reaches the JFET pinch-off voltage and is continuous decreasing. Therefore, the SiC JFET channel is not any more completely pinched-off and the cascode current rises very fast with a capacitive current peak. Once, the cascode drain current $i_{D,C}$ reaches the load current the freewheeling diode stops to conduct and the load current is commutated to the Si-SiC cascode. The MOSFET drain-source voltage is also decreasing while the gate-source voltage is still equal to the Miller plateau voltage.

Interval T_4: The low-voltage MOSFET is completely turned on and $v_{GS,M}$ increases to the nominal gate voltage V_G. The JFET gate-source voltage $v_{GS,J1}$ reaches the cascode Miller voltage $V_{M,C}$ and keeps the voltage level over the whole time interval, thus resulting in

$$\frac{d(v_{GS,J1})}{dt} = 0. \tag{2.22}$$

The constant voltage $v_{GS,J1}$ is also applied across the JFET gate resistor $R_{GS,J1-M}$ and therefore the current which is responsible for discharging the JFET drain-gate capacitors ($C_{DG,J1}$ and $C_{DGa,J1}$) can be calculated to

$$i_{GS,J1-M} = \frac{v_{GS,J1}}{R_{GS,J1-M}}. \tag{2.23}$$

The current $i_{GS,J1-M}$ is separated into two parts depending on the impedance of the capacitor $C_{DG,J1}$ and the series connection of the capacitor $C_{DGa,J1}$ and resistor R_{damp}. The analytical expression valid during this time period is

$$\begin{aligned} i_{GS,J1-M} &= i_{G,J1} + i_{DGa,J1} \\ &= C_{DG,J1}(v_{DS,J1}) \cdot \frac{d(v_{DS,J1})}{dt} + C_{DGa,J1} \cdot \frac{d(v_{DGa,J1})}{dt}. \end{aligned} \tag{2.24}$$

Due to the nonlinear characteristic of the SiC JFET internal drain-gate capacitance $C_{DG,J1}(v_{DG,J1})$, which is strongly depending on the corresponding drain-gate voltage $v_{DG,J1}$, the $\mathrm{d}v/\mathrm{d}t$ is mainly controlled by the additional drain-gate capacitor $C_{DGa,J1}$. From the measurements,

the drain-gate capacitance at 400 V is

$$C_{DG,J1}(400\,\mathrm{V}) \approx 25\,\mathrm{pF} < C_{DGa,J1}, \tag{2.25}$$

and therefore smaller than the additional capacitor [80]. With a total drain-gate capacitance of 125 pF the calculated fall time is approximately 150 ns.

While the current $i_{GS,J1-M}$ discharges the drain-gate capacitors of the SiC JFET, the voltage $v_{DS,J1}$ decreases linearly. The cascode drain current is the sum of the load current and the discharge currents

$$i_{D,C} = i_{G,J1} + i_{DGa,J1} + i_L. \tag{2.26}$$

In Figure 2.11 (c) a small increase in cascode current is visible as expressed in Eq. (2.26) over the whole time interval.

Interval T_5: In the last time interval of the turn-on transition, $v_{GS,J1}$ decreases to the on-voltage of the conduction mode. The final discharging process is truly an RC-circuit formed by the JFET gate-source capacitor $C_{GS,J1}$ and the JFET gate resistor $R_{GS,J1-M}$.

The dv/dt limitation takes place in the fourth time interval where the discharge of the capacitor is occurring. The resistance R_{damp} is required to damp occurring MOSFET gate drive oscillations. The dv/dt limitation is mainly controlled by two parameters, i.e. the values of $C_{DGa,J1}$ and $R_{GS,J1-M}$.

The turn-off transition is analog to the turn-on transition and therefore only the special and challenging factors are discussed. The MOSFET drain-source voltage $v_{DS,M}$ is increasing until the SiC JFET pinch-off voltage is reached. At this point the JFET drain-source voltage $v_{DS,J1}$ starts to increase, while the MOSFET drain-source voltage is further increasing until the whole voltage is blocked by the cascode and no further change of $v_{DS,J1}$ occurs. The SiC JFET gate-source voltage is constant, close to the pinch-off voltage level. The JFET channel, however, is still not completely pinched-off and therefore a drain current is flowing. After the actual turn-off transition at t$\approx$ 340 ns the JFET gate-source voltage rises very fast caused by the capacitor $C_{GS,J1}$ charging current

$$-i_{GS,J1-M} = \frac{v_{DS,M} - v_{GS,J1}}{R_{GS,J1-M}} = C_{GS,J1}\Big(-\frac{d(-v_{GS,J1})}{dt}\Big). \tag{2.27}$$

The JFET gate-source diode is driven into avalanche operation until the dynamic balancing process is finished. Also the low-voltage MOSFET is driven close to its avalanche mode and under certain conditions the maximal MOSFET blocking voltage could possibly be reached. In case of repetitive operation at high frequency, the gate-source diode will then not be able to recover properly and will operate continuously in avalanche mode. This effect can be observed by the turn-on transition in Figure 2.11 (b) where the JFET gate-source voltage is above the pinch-off voltage.

In order to provide simulation results demonstrating the before discussed dv/dt behavior, the accurate avalanche behavior of the SiC JFET gate-source diode has to be implemented. In the SPICE model used in this thesis ideal behavior is implemented and no avalanche mode can be observed. Therefore, no simulation results regarding this dv/dt control technique are presented. It should be mentioned, that the SPICE model from SiCED has implemented this feature of the SiC JFET.

Both concepts are properly working and allow to adjust the dv/dt switching transient of the Si-SiC cascode. The first concept advantageously ensures operation in the nominal and specified ranges of the devices. For the second concept there are more parameters to control

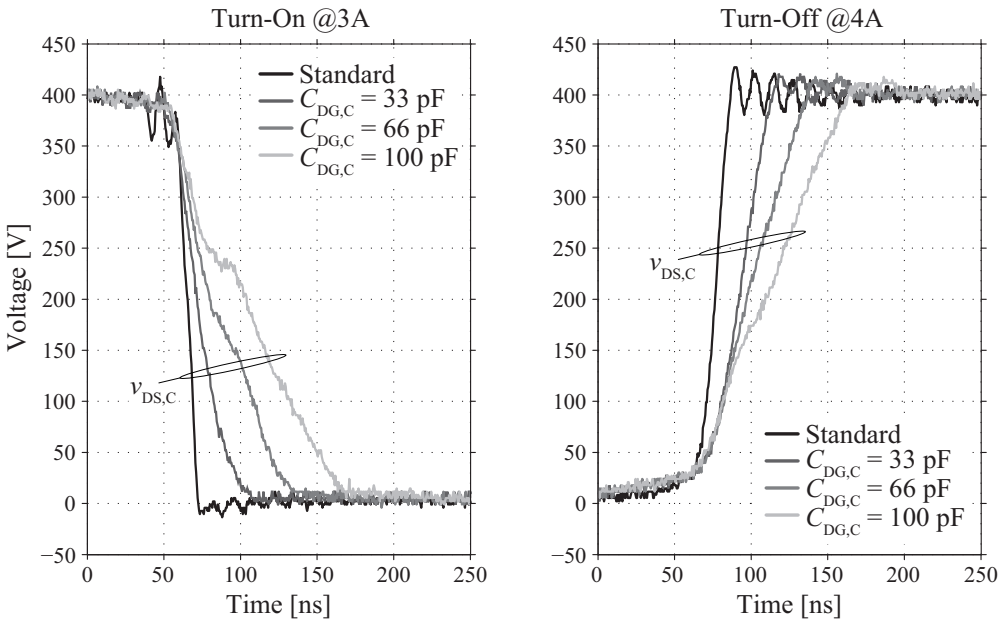

Figure 2.12: Measurement results of the dv/dt control concept A at V_{dc}=400 V and different values of the drain-gate capacitance $C_{DG,C}$.

the dv/dt, but an avalanche of the JFET gate-source diode could occur. Furthermore, both concepts have additional losses due to the additional capacitors and the decreased dv/dt of the cascode voltage edges. The resulting energy losses are discussed in Section 2.6. Depending on the application of the cascode, a combination of both concepts in addition to conventional techniques lead to an optimized switching behavior. In the following a set of experimental results clearly demonstrate the controllability of the Si-SiC cascode dv/dt while applying the new concepts.

2.5.3 Measurement Results

In the following measurement results are presented to verify, with different values of the parameters ($C_{DG,M}, C_{DGa,J1}$ and $R_{GS,J1-M}$), both concepts which are discussed in Section 2.5.2 . The measurement labeled as standard means the cascode topology with a low-voltage MOSFET and the SiC JFET without additional components. The gate resistance $R_{G,C}$ for this configuration is selected to 4.7 Ω. For all the other measurements verifying the both concepts, a gate resistance of $R_{G,C}$=20 Ω is

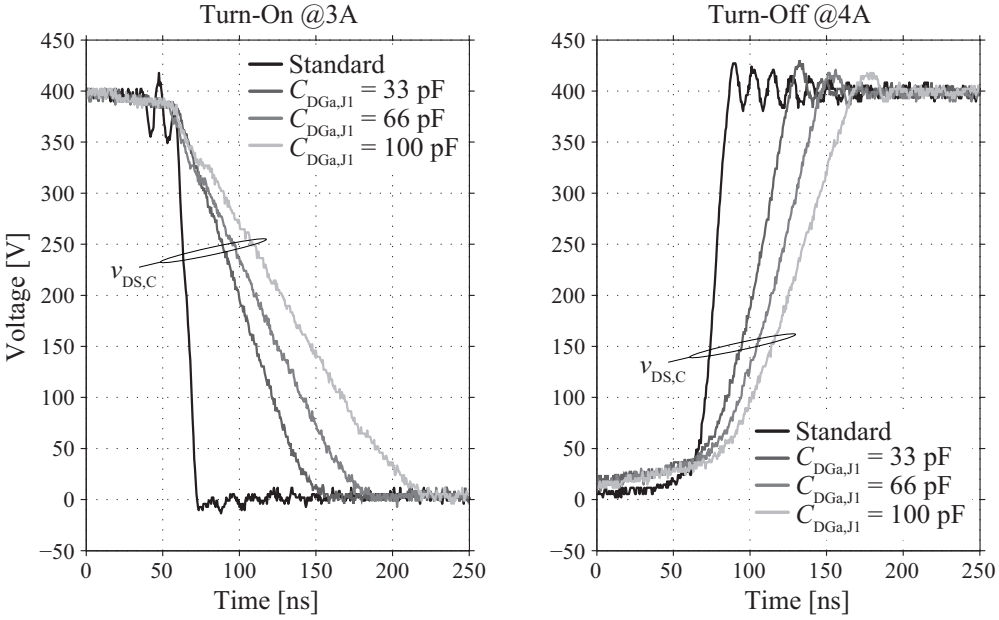

Figure 2.13: Measurement results of the dv/dt control concept B at V_{dc}=400 V and different values of the capacitance $C_{DGa,J1}$, damping resistor R_{damp}=100 Ω and JFET gate resistor $R_{GS,J1-M}$=47 Ω.

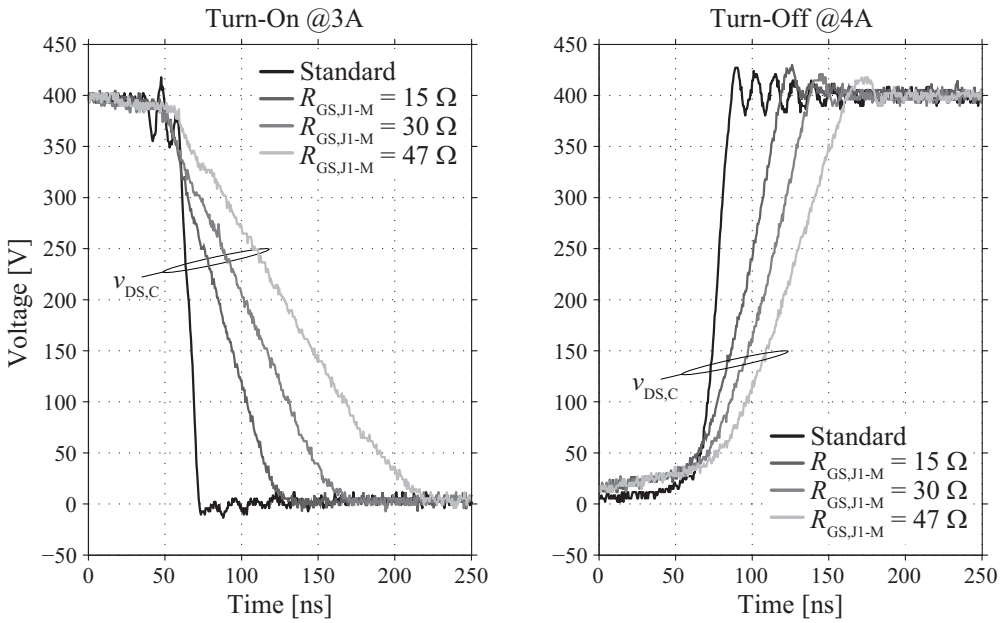

Figure 2.14: Measurement results of the dv/dt control concept B at V_{dc}=400 V and different values of the JFET gate resistor $R_{GS,J1-M}$, drain-gate capacitance $C_{DGa,J1}$=100 pF and damping resistor R_{damp}=100 Ω.

applied.

In Figure 2.12 the measurement results of concept A with the additional drain-gate capacitor are presented. The tests are performed with three values of $C_{DG,C} = \{33\,\text{pF}, 66\,\text{pF}, 100\,\text{pF}\}$. The larger the additional drain-gate capacitor, the lower the resulting dv/dt value. The fall time approximately calculated with Eq. (2.19) scales directly with the drain-gate capacitance assuming same gate resistor and gate drive voltage.

The experimental voltage waveforms of concept B with the RC-element and the JFET gate resistor $R_{GS,J1-M}$ are demonstrated in Figure 2.13 and Figure 2.14. On the one hand, the dv/dt is controlled by different values of drain-gate capacitor $C_{DGa,J1} = \{33\,\text{pF}, 66\,\text{pF}, 100\,\text{pF}\}$ in Figure 2.13, on the other hand the voltage rate of change is regulated by different values of the SiC JFET gate resistors $R_{GS,J1-M} = \{15\,\Omega, 30\,\Omega, 47\,\Omega\}$. In addition, all the measurements show, that the ringing at turn-off is apparent damp with controlled and lower dv/dt values.

2.6 Si-SiC Cascode Power Losses

Based on the experimental on/off switching transitions performed with the test setup shown in Figure 2.3, the switching energy losses of the Si-SiC cascode are evaluated. The turn-on/off energy losses are calculated from the measured switching voltage $v_{DS,C}$ and switching current $i_{D,C}$ waveforms.

In Figure 2.15 (a) the energy losses of concept A and concept B are depicted in dependency of the voltage rate of change (dv/dt). With lower and controlled dv/dt values, the energy losses are increasing. Due to the longer fall and rise time of the Si-SiC cascode the integration of voltage and current over time results in larger values, i.e. in increased energy losses. Moreover, the required passive elements for controlling the dv/dt behavior generate additional energy losses. The energy stored in

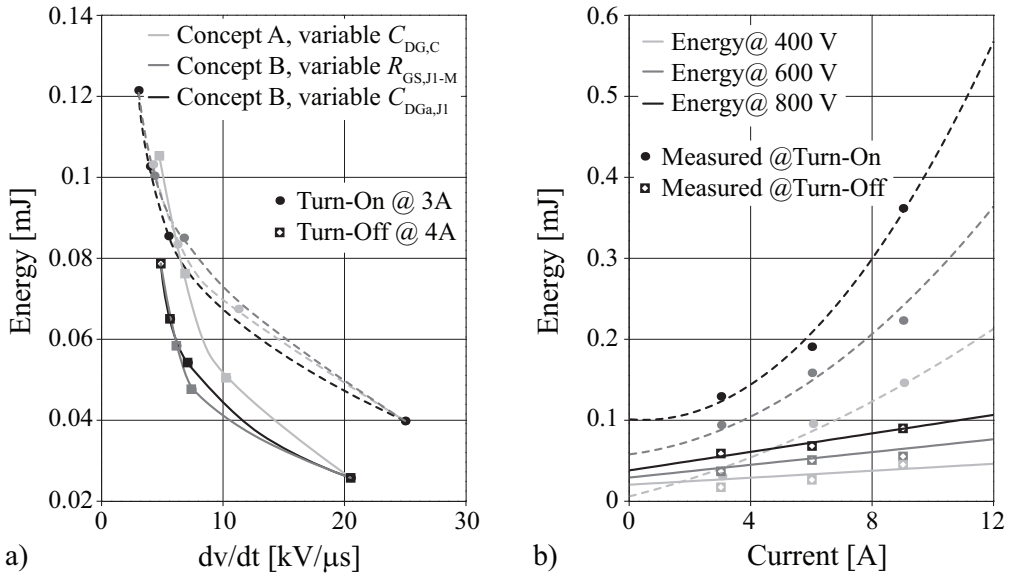

Figure 2.15: Switching energy losses measured in a buck configuration comprising a SiC Diode (*C2D10120*) and the Si-SiC cascode (SiC JFET (V_{p-off}=22.3 V, $R_{DS(on),J1}$=0.33 Ω), MOSFET (*IRF2804*)): (a) Turn-on/off energy losses of the dv/dt control concepts A and B at 400 V. (b) Evaluated energy losses of the standard Si-SiC cascode at dc-link voltage levels of $V_{dc-link}$ = {400 V, 600 V, 800 V}. Note: The measurements are performed at room temperature.

the capacitor is calculated with

$$E_C = \frac{1}{2} \cdot C \cdot V_C^2. \tag{2.28}$$

In case of concept A, the additional drain-gate capacitor $C_{DG,C}$ of 100 pF stores an energy at 400 V of 8 μJ. The capacitor energy is completely dissipated per switching cycle.

The measured energy losses at turn-on/off for concept A with $C_{DG,C}$= 100 pF result as $\approx$ 120 μJ (on) and $\approx$ 105 μJ (off). Comparing these values with the measured energy losses of the standard Si-SiC cascode (measurement with highest dv/dt values: lower right corner) of $\approx$ 40 μJ (on) and $\approx$ 28 μJ (off) makes clear that the larger energy losses by lower dv/dt values are mainly caused by the lower rate of change of the voltage. The influence of the additional energy losses due to the capacitor is comparably small. Concept A and B show almost same turn-on energy losses. However, at the turn-off switching transitions concept A shows higher energy losses than concept B especially at lower dv/dt values or larger values of $C_{DG,C}$. This additional amount of energy losses can be partially explained by the cascode drain-source voltage demonstrated in Figure 2.12. At turn-off the drain-source voltage $v_{DS,C}$ increases fast up to 150 V. At this point the measured waveform shows almost an s-shaped characteristic most probably caused by transient turn-off (for a very short time) of the SiC JFET (cf. Figure 2.10 (b) right hand side at t=250 ns). Therefore, a short delay of the increase in voltage occurs while almost the whole drain current is flowing through the device.

In case of concept B it should be considered, that the stored energy in capacitor $C_{DGa,J1}$ is not completely dissipated in the Si-SiC cascode due to the series resistors R_{damp} and $R_{GS,J1-M}$. Furthermore, the energy losses caused by the avalanche mode of the JFET gate-source diode (cf. Figure 2.11 (b)) are not considered in the analysis and in Figure 2.15 (a).

In Figure 2.15 (b) the energy losses of the standard Si-SiC cascode are presented for different voltage and current levels measured at room temperature. The turn-on energy losses increase as a second order polynomial function, whereas the turn-off energy losses increase linearly with current. At the SiC JFET nominal current of 5 A hard switching turn-on losses don't exceed the value of 200 μJ. Therefore, the Si-SiC cascode is an attractive alternative to state-of-the-art semiconductor technology.

Chapter 3

Si MOSFET/SiC JFET SuperCascode

The requirements on future semiconductor switches are challenging in terms of high power level combined with high switching frequencies. Using wide band gap semiconductors as e.g. SiC allows to realize the high switching frequencies as introduced in Section 1.3.2. The high power rating can be achieved either by a high current or a high voltage rating or a combination of both. Due to the limited current rating of present wide band gap semiconductor, e.g. SiC JFET (I_D=5 A, I_D=20 A), the fast switching, high power devices have to operate with high voltage. Therefore several discrete devices are connected in series to build a high voltage switch. Such a device for switching at a high operating voltage was invented in 2000 [81]. There, a low voltage switching element and a first high voltage switching element are connected in a cascode configuration (cf. Chapter 2). In order to extend the operating voltage range further, high voltage elements are connected in series with the first high voltage switching element. Further inventions were filed based on the idea of stacked semiconductor devices to achieve high voltage operation in 2002 [82] and 2004 [83].

In this chapter, detailed investigations of the stacked switch, i.e. a theoretical analysis and verification with experimental measurements, are presented. Based on this investigations, a novel stacked switch configura-

tion is developed and the transient switching as well as the static behavior are analyzed in depth.

3.1 Stacked High Voltage Switch

Currently, fast single switches with several kilovolts operating capability based on wide band gap materials are under investigations, e.g. a 10 kV SiC MOSFET [30] or a 6.5 kV SiC JFET [31], but not yet commercially available. Therefore, the series connection of several lower voltage switches, e.g. 1.2 kV devices, is an attractive alternative for building a switch with a blocking capability of several kilovolts. Such stacked high voltage switch, in future could be also used for a series connection of high voltage switches to achieve an even higher operating voltage. The more high voltage devices with a blocking voltage $V_{(BR),DSS,single}$ are stacked, the higher the possible operating voltage of the resulting switch,

$$V_{(BR),DSS,stacked} = n \cdot V_{(BR),DSS,single}, \tag{3.1}$$

whereas n is the number of single switches. The power rating of the stacked high voltage switch increases linearly with n as the same current flows through each element of the series connection. The voltage across the whole switch is higher than the allowable operating voltage of each single switch. Consequently, proper distribution of the total blocking voltage to the individual switches has to be ensured. Two control methods could be applied for voltage symmetrization. On the one hand, there is the well known and often used technique to actively control each element of the series connection and on the other hand, there is a technique where just the first element in the series connection is actively controlled and all other elements are controlled by a passive circuits.

3.1.1 Gate Driver for Each Power Device

Control methods, for active gate control of all the series connected devices as introduced in Section 1.3 are well known and summarized in [19]. Experimental experiences with series connected IGBTs [84] have shown unsymmetrical voltage sharing due to differences of the parasitic device parameters like collector-emitter capacitances, leakage currents and switching delays. To overcome the voltage unbalance, different methods

for voltage balancing are developed. A list of possible concepts is given in the following:

- Load side voltage balancing:
  - Impedance symmetrization
  - Clamp circuits
  - Snubber circuits; active, lossless or passive
- Gate side voltage balancing
  - $\mathrm{d}v/\mathrm{d}t$- and $\mathrm{d}i/\mathrm{d}t$ control
  - Active overvoltage protection by dynamic clamp circuits
  - High precision gate drive timing
  - Cascaded synchronization
  - Time delay compensation
- Active Gate controlled voltage balancing.

As mentioned above, numerous concepts have been developed in the past, for active voltage balancing of stacked switches. The effort to realize such a switch is significantly, considering the auxiliary supply and control of the gate drivers (galvanically isolated) and the balancing control. Furthermore, this kind of voltage sharing control is limited by the turn-on and turn-off times of the stacked switching. In the time range of μs a delay of the gate drive signal is negligible. However, for higher switching frequencies and/or faster turn-on and turn-off transients in the range of 10 ns. A delay could be critical for a proper switching behavior. Therefore, building a high voltage stacked switch with only one active controlled element is favorable. All other switches are then controlled passively and/or the voltage balancing is by additional circuits. Such a switch topology is introduced and and investigated in the following.

3.1.2 Single Gate Driver Topologies

The series connection of power devices with a single gate driver signal, which is applied to the power devices nearest to the common ground (first power device), reduces the control effort to a minimum. All other high voltage devices connected in series are controlled by passive auxiliary elements. Depending on the semiconductor type, i.e. whether depletion mode device (normally-on) or enhancement mode device is em-

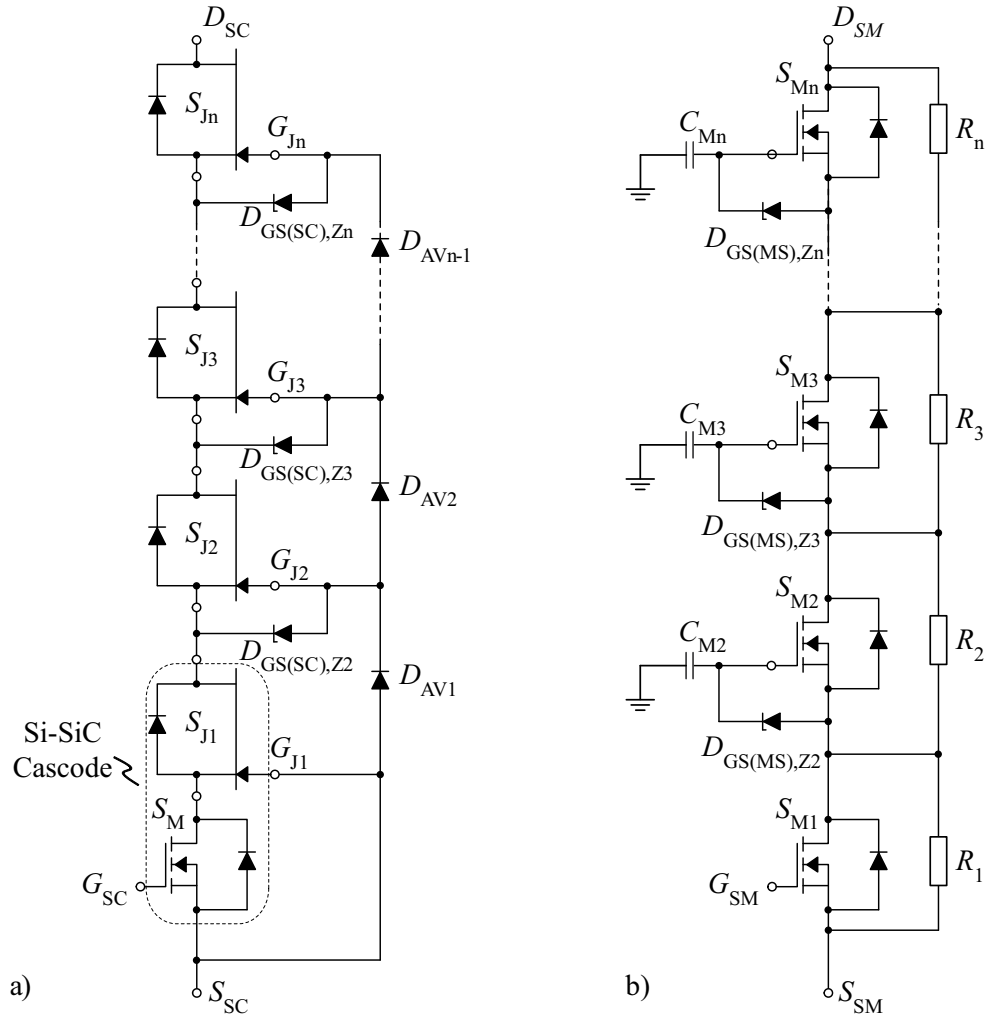

Figure 3.1: Topologies of series connected high voltage switches; (a)'Standard' stacked high voltage switch topology according to [81] for normally-on high voltage devices and (b) series connection of normally-off devices as proposed in [85].

ployed (normally-off) different stacked topologies have to be applied. In Figure 3.1 two stacked high voltage switch topologies are presented. The series connection for high voltage normally-on devices, e.g. SiC JFETs, is shown on the left side (a). Based on the Si-SiC cascode topology, the whole switch acts as a three-terminal device (G_{SC},S_{SC},D_{SC}) with a normally-off characteristic. Based on the application and investigation of 1.2 kV SiC JFETs in this thesis, the topology builds the basis of the research work on static and dynamic switching characteristics described in the following where the topology is called 'Standard' Si-SiC SuperCascode (***SSiSiCSC***). The topology presented in Figure 3.1 (b) represents only one topology of several topologies proposed [85] for connecting several normally-off switching devices in series. These topologies are not discussed in this thesis and therefore not further considered.

3.1.3 Basic Operation Principle

The basic concept of the 'Standard' SiC SuperCascode shown in Figure 3.1 (a) is described in [26] and [27]. There, also the static blocking characteristics and the dynamic switching behavior are discussed based on experiments and simulations ($DESSIS - ISE^{TM}$).

In the on-state the MOSFET of the SSiSiCSC is turned-on by a positive gate voltage. With a turned-on MOSFET also the first JFET switch S_{J1} is conducting, since its gate is connected to its source via the MOSFET. Assuming ideal semiconductor devices and therefore a zero voltage drop across the MOSFET, the gate-source voltage of the first SiC JFET is $v_{GS,J1} = 0\,\mathrm{V}$ and the JFET is in the on-state (normally-on device). Also the second SiC JFET S_{J2} is conducting since the gate-source voltage of S_{J2} is shorted via the turned-on S_{J1}, the low-voltage MOSFET and the avalanche/balancing diode D_{AV1}. Similar considerations can be performed for the upper JFETs.

For turning the cascaded switch off, first the MOSFET is turned-off via its gate and the drain-source voltage of the MOSFET rises until the pinch-off voltage $V_{p-off,J1}$ of S_{J1} is reached. Then, S_{J1} turns-off and blocks the rising drain-source voltage of the *SSiSiCSC* until the avalanche voltage of diode D_{AV1} is reached. Due to the avalanche of diode D_{AV1}, the gate potential of S_{J2} is fixed with respect to the source of the *SSiSiCSC* and does not rise any more. However, the source potential of S_{J2} continues to rise with the increasing drain-source voltage of S_{J1}, so

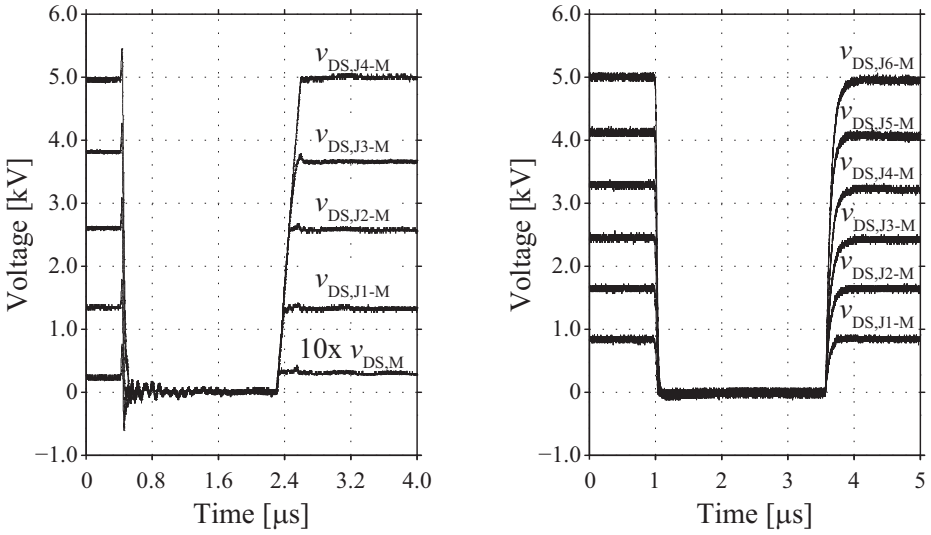

Figure 3.2: Symmetrical voltage sharing during static off behavior; Experimental measurements with (a) inductive load (MOSFET: *IRL3705*/55 V/TO-220 & 4 SiC JFETs: 1.5 kV/TO-220/SiCED and (b) resistive load (MOSFET: *IRLR024N*/55 V/D^2-Pak & 6 SiC JFETs: 1.2 kV/TO-220/SiCED).

that the gate-source voltage of S_{J2} becomes negative and S_{J2} turns-off as soon as its pinch-off voltage is reached. This sequential/simultaneous turn-off behavior, which could be seen in Figure 3.2, continues with the upper JFETs until the blocking voltage is reached.

Static Off Behavior

After the sequential/simultaneous turn-off, the static voltage distribution in the off-state (cf. Figure 3.2) is mainly determined by the avalanche voltage of the diodes $D_{AV1} \cdots D_{AV(n-1)}$. For a controlled and stable avalanche, i.e. for a controlled static voltage distribution, a certain leakage current through the balancing diodes is required. In order to guarantee this leakage current independently of the JFET parameters, resistors ($R_{GS2} \ldots R_{GSn}$) instead of Zener diodes ($D_{GS,Z2} \ldots D_{GS,Zn}$) [82], must be connected between the gate and the source of the upper JFETs as shown in Figure 3.3. With the resistors, the leakage current in steady state is defined by the resistance value and the JFETs pinch-off voltages,

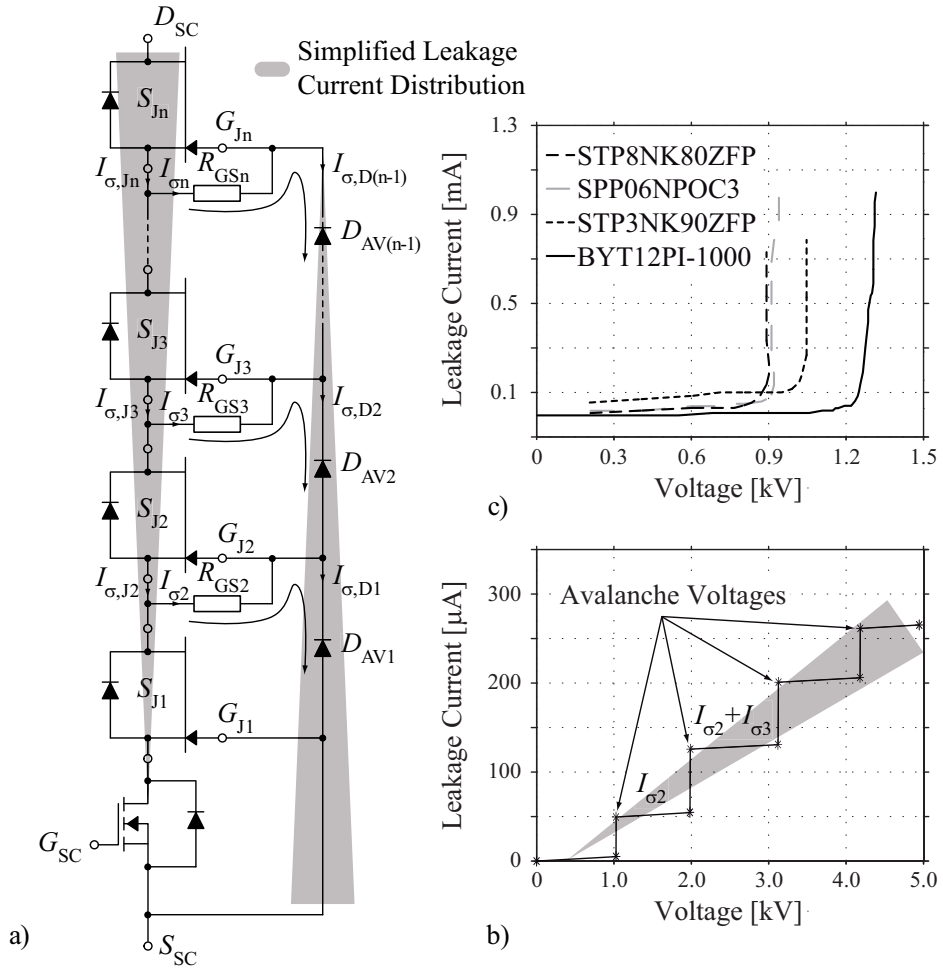

Figure 3.3: (a) Leakage current distribution in the Si-SiC SuperCascode with additional balancing resistors $R_{GS2} \ldots R_{GSn}$ for static off behavior. (b) Total leakage current of Si-SiC SuperCascode is increasing with increasing blocking voltage. (c) Static avalanche behavior of different diode types.

which is equal to the voltage drop across the resistor in the off-state, thus

$$I_{\sigma i} = \frac{V_{p-off,Ji}}{R_{GSi}} \qquad i = 2 \ldots n \tag{3.2}$$

where n is the number of series connected SiC JFETs.

By inserting the resistor also a kind of control loop of the voltage distribution in the off-state is initiated (cf. Figure 3.3): In case for example the drain-source voltage of S_{J2} would increase and/or the leakage current through S_{J2} would decrease also the current through resistor R_{GS2},

which flows via the voltage balancing diodes to ground, would decrease if it is assumed that the leakage current through S_{J1} is constant. This would result in a reduced voltage drop across resistor R_{GS2}. Consequently, the gate-source voltage of S_{J2} would decrease, so that the leakage current through S_{J2} would increase what stabilizes the gate-source voltage as well as the drain-source voltage of S_{J2}. This control mechanism leads to a stable leakage current through the resistors and the diodes, so that the voltage sharing between the devices is stabilized by the avalanche voltage of the diodes, which determine the gate potentials of the JFETs. The leakage current for a lower JFETs flows via the upper JFETs, so that the current in the JFETs decreases from the upper to the lower and of the *SSiSiCSC* and the current in the voltage balancing diodes increases from the upper to the lower one as symbolized by the triangular arrows in Figure 3.3 and expressed with the following inequalities

$$I_{\sigma,J2} < I_{\sigma,J3} < \cdots < I_{\sigma,Jn} \qquad \text{(JFET currents)}, \tag{3.3}$$

$$I_{\sigma,D1} > I_{\sigma,D2} > \cdots > I_{\sigma,D(n-1)} \qquad \text{(diode currents)}. \tag{3.4}$$

Dynamic Behavior

During the switching process the inner potentials of the stacked switches are changing dynamically and are mainly defined by the junction capacitances of the balancing diodes. The behavior of these capacitances during rising or falling voltage are affecting directly the gate of each upper JFET. In Figure 3.4 for example, the drain-source voltages of two series connected JFETs during switching are shown. There, the junction capacitance of the voltage balancing diode (avalanche diode) has been varied. The larger this capacitance is, the more the turn-on transients of the two JFETs are synchronized, since the capacitance tries to keep the voltage across the balancing diode constant during the turn-on. This leads to a rapidly increasing gate-source voltage of JFET S_{J2} as soon as the drain voltage of the first JFET S_{J1} starts to fall. The resistor R_{D1} in series to C_{T1} is added for damping oscillations during the switching transient.

Based on Figure 3.4 it seems that a larger capacitance value for C_{T1} results in a more synchronous switching. However, at turn-off a too large value for C_{T1} results in an asynchronous switching operation and an unbalanced voltage distribution as could be seen in Figure 3.5. The reason

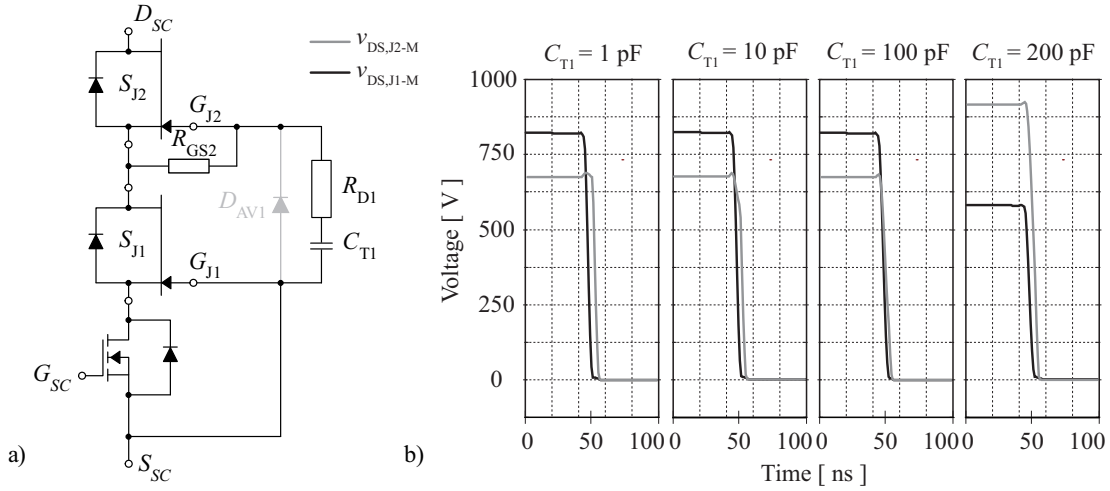

Figure 3.4: (a) Simulation setup of two series connected JFETs. (b) Drain-source voltages of the JFETs in a Si-SiC SuperCascode consisting of two JFETs for different values of the auxiliary capacitor C_{T1} ranging from 10 pF to 200 pF ($R_{D1} = 50\,\Omega$, $R_{GS2} = 240\,\mathrm{k}\Omega$, $V_{dc} = 1.5\,\mathrm{kV}$).

for this is, that at the beginning of the turn-off the capacitor is discharged, so that the gate potential of JFET S_{J2} is held down. When S_{J1} now starts to turn-off, the gate voltage of S_{J2} immediately becomes negative and turns-off S_{J2} faster than S_{J1}, so that S_{J2} is blocking the largest share of the voltage.

The parasitic junction capacitances of the balancing diodes D_{AV1} $\ldots D_{AV(n-1)}$ have similar influence on the switching transients as capacitors C_{T1} $\ldots C_{T(n-1)}$. However, the value of the capacitance changes with the voltage across the diode and it is the smallest, when a diode is in avalanche. Thus, the effect on turn-on is much smaller (where a large capacitance value is advantageous) than the effect on turn-off, where the capacitance value is maximal, but where a small capacitance would be advantageous. Therefore, it is difficult to achieve an optimal transient performance just with the parasitic junction capacitance of the diodes. For achieving an optimal behavior, i.e. fast and synchronous turn-on and off transients, a minimal junction capacitance of the balancing diode in combination with a parallel connected adjustable capacitor/resistor auxiliary circuit is required.

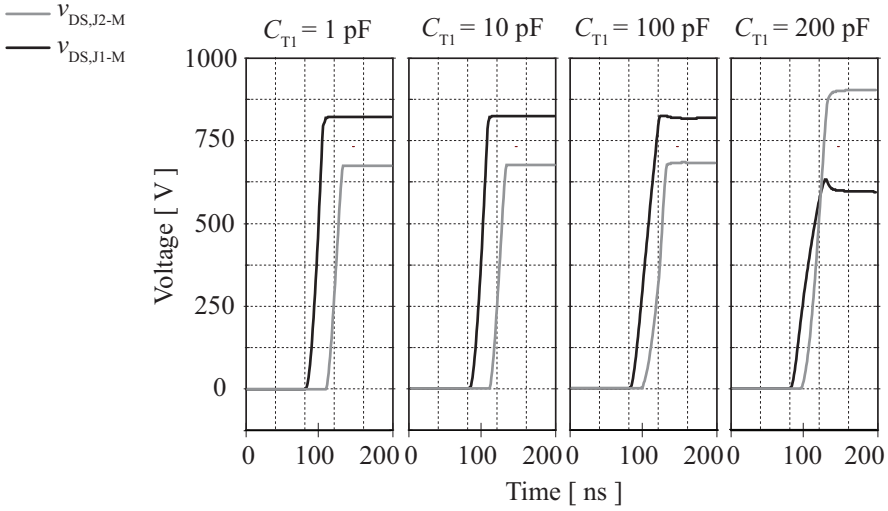

Figure 3.5: Drain-source voltages of the JFETs of a Si-SiC SuperCascode consisting of two JFETs for different values of the auxiliary capacitor C_{T1} ranging from 10 pF to 200 pF ($R_{D1} = 50\,\Omega$, $R_{GS2} = 240\,\mathrm{k}\Omega$, $V_{dc} = 1.5\,\mathrm{kV}$).

3.2 Modified Si-SiC SuperCascode

The *SSiSiCSC* topology is modified as a result of the investigation on the dynamic switching behavior. The resulting topology (cf. Figure 3.7 a)) is herein called 'Modified' Si-SiC SuperCascode (***MSiSiCSC***). Additional *RC*-elements are parallel connected to each balancing diode to achieve optimal transient behavior. Transient simulation results of the *MSiSiCSC* with 6 SiC JFETs connected in series are presented in Figure 3.6. The simulation waveforms on the top (a) show the turn-on and turn-off behavior and illustrate the effect of a critical capacitance value C_{crit} at the top most SiC JFET S_{J6}. A larger capacitance value larger than C_{crit} for C_{T5} would result in an overvoltage across S_{J6}. The operation under this condition (repetitive avalanche operation) is unacceptable in continuous operation mode and must be avoided.

In order to make the Si-SiC SuperCascode more robust against device tolerances and to avoid any overvoltages, diode D_{AVn} and/or capacitor C_{Tn} and resistor R_{Dn} can be added as shown in Figure 3.7. The upper capacitor C_{Tn} mainly leads to a more balanced voltage distribution for capacitors C_{T1} to $C_{T(n-1)}$ as the circuit acts as dynamic voltage divider. With diode D_{AVn} a similar stabilization could be achieved, but also the

maximal blocking voltage of the *MSiSiCSC* is limited to

$$V_{(BR),DSS,SC} = n \cdot V_{aval}. \tag{3.5}$$

Furthermore, the fast transient behavior achieved at Figure 3.6 (a) is slowed down as presented with the simulation results in (b). Therefore, the optimal solution for very fast transients requires small junction capac-

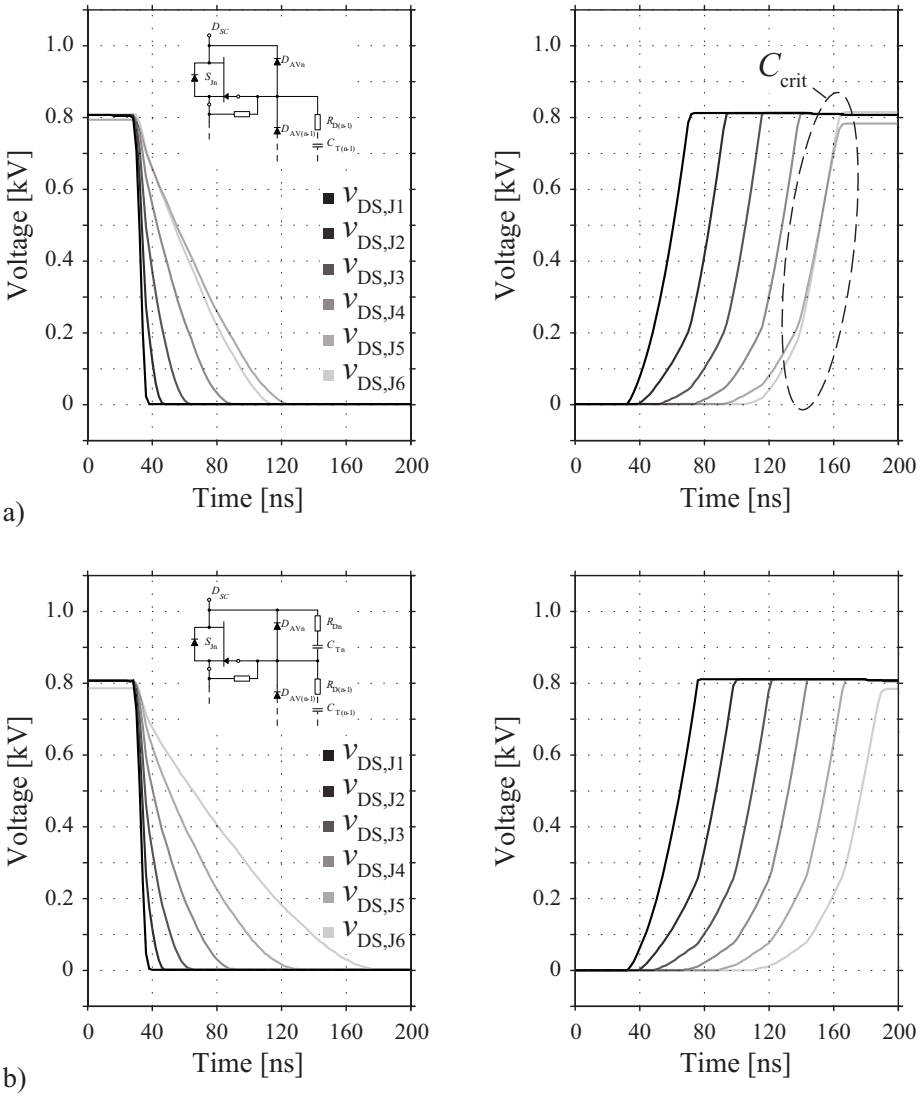

Figure 3.6: SPICE based simulation results of the *MSiSiCSC*; (a) Transient behavior at the critical limit of the junction capacitance (without the elements R_{Dn} and C_{Tn}, cf. Figure 3.7). (b) Trade off between slower transient behavior and robustness of the *MSiSiCSC* (with the auxiliary elements).

itances of the balancing diodes and additional well adjusted RC-elements. Connecting m balancing diodes in series, as illustrated in Figure 3.7 (b),

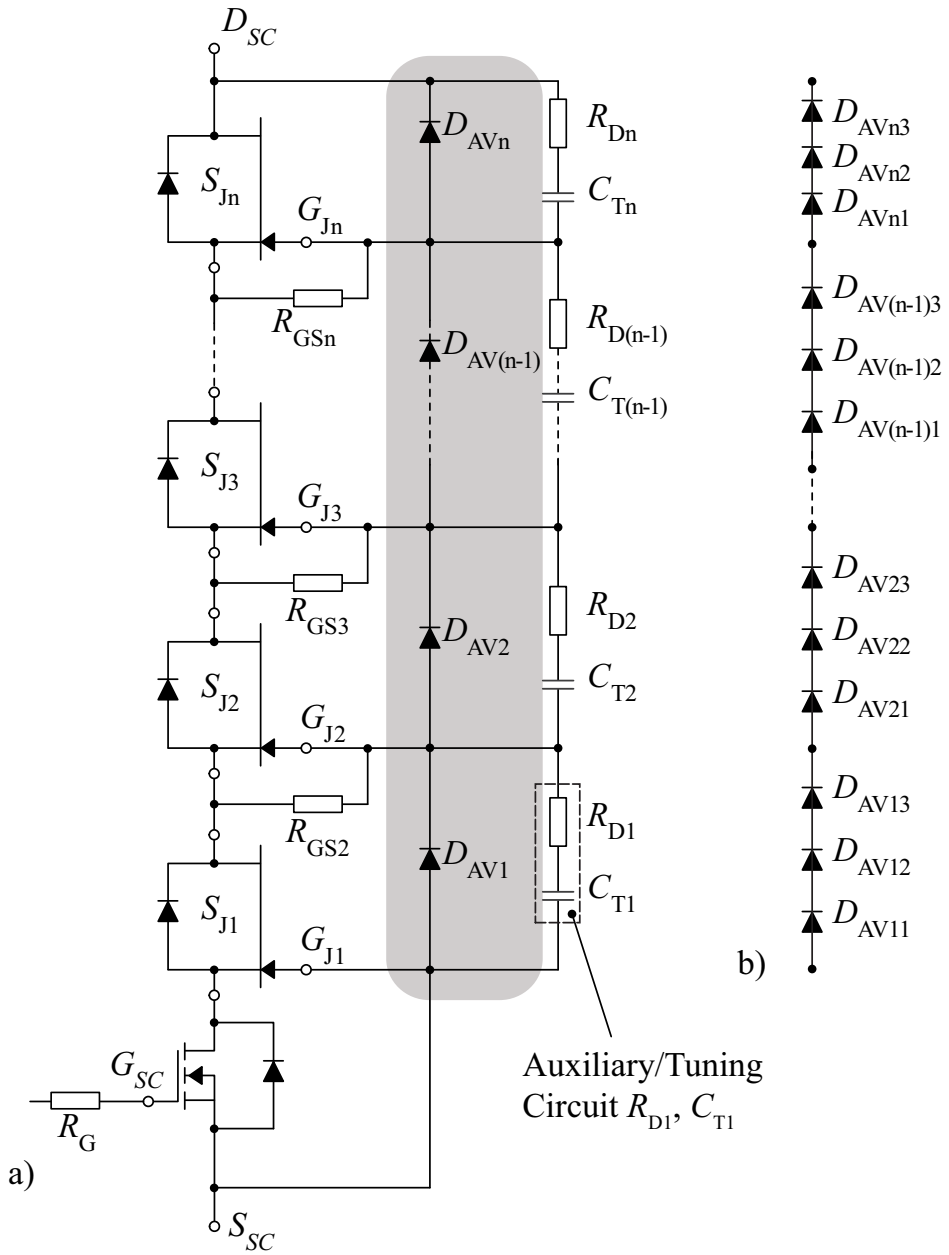

Figure 3.7: (a) Auxiliary resistors $R_{D1} \ldots R_{Dn}$ and capacitors $C_{T1} \ldots C_{Tn}$ for optimal dynamic voltage balancing across the SiC JFETs. (b) Reducing the effective junction capacitance per stage by increasing the number of series connected balancing diodes.

result in a smaller equivalent junction capacitance $C_{eq,D,AVi}$ between the gates of the SiC JFETs as given by

$$C_{D,AVi} > C_{eq,D,AVi} = \Big(\sum_{s=1}^{m} \frac{1}{C_{D,AVis}} \Big)^{-1}. \tag{3.6}$$

Therefore, the control could be influenced by the additional *RC*-elements in such a way, that the transient behavior becomes very fast and at the same time no overvoltage occurs at the top most switch considering any device tolerances. Preferably, this results in decreasing capacitance values from C_{T1} to C_{Tn}.

$$C_{T1} > C_{T2} > \cdots > C_{Tn} \tag{3.7}$$

3.3 Experimental Results *MSiSiCSC*

During the experimental investigation of the Si-SiC SuperCascode different test setups were developed. Figure 3.8 summarizes the realized experimental setups for the Si-SiC SuperCascode and shows in (a) the first setup and in (c) the final test setup before operating the Si-SiC SuperCascode in the dc-dc converter prototype (cf. Chapter 4 and Chapter 5). The experimental results presented and analyzed in the following have been measured with one of these test setups. The development process of the different test setups was running in parallel with the research work of the Si-SiC SuperCascode. Therefore, each new test setup has been developed and optimized in sense of avoiding previous disadvantages in component arrangement, wiring inductance loops and the accessibility for measuring and mounting components to a heating plate. Finally, a modular test setup up (cf. Figure 3.8 (c)) was resulting which combines all advantages of the previous built setups. The same Si-SiC SuperCascode modules as evaluated in the third test setup, are later applied in the dc-dc converter prototype (cf. Si-SiC SuperCascode module Figure 5.3). The discussion of the following experimental results is based on the schematic shown in Figure 3.7 and thus using the same nomenclature for the components. It has to be noticed that the capacitor C_{Tn}/resistor R_{Dn} auxiliary circuit is not assembled and therefore the measurements are performed without those elements.

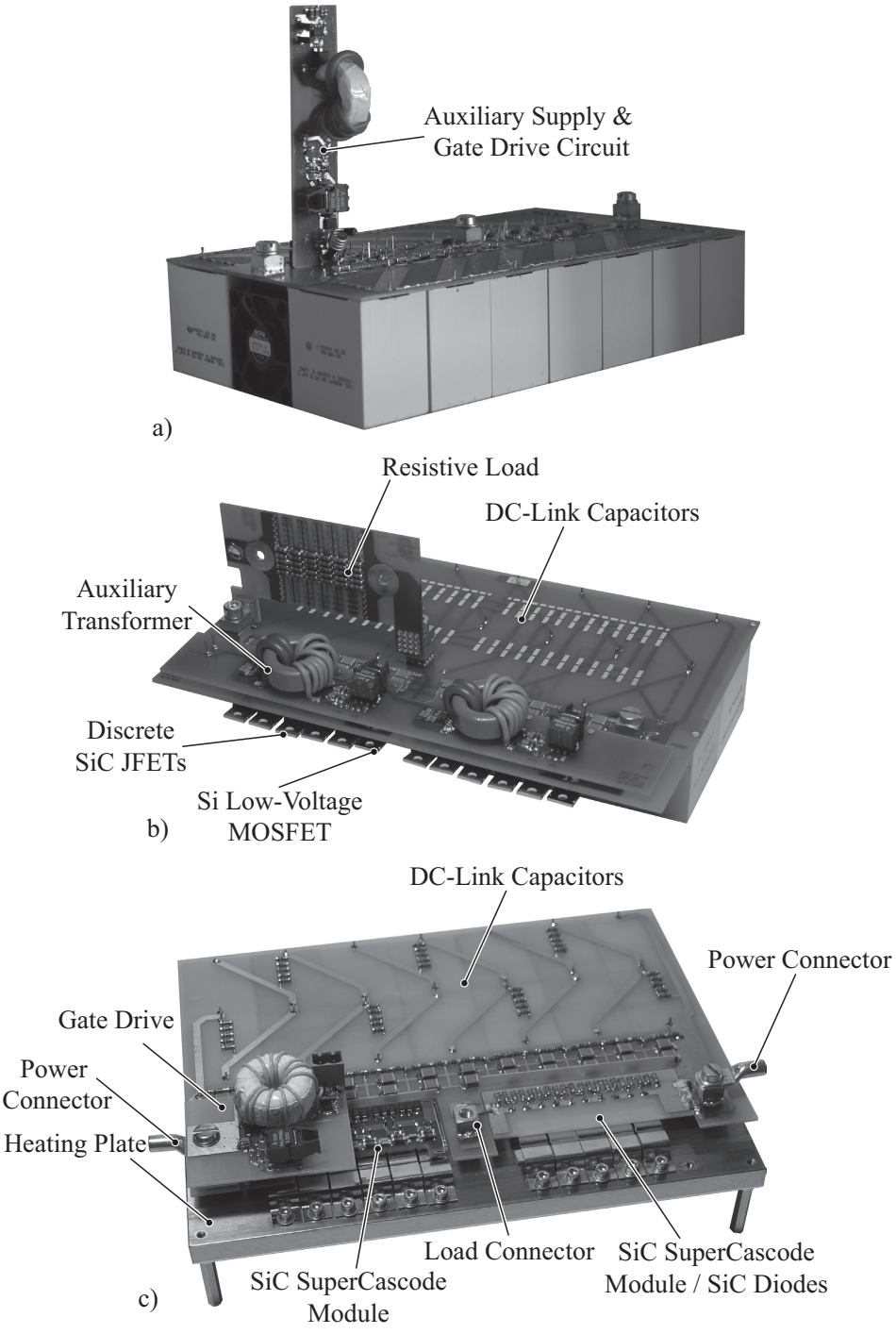

Figure 3.8: Si-SiC SuperCascode experimental setups with a dc-link voltage of 5 kV; (a) first test setup for discrete series connection of SiC JFETs, (b) test setup for optimized low inductive resistive load measurements and (c) final modular test setup for various experimental measurements including measurements at elevated temperatures.

3.3.1 Different Values of R_G and R_{GSn}

The *MSiSiCSC* contains of two different gate resistors; the conventional, preferably low ohmic gate resistor R_G at the gate G_{SC} of the low voltage switch and the gate-source resistor R_{GSn} at each upper SiC JFET. In

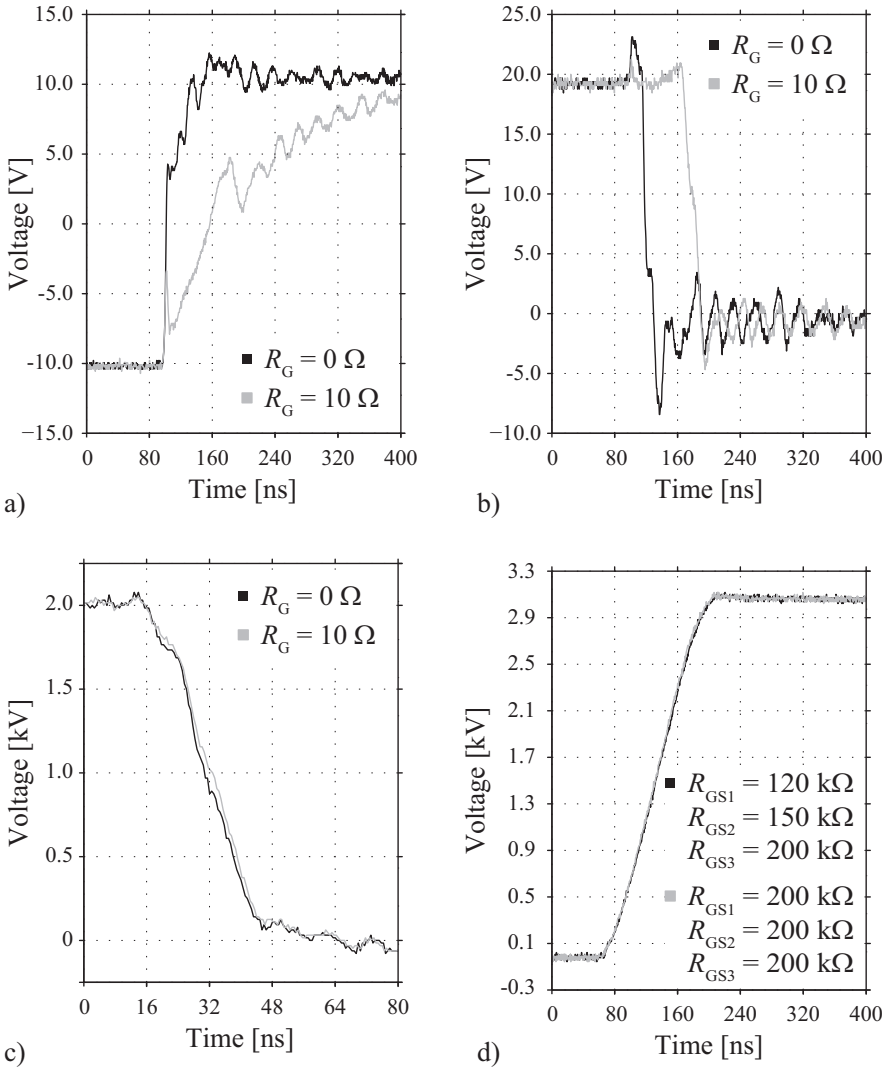

Figure 3.9: Transient behavior with different gate/gate-source resistors; (a) MOSFET gate-source voltage, (b) low-voltage MOSFET drain-source voltage and (c) Si-SiC SuperCascode drain-source voltage at $V_{dc} = 2\,\text{kV}$ measured with 3 SiC JFETs in series at turn-on transition; (d) turn-off behavior with 4 SiC JFETs in series, measured at $V_{dc} = 3\,\text{kV}$ with different values of the gate/gate-source resistors.

Section 2.5 the dv/dt controllability is analyzed of the Si-SiC cascode switch. There, the influence of different gate resistors is evaluated based on simulation results (cf. Figure 2.8). According to the findings and the analysis, the dv/dt behavior is not influenced by the gate resistor, however a time delay of the turn-on/off switching transition is generated. The same effect is measured with the Si-SiC SuperCascode as shown with the measurement results in Figure 3.9 (a)-(c). In Figure 3.9 (c) the time delay caused by the larger value of the gate resistor R_G is neglected in order to see the equal dv/dt transient behavior of the two measurements. The observed switching characteristic can be expressed with the following equation

$$\left.\frac{dv_{DS,SC}}{dt}\right|_{R_G=0\Omega} = \left.\frac{dv_{DS,SC}}{dt}\right|_{R_G=10\Omega} \tag{3.8}$$

which is valid for turn-on as well as for the turn-off behavior of the *MSiSiCSC*. Figure 3.9 (d) presents the turn-off behavior with different values of the gate-source resistors (R_{GS1},R_{GS2},R_{GS3}). Also these resistors have no influence on the dynamic dv/dt behavior.

3.3.2 Standard vs. Modified SuperCascode

The dynamic behavior is strongly influenced by the parasitic capacitances of the balancing diodes as analyzed with simulation results (cf. Figure 3.4 - Figure 3.6). To verify the simulation results and to identify how strong the influence of an additional capacitor (in parallel to the junction capacitance of the balancing diode) is, measurements have been performed with the standard (*SSiSiCSC* presented in Figure 3.3 where gate-source resistors are used instead of Zener diodes) and the modified SuperCascode topology (*MSiSiCSC* depicted in Figure 3.7). The resulting experimental waveforms are presented in Figure 3.10.

In Figure 3.10 (a) the MOSFET gate-source voltage $v_{GS,M}$ and the Si-SiC SuperCascode drain-source voltage $v_{DS,SC}$ during turn-on transition are presented. While the drain-source voltage is decreasing fast and/or the switch is turning-on, the gate-source voltage waveform shows strong oscillations. Therefore proper turn-on behavior is not guaranteed in continuous operating mode. The reason of the oscillations is that in the applied Si-SiC SuperCascode configuration only the capacitor C_{Tn} of the auxiliary circuit is assembled, but not the damping resistor R_{Dn}.

Consequently, the capacitor C_{Tn} and the SiC JFET gate-source capacitor $C_{GS,J1}$ are connected in series and produce strong oscillations at the gate G_{SC}, also because of the high $\mathrm{d}v/\mathrm{d}t$ value.

The same experimental measurement, with the assembled damping resistor R_{Dn}, is presented in Figure 3.10 (b). Obviously, the gate-source oscillations are eliminated without loosing the excellent switching perfor-

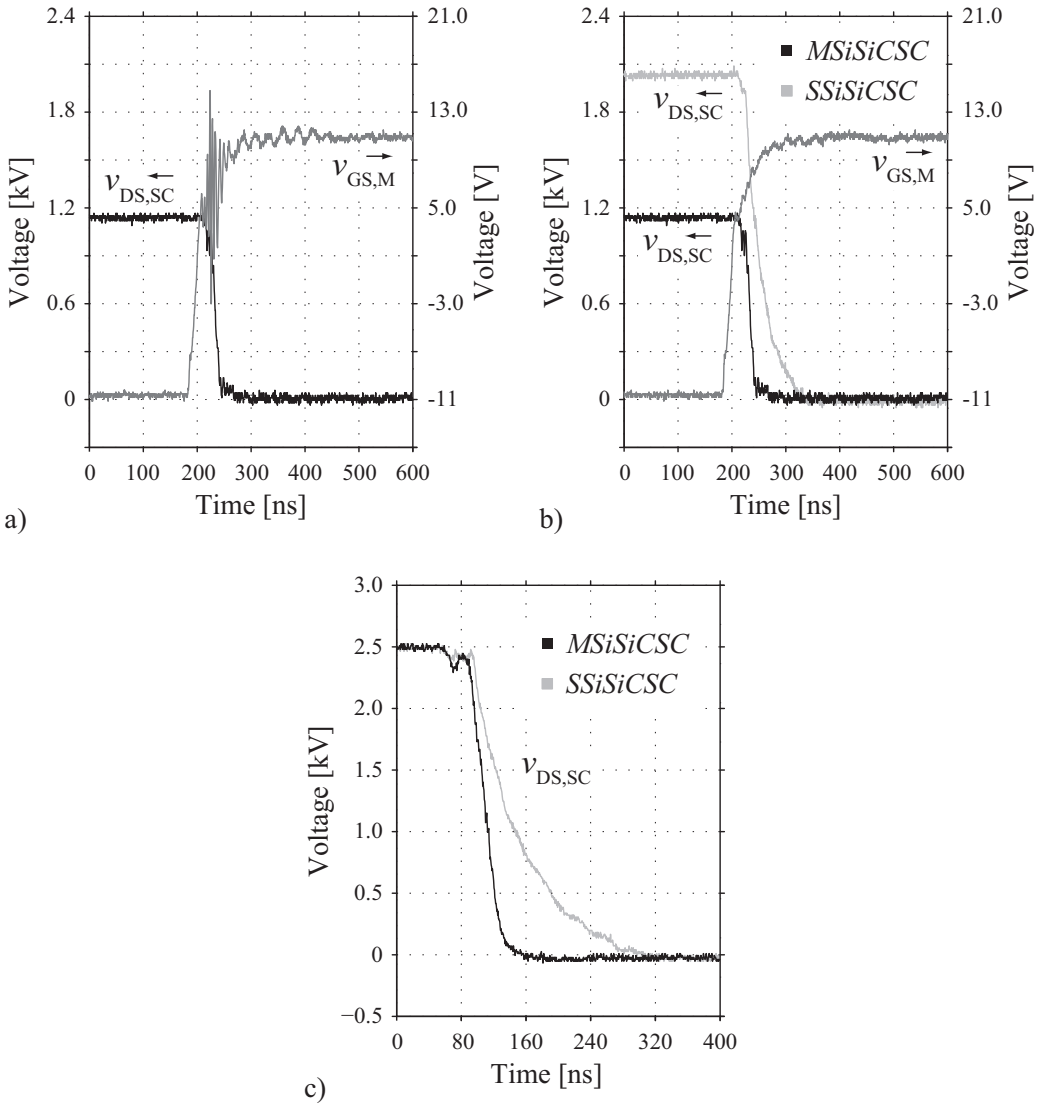

Figure 3.10: (a) Occurring oscillation in the MOSFET gate-source voltage due to the missing damping resistor R_{Dn}. (b) The gate-source voltage oscillation is completely eliminated with assembling the damping resistor R_{Dn}. (c) Transient turn-on switching performance of the *SSiSiCSC* compared to the *MSiSiCSC*.

mance of the *MSiSiCSC* at a dc-link voltage of almost 1.2 kV. In addition, the measured turn-on behavior of the *SSiSiCSC* at 2 kV is included in the same figure. Although, the two Si-SiC SuperCascode configurations are switched at different dc-link voltages, the same fast and proper switching behavior of the *MSiSiCSC* is visible.

Figure 3.10 (c) presents the turn-on behavior of the standard and modified Si-SiC SuperCascode at a dc-link voltage of 2.5 kV. The turn-on transient of the *MSiSiCSC* shows an improved switching behavior with a reduced turn-on time of 100 ns compared to the *SSiSiCSC*. Due to the better and controllable switching behavior of the modified Si-SiC SuperCascode, the following experimental results are only measured with the modified configuration (*MSiSiCSC*).

The experimental results of the *MSiSiCSC*, switching with resistive load, are shown in Figure 3.11. It has to be noted here, that these results are one of the first measurement results with resistive load (accordingly, not optimally tuned auxiliary circuit and first generation 1.5 kV SiC JFETs are used) which has been measured. The 90 % - 10 % fall time of the voltage is 190 ns and the rise time 200 ns. The large rise time results due to the relatively low load current i_L, which charges the out-

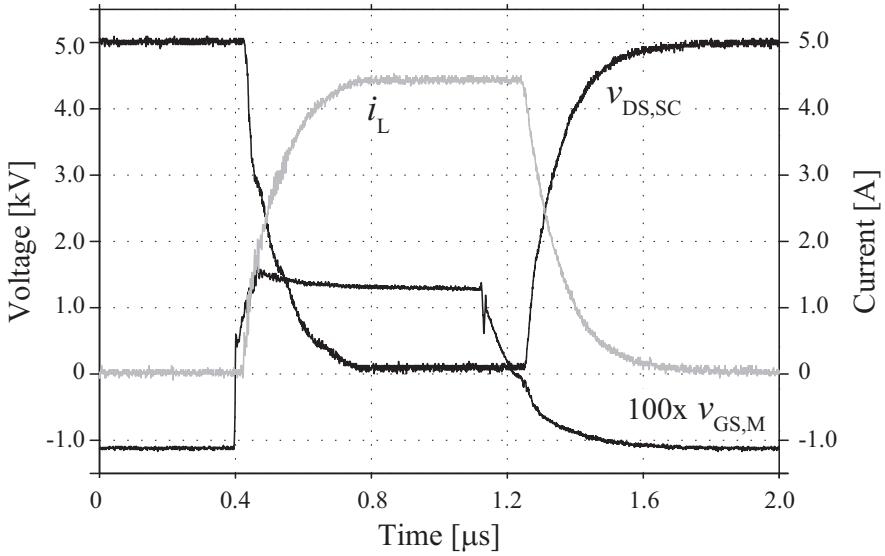

Figure 3.11: Measurement results for the *MSiSiCSC* with a gate-source voltage of 12 V and 1.1 kΩ purely resistive load. Test bench configuration: SiC JFETs: 1.5 kV/5 A(TO-220/SiCED), Si MOSFET: *IRL3705*, 55 V (TO-220), balancing diodes: *BYT12PI1000*, 1000 V (TO-220).

put capacitor of the Si-SiC SuperCascode and the parasitic capacitors of the load. The turn-off waveform is determined by the *RC*-time constant formed by the load resistor and the parasitic capacitors. Accordingly, the turn-off time of the SiC JFET is much shorter as could be seen in the linear voltage rise and its linear dependency from the load current presented in Figure 3.32. The turn-on transient is very fast at the beginning and then slows down due to *RC* charging process of the SiC JFET gates in the Si-SiC SuperCascode. As initially stated, these measurement results have been performed with not optimally tuning auxiliary circuits and therefore further improvements will be presented later in this thesis.

The turn-on behavior of the *MSiSiCSC* at 5 kV and low inductive load current i_L is shown in Figure 3.12. Illustrated are the drain-source voltage $v_{DS,J6-M}$, the MOSFET drain-source voltage $v_{DS,M}$ and gate-source voltage $v_{GS,M}$ measured at two different load current of 0 A in (a) and 3 A in (b). The corresponding Si-SiC SuperCascode configuration of the snubber/tuning circuit is given in the caption of Figure 3.12. During the fast ($\mathrm{d}v/\mathrm{d}t$ of 57.1 $^{\mathrm{kV}}/_{\mu\mathrm{s}}$ @$i_L = 0$ A and $\mathrm{d}v/\mathrm{d}t$ of 80 $^{\mathrm{kV}}/_{\mu\mathrm{s}}$ @$i_L = 3$ A) hard switching transitions of the *MSiSiCSC* it can be observed that with zero load current all the three measured voltages show oscillations, whereas the oscillations are reduced with a load current of 3 A. A conducted load

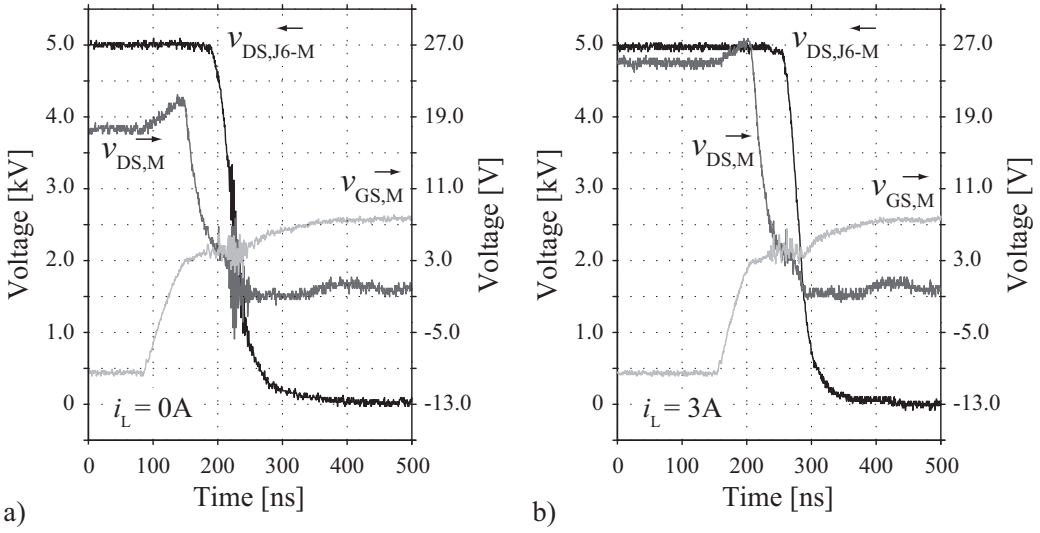

Figure 3.12: Turn-on characteristics at $V_{dc} = 5$ kV with (a) $I_L = 0$ A and (b) $I_L = 3$ A; Experimental configuration: 6 SiC JFETs in series, $R_{GS2} \ldots R_{GS6} = 200\,\mathrm{k\Omega}$, $C_{T1} \ldots C_{T5} = \{66, 58, 37, 25, 20\}$ pF, $R_{D1} \ldots R_{D5} = 50\,\Omega$ and $R_G = 30\,\Omega$.

current helps to charge/discharge the capacitance and reduces the voltage oscillations. Both measurements have been performed with a large gate resistor, i.e. R_G=30 Ω. The large value of the gate resistor is needed to damp the oscillations at zero current. As analyzed in Section 2.5 and in Figure 3.9 the dv/dt at turn-on/off is not influenced. Using a lower gate resistor causes stronger oscillations and a proper switching behavior is not guaranteed. Instead of applying a larger gate resistor also the Si low-voltage MOSFET channel can be used as damping element by controlling the applied gate-source voltage $v_{GS,M}$.

Finally, the behavior of $v_{DS,M}$ should be commented because of the depicted voltage level at $t = 0$. At Figure 3.12 (a) the MOSFET drain-source voltage is equal to SiC JFET pinch-off voltage $V_{p-off,J1}$ (steady state). In Figure 3.12 (b) the switching behavior is shown in the middle of several turn-on/off transitions (and/or in the middle of a double pulse) where e.g. the MOSFET drain-source voltage not yet reached the steady state condition. Therefore, the *MSiSiCSC* is still in a dynamic balancing process and the first SiC JFET gate-source voltage $v_{GS,J1}$ drives the

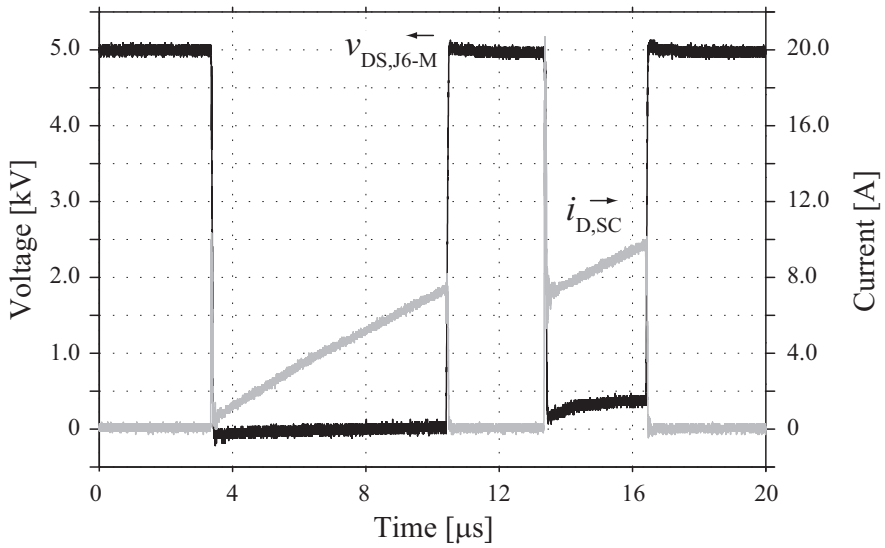

Figure 3.13: Double pulse switching behavior at high load current and V_{dc} = 5 kV; Experimental configuration: SiC JFETs: $S_{J1,lvs} \ldots S_{J6,lvs}$ = {1,2,3,4,5,6}, $S_{J1,hvs} \ldots S_{J6,hvs}$ = {7,8,9,10,11,12} (cf. Appendix A), MOSFET: $IRLR024N$, balancing diodes: $BZT03SERIES$, $R_{GS2} \ldots R_{GS6}$ = 240 kΩ, $C_{T1} \ldots C_{T5}$ = {76, 66, 55, 33, 15} pF, $R_{D1} \ldots R_{D5}$ = 50 Ω and R_G = 30 Ω.

diode into the avalanche mode. Before the dynamic balancing process is finished, the next switching action is already initiated at $t = 150\,\text{ns}$.

The *MSiSiCSC* switching behavior at higher load current is presented in Figure 3.13. The double pulse tests have been carried out with the configuration given in the caption. At the first pulse, of the double pulse test, the measured switching behavior shows excellent characteristics without ringing or oscillations. However, observing the second pulse, the *MSiSiCSC* is not turned-on properly as can be seen by the high on-voltage $v_{DS,J6-M} \approx 450\,\text{V}$. At the same time the drain current $i_{D,SC}$ is increasing linearly caused by the inductive load without any ringing. Therefore, the *MSiSiCSC* seems to increase its on-resistance and a larger voltage drop across each SiC JFET channel occurs. Various experimental results on single SiC JFET devices have shown, that a load current of 10 A does not affect the voltage drop so dramatically. Since the low-voltage MOSFET has shown a proper turn-on/off behavior, it is therefore assumed that the passively controlled SiC JFETs are not turning-on completely. Additionally, the turn-on behavior of the SiC JFETs is somehow depending on the load current. To identify the condition which leads to the high *MSiSiCSC* voltage drop in conduction mode, it is necessary to measure the gate-source voltage of each SiC JFET and preferably all of them simultaneously. In practice this measurement leads to a challenging task in terms of measurement equipment, parasitic capacitive effects of voltage probes influencing the transient behavior, and well defined calibration of various oscilloscopes. Therefore, the SPICE simulation model introduced in Section 2.3 is used and extended to the *MSiSiCSC* to analyze the current limitation issue.

3.4 *MSiSiCSC* Current Limitation

The *MSiSiCSC* topology shows excellent switching characteristics for low load current as presented with experimental results (cf. Figure 3.12). If the load current is increased, the switching behavior is still working properly but a high forward voltage drop of the *MSiSiCSC* occurs (cf. Figure 3.13) which results in very high conduction losses and therefore would not allow a continuous operation in a dc-dc converter. Thus, the high forward voltage drop is analyzed in detail and investigations have been made to eliminate the current limiting behavior.

3.4.1 'Quasi' Static On-Behavior

In Section 3.1.3 the behavior and the voltage distribution at the gates of the JFETs during the on-state have already been shortly discussed. There, it has been assumed that the voltage drops across the MOSFET and the JFET channels are zero in the 'quasi' [1] on-state. This, however,

[1] Achieving proper static on-behavior of the Si-SiC SuperCascode is depending on leakage currents, equalizing and discharging/charging currents, e.g. the gate-source

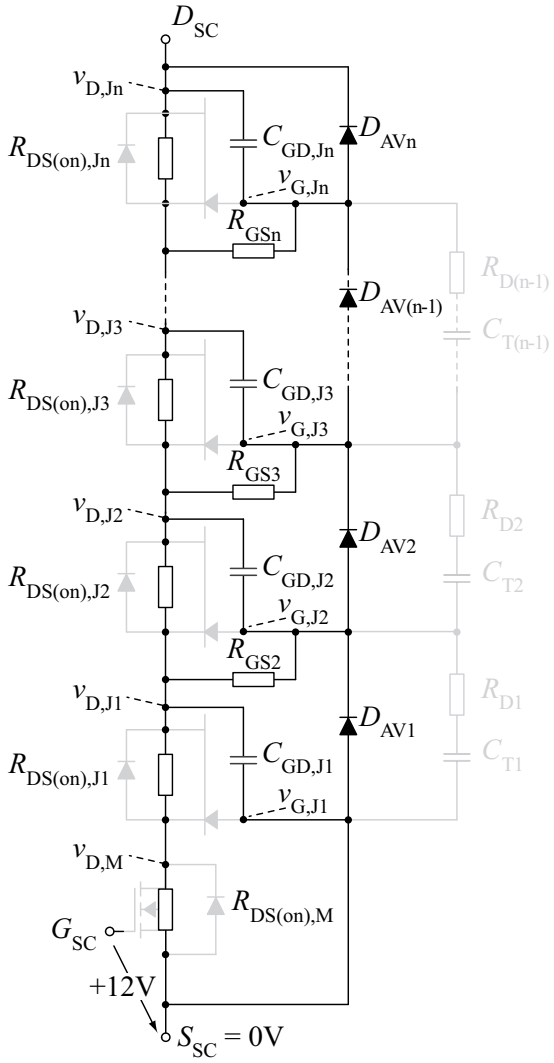

Figure 3.14: Voltage distribution in the Si-SiC SuperCascode during conduction mode influenced by the on-resistances of each semiconductor device and the load current.

is not true at higher current levels due to the relatively high on-resistance of the JFETs, which results in a forward voltage drop in the range of a few volts at nominal current. In Figure 3.14 the influence of the forward voltage drop on the voltage distribution at a nominal drain current $i_{D,SC}$ of 5 A and for assumed on-resistances at 25 °C (Si low-voltage MOSFET *IRLR024N*/SiC JFET) of

$$R_{DS(on),M} = 65\,\mathrm{m\Omega} \tag{3.9}$$

$$R_{DS(on),Ji} = 0.3\,\Omega \tag{3.10}$$

is visible. Due to the on-resistance of S_{J1} and the MOSFET, the drain potential of S_{J1} (source potential of S_{J2}) is

$$\begin{aligned} v_{D,J1} &= i_{D,SC} \cdot (R_{DS(on),M} + R_{DS(on),J1}) \\ &= 1.825\,\mathrm{V} \end{aligned} \tag{3.11}$$

with respect to the source of the *MSiSiCSC*. The gate of S_{J2} is not lower than the forward voltage drop of the balancing diode D_{AV1} given by

$$\begin{aligned} v_{G,J2} &= v_{F,DAV1m} \\ &= 1.0\,\mathrm{V} \quad (\mathrm{max} = 1.2\,\mathrm{V}). \end{aligned} \tag{3.12}$$

After turn-on the potential of the gate of S_{J2} is usually at its lower boundary since the discharging current for the drain-gate capacitor $C_{DG,J1}$ must flow via the balancing diode D_{AV1} or the auxiliary/tuning circuit respectively. Therefore, the gate-source voltage of S_{J2}, considering Eq. (3.11) and Eq. (3.12), is

$$v_{GS,J2} = -(v_{D,J1} + v_{G,J2}) \tag{3.13}$$

in worst case. These considerations can be also performed for the upper SiC JFETs, what finally results in a worst case gate-source voltage for

voltage $v_{GS,J1}$ at turn-off is driven into avalanche mode. With a high operating switching frequency, $v_{GS,J1}$ is not able to return to steady state and will turn-on between avalanche and pinch-off voltage. Therefore, the static on-behavior is called 'quasi' static on-behavior (means not pure steady state operation).

S_{Jn} of

$$v_{GS,Jn} = -(v_{D,Jn} + v_{G,Jn}) \tag{3.14}$$

$$= -\Big(i_{D,SC} \cdot \Big(R_{DS(on),M} + \sum_{i=1}^{n-1} R_{DS(on),Ji}\Big) + (n-1) \cdot m \cdot v_{F,DAV}\Big), \tag{3.15}$$

where m denotes the number of balancing diodes connected in series.

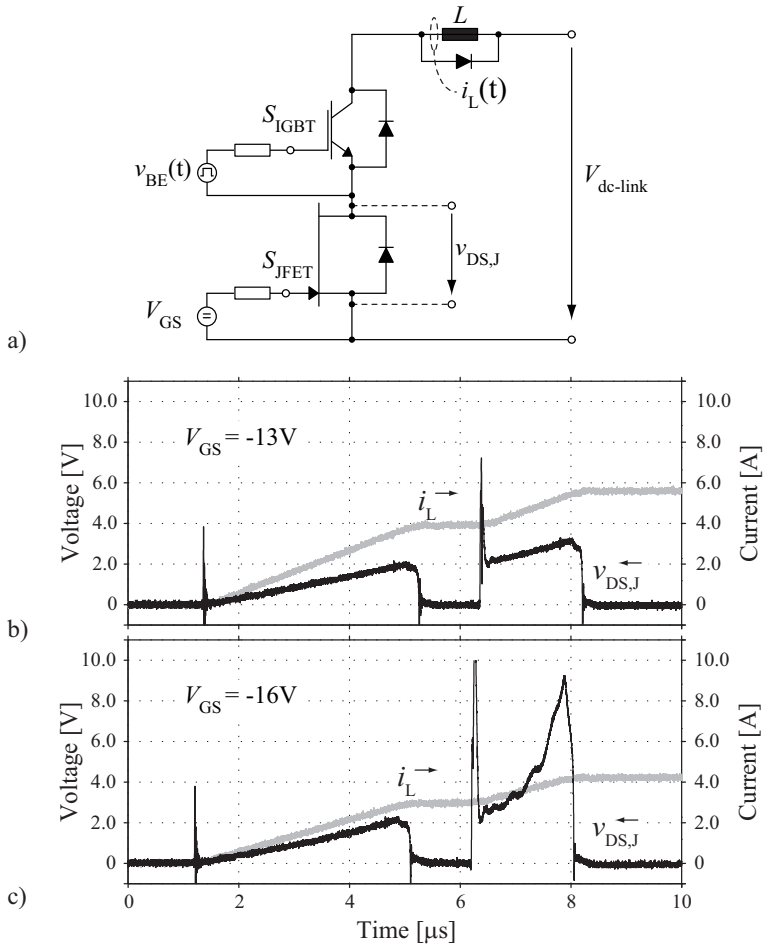

Figure 3.15: Schematic of the experimental setup for evaluating the SiC JFET (Nr. 13, Appendix A) behavior by impressed inductive current and partial pinched-off drain-source channel (a). Illustrated are i_L and $v_{DS,J}$ at (b) V_{GS} = -13 V and $V_{dc-link}$ = 800 V and (c) V_{GS} = -16 V and $V_{dc-link}$ = 600 V.

Entering numerical values in to Eq. (3.15) ($I_{D,SC} = 5\,\mathrm{A}$, $n = 6$ and $m = 3$) results in a worst case gate-source voltage at 25 °C of

$$v_{GS,Jn} = -22.825\,\mathrm{V}. \tag{3.16}$$

Considering the SiC JFETs pinch-off voltage range (cf. Appendix A) most SiC JFETs are already completely turned-off for such a gate-source voltage, i.e. the $R_{DS(on),Ji}$ is drastically increasing. This is especially critical due to the SiC JFET characteristic, which results in a significant increase of the on-resistance already for gate-source voltages smaller than the pinch-off voltage as shown in Figure 3.15. There, an experimental test setup has been performed to evaluate the SiC JFET switching behavior with an nearly pinched-off channel and an impressed inductive current. In Figure 3.15 (b) the gate-source voltage of the SiC JFET is constant $V_{GS} = -13\,\mathrm{V}$ and characteristic current and voltage waveforms are depicted for a proper inductive double pulse. Decreasing the gate-source voltage to $V_{GS} = -16\,\mathrm{V}$, whereas the pinch-off voltage of the device under test is $V_{p-off} = 23.9\,\mathrm{V}$, results in a sharp increase of the drain-source voltage $v_{DS,J}$ while the inductive load current is increasing linearly. This effect is caused by the almost pinched-off channel and/or significantly higher on-resistance.

Beside the theoretical analysis, an extended SPICE simulation model is implemented to confirm the findings by simulation results. Figure 3.16 shows key waveforms describing the current limiting effect of the *MSiSiCSC*. There, continuous simulation results for three on-off-cycles are presented. The drain currents $i_{D,J1} \ldots i_{D,J6}$ are slowly increasing to illustrate the current limitation. In Figure 3.16 (b) the drain-source voltages and (c) the gate-source voltages are illustrated. In the first on-state interval, the *MSiSiCSC* shows a proper and fast switching behavior. However, the SiC JFETs are not properly turned-on i.e. the gate-source voltages don't reach $\approx 0\,\mathrm{V}$. The gate-source voltages of the upper SiC JFETs are far away from zero volts and are nearly equal to their pinch-off voltages ($V_{p-off,Ji}$=23 V). Slightly increasing of the load current decreases even more the gate-source voltages as illustrated with the second and third simulation cycle. At a certain point, the gate-source voltage affects the SiC JFET channel and the on-resistance increase sharply. In turn this influences first the forward voltage drop of the upper SiC JFETs and finally the entire Si-SiC SuperCascode as simulated in the third cycle.

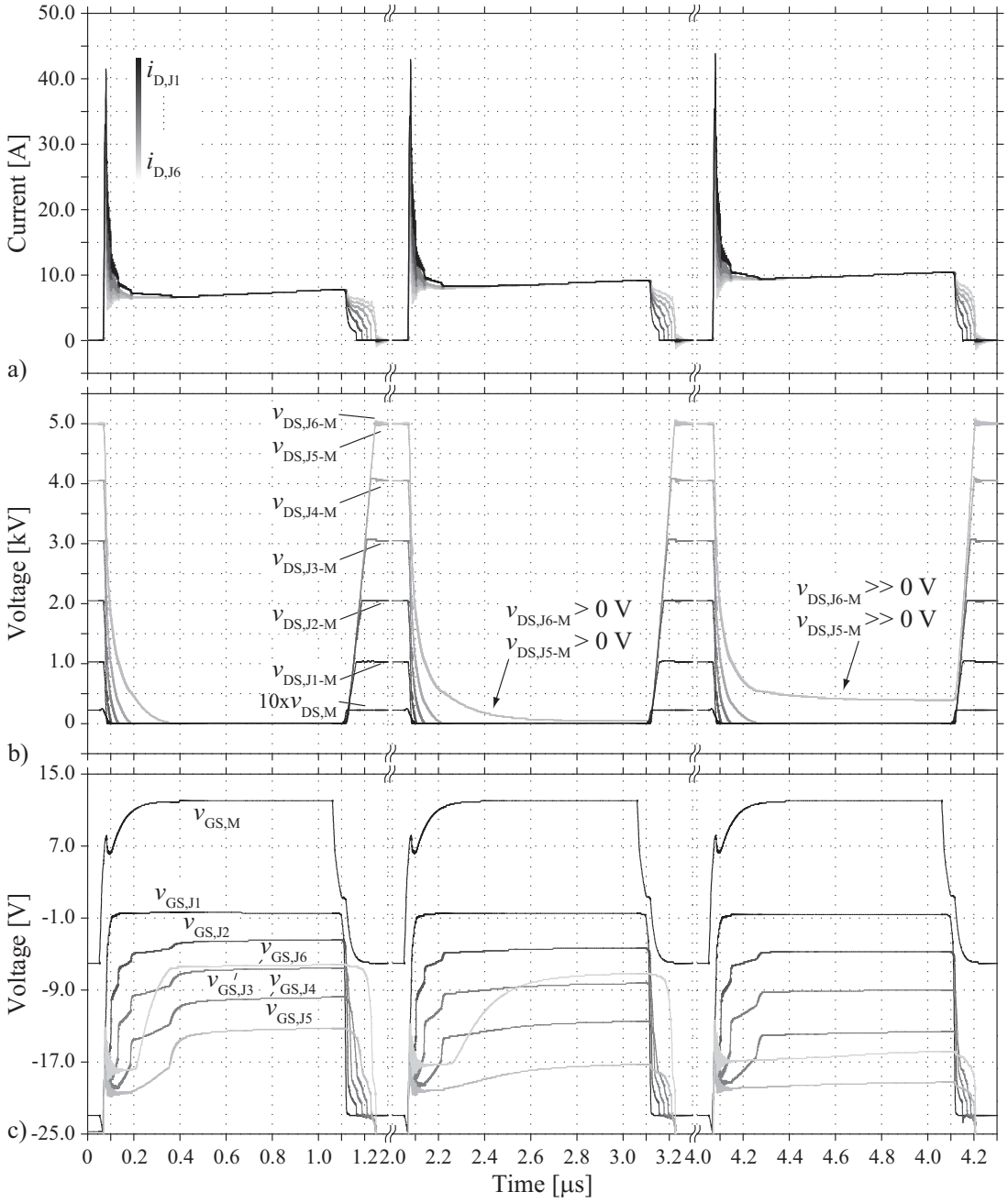

Figure 3.16: SPICE simulation results of the *MSiSiCSC* illustrates the current limiting effect and shows the enormous voltage drop of the Si-SiC SuperCascode, caused by the voltage drop across the on-resistances and forward voltage drop of the balancing diodes, during on-state mode and for different inductive load currents. (a) Shows the drain current of each SiC JFET $i_{D,J1} \ldots i_{D,J6}$; (b) the drain-source voltages $v_{DS,M} \ldots v_{DS,J6-M}$ of all switches stacked in series are illustrated; (c) the corresponding gate-source voltages $v_{GS,M} \ldots v_{GS,J6}$ are presented.

The current limitation effect of the *MSiSiCSC* is mainly caused by the drain-gate capacitance $C_{DG,Ji}$ (also called 'Miller' capacitance) of each SiC JFET. Compared to the nonlinear junction capacitance C_{DAVim} the nonlinear drain-gate capacitor shows a significantly larger value and the relation can be expressed as

$$C_{DG,Ji} >> C_{DAVim}. \tag{3.17}$$

At turn-on, these parasitic capacitors must be discharged and therefore the SiC JFET gates reach a negative potential considering the forward voltage drop of the series connected balancing diodes (assuming the MOSFET source potential as reference). In combination with the voltage drop across each SiC JFET and the Si MOSFET channel on-resistance, the gate-source voltages of the upper SiC JFET are closer to the corresponding pinch-off voltage than to zero volts which is required for proper on-state mode.

The considerations of the current limitation effect in the *MSiSiCSC* have been made at a temperature of 25 °C. Resulting was a gate-source voltage equal or above to the pinch-off voltage. Assuming an elevated temperature of 125 °C, which is existing in a continuously operating power electronic systems, the condition is even worse due to the positive temperature coefficient of the SiC JFET devices.

3.4.2 Reduction of the Current Limitation Effect

In order to reduce the influence of the diode forward voltage drop and the voltage drop across the single SiC JFETs, two possibilities are considered:

- using a lower on-resistance SiC JFET (120 mΩ/1.2 kV/20 A, SiCED),
- develop an additional passive circuit for reducing the current limitation effect.

The lower on-resistance of 120 mΩ results in a lower voltage drop at the nominal current. However, the larger die size leads most probably to an increased drain-gate capacitance which causes discharging currents flowing through the balancing diodes. Therefore, the gate-source voltage levels are expected to be similar as for the evaluated SiC JFET (1.2 kV/5 A). For verification, experimental test would have to be performed with an according *MSiSiCSC* setup. Since, 120 mΩ SiC JFET

became available only at the end of this thesis, this possibility was not pursued any further.

The investigation and evaluation (cf. Section 3.4) of the current limitation effect resulted in the development of an additional auxiliary circuit for the Si-SiC SuperCascode which is introduced and analyzed in the next chapter.

3.5 Novel Modified Si-SiC SuperCascode

The *MSiSiCSC* topology has been investigated in detail based on experimental and simulation result in the previous chapters. It was figured out, that the proposed topology is showing proper inductive and resistive switching behavior for low load currents. At larger load currents, the analysis of the *MSiSiCSC* topology showed, that an additional auxiliary passive circuit, called - current limitation prevention circuit - is required. Therefore, the resulting Si-SiC SuperCascode topology is herein called 'Novel Modified' Si-SiC SuperCascode (***NMSiSiCSC***). The novel topology as well as the current limitation circuit is introduced in the following.

3.5.1 Modified Switch Topology & Operating Principle

The schematic of the *NMSiSiCSC* topology is depicted in Figure 3.17, where the circuit extension is already included. In this circuit, small capacitors C_{CLi} and Zener diodes D_{CLi} are connected in parallel and in series to the voltage balancing diodes D_{AVim}. The additional capacitors are charged up by the leakage current flowing in the off-state and during turn-off, until the antiparallel Zener diodes limit the rising voltage. The voltage across the capacitors (comparable with a constant voltage source) compensates the voltage drop across the voltage balancing diodes and also partly the voltage drop caused by the on-resistance. Therefore, the required Zener voltage can be approximately calculated from Eq. (3.11) and Eq. (3.12) as

$$V_{R,DCLi} \approx m \cdot V_{F,DAVim} + I_{D,SC} \cdot R_{DS(on),Ji}. \tag{3.18}$$

The upper limit of the Zener diode/capacitor voltage is reached, when

during the on-state the gate-source diode of the JFETs start to conduct, what discharges the capacitors rapidly. In any case during turn-on the capacitor C_{CLi} voltage drops because the parasitic drain-gate capacitor of the corresponding JFET is discharged. To limit the voltage drop, the

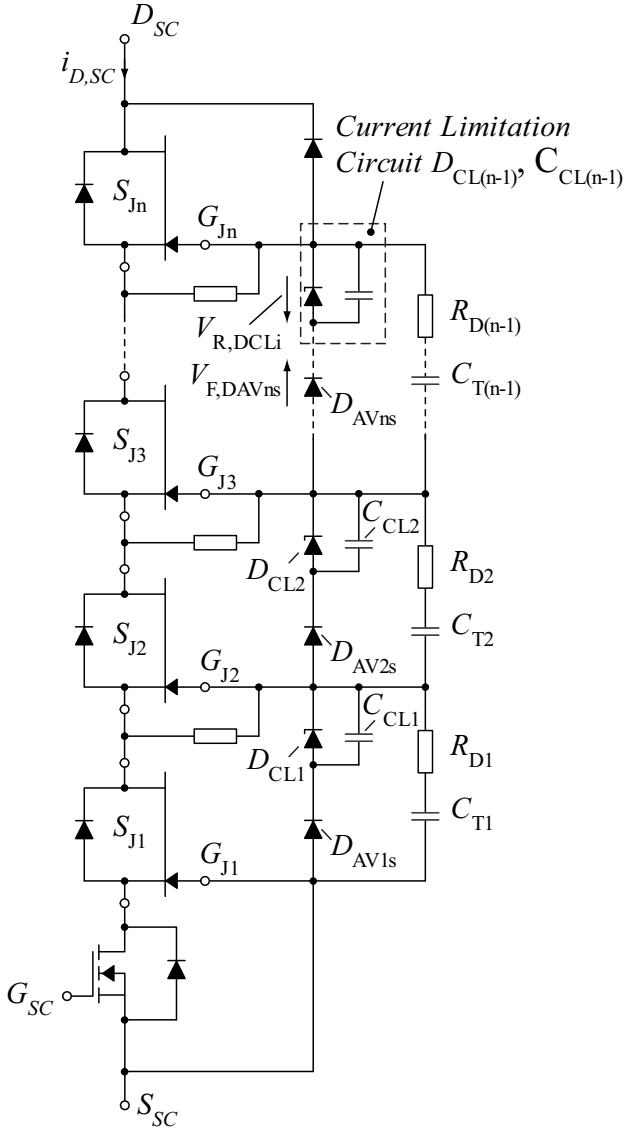

Figure 3.17: Novel modified Si-SiC SuperCascode topology with proposed auxiliary circuit consisting of capacitors $C_{CL1} \dots C_{CL(n-1)}$ and Zener diodes $D_{CL1} \dots D_{CL(n-1)}$ for compensating the voltage drop across the balancing diodes and the on-resistances of each SiC JFET, so that an increase of the forward voltage drop of the SuperCascode at higher drain currents is avoided.

selected capacitor should be much larger than the drain-gate capacitance, i.e.

$$C_{CLi} >> C_{DG,Ji}(@v_{DG,Ji} = 0\,\mathrm{V}). \tag{3.19}$$

In the following, simulation and experimental results are presented to verify the necessity of the current limitation prevention circuit. In Figure 3.18 SPICE simulation results are depicted, achieved with the same

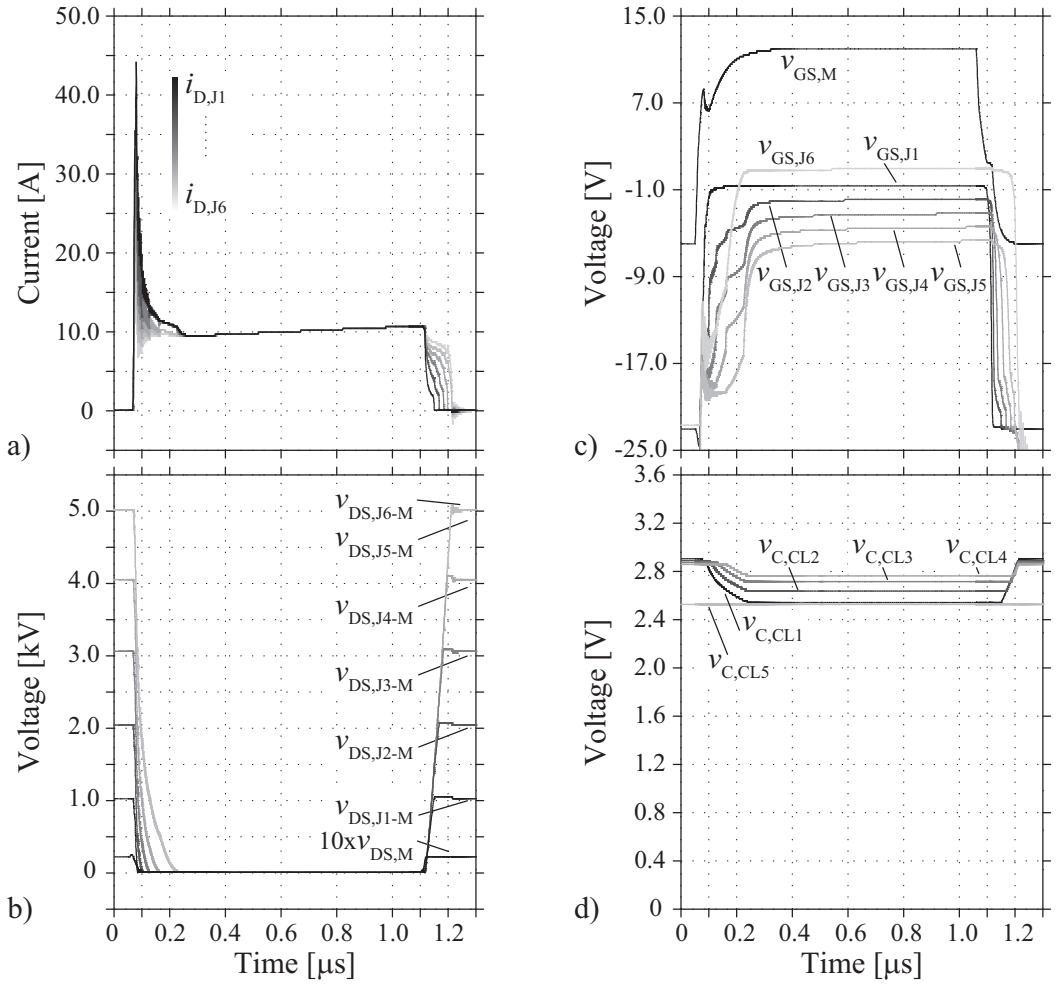

Figure 3.18: SPICE simulation results of the *NMSiSiCSC*. Following simulation waveforms are shown; (a) SiC JFET drain currents , (b) Si-SiC SuperCascode drain-source voltages, (c) MOSFET and SiC JFET gate-source voltages and (d) voltage across the capacitor of the current limitation prevention circuit ($V_{R,DCLi} = 3.3\,\mathrm{V}$, $C_{CLi} = 1\,\mu\mathrm{F}$).

simulation parameters and/or circuit as the results illustrated in Figure 3.16 for the third turn-on cycle, except that in Figure 3.18 the current limitation prevention circuit was included. The load current of the two simulation runs are the same and so are the drain-source currents. The drain-source voltages show a fast and proper turn-on transient and on-state behavior in Figure 3.18. Comparing the gate-source voltages from Figure 3.16 and Figure 3.18 makes obvious that the gate-source voltages are kept small and close to zero volts in the *NMSiSiCSC* topology due to the added current limitation prevention circuit. Finally, the capacitor voltages $v_{C,CLi}$ of the current limitation circuits are shown in Figure 3.18 (d). The local steady state capacitor voltage in the off-interval is around 2.9 V whereas the voltage during on-state depends on the position of the capacitor in the stacked switch. The voltage of the lower positioned capacitor is 2.55 V and for upper located capacitor 2.7 V. The reason of this voltage difference is that the parasitic drain-gate capacitor discharging currents are conducted through the balancing diodes and the largest discharge current occurs at the first balancing diode.

In Figure 3.19, the experimental verification of the current limitation prevention circuit is presented for resistive and inductive load. Both measurements show a proper switching behavior and/or a forward voltage drop is avoided.

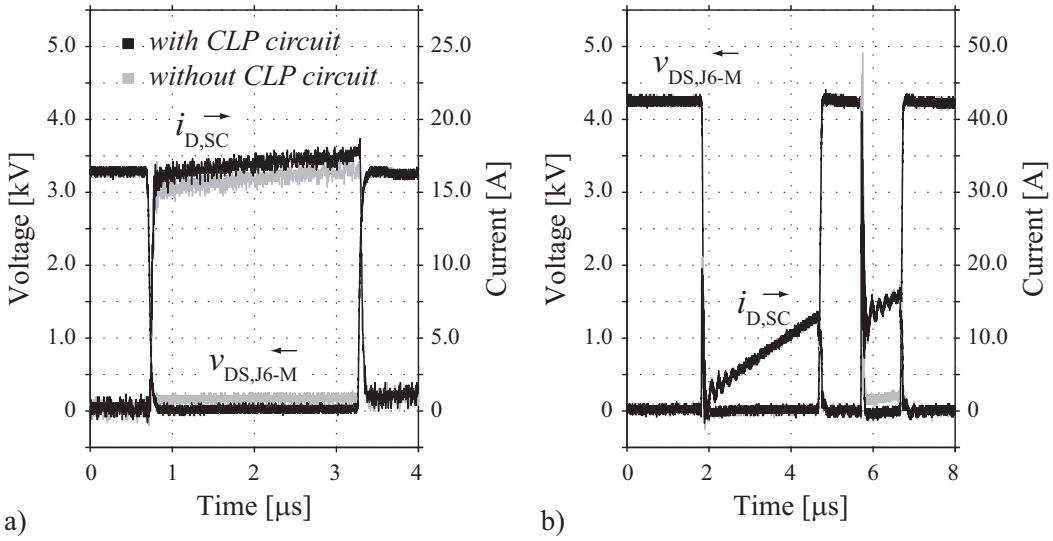

Figure 3.19: Experimental measurements with and without current limitation prevention (*CLP*) auxiliary network; (a) resistive load and (b) inductive load.

3.6 Experimental Results (*NMSiSiCSC*)

In this section, further experimental results of the *NMSiSiCSC* are presented. The measurements have been performed with inductive and resistive load and using the test setup shown in Figure 3.8 (c).

3.6.1 Inductive Load

The experimental measurements in Figure 3.20 (a) and (b) are performed using the same load and test circuit configurations. The only difference is that the semiconductors (SiC diodes and Si-SiC SuperCascode) are not mounted to a heat sink for (a) whereas the devices are mounted to a heat sink in (b). As the base plates of the TO-220 packages and the heat sink are forming parasitic parallel-plate capacitors $C_{TO220-HS}$, larger peak currents and/or turn-on oscillations are resulting. The approximate value of parasitic package-heat sink capacitance is calculated to

$$C_{TO-220-HS} = \epsilon_0 \epsilon_r \cdot \frac{A_{TO-220}}{d} \approx 55\,\text{pF}. \tag{3.20}$$

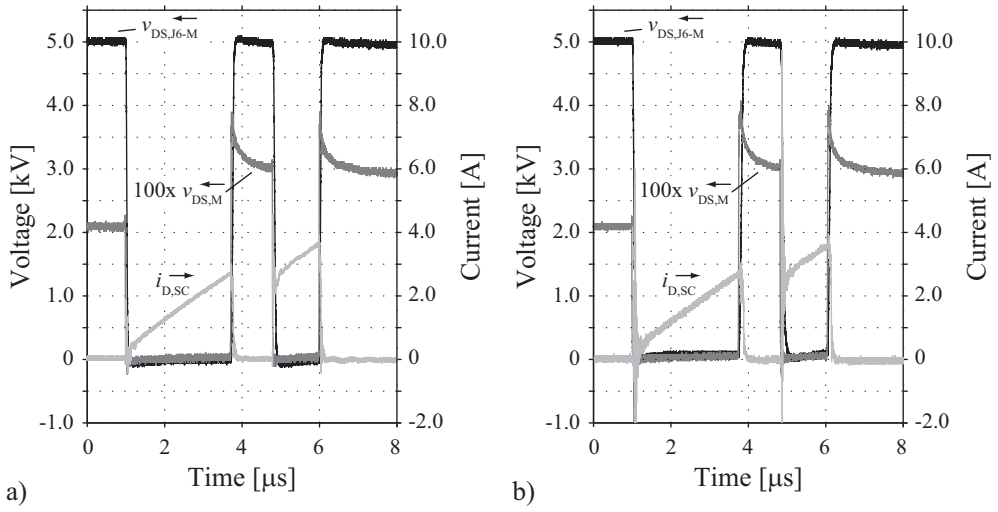

Figure 3.20: Double pulse measurements (buck topology: SiC diode/Si-SiC SuperCascode) with inductive load at a dc-link voltage of 5 kV: (a) semiconductor devices are not mounted to a heat sink. (b) semiconductor devices are mounted on a heat sink resulting in parasitic capacitive currents to ground.

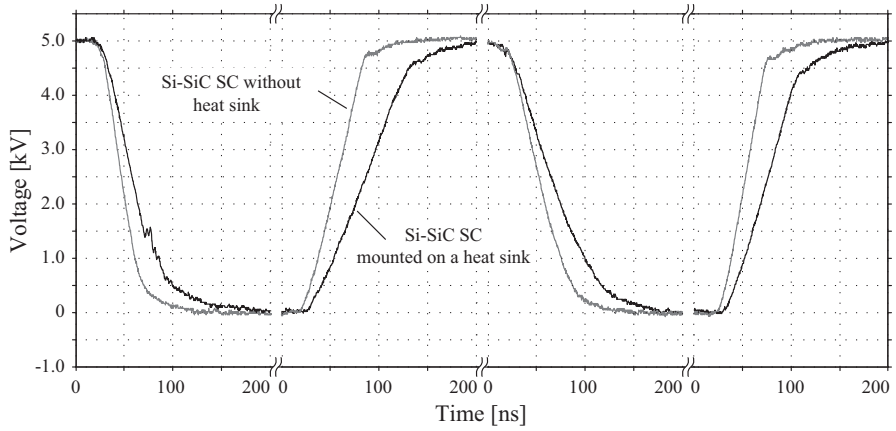

Figure 3.21: Zoomed view of turn-on/off transients of the drain-source voltages $v_{DS,J6-M}$ shown in Figure 3.20 (a) and (b).

Special in the Si-SiC SuperCascode configuration is that each parasitic capacitor to the heat sink sees a different potential at turn-on and therefore the induced capacitive earth current is proportional to the corresponding dv/dt. Zooming into the drain-source voltage $v_{DS,J6-M}$ on/off and off/on transition of Figure 3.20 (a) and (b) and combining the on/off transients in Figure 3.21 allows to compare the rise and fall times of both measurements. Obviously, the voltage edges without heat sink are generally about 50 ns faster for the on- and off-transients than the setup where

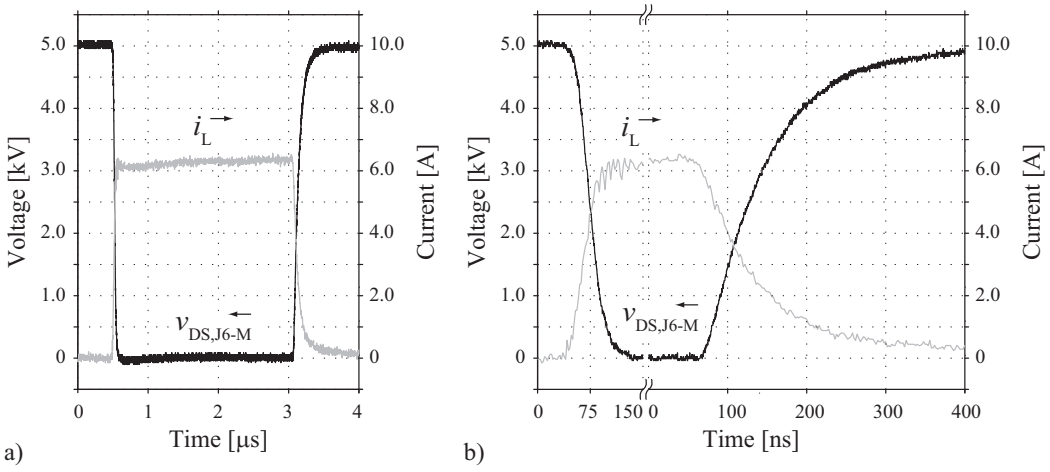

Figure 3.22: (a) Measurement result for the *NMSiSiCSC* with a gate voltage of 12 V and 800 Ω purely resistive load. (b) Zoomed view around turn-on and turn-off.

the parasitic package heat sink capacitors take effect.

3.6.2 Resistive Load

In Figure 3.22 the experimental results for resistive switching behavior are presented. There, measurements of the switch voltage $v_{DS,J6-M}$ and the load current i_L for a purely resistive load have been performed. The 90 % - 10 % fall time of the voltage is smaller than 50 ns and significantly smaller compared to the resistive measurments presented in Figure 3.11. The fall time is also in the range of 100 ns, but depending on the load current, as the Si-SiC SuperCascode turns-off very fast and then the $\mathrm{d}v/\mathrm{d}t$ is only determined by the output capacitance and the load current charging the capacitor.

Component	**Specification**
SiC VJFET S_{Jn}	SiCED JFET, TO-220 V_{DS}=1200 V, I_D=5 A, $R_{DS(on)}$=0.3 Ω
Si MOSFET S_M	IR, IRLR024N, D-Pak V_{DS}=55 V, I_D=17 A, $R_{DS(on)}$=65 mΩ
Resistor R_{GSn}	Standard SMD resistor, 1206 R = 243 kΩ, P_{diss}=125 mW, V_{DC}=200 V
Zener Diode D_{AVni}	VISHAY, BZG03C270(200), DO214AC $V_{Z(typ)}$=270 V ∀ i∈{1,2,3}, $V_{Z(typ)}$=200 V ∀ i=4 P_{diss}=1.25 W, V_F=1.2 V
Pulse Resistor R_{Dn}	VISHAY, CMB 0207, MELF, R = 100 Ω (R_{Dn}=50 Ω), continuous pulse load capability
HV Capacitor C_{Tn}	SMD capacitor, 1206, X7R V_{DC}=2 kV, $C_{T1}\ldots C_{T5}$={100,88,66,33,15} pF
Zener Diode D_{CLn}	SMD Zener diode, SMB $V_{Z(typ)}$=3.3 V, P_{diss}=1.5 W, V_F=1.5 V
LV Capacitor C_{CLn}	SMD capacitor, 0805, X7R V_{DC}=25 V, C_{CLn}=1 μF

Table 3.1: Components of the novel Si-SiC SuperCascode (cf. schematic shown in Figure 3.23 and realized hardware prototype in Figure 5.3).

3.7 Power Losses of the Novel Si-SiC Super-Cascode

Finally, the power losses of the Si-SiC SuperCascode (*NMSiSiCSC*) are analyzed and calculated. The total power losses of the Si-SiC SuperCascode are due to semiconductor losses and losses of the auxiliary network. The reference and final switch configuration is presented in Figure 3.23 and the components used in the laboratory prototype are listed in Table 3.1. The derivation of the power losses is made analytically for n cascaded SiC JFETs and finally numerically calculated for six cascaded SiC JFETs ($n = 6$) as realized for the prototype. The Si-SiC SuperCascode losses are subdivided into static blocking losses, conduction losses and switching losses.

3.7.1 Static Blocking Losses

In Section 3.1.3 the static off behavior has been described and the necessity of a well defined leakage current for a proper static voltage distribution has been figured out. Because of this leakage current through the components and the applied blocking voltages, static blocking losses occur in the Si-SiC SuperCascode configuration. Figure 3.24 illustrates the static off condition with the leakage currents and the applied voltages for a part of the *NMSiSiCSC*. As given in Eq. (3.2) the gate-source resistors R_{GSi} and the corresponding SiC JFET pinch-off voltages are defining the leakage currents $I_{\sigma i}$. In relation to the leakage currents flowing through the gate-source resistors, the leakage current appearing in the i-th SiC JFET can be expressed with

$$I_{\sigma,Ji} = I_{\sigma,Jn} - \sum_{s=i+1}^{n} I_{\sigma s}. \tag{3.21}$$

The leakage current occurring in the i-th group of series connected balancing diodes results in

$$I_{\sigma,Di} = I_{\sigma(i+1)} + I_{\sigma,D(i+1)} = \sum_{s=i+1}^{n} I_{\sigma s}. \tag{3.22}$$

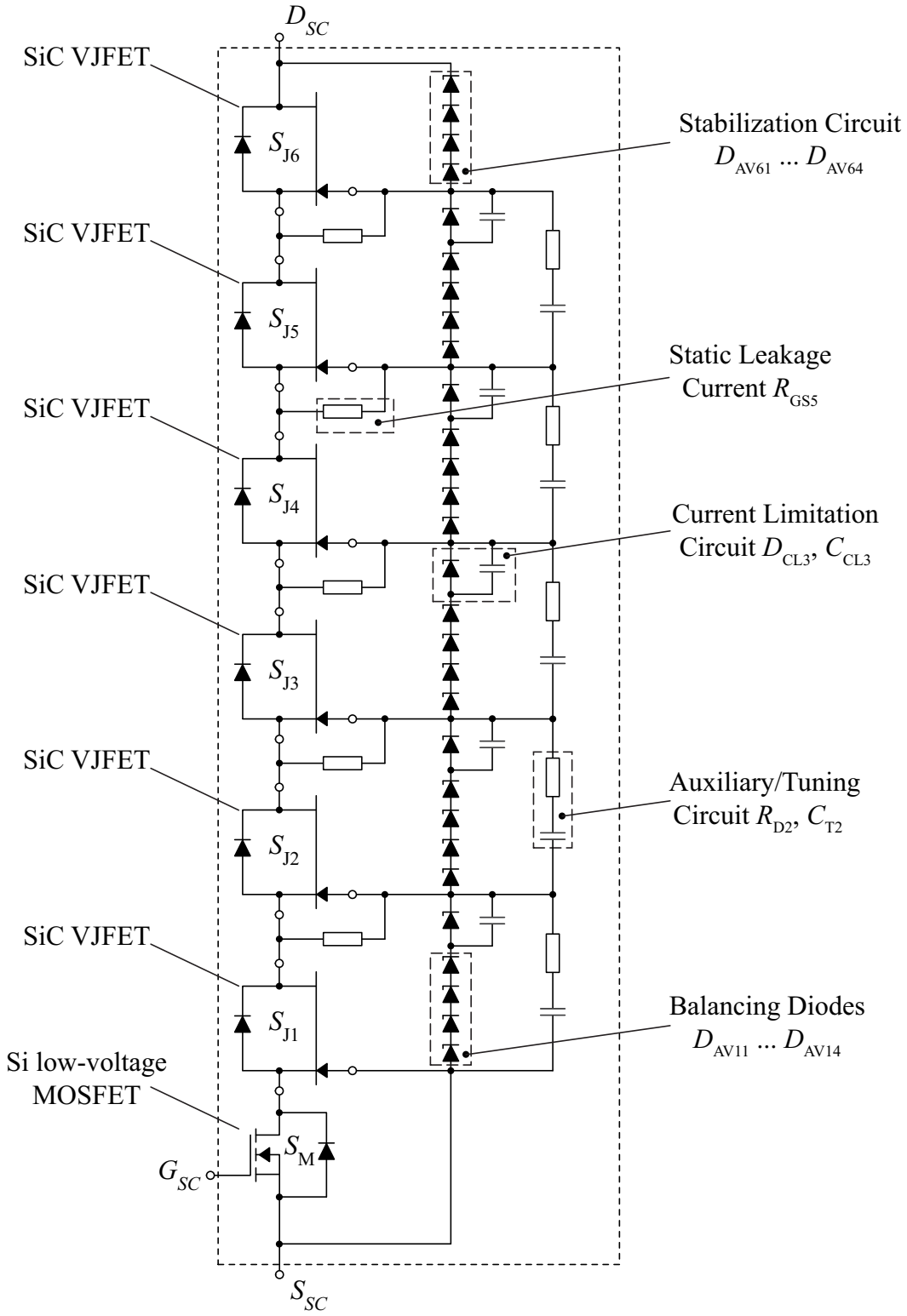

Figure 3.23: Schematic of the novel Si-SiC SuperCascode and realized high voltage switch (cf. Figure 5.3).

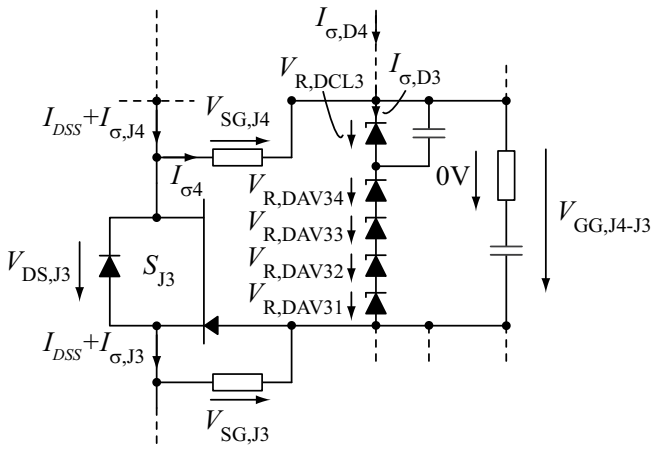

Figure 3.24: Part of the *NMSiSiCSC* circuit schematic considered for analyzing the leakage currents and the applied voltages during static off behavior.

Assuming, that the additional static leakage current of the series connected active components is I_{DSS} and the fact that $I_{DSS} \ll I_{\sigma i}$, I_{DSS} is neglected in the static off-state loss calculation. Out of this assumption the following equation is resulting

$$I_{\sigma,Jn} = I_{\sigma,D1}. \tag{3.23}$$

It is further assumed, that the leakage currents are dc currents and varying only marginally with temperature changes of the high value gate-source resistors.

The blocking voltages applied to the SiC JFETs are depending on the number m of series connected balancing diodes and their avalanche voltage value. Due to the blocking voltage capability of a single SiC JFET of 1.2 kV, a lower avalanche voltage is required. Therefore, four Zener diodes (m=4) are connected in series, whereas three of them are 270 V Zener diodes (D_{AVis}, s$\in\{1,2,3\}$) and one is 200 V Zener diode (D_{AVi4}). Additionally, the low-voltage Zener diode ($V_{Z,DCLi}$=3.3 V) of the current limitation prevention network has to be considered. Hence, the following analytical inequality is derived

$$V_{(BR),DSS,Ji} > \sum_{s=1}^{m-1} V_{R,DAVis} + V_{R,DAVi4} + V_{R,DCLi}. \tag{3.24}$$

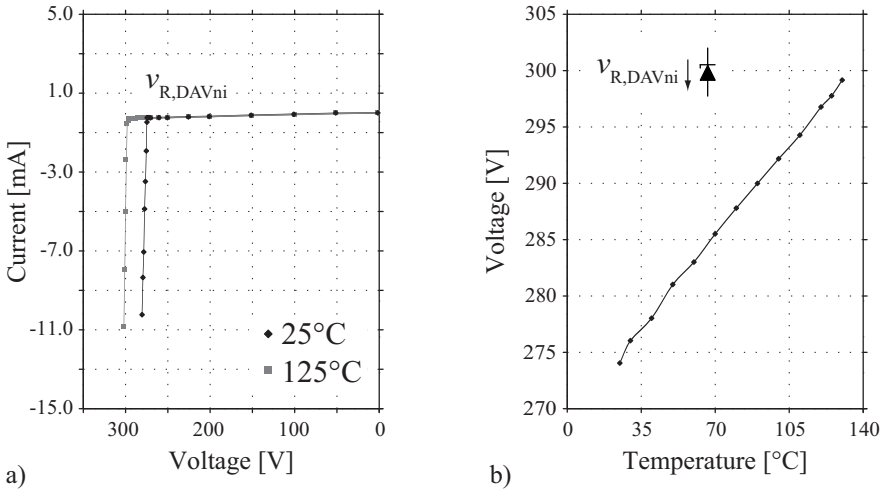

Figure 3.25: Static avalanche voltage of a single balancing diode D_{AVis} is increasing with higher temperature as illustrated in (a) and (b).

In Figure 3.25, static avalanche voltage measurements of a single 270 V Zener diode at a temperature of 25 °C and 125 °C are presented. Obviously, the avalanche characteristic of the employed Zener diode shows a positive temperature coefficient and therefore the absolute value of the avalanche voltage $|v_{D,AVis}|$ is increasing with the temperature. At a leakage current of $I_{\sigma,Di} < 0.1\,\mathrm{mA}$ avalanche voltages of

$$V_{R,DAVis(T=25\,^{\circ}\mathrm{C})} \approx 274\,\mathrm{V} \tag{3.25}$$

$$V_{R,DAVis(T=125\,^{\circ}\mathrm{C})} \approx 299\,\mathrm{V} \tag{3.26}$$

are achieved for the corresponding temperatures. The avalanche voltage difference caused by the increased temperature is 25 V only for a single Zener diode. As a consequence for the *NMSiSiCSC* the gate-source voltages and/or corresponding blocking voltages of the individual SiC JFETs are increasing with temperature as illustrated in Figure 3.26.[2] The experimentally defined voltages of the Si-SiC SuperCascode can be calculated

[2]Due to the compact layout of the *NMSiSiCSC* and thick cooper layer of the PCB connecting all the components, the balancing diodes are heating up together with the SiC JFETs which are mounted on the heating plate. The temperature is measured on the heating plate and therefore just an approximation of the actual diode temperatures.

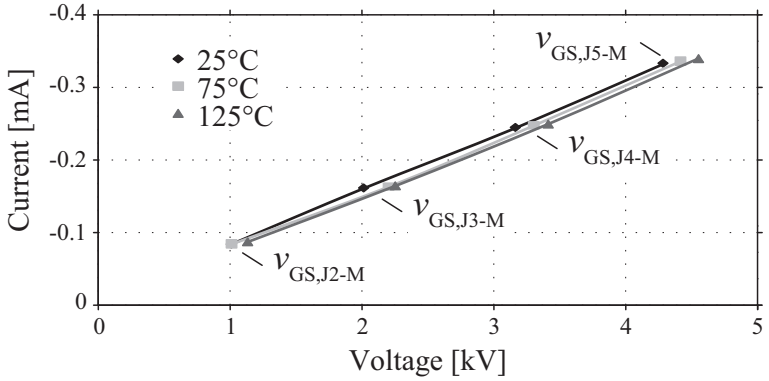

Figure 3.26: Static voltages $V_{GS,Ji-M}$ of the Si-SiC SuperCascode showing a positive temperature coefficient, i.e. the voltages are increasing with temperature.

by (i∈{1 . . . (n-1)})

$$V_{GG,J(i+1)-Ji} = V_{GS,J(i+1)-M} - V_{GS,Ji-M}. \tag{3.27}$$

Based on the avalanche voltages the blocking voltage of each SiC JFET can be calculated with

$$V_{DS,Ji} = V_{SG,J(i+1)} + V_{GG,J(i+1)-Ji} - V_{SG,Ji}. \tag{3.28}$$

Assuming, that the source-gate voltages $V_{SG,J(i+1)}$ and $V_{SG,Ji}$ are equal, the blocking voltage of each SiC JFET is increasing with the increase of the avalanche voltages of the series connected balancing diodes. The

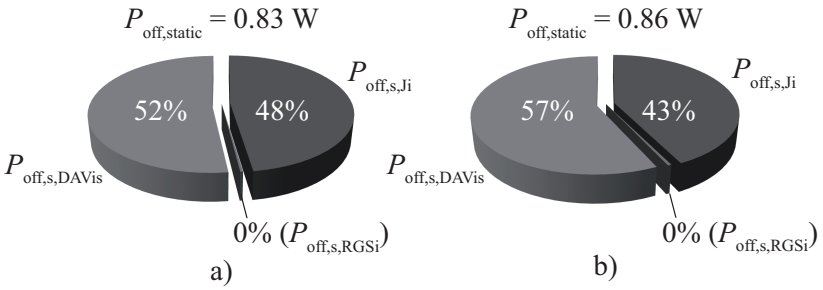

Figure 3.27: Distribution of the static blocking losses in the *NMSiSiCSC* at a total blocking voltage of $V_{DS,J6-M}$=5 kV, gate-source resistors of R_{GSi}=243 kΩ and a temperature of: (a) T=25 °C and (b) T=125 °C.

reverse gate-source characteristic of the SiC JFET is also varying with temperature as presented in [86]. However, a change ΔT on temperature takes much less influence on the source-gate voltage than on the avalanche voltage,

$$\Delta V_{SG,J(i+1)}(\Delta T) \ll \Delta V_{GG,J(i+1)-Ji}(\Delta T). \tag{3.29}$$

Based on the derived leakage currents and the voltages occurring across the respective components the static blocking losses can be calculated to

$$\begin{aligned} P_{off,static} &= P_{off,s,RGSi} + P_{off,s,Ji} + P_{off,s,DAVis} \\ &= \frac{1}{T_S}\int_0^{t_{off}} \Big(R_{GSi} \cdot \sum_{s=2}^{n} I_{\sigma s}^2 + \sum_{s=2}^{n} I_{\sigma,Js} \cdot V_{DS,Js} \\ &\quad + \sum_{s=1}^{n-1} I_{\sigma,Ds} \cdot V_{GG,J(s+1)-Js} \Big) dt. \end{aligned} \tag{3.30}$$

Figure 3.27 shows the calculated static off-state losses as well as the distribution to the JFET switches, balancing diode circuits and the gate-source resistors. The blocking losses are marginal and can be neglected for further power loss considerations. However, it has to be noted here, that the blocking losses could be critical for the balancing diodes which are not mounted to a heat sink. Furthermore, the leakage current is depending on the pinch-off voltage of each SiC JFET, the corresponding gate-source resistor and the number of cascaded SiC JFETs. Assuming only lower gate-source resistors of R_{GSi}=150 kΩ within the Si-SiC Super-Cascode would increase the leakage current and/or the static blocking losses from $P_{off,static}$=0.83 W to $P_{off,static}$=1.4 W at a temperature of 25 °C (dynamic avalanche losses are not included).

3.7.2 Conduction Losses

The on-state characteristic of the *NMSiSiCSC* is depending on different factors like load current, junction temperature of the power semiconductors and the SiC JFET gate-source voltages as analyzed in Section 3.4.1 in detail. Due to all these factors determining the occurring on-resistance accurately for each discrete device of the *NMSiSiCSC* is challenging.

On the one hand the power semiconductor on-resistance increases

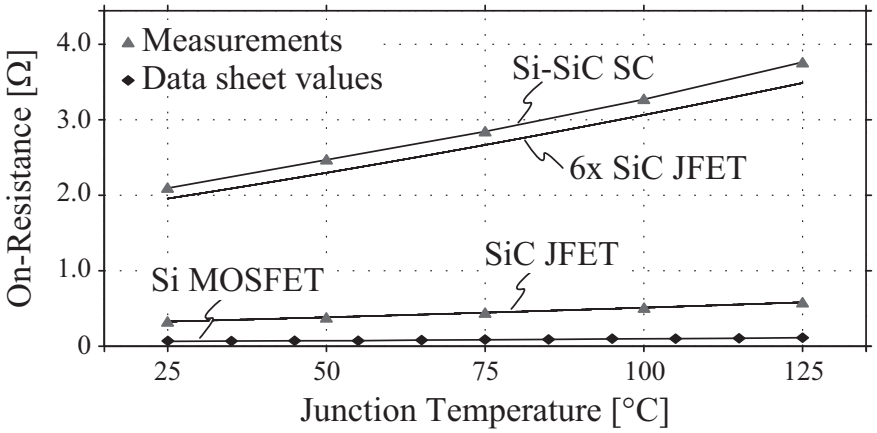

Figure 3.28: Experimentally determined dependence of the on-resistance of a single SiC JFET on the junction temperature T_j and quasi ideal on-resistance ($V_{GS,Ji} \approx 0\,\mathrm{V}$) of the Si-SiC SuperCascode. The on-resistance of the low-voltage Si MOSFET is small compared to the cascaded SiC JFETs.

with the junction temperature T_j as illustrated in Figure 3.28 for the low-voltage MOSFET and the SiC JFET. The SiC JFET on-resistance can be analytically well expressed in dependency on the junction temperature with

$$R_{DS(on),J}(T_j) = R_{DS(on),J}(25\,^{\circ}\mathrm{C}) \cdot \left(\frac{(T_j + 273.15\,\mathrm{K})}{298.15\,\mathrm{K}} \right)^{2.0}, \quad (3.31)$$

where T_j is given in °C The on-resistance of the Si-SiC SuperCascode results in six times the single SiC JFET on-resistance given in Eq. (3.31). Comparing this ideal calculated value ($V_{GS,Ji} = 0\,\mathrm{V}$) to the measured on-resistance of the *NMSiSiCSC* (measured with low drain current $< 1\,\mathrm{A}$), a difference in on-resistance appears although the current limitation prevention circuit is implemented. This could be caused by the gate-source voltages which vary from zero volts (resulting in higher on-resistance) or small tolerances in the on-resistances of the individual SiC JFETs.

The gate-source voltages of the *NMSiSiCSC* during on-state are not zero and/or the SiC JFET channel is not opened completely. Therefore additional measurements of the dependency of the on-resistance on the load current and for partially pinched-off channels, are performed and presented in Figure 3.29. It is clearly visible that the on-resistance is increasing up to gate-source voltage $v_{GS,Ji}$ of $\approx$ -10 V and with increasing

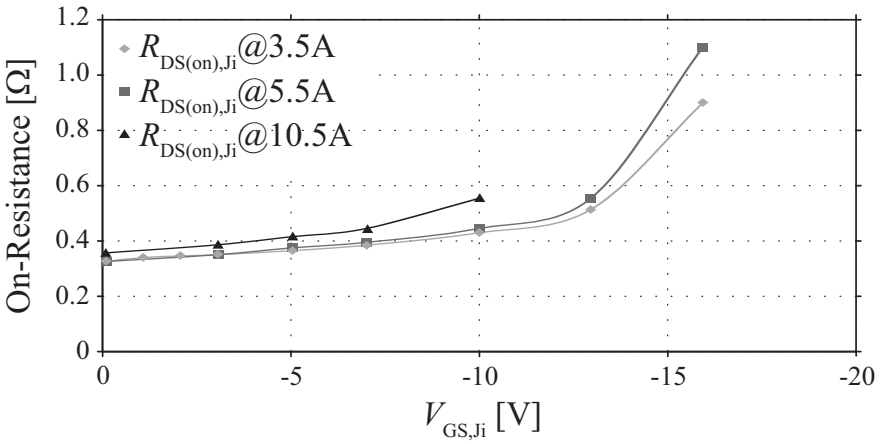

Figure 3.29: On-resistance of a single SiC JFET (V_{p-off}=23.9 V) depending on the corresponding gate-source voltage and drain current at T_j=25 °C.

drain current. With larger gate-source voltages the channel is more and more pinched-off and the on-resistance increases sharply.

The conduction losses of the *NMSiSiCSC* are derived as

$$P_{c,F} = I^2_{D(rms),SC} \cdot \Big(R_{DS(on),M}(T_j) + \sum_{i=1}^{n} R_{DS(on),Ji}(T_j; v_{GS,Ji}) \Big), \tag{3.32}$$

where each SiC JFET on-resistance is depending on the junction temperature T_j and the gate-source voltage $v_{GS,Ji}$.

Reverse Conduction

In freewheeling operation of the *NMSiSiCSC* the reverse current could flow in the anti-parallel body diode of the SiC JFET, in the balancing diodes, or in the SiC JFET channel. As already mentioned for the Si-SiC cascode, the two first aforesaid current paths are unlikely and have to be only considered at high drain currents larger than the nominal current. Therefore, the reverse conduction losses are only depending on the SiC JFET on-resistances and the negligible losses of the parasitic anti-parallel diode of the low-voltage MOSFET. The reverse conduction

losses are derived to

$$P_{c,R} = I_{revD(avg),SC} \cdot v_{FD,M} + I^2_{revD(rms),SC} \cdot \left(R_{D(on),M}(T_j) + \sum_{i=1}^{n} R_{DS(on),Ji}(T_j) \right). \quad (3.33)$$

In the freewheeling mode, the source potential of each SiC JFET is lower than the gate potential (reference potential is the MOSFET source) due to the voltage drop across the SiC JFET channel. Therefore, the SiC JFET channels are completely open and the on-resistance is only depending on the junction temperature.

Calculating the overall conduction losses of the *NMSiSiCSC* at nominal ratings of P_n=25 kW, V_1=5 kV,T_j=125 °C and with the phase-shift modulated dc-dc converter (cf. Chapter 4) results in

$$\begin{aligned} P_{c,total} &= P_{c,F} + P_{c,R} \\ &= 79.1\,\mathrm{W} + 6.0\,\mathrm{W} = 85.1\,\mathrm{W}. \end{aligned} \quad (3.34)$$

In forward conduction mode an average on-resistance per SiC JFET of 0.61 Ω is assumed to consider the influence of the gate-source voltages and in reverse conduction mode an on-resistance of 0.58 Ω is assumed (cf. Eq. (3.31)).

3.7.3 Switching Losses

For determining the switching losses of a fast, high voltage switch, built with discrete devices (*NMSiSiCSC*) accurately, an accurate voltage and current measurement has to be ensured. Both measurement have to be with high bandwidth and in addition an influence on the test setup and/or the switching transients by inserting the probes, especially the current sensor must be avoided. In general, it is important to use suitable measurement equipment to measure switching transients with $\mathrm{d}v/\mathrm{d}t$ values of about 100 $^{\mathrm{kV}}/_{\mu\mathrm{s}}$. The voltage probe and current sensor used for the switching loss measurements of the *NMSiSiCSC* are:

- *PPE 20 kV* (LeCroy): ≤ 20 kV dc incl. peak ac, 100 MHz, 100 MΩ, 1000:1

- current transformer: designed and assembled as described in [87] and [88].

The switching power losses, which occur in the *NMSiSiCSC* are depending on various parameters. In particular, the selection of the free-

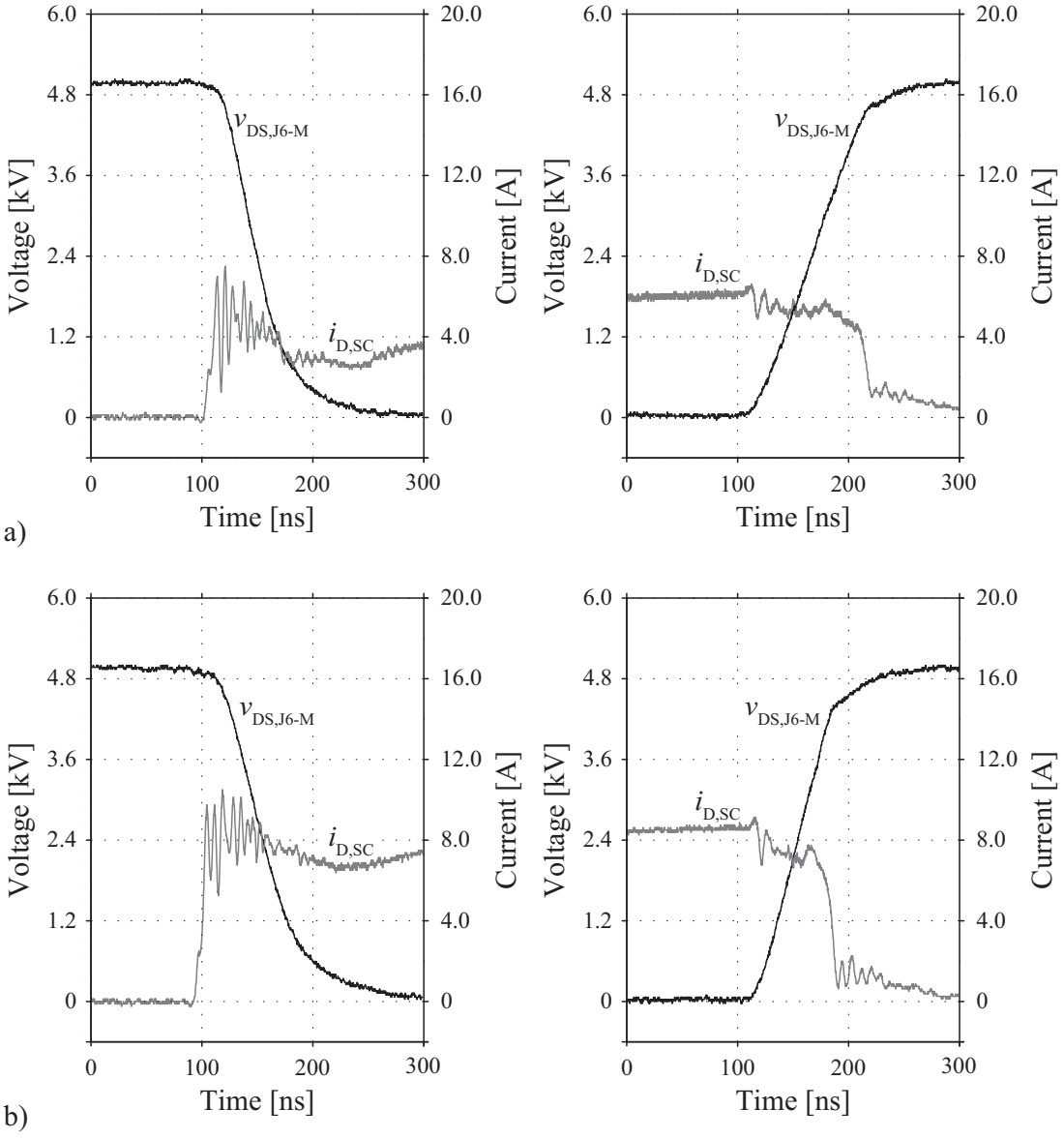

Figure 3.30: Switching behavior of the *NMSiSiCSC* in a buck topology (cf. Figure 3.32 (b)) using series connected SiC diodes as freewheeling diode at a junction temperature of 75 °C: (a) Turn-on/off transient for 3 A/6 A and (b) turn-on/off transient for 7 A/9 A.

wheeling diode in combination with the Si-SiC switch is of importance, because the reverse recovery characteristic of the diode influence significantly the switching behavior. To minimize this effect SiC diodes from CREE C2D10120D, stated as zero reverse recovery current, are used in the switching loss measurements. A substantial further influencing factor is the mechanical setup and/or associated parasitic capacitances (cf. Section 3.6) and commutation inductances. In order to measure the occurring switching losses of the *NMSiSiCSC* accurately any parasitic capacitive current must be avoided what is a challenge at $\mathrm{d}v/\mathrm{d}t$ values of $100\,\mathrm{kV}/\mu\mathrm{s}$ and a dc voltage of 5 kV since the oscilloscope is capacitive coupled to the grid (despite the use of isolation transformers).

In consequence, a *NMSiSiCSC* module is developed which comprises a complete high voltage switch with the additional auxiliary circuits. Therefore, the switching losses can be evaluated using a test bench which includes the final arrangement of all discrete devices and their mounting on a heat sink.

In Figure 3.30 measured on/off switching transients of the *NMSiSiCSC* are depicted. The evaluation of the turn-on/off energies at discrete switch currents and device junction temperatures of 25 °C, 75 °C and 125 °C result in energy loss functions shown in Figure 3.31. The current dependency of the energy losses can be approximated with a linear polynomial

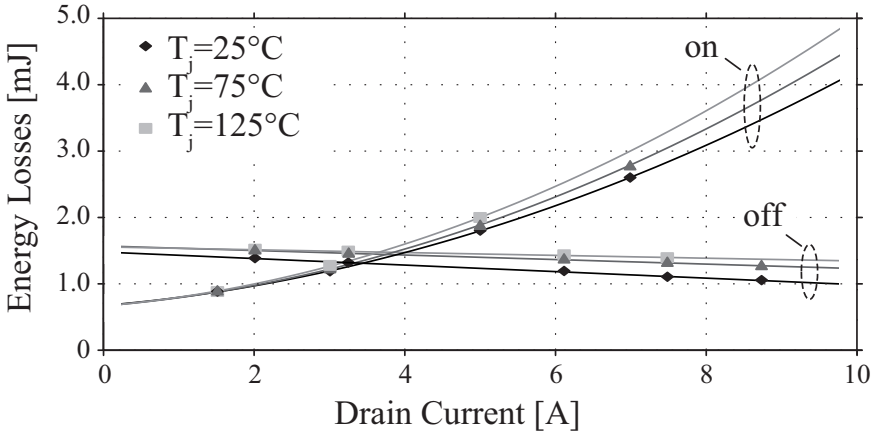

Figure 3.31: Experimentally determined switching energy losses of the *NMSiSiCSC* depending on the switched current $i_{D,SC}$. The switching loss measurements are performed at different temperatures and at the nominal voltage of 5 kV.

on	$k_{2,SC}[mWsA^{-2}]$	$k_{1,SC}[mWsA^{-1}]$	$k_{0,SC}[mWs]$
$T_j = 25\,^{\circ}\mathrm{C}$	0.0257923	0.0988583	0.68474
$T_j = 75\,^{\circ}\mathrm{C}$	0.0299943	0.0972464	0.678136
$T_j = 125\,^{\circ}\mathrm{C}$	0.0338291	0.101223	0.676857
off	$k_{2,SC}[mWsA^{-2}]$	$k_{1,SC}[mWsA^{-1}]$	$k_{0,SC}[mWs]$
$T_j = 25\,^{\circ}\mathrm{C}$	-	-0.0490177	1.47881
$T_j = 75\,^{\circ}\mathrm{C}$	-	-0.0339803	1.57008
$T_j = 125\,^{\circ}\mathrm{C}$	-	-0.0211619	1.5562

Table 3.2: Switching power loss parameters for calculating the turn-on/off losses of the *NMSiSiCSC*.

for off-behavior and second order polynomial for on-behavior,

$$E_{on,SC}(T_j) = k_{2,SC}(T_j) \cdot i_{DS}^2 + k_{1,SC}(T_j) \cdot i_{DS} + k_{0,SC}(T_j), \quad (3.35)$$

$$E_{off,SC}(T_j) = k_{1,SC}(T_j) \cdot i_{DS} + k_{0,SC}(T_j). \quad (3.36)$$

The corresponding calculated coefficients of the polynomials are listed in Table 3.2.

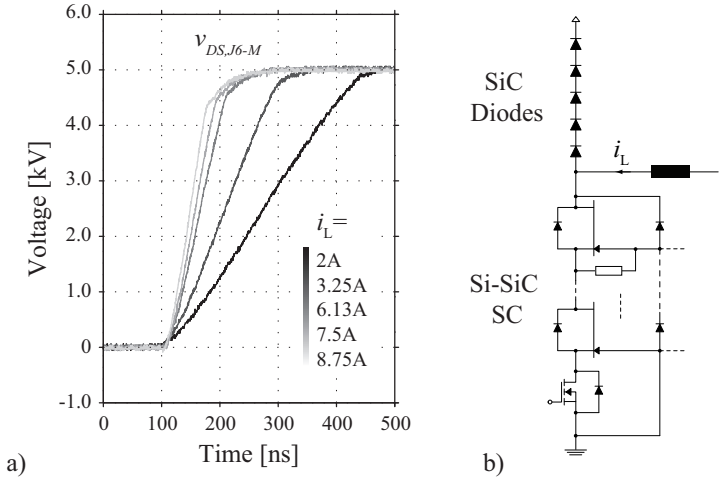

Figure 3.32: (a) Voltage waveforms during turn-off for different load currents. (b) Schematic of the experimental setup (cf. Figure 3.8).

The resulting switching losses in Figure 3.31 show that with elevated temperatures the turn-on energy losses are increasing with second order. However up to the nominal current of 5 A the turn-on energy losses are almost temperature independent. The turn-off energy is approximately independent of the drain current. This is caused by the parasitic capacitances of the HV switch, which enables soft switching conditions during turn-off. In Figure 3.32 the voltage waveforms for different load currents are shown. There, it could be seen that the $\mathrm{d}v/\mathrm{d}t$ is only controlled by the load current and the parasitic capacitances. Therefore, the turn-off energy, is the energy stored in the parasitic capacitors and the turn-off losses of the SiC JFETs are negligible.

3.8 Avalanche Behavior

In order to utilize the *NMSiSiCSC* as a fast high voltage switch in e.g. flyback or forward converter, safe operation under avalanche has to be ensured. Therefore, the avalanche behavior of the Si-SiC SuperCascode is analyzed and discussed in the following. At this point, it should be considered that a deeper physical discussion about the dynamic avalanche behavior of diodes and power switches is beyond the scope of this thesis.

To prevent transient overvoltages as e.g. caused by leakage inductances of transformers or wiring inductances, usually passive snubbers are applied across the switch. Generally, snubber circuits have to be designed with a sufficient margin to the maximum rated blocking voltage which could lead to significantly snubber power losses. To reduce or even avoid snubber circuits, the power electronics design has to fulfill one of the following requirements: (1) the power switch provides a blocking voltage much higher than the dc supply voltage and therefore never reaches the avalanche mode; (2) the avalanche of the power switch regularly occurs for limiting transient switching overvoltages. The requirement (1) cannot be satisfied in the intended applications due to the proportional increase of the on-resistance and/or resulting higher conduction losses. With a high avalanche robustness of the switch, snubberless operation becomes possible and furthermore costs on the system level are reduced what could be interesting, considering the comparably high costs of SiC components [89].

In practice, for the avalanche operation of a power semiconductor

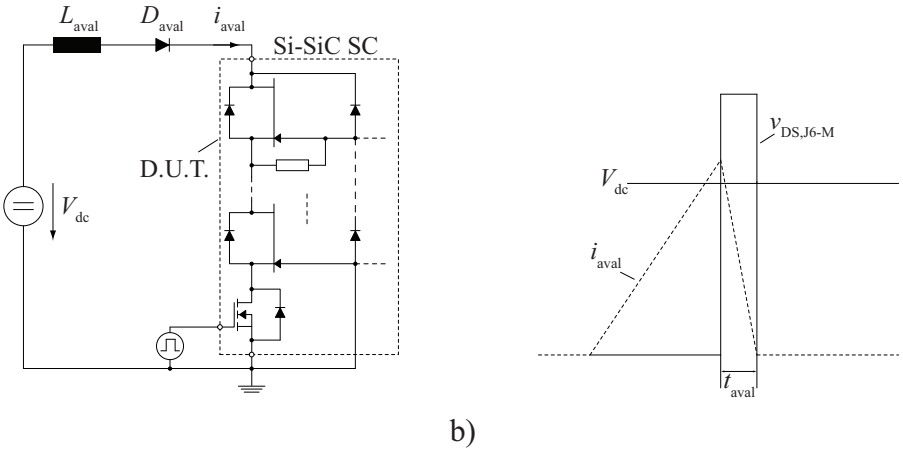

Figure 3.33: (a) Unclamped inductive switching test circuit. (b) Unclamped inductive switching waveforms.

switch two modes have to be distinguished [90]:

- single pulse avalanche energy E_{AS}
- repetitive avalanche energy E_{AR}.

A typical circuit for performing avalanche tests and the theoretical unclamped inductive switching waveforms are illustrated in Figure 3.33. First, the device under test (D.U.T., herein the *NMSiSiCSC*) is turned-on and the current $i_{D,SC}$ increases due to the dc-link voltage V_{dc} which is applied across the inductor L_{aval}. When the D.U.T. is turned-off, the voltage increases to the avalanche breakdown level. There, the diode D_{aval} guarantees, that no current is flowing back to the supply. The current decreases nearly linearly and the energy stored in the inductor,

$$E_A = 0.5 \cdot L_{aval} \cdot i^2_{D,SC,off}, \tag{3.37}$$

is dissipated in the *NMSiSiCSC*.

Before the avalanche behavior of the Si-SiC SuperCascode (*NMSiSiCSC*) is analyzed, the single components, i.e. the Si low-voltage MOSFET, the SiC JFET and the Si balancing diodes are characterized in Table 3.3 and Table 3.4 concerning their avalanche and power dissipation behavior. Low-voltage MOSFETs are frequently used in automotive applications and therefore most devices are avalanche rated. In contrast less is known

and/or published about the avalanche capability of SiC JFET. In [89] single pulse and repetitive avalanche tests were performed successfully with the Si-SiC cascode and high avalanche ruggedness in cascode operation was confirmed. Static avalanche behavior tests of a single SiC JFET showed that the avalanche breakdown of a SiC pn-junction is characterized by a positive temperature coefficient.

Semiconductor type	$E_{AS}, [mJ]$	$E_{AR}, [mJ]$	Test condition
Si low-voltage MOSFET (*IRLR024N*)	68	4.5	[91]
Si-SiC cascode	350	0.285	[89]

Table 3.3: Admissible avalanche energies E_{AS} and E_{AR} of the Si MOSFET and the Si-SiC cascode.

The balancing diodes implemented in the *NMSiSiCSC* are regular Zener diodes with high power dissipation capability. These diodes are operated in the controlled or clamped avalanche mode, respectively. This avalanche mode is not comparable with an unclamped avalanche condition which occurs in above mentioned applications.

The maximum operating voltage of the *NMSiSiCSC* is determined by the balancing diodes and is approximately 6.05 kV. Regarding only the series connected SiC JFETs the maximum blocking voltage is 7.2 kV and therefore higher than the resulting avalanche voltage of the balancing diodes. In case of avalanche condition, at first the whole avalanche energy is dissipated in the balancing diodes. Due to the voltage margin of the SiC JFETs of about 1.2 kV the SiC devices are not affected by the avalanche. Therefore, to guarantee operation under avalanche condition requires avalanche rated balancing diodes. According to the sim-

Semiconductor type	$P_{diss}, [W]$	$P_{ZSM}, [W]$	Test condition
balancing diodes (*BZG03C270(200)*)	3	60	[92]

Table 3.4: Power dissipation of the used Si Zener diodes.

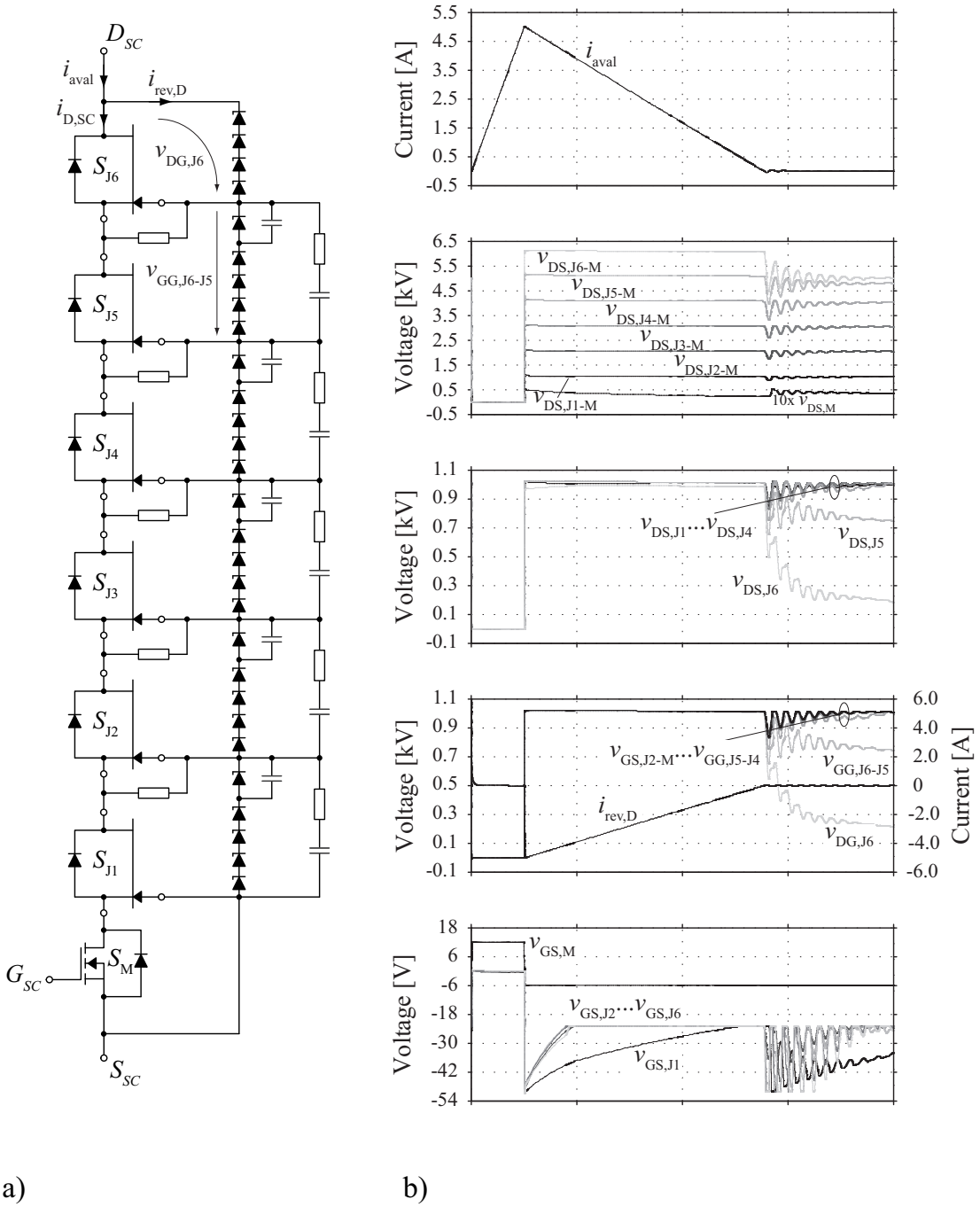

Figure 3.34: Avalanche simulation results for the *NMSiSiCSC*: (a) Device under test (Si-SiC SuperCascode) and (b) simulated and evaluated waveforms under avalanche condition.

plified SPICE simulation results, the whole avalanche current is flowing in reverse direction through the balancing diodes and thus each diode experiences high power losses. In addition, the simulation results of the gate-source voltages show strong ringing at the end of the avalanche interval. Also the gate-source diodes of all the SiC JFETs are driven into avalanche what could lead to thermal or overvoltage breakdown. However, as mentioned above the simulation results are not perfectly accurate due to missing models of the avalanche behavior. The *NMSiSiCSC* implemented as presented in Figure 3.23 is not avalanche rated and would fail under avalanche condition. Replacing the balancing diodes with avalanche rated diodes would help, however the critical part of the *NMSiSiCSC* - the junction capacitances - have to be considered.

In summary the avalanche behavior of the *NMSiSiCSC* should be analyzed in more detail in the course of future research.

Chapter 4

Bidirectional 25 kW/50 kHz DC-DC Converter

The investigations on the *NMSiSiCSC* (cf. Chapter 3) have shown fast and proper transient behavior at high operating voltages. To verify the switching behavior, the continuous operating mode and the applicability of the novel developed Si-SiC SuperCascode in typical application areas as introduced in Chapter 1, a bidirectional galvanically isolated dc-dc converter is selected (Figure 4.1).

This chapter describes the design of the exemplary chosen dc-dc converter topology. Therefore, the defined specifications as well as the converter topology are discussed before the characteristic voltage and current waveforms, based on the phase-shift modulation scheme, are analyzed. The calculation of the voltage and current stresses of the active and passive components are made in a wide range analytically. For this reason different assumptions have been made to simplify the calculations, which however are not impairing the accuracy. Out of the voltage and current stresses the power losses of the active and passive components have been calculated. Out of this, an efficiency estimation of the converter based on *NMSiSiCSC* is performed. Finally, the galvanically isolated gate drive circuits including the auxiliary power supplies are discussed. To complete

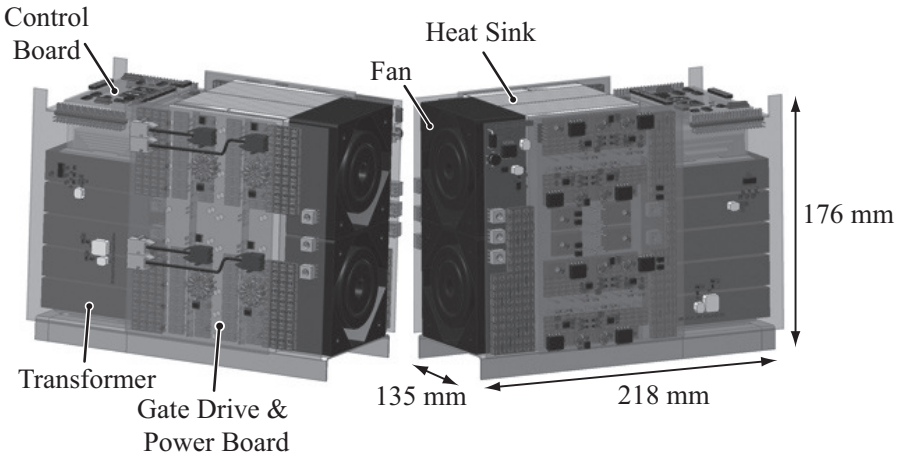

Figure 4.1: 3D-model of the DAB dc-dc converter.

the hardware design a suitable heat sink with a low thermal resistance is designed.

4.1 Topology and Specifications

The topology and the schematic of the selected dc-dc converter is presented in Figure 4.2 with the specifications given in Table 4.1. The high voltage side dc-link voltage of V_1 is determined as a result of the Si-SiC SuperCascode investigations and the number of cascaded SiC JFETs. Hence, the full bridge on the HV side is realized with four Si-SiC SuperCascodes. Due to the limited current rating of the used SiC JFETs of I_D=5 A, the nominal power of the dc-dc converter is defined to P_n=25 kW.

One goal of future BTB systems and power electronics converter design is reduction in terms of size, especially of the passive components. A high switching frequency will result in smaller magnetic components, i.e. a smaller transformer but the HF losses increase considerably. For that reason a switching frequency of 50 kHz is specified to limit HF losses. On the low voltage (LV) side a three-level topology has been chosen so that fast 600 V IGBTs, which are appropriate for operating at 50 kHz and higher power levels, can be used. With the defined voltage of V_2=700 V, the operating voltage of the three-level inverter is 350 V, which allows the usage of 600 V devices.

dc-link voltage HV side V_1	5 kV
dc-link voltage LV side V_2	700 V
nominal power P_n	25 kW
switching frequency f_s	50 kHz
transformer turns ratio $n:1$	79:11
phase-shift modulation DC / ZVS	50%
semiconductor HV side	*NMSiSiCSC*
topology of HV side / LV side	2-level / 3-level full bridge

Table 4.1: Specification of the DAB dc-dc converter.

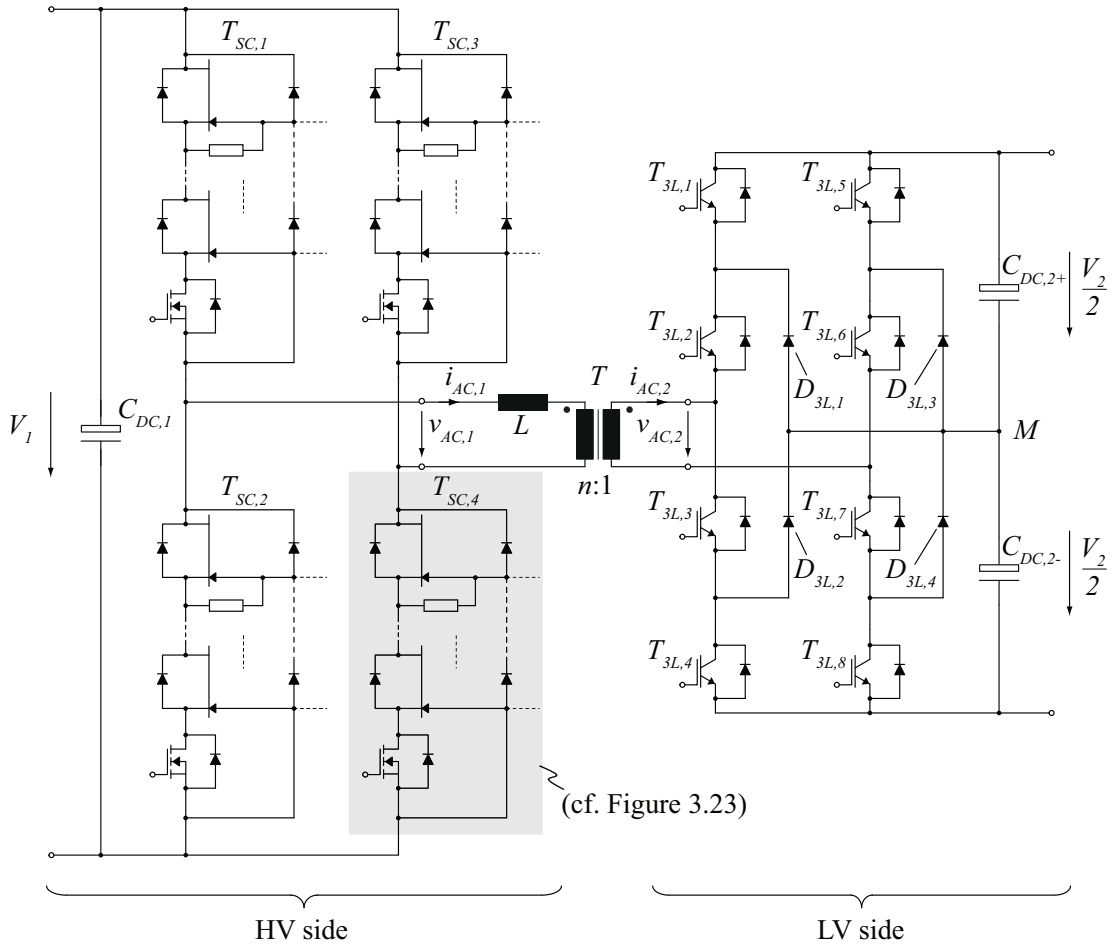

Figure 4.2: Schematic of the realized (cf. Chapter 5) bidirectional dc-dc converter based on the *NMSiSiCSC*.

4.2 Operating Principle

The bidirectional galvanically isolated dc-dc converter topologies and their various modulation methods are already well analyzed and evaluated in different international publications as [93], [94], [95], [96] and [97].

In [98], an extensive comparative evaluation of bidirectional dc-dc converter topologies has been performed and a detailed analysis of various modulation methods and of the realization of those power electronic systems have been investigated. Because of the existing excellent evaluation of DAB converters, herein the focus will be on the phase-shift modulation with 50 % duty cycle (DC), also known as rectangular mode. Based on this modulation method the operating principle of the proposed dc-dc converter is discussed in the following section.

4.2.1 Phase-Shift Modulation

As modulation method the common phase-shift operation is chosen for the DAB converter. The low computational complexity, the simplicity of the circuit and the reduced power losses due to zero voltage switching (ZVS) are the main reasons for the wide application of this method.

The phase-shift modulation operates with a constant switching frequency f_s and with maximal duty cycle of DC=50 %. The semiconductors at the HV side full bridge are commutated to apply a positive voltage, $v_{AC,1}$=+V_1, during the first half period and a negative voltage, $v_{AC,1}$=−V_1, during the second half period to the high frequency transformer T and/or leakage inductance L. Resulting is a rectangular primary inductor/transformer voltage as shown in Figure 4.4. The LV side semiconductors generate in the same way a rectangular voltage, $v_{AC,2}$=+/-V_2 on the LV side of the transformer. Assuming ideal active and passive components, constant dc-link voltages V_1 and V_2 and refering all LV side quantities to the HV side a simplified lossless model, as depicted in Fig-

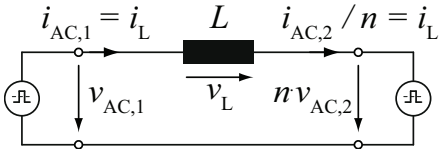

Figure 4.3: Ideal lossless model of the DAB.

ure 4.3, is resulting. The derived lossless model of the DAB is used for simplifying the calculation of the DAB converter and builds the basis of further analysis of the phase-shift modulation.

Depending on the switching states of the HV side semiconductors ($T_{SC,1} \cdots T_{SC,4}$) and the LV side switches ($T_{3L,1} \cdots T_{3L,8}$), the voltage across the leakage inductance v_L is resulting to

$$v_L(t) = v_{AC,1}(t) - n \cdot v_{AC,2}(t). \tag{4.1}$$

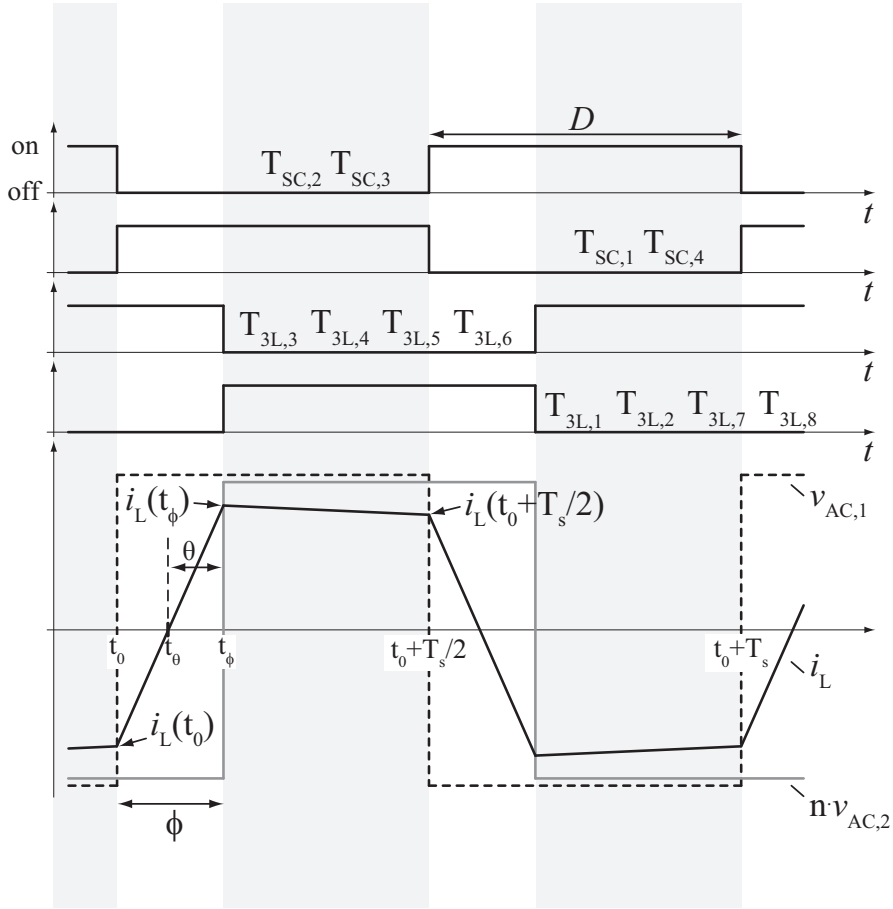

Figure 4.4: Switching states and characteristic waveforms for the phase-shift modulation of the proposed DAB converter cf. Figure 4.2 (ϕ indicates the phase-shift between the transformer voltages, which determines the transferred power of the bidirectional converter).

As a consequence of the applied inductor voltage v_L, the inductor current i_L is generated according to

$$i_L(t) = i_L(t_0) + \frac{1}{L} \int_{t_0}^{t_0+T_S} v_L(t)\, dt. \tag{4.2}$$

The instantaneous power $p_1(t)$, generated by the time varying voltage sources $v_{AC,1}(t)$ and $v_{AC,2}(t)$[1], considered over one switching cycle lead to an average power of

$$P_1 = \frac{1}{T_S} \int_{t_0}^{t_0+T_S} p_1(t)\, dt = \frac{2}{T_S} \int_{t_0}^{t_0+\frac{T_S}{2}} v_{AC,1}(t) \cdot i_L(t)\, dt. \tag{4.3}$$

Relating to the lossless model of the DAB converter, the average power of both sides are the same and can be expressed with

$$P_1 = P_2 = \frac{2V_1}{T_S} \int_{t_0}^{t_0+\frac{T_S}{2}} i_L(t)\, dt. \tag{4.4}$$

The evaluation of the inductor current i_L over half a switching cycle leads to an analytical expression for the average power P_1. Figure 4.4 shows the inductor/transformer current i_L in steady state operation. To determine the current i_L, the time interval $t \in [t_0 \cdots t_\phi]$ starting with an initial current of $i_L(t_0)$ and the time interval $t \in [t_\phi \cdots t_0 + \mathrm{T_S}/2]$ are analyzed. Resulting is the following expression for the inductor current i_L, whereas a positive phase shift angle ϕ is assumed

$$i_L(t) = \begin{cases} i_L(t_0) + \frac{V_1+n\cdot V_2}{L} \cdot t & t_0 \le t < t_\phi, \\ i_L(t_\phi) + \frac{V_1-n\cdot V_2}{L} \cdot (t-t_\phi) & t_\phi \le t < t_0 + \frac{T_S}{2}. \end{cases} \tag{4.5}$$

The inductor current i_L is a purely ac current (i.e. the dc component

[1] The average values of $v_{AC,1}$ and $v_{AC,2}$ and therefore of v_L, evaluated over one switching period in steady state operation, are zero in order to avoid saturation of the HF transformer.

is zero) to avoid the saturation of the HF transformer. The average value of i_L over one switching cycle is zero and therefore the current shows the following half cycle symmetry $-i_L(t_0)=i_L(t_0+\mathrm{T_S}/2)$. Out of this, the characteristic current values of the phase-shift modulation ($\phi > 0$) are calculated to

$$i_L(t_0) = \frac{\pi \cdot (nV_2 - V_1) - 2\phi nV_2}{4\pi f_s L}, \tag{4.6}$$

$$i_L(t_\phi) = \frac{\pi \cdot (nV_2 - V_1) + 2\phi V_1}{4\pi f_s L}. \tag{4.7}$$

In case a negative phase shift angle ϕ is considered, similar results for the transformer current $i_L(t)$ are achieved. With equations, Eq. (4.4) to Eq. (4.7), the transferred power of the bidirectional dc-dc converter results over the full phase-shift range to

$$P = P_1 = P_2 = \frac{V_1 \cdot nV_2 \cdot \phi \cdot (\pi - |\phi|)}{2\pi^2 f_s L} \quad \forall \quad -\pi \leq \phi \leq \pi. \tag{4.8}$$

A positive power $P > 0$ implies, that the power is transferred from HV side to the LV side and a negative power $P < 0$ denotes, a power transfer in the opposite direction from LV to HV side as shown in Figure 4.5. The amount of transferred power is controlled by the phase-shift angle ϕ and the leakage inductance L which is used as energy storing element. The transferred power depends nonlinearly on the phase-shift angle and is limited by the switching frequency f_s and the leakage inductance L. The minimal phase-shift angle and with this the minimal controllable power step is given by the clock frequency of the control board. Depending on the nonlinear relation of power and phase-shift angle, the highest gradient is with a phase-shift angle of zero degree. There the maximal power step and/or the minimal controllable power will appear at this point. With an increased phase-shift angle, the power step will decrease and the controllable power will be smaller. In [94] the active and reactive power are shown as a function of the phase-shift angle. A high phase-shift angle will increase significantly the reactive part of the power and only slightly the active power. Consequently, the efficiency of the converter is reduced. With a small phase-shift angle, the control signal constrains the

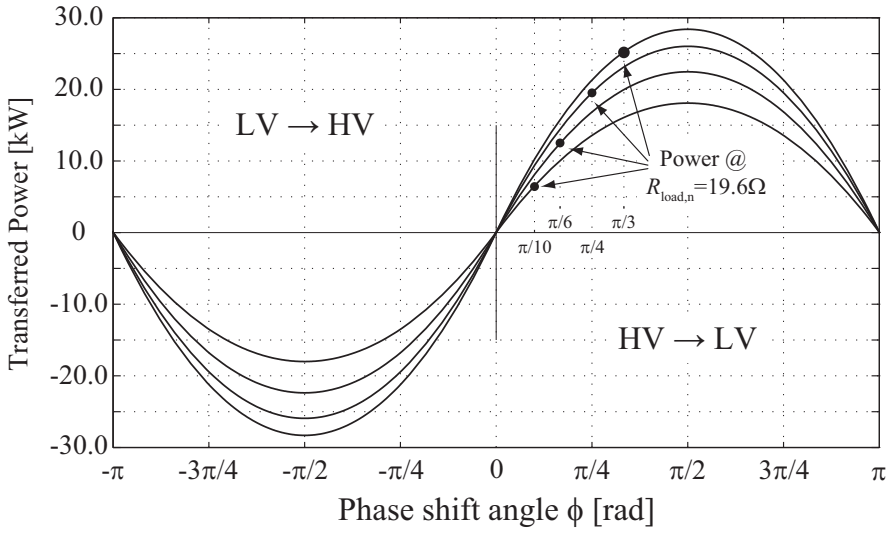

Figure 4.5: Transferred power of the DAB converter depending on the phase-shift angle. The maximal power transfer at nominal load of $R_{load,n}$=19.6 Ω is highlighted with a black circle for different phase-shift angles.

controllability of the power steps. Therefore, an operation in the phase-shift interval of $[\pi/4 \ldots \pi/3]$ is favorable and chosen for the considered DAB converter. The nominal phase-shift angle

$$\phi_n = \frac{\pi}{3} \tag{4.9}$$

is chosen to transfer the nominal power P_n.

The experimental testing of the DAB prototype was mainly controlled and performed by the HV side control and the implemented *NMSiSiCSC*. Based on Eq. (4.8) the transferred power from the HV side to LV side at nominal load of $R_{load,n}$=19.6 Ω can be calculated and is illustrated in Figure 4.6. Due to the laboratory power supply current capability of 2 A and the nonlinear characteristic of the transferred power, the experimental testing and operation of the DAB prototype at nominal phase-shift angle was limited. Thus, the maximal applicable voltage to the HV side (HV *NMSiSiCSC*) was determined by the laboratory power supply. To apply an increased dc-link voltage to the HV side the phase-shift angle has to be decreased to lower values. As earlier mentioned this results in an increased reactive power generation and a decreased active power transfer. Figure 4.7 illustrates the resulting LV side voltage V_2 at the

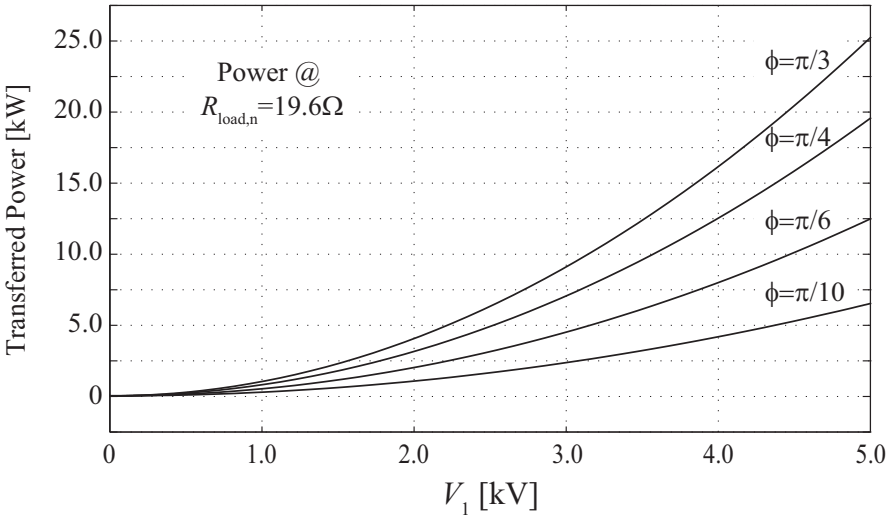

Figure 4.6: Transferred power at nominal load with different phase-shift angles $\phi \in \{\ \pi/3, \pi/4, \pi/6, \pi/10\ \}$. Depending on the applied HV side dc-link voltage level the power of the DAB prototype can be controlled.

nominal load and for V_1=5 kV and V_1=2.5 kV depending on the phase-shift angle. At a small phase-shift angle almost no voltage is applied at the LV side and this results in an high HV side to LV side voltage ratio which is also shown in Figure 4.7. Compared to the transformer turns ratio n:1, the voltage turns ratio at nominal load is much larger at small phase-shift angles,

$$\frac{V_1}{v_2} >> n, \tag{4.10}$$

which strongly influences the transformer/semiconductor current waveforms (cf. Figure 4.8 (a) and Figure 4.9 (a)). At the nominal phase-shift angle of $\phi = \pi/3$, the transformer turns ratio and the voltage ratio are almost equal which results in almost a constant current during the time period of $[t_\phi \ldots t_0 + T_s/2]$ (cf. Figure 4.4) for the positive cycle; of course the same applies for the negative cycle. To achieve the same current waveforms for different phase-shift angles and therefore mainly active power transfer the load condition must be adjusted so that the ratios (transformer and voltage) are approximately equal.

In the following, the DAB converter power losses of the active (Section 4.3) and passive components (Section 4.4) are investigated at nom-

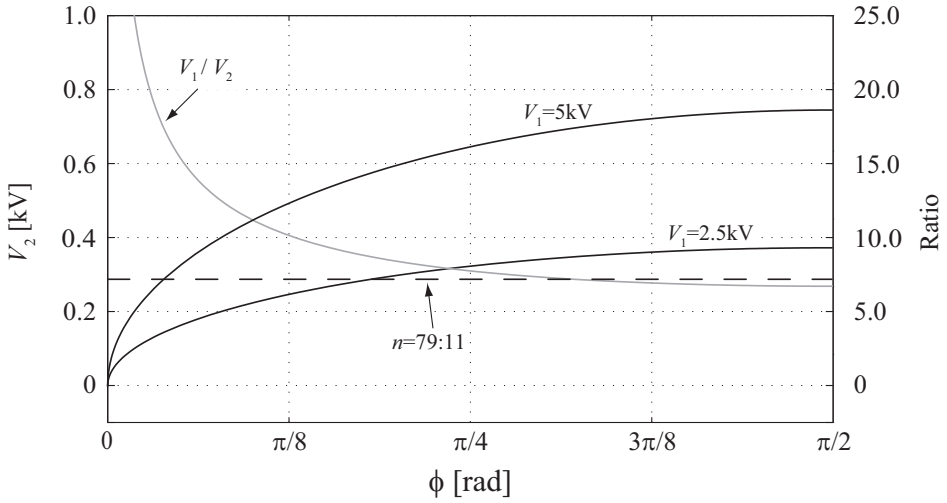

Figure 4.7: LV side and HV side voltage relation depending on the phase-shift angle under nominal load condition of $R_{load,n}$=19.6 Ω. Fixed transformer and varying voltage ratio under nominal load condition versus phase-shift angle.

inal load condition and for the nominal phase-shift angle.

4.3 Semiconductor Selection

As earlier considered, the demonstrator model is mainly built to verify and investigate the proper operation of the HV Si-SiC SuperCascode in a common power converter application. Therefore, the full bridge on the HV side is built with the *NMSiSiCSC*. On the LV side, the semiconductors have to be determined based on minimal power losses and suitable thermal behavior during continuous operation. As a consequence of the given converter specifications (cf. Table 4.1), especially the power level and the operating switching frequency, the available semiconductors are already limited to the 600 V fast switching semiconductor family.

The evaluation of the power losses of the HV and LV side semiconductors is depending on the root mean square (RMS) and average (AVG) current values as well as on the applied blocking voltages. The current and voltage stress on the semiconductors are therefore derived in the following.

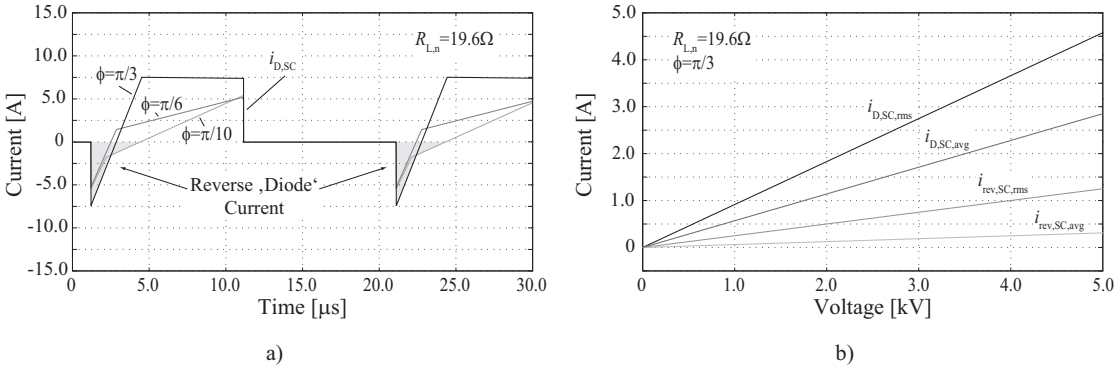

Figure 4.8: Power transfer from HV to LV side: (a) Different current profiles on the HV side switches depending on the phase-shift angle ($v_{AC,1}$>0 V is applied and therefore $T_{SC,1}$ and $T_{SC,4}$ are conducting). (b) RMS and average currents on the HV side at nominal load and nominal phase-shift angle subject to the HV side dc-link voltage.

4.3.1 Current and Voltage Stresses

The phase-shift modulation of the DAB converter determines the transformer current on the HV side as well as on the LV side as shown in Figure 4.4. Out of this, the RMS and AVG currents of the HV side switches and of the LV side switches can be calculated. The maximal voltage stress on the HV and on the LV side components is determined by the converter specification.

HV side - *NMSiSiCSC*

According to the dc-dc DAB topology, the specified dc-link voltage of the HV side determines the blocking voltage rating in continuous operation of the switches to 5 kV. In steady state operation the current is flowing through $T_{SC,1}$ and $T_{SC,4}$ during the first half cycle and through $T_{SC,2}$ and $T_{SC,3}$ during the second half cycle (cf. Figure 4.2 and Figure 4.4). While a positive voltage $v_{AC,1}$=+5 kV is applied during the first half cycle and the current i_L>0 A is positive as illustrated in Figure 4.8 (a), the current flows trough the switches and the RMS and AVG value can

be calculated as

$$I_{D,SC,rms} = \sqrt{\frac{1}{T_s}\int_{t_\theta}^{t_0+\mathrm{Ts}/2} i_L^2(t)\ dt} \quad \text{and} \tag{4.11}$$

$$I_{D,SC,avg} = \frac{1}{T_s}\int_{t_\theta}^{t_0+\mathrm{Ts}/2} i_L(t)\ dt, \tag{4.12}$$

whereas t_θ denotes the zero crossing of the inductor current i_L. At a negative current i_L<0 A and a positive voltage $v_{AC,1}$>0 V the current flows in reverse direction from source to drain. As earlier was mentioned, the reverse current can be conducted through the antiparallel MOSFET diode but also through the MOSFET channel. Moreover, the reverse current is conducted in any case, determined by the *NMSiSiCSC* topology, through the cascaded SiC JFET channels. Therefore, the reverse 'diode' current is derived as

$$I_{rev,SC,rms} = \sqrt{\frac{1}{T_s}\int_{t_0}^{t_\theta} i_L^2(t)\ dt} \quad \text{and} \tag{4.13}$$

$$I_{rev,SC,avg} = \frac{1}{T_s}\int_{t_0}^{t_\theta} i_L(t)\ dt. \tag{4.14}$$

With respect to Eq. (4.11) to Eq. (4.14) the current stress in the switch can be calculated depending on the HV side dc-link voltage as presented in Figure 4.8 (b).

LV side - Fast 600 V IGBT

On the LV side, the three-level topology is selected so that fast 600 V IGBTs, which are appropriate for operating at 50 kHz and higher power levels, can be used. With the specified LV side dc-link voltage of 700 V, the operating voltage is 350 V, what allows the usage of 600 V devices. The LV side RMS and AVG currents are equivalently calculated as the HV side currents considering the phase-shift angle and the transformer turns ratio. Therefore, the IGBT RMS and AVG currents are calculated

as

$$I_{IGBT,rms} = \sqrt{\frac{1}{T_s} \int_{t_0+\mathrm{Ts}/2(1+(\phi-\theta)/\pi)}^{t_0+\mathrm{Ts}/2(1+\phi/\pi)} (n \cdot i_L(t))^2 \, dt}, \tag{4.15}$$

$$I_{IGBT,avg} = \frac{1}{T_s} \int_{t_0+\mathrm{Ts}/2(1+(\phi-\theta)/\pi)}^{t_0+\mathrm{Ts}/2(1+\phi/\pi)} n \cdot i_L(t) \, dt, \tag{4.16}$$

and the RMS and AVG current of the reverse current which flows through the antiparallel diode can be derived with

$$I_{D,rms} = \sqrt{\frac{1}{T_s} \int_{t_\phi}^{t_0+\mathrm{Ts}/2(1+(\phi-\theta)/\pi)} (n \cdot i_L(t))^2 \, dt}, \tag{4.17}$$

$$I_{D,avg} = \frac{1}{T_s} \int_{t_\phi}^{t_0+\mathrm{Ts}/2(1+(\phi-\theta)/\pi)} n \cdot i_L(t) \, dt. \tag{4.18}$$

In Figure 4.9 (b) the RMS and AVG currents on the LV side are depicted depending on the HV side dc-link voltage. Obviously, the current mainly flows through the antiparallel diode if the power transfer is from HV to the LV side. With reverse power transfer, from LV to HV side, the main current stress occurs on the IGBT devices. To optimize the DAB converter operation regarding efficiency and power density suitable semiconductor devices for the LV side have to be selected. Therefore,

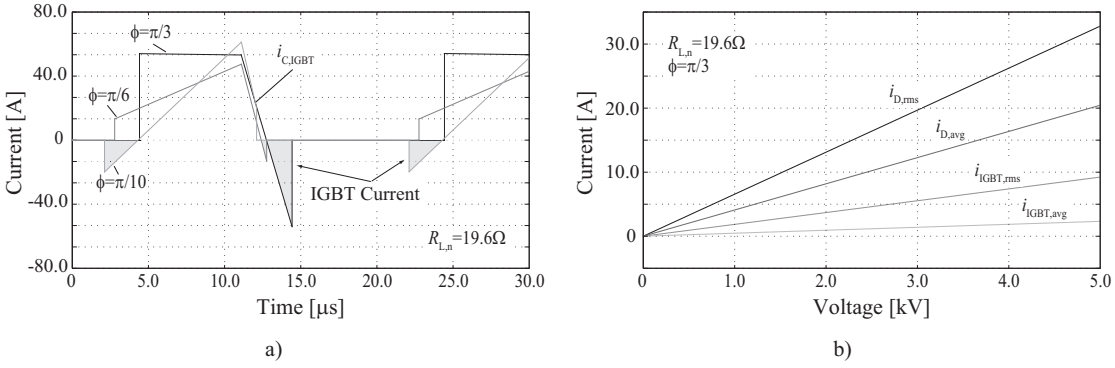

Figure 4.9: Power transfer from HV to LV side: (a) Different current profiles on the LV side switches depending on the phase-shift angle. (b) RMS and average currents on the LV side at nominal load and nominal phase-shift angle subject to the HV side dc-link voltage.

Component	Specification
Si PT IGBT $T_{3L,k}$	APT, APT40GP60B (Power MOS 7) TO-247, V_{CES}=600 V, I_C=62 A $V_{CE(on)}$=1.15 V, $R_{CE(on)}$=20.6 $m\Omega$
Antiparallel diode $T_{D3L,k}$ three-level diode $D_{3L,l}$	IXYS, DSEI120-06A (FRED) TO-247, V_{RRM}=600 V, I_{FAV}=77 A V_F=0.8 V, $R_{AK(on)}$=3.8 $m\Omega$

Table 4.2: Used LV side semiconductors ($T_{3L,k}$ and $T_{D3L,k}$, k $\in$ {1,...,8} and $D_{3L,l}$, l $\in$ {1,...,4}) and the corresponding main characteristics at a case temperature of T_C=100/125 °C.

mainly two approaches for IGBT solutions have been investigated: single package (IGBT and diode integrated into a single package) or discrete setup. The evaluation of these two approaches shows that although in the single package a suitable IGBT was available the performance was penalized by the diode characteristic while the power is transferred from HV to LV side. The single package and the discrete setup are comparable if the power transfer is from LV to HV side because the main current stress occurs in the IGBT and the IGBT device is the same. Consequently, the best approach for bidirectional operation is a discrete setup with an IGBT package and antiparallel connected the diode package. The main characteristics of the selected devices for the three-level inverter are summarized in Table 4.2.

4.3.2 Semiconductor Power Losses

The semiconductor power losses are distinguished into conduction and switching losses and herein further separated into HV side and LV side semiconductor losses. For calculating the incidental losses in the semiconductors the corresponding RMS and AVG currents through the semiconductors denoted by Eq. (4.11) to Eq. (4.18), as well as the specific semiconductor parameters in Table 3.1 and Table 4.2 are decisive.

HV side - *NMSiSiCSC*

The detailed power loss analysis of a single *NMSiSiCSC* switch is performed in Section 3.7. There, the *NMSiSiCSC* characteristic blocking losses are given in Eq. (3.30) which are neglected for the DAB semiconductor loss analysis. The total conduction losses are derived in Eq. (3.34) and finally the turn-on/off energy functions are determined in Eq. (3.37) and Eq. (3.36). According to the investigated switching losses of the *NMSiSiCSC*, the turn-off energy is the energy stored in the parasitic capacitors and therefore the turn-off losses as well as the turn-on losses are negligible ($P_{on/off,SC} \approx 0\,\mathrm{W}$) regarding the soft switching condition of ZVS. Out of this, the total DAB semiconductor losses on the HV side can be expressed as

$$P_{HVS,DAB} = 4 \cdot P_{c,SC}. \tag{4.19}$$

LV side - *APT40GP60B and DSEI120-06A*

For calculating the conduction losses on the LV side, the IGBT and antiparallel diode specific characteristics have been investigated. Based on experimental measurements on the final test bench, the data sheet values of the two semiconductors are verified. The extracted data sheet values are plotted in Figure 4.10. From Figure 4.10 (a) and (b) the on-state or forward voltages $V_{CE(on)}$ and V_F and the on-resistances $R_{CE(on)}$ and $R_{AK(on)}$ can be extracted. With respect to this data, the conduction losses of the IGBT devices can be calculated as

$$P_{c,IGBT} = V_{CE(on)} \cdot I_{IGBT,avg} + R_{CE(on)} \cdot I^2_{IGBT,rms}, \tag{4.20}$$

and the conduction losses of the antiparallel diodes can be derived as

$$P_{c,D} = V_F \cdot I_{D,avg} + R_{AK(on)} \cdot I^2_{D,rms}. \tag{4.21}$$

On the LV side, ZVS condition is hardly achieved and hence the IGBT devices are operated most of the time in hard switching condition. The turn-on and turn-off energy losses illustrated in Figure 4.10 (c) and (d) are approximated with a second order polynomial function depending on the switched collector-emitter current i_{CE}. Resulting are the turn-on/off

energy loss functions according to Eq. (4.22) and Eq. (4.23)

$$E_{on,IGBT}(T_j) = k_{2,I}(T_j) \cdot (\mathrm{I_{CE}}/10)^2 + k_{1,I}(T_j) \cdot \mathrm{I_{CE}}/10 + k_{0,I}(T_j), \quad (4.22)$$

$$E_{off,IGBT}(T_j) = k_{2,I}(T_j) \cdot (\mathrm{I_{CE}}/10)^2 + k_{1,I}(T_j) \cdot \mathrm{I_{CE}}/10 + k_{0,I}(T_j). \quad (4.23)$$

The corresponding calculated energy loss coefficients of the polynomials

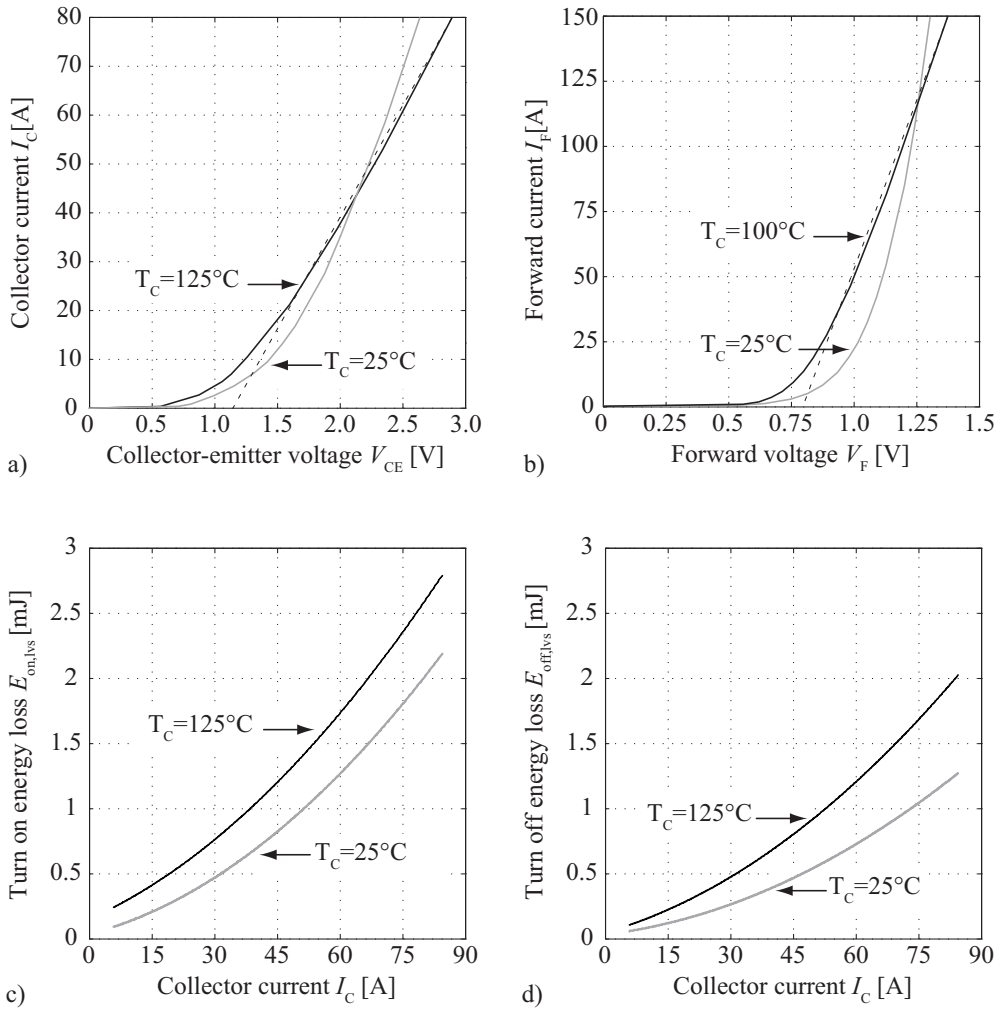

Figure 4.10: Extracted data sheet values of the discrete devices IGBT $APT40GP60B$ and diode $DSEI120-06A$ at case temperatures of T_C=25 °C and T_C=100/125 °C: (a) Forward characteristic of the IGBT and (b) of the antiparallel diode; Turn-on energy losses (c) and turn-off energy losses (d) at an applied voltage of 400 V, a gate-emitter voltage of 15 V and a gate resistance of 5 Ω.

on	$k_{2,I}, [mWsA^{-2}]$	$k_{1,I}, [mWsA^{-1}]$	$k_{0,I}, [mWs]$
$T_j = 25\,^{\circ}\mathrm{C}$	0.0255	0.0698	-0.0041
$T_j = 125\,^{\circ}\mathrm{C}$	0.0254	0.1363	0.08
off	$k_{2,I}, [mWsA^{-2}]$	$k_{1,I}, [mWsA^{-1}]$	$k_{0,I}, [mWs]$
$T_j = 25\,^{\circ}\mathrm{C}$	0.0161	0.0283	0.0152
$T_j = 125\,^{\circ}\mathrm{C}$	0.0213	0.0825	0.0029

Table 4.3: Switching power loss parameters for calculating the turn-on/off losses of the used IGBT $APT40GP60B$.

are listed in Table 3.3. On the basis of the energy loss functions, the IGBT on/off switching losses can be approximately determined and calculated as

$$P_{on,IGBT} = f_s \cdot E_{on,IGBT}(T_j) \cdot \frac{v_{CE,a}}{400\,\mathrm{V}}, \tag{4.24}$$

$$P_{off,IGBT} = f_s \cdot E_{off,IGBT}(T_j) \cdot \frac{v_{CE,a}}{400\,\mathrm{V}}. \tag{4.25}$$

With adding all the above defined power losses, the total LV side semiconductor losses can be calculated as

$$P_{LVS,DAB} = 8 \cdot (P_{c,IGBT} + P_{c,D} + P_{on,IGBT} + P_{off,IGBT}). \tag{4.26}$$

4.4 Passive Components Design

For the typical application of the DAB dc-dc converter a suitable design of the passive components like HF/HV transformer, leakage inductance and input and output capacitors is required. Based on the prototype specifications in Table 4.1 the design of the passive elements is performed for the worst case condition which occurs with a phase-shift angle of zero. In Section 4.4.1 the transformer design which integrates the required leakage inductance for proper operation of the DAB converter is investigated, before in Section 4.4.2 the input and output dc-link capacitors are analyzed and determined.

4.4.1 HF/HV Transformer

Beside the *NMSiSiCSC*, the 25 kW transformer operating at 50 kHz is an essential component of the DAB converter with respect to efficiency and power density. The voltage and current waveforms of the transformer (illustrated in Figure 4.4), which determine the design, are fixed by the phase-shift operation of the converter. There, as already mentioned a phase-shift angle of $\pi/3$ is chosen for transferring the power of 25 kW.

Core and HF Winding Losses

For sinusoidal voltage excitation of the transformer, the core losses can be calculated with the most popular formula known as Steinmetz equation, herein called the Standard Steinmetz Equation (SSE):

$$P_{core,SSE} \propto N_p \cdot V_e \cdot k \cdot f_s^{\alpha} \cdot \hat{B}^{\beta}, \tag{4.27}$$

where N_p is the number of parallel cores, f_s is the frequency of the voltage excitation, $\hat{B}$ is the peak flux amplitude and k, α and β are the Steinmetz

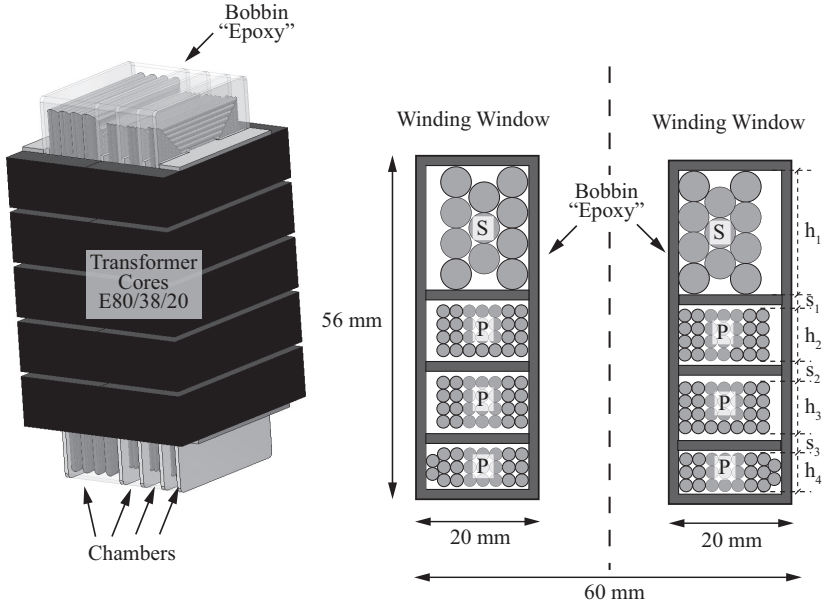

Figure 4.11: 3D-model of the 5 kV/50 kHz transformer designed with five parallel EE80/38/20 cores and the optimized winding arrangement integrating the required leakage inductance.

parameters found by curve fitting. However, the phase-shift operation of the DAB converter results in a non-sinusoidal magnetization of the core and therefore Eq. (4.27) and the corresponding parameters are not any more valid. This is investigated in various publications as e.g. [99] or [100].

Based on the resulting voltage waveforms and the non-sinusoidal core loss calculation approach, different core materials (ferrite, iron powder, nanocrystalline) have been compared with the loss model presented in [101], which is based on data sheet values. There, the lowest overall losses and a compact design resulted with five parallel EE80/38/20 cores made of N87 material (cf. Figure 4.11). With this design the flux density amplitude $\hat{B}$ at nominal power is 110 mT and the primary winding is realized with N_1=79 turns and N_2=11 turns, are employed for the secondary winding.

For the winding, litz wire is used in order to limit the losses due to skin- and proximity effect. For the switching frequency of 50 kHz the skin depth can be calculated with

$$\delta = \frac{1}{\sqrt{\pi \cdot f_s \cdot \mu_0 \cdot \mu_{r,Cu} \cdot \sigma_{Cu}}} \tag{4.28}$$

to δ=0.3 mm, whereas $\mu_0 = 4\pi \cdot 10^{-7}\,{}^{\mathrm{Vs}}/_{\mathrm{Am}}$ and $\mu_{r,Cu}$=1 are the permeability and the relative permeability of the conductor respectively and σ is the conductivity of the conductor. Using litz wire helps to minimize skin effect losses. However, as the specified operating frequency is 50 kHz eddy current and/or proximity effect losses become serious and can not be neglected. Therefore, the effective eddy current resistance R_{ec} needs to be considered to calculate the winding copper losses. According to [67], the net winding resistance can be expressed by

$$R_{ac} = F_R \cdot R_{dc} = \left(1 + \frac{R_{ec}}{R_{dc}}\right) \cdot R_{dc} \tag{4.29}$$

whereas F_R denotes the frequency dependent resistance factor. Depending on the number and diameter of the litz wire strands the dc resistance is calculated with

$$R_{dc} = \frac{4 \cdot N_{turns} \cdot l_w}{\sigma_{Cu} \cdot N_{strands} \cdot \pi \cdot d^2_{strand}}. \tag{4.30}$$

In [102] a method is presented for finding the optimal number of litz wire

	Turns	Strands	External diameter	Cross section
Primary	79	175	1.83 mm/0.1 mm	1.38 mm^2
Secondary	11	1260	5.12 mm/0.1 mm	9.90 mm^2

Table 4.4: Specification of the transformer windings made of litz wire.

strands to minimize the resistance factor. To calculate approximately the ac resistance of the transformer prototype in this thesis, a resistance factor of F_R=1.5 is assumed. The characteristic parameters of the used litz wires are summarized in Table 4.4. Out of this, the total winding copper losses on the primary and secondary side of the transformer windings can be calculated with

$$P_{copper} = R_{ac,p} \cdot I^2_{Tp,rms} + R_{ac,s} \cdot I^2_{Ts,rms}. \tag{4.31}$$

The arrangement of the windings as well as the insulation requirements is significantly influenced by the high operating voltage. In order to ensure large enough creepage distances, the bobbin it is advantageously manufactured as a single piece. There, POM (polyoxymethylene) material which has a dielectric strength of 40 kV/mm could be used, but the mechanical properties of this material impede a bobbin design with thin walls ($\approx$ 1 mm).

Therefore, Epoxy, which shows good mechanical and electric characteristics with several kV/mm dielectric strength, is utilized in the prototype. An alternative would be to use selective laser sintering (rapid prototyping), which also allows the manufacturing of a single piece bobbin.

Besides the bobbin also the litz wires have isolation strengh, since the isolation is made of three layers of mylar coating. This allows to omit a separate layer insulation. In order to reduce the voltage between successive layers and therefore the parasitic capacitance of the transformer, the high voltage winding is divided in three chambers. The turns in the chambers are wound in conventional manner (forth-back-forth etc.). The reduced layer voltage is also important for operation at high switching frequency and high $\mathrm{d}v/\mathrm{d}t$-values.

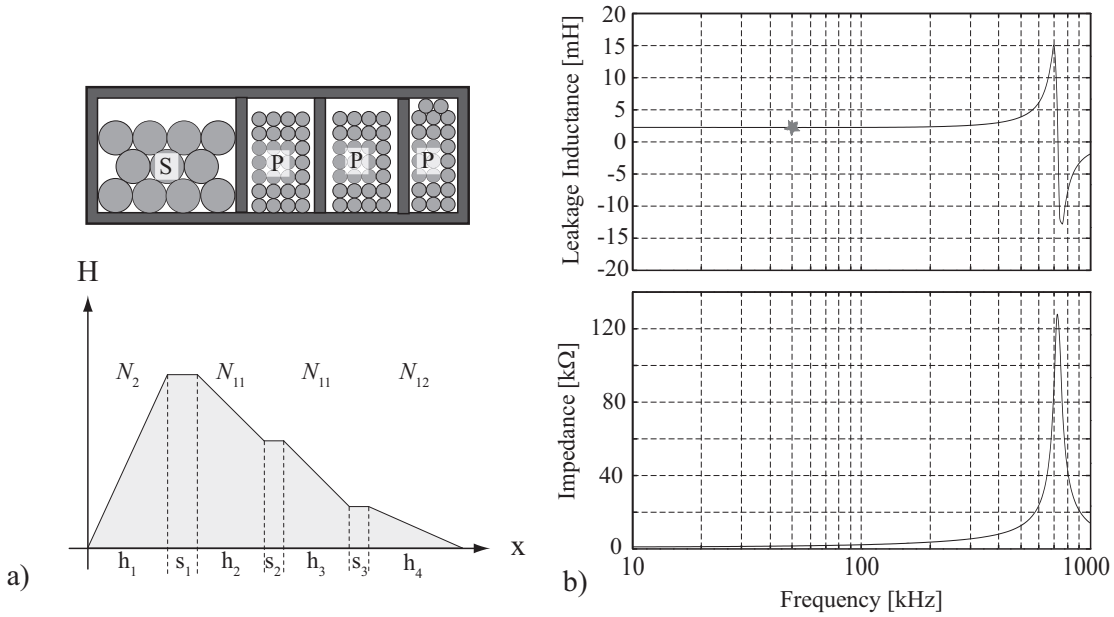

Figure 4.12: (a) Simplified distribution of the magnetic field between the primary and secondary winding for the approximative calculation of the leakage inductance L. (b) Measured HV/HF transformer leakage inductance of 2.07 mH at the nominal frequency of 50 kHz.

Series (Leakage) Inductance

For proper operation of the DAB converter the series inductance between the primary H-bridge and the secondary three-level H-bridge configuration must not be too small. In the considered converter design a series inductance of

$$L = 2.23\,\mathrm{mH} \tag{4.32}$$

(referred to the primary) is required at the nominal operating point, which is integrated as leakage inductance in the HV/HF transformer. Therefore, to better control and optimize the leakage inductance, primary and secondary winding are separated.

For the analytical estimation of the transformer leakage inductance, it is assumed that the H-field in the core is zero and that the field lines are orthogonal to the core ($\mu \to \infty$). With these assumptions a field distribution as shown in Figure 4.12 (a) results for balanced magnetomotive forces, i.e. $N_1 I_{1(rms)} = N_2 I_{2(rms)}$. The energy stored in the magnetic

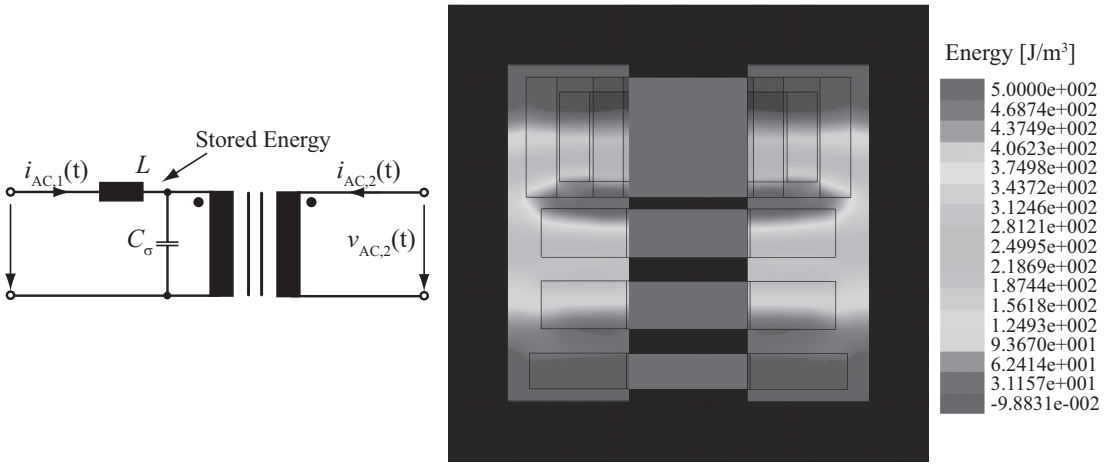

Figure 4.13: 3D-FEM simulation of the energy density in a cut view of one of the cores. There, balanced magnetomotive forces $N_1 I_{1(rms)} = N_2 I_{2(rms)}$ have been assumed, so that the magnetic field only represents the energy stored in the leakage inductance.

field is equal to the energy stored in the leakage inductance. The energy stored in the magnetic field can be calculated by

$$W_m = \int_V \frac{1}{2} BH \, dV = \frac{1}{2} L \hat{I}_1^2. \tag{4.33}$$

Evaluating the Eq. (4.33) for the magnetic field distribution of the prototype and equating this to the energy stored in the leakage inductance results in

$$\begin{aligned} L = \mu_0 \frac{l_w}{l} \Big(& \frac{2h_2 N_{11}^2 + h_4 N_{12}^2}{3} + \frac{h_1 I_{2(rms)}^2 N_2^2 + 3 I_{2(rms)}^2 N_2^2 s_1}{3 I_{1(rms)}^2} \\ & + \frac{(h_2 + s_2)}{I_{1(rms)}^2} \cdot \left((-2 I_{1(rms)} N_{11} + I_{2(rms)} N_2)^2 \right. \\ & \left. + (-I_{1(rms)} N_{11} + I_{2(rms)} N_2)^2 \right) \Big), \end{aligned} \tag{4.34}$$

whereas $h_2 = h_3$ and $s_2 = s_3$ is assumed and l_w denotes the average length of a winding turn and l is the length of the winding window.

Besides the analytical calculations of the leakage inductance also a 3D-FEM simulations with $MAXWELL^{TM}$ depicted in Figure 4.13 have

been performed, in order to investigate the filed distribution in detail. The FEM simulation converges towards a total stored energy of 45.574 mJ. Thereof, with Eq. (4.33) a simulated leakage inductance of

$$L_{sim} = 2.02\,\text{mH} \tag{4.35}$$

is resulting. This corresponds well with the analytical calculation resulting in $L_{calc} = 2.0\,\text{mH}$.

Table 4.5 summarizes the dimensions and specifications of the HV/HF transformer prototype at nominal operating conditions.

4.4.2 DC-Link Capacitors

In order to keep a high power density of the DAB prototype, the dc-link capacitor banks on the HV and LV side are realized with multilayer ceramic chip capacitors. The design of the capacitor bank values is based on the allowable voltage ripple of the dc-dc converter, whereas the load on the HV as well as on the LV side has to be considered. Further essential parameters for determining the capacitor values are the tolerable ripple current stress and the equivalent series resistance ESR which mainly influence each capacitor temperature rise and therefore the capacitors

Material		N87
Core		5 × E80/38/20
Dimensions		155mm x 80mm x 76mm
Turns ratio		79:11
Power		25 kW
Core losses	($100°C$)	11 W
HF losses	($100°C$)	48 W
Leakage inductance		2.07 mH
Specified max. flux density		110 mT
Effective core cross section		1950 mm^2
Effective core volume		359000 mm^3

Table 4.5: Parameters of the 5 kV, 50 kHz transformer at nominal operating point of 25 kW and phase-shift angle of $\pi/3$.

lifetime.

The losses of the dc-link capacitors are mainly due to the ESR which is depending on the dissipation factor $tan(\delta)$ provided by the capacitor manufacturer and on the spectral distribution of the capacitor current. The equivalent series resistance can be expressed for each frequency f_k as

$$ESR_k = \frac{tan(\delta_k)}{2\pi \cdot f_k \cdot C}. \tag{4.36}$$

Based on the spectral analysis of the capacitor current with a Fast Fourier Transformation (FFT) and an assumed constant dissipation factor $tan(\delta)$ of 0.05, the total capacitor losses can be approximately calculated with

$$P_{cap,ESR} = \frac{1}{2\pi \cdot C} \cdot tan(\delta) \sum_{k=1}^{\infty} \frac{I^2_{cap,(rms),k}}{f_k}. \tag{4.37}$$

For the HV and LV side ceramic capacitor banks, single ceramic capacitors 600 V/560 nF/X7R from Holystone are parallel and series connected to reach 1 μF on the HV side and 50 μF on the LV side.

4.5 Efficiency Estimation

The power loss analysis of the DAB dc-dc converter components is presented in Figure 4.14 with the efficiency curve versus the transferred power. The efficiency evaluation is given at room temperature and at a junction temperature of T_j=125 °C which result in about 1.2% difference in power losses. Due to the complexe topology of the *NMSiSiCSC*, with all the required passive networks, it is not trivial to estimated the exact operating condition of each cascaded SiC JFET. Especially, the on-resistance value of each SiC JFET and the acting parasitic capacitance is difficult to determine only with the theoretical approach. Therefore, the unrealistic operation at room temperature and a junction temperature of T_j=125 °C serve to illustrate the range in which the practical verified efficiency should be. The main power loss contribution is coming from the semiconductors on the HV and LV side whereas the transformer core and copper losses as well as the equivalent series resistance losses from the dc-link capacitors can be almost neglected.

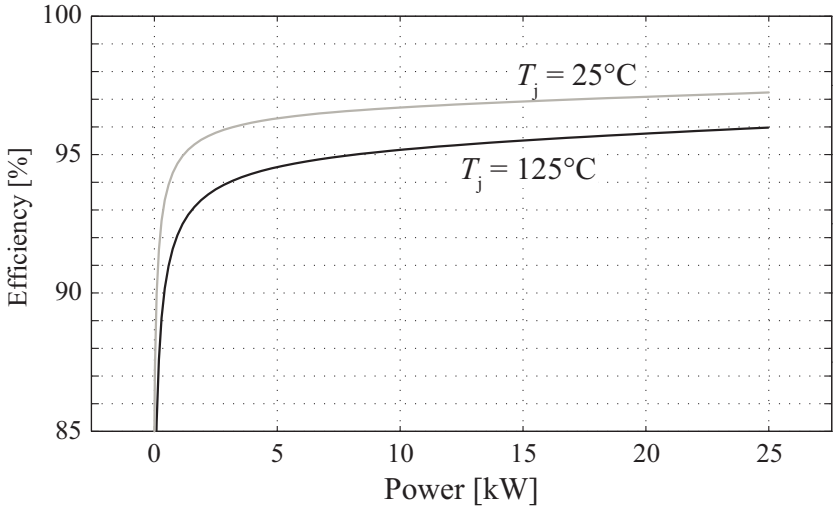

Figure 4.14: Total efficiency of the DAB dc-dc converter based on the *NM-SiSiCSC* in dependency of the transferred power from HV to LV side ($\phi = \pi/3$ and nominal load condition). The efficiency characteristic is depicted for a theoretical operation of the power semiconductors with a junction temperature equal to room temperature and a junction temperature of 125 °C.

4.6 Gate Control

For the implementation of the phase-shift modulation and generation of the corresponding gate signals on the HV and LV side of the DAB dc-dc converter, the PES dsp+ board (cf. Section 5.1) is used. Among others, the board contains a Digital Signal Processor (DSP) as well as a Field Programmable Gate Array (FPGA). The code which is used for the converter prototype investigated in this thesis was mainly developed in [98]. Therefore, the code had to be adapted to the slightly different DAB topology and to the different prototype specification parameters given in Table 4.1. With the DSP/FPGA the gate signals of the HV and LV side are generated, then distributed and wired via the PCB to the corresponding gate drive circuit. Due to the medium voltage application there are several requirements for the galvanically isolated gate drive circuit. On the one hand, the gate drive auxiliary power supply needs to be galvanically isolated and on the other hand isolation needs to be provided for the gate drive circuit and the gate signal path. Especially, each of the power switches with floating potential requires separate galvanic isolation because the potentials of the switches are depending on

the switching status. On the other hand the signal propagation delay and the switch on/off delay time must be marginal in order to guarantee proper modulation and operation of the prototype. The latter is mainly influenced by the layout of the gate drive circuit and the resulting para-

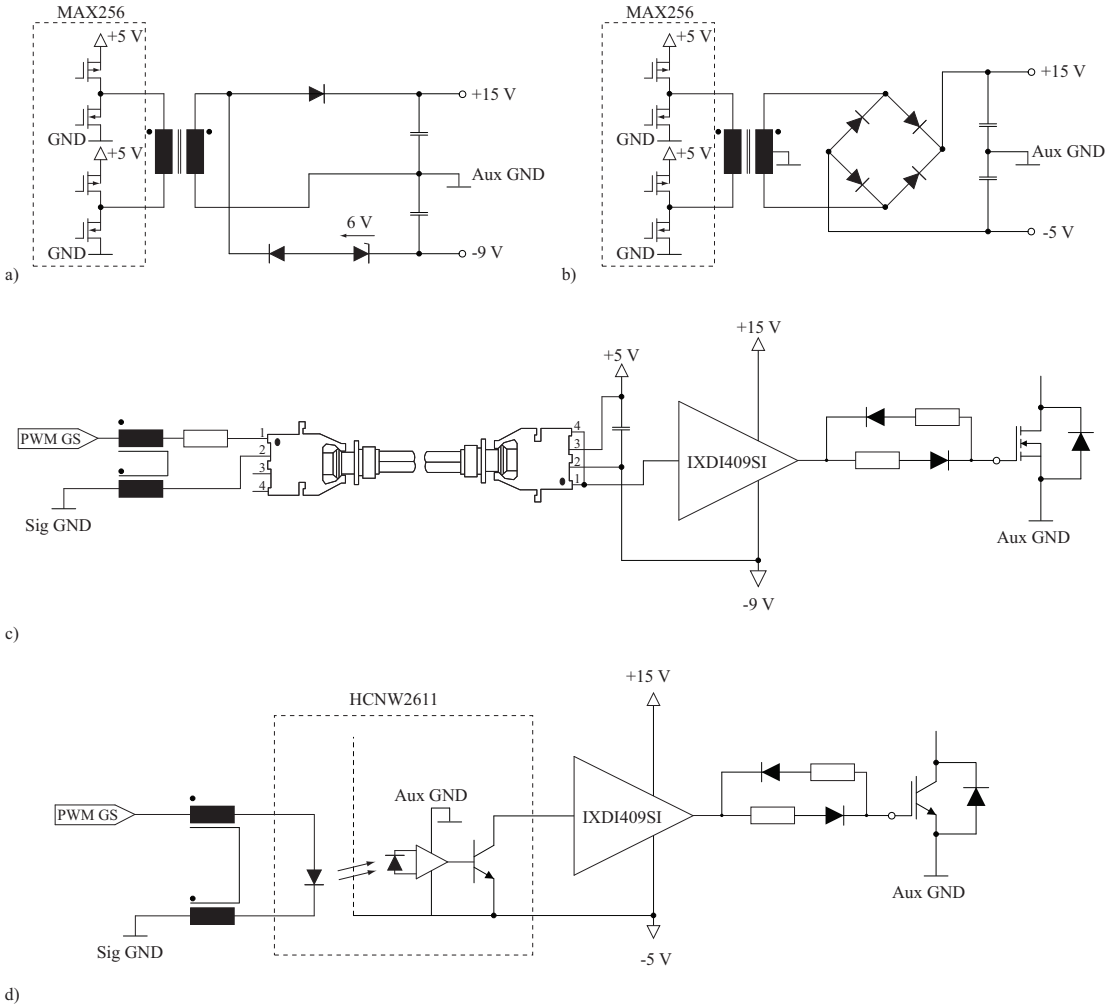

Figure 4.15: Basic schematics of the HV and LV side gate drive circuits and the corresponding auxiliary power supply: (a) The auxiliary power supply of the HV side is realized with a voltage doubler and a HF transformer which provides galvanic isolation and withstands the HV side dc-link voltage of 5 kV. (b) The LV side gate drive supply is implemented with a full diode rectifier bridge using a center tap transformer to generate the auxiliary supply voltages. An inverting 9 A gate driver (IXYS) is applied on the HV and LV side, whereas the gate signal isolation is realized with fiber optics (c) on the HV side and with an optocoupler $HCNW2611$ (d) on the LV side.

sitic inductances and can be minimized by proper design of the current paths on the PCB.

In Figure 4.15 the gate drive circuits used in the prototype converter of this thesis are depicted with basic schematics limited to the main components. The auxiliary gate drive supply of the HV side is presented in Figure 4.15 (a) whereas the corresponding gate drive circuit is illustrated in (c). According to the specified dc-link voltage on the HV side of 5 kV, the components which provide galvanic isolation have to withstand at least this voltage level. As for industrial medium voltage converter systems, the option to transfer the gate signals via optical fibers was selected. For the gate drive supply, a HF transformer provides galvanic isolation which has to withstand a fault voltage of several kV. Therefore, a toroidal core R 20/7 from Epcos and silicon isolated litz wire for the turns were selected. To minimize the stray flux of the transformer the primary and secondary windings are wound on top of each other. Out of this, a center tap transformer with unsymmetric output voltage of +15 V/-9 V is difficult to realize. Accordingly, a modified version of voltage doubler with an additional zener diode is used to achieve the desired turn-on/off voltage levels.

The LV side gate drive supply is presented in Figure 4.15 (b) and the gate drive circuit is shown in (d). The galvanic isolation of the supply is also provided by a HF transformer whereas this transformer has to withstand a dc-link voltage of 700 V. Due to the lower dc-link voltage on the LV side, instead of a fiber optic transmitter a compact optocoupler $HCNW2611$ guaranteeing an isolation voltage of 1.4 kV is used.

4.7 Heat Sink

The power density of the DAB dc-dc converter is influenced by the converter efficiency and the effectiveness of the cooling system to dissipate the power losses. The temperature distribution within the heat sink is depending on the thermal conductivity of the utilized material. Aluminum exhibits a heat conductivity of λ=237 $^{\mathrm{W}}/_{\mathrm{mK}}$, whereas copper features λ=401 $^{\mathrm{W}}/_{\mathrm{mK}}$. Therefore, the temperature distribution in case of a copper heat sink is more homogeneous than for aluminum. This ensures that all fins uniformly contribute dissipating heat and/or are used optimally. However, aluminum is significantly more favorable, as it shows

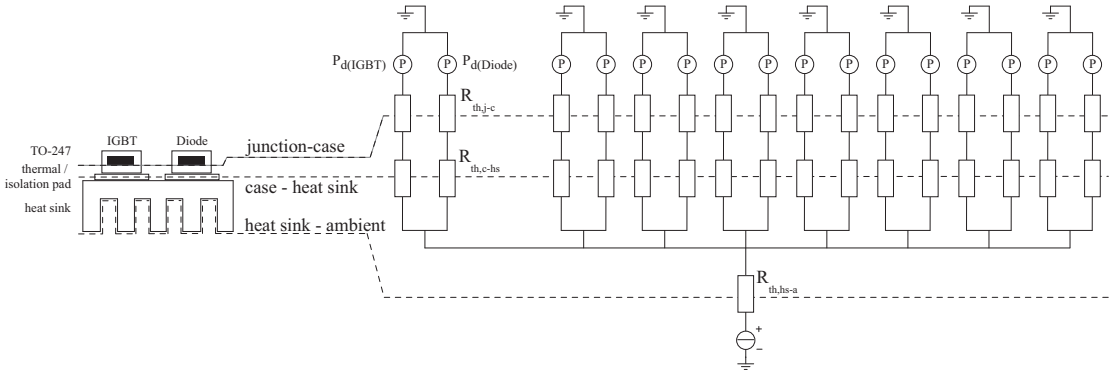

Figure 4.16: Thermal equivalent circuit related to the LV side semiconductors.

lower weight than copper and is much easier to manufacture. Out of this, a forced air cooled aluminum heat sink is employed.

Based on the power loss analysis of the HV and LV side semiconductors and the specified thermal resistances of the devices, the required thermal resistance $R_{th,hs-a}$ of the heat sink can be estimated regard-

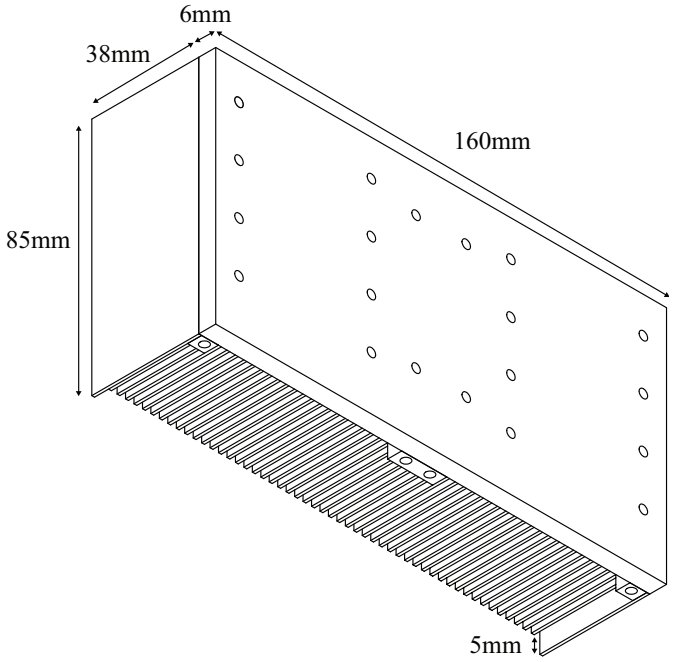

Figure 4.17: Dimensions of the sub-optimal heat sink used for the HV side and LV side. The holes visible on the heat sink surface are for the LV side semiconductors.

ing the thermal equivalent circuit presented in Figure 4.16. Assuming an ambient temperature of T_{amb}=40 ℃ and a junction temperature of T_j=125 ℃, the maximal allowable heat sink thermal resistance is resulting to $R_{th,hs-a}$=0.1 ℃/w[2].

In [103] a method has been investigated to design a sub-optimal heat sink that provides the minimum thermal resistance for a certain manufacturing procedure. Applying this method for the DAB prototype, a heat sink with a thermal resistance of 0.0968 ℃/w and overall dimensions of 160 mm length, 85 mm width and 44 mm height is resulting. The thickness of the fins is only 1 mm and the distance between the fins is 2 mm. To ensure uniform air pressure distribution a small air chamber in front of the fins is realized as shown in Figure 4.17. Additional to the heat sink calculation, thermal simulations with the software package *ICEPAK* have been performed to verify the calculated results and to optimize the arrangement of the semiconductors to avoid hot spots. For the forced air cooled setup in *ICEPAK* powerful fans ebm Papst 8212*JN* (80 mm x 80 mm x 38 mm) are used. The simulation results are in good agreement with the calculated results and show an even slightly better performance of the heat sink.

[2]For an isolation of each semiconductor case against the heat sink a high performance capton foil, with a thermal resistance of $R_{th,c-hs}$=0.1 ℃/w, is used.

Chapter 5

Prototype - DAB Converter

In order to verify the proper operation of the *NMSiSiCSC* under continuous mode operation, the efficiency calculations of the bidirectional dc-dc converter and the proper operation of the HV/HF transformer, a demonstrator of the proposed DAB converter (cf. Chapter 4) has been realized. The *NMSiSiCSC*, which features fast and high voltage switching allows to realize a compact prototype. Especially, the volume of the magnetic components i.e. the HV/HF transformer can be limited by HF operation. In summary, the DAB converter is built with an advanced power density of $4.65\,^{\mathrm{kW}}/_{\mathrm{litre}}$ [1] as shown in Figure 5.1.

The realization of the demonstrator prototype is discussed in the following Section 5.1. Subsequently, the experimental results of the bidirectional dc-dc converter are presented and analyzed in Section 5.2.

[1] **Note**: The prototype at this stage is not built with highest power density. The power density could be further increased if the *NMSiSiCSC* would be integrated onto a power module instead of a realization with discrete switches. Furthermore, if the packages would be able to handle elevated temperatures higher than $T_{j,pack}$=175 °C the volume of the heat sinks would decrease.

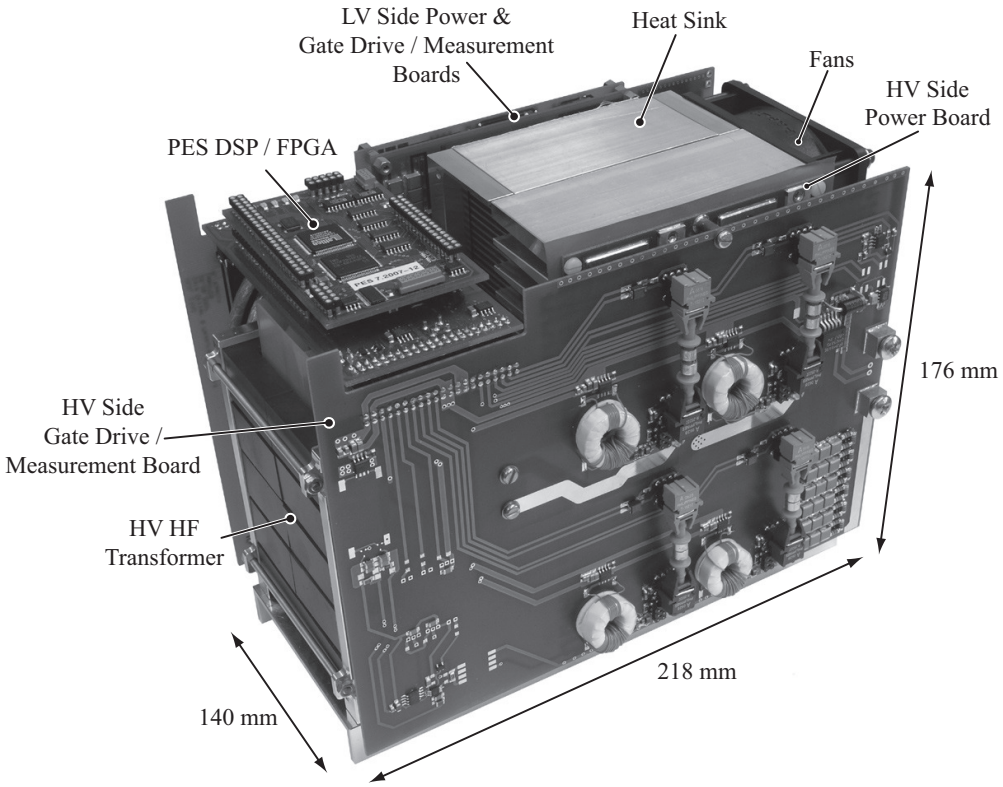

Figure 5.1: Photo of the realized laboratory prototype (P_n=25 kW, V_1=5 kV, V_2=700 V and f_s=50 kHz).

5.1 Hardware Realization

The description of the DAB prototype is with reference to the four main hardware parts, namely the HV side, the LV side, the HV/HF transformer and the digital DSP/FPGA controller part.

HV side

The HV side full bridge contains four *NMSiSiCSC* modules as shown in Figure 5.2. The single module, presented in Figure 5.3, consists of several active and passive elements, as are discussed extensively in the previous chapters. In Table 3.1 all *NMSiSiCSC* elements are listed and illustrated in Figure 3.23 with the final schematic. In order to guarantee the creepage distance between the discrete SiC JFETs, a spacer for the SiC JFETs

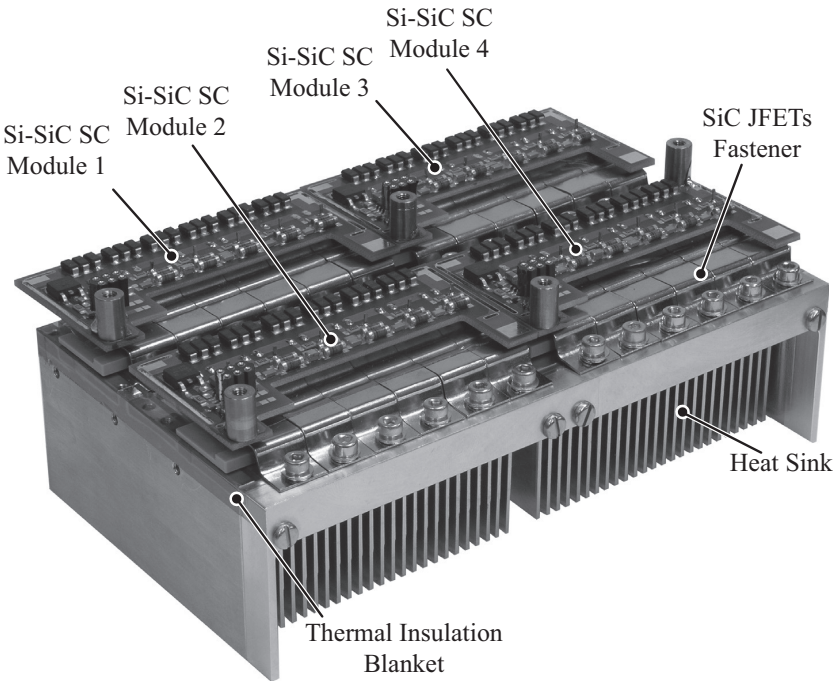

Figure 5.2: HV side full bridge with heat sink. The Si-SiC SuperCascode modules 1 to 4 consist of the following switch configurations (cf. Appendix A): module 1: $S_{J1} \ldots S_{J6} = \{20,21,22,23,24,25\}$, module 2: $S_{J1} \ldots S_{J6} = \{32,33,34,35,36,37\}$, module 3: $S_{J1} \ldots S_{J6} = \{14,15,16,17,18,19\}$, module 4: $S_{J1} \ldots S_{J6} = \{26,27,28,29,30,31\}$.

is manufactured from *PEEK*[2] material. Each module consists of an own gate driver directly mounted on the printed circuit board close to the low-voltage MOSFET. Furthermore, three connectors are placed on each module: the power connector, realized with a cooper pipe including a screw thread; the module connector and the connector for the gate signal and the galvanically isolated auxiliary supply of the gate driver.

Figure 5.2 shows the HV side full bridge containing the four *NM-SiSiCSC* modules mounted on the heat sink (cf. Section 4.7). In order to guarantee isolation between each single SiC JFET and the heat sink, a thermally conductive and electrically isolating foil covers the heat sink surface. The material of the thermal insulation foil has to provide high dielectric strength, i.e. has to sustain high temperatures of up to 140 °C

[2]**Polyetheretherketon (PEEK)**: dielectric strength (IEC 60243-1) 25 kV/mm, comparative tracking index (IEC 60112) 150, thermal conductivity (DIN 52 612) 0.25 W m/K, maximal temperature 240 °C, detailed specifications given in [104].

without changing dielectric strength capability. In addition, the thermal resistance should be as small as possible to provide optimal heat transfer. *Kapton*[3] is a material which features the required mechanical, electrical and thermal properties. All of the discrete SiC JFETs are pressed on the isolation foil and on the heat sink to ensure an optimal heat transfer. For each SiC JFETs a single fastener is provided to balance TO-220 package

[3]**Kapton (polyimide film)**: dielectric strength 100 kV/mm, temperature resistance -75 °C to +260 °C, leakage resistance $> 10^{12}\,\Omega$, detailed specifications given in [105].

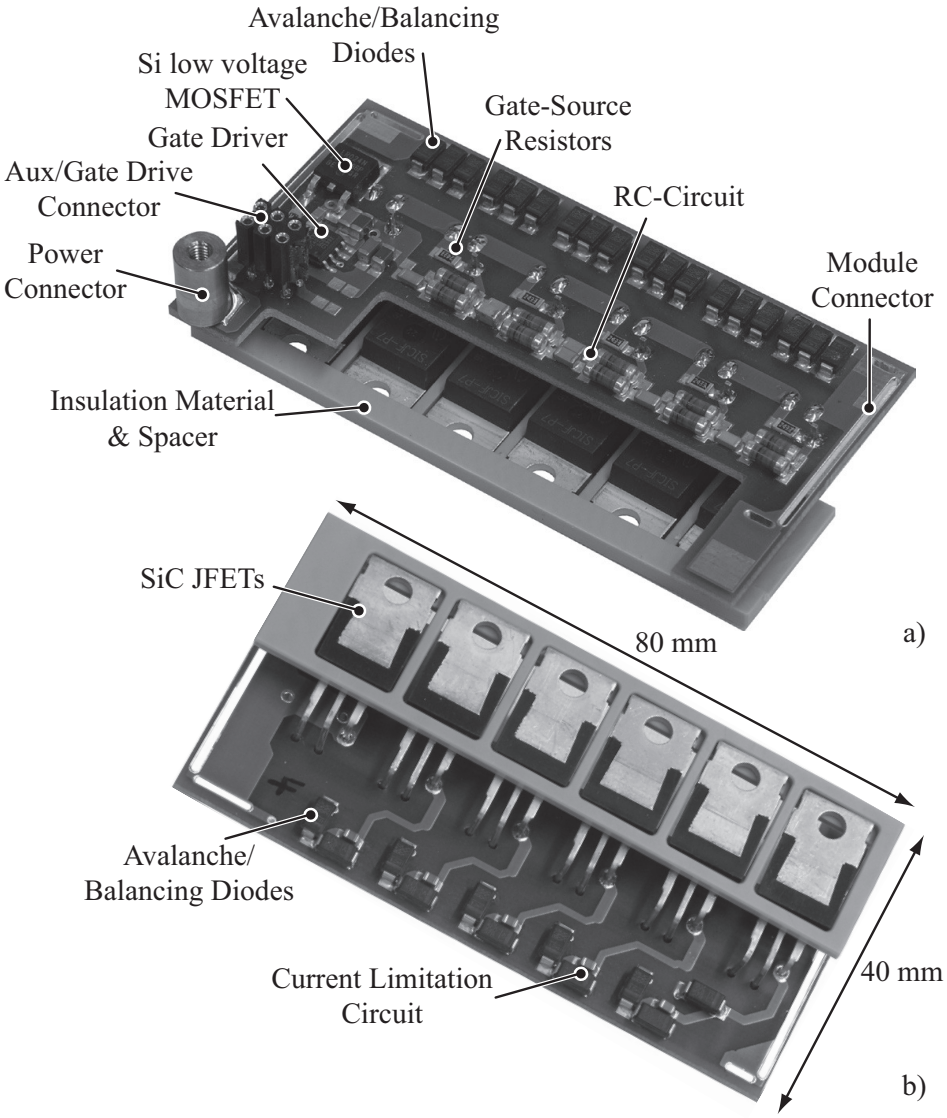

Figure 5.3: *NMSiSiCSC* module: (a) top side and (b) bottom side.

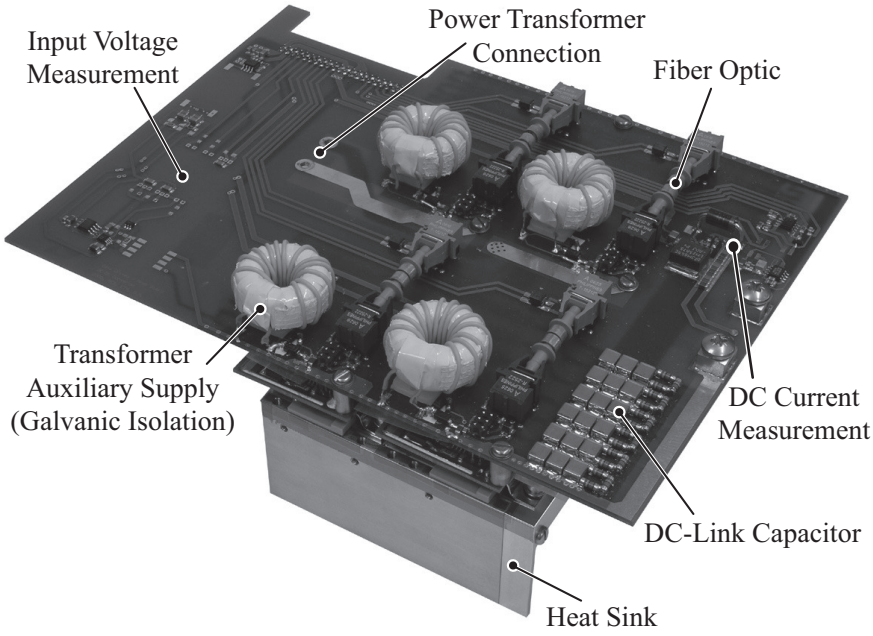

Figure 5.4: Complete hardware setup of the HV side with mounted gate drive and auxiliary power supply board.

height variations.

Directly on the top of the power board (*NMSiSiCSC* modules) the gate drive and measurement board is located as presented in Figure 5.4. Each gate drive circuit consists of a galvanically isolated auxiliary supply (relatively large auxiliary transformers are required to withstand the voltage of $> 5\,\mathrm{kV}$ in case of a failure) feeding the corresponding gate driver. The gate drive signals are generated by the digital signal processor (DSP) and FPGA and are transferred via optic fibers. Nevertheless, to achieve a compact layout, the fiber optic transmitters and receivers are mounted on the gate drive board close to each other but still with enough distance to provide sufficient isolation. Moreover, the dc-link capacitor is realized with several series and parallel connected ceramic capacitors, which are mounted on the top and bottom side of the gate drive/auxiliary supply board. Also located on this PCB are the input dc current and the input voltage measurement circuits.

LV side

The hardware realization of the LV side is similar to the HV side regarding heat sink, power board and gate drive/measurement board as shown in Figure 5.5. Due to the lower dc-link voltage of 700 V optocouplers are used for isolating the gate drive signals instead of using optic fibers. The auxiliary supply of all gate drivers is galvanically isolated. Comparable to the HV side, series and parallel connected ceramic capacitors build the dc-link capacitor. Furthermore, the dc output current and the dc-link output voltage measurement circuits of the three-level inverter are located on the gate drive/measurement board. The discrete IGBTs and diodes packages of the three-level inverter are pressed on an isolation foil and are mounted on the heat sink.

HV/HF transformer

The realized HV/HF transformer comprises five parallel EE80/38/20 cores which are pressed to each other by two aluminum plates as presented in Figure 5.6. Between the two plates and the cores, a thermally conductive foil is placed to improve the heat transfer from the cores to

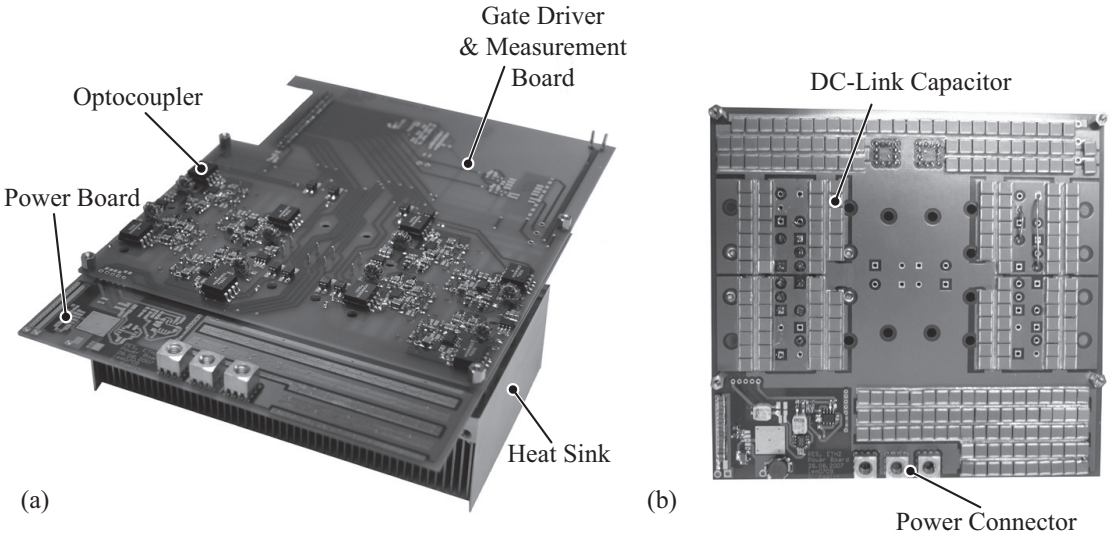

Figure 5.5: LV side hardware setup; (a) complete LV side with power and gate drive board mounted on the heat sink, (b) the power board with the ceramic dc-link capacitors.

the plates and the air. Additionally, air gaps between the cores facilitate the cooling of the transformer cores. For the primary and the secondary winding, litz wires are used. The bobbin of the transformer guarantees isolation between the windings and also between the windings and the cores. As bobbin material EPOXY was selected due to the excellent mechanical and electrical characteristics.

DSP/FPGA & Interface Board

The main task of the DSP/FPGA is to control the switches (to generate PWM-signals for HV and LV side), to regulate the transferred power and to protect the dc-dc converter against overcurrent or overvoltage. To control and evaluate the measurements from the HV and LV side only one DSP/FPGA board is used. Therefore, an interface board connecting HV and LV side is realized. The DSP/FPGA control board can easily be plugged on the interface board. The transformer ac current measurement is directly connected to the interface board and therefore to the FPGA which is able to act with very short delay in case of a failure. DSP/FPGA board and interface board are shown in Figure 5.7.

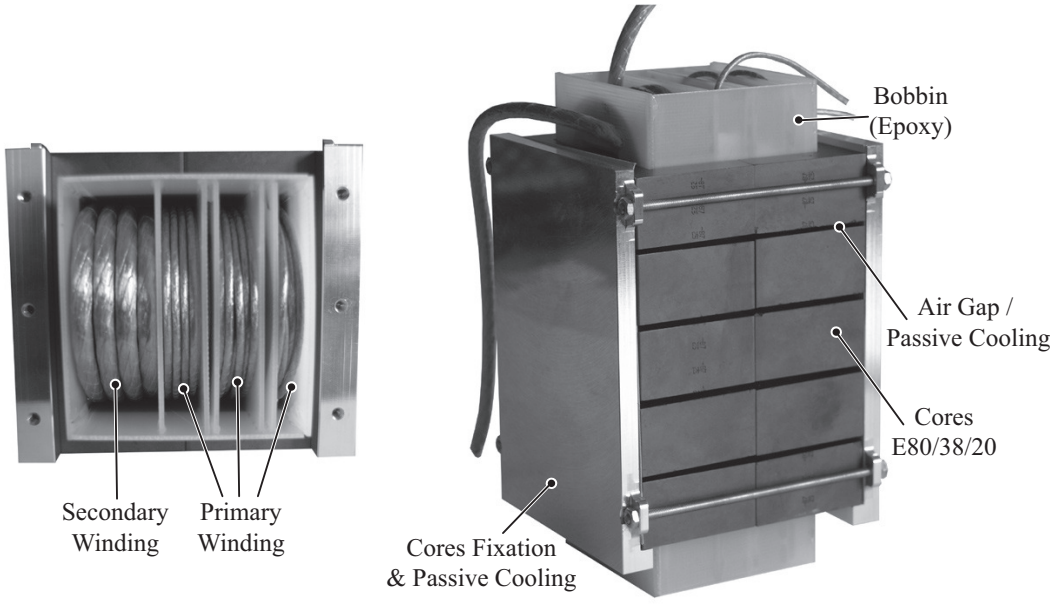

Figure 5.6: Hardware realization of the 25 kW 50 kHz 5 kV/700 V transformer.

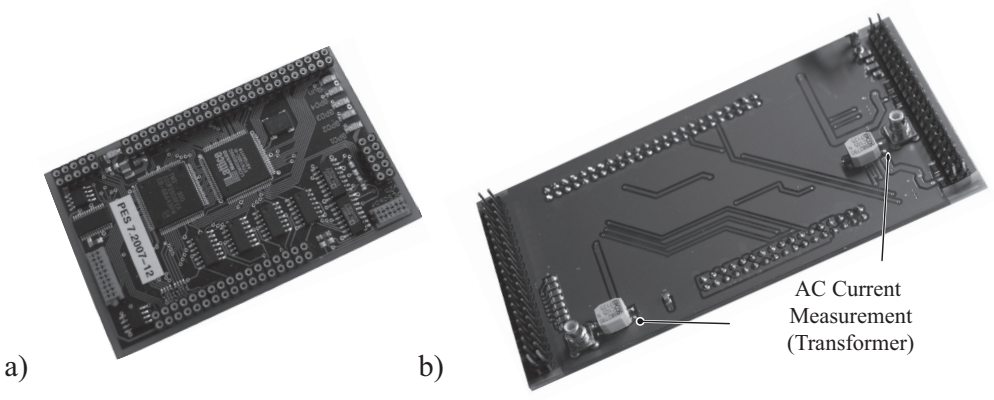

Figure 5.7: (a) DSP/FPGA control board PESdsp+ developed at the ETHZ PES laboratory to support rapid prototyping of digital converter control systems and (b) corresponding interface board connecting HV and LV side of the DAB prototype.

5.2 Experimental Results - Performance

This section covers the experimental verification of the DAB prototype discussed in the previous Section 5.1. There, the main focus is on the HV side, featuring the *NMSiSiCSC* in full bridge configuration. Additionally, the ZVS condition and the control of the power transfer via the phase-shift angle is carefully inspected. The measurements were performed in open loop configuration and the power transfer of the DAB converter was only tested from HV to LV side. All measurements of the dc-dc converter were with nominal (resistive) load on the LV side. The power was provided by a high voltage power supply (10 kV/2 A) at the HV side. Due to the power supply current limitation of 2 A, measurements at full load of 25 kW could not been performed. Therefore, the transformer design could not be tested concerning the thermal behavior and the electrical isolation at nominal power.

The following experimental results have been exclusively gained with the DAB prototype presented in Section 5.1. To avoid transformer saturation, additional series film capacitors were added on the HV side for all measurements. It has to be considered that the nomenclature used in the experimental results is based on the schematics given in Figure 3.23 and Figure 4.2.

ZVS condition at HV side

The *NMSiSiCSC*s at the HV side are operated under ZVS condition to minimize the turn-on energy loss as analyzed in Section 3.7.3 and for maximizing the DAB converter efficiency. In Figure 5.8 the Si low-voltage MOSFET gate-source voltage of the *NMSiSiCSC* $T_{SC,2}$ and the $v_{DS,J6-M}$ of $T_{SC,4}$ is depicted for continuous operation with a switching frequency of 50 kHz. The voltage waveforms illustrate fast and proper switching behavior at turn-on and turn-off transitions. The zoomed view at $t = 5\,\mu$s for a time interval of $1\,\mu$s on the right-hand side shows perfect ZVS without ringing of the drain-source voltage and/or oscillations in the gate-source voltage.

Transformer voltage and current waveforms

As mentioned earlier, the three-level inverter on the LV side is modulated and operated as a two-level full-bridge topology, i.e. the additional possible voltage levels are not considered in the modulation scheme. Therefore, the voltage of the transformer HV and LV side are equal in absolute value to the dc-link voltage of the HV and LV side. In Figure 5.9 the character-

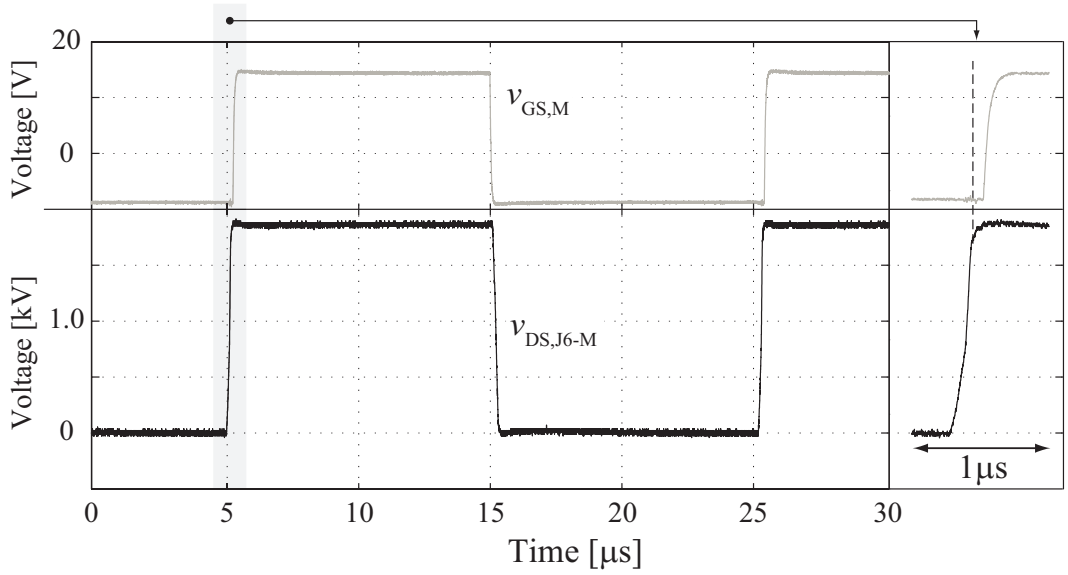

Figure 5.8: Measured Si low-voltage MOSFET gate-source voltage $v_{GS,M}$ (-9 V/+15 V) of $T_{SC,4}$ and *NMSiSiCSC* drain-source voltage $v_{DS,J6-M}$ ($T_{SC,2}$) at a dc-link voltage of V_1=1.83 kV and switching frequency of 50 kHz.

istic waveforms of the DAB converter, namely the transformer voltages and currents, are presented. Thereby, it can be observed that the HV to LV side dc-link voltage ratio is almost equal to the transformer turns ratio. This leads to only slightly changing transformer currents $i_{AC,1}$ and $i_{AC,2}$ in intervals where the dc-link voltages are applied with the same polarity at the HV and LV side to the transformer and/or $v_{ac,1} \approx n \cdot v_{ac,2}$ is given. Regarding the LV side transformer voltage $v_{ac,2}$ it is visible when the current is flowing through the antiparallel diode and when it is flowing through the IGBT. Due to the larger forward voltage drop of the IGBT, less voltage is applied to the transformer for $v_{ac,2} < 0$ / $i_{AC,2} > 0$ and $v_{ac,2} > 0$ / $i_{AC,2} < 0$. This effect cannot be observed at the HV side transformer voltage because the current is flowing in forward and reverse direction through the cascaded SiC JFET channels.

Voltage distribution of the *NMSiSiCSC* during continuous operation

The most challenging issue of the *NMSiSiCSC* is to achieve symmetric voltage distribution across all cascaded semiconductor devices in tran-

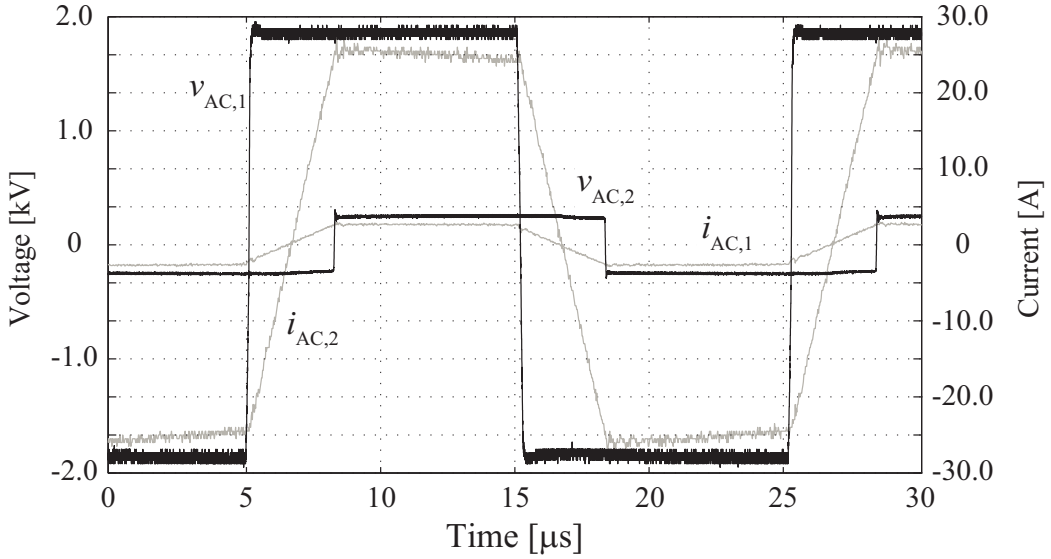

Figure 5.9: Measured voltage ($v_{ac,1}$=±1.83 kV,$v_{ac,2}$=±251 V) and current waveforms ($i_{AC,1}$,$i_{AC,2}$) of the transformer for phase shift modulation $\phi=\frac{\pi}{3}$ and a switching frequency of f_s=50 kHz. At this operating point the transferred power is 3.4 kW at a measured efficiency of 93.8 %.

sient condition. In Figure 5.10 voltages $v_{ds,J1}$ and $v_{ds,SC}$ are measured at different phase-shift angles i.e. ϕ=π/3 and ϕ=π/4. It can be clearly observed that the SiC JFETs are not taking over the blocking voltage sequentially, which means that SiC JFET J_1 would take the whole avalanche voltage of 1.0 kV before a voltage is applied to the upper SiC JFETs. In contrast, the voltage appears simultaneously across all cascaded switches. Therefore, $v_{ds,J1}$ is increasing with increasing $v_{ds,SC}$ which is equal to the HV side dc-link voltage. Due to a rated blocking voltage of the *NMSiSiCSC* of 6 kV, the voltage across the first SiC JFET will reach the nominal operating voltage of 1.0 kV close to the nomial HV side voltage of 5 kV.

Phase-Shift Angle of ϕ=π/4

In Figure 5.11 the experimental results show the transformer voltages and currents at phase-shift modulation with ϕ=π/4. The transferred power amounts to 4.6 kW and results in a measured DAB converter efficiency of 94.7 %. Due to the reduced phase-shift angle a higher reactive power

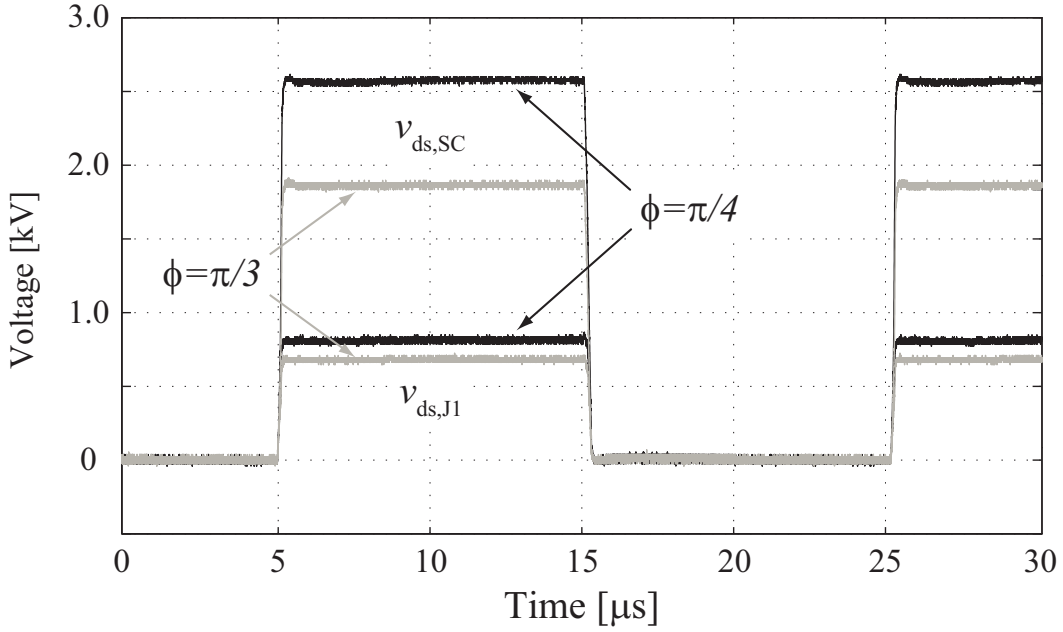

Figure 5.10: Measured *NMSiSiCSC* voltages $v_{ds,J1}$ and $v_{ds,SC}$ under continuous operation, at a switching frequency of f_s=50 kHz and at phase-shift angles of ϕ=π/3 and ϕ=π/4.

and/or higher circulating currents are generated and less active power is transferred to the load compared to the operation with nominal phase-shift angle and same HV side dc-link voltage. Comparing the measurements presented in Figure 5.9 with the experimental results depicted in Figure 5.11, change in the current is clearly visible also for intervals where the transformer voltages $v_{ac,1}$ and $v_{ac,2}$ show equal signs. The reason of the current variation over time is that the dc-link voltage ratio is unequal to the transformer turns ratio at this operating point.

DAB Prototype Performance

In order to verify the efficiency calculated in Section 4.5, the efficiency of the laboratory prototype has been measured. It has to be noted here, that efficiency measurement of the DAB converter based on *NMSiSiCSC* is challenging as it requires suitable HV power analyzer with high accuracy and well calibrated voltage meters and shunt resistors. Furthermore, the operation status of the *NMSiSiCSC* is strong depending on the temperature and electromagnetic interference induced by ultra fast switching of the power semiconductors could disturb the electrical power measure-

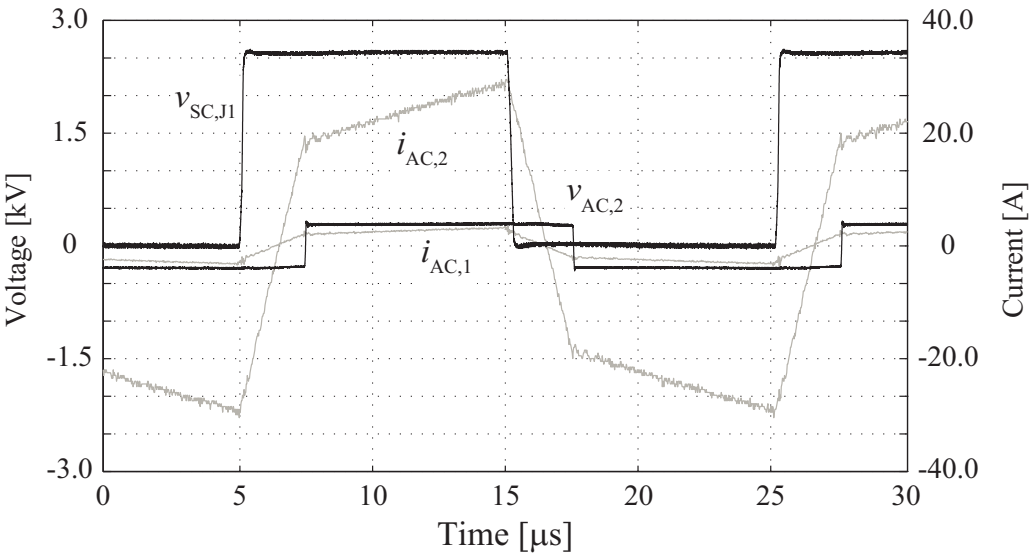

Figure 5.11: Measured voltage ($v_{ac,1}$=±2.52 kV,$v_{ac,2}$=±292 V) and current waveforms ($i_{AC,1}$,$i_{AC,2}$) of the transformer for phase shift modulation $\phi=\frac{\pi}{4}$ and a switching frequency of f_s=50 kHz. At this operating point the transferred power is 4.6 kW at a measured efficiency of 94.7 %.

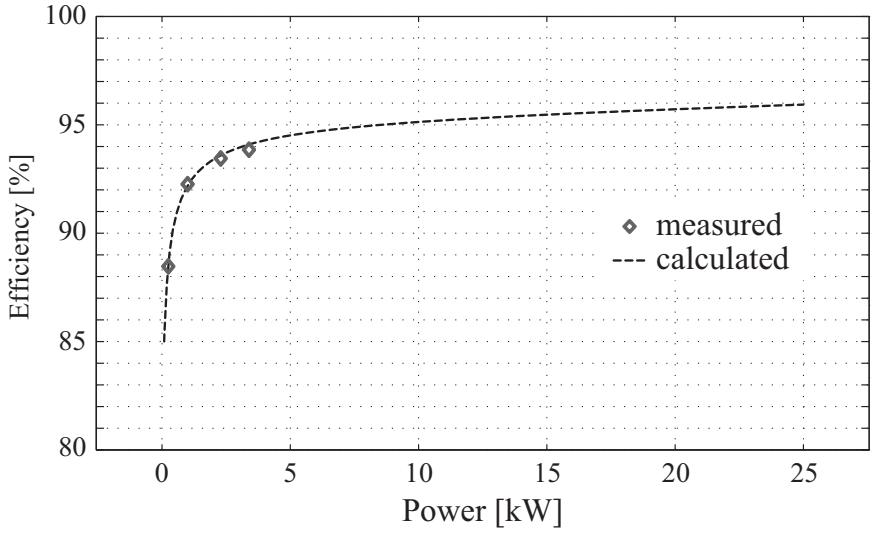

Figure 5.12: Efficiency of the DAB converter prototype as a function of the transferred power. The converter has been operated at f_s=50 kHz, nominal load and with a phase-shift angle of ϕ=π/3.

ment. Out of this, a calorimetric determination of the DAB converter power losses as presented in [106] would be advantageous and ensure high accuracy.

The measured efficiency of the DAB converter based on the *NM-SiSiCSC* as a function of the transferred power is shown in Figure 5.12. As can be observed the calculated efficiency characteristic fits very well with the measured experimental results at the given operating conditions. Out of this, the efficiency of the investigated DAB prototype could be estimated as 96 % at nominal operation, i.e. at a power level of 25 kW.

Chapter 6

Summary and Outlook

6.1 Summary

The current thesis mainly contributes an ultra fast, HV cascaded switch topology based on wide band gap semiconductors (*NMSiSiCSC*) which could help to solve future smart grid power electronics challenges, as e.g. the introduction and integration of dc grids and solid state transformers. The novel developed cascaded SiC JFET switch structure is based on the series connection of a low-voltage MOSFET and series connected SiC JFETs. For proper operation of the proposed basic switch at a high voltage level and high operating frequency, additional passive circuits are of paramount importance and are proposed, analyzed and designed. Furthermore, to the author's knowledge no cascaded topologies of SiC JFETs have been reported consisting of six series connected SiC JFETs achieving a blocking voltage of 6 kV and switching speeds in the range of $120\,^{\mathrm{kV}}/_{\mu s}$. These results have been achieved with individual research results summarized in the following.

In **Chapter 1** the motivation and need of HV fast switching devices in next-generation BTB systems is discussed. Therefore, a state-of-the-art analysis of Si and SiC technology semiconductors is performed. The findings illustrate, that there is no state-of-the-art semiconductor available which combines HV ($3\,\mathrm{kV} < V_{(BR),DSS}$) and fast switching ($25\,\mathrm{kHz} < f_s$) operation. Therefore, the upcoming wide band gap semiconductors e.g.

SiC offer excellent physical and electrical characteristic for HV and fast switching operation. Due to the lack of discrete SiC switches with a blocking voltage $> 3\,\mathrm{kV}$, the investigations in this thesis were focused on cascading SiC JFETs mainly analyzed in Chapter 2 and Chapter 3.

In **Chapter 2** the basic operation principle of the Si-SiC cascode which comprises a low-voltage MOSFET and a series connected SiC JFET is analyzed and discussed. This cascode topology builds the basis of the main investigation on the Si-SiC SuperCascode in this thesis. Furthermore, the cascode structure changes the normally-on characteristic of the HV SiC JFET into a favorable normally-off characteristic of the cascode. In order to evaluate the predicted fast switching behavior of SiC JFETs a test setup is built to experimentally analyze turn on/off switching transients. Besides the experimental investigations of the Si-SiC cascode also a SPICE simulation model of the SiC JFET is introduced. By comparing simulated and measured transient waveforms a good accordance is established. The experimental transient analysis shows that the switching speed reaches values up to $45\,^{\mathrm{kV}}/_{\mu\,\mathrm{s}}$ which could lead to electromagnetic interference effects. To avoid those disturbances the $\mathrm{d}v/\mathrm{d}t$ is preferably decreased for specified power electronics applications. It turns out, that conventional $\mathrm{d}v/\mathrm{d}t$ control methods cannot be applied to the cascode topology. So, novel $\mathrm{d}v/\mathrm{d}t$ techniques especially specified for the Si-SiC cascode are proposed. The new methods are analytically derived and verified with experimental measurements.

Based on the investigations of the Si-SiC cascode, the stacked switch, also called Si-SiC SuperCascode, which is consisting of a low-voltage Si MOSFET and several cascaded SiC JFETs is investigated in **Chapter 3**. First of all, the states of the Si-SiC SuperCascode are distinguished into static on, static off and dynamic behavior to explain the basic operation principle. To gain a deeper insight into the internal potentials of the cascaded switch, the SPICE model introduced for the Si-SiC cascode is extended to the Si-SiC SuperCascode. With various experimental measurements on different test setups and numerous simulation runs with different component parameters, the basic Si-SiC SuperCascode invented in 2004 is further developed into a novel modified Si-SiC SuperCascode (*NMSiSiCSC*). The novel developed Si-SiC SuperCascode includes two novel passive auxiliary circuits whereas one is for tuning and controlling the switching speed and the other is to avoid current limitation of the switch. Those passive circuits are required to guarantee proper op-

eration under HV and nominal/high load current operation. The investigations are verified experimentally and also with SPICE simulations. In the course of an extensive evaluation of the novel Si-SiC SuperCascode measurements for inductive and resistive load at nominal current of 5 A are successfully performed. Subsequently, the power losses of the *NMSiSiCSC* are analyzed and separated into static blocking losses, conduction losses and switching losses. Finally, the avalanche behavior of the Si-SiC SuperCascode is discussed based on SPICE simulation results.

In **Chapter 4** the 25 kW 50 kHz 5 kV/700 V bidirectional galvanically isolated dc-dc converter topology, selected to evaluate the Si-SiC SuperCascode operation in a typical application is described, and specifications are given. After that, the characteristic voltage and current waveforms resulting for basic phase-shift modulation are analyzed. Out of the voltage and current stresses the power losses of the semiconductors and passive components are calculated. According to the total calculated power losses an efficiency estimation of the dc-dc converter based on the Si-SiC SuperCascode is given.

According to the design in the previous chapter, the hardware realization of the DAB converter prototype is discussed in **Chapter 5**. Resulting is a compact HV/HF demonstrator with a high power density of $4.65\,^{\mathrm{kW}}/_{\mathrm{liter}}$. Furthermore, achieved experimental results of the converter prototype are presented and discussed.

6.2 Publications

During the Ph.D. project the following papers were published:

[I] D. Aggeler, J. Biela, S. Inoue, H. Akagi, and J. W. Kolar, **"Bi-directional isolated DC-DC converter for next-generation power distribution - Comparison of converters using Si and SiC devices"**, *in Proceedings of the 4th Power Conversion Conference (PCC '07)*, Nagoya, Japan, pp. 510-517, April 2-5, 2007.

[II] D. Aggeler, J. Biela, and J. W. Kolar, **"A compact, high voltage 25 kW, 50 kHz DC-DC converter based on SiC JFETs"**, *in Proceedings of the 23rd Annual IEEE Applied Power Electronics Conference and Exposition (APEC '08)*, Austin, USA, pp. 801-807, February 24-28, 2008.

[III] J. Biela, D. Aggeler, D. Bortis, and J. W. Kolar, **"5 kV/200 ns pulsed power switch based on a SiC-JFET Super Cascode"**, *in Proceedings of the IEEE International Power Modulator Conference (PMC '08)*, Las Vegas, USA, pp. 358-361, May 27-31, 2008.

[IV] J. Biela, D. Aggeler, S. Inoue, H. Akagi, and J. W. Kolar, **"Bi-directional isolated DC-DC converter for next-generation power distribution - Comparison of converters using Si and SiC devices"**, *IEEJ Transactions on Industry Applications*, vol. 128, no. 7, pp.901-909, 2008.

[V] D. Aggeler, J. Biela, and J. W. Kolar, **"Solid-State Transformer based on SiC JFETs for future energy distribution systems"**, *in Proceedings of the Smart Energy Strategies Conference (SES '08)*, Zurich, Switzerland, September 8-10, 2008.

[VI] J. Biela, D. Aggeler, D. Bortis and J. W. Kolar, **"Balancing circuit for a 5 kV/50 ns pulsed power switch based on SiC-JFET Super Cascode"**, in Proceedings of the 17^{th} IEEE Pulsed Power Conference (PPC '09), Washington, USA, June 28 - July 2, 2009.

[VII] D. Aggeler, J. Biela, and J. W. Kolar, **"Controllable dv/dt behaviour of the SiC MOSFET/JFET Cascode - An alternative hard commutated switch for telecom applications"**, in Proceedings of the 25^{th} Annual IEEE Applied Power Electronics Conference and Exposition (APEC '10), Palm Springs (California), USA, Feb. 21-25, 2010.

6.3 Patent Applications

[I] D. Aggeler, J. Biela, and J. W. Kolar,**"JFET-Serieschaltung"**, CH Patent (CH700419).

[II] D. Aggeler, J. Biela, and J. W. Kolar, **"Verfahren zur Steuerung des du/dt Verhaltens einer Kaskodeschaltung"**, CH Patent (CH700697).

[III] D. Aggeler, J. Biela, and J. W. Kolar, **"Schalteinrichtung mit JFET-Serieschaltung"**, CH Patent.

6.4 Outlook

The thesis at hand, summaries the investigations on a novel cascaded switch topology based on wide band gap semiconductors and passive

snubber circuits, which is verified and successfully tested with a DAB dc-dc converter prototype. Besides the results achieved in this thesis there are some challenges left for future research.

As mentioned before, although the *NMSiSiCSC* is experimentally tested and verified at nominal voltage and current, the DAB dc-dc converter prototype could not operate at nominal power level due to the current limitation of the laboratory power supply. Especially to demonstrate the proper thermal and electrical behavior of the compact HV/HF transformer at nominal power would be interesting for realizing medium voltage dc-dc converters and/or solid-state transformers.

The *NMSiSiCSC* has been successfully built and experimentally tested with cascaded SiC JFETs each rated at a blocking voltage of 1.2 kV. The same concept and switch topology including the snubber circuits could be used for developing a switch with significantly higher blocking capability if the single switch would be rated for a blocking voltage of e.g. 5 kV. This technology step would offer to build easily e.g. an ultra fast 20 kV switch with four devices connected in series. Such an ultra fast HV switch is definitely a topic to be investigated in further research work.

The *NMSiSiCSC* is developed with discrete semiconductor devices. Further research vectors could include a HV package of the *NMSiSiCSC* to minimize parasitic inductances and capacitances.

Finally, also the continuous inductive operation in a wide current range will influence differently the SiC JFET lifetime due to variable voltage/current stress of the lower and upper SiC JFETs and could be an area of research itself. In particular, the inner potentials will determine the behavior of the *NMSiSiCSC* and might be interesting for a wide current range operation.

Appendix A

SiC JFET Specifications

The SiC JFETs used in various experimental measurements during this research work, have been provided by SiCED [31]. Therefore, the basic characteristic data of the SiC JFETs have been determined by SiCED and are summarized in the following Table A.1. Each SiC JFET is labeled with a reference number which is also given at the presented measurement results.

Ref. Number $Nr.$	Pinch-off Voltage $V_{pinch-off}$ [V] @ V_{ds}=400 V	Blocking Voltage V_{rb} [kV] @ I_{DSS}=2 mA	On-Resistance $R_{DS(on)}$ [Ω]
1	20.6	1.340	0.32
2	19.9	1.396	0.32
3	19.4	1.374	0.33
4	18.8	1.434	0.33
5	19.1	1.406	0.33
6	18.8	1.438	0.33
7	20.3	1.330	0.33
8	19.7	1.408	0.32
9	20.4	1.350	0.33
10	18.9	1.422	0.33
11	20.4	1.372	0.32
12	20.9	1.292	0.31
13	23.9	1.254	0.30

	@ V_{ds}=800 V		
14	9.6	1.777	0.37
15	11.0	1.787	0.43
16	12.5	1.780	0.39
17	13.1	1.759	0.39
18	14.6	1.671	0.3
19	15.2	1.758	0.37
20	9.4	1.799	0.44
21	9.4	1.660	0.40
22	10.6	1.860	0.39
23	12.5	1.778	0.36
24	13.2	1.762	0.39
25	14.2	1.703	0.34
26	9.8	1.801	0.41
27	10.8	1.708	0.43
28	12.1	1.788	0.35
29	12.7	1.777	0.38
30	13.7	1.747	0.36
31	15.2	1.574	0.31
32	9.4	1.858	0.41
33	10.4	1.788	0.43
34	11.1	1.790	0.42
35	12.6	1.725	0.42
36	13.4	1.756	0.37
37	15.1	1.619	0.32

Table A.1: Basic characteristic data of the SiC JFETs.

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Vita

Name	Daniel Aggeler
Birth	22^{th} April 1981
Place of birth	Walenstadt, SG (Switzerland)
Citizen of	Switzerland
Education	1988 – 1994 Primary School, Heiligkreuz
	1994 – 1996 Secondary School, Mels
	1996 – 2000 Gymnasium, Kantonsschule Sargans Matura Typus C
University	2000 – 2006 ETH Zürich M.Sc. in Electrical Engineering
	2001 Unaxis Balzers AG Industry Internship
	2003 – 2010 ETH Zürich Certificat of Teaching Ability (Didaktischer Ausweis) in Electrical Engineering
	2005 Itaipu Binacional, Brazil Industry Traineeship
Doctorate	2006 – 2010 Doctorate at the Power Electronic Systems Laboratory (PES), ETH Zürich
Work	2010 – present R&D Scientist Automation Devices, Power Electronic Systems ABB Switzerland Ltd. Corporate Research, Baden-Daettwil, Switzerland