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## Novel Hybrid Unidirectional Three-Phase AC-DC Converter Systems



by

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## Notation

### Acronyms

international special committee on radio interference
(comite international special des perturbations radioelectriques)
common mode
differential mode
digital signal processor
electro-hydrostatic actuator
electro-magnetic compatibility
electro-magnetic interference
electronic smoothing inductor
integrated circuit
insulated gate bipolar transistor
line impedance stabilization network
line interphase transformer
magnetomotive force
metal-oxide-semiconductor field-effect transistor
printed circuit board
pulse width modulation
root-mean-square
total harmonics distortion
uninterruptible power supply

### Symbols

a	phase <i>a</i>
a'	LIT (line interphase transformer) input on phase a
$A_{cu}$	current density in windings
$A_E$	cross section aria of magnetic core
$A_W$	required total winding aria for magnetic components
b	phase <i>b</i>
В	flux density
b'	LIT input of phase b
С	phase c
С	DC-link capacitor in ESI
c'	LIT input on phase c
$C_{DC1}$	upper side DC-link capacitor in ESI
$C_{DC2}$	lower side DC-link capacitor in ESI
$C_m$	center point of output voltage
$C_N$	filter capacitor
$C_{O}$	output capacitor
$C_{O1}$	upper side output capacitor
$C_{O2}$	lower side output capacitor
$C_r$	filter capacitor in mains side filter
$C_1$	filter capacitor in mains side filter
$C_{1d}$	filter capacitor in mains side filter
$C_2$	filter capacitor in load side filter
$C_{2d}$	filter capacitor in load side filter
D	duty cycle
$D_{avg}$	average duty cycle
DB	diode bridge
$D_{max}$	maximum duty cycle
$d_1$	local average duty cycle for $T_1$
$D_1$	diode
$d_2$	local average duty cycle for $T_2$
$D_2$	diode
$D_3$	diode
$D_4$	diode
E	half of output voltage
$E_{di}$	half of output voltage at no load
$f_{IN}$	input frequency
$f_{IN,Nom}$	nominal input frequency
$f_S$	switching frequency

HPF	high pass filter
$i_a$	mains current on phase a
$I_a$	RMS value of input current on phase <i>a</i>
$i_{af(1)}$	fundamental component in phase a current
$i_{aj}$	injection current on phase a
<i>i</i> <sub>ar</sub>	diode bridge input current in Minnesota rectifier
$i_b$	mains current on phase b
$i_c$	mains current on phase c
$i_{c,esi}$	current flowing to ESI connected to output capacitor in series
$I_{CO}$	RMS value of output capacitor current
$I_{c,rms}$	RMS value of DC-link capacitor current in ESI
$i_d$	diode bridge output current
$i_F$	detected current for active damping
$I_{IN}$	RMS value of input current
$I_{IN,d}$	d-component of detected input current
$I_{IN,q}$	q-component of detected input current
$i_j$	injection current
$I_L$	inductor current
$i_O$	pulsing output current
$I_O$	output current
$i_{rec1}$	diode bridge output current (positive side)
$i_{rec2}$	diode bridge output current (positive side)
$i_{rn1}$	diode bridge output current (negative side)
$i_{rn2}$	diode bridge output current (negative side)
$i_N$	mains current
$I_W$	RMS current on windings in magnetic components
$i_Z$	detected signal as $u_{R1}' + u_{R2}'$ for zero sequence current
$i_0$	zero sequence current
$i_1$	split current to partial rectifier system from mains
$i_{1a}$	split input current of phase <i>a</i> to partial rectifier system
$i_{1b}$	split input current of phase b to partial rectifier system
$i_{1c}$	split input current of phase c to partial rectifier system
$i_2$	split current to partial rectifier system from mains
$i_{2a}$	split input current of phase <i>a</i> to partial rectifier system
$i_{2b}$	split input current of phase b to partial rectifier system
$i_{2c}$	split input current of phase c to partial rectifier system
$I_{IN}^{*}$	amplitude of input current reference
$I_{IN}^{*}\cos(\theta_{ref,F})$	feed forward value for d-component of input currents
$I^*_{IN} sin(\theta_{ref,F})$	feed forward value for q-component of input currents
$k_{(n)}$	coefficient of harmonics amplitude defined as $1/n^2$

$k_W$	filling factor of windings for magnet components
$K_{ u,\lambda}$	coupling coefficient where v and $\lambda$ denote corresponding windings
$k_1$	coefficient of 2 <sup>nd</sup> degree in equation for switching loss calculation
$k_2$	coefficient of 1 <sup>st</sup> degree in equation for switching loss calculation
Ĺ	inductor
$L_C$	stray inductance of wire in aircraft system
$L_G$	stray inductance of electronic generator
$L_N$	mains side inductor
$LPF_1$	low pass filter for output current measurement
$LPF_2$	low pass filter for control signal
$L_{\rm S}$	leakage inductance of LIT
$\tilde{L_{II}}$	diode bridge side inductor
$\tilde{L_1}$	filter inductor in mains side filter
$L_{1d}$	filter inductor in mains side filter
$L_v$	magnetizing inductance where v denotes corresponding windings
m	number of phase
M	motor
n	harmonics order
Ν	neutral point of mains
$N_S$	sector number
$N_t$	number of turns for magnetic components
p	number of steps of staircase waveforms
$P_{con.D1}$	conduction loss of $D_1$
$P_{con,T1}$	conduction loss of $T_1$
$P_{DL}$	VA rating of input inductor
$P_{D,LIT}$	VA rating of LIT
$P_{IN}$	input power
$P_O$	output power
$P_{O,Nom}$	nominal output power
$P_S$	switching loss of power transistor
$P_{V,D}$	loss of one diode in diode bridge
$P_{v,ges}$	total loss of diode bridges
R	controller gain for ESI
$R_C$	stray resistance of wire in aircraft system
$R_{cu(L)}$	winding resistance of input inductor
$R_{cu(wA)}$	winding resistance of winding $w_A$
$R_{cu(wB)}$	winding resistance of winding $w_B$
$R_G$	stray resistance of electronic generator
$R_{g(on)}$	gate resistor for turn-on
$R_{g(off)}$	gate resistor for turn-off
$r_T$	coefficient for loss calculation of diode

$R_{th,j-c}$	thermal resistance between junction and case
$R_{th,h-a}$	thermal resistance between heat sink and air
$R_{ON}$	on resistance of power transistor
$r_1$	point of diode bridge output (positive side)
$R_1$	shunt resistor
$R_{1d}$	damping resistor in mains side filter
$r_2$	point of diode bridge output (positive side)
$R_2$	shunt resistor
$R_{2d}$	damping resistor in load side filter
$R_3$	shunt resistor
$S_{eff}$	current density of windings for magnet components
T	mains period
$T_a$	temperature of air
$t_d$	delay time of $T_{g1}$ to measure zero sequent current
$T_{g1}$	gate signal for $T_1$
$T_{g1}'$	signal for zero sequence current
$T_{g2}$	gate signal for $T_2$
$T_h$	temperature of heat sink
$T_j$	junction temperature
$T_{j-c}$	temperature difference between junction and case
$T_{ra}$	LIT on phase <i>a</i>
$T_{rb}$	LIT on phase <i>b</i>
$T_{rc}$	LIT on phase c
$T_{ri}$	switching frequency triangular signal to compare with duty cycle
$T_{ri_1}$	switching frequency triangular signal to compare with duty cycle for $T_1$
$T_{ri_2}$	switching frequency triangular signal to compare with duty cycle for $T_2$
$t_s$	period of measurement for zero sequence current
$t_1$	turn-on period of $T_1$ and $T_2$ in ESI
$T_1$	power transistor
$t_2$	turn-on and turn-off period of $T_1$ and $T_2$ in ESI
$T_2$	power transistor
$t_3$	turn-off period of both power transistors in ESI
$t_4$	turn-off and turn-on period of $T_1$ and $T_2$ in ESI
<i>u</i> '	LIT input voltage
u'*	control value of LIT input voltage
$u_a$	mains voltage of phase a
$u_{aa'}$	voltage between a and a'
$u_{ab}$	input line-to-line voltage between $a$ and $b$
$u_{a'b'}$	voltage between a' and b'
$u_{a'C}$	voltage between $a'$ and $C_m$
$u_{aN}$	input voltage of phase a

$u_{a'N}$	LIT input voltage of phase a
$u_{a'Nf}$	fundamental voltage of $u_{a'N}$
$u_b$	mains voltage of phase b
$u_{bc}$	input line-to-line voltage between phase $b$ and $c$
$u_{b'C}$	voltage between $b'$ and $C_m$
$u_{bN}$	input voltage of phase b
$\mathcal{U}_{c}$	mains voltage of phase c
$U_C$	DC-link voltage in ESI
$U_C^*$	reference for DC-link voltage in ESI
$u_{ca}$	input line-to-line voltage between phase c and a
$\mathcal{U}_{C'C}$	voltage between $c'$ and $C_m$
$u_{cN}$	input voltage of phase c
$u_{c1}$	voltage modulation in current-type hybrid rectifier using ESIs
$u_{c2}$	voltage modulation in current-type hybrid rectifier using ESIs
$U_{C1}$	voltage on divided DC-link voltage (upper side)
$U_{C2}$	voltage on divided DC-link voltage (lower side)
$u'*_d$	d-component of control value for LIT input voltage
$U_{D,max}$	maximum voltage stress on diode bridge
$u_e$	voltage across ESI
<i>u</i> ' <sub><i>F</i></sub>	amplitude of feed forward value for LIT input voltage
$U_F$	forward voltage drop on diode
$u'_F \cos(\theta_{ref,F})$	feed forward value for d-component of LIT input voltage
$u_{FF}$	feed forward signal
$u'_{F}\sin(\theta_{ref,F})$	feed forward value for q-component of LIT input voltage
$U_{f,0}$	coefficient for loss calculation of diode
$\hat{u}_i$	peak amplitude of mains voltage
$U_{IN}$	RMS value of input line-to-line voltage
$u_{j1}$	voltage of upper side IGBT in inverter
$u_{j2}$	voltage of lower side IGBT in inverter
$u_k$	$\sin \phi_f$
$u_{k,Nom}$	$u_k$ at nominal condition
$u_L$	voltage across inductor
$u_{La}$	voltage drop on input inductor
$u_N$	mains voltage
$U_N$	RMS value of input phase voltage
$u_{NC}$	voltage between $N$ and $C_m$
$\mathcal{U}_{N,d}$	d-component of mains voltage
$U_{N,Nom}$	nominal input phase voltage
$u_{N,q}$	q-component of mains voltage
$U_O$	output voltage

$U_O^*$	reference for output voltage
$U_{O1}$	voltage across four power transistors in ESI
$U_{O2}$	voltage on output capacitor connected to ESI in series
$u'_q^*$	q-component of control value for LIT input voltage
<i>U<sub>r</sub></i>	rectified three-phase input voltage
$u_{r,ac}$	AC component of rectified three-phase input voltage
$u_{R1}$	current measurement flowing on $R_1$
$u_{R1}'$	$u_{R1}$ in period of $t_s$
$u_{r1C}$	voltage between $r_1$ and $C_m$
$u_{R2}$	current measurement flowing on $R_2$
$u_{R2}'$	$u_{R2}$ in period of $t_s$
$u_{r2C}$	voltage between $r_2$ and $C_m$
$u_{R3}$	current measurement flowing on $R_3$
$U_{u1}$	duty cycle of single-switch topology
$U_{u2}$	duty cycle of two-switch topology
$\mathcal{U}_{wB}$	voltage across $w_B$
<i>u</i> ' <sub>(00)</sub>	<i>u</i> ' when $T_1$ and $T_2$ are off
<i>u</i> ' <sub>(01)</sub>	<i>u</i> ' when $T_1$ is off and $T_2$ is on
$u_1$	local average value of diode bridge output voltage (voltage across $T_1$ )
<i>u</i> ' <sub>(10)</sub>	<i>u</i> ' when $T_1$ is on and $T_2$ is off
<i>u</i> ' <sub>(11)</sub>	<i>u</i> ' when $T_1$ and $T_2$ are on
$u_{1aC}$	voltage between $1a$ and $C_m$
$u_{1a2a}$	voltage between $1a$ and $2a$
$u_{1a2a,int}$	integration of $u_{1a2a}$
$u_{1bC}$	voltage between 1b and $C_m$
$u_{1b2b}$	voltage between 1b and 2b
$u_{1cC}$	voltage between $1c$ and $C_m$
$u_{1c2c}$	voltage between $1c$ and $2c$
$u_2$	local average value of diode bridge output voltage (voltage across $T_2$ )
$u_{2aC}$	voltage between $2a$ and $C_m$
$u_{2bC}$	voltage between $2b$ and $C_m$
$u_{2cC}$	voltage between $2c$ and $C_m$
$U_{\psi}$	RMS voltage of $u_{1a2a}$
$v_m$	control signal for ESI
$W_A$	winding of LIT
$W_{A+B}$	winding of LIT
$W_B$	winding of LIT
Ζ	impedance
1 <i>a</i>	diode bridge input side on split phase a
1 <i>b</i>	diode bridge input side on split phase b
1 <i>c</i>	diode bridge input side on split phase c

2a	diode bridge input side on split phase a
2 <i>b</i>	diode bridge input side on split phase b
2c	diode bridge input side on split phase $c$
α	coefficient of $u_1$ for amplitude of LIT input voltage
β	coefficient of $u_2$ for amplitude of LIT input voltage
$\delta_{(00)}$	switching state when $T_1$ and $T_2$ are off
$\delta_{(01)}$	switching state when $T_1$ is off and $T_2$ is on
$\delta_{(10)}$	switching state when $T_1$ is on and $T_2$ is off
$\delta_{(11)}$	switching state when $T_1$ and $T_2$ are on
$\phi_{\!f}$	phase angle between mains voltage and LIT input voltage
$\eta$	efficiency
$\theta_N *$	control value for phase angle of LIT input voltage
$ heta_{ref,F}$	phase angle between mains voltage vector and reference current vector
$ heta_\omega$	phase angle of mains voltage
$\omega_{f}$	fundamental angular frequency of mains
$\omega_N$	mains angular frequency
Ψ	magnetic flux
$\psi_{sw}$	magnetic flux of switching frequency component
%Z	percent impedance of input inductor

## Abstract

In order to reduce harmonics, many rectifier topologies have been developing. Passive rectifiers, which employ only passive components, e.g. phase shifting transformers, diode bridges, and inductors etc., show some advantages concerning high efficiency, low EMC, low complexity, and high reliability. The passive components could be compact if mains frequency is high as in aircraft and micro gas turbine applications. However, the output voltage is unregulated. Furthermore, the input current of the passive rectifiers results in a staircase waveform which is not high quality if compared to active rectifiers. In this thesis, the drawbacks of the passive rectifiers are reduced.

A diode bridge rectifier whose harmonics are reduced by adding an inductor to a diode bridge is widely used in motor drive applications. Mains current quality of the diode bridge rectifier is improved if a large inductance of the passive inductor is employed. However, the inductor is bulky, heavy and occupies a large space. In this thesis, the power density of the diode bridge rectifier is improved. The Electronic Smoothing Inductor, which is able to control a current to a constant value, is applied to the diode bridge output to act as a passive inductor. A control scheme for the DC-link voltage and active damping control for filter resonances are proposed. Moreover, the filtering concept is established to effectively attenuate EMI emission. The system dimensioning of the rectifier system is also introduced. A 5kW prototype shows a significant improvement in power density. The behaviours of the proposed rectifier system are tested by assuming practical conditions, e.g. not only ideal but also unbalanced and distorted input conditions. The dynamic behaviours are also evaluated. From the results, it is verified that the Electronic Smoothing Inductor has a similar characteristic to a passive inductor having a large inductance. Therefore, the proposed rectifier system brings a significant improvement in power density without impairing any features of a diode bridge rectifier.

On the other hand, the passive 12-pulse rectifier can be extended to a hybrid rectifier having two active switches operated in an interleaved manner. The proposed topology

ensures a controlled output voltage. Furthermore, modulation schemes to realize a purely sinusoidal input current are proposed. A 10kW prototype has been build with respect to future more-electric aircraft applications. The design procedure including the magnetic components and the active parts is introduced in this thesis. The proposed hybrid rectifier and the control schemes are verified by numerical simulations and experimental results. The output voltage is regulated. Furthermore, the input current is improved from a 12-pulse staircase shape to sinusoidal by the proposed triangular modulation. Moreover, the proposed closed loop control of input currents is performed to track a reference independently of mains voltages e.g. unbalanced and distorted input voltages. Therefore, both output voltage regulation and improvement of input current quality for the 12-pulse rectifier have been achieved by the proposed schemes.

This thesis presents two rectifier systems which perform successfully. Both systems are hybrid and allow output power to flow without switching behaviours. Therefore, the proposed rectifier systems have not only high quality characteristics but also a high reliability. The system configurations, control schemes and their features are introduced.

## Kurzfassung

In der Vergangenheit wurden viele unterschiedliche Gleichrichterstrukturen untersucht, wobei häufig eine Reduktion der Harmonischen in den Phasenströmen im Vordergrund stand. Passive Gleichrichter, also Gleichrichter mit rein passiven Elementen wie Diodenbrücken, Induktivitäten oder etwa Phasenschieber-Transformatoren, zeichnen sich durch ihren hohen Wirkungsgrad, geringe Komplexität, hohe Zuverlässigkeit und geringen elektromagnetischen Störaussendungen aus, weisen jedoch bei netzfrequenten Anwendungen ein großes Volumen auf. Durch höhere Netzfrequenzen, wie diese etwa in Anwendungen in der Flugzeugindustrie oder in Mikrogasturbinen vorkommen, kann die Baugröße der passiven Gleichrichter signifikant reduziert werden, so dass diese eine interessante Alternative zu aktiven Systemen darstellen. Allerdings stellen die ungeregelte Ausgangsspannung und der treppenförmige Eingangsstrom noch eine signifikante Limitierung der rein passiven Gleichrichter dar. Dies resultiert im Vergleich zu aktiven Gleichrichtertopologien in einer wesentlich geringeren Stromqualität, weshalb in dieser Arbeit Konzepte für hybride Gleichrichterstrukturen vorgestellt werden, welche diese Einschränkungen beseitigen.

Diodengleichrichter, welche durch Hinzufügen einer Induktivität zur Diodenbrücke reduzierte Strom-Oberschwingungen aufweisen, werden häufig in elektrischen Antrieben eingesetzt. Dabei kann die Qualität der Phasennetzströme des Diodengleichrichters verbessert werden, indem ein großer Induktivitätswert für diese Induktivität gewählt wird. Dies resultiert jedoch in einer unhandlichen, schweren und vor allem großen Induktivität. Um die Leistungsdichte des Gleichrichters zu erhöhen, wird ein kompaktes leistungselektronisches System mit einer kleinen Induktivität an den Ausgang der Diodenbrücke geschaltet, welches sich durch geeignete Regelung wie eine große passive Induktivität verhält ("elektronische Glättungsdrossel"). Zudem werden Regelungsverfahren für die Stabilisierung der Ausgangsgleichspannung und ein Verfahren zur aktiven Dämpfung von Filterresonanzen vorgestellt und die Unterdrückung von Harmonischen sowie das EMV Verhalten untersucht. Die Dimensionierung des Gleichrichtersystems unter Verwendung der elektronischen Glättungsdrossel wird ausführlich beschrieben. Ein 5 kW Prototyp zeigt eine signifikante Erhöhung der Leistungsdichte. Das Verhalten des vorgeschlagenen Gleichrichtersystems wird nicht nur unter idealen, sondern auch unter praxisnahen Bedingungen wie verzerrten oder unsymmetrischen Netzspeisungen getestet. Ebenso wird das dynamische Verhalten des Systems evaluiert. Die erhaltenen Ergebnisse verifizieren, dass die elektronische Glättungsdrossel die Charakteristik einer passiven Drossel mit hohem Induktivitätswert nachbilden kann. Das vorgeschlagene Gleichrichtersystem resultiert daher in einer signifikanten Erhöhung der Leistungsdichte, ohne dass die grundlegende Struktur des Diodengleichrichters verändert wird.

Alternativ kann ein 12-Puls-Gleichrichtersystem durch zwei, phasenverschoben arbeitende Schalter zu einem hybriden Gleichrichter erweitert werden. Die vorgeschlagene Topologie stellt eine geregelte Ausgangsspannung sicher und mit den vorgestellten Modulationsverfahren wird ein rein sinusförmiger Eingangsstrom ermöglicht. Zur Validierung der Konzepte wurden numerische Simulationen durchgeführt und ein Prototyp mit einer Leistung von 10 kW realisiert, der den Anforderungen der Flugzeugindustrie (More-Electric Aircraft) gerecht wird. Überdies wird eine Designprozedur, welche sowohl die magnetischen als auch die aktiven Bauelemente beinhaltet, beschrieben. Die Ausgangsspannungsregelung stellt eine konstante DC-Ausgangsspannung sicher. Darüber hinaus wird der 12-pulsige, treppenförmige Eingangsstrom durch eine geeignete Dreieck-PWM-Modulation in einen sinusförmigen Eingangsstrom übergeführt. Zudem ermöglicht die vorgeschlagene Regelungsstruktur die Eingangströme proportional zu einem Referenzsignal unabhängig zu den Netzspannungen zu führen, was besonders in verzerrten oder unsymmetrischen Netzen von Bedeutung ist. Daher kann sowohl die Regelung der Ausgangsspannung als auch eine Verbesserung der Eingangsstromqualität für den 12-Puls-Gleichrichter durch das Regelungsverfahren erreicht werden.

Diese Arbeit präsentiert zwei erfolgreich realisierte Gleichrichtersysteme. Beide Systeme sind hybrid und ermöglichen einen Leistungsfluss an den Ausgang auch ohne Schalthandlungen. Daher besitzen die beiden vorgeschlagenen Gleichrichtersysteme neben hohen qualitativen Eigenschaften auch eine hohe Zuverlässigkeit und sind sehr gut für einen zukünftigen industriellen Einsatz geeignet.

# Chapter 1

## Introduction

In 1879, Thomas Edison invented the first electric lamp. Since then, utilization of electricity has been rapidly developing and now power electronics are widely used in many applications such as in industry, transformation, computers, lights, homes, and so on. Power systems are globally constructed and the consumed electric power is still increasing. The field of power electronics is also increasing, e.g. car and aircraft manufactures consider using more electrical power while reducing oil consumption.

Since most of power systems utilize AC voltages for transmission and DC voltages are easily managed in power electronics equipment, rectifiers which achieve AC to DC conversion are required. A diode bridge rectifier, which composes of only a diode bridge and a capacitor, generates high harmonics on mains. Although, the diode bridge rectifiers show high power density, high efficiency, high reliability, low complexity, input currents include a high THD which is acceptable in only small power applications. Many rectifiers are connected to a power system and therefore the pollution caused by harmonics is a serious issue. For instance, capacitors and/or resistors are burned and/or malfunctions are caused in equipment if high harmonics are present in power systems. Therefore, rectifiers should give low harmonics to the mains.

Many rectifier topologies have been developed so far. The active rectifiers are one solution to reduce harmonics and volume of the passive components, i.e. current can be actively controlled and bulky passive components are not necessary. Therefore, a purely sinusoidal current can be provided by the active rectifiers. However, a high mains current quality is not required in some applications, e.g. a rectangular or a multi level staircase waveform including a low level of harmonics is acceptable in some

areas. For instance, rectifiers drawing rectangular currents are widely applied in motor drive applications. For the active rectifiers, a high switching frequency is also required in order to obtain a purely sinusoidal input current and reduce the volume of passive components, which causes a reduction in the efficiency by 2 or 3% due to high switching losses. The realization effort of the active rectifiers is also high because controller and EMI filter designs are complicated. The other features of the active rectifiers are bidirectional power flow and controllability of output voltage, which allow regeneration from a load to the mains and output voltage regulation. However, the function for regeneration is not needed in many applications. Accordingly, active rectifiers have some drawbacks and passive rectifiers can be useful in some areas; active rectifiers are not focused in this thesis.

Several passive rectifiers have been developed to reduce harmonics on the mains [1]. Furthermore, hybrid rectifiers, which are combined passive rectifiers and active switches such as MOSFETs and IGBTs, have been proposed. In **Fig.1-1**, passive rectifiers and hybrid rectifiers are classified. It is noted that the detail classification of active rectifiers are not shown here.



Fig.1-1: Classification of three-phase rectifier concepts with low effect on the mains.

The typical passive rectifiers are shown in **Fig.1-2**. 6-pulse staircase waveform can be obtained by a single bridge rectifier using a three-phase  $\Delta$ -Y phase shifting transformer connected between the diode bridge and the mains (cf. Fig.1-2(a)). The input current quality is then improved compared to a rectangular shape. Furthermore, the input current  $i_a$  can be closer to a sinusoidal shape if two diode bridges are arranged (cf. Fig.1-2(b)) i.e. a three-phase  $\Delta$ - $\Delta$  transformer and a diode bridge are additionally connected to the 6-pulse rectifier. By using two 6-pulse rectifiers, the input current is converted to a 12-pulse staircase shape and the THD is reduced. For instance, 5<sup>th</sup> and 7<sup>th</sup> harmonics are eliminated by 12-pulse rectifiers. It is noted that the diode bridge outputs can be connected in series if a high output voltage is needed. Furthermore, the  $\Delta$ - $\Delta$  transformer can be omitted if isolation between mains and load is not required. Several non-isolated phase shifting transformers have also been

proposed. As an example, the well-know winding arrangement for a non-isolated phase shifting transformer employed in a passive 12-pulse rectifier is depicted in **Fig.1-3**. The non-isolated transformer can be compact compared to isolated one.

The 11<sup>th</sup> and 13<sup>th</sup> harmonics can also be cancelled by 18-pulse rectifiers which employ three 6-pulse rectifiers. Therefore, input current quality can be improved by increasing the number of 6-pulse rectifiers. However, the numbers of diode bridges and transformers are also increased e.g. four diode bridges are normally required for a 24pulse rectifier. Furthermore, the phase shifting transformers are bulky if the passive rectifiers are applied to 50 or 60Hz mains frequency. However, the transformers can be compact if mains frequency is high, e.g. 400Hz mains frequency as utilized in aircrafts. Since the passive rectifiers have neither active switches nor control circuit, there are some advantages which are mainly a high efficiency, low EMC, and high reliability. Therefore, the passive rectifiers are normally used for high power applications in which the volume of the transformers is not a serious issue.



**Fig.1-2**: Conventional passive rectifiers and the theoretical input current shapes for 6-pulse (**a**) and 12-pulse (**b**) with isolation transformer(s).



Fig.1-3: Conventional 12-puslse rectifier topology with a non-isolated transformer.

On the other hand, output voltage of passive rectifiers cannot be regulated and hence output voltage changes depending on input voltage and output power. In order to solve this problem and improve input current quality, there are some hybrid approaches which are combined passive rectifiers and active switches. In **Fig.1-4**, the active switches, the fast recovery diodes, and the inductors, which comprise the boost stages, are employed between the load and each output of the passive rectifier [8]. The output voltage is then controlled by adjusting the duty cycle of the active switches. The volume of the inductors can also be reduced by using a high switching frequency. However, the inductors and the first recovery diodes are connected to both positive and negative lines in order to mitigate a zero sequence current flowing between the boost stages. This causes a high conduction loss.



Fig.1-4: A conventional hybrid rectifier which can regulate output voltage.

Input current quality can also be improved by hybrid rectifiers. Several hybrid topologies to reduce input current harmonics have been proposed. One of the conventional hybrid rectifiers shown in **Fig.1-5** employs the bidirectional switches to the 12-pulse rectifiers [7]. Input current waveforms is improved from a 12-pulse to 24-pulse shape with switching operation of the bidirectional switches. Each bidirectional switch is turned on twice a mains cycle and therefore the switching frequency is not high. The voltage across the phase shifting transformer can be alternatively selected by switching operation e.g. the full output voltage at turn-off state or the half output voltage at turn-on state. Therefore, the number of staircase steps of the phase shifting transformer input voltage  $u_{a'N}$  is increased to double and input current harmonics can be reduced.



**Fig.1-5**: A conventional hybrid rectifier which can improve input current quality from 12-pulse to 24-pulse waveforms.

In **Fig.1-6**, the auxiliary current injection circuit is employed to reduce input current harmonics [8]. A triangular current synchronized with mains frequency is actively generated from the PWM controlled auxiliary circuit and injected to both diode bridge outputs ( $i_{rec1}$  and  $i_{rec2}$ ). The frequency of the triangular injection current  $i_j$  is sixfold mains frequency if the main circuit is a 12-pulse rectifier. The phase angle of both  $i_{rec1}$  and  $i_{rec2}$  is 180° shifted to each other and the amplitude should be modulated from 0 to  $I_O/2$ . Then a purely sinusoidal input current is achieved. Several current injection schemes to passive rectifiers have also been proposed in that an auxiliary circuit is employed to inject and/or modulate the diode bridge output currents [10] [11].

As the other example, Minnesota rectifier [12], which is an extended topology from a 6-pulse rectifier, is shown in **Fig.1-7**. In this hybrid rectifier, a three times mains frequency harmonic current  $i_{aj}$  whose shape is equal to a middle phase of three-phase

sinusoidal references is injected and an input current resulting from  $i_a=i_{ar}-i_{aj}$  can be purely sinusoidal [13]. The injection network consists of the passive components and the currents flowing to the injection network and *L* are actively controlled by the switches  $T_1$  and  $T_2$ . Accordingly, the performance of the passive rectifier is improved where active switches help to modulate the injection current.



**Fig.1-6**: A conventional hybrid rectifier which can achieve purely sinusoidal input currents by a current injection from the auxiliary circuit.



**Fig.1-7**: A conventional hybrid rectifier (Minnesota rectifier) which can achieve purely sinusoidal input currents by a current injection scheme.

As described above, rectifier topologies are classified into active rectifiers, passive rectifiers, and hybrid rectifiers (cf. Fig.1-1). Hybrid systems allow combining the advantages of the passive and active approaches, especially if the active system part would process only a fraction of the total throughput power. There, both passive and hybrid rectifiers can also be divided into voltage-type and current-type. The voltage-type and the current-type are respectively defined as either voltage or current is impressed on the diode bridge output i.e. an inductor is employed on the mains side in the voltage-type (cf. Fig.1-5) and on the diode bridge output side in the current-type (cf. Fig.1-2). Several approaches to achieve a purely sinusoidal input current in the current-type hybrid rectifiers have been proposed. However, no solution has been proposed in the voltage-type hybrid rectifiers so far. Furthermore, the phase shifting transformer of the voltage-type passive rectifiers for achieving a controlled output voltage and/or a purely sinusoidal input current by PWM control.

### **1.1 Organization of the thesis**

In this thesis, two hybrid rectifier systems are derived, analyzed, and experimentally verified. First, a three-phase diode bridge employed as front-end in variable speed drive converter systems should be extended by adding the Electronic Smoothing Inductor which is able to control the diode bridge DC output current to a constant value and therefore reduces THD of the mains current, the output capacitor current stress, and the output voltage ripple. Furthermore, a concept for applications in future More Electric Aircraft should be addressed based on a 12-pulse line interphase transformer (voltage-type) rectifier where interleaved boost-type output stages provide an output voltage base for designing the proposed rectifiers should be established in order to facilitate a transfer of the concepts into future industry systems. Finally, both concepts should be evaluated against the state of the art in order to clarify advantages and weaknesses.

The practical realization and the performance of the Electronic Smoothing Inductor topology are introduced in **section 2**. The control scheme to ensure a constant DC-link voltage and attenuation of filter resonances are proposed. Furthermore, the filtering concept, which effectively reduces EMI emission noises with a low volume and a low loss, is proposed. The simulation results and the system dimensioning are introduced and a 5kW prototype was build in order to verify the performance. The system behaviours and the features not only for ideal conditions but also for non-ideal

conditions, e.g. unbalanced and distorted mains voltages behaviours and dynamic operation, are discussed.

In section 3, the passive voltage-type 12-pulse rectifier is extended to a hybrid type with installed boost stage(s). The drawbacks of the conventional passive rectifiers are introduced and the novel hybrid rectifiers are proposed. The several control schemes, e.g. the constant duty cycle control resulting in a 12-step staircase input current, the triangular modulation scheme achieving a purely sinusoidal input current, and the closed loop control reducing an influence of non-ideal mains voltage on input current quality, have also been proposed. The detailed design procedure including the magnetic components and the active part is introduced. Finally, the proposed hybrid rectifiers are verified and the control schemes are compared by numerical simulation and experimental measurements.

In section 4, future work to extend and improve the performance of both rectifier topologies are introduced.

Finally, the futures and the advantages of both hybrid rectifier topologies are summarized in **section 5**.

## **1.2** Contributions of this work

The main contributions of this work are listed in the followings:

- control schemes for the Electronic Smoothing Inductor are proposed. DC-link voltage is successfully controlled and filter resonances are actively damped by the proposed control schemes;
- filtering concept for the Electronic Smoothing Inductor is proposed. Low voltage components can be utilized in the filter and the filter performance is verified by simulation and experimental results;
- it is demonstrated that the proposed rectifier system using the Electronic Smoothing Inductor shows much higher power density compared to a conventional passive diode bridge rectifier;
- it is verified that a rectifier employing the Electronic Smoothing Inductor has a similar performance to a diode bridge rectifier employing a large inductor;
- a conventional voltage-type 12-pulse passive rectifier is extended to hybrid rectifiers. Two kinds of hybrid rectifiers are proposed and controllability of output voltage is obtained;
- zero sequence current flowing between diode bridges via a phase shifting transformer is reduced by the proposed low cost control scheme.
- several input current control schemes for the hybrid 12-pulse rectifiers are proposed and advantages and drawbacks are theoretically and experimentally clarified;
- modulation functions of the hybrid 12-pulse rectifier for achieving a purely sinusoidal input current are derived and the improvement verified by numerical simulation and measurements;
- a closed loop control scheme, which ensures low input current harmonics independent of unbalanced and/or distorted input voltages, is proposed for the hybrid 12-pulse rectifier. The capability of the control scheme is verified by numerical simulation and experimental results.

### **1.3 Publications**

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- Gong, G. Heldwein, M.L. Drofenik, U. Mino, K., Kolar, J.W., Comparative Evaluation of Three-Phase High Power Factor AC-DC Converter Concepts for Application in Future More Electric Aircrafts., Proceedings of the 19th Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim (California), USA, February 22 - 26, Vol. 2, pp. 1152 - 1159 (2004).
- Nussbaumer, T. Mino, K., Kolar, J.W., Design and Comparative Evaluation of Three-Phase Buck Boost and Boost Buck Unity Power Factor PWM Rectifier Systems for Supplying Variable DC Voltage Link Converters., Proceedings of the 10th European Power Quality Conference (PCIM), Nuremberg, Germany, May 25 - 27, Vol. 1, pp. 126 - 135 (2004).
- 4. Mino, K. Gong, G. Kolar, J.W., Novel Hybrid 12-Pulse Line Interphase Transformer Boost-Type Rectifier with Controlled Output Voltage., Proceedings of the 4th International Power Electronics and Motion Control Conference, Xian, China, Aug. 14 - 16, Vol. 2, pp. 924 - 931 (2004).
- 5. Mino, K. Heldwein, M.L. Kolar, J.W., Ultra Compact Three-Phase Rectifier with Electronic Smoothing Inductor., Proceedings of the 20th Annual IEEE Applied Power Electronics Conference and Exposition, Austin (Texas), USA, March 6 10, Vol. 1, pp. 522 528 (2005).
- Mino, K. Nishida, Y. Kolar, J.W., Novel Hybrid 12-Pulse Line Interphase Transformer Boost-Type Rectifier with Controlled Output Voltage and Sinusoidal Utility Currents., Proceedings of the 2005 International Power Electronics Conference (IPEC'05), Niigata, Japan, April 4 - 8, CD-ROM, ISBN: 4-88686-065-6 (2005).
- Gong, G. Heldwein, M. L. Drofenik, U. Mino, K. Kolar, J. W., Comparative Evaluation of Three-Phase High-Power-Factor AC-DC Converter Concepts for Application in Future More Electric Aircraft., IEEE Transactions on Industrial Electronics, vol. 52, no. 3, pp. 727-737, June 2005.

- 8. Mino, K. Gong, G. Kolar, J. W., Novel Hybrid 12-Pulse Boost-Type Rectifier with Controlled Output Voltage., IEEE Transactions on Aerospace and Electronic Systems, vol. 41, no. 3, July 2005, pp. 1008 - 1018.
- Mino, K. Nishida, Y. Kolar, J. W., Novel Hybrid 12-Pulse Line-Interphase-Transformer Boost-Type Rectifier with Controlled Output Voltage and Sinusoidal Utility Currents., the IEEJ Transactions of the Institute of Electrical Engineers of Japan, vol. 127-D, no. 4, April 2007, pp.382-390.

### **1.4 Patent applications**

1. Mino, K. Nishida, Y. Kolar, J. W., Rectifying Circuit, Japanese patent, JP2006211867, 10-Aug.-2006

## **Chapter 2**

## **Electronic Smoothing Inductor**

The Electronic Smoothing Inductor (ESI) [18][19] is one attractive topology in order to reduce not only the harmonic current level but also volume and output voltage ripple of three-phase rectifiers with a low realization effort. In [19], the circuit topology and the control schemes for the ESI have been proposed and the basic operation has also been demonstrated with a laboratory prototype. However, aspects relevant for implementation in industry or motor drive applications such as the detailed control strategy and the EMI filter design have not been considered.

In this section, a practical realization of the ESI is presented. The control concept for DC-link voltage and the active damping for filter resonances are proposed. Furthermore, the main circuit design for a 5kW prototype including the EMI filter for fulfilling the requirements of CISPR 22 - Class A is described. The proposed schemes are verified and evaluated by numerical simulation and experimental results with assumption of conditions such as not only nominal operation but also unbalanced and distorted input voltages and dynamic operation.

### 2.1 Conventional three-phase rectifiers

Three-phase rectifiers are widely used in motor drives, UPSs, telecommunications, industrial equipment and so on. It is necessary that these three-phase rectifiers should have a low effect on the mains. This is typically achieved by applying inductor(s) on

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the DC side and/or mains side of a three-phase diode bridge as the simple solutions (cf. Fig.2-1). High reliability and a low EMC as well as cost saving are the main advantages of these passive rectifiers. In Fig.2-2, simulation results for Fig.2-1(a) are shown. A non-sinusoidal current flows on the mains and the current has a high distortion especially if the inductance of inductor L is small. In order to reduce the THD and improve the power factor, the inductance must be increased. However, the inductance to achieve a sufficient input current quality is significantly large, which results in a bulky and weighty inductor. In the case that  $L=\infty$  is employed, the input current forms a 120° wide interval rectangular shape showing 0.955 (=3/ $\pi$ ) of the power factor and 31% of THD. The passive rectifier is widely used in motor drive applications if the input current is smooth in 120° wide intervals. The ripple currents are also dependent on the inductance of L and the current stresses are high if the inductance is small as shown in Fig.2-3. Therefore, a larger volume for the output capacitor having an enough ripple current capability is required if a smaller inductance of L is employed. Furthermore, an increase in the current capabilities of the other components such as the inductor, the diode bridge, fuses, breaker, wires etc. should be considered. Accordingly, the inductance of L must be enough large in order to practically apply to a system. However, the volume, weight, and power density are significantly impaired.

Moreover, the increased *L* also worsens dynamic behaviour of the output voltage because the characteristic impedance  $Z^2 = L/C_0$  is increased as compared to the load resistance which reduces the damping of the  $LC_0$  smoothing filter. This problem is additionally intensified in the case of supply to nonlinear loads.



**Fig.2-1**: The conventional three-phase rectifiers with inductor(s) on the DC side (a) and the mains side (b) of the diode bridge.

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**Fig.2-2**: Simulation results of input current waveforms (a), THD and power factor (b) of the conventional passive rectifier shown in Fig.2-1(a) in dependence on the inductance of *L*. Simulation parameters: Input line to line voltage is  $400V_{rms}$  and output power is 5kW.



**Fig.2-3**: Simulation result of current stress ( $I_L$  on the inductor L,  $I_a$  on the mains, and  $I_{CO}$  on the output capacitor  $C_O$ ) of the conventional passive rectifier shown in Fig.2-1(a). Simulation parameters are as Fig.2-2.

In order to reduce volume and weight of passive components such as magnetic components and capacitors, many active rectifier topologies using turn-off power semiconductors have been developed. In **Fig.2-4**, the simplest three-phase active rectifiers employing single-switch [20] are shown. A current flowing to the diode
bridge outputs can be controlled to be smooth (except for a switching frequency current ripple). Therefore, the input current THD and the volume of L can be reduced. However, the impressed voltage on the power semiconductors is the full output voltage, which causes a high loss in the power semiconductors and a high volume of the heat sink.



**Fig.2-4**: Conventional active rectifiers using single-switch and placing inductor(s) on DC side (a) or mains side (b).

# 2.2 Principle of operation

The ESI is able to control a diode bridge output current and makes it possible to reduce not only mains current harmonics but also output voltage ripple. In this section the principle of operation and the advantages of the ESI are described. The basic circuit configuration of the ESI connected to the diode bridge output, the time behaviour of the voltages, and the gate signals of the power transistors are depicted in **Fig.2-5**. The ESI consists of an inductor, two MOSFETs, two diodes, and DC-link capacitor. The ESI voltage  $u_e$  is the difference between the rectified input voltage  $u_r$  and the output voltage  $U_o$ . Accordingly  $u_e$  varies within the range given by

$$\frac{\sqrt{3}}{2}\hat{u}_i - U_O(=-0.089\hat{u}_i) \le u_e \le \hat{u}_i - U_O(=0.045\hat{u}_i)$$
(2-1).

where  $\hat{u}_i$  denotes the amplitude of the line-to-line input voltage. DC-link voltage  $U_C$  has to be higher than  $u_e$  in order to avoid any inrush currents flowing to C and to keep controllability of the current flowing to ESI. However, it is clearly seen from (2-1) that  $u_e$  is much lower than  $\hat{u}_i$ . Therefore, DC-link voltage  $U_C$  can be adjusted to a low level.

The inductor current  $I_L$  is controlled to a constant value (DC current with superimposed switching frequency current ripple) by operating  $T_1$  and  $T_2$  with a variable duty cycle. In the turn-on period of both  $T_1$  and  $T_2$  shown as  $t_1$  in Fig.2-5(c), the DC-link capacitor *C* is discharged as shown in **Fig.2-6**(a) and  $I_L$  increases. On the other hand, *C* is charged and  $I_L$  decreases when both transistors are turned off (cf.  $t_3$  in Fig.2-5(d) and Fig.2-6(c)). In the period when either  $T_1$  or  $T_2$  is turned on (cf.  $t_2$  in Fig.2-5(c) or  $t_4$  in Fig.2-5(d)),  $I_L$  does not flow in *C* as depicted in Fig.2-6(b) and (d). Therefore, *C* is charged when  $u_e$  is positive. Then the average duty cycle of the power transistors is smaller than 50% in order to ensure a turn-off period for both  $T_1$  and  $T_2$  simultaneously (cf.  $t_3$  in Fig.2-5(d)). On the other hand, *C* is discharged when  $u_e$  is negative and the average duty cycle is then higher than 50% in order to generate both turn-on periods at same time (cf.  $t_1$  in Fig.2-5(c)). Therefore, a 3-level operation (*C* is discharged, bypassed, and charged) is realized. This topology brings the following advantages:

• low voltage semiconductors such as Schottky diodes showing almost no reverse recovery and power MOSFETs having a low on resistance and high speed switching characteristics can be employed in the ESI because  $U_C$  can be adjusted to a lower level, which allows a high switching frequency, low conduction losses, and low switching losses;

- the inductance of *L* and/or the switching frequency current ripple is small because the apparent switching frequency is a double as shown in Fig.2-5(c) and (d);
- the volume and the weight of the ESI are considerably smaller when compared to a conventional passive smoothing inductor shown in Fig.2-1;
- the ripple current stress on the output capacitor  $C_o$  is lower as compared to passive rectifiers and active rectifiers due to an almost constant DC-line current.



**Fig.2-5:** Circuit schematic of the ESI connected to the output of diode bridge (**a**), time behaviour of operational voltages (**b**), gate signals at  $u_e < 0$  (**c**) and  $u_e > 0$  (**d**).



**Fig.2-6:** Current paths in the ESI at the period  $t_1$  (**a**),  $t_2$  (**b**),  $t_3$  (**c**), and  $t_4$  (**4**) shown in Fig.2-5.

The inductor L can be also connected on the mains side as shown in **Fig.2-7** instead of the DC side (cf. Fig.2-5(a)). The simulation result shows that the input currents are improved to nearly rectangular shapes (**Fig.2-8**). In the case of the mains side inductor scheme, the input current ripple is higher (Fig.2-8(b)) if compared to the DC side scheme (Fig.2-8(a)). When one diode in the diode bridge starts to conduct, the input current flowing to the mains side inductor is increased quickly. Then the input current is overshot and oscillated. In the DC side inductor scheme, the input current ripple is smaller (cf. Fig.2-8(a)) because the inductor current is not rapidly changed compared to the mains side inductors. Accordingly, the DC side inductor scheme has advantageous concerning a smaller ripple current. Therefore, the DC side inductor scheme is focused on in this thesis.



**Fig.2-7**: Three-phase rectifier system employing an ESI divided into one part on the mains side inductor *L* and the other part on DC side.



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**(b)** 

**Fig.2-8**: The simulation results of the ESI employing DC side inductor (**a**) as Fig.2-5 and mains side inductor (**b**) as Fig.2-7. The simulation parameters: the input line-to-line voltage  $400V_{rms}$ , *L*= $400\mu$ H in (**a**) and  $200\mu$ H in (**b**), *C*=1.32mF, *C*<sub>0</sub>= $47\mu$ F, the switching frequency 70kHz, the dc-link voltage  $70V_{dc}$ , the output voltage  $536V_{dc}$ , and the output power 5kW.

# 2.3 Control scheme

## 2.3.1 Hysteresis control

The hysteresis control and the PWM control have been presented and both control schemes have been theoretically compared (cf. Fig.5 and Fig.7 in [19]). The simulation result of the hysteresis control is shown in **Fig.2-9**. In this simulation, the current flowing to the ESI is limited to within  $\pm 5\%$  by the hysteresis control. Therefore, the drawbacks of the hysteresis control are variable switching frequency, which brings difficulties in design and/or attenuate switching ripple. In the case of the PWM control, frequency of ripple current is double the switching frequency (cf. Fig.2-5(c) and (d)). However, the hysteresis control causes 2-level operation because the power transistors  $T_1$  and  $T_2$  are driven by the same signal. Therefore, a higher switching frequency ripple and/or a higher switching frequency are present if compared to the PWM control. Consequently, the hysteresis control results in a large volume of EMI filter, high EMI noise, and/or high switching losses. Therefore, the PWM control (3-level behaviour) is advantageous and focused on in this thesis.



**Fig.2-9**: The input current waveforms controlled by hysteresis control. The simulation parameters are as Fig.2-8(a).

### 2.3.2. PWM control

The basic control scheme including the proposed DC-link voltage control and the active damping for reducing resonances is described in this section. The control block

diagram is shown in **Fig.2-10**. The ESI is placed in the negative DC line to allow measuring all the currents required for the control implementation by shunt resistors which are cheaper and of smaller volume compared to current transducers. The ESI input current  $I_L$  is controlled to reach the output current  $I_O$  by using a feed forward control. There, a low-pass filter  $LPF_1$  has to be employed for attenuating high frequency components present in the case of pulsating load current such as when the rectifier is supplying a PWM inverter or a DC-DC converter. To detect the average output current, several low pass filters are connected in series in  $LPF_1$  in order to achieve a sufficient attenuation of pulsating load currents as well as minimizing the detection delay time when the load is dynamically changed. In this case, two low- pass filters, each with a cut-off frequency of 5.3kHz, are employed, which has enough attenuation for a pulsing signal higher than 10kHz. It is noted that the number of series connections of the low pass filter can be increased if a higher attenuation is required instead of impairing load dynamic response.

The loss compensation value R, which is the gain for the current control, is adjustable in order to control the current shape of  $I_L$  [19].  $I_L$  has a sixfold mains frequency ripple and the detected ripple is multiplied by the R-value. Therefore, a high R-value produces a low sixfold mains frequency current ripple on the DC-line. For the 5kW ESI, the R-value is set to 30 in order to keep the low ripple in the control signal line and to achieve sufficient current controllability. For attenuating the equivalent switching frequency ripple, a low pass filter  $LPF_2$  should be employed in the main control loop. The cut-off frequency is selected around 400Hz, which should be higher than the sixfold mains frequency (300Hz or 360Hz) and enough to reduce the equivalent switching frequency (140kHz) ripple to a sufficient level.

For controlling the DC-link voltage  $U_c$ , a PI-type controller is used and connected in parallel to the main control loop. This allows adjusting offset of control signal  $v_m$ . If no loss is generated in the DC-link capacitor *C*, the offset should be zero. However, an offset is needed to increase the charge current into *C* because the loss in *C* is not zero in practice.

Resonant currents that normally occur at times of diode bridge commutations are detected by using a high-pass filter and are actively damped by feeding back into the main control loop. The high pass filter, *HPF*, is used to sense the resonant currents and to block the low frequency components of the rectifier current such as the sixfold mains frequency. The cut-off frequency is adjusted to 723Hz. Finally, the gate signals  $T_{g1}$  and  $T_{g2}$  are determined by intersecting the control signals and a triangle waveform.





**Fig.2-10**: Practical implementation of rectifier system including ESI and current and voltage sensing (a) and control block diagram in case of the PWM control (b).

# 2.4 System dimensioning

In this section the system dimensioning and selection of the main components for the 5kW prototype including the ESI and the EMI filters are introduced.

### 2.4.1 Main components

The specifications of the prototype of the rectifier system including the ESI are defined as:

Input line-to-line voltage:	$U_{IN} = 400 V_{rms} \pm 15\% (50/60 Hz)$
Nominal output power:	$P_O = 5 \mathrm{kW}$
Nominal output voltage:	$U_O = 540 \mathrm{V_{dc}}$
Nominal output current:	$I_O = 9.26 A_{dc}$
Switching frequency:	$f_s = 70 \mathrm{kHz}$
	(effective frequency: 140kHz)

The switching frequency  $f_S$  is set so that the resulting effective switching frequency, which is  $2f_S$ , is below the minimum frequency of the EMI standard. In this case, the use of an effective frequency of 140kHz is below the 150kHz starting frequency of CISPR 22. The inductance *L* is selected so that the amplitude of the ripple current is within ±15% of DC current  $I_L$  at the nominal operating point. Accordingly, the inductance is calculated by using

$$L = \frac{(\sqrt{3/2})\hat{u}_i - (U_O - U_C)}{0.3I_L \times 2f_S} D_{\max}$$
(2-2)

where  $D_{\text{max}}$  denotes the maximum duty cycle of the power transistors. The required inductance, which is calculated as 40µH, is divided into two 20µH inductors and connected to both input lines of the ESI. This could help in reducing common mode noise. To achieve DC current control,  $U_C$  must be set as  $U_C \ge 0.089\hat{u}_i$  (cf. (2-1)). In order to guarantee the operation also for unbalanced mains voltage,  $U_C$  is adjusted to  $70V_{dc}$  (=0.12 $\hat{u}_i$  at  $U_{IN}$ =400V<sub>rms</sub>). The current stress on *C* defined in [19] is

$$I_{C,rms} = 0.186 I_L \sqrt{\frac{\hat{u}_i}{U_C}}$$

$$\tag{2-3}$$

Capacitors having sufficient ripple current capability are selected for *C* and  $C_0$  respectively. Theoretically the average duty cycle of  $T_1$  and  $T_2$  is 0.5 (considering a  $\pi/3$ -wide interval of the mains period) and the current stress on the power transistors  $T_1$  and  $T_2$  and the power diodes  $D_1$  and  $D_2$  is equal. **TABLE 2-1** lists the main components. The 150V MOSFETs and Schottky diodes are selected in order to obtain

a sufficient voltage margin assuming the DC-link voltage (= $70V_{dc}$ ) and spike voltage during switching states.

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Component	Symbol	Value
Inductor	L	20µH (2 in series)
DC-link capacitor	С	$330 \mu F / 100 V_{dc}$ (4 in parallel)
Schottky diode	$D_1, D_2$	150V / 2×10A
MOSFET	$T_1, T_2$	150V / 41A
Three-phase rectifier bridge	DB	800V / 28A
Output capacitor	Co	$47\mu F / 400 V_{dc}$ (2 in parallel, 2 in series
Heat sink and fan		0.7K/W

**TABLE 2-1**: Main circuit components of 5kW ESI prototype:  $U_{IN}$ =400V<sub>rms</sub>,  $P_O$ =5kW,  $f_S$ =70kHz.

# 2.4.2 Filtering concept and realization

Due to the high switching frequency of the ESI, an EMI filter attenuating the high frequency components is required. The chosen filtering strategy and the topology are presented in **Fig.2-11**. As the converter is a three-phase rectifier, a conventional approach would be to place a three-phase filter topology only at the input side of the diode bridge so that it is responsible for filtering any noise that could be coupled to the power grid. However, since the high frequency ESI is inserted in the DC-line, part of the filter stage should be also placed directly at the ESI input and/or on the DC side. This brings some advantages, namely:

- the rated voltage for the load side filter capacitors is much lower than for the mains side filter capacitors and the total number of components is smaller as just a single filter stage has to be employed;
- since the load side filter is connected with the output capacitor in series, the RMS current in the output capacitor is decreased;
- the high frequency noise coupled to the output and to the input is lowered by the load side filter. This causes the mains side filter to be of smaller volume and the output voltage to present a lower high frequency ripple;
- high frequency noise is filtered more effectively and/or total volume of the filter can be reduced because the noise is directly filtered close to its origin.

For the system described in this thesis, the filter is designed according to the requirements of CISPR-22 for equipment classified as Class A. The design of the filter

stages is performed by using a procedure described in [22]. The components used in the filters are listed in **TABLE 2-2**.



Fig.2-11: Filtering concept and topology for rectifier employing the ESI.

<b>TABLE 2-2.</b> Livit Thick components of 5KW LST prototype for fulfilling CIST K 22 Class A	<b>TABLE 2-2</b> : EMI Filter components of 5kW ESI prototype for full	ılfilling CISPR 22 – Class A
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Component	Symbol	Value
Capacitor	$C_1$	470nF / 275V <sub>ac</sub>
Capacitor	$C_{1d}$	$68nF/275V_{ac}$ , 3 in parallel
Resistor	$R_{1d}$	$39\Omega/0.25W$ , 3 in parallel
Inductor	$L_1, L_{1d}$	40µH
Resistor	$R_{L1d}$	$33\Omega/0.25W$ , 3 in parallel
Capacitor	$C_2$	$680 nF / 100 V_{dc}$
Capacitor	$C_{2d}$	$10nF/100V_{dc}$
Resistor	$R_{2d}$	$18\Omega/0.25W$ , 6 in parallel

# 2.5 Simulation results

In this section the principle of operation and the control scheme are verified by using simulation software PSIM. The input phase current waveforms are shown in **Fig.2-12**. By applying the active damping control, the resonant current peaks occurring after the commutations of the diode bridge are reduced in amplitude as can be seen in Fig.2-12(a) and (b). The gain of the *HPF* (cf. Fig.2-10) for detecting the resonance is adjusted to 2 here. **Fig.2-13** shows the input current THD in dependence on the output power. The THD is 30% at the nominal output power, which is close to the THD of the theoretical 120° rectangular shape resulting in 31%. The improved THD can be maintained within the wide operating range.

**Fig.2-14** shows the output voltage  $U_o$  and the DC-link voltage  $U_c$ . It can be seen that the DC-link voltage is successfully controlled to the low value of  $70V_{dc}$  and the output voltage ripple is small due to the almost constant DC current. It should be noted that the capacitance of the output capacitor is only  $47\mu$ F which is the minimum value to have the ripple current capability of the rectifier. Output voltage of the conventional three-phase diode bridge rectifier (cf. Fig.2-1) under a heavy load is theoretically the average of the rectified three-phase input voltage as expressed by

$$U_O = \hat{u}_i \frac{3}{\pi} \tag{2-4}$$

neglecting the voltage drops of the power semiconductors and inductor. However, the output voltage under a light load is higher than (2-4). When no-load is supplied, the output capacitor is charged at peak of amplitude of the input line-to-line voltage. In the case of a rectifier employing the ESI, output voltage could also be of a similar characteristic. The output voltage dependency on the output power is investigated by numerical simulation (cf. **Fig.2-15**). The rectifier output voltage in the low output power range is higher compared to the high output power range. The output voltage is  $536V_{dc}$  at the nominal output power, which is identified to (2-4), and  $563V_{dc}$  at no load, which corresponds to the peak of the line-to-line mains voltage. It is noted that the voltage drops of the power semiconductors and the inductor are assumed in the simulation. Accordingly, it is verified that the output voltage characteristic of the rectifier using the ESI is similar to that of the conventional diode bridge rectifier.

The circuit operation within the half period of the mains frequency (the positive period of the phase a voltage) is shown in **Fig.2-16** and **Fig.2-17**. It is noted that the behaviour within another half period (the negative period of the phase a voltage) is identical to the shown operation if the mains voltage is ideal due to the rectification of the mains voltage. In order to clearly show the simulation results, only half period is illustrated here. From Fig.2-16(a) and (b), the principle of the operation is verified that

the DC-link capacitor is charged within the positive period of the ESI voltage and is discharged within the negative period. The high frequency current ripples flowing to the output capacitor  $C_0$  and the mains side filter capacitor  $C_r$  (cf. Fig.2-17(b) and (c)) are much lower than the ESI inductor current ripple (cf. Fig.2-17(a)). Therefore, it is confirmed that the load side filter attenuates the high frequency current ripple coupled from the ESI (noise origin) to the load and the mains side filter. The RMS value of the high frequency current ripple flowing to the ESI inductor is  $0.49A_{\rm rms}$  and reduced to  $0.14A_{\rm rms}$  in the output and mains side capacitors.



**Fig.2-12**: Simulated input current waveforms without active damping (**a**), with active damping (**b**) for the nominal operating condition.





Fig.2-13: Simulated input current THD in dependence on the output power.



**Fig.2-14**: Simulated output voltage  $U_O$  and DC-link voltage  $U_C$  waveforms at the nominal operating condition.



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Fig.2-15: Simulated output voltage  $U_0$  in dependence on the output power.



**Fig.2-16**: Simulated circuit operation of the ESI voltage (a) and the DC-link capacitor current (b) shown within the half period of the mains frequency.



**Fig.2-17**: Simulated circuit operation of the ESI inductor current (**a**), the output capacitor current (**b**), and the mains side filter capacitor current (**c**) shown within the half period of the mains frequency.

The simulation result of the differential mode filter performance is depicted in **Fig.2-18**. The expected simulation result shows that the designed filters for ESI can fulfil CISPR 22-class A limit. It is noted that the spectrum of the test receiver and the quasipeak value are calculated by the same procedure with [22].



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**Fig.2-18**: Expected differential mode filtering result with the designed filters at the nominal condition. Shown: CISPR 22 – Class A limit line; input signal spectrum for the test receiver and; calculated quasi-peak measurement values for the critical frequencies.

# 2.6 Experimental results

In this section the experimental results of the 5kW prototype at steady state, unbalance and distorted input voltages and dynamic operation are introduced. The photograph of the 5kW three-phase rectifier including ESI is shown in **Fig.2-19**. The prototype includes the complete rectifier system such as the three-phase diode bridge, the EMI filters, the output capacitors, a pre-charge circuit, the ESI, and the control and protection circuits. The overall size is  $10.5 \times 10.1 \times 6$ cm<sup>3</sup>, which has a high power density of 7.9kW/dm<sup>3</sup> and the weight is 560g.



**Fig.2-19**: Photograph of the complete 5kW rectifier prototype (includes ESI, diode bridge, output capacitor, EMI filters, control circuits, etc.). Power density: 7.9kW/dm<sup>3</sup>, size 10.5cm×10.1cm×6.0cm ( $4.1^{"}\times4.0^{"}\times2.6^{"}$ ), weight: 560g (19.8 ounces). (a): input and output terminal side, (b): ESI inductor and DC-link capacitor side.

The proposed rectifier employing the ESI is compared to the conventional rectifier (cf. Fig.2-1(a)) concerning the volume of the main parts in **Fig.2-20**. The passive inductor used in the conventional inductor is very bulky and occupies much of the space of the rectifier (86%). The volume of the ESI inductor is only 1.9% of the passive inductor. It is noted that the inductance of 10mH for the passive inductor is chosen from Fig.2-2. The increased inductance of more than 10mH causes further reduction of the THD. However, it would also cause a higher volume and does not have much influence on the THD and the power factor. Therefore, the inductance of 10mH is the sufficient value and 195J10 (10mH, 10A) manufactured by HAMMOND is selected here. In case of a 10mH passive inductor, the sixfold mains frequency current ripple is three times higher (cf. Fig.2-2(a) and Fig.2-12(b)) compared to the rectifier employing the ESI. Therefore, the number of parallel connections of the output capacitor must be increased in order to guarantee the ripple current capability. The total volume of the conventional rectifier is 973cm<sup>3</sup> whereas the proposed rectifier shows only 470cm<sup>3</sup>. Accordingly, the volume is reduced more than half (48%) by using the ESI.



Fig.2-20: Volume of the main parts in the rectifier using the ESI and the conventional diode rectifier.

### 2.6.1 Steady state operation

The measured input currents for the cases where active damping is turned off and turned on are shown in **Fig.2-21**. By applying the active damping, the resonances of the input current are clearly reduced (Fig.2-21(b)) as compared to the input current waveform without the active damping (Fig.2-21(a)). The experimental result shows that the input current waveforms are in close correspondence to the simulation results (cf. Fig.2-12). As shown in **Fig.2-22** the designed prototype can operate under light load condition.



**Fig.2-21**: Measured input current waveforms without active damping (**a**), with active damping (**b**) for the nominal operating condition.



**Fig.2-22**: Measured input current waveforms under light load condition at  $P_O = 1$ kW (**a**),  $P_O = 2$ kW (**b**),  $P_O = 3$ kW (**c**), and  $P_O = 4$ kW (**d**). Operating condition:  $U_{IN} = 400$ V<sub>rms</sub> / 50Hz, and  $f_S = 70$ kHz.

The measured THD and the power factor are depicted in **Fig.2-23** and **Fig.2-24**. It can be clearly seen that the THD and the power factor are improved in the wide operating range. The THD and the power factor at the nominal operating point are 28.4% and 0.958, which are close to those of a theoretical 120° rectangular shape resulting in 31.0% and 0.955 respectively. The measured THD is slightly lower than the theoretical rectangular THD because of the curve of the current shape (cf. Fig.2-21(b)). In **Fig.2-25**, the output voltage and the DC-link voltage are measured. The output voltage is  $532V_{dc}$  at the nominal output power, which is identical to the result of the theoretical equation for the passive rectifier (2-4) with assumption of the voltage drops on the power semiconductors. The DC-link voltage is successfully adjusted to  $70V_{dc}$ .

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**Fig.2-23**: Measured input current THD in dependence on output power and variation of input voltages showing  $460V_{rms}$ ,  $400V_{rms}$ , and  $340V_{rms}$ .



**Fig.2-24**: Measured power factor in dependence on the output power and variation of input voltages as Fig.2-23.

The output voltage characteristics in dependence on the output power are illustrated in **Fig.2-26**. The output voltage is increased in a low output power range, which is in correspondence with the simulation results (cf. Fig.2-15). The output voltage at no load is also identical to the peak of the line-to-line mains voltage. The DC-link voltage can be set and controlled at  $70V_{dc}$  (cf. Fig.2-25) and does not change so much depending on the output power as shown in **Fig.2-27**. The variation of the DC-link voltage change is less than 1V within the power range. Therefore, it is verified that the proposed control scheme is able to adjust and control the DC-link voltage.

The measured control signal  $v_m$  (see Fig.2-10) is shown in **Fig.2-28**. This shape is similar to the ESI voltage  $v_e$ . When  $v_e$  is positive,  $v_m$  is negative and a duty cycle of the MOSFETs is then lower. This means that the DC-link capacitor *C* is charged (cf. Fig.2-5(d)). On the other hand, the duty cycle is increased and *C* is discharged when  $v_m$  is positive and  $v_e$  is negative. The average value of  $v_m$  is almost zero, neglecting an offset to compensate a loss generated in *C*.



Fig.2-25: Measured DC-link voltage  $U_C$  and output voltage  $U_O$  waveforms at the nominal condition.



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**Fig.2-26**: Measured output voltage  $U_O$  in dependence on output power and variation of input voltages as Fig.2-23.



Output power (kW)

**Fig.2-27**: Measured DC-link voltage  $U_C$  in dependence on output power.



**Fig.2-28**: Measured control signal  $v_m$  at the nominal operating condition.

The system efficiency is depicted in **Fig.2-29**. It should be pointed out that the measured efficiency includes the losses consumed in the whole system of the rectifier, e.g. losses in the diode bridge, the output capacitor, the EMI filters, the control board, and the fan are included. This result shows that a high efficiency is maintained in the wide power range. The high efficiency of 98.3% at the nominal operating point ( $U_{IN}$  =400V<sub>rms</sub>/50Hz,  $P_O$  =5kW,  $f_S$ =70kHz) is obtained here.

The distribution of the losses in the whole system is shown in **Fig.2-30**. The switching losses are measured from the prototype and the losses of the other components are analytically calculated. The total loss of the whole system is 62.6W and each loss component in the ESI and the EMI filters is relatively lower compared to the loss of the diode bridge. The total loss in the ESI, which includes those of the MOSFETs, the Schottky diodes, the inductors, and DC-link capacitor, is 24.8W and approximately equal to the loss of the diode bridge. This calculation result clearly shows that the low losses are due to the use of low voltage components in the ESI.

**Fig.2-31** shows the EMI measurements. The proposed filtering concept is for differential mode filters and the prototype does not include any common mode filters. In order to evaluate the proposed filter, the measurements are taken by using the differential/common mode noise separator [23], which is able to separate a detected total conductive noise by LISN to differential and common mode noise measurements. It is verified that both differential mode and common mode noise are below CISPR Class–A limit. Accordingly, the proposed filtering concept is successfully designed and performed to fulfil the standard. The CM (common mode) noise is quite low even

when no common mode filter is employed, since a common mode current theoretically depends on voltage variation of power semiconductors coupled to GND via stray capacitances. However, the voltage variation in the ESI is much lower, which is only 70V neglecting any spike voltage, if compared to the active rectifiers resulting in the full or half output voltage variation (cf. Fig.2-2 to Fig.2-7). This would bring a reduction of volume and a low realization effort for a common mode filter.



**Fig.2-29**: Measured efficiency in dependence on output power and variation of input voltages as Fig.2-23.



Fig.2-30: Distribution of system losses at the nominal condition of 5kW.



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Fig.2-31: Measured quasi-peak EMI noises of differential mode (a) and common mode (b).

## 2.6.2 Comparisons between passive and active modes

The rectifier using ESI is a hybrid type, which is able to operate not only in an active mode but also in a passive mode. By maintaining the turn-on state of the MOSFETs, no current flows into the DC-link capacitor C (cf. Fig.2-6(b) and (d)). A current flowing to ESI is then not controlled and the rectifier operates in a passive mode, which is equivalent to the conventional diode rectifier (cf. Fig.2-1(a)) with a low inductance of the inductor L because an ESI can equivalently be divided to an inductive part as L and a resistive part as the power semiconductors. In this section, behaviour of the passive mode is introduced and compared to the performance of the active mode.

In **Fig.2-32**, the measurement of the input current at the passive mode is demonstrated. Then, the ESI does not operate with all the MOSFETs being always turned on. In this case, the DC-link voltage is almost zero and the current flows on  $T_1$  and  $D_2$  (cf. Fig.2-6(b)), and also  $D_1$  and  $T_2$  (cf. Fig.2-6(d)). It is verified that the system is able to operate at also a passive mode. However, the input current has a higher distortion compared to the active mode (cf. Fig.2-21(b)). The comparison of the input current harmonics is depicted in **Fig.2-33**. Each harmonic component is relatively lower if the ESI operates (the active mode). The THD and the power factor in dependence on the output power are shown in **Fig.2-34** and **Fig.2-35**. By operating the ESI, the THD and the power factor are greatly improved in the whole operating range. Especially, higher improvements are obtained around the low and middle power range. The THD at the nominal output power is then reduced from 41.6% to 28.4% and the power factor is improved from 0.923 to 0.958.

In **Fig.2-36**, the output voltage at the passive mode is shown. The comparison to the active mode (cf. Fig.2-25) makes us clearly understand that the output voltage ripple can be significantly reduced. The output voltage ripple is then reduced from  $81.1V_{pp}$  to  $14.1V_{pp}$ . This allows use of a much lower volume of output capacitor.

In active mode, the power transistors must be driven. Therefore switching losses are generated and the core loss in the inductor is increased because of a high frequency current ripple. Accordingly, the efficiency in the case of the active mode is reduced compared to the passive mode (cf. **Fig.2-37**). However, the reduction of the efficiency at the nominal output power is only 0.4%. It is also verified from Fig.2-30 that the critical increased loss components such as the switching losses and the loss in the inductors are relatively low. Therefore, the efficiency is not reduced so much when the ESI actively operates.



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Fig.2-32: Measured input current in case of passive mode at the nominal operating point.



Fig.2-33: Input current harmonics in cases of passive and active modes at the nominal operating point.





Output power (kW)

Fig.2-34: Measured input current THD in dependence on output power in cases of passive and active modes.



Fig.2-35: Measured power factor in dependence on output power in cases of passive and active modes.



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Fig.2-36: Measured output voltage  $U_o$  and DC-link voltage  $U_c$  in cases of passive mode at the nominal operating point.



Fig.2-37: Measured efficiency in dependence on output power in cases of active and passive modes.

### 2.6.3 Unbalanced and distorted input voltage behaviours

The rectifier has to be able to operate not only in an ideal condition but also in practical situations such as unbalanced and/or distorted input voltage, dynamic input voltage and load changes, and so on. In this section, unbalanced and distorted input voltage behaviours of the rectifier employing the ESI are demonstrated.

In Fig.2-38, measured input current behaviours in the cases of both passive and active modes under balanced and  $\pm 15\%$  unbalanced amplitudes of the phase b input voltage are shown. It is noted that the nominal input phase voltage of  $230V_{rms}$  is then input to the phase a and c. Therefore, the amplitude of the phase b is the only change here. By operating the ESI, the input currents are improved; nevertheless the input phase voltages are unbalanced as shown in Fig.2-38(d) to (f). The conducting period of the input current changes depending on the unbalanced input voltage. The low  $u_b$  results in the narrow period of  $i_b$  and the high  $u_b$  causes the wider period of  $i_b$ . A conducting period of input current theoretically depends on a relationship of each amplitude of the input phase voltages (cf. Fig.2-41). If each input phase voltage is balanced, the conducting period is 120° for all phases. However, input current can flow when the phase voltage is highest or lowest in all phases. Therefore, the conducting period of input current is not 120° if the input voltages are not balanced. It is noted that the unbalanced input voltage causes the output voltage variation as shown in Fig.2-39. The equation (2-4) is then not valid. The output power is also changed if the load resistor is constant.

**Fig.2-40** shows the input current harmonics at the unbalanced input voltage in the case of the passive and active modes. Although the unbalanced input voltage is supplied to the rectifier, the input current harmonics are reduced by operating the ESI, which can be clearly seen by comparing Fig.2-40(a) and (b). Since the input voltage is not balanced, odd 3N order ( $3^{rd}$ ,  $9^{th}$ ,  $15^{th}$  etc.) harmonics are additionally generated. Those odd 3N order harmonics cannot be attenuated because the ESI is not able to control the conducted phase angle of input currents. This is because the conducted phase angle depends only on the relationship of each input phase voltage. It can be seen from Fig.2-38 that the higher amplitude of the phase voltage causes the wider conducting period of the input current and the narrower conducting period of the other input currents. The ESI is able to control a current but cannot control the relative amplitudes of the input phase voltages. Therefore, there is no influence on the odd 3N order harmonics. The same feature is shown in the passive rectifiers (cf. Fig.2-1(a)).



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**Fig.2-38**: Measured input phase voltage  $u_b$  and input current  $i_b$  at unbalanced input voltage, passive mode (a) to (c), and active mode (d) to (f);  $u_b$  is 15% decreased (a) and (d), is balanced (b) and (e), and is 15% increased (c) and (f).



Unbalanced ratio of input voltage (%)

**Fig.2-39**: Measured output voltage at unbalanced input voltage. Amplitude of phase *b* voltage is unbalanced and the other phase voltages are constant at  $230V_{rms}$ .



**Fig.2-40:** Measured input current harmonics of passive mode (**a**) and active mode (**b**) at unbalanced input voltage as Fig.2-38.



**Fig.2-41**: Relationship of amplitudes of input voltages and phase angle of input currents in cases that  $u_b$  is lower (a), is balanced (b), and is higher (c) than the other input phase voltages.

The THD characteristics in dependence on the ratio of the unbalanced input voltage are illustrated in **Fig.2-42**. Here, the amplitude of the phase *b* voltage varies and the phase *a* and *c* voltages are constant. When  $u_b$  is higher than the other phase input voltages, the conducting period of  $i_b$  is increased and the THD is reduced. On the other hand, the lower input phase voltage of  $u_b$  brings the higher THD of  $i_b$  e.g. if  $v_a$  and  $v_c$  are lower, THD of  $i_a$  and  $i_c$  is higher. The THD of  $i_b$  is the most variable in this case and the variation of the THD change is 3.2% in the range of unbalanced ratio. The power factor is not much changed as shown in **Fig.2-43** because the average THD of all input phase currents are almost constant in dependence on the unbalanced input voltage ratio (cf. Fig.2-42).

In **Fig.2-44**, it is verified that the output voltage ripple is again reduced by operating the ESI when the unbalanced input voltage is supplied. In the case of the passive mode under the unbalanced input voltage, the higher output voltage ripples are demonstrated. The output voltage ripple dependence on the unbalanced input voltage ratio is illustrated in **Fig.2-45**. In the passive mode, the output voltage ripple is increased depending on the ratio of the unbalanced input voltage. However, the output voltage ripple is not increased so much in the active mode. Therefore, the ESI is able to compensate the influence of the unbalanced input voltage and keep the lower output voltage ripple. By operating the ESI, the output voltage variation is improved from 46.1V to 11.4V within the change of the unbalanced input voltage ratio.



Unbalance ratio of input voltage (%) **Fig.2-42**: Measured input current THD at unbalanced input voltage as Fig.2-38.



Unbalanced ratio of input voltage (%)

Fig.2-43: Power factor characteristic in dependence on unbalanced input voltage as Fig.2-38.



Fig.2-44: Measured output voltage ripples as Fig.2-38.


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**Fig.2-45:** Measured output voltage ripple characteristics in dependence on unbalanced input voltage ratio.

## 2.6.4 Distorted input voltage behaviour

In this section, distorted input voltage behaviours of the rectifier using the ESI are discussed. In **Fig.2-46**, the rectifier is operated in the passive mode and the distorted input voltage is then supplied. The  $3^{rd}$ ,  $5^{th}$ , and/or  $7^{th}$  harmonics are then included in the fundamental amplitude as shown in **Fig.2-47**. Furthermore, the waveforms in the cases of the active mode are shown in **Fig.2-48**. In those measurements, the output power is less than 4kW, e.g. 3.9kW for (a), 3.5kW for (b), and 3.6kW for (c) respectively because of the limited power supply of the functional power source that is used for the measurements here.

In the active mode, the input current distortion is clearly reduced also in the case of the distorted input voltages, which can be seen by comparing Fig.2-46 and Fig.2-48. The control signals  $v_m$  shown in Fig.2-48(g) to (i) change to keep the constant current flowing to the ESI. Therefore, the output voltage ripple is also reduced. However, the number of the pulses of the input current is increased in Fig.2-48(c). As described before, the ESI is not able to control a conducting phase angle of an input current. It depends on the relationship of each input phase voltage and is not related to the ESI current. In Fig.2-48(c),  $i_b$  does not flow when  $u_b$  is not highest or lowest in the all phase voltages. Accordingly,  $i_b$  is conducted depending on the amplitude of the input voltages. A similar behaviour is demonstrated in the passive mode (cf. Fig.2-46(c)).

#### LeCroy LeCroy eCro $u_{b}$ $u_b$ $u_b$ $i_b$ $i_h$ 100V/div, 7A/div, 2ms/div (a) 100V/div, 7A/div, 2ms/div (**b**) 100V/div, 7A/div, 2ms/div (c) LeCroy LeCroy LeCroy *U<sub>0</sub>*: 100V/div U<sub>0</sub>: 100V/div U<sub>0</sub>: 100V/div 2ms/div (**d**) 2ms/div (e) 2ms/div (f)

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**Fig.2-46:** Behaviors under passive mode in case that distorted input voltages are supplied as  $3^{rd}$  harmonic injection (**a**) and (**d**),  $3^{rd}$  and  $5^{th}$  harmonic injections (**b**) and (**e**), and  $3^{rd}$ ,  $5^{th}$ , and  $7^{th}$  harmonic injections (**c**) and (**f**).



**Fig.2-47**: The injected input voltage harmonics in the case of the distorted input voltage operation.  $3^{rd}$  (**a**),  $3^{rd}$  and  $5^{th}$  (**b**), and  $3^{rd}$ ,  $5^{th}$  and  $7^{th}$  (**c**) harmonics are included to fundamental amplitude.



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**Fig.2-48:** Behaviors under active mode in the case that distorted input voltages are supplied as  $3^{rd}$  harmonic injection (**a**), (**d**), and (**g**),  $3^{rd}$  and  $5^{th}$  harmonic injections (**b**), (**e**), and (**h**), and  $3^{rd}$ ,  $5^{th}$ , and  $7^{th}$  harmonic injections (**c**), (**f**) and (**i**).

The input current spectrums in the case that the distorted input voltages are supplied to the rectifier are shown in **Fig.2-49**. The input current harmonics are again reduced by operating the ESI at the distorted input voltages. The THD in the case of the passive mode is 50.5%, 69.8%, and 103.9% at the  $3^{rd}$  injection, the  $3^{rd}$  and  $5^{th}$  injections, and the  $3^{rd}$ ,  $5^{th}$ , and  $7^{th}$  injections respectively. In the active mode, the THD is greatly improved by 29.9%, 26.3%, and 56.8%.





**Fig.2-49:** Input current harmonics in the cases of passive mode (**a**) and active mode (**b**) at distorted input voltage as Fig.2-47.

## 2.6.5 Dynamic operation

The start-up and the shut-down behaviours of the ESI are given in **Fig.2-50**. Before the ESI start-up, the input voltage is already supplied, the load current is flowing and the control circuit is keeping the transistors turned on  $(U_C = 0V)$ . At the start-up, the control circuit then starts switching the MOSFETs and the DC-link voltage  $U_C$  changes from zero to  $70V_{dc}$  without any large overshoot (cf. Fig.2-50(a)). The waveforms of the input current  $i_a$  and the output voltage  $U_O$  are immediately improved

once  $U_C$  is charged. If no load is connected,  $U_C$  cannot be charged because no current flows in the ESI. Once the load current flows,  $U_C$  can be charged and the ESI is then able to operate.

Under no-load conditions, the DC-link capacitor voltage,  $U_c$ , can be charged up during a pre-charge operation if a large output capacitor  $C_o$  is employed (cf. Fig.10 in [19]) because the voltages on the capacitors C and  $C_o$  depend on a ratio of the capacitances. Under pre-charge operation both MOSFETs are turned off and then Cand  $C_o$  are connected in series as the equivalent circuit with a resistor to limit an inrush current. Consequently, the ESI can operate once  $U_c$  is charged. For the case that a large output capacitance is employed in  $C_o$ , when  $U_c$  reaches the nominal voltage, the control circuit must start to operate by turning on the MOSFETs in order to avoid an over voltage on the DC-link. During the ESI shut-down operation (cf. Fig.2-50(b)), the duty cycle of MOSFETs is gradually increased in order to prevent any step changes in the ESI current. Once  $U_c$  reduces to zero, the MOSFETs are permanently turned on so that the DC-link capacitor is bypassed. The system is then working in a passive mode.



**Fig.2-50**: Measured dynamic behaviours of input current  $i_a$ , DC-link voltage  $U_c$ , and output voltage  $U_0$  waveforms at start-up (**a**) and shut-down (**b**) at the nominal operating condition.

The dynamic operation during step load changes is shown in **Fig.2-51**. The load is changed from 3 to 100% of the nominal output power (cf. Fig.2-51(a)). The small oscillation of the DC-link voltage, which is approximately  $\pm 15V$ , occurs after the load condition is changed. However, the peak voltage is 82V which is below the rated voltage of the DC-link capacitor (100V) and settles within 25ms. When the load power is changed from 100 to 3% (cf. Fig.2-51(b)) no large overshoot or undershoot of the voltages occurs. Accordingly, it is verified that the ESI is able to operate under start-up, shut-down, and dynamically changing load conditions.



**Fig.2-51**: Measured dynamic behaviours of input current  $i_a$  and DC-link voltage  $U_c$ , and output voltage  $U_o$  at the changes from 3 to 100% (a) and from 100 to 3% (b) of the nominal output power.

In order to compare with the passive rectifier (cf. Fig.2-1(a)) at the load change, the simulation results are shown in **Fig.2-52** and **Fig.2-53** respectively. For the simulations, the passive inductor of L=10mH is selected to show the comparative THD and power factor (cf. Fig.2-2) to the rectifier using the ESI (THD: 28.4%, power factor: 0.958) and the capacitance of  $C_0=141\mu$ F (three times higher compared to the proposed rectifier system) is used to have the sufficient ripple current capability. As the results, the higher input current overshoot at the load change from 3 to 100% (cf. Fig.2-51 (a) and Fig.2-52(a)) and the higher output voltage oscillation after the load change (cf. Fig.2-51 (a) and Fig.2-52(b)) are present. Since the damping factor is smaller due to the large passive inductance, the output voltage does not settle down quickly. The higher output voltage overshoot also appears at the load change from 100 to 3% (cf. Fig.2-51 (b) and Fig.2-53(b)) because the higher energy stored in the passive inductor is transferred to the output capacitor. Accordingly, the ESI causes the lower input current and output voltage fluctuations at the load change.



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**Fig.2-52**: Simulation results of input current (a) and output voltage (b) of passive rectifiers (cf. Fig.2-1(a)) at load change. Simulation parameters: load change as Fig2-51(a), L=10mH, and  $C_0=141\mu$ F.



**Fig.2-53**: Simulation results of input current (a) and output voltage (b) of passive rectifiers (cf. Fig.2-1(a)) at load change. Simulation parameters: load change as Fig2-51(b), L=10mH, and  $C_0=141\mu$ F.

## 2.7 Conclusions

The practical realization and the behaviour of the rectifier using the ESI have been introduced in this section. The DC-link voltage control and active damping of the resonant currents have been proposed and verified by numerical simulations. A 5kW prototype, which has a high power density of 7.9kW/dm<sup>3</sup>, has been built and experimentally evaluated. The DC-link voltage is successfully controlled and resonances are reduced by the proposed control scheme. The high efficiency of 98.3% and the improved power factor of 0.956 as well as the improved THD of 28.4% at the nominal operating point are obtained with the prototype. Furthermore, the EMI filtering concept to effectively attenuate conductive noise with low voltage components have been presented and the performance is verified by simulation and experimental results. In addition, the unbalanced and distorted input voltage behaviours, the dynamic operation during start-up and shut-down, and the load steps are successfully demonstrated. In this thesis, it is verified that an ESI is able to behave as a passive inductor having a large inductance. Therefore, the volume of the passive rectifier can be greatly reduced without impairing the performance in any way.

# **Chapter 3**

# Hybrid 12-Pulse Line Interphase Transformer Boost-Type Rectifier

Until recently, five independent power sources, which are three hydraulic and two electric systems, are equipped in large category aircrafts [28]. More Electric Aircraft, which is a new and basic concept of utilizing electric power to drive aircraft subsystems, is widely recognized as the future trend in the aerospace industry. On future More Electric Aircraft, the conventional fly-by-wire hydraulic flight control surface (rudder, aileron, spoiler etc.) actuation, which is supplied from the centralized hydraulic generation and distribution systems, will be associated with electrically powered electro-hydrostatic actuators (EHA). This will allow elimination of one hydraulic system without impairing safety objectives because one hydraulic supply is replaced by two electrical systems and/or the power source redundancy is increased. Further advantages are higher flexibility in routing and weight and cost savings due to the reduction of the total number of hydraulic generation and distribution components as well as higher efficiency and less maintenance.

The hydraulic power of the EHAs is generated locally by dedicated hydraulic pumps which are driven by variable speed electric motors being fed by an inverter from a DC link voltage as shown in **Fig.3-1** [29]. In order to prevent distortion of the supply voltage and/or interference with sensitive avionics equipment, rectifier concepts with low effects on the mains have to be employed. There, (currently) only unidirectional

power conversion is required; energy which is fed from the loaded surface back into the DC link is dissipated in a resistive dump circuit (cf. Fig.3 in [30]). In order to reduce weight and cost of aircraft, the electric generator is simplified by eliminating the gearbox to ensure constant frequency output in modern aircrafts. Accordingly, network frequency is not constant (360 - 800Hz) and dependent on the condition of the engine speed.



Fig.3-1: Electronic power system in an aircraft.

On the other hand, a micro gas turbine was developed for military objectives and the generator concept is now attractive for cogeneration systems due to an improvement of total system efficiency, i.e. a heat energy generated in a process can be converted to an electrical energy by a micro gas turbine system. In micro gas turbine systems, a rectifier and an inverter are used (cf. **Fig.3-2**) in order to achieve a frequency conversion from a generated frequency to 50Hz or 60Hz. The generated frequency and voltage, which are dependent on the rotation speed of the micro gas turbine, have to be converted to a constant DC voltage by an active rectifier in order to obtain a constant AC voltage connected to a grid. Normally, six IGBTs are employed in the active rectifier. However, the generated frequency from micro gas turbines is high (500Hz to several kHz) and therefore it is not easy to realize a high mains quality and/or high conversion efficiency due to the limitation of switching frequency and switching speed of IGBTs.



Fig.3-2: Typical micro gas turbine generation system.

In this section, drawbacks of passive rectifiers concerning a variation of the output voltage and a non-sinusoidal input current like a staircase waveform are introduced. Furthermore, novel hybrid line interphase 12-pulse rectifiers, which can compensate the drawbacks, are proposed. Moreover, the principle of operation and the system dimensioning are introduced. Different control strategies are also proposed and analyzed by the numerical simulations and the experimental results.

## 3.1 Conventional 12-pulse rectifiers

Several passive rectifier concepts which comprise isolated and/or non-isolated phase shifting transformers, diodes, and inductors have been proposed in the literature [1]. The passive rectifiers are advantageous in respect of high efficiency, low complexity, low EMC, and high reliability. Furthermore, for high input frequency applications like aircraft and micro gas turbine systems, magnetic components such as transformers and inductors in the passive rectifiers have only a low volume and a low weight. Moreover, low-order input current harmonics of the passive rectifiers can be eliminated e.g. 5<sup>th</sup> and 7<sup>th</sup> harmonics in the case of 12-pulse rectifiers are cancelled, which cannot be achieved by diode bridge rectifiers employing AC and/or DC side inductor(s) (cf. Fig2-1). Accordingly, THD, power factor, and output voltage ripple are improved as compared to the diode bridge rectifiers.

The voltage-type rectifier proposed by Niermann [4], [5] shows the lowest VA rating of the phase shifting transformer, e.g. 13.4% for 12-pulse rectifier. This topology is an attractive candidate for aircrafts due to a low volume and weight. **Fig.3-3** shows the conventional voltage-type 12-pulse rectifier using the Line Interphase Transformer (LIT) which is a non-isolated transformer. However, isolation between generator and load is not necessary in aircraft and micro gas turbine applications. Therefore, this research is focused on the voltage-type 12-pulse rectifier employing the LIT.



Fig.3-3: Conventional voltage-type 12-pulse LIT rectifier proposed by Niermann.

The principle of operation of the conventional voltage-type 12-pulse LIT rectifier is briefly described in the following. From the MMF relationship of the LIT, the turns ratio  $w_A$  and  $w_B$  of the windings and the currents flowing to the diode bridges  $i_{1a}$  and  $i_{2a}$  can be expressed as

$$(w_A + w_B)i_{1a} - w_A i_{2a} = w_B i_b \tag{3-1}.$$

For 12-pulse operation, the phase shift between  $i_{1a}$  and  $i_{2a}$  ( $i_{1b}$  and  $i_{2b}$ ,  $i_{1c}$  and  $i_{2c}$ ) should be 30° and equal portioning of input currents to diode bridges, i.e.  $|i_{1a}|=|i_{2a}|$ ,  $|i_{1b}|=|i_{2b}|$ , and  $|i_{1c}|=|i_{2c}|$  with ±15° phase angle with respect to input currents  $i_a$ ,  $i_b$ , and  $i_c$  are required as shown in **Fig.3-4**. From the geometrical relationship in Fig.3-4, the turns ratio is obtained by

$$w_A : w_A + w_B = 2 : \sqrt{3} + 1 \tag{3-2}$$

and results in

$$\frac{w_B}{w_A} = \frac{\sqrt{3} - 1}{2} = 0.366\tag{3-3}$$

The relationship between  $|i_{1a}| (=|i_{2a}|)$  and  $|i_a|$  can be also solved from Fig.3-4 as

$$|i_{1a}| = |i_{2a}| = \frac{|i_a|}{2\cos 15^\circ} = 0.5176 |i_a|$$
 (3-4).

The simulation result is depicted in **Fig.3-5**. The phase angle of the voltage between the neutral point of the output, *C*, and each input to the diode bridges, e.g.  $u_{1aC}$ ,  $u_{1bC}$ ,  $u_{1cC}$ ,  $u_{2aC}$ ,  $u_{2bC}$ , and  $u_{2cC}$ , depend on current conductions to the corresponding diodes. Since the phase angle between  $i_{1a}$  and  $i_{2a}$  is 30°, the phase angle of voltage  $u_{2aC}$  is also 30° delayed compared to  $u_{1aC}$ . The LIT voltage  $u_{1a2a}$  is then given by

$$u_{1a2a} = u_{1aC} - u_{2aC} \tag{3-5}$$

and results in the amplitude of 2*E* with the wide interval 30° which is equal to the phase difference between  $i_{1a}$  and  $i_{2a}$ . Furthermore, the voltage between *C* and *a*' is shown as

$$u_{a'C} = u_{1aC} - \frac{w_A + w_B}{2w_A + w_B} u_{1a2a} - \frac{w_B}{2w_A + w_B} u_{1c2c}$$
(3-6)

and common voltage between C and N is given from

$$u_{NC} = \frac{1}{3} (u_{a'C} - u_{b'C} - u_{c'C})$$
(3-7)

Finally, the LIT input voltage is obtained by

$$u_{a'N} = u_{a'C} - u_{NC} \tag{3-8}$$

and results in a 12-pulse staircase shape as can be seen in Fig.3-5(d). Therefore, input currents are also improved to 12-pulse shapes and the THD and an output voltage ripple can be reduced.

On the other hand, the amplitude of fundamental voltage of  $u_{a'N}$  is expressed using

$$\hat{u}_{a'Nf} = \frac{4}{3} E \frac{\sin(180^{\circ}/p)}{\pi/p} \sin \omega t = \hat{u}_a$$
(3-9)

where  $\hat{u}_a$  is the amplitude of the mains phase voltage and p (=12) is the number of steps of the staircase waveform. Amplitudes of  $\hat{u}_{a'Nf}$  and  $\hat{u}_a$  should be equal if no load is assumed (no voltage drop on the input inductor). Accordingly, the output voltage results in

$$U_o = 2E = \hat{u}_a \frac{3\pi/p}{2\sin(180^\circ/p)} = 1.5176\hat{u}_a$$
(3-10)

where voltage drops on diodes, inductors are neglected and ideal coupling of the LIT is assumed here.



Fig.3-4: Relationship of current vectors of the 12-pulse LIT rectifier.

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**Fig.3-5**: Time behaviours of the conventional 12-pulse line interphase transformer (voltage-type passive) rectifier.

The drawbacks of the passive rectifier concerning variation of output voltage and staircase input current shapes are verified by a 10kW prototype for aircraft applications [15]. From **Fig.3-6**, the output voltage is quite dependent on the output power, the input frequency, and the input voltage. This is caused by varying input voltage (cf. (3-10)), voltage drops across inductors, diodes, and LIT. Passive rectifiers cannot compensate the variation of output voltage due to lack of controllability.

**Fig.3-7** shows the input current waveforms and the corresponding harmonics. The typical 12-pulse staircase input current waveforms, which have better quality if compared to the diode bridge rectifiers, are obtained. However, the input currents are not sinusoidal compared to active rectifiers. Although, the  $5^{th}$  and  $7^{th}$  harmonics can be eliminated, the  $11^{th}$ ,  $13^{th}$ , and higher harmonics still remain in the input currents due to the 12-pulse property. In this section, the passive voltage-type rectifier is extended and the drawbacks are overcome.



**Fig.3-6**: The output voltage dependency on output power, input voltage, and input frequency of the conventional 12-pulse LIT rectifier.



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**Fig.3-7**: Input current waveforms (**a**) and normalized input current harmonics (**b**) of the conventional passive (voltage-type) 12-pulse LIT rectifier. Operating condition: Input voltage  $U_N$ =115V<sub>rms</sub> / 400Hz and output power  $P_O$ =10kW.

# 3.2 Novel hybrid 12-pulse rectifiers

Controlled output voltage and sinusoidal input currents can be achieved by active rectifiers. However, active rectifiers need a large number of power semiconductors and gate drivers, and a complex controller. In order to realize controllability of output voltage and an improvement of input current harmonics with a low effort, the novel hybrid rectifier topologies, i.e. the single-switch topology and the two-switch topology, are proposed in this thesis. Those topologies are shown in **Fig.3-8** and **Fig.3-9** respectively. The proposed circuits are able to control the output voltage by adding a minimum number of active components and a very simple control circuit. Due to the simplicity of the approach, the main advantages of the passive system, i.e. a low complexity and a high reliability are still given. Input current waveforms would also be improved by a sufficient modulation of the active switches.

In Fig.3-8, a single-switch boost converter is integrated into the conventional 12-pulse passive rectifier. The boost stage is composed of only a power transistor  $T_1$  and a first recovery diode  $D_1$ . Furthermore, the single-switch topology can forward power to load even if  $T_1$  is permanently turn-off. Accordingly, the single-switch topology has a low realization effort and a high reliability. The output voltage of the system can be derived as

$$U_o = \frac{1.5176\hat{u}_a}{1 - D_{u1}} \tag{3-11}$$

where  $D_{u1}$  denotes the duty cycle for the power transistor  $T_1$ . It is noted that voltage drops on inductors, power semiconductors, and LIT are neglected here. The rectifier is then able to control the output voltage to a constant value by adjusting the duty cycle  $D_{u1}$ .

The main circuit configuration of the two-switch topology (cf. Fig.3-9) includes two boost converters which are connected to each output of the diode bridges. The power transistors  $T_1$  and  $T_2$  can be operated in an interleaved manner in order to reduce switching frequency current ripple. Since only two active switches are employed, a low realization effort is still given. The output voltage  $U_0$  of the system can be obtained in analogy to (3-11) as

$$U_o = \frac{1.5176\hat{u}_a}{1 - D_{u2}} \tag{3-12}$$

where  $D_{u2}$  is a constant duty cycle for  $T_1$  and  $T_2$ .



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**Fig.3-8**: Main circuit configuration of single-switch topology which includes single-switch boost stage into the conventional passive (voltage-type) 12-pulse LIT rectifier.



**Fig.3-9**: Main circuit configuration of two-switch topology which includes two-switch boost stage into the conventional passive (voltage-type) 12-pulse LIT rectifier.

# 3.3. Principle of operation

## 3.3.1 Single-switch topology

The theoretical voltage operation of the single-switch topology (cf. Fig.3-8) is depicted in **Fig.3-10**. It is noted that voltage drops on semiconductors and inductors are neglected and ideal transformers are assumed. When  $i_{1a}$  and  $i_{2a}$  are positive and  $T_1$  is turned-on, the voltages  $u_{1aC}$  and  $u_{2aC}$  are clamped at -E, even though the upper diode is conductive. 1*a* and 2*a* are then conducted to the negative side via the diode bridges and  $T_1$ . On the other hand, 1*a* and 2*a* are conducted via the diode bridges and  $D_1$  during turn-off period of  $T_1$ . Then  $u_{1aC}$  and  $u_{2aC}$  are clamped at -E despite of the switching state of  $T_1$  because 1*a* and 2*a* are always conducted to the negative side. The voltages shown in Fig.3-10 can be calculated by the same equations (cf. (3-5) to (3-10)) for the conventional passive 12-pulse LIT rectifier. Accordingly, the voltages  $u_a N$  exhibit the typical shapes of a passive 12-pulse rectifier (cf. Fig.3-10(e)) but with chopping at switching frequency.

## 3.3.2 Two-switch topology

In **Fig.3-11**, calculated time behaviours of voltages in case of the two-switch topology (cf. Fig.3-9) are shown. The calculation has been done in the same way as for the single-switch topology (cf. Fig.3-8). In the two-switch topology,  $T_1$  and  $T_2$  can be operated in an interleaved manner in order to reduce switching frequency current ripple. The voltages  $u_{1aC}$  and  $u_{2aC}$  are dependent on the switching states of  $T_1$  and  $T_2$  respectively as in the behaviours of the single-switch topology when  $i_{1a}$  and  $i_{2a}$  are positive (cf. Fig.3-10(a)-(c)). Since the phase angle of control signals for  $T_1$  and  $T_2$  are 180° shifted to each other,  $u_{1a2a}$  cannot be cancelled in the period from  $\pi/6$  to  $\pi$  (cf. Fig.3-10(d) and Fig.3-11(d)). This would cause a higher iron loss in LIT compared to the single-switch topology. However, the LIT input voltage  $u_{aN}$  changes with double switching frequency and does not reach zero in every turn-on period of  $T_1$  and  $T_2$ . Accordingly, the amplitude of the inductor voltage  $u_{aa'}$ , which is the difference between  $u_{aN}$  and  $u_{aN}$ , is much smaller compared to the single-switch topology (Fig.3-10(f) and Fig.3-11(f)). Therefore, switching frequency input current ripple and/or switching frequency could be reduced.

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**Fig.3-10**: Calculated time behaviours of gate signal for  $T_1$  (**a**), voltages  $u_{1aC}$  (**b**),  $u_{2aC}$  (**c**),  $u_{1a2a}$  (**d**),  $u_{aN}$  and  $u_{aN}$  (**e**), and  $u_{aa'}$  and  $u_{aN}$  (**f**) of the single-switch topology (cf. Fig.3-8).



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Fig.3-11: Calculated time behaviours of the two-switch topology (cf. Fig.3-9) as Fig.3-10.

## **3.4** Purely sinusoidal input current control theory

A remaining disadvantage of the proposed hybrid rectifiers compared to active rectifiers is a staircase input current shape resulting in low-order harmonics which cannot be eliminated by input EMI filters. Several topologies which can improve input current quality have been proposed for current-type passive rectifiers [9]-[13]. However, no solution for voltage-type systems, which show the lowest VA rating of LIT, has been proposed so far. For the voltage-type rectifier, input currents could be controlled to a sinusoidal shape by a voltage injection to the diode bridge outputs, i.e. a voltage injection might be required for the voltage-type rectifiers as well as a current injection for the current-type rectifiers. In this section, the modulation functions to achieve a purely sinusoidal input current are derived and a novel space vector control scheme is proposed.

## 3.4.1 Derivation of modulation function

The modulation functions of the diode bridge output voltages for achieving a purely sinusoidal input current are derived in the following. For the passive rectifier operating a continuous input current shape and a constant output voltage  $U_0$ , LIT input voltages  $u_a N$ ,  $u_b N$ ,  $u_c N$  exhibit a staircase shape. There, the different voltage levels are directly determined by  $U_0$  and the LIT turns ratios (cf. (3-3)). In the two-switch topology (cf. Fig.3-9), the local voltage of the diode bridge outputs can be independently modulated by a control signal for the switches, e.g. the diode bridge output voltage is zero at the turn-on state of the switch and  $U_0$  at the turn-off state and therefore an average of the diode bridge output voltage in a switching cycle can be controlled by a modulation of the corresponding switch. Accordingly, realization of the modulation to achieve a sinusoidal input current could be possible by suitable switching patterns.

There, a novel control scheme for improving the input current quality and/or for lowering the amplitudes of low frequency current harmonics of the two-switch topology is presented. A purely sinusoidal LIT input voltage shape and/or a related space vector

$$\underline{u'} = \hat{u}'(\cos\varphi_N + j\cos\varphi_N) \tag{3-13}$$

 $(\varphi_N = \omega_N t, \text{ where } \omega_N \text{ is the mains angular frequency and } \varphi_N \text{ is the phase of the mains current space vector } \underline{i}_N)$  could be achieved in the average over a pulse period by proper modulation of diode bridge output voltages. This would result in a purely sinusoidal current drawn from the mains, i.e. if  $\underline{u}'$  can be a purely sinusoidal, input current is also a purely sinusoidal and low frequency harmonics would be eliminated.

For the calculation of the corresponding time behavior of the diode bridge output voltages, the considerations can be restricted to a 30°-wide interval (360°/12) of the mains period due to the 12-pulse property of the circuit, e.g. only  $\varphi_N = (+15^\circ, -15^\circ)$  is considered in the following. The (purely sinusoidal) mains current  $\underline{i}_N$  is split into two current space vectors  $\underline{i}_1$  and  $\underline{i}_2$  which are displaced in phase by  $\pm 15^\circ$  (with reference to  $\underline{i}_N$ ) and are occurring at the LIT outputs. Accordingly, we have for the input voltage space vectors of the diode bridges in the  $\varphi_N$  interval considered

$$\underline{u}_{1} = \frac{2}{3}u_{1}$$

$$\underline{u}_{2} = \frac{2}{3}u_{2}$$
(3-14)

 $(i_{1a} \text{ and } i_{2a}>0, i_{1b}, i_{2b}, i_{1c}, \text{ and } i_{2c}<0)$  where  $u_1$  and  $u_2$  are denominating the local average values of the diode bridge output voltages. This results in a LIT input voltage space vector

$$\underline{u'} = \underline{u}_2 - (\underline{u}_2 - \underline{u}_1)(\frac{w_A}{2w_A + w_B}) + \underline{u}_{wB}$$
(3-15)

corresponding to (3-6).  $\underline{u}_{wB}$  denotes the space vector of the voltage occurring across the windings  $w_B$  which is related to the voltage difference ( $\underline{u}_2 - \underline{u}_1$ ) being present across  $w_A$  and  $w_{A+B}$  by

$$\underline{u}_{wB} = (\underline{u}_2 - \underline{u}_1)(\frac{w_B}{2w_A + w_B})e^{-j\frac{2\pi}{3}}$$
(3-16).

There, the cyclic changing of the phases has been considered by a phase shift of  $-120^{\circ}$ . Combining (3-13)-(3-16) results in

$$u_{1} = \frac{3}{2}\hat{u}'(\cos\varphi_{N} + (2 + \sqrt{3})\sin\varphi_{N}) = \alpha\hat{u}'$$

$$u_{2} = \frac{3}{2}\hat{u}'(\cos\varphi_{N} - (2 + \sqrt{3})\sin\varphi_{N}) = \beta\hat{u}'$$
(3-17).

 $u_1$  and  $u_2$  are depicted in **Fig.3-12** by using the coefficients  $\alpha$  and  $\beta$  (see the full lines). As can be seen from a graphical representations of  $u_1$  and  $u_2$  and/or from the calculations of  $u_{1,\varphi N=-15^\circ}=u_{2,\varphi N=+15^\circ}=0$ ,  $u_{2,\varphi N=0^\circ}=u_{1,\varphi N=0^\circ}=1.5\hat{u}$ , and  $u_{1,\varphi N=+15^\circ}=u_{2,\varphi N=-15^\circ}=2.9\hat{u}$ ,  $u_1$  and  $u_2$  can be linearly approximated (see the dashed lines) to

$$u_{1} = 3\hat{u}'\left(\frac{1}{2} + \frac{6}{\pi}\varphi_{N}\right)$$

$$u_{2} = 3\hat{u}'\left(\frac{1}{2} - \frac{6}{\pi}\varphi_{N}\right)$$
(3-18).

As shown in Fig.3-12,  $u_1$  and  $u_2$  in the period -45° to -15°, 15° to 45°, and in the other 30°-wide intervals should be symmetric to  $u_1$  and  $u_2$  shown in -15° to 15° due to the

12-pulse property. Accordingly, the modulation voltages  $u_1$  and  $u_2$  form the triangular shapes.



**Fig.3-12**: The voltage modulations at diode bridge outputs in order to achieve purely sinusoidal input currents. Full lines are calculated by the equation (3-17) and dashed lines are approximated by (3-18).

The calculated results of the voltage modulation over the mains period as in Fig.3-5 are shown in **Fig.3-13** where  $\hat{u} \approx \hat{u}_{aN}$ , ideal coupling of LIT,  $2E=U_0\approx 3\hat{u}_a$  corresponding to the global average value  $D_{avg}=0.5$  of the duty cycle for  $T_1$  and  $T_2$  are assumed. The result shows that a purely sinusoidal LIT input voltage  $u_{aN}$  (= $\hat{u}$ ) can be obtained by the optimum voltage modulation (cf. Fig.3-13(a)). Consequently, a staircase input current of the voltage-type 12-pulse LIT rectifier can be improved to a purely sinusoidal shape by voltage modulation at diode bridge outputs (cf. (3-17)). The triangular modulation, which is the linear approximation obtained by (3-18), results in the almost sinusoidal voltage shape on  $u_{aN}$  (cf. Fig.3-13(b)) and would cause a high input current quality. Therefore, the triangular modulation could be another option to improve input current harmonics because the control signals for the triangular modulation can be easily generated by a simple controller, e.g. an analog control circuit.

As a high (or low) duty cycle of  $T_1$  and  $T_2$  results in a low (or high) local average voltage at the diode bridge outputs, duty cycles  $d_1$  for  $T_1$  and  $d_2$  for  $T_2$  are respectively expressed as

$$d_{1} = 1 - \frac{u_{1}}{U_{O}}$$

$$d_{2} = 1 - \frac{u_{2}}{U_{O}}$$
(3-19)
initial in Fig. 3.14

and depicted in Fig.3-14.



**Fig.3-13**: Calculated time behaviors of voltages of the voltage-type 12-pulse LIT rectifier (twoswitch topology (cf. Fig.3-9)) operated by the optimum modulation according to the equation (3-17) to achieve a purely sinusoidal input current (**a**) and the triangular modulation (linear approximation) according to the equation (3-18) (**b**).



**Fig.3-14**: The calculated time behaviors of duty cycle for  $T_1$  and  $T_2$  in order to achieve a purely sinusoidal input current. Full lines shows the optimum modulation calculated by the equation (3-17) and (3-19) and dashed line shows the triangular modulation (linear approximation) calculated by (3-18) and (3-19).

## 3.4.2 Space vector control

In the previous section, the modulation functions to achieve a purely sinusoidal input current are derived. However, the modulation functions are assumed for an ideal condition and non-ideal conditions such as unbalanced and/or distorted mains voltages, which would cause a distorted input current, are not considered. A closed loop control would be applied to the two-switch topology (cf. Fig.3-9) and ensure a purely sinusoidal input current even in non-ideal cases. In this section, the closed loop control based on a space vector theory is described [31].

Due to the 30° phase shift of the splitting currents ( $i_{1a}$  and  $i_{2a}$ ,  $i_{1b}$  and  $i_{2b}$ ,  $i_{1c}$  and  $i_{2c}$ ) to the two diode bridges, there are 12 different combinations of current signs, which are defining 12 sectors as shown in Fig.3-15. In each sector, four possible switching states are given: (00), (01), (10) and (11). In case of (11) both switches are turned on resulting in  $\underline{u}_1 = \underline{u}_2 = 0$ , and  $\underline{u}' = 0$  and in an increasing inductor current. In state (00), both switches are off and the rectifier behaves like a purely passive 12-pulse rectifier. In the two active states given by (01) ( $T_1$ : off,  $T_2$ : on) and (10) ( $T_1$ : on,  $T_2$ : off) where only one switch is turned on, the two space vectors  $\underline{u}'_{(01)}$  and  $\underline{u}'_{(10)}$ , which are rotated by  $\pm 15^{\circ}$  (= $\pm \pi/12$ ) with respect to vector  $\underline{u}'_{(00)}$ , can be formed (cf. **Fig.3-16**). By means of vectors  $\underline{u}'_{(00)}$ ,  $\underline{u}'_{(01)}$  and  $\underline{u}'_{(10)}$  any reference vectors in the diamond (cf. Fig.3-16) defined by the sum of voltage vectors  $\underline{u}'_{(10)}$  and  $\underline{u}'_{(01)}$  could be generated in time average over a switching pulse period. Accordingly, a possible state of the space vector is limited in the area. However, a purely sinusoidal LIT voltage, which results in a sinusoidal input current, can be generated within the imitated space vector. A reference voltage vector has to be calculated in order to achieve a closed loop control. The reference voltage vector is formed by geometrically adding the rectifier voltage space vectors

$$\underline{u}'^{*} = \delta_{(10)} \underline{u}'_{(10)} + \delta_{(11)} \underline{u}'_{(11)} + \delta_{(01)} \underline{u}'_{(01)}$$
(3-20)

weighted by the relative switching states  $j = (T_1; T_2)$ . These switching states can be calculated from simple geometrical considerations (cf. Fig.3-16).

From the purely sinusoidal modulation functions (3-17) and (3-19), the duty cycles for sector 0 results in

$$\delta_{(10)} = 1 - \frac{3}{2} \frac{\hat{u}'^*}{U_o} (\cos \varphi_N + (2 + \sqrt{3}) \sin \varphi_N)$$
  

$$\delta_{(01)} = 1 - \frac{3}{2} \frac{\hat{u}'^*}{U_o} (\cos \varphi_N - (2 + \sqrt{3}) \sin \varphi_N)$$
  

$$\delta^{(11)} = 3 \frac{\hat{u}'^*}{U_o} \cos \varphi_N - 1$$
(3-21).



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Fig.3-15: Sector definition in dependence on ideal diode bridge input currents



Fig.3-16: Space vector which can be generated from the two-switch topology.

Similar equations can be derived for the other sectors, i.e. the same equations are used in the even sectors and the modulation waveforms are symmetric in the odd sectors as shown in Fig.3-15. The linear approximations (the triangular modulation) can also be obtained from (3-18) and (3-19) and results in

$$\delta_{(10)} = 1 - \frac{3\hat{u}^{**}}{U_{O}} (\frac{1}{2} + \frac{6}{\pi} \varphi_{N})$$

$$\delta_{(01)} = 1 - \frac{3\hat{u}^{**}}{U_{O}} (\frac{1}{2} - \frac{6}{\pi} \varphi_{N})$$

$$\delta_{(11)} = \frac{3\hat{u}^{**}}{U_{O}} - 1$$
(3-22).

# 3.5 System dimensioning

System dimensioning for a practical realization of the passive 12-pulse rectifier and the hybrid 12-pulse rectifiers (the single-switch topology (cf. Fig.3-8) and the two-switch topology (cf. Fig.3-9)) are introduced in this section. First, the 12-pulse passive rectifier is designed and the detailed procedure is described. For the hybrid rectifier designs, the passive rectifier is expanded, i.e. passive components such LIT, input inductors, and diode bridges can be utilized in the hybrid 12-pulse rectifiers if an increased copper loss and iron loss caused by a high frequency switching is considered. Next, the additional components needed for the hybrid 12-pulse rectifiers, which are fast recovery diodes and power transistors, are selected. Temperature for the components of hybrid rectifiers will be increased compared to the passive rectifier due to additional losses. Therefore, cooling capability has to be considered in order to avoid an overtemperature of power semiconductors, LIT, and/or input inductor. For the rectifier system, the following parameters are assumed for the future More Electronic Aircraft applications.

Input phase voltage:	$U_N = 96 V_{rms} \dots 132 V_{rms}$
Input frequency:	$f_{IN} = 360$ Hz800Hz
Nominal input phase voltage:	$U_{N,Nom} = 115 \mathrm{V_{rms}}$
Nominal input frequency:	$f_{IN,Nom}$ =400Hz
Nominal output power:	$P_{O,Nom}=10\mathrm{kW}$
Maximum admissible current harmonics:	$I_{IN,(11)} \leq 0.1 I_{IN,(1)}$
	$I_{IN,(13)} \le 0.08 \ I_{IN,(1)}$

## 3.5.1 Passive rectifier

In the passive 12-pulse rectifier (passive mode:  $T_1$  and  $T_2$  are permanently turned off), 5<sup>th</sup> and 7<sup>th</sup> harmonics on the mains are eliminated. However, 11<sup>th</sup> and 13<sup>th</sup> harmonics are present. Therefore, the input inductor should be designed in order to fulfil the requirements of the maximum admissible current harmonics shown above, e.g. 11<sup>th</sup> and 13<sup>th</sup> harmonics must be less than 10% and 8% of the fundamental current respectively, within the whole operating range. Generally, the harmonics of the harmonics of the harmonics as shown in

$$\frac{\hat{u}_{a'N(n)}}{\hat{u}_{a'N(1)}} = \frac{1}{n} \qquad (\text{e.g. } n=11: 9.091\%, n=13: 7.692\%) \tag{3-23}.$$

The harmonic current flowing to the input inductors is given by

$$\hat{i}_{a(n)} \approx \frac{\hat{u}_{a(N(n))}}{n\omega L} \approx \frac{\hat{u}_{a(1)}\frac{1}{n}}{n\omega L} = \frac{1}{n^2} \frac{\hat{u}_{a(1)}}{\omega L}$$
(3-24).

According to (3-24), the coefficient of  $\hat{i}_{a(n)}$  defined as

$$k_{(n)} = \frac{1}{n^2} \tag{3-25}$$

which shows the proportional amplitude of input current harmonics, i.e.

$$k_{(11)} = \frac{1}{11^2} = 0.00826$$
 and  $k_{(13)} = \frac{1}{13^2} = 0.00592$  (3-26).

The relationship of amplitudes between  $k_{(11)}$  and  $k_{(13)}$  is

$$\frac{k_{(13)}}{k_{(11)}} = 0.717 < 0.8 \tag{3-27}.$$

Therefore, the system can fulfil the requirement of  $13^{\text{th}}$  and higher harmonics if  $11^{\text{th}}$  harmonic is less than  $0.1i_{a(1)}$ . Accordingly, the inductance of the input inductors should be decided in order to fulfil the requirement of the  $11^{\text{th}}$  harmonic.

In the case that the input voltage is the maximum and the input frequency is the minimum, the 11<sup>th</sup> harmonic of the input current shows a maximum over all operating conditions. The equation to solve the inductance can be obtained from (3-24) and results in

$$L = \frac{\hat{u}_{a(1),MAX}}{n^2 \cdot 2\pi \cdot f_{IN,MIN} \cdot \hat{i}_{a(11)}} = \frac{\hat{u}_{a(1),MAX}}{11^2 \cdot 2\pi \cdot f_{IN,MIN} \cdot 0.1 \hat{i}_{a(1)}}$$
(3-28)

where n=11 and the maximum admissible  $11^{\text{th}}$  current harmonics of  $I_{IN,(11)}=0.1I_{IN,(11)}$  are considered. In order to calculate the inductance, the amplitude of the fundamental input current  $\hat{i}_{a(1)}$  has to be known.

The unknown parameter of  $\hat{i}_{a(1)}$  can be solved by the following procedure. Generally, output power can be expressed as

$$P_{O} = \eta P_{IN} = \eta \frac{3}{2} \hat{u}_{a(1)} \hat{i}_{a(1)} \cos \varphi_{f} = \eta \frac{3}{2} \hat{u}_{a(1)} \hat{i}_{a(1)} \sqrt{1 - \sin^{2} \varphi_{f}}$$
(3-29).

On the other hand, the phase difference can be obtained from **Fig.3-17** and expressed as

$$\sin \varphi_f = 2\pi f_{IN} L \frac{\hat{i}_{a(1)}}{\hat{u}_{a(1)}}$$
(3-30).

(3-28) and (3-30) result in

$$\sin \varphi_f = \frac{1}{\left(11^2 \cdot 0.1\right)} \frac{\hat{i}_{a(1)}}{\hat{i}_{a(1)}} \frac{\hat{u}_{a(1),MAX}}{\hat{u}_{a(1)}} \frac{f_{IN}}{f_{IN,MIN}}$$
(3-31).

Moreover, (3-29) and (3-31) form

$$\left(\frac{P_O}{\frac{3}{2}\eta\hat{u}_{a(1)}}\right)^2 = \hat{i}_{a(1)}^2 \left[1 - \frac{1}{\left(11^2 \cdot 0.1\right)^2} \left(\frac{\hat{i}_{a(1)}}{\hat{i}_{a(1)}}\right)^2 \left(\frac{\hat{u}_{a(1),MAX}}{\hat{u}_{a(1)}}\right)^2 \left(\frac{f_{IN}}{f_{IN,MIN}}\right)^2\right]$$
(3-32).

By substituting  $\hat{u}_{a(1),MAX}$  and  $f_{IN,MIN}$  to  $\hat{u}_{a(1)}$  and  $f_{IN}$  in (3-32), it becomes

$$\left(\frac{P_O}{\frac{3}{2}\eta\hat{u}_{a(1),MAX}}\right)^2 = \hat{i}_{a(1)}^2 \left[1 - \frac{1}{\left(11^2 \cdot 0.1\right)^2}\right]$$
(3-33)

where  $\hat{u}_{a(1),MAX}$  and  $f_{IN,MIN}$  are the most critical operating point for the input current harmonics. Here,  $\hat{i}_{a(1)}$  can be given by

$$\hat{i}_{a(1)} = \frac{P_O}{\frac{3}{2}\eta \hat{u}_{a(1),MAX}} \frac{1}{\sqrt{1 - \frac{1}{\left(11^2 \cdot 0.1\right)^2}}}$$
(3-34).

Considering the efficiency to be  $\eta = 98\%$  at  $\hat{u}_{a(1),MAX}$ , the peak value of the fundamental input current  $\hat{i}_{a(1)}$  results in 36.5A where reduction of the power factor due to voltage drop on the input inductors is neglected. Now, the inductance of the input inductor can be calculated by (3-28) and results in 188µH.



**Fig.3-17**: Voltages of  $u_{aN}$  and  $u_{a'N}$  (**a**) and the phase angle (**b**).

Since the inductance is already decided, the amplitude of fundamental input current can be obtained. The equation at any operating point of  $\hat{u}_{a(1)}$  and  $f_{IN}$  is expressed from (3-29) and (3-30) as

$$-\left(\frac{P_O}{\frac{3}{2}\eta\hat{u}_{a(1)}}\right)^2 = \left(\frac{2\pi f_{IN} L}{\hat{u}_{a(1)}}\right)^2 \hat{i}_{a(1)}^4 - \hat{i}_{a(1)}^2$$
(3-35)

and results in

$$\hat{i}^{2}{}_{a(1)} = \frac{1}{2} \left( \frac{\hat{u}_{a(1)}}{2\pi f_{IN}L} \right)^{2} \pm \sqrt{\frac{1}{4} \left( \frac{\hat{u}_{a(1)}}{2\pi f_{IN}L} \right)^{2} - \left( \frac{P_{O}}{3\eta \pi f_{IN}L} \right)^{2}}$$
(3-36).

The voltage drop  $\hat{u}_{La}$  on the input inductor shown as  $\hat{u}_{La} = \omega L \hat{i}_{a(1)}$ 

(3-37)

causes a variation of the output voltage depending on  $f_{IN}$  and  $i_{a(1)}$ . Generally, output voltage can be obtain as

$$2E_d = 2E_{di}\cos\phi_f \tag{3-38}$$

where  $2E_{di}$  is output voltage at no load. Ideal conditions are assumed here, e.g. no leakage inductance and voltage drops on the diodes. The phase displacement factor  $\cos \phi_f$  can be obtained from (3-30) and expressed as

$$\cos\phi_f = \sqrt{1 - \sin^2 \phi_f} = \sqrt{1 - u_K^2}$$
 (3-39)

and

$$u_K = \sin \phi_f = 2\pi f_{IN} L \frac{\dot{i}_{a(1)}}{\dot{u}_{a(1)}}$$
(3-40).

Hence,  $u_K$  depends on  $\hat{i}_{a(1)}$  and  $f_{IN}$ . The varying  $u_K$  can be shown as

$$u_K = u_{K,Nom} \frac{\hat{t}_{a(1)}}{\hat{t}_{a(1),Nom}}$$
 (*f<sub>IN</sub>*: constant) (3-41),

$$u_K = u_{K,Nom} \frac{f_{IN}}{f_{IN,Nom}} \qquad (\hat{\imath}_{a(1)}: \text{ constant}) \qquad (3-42),$$

and

$$u_{K} = u_{K,Nom} \frac{\hat{i}_{a(1)}}{\hat{i}_{a(1),Nom}} \frac{f_{IN}}{f_{IN,Nom}} \qquad (\hat{i}_{a(1)} \text{ and } f_{IN} \text{: variable}) \qquad (3-43).$$

where  $u_{K,Nom}$  denotes  $u_K$  at nominal condition.

The percentage impedance of the input inductor at the nominal condition can be obtained by

$$\% Z = u_{K,Nom} \times 100 = \frac{2\pi f_{IN,Nom} L \hat{i}_{a(1),Nom}}{\hat{u}_{a(1),Nom}} \times 100$$
(3-44)

and results in 12.2%. Furthermore, the VA rating of the input inductor at nominal condition is expressed by

$$P_{DL} = 0.5 u_{K,Nom} P_{O,Nom}$$
(3-45).

Those results show that VA rating of the input inductor is 6.1% and 610VA.

In order to realize a compact volume of the input inductors, a three-limb core is selected with respect to the following values:

Current density	у;	$S_{eff} \leq 5.0 \text{ A/mm}^2$
Filling factor of	of the windings;	$k_W \approx 0.5$
Maximum flux	density;	$\hat{B} \leq 2.0T$ (TRAFOPERM N2, 0.1mm).
The input inductor is c	lesigned and realized	d as follows:
value	188µH,	

magnetic core	S3U 48b,
material	Trafoperm N2/0.1mm,
air gap	1.46mm,
number of turns	25.

Then, the maximum flux density is 1.2T (< 2.0T) at the highest amplitude of the input current 54.5A.

The LIT for the voltage-type 12-pulse rectifier must be composed of three singlephase cores or a five-limb core which have a zero-sequence flux path(s) in order to avoid zero sequence voltage [5]. The LIT should also have a small leakage inductance. Here, three single-phase cores are selected for the LIT. **Fig.3-18** shows a theoretical time behaviour of the LIT voltage  $u_{a1a2}$  corresponding to Fig.3-5(b) and variation of the magnetic flux  $\psi$ .



**Fig.3-18**: Time behavior of LIT voltage  $u_{1a2a}$  and the magnetic flux  $\psi$ .

The peak amplitude of the magnetic flux can be expressed by

$$\hat{\psi} = \frac{1}{2} \Delta \psi = \frac{1}{2} \int_{0}^{T/12} u_{1a2a} dt = \frac{2ET}{24}$$
(3-46)

where T is the mains period. The maximum magnetic flux is given in

$$\widehat{\psi}_{\max} = \frac{1.517 \widehat{u}_{aN,MAX}}{24 f_{IN,MAX}}$$
(3-47).

With consideration of the worst case at  $f_{IN,MIN}$ =360Hz and  $U_{N,MAX}$ =132V<sub>rms</sub>, the maximum magnetic flux results in 32.8mVs. The magnetic flux can also be expressed by

$$\hat{\psi} = \hat{B}A_E(2w_A + w_B) = \hat{B}A_Ew_A(2 + \frac{w_B}{w_A}) = 2.366w_A\hat{B}A_E$$
(3-48)

with peak amplitude of flux density  $\hat{B}$ , cross section area  $A_E$  of core, number of turn of  $w_A$ , and the turns ratio ( $w_B / w_A = 0.366$ ) of  $w_A$  and  $w_B$ .

On the other hand, the relationship between RMS voltage of  $u_{1a2a}$  denoting  $U_{\psi}$  and peak amplitude of magnetic flux  $\hat{\psi}$  for sinusoidal shapes (cf. **Fig.3-19**) can be shown by

$$\sqrt{2}U_{\psi} \int_{0}^{T/2} \sin\frac{2\pi}{T} t dt = 2\hat{\psi} , \qquad (3-49)$$

and solved as

$$U_{\psi} = \frac{\sqrt{2}\pi}{T}\hat{\psi}$$
(3-50).



Fig.3-19: Sinusoidal waveforms of LIT voltage and magnetic flux.

Then, VA rating of LIT can be obtained by a product of  $U_{\psi}$  and the RMS current  $I_W$  flowing in windings as shown in

$$P_{D,LIT} = 0.5m \frac{\sqrt{2\pi}}{T} \sum \hat{\psi}_{W} I_{W}$$
(3-51)

where m (=3) is the number of the phases. Accordingly, the VA rating of LIT can be solved by

$$P_{D,LIT} = 1.5 \frac{\sqrt{2\pi}}{T} \left( \hat{\psi} i_{a1,rms} + \frac{w_B}{2w_A + w_B} \hat{\psi} i_{a,rms} \right)$$
(3-52).

By substituting

$$\begin{cases} \hat{\psi}_{1a2a} = \frac{2E_d}{24}T \\ \frac{W_B}{W_A} = 0.366 \\ i_{a,rms} = \frac{i_{1a,rms}}{0.518} \\ i_{1a,rms} = \frac{I_O}{2 \times 0.955\sqrt{2}} \\ P_O = 2E_d I_O \end{cases}$$
(3-53),

the VA rating of LIT results in  $0.134P_O$  and shows only 13.4% of output power.

For minimizing core volume of the LIT, required total winding area  $A_W$  for  $2w_A+2w_B$  and cross section area  $A_E$  of core are required (cf. **Fig.3-20**). The necessary winding area is given by

$$A_W = \frac{A_{cu}N_t}{K_W} = \frac{I_W N_t}{S_{eff}K_W}$$
(3-54)

where  $I_W$  is RMS value of the current flowing to the windings as shown in **Fig.3-21** and  $N_t$  is total turns number of the windings. The sufficient value  $K_W \approx 0.5$  is assumed as a filling factor of the total winding for one phase. The winding area  $A_{cu}$  for one turn is defined as

$$A_{cu} = \frac{I_W}{S_{eff}} \tag{3-55}$$



Fig.3-20: Structure of LIT for one-phase.

The total winding area is obtained as



**Fig.3-21**: Windings and current distribution of LIT for one phase

$$A_{W,ges} = \frac{1}{S_{rms}k_W} \left[ \frac{0.5176\hat{i}_a}{\sqrt{2}} (w_A + w_B) + \frac{0.5176\hat{i}_a}{\sqrt{2}} w_A + \frac{\hat{i}_a}{\sqrt{2}} w_B \right]$$
$$= \frac{w_A\hat{i}_a}{S_{rms}k_W\sqrt{2}} \left[ 0.5176 \times (1 + \frac{w_B}{w_A}) + 0.5176 + 0.366 \right]$$
$$= \frac{1.125w_A\hat{i}_a}{S_{rms}k_W}$$
(3-56).  
From (3-48),  $A_F$  forms

$$A_E = \frac{\hat{\psi}}{2.366w_A \hat{B}} \tag{3-57}$$

The product of the winding area (3-56) and the core area (3-57) gives
$$A_E A_W = \frac{0.475 \hat{\psi} \, \hat{i}_a}{k_W \, S_{eff} \, \hat{B}}$$
(3-58).  
lowing values are assumed:

The fol

maximum amplitude of input current 54.5A:  $\hat{B} = 1.5 \text{ T};$ maximum magnetic flux density  $S_{eff} = 4.5 \,\text{A/mm}^2;$ maximum current density  $K_W = 0.5$ , filling factor and then (3-58) results in 25.2 cm<sup>4</sup>.

For optimization of core size, the core should be selected to fulfil the requirement  $(A_E A_W \ge 25.2 \text{ cm}^4)$ . The following core shows a sufficient value  $A_E A_W = 26.3 \text{ cm}^4$  $(A_W=5.85 \text{ cm}^2 \text{ and } A_E=4.5 \text{ cm}^2)$  and selected:

magnetic core	SM 65 ×2;
material	Trafoperm N2/0.1mm.

For the calculation of the number of turns, (3-56) can be used as

$$w_A = \frac{A_W k_W S_{eff}}{1.125\hat{i}_a}$$
(3-59).

According to the required winding ratio (cf. (3-3)), the numbers of the turns result in  $w_A=21$  and  $w_B=8$ .

In order to select sufficient diode bridges and avoid overtemperature with minimum volume of a heat sink, loss in the diode has to be estimated. For calculation of loss and junction temperature, average current and RMS current have to be known. The average current  $\bar{i}_{d,\max}$  flowing to the diode bridge output at worst case is calculated as

$$\bar{i}_{d,\max} = 0.5176\hat{i}_{a,\max} \frac{3}{\pi} = 0.494\hat{i}_{a,\max}$$
 (3-60)

where  $\hat{i}_{1a,\max} = \hat{i}_{2a,\max} = 0.5176\hat{i}_{a,\max}$  from (3-4) and a purely sinusoidal input currents flowing to the diode bridges are assumed. The maximum peak input current  $\hat{i}_{a(1) \text{ max}}$ within the whole operating range has to be considered. Then, the average current at worst case is delivered as  $\bar{i}_{d,\text{max}} = 26.9$  A with  $\hat{i}_{a,\text{max}} = 54.5$  A. Here, the average current flowing into a diode results in

$$_{d.avg} = 1/3 \,\overline{i}_{d,\max}$$
 (3-61).

 $I_{d.avg}$  can also be obtained by the other method. Average current flowing into one diode,  $i_{d.avg}$ , can be written by

$$i_{d,avg} = 0.5176\hat{i}_a \frac{1}{2\pi} \int_0^{\pi} \sin t dt = \frac{0.5176\hat{i}_a}{\pi}$$
(3-62).

On the other hand, the maximum RMS value of the diode current  $i_{d,rms,max}$  is then calculated as

$$i_{d,rms,\max} = 0.5176\hat{i}_{a,\max}\sqrt{\left(\frac{1}{2\pi}\int_{0}^{\pi}\sin^{2}tdt\right)} = \frac{0.5176\hat{i}_{a,\max}}{2}$$
(3-63)

where the maximum RMS current  $\hat{i}_{a,\max} = 54.5 A$  in the whole operating range should be considered.

The voltage stress on diode bridges is identical to the maximum output voltage as shown in

$$V_{D,max} = 1.5176\hat{u}_{aN,max} \tag{3-64}$$

(cf. (3-10). With the amplitude of the maximum input voltage  $\hat{u}_{aN,max} = \sqrt{2} \times 132 V_{rms}$ , the maximum voltage results in 284V. Therefore, a 600V diode is sufficient. It is noted that voltage drops on the magnet components and diodes are neglected here.

The three-phase diode bridge module VUE35-06N07 manufactured by IXYS is selected with the consideration of the following values in the data sheet. The diode module has advantages concerning compact size due to integrated six diodes in a package and isolation between case and junction.

$$I_{d,avg} = 56A @ T_{C} = 85^{\circ}C$$
  
 $U_{f,0} = 1.13V$   
 $r_{T} = 13 m\Omega$   
 $U_{max} = 600V$   
 $T_{j,max} = 150^{\circ}C$   
 $R_{th,i-c} = 1.9 \text{ K/W}$ 

The loss of one diode is generally given by the following equation

 $P_{V,D} = U_{f,0} \cdot i_{d,avg,max} + i^2_{d,rms,max} \cdot r_T$  (3-65) and results in 12.7W for each diode. The total loss of two diode bridges is then obtained by

 $P_{v,ges} = 12P_{V,D}$  (3-66)

and calculated as 152.4W. The temperature difference between the heat sink and the junction at the worst case is  $\Delta T_{j-c}=24^{\circ}C$  (=12.7W × 1.9K/W). For keeping lower temperature than the maximum absolute junction temperature  $T_{j,max}=150^{\circ}C$ , the junction temperature at the worst case is set at 140°C with 10°C margin. The temperature of the heat sink has to be less than

$$T_h = 140 - \Delta T_{j-c} = 116^{\circ} \text{C}$$
 (3-67).

The heat sink should also be selected with consideration of the maximum ambient temperature of  $T_a=50^{\circ}$ C. The thermal resistance between the heat sink and air is calculated by

$$R_{th,h-a} \leq (T_h - T_a) / P_{v,ges} \tag{3-68}$$

and results in  $R_{th,h-a} \leq 0.43 \text{ K/W}$ .

The prototype of the passive rectifier is shown in **Fig.3-22**. The overall size is 3740 (22 x 17 x 10) cm<sup>3</sup> and the weight is 4.4kg. Therefore, the prototype shows 2.67kW/cm<sup>3</sup> and 2.27kW/kg, which are comparable to the active rectifiers for the aircraft applications [15].



**Fig.3-22**: A 10kW prototype of the passive voltage-type 12-pulse rectifier. The overall dimensions:  $22 \times 17 \times 10$  cm<sup>3</sup>.

# 3.5.2 Hybrid rectifier

The designed input inductors, the LIT, and the selected diode bridges for the passive rectifier can be also useful for the hybrid rectifier. However, the losses in the magnet components, i.e. the input inductor and the LIT, are increased due to switching frequency current and voltage ripples. Furthermore, power transistors and fast recovery diodes must be selected and output capacitors must have a sufficient current capability for higher switching frequency current ripple.

In both hybrid rectifiers i.e. the single-switch topology (cf. Fig.3-8) and the two-switch topology (cf. Fig.3-9), LIT voltage varies with switching frequency as shown in **Fig.3-23**. The amplitude of magnetic flux in both systems is identical and calculated by

$$\hat{\psi} = \frac{1}{2} \Delta \psi = \frac{1}{2} \int U_O(1-D) dt = \frac{1}{24} U_O T(1-D)$$
(3-69)

where *D* is a duty cycle of the power transistors. Hence  $\hat{\psi}$  mainly depends on mains frequency. Therefore, a switching frequency magnetic flux ripple is neglected here. From the relationship between  $U_O$  (=2*E*) and *D* corresponding to (3-11) and (3-12),  $\hat{\psi}$ is also identical to the passive rectifier (cf. 2-46), i.e.  $\hat{\psi}$  is constant with increasing  $U_O$ and *D*. However,  $u_{1a2a}$  chops with switching frequency in the wide interval from  $\pi/6$  to



**Fig.3-23**: Time behaviors of LIT voltage  $u_{1a2a}$  and magnetic flux  $\psi$  in single-switch topology (cf. Fig.3-8) (a) and two-switch topology (cf. Fig.3-9) (b).

 $\pi$  (cf. Fig.3-23(b)) in the case of the two-switch topology, which causes a switching frequency magnetic flux ripple and additional core loss generated in LIT. Amplitude of magnetic flux ripple varying with switching frequency is expressed as

$$\widehat{\psi}_{sw} = \frac{1}{2} \Delta \psi_{sw} = \frac{1}{2} \int U_O D f_S dt = \frac{1}{2} U_O D f_S$$
(3-70).

It should be noted that the maximum magnetic flux occurs right after shut-down from a steady state operation, i.e. output voltage is boost without switching (D=0). Then, the maximum magnetic flux assumed by

$$\hat{\psi}_{\text{max}} = \frac{1}{24} U_0 T$$
 (with  $U_0 = 2E = \frac{1 - 1.5176\hat{u}_a}{D}$ ) (3-71)

is generated.

Due to increased losses of magnetic components, air forced cooling has to be employed not only for the power semiconductors but also for the magnetic components.

The boost stage of the hybrid rectifiers is designed here. The current stress of the power transistor  $T_1$  and the diode  $D_1$  in the single-switch topology (cf. Fig.3-8) is double if compared to the two-switch topology (cf. Fig.3-9) because both diode bridge output currents flow into  $T_1$  or  $D_1$  with an identical duty cycle to the two-switch topology (cf. Fig.3-12 and Fig.3-13). Therefore, double number of parallel connections for  $T_1$  and  $D_1$  is required in the single-switch topology so that the current stress is identical in both topologies. Accordingly, the number of components and losses for power transistor and fast recovery diode are equal in the both hybrid rectifiers. For reduction of the heat sink volume, the switching losses of the power semiconductors are evaluated. The dependence of the measured switching loss characteristics resulting for employing a CoolMOS (600V/47A, SPW47N60C3, Infineon) in combination with an ultra fast recovery diode (600V/30A, DSPEP 30-60BR, IXYS) is depicted in **Fig.3-24**. Accordingly, the power transistor switching losses can be calculated as

$$P_{S} = f_{S}(k_{1}i^{2}{}_{d,rms} + k_{2}i_{d,avg})$$
(3-72)

(cf. [32]) where  $i_{d,rms}$  and  $i_{d,avg}$  denote the RMS and the average values of the diode bridge output current. It is noted that equal current stress with the same number of components in both hybrid systems is assumed. It is also assumed that continuous sinusoidal currents flow into the diode bridge inputs. There, we have for  $i_{d,rms}$  and  $i_{d,avg}$ 

$$i_{d,rms} = \hat{i}_{1a} \sqrt{\frac{1}{\pi/3} \int_{\frac{1}{3}\pi}^{\frac{2}{3}\pi} \sin^2 t dt} = 0.956 \hat{i}_{1a}$$
(3-73)



Chapter 3 HYBRID 12-PULSE LINE INTERPHASE TRANSFORMER BOOST-TYPE RECTIFIER

**Fig.3-24**: Dependence of the switching losses of a CoolMOS power transistor (600V/47A, SPW47N60C3, Infineon) in combination with an ultra fast recovery diode (600V/30A, DSPEP 30-60BR, IXYS). Parameters: Switching voltage  $U_0=350V_{dc}$ , turn-on gate resistor  $R_{g(of)}=5\Omega$ , turn-off gate resistor  $R_{g(off)}=2.5\Omega$ . The switching losses were measured during actual system operation.

and

$$i_{d,avg} = \frac{\hat{i}_{1a}}{\pi/3} \int_{\frac{1}{3}\pi}^{\frac{2}{3}\pi} \sin t dt = 0.955 \hat{i}_{1a}$$
(3-74)

According to Fig.3-24, the switching losses are characterized for the transistor turn-on  $k_1=0.4943\mu\text{Ws/A}^2$ ,  $k_2=13.33\mu\text{Ws/A}$  and for the transistor turn-off  $k_1=0.6114\mu\text{Ws/A}^2$ ,  $k_2=1.469\mu\text{Ws/A}$ , and for the diode reverse recovery  $k_1=0.1486\mu\text{Ws/A}^2$  and  $k_2=4.789\mu\text{Ws/A}$  respectively.

The conduction losses of the power transistors and the diodes can be calculated as

$$P_{con,T1} = i^2 d_{,rms} R_{ON} D \tag{3-75}$$

and

$$P_{con,D1} = U_F i_{d,ave} (1 - D)$$
(3-76)

With reference to the data sheet we have the turn-on resistance for the CoolMOS  $R_{ON}=0.133\Omega$  and for the diode (DSPEP 30-60BR)  $U_F=1.75V$  at a junction temperature of 125°C. For the estimation of losses in the power semiconductor, switching frequency and duty cycle D corresponding to output voltage must be decided. In order to avoid any inrush current, the output voltage must be controlled to a higher value than  $1.5176 \hat{u}_{a,\text{max}}$  which corresponds to the theoretical maximum output voltage of the passive rectifier (cf. (3-10)). In this case, the output voltage is selected at  $U_O=350V_{dc}$  ( $\geq 283V=1.5176 \hat{u}_{a,\text{max}}$ ). The duty cycle to obtain the output voltage can be calculate by

$$D = 1 - \frac{1.5176\hat{u}_a}{U_o} \tag{3-77}$$

(cf. (3-11) and (3-12)) and results in  $D\approx0.3$  with the nominal input voltage  $U_N=115_{\rm rms}$ . The switching frequency should be sufficiently higher than the maximum mains frequency of 800Hz in order to achieve a high input current quality. The switching frequency can be calculated by

$$f_{S} \ge \frac{\hat{u}_{a}D}{0.2\hat{i}_{a}L} \tag{3-78}$$

so that the peak-to-peak value of the switching frequency current ripple is less than  $\pm 10\%$  of amplitude of the mains current ( $\hat{i}_a = 43$ A at the nominal operating point by assuming efficiency  $\eta=0.95$ ) in the case of the single-switch topology. Here, the switching frequency is set at 33kHz, which also realizes a sufficient number of switching pulses (41 pulses) in the minimum mains period (1/800Hz). It should be noted that switching frequency current ripple in the case of the two-switch topology is lower due to its interleaved manner and a low switching voltage ripple across the input inductor (cf. Fig.3-11(e) and (f)).

In order to design a heat sink with a high reliability, the worst case of all the operating points must be considered. The maximum RMS input current occurs at  $U_N=96V_{rms}$ ,  $f_{IN}=800$ Hz, and  $P_O=10$ kW where the efficiency is 90% considering the increased power losses and the phase displacement of fundamental mains current and the mains voltage ( $\cos\varphi=0.837$ ). The calculated maximum losses in the active part are listed in **TABLE 3-1**. There, the maximum temperature difference of the MOSFET junction and the case is  $\Delta T_{j-c}=34.8^{\circ}$ C and for the fast recovery diodes  $\Delta T_{j-c}=42.9^{\circ}$ C which is admissible for a heat sink temperature of  $82.1^{\circ}$ C (= $125^{\circ}$ C -  $42.9^{\circ}$ C) where the maximum junction temperature  $T_j=125^{\circ}$ C with  $25^{\circ}$ C margin is assumed. The required thermal resistance between the case and air should be less than 0.26K/W with consideration of the maximum ambient temperature  $50^{\circ}$ C. It is noted that loss in the

boost stage in the case of both hybrid rectifiers is theoretically equal because the voltage and current stress are identical.

**TABLE 3-1**: Losses in the boost stage of the hybrid rectifiers (single-switch and two-switch topologies) at the worst case i.e.  $U_N$ =96V<sub>rms</sub>,  $f_{IN}$ =800Hz,  $U_O$ =350V<sub>dc</sub>,  $P_O$ =10kW,  $f_P$ =33kHz.

MOSFET $T_1, T_2$		Conduction loss	67W	116W	
	$T_1, T_2$	Turn-on loss	30W		
		Turn-off loss	19W		
Diode $D_1, I$	ת ת	Conduction loss	29W	- 39W	
	$D_1, D_2$	Reverse recovery loss	10W		
Total loss in boost stage			310W		

In the case of passive rectifiers, current flowing to the magnetic components includes only low frequency components. However, switching frequency current ripple flows in the hybrid rectifiers. In **Fig.3-25**, the winding resistances of the input inductor and the LIT are calculated. The resistances are constant with frequency increase up to 10kHz and increased in the higher frequency rage due to skin effect and proximity effect. However, the resistances are not high at the switching frequency 33kHz because all windings are realized in thin copper foils. In the case of the two-switch topology, frequency of ripple current is double, e.g. 66kHz, the amplitude of the ripple current is nevertheless much lower. Therefore, the high frequency ripple current does not influence the copper losses in the magnetic components.



**Fig.3-25**: Calculated winding resistances of magnet components,  $R_{cu}(w_A)$ ,  $R_{cu}(w_B)$ , and  $R_{cu}(L)$  denote winding resistances of  $w_A$  and  $w_B$  of the LIT and the input inductor *L*.

On the other hand, the leakage inductance of the LIT can be estimated by

$$L_{S} = \left[ L_{A} \sqrt{L_{B} L_{AB}} (K_{AB,A} K_{A,B} - K_{AB,B}) - 2L_{B} \sqrt{L_{A}} (K_{A,B} K_{AB,B} - K_{AB,A}) + L_{AB} \sqrt{L_{B} L_{A}} (K_{A,B} - K_{AB,A} K_{AB,B}) + L_{AB} (L_{A} - K^{2}{}_{AB,B} L_{B} - K^{2}{}_{AB,A} L_{A} + L_{B}) + L_{A} L_{B} (1 - K^{2}{}_{A,B}) \right] / \left[ L_{A} + 2K_{AB,A} \sqrt{L_{A} L_{AB}} + L_{AB} \right]$$
(3-79)

where  $L_{\nu}$  denotes the magnetizing inductance and  $K_{\nu,\lambda}$  denotes the coupling coefficient between two respective windings. From the geometrical distances of the windings and (3-79), the leakage inductance results in  $L_S$ =20µH.  $L_S$  would help to reduce switching frequency current ripple if  $L_S$  would act as a series connection with the input inductor.

Since the two-switch topology has the advantages concerning a lower switching frequency current ripple and the possibility to realize a purely sinusoidal input current, this thesis is mainly focused on the two-switch topology (cf. Fig.3-9). In order to verify the principle of operation, a 10kVA prototype of the two-switch topology has been built. The main components are listed in **TABLE 3-2** and the 10kW laboratory prototype is shown in **Fig.3-26**. In the prototype, the diode bridges and the power semiconductors in the boost stage are connected to the PCB and mounted on the heat sink together. In order to avoid a high temperature of the magnetic components (the LIT and the input inductor), fans are employed for cooling not only the heat sink but also the magnetic components. An output capacitor having a sufficient ripple current capability is selected.

The power density of the hybrid prototype is 1.56kW/cm<sup>3</sup>, which is slightly reduced from the passive system due to the increased heat sink volume and the PCB. However, a high power density is still given. The power density could be increased if a five-limb core is employed for the LITs instead of three three-limb cores and the input inductors are integrated in the LIT as leakage inductances. This will be described in Section 4.

Component	Symbol	Туре
		Value: 188µH
Input inductors	L	Core: S3U 48b
		Material: Trafoperm N2/0.1mm
		$w_{A+B}$ : 29turns $w_A$ : 21 turns, $w_B$ : 8 turns
		Value: $L_{AB} = 5.2$ mH, $L_A = 2.5$ mH, $L_B = 0.35$ mH,
LIT	$Tr_{a}, Tr_{b}, Tr_{b}$	$L_S = 20 \mu H$
		Core: 2×SM 65
		Material: Trafoperm N2/0.1mm
Diode bridge		600V/56A, 2×VUE 35-06NO7, IXYS
MOSFET	$T_1, T_2$	600V/47A, SPW47N60C3, Infineon
Output diode	$D_1, D_2$	600V/30A, DSPEP 30-60BR, IXYS
Output capacitor	$C_O$	$2 \times 560 \mu F/400 V_{dc}$ , Rubycon

**TABLE 3-2**: List of components employed in the two-switch topology (cf. Fig.3-9).



**Fig.3-26**: A 10kW Prototype of the two-switch topology (cf. Fig.3-9); overall dimensions:  $24.0 \times 22.9 \times 11.7$  cm<sup>3</sup>

# 3.6 Control scheme

# 3.6.1 Single-switch topology

For the advantages concerning a lower switching frequency current ripple due to its interleaved manner and a realization for a purely sinusoidal input current, this thesis is focused on the two-switch topology (cf. Fig.3-9). In order to compare to the two-switch topology by numerical simulation, the control scheme of the single-switch topology (cf. Fig.3-8) is briefly introduced here. The control block diagram of the single-switch topology is depicted in **Fig.3-27**. The output voltage  $U_0$  is fed back and controlled by the PI-type controller to adjust to the reference value  $U_0^*$ . The output current of the diode bridges is detected as the voltage  $u_{R3}$  across the shunt resistor  $R_3$  (cf. Fig.3-8) and the average current control is achieved by the feedback control using the PI-type controller. Therefore, the controller protects against an overcurrent because an overcurrent causes an increased  $u_{R3}$  and a reduction of the duty cycle  $D_{u1}$ . The gate signal  $T_{g1}$  of the power transistor  $T_1$  is determined by intersecting zero and a subtraction of  $D_{u1}$  from the switching frequency triangular waveform  $T_{ri}$  swinging from zero to 100% of the duty cycle.



Fig.3-27: Control block diagram of the single switch topology (cf. Fig.3-8).

# 3.6.2 Two-switch topology

The basic control strategy for the two-switch topology (cf. Fig.3-9) is shown in **Fig.3-28**. The control method is similar to the single-switch topology (cf. Fig.3-27) except for the interleaved manner and the zero sequence current control. The gate signals  $T_{g1}$  for  $T_1$  and  $T_{g2}$  for  $T_2$  are determined by intersecting zero and a subtraction of  $D_{u2}$  from the switching frequency triangular waveforms  $T_{ri_1}$  and  $T_{ri_2}$  respectively. In order to realize the interleave manner, phase angles of  $T_{ri_1}$  and  $T_{ri_2}$  are 180° shifted to each other.

In the case of the two-switch topology, a slight difference in the duty cycles of  $T_1$  and  $T_2$  would result in a zero sequence current flowing between the two rectifier bridges via the LIT. Accordingly, the currents in the two partial systems would not be

balanced, which would cause higher current stresses on the power components and low frequency distortion on the mains. Therefore, a zero sequence current control ensuring equal current partitioning has to be employed in the two-switch rectifier. There, the simplest way is to directly measure the zero sequence current  $i_0$ , i.e. the sum of the input or output currents of diode bridges  $i_0=i_{1a}+i_{1b}+i_{1c}=-(i_{2a}+i_{2b}+i_{2c})$  or  $i_0 = i_{rec1} - i_{rn1} = i_{rec2} - i_{rn2}$ , using a through-hole current transducer and to adjust the duty cycles by negative feedback in order to eliminate  $i_0$ . Alternatively, a zero sequence current control (cf. Fig.3-28) based on a lower cost current measurement of  $i_0$  with shunt resistors  $R_1$  and  $R_2$  (cf. Fig.3-9) could be implemented. Corresponding key waveforms are depicted in **Fig.3-29**. When the voltages  $u_{R1}$  and  $u_{R2}$  across the shunt resistors  $R_1$  and  $R_2$  are identical within the turn-on period of  $T_1$ , no zero sequence current  $i_0$  is present in the system. On the contrary,  $i_0$  can be detected as a difference between  $u_{R1}$  and  $u_{R2}$ . In the control circuit as shown in Fig.3-28, the shunt voltages  $u_{R1}$ and  $u_{R2}$  are added in a period  $t_s$  which is generated from the gate signal  $T_{g1}$  (for  $T_1$ ) considering a delay time  $t_d$  in order to avoid detection of a large current peak resulting from the reverse recovery of diode  $D_1$ . For a positive average value of signal  $i_Z$ , a zero sequence current is flowing in  $T_1$  from drain to source and to the other diode bridge. In this case the control circuit reduces the duty cycle of  $T_1$  and increases the duty cycle of  $T_2$ , which results in a reduced zero sequence current. The controller has been built with analogous ICs and set on the same PCB for the power circuit.

**Remark**: As an alternative to providing a control loop, the occurrence of a zero sequence current  $i_0$  also can be prevented by two additional diodes  $D_3$  and  $D_4$  as shown



Zero sequent current control

Fig.3-28: Control block diagram comprising an interleave manner and a zero sequence current decoupling based on current measurement by shunt resistors for the two-switch topology (cf. Fig.3-9).

in **Fig.3-30** as Fig.1-4 [8]. By using the diodes, current measurement and the control circuit for  $i_0$  can be omitted. However, higher conduction losses will be generated in the system. Therefore, this concept has not been analyzed in more detail in this thesis.



**Fig.3-29**: Time behaviors of generated key waveforms by zero sequence current control corresponding to Fig.3-28.



**Fig.3-30**: Alternative circuit configuration of the two-switch topology (cf. Fig.3-9) in order to omit the zero sequence current control and zero sequence current measurement by adding diodes  $D_3$  and  $D_4$ .

# 3.6.3 Purely sinusoidal input current control (triangular modulation)

For achieving purely sinusoidal input currents, modulation for  $T_1$  and  $T_2$  is additionally required (cf. Fig.3-14). The control circuit diagram including triangular modulation is depicted in **Fig.3-31**. The optimum modulation shapes are very close to the triangular modulation shapes (the linear approximations) which allows a simple realization. Accordingly, the triangular modulation is used here. In order to generate the synchronized triangular modulation signal to mains frequency, an input voltage (e.g  $u_a$ ,  $u_b$ , and/or  $u_c$ ) must be detected and the phase angle of the triangular signal is adjusted to that of the input current. The triangular modulation signal is then injected to a constant control signal  $D_{avg}$  which is generated from the feedback control for  $U_o$  and the average current control for  $i_{rec1}$  and  $i_{rec2}$ . In order to control to a purely sinusoidal input current,  $D_{avg}$  must be around 0.5 due to the realization of the optimum modulation as shown in (3-19) corresponding to Fig.3-14. However, the output voltage can be controlled by changing  $D_{avg}$ , which would cause a slight distortion of input currents. The detailed performance will be discussed in section 3.7.

The low cost zero sequence current control scheme using shunt resistors is not employed here due to the variable duty cycle from zero, i.e.  $i_0$  cannot be detected when the duty cycle  $d_1$  or  $d_2$  is around zero. Accordingly, a through-hole current transducer is employed in order to detect  $i_0$ . For the current measurements of  $i_{rec1}$  and  $i_{rec2}$  for the average current control, the shunt resistors  $R_1$  and  $R_2$  are employed.



**Fig.3-31**. Control block diagram for realization of purely sinusoidal input currents by injecting the triangular modulation signal to the main control loop.

**Remark**: The zero sequence current control employing shunt resistors could be possible in the case of also the triangular modulation if sampling of a current measurement for  $i_0$  is done at proper timing, i.e.  $i_0$  is measured at which  $d_1$  or  $d_2$  is not around zero. Since zero sequence current does not include high frequency components (cf. Fig.3-60(a)), it is not necessary to measure  $i_0$  in every turn-on state. Alternatively,  $i_0$  can be detected by not only  $T_1$  current but also  $T_2$  current if an additional shunt resistor is connected to  $T_2$  in series. This would make it possible to measure  $i_0$  with switching frequency, i.e.  $i_0$  can be detected from  $T_2$  current when  $d_1$  is around zero.

# 3.6.4 Closed loop control

The control block diagram for the closed loop control of input current is shown in **Fig.3-32**. There, a digital control is implemented and Texas Instruments TMS320F2808 fixed-point DSP running at 100MHz is used for the realization of the controller. The closed loop control is achieved by being fed the d- and q-components of input currents back to the feed forward signals  $u'_F \cos \theta_{ref,F}$  and  $u'_F \sin \theta_{ref,F}$  which are based on the optimum modulation or the triangular modulation. A Phase-Locked-Loop (PLL) controller is executed to determine the d-component and the phase angle  $\theta_{\sigma}$  of the mains voltage  $U_N$ , while the q-component of  $U_N$  is regulated to zero. With  $\theta_{\sigma}$  also the d- and q- components of the input current are calculated. These values are compared with their reference values  $I^*_{IN}\cos \theta_{ref,F}$  and  $I^*_{IN}\sin \theta_{ref,F}$  and the difference is fed into the PI-controllers.

The reference value  $I^*_{IN}$  is determined by a voltage controller, which regulates the output voltage, or fixed by user and the phase angle  $\theta_{ref,F}$  between the mains voltage vector  $\underline{u}_N$  and the reference current vector  $\underline{i}_N$  is calculated using

$$\theta_{ref,F} = \arctan \frac{\omega LI *_{IN}}{\sqrt{u^2_{N,d} - (\varpi LI *_{IN})^2}}$$
(3-80),

which can be derived from Fig.3-17(b). The feed-forward signals  $u'_F \cos \theta_{ref,F}$  and  $u'_F \sin \theta_{ref,F}$  for the d- and q-components are added to the controller output. The amplitude of  $u'_F$  is also given from Fig.3-17(b) as

$$u'_{F} = \sqrt{u^{2}_{N,d} - (\varpi LI^{*}_{IN})^{2}}$$
(3-81).

After the summation the *d*- and *q*- components of the reference vectors  $u'_{d}^{*}$  and  $u'_{q}^{*}$  are given and the amplitude  $|u'^{*}|$  and the phase angle  $\theta_{N}^{*}$  of the reference vector for the LIT input voltage are calculated.

In the next step, the reference vector is rotated back to sector 0 by adding the mains phase angle  $\theta_{\pi}$  and subtracting  $N_s \pi/6$  from  $\theta_N *$  where  $N_s$  denotes the sector number. The result should be within the allowed region  $\pm 15^{\circ}$  (= $\pi/6$ ), which is determined by the sector borders. In order to eliminate numerical/measurement errors, the phase angle is limited to  $\pm 15^{\circ}$ . Thereafter, the phase angle is multiplied by 1 if the  $N_s$  is even and by -1 if  $N_s$  is odd in order to obtain a triangular reference phase angle which starts at -15° rises up to 15° and then ramps down to -15° again (cf. Fig.3-14) instead of a sawtooth-like phase angle, which jumps to -15° as soon as it reaches 15°. This time behavior of the reference phase angle is required to obtain the modulation signals, which can be calculated using (3-21) or (3-22). It is noted that the zero sequence current control is also applied in the same way to Fig.3-31 using a current transducer.



**Fig.3-32**: Control block diagram for the closed loop control employed in the two-switch topology (cf. Fig.3-9).

# **3.7.** Simulation results

In this section, the principle of operation and the control schemes of the single-switch topology (cf. Fig.3-8) and the two-switch topology (cf. Fig.3-9) are verified by numerical simulations. Furthermore, several control schemes, e.g. the constant duty cycle control, triangular modulation, 24-pulse modulation and closed loop control are compared.

# 3.7.1. Single-switch topology

In Fig.3-33, the simulated waveforms of the single switch topology (cf. Fig.3-8) are shown. The input currents have the switching frequency ripple. However, the typical input current shape of a 12-pulse rectifier such as a 12-step staircase waveform is present. The voltage waveforms across the LIT ( $u_{1a2a}$  and  $u_{a'N}$ ) and the input inductor  $(u_{aa'})$  are identical to the theoretical operation (cf. Fig.3-10). The input current harmonics are depicted in Fig.3-34. It is verified that the 5<sup>th</sup> and 7<sup>th</sup> harmonics are eliminated and the lowest harmonics number generated in the input current is 11<sup>th</sup>, which corresponds to the typical 12-pulse feature. The switching frequency current ripple (33kHz) is comparable to the 11<sup>th</sup> and 13<sup>th</sup> harmonics. However, high frequency ripple current would be easily attenuated by adding a filter on the mains. The simulation results show that the THD is 6.7% and the 11<sup>th</sup> and 13<sup>th</sup> components are respectively 5.4% and 3.7%. The 11<sup>th</sup> and 13<sup>th</sup> harmonics correspond to passive operation (cf. Fig.3-7(b)). Therefore, the requirement of input current harmonics for the aircraft applications can be fulfilled by the single-switch topology. The output voltage is then controlled at  $350V_{dc}$ . It is noted that the ideal condition, e.g. no voltage drops on the power semiconductors and ideal coupling of the LIT, is assumed in this simulation. The simulation result with consideration of the winding resistance and the leakage inductance would show almost equal behavior to Fig.3-33 because the stray components are relatively much lower.

# 3.7.2. Two-switch topology

**Fig.3-35** shows the simulation results of the two-switch topology (cf. Fig.3-9) using the constant duty cycle control. It is clearly verified that the switching frequency current ripple included in the input currents is much lower compared to the single switch topology (cf. Fig.3-33(a)). In the case of the two-switch topology, the time behaviors of the voltages are also identical with the theoretical calculations (cf. Fig.3-11). In **Fig.3-36**, the input current harmonics are depicted. From the input current



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**Fig.3-33:** Simulated waveforms of the single-switch topology (cf. Fig.3-8); (**a**) time behavior of the input phase currents  $i_a$ ,  $i_b$  and  $i_c$ ; (**b**) mains phase voltage  $u_{aN}$  and LIT voltage  $u_{1a2a}$ ; (**c**) mains phase voltage  $u_{aN}$  and corresponding LIT input voltage  $u_{a'N}$ ; (**d**) mains phase voltage  $u_{aN}$  and corresponding input inductor voltage  $u_{aa'}$ . Simulation parameters:  $U_N=115V_{rms}$ ,  $f_{IN}=400Hz$ ;  $U_O=350V_{dc}$ ,  $P_O=10kW$ , switching frequency  $f_S=33kHz$ ,  $D_{u1}=0.3$ .



**Fig.3-34:** Simulated input current spectrums of the single-switch topology (cf. Fig.3-8); (a) low order harmonics, (b) high order harmonics. Simulation parameters as Fig.3-33.

spectrum, it is also verified that the input current harmonics around 33kHz are significantly reduced as compared to the single switch topology (cf. Fig.3-34(b) and Fig.3-36(b)). However, the switching frequency harmonic cannot be cancelled completely due to difference of the LIT input voltage  $u_{a'N}$  and the input inductor voltage  $u_{aa'}$  during the turn-on periods of  $T_1$  and  $T_2$  (cf. Fig.3-11(e) and (f)), i.e. amplitudes of  $u_{a'N}$  and  $u_{aa'}$  at turn-on period of  $T_1$  are different from those at turn-off period of  $T_2$ , which cause a slight switching frequency (33kHz) current ripple. However, the switching frequency current ripple is then greatly reduced from 3.1% to

0.60%. The low order harmonics are equal in both hybrid systems (the single-switch and two-switch topologies). The output voltage is also controlled at  $350V_{dc}$ .



**Fig.3-35**: Simulated waveforms of the two-switch topology (cf. Fig.3-9) using the constant duty cycle control. Simulation parameters as Fig.3-33.





**Fig.3-36**: Simulated input current spectrums of the two-switch topology (cf. Fig.3-9); (a) low order harmonics, (b) high order harmonics. Simulation parameters as Fig.3-33.

The two-switch topology is also advantageous concerning output voltage ripple. The simulation results of the output voltage waveforms are shown in **Fig.3-37**. In the case of the two-switch topology, the output voltage ripple is lower (cf. Fig.3-37(a) and (b)). The amplitude of the output voltage ripple is reduced from 0.336V to 0.124V. It is noted that the capacitance of the output capacitor is 1mF and the pure capacitance (no series resistance and inductance) is assumed here. This would bring benefits in reducing the volume and the number of parallel connections of the output capacitor.



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**Fig.3-37**: Simulated output voltages of the single-switch topology (cf. Fig.3-8) (a) and the twoswitch topology (cf. Fig.3-9) (b). Simulation parameters as Fig.3-33.

The two-switch topology would be comparable to a parallel connection of two singleswitch discontinuous-mode boost-type rectifier systems [21] operating in an interleaved manner as shown in Fig.3-38. In this rectifier, input currents to diode bridges,  $i_{1\nu}$  and  $i_{2\nu}$  (v denotes the mains phase a, b, and c) are discontinuous and include a high switching frequency current ripple. However,  $T_1$  and  $T_2$  are controlled in an interleaved manner and therefore the sum of both currents  $i_{1\nu}$  and  $i_{2\nu}$  results in a lower switching frequency current ripple. This brings a reduction of a filter on mains side. The diodes  $D_3$  and  $D_4$  are connected in such a way as to avoid a zero sequence current which flows between two systems. The control circuit is shown in Fig.3-39. The control method is similar to the two-switch topology (cf. Fig.3-28) except for the feed forward control for input currents. The simulation results without the feed forward control are illustrated in **Fig.3-40**.  $T_1$  and  $T_2$  are driven by the constant duty cycle at  $D_{avg}$ =0.17 corresponding to  $U_O$ =350V<sub>dc</sub>. In the input currents, the low frequency harmonics such as 5<sup>th</sup> and 7<sup>th</sup> components remain and the THD results in 12.6% which is higher if compared to the two-switch topology, e.g. 6.7% of THD is achieved by the two-switch topology with the constant duty cycle. In order to reduce



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Fig.3-38: Parallel connection of two three-phase single-switch discontinuous mode boost rectifiers.



**Fig.3-39**: Control block diagram including feed forward control for input currents of two parallel connected three-phase single-switch discontinuous mode boost rectifiers (cf. Fig.3-38) operating in an interleaved manner.



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**Fig.3-40**: Simulated input current waveforms (**a**), output voltage (**b**), and input current harmonics (**c**) of two parallel connected three-phase single-switch discontinuous mode boost rectifiers (cf. Fig.3-38) operating in an interleaved manner with open loop control. Simulation parameters:  $U_N$ =115V<sub>rms</sub>,  $f_{IN}$ =400Hz,  $U_O$ =350V<sub>dc</sub>,  $P_O$ =10kW,  $f_S$ =33kHz with constant duty cycle of  $D_{avg}$ =0.17,  $L_N$ =188µH,  $L_U$ =15µH,  $C_N$ =2µF and  $C_O$ =1mF.

the THD of the competitive rectifier, the feed forward control is tested in simulation. For generating the feed forward signal, the input line-to-line voltages  $u_{ab}$ ,  $u_{bc}$ , and  $u_{ca}$ are rectified, which results in  $u_r$ , and only AC components of  $u_r$  are detected as  $u_{r,ac} = u_r - u_{r,avg}$ . The feed forward signal is then obtained by multiplying a gain P and  $u_{r,ac}$ . The feed forward control is verified by the simulation results as shown in **Fig.3**-**41**. The 5<sup>th</sup> harmonic is reduced by applying the feed forward control. However, the 7<sup>th</sup> harmonic is increased (cf. Fig.3-40(c)). The relationship of  $5^{th}$  and  $7^{th}$  harmonic amplitudes is dependent on P. A higher P results in lower 5<sup>th</sup> and higher 7<sup>th</sup> harmonics. The THD and the output voltage ripple are slightly reduced from 12.6% to 11.1% and from  $0.40V_{pp}$  to  $0.29V_{pp}$  respectively. Consequently, the THD cannot be reduced efficiently because the competitive rectifier cannot eliminate the 5<sup>th</sup> and 7<sup>th</sup> harmonics. It is noted that a zero sequence current can be reduced in the same way with the twoswitch topology, which allows omitting two diodes in the boost stage and results in a reduction of the conduction loss. However, the two-switch topology shows a lower THD and lower output voltage ripple (cf. Fig.3-37(b) and Fig.3-41(b)). Therefore, the parallel connection of two single-switch discontinuous-mode boost-type rectifier systems is not investigated in detail in this thesis.

# 3.7.3 Purely Sinusoidal input current control (triangular modulation)

The proposed modulation scheme to ensure a purely sinusoidal input current is verified by the numerical simulations and compared to the constant duty cycle operation. To easily generate the modulation functions in a practical implementation, the triangular approximation (cf. (3-18) and (3-19)) is assumed in the numerical simulations. It should be noted that the simulation results with the optimum modulation functions (cf. (3-17) and (3-19)) show almost equal behavior, e.g. approximately equal THD (the difference is less than 0.1%) and a slightly higher output voltage (only  $3.5V_{dc}$  higher). The simulation results are shown in **Fig.3-42**. The input currents are almost purely sinusoidal and a lower value of the input current THD, which is 0.8%, is obtained. Therefore, it is verified from the simulation that the input currents are improved as compared to the constant duty cycle control (cf. Fig.3-35(a) and Fig.3-42(a)). It is also seen from **Fig.3-43** that the low order harmonics (11<sup>th</sup> and 13<sup>th</sup>) are almost eliminated (cf. Fig.3-36(a) and Fig.3-43(a)). The normalized switching frequency (33kHz) current ripple is slightly increased and the double switching frequency (66kHz) component is reduced by using the triangular modulation (cf. Fig.3-36(b) and Fig.3-43(b))due to the different duty cycles of  $T_1$  and  $T_2$  which makes the interleaving less effective, i.e. cancellation of the switching frequency current ripple caused by interleaving is not effective if the duty cycles of  $T_1$  and  $T_2$  are different, especially at  $d_1=0$  and  $d_2=1$ ,  $d_1=1$  and  $d_2=0$  (cf. Fig.3-14).



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**Fig.3-41**: Simulated input current waveforms (**a**), output voltage (**b**), and input current harmonics (**c**) of two parallel connected three-phase single-switch discontinuous mode boost rectifiers (cf. Fig.3-38) operating in an interleaved manner with closed loop control. Simulation parameters as Fig.3-40 but with feed forward control.



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**Fig.3-42:** Simulated waveforms of the two-switch topology (cf. Fig.3-9) using the triangular modulation (cf. (3-18) and (3-19) corresponding to the linear approximations in Fig.3-14). The simulation parameters as Fig.3-33 but  $D_{u2}$ =0.5 and  $U_O$ =480V<sub>dc</sub>.

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**Fig.3-43**: Simulated input current spectra of the two-switch topology (cf. Fig.3-9) using triangular modulation; (a) low order harmonics, (b) high order harmonics. Simulation parameters as Fig.3-35.

The LIT voltage  $u_{1a2a}$  and the integrated LIT voltage  $u_{1a2a,int}$ , which is equivalent to the magnetic flux of the LIT, are depicted in **Fig.3-44**.  $u_{1a2a}$  and  $u_{1a2a,int}$  are varying over a half mains period. As compared to the constant duty cycle control, the peak amplitude of  $u_{1a2a,int}$  resulting from the triangular modulation is double (cf. Fig.3-44(a) and (b)) if the switching frequency magnetic flux ripple is neglected. Furthermore,  $u_{1a2a,int}$  oscillates with the frequency of the triangular modulation, i.e. with sixfold mains frequency within a 150°-wide interval. This causes a higher maximum flux density, volume, and core loss of the LIT. In the case of current-type hybrid rectifiers (cf. [9]-[11]), injected current swinging approximately from 0 to 200% against the average

value is required in order to achieve a purely sinusoidal input current. Maximum magnetic flux of an inductor, which is imposed by the current injection, would be higher due to a higher peak current. Therefore, there is the duality that the flux density of the inductor is increased in current-type hybrid rectifiers and the flux density of the LIT is increased in voltage-type hybrid rectifiers.



**Fig.3-44**: Simulated LIT voltage  $u_{1a2a}$  and magnetic flux  $u_{1a2a,int}$  in case of the constant duty cycle control (a) and triangular modulation (b) at  $D_{avg}=0.5$  and  $U_O=480V_{dc}$  in case of the two-switch topology (cf. Fig.3-9).

For  $D_{avg}=0.5$ , the output voltage is around  $480V_{dc}$  in the case of  $U_N=115V_{rms}$  (cf. (3-12)). Therefore, the voltage margin would not be sufficient for employing 600V power semiconductors, especially if input voltage fluctuation is considered, i.e. the output voltage is  $567V_{dc}$  if the input voltage is  $132V_{rms}$  which is the maximum for the aircraft applications. It is noted that the voltage drops on input inductor, LIT, and power semiconductors are neglected here. On the other hand, the output voltage should be set to  $350V_{dc}$  corresponding to  $D_{avg}=0.3$  with respect to future more electronic aircraft applications. The input current waveforms and the current spectrum for  $D_{avg}=0.3$  are shown in **Fig.3-45** and **Fig.3-46** respectively. The output voltage is then controlled to  $350V_{dc}$ . However, the input current harmonics are increased (cf. Fig.3-42(a) and Fig.3-45(b)) because the triangular modulation of  $D_{avg}=0.5$  cannot be realized (cf. Fig.3-45(b))

45(a)). In order to achieve the triangular modulation with  $D_{avg}=0.3$ , the variation of the duty cycles  $d_1$  and  $d_2$  is set from 0 to 0.6 (= $2D_{avg}$ ). Although the input current harmonics are increased by adjusting  $D_{avg}$  (from 0.5 to 0.3) of the triangular modulation, the input current quality is still higher if compared to the constant duty cycle control (cf. Fig.3-35(a) and Fig.3-45(b)). It can also be verified from Fig.3-36(a) and Fig.3-46(a) that the low order harmonics are reduced. The 11<sup>th</sup> and 13<sup>th</sup> harmonics are improved from 5.5% to 3.5% and from 3.7% to 2.6% respectively. The inductance of the input inductors, which is selected for the compliance to the limits given for the amplitudes of the 11<sup>th</sup> and 13<sup>th</sup> current harmonics, can be significantly reduced by the proposed modulation scheme. For example, in the case of  $D_{avg}=0.3$  the inductance could be reduced from 188µH to 55µH for the same low order input current harmonics, which results in a significant reduction of the inductor weight and volume.



**Fig.3-45**: Simulated waveforms of triangular modulations (a) and input currents (b) in case of the two-switch topology (cf. Fig.3-9). Simulation parameters as Fig.3-42 but  $D_{avg}$ =0.3 and  $U_0$ =350V<sub>dc</sub>.

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**Fig.3-46**: Simulated input current spectra of the two-switch topology (cf. Fig.3-9) using triangular modulation; (a) low order harmonics, (b) high order harmonics. Simulation parameters as Fig.3-45.

# 3.7.4 24-pulse modulation

The two-switch topology (cf. Fig.3-9) can also improve the input current from a 12pulse shape to a 24-pulse shape by a rectangular modulation [33]. This causes a benefit concerning elimination of the 11<sup>th</sup> and 13<sup>th</sup> harmonics and an improvement of the input current quality. In this thesis, the 24-pulse modulation scheme is briefly verified and compared to the constant duty cycle control and the triangular modulation. The duty cycles for the 24-pulse modulation are shown in **Fig.3-47**. The duty cycles  $d_1$ for  $T_1$  and  $d_2$  for  $T_2$  are modulated from 0.25 to 0.75 with the sixfold mains frequency and  $d_1$  and  $d_2$  are 180° phase shifted to each other. Therefore, both average duty cycles



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**Fig.3-47**: Duty cycles  $d_1$  for  $T_1$  (a) and  $d_2$  for  $T_2$  (b) of the two-switch topology (cf. Fig.3-9) using the 24-pulse modulation.

are 0.5.  $d_1$  and  $d_2$  should also be synchronized to mains frequency. Accordingly, the control circuit is the same as in Fig.3-31 but the sixfold mains frequency rectangular signal having an amplitude from -0.25 to 0.25 should be injected to  $D_{avg}$  instead of the triangular modulation signal. In **Fig.3-48**, it is verified that the 24-pulse operation is realized by changing the pulse widths of  $u_{a'N}$  and  $u_{aa'}$  at the middle points of every 30°-wide interval. The input current quality is clearly improved as compared to the constant duty cycle control (cf. Fig.3-35(a)).

From Fig.3-48(a), the input current waveform seems to be purely sinusoidal. Since the input inductor is designed to attenuate the 11<sup>th</sup> and 13<sup>th</sup> harmonics, the 23<sup>rd</sup> and 25<sup>th</sup> harmonics, which are theoretically generated by a 24-pulse operation, are greatly reduced. However, the 23<sup>rd</sup> and 25<sup>th</sup> harmonics cannot been eliminated due to the 24-pulse operation, which is verified by the input current harmonics shown in **Fig.3-49**. The 11<sup>th</sup> and 13<sup>th</sup> harmonics are almost eliminated and the 23<sup>rd</sup> and 25<sup>th</sup> harmonics still remain. As compared to the triangular modulation, the THD is increased from 0.8% to 2.0%. The switching frequency current ripple is almost equal in both modulation schemes (cf. Fig.3-43(b) and Fig.3-49(b)).



**Fig.3-48**: Simulated waveforms of the two-switch topology (cf. Fig.3-9) using the 24-pulse modulation. Simulation parameters as Fig.3-42.



**Fig.3-49**: Simulated input current spectrum of the two-switch topology (cf. Fig.3-9) using the 24-pulse modulation; (a) low order harmonics, (b) high order harmonics. Simulation parameters as Fig.3-42.

The simulation results of the THD in dependency on  $D_{avg}$  are shown in **Fig.3-50**. Since the modulation and/or duty cycle ranges are limited from 0 to 1, the amplitude of the duty cycles  $d_1$  and  $d_2$  are modified from 0 to  $2D_{avg}$  for  $D_{avg}<0.5$  and  $2D_{avg}$  -1 to 1 for  $D_{avg}>0.5$  in the case of the triangular modulation in order to adjust the average duty cycle. For the 24-pulse modulation, the same amplitude of the modulations, which is  $\pm 0.25$ , can be achieved within  $0.25 < D_{avg} < 0.75$ . In  $D_{avg} < 0.25$ ,  $d_1$  and  $d_2$  for the 24-pulse modulation vary within the same amplitude to the triangular modulation due to the

duty cycle limitation. For both the triangular modulation and the 24-pulse modulation, the simulation results show that the optimum  $D_{avg}$  to reduce the THD is around 0.5 (cf. Fig.3-50). Due to the elimination of low order harmonics, the lowest THD is achieved by the triangular modulation within the whole operating range as compared to the other control schemes. In the range of  $D_{avg}$ >0.5, the THD resulting from the 24-pulse modulation is greatly increased. This is caused by the discontinuous duty cycle modulations and the higher output voltage resulting in the high LIT and input inductor voltages, i.e. the average pulse width within every  $15^{\circ}$ -wide interval (=360°/24) is not constant because of the discontinuous modulation and insufficient number of pulses (only 3 or 4 pulses in the 15°-wide interval in the case of  $f_{IN}$ =400Hz and more critically with  $f_{IN}$ =800Hz which is the maximum mains frequency for the aircraft applications) and higher LIT and input inductor voltages allow rapid change of input currents. In order to avoid this problem, the switching frequency should be synchronized with the mains frequency and number of pulses should be equal in every 15°-wide interval. The other solution is that a much higher switching frequency should be set in order to be able to neglect an average pulse width difference, which however would cause a higher switching loss. In the triangular modulation, there is no such problem and no influence on low order harmonics because the modulation signals for  $d_1$  and  $d_2$  smoothly change.



**Fig.3-50**: Simulated THD in dependence on  $D_{avg}$  in two-switch topology (cf. Fig.3-9) using the constant duty cycle control, triangular modulation, and 24-pulse modulation. Simulation parameters as Fig.3-42.

The simulated input currents in the high  $D_{avg}$  range for both modulation schemes are compared in **Fig.3-51**. By increasing the switching frequency up to 100kHz, the THD resulting from the 24-pulse modulation with  $D_{avg}$ =0.7 is reduced from 9.8% to 6.3%. However, the THD is still higher compared to the triangular modulation. In the triangular modulation, almost sinusoidal input current is also achieved in the higher  $D_{avg}$  range. However, the 11<sup>th</sup> and 13<sup>th</sup> harmonics are increased in the 24-pulse modulation (cf. **Fig.3-52**). Therefore, the triangular modulation has a higher ability to improve input current quality in a wide operating range.



**Fig.3-51**: Simulated input current waveforms of the two-switch topology (cf. Fig.3-9) using the 24pulse modulation (a) and the triangular modulation (b). Simulation parameters as Fig.3-42 but  $D_{avg}$ =0.7 corresponding to  $U_0$ =798V<sub>dc</sub> and  $f_S$ =100kHz.
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**Fig.3-52**: Simulated input current harmonics of the two-switch topology (cf. Fig.3-9) using 24-pulse modulation (**a**) and triangular modulation (**b**). Simulation parameters as Fig.3-51.

In **Fig.3-53**, the simulated LIT voltage  $u_{1a2a}$  and the magnetic flux  $u_{1a2a,int}$  in the case of the 24-pulse modulation are also simulated as in Fig.3-44. The maximum  $u_{1a2a,int}$  shows the same value to that with the triangular modulation, which is double that of the constant duty cycle control (cf. Fig.3-44). The shapes of  $u_{1a2a,int}$  in both modulation schemes are slightly different. However, the variation frequency of  $u_{1a2a,int}$ , which is the sixfold mains frequency, is also identical. Therefore, the iron loss generated in the LIT would be almost equal in both modulation schemes (the triangular modulation and the 24-pulse modulation).



**Fig.3-53**: Simulated LIT voltage  $u_{1a2a}$  and magnetic flux  $u_{1a2a,int}$  in the case of the 24-pulse modulation at  $D_{avg}$ =0.5 and  $U_0$ =480V<sub>dc</sub>. Simulation parameters as Fig.3-44.

The output voltage dependency on  $D_{avg}$  is simulated as in **Fig.3-54**. The output voltage is identical to that given by the theoretical equation (cf. (3-12)) in all the modulation schemes, which are the constant duty cycle control, the triangular modulation, and the 24-pulse modulation. Voltage drops on the power semiconductors are neglected and the ideal coupling of the LIT are assumed here. It is noted that the simulated output voltage dependency of the single-switch topology (cf. Fig.3-8) is also identical to that from the theoretical equation (cf. (3-11)). Therefore, it is verified that the proposed hybrid rectifiers can control the output voltage by adjusting duty cycles.



**Fig.3-54**: Simulated output voltage in dependence on  $D_{avg}$ . Voltage drops on power semiconductors and leakage inductance of LIT are neglected. Simulation parameters as Fig.3-42.

# 3.7.5 Closed loop control

The closed loop control strategy was verified by the numerical simulations. In **Fig.3-55**, the simulated input currents resulting at the ideal condition, e.g. the symmetric mains voltage, are shown. The input currents are distorted at the particular phase angles and a higher THD of 3.8% is present compared to the open loop control (cf. Fig.3-42(a) and Fig.3-55(a)). This distortion is caused by the reason similar to that with the 24-pulse modulation described in the previous section. Since the input current is controlled by the three voltage vectors  $u'_{(10)}$ ,  $u'_{(00)}$ , and  $u'_{(01)}$  resulting in a LIT reference voltage  $u'^*$  (cf. (3-20) and Fig.3-16), every switching cycle should be within the same sector. If  $u'_{(10)}$  and  $u'_{(00)}$  is generated in one sector, e.g. sector 0, and  $u'_{(01)}$  is performed in the next sector, e.g. sector 1, the input current would differ from the reference value. This distortion can be reduced if the switching frequency is high, e.g. the pulse width of one jumped voltage vector to the next sector can be very narrow and therefore the input current distortion can be reduced.



**Fig.3-55**: Simulated input current waveforms of the two-switch topology (cf. Fig.3-9) using the closed loop control based on the space vector control. Simulation parameters as Fig.3-42 but  $f_S$ =33kHz (a) and  $f_S$ =100kHz (b).

Also, the sectors are defined by assuming the phase angles of purely sinusoidal input currents to the diode bridges (cf. Fig.3-15), i.e. the phase angle of each sector depends on the polarity of the diode bridge input currents. However, the sectors are decided from the input voltage measurements (cf. Fig.3-32), which are not related to real sector angles if input currents are not ideal. Therefore, distorted input currents cause a sector angle error, which results in input current distortions again. In order to reduce the distortion, the switching frequency is increased to 100kHz (cf. Fig.3-55(b)). The THD is improved to 2.6% because not only high frequency current ripple but also the low order harmonics, e.g. 3<sup>rd</sup> and 5<sup>th</sup> harmonics, are reduced (cf. **Fig.3-56**(a) and (b)). However, the low order harmonics still remain.



**Fig.3-56**: Simulated input current harmonics with  $f_S$ =33kHz (a) and  $f_S$ =100kHz (b) correspond to Fig.3-55.

To demonstrate the capability of the control strategy, the simulated behaviors at the step change of the reference current from 26A to 41A, which corresponds to the output power of 10kW at  $U_N$ =115V<sub>rms</sub>, is shown in **Fig.3-57**. There, also the d- and q-components of the input currents are depicted. It can be seen that the input current rapidly assumes the reference values. Therefore, the closed loop control has the ability to control the input currents to be a reference value. It is noted that the step change to the different direction, e.g. reduction of input current reference value, results in symmetrical behavior and the load resistor is constant before and after the step changes.



**Fig.3-57**: Simulated step change behaviors of input currents (**a**), d-component (**b**), and q-component (**c**). Simulation parameters as Fig.3-55(b) but step change of reference current from 26 to 41A.

A main advantage of closed loop input current control is the ability to directly control input currents despite fluctuations of input voltages. In order to verify this feature, a simulation was performed with the unbalanced and distorted input voltages. In **Fig.3-58**,  $\pm 5\%$  of the unbalance input voltages, e.g. -5% for  $u_{aN}$ , 5% for  $u_{bN}$ , and -5% for  $u_{cN}$  in the amplitudes, were then input to the rectifier. In the case of open loop control, the amplitudes of the input currents are also unbalanced, e.g. especially  $i_c$  is lower because the LIT input voltage of phase *c* depends on both lower input voltages  $u_{aN}$  and  $u_{cN}$  (cf. Fig.3-9), and the input currents include the distortion (cf. Fig.3-42(a) and Fig.3-58(a)). There is no solution to reduce the unbalanced amplitudes and the distortions by open loop control if the mains voltage is non-ideal. However, the amplitudes of the input currents are almost balanced and lower distortion is achieved by the closed loop control (cf. Fig.3-58(b)). The THD is then 5.2% which is not much increased from the result of the ideal mains voltage behavior (cf. Fig.3-55(b)).



**Fig.3-58**: Simulated input current waveforms resulting from open loop control (**a**) and closed loop control (**b**) at unbalanced input voltages. Simulation parameters as Fig.3-55(b) but  $\pm$ 5% unbalanced input voltage (-5% for  $u_{aN}$ , 5% for  $u_{bN}$ , and -5% for  $u_{cN}$  in the amplitudes).

The distorted input voltage behaviors are tested in **Fig.3-59**. In this simulation, 5% amplitude of  $5^{\text{th}}$  harmonic is contained in all input phases. A slight improvement of the input current quality is obtained by the closed loop control. It can be seen from the waveforms that the  $5^{\text{th}}$  harmonic is reduced. The THD resulting from the open loop control is then 7.9% and reduced to 6.9% by the closed loop control. When the distortion amplitude is 10%, the THD is increased up to 15.0% in the case of open loop control. However, a lower THD, which is 10.9%, results. Therefore, the closed loop control scheme is able to improve input current harmonics especially in the case of non-ideal mains voltage conditions.



**Fig.3-59**: Simulated input current waveforms resulting from open loop control (**a**) and closed loop control (**b**) at distorted input voltages. Simulation parameters as Fig.3-55(b) but including 5% amplitude of  $5^{\text{th}}$  harmonic in  $u_{aN}$ ,  $u_{bN}$ , and  $u_{cN}$ .

# 3.8 Experimental results

In this section, the principle of operation and the theoretical analysis of the two-switch topology (cf. Fig.3-9) using the different control schemes, which are constant duty cycle control, triangular modulation, 24-pulse modulation, and also closed loop control, are experimentally verified by using the 10kW prototype.

# 3.8.1. Constant duty cycle control

The experimental results of the input current waveforms, the zero sequence current, and the input current harmonics resulting from the constant duty cycle control are shown in **Fig.3-60**.  $D_{ave}=0.3$  corresponding to  $U_0=350V_{dc}$  is adjusted and a zero sequent current is measured by the different methods. In Fig.3-60(b), all diode bridge input currents of one partial system  $(i_{1a}, i_{1b}, and i_{1c})$  are measured by a through-hole type current transducer (LA 55-P, 50A, LEM Components), which results in a measurement of a zero sequent current. In the other way, the proposed zero sequence current control (cf. Fig.3-28 and Fig.3-29) is implemented in Fig.3-60(c). In the case of applying the zero sequence controls (cf. Fig.3-60(b) and (c)), the input current waveforms are in good correspondence with the simulation results (cf. Fig.3-35(a)). Zero sequence current flows if no control is applied (cf. Fig.3-60(a)). However, the zero sequence current is successfully attenuated by both methods as shown in Fig.3-60(b) and (c). For both concepts, the almost equal THD values, which are 5.2% for the zero sequence current measurement using the current transducer (cf. Fig.3-60(b) and (e)) and 5.7% for the proposed method (cf. Fig.3-60(c) and (f)), are obtained. The slight difference is caused by sampling error of the zero sequence value, which results in the slight remnant of the zero sequence current and the small increase in the low order harmonics (2<sup>nd</sup>, 4<sup>th</sup>, and 5<sup>th</sup>). Lack of zero sequence current control brings low order harmonics (cf. Fig.3-60(a) and (d)) and the THD is then greatly increased to 13.7%. In Fig.3-60(f), 11<sup>th</sup> is the highest harmonics component in the input current and is only 4.2% of the fundamental value, which corresponds to passive operation (cf. Fig.3-7) and the output voltage is controlled to  $350V_{dc}$  within the whole operating range as shown in **Fig.3-61**. Therefore, the hybrid rectifier using a constant duty cycle can control the output voltage without impairing input current quality.



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employing a zero sequence current control where  $i_0$  is measured using a through-hole current transducer LA 55-P (50A, LEM Components); (c) and (f) as (a) and (d) but with proposed zero sequence current control employing shunt resistors for zero sequence Fig.3-60: Measured input current waveforms  $i_a$ ,  $i_b$ ,  $i_c$ , zero sequence current  $i_0$ , and input current harmonics of the two-switch topology (cf. Fig.3-9) using the constant duty cycle control; (a) and (d) without zero sequence current control; (b) and (e) as (a) and (d) but current determination. Operating parameters:  $U_N=115$ V<sub>rms</sub>,  $f_{IN}=400$ Hz,  $U_O=350$ V<sub>dc</sub> ( $D_{avg}=0.3$ ),  $P_O=10$ kW,  $f_S=33$ kHz.



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**Fig.3-61**: Output voltage characteristics in dependence on output power, input voltage, and input frequency of the two-switch topology (cf. Fig.3-9) using constant duty cycle control. Operating conditions:  $U_0$ =350V<sub>dc</sub> and  $f_s$ =33kHz.

The measured LIT voltage  $u_{1a2a}$  and  $u_{a'b'}$  with reference to  $u_{aN}$  of the two-switch topology (cf. Fig.3-9) are shown in **Fig.3-62**. It is noted that  $u_{a'b'}$  is the line-to-line voltage at the LIT inputs and differs from the LIT phase voltage  $u_{a'N}$  only in amplitude by a factor of  $\sqrt{3}$  and 30° phase shift, which are the same as in the well known three-phase theory. Therefore, the measured waveforms are in close correspondence to the simulated waveforms (cf. Fig.3-35(b) and (c)). In **Fig.3-63**, the input current waveforms and the harmonics at the maximum mains frequency of 800Hz for the aircraft applications are measured. The input current quality is higher compared to a lower mains frequency (cf. Fig.3-60(c) and (f)) due to the higher frequency component of the 11<sup>th</sup> and 13<sup>th</sup> harmonics, which can be effectively reduced by the input inductors. The THD is then reduced to 3.1%. The 11<sup>th</sup> harmonic is the highest component and only 4.2% at  $f_{IN}$ =400Hz and 2.0% at  $f_{IN}$ =800Hz with reference to the fundamental value, which can fulfil the standard for the aircraft applications.

The efficiency and the power factor in dependence on the output power for the twoswitch topology (cf. Fig.3-9) are depicted in **Fig.3-64**. At the nominal operating point  $(U_N=115V_{rms}, f_{IN}=400\text{Hz}, U_O=350V_{dc}, P_O=10\text{kW})$ , 95.0% of the efficiency and 0.95 of the power factor are obtained. The output voltage is then controlled to  $U_O=350V_{dc}$ 

independent of the operating condition. As no input filter has been considered, the amplitude of the switching frequency input current ripple is comparable to the fundamental amplitude for a low output power range, which results in a relatively low power factor. Therefore, the power factor in a low power range can be increased by adding filter capacitors on mains. The low power factor in high output power and high mains frequency ranges is due to phase displacement between input current and input voltage resulting from the voltage drop across the input inductors. One has to point out that the system fulfills the requirements concerning low frequency input current harmonics within the whole operating range.



**Fig.3-62**: Measured LIT voltage  $u_{1a2a}$  and mains line-to-line voltage  $u_{ab}$  (**a**), LIT input line-to-line voltage  $u_{a'b'}$  and  $u_{ab}$  (**b**) of the two-switch topology (cf. Fig.3-9) using the constant duty cycle control. Operating conditions as Fig.3-60(c) and (d).



**Fig.3-63**: Measured input current waveforms (**a**) and harmonics (**b**) of the two-switch topology (cf. Fig.3-9) using the constant duty cycle control. Operating conditions as Fig.3-60(c) and (d) but  $f_{IN}$ =800Hz.

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**Fig.3-64**: Measured efficiency (a) and power factor (b) characteristics of the two-switch topology (cf. Fig.3-9) using the constant duty cycle control in dependence on output power for different input voltages and frequencies. Operating conditions:  $U_O=350V_{dc}$  and  $f_S=33kHz$ .

# 3.8.2 Comparative evaluation of the single-switch topology and two-switch topology

The distribution of the losses of the single-switch topology (cf. Fig.3-8) and the twoswitch topology (cf. Fig.3-9) is depicted in **Fig.3-65**. The single-switch topology using the same switching frequency (33kHz) shows the higher iron loss of the input inductors due to the higher switching frequency current ripple (cf. Fig.3-33(a) and Fig.3-35(a)). Since the frequency and amplitude of the fundamental currents are high, the iron loss resulting from the fundamental component cannot be neglected. However, the iron loss caused from the switching frequency components is dominant in the case of the single-switch topology because the switching frequency current ripple is 4.2 times higher compared to the two-switch topology. On the other hand, the higher LIT iron loss occurs for the two-switch topology due to chopping  $u_{a1a2}$  with the switching frequency within 150°-wide interval from  $\pi/6$  to  $\pi$  of mains period (cf. Fig.3-11, Fig.3-23, Fig.3-35(b), and Fig.3-36(a)).



**Fig.3-65**: Distribution of the losses of the two-switch topology (cf. Fig.3-9) for the switching frequency of  $f_S$ =33kHz and of the single-switch topology (cf. Fig.3-8) for  $f_S$ =33kHz and  $f_S$ =66kHz. Assumed operating conditions:  $U_N$ =115V<sub>rms</sub>,  $f_{IN}$ =400Hz,  $U_O$ =350V<sub>dc</sub> ( $D_{avg}$ =0.3),  $P_O$ =10kW.

As described before, the two-switch topology (cf. Fig.3-9) shows a lower switching frequency current ripple due to its interleaved manner. Therefore, the loss distribution of the single-switch topology (cf. Fig.3-8) using double switching frequency (66kHz), which would result in a switching frequency current ripple comparable to the two-switch topology, is also calculated here. However, the switching frequency current ripple is almost double, as shown in the simulation results (cf. Fig.3-35(a), Fig.3-36(b) and **Fig.3-66**). This is caused by variation of LIT and input inductor voltages, i.e. switching frequency current ripple depends on variation of  $u_{aN}$  and amplitude of  $u_{aa'}$ , which are higher in the case of the single-switch topology (cf. Fig.3-33(d) and Fig.3-35(d)). The iron loss resulting from the double switching frequency (66kHz) can only be slightly reduced.



**Fig.3-66**: Simulated input current waveforms (**a**) and input current spectrum (**b**) of the single-switch topology (cf. Fig.3-8) for the switching frequency of  $f_S$ =66kHz. Simulated parameters:  $U_N$ =115V<sub>rms</sub>,  $f_{IN}$ =400Hz,  $U_O$ =350V<sub>dc</sub> ( $D_{avg}$ =0.3),  $P_O$ =10kW.

**TABLE 3-3** summarizes the total losses and the calculated efficiencies. Consequently, a slight reduction of the efficiency is shown in the case of the single-switch topology (cf. Fig.3-8) with  $f_s$ =33kHz. In the case of the double switching frequency (66kHz) employed in the single-switch topology, the efficiency cannot be improved due to the higher switching losses. The efficiency of the two-switch topology (cf. Fig.3-9) shows the highest value. Accordingly, the two-switch topology is advantageous over the single-switch rectifier concerning not only switching frequency input current ripple but also the higher efficiency and/or input filter and heat sink volume reduction. Therefore, the two-switch topology has to be preferred for high power density applications. It should be noted that the efficiency could be improved if we use the latest power semiconductor and magnetic materials. For instance, the switching losses can be greatly reduced if a Silicon Carbide Schottky diode is employed.

**TABLE 3-3**: Calculated total losses and efficiencies for the single-switch topology (cf. Fig.3-8) using  $f_S$ =33kHz and 66kHz and the two-switch topology (cf. Fig.3-9) using  $f_S$ =33kHz. Assumed operating parameters:  $U_N$ =115V<sub>rms</sub>,  $f_{IN}$ =400Hz,  $U_O$ =350V<sub>dc</sub> ( $D_{avg}$ =0.3),  $P_O$ =10kW.

System		Total loss	Efficiency
		[W]	[%]
Single-switch topology	$f_S$ =33kHz	502	95.2
	$f_S$ =66kHz	548	94.8
Two-switch topology	$f_S$ =33kHz	488	95.4

# 3.8.3 Purely Sinusoidal input current control (triangular modulation)

The proposed triangular modulation to improve input current quality is verified by the prototype. In this section, the experimental results of the triangular modulation are introduced and compared to the different control schemes, i.e. the constant duty cycle control and the 24-pulse modulation.

Since  $D_{avg}=0.5$  causes higher current and voltage stresses on the power semiconductors compared to  $D_{avg}=0.3$ , especially both current and voltage stresses are increased in the power transistor, the maximum output power is limited at around 7.5kW. The input voltage is adjusted to  $95V_{rms}$  instead of  $115V_{rms}$  in order to ensure a sufficient voltage margin on the 450V output capacitor which replaces the 400V capacitor for the measurements. The output voltage is then  $408V_{dc}$  at no load. The measured input current waveforms and the harmonics performed by the different control schemes, i.e. the constant duty cycle control, the triangular modulation, and the 24-pulse modulation at  $D_{avg}=50\%$  are shown in **Fig.3-67**. It is verified that the



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 $U_{N}=95$ V<sub>rms</sub>,  $f_{IN}=400$ Hz,  $U_{O}=370$ V<sub>dc</sub> ( $D_{avg}=0.5$ ),  $f_{S}=33$ kHz,  $P_{O}=7.7$ kW.

triangular modulation is able to improve the input current waveforms to the sinusoidal shapes (cf. Fig.3-67(b)) and the  $11^{\text{th}}$  and  $13^{\text{th}}$  harmonics are almost eliminated (cf. Fig. 3-67(e)). The THD resulting from the constant duty cycle is 4.6% (c.f. Fig.3-67(a) and (d)) and reduced to 1.7% by applying the triangular modulation. In the case of 24-pulse modulation, the THD is 2.5%, which is lower if compared to the constant duty cycle control but with the triangular modulation. Although, the  $11^{\text{th}}$  and  $13^{\text{th}}$  harmonics are improved from the constant duty cycle, they still remain (cf. Fig.3-67(f)). This is caused by different average pulse width as described in the section 3.7.4. It is also seen from Fig.3-67(c) that the input currents controlled by the 24-pulse modulation are distorted at the particular phase angles. Accordingly, the proposed triangular voltage modulation causes the lowest THD in the modulation schemes.

The power factor and efficiency characteristics for the different modulation schemes are illustrated in Fig.3-68. The highest power factor is also achieved by the triangular modulation (cf. Fig.3-68(a)). The power factor at maximum output power is improved from 0.950 to 0.971 as compared to the constant duty cycle control. It should be noted again that the low power factor in the high power range is caused by a phase displacement between input voltage and input current due to the voltage drop on the input inductor. In the low power range, the highest power factor characteristic is achieved by the constant duty cycle control. The input currents to the diode bridges are then discontinuous. Therefore, the principle of operation described in the section 3.3 cannot be performed in the low power range. The efficiency characteristics achieved by triangular modulation and 24-pulse modulation are almost equal (cf. Fig.3-68(b)). As shown in Fig.3-44 and Fig.3-53, iron loss in the LIT is relatively higher in the case of triangular modulation and 24-pulse modulation. Therefore, a slightly lower efficiency is obtained as compared to the constant duty cycle control. However, the inductance of the input inductor can be reduced by applying triangular modulation because the inductance is designed in order to reduce 11<sup>th</sup> harmonics for the passive mode and/or the constant duty cycle. Therefore, loss in the input inductor can be reduced by applying a lower inductance and then the efficiency would be comparable to the constant duty cycle control.



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**Fig.3-68**: Measured power factor (**a**) and efficiency characteristics (**b**) of the two-switch topology (cf. Fig.3-9) in dependency on output power and different modulation schemes. Operating parameters as Fig.3-67.

# 3.8.4 EMC behaviour

The EMI conductive emissions are measured and illustrated in Fig.3-69. Since the mains frequency is high as compared to 50Hz or 60Hz, a normal LISN (Line Impedance Stabilization Network) cannot be utilized. Therefore, a LISN which is able to input 400Hz is used in the measurements. The rectifier is powered via the LISN and the input current to the rectifier is measured. It is noted that the measured EMI noises are high because no filter is applied. The emission in the passive mode, which means  $T_1$  and  $T_2$  are permanently turned off, is much lower because there is no high switching operation. In the active modes (during switching  $T_1$  and  $T_2$ ), the peak values for the constant duty cycle control and the 24-pulse modulation are almost equal and show 92dBµA around the frequency of 1MHz to 2MHz. However, the peak value is reduced to 85dVuA by the triangular modulation. This is caused by a property of the triangular modulation as can be seen from Fig.3-42(d). The pulse width of the input inductor voltage is lower when the amplitude is higher as compared to the other modulation schemes (cf. Fig.3-35(d), and Fig.3-47(c)). This prevents any step change and results in a lower ripple current. This can also be seen from the simulation results as shown in Fig.3-70. The simulated DM (differential mode) emission for the triangular modulation is lowest around 1MHz and higher frequency range. It is noted that the simulation results include only differential mode emission and common mode emission is not assumed. Therefore, the triangular modulation brings an advantage to reduce volume of an EMI filter.



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using the constant duty cycle control (b), the triangular modulation (c), and the 24-pulse modulation (d). Simulated parameters: **Fig.3-70**: Simulated DM conductive emissions of the two-switch topology (cf. Fig.3-9) at the passive mode ( $T_1$  and  $T_2$  are turn-off) (**a**),  $U_{N}=115$ V<sub>ms</sub>,  $f_{IN}=400$ Hz,  $U_{O}=480$ V<sub>dc</sub> ( $D_{avg}=0.5$ ),  $f_{S}=33$ KHz,  $P_{O}=10$ kW.

# 3.8.5 Closed loop control

In order to increase the operating range to the full output power in the two-switch topology (cf. Fig.3-9), the prototype is modified as shown in Fig.3-71 and TABLE 3-4. The latest power transistors and diodes, which are the 900V CoolMOS (IPW90R120C3) and 1200V SiC Schottky diode (C2D20120D), are employed to reduce the switching losses. Since there is no reverse recovery in Schottky diodes, the reverse recovery loss in the diodes as well as the turn-off loss in the power transistors can be reduced, i.e. a high peak current caused by a reverse recovery does not flow to the MOSFET at turn-on. The voltage ratings of the power semiconductors and the diodes are also increased for ensuring the operation at  $D_{avg}=0.5$  and/or the maximum input phase voltage of  $132V_{rms}$ . The digital control is implemented and the optimum modulation is used because the complex functions are easily realized by a digital control. The prototype consists of two PCBs. The DSP is mounted on the control board. The power board hosts not only the power parts, but also an auxiliary power supply, a pre-charge circuit, analogue measurements, and level-shifting circuits for use by the DSP control board. It is noted that the same input inductor and LIT with Fig.3-22 and Fig.3-26 are utilized in the prototype and the switching frequency is slightly increased to 40kHz.



**Fig.3-71**: A 10kW prototype of the two-switch topology (cf. Fig.3-9) which can operates at  $D_{avg}$ =0.5, the maximum input voltage  $U_N$ =132V<sub>rms</sub>, and  $f_S$ =40kHz. Digital control is implemented.

<b>TABLE 3-4</b> . List of components employed in Fig.3-71.			
Component	Symbol	Туре	
Diode bridge		VUE75-12NO7, IXYS, 1200V/75A,	
MOSFE\$T	$T_1, T_2$	IPW90R120C3, Infinion, 900V/36A, 3 in parallel	
Output diode	$D_1, D_2$	C2D20120D, CREE, 1200V/20A, 2 in parallel	
Output capacitor	$C_O$	$680^{1}$ F, $400V_{dc}$ , 2 in series	
Current sensor		CMS4050, 50A, Sensitec	
Controller		TMS320F2808 DSP board, Texas instruments	

TABLE 3-4: List of components employed in Fig.3-71

The closed loop control scheme (cf. Fig.3-32) for input current is verified by the prototype. In **Fig.3-72**, the measured input current waveforms and the harmonics for the symmetrical and the asymmetrical mains voltages are shown. Fig.3-72(a) demonstrates that the 12-step staircase shapes are improved to sinusoidal shapes.



**Fig.3-72**: Measured input current waveforms and harmonics for symmetric mains voltages (**a**) and (**c**) and for asymmetric mains voltages with  $\pm 5\%$  of unbalanced amplitudes (**b**) and (**d**). Operating conditions as Fig.3-42 but  $f_s$ =40kHz.

Accordingly, the ability of the closed loop control to track a sinusoidal reference current is verified. From the input current harmonics as shown in Fig.3-72(c), the 11<sup>th</sup> and 13<sup>th</sup> harmonics are almost eliminated and the THD is then 1.2%. In Fig.3-72(b),  $\pm$ 5% amplitude of the mains voltage is unbalanced. However, the input currents are then controlled to the sinusoidal shapes and the amplitudes are almost balanced. The input current harmonics are close to the symmetrical one (cf. Fig.3-72(c) and (d)) and the 2.2% of THD is present. Those results are also identical to the simulation results (cf. Fig.3-58(b)).

The input current measurement for the distorted mains voltages is illustrated in **Fig.3**-**73**. The 5% of 5<sup>th</sup> harmonic is included in the mains voltages here. However, the input



**Fig.3-73**: Measured input current waveforms (a) and harmonics (b) for 5% 5<sup>th</sup> harmonics mains voltages. Operating conditions as Fig.3-72.



Fig.3-74: Measured input current waveforms at step change of reference current from 15A to 40A.

currents are sinusoidal and the 2.7% of THD is obtained. The behaviour of the step change of the reference for the input current is performed in **Fig.3-74**. The reference is changed from 15A to 40A and then the amplitude of the input currents rapidly goes up to track the reference. Therefore, it is verified also from the experimental results that the closed loop control is able to control input currents directly and to reduce an influence of mains voltage fluctuations on input currents.

# **3.9 Conclusions**

In this section, hybrid 12-pulse rectifiers such as the single-switch topology (cf. Fig.3-8) and the two-switch topology (cf. Fig.3-9) are proposed. The controlled output voltage can be obtained by the proposed hybrid rectifiers with different control schemes. Furthermore, the modulation functions for achieving a purely sinusoidal input current are derived and the closed loop input current control scheme based on the space vector theory is proposed. The proposed hybrid rectifiers and the control schemes are verified by the numerical simulations. The two-switch topology is advantageous concerning lower switching frequency current ripple and realization of a purely sinusoidal input current. A 10kW prototype has been built for verifying the principle of operation and the theoretical analysis. The zero sequence current resulting in low harmonics on the mains and higher current stress can be reduced by the proposed control scheme which can be realized at a lower cost. A slightly higher efficiency can be obtained by the two-switch topology compared to the single-switch topology. A purely sinusoidal input current is achieved and the THD and the power factor are improved by the proposed modulation scheme. The triangular modulation shows the lowest THD compared to the constant duty cycle control and the 24-pulse modulation. The efficiency could be comparable to the constant duty cycle control if the input inductor were to be optimized for triangular modulation. In order to achieve a purely sinusoidal input current, the average duty cycle must be around 0.5. However, it is necessary to adjust the average duty cycle for controlling the output voltage. The THD is then increased and the input current is not purely sinusoidal if the average duty cycle is not 0.5. The triangular modulation schemes, however, show the lowest THD with varying average duty cycle as compared to the other control schemes. The closed loop control is able to control input currents directly to track a reference generated in the controller and yield a high input current quality even if non-ideal input voltages (distorted and/or unbalanced) are supplied to the rectifiers.

Consequently, the proposed hybrid rectifiers and control schemes can realize a low effect on the mains. Moreover, the output voltage is controlled to a constant value, which allows an optimum design for an inverter and a motor connected to the rectifier. Furthermore, the proposed hybrid rectifiers have a high reliability because the systems can operate in a passive mode (power transistors are permanently turn-off). Therefore, the proposed hybrid rectifier would be suitable for aircraft and micro gas turbine applications.

# Chapter 4

# Outlook

In this thesis, two kinds of hybrid rectifiers are introduced and excellent performances are demonstrated by prototypes having high power densities. In future, extended work on both hybrid topologies will be done.

# 4.1 Electronic smoothing inductor

The ESI topology will be investigated in detail by applying it to an inverter that drives a motor. For instance, the ESI can also be connected to the output capacitor  $C_0$  in series as shown in **Fig.4-1**. In order to charge and discharge the DC-link capacitor C, the bidirectional current ( $i_{C,esi}=i_0-I_L$ ) must be controlled. Therefore, four switches are employed. 3-level voltage modulation ( $U_{02}-U_C$ ,  $U_{02}$ , or  $U_{02}+U_C$ ) is then present at the rectifier output voltage  $U_0$ . The DC current  $I_L$ , which can be controlled by the ESI, is increased at  $U_0=U_{02}-U_C$  and decreased at  $U_0=U_{02}+U_C$ . There, a current path to bypass C also exists. Therefore, the same operation is obtained as with the rectifier where ESI is employed on the diode bridge output line (cf. Fig.2-8).

The 3-level output voltage modulation would benefit the inverter. For instance, we can reduce the switching voltage of the IGBTs by synchronizing an operational frequency of the ESI to an inverter switching timing. In the case that the ESI is not applied (or in a passive mode),  $U_0$  is always equal to  $U_{02}$ , neglecting the voltage drops on the MOSFETs, and the IGBT voltage stress is also  $U_{02}$  as shown in **Fig.4-2**(a). However, the IGBT voltage can be reduced to  $U_0$ - $U_c$ , which is lower than  $U_{02}$ , at the switching timings if the ESI operation is synchronized to the IGBT switching behaviour (cf.

Fig.4-2(b)). This would be possible because an operational frequency of the ESI can be much higher than that of the inverter e.g. the switching frequency of an inverter is normally set around 15kHz to avoid acoustic noise and minimize switching losses and the equivalent switching frequency of the ESI is demonstrated at 140kHz in this thesis. The lower switching voltage would bring some advantages. For instance, since switching loss depends on the switching voltage, switching losses of IGBTs and diodes in the inverter would be reduced. The peak of the spike voltage of IGBTs or diodes at a switching transition can also be reduced e.g. a sufficient voltage margin would be obtained. Therefore, a high dv/dt could be realized by using a lower gate resistor without a large overshoot voltage, which will also result in reduced switching losses. Furthermore, it might be a possible to apply lower rating voltage IGBTs and diodes.



Fig.4-1: A variation for applying ESI which is connected to the output capacitor in series.



**Fig.4-2**: Theoretical IGBT switching voltages without ESI or with passive operation (**a**) and with operation of ESI to reduce IGBT voltages at the switching transitions.

Two MOSFETs could be replaced by diodes  $D_1$  and  $D_2$  as illustrated in **Fig.4-3**. Here, the number of capacitors is increased ( $C_{DC1}$  and  $C_{DC2}$ ). In this operation, 2-level voltage modulation (alternatively  $U_{02}+U_{C1}$  or  $U_{02}-U_{C2}$ ) will be performed for both rectifier and inverter. The voltage stress on the power semiconductors in the ESI will be double due to the series connection of  $C_{DC1}$  and  $C_{DC2}$  if  $U_{C1}$  and  $U_{C2}$  are equal. Alternatively,  $U_{C1}$  and  $U_{C2}$  are controlled to different levels. As shown in (2-1), in order to control current flowing to the inductor L, more than 8.9% of the amplitude of the input line-to-line voltage  $\hat{u}_i$  is required for the DC-link voltage at  $u_r \leq U_O \; (=3 \hat{u}_i / \pi)$ . However, only 4.5% of  $\hat{u}_i$ , which is almost half, is needed at  $u_r \ge U_0$ . Therefore,  $U_{C1}$ can be adjusted to half of  $U_{C2}$  and the voltage stress on the power semiconductors is reduced. Since  $U_C = 70 V_{dc}$  in the prototype (cf. 2-13) is sufficient for a  $400 V_{rms}$  line-toline mains voltage with the assumption of  $\pm 15\%$  mains voltage variation, the total DClink voltage (= $U_{C1} + U_{C2}$ =1.5 $U_C$ ) in the ESI (cf. Fig.4-3) would be 105V<sub>dc</sub>. Therefore, the 150V power semiconductors are still suitable. Furthermore, AC-DC and DC-AC conversions would be independently controlled e.g.  $T_1$  controls a current flowing to L and  $T_2$  controls a discharge current from  $C_0$ . Therefore, the voltage levels of  $U_0$  $(=U_{O2}+U_{C1} \text{ or } U_{O2}-U_{C2})$  are decided only by the switching state of  $T_2$  independently of the rectifier operation. Accordingly, switching timings of  $T_2$  could be easily synchronized to inverter switching timings and therefore a reduction of the IGBT switching voltage could be easily achieved.



Fig.4-3: A variation for applying ESI where two MOSFETs are replaced by diodes from Fig.4-1.

# 4.2 Hybrid 12-pulse rectifier

In the hybrid 12-pulse rectifier, the volume of the magnetic components will be minimized. For instance, the LIT composed of three three-limb cores can be integrated by a five-limb core as shown in Fig.4-4(a). Then only two EE cores are required and the volume of the cores can be reduced to 2/3 compared to the conventional three three-limb cores. The input inductor is also integrated into the LIT by using a leakage inductance if it is only generated between the primary winding  $(w_B)$  and the other windings ( $w_{A+B}$  and  $w_A$ ). In Fig.4-4(b), the winding structure is illustrated. In order to reduce copper loss,  $w_B$  should be close to the center leg to reduce the winding distance because a current flowing to  $w_B$  is the highest compared to the other windings. For generating a sufficient leakage inductance, a leakage layer will be inserted between  $w_B$ and the other windings. One has to note that  $w_{A+B}$  and  $w_A$  must have a high coupling coefficient and therefore should be close to each other. When using a ferrite film, which is mechanically flexible and composed of ferrite powder and plastic e.g. Ferrite Polymer Composite manufactured by EPCOS, to the leakage layer, the leakage inductance can be effectively generated without occupying a large space for the leakage layer because the permeability and flux density of the leakage layer will be greatly increased if compared with using air. Acoustic noise generated from the magnetic components should also be considered. In high mains frequency applications, e.g. 400Hz, or several kHz, the fundamental frequency is within the audio range. The cores and windings should be mechanically fixed by a varnish. Furthermore, the size of the magnetic components should not have a resonance to the mains frequency. In further work, the design for the magnetic integrations and the evaluations in the system will be done.



**Fig.4-4**: Magnetic integrations of LIT composed of a five-limb core (**a**) and input inductor (**b**) for the hybrid 12-pulse rectifier.

In this thesis, the voltage-type hybrid 12-pulse rectifier is focused upon. However, the modulation schemes to achieve a purely sinusoidal input current would also apply to current-type 12-pulse rectifiers. Therefore, the hybrid 12-pulse rectifier employing the inductors on DC side with interleaved boost stages (cf. **Fig.4-5**) should be addressed in

future work. The current type passive rectifier using the LIT and inductors on DC side has been proposed [34] and the VA-rating of the LIT for the current-type is slightly increased from 13.4% to 13.7% [35] compared to the voltage-type. However, the difference of the VA-rating is very small and the current-type rectifier would bring an advantage that a maximum output power is higher due to no phase displacement on mains, i.e. the phase angle between the mains voltage and the current is equal if we could neglect the line impedance on the mains. Furthermore, the PLL to measure a phase angle of mains (cf. Fig.3-32) is not required and therefore the control circuit could be simplified. In the simulation result (cf. Fig.4-6(a)), the almost sinusoidal input currents are present even in the case of the constant duty cycle and the input currents are improved by the triangular modulation (cf. Fig.4-6(b)). It is noted that the pulsing currents flow to the diode bridge inputs  $(i_{1a}, i_{1b}, and i_{1c})$  and therefore a small filter is required as  $C_N$  and  $L_N$  to attenuate a switching frequency current ripple on mains. Since the inductance of  $L_N$  is very small, a line inductance on mains could be utilized for  $L_N$ . In Fig.4-6(b), the amplitude of the duty cycles  $d_1$  and  $d_2$  is lower to achieve a sinusoidal input currents compared to the voltage type, i.e. only  $\pm 0.1$  (0.4 to 0.6) variation for the duty cycles is used in this simulation. The current shapes are dependent on the inductance of L and the output voltage  $U_0$  which influence on



**Fig.4-5**: A current type hybrid 12-pulse line interphase transformer rectifier with interleaved boost stages.



**Fig.4-6**. The simulation results of the current-type hybrid rectifier (cf. Fig.4-5) using the constant duty cycle (a) and the triangular modulation (b) at  $D_{avg}$ =0.5 and  $U_O$ =505V<sub>dc</sub>. Circuit parameters:  $U_N$ =115V<sub>rms</sub>,  $f_{IN}$ =400Hz,  $P_O$ =10kW,  $f_S$ =100kHz, L=188µH,  $C_N$ =10µF,  $L_N$ =5µH, and  $C_O$ =1mF.



**Fig.4-7**. The simulation results as Fig.4-6 but  $D_{avg}$ =0.3 and  $U_0$ =358V<sub>dc</sub>.

di/dt of the diode bridge input currents after a switching state change. Therefore, the optimum modulation depends on an operating condition. In the case of  $D_{avg}$ =0.3 (cf. **Fig.4-7**), the input current shapes can be improved by the triangular modulation compared to the constant duty cycle. However, the low order harmonics still remain, which is similar to the feature of the voltage-type (Fig.3-35 and Fig.3-45). In further work, the optimum modulation functions and the optimum circuit parameters for the current-type hybrid rectifier will be derived. Moreover, both systems of the voltage-type and current-type will be compared concerning volume including an EMI filter, efficiency and controllability.

The boost stages can be replaced by the ESIs as shown in **Fig.4-8** [11]. In the simulation results (cf. **Fig.4-9**), the input current shapes are improved to sinusoidal by triangular modulation. It is noted that the power transistors in each ESI are driven by the same gate signal, e.g.  $d_1$  and  $d_2$  are used for the upper and lower side ESIs respectively. The pulsing currents flow to the diode bridge inputs, which is similar to the operation of the current-type hybrid 12-pulse rectifier with interleaved boost stages (cf. Fig.4-6 and Fig.4-7). The current-type hybrid 12-pulse rectifier using ESIs is advantageous compared to the passive rectifiers concerning input current



Fig.4-8: A current-type hybrid 12-pulse line interphase transformer rectifier using ESIs.

controllability. Furthermore, volume of *L* and/or the switching frequency current ripple might be reduced if the PWM control (cf. Fig.2-5 and Fig.2-6) can be employed, e.g. 3-level operation could be realized and then the equivalent frequency would be double. In future work, the control method to realize 3-level operation will be considered. Moreover, a control scheme to reduce the input current harmonics will be investigated. Finally, the current-type hybrid 12-pulse rectifier using ESIs will be compared to the passive rectifiers. In **Fig.4-10**, the ESI topology is applied to a 12-pulse rectifier with the isolation transformers and two ESIs are integrated (cf. Fig.4-8). Therefore, one pair of MOSFET and diode and one of the DC-link capacitors could be omitted. If the integrated ESI is applied to the 12-pulse rectifier with a non-isolated transformer like the LIT (cf. Fig.4-8), a zero sequence current would be present via the LIT and the partial currents ( $i_{rec1}$ ,  $i_{rec2}$ ) would not be balanced. However, there is no path for a zero sequence current in rectifiers employing isolation transformers (cf. Fig.4-10). In future work, the rectifier topology using the integrated ESIs will be investigated in detail.



**Fig.4-9**. The simulation results of the current-type hybrid rectifier using the ESIs (cf. Fig.4-8) and constant duty cycle (a) and the triangular modulation (b) at  $D_{avg} \approx 0.5$  and  $U_O = 247 V_{dc}$ . Circuit parameters:  $U_N = 115 V_{rms}$ ,  $f_{IN} = 400$ Hz,  $P_O = 10$ kW,  $f_S = 100$ kHz, L = 100µH, C = 1mF,  $U_C = 247$ V  $C_N = 10$ µF,  $L_N = 5$ µH, and  $C_O = 1$ mF.



**Fig.4-10**: A current-type hybrid 12-pulse rectifier where ESIs are applied to the interleaved boost stage and two ESIs are integrated.

# Chapter 5 Summary

In this thesis, two hybrid rectifier systems and the control schemes are proposed. The control schemes and the filtering concept of the rectifier using the Electronic Smoothing Inductor topology for practical realization are introduced. The rectifier has the ability to improve the input current quality and output voltage ripple. The 5kW prototype shows the high power density and a performance similar to that of a diode bridge rectifier using a large passive inductor. Hence the volume of a diode bridge rectifier can be reduced without impairing any characteristics by applying the proposed Electronic Smoothing Inductor systems.

The hybrid 12-pulse rectifier would be suitable for high mains frequency applications like aircraft and micro gas turbines. The rectifier can eliminate not only the 5<sup>th</sup> and 7<sup>th</sup> harmonics but also the 11<sup>th</sup> and higher harmonics, which results in a purely sinusoidal input current. Thus complex line interphase transformers like 18-pulse or 24-pulse devices are not necessary if the proposed topology is applied.

Both systems proposed in this thesis are hybrid and able to operate without driving the active switches. The rectifiers hence exhibit high reliability. This would greatly benefit not only aircraft applications but also others.
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