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ULTRA-FLAT ISOLATED SINGLE-PHASE AC-DC CONVERTER SYSTEMS

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Abstract

Ultra-flat power converter systems are highly demanded in modern applications, such as flat-screens, (O)LED lighting systems, smart surfaces, or automotive applications. The research in power electronics, however, has generally focused on cuboid-shaped converter systems as these shapes enable to use optimal components concerning efficiency and/or power density which are important figures of merit to quantify and compare the performance of power converters. For ultra-flat converters, however, high performance standard components are not applicable or available and thus the high efficiency of conventionally shaped systems might not be achieved. Nevertheless, the large surface area of an ultra-flat power converter comprises a superior cooling capability compared to cuboid-shaped systems and the lower efficiency might not compromise the power density. Obviously, the translation of figures of merit from conventionally shaped to ultra-flat systems is not directly feasible anymore and ultra-flat systems call for a distinct analysis related to the achievable performance.

This thesis analyzes the implications of an extreme height limitation of 1 mm on the converters efficiency and its power density presented for the example of a typical single-phase PFC rectifier with an output power of 200 W. In order to achieve the low thickness each component has to be integrated into the printed circuit board (PCB). **Chapter 1** presents a review of integration principles for power components which shows that sophisticated integration methods for capacitors and semiconductors already exist. The integration of magnetic components, however, remains to be solved in order to manufacture a 1 mm thin rectifier.

Besides the PCB-integration of power components also a thorough topology selection is crucial to build an ultra-flat rectifier. **Chapter 2** details the requirements on the topology based on the implications imposed by the PCB-integration. Based on this discussion, two topologies are identified to be suitable for the realization of a 1 mm thin PFC rectifier: a totem-pole-based boost-type rectifier discussed in **Chapter 3** and a flyback-type PFC rectifier presented in **Chapter 4**. Both topologies enable soft-switching which allows for a high switching frequency and therefore small passive components. Low switching losses are of particular interest as the generated power loss of each component has to be transferred through the PCB to the ambient. Furthermore, the proposed topologies allow to employ several paralleled and interleaved converter cells which utilize the superior cooling capability imposed by

the large surface as the power losses are distributed over the area.
For both topologies, the analysis, the design, and the control are described and validated by measurement results. For the boost-type rectifier a new modulation scheme is proposed which allows for ZVS over the entire mains period. For it, the nonlinearity of the MOSFETs' output capacitances has to be considered and a novel modeling approach is derived which includes this nonlinearity. The flyback converter is designed with respect to the implications imposed by the PCB-integration of the flyback transformer which is realized based on the design procedure presented in the next chapter.

The integration of the magnetic core into the PCB and windings composed of tracks and vias enable the implementation of extremely thin inductors and transformers. For it, specific implications concerning the anisotropy of the material, the allowable core losses per area, the isolation between the magnetic sheets, or the reluctance of the component have to be considered. **Chapter 5** presents a holistic design procedure for PCB-integrated inductors and transformers which takes all these specific properties into account. Measurements on a prototype of a PCB-integrated flyback transformer are used to validate the procedure.

In order to comply with international standards, a PFC rectifier requires an EMI filter. Conventionally employed EMI filters typically consist of small filter capacitances in order to keep the reactive power consumption low. To achieve the required attenuation large filter inductors are applied.
The PCB-integration of the cores limits the choice of applicable materials and a sophisticated core manufacturing process is needed as short-circuits between the magnetic foils result in an eddy-current caused impedance drop at higher frequencies which degrades the filter performance. The specific implications on the design of an ultra-flat EMI filter are presented in **Chapter 6**.

Chapter 7 of the thesis presents a conclusion of the achieved results and an outlook on topics for the continuation of research on ultra-flat PCB-integrated converter systems.

Kurzfassung

Die Nachfrage nach ultra-flachen leistungselektronischen Schaltungen für moderne Anwendungen, wie beispielsweise Flachbildschirme, (O)LED Beleuchtungen oder in der Automobilindustrie, ist hoch und ständig steigend. Der Fokus im Bereich leistungselektronischer Forschung lag bislang jedoch auf würfel- oder quaderförmigen Konvertern, die sich aus der Verwendung der jeweils optimalen Bauteile bezüglich Effizienz und/oder Leistungsdichte, die oft als wichtige Vergleichsparameter der Funktionalität eines Konverters angegeben werden, ergeben. Die spezifischen Bauelemente sind jedoch auf Grund ihrer Grösse für ultra-flache Systeme nicht mehr anwendbar, was dazu führt, dass das Effizienzniveau konventionell geformter Konverter nicht gehalten werden kann. Die flache Struktur bietet jedoch eine verhältnismässig grosse Oberfläche, die vorteilhaft für die Abführung der verursachten Verluste verwendet werden kann. Die Leistungsdichte des Konverters bleibt dadurch trotz der geringeren Effizienz unbeeinflusst. Allerdings können die bisherigen Betrachtungen bezüglich verschiedener Schlüsselkriterien von Leistungskonvertern nicht unmittelbar auf ultra-flache Systeme übertragen werden und eine separate Analyse der erreichbaren Funktionalität in Hinblick auf die Dicke des Systems ist notwendig.

Im Rahmen dieser Arbeit wird der Einfluss einer Höhenlimitierung des Gesamtsystems von 1 mm auf die Effizienz und die Leistungsdichte beispielhaft an einem einphasigen Gleichrichtersystems mit sinusförmigem Eingangsstrom und einer Ausgangsleistung von 200 W analysiert. Die extrem geringe Dicke des Konverters kann nur erreicht werden, wenn alle Komponenten in die Leiterplatte integriert werden. In diesem Kontext beschreibt **Kapitel 1** moderne Integrationsmethoden für die erforderlichen Bauelemente eines Leistungskonverters und es zeigt sich, dass Kondensatoren und Leistungshalbleiter durch ausgeklügelte Techniken in die Leiterplatte integriert werden können. Die Integration magnetischer Komponenten hingegen ist bislang nicht gelöst und erfordert die Erarbeitung geeigneter Lösungen, um einen Gleichrichter mit einer Dicke von nur 1 mm realisieren zu können.

Neben der Integration aller Komponenten in die Leiterplatte, stellt die Topologieauswahl einen weiteren wichtigen Punkt für die Realisierung des 1 mm dünnen Konverters dar. **Kapitel 2** stellt wichtige Aspekte mit Hinblick auf die extreme Höhe vor und identifiziert zwei Topologien, die sich als besonders vorteilhaft erweisen: Ein, von einer Hochsetzstellertopologie abgeleiteter Gleichrichter wird in **Kapitel 3**

diskutiert während ein, auf einem Flyback-Konverter basierender Gleichrichter in **Kapitel 4** präsentiert wird. Beide Topologien ermöglichen weiches Schalten, was eine hohe Schaltfrequenz und demzufolge kleine passive Bauteile erlaubt. Des Weiteren können die Topologien in mehrere parallel und zeitversetzt betriebene Teilsysteme unterteilt werden, was zur vorteilhaften Ausnutzung der guten thermischen Eigenschaften des ultra-flachen Volumens führt.
Entwurf und Reglerdesign beider Systeme werden beschrieben und durch Messungen an Prototypen verifiziert. Für den hochsetzstellerbasierenden Gleichrichter wird eine neues Modulationsverfahren vorgestellt, das weiches Schalten über die gesamte Netzperiode erlaubt. Die Modulation basiert auf einer detailierten Beschreibung der nichtlinearen Ausgangskapazitäten der verwendeten MOSFETs und diesbezüglich wird ein neues Model für diese Nichtlinearität erarbeitet und erläutert. Bei der Auslegung des Flyback-Konverters werden besonders die Einflüsse eines leiterplatten-integrierten Transformators berücksichtigt. Der Flyback-Transformator ist dabei basierend auf der in **Kapitel 5** vorgestellten Entwurfsmethode in die Leiterplatte integriert.

Die Integration des magnetischen Kerns in die Leiterplatte und die Realisierung der Wicklungen durch Leiterbahnen und Durchkontaktierungen erlauben den Aufbau magnetischer Komponenten extremer geringer Dicke. Das Design allerdings erfordert die Berücksichtigung verschiedener Effekte, die in Zusammenhang mit der Integration auftreten. Beispielsweise müssen die Anisotropie des Kernmaterials, die maximal zulässige flächenbezogene Verlustleistungsdichte, die Isolation zwischen den Kernschichten oder ein durchdachtes Reluktanzmodel des Kerns im Entwurf des magnetischen Bauteils berücksichtigt und eingearbeitet sein. **Kapitel 5** stellt daher einen gesamtheitlichen Designablauf für den Entwurf einer leiterplatten-integrierten Spule oder eines integrierten Transformators vor, der die erwähnten Besonderheiten mit einbezieht. Die theoretischen Überlegungen werden durch Messungen an einem Prototypen bestätigt.

Internationale Standards bezüglich der Netzqualität erfordern ein EMV Eingangsfilter eines aktiven Gleichrichters. Um die Blindleistungsaufnahme zu minimieren, verwenden herkömmlich entworfene EMV Filter möglichst kleine Kapazitäten, während grosse Filterspulen eingesetzt werden, um die erforderliche Dämpfung zu erreichen. Die Integration der magnetischen Kerne beschränkt jedoch die Auswahl der verfügbaren Materialen und die fertigungstechnischen Anforderun-

gen an die Kernherstellung sind für EMV Spulen besonders hoch, da Kurzschlüsse zwischen magnetischen Folien Wirbelströmen hervorrufen, die zu einer Verringerung der Impedanzen und demzufolge der Filterdämpfung insbesondere bei hohen Frequenzen führen. Die spezifischen Einflüsse der Leiterplatten-Integration auf den EMV Filterentwurf werden in **Kapitel 6** beschrieben.

Abschliessend werden die erzielten Resultate dieser Arbeit in **Kapitel 7** zusammengefasst und ein Ausblick auf zukünftige Forschungsthemen und Anwendungen ist gegeben.

Glossary

Abbreviations

2-D	...	two dimensional
3-D	...	three dimensional
BCM	...	boundary conduction mode
CCM	...	continuous conduction mode
CE	...	conducted emission
CiP	...	chip in polymer
CISPR	...	Comité International Spécial des Perturbations Radioélectriques
CM	...	common mode
CUT	...	core under test
DAB	...	dual active bridge
DCM	...	discontinuous conduction mode
DF	...	displacement factor
DM	...	differential mode
DSP	...	digital signal processor
DPF EMI	...	electro-magnetic compatibility
ESR	...	equivalent series resistance
FEM	...	finite element method
FPC	...	ferrite polymer compound
FPGA	...	field programmable gate array
HF	...	high frequency
IEC	...	International Electrotechnical Commission
LED	...	light emitting diode
LF	...	low frequency
LISN	...	line impedance stabilization network
MID	...	molded interconnection device
NL	...	noise level
OLED	...	organic light emitting diode
PCB	...	printed cirucit board

PF	...	power factor
PFC	...	power factor correction
RMS	...	root mean square
SEPIC	...	single ended primary inductance converter
SMD	...	surface mounted device
TCM	...	triangular current mode
THD	...	total harmonic distortion
TV	...	television
VS	...	valley switching
ZVS	...	zero voltage switching

Principle notation

x	...	instantaneous value of x
$\bar{x}$	...	local average value with regard to a switching cycle of x
x_{rms}	...	local RMS value with regard to a switching cycle of x
X	...	global RMS or Dc value of x
$\hat{X}$	...	peak value of x
$\bar{X}$	...	quiescent value of x
$\hat{x}$	...	small-signal value of x
$x^{'}$	...	quantity x referred to the primary side of a transformer

Contents

1 Introduction

1.1 Motivation

The trend towards flat, flexible, mobile, or stylish electronic systems can be observed in many consumer applications. For instance, for solar energy systems recently cost-efficient thin film solar cells in very large modules have been presented and the mass production is about to emerge [1]. **Fig. 1.1** (a) shows an example of a thin film solar cell which is a flexible and mobile power source and can be applied for remote or mobile energy harvesting. In order to avoid the overall system to become bulky an appropriate power converter is necessary which should preferably show a similar aspect ratio[1] yielding a very thin overall system. In that regard, [2] reports the design and the implementation of a 25 W single-phase inverter with a thickness of 4 mm (incl. PCB). The inverter is aimed for a direct system integration of the thin-film solar cell including the converter into building materials, e.g. a roof shingle, which would considerably reduce the costs of installation and represent an important step for solar energy systems to be competitive to fossil energy sources [3, 4].

Other recent applications for ultra-flat power converters are drivers for OLED flat screens or OLED lighting systems [5–8]. OLED lighting systems, cf. **Fig. 1.1** (b), are increasingly becoming an important source of light as they are thin, flat, light-weight, and flexible at a reasonable illumination efficiency (up to $50 - 75\,\mathrm{lm/W}$) [9, 10]. Contrary to LED

[1] The aspect ratio $r = h/\sqrt{a\,b}$ is defined as the ratio between the height h and the characteristic linear dimension area of a cuboid-shaped box with length a and width b.

lights, OLEDs are wide-area light sources which allow for a discreet and planar illumination of rooms. The color of the light and the off-state appearance of the lamp, e.g. black, white, or transparent, can be chosen which makes the lamps attractive for stylish and modern applications. The OLED lamp features a height of typically 1.5 . . . 2 mm [9, 11].
The OLED technology is also applied to flat screens and flexible displays, cf. **Fig. 1.1** (c). Recently, a commercially available OLED TV (55" wide screen) with a thickness of only 4 mm emerged on the market [12]. Unfortunately, the bulky power supply has to be packed into the screen's holder which determines the size and the application of the screen. With an ultra-flat power supply the screen could be installed in floors, ceilings, and walls without further ado and the ultra-flat shape of the screen could really be utilized. A prominent application for ultra-flat screens are smart surfaces. **Fig. 1.1** (d) shows a table which con-

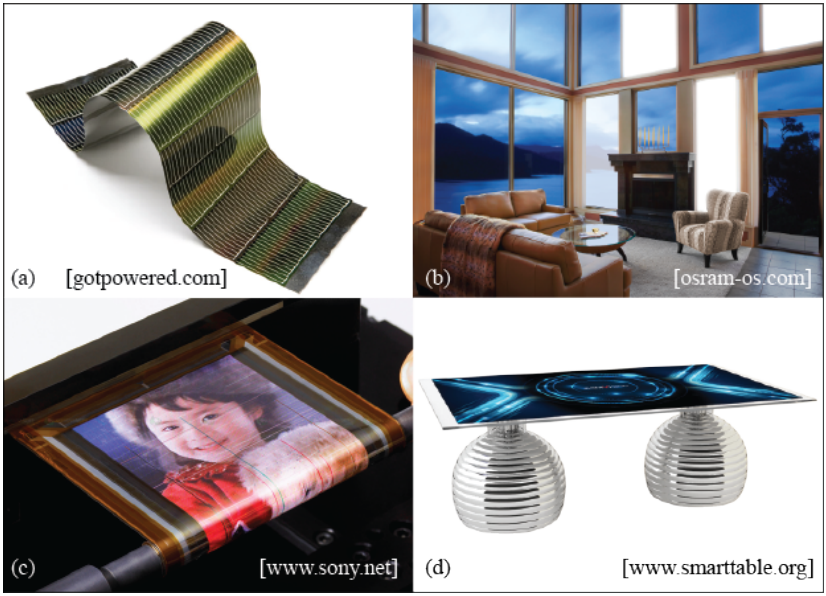


Fig. 1.1: Applications for ultra-flat power converters: (a) Thin film solar cells; (b) OLED lighting systems; (c) Flexible OLED displays; (d) Smart surfaces, here realized as a table with a touch sensitive desk top.

sists of an intelligent touch screen desktop. Similar to ultra-flat TV, the power supply unit is packed into the table legs. In order to decrease the size of smart surface systems, the employment of converter systems with extreme aspect ratios is crucial [13].

Obviously, both applications, OLED lamps and OLED screens, would take advantage if the power unit could also feature an ultra-flat shape. Recent publications [6, 10, 14], which take the thickness of the converter into consideration, report a height of only 6 mm for a 60 W resonant DC-DC converter employed as OLED lamp driver. There, the resonance capacitor as well as the transformer are integrated into the printed circuit board (PCB) whereas the transformer core consists of ferrite polymer compound (FPC) layers [15].

The presented applications and the increasing research activity confirm the demand for ultra-flat power systems. However, the minimum height achieved so far for low power DC-DC converters, e.g. $P = 60\,\mathrm{W}$, is still more than 4 mm [10] whereas the minimum height of single-phase power factor correction (PFC) rectifiers, which are usually used as front-end power stage, is typically between $1 \ldots 2\,\mathrm{cm}$ for 70 W systems [16]. A thorough analysis which pushes the height limitation of rectifier systems down to 1 mm has not yet been done and therefore, the converter systems presented in this thesis are aimed to outperform the state-of-the-art height requirement by a factor of 10 and to realize PFC rectifier systems with a rated power of 200 W and a total thickness of only

$$h = 1\,\mathrm{mm}.$$

Over the last decades, the evolution of power electronic systems has shown a trend towards higher power densities, either due to limited space requirements [17] or indirectly driven by cost and/or weight reductions (aircraft applications [18, 19], server farms [20]). In the systems presented in [17–20], the increase of power density is accompanied by an increase of efficiency as the reduced volume provides less surface area for power loss dissipation.

During the last years rising energy costs and increasing environmental awareness have shifted the focus towards highly-efficient power systems. Converter systems with ultra-high efficiency, however, are large and expensive [21]. For that reason, the economic realization requires a trade-off between the power density ρ and the efficiency η of a converter system for which the ρ-η-Pareto Front, e.g. presented in [22], is a vivid representation. The analyses in [20–22], however, are based on cube-

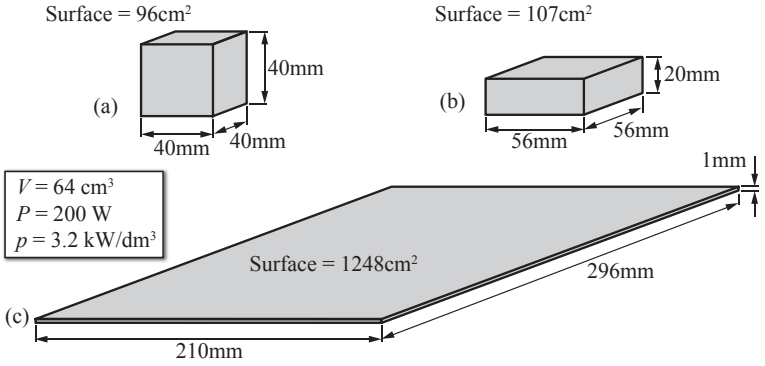


Fig. 1.2: Comparison of the surface areas for different converter outlines at constant volume of $V = 64\,\mathrm{cm}^3$ and an output power of $P = 200\,\mathrm{W}$.

shaped converter systems and needs to be modified for flat converters, since most of the components, e.g. inductors and capacitors, are subject to particular limitations [23].

As typical benchmark indicators used in power electronics, the power density and the efficiency allow for a fair comparison between several power converter systems. The power density is a major figure of merit as it specifies the power which can be transferred for a given converter volume. It is desirable to achieve a high power density in order to obtain compact, light-weight, and cost-efficient power converters. State-of-the-art single-phase PFC rectifiers achieve a power density of about $1.5\,\mathrm{kW/dm}^3$ [24]; up-to-date literature documents PFC rectifiers with a power density of over $5\,\mathrm{kW/dm}^3$ for a cuboid-shaped volume[2] ($62 \times 34.5 \times 25.5\,\mathrm{mm}^3$) [25].

Compared to cuboid-shaped boundary boxes, an ultra-flat converter system features a large surface with respect to its volume, e.g. $1248\,\mathrm{cm}^2$ in **Fig. 1.2** (c). A large surface results in an improved heat dissipation ability, i.e. the heat caused by the converter's losses can easily be removed by means of the large surface. **Fig. 1.2** (a) and **Fig. 1.2** (b) depict typical cuboid-shaped volumes with comparably small surfaces

[2]The volume of a power converter is defined by a cuboid-shaped boundary box around the outlines of the system.

of 96 cm^2 and 107 cm^2, respectively. As a consequence, less heat can be dissipated and thus less losses are tolerated in such systems. The shape of the converter already limits the minimal allowable efficiency for a given power density.
Ultra-flat power electronic systems, however, might not achieve the high efficiency of cuboid-shaped systems due to the suboptimal components which have to be employed in order to meet the height limitation. Still, it is expected that the power density can be kept constant by reason of the large surface available for heat dissipation.

Obviously, the translation of performance indicates, e.g. power density or efficiency, from conventionally shaped to ultra-flat systems is not directly feasible and ultra-flat systems require for a distinct analysis related to the achievable performance.

In that context, the conducted research focuses on the analysis and the comprehension of the implications of the extremely low converter height on the efficiency and on the total footprint size required for a galvanically isolated single-phase PFC rectifier. With respect to the stringent height limitation, the converter systems are entitled as *Power Sheets* [23].

1.2 Specifications

As already mentioned, PCB-integrated converter systems with a thickness of not more than 1 mm are beneficial for various applications. **Tab. 1.1** lists several conventional products which would benefit from an ultra-flat power supply and it can be seen that apart from plasma screens the power consumption is typically between 5 W and 200 W. In that regard, the output power of the investigated converter systems is specified to be $P_{\mathrm{out}} = 200\,\mathrm{W}$ as the systems could easily be downscaled. The power converters consist of either a single-phase PFC rectifier and a series-connected DC-DC converter with galvanic isolation or a single-stage topology which enables a sinusoidal input current, the galvanic isolation, and the output voltage regulation in one conversion step.

The converters are aimed for the European low-voltage grid with an input voltage of $V_{\mathrm{n}} = 230\,\mathrm{V}$ and a mains frequency of $f_{\mathrm{m}} = 50\,\mathrm{Hz}$. The output voltage is defined to be $V_{\mathrm{out}} = 20\,\mathrm{V}$ which is a widely used voltage level for many applications, e.g. laptops chargers. The output voltage, however, can be adjusted to other levels without changing the topology. Since the applications listed in **Tab. 1.1** are targeted for the

Tab. 1.1: Power consumption of typical applications for ultra-flat converters.

Application	Power consumption	Source	
Laptop charger	50 W . . . 90 W	Lenovo	[26]
LED flat screen	60 W . . . 80 W	Samsung	[27]
OLED screen	100 W . . . 180 W	LG	[12]
Plasma screen	150 W . . . 500 W	Samsung	[27]
LED panel	12 W . . . 60 W	abalight, Derun	[28, 29]
OLED panel	5 W . . . 10 W	Philips, Osram	[9, 11]

use in residential environments the EMI filters of PFC rectifiers are specified to comply with the EMI standard CISPR 11, Class B [30].

In the context of safety standards for the use in residential environments, a further specification of the *Power Sheet* is the galvanic isolation. Therefore, a transformer is required which withstands a test voltage of 1500 V for 60 s [31]. In order to achieve this isolation voltage with a PCB-integrated transformer high voltage PCB layers can be applied which are already commercially available and applied to high voltage gate drivers [32, 33].

Tab. 1.2 lists the specifications and **Fig. 1.3** depicts the block diagram of the considered power converters.

PFC rectifiers have to provide energy to the load in case of a mains failure for a certain time (typ. 20 ms in a 50 Hz system). This hold-up time is typically ensured by applying a large electrolytic capacitor either in the DC link or at the output of the converter. So far no ultra-flat electrolytic capacitors with a thickness of 1 mm, a capacitance value of several µF, and a rated voltage of 25 V are available and the realization of a large capacitance with thin ceramic capacitors would require a large area. As a consequence, with current technology, the hold-up time requirement can not yet be fulfilled with reasonable converter area.

1.3 PCB-integration of power components

The implementation of 1 mm thin converter systems can only be achieved if each component of the converter is integrated into the PCB. The PCB-integration of the components has a major impact on the performance of the converter as conventionally used elements cannot

Tab. 1.2: Specifications of the *Power Sheet* at a thickness of 1 mm.

Quantity		Value
V_{n}	=	230 V
f_{m}	=	50 Hz
V_{out}	=	20 V
P_{out}	=	200 W
T_{amb}	=	45 °C
EMI limit: CISPR 11, Class B		
Galvanically isolated, 1.5 kV		

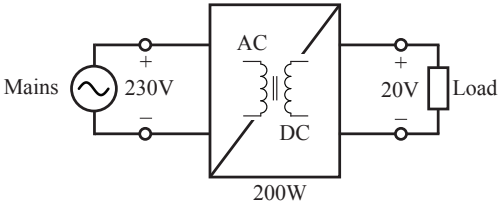


Fig. 1.3: Block diagram of the *Power Sheet*.

be applied anymore and only devices with a thickness lower than 1 mm are possible to integrate. In that respect, sophisticated methods to embed the components into the PCB are presented in this section.

1.3.1 Integrated capacitors

PCB-integrated capacitors are state-of-the-art in high frequency applications where the capacitors are used as filter and/or matching capacitors. There, only small capacitance values in the range of several pF are required and the applied voltage is in the range of only a few volts [34–36].

In power electronic systems, however, capacitances of up to several hundred µF are needed as output or Dc link capacitors. Moreover, these applications require for a high voltage rating of the capacitors since the Dc voltage of a boost-type PFC rectifier with an input voltage of 230 V is roughly 400 V. Thus, capacitors for power converters have to be rated for high voltages up to several hundreds of Volts.

The PCB-integration of capacitors can be divided into two meth-

Tab. 1.3: Available materials for embedded capacitors.

	Faradflex	**DuPont** HK04	**3M** C-ply
C/Area ($\mathrm{nF/cm^2}$)	0.57	0.26	1.25
$\tan(\delta)$	0.016 @ 1 MHz	0.005 @ 1 MHz	0.005 @ 1 kHz
$E_{\max}$ (kV/mm)	400	315	130
Thickness (µm)	8	12	11
Source:	faradflex.com	dupont.com	3m.com

ods [37]. Either separate chips and/or specifically manufactured parts are embedded into the PCB or structured layers composed of capacitive material can be employed.

Capacitive layers suitable for the PCB-integration are available and several publications report the successful PCB-integration of filter or resonance capacitors in power converters [38, 39]. The employed materials are either FR4 laminates which are enhanced with high dielectric powder or polymer compounds [37,40]. Although capacitive layers offer the benefit of low cost and large scale manufacturing because the integration process is compatible with the standard PCB manufacturing process, the achievable capacitance density is low and so far, no publication reports the utilization of capacitive layers for high voltages, e.g. as a DC link capacitor, which is a major challenge to the manufacturing process and the material. **Tab. 1.3** lists the properties of available capacitive materials. Detailed datasheet information about the capacitance degradation with increasing temperature or applied voltage is not available.

The second integration method is to integrate SMD capacitor chips directly into the PCB. For this, SMD chips with a very low profile are necessary. Murata [41] already offers a wide spectrum of ultra-flat capacitor chips, e.g. 10 µF/25 V in a 0603 footprint, and ultra-thin 1005

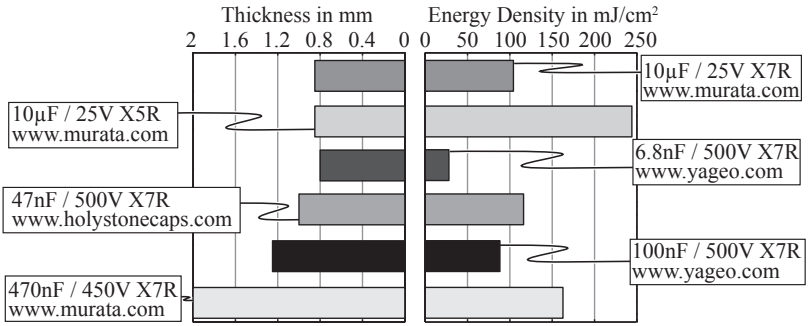


Fig. 1.4: Energy density of available chip capacitors. The calculation does not consider the capacitance drop over the voltage range.

chips with a thickness of only 50 µm are available (100 nF/4 V) [41]. Holystone [42] also has a chip series which is addressed to height restricted applications. A line-up of achievable energy densities per area for available capacitor chips is given in **Fig. 1.4**.

Capacitors with high voltage capabilities are also commercially available. A capacitor (47 nF/500 V) with a profile of 1 mm is available by [42]. Larger capacitance values can be found at the expense of an increased thickness, cf. **Fig. 1.4**, (470 nF/450 V, 1210 package, $h = 2$ mm [41]). X2 capacitors which are important for EMI filtering are already available by Murata and Holystone with acceptable capacitance values (56 nF/230 V). However, the packages are typically 2 . . . 3 mm thick. There are, of course, other chip manufacturer which also have thin chips in their portfolio [43–48].

The integration of capacitors is challenging as the height restriction of 1 mm is a stringent limit for off-the-shelf components. However, as chip manufacturer continuously increase the energy density and/or decrease the size of the packages it is a matter of time until the 1 mm limit can be met for all capacitors needed in a power converter. Specific components could already be manufactured.

The capacitors for the prototypes in this thesis are realized with newest available capacitor technology and the chips could directly be integrated into the PCB.

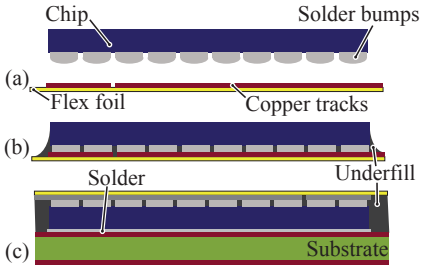


Fig. 1.5: Flip-chip integration principle where in (a) the chip with solder bumps is placed on a flexfoil. (b) Soldering of the bumps and underfill. (c) Soldering of the chip onto a substrate.

1.3.2 Integrated active components

The integration of active components into the PCB is a further important step for a low profile electronic system. Similar to PCB-integrated capacitors, integrated actives can also be divided into two methods: either the bare chip is embedded in the PCB or an ultra-flat package can directly be integrated into the PCB.

Integration of the bare chip

The direct PCB-integration of a semiconductor chip has the advantage of allowing a compact setup and also features improved electrical and thermal properties compared to wire bonded chips because the bonding wires limit the current rating and furthermore, in case of power switches the bonding implies a parasitic inductance which causes over-voltages during switching transitions.

Since integrated chips are directly soldered to a substrate or a foil, bond wires are avoided which reduces the parasitic inductance and as a large area of the dice (up to 80 % of the chip area) is connected the current carrying capability as well as the thermal conductivity increases. Compared to conventional wire-bonded assemblies, the embedded chips can be considered to be cooled on both sides as top and bottom surface of the dice are soldered to a metallized substrate which increases the thermal conductivity. The double-sided cooling achieves an improvement in thermal conductivity of up to 44 % compared to a wire-bonded chip [49]. These values are strongly affected by the chip area which is

contacted and it is beneficial to connect as much area as possible.
A further advantage of integrated chips is the possibility of 3-D routing which enhances the flexibility of the interconnection compared to 2-D routing. This allows for short interconnections between components and, consequently, a small impedance which reduces the susceptibility to HF interferences [50, 51].

Recent studies have investigated integration methods [52–55] whereas the flip-chip assembly, the chip-in-polymer (CiP) approach, and the molded interconnect device (MID) are of particular interest for power electronic converter systems.

Flip-chip assemblies

Flip-chip assemblies have been state-of-the-art for many years. Originally, they were used for processor chips with many connections which could no more be wire bonded. Nowadays, this technique is used for almost any kind of chip as for example for mobile communication devices and sensor packaging. The flip-chip integration is also applied to power electronic switches which is discussed in [53]. The integration principle can be seen in **Fig. 1.5** where in (a) the chip with solder bumps is placed on a flex foil. The flex foil allows an integration of chips or other components with different thicknesses next to each other. After the bumps are soldered in a reflow process an underfill is placed, cf. **Fig. 1.5** (b), which fills out all cavities. The underfill determines the stability and the thermal properties of the assembly and is therefore essential with regard to reliability. After this process the assembly is flipped and the other side of the chip is soldered to a substrate, cf. **Fig. 1.5** (c).

The heat transfer of a flip-chip assembly is strongly affected by the solder bumps and the flex foil. Compared to copper, these bumps and the flex foil have a rather high thermal resistance and thus the flip-chip approach has to be considered as a single-sided cooling assembly from a thermal point of view. The thermal improvement is only about $5 \ldots 15\,\%$ compared to wire-bonded chips [49].

Prototypes have already been built with a half bridge consisting of OptiMOS switches by Infineon [56]. [53] and [57] show that the stray inductance of the chip can be significantly reduced ($4 - 8\,\mathrm{nH}$) compared to wire-bonded MOSFETs ($13 - 15\,\mathrm{nH}$ in a TO220 package). Furthermore, the on-resistance could be reduced to $R_{\mathrm{DS(on)}} = 3.7\,\mathrm{m\Omega}$, e.g. compared to $4.1 - 5.6\,\mathrm{m\Omega}$ for a TO220 package. **Tab. 1.4** lists the

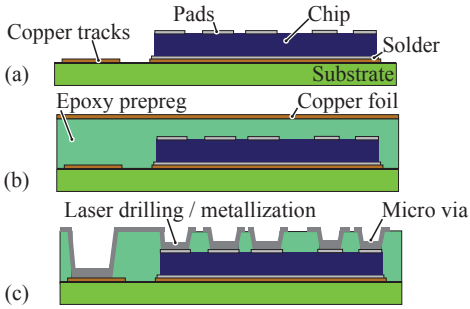


Fig. 1.6: Chip in polymer setup. (a) Soldering and adhesion of the chip onto a substrate. (b) Lamination of the chip with an epoxy prepreg layer covered by a copper foil. (c) Laser drilling and metallization of micro vias.

parameters of the measurement setup discussed in [53].

Chip in polymer approach

The chip in polymer (CiP) approach can also be applied for power switches [52, 53]. The fabrication process is depicted in **Fig. 1.6**. Contrary to flip-chip methods, the thin chip ($<50\,\mu m$) is glued and soldered to a substrate and subsequently a standard vacuum lamination process takes place, cf. **Fig. 1.6** (b). Due to the adhesion of the chip the mechanical and the electrical connection to the substrate are separated which increases the reliability compared to flip-chip assemblies. After the lamination process, the connections to the chip are realized using micro vias which are laser drilled and subsequently metallized, cf. **Fig. 1.6** (c). The copper vias have a low thermal resistance and therefore an improved thermal behavior is observed compared to the flip-chip approach. Furthermore, the micro vias have a low electrical impedance and hence a large bandwidth can be achieved [53].

If several chips are to be embedded with different thicknesses the lamination process balances the differences so that a planar layer can be achieved. With this method active and passive components could be integrated in a single step.

An implemented prototype half bridge with OptiMOS switches [56] has been reported in [53], cf. **Tab. 1.4**.

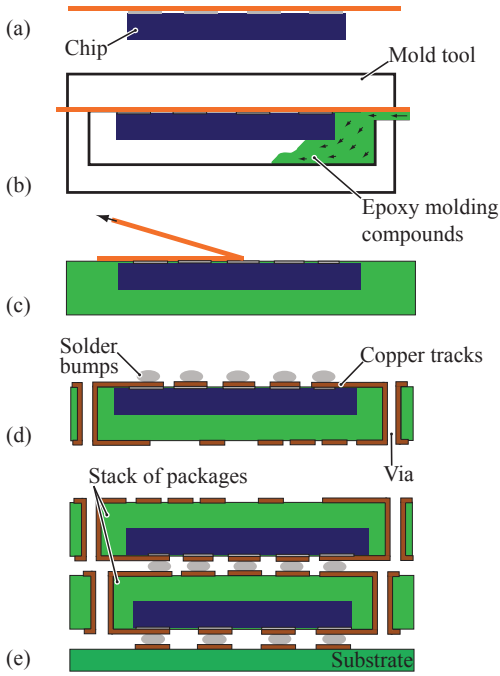


Fig. 1.7: Schematic of MID stack. Due to the vertical arrangement only short interconnections are required.

Molded interconnection device technology

The integration of microcontrollers, memory chips, or FPGAs can be done with the molded interconnection device (MID) technology [52]. **Fig. 1.7** shows the manufacturing process. The chip is first adhered to a removable foil, cf. **Fig. 1.7** (a), which is then encapsulated by a mold tool into which an epoxy molding compound is injected, cf. **Fig. 1.7** (b). This compound is the carrier of the chip and it is crucial that the thermal expansion coefficient is matched to the assembly. After this step the foil is removed, pads are metallized, vias are drilled, and solder bumps are placed on the pads, cf. **Fig. 1.7** (c) and (d). This package can now be flipped and stacked on other packages which enables very short interconnection distances and a very high bandwidth. For instance, the

Tab. 1.4: Implemented prototypes described in the literature with integrated active power electronic components.

Flip Chip	Half bridge leg [53]: Infineon OptiMOS 100 V (Area: 26 mm^2) Diodes: IXZA DWS (36–80 A) $V = 40\,V$, $I = 25\,A$
CiP	Half bridge leg [53]: Infineon OptiMOS 55 V Diodes: IR 30CPQ100 [58] $V = 30\,V$, $I = 25\,A$
MID	3-D package stack for automotive applications [52]: 76 I/O's
Embedded power technology	Half bridge leg with gate drive circuit [54]: Switches: IXFD24N50-7X $V = 400\,V$, $I = 10\,A$, $f_S = 500\,kHz$ Area: $8.84 \times 7.18\,mm^2$, $T_{max} = 125\,°C$

connection distance of a DSP and a FPGA could be minimized using this technique.
[52] reports the realization of a prototype for automotive applications with 76 I/O pins, cf. **Tab. 1.4**. Since the cooling of a MID assembly is difficult due to the stacked structure, the MID is only interesting for DSP or other control chips and not for power semiconductors.

Besides the presented technologies there are further more specific methods to integrate the bare chip into the PCB. In [54, 55] voltages up to 400 V and currents up to 50 A have been applied to integrated switches with integration methods which are related to the flip-chip technology. Good results were presented concerning internal inductance and thermal management.

Integration of semiconductor packages

An easy and straightforward way to integrate active switches into the PCB is to bury the chip together with its package. This, of course,

Tab. 1.5: Commercially available MOSFETs with a low thickness.

Type	V_{DS} (V)	$R_{DS(on)}$ (mΩ)	**Package**	**Height** (mm)
IPL60R199CP [56]	650	199	ThinPAK	1.0
STL57N65M5 [59]	650	69	PowerFLAT	0.9
STL23N85K5 [59]	850	200	PowerFLAT	0.9
SiZ916DT [60]	30	1.3	PowerPAIR	0.75
IRLH5030PbF [58]	100	9.9	PQFN	0.83

requires for thin packages. Semiconductor manufacturers recently introduced MOSFETs with a package as thin as 1 mm or less. **Tab. 1.5** lists off-the-shelf switches with different voltage rating featuring a flat package. The ongoing research in packaging technologies will further decrease the size of the packages and the steadily increasing portfolio of flat packages will spread out to many more types of switches. Although the previously presented integration methods achieve an even flatter assembly the direct PCB-integration of switches benefits from its simple and cost effective manufacturability which also results in a shorter production time for a prototype.

The integration of signal components like DSP, FPGA, or OpAmps within their packages cannot be applied for all components as the packages are yet too thick. For these components only an integration of the bare chip would result in the desired thickness as smaller packages are not yet available. In **Tab. 1.6** an overview of signal components their packages and the respective thickness is given. Still, these components also benefit from the efforts made in packaging technology and flatter chips might be available in future.

The previous discussion about the PCB-integration of power switches reveals that the integration of the overall package appears to be the most appropriate way to implement the *Power Sheet* as it is a simple and time efficient approach.

1.3.3 Integrated magnetic components

Besides capacitors and switches, the third member in the family of power electronic components are magnetic devices. Considerable effort

Tab. 1.6: Typical packages of signal components.

Component	Example	Package	Height
DSP	TMS320F2808	S-PBGA	1.4 mm
FPGA	LCMX0228	fpBGA	1.1 mm
Signal coupler	ADuM1100	SOIC-8	1.5 mm
OPV	LPV358	R-PDSO-G8	0.9 mm
Comparator	LT1715	MSOP-10	0.86 mm
Gate Drive	IXDN402	SOP-8	1.5 mm

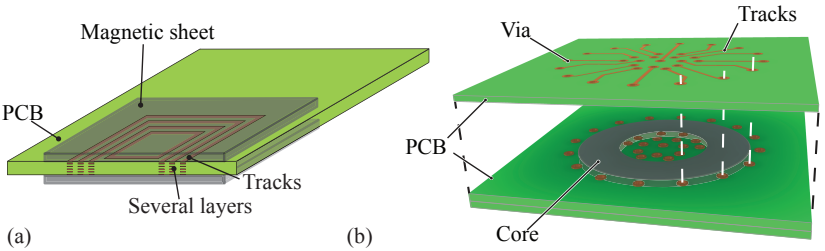


Fig. 1.8: Basic principles to realize a PCB-integrated inductor: (a) PCB-track windings on several layers which are covered with magnetic sheets on top and bottom. (b) PCB-integrated core and the windings are realized as tracks and vias.

has already been made to reduce the size and to integrate magnetic components into the PCB, e.g. [38, 61, 62]. For low power and high frequency converters these methods are well applied [38, 62]. For the realization of a single-phase AC-DC PFC rectifier, however, so far no inductors or transformers with a thickness of 1 mm have been presented and it states a major challenge to get there.

In principle, there are two possibilities to integrate a transformer or an inductor into the PCB. The first is to realize the windings as PCB tracks and to place magnetic sheets on top and bottom of the PCB, cf. **Fig. 1.8** (a). The magnetic sheets reduce the reluctance of the setup resulting in a higher inductance value for a given number of turns. The distance between the two magnetic foils is usually determined by the thickness of the PCB and this distance is basically an air gap. The

achievable area-related energy density is therefore rather low.

The second integration method is to integrate the core into the PCB and to realize the windings as PCB tracks and vias. **Fig. 1.8** (b) presents the setup of a toroidally wound core. However, a stack of magnetic foils can also be integrated which allows for almost arbitrary core shapes. Compared to the first integration principle, this integration method facilitates a closed core configuration and an air gap can be designed to adjust the indcutance value. As a consequence, the energy density is higher compared to the first integration method.

In this context, Chapter 5 gives a brief overview of achieved results with regard to ultra-flat magnetics and identifies the integration method presented in **Fig. 1.8** (b) to be most appropriate for the realization of magnetic components needed for the implementation of a 1 mm thin PFC rectifier system.

1.4 Objectives and new contributions of this work

The objective of this thesis is to select, analyze, design, and experimantally verify a converter topology which enables the implementation of the ultra-flat single-phase PFC rectifier specified in Section 1.2. The main challenge to achieve this goal is the design, the optimization, and the realization of ultra-flat magnetic components which determine the achievable efficiency and the achievable power density of the rectifier.

The new contributions of this work are:

- a new modulation scheme for a totem-pole based PFC rectifier which enables ZVS over the entire mains period; in that context, a simplified analytical model of the nonlinear output capacitances of the employed MOSFETs is derived which allows for a closed-form converter description and thus for an analytical system optimization;
- the analysis, the design, and the implementation of a single-phase flyback-type PFC rectifier system which employs a PCB-integrated flyback transformer;
- a method to integrate magnetic components into the PCB with almost arbitrary core shapes that allows for the implementation of inductors and transformes required in single-phase PFC rectifiers;

- the elaboration of several implications imposed by the PCB-integration which include anisotropic core losses, the requirement for isolation between the magnetic sheets, a proper reluctance model needed for the air gap calculation, the definition of a maximum allowable power loss per area, and methods to reduce the leakage inductance for transformer applications;
- a multi-objective optimization procedure for PCB-integrated magnetic components with respect to the efficiency and/or the area-related power density of the magnetic component;
- a guideline for the design and the realization of an ultra-flat EMI filter with PCB-integrated filter inductors.

1.5 Outline of the thesis

The thesis is aimed to cover all important aspects for the design and the implementation of an ultra-flat power electronic system.

Chapter 1 starts with a motivation to the topic and states the specifications for the converters under investigation. Moreover, an overview of recent integration methods for power electronic components is given.

Chapter 2 discusses important topology requirements with regard to the PCB-integration of all components. Based on the discussion an appropriate topology selection for an ultra-flat converter system is feasible.

Chapter 3 details the design, the control, and the implementation of a boost-type PFC rectifier which features a new modulation scheme in order to achieve soft switching over the entire mains period. For it, a model for the nonlinear capacitances of the applied switches is introduced. The theory is verified by measurements on a prototype.

Chapter 4 presents a flyback-type PFC rectifier with a PCB-integrated flyback transformer. The design of each component and the control synthesis is detailed and validated with measurements on a prototype.

Chapter 5 comprehends the PCB integration of magnetic components. Several specific issues are illuminated and a holistic design procedure is proposed which allows for the optimal design of PCB-integrated inductors and/or transformers with respect to the efficiency and/or the power density.

Chapter 6 investigates the impact of the PCB-integration on the design of an EMI filter for the flyback-type PFC rectifier. It is shown that with an adequate core manufacturing the implementation of an ultra-flat filter which complies with the specified standard is possible.

Chapter 7 concludes the thesis with a discussion of the achieved results and gives an outlook on possible future research works.

1.6 List of publications

Different parts of this thesis have been published in international journals or conference proceedings. These publications are listed below.

Conference papers

1. C. Marxgut, J. Mühlethaler, F. Krismer, and J. W. Kolar, *Multi-objective optimization of ultra-flat magnetic components with a PCB-integrated core*, in Proc. of the 8th IEEE/IEEJ International Conference on Power Electronics (IPEC & ECCE Asia), Jeju, South Korea, May 30-June 3, 2011.

2. C. Marxgut, J. Biela, J. W. Kolar, *Interleaved Triangular Current Mode (TCM) resonant transition, single-phase PFC rectifier with high efficiency and high power density*, in Proc. of the IEEE/IEEJ International Power Electronics Conference (IPEC & ECCE Asia), Sapporo, Japan, June 21-24, 2010.

3. C. Marxgut, J. Biela, J. W. Kolar, *Design of a multi-cell, DCM PFC rectifier for a* 1 mm *thick,* 200 W *off-line power supply - The Power Sheet*, in Proc. of the 6th IEEE International Conference on Integrated Power Electronic Systems (CIPS), Nuremburg, Germany, March 16-18, 2010.

4. C. Marxgut, J. Biela, J. W. Kolar, *DC-DC converter for gate power supplies with an optimal air transformer*, in Proc. of the 25th IEEE Applied Power Electronics Conference and Exposition (APEC), Palm Springs, CA, February 21-25, 2010.

Journal papers

1. C. Marxgut, F. Krismer, D. Bortis, J. W. Kolar, *Ultra-flat interleaved Triangular Current Mode (TCM) single-phase PFC rectifier*, IEEE Transactions on Power Electronics, Vol. 29, No. 2, pp. 873–882, February 2014.

2. C. Marxgut, J. Mühlethaler, F. Krismer, J. W. Kolar, *Multi-objective optimization of ultra-flat magnetic components with PCB-integrated core*, IEEE Transactions on Power Electronics, Vol. 28, No. 7, pp. 3591–3602, July 2013.

Patents

1. J. W. Kolar, J. Miniböck, J. Biela, C. Marxgut, *Bidirektionaler, verlustarm schaltender AC-DC-Konverter*, filed 17th Sept. 2009.

2. J. Biela, C. Marxgut, J. W. Kolar, *Träger für eine elektronische Schaltung*, CH 701761 A2.

2 Topologies

Besides the integration of all components into the PCB, a proper topology selection is also crucial for the successful implementation of an ultra-flat converter system with a thickness of only 1 mm.

Therefore, this chapter highlights important issues with regard to the implications imposed by the PCB-integration. Based on the requirements, the topology can be selected whereby two-stage and single-stage converter architectures are considered. For both types, a PFC rectifier has been implemented which is detailed in Chapter 3 and Chapter 4, respectively.

2.1 Topology requirements

In the design of power electronic converters, there has always been a trend towards lower volume and/or higher power density, which is driven by a general requirement for decreasing functional volume and cost [63]. Recently, environmental issues are of increasing interest, and therefore also the efficiency of converter systems is of major concern. Thus, the design of a power electronic converter has to consider multiple objectives:

- Minimizing the volume and thus maximizing the power density,
- Minimizing the weight,
- Maximizing the efficiency,
- Minimizing costs,
- Maximizing reliability.

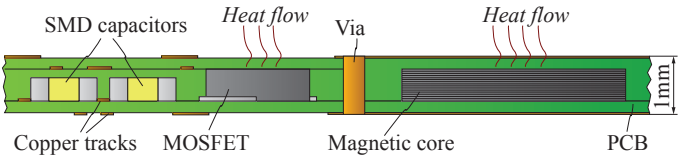


Fig. 2.1: Cross-section of a PCB with integrated components; the transformer core, SMD capacitors, and power MOSFETs, e.g. ThinPAK package [56], are embedded in the PCB which allows for ultra-flat systems.

Several publications report the optimized design of DC-DC converters, single-phase AC-DC rectifiers, and three-phase AC-DC rectifiers with regard to one or several of the aforementioned objectives [20, 22, 63, 64]; in each publication it is stated that a proper thermal management, low switching losses, and low EMI noise are crucial in order to achieve an optimized design and to fulfill the specified requirements.

The design of ultra-flat converters also aims for the listed objectives and due to stringent height limitation particular care must be taken on the thermal management, the switching losses, and the EMI noise; these issues are highlighted in this section.

2.1.1 Cooling capabilities of ultra-flat systems

In order to obtain a 1 mm thin power converter system, all components have to be integrated into the PCB. This, however, implies that the losses of the components must be transferred through the PCB to the ambient as shown in **Fig. 2.1**.

Considering that the volume of a power converter is defined as a cuboid-shaped boundary box around the outlines of the system, the heat removal capability of a converter increases with the surface area of the boundary box [65] and thus, an ultra-flat converter has excellent thermal preconditions, cf. **Fig. 1.2**.

In order to facilitate the good heat removal capability of an ultra-flat system, the components should be arranged such that the generated losses are evenly spread over the surface area. A topology consisting of several subsystems and/or cells divides the transferred energy to each subsystem. If the subsystems are evenly distributed over the surface

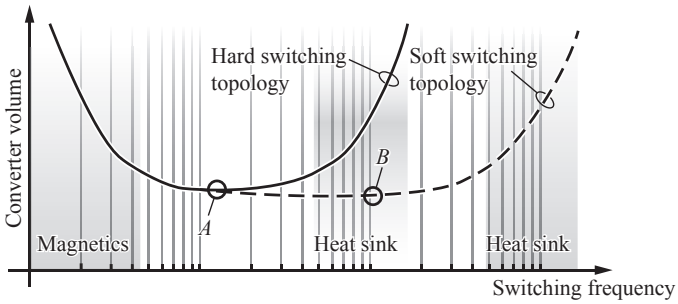


Fig. 2.2: Converter volume as a function of the switching frequency. Point A refers to the minimal converter volume for hard switching topologies whereas point B indicates the minimal converter volume for soft switching topologies [20].

area the losses are also well balanced over the entire surface contrary to topologies consisting of only one conversion cell [66]. Accordingly, a multi-cell topology approach should be employed for an ultra-flat converter system.

2.1.2 Soft switching

An important parameter of a power electronic system is the switching frequency as it has major impact on the trade-off between power density and efficiency of the converter. With increased switching frequency the switching losses will increase, however, the sizes of energy storage elements, such as capacitors and inductors, will decrease [20, 22].

According to **Fig. 2.2** the converter volume is mainly determined by the volume of magnetic components at low switching frequencies [22]. Point A indicates the lowest volume for hard switching topologies. At high switching frequencies the converter volume increases again as a larger heat sink is required to remove the heat generated by switching losses.

In order to reduce the detrimental switching losses, a soft switching topology can be applied. This allows to operate at higher switching frequencies. With the use of soft-switching techniques the increase of volume due to the increasing heat sink size is shifted towards higher frequencies and the lowest converter volume results at a higher frequency, cf. B in **Fig. 2.2**. Still, switching losses and other frequency dependent

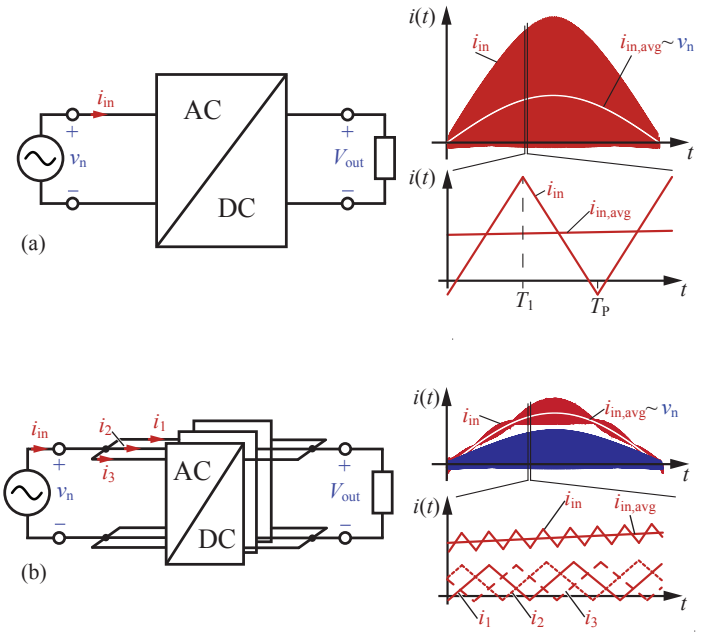


Fig. 2.3: Interleaving of several converter cell reduces the input current ripple. The waveforms are shown for a boost-type PFC rectifier [67]; however, the basic principle is valid also for other PFC topologies. (a) Single cell operation with a high input current ripple. (b) Interleaved multi-cell operation where the input current ripple is reduced for the same average input current $\bar{i}_{in}$.

loss components remain increasing with increasing frequency; as a consequence, there is an upper limit of the switching frequency also for soft switching topologies.

Since a soft-switching topology allows for a more compact system it is applied for the *Power Sheet*.

2.1.3 EMI filter

As specified in Section 1.2, the PFC rectifier must comply with the CISPR 11 standard which requires for an EMI filter. Since the EMI filter of conventional power converters allocates up to one-third of the

overal converter volume, cf. [22], measures to reduce the EMI noise are important in order to obtain a small EMI filter size.

A reduction of the differential mode (DM) EMI filter size can be achieved if the input current ripple of the converter is reduced. An interleaving of n switching cells results in a smoothed input current and the cancelation of the first n harmonics. If the switching frequency is higher than 150 kHz, which is the lower limit of the frequency band specified by CISPR 11, the DM filter size can be reduced ([68], depending on the number of parallel connected converter cells).

Fig. 2.3 (a) shows the input current of a boost-type PFC rectifier operating in boundary conduction mode (BCM) [67]. There, the input current ripple is very large in order to obtain a desired local average input current $\bar{i}_{\mathrm{in}}$. The ripple content of the input current i_{in} can be reduced if an interleaving of several converter cells is applied as depicted in **Fig. 2.3** (b). This reduces the DM noise and further, if $f_{\mathrm{S}} > 150\,\mathrm{kHz}$, the DM EMI filter size. As a consequence, the selected topology should enable the interleaving of several converter cells. So the multi-cell configuration is not only beneficial to distribute the losses but might also yield a reduction of the DM EMI filter size.

2.2 Conventional PFC rectifier systems

Passive single-phase AC-DC rectifiers employing a diode full bridge in the input, cf. **Fig. 2.4**, draw a nonsinusoidal current and/or low frequency harmonics from the mains [69]. Accordingly, the reactive (distortion) power consumption is increased which entails a higher volt-ampere rating. In addition, the harmonic current components cause a voltage drop over the grid impedance which results in a distortion of the input voltage for other electronic systems connected in parallel.

In order to avoid these unwanted effects, a power factor correction (PFC) has to be implemented which has to comply with the IEC 61000-3-2 regulations [70] which are listed in **Tab. 2.1**; the equipment is classified into four categories:

- Class B: Portable equipment.
- Class C: Lighting equipment.
- Class D: Monitors, screens, TV, and computers.

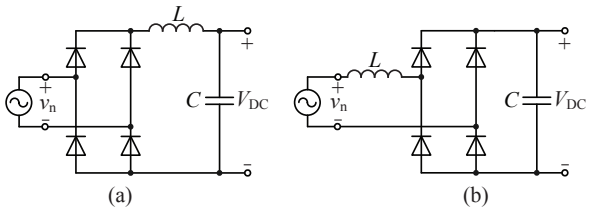


Fig. 2.4: Passive AC-DC rectifier realizations where in (a) the smoothing inductor is placed on the DC side and in (b) on the AC side of the diode bridge.

Tab. 2.1: IEC 61000-3-2 limitations for input current harmonics [70].

Odd harm. n	Class A (A)	Class B (A)	Class C I_n/I_1 (%)	Class D (mA/W)
3	2.3	3.45	30	3.4
5	1.14	1.71	10	1.9
7	0.77	1.16	7	1
9	0.4	0.6	5	0.5
11	0.33	0.5	3	0.35
13	0.21	0.32	3	0.3
15 – 39	$0.15 \cdot 15/n$	$0.225 \cdot 15/n$	3	$3.85/n$
Even harm.				
2	1.08	1.62	2	–
4	0.43	0.65	–	–
6	0.3	0.45	–	–
8 – 40	$0.23 \cdot 8/n$	$0.35 \cdot 8/n$	–	–

- Class A: Equipment which is not covered by one of the other classes.

Each category has limits from the 2^{nd} to the 39^{th} harmonic component. In Class A and B the limits are specified as absolute values whereas in Class C and Class D the limits are defined relative to the fundamental current component or the output power, respectively.

2.2.1 Passive single-phase rectifiers

Single-phase AC-DC rectifiers designed to comply with IEC 61000-3-2 can be divided into three groups of architectures [71]. The simplest architecture is a line commutated diode rectifier which consists of a diode rectifier, a DC-link capacitor, and an inductor either on the DC side, cf. **Fig. 2.4** (a), or on the AC side, cf. **Fig. 2.4** (b). The advantage of having only a few components (basically an inductor, a capacitor, and four diodes) and no control effort is opposed by the rather poor power factor and the low efficiency and/or low power density obtained at high power levels. Therefore, passive AC-DC rectifiers are typically only applied for low power levels and for Class A which is less stringent than the other classes [71].

The alternative PFC architectures are single-stage and two-stage PFC rectifier systems, which are presented in the following.

2.2.2 Two-stage converter systems

A two-stage converter systems, consisting of a boost-type PFC rectifier and a series-connected DC-DC converter, is the most common architecture for off-line power supplies employed for computers and telecom applications [72]. The PFC rectifier is applied to reduce the line-current harmonics in order to meet the worldwide standards, cf. [70] and **Tab. 2.1**, and the DC-DC converter provides galvanic isolation as well as a precise and dynamic output voltage regulation. **Fig. 2.5** (a) presents a block diagram of a two-stage converter; voltage levels according to the specifications given in Section 1.2 are indicated.

The realization of an ultra-flat PFC rectifier would benefit from a topology which features the characteristics discussed in Section 2.1. Therefore, Chapter 3 presents a totem-pole-based boost-type PFC rectifier with a new modulation scheme which combines several advantages that are important for the realization of an ultra-flat power supply, i.e. a multi-cell topology and ZVS.

The DC link voltage of a boost-type PFC rectifier employed in the European grid is typically $380 \ldots 450\,\mathrm{V}$. The DC link capacitor C_{DC}, cf. **Fig. 2.5** (a), has to smooth the inherent power variation of single-phase AC-DC converters which leads to considerable capacitance values, e.g. $C_{\mathrm{DC}} = 40\,\mu\mathrm{F}$ for $V_{\mathrm{out}} = 400\,\mathrm{V}$, and $P_{\mathrm{out}} = 200\,\mathrm{W}$, for a maximum output voltage ripple of $20\,\mathrm{V}$ [67]. The hardware realization of ultra-thin 400 V-capacitors, however, poses a challenge to the converter design

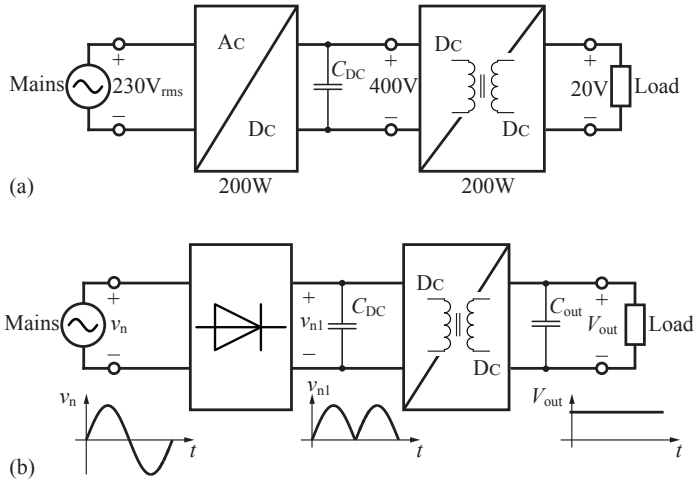


Fig. 2.5: (a) Block diagram of a two-stage realization of the *Power Sheet*. (b) Structure of a single-stage topology employing a diode rectifier bridge at the input.

because they are only available with small capacitance values (several ten nF) and, hence, require a considerable footprint size, i.e. $A = 100\,\mathrm{cm}^2$ for the aforementioned DC link capacitor.
Moreover, the PFC rectifier requires a separate DC-DC converter stage connected in series to generate the specified isolated output voltage of 20 V. This implies that, besides the boost inductor, another magnetic component, i.e. the HF transformer of the DC-DC stage is required. In terms of reducing the required area of the converter, a single-stage system would be beneficial where one magnetic component enables the PFC functionality and the galvanic isolation.

2.2.3 Single-stage converter systems

A single-stage converter topology only employs a single magnetic component at the expense of an increased filtering effort on the low voltage side (compared to two-stage topologies with a high voltage DC link capacitance and voltage controlled DC-DC converter) for the same output voltage ripple and a more complex control structure [73]. The architecture of a single-stage converter is illustrated in **Fig. 2.5** (b).

Chapter 4 presents two single-stage power converter topologies: a flyback converter and a Dual Active Bridge (DAB) converter which combine the PFC functionality and the DC-DC conversion and directly convert the mains' AC voltage into a DC voltage of $V_{\mathrm{out}} = 20\,\mathrm{V}$. The DC link voltage, v_{n1}, of the proposed converter circuits varies according to the absolute value of the mains voltage v_{n}, cf. **Fig. 2.5** (b),

$$v_{\mathrm{n1}} \approx |v_{\mathrm{n}}|, \tag{2.1}$$

and only a small capacitance C_{DC} is allowed in order to not impair the sinusoidal input current shaping by the converter stage. The capacitor C_{out}, used to buffer the output voltage V_{out}, has to show a large capacitance in order to provide filtering of the converter power flow pulsation with twice the mains frequency.

However, it is considerably more difficult to realize the high voltage DC link capacitor C_{DC} under the extreme converter height limitation, needed for the two-stage system, than the low voltage capacitor C_{out} because low voltage chips with a very small package are available featuring a capacitance of several µF, e.g. $C = 10\,\mu\mathrm{F}$, Package: 0805, $h < 1\,\mathrm{mm}$ [41].

3

Triangular Current Mode PFC Rectifier

The front-end converter of the two-stage architecture, cf. Section 2.2.2, is typically a PFC rectifier. As mentioned there, the implementation of the converter system tends to require a larger footprint area compared to single-stage systems due to a high voltage DC link capacitor and because a series-connected galvanically isolated DC-DC converter needs an additional magnetic device.

Nonetheless, two-stage topologies offer benefits as the PFC stage and the DC-DC stage are decoupled via the DC link and so both systems can be optimized with narrow specifications which results in a higher efficiency compared to single-stage systems [71]. Besides, a two-stage system allows for a dynamic and tight output voltage control without having direct impact on the input current quality.

This chapter presents the evaluation of a new TCM PFC rectifier topology which is suitable for the realization of an ultra-flat converter system. Based on state-of-the-art boost-type PFC rectifier systems, the topology and particularly its modulation are adapted in a way that fulfills each of the requirements postulated in Section 2.1, i.e. soft switching and a multi-cell configuration. Section 3.1 briefly discusses the derivation of the proposed TCM topology from a conventional brigdeless PFC rectifier.

The operation of the converter is detailed in Section 3.2 and it is shown that the modulation requires accurately estimated timing values in order to obtain a sinusoidal input current. For it, the nonlinear capacitances of the switches have to be included in the analysis and since the imposed nonlinearity does not allow for a closed-form solution of the

currents and the timing values, a new capacitance model is proposed in Section 3.3 with which all converter currents and the respective timings can be calculated in an analytical way.
Based on the capacitance model, the design and the optimization of the converter with respect to the power density and/or the efficiency is detailed in Section 3.4. It is shown that the boost inductors have major impact on the overall system performance. Section 3.5 discusses the control of the converter which includes the interleaving control of several boost cells. The theoretical analysis is validated using measurements on a prototype. The constructed 200 W PFC rectifier prototype presented in Section 3.6 features a thickness of 5 mm since the inductors are not yet integrated into the PCB. Nevertheless, the topology proofs to be an appropriate choice for an ultra-flat system.

3.1 Introduction

A comparison of several PFC rectifier topologies presented in [74] renders the bridgeless PFC rectifier, cf. **Fig. 3.1** (a), to be a promising candidate regarding high efficiency and high power density, as the number of semiconductors in the conduction path is reduced compared to conventional boost-type rectifiers which employ a diode bridge at the input [75, 76]. The bridgeless topology, however, suffers from considerable common-mode (CM) noise as the output rails are floating during the negative mains half-wave. As a consequence, arrangements with either capacitors or diodes as CM return path have to be employed which cause additional losses and increase the circuit complexity [22, 76–78].

A modification of the bridgeless PFC rectifier is the totem-pole bridgeless PFC rectifier depicted in **Fig. 3.1** (b) and presented in [76]. Compared to the basic bridgeless topology, a diode and a switch are interchanged which allows the output-rails to be connected to the mains for the complete mains period through one of the diodes. Thus, the CM noise is considerably reduced. In continuous conduction mode (CCM) of operation, however, the bridge-leg that is composed of the switches suffers from significant reverse recovery losses. Low switching losses can only be achieved for operation in boundary conduction mode (BCM) or in discontinuous conduction mode (DCM) which allow for reduced switching losses.

With the BCM modulation technique proposed in [79] the operating range for soft switching, i.e. zero voltage switching (ZVS), is

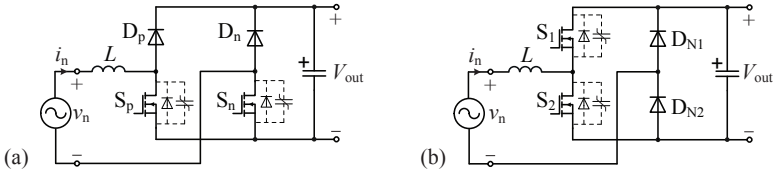


Fig. 3.1: (a) Bridgeless PFC rectifier with parasitic output capacitances of the MOSFETs. D_p and S_p shape i_n for $v_n > 0$ whereas D_n and S_n shape i_n for $v_n < 0$ [76]. (b) Totem-pole bridgeless PFC boost rectifier [76].

limited to $|v_n| \leq V_{out}/2$; for larger input voltages valley switching has to be employed to reduce the switching losses. Full range ZVS over the entire mains period can be achieved with an advanced modulation technique [67, 80], entitled *Triangular Current Mode* (TCM) due to the triangular-shaped inductor currents, which require numerical calculations [67] or measurement results [80] to determine the timing parameters needed to operate the converter. For the TCM operation the diodes D_{N1} and D_{N2} must be replaced by actively switched semiconductors such as MOSFETs what also reduces the conduction losses. The resulting circuit, depicted in **Fig. 3.2** (a), even enables bidirectional power flow.

A drawback of the TCM PFC rectifier is the large input current ripple which makes a large differential-mode (DM) EMI filter necessary. Since the proposed converter is operated with a switching frequency higher than 150 kHz, an interleaved arrangement of n converter cells facilitates a reduced filter size, e.g. the setup with three interleaved converter cells depicted in **Fig. 3.2** (b) cancels the first and the second harmonic component of the inductor current i_{L1} in the input current i_n. A two-cell configuration of this converter is discussed in [81], however, the interleaving control is not detailed and the applied modulation does not allow for ZVS within the whole mains period. Thus, a detailed analysis of the interleaving of three cells, cf. **Fig. 3.2** (b), is described in this chapter.

The interleaved 3-cell TCM PFC rectifier depicted in **Fig. 3.2** (b) is considered to be the most appropriate topology regarding the ultra-flat converter system as it features:

- low conduction losses due to synchronous rectification,

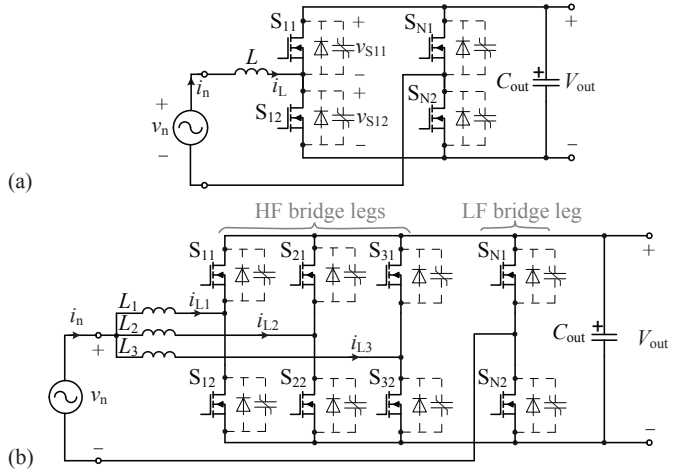


Fig. 3.2: (a) Single-cell and (b) 3-cell configuration of a TCM PFC rectifier system facilitating ZVS over the entire mains period.

- ZVS over the entire mains period,
- a reduced DM EMI filter effort due to interleaved inductor currents,
- low common-mode noise, and
- bidirectional operation.

3.2 Basic operation

This section presents the basic principle of the operation of a TCM PFC rectifier and points out the difference between valley switching and the proposed triangular mode modulation technique which allows for ZVS during the entire mains period.

For positive input voltages v_n, S_{N2} is turned ON and S_{N1} is turned OFF, cf. **Fig. 3.2** (a). The resulting simplified circuit is given in **Fig. 3.3** (a) and the converter operation is explained based on this circuit. The explanation, however, is similar for negative input voltages.

There, only the roles of the upper switch S_{11} and the lower switch S_{12} are interchanged.

The typical waveform for boundary conduction mode and the specifications of the variables are depicted in **Fig. 3.3** (b) [79]. The switching period is split into two main intervals and two short resonant transitions. The initial conditions are

$$i_L(t_0) = 0, \qquad v_{S12}(t_0) = 0. \tag{3.1}$$

Interval 1 $[t_0 \dots t_1]$

During *Interval 1* the switch S_{12} is turned ON, v_n is applied to the inductor L, and the inductor current i_L increases linearly. As soon as the current $\hat{I}_S$ is reached or the ON-time of S_{12}, T_{on}, defined by the controller, cf. Section 3.5, has passed, S_{12} is turned OFF. The final values of the inductor current and voltage across the MOSFET are

$$T_{on} = t_1 - t_0, \qquad i_L(t_1) = \hat{I}_S, \qquad v_{S12}(t_1) = 0. \tag{3.2}$$

Interval 2 $[t_1 \dots t_2]$

During this interval, a switching transition takes place in which the nonlinear MOSFET output capacitance C_{oss2} is charged and C_{oss1} is discharged. The voltage transitions across the switches, v_{S11} and v_{S12}, are determined by the nonlinear capacitances. The switch voltages and currents during this interval can only be evaluated using numerical and iterative methods. Since the inductor current i_L is large, however, the switching transition is very fast and *Interval 2* can usually be neglected;

$$T_{s1} = t_2 - t_1, \qquad i_L(t_2) = \hat{I}_{SS} \approx \hat{I}_S, \qquad v_{S12}(t_2) = V_{out}. \tag{3.3}$$

Interval 3 $[t_2 \dots t_3]$

When C_{oss2} is fully charged the body diode of S_{11} starts to conduct the inductor current i_L and *Interval 3* starts. After an interlocking delay time, cf. Section 3.5, S_{11} is turned-ON at zero voltage. During *Interval 3* the voltage applied to the inductor is negative and i_L decreases,

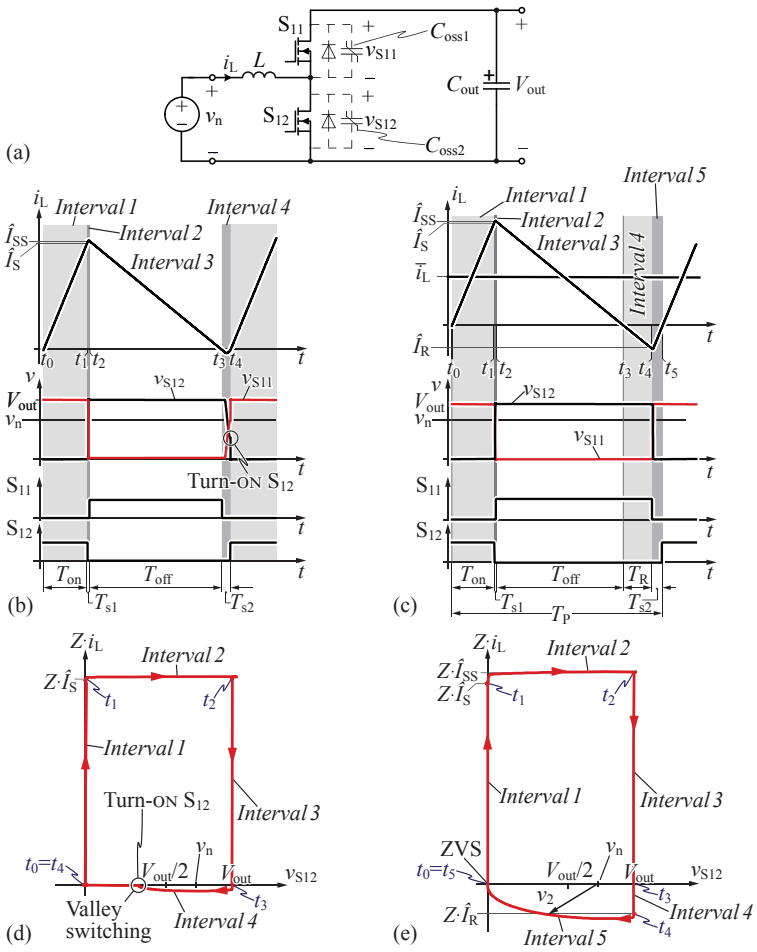


Fig. 3.3: (a) Single-cell configuration for positive mains voltage. (b) Current and voltage waveforms for valley switching. (c) Current and voltage waveforms for the proposed ZVS strategy, i.e. TCM operation. A detailed view of the switching transitions in *Intervals 4* and *5* is given in **Fig. 3.6**. (d) *V-Zi* plot for valley switching. (e) *V-Zi* plot for ZVS.

$$T_{\text{off}} = t_3 - t_2, \qquad i_{\text{L}}(t_3) = 0, \qquad v_{\text{S12}}(t_3) = V_{\text{out}}. \tag{3.4}$$

Interval 4 $[t_3 \dots t_4]$

Once i_L reaches zero, S_{11} is turned OFF and *Interval 4* begins. L, C_{oss1}, and C_{oss2} form a resonant circuit which starts to oscillate. The behavior of the oscillation depends on the input to output voltage ratio $v_\mathrm{n}/V_\mathrm{out}$. For $v_\mathrm{n}/V_\mathrm{out} < 1/2$, v_{S11} rises to V_out and v_{S12} declines to zero and ZVS is achieved [79].

If $v_\mathrm{n}/V_\mathrm{out}$ exceeds $1/2$, the instantaneous switch voltage $v_{\mathrm{S12}}(t)$ does not reach 0 and ZVS cannot be achieved. Instead, the turn-ON instant has to coincide with the instant when v_{S12} is minimal in order to minimize the switching losses; this switching scheme is denominated as valley switching (cf. **Fig. 3.3** (b) and **Fig. 3.4** (a)). This is pointed out in the *V-Zi* plot in **Fig. 3.3** (d). The *V-Zi* plot shows a state graph of v_{S12} and i_L which are the state variables of the system. If the system trajectory reaches the ordinate after a switching cycle, ZVS can be achieved. Thus, the *V-Zi* plot clearly shows whether or not ZVS can be achieved,

$$i_\mathrm{L}(t_4) = 0, \tag{3.5}$$

$$v_{\mathrm{S12}}(t_4) = \begin{cases} 0 & \text{for } v_\mathrm{n}/V_\mathrm{out} < 1/2, \\ 2\,v_\mathrm{n} - V_\mathrm{out} & \text{for } v_\mathrm{n}/V_\mathrm{out} \geq 1/2.^{1} \end{cases} \tag{3.6}$$

To overcome the drawback of losing ZVS during the mains period a modified modulation technique can be applied. During *Intervals 1 - 3*, the current waveforms shown in **Fig. 3.3** (c) are similar to the waveforms depicted in **Fig. 3.3** (b). However, S_{11} remains in the ON state after the zero crossing of i_L and the current keeps decreasing linearly, cf. *Interval 4* in **Fig. 3.3** (c),

$$T_\mathrm{R} = t_4 - t_3, \qquad i_\mathrm{L}(t_4) = \hat{I}_\mathrm{R}, \qquad v_{\mathrm{S12}}(t_4) = V_\mathrm{out}. \tag{3.7}$$

Interval 5 $[t_4 \dots t_5]$

As soon as a defined current $\hat{I}_\mathrm{R}$ is reached or a given reverse conduction time T_R has passed, cf. Section 3.5, S_{11} is turned OFF and an oscillation starts (*Interval 5*). Contrary to the previous situation shown in

[1] Eq. (3.6) assumes that the output capacitance is linear. An analytical expression which includes the nonlinearity of the capacitance is not feasible.

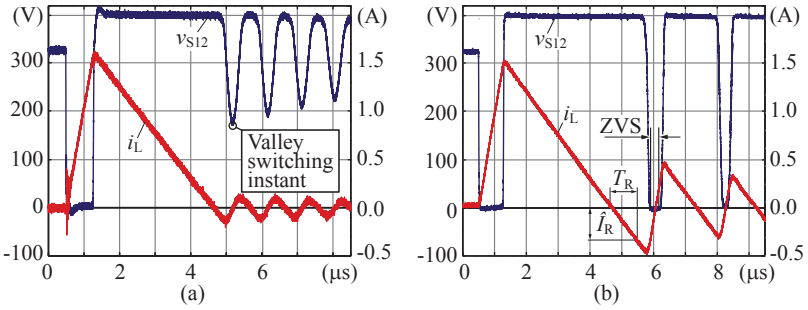


Fig. 3.4: Measurement results of a boost cell (a) without and (b) with an extended reverse conduction time T_R, cf. **Fig. 3.3** (b) and (c). In order to minimize the switching losses, valley switching can be applied, cf. (a), whereas the extension of T_R allows for ZVS over the whole mains period, cf. (b). (Parameters: $v_n = 328\,V$, $V_{out} = 400\,V$, $T_{on} = 750\,ns$)

Fig. 3.3 (b) the energy stored in the inductor now is large enough to completely charge C_{oss1} and discharge C_{oss2}. Thus, v_{S12} reaches 0 during *Interval 5*. The negative current $\hat{I}_R$ enlarges the elliptic oscillation trajectory, cf. v_2 in the *V-Zi* diagram of **Fig. 3.3** (e), and v_{S12} decreases to 0. Consequently, ZVS can be achieved over the complete mains period by controlling the ON-time of S_{11} and thus controlling the reverse current $\hat{I}_R$ in the inductor L. At $t = t_5$, S_{12} can be turned ON with ZVS and a new switching cycle starts;

$$T_{s2} = t_5 - t_4, \qquad i_L(t_5) = \hat{I}_{Rv}, \qquad v_{S12}(t_5) = 0. \tag{3.8}$$

Fig. 3.4 presents measurement results which illustrate the difference between valley switching and the proposed TCM concept. Obviously, applying an additional reverse current $\hat{I}_R$ allows for ZVS which is particularly important at high switching frequencies.

Average input current

A PFC rectifier shapes the input current $i_n(t)$ to be proportional to the input voltage $v_n(t)$. The local average current through an inductor, $\bar{i}_L(t)$, cf. **Fig. 3.3** (c), has thus to be controlled by adjusting the ON-time T_{on} and the reverse conduction time T_R for each switching cycle.

With known T_{on} and T_{R} the switching frequency, the duty cycle, all converter currents, and the losses of the converter can be determined.

From **Fig. 3.3** (c) it can be concluded that there is an infinite set of combinations $\{T_{\mathrm{on}}, T_{\mathrm{R}}\}$ which lead to a required average current $\bar{i}_{\mathrm{L}}$ since an increase of T_{on} can be compensated by a respective increase of T_{R} so that the average value of the input current $\bar{i}_{\mathrm{L}}$ is constant over the switching period. The infinite set of applicable parameters $\{T_{\mathrm{on}}, T_{\mathrm{R}}\}$ can also be used to adjust the switching period, T_{P}. This can be beneficially employed to control the phase shift of several interleaved boost cells because the switching cycle of a cell can be prolonged with respect to another cell, cf. Section 3.5. However, large values of $\hat{I}_{\mathrm{S}}$ and $\hat{I}_{\mathrm{R}}$ result in an increased RMS values of i_{L} and in a higher flux density swing in the boost inductor which increases copper and core losses. As a consequence, it is beneficial to keep $\hat{I}_{\mathrm{S}}$ and $|\hat{I}_{\mathrm{R}}|$ as small as possible.

The average current $\bar{i}_{\mathrm{L}}(t)$ can be calculated numerically by integrating the inductor current, cf. **Fig. 3.3** (c), over a switching period,

$$\bar{i}_{\mathrm{L}} = \frac{1}{T_{\mathrm{P}}} \sum_{j=1}^{5} \int_{t_{j-1}}^{t_j} i_{\mathrm{L}}(t)\,\mathrm{d}t. \tag{3.9}$$

Due to the nonlinearity of the MOSFETs' output capacitances *Interval 2* and *Interval 5* can only be described by solving a nonlinear differential equation of the charge $q(t)$ in the capacitances,

$$L \cdot \frac{\mathrm{d}^2 q(t)}{\mathrm{d}t^2} + v_{\mathrm{C}}(q(t)) = v_{\mathrm{n}}, \tag{3.10}$$

where $v_{\mathrm{C}}(q(t))$ represents the voltage applied to the parallel connection of the output capacitances C_{oss1} and C_{oss2}. This results in a considerable calculation effort as (3.10) can only be solved iteratively [67]. To simplify the calculation, an adequate model of the capacitance during the switching transition is detailed in the next section.

3.3 Closed-form analytical converter model

This section presents a simple and accurate model that allows for closed-form solutions of the inductor current and the durations of the different time intervals within a switching period of a TCM PFC rectifier. The closed-form expressions enable the calculation of the timing parameters

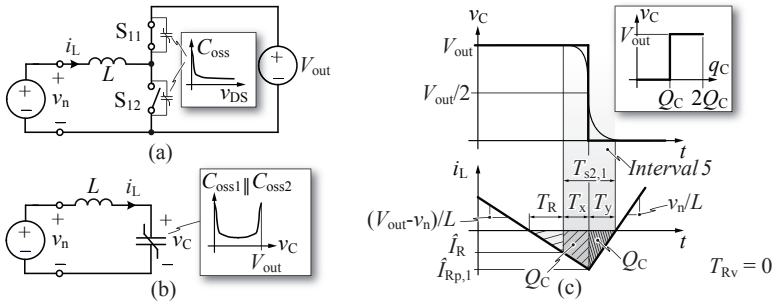


Fig. 3.5: (a) Bridge-leg for positive input voltage during *Interval 4*, cf. **Fig. 3.3** (c). (b) During the switching transition (*Interval 5* in **Fig. 3.3** (c)) both capacitors are connected in parallel. (c) Proposed model of the parallel connected nonlinear output capacitances of the switches for $v_\mathrm{n} \geq V_\mathrm{out}/2$. The peak current $\hat{I}_\mathrm{Rp}$ is assumed to occur when the voltage v_C is decreased to half of the initial value.

needed for the control and the converter design which are further used for the loss evaluation of each component. The section is subdivided into two cases. The first case consideres $v_\mathrm{n} > V_\mathrm{out}/2$ where an additional time T_R is required to achieve ZVS. In the second case, $v_\mathrm{n} \leq V_\mathrm{out}/2$, T_R is not required to achieve ZVS but the oszillation needs to be modelled accurately in order to determine the timing values needed for the design and the control.

Case I: $v_\mathrm{n} > V_\mathrm{out}/2$

Considering a positive input voltage $v_\mathrm{n} \geq V_\mathrm{out}/2$ and starting at *Interval 4* in **Fig. 3.3** (c), the equivalent circuit shown in **Fig. 3.5** (a) is obtained. There, the inductor current i_L is decreasing, C_oss1 is discharged, and C_oss2 is charged.

As soon as S_{11} is turned OFF, C_oss1 and C_oss2 are connected in parallel and the equivalent circuit illustrated in **Fig. 3.5** (b) is obtained. In order to discharge C_oss2 the charge Q_C,

$$Q_\mathrm{C} = \int_0^{V_\mathrm{out}} C_\mathrm{oss2}(v_\mathrm{C})\,\mathrm{d}v_\mathrm{C} \tag{3.11}$$

has to be removed and, assuming identical switches, the same charge Q_C is needed to charge C_oss1 to V_out. Consequently, as soon as the time

integral of the current i_L during *Interval 5* exceeds $2\,Q_\mathrm{C}$, ZVS can be achieved as v_C declines to zero.

The most simple capacitance model reduces the expression for the voltage across the parallel connected capacitances $C_\mathrm{oss1}||C_\mathrm{oss2}$ to

$$v_\mathrm{C}(q_\mathrm{C}) = \begin{cases} V_\mathrm{out} & \text{for } q_\mathrm{C} > Q_\mathrm{C}, \\ 0 & \text{for } q_\mathrm{C} \leq Q_\mathrm{C}, \end{cases} \tag{3.12}$$

whereas q_C is the charge stored in the capacitance $C_\mathrm{oss1}||C_\mathrm{oss2}$. **Fig. 3.5** (c) illustrates the waveforms obtained with the proposed model. It can be seen that a triangular-shaped current i_L results and the derivation of an analytical expression becomes feasible. The proposed model (3.12) is based on the condition that

$$\int_{t_4}^{t_5} |i_\mathrm{L}(t)|\,\mathrm{d}t \geq 2 \cdot Q_\mathrm{C}, \tag{3.13}$$

which can be assured by controlling the reverse current $\hat{I}_\mathrm{R}$.

A simulation is used to validate the model and to compare it to other conventionally used models for nonlinear output capacitances, i.e. the (linear) energy-equivalent capacitance C_ee and the (linear) charge-equivalent capacitance C_qe [82],

$$C_\mathrm{ee}(V_\mathrm{out}) = \frac{2}{V_\mathrm{out}^2} \int_0^{V_\mathrm{out}} C_\mathrm{oss}(v_\mathrm{DS})\, v_\mathrm{DS}\,\mathrm{d}v_\mathrm{DS}, \tag{3.14}$$

$$C_\mathrm{qe}(V_\mathrm{out}) = \frac{1}{V_\mathrm{out}} \int_0^{V_\mathrm{out}} C_\mathrm{oss}(v_\mathrm{DS})\,\mathrm{d}v_\mathrm{DS}. \tag{3.15}$$

Fig. 3.6 presents the simulation results. For each model the required negative current $\hat{I}_\mathrm{R}$ is calculated in order to achieve ZVS and compared to the nonlinear capacitance model specified in the datasheet of the applied MOSFET. **Fig. 3.6** (a) shows that the energy-equivalent model yields a poor approximation of the inductor current, the model even fails to predict whether ZVS can be achieved. The charge-equivalent model achieves a better approximation, cf. **Fig. 3.6** (b), however, resonant states need to be considered during *Intervals 2* and *5*. The proposed model achieves a very good approximation of the inductor current

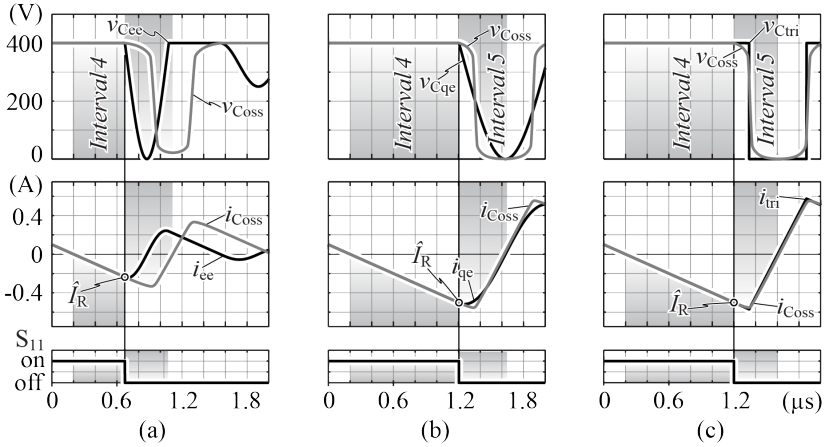


Fig. 3.6: Comparison between different capacitor models. In simulations, each model is compared to the nonlinear capacitance given in the datasheet of the switch. (a) Energy equivalent linear capacitance, (b) charge equivalent linear capacitance, and (c) proposed charge model (3.12) of the capacitance.

without the need for resonant states, cf. **Fig. 3.6** (c), which renders this model most suitable with respect to an analytical investigation of the TCM PFC rectifier.

The required negative current $\hat{I}_\mathrm{R}$ is independent of the output power but depends on V_out, v_n, and the selected switch which defines Q_C, cf. (3.11). Considering **Fig. 3.5** (c), $\hat{I}_\mathrm{Rp}$ can be calculated with

$$Q_\mathrm{C} = \frac{-\hat{I}_\mathrm{Rp,1}\, T_\mathrm{y}}{2} \quad \Rightarrow \quad \hat{I}_\mathrm{Rp,1} = -\sqrt{\frac{2\,Q_\mathrm{C}}{L}\, v_\mathrm{n}}, \tag{3.16}$$

whereas $L\,\mathrm{d}i/\mathrm{d}t = L\,(-\hat{I}_\mathrm{Rp,1})/T_\mathrm{y} = v_\mathrm{n}$ has been substituted. With (3.16), $\hat{I}_\mathrm{R}$ can be calculated with the same approach which yields

$$\hat{I}_\mathrm{R} = -\sqrt{\frac{2\,Q_\mathrm{C}}{L}\,(2\,v_\mathrm{n} - V_\mathrm{out})}. \tag{3.17}$$

Applying the presented model of the nonlinear capacitances to *Interval 5* allows for an analytical description of the entire switching cycle and a closed-form converter model is obtained. As already mentioned,

Interval 2 is also determined by a switching transition including nonlinear MOSFET capacitances but due to the large inductor current i_L the switching transition is very fast and *Interval 2* can be neglected.

Considering **Fig. 3.8** (a), the average current in the inductor over a switching period is

$$\bar{i}_\mathrm{L} = \frac{1}{T_{\mathrm{P},1}} \left(\frac{\hat{I}_\mathrm{S} \cdot T_\mathrm{on}}{2} + \frac{\hat{I}_\mathrm{S} \cdot T_\mathrm{off}}{2} + \frac{\hat{I}_\mathrm{R} \cdot T_\mathrm{R}}{2} - 2 \cdot Q_\mathrm{C} \right). \tag{3.18}$$

The relation between inductor current and inductor voltage applied to each interval results in

$$\hat{I}_\mathrm{S} = \frac{v_\mathrm{n}}{L} \cdot T_{\mathrm{on},1}, \quad T_\mathrm{off} = \frac{L \cdot \hat{I}_\mathrm{S}}{V_\mathrm{out} - v_\mathrm{n}}, \quad T_\mathrm{R} = \frac{L \cdot (-\hat{I}_\mathrm{R})}{V_\mathrm{out} - v_\mathrm{n}}. \tag{3.19}$$

The switching period is defined by

$$T_{\mathrm{P},1} = T_{\mathrm{on},1} + T_\mathrm{off} + T_\mathrm{R} + T_{\mathrm{s2},1}, \tag{3.20}$$

with

$$T_{\mathrm{s2},1} = L \cdot \frac{-(\hat{I}_{\mathrm{Rp},1} - \hat{I}_\mathrm{R})}{V_\mathrm{out} - v_\mathrm{n}} + L \cdot \frac{-\hat{I}_{\mathrm{Rp},1}}{v_\mathrm{n}}. \tag{3.21}$$

Substitution of (3.19) - (3.21) into (3.18) yields the ON-time $T_{\mathrm{on},1}$ for a desired average current $\bar{i}_\mathrm{L}$, cf. (3.22), and consequently all timing and current values for $v_\mathrm{n} > V_\mathrm{out}/2$,

$$T_{\mathrm{on},1} = \frac{L \cdot \bar{i}_\mathrm{L}}{v_\mathrm{n}} + \sqrt{\frac{L}{v_\mathrm{n}^2} \cdot \left(L\,\bar{i}_\mathrm{L}^2 + 2\,Q_\mathrm{C}\,v_\mathrm{n} + 2\,\bar{i}_\mathrm{L} \cdot \sqrt{2\,Q_\mathrm{C}\,L\,v_\mathrm{n}} \right)}. \tag{3.22}$$

Case II: $v_\mathrm{n} \leq V_\mathrm{out}/2$

The same considerations discussed for $v_\mathrm{n} > V_\mathrm{out}/2$ can be done for low input voltages. In this case, ZVS is achieved without any additional time T_R. Nevertheless, the timing of the switching transition needs to be quantified in order to obtain the timing values required for the control and the current values for the design.

Since T_R is zero for $v_\mathrm{n} \leq V_\mathrm{out}/2$, *Interval 4* is skipped and immediately after the zero-crossing of the inductor current i_L *Interval 5* starts, cf. **Fig. 3.7**. It can be seen that (3.13) is inherently fulfilled which ensures ZVS. After $T_{\mathrm{s2},2}$ has passed, i_L is still negative and commutates

to the body diode of S_{12} and as soon as T_{Rv} has passed a new switching cycle begins.

All required currents can be calculated similarly to the previous paragraph. The results are:

$$\hat{I}_{Rp,2} = -\sqrt{\frac{2\,Q_C}{L} \cdot (V_{out} - v_n)}, \tag{3.23}$$

$$\hat{I}_{Rv} = -\sqrt{\frac{2\,Q_C}{L} \cdot (V_{out} - 2\,v_n)}, \tag{3.24}$$

$$T_{Rv} = L\,\frac{\hat{I}_{Rv}}{v_n}, \tag{3.25}$$

$$T_{s2,2} = L\,\frac{-(\hat{I}_{Rp} - \hat{I}_{Rv})}{v_n} + L\,\frac{-\hat{I}_{Rp}}{V_{out} - v_n}. \tag{3.26}$$

The switching period is defined by

$$T_{P,2} = T_{on,2} + T_{off} + T_{s2,2} + T_{Rv}, \tag{3.27}$$

The resulting ON-time for $v_n \le V_{out}/2$ is

$$T_{on,2} = \frac{L \cdot \bar{i}_L}{v_n} + \sqrt{\frac{L}{v_n^2} \cdot \left(L\,\bar{i}_L^2 + \right.} \tag{3.28}$$

$$+ \left. \overline{2\,Q_C\,(V_{out} - v_n) + 2\,\bar{i}_L \cdot \sqrt{2\,Q_C\,L\,(V_{out} - v_n)}}\right). \tag{3.29}$$

Overall solution

Combining the equations for the two cases enables the analytical description over the mains period. Thus, the respective timing values are

$$T_{on} = \begin{cases} T_{on,1} & \text{for } v_n > V_{out}/2, \\ T_{on,2} & \text{for } v_n \le V_{out}/2, \end{cases} \tag{3.30}$$

$$T_R = \begin{cases} \frac{L \cdot (-\hat{I}_R)}{V_{out} - v_n} & \text{for } v_n > V_{out}/2, \\ 0 & \text{for } v_n \le V_{out}/2, \end{cases} \tag{3.31}$$

$$T_{s2} = \begin{cases} T_{s2,1} & \text{for } v_n > V_{out}/2, \\ T_{s2,2} & \text{for } v_n \le V_{out}/2, \end{cases} \tag{3.32}$$

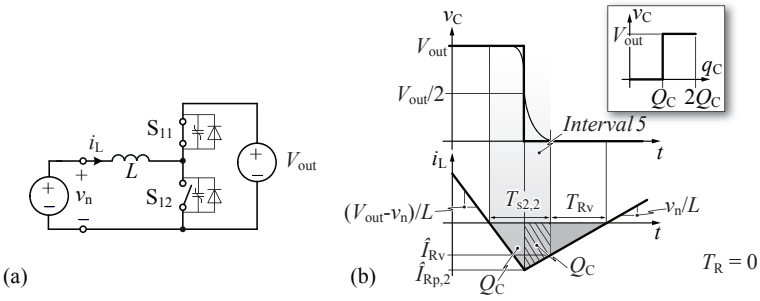


Fig. 3.7: (a) Equivalent circuit of a TCM boost cell for $v_\mathrm{n} > 0$. (b) Simplified capacitance model applied for $v_\mathrm{n} \leq V_\mathrm{out}/2$.

$$T_\mathrm{Rv} = \begin{cases} 0 & \text{for } v_\mathrm{n} > V_\mathrm{out}/2, \\ L\,\frac{\hat{I}_\mathrm{Rv}}{v_\mathrm{n}} & \text{for } v_\mathrm{n} \leq V_\mathrm{out}/2, \end{cases} \tag{3.33}$$

$$T_\mathrm{P} = \begin{cases} T_\mathrm{P,1} & \text{for } v_\mathrm{n} > V_\mathrm{out}/2, \\ T_\mathrm{P,2} & \text{for } v_\mathrm{n} \leq V_\mathrm{out}/2, \end{cases} \tag{3.34}$$

and the current values result to be

$$\hat{I}_\mathrm{S} = \frac{v_\mathrm{n}}{L} \cdot T_\mathrm{on}, \tag{3.35}$$

$$\hat{I}_\mathrm{R} = \begin{cases} -\sqrt{\frac{2\,Q_\mathrm{C}}{L}\,(2\,v_\mathrm{n} - V_\mathrm{out})} & \text{for } v_\mathrm{n} > V_\mathrm{out}/2, \\ 0 & \text{for } v_\mathrm{n} \leq V_\mathrm{out}/2, \end{cases} \tag{3.36}$$

$$\hat{I}_\mathrm{Rp} = \begin{cases} \hat{I}_\mathrm{Rp,1} & \text{for } v_\mathrm{n} > V_\mathrm{out}/2, \\ \hat{I}_\mathrm{Rp,2} & \text{for } v_\mathrm{n} \leq V_\mathrm{out}/2, \end{cases} \tag{3.37}$$

$$\hat{I}_\mathrm{Rv} = \begin{cases} 0 & \text{for } v_\mathrm{n} > V_\mathrm{out}/2, \\ -\sqrt{\frac{2\,Q_\mathrm{C}}{L} \cdot (V_\mathrm{out} - 2\,v_\mathrm{n})} & \text{for } v_\mathrm{n} \leq V_\mathrm{out}/2. \end{cases} \tag{3.38}$$

The evaluation of (3.30) - (3.38) over a half cycle of the mains frequency results in the timing and current values presented in **Fig. 3.8** (c) and (d), respectively. As can be seen, the effect of the two cases, at $t = 2.1\,\mathrm{ms}$ where $v_\mathrm{n} = V_\mathrm{out}/2$, changes the slope of the current waveforms. However, the average current i_L shows the desired sinusoidal shape which is based on the proper calculation of the ON-time.

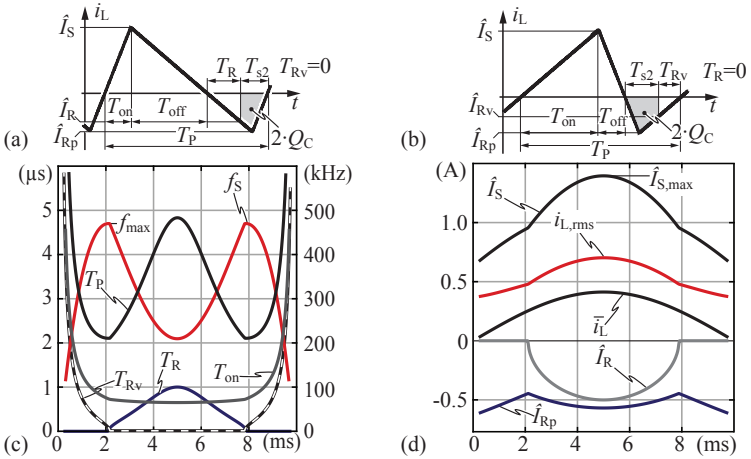


Fig. 3.8: (a) Inductor current waveform for $v_\mathrm{n} > V_\mathrm{out}/2$ and (b) for $v_\mathrm{n} \leq V_\mathrm{out}/2$. (c) Resulting switching timings and the switching frequency f_S over a half mains period. (d) Current values shown over a half mains period whereas $i_\mathrm{L,rms}$ is the local RMS value and $\bar{i}_\mathrm{L}$ is the local average value of the inductor current. Parameters: $V_\mathrm{n} = 230\,\mathrm{V}$, $V_\mathrm{out} = 400\,\mathrm{V}$, $L = 150\,\mu\mathrm{H}$, $Q_\mathrm{C} = 75.2\,\mathrm{nC}$, $P_\mathrm{out,i} = 200\,\mathrm{W}/3$. The output power is divided because three converter cells are considered.

3.4 Design of the converter

The closed-form description of the TCM PFC rectifier derived in the previous section allows for an analytical determination of the design parameters for the converter system. There are basically four parameters to be determined:

- The number of interleaved boost cells n_c,
- the output capacitor C_out,
- the boost inductors $L_{1\ldots\mathrm{n_c}}$,
- and the switches of all bridge legs.

The specifications considered for the converter design are listed in **Tab. 1.2**. Additionally, an output voltage ripple amplitude of $\Delta v_\mathrm{out} = 20\,\mathrm{V}$, cf. **Fig. 3.9** (a), has been considered which is a conventionally

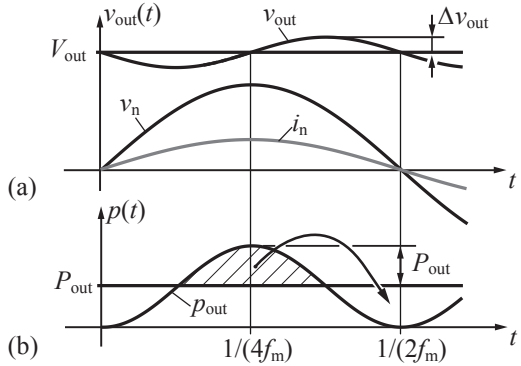


Fig. 3.9: The output capacitor has to smooth the power variation in single-phase AC-DC systems as indicated.

used value for a boost type PFC rectifier as it ensures the proper boost operation for the entire input voltage range including a tolerance of 10 % and still features a safety margin of

$$V_{out} - \Delta v_{out} - 1.1 \cdot \sqrt{2} \cdot V_n = 22\,\text{V}. \tag{3.39}$$

Besides, in the design a system efficiency of $\eta_{calc} = 90\,\%$ is assumed which accounts for the losses of the converter.

3.4.1 Output capacitor

The output capacitor C_{out} has to smooth the inherent energy flow variation of the output of single-phase AC-DC systems as illustrated in **Fig. 3.9**. In a PFC rectifier the input current i_n is directly proportional to the input voltage v_n and thus, a power variation with twice the mains frequency results,

$$\begin{aligned} p_{out}(t) &= \eta\, v_n(t)\, i_n(t) = \eta\, V_n\, I_n \cdot (1 - \cos(2\,\omega_m t)) = \\ &= P_{out} \cdot (1 - \cos(2\,\omega_m t))\,, \end{aligned} \tag{3.40}$$

where η accounts for the converter efficiency and $\omega_m = 2\pi f_m$ is the mains angular frequency.

The output power $p_{out}(t)$ consists of a constant power P_{out} which is aimed for the load and a time varying component $\Delta p_{out} = -P_{out} \cdot \cos(2\,\omega_m\, t)$ which is delivered to C_{out}. Accordingly, C_{out} has to deliver

energy to the load when $p_{\mathrm{out}}(t) < P_{\mathrm{out}}$. Assuming a constant output voltage V_{out}, the capacitor current can be derived with

$$i_{\mathrm{Cout}}(t) \approx \frac{\Delta p_{\mathrm{out}}(t)}{V_{\mathrm{out}}} = \frac{-P_{\mathrm{out}} \cdot \cos(2\,\omega_{\mathrm{m}}\,t)}{V_{\mathrm{out}}}. \tag{3.41}$$

With $i = C \cdot \mathrm{d}v/\mathrm{d}t$, the output voltage is

$$\begin{aligned} v_{\mathrm{out}}(t) &\approx V_{\mathrm{out}} + \frac{1}{C_{\mathrm{out}}} \int_0^t i_{\mathrm{Cout}}(\tau)\mathrm{d}\tau \\ &= V_{\mathrm{out}} - \frac{P_{\mathrm{out}}}{V_{\mathrm{out}}} \cdot \frac{1}{2\omega_{\mathrm{m}} C_{\mathrm{out}}} \cdot \sin(2\,\omega_{\mathrm{m}}\,t). \end{aligned} \tag{3.42}$$

Accordingly, the maximum output voltage ripple, cf. **Fig. 3.9** (a), results to be

$$\Delta v_{\mathrm{out}} = \frac{P_{\mathrm{out}}}{V_{\mathrm{out}}} \cdot \frac{1}{2\,\omega_{\mathrm{m}} C_{\mathrm{out}}}, \tag{3.43}$$

and the required capacitance for a specified Δv_{out} can be calculated. For a voltage ripple amplitude of $\Delta v_{\mathrm{out}} = 20\,\mathrm{V}$ of the output voltage, C_{out} is

$$C_{\mathrm{out}} = \frac{P_{\mathrm{out}}}{2\,\omega_{\mathrm{m}} \cdot \Delta v_{\mathrm{out}} \cdot V_{\mathrm{out}}} = 40\,\mu\mathrm{F}. \tag{3.44}$$

Conventionally used electrolyte capacitors are not applicable with respect to the height limitation. As presented in Section 1.3, chip capacitors with a voltage rating of 450 V which are thinner than 1 mm are nowadays available. By the time of implementation of the TCM PFC rectifier, capacitor chips exceeding the height limitation have been employed ($h = 2\,\mathrm{mm}$, $A = 100\,\mathrm{cm}^2$) in order to enable a reasonable footprint. Today, however, capacitor chips are available with the same footprint size but with a height of 1 mm.

In any case many capacitor chips are connected in parallel to realize the output capacitor and thus the ESR is very low ($\tan(\delta) < 0.01$). For that reason, the losses in the output capacitor have been neglected.

3.4.2 Switches

The maximum blocking voltage of the switches is approximately equal to the output voltage V_{out}. Considering the output voltage ripple in

Tab. 3.1: Parameters of the employed MOSFETs IPR60R385CP [56].

$R_{\mathrm{DS(on)}}$	=	385 mΩ @ 25 °C,	$V_{\mathrm{DS,max}}$	=	650 V,
Q_{C}	=	75.2 nC,	$Q_{\mathrm{g,typ}}$	=	17 nC,
Package	:	ThinPAK 8 × 8			

the capacitor C_{out}, the maximum drain-source voltage is thus

$$V_{\mathrm{DS,max}} = V_{\mathrm{out}} + \Delta v_{\mathrm{out}} = 420\,\mathrm{V}. \tag{3.45}$$

The ultra-flat design of the converter requires for MOSFET's with a thin package. Recently, Infineon [56] and ST [59] presented MOSFETs with a package thickness of $h \leq 1\,\mathrm{mm}$. Although the range of different switches with these packages is steadily increasing only one switch type with the required voltage rating has been available and is thus considered in the design. The parameters of the employed MOSFETs are listed in **Tab. 3.1**. For applications where a wide range of switches is available, the most suitable MOSFET is selected such that with its component parameters, $R_{\mathrm{DS(on)}}$, Q_{S}, and $Q_{\mathrm{g,typ}}$, a certain optimization target is achieved, e.g. minimum losses. For the sake of clarity and because only a single switch type has been available the design procedure presented in the following paragraphs is done for the chosen MOSFET.

Since the TCM PFC rectifier allows for ZVS over the entire mains period, switching losses have been neglected in the analysis and only conduction losses and the losses of the gate drive units are considered.

Conduction losses

The calculation of the currents through the switches of the HF bridge legs, cf. **Fig. 3.2** (b), is based on (3.30) which defines the required ON-time to obtain a specified average current $\bar{i}_{\mathrm{L}}$ in the inductor L, see **Fig. 3.8**. Knowing T_{on} enables the determination of all other currents and timing values during a switching cycle for a given

- input voltage v_{n},
- output voltage V_{out},
- output power $P_{\mathrm{out,i}} = P_{\mathrm{out}}/n_{\mathrm{c}}$,
- effective output charge of each MOSFET Q_{C}, and

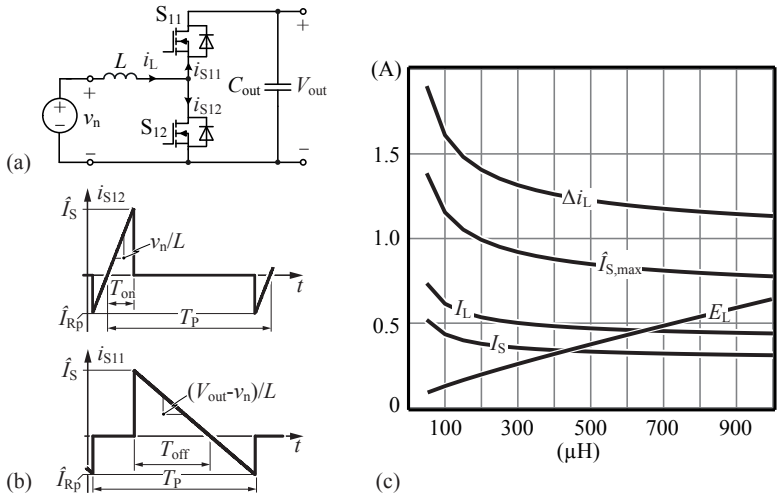


Fig. 3.10: (a) Equivalent circuit of a single cell for positive v_n and (b) the respective MOSFETs current waveforms for $v_\mathrm{n} > V_\mathrm{out}/2$. (c) Calculated currents and the energy stored in the boost inductance as a function of the inductance value L for three paralleled boost cells ($n_\mathrm{c} = 3$).

- inductance L,

which was shown in the previous section. Note that the output power $P_\mathrm{out,i}$ of a single boost cell scales with n_c which also changes the local average current $\overline{i}_\mathrm{L}(t)$. Thus the inductor current is

$$\overline{i}_\mathrm{L}(t) = \frac{\sqrt{2}\,P_\mathrm{out,i}}{\eta_\mathrm{calc}\,V_\mathrm{n}} \cdot \sin(\omega_\mathrm{m}\,t) = \frac{\sqrt{2}\,P_\mathrm{out}}{n_\mathrm{c}\,\eta_\mathrm{calc}\,V_\mathrm{n}} \cdot \sin(\omega_\mathrm{m}\,t). \tag{3.46}$$

Considering **Fig. 3.10** (b), the local RMS values, $i_\mathrm{S11,rms}$ and $i_\mathrm{S12,rms}$, of the switch currents for the mains period can immediately be derived with

$$i_\mathrm{S12,rms} = \sqrt{\frac{\hat{I}_\mathrm{S}^2}{3} \cdot \frac{T_\mathrm{on}}{T_\mathrm{P}} + \frac{\hat{I}_\mathrm{Rp}^2}{3\,T_\mathrm{P}} \cdot \frac{L \cdot (-\hat{I}_\mathrm{Rp})}{v_\mathrm{n}}}, \tag{3.47}$$

$$i_\mathrm{S11,rms} = \sqrt{\frac{\hat{I}_\mathrm{S}^2}{3} \cdot \frac{T_\mathrm{off}}{T_\mathrm{P}} + \frac{\hat{I}_\mathrm{Rp}^2}{3\,T_\mathrm{P}} \cdot \frac{L \cdot (-\hat{I}_\mathrm{Rp})}{V_\mathrm{out} - v_\mathrm{n}}}, \tag{3.48}$$

whereas T_P and $\hat{I}_\mathrm{Rp}$ are defined in (3.30) and (3.37), respectively. Note, that (3.47) and (3.48) are valid for $v_\mathrm{n} > V_\mathrm{out}/2$ and for $v_\mathrm{n} \leq V_\mathrm{out}/2$.

Since the modulation for the negative half line cycle is complementary to the positive cycle both switches have the same RMS current over a mains period which is

$$I_\mathrm{S} = \sqrt{\frac{1}{T_\mathrm{m}} \cdot \left(\int_0^{T_\mathrm{m}/2} i_\mathrm{S11,rms}(t)^2 \,\mathrm{d}t + \int_0^{T_\mathrm{m}/2} i_\mathrm{S12,rms}(t)^2 \,\mathrm{d}t \right)}, \quad (3.49)$$

and thus, assuming a negligible junction temperature change of the MOSFET during a full line cycle, the conduction losses $P_\mathrm{cond,HF}$ of the HF bridge legs can be calculated as

$$P_\mathrm{cond,HF} = 2\, n_\mathrm{c} \cdot R_\mathrm{DS(on)}\, I_\mathrm{S}^2. \quad (3.50)$$

Fig. 3.10 (c) presents the RMS current I_S through the HF MOSFETs as a function of the inductance value L and for $n_\mathrm{c} = 3$. As can be seen, for inductances higher than $L = 150\,\mu\mathrm{H}$ the current is almost constant and the inductance has minor influence on the conduction losses of the switches.

The current through the LF bridge leg composed of the switches $\mathrm{S_{N1}}$ and $\mathrm{S_{N2}}$, cf. **Fig. 3.2** (b), is the sum of all inductor currents. Each switch conducts during one half cycle and assuming a proper interleaving control, the RMS current through each switch can be approximated with the input current I_n, i.e. the HF current ripple of i_n is neglected:

$$I_\mathrm{Sn} \approx \frac{I_\mathrm{n}}{\sqrt{2}} = \frac{P_\mathrm{out}}{\sqrt{2}\,\eta_\mathrm{calc}\, V_\mathrm{n}} = 683\,\mathrm{mA}. \quad (3.51)$$

The conduction losses $P_\mathrm{cond,LF}$ in the LF bridge leg is

$$P_\mathrm{cond,LF} = 2\, R_\mathrm{DS(on)}\, I_\mathrm{Sn}^2 = 420\,\mathrm{mW}, \quad (3.52)$$

whereas $R_\mathrm{DS(on)} = 450\,\mathrm{m\Omega}$ at $50\,^\circ\mathrm{C}$ has been applied.

Gate drive unit losses

The losses caused by the gate drive units are determined with

$$P_\mathrm{gd} = 2\, n_\mathrm{c} \cdot Q_\mathrm{g,typ} \cdot V_\mathrm{GS} \cdot \frac{2}{T_\mathrm{m}} \int_0^{T_\mathrm{m}/2} f_\mathrm{S}(t)\mathrm{d}t. \quad (3.53)$$

V_GS is the gate-source voltage which is 12 V in the case at hand.

3.4.3 Boost inductors

In order to design the boost inductor of the TCM PFC rectifier, the applied currents and the switching frequency need to be derived. Since the inductance value L is not yet determined, several parameters required for the inductor design need to be evaluated as a function of L. The needed parameters are:

- The RMS current I_{L} which determines the winding losses.
- The peak current $\hat{I}_{\mathrm{S,max}}$ which is needed to comply with the saturation limit.
- The ripple current Δi_{L},
- and the design frequency f_{d} which determine the core losses.

Based on these parameters, the inductor geometry can be designed and optimized with respect to a certain goal, e.g. high efficiency or a small footprint size. With respect to an ultra-flat realization of the boost inductor, the parameters are applied to the design procedure which is presented in Section 5.3. The considered integration method is illustrated in **Fig. 1.8** (b) where the core is integrated into the PCB and the windings are realized as tracks and vias.

Apart from the electrical parameters, i.e. the currents and the switching frequency, geometric and magnetic input parameters are needed, e.g. the applied core material, the thickness of the core, the required isolation distance between the tracks, etc. The result of the proposed design procedure is an optimized ultra-flat inductor design with respect to the efficiency η_{L} and/or the area-related power density α_{L}:

$$\eta_{\mathrm{L}} = \frac{P_{\mathrm{out,L}}}{P_{\mathrm{out,L}} + P_{\mathrm{L}}}, \qquad \alpha_{\mathrm{L}} = \frac{P_{\mathrm{out,L}}}{A_{\mathrm{L}}}, \tag{3.54}$$

where $P_{\mathrm{out,L}}$ is rated power of the inductor, P_{L} is the sum of core and winding losses of the inductor, and A_{L} is the total required footprint size of the inductor.

This design procedure can be executed for a specified range of $L \in [L_{\mathrm{min}} \dots L_{\mathrm{max}}]$ and the resulting α-η Pareto Front shows a trade-off between an efficient or a compact setup for several applied inductance values and allows for the determination of the optimal L.

In the following paragraphs, analytical expression for the currents and the design frequency are derived as a function of L which are needed for the inductor design procedure.

Winding losses

Considering the inductor current waveform illustrated in **Fig. 3.8** (a) and (b) and applying some basic algebra, the local RMS current can be derived

$$i_{\mathrm{L,rms}} = \sqrt{\frac{1}{3\,T_\mathrm{P}} \frac{V_\mathrm{out}}{V_\mathrm{out} - v_\mathrm{n}} \cdot \left(\hat{I}_\mathrm{S}^2\, T_\mathrm{on} + \hat{I}_\mathrm{Rp}^2 \cdot \frac{L\,(-\hat{I}_\mathrm{Rp})}{v_\mathrm{n}} \right)}, \tag{3.55}$$

and the integration over a half line cycle yields the RMS current I_L over a mains period

$$I_\mathrm{L} = \sqrt{\frac{2}{T_\mathrm{m}} \int_0^{T_\mathrm{m}/2} i_{\mathrm{L,rms}}(t)^2 \,\mathrm{d}t}. \tag{3.56}$$

Fig. 3.10 (c) depicts I_L as a function of the inductance L and for $n_\mathrm{c} = 3$. With the RMS value of the inductor current, the winding losses of the converter for a particular inductor design can be calculated,

$$P_\mathrm{wind} = n_\mathrm{c} \cdot R_\mathrm{wind} \cdot I_\mathrm{L}^2. \tag{3.57}$$

Core losses

The design of the boost inductor is based on the maximum core losses within a mains period. Referring to the Steinmetz equation [83], the core losses in an inductor are proportional to

$$P_\mathrm{core} \propto f_\mathrm{S}^\alpha \cdot (\Delta B)^\beta \propto f_\mathrm{S}^\alpha \cdot (\Delta i_\mathrm{L})^\beta. \tag{3.58}$$

The impact of a Dc offset of the core excitation can also be included in (3.58). For the considered material Vitrovac 6155F, however, the impact of the Dc offset is negligible, cf. Chapter 5. With (3.58) the operating point with maximum core losses can be determined.

The flux density swing ΔB is proportional to the inductor ripple current $\Delta i_\mathrm{L} = \hat{I}_\mathrm{S} - \hat{I}_\mathrm{Rp}$, cf. **Fig. 3.8**, and considering (3.35) and (3.37) Δi_L can be calculated over a half line cycle. The resulting current

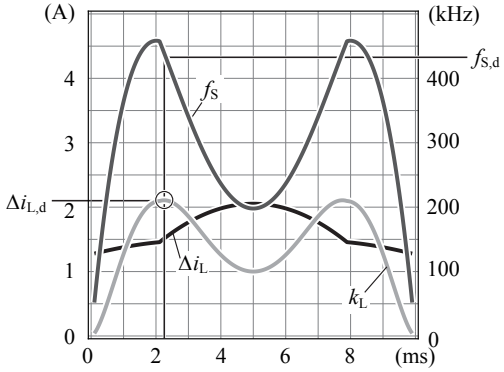


Fig. 3.11: Switching frequency f_S, inductor ripple current Δi_L, and relative core losses $k_L(n_c, L)$, cf. (3.59), calculated for $L = 150\,\mu H$, $n_c = 3$, and VITROVAC 6155F (easy direction, cf. **Tab. 5.2**).

ripple Δi_L is shown in **Fig. 3.11** for an inductance of $L = 150\,\mu H$ and for $n_c = 3$. **Fig. 3.11** also presents the switching frequency $f_S = 1/T_P$ evaluated with (3.34) over a half line cycle. The core loss ratio

$$k_L(n_c, L) = \frac{P_{core}(f_S(t), \Delta i_L(t))}{P_{core}(\Delta i_{L,max})} \tag{3.59}$$

can be calculated for each combination of $\{n_c, L\}$ and for a specified core material. Note that $P_{core}(\Delta i_{L,max})$ occurs at $t = 5\,ms$ where $\bar{i}_L$ is maximal. **Fig. 3.11** plots $k_L(n_c, L)$ over a mains half line cycle for VITROVAC 6155F, $n_c = 3$, and $L = 150\,\mu H$ and it can be seen that the maximum core losses occur neither at $t = 5\,ms$ (maximum Δi_L) nor at $t \approx 1.1\,ms$ (maximum f_S) but in between. The frequency $f_{S,d}$ and the ripple current $\Delta i_{L,d}$ which yield the maximal core losses have to be considered for the design of the boost inductor.

The maximal allowable power loss per area, p_{loss}, which is introduced in Section 5.2.4, limits the allowable ΔB and hence Δi_L. The saturation flux density limits the maximal inductor current occuring during a mains period,

$$\hat{I}_{S,max} = \hat{I}_S(v_n = 325\,V + 10\,\%). \tag{3.60}$$

With all input parameters required for the inductor design procedure being known as a function of the L, the inductor design procedure can

Tab. 3.2: Input parameters for the design procedure of the TCM PFC rectifier.

V_n	=	230 V	a_start	=	2 mm
V_out	=	400 V	a_stop	=	30 mm
P_out	=	200 W	Δa	=	1 mm
n_c	=	2 . . . 5	p_loss	=	0.3 W/cm^2
L_start	=	50 µH	d_core	=	0.8 mm
L_stop	=	1 mH	d_track	=	35 µm
ΔL	=	50 µH	d_iso	=	0.5 mm
N_start	=	10	d_cv	=	1 mm
N_stop	=	400	Material: VITROVAC 6155F		
ΔN	=	2	Switches: see Tab. 3.1		
J_max	=	20 A/mm^2	A_wiring	=	100 cm^2
η_calc	=	0.9	A_Cout	=	100 cm^2
P_aux	=	2 W	A_EMI	=	100 cm^2

be embedded into the design procedure of the overall converter system which is detailed in the following subsection.

3.4.4 Converter optimization

Since analytical models of several loss components of the TCM PFC rectifier are determined, a design procedure can be applied which iterates over a specified input parameter range to yield the optimal converter design with respect to the efficiency η and/or the area-related power density α:

$$\eta = \frac{P_\mathrm{out}}{P_\mathrm{out} + P_\mathrm{loss,tot}}, \qquad \alpha = \frac{P_\mathrm{out}}{A_\mathrm{tot}}, \tag{3.61}$$

where P_out is output power of the converter, $P_\mathrm{loss,tot}$ is the sum of all converter losses, and A_tot is the total required footprint size of the converter.

Fig. 3.12 depicts the design procedure of the TCM PFC rectifier. The input parameters given in the flowchart are either defined by the converter specification or are geometrical, electrical, and magnetical

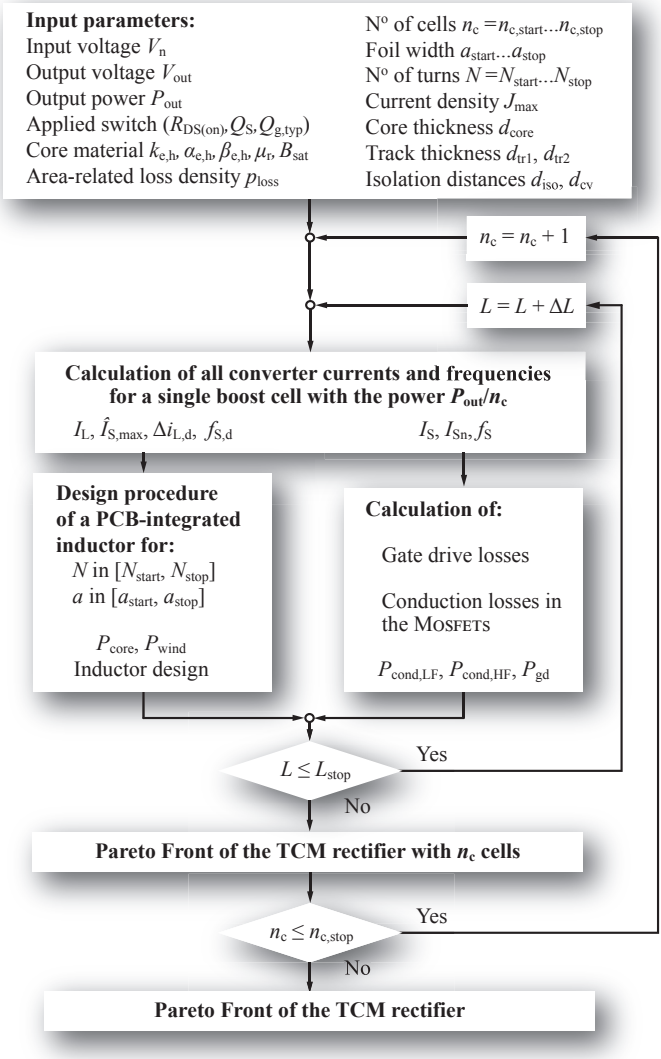


Fig. 3.12: Flowchart of the design of the TCM PFC rectifier. The design procedure of a PCB-integrated inductor is done according to **Fig. 5.15**.

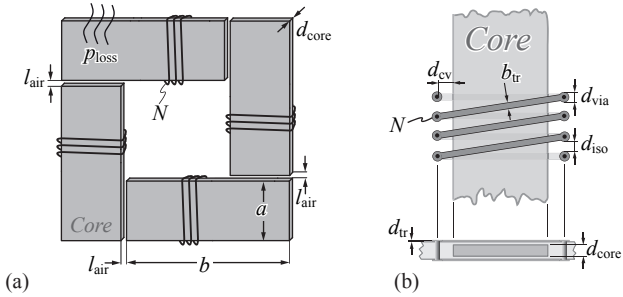


Fig. 3.13: (a) Scaleable model of the considered PCB-integrated boost inductor. (b) Winding parameters.

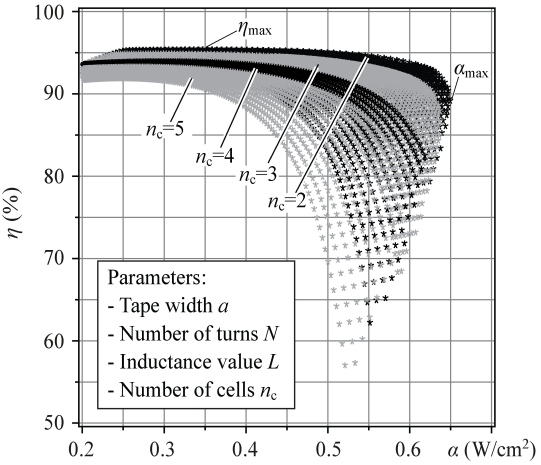


Fig. 3.14: α-η-Pareto Front of the TCM PFC rectifier for several numbers of interleaved converter cells and the input parameters listed in **Tab. 3.2**. The maximum efficiency is $\eta_{max} = 95.7\,\%$ and the maximum area-related power density is $\alpha_{max} = 0.65\,\mathrm{W/cm^2}$.

parameters of the PCB-integrated inductor. The scaleable model of the considered inductor is illustrated in **Fig. 3.13** (a) and the winding parameters are shown in **Fig. 3.13** (b). A detailed discussion of all parameter and the inductor design procedure is given in Chapter 5.

With all input parameters, the converter currents and the switching

frequencies for a certain n_c and L can be calculated. With the inductor currents Δi_L, I_L, $I_{S,max}$, and the design frequency f_d known, the design procedure for the boost inductor can be executed which results the geometric parameters and the power losses for several values of the number of turns N and the core width a, cf. **Fig. 3.13**. The conduction losses in the MOSFETs and the gate drive losses can be calculated and an auxiliary power loss of $P_{aux} = 2\,W$ has been considered which accounts for the power consumption of the DSP and the FPGA.

Furthermore, the area requirement for the output capacitor C_{out} and for the wiring and placement of components is included in the procedure, $A_{Cout} = 100\,cm^2$ and $A_{wiring} = 100\,cm^2$.

The required attenuation of the EMI filter of the PFC rectifier depends on the number of parallel cells n_c and the applied inductor value L. A sophisticated modelling of the EMI filter size is needed to derive the relation between the required EMI footprint size and these two values, i.e. n_c and L [84,85]. For the sake of simplicity, in this optimization procedure, the required footprint size of the EMI filter is assumed to be $A_{EMI} = 100\,cm^2$ for all designs which is based on a comparable design of a PCB-integrated EMI filter for a flyback type rectifier, cf. Chapter 6.

So, the area contributions considered in the design optimization are

$$A_{tot} = n_c \cdot A_L + A_{Cout} + A_{wiring} + A_{EMI}, \tag{3.62}$$

and the considered losses are

$$P_{loss,tot} = n_c \cdot (P_{core} + P_{wind}) + P_{cond,HF} + P_{gd} + P_{cond,LF} + P_{aux}. \tag{3.63}$$

The resulting Pareto Front for the converter system is presented in **Fig. 3.14**. Each point represents a possible design and as can be seen the amount of different designs is large due to the large input parameter space. In order to obtain an optimal design, first the number of parallel boost cells n_c will be addressed.

Fig. 3.14 shows the range of possible designs for different n_c. The highest power density $\alpha_{max} = 0.65\,W/cm^2$, which corresponds to a $175 \times 175\,mm^2$ large PCB, and the highest efficiency $\eta_{max} = 95.7\,\%$ can be obtained for two interleaved boost cells ($n_c = 2$). The reason behind that is the low specified output power. Referring to **Fig. 3.8** (a), the inductor current i_L consists of a positive and a negative current share during a switching period. The negative current is required to ensure ZVS. The peak current $\hat{I}_S$ is determined by the average current $\bar{i}_L$, which is defined by the required output power, and by the negative current

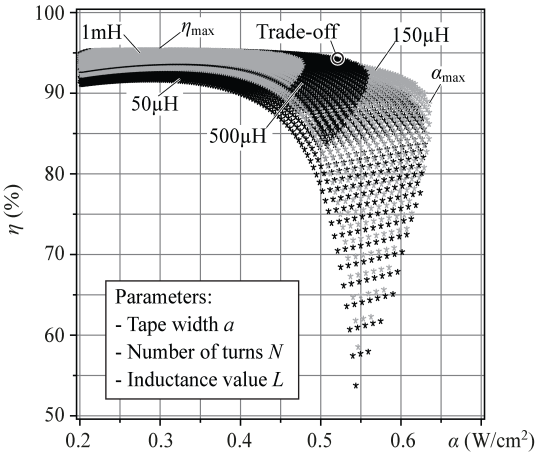


Fig. 3.15: Pareto Front of the TCM PFC rectifier for $n_c = 3$ parallel boost cells. The optimal efficiency is at $\eta_{max,3} = 95.4\,\%$ and the maximum power density is $\alpha_{max,3} = 0.63\,\mathrm{W/cm^2}$.

contribution during a switching period. Even if no energy is transferred to the output, i.e. for $\hat{I}_{Rp} = -\hat{I}_S$, the ripple current in the inductor, $\hat{I}_S - \hat{I}_{Rp}$, causes conduction and core losses. For a higher output power (>1 kW), the influence of the negative current contribution is small. In the case at hand, however, the output power of only 200 W is divided to the n_c paralleled boost cells and the average inductor current $\bar{i}_L$ is low. Thus, the inductor current ripple Δi_L is significantly determined by the negative current, I_{Rp}, needed for ZVS which decreases the achieveable power density and the achieveable efficiency.

The difference of α between $n_c = 2$ and $n_c = 3$, however, is very small ($A_{min,2} = 306\,\mathrm{cm^2}$, $A_{min,3} = 318\,\mathrm{cm^2}$) and since a higher number of interleaved cells also improves the distribution of the losses and simplifies the design and the implementation of the PCB-integrated boost inductors the number of parallel boost cells is chosen to be

$$n_c = 3, \tag{3.64}$$

which allows for $\eta_{max,3} = 95.4\,\%$ or $\alpha_{max,3} = 0.63\,\mathrm{W/cm^2}$.

Fig. 3.15 illustrates the Pareto Front for a TCM rectifier consisting of $n_c = 3$ boost cells which allows for a good insight into the impact of

different inductance values on the system performance.

The stored magnetic energy in the boost inductor, E_{L}, increases with increasing L which is shown in **Fig. 3.10** (c). Since the stored energy is proportional to the inductor volume, cf. [84], a high power density requires for a low inductance value. This is confirmed by the results of the design procedure. For example, for $L = 150\,\mu\mathrm{H}$ the achievable power density is $\alpha = 0.63\,\mathrm{W/cm^2}$ whereas for $L = 500\,\mu\mathrm{H}$ only $\alpha = 0.56\,\mathrm{W/cm^2}$ can be reached. With decreasing inductance, however, the switching frequency and the flux density swing increase which results in higher inductor losses. In order to comply with the maximum allowable power loss per area, p_{loss}, cf. Section 5.2.4, the inductor needs a larger footprint size. Thus, α decreases for $L < 150\,\mu\mathrm{H}$. The optimal inductance with regard to the power density is $L = 150\,\mu\mathrm{H}$.

The optimal inductance with regard to the efficiency is $L = 1\,\mathrm{mH}$ where $\eta_{\mathrm{max},3} = 95.4\,\%$ can be achieved because for high inductance values the switching frequency and the inductor current ripple are low which allows for low core losses.

For the implemented prototype an inductance of

$$L = 150\,\mu\mathrm{H} \tag{3.65}$$

has been chosen as it allows for the highest power density or a reasonably high efficiency of the converter ($\alpha_{\mathrm{max},3} = 0.63\,\mathrm{W/cm^2}$, $\eta_{\mathrm{max},3,150\mu\mathrm{H}} = 94.7\,\%$).

Since the number of parallel boost cells n_{c} and the inductance value L are determined, the design of the inductor remains to be optimized. Applying the design procedure discussed in Section 5.3 to the boost inductor yields the α-η-Pareto Front presented in **Fig. 3.16** (a) which depicts several inductor designs with the number of turns N and the core width a as parameters. The optimal designs with respect to η or α are indicated and an illustration of the inductor with PCB-integrated core and with the windings realized as tracks and vias is shown in **Fig. 3.16** (b); there, the dimensions for both optima are given and depending on the application or the preference a trade-off between those two values can be chosen. A thorough discussion of the Pareto Front of a PCB-integrated magnetic component is given in Section 5.3.

Considering an inductor design which allows for a reasonable trade-off between the efficiency $\eta = 95.7\,\%$ and the power density $\alpha = 1.74\,\mathrm{W/cm^2}$ indicated in **Fig. 3.16** (a), the core losses are $P_{\mathrm{core}} = 2.6\,\mathrm{W}$ and winding losses are $P_{\mathrm{wind}} = 0.7\,\mathrm{W}$. For this inductor design, the

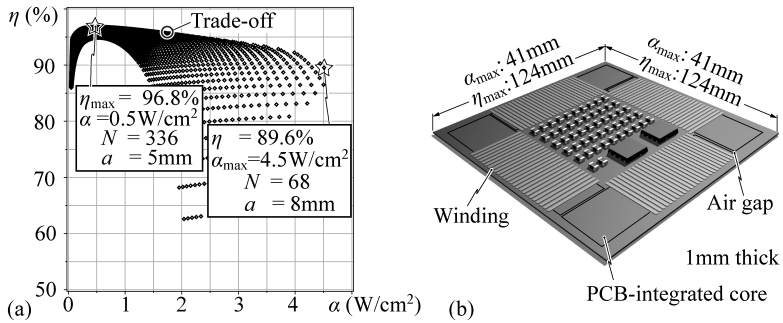


Fig. 3.16: (a) α-η-Pareto Front of a PCB-integrated boost inductor which allows for an ultra-flat realization of the converter system. (b) 3-D sketch of a PCB-integrated boost inductor.

achievable performance of the 3-cell TCM PFC rectifier is $\eta = 94.0\,\%$ and $\alpha = 0.52\,\mathrm{W/cm^2}$, cf. **Fig. 3.15**. The core losses of the three inductors account for 70 % of the total losses $P_{\mathrm{loss,tot}} = 14.2\,\mathrm{W}$. Thus, the PCB-integrated inductor truly determines the power density and the efficiency of the TCM PFC rectifier.

In that context, the question arises if TCM operation is benefical at all because the modulation increases the flux density swing in the core and the RMS value of the inductor currents compared to a conventional BCM modulation scheme. Considering a design with the efficiency $\eta = 94.0\,\%$, the conventional BCM operation which loses ZVS during the mains period reduces the inductor losses by 4.1 W (5.7 W instead of 9.8 W for all three inductors). This inductor loss reduction, however, comes at the expense of switching losses which are 1.9 W for each of the six switches. As a consequence the overall losses increase by 7.3 W which would decrease the efficiency from 94.0 % to 90.3 %. Altogether, TCM operation can really be considered to be an appropriate modulation scheme for the considered PFC rectifier system.

3.5 Control of the TCM PFC rectifier

Based on the switching cycle discussed in Section 3.2 and the simplified model of the switching transition detailed in Section 3.3, the converter control is described in this section. **Fig. 3.17** (a) exemplarily depicts

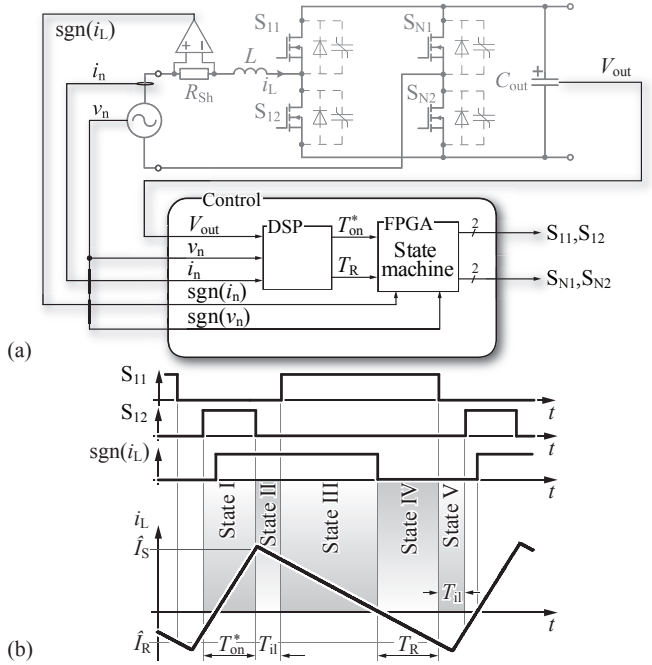


Fig. 3.17: (a) Schematic and simplified control structure of a single-cell TCM PFC rectifier which shows all required measurements. The state machine goes through each stage depicted in (b). It requires T^*_{on} and T_R which are determined in the DSP and the zero-crossing signal of the inductor current. A constant interlock delay T_{il} is considered.

one of the three cells of the TCM rectifier including an overview of the control structure. The input quantities required for the control are the input voltage v_n, the output voltage V_{out}, the input current i_n, and the sign of the inductor current which is determined using a shunt resistor and a high-speed comparator in each inductor path [67]. For power converters up to several kW a current transformer with saturable core may be employed instead of the shunt resistors to reduce the conduction losses [86].

The DSP calculates the required ON-time T_{on} and the reverse conduction time T_R according to the instantaneous values of v_n, V_{out}, and i_n. With T_{on}, T_R, and the sign of the inductor current, a state machine

implemented in a FPGA generates the switching pattern illustrated in **Fig. 3.17** (b). The transitions between the five states are determined by either the specified timing value (State I, II, IV, and V) or the zero-crossing detection (State III → State IV). A constant interlocking delay time T_{il} is assumed for State II and V ($T_{\mathrm{il}} = 400\,\mathrm{ns}$ for the realized prototype).

The zero-crossing detection of the currents is slightly time delayed because of the measurment and the required computation time of FPGA and DSP. Therefore, in practive I_{Rp} is slightly larger than the theoretically required value and *Interval 6* comes to pass even for $v_{\mathrm{n}} > V_{\mathrm{out}}/2$, cf. Section 3.4. During the inductor current i_{L} flows through the body diode of S_{12} the switch can be turned-ON with ZVS. So, contrary to the analysis of Section 3.2, State I starts before the zero-crossing of the i_{L}, cf. **Fig. 3.17** (b), as the triggering of State I using the zero-current signal would be slightly time delayed and S_{12} would be turned-ON without ZVS. The feedback controller regulates the ON-time T^{*}_{on} in order to account for the additional time before the zero-crossing of i_{L}. The time delay of the zero-crossing signal triggering State IV is not critical as there is no switching transition involved which could lose ZVS.

Extending the control structure depicted in **Fig. 3.17** to a 3-cell configuration yields the simulation result presented in **Fig. 3.18**. The magnified part shows the input current i_{n} and the three inductor currents $i_{\mathrm{L1...L3}}$ and illustrates the input current ripple reduction achieved by means of interleaving the inductor currents. Applying a 1^{st} order low pass filter with a cut-off frequency of $f_{\mathrm{c}} = 16\,\mathrm{kHz}$ the depicted input current i^{*}_{n} with simulated THD and power factor values of THD = 6.9 % and PF = 99.6 % results at $V_{\mathrm{n}} = 230\,\mathrm{V}$, $V_{\mathrm{out}} = 400\,\mathrm{V}$, $P_{\mathrm{out}} = 200\,\mathrm{W}$.

Fig. 3.19 presents the principle of the implemented interleaving control for two boost cells with the corresponding inductor currents i_{L1} and i_{L2}. There, the boost cell conducting i_{L1} is considered as master cell to which all other cells are synchronized. The required input signals are the zero-crossing signal of each inductor current. Each boost cell signals the end of a period (EoP_i) with a corresponding zero-crossing signal, which is obtained from a change of the sign of the respective inductor current, $\mathrm{sgn}(i_{\mathrm{L1}})$ or $\mathrm{sgn}(i_{\mathrm{L2}})$[2]. Depending on the cell which generates the EoP signal, the counter value, y_1 or y_2, is obtained and the counter is reset. y_1 and y_2 are proportional to $T_{\mathrm{P}} - \Delta T$ and to

[2]For $v_{\mathrm{n}} > 0$ the rising edges of $\mathrm{sgn}(i_{\mathrm{L1}})$ and $\mathrm{sgn}(i_{\mathrm{L2}})$ issue the respective signals EoP_1 and EoP_2. For $v_{\mathrm{n}} < 0$ the falling edges of $\mathrm{sgn}(i_{\mathrm{L1,2}})$ issue $\mathrm{EoP}_{1,2}$.

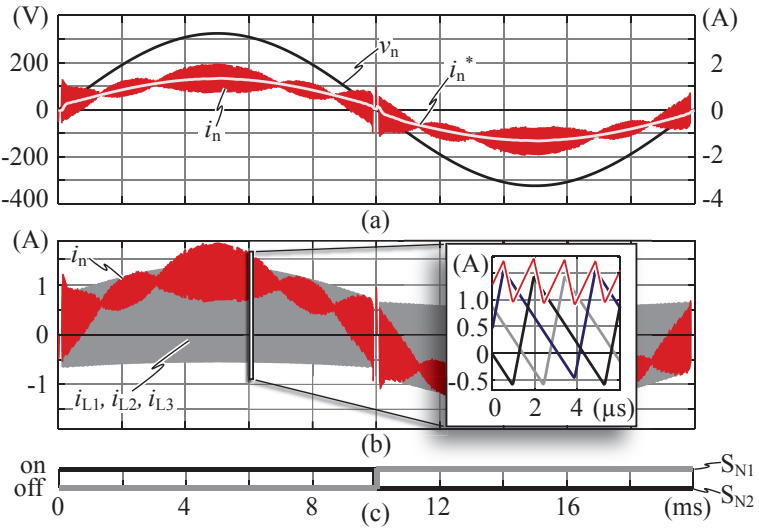


Fig. 3.18: Simulation results for a 200 W 3-cell TCM rectifier system, cf. **Fig. 3.2** (b). (a) Mains voltage v_n, input current i_n, and 1st order low pass filtered input current i_n^* ($f_c = 16\,\text{kHz}$). (b) Inductor currents including a magnified view which shows the smoothing effect of the superposition on the input current i_n. (c) Gate signals of the low frequency switching bridge-leg.

ΔT, respectively, and the desired delay between the two phases can be adjusted by selecting the ratio between y_1 and y_2. For example, a delay of $T_P/3$ requires y_1 to be twice the value of y_2, cf **Fig. 3.19**. Any deviation from this ratio is used as control parameter, ΔT_{on}, and added to the slave cell as an extension or a reduction of its ON-time.

The interleaving control and the state machines for each boost cell are implemented in a FPGA. **Fig. 3.20** presents the implemented control of the multi-cell TCM PFC rectifier. The sign of the input voltage, $\text{sgn}(v_n)$, defines which switch of a bridge-leg is considered as boost switch and which is the free-wheeling switch. E.g. for positive v_n, S_{x1} is the free-wheeling switch and S_{x2} is the boost switch where x corresponds to the bridge-legs $x = 1 \ldots 3$.

The bridge-leg with S_{N1} and S_{N2} switches synchronously to the mains frequency, cf. **Fig. 3.18** (c). For positive input voltages v_n, S_{N1} is turned-OFF while S_{N2} is turned-ON and vice versa. This bridge-leg

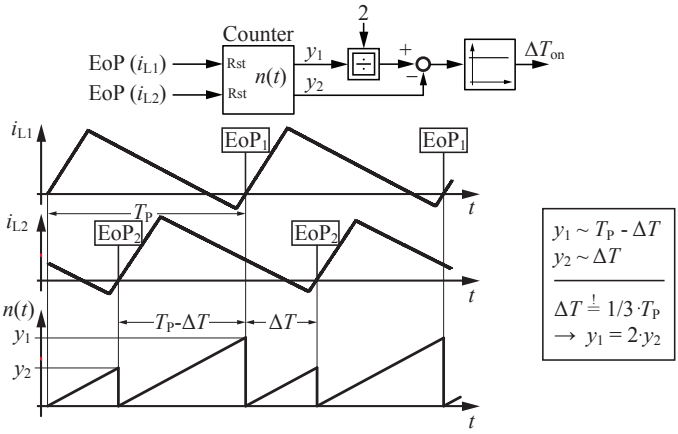


Fig. 3.19: Evaluation of the control signal for the interleaving control which is based on the End-of-Period signals (EoP) of each inductor current $i_{L1} - i_{L2}$. A counter is reset at EoP of each current and the values are then compared to each other.

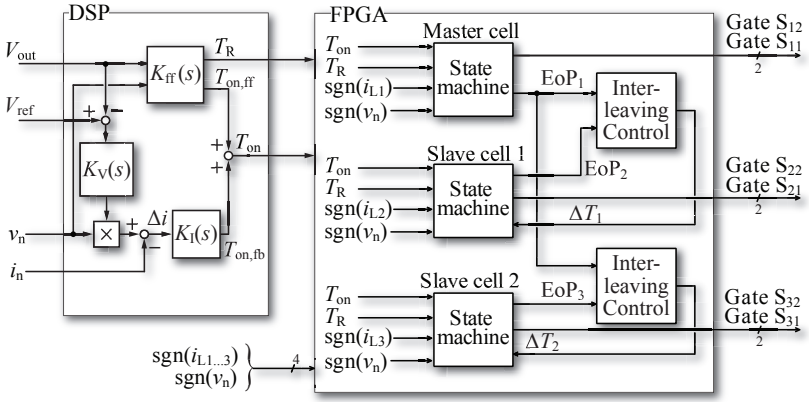


Fig. 3.20: Schematic of the control structure of the converter system which is subdivided into the state machine of each HF bridge-leg and the interleaving control of the inductor currents which are implemented in a FPGA and a superimposed input current and output voltage control realized in a DSP.

is hard-switched and considerable charging currents occur during the switching transitions. In order to prevent high charging currents during the switching operation of S_{N1} and S_{N2}, the switching speed of the LF bridge leg is decreased by selecting a very high gate resistance of 20 kΩ, which yields a total turn-ON time of 60 µs. The slow switching speed of the LF bridge-leg has no effect on the converter operation if the LF bridge-leg is switched during the zero-crossing of v_n, since the converter system is only switching if the rectified input voltage is greater than a certain threshold voltage. The selected threshold voltage of 22 V facilitates a maximum OFF-time of 196 µs at maximum mains voltage, $V_{n,max} = 230\,V + 10\,\%$, and thus enough time to turn-ON S_{N1} or S_{N2}. With this modification the current spikes reported in [81] are avoided and a smooth zero crossing of the input voltage is achieved without the need for a special gate signal pattern applied to the HF bridge-legs as proposed in [80].

The control structure implemented in the DSP consists of a (mains voltage) feed-forward controller $K_{ff}(s)$, a current controller $K_I(s)$, and a superimposed output voltage controller $K_V(s)$. The current controller and the output voltage controller are conventionally designed PI-controllers, e.g. [82, 87]. The feed-forward controller K_{ff} calculates $T_{on,ff}$ and T_R according to (3.22) and (3.17), respectively.

3.6 Laboratory setup

In order to validate the proposed model and the simulation results, a 200 W TCM PFC rectifier has been designed and implemented. Due to the manufacturing effort, the boost inductors are not PCB-integrated but consist of EIR cores [43] which allow for a flat realization of the inductors with a thickness of $h = 5$ mm. All components of the implemented prototype are surface mounted in order to simplify the manufacturing, tests, and measurements. A converter thickness of 1 mm would be feasible with all components being integrated into the PCB.

Fig. 3.21 shows the prototype and labels each functional block; **Tab. 3.3** lists the circuit parameters of the prototype. **Fig. 3.22** (a) and (b) present the measured inductor currents and the switch voltage v_{S12} for the prototype being operated as DC-DC converter at two different operating points. Obviously, v_{S12} declines to 0 V and ZVS is achieved. Furthermore, the interleaving control of the inductor currents works properly. The absolute value of the measured peak reverse

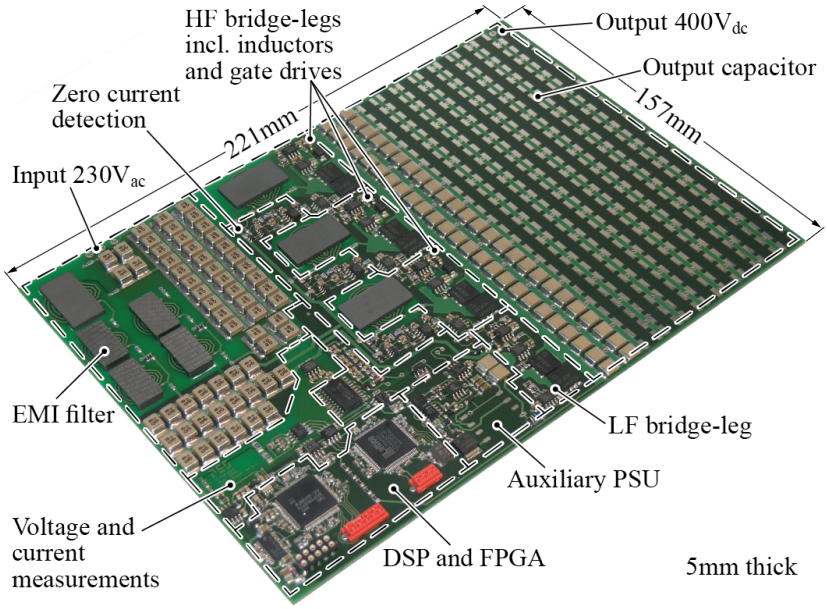


Fig. 3.21: Prototype of a flat TCM boost-type PFC rectifier with three interleaved boost-cells. All components are selected with respect to a flat realization of the converter.

current $\hat{I}_{\mathrm{Rp}}$ is greater than the calculated value ($\hat{I}_{\mathrm{Rp,calc}} = -570\,\mathrm{mA}$, $\hat{I}_{\mathrm{R,meas}} = -750\,\mathrm{mA}$ at $v_{\mathrm{n}} = 325\,\mathrm{V}$ and $V_{\mathrm{out}} = 400\,\mathrm{V}$) due to the time delay imposed by the zero-current detection, the signal processing in the FPGA, and the turn-off delay of the switch.

Fig. 3.22 further depicts the measured efficiencies for both Dc-Dc operating points and **Fig. 3.23** lists the loss contribution calculated according to Section 3.4 for each component. The calculated efficiencies agree well to the measured values. As expected, the core losses of the boost inductor determine the overall efficiency and hence, a reduction of the core losses enables a further efficiency improvement. Note that the core losses at $v_{\mathrm{n}} = 230\,\mathrm{V}$ are higher than at 325 V because the operating point at 230 V is closer to the operating point where the maximum core losses occur ($f_{\mathrm{S,d}}$, $\Delta i_{\mathrm{L,d}}$, see **Fig. 3.11**).

For PFC rectifier operation the prototype achieves an efficiency of $\eta = 94.6\,\%$ and a power factor PF $= 99.3\,\%$ at full load, i.e.

Tab. 3.3: Circuit parameters of the 200 W TCM PFC rectifier depicted in **Fig. 3.21**.

Size: 221 mm × 157 mm × 5 mm			
Inductors EIR 23/5/13 [43]		**DSP and FPGA**	
L	150 µH	DSP	TMS320F2808 [88]
N	20	FPGA	LCMXO2280C [89]
I_{sat}	1.85 A		
Material	N49		
Mosfets IPL60R385CP [56]		**Output capacitor [41]**	
$R_{DS(on)}$	385 mΩ @ 25 °C	C	220 nF
$V_{DS,max}$	650 V	V_{max}	630 V
$Q_{g,typ}$	17 nC	Package	2220
Package	ThinPAK 8 × 8	230 in parallel	

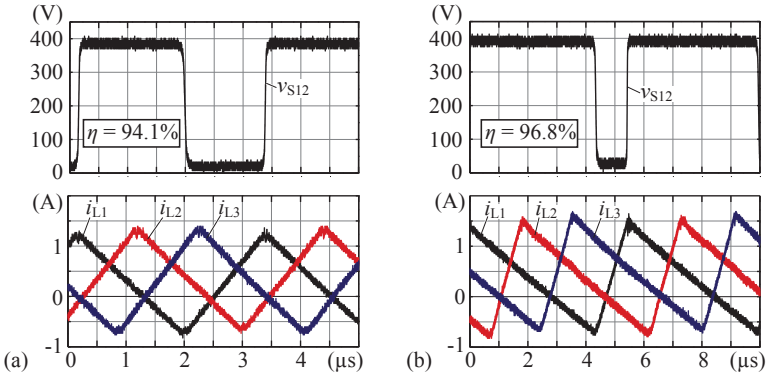


Fig. 3.22: Measurement results of converter system operating in Dc-Dc mode. (a) $v_n = 230\,V$, $V_{out} = 400\,V$, and $P_{out} = 200\,W$. (b) $v_n = 325\,V$, $V_{out} = 400\,V$, and $P_{out} = 400\,W$.

$P_{out} = 200\,W$. **Fig. 3.24** (a) presents the measurement result of the input voltage v_n and the input current i_n and **Fig. 3.24** (b) illustrates the measured efficiency η and power factor PF as a function of the load.

As mentioned in Section 3.4, the TCM converter suffers from core

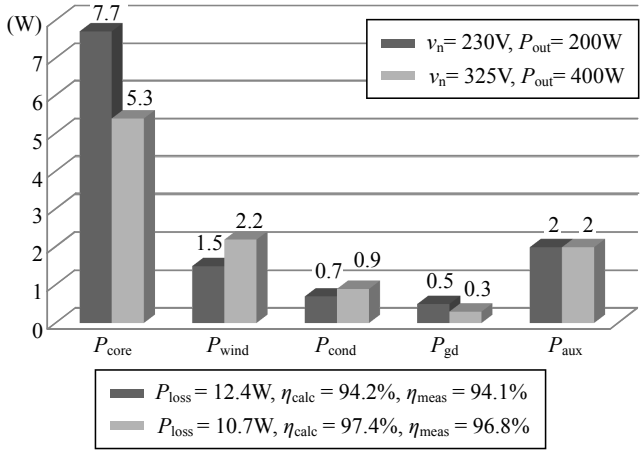


Fig. 3.23: Balance of losses for the TCM rectifier operated as DC-DC converter.

and winding losses due to applied modulation particularly at low load condiction. Multi-cell configurations can benefit at light load operation from cell shedding, cf. [68], and thus, for lower output power one or two cells are turned OFF. **Tab. 3.4** lists the cell shedding partitioning employed for the implemented prototype. A proper control which allows a smooth transition at a load change has not been implemented and is subject to further research but several methods are already presented [90, 91]. Nonetheless, the efficiency suffers due to the inherent core and winding losses. For a high power TCM rectifier with $P_{out} = 3.3\,\text{kW}$, as e.g. presented in [68], the efficiency is over 99 % over the entire load range at a power density of $1.1\,\text{kW/dm}^3$. There, the inductor losses caused by the TCM modulation have minor impact on the overall system performance.

Tab. 3.4: Cell shedding partitioning.

Load	N° of active cells
20 . . . 40 %	1
40 . . . 60 %	2
60 . . . 100 %	3

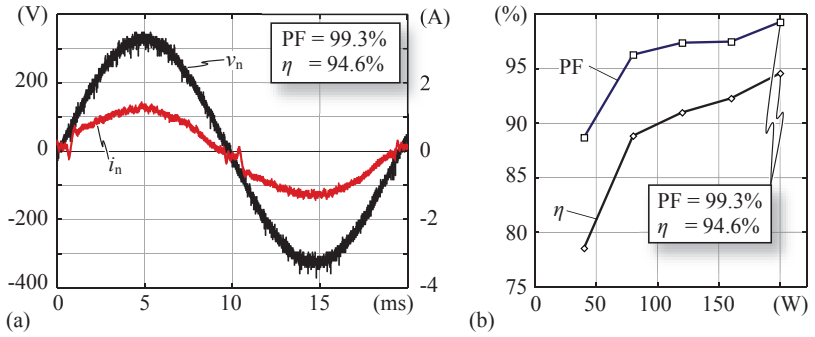


Fig. 3.24: (a) Measured input voltage v_n and input current i_n of the TCM PFC rectifier ($V_n = 230\,V$, $V_{out} = 400\,V$, $P_{out} = 200\,W$). (b) Measured efficiency η and power factor PF as a function of the output power P_{out}.

3.7 Conclusion

This chapter presents the analysis and the modeling of a single-phase multi-cell TCM PFC rectifier. Due to the tight converter requirements imposed by the low thickness of only 1 mm a modified multi-cell totem-pole PFC rectifier is considered to be most appropriate, since this topology enables low conduction losses and low switching losses.

It is shown that full-range ZVS can be achieved with a specific modulation technique entitled *Triangular Current Mode* (TCM). However, the nonlinear output capacitances of the MOSFETs need to be considered because of the strong impact on the inductor current waveform and on the timing parameters. Therefore, a simplified capacitance model is proposed which facilitates the derivation of closed-form expressions and yields accurate timing values.

Based on the analytical converter model an optimization procedure is presented with regard to the efficiency and/or the area-related power density. It is shown that the core losses determine the performance of the converter as they account for almost 80 % of the overall losses.

The chapter further discusses the implemented control structure and in particular the interleaving control of the inductor currents is detailed. All theoretical considerations are validated by measurements on a prototype of a 200 W 3-cell TCM PFC rectifier. The realized PFC rectifier

achieves an efficiency of $\eta = 94.6\,\%$ and a power factor of $\mathrm{PF} = 99.3\,\%$ at a footprint size of $221\,\mathrm{mm} \times 157\,\mathrm{mm}$ and a thickness of $h = 5\,\mathrm{mm}$.

The presented design procedure indicates that the realization of a $1\,\mathrm{mm}$ thin 3-cell TCM PFC rectifier with a calculated efficiency of $\eta = 94\,\%$ would require a footprint size of $A = 385\,\mathrm{cm}^2$, i.e. a square PCB with a length of approximately $20\,\mathrm{cm}$.

4

Flyback-type PFC Rectifier

PFC rectifier systems are typically realized either as a two-stage architecture or a single-stage topology, cf. Chapter 2. Contrary to a two-stage topology, a single-stage topology offers the benefit of requiring only a single magnetic component to achieve the PFC functionality and to feature the galvanic isolation. Besides, the energy storage capacitors needed to smooth the inherent power variation of a single-phase system can be implemented at the low voltage output of the converter and conventional ceramic capacitor chips with reasonable area requirement can be employed.

Section 4.1 discusses two promising candidate topologies for the ultra-flat PFC rectifier, a flyback converter and a Dual Active Bridge converter. Based on this discussion, the flyback-type PFC rectifier with active snubber is considered to be most appropriate with respect to the given specifications.

Section 4.2 details the operation of a flyback converter and shows the impact of the flyback transformer's leakage inductance on the converter efficiency and the voltage stress applied to the power switch. In order to limit the voltage spikes over the power switch a snubber circuit has to be employed. Thus, passive and active snubber circuits for flyback converters are discussed. Due to the inherently large leakage inductance of PCB-integrated transformers an active snubber is considered in order to avoid excessive losses in the snubber circuit.

Section 4.3 explains the modulation scheme employed for a flyback converter with active snubber. With regard to the modulation scheme and the specifications, Section 4.4 gives a step-by-step design procedure for the considered flyback-type PFC rectifier. The flyback transformer of the converter determines the power density and the efficiency to a

large extend. The design procedure presented in Section 5.3 has been applied to determine the optimal flyback transformer with respect to efficiency and/or a small footprint size. Section 4.5 presents the analysis of a small-signal model and the design of the control structure. Finally, Section 4.6 discusses the measurement results of the realized converter system.

4.1 Topology comparison

For many years, single-stage AC-DC converters have been investigated because of the potential benefits concerning the power density and the costs particularly for low power PFC rectifiers [73, 92, 93]. In the presented topologies, the second conversion stage is traded against a more complex circuitry and control structure. Beside the HF transformer, the topologies usually require an additional magnetic component which is not desirable with respect to the PCB-integration.

Two promising topologies which offer the benefit of a single-stage energy convertion while maintaining the circuit complexity comparably low are the flyback converter and the Dual Active Bridge converter. A comparison between the these two architectures which are depicted in **Fig. 4.1** is given in the following in order to find the most suitable topology to implement an ultra-flat PFC rectifier.

4.1.1 Flyback converter

The flyback converter depicted in **Fig. 4.1** (a) applies the voltage v_{n1} to the transformer during the turn-ON time, $d\,T_{\mathrm{P}}$, of the semiconductor switch S_1, which increases the magnetic energy stored in the transformer (two-winding inductor) core. During the turn-OFF time of S_1 the transformer's magnetizing inductance transfers the stored magnetic energy to the output. The flyback converter can be operated with continuous magnetic flux (Continuous Conduction Mode, CCM) or discontinuous magnetic flux (Discontinuous Conduction Mode, DCM). **Fig. 4.2** depicts typical waveforms of the transformer voltages and the magnetizing current for converter operation in CCM and DCM.

CCM operation:

Two different converter states occur for CCM operation, cf. **Fig. 4.2** (a):

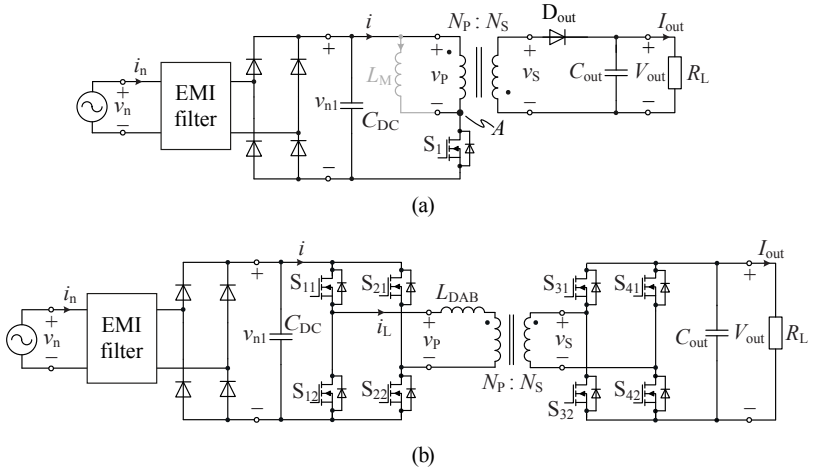


Fig. 4.1: Converter topologies initially considered for a single-phase PFC rectifier: (a) flyback converter (the magnetizing inductance L_M is integrated in the HF transformer and is therefore depicted in gray), (b) Dual Active Bridge (DAB) converter.

- *State I*; S_1 is turned ON and D_out blocks: the input voltage is applied to the primary side winding of the transformer, $v_\mathrm{P} = v_\mathrm{n1}$, and the current i_M in the transformer magnetizing inductance increases linearly.

- *State II*; S_1 is turned OFF and D_out conducts: the output voltage is applied to the secondary side winding of the transformer, $v_\mathrm{S} = V_\mathrm{out}$, and the current i_M in the transformer magnetizing inductance decreases linearly.

During steady state operation and for the assumption of constant voltages v_n1 and V_out during one switching period, the duty cycle d and the peak-to-peak variation of the magnetizing current, ΔI_M, are

$$d = \frac{n\,V_\mathrm{out}}{v_\mathrm{n1} + n\,V_\mathrm{out}}, \tag{4.1}$$

$$\Delta I_\mathrm{M} = \frac{(1-d)\cdot n\,V_\mathrm{out}}{f_\mathrm{S} L_\mathrm{M}}, \tag{4.2}$$

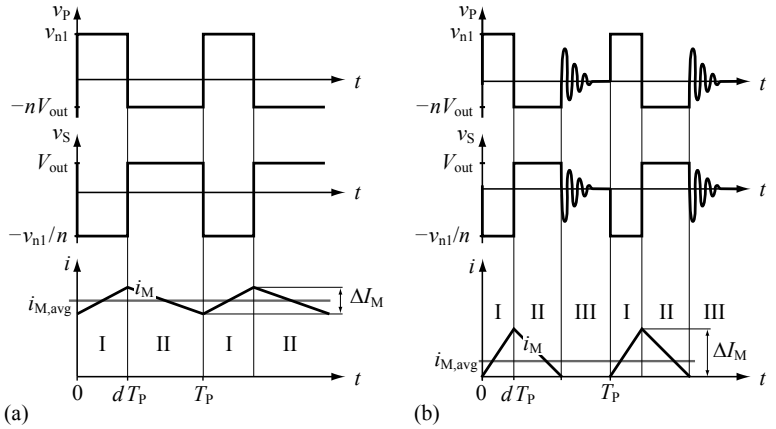


Fig. 4.2: Drawings of typical waveforms of the transformer voltages, v_P and v_S, and the magnetizing current, i_M; (a) CCM operation and (b) DCM operation. For DCM operation, the transformer voltages v_P and v_S show a ringing at the start of state III, since the potential at node A in **Fig. 4.1** is not defined, i.e. neither S_1 nor D_{out} conducts.

with

$$n = \frac{N_P}{N_S}. \tag{4.3}$$

The average output current $\bar{I}_{out} \approx I_{out}$ defines the output power $P_{out} \approx V_{out} \cdot I_{out}$ (provided that the variation of the voltage applied to C_{out} can be neglected, i.e. $V_{out} \approx$ constant). According to (4.1) the (stationary) duty cycle d is only determined by the input and output voltage; selecting a duty cycle different from (4.1) changes the current level and accordingly the power flow. This allows to sinusoidally shape the input current and/or select the current amplitude according to the load power demand.

DCM operation:

For DCM operation, three different converter states occur, cf. **Fig. 4.2** (b):

- *State I*; S_1 is turned ON and D_{out} blocks: the input voltage is applied to the primary winding of the transformer, $v_P = v_{n1}$,

and the current i_{M} in the transformer magnetizing inductance increases.

- *State II*; S_1 is turned OFF and D_{out} conducts: the output voltage is applied to the secondary side winding of the transformer, $v_{\mathrm{S}} = V_{\mathrm{out}}$, and the current i_{M} in the transformer magnetizing inductance decreases.
- *State III*; $i_{\mathrm{M}} = 0$, S_1 is turned OFF, and D_{out} blocks: this state typically starts with a ringing on v_{P} and v_{S}, since the potential in node A in **Fig. 4.1** is not defined during State III.

During steady-state operation and for the assumption of constant voltages v_{n1} and V_{out} during one switching period, the duty cycle d and the peak-to-peak variation of the magnetizing current, ΔI_{M}, are

$$d = \sqrt{\frac{2 f_{\mathrm{S}} L_{\mathrm{M}} \cdot P_{\mathrm{out}}}{v_{\mathrm{n1}}^2}}, \tag{4.4}$$

$$\Delta I_{\mathrm{M}} = \sqrt{\frac{2 P_{\mathrm{out}}}{f_{\mathrm{S}} L_{\mathrm{M}}}}. \tag{4.5}$$

The maximum power achieveable with DCM operation for a local input voltage level v_{n1} is

$$P_{\mathrm{max,DCM}} = \frac{(v_{\mathrm{n1}} \cdot n\, V_{\mathrm{out}})^2}{2\, f_{\mathrm{S}}\, L_{\mathrm{M}} \cdot (v_{\mathrm{n1}} + n\, V_{\mathrm{out}})^2}. \tag{4.6}$$

4.1.2 Dual Active Bridge (DAB) converter

The DAB converter consists of two voltage-sourced full bridge circuits, which are connected to the inductor L_{DAB} and the transformer, according to **Fig. 4.3** (a). The converter model most often used to investigate the DAB, e.g. in [94, 95], is shown in **Fig. 4.3** (b); it assumes:

- negligible converter losses,
- negligible magnetizing current,
- negligible parasitic capacitances of the transformer, e.g. no coupling capacitance between primary and secondary sides,
- all quantities referred to the primary side,

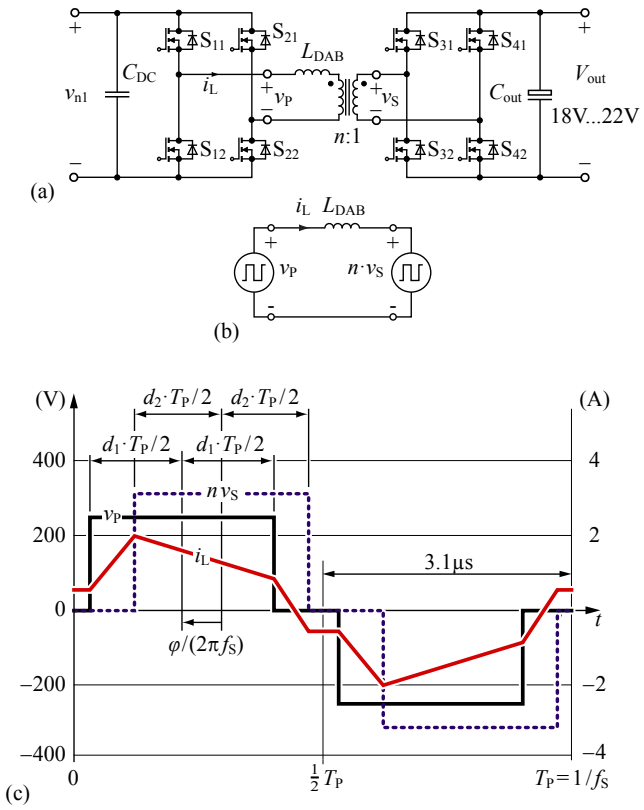


Fig. 4.3: (a) DAB converter topology ($v_{n1} = 0...325\,\text{V} \pm 10\,\%$); (b) employed electrical model of the DAB converter; (c) general waveforms of v_P, v_S, and i_L used to define d_1, d_2, and φ; the waveforms are calculated for $V_1 = 250\,\text{V}$, $V_2 = 20\,\text{V}$, $d_1 = 0.37$, $d_2 = 0.35$, $\varphi = 0.5\,\text{rad}$, $L = 97\,\mu\text{H}$, and $n = 15.7$.

- constant supply voltages v_{n1} and V_{out}.

The DAB output power is adjusted by varying one or more of the four control parameters shown in **Fig. 4.3** (c) and listed below.[1]

[1] The duty cycles are defined as the durations of the positive active time intervals divided by T_P, e.g. if T_1 is the duration of the time interval with $v_P(t)$ being equal to $+v_{n1}$ then $d_1 = T_1/T_P$. The phase shift, φ, is measured between the center points

- The phase shift φ between $v_{\mathrm{P}}(t)$ and $v_{\mathrm{S}}(t)$: $-\pi < \varphi < \pi$,
- the duty cycle d_1 of $v_{\mathrm{P}}(t)$ with $0 < d_1 < 0.5$,
- the duty cycle d_2 of $v_{\mathrm{S}}(t)$ with $0 < d_2 < 0.5$, and
- the switching frequency f_{S}.

The modulation scheme used to determine the RMS currents listed in **Tab. 4.1** employs all four control parameters in order to achieve increased converter efficiency [96, 97]:

- the duty cycles, d_1 and d_2, are calculated with respect to minimum transformer RMS currents [82];
- increased switching frequencies are used at low power levels, according to [96], in order to achieve a reduction of the transformer RMS currents; the maximum switching frequency is limited to 320 kHz;
- the phase angle, φ, is calculated with respect to the required output power.

The transformer turns ratio, n, and the converter inductance, L_{DAB}, are calculated with respect to minimum peak magnetic energy stored in L_{DAB}. Details on the DAB converter are given in [82, 98, 99].

4.1.3 Comparison of flyback converter and DAB converter

Both power converters, the flyback converter and the DAB converter, allow for an operation with low switching losses [98, 100] and therefore, the use of a high switching frequency is feasible. Apart from that, however, the two power converter topologies are entirely different and thus feature different advantages. The flyback converter is particularly advantageous with respect to the simple circuit structure, the single low side switch needed, and a simple converter control strategy. This converter, however, generates high RMS currents in the transformer and the rectifier diode $\mathrm{D_{out}}$. Furthermore, a snubber circuit, which absorbs

of the positive active time intervals of v_{P} and v_{S}. It can be shown that the sign of φ determines the power transfer direction with this definition; e.g. $\varphi > 0$ causes a power transfer from the primary to the secondary side.

Tab. 4.1: Benchmark values calculated for the flyback and the DAB converter: transformer currents, magnetic energies stored in L_{M} and L_{DAB}, and semiconductor currents and voltages.

	Flyback converter	**DAB converter**
Assumptions:		
Switching frequency:	$160\,\mathrm{kHz} \leq f_{\mathrm{S}} \leq 320\,\mathrm{kHz}$	$160\,\mathrm{kHz} \leq f_{\mathrm{S}} \leq 320\,\mathrm{kHz}$
Input voltage range:	$0 \leq v_{\mathrm{n1}} \leq 325\,\mathrm{V} \pm 10\,\%$	$0 \leq v_{\mathrm{n1}} \leq 325\,\mathrm{V} \pm 10\,\%$
Output voltage:	$V_{\mathrm{out}} = 20\,\mathrm{V} \pm 10\,\%$	$V_{\mathrm{out}} = 20\,\mathrm{V} \pm 10\,\%$
Transformer:		
Turns ratio, n:	13	15.7
RMS current, primary side:	1.84 A	1.41 A
RMS current, secondary side:	24.1 A	22.1 A
Inductor:		
Inductance:	$L_{\mathrm{M}} = 130\,\mu\mathrm{H}$	$L_{\mathrm{DAB}} = 97\,\mu\mathrm{H}$
Peak inductor current:	6.9 A	2.1 A
Peak stored magnetic energy:	3 mJ	210 µJ
Semiconductors:		
Peak switch voltages	S_1: 780 V	S_{11}, S_{12}, S_{21}, S_{22}: 360 V S_{31}, S_{32}, S_{41}, S_{42}: 20 V
Switch RMS currents	S_1: 1.84 A	S_{11}, S_{12}, S_{21}, S_{22}: 1.00 A S_{31}, S_{32}, S_{41}, S_{42}: 15.7 A
Peak diode blocking voltage:	D_{out}: 60 V	—
Average diode current	D_{out}: 12.5 A	—
Diode RMS current	D_{out}: 24.1 A	—

the magnetic energy stored in the leakage inductance of the transformer, is required in order to avoid overvoltage spikes between the drain and source connections of the semiconductor switch S_1; passive and active

snubber realizations are detailed in Section 4.2.2.
In comparison, the DAB converter achieves a reduction of the transformer RMS currents and avoids the need for additional snubber circuitry since v_{n1} and V_{out} limit the drain to source voltages of all semiconductor switches. The DAB converter, however, requires eight semiconductor switches, four high side gate drivers, and a complex modulation scheme in order to achieve high converter efficiency within the wide input voltage range [82].

Tab. 4.1 summarizes the different currents and voltages calculated for the two converter topologies. Based on this data the flyback converter is selected; the main reasons for this selection are listed below:

- The realization effort due to the simple circuit structure of the flyback converter is less than the effort needed to realize the DAB converter.
- The modulation scheme employed for the flyback converter is considerably simpler than that of the DAB.
- Technically reasonable peak and RMS current values are calculated for the semiconductors (S_1 and D_{out}, cf. **Tab. 4.1**) and the transformer windings, due to the comparably low specified output power of 200 W; e.g. the transformer RMS currents calculated for the flyback converter (primary: 1.84 A, secondary: 24.1 A) are only slightly higher than the currents calculated for the DAB converter (primary: 1.41 A, secondary: 22.1 A).

4.2 Basic operation of a flyback converter

The topology comparison performed in the previous section identifies the flyback-type PFC rectifier as the topology of choice for a PCB-integrated system. This section highlights the specific properties of flyback converters and focuses on the implications of the PCB-integrated components on the topology.

4.2.1 Operation mode

According to the explanations given in Section 4.1 the flyback converter can either operate in CCM or in DCM. With respect to the size of

the ultra-flat flyback transformer the question arises, whether CCM or DCM operation is more advantageous.

It can be shown, that the volume of an inductor L_M, Vol_L, is directly proportional to the stored energy E_M [84],

$$Vol_\mathrm{L} \propto E_\mathrm{M}. \tag{4.7}$$

Therefore, for both operation modes the stored energy in the flyback transformer has been calculated for a given operating point ($v_{\mathrm{n1}} = 325\,\mathrm{V}$, $V_\mathrm{out} = 20\,\mathrm{V}$, $n = 13$, $P_\mathrm{out} = 200\,\mathrm{W}$, and $f_\mathrm{S} = 160\,\mathrm{kHz}$). Referring to **Fig. 4.1** (a) and assuming an ideal converter, the output power P_out and the input voltage v_{n1} define the required average input current,

$$\bar{i} = P_\mathrm{out}/v_{\mathrm{n1}} = 615\,\mathrm{mA}. \tag{4.8}$$

For CCM, cf. **Fig. 4.4** (a), the average magnetizing current is

$$\bar{i}_\mathrm{M} = \bar{i}/d = 1.38\,\mathrm{A}, \tag{4.9}$$

whereas the duty cycle d is calculated according to (4.1). The ripple current in the flyback transformer is

$$\Delta i_\mathrm{M} = \frac{v_{\mathrm{n1}} \cdot d\,T_\mathrm{P}}{L_\mathrm{M}}, \tag{4.10}$$

and, with it, the RMS value of the magnetizing current, $i_{\mathrm{M,rms}}$, as well as the peak current $\hat{I}_\mathrm{M}$ can easily be calculated as

$$\hat{I}_\mathrm{M} = \bar{i}_\mathrm{M} + \frac{1}{2}\Delta i_\mathrm{M}, \qquad i_{\mathrm{M,rms}} = \bar{i}_\mathrm{M} \cdot \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_\mathrm{M}}{2 \cdot \bar{i}_\mathrm{M}}\right)^2}. \tag{4.11}$$

For DCM operation, cf. **Fig. 4.4** (b), the duty cycle d_1 has to be adjusted to transmit the desired power to the output and it can be derived with

$$\bar{i} = \frac{1}{2}\,d_1 \cdot \hat{I}_\mathrm{M} = \frac{1}{2}\,d_1 \cdot \frac{v_{\mathrm{n1}} \cdot d_1\,T_\mathrm{P}}{L_\mathrm{M}}, \tag{4.12}$$

which yields

$$d_1 = \sqrt{\frac{2\,f_\mathrm{S} \cdot L_\mathrm{M} \cdot P_\mathrm{out}}{v_{\mathrm{n1}}^2}}. \tag{4.13}$$

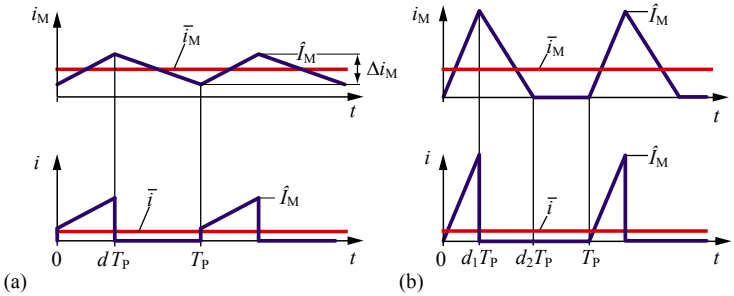


Fig. 4.4: Current waveforms of a flyback transformer, cf. **Fig. 4.1** (a), considered to compare the flyback transformer characteristics for CCM (a) and DCM (b).

The peak magnetizing current $\hat{I}_M$ and the RMS value of the magnetizing current, $i_{M,rms}$, are determined with

$$\hat{I}_M = \frac{v_{n1} \cdot d_1\, T_P}{L_M}, \qquad i_{M,rms} = \hat{I}_M \cdot \sqrt{\frac{d_1 + d_2}{3}}, \tag{4.14}$$

whereas d_2 is defined with

$$d_2 = \frac{L_M \cdot \hat{I}_M}{n\, V_{out}}. \tag{4.15}$$

Considering (4.13), the boundary between CCM and DCM can be calculated with

$$\frac{v_{n1} d_1}{L_M} = \frac{n\, V_{out}(1 - d_1)}{L_M}, \tag{4.16}$$

which yields a magnetizing inductance of $L_M = 326\,\mu H$ for the considered operating point. The maximum value of the energy stored in the flyback inductor is calculated with respect to the corresponding peak current $\hat{I}_M$,

$$E_M = \frac{1}{2}\, L_M \cdot \hat{I}_M^2. \tag{4.17}$$

Fig. 4.5 (a) depicts the stored magnetic energy E_M as a function of L_M, for the given operating point. As can be seen, the peak energy in the transformer is constant for DCM operation; in CCM the stored energy increases which results in a larger required volume. The small

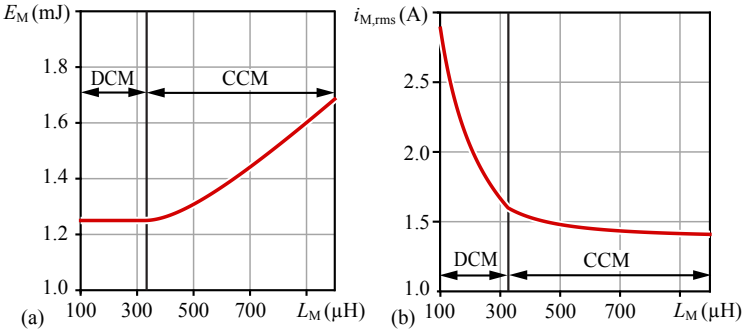


Fig. 4.5: (a) Energy, E_M, stored in L_M as a function of the inductance value. (b) RMS value of the magnetizing current, $i_{M,rms}$, plotted as a function of L_M. Parameters: $v_{n1} = 325\,V$, $V_{out} = 20\,V$, $n = 13$, $P_{out} = 200\,W$, and $f_S = 160\,kHz$.

volume for DCM operation, however, comes at cost of higher RMS currents, cf. **Fig. 4.5** (b). A trade-off between minimum E_M and acceptable RMS current $i_{M,rms}$ is obtained for the operation between DCM and CCM, the so-called Boundary Conduction Mode (BCM). Therefore, the flyback converter is designed for boundary mode operation.

The BCM operation of the converter implies a variable switching frequency. The switching frequency range of the converter is limited to values between

$$f_{min} = 160\,kHz \quad \text{and} \quad f_{max} = 320\,kHz, \tag{4.18}$$

as this frequency range results in a good compromise between core losses and inductance value L_M [101, 102].

4.2.2 PCB-integrated flyback transformer

The flyback transformer is the most important component of a flyback converter as it determines the operation mode, the efficiency, the power density, and the additional snubber circuitry for recovering the leakage energy. Thus, a proper transformer design is crucial, particularly if the PCB-integration of core and windings is considered [103].

Leakage inductance of a flyback transformer

The basic principles for PCB-integrated magnetics suitable to realize a single-phase AC-DC converter are presented in Chapter 5 and it is shown that the PCB-integration of the core and the windings being realized as tracks and vias allow to comply with the specified height limitation and results in a high energy density. Due to the PCB-integration of the core, however, the PCB thickness determines the core's height. The core cross-sectional area A_e is calculated with

$$A_\mathrm{e} = d_\mathrm{core} \cdot b_\mathrm{core} \cdot k_\mathrm{fe}, \tag{4.19}$$

where d_core is the thickness, b_core is the width of the core, and k_fe is the core filling factor. Eq. (4.19) shows that with a limited core thickness d_core a required A_e can only be obtained by increasing the core width b_core. Thus, a large required A_e leads to a large footprint size of the transformer. In order to achieve a required inductance value, the number of turns N and/or the core cross-section A_e can be adjusted:

$$L \propto N^2 \frac{A_\mathrm{e}}{l_\mathrm{m}}. \tag{4.20}$$

However, since the turns are realized using vias in the winding window of the core, cf. **Fig. 4.6**, an increased N automatically results in a larger winding window and thus a larger footprint area, too.

The realization of a PCB-integrated flyback transformer for the full rated output power of 200 W, cf. Section 1.2, would result in large area requirements for core and windings. This implies not only considerable manufacturing effort but also that primary and secondary windings are spacially distributed over a large area and thus a comparably large leakage inductance of the transformer would have to be expected as the leakage flux is high due to the large distance between primary and secondary windings, cf. **Fig. 4.6**.

Although an interleaving of primary and secondary windings reduces the leakage inductance of a PCB-integrated transformer, cf. Section 5.2.6, the leakage coefficient[2] of the flyback transformer still is large compared to conventional transformers (conventional flyback transformers: $\sigma = 0.5 \ldots 5\,\%$, PCB-integrated flyback transformer: $\sigma = 10 \ldots 20\,\%$).

[2]The leakage coefficient of a transformer, σ, is defined by $\sigma = \frac{L_\sigma}{L_\sigma + L_\mathrm{M}}$, whereas L_σ is the leakage inductance and L_M represents the magnetizing inductance.

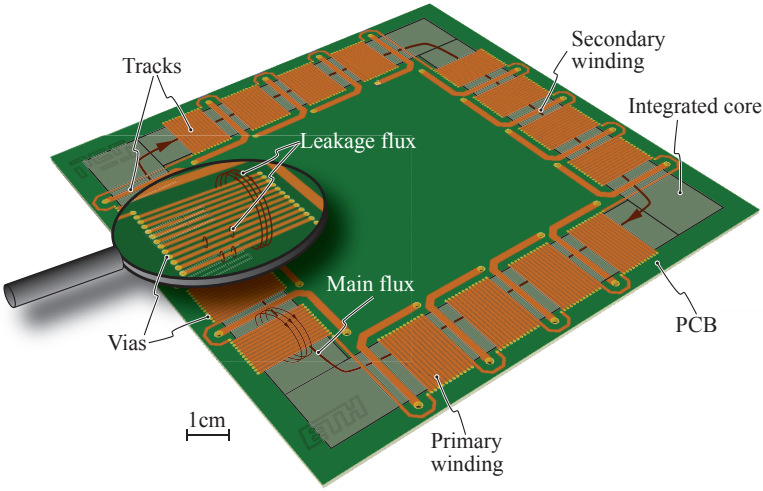


Fig. 4.6: Illustration of a PCB-integrated flyback transformer. In order to maximize the magnetic coupling an interleaving of primary and secondary windings is applied. Nevertheless, the amount of leakage flux is still larger than for cuboid transformer shapes due to the large spacial distances between the windings.

Reasonable values of the leakage inductance can be obtained if smaller transformers are employed which enable a more compact setup and a reduced leakage flux. Therefore, a multi-cell architecture according to **Fig. 2.3** (b) is applied, which divides the output power to several small subsystems - each consisting of a flyback cell. Besides, a multi-cell converter allows for a distribution of losses, cf. Section 2.1; thus, the excellent heat removal capabilities of ultra-flat systems can be utilized.

Impact of the leakage inductance on a flyback converter

One aspiration in the design of a transformer is to achieve a tight magnetic coupling between primary and secondary windings. In real transformers, however, perfect coupling cannot be achieved and each winding excites a certain amount of leakage flux. The equivalent circuit of an ideally coupled transformer is therefore extended with a series connected leakage inductance L_σ, indicated in **Fig. 4.7** (a).

In a flyback converter operating in BCM or DCM, the magnetizing current declines to zero in each switching interval and, assuming ideal coupling, all energy is transferred from the primary to the secondary winding. However, due to non-ideal magnetic coupling, a certain amount of energy is stored in the leakage inductance which has to be removed every switching cycle.

Fig. 4.7 (a) presents a basic flyback cell where the leakage inductance L_σ is included in the transformer model. In order to explain the current commutation from the primary side to the secondary side the equivalent circuit shown in **Fig. 4.7** (b) is used; there the secondary side is referred to the primary side.

At the beginning of every switching interval the primary current i_P increases from 0 A according to

$$i_\mathrm{P}(t) = \frac{v_\mathrm{n1}}{L_\sigma + L_\mathrm{M}} \cdot t. \tag{4.21}$$

S_1 is turned OFF at $t = dT_\mathrm{P}$ when $i_\mathrm{P}(dT_\mathrm{P}) = \hat{I}_\mathrm{P}$. The current commutation from primary to secondary side requires i_P to decrease to zero. Therefore, a voltage v_σ must be applied to the leakage inductance L_σ as indicated in **Fig. 4.7** (b). v_σ increases the voltage stress over S_1 as depicted in **Fig. 4.7** (c). Furthermore, the overlapping of drain current and drain-source voltage in S_1 during the commutation time t_σ results in switching losses.

Passive snubber circuit

In order to avoid high switching losses and excessive voltage stress over S_1, a snubber circuit has to be considered which bypasses $i_\mathrm{P}(t)$ as soon as $v_\mathrm{S1}(t) = \hat{V}_\mathrm{S1}$. **Fig. 4.8** depicts a widely used snubber circuit consisting of a resistor, a capacitor, and a diode (RCD-snubber). After turn-OFF of S_1, when $v_\mathrm{S1}(t)$ exceeds the sum of v_n1 and the snubber voltage v_Sn, the diode D_Sn becomes forward biased and $i_\mathrm{P}(t)$ flows through the snubber capacitor C_Sn. Thus, $v_\mathrm{S1}(t)$ is clamped to $\hat{V}_\mathrm{S1} = v_\mathrm{n1} + v_\mathrm{Sn}$; this limits the voltage stress over S_1 and shifts the losses caused by the leakage inductance from the power switch to the snubber circuit; the occuring losses can be calculated as follows.

Considering a linear change of i_P ($\mathrm{d}i_\mathrm{P}/\mathrm{d}t = \text{const.}$) during the commutation interval t_σ, the slope of i_P can be evaluated with

$$\frac{\mathrm{d}i_\mathrm{P}}{\mathrm{d}t} = \frac{\hat{I}_\mathrm{P}}{t_\sigma} = \frac{-v_\sigma}{L_\sigma} = \frac{\hat{V}_\mathrm{S1} - (V_\mathrm{out}^{'} + v_\mathrm{n1})}{L_\sigma}, \tag{4.22}$$

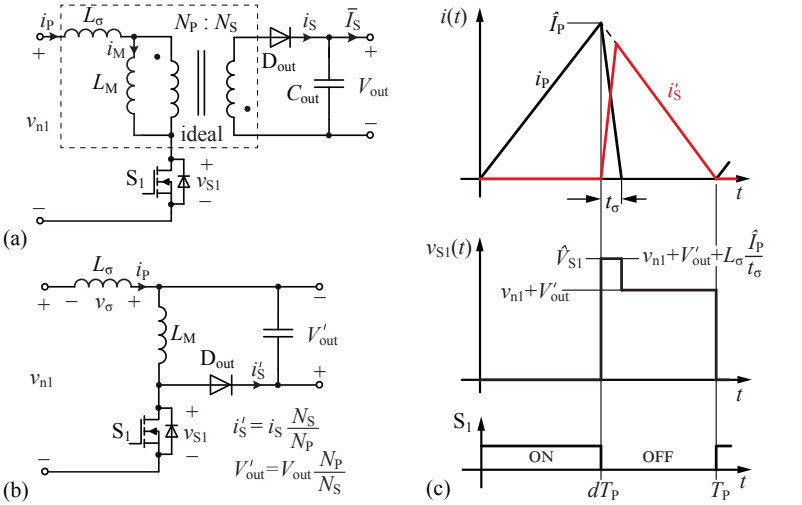


Fig. 4.7: (a) Flyback cell with a non-ideal transformer model which includes the leakage inductance L_σ. (b) Simplified equivalent circuit (primary side referred). (c) Current commutation and voltage over the switch S_1 for boundary conduction mode.

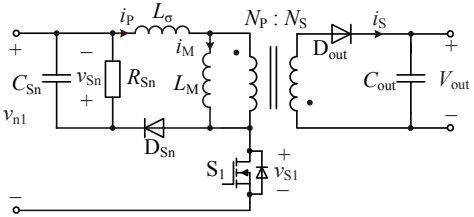


Fig. 4.8: Realization of a passive snubber used to absorb the energy stored in the leakage inductance of the flyback transformer.

where $V_{\text{out}}^{'}$ is the output voltage transformed to the primary side, cf. **Fig. 4.7**. The snubber voltage v_{Sn} and the current flowing into C_{Sn} determine the energy transferred to the snubber circuit, E_σ:

$$E_\sigma = \frac{1}{2}\hat{I}_{\text{P}} \cdot t_\sigma \cdot v_{\text{Sn}} = \frac{1}{2} L_\sigma \hat{I}_{\text{P}}^2 \cdot \frac{\hat{V}_{\text{S1}} - v_{\text{n1}}}{\hat{V}_{\text{S1}} - (V_{\text{out}}^{'} + v_{\text{n1}})}, \tag{4.23}$$

whereas (4.22) and $v_{\mathrm{Sn}} = \hat{V}_{\mathrm{S1}} - v_{\mathrm{n1}}$ are substituted.

In order to show the impact of the leakage energy loss on the converter efficiency, the loss energy has to be split up into loss contributions $P_{\mathrm{loss},i}$,

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{P_{\mathrm{in}} - \sum_i P_{\mathrm{loss},i}}{P_{\mathrm{in}}} = 1 - \sum_i \frac{P_{\mathrm{loss},i}}{P_{\mathrm{in}}} = 1 - \Delta\eta. \tag{4.24}$$

Thus, the efficiency drop $\Delta\eta_\sigma$ due to the energy in the leakage inductance, E_σ, is [104]

$$\begin{aligned} \Delta\eta_\sigma &= \frac{P_\sigma}{P_{\mathrm{in}}} = \frac{E_\sigma}{E_{\mathrm{in}}} = \\ &= \frac{1}{2} L_\sigma \hat{I}_{\mathrm{P}}^2 \cdot \frac{\hat{V}_{\mathrm{S1}} - v_{\mathrm{n1}}}{\hat{V}_{\mathrm{S1}} - (V'_{\mathrm{out}} + v_{\mathrm{n1}})} \cdot \frac{1}{\frac{1}{2}(L_{\mathrm{M}} + L_\sigma)\,\hat{I}_{\mathrm{P}}^2} = \\ &= \frac{L_\sigma}{L_\sigma + L_{\mathrm{M}}} \cdot \frac{1 - \frac{v_{\mathrm{n1}}}{\hat{V}_{\mathrm{S1}}}}{1 - \frac{V'_{\mathrm{out}} + v_{\mathrm{n1}}}{\hat{V}_{\mathrm{S1}}}}. \end{aligned} \tag{4.25}$$

Eq. (4.25) shows that the minimal efficiency drop $\Delta\eta_\sigma$ would be obtained if an infinitely high voltage stress over S_1 could be tolerated; in this case it would be

$$\Delta\eta_\sigma = \frac{L_\sigma}{L_\sigma + L_{\mathrm{M}}}, \tag{4.26}$$

which is the definition of the leakage coefficient $\sigma = \frac{L_\sigma}{L_\sigma + L_{\mathrm{M}}}$. As a consequence, a flyback converter with a transformer which has a leakage coefficient of $\sigma = 3\,\%$ would suffer from an efficiency drop of at least $3\,\%$ if a passive snubber circuit would be employed.

For PCB-integrated flyback transformers leakage coefficients of over $10\,\%$ have to be expected due to the spacial distances between primary and secondary winding, cf. **Fig. 4.6**; a passive snubber can therefore not be applied but an active snubber must be considered.

Active snubber circuit

In order to recycle the energy stored in the leakage inductance L_σ and to minimize the turn-OFF voltage stress over the power switch S_1, active snubbers are widely used [105–108]. **Fig. 4.9** depicts a realization of an

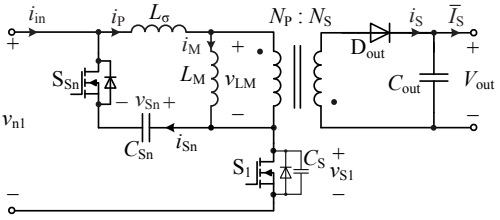


Fig. 4.9: Realization of an active snubber circuit which enables the recycling of the energy stored in the leakage inductance.

active snubber consisting of a snubber capacitor C_{Sn} and a snubber switch S_{Sn}.

Besides providing the recycling of the leakage energy and limiting the voltage stress over S_1, active snubber circuits enable zero-voltage switching (ZVS) for the power switch S_1 as the primary current i_P can be negative with respect to the magnetizing current i_M. This negative i_P can be used to discharge the parasitic capacitance of S_1 and thus enables ZVS [109].

In the following section, a thorough discussion on the switching intervals of a flyback converter employing an active snubber is given.

4.3 Operation of a flyback converter with active snubber

4.3.1 Continuous conduction mode

A switching period of a flyback converter with active snubber can be subdivided into six intervals [106]. **Fig. 4.10** shows the respective converter configuration for each interval whereas inactive components are marked in gray. The resulting voltage and current waveforms are presented in **Fig. 4.11**.

The output capacitances of the power switch S_1, the snubber switch S_{Sn}, and the output rectifier D_{out} are depicted in **Fig. 4.10** (a). In order to keep focus on the basic operation principle these capacitors are assumed to be linear. However, output capacitances of MOSFETs and diodes depend on the applied voltage. Furthermore, the impact of the parasitic capacitance C_D is neglected for the sake of simplicity [106,107].

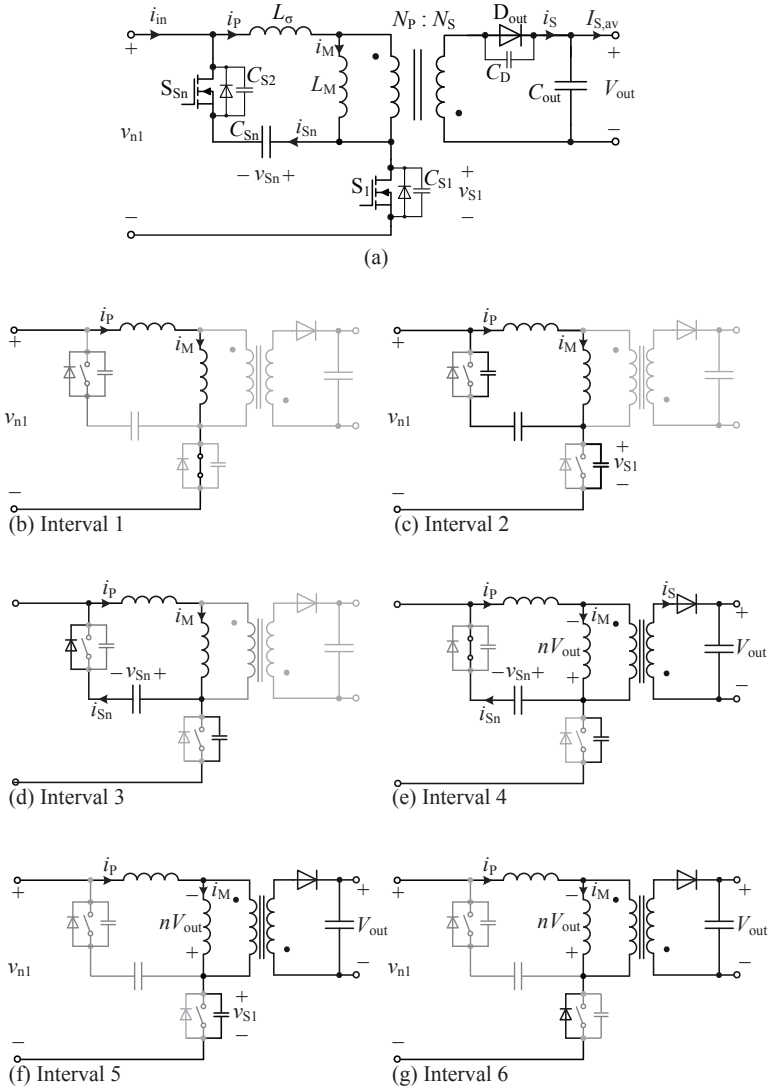


Fig. 4.10: Flyback converter stages illustrated for each interval.

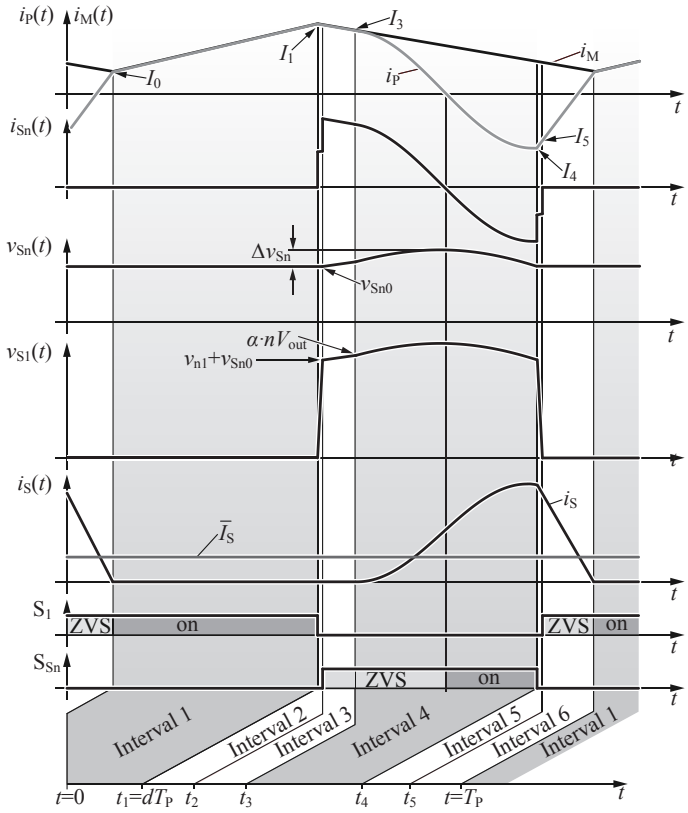


Fig. 4.11: Flyback converter waveforms operating in CCM for a switching period T_P.

Initial conditions: Considering steady-state conditions of the converter, the initial values of each state variable are constant, cf. **Fig. 4.11**:

$$i_P(t) = I_0 \qquad i_M(t) = I_0$$
$$v_{S1}(t) = 0 \qquad v_{Sn}(t) = v_{Sn0}.$$

In order to simplify the following equations the ratio between leakage

inductance and magnetizing inductance is introduced,

$$\beta = \frac{L_\sigma}{L_M}, \qquad \alpha = 1 + \beta. \tag{4.27}$$

Interval 1, cf. **Fig. 4.10** (b): At t_0 the output rectifier D_{out} stops conducting, the power switch S_1 is turned ON, and S_{Sn} is in OFF-state. i_P and i_M increase linearly according to

$$i_P(t) = i_M(t) = I_0 + \frac{v_{n1}}{L_M \cdot \alpha} \cdot t. \tag{4.28}$$

This interval ends when $t = t_1 = d\,T_P$ where d is the duty cycle of the power switch S_1.

Interval 2, cf. **Fig. 4.10** (c): At $t = t_1$, S_1 is turned OFF and $i_P(t) = i_M(t) = I_1$. The primary current charges C_{S1} and discharges C_{S2} which account for the output capacitances of S_1 and S_{Sn}, respectively; as the charging transition is very fast a linear voltage ramp can be assumed,

$$v_{S1}(t) = \frac{I_1}{C_{S1} + C_{S2}} \cdot (t - t_1). \tag{4.29}$$

Interval 3, cf. **Fig. 4.10** (d): When v_{S1} exceeds $v_{n1} + v_{Sn0}$ the body diode of S_{Sn} is forward biased and i_M commutates to the snubber circuit and the circuit composed of C_{Sn}, C_{S1}, L_M, and L_σ begins to resonate,

$$\begin{aligned} i_M(t) = i_P(t) &= A_1 \cdot \sin(\omega_1 \cdot (t - t_2) + \phi_1), \\ v_{Sn}(t) &= -A_1 Z_1 \cdot \cos(\omega_1 \cdot (t - t_2) + \phi_1), \end{aligned} \tag{4.30}$$

with

$$A_1 = \sqrt{I_1^2 + \left(\frac{v_{Sn0}}{Z_1}\right)^2}, \qquad \tan(\phi_1) = \frac{Z_1 \cdot I_1}{-v_{Sn0}}, \tag{4.31}$$

$$\omega_1 = \frac{1}{\sqrt{(C_{Sn} + C_{S1}) \cdot \alpha L_M}}, \qquad Z_1 = \sqrt{\frac{\alpha L_M}{C_{Sn} + C_{S1}}}. \tag{4.32}$$

Interval 3 ends when $v_{Sn} = nV_{out} \cdot \alpha$, where $n = N_P/N_S$ represents the turns ratio of the flyback transformer.

Interval 4, cf. **Fig. 4.10** (e): At $t = t_3$ the output rectifier D_{out} is forward biased and the output voltage V_{out} is clamped to the secondary winding. The magnetizing current i_M decreases linearly according to

$$i_{\mathrm{M}}(t) = I_3 - \frac{nV_{\mathrm{out}}}{L_{\mathrm{M}}} \cdot (t - t_3), \tag{4.33}$$

while the primary current i_{P} oscillates in the resonant tank composed of L_σ, C_{Sn}, and C_{S1},

$$\begin{aligned} i_{\mathrm{P}}(t) &= A_2 \cdot \sin(\omega_2 \cdot (t - t_3) + \phi_2), \\ v_{\mathrm{Sn}}(t) &= n\, V_{\mathrm{out}} - A_2 Z_2 \cdot \cos(\omega_2 \cdot (t - t_3) + \phi_2), \end{aligned} \tag{4.34}$$

with

$$A_2 = \sqrt{I_3^2 + \left(\frac{n\, V_{\mathrm{out}} \cdot \beta}{Z_2}\right)^2}, \qquad \tan(\phi_2) = \frac{Z_2 \cdot I_3}{-n\, V_{\mathrm{out}} \cdot \beta} \tag{4.35}$$

$$\omega_2 = \frac{1}{\sqrt{(C_{\mathrm{Sn}} + C_{\mathrm{S1}}) \cdot L_\sigma}}, \qquad Z_2 = \sqrt{\frac{L_\sigma}{C_{\mathrm{Sn}} + C_{\mathrm{S1}}}}. \tag{4.36}$$

During this interval i_{P} becomes negative and, in order to achieve ZVS, $\mathrm{S_{Sn}}$ has to be turned ON before this zero crossing. In **Fig. 4.11** the ZVS time range of $\mathrm{S_{Sn}}$ is indicated which coincides with the conduction time of its body diode. However, it is beneficial to turn ON $\mathrm{S_{Sn}}$ as early as possible because conduction losses in the switch can be reduced.

The secondary current i_{S} is determined by

$$i_{\mathrm{S}}(t) = n \cdot (i_{\mathrm{M}}(t) - i_{\mathrm{P}}(t))\,. \tag{4.37}$$

Interval 5, cf. **Fig. 4.10** (f): $\mathrm{S_{Sn}}$ turns OFF at $t = t_4$ and L_σ resonates with $C_{\mathrm{S1}} + C_{\mathrm{S2}}$. The amount of energy stored in the leakage inductance L_σ and the energies required to fully discharge C_{S1} and charge C_{S2} determine if ZVS of $\mathrm{S_1}$ can be achieved: Thus, if

$$E_\sigma \geq E_{\mathrm{C_{S1}}} + E_{\mathrm{C_{S2}}}|_{\mathrm{t=t_4}}, \tag{4.38}$$

C_{S1} is discharged and C_{S2} is charged and the current commutates to the body diode of $\mathrm{S_1}$ and ZVS can be achieved. The current and voltage waveforms in interval 5 are

$$\begin{aligned} i_{\mathrm{P}}(t) &= A_3 \cdot \sin(\omega_3 (t - t_4) + \phi_3), \\ v_{\mathrm{Sn}}(t) &= v_{\mathrm{n1}} + n\, V_{\mathrm{out}} - A_3 Z_3 \cdot \cos(\omega_3 (t - t_4) + \phi_3), \end{aligned} \tag{4.39}$$

with

$$A_3 = \sqrt{I_4^2 + \left(\frac{n\,V_{\text{out}} - v_{\text{Sn0}}}{Z_3}\right)^2}, \quad \tan(\phi_3) = \frac{Z_3 \cdot I_4}{-(n\,V_{\text{out}} - v_{\text{Sn0}})} \tag{4.40}$$

$$\omega_3 = \frac{1}{\sqrt{L_\sigma \cdot (C_{\text{S1}} + C_{\text{S2}})}}, \qquad Z_3 = \sqrt{\frac{L_\sigma}{C_{\text{S1}} + C_{\text{S2}}}}. \tag{4.41}$$

The magnetizing current $i_{\text{M}}(t)$ keeps decreasing linearly and (4.33) is still valid.

If ZVS can be achieved, the current i_{P} commutates to the body diode of S_1 which is the beginning of interval 6. However, if ZVS cannot be obtained, S_1 has to be turned ON while there is still charge in the output capacitance C_{S1} and in C_{S2} which results in switching losses. Due to the inherently large leakage inductance of the PCB-integrated flyback transformer the energy stored in L_σ is large enough to always fulfill (4.38). After the turn-ON of S_1 interval 6 begins.

Interval 6, cf. **Fig. 4.10** (g): During this interval, i_{P} increases linearly until $i_{\text{P}}(T_{\text{P}}) = i_{\text{M}}(T_{\text{P}})$,

$$i_{\text{P}}(t) = I_5 + \frac{v_{\text{n1}} + n \cdot V_{\text{out}}}{L_\sigma} \cdot (t - t_5), \tag{4.42}$$

while the magnetizing current still decreases according to (4.33).

This concludes a switching cycle and the next period is beginning with interval 1.

4.3.2 Discontinuous conduction mode

Similar to the conventional flyback converter, the flyback converter with active snubber can be operated in CCM or in DCM[3]. For light load when the load current $\bar{I}_{\text{S}}$ is small, the waveforms given in **Fig. 4.12** result. The operation is very similar to CCM; the only difference is that during interval 4 the secondary current i_{S} decreases to zero and hence the output rectifier turns OFF before S_{Sn} is turned OFF. S_{Sn} is

[3]Compared to flyback converters without active snubber where the DCM operation is characterized by an interval during which the magnetizing current is zero, in the proposed converter employing an active snubber the magnetizing current keeps flowing. However, the secondary current i_{S} declines to zero before the end of the switching period and therefore this mode of operation is entitled as DCM [106].

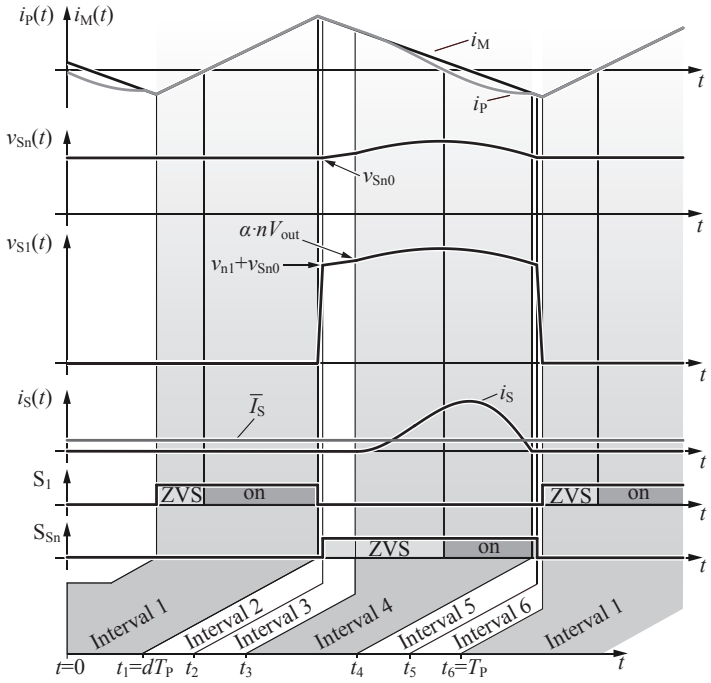


Fig. 4.12: Flyback converter waveforms operating in DCM for a switching period T_P.

turned OFF at t_5 when both i_P as well as i_M are negative; thus, the energy in the leakage inductance L_σ and the energy in the magnetizing inductance L_M are used to discharge C_{S1} and to charge C_{S2}.

As soon as v_{S1} reaches zero, the new switching cycle starts with interval 1.

4.3.3 Conclusion

Due to the active snubber circuit different current and voltage waveforms occur compared to a conventional flyback converter. CCM and DCM are very similar when an active snubber circuit is employed. In particular, the transition from CCM to DCM and vice versa does not change the voltage transfer ratio V_{out}/v_{n1} [106]. As a consequence, the

simplified model used to design each component in the converter which is discussed in the following section can be applied to CCM and DCM. Furthermore, the small signal model of the converter used to design the controllers of the converter system, cf. Section 4.5, is independent of the mode of operation. This simplifies the design of the converter and of the controller considerably.

In summary it can be seen that the discussed modulation of a flyback converter comprising an active snubber has following properties:

- Recycling of the energy E_σ stored in the leakage inductance.
- Reduction of voltage stress over the power switch [106].
- Reduction of switching losses due to ZVS or at least valley switching if (4.38) cannot be fulfilled [110].

A multi-cell flyback-type PFC rectifier employing an active snubber is therefore considered as an appropriate topology to realize the *Power Sheet*.

4.4 Design of the flyback PFC rectifier

This section discusses the design of the main power components of a flyback converter with active snubber, cf. **Fig. 4.9**, apart from the flyback transformer which is detailed in Chapter 5. The respective converter specifications of Section 1.2 are listed again in **Tab. 4.2**. The previous section showed that the current and voltage waveform in the considered topology do not differ for CCM and DCM. The design of each component is thus identical for both modes which is particularly beneficial when the converter is operated at the boundary of CCM and DCM since parameter tolerances could force the converter to operate in one or the other mode.

In the design six parallel flyback cells are considered; therefore, the output power of each cell is the total rated power divided by six. The design is carried out for a converter cell of $P_{\mathrm{out},i} = 38\,\mathrm{W}$ rated power which includes a safety margin for the design with respect to the expected efficiency.

4.4.1 Design based on a simplified converter model

The waveforms presented in **Fig. 4.11** and **Fig. 4.12** show very different characteristics compared to a conventional flyback converter. Nevertheless, applying some simplifications, an accurate design of each component is possible with reasonable effort [108]:

- The analysis of currents and voltages is simplified by assuming piecewise linear waveforms rather than considering intervals with sinusoidal waveforms. Furthermore, the short switching intervals (interval 2, interval 3, interval 5, and interval 6) are neglected in this model. **Fig. 4.13** presents the resulting current waveforms.

- The converter design requires for an initial assumption of the leakage inductance L_σ and of the efficiency to calculate the RMS currents and average currents of the model. 3-D FEM simulations show that the leakage inductance of a PCB-integrated flyback transformer is in the range of $10 \ldots 20\,\%$ of the magnetizing inductance L_M, cf. **Fig. 5.13**. As a result, in this design the leakage inductance is assumed to be $L_\sigma \approx L_\mathrm{M}/10$.

- Watson *et. al* [107] reports an efficiency of $89\,\%$ for a flyback converter with active snubber for an output power of $P_\mathrm{out} = 200\,\mathrm{W}$. Assuming that a PCB-integrated transformer generates more losses than an optimized conventional transformer, an efficiency of $\eta = 0.8$ is considered for this design.

Tab. 4.2: Specifications of the flyback-type PFC rectifier which is split into six modules of $P_{\mathrm{out},i} = 38\,\mathrm{W}$ each.

Quantity		Value
V_n	=	$230\,\mathrm{V_{rms}}$
f_m	=	$50\,\mathrm{Hz}$
V_out	=	$20\,\mathrm{V}$
P_out	=	$200\,\mathrm{W}$
f_min	=	$160\,\mathrm{kHz}$

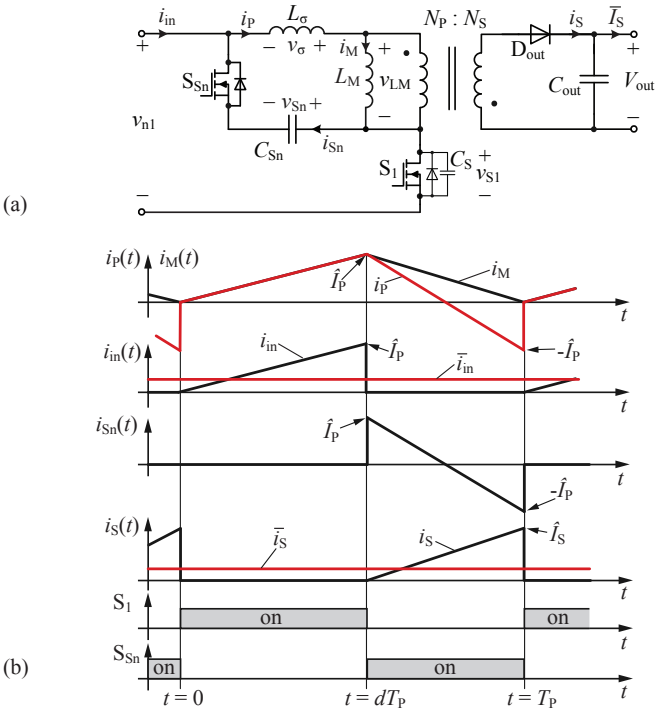


Fig. 4.13: (a) Flyback converter with active snubber. (b) Simplified waveforms of the flyback converter operating in BCM where the switching intervals are neglected and each waveform is considered as being piecewise linear.

Turns ratio n

The turns ratio n can be determined with the maximum allowable voltage stress of S_1, $\hat{V}_{S1}$ [105]. Assuming perfect clamping, the maximum voltage stress occurs at the maximum input voltage $\hat{V}_{n1}$,

$$\hat{V}_{S1} = \hat{V}_{n1} + v_\sigma + n\,V_{out}, \tag{4.43}$$

where v_σ is the voltage over the leakage inductance L_σ commutating the current to the secondary side, cf. **Fig. 4.13** (a). In order to consider a safety margin of $k_{sn} = 15\,\%$ and tolerating a voltage overshoot of

$v_\sigma = 150\,\mathrm{V}$, the turns ratio is

$$\hat{V}_{\mathrm{S1}} = \frac{1}{1+k_{\mathrm{sn}}} \cdot \left(1.1 \cdot \sqrt{2} V_{\mathrm{n}} + v_\sigma + n\, V_{\mathrm{out}}\right). \tag{4.44}$$

In (4.44) a tolerance of the input voltage of 10 % is considered. Applying a MOSFET featuring a drain-source voltage of 900 V yields a turns ratio of

$$n = 13. \tag{4.45}$$

Voltage conversion ratio $V_{\mathrm{out}}/v_{\mathrm{n1}}$

The voltage transfer ratio $V_{\mathrm{out}}/v_{\mathrm{n1}}$ and accordingly the duty cycle d of the power switch S_1 can easily be determined with the volt-second balance of the magnetizing inductance L_{M}. During the ON-time of S_1 the voltage applied to the magnetizing inductance L_{M} is, cf. **Fig. 4.13** (a),

$$v_{\mathrm{LM}} = \frac{v_{\mathrm{n1}}}{1+\beta} = \frac{v_{\mathrm{n1}}}{\alpha}, \tag{4.46}$$

while during the OFF-time of S_1 it is

$$v_{\mathrm{LM}} = n \cdot V_{\mathrm{out}}. \tag{4.47}$$

In steady-state operation, the positive and the negative voltage-time integrals applied to L_{M} are equal,

$$\frac{v_{\mathrm{n1}}}{\alpha} \cdot d\, T_{\mathrm{P}} = n V_{\mathrm{out}} \cdot (1-d) T_{\mathrm{P}}, \tag{4.48}$$

and thus

$$\frac{n V_{\mathrm{out}}}{v_{\mathrm{n1}}(t)} = \frac{1}{\alpha} \cdot \frac{d(t)}{1-d(t)}, \tag{4.49}$$

and/or

$$d(t) = \frac{\alpha \cdot n V_{\mathrm{out}}}{v_{\mathrm{n1}}(t) + \alpha \cdot n V_{\mathrm{out}}}, \tag{4.50}$$

whereas α is specified according to (4.27). Eq. (4.50) is valid for both CCM and DCM, which can easily be shown by applying (4.46) and (4.47) for DCM as well. **Fig. 4.15** (a) shows the duty cycle d over a quarter of the mains period, $T_{\mathrm{m}}/4$, for the specifications given in **Tab. 4.2**.

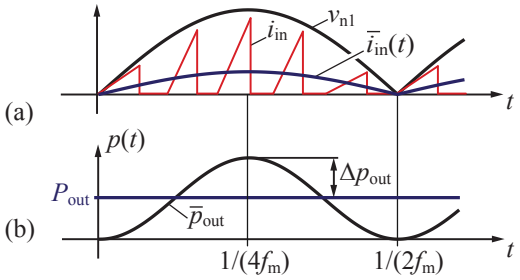


Fig. 4.14: (a) Input current i_{in}, average input current $\bar{i}_{in}$, and input voltage v_{n1} over half of a mains period, and (b) output power variation as typical for single-phase AC-DC rectifiers. $\bar{p}_{out}$ denotes the local averaged output power with regard to a switching cycle.

Magnetizing inductance L_M

The design of the magnetizing inductance L_M is very similar to the design in a conventional flyback converter. L_M is determined by the specified switching frequency range of the converter, cf. **Tab. 4.2**. In this simplified model the input current $i_{in}(t)$ is considered to be triangular shaped during a switching cycle, cf. **Fig. 4.13** (b). Hence, the peak current $\hat{I}_P(t)$ is given by

$$\hat{I}_P(t) = \frac{v_{n1}(t)}{\alpha \cdot L_M} \cdot d(t)\, T_P(t) = \frac{v_{n1}(t)}{\alpha \cdot L_M} \cdot \frac{d(t)}{f_S(t)}. \tag{4.51}$$

As a consequence, the average input current $\bar{i}_{in}(t)$ during one switching period is

$$\bar{i}_{in}(t) = \frac{1}{2} \cdot \hat{I}_P(t) \cdot d(t) = \frac{v_{n1}(t)}{2 \cdot \alpha L_M} \cdot \frac{d(t)^2}{f_S(t)}. \tag{4.52}$$

For perfect PFC behavior the average input current $\bar{i}_{in}(t)$ must follow the input voltage $v_{n1}(t)$ as indicated in **Fig. 4.14** (a); the local average output power of the converter $\bar{p}_{out}(t)$ is

$$\begin{aligned} \bar{p}_{out}(t) &= \eta \cdot v_{n1}(t) \cdot \bar{i}_{in}(t) = \eta \cdot V_n \cdot I_{in} \cdot (1 - \cos(2\,\omega_m t)) = \\ &= P_{out} \cdot (1 - \cos(2\,\omega_m t))\,, \end{aligned} \tag{4.53}$$

where η is an assumed efficiency value of the converter and $\omega_m = 2\pi f_m$ is the mains angular frequency. Combining (4.52) with (4.53) and solving

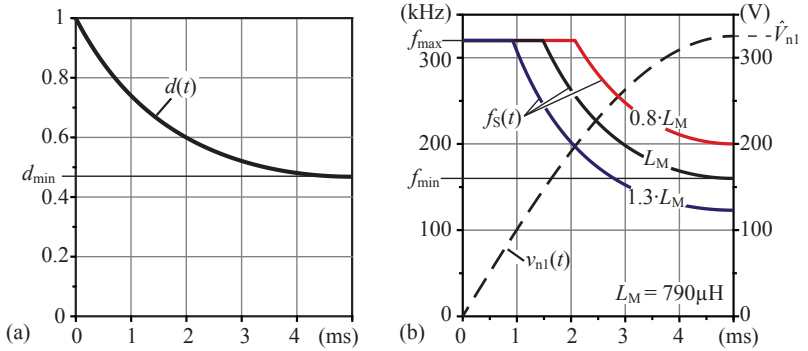


Fig. 4.15: (a) Duty cycle d over a quarter, $T_m/4$, of the mains period. (b) Switching frequency f_S for several values of L_M and input voltage v_{n1}.

for f_S yields

$$f_S(t) = \frac{v_{n1}(t)^2}{2 \cdot \alpha L_M} \cdot \frac{\eta \cdot d(t)^2}{P_{out} \cdot (1 - \cos(2\,\omega_m t))}. \tag{4.54}$$

Fig. 4.15 (b) illustrates f_S for several values of L_M over a quarter of the mains period. As can be seen, the minimal switching frequency f_{min} occurs at maximum input voltage $\hat{V}_{n1} = \sqrt{2}\,V_n$. Furthermore, **Fig. 4.15** (b) shows that an increase of the magnetizing inductance L_M results in a lower switching frequency. In order to operate in the specified frequency range, cf. (4.18) the maximum switching frequency is limited to $f_{max} = 320\,\text{kHz}$. Thus, the operation mode changes from BCM to DCM as soon as $f_S(t) > f_{max}$.

The magnetizing inductance can be evaluated using the initial assumptions $L_\sigma \approx L_M/10$ and $\eta \approx 0.8$ and with the specifications given in **Tab. 4.2** at maximum input voltage; the evaluation of (4.54) yields

$$f_{min} = \frac{V_n^2}{2 \cdot \alpha L_M} \cdot \frac{\eta \cdot d_{min}^2}{2 \cdot P_{out}} \quad \Rightarrow \quad L_M = 790\,\mu\text{H}. \tag{4.55}$$

Leakage inductance L_σ

The setup of a conventional flyback transformer allows for comparably small leakage coefficients σ (typ. $\sigma = 2 \ldots 5\,\%$). In order to achieve

ZVS, the leakage inductance must hold, cf. [108],

$$L_\sigma \geq \frac{(C_{S1} + C_{S2}) \cdot (v_{n1} + n\, V_{out})^2}{\hat{I}_P^2}. \tag{4.56}$$

This condition may be violated if transformers with very low leakage inductances are used. PCB-integrated transformers, however, feature an inherently large leakage inductance ($\sigma > 10\,\%$) and therefore, (4.56) is fulfilled without any further ado.

Snubber capacitor C_{Sn}

The value of the snubber capacitor C_{Sn} has to be designed ensuring that half of the resonance period of the L_σ–C_{Sn} tank, $T_\sigma/2$, is larger than the duration of interval 4, T_4, cf. **Fig. 4.11**,

$$T_4 < \frac{T_\sigma}{2} = \pi \cdot \sqrt{L_\sigma C_{Sn}}. \tag{4.57}$$

Considering $T_P > T_4$, allows for a conservative estimation of the lower bound of T_σ,

$$T_4 < T_P = \frac{1}{f_S} < \frac{T_\sigma}{2} = \pi \cdot \sqrt{L_\sigma C_{Sn}}, \tag{4.58}$$

which yields for the lower bound of C_{Sn},

$$C_{Sn} > \frac{1}{L_\sigma} \left(\frac{T_{P,max}}{\pi} \right)^2 = \frac{1}{L_\sigma} \left(\frac{1}{\pi\, f_{min}} \right)^2 = 50\,\text{nF}. \tag{4.59}$$

The ripple voltage Δv_{Sn} of the snubber capacitor can be calculated with (4.34). **Fig. 4.16** presents the respective equivalent circuit and shows Δv_{Sn} as a function of the snubber capacitance C_{Sn}, cf. **Fig. 4.11**. As can be seen, a large value of C_{Sn} which would increase size and costs of the component is not necessary as already for capacitances of a few 10 nF a low voltage ripple Δv_{Sn} is achieved. Therefore, for an assumed leakage inductance $L_\sigma = L_M/10 \approx 80\,\mu\text{H}$, the snubber capacitance is chosen to be $C_{Sn} = 50\,\text{nF}$.

The maximum voltage over C_{Sn}, $\hat{V}_{Csn}$, occurs at maximum input voltage $\hat{V}_{n1}$ which yields with (4.34)

$$\hat{V}_{Csn} = 1.1 \cdot \hat{V}_{n1} + \Delta v_{Sn} = 364\,\text{V}. \tag{4.60}$$

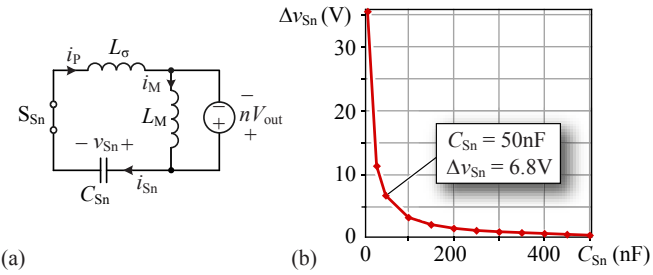


Fig. 4.16: (a) Equivalent circuit during the on-time of S_{Sn}. (b) Snubber voltage ripple Δv_{Sn} as a function of the snubber capacitance C_{Sn} for the specifications according to **Tab. 4.2** and a leakage inductance $L_\sigma = 80\,\mu H$; the input voltage is $v_{n1} = 325\,V$, and the output power is $P_{out} = 76\,W$.

In order to estimate the RMS current through C_{Sn} in this simplified model, the current i_{Sn} is approximated by a sawtooth waveform, cf. **Fig. 4.13** (b). This assumption is justified if the duration of one oscillation of the $L_\sigma - C_{Sn}$ resonance tank is significantly larger than the duration of interval 4, which has already be ensured with the design of the snubber capacitor C_{Sn}.

The current $\hat{I}_P$, cf. **Fig. 4.13** (b), varies over the mains period according to (4.51) and, therefore, the RMS value of i_{Sn} during one switching period, $i_{Sn,rms}(t)$, is

$$i_{Sn,rms}(t) = \hat{I}_P(t) \cdot \sqrt{\frac{1-d(t)}{3}} = \frac{v_{n1}(t)}{\alpha L_M} \cdot \frac{d(t)}{f_S(t)} \cdot \sqrt{\frac{1-d(t)}{3}}. \quad (4.61)$$

The RMS current over one mains period can be determined by integration of $i_{Sn,rms}$ as

$$I_{Sn} = \sqrt{\frac{1}{T_m} \int_0^{T_m} \hat{I}_P^2(t) \cdot \frac{1-d(t)}{3} \cdot \mathrm{d}t} = 292\,mA, \quad (4.62)$$

with $T_m = 1/f_m$. The chosen capacitors are SMD chips (footprint 0805 [47]) with a dissipation factor $\tan(\delta) = 2.5\,\%$ and a voltage rating of 500 V. The losses in the snubber capacitor are

$$P_{Csn,loss} = \frac{\tan(\delta)}{2\,\pi\,f_S \cdot C_{Sn}} \cdot I_{Sn}^2 = 44.7\,mW, \quad (4.63)$$

whereas $f_S = f_{min}$ in order to consider the worst case.

Snubber switch S_{Sn}

During the turn-ON interval of S_1, the voltage

$$v_{Ssn1} = v_{n1} + v_{Csn} \tag{4.64}$$

is applied to S_{Sn}. Thus, the voltage rating of S_1 and S_{Sn} are the same and a 900 V switch has to be applied, cf. (4.44).

The RMS current through the switch is already calculated in (4.62). The chosen MOSFET is an IPD90R1K2C3 from Infineon [56]; the specifications are listed in **Fig. 4.17**.

Very low switching losses are expected due to ZVS. Therefore, the loss calculation only accounts for the conduction losses. In order to consider the increase of $R_{DS(on)}$ with increasing junction temperature T_J, an iterative loss calculation is applied[4]. **Fig. 4.18** (a) shows the procedure which terminates when the junction temperature increase is smaller than T_{limit} which is set to 1 °C in this design. **Fig. 4.18** (b) depicts the dependency of the on-state resistance of an IPD90R1K2C3 on the junction temperature. In the loss calculation the typical value of $R_{DS(on)}$, cf. **Fig. 4.18** (b), is applied. The junction temperature can be estimated by considering the thermal equivalent circuit presented in **Fig. 4.18** (c) [112]. In the calculation, an ambient temperature according to **Tab. 1.2** is considered and the thermal resistance R_{thJA} from the junction to the ambient is taken from the datasheet for the specified footprint (TO-252: $R_{thJA} = 62\,K/W$).

After two iteration steps the conduction loss converges to $P_{Sn,cond} = 135\,mW$ and the junction temperature is $T_J = 53.4\,°C$ ($T_{amb} = 45\,°C$).

Power switch S_1

The design of the turns ratio n already determines the required voltage rating of the power switch S_1, which is $V_{DS} = 900\,V$. The current through S_1 can be determined similar to I_{Sn}, cf. (4.61) and (4.62). As i_{in} is assumed to be triangular shaped, the RMS value for one switching period T_P is

$$i_{in,rms}(t) = \hat{I}_P(t) \cdot \sqrt{\frac{d(t)}{3}} = \frac{v_{n1}(t)}{\alpha L_M} \cdot \frac{d(t)}{f_S(t)} \cdot \sqrt{\frac{d(t)}{3}}, \tag{4.65}$$

[4] A closed-form solution could also be obtained with a curve fit of the temperature dependency of $R_{DS(on)}$ [111].

and the RMS current over a mains period can be calculated with

$$I_{\text{in}} = \sqrt{\frac{1}{T_{\text{m}}} \int_0^{T_{\text{m}}} \hat{I}_{\text{P}}^2(t) \cdot \frac{d(t)}{3} \cdot \text{d}t} = 296\,\text{mA}. \tag{4.66}$$

As for S_{Sn}, an IPD90R1K2C3 from Infineon [56] is applied (characteristics given in **Fig. 4.17**) and the conduction losses are calculated similar, cf. **Fig. 4.18**. The conduction losses in S_1 are thus $P_{\text{S1,cond}} = 135\,\text{mW}$ at a junction temperature of $T_{\text{J}} = 53.4\,^{\circ}\text{C}$.

Output rectifier

With the given specifications comparably large currents on the secondary side ($\approx 4\,\text{A}$) result. In order to reduce the conduction losses, the output diode D_{out} is replaced by the MOSFET S_{out} with a low ON-state resistance. The voltage stress of S_{out} is equal to that of the diode of a conventional flyback converter,

$$\hat{V}_{\text{Sout}} = V_{\text{out}} + \frac{\hat{V}_{\text{n1}}}{n} = V_{\text{out}} + \frac{1.1 \cdot \sqrt{2} V_{\text{n}}}{n} = 47.5\,\text{V}, \tag{4.67}$$

where 10 % tolerance of the mains voltage are considered. In order to consider a safety margin, a 100 V MOSFET is applied in the design.
The current stress in S_{out} can be estimated by assuming the simplified current waveform depicted in **Fig. 4.13** (b). The calculation of the RMS

Quantity		Value
$V_{\text{DS,max}}$	=	900 V
$R_{\text{DS(on)}}$	=	1.2 Ω @ 25 °C
$Q_{\text{g,typ}}$	=	28 nC
I_{D}	=	5.1 A
V_{GS}	=	±20 V

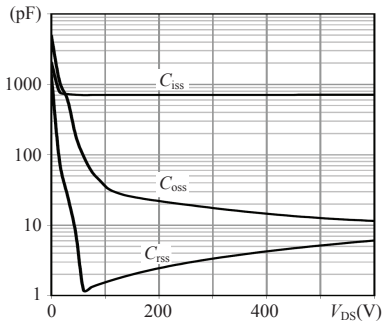


Fig. 4.17: Parameters of the IPD90R1K2C3 MOSFET from Infineon [56].

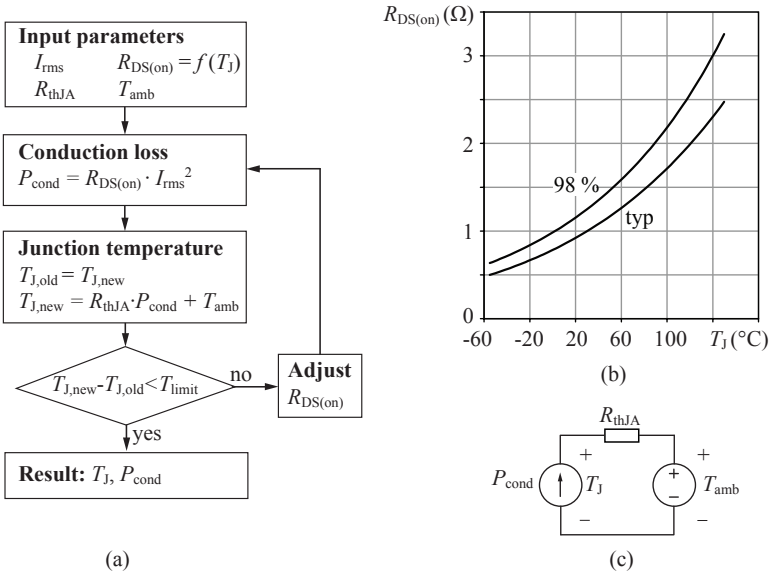


Fig. 4.18: (a) Block diagram of the conduction loss calculation. (b) $R_{DS(on)}$ as a function of the junction temperature T_J for the power MOSFET IPD90R1K2C3 [56]. (c) Simplified thermal equivalent circuit used to estimate T_J [112].

current is similar to the input current evaluation; thus,

$$I_S = \sqrt{\frac{1}{T_m} \int_0^{T_m} (n\,\hat{I}_P(t))^2 \cdot \frac{1 - d(t)}{3} \cdot \mathrm{d}t} = 3.8\,\mathrm{A}. \tag{4.68}$$

The maximum current is applied to S_{out} when $\hat{I}_P(t)$ is at its maximum which is at maximum input voltage $\hat{V}_{n1}$ or respectively at $t = T_m/4$,

$$\hat{I}_S = n\,\hat{I}_P(t = T_m/4) = 16.73\,\mathrm{A}. \tag{4.69}$$

The employed MOSFET is a BSC205N10LS from Infineon [56] which features the characteristics listed in **Tab. 4.3**.

The conduction losses in S_{out} are determined according to **Fig. 4.18** (a). After four iteration steps the losses converge to

$$P_{Sout,cond} = 375\,\mathrm{mW} \tag{4.70}$$

at a junction temperature of $T_J = 68\,°\mathrm{C}$.

Tab. 4.3: Characteristics of power MOSFET BSC205N10LS from Infineon [56].

Quantity		Value
$V_{\mathrm{DS,max}}$	=	100 V
$R_{\mathrm{DS(on)}}$	=	20.5 mΩ
$Q_{\mathrm{g,typ}}$	=	31 nC
I_{D}	=	45 A
V_{GS}	=	±20 V

Output capacitor C_{out}

The design of the output capacitor is already discussed in Section 3.4 and therefore it is not elaborated here. The discussion yields the equation

$$C_{\mathrm{out}} \geq \frac{P_{\mathrm{out}}}{2\,\omega_{\mathrm{m}} \cdot \Delta v_{\mathrm{out}} \cdot V_{\mathrm{out}}}, \tag{4.71}$$

with which the required output capacitance C_{out} for a specified voltage ripple Δv_{out} can be determined. For a voltage ripple amplitude of 2 V of the output voltage, C_{out} is

$$C_{\mathrm{out}} = 1.51\,\mathrm{mF}. \tag{4.72}$$

In conventional AC-DC converters C_{out} is typically realized with electrolytic capacitors; there the maximum allowable RMS current in the capacitor may be the limiting factor, i.e. determines the minimum required C_{out} rather than the output voltage ripple. However, in an ultra-flat power supply only ceramic capacitors can be used which show a comparably high current rating per unit capacitance and therefore the design is determined by the output voltage ripple.

The output capacitor is realized with 160 capacitor chips connected in parallel where each has a capacitance of 10 µF, a rated voltage of 25 V, and a dissipation factor of $\tan(\delta) < 0.125$ [41]. Thus, the losses in C_{out} can be neglected.

Design summary

In the previous subsections each power component of the flyback-type single-phase PFC rectifier apart from the flyback transformer, cf. Sec-

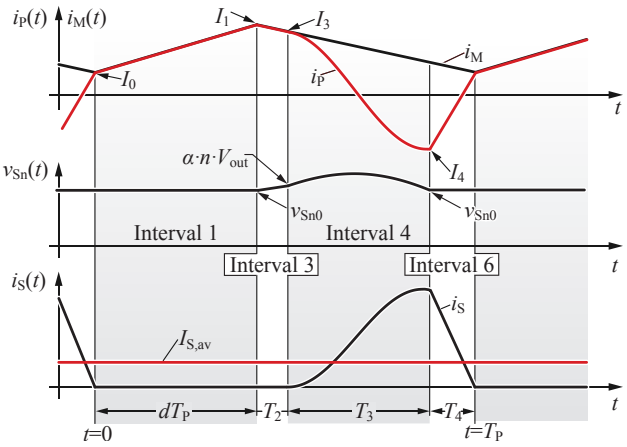


Fig. 4.19: Converter waveforms considered in the accurate model. The intervals are termed according to **Fig. 4.11** in order to be consistent.

tion 5.3, is designed. **Tab. 4.4** lists a summary of the achieved results, the requirements for the components, and the selected elements.

4.4.2 Accurate converter model

The model described in Section 4.4.1 allows for a straightforward design of each power component of the flyback converter. In order to justify the simplifications, an accurate model of the converter is presented in this section. In this improved model the steady-state current and voltage waveforms are not considered to be piecewise linear but the actual sinusoidal characteristics are included.

Fig. 4.19 shows the waveforms of a switching period in this model (the corresponding equivalent circuits are depicted in **Fig. 4.10**). Compared to **Fig. 4.11**, the switching intervals (interval 2 and interval 5 in **Fig. 4.11**) are neglected as they are very short. Furthermore, the parasitic output capacitance of S_1, C_{S1}, is neglected as it is significantly small compared to the snubber capacitor C_{Sn} and, therefore, has negligible impact on the waveforms. Still, the model is too complex to solve it analytically and thus it is solved numerically for a given set of parameters.

The model consists of nine equations whereas several are nonlinear.

Tab. 4.4: Circuit parameters of the 38 W flyback-type PFC rectifier.

Flyback transformer			
L_M	$= 790\,\mu\mathrm{H}$	I_P	$= 415\,\mathrm{mA}$
n	$= 13$	I_S	$= 3.8\,\mathrm{A}$
MOSFETs			
Power switch $\mathbf{S}_1$:		IPD90R1K2C3 [56]	
$R_\mathrm{DS(on)}$	$= 1.2\,\Omega$ @ $25\,^\circ\mathrm{C}$		
V_DS	$= 900\,\mathrm{V}$	I_S1	$= 296\,\mathrm{mA}$
$Q_\mathrm{g,typ}$	$= 28\,\mathrm{nC}$	$\hat{V}_\mathrm{S1}$	$= 775\,\mathrm{V}$
Package:	= TO-252	$P_\mathrm{S1,cond}$	$= 135\,\mathrm{mW}$
Snubber switch $\mathbf{S}_\mathrm{Sn}$:		IPD90R1K2C3 [56]	
$R_\mathrm{DS(on)}$	$= 1.2\,\Omega$ @ $25\,^\circ\mathrm{C}$		
V_DS	$= 900\,\mathrm{V}$	I_Sn	$= 292\,\mathrm{mA}$
$Q_\mathrm{g,typ}$	$= 28\,\mathrm{nC}$	$\hat{V}_\mathrm{Sn}$	$= 775\,\mathrm{V}$
Package:	= TO-252	$P_\mathrm{Sn,cond}$	$= 135\,\mathrm{mW}$
Output rectifier switch $\mathbf{S}_\mathrm{out}$:		BSC205N10LS [56]	
$R_\mathrm{DS(on)}$	$= 20.5\,\mathrm{m}\Omega$ @ $25\,^\circ\mathrm{C}$	I_S	$= 3.8\,\mathrm{A}$
V_DS	$= 100\,\mathrm{V}$	$\hat{I}_\mathrm{S}$	$= 16.7\,\mathrm{A}$
$Q_\mathrm{g,typ}$	$= 31\,\mathrm{nC}$	$\hat{V}_\mathrm{Sout}$	$= 47.5\,\mathrm{V}$
Package:	= TDSON-8	$P_\mathrm{Sn,cond}$	$= 375\,\mathrm{mW}$
Capacitors			
Snubber capacitor $C_\mathrm{Sn} = 50\,\mathrm{nF}$:			
C	$= 10\,\mathrm{nF}$		
$\tan(\delta)$	$= 2.5\,\%$	I_Sn	$= 292\,\mathrm{mA}$
V_rated	$= 500\,\mathrm{V}$	$\hat{V}_\mathrm{Csn}$	$= 376\,\mathrm{V}$
Package:	= 0805 (5 in parallel)	$P_\mathrm{CSn,loss}$	$= 44.7\,\mathrm{mW}$
Output capacitor $C_\mathrm{out} = 1.51\,\mathrm{mF}$:			
C	$= 10\,\mu\mathrm{F}$		
V_rated	$= 25\,\mathrm{V}$	$\hat{V}_\mathrm{Cout}$	$= 22\,\mathrm{V}$
Package:	= 0805 (160 in parallel)	$\tan(\delta)$	< 0.125

In order to find a solution, i.e. the converter's steady-state current and voltage waveforms, a nonlinear minimization problem has been stated consisting of the linear and the nonlinear equations and constraints of each parameter. The equations needed to solve the model are basically already derived in Section 4.3; however to clarify the model they are discussed in the following.

The input parameter required to solve the equations are

- the input voltage v_{n1},
- the output voltage V_{out},
- the output power $\bar{p}_{\mathrm{out}}$,
- and the converter parameters L_{M}, L_{σ}, C_{Sn}, and n.

The resulting parameters needed to characterize the steady-state current and voltage waveforms are, cf. **Fig. 4.19**,

- the currents I_0, I_1, I_3, I_4,
- the initial snubber voltage v_{Sn0},and
- the interval durations T_2, T_3, T_4, T_{P}.

The duty cycle d is calculated according to (4.50).

Timing of a switching cycle

The first equation states that the sum of the durations of the individual intervals must be the length T_{P} of a switching cycle, cf. **Fig. 4.19**:

$$T_{\mathrm{P}} = d \cdot T_{\mathrm{P}} + T_2 + T_3 + T_4. \tag{4.73}$$

Magnetizing current $i_{\mathrm{M}}(t)$

The magnetizing current i_{M} increases linearly starting from I_0 at $t = 0$ and reaches I_1 at $t = d\,T_{\mathrm{P}}$,

$$I_0 + \frac{v_{\mathrm{n1}}}{L_{\mathrm{M}} + L_{\sigma}} \cdot d\,T_{\mathrm{P}} = I_1. \tag{4.74}$$

Interval 3 is basically a resonance interval as the circuit composed of C_{Sn}, L_{M}, and L_{σ} starts to resonate, cf. **Fig. 4.10** (d). However, taking into account that

$$T_2 \ll \frac{2\pi}{\omega_1} = 2\pi \cdot \sqrt{\alpha\, L_{\mathrm{M}} \cdot C_{\mathrm{Sn}}}, \tag{4.75}$$

a linear current decrease of i_{M} can be assumed during this interval,

$$I_1 - \frac{v_{\mathrm{Sn0}}}{L_{\mathrm{M}} + L_{\sigma}} \cdot T_2 = I_3, \tag{4.76}$$

whereas in (4.75) ω_1 is defined according to (4.32). During interval 4 and interval 6, i_{M} is decreasing linearly according to

$$I_3 - \frac{n\, V_{\mathrm{out}}}{L_{\mathrm{M}}} \cdot (T_3 + T_4) = I_0. \tag{4.77}$$

This equation, however, is not required to solve the system but is presented for the sake of integrity. Eqs. (4.74) and (4.76) characterize the magnetizing current i_{M} and thus two equations of the analytical model are derived.

Primary current $i_{\mathrm{P}}(t)$

The primary current i_{P} is identical to i_{M} during interval 1 and interval 3. The current waveform during the resonance interval 4 is determined in (4.34). Substitution of the initial and final conditions of the interval into (4.34) yields

$$I_3 \cdot \cos(\omega_2 \cdot T_3) - \frac{nV_{\mathrm{out}}}{\omega_2 \cdot L_{\mathrm{M}}} \cdot \sin(\omega_2 \cdot T_3) = I_4, \tag{4.78}$$

whereas ω_2 is defined by (4.36). During interval 6, i_{P} is characterized by a linear current rise according to

$$I_4 + \frac{v_{\mathrm{n1}} + n\, V_{\mathrm{out}}}{L_{\sigma}} \cdot T_4 = I_0. \tag{4.79}$$

Eqs. (4.78) and (4.79) define the oscillation intervals of the leakage current and two equations of the analytical model are obtained.

Snubber capacitor voltage $v_{\mathrm{Sn}}(t)$

The voltage over the snubber capacitor, v_{Sn}, is constant during interval 1. In interval 3, a linear approximation based on (4.75) can be applied. Thus, the voltage is assumed to increase linearly,

$$v_{\mathrm{Sn0}} + \frac{I_3}{C_{\mathrm{Sn}}} \cdot T_2 = \alpha \cdot n\, V_{\mathrm{out}}. \tag{4.80}$$

During the resonance interval 4, the voltage v_{Sn} is determined by (4.34). Applying the initial and the final conditions of this interval to (4.34) yields

$$n\,V_{\mathrm{out}} \cdot (1 + \beta \cdot \cos(\omega_2 \cdot T_3)) + Z_2 \cdot I_3 \cdot \sin(\omega_2 \cdot T_3) = v_{\mathrm{Sn0}}. \tag{4.81}$$

Thus, the voltage applied to the snubber capacitor, $v_{\mathrm{Sn}}(t)$, is derived and two equations of the analytical model are determined.

Energy balance

As this model does not include losses, the energy balance can be applied to each interval. During interval 3, energy is transferred from the inductors L_{M} and L_σ to the snubber capacitor C_{Sn}. Thus, the reduction of energy in the inductors leads to an increase of energy in C_{Sn},

$$\frac{1}{2}\,(L_{\mathrm{M}} + L_\sigma) \cdot (I_1^2 - I_3^2) + \frac{1}{2}\,C_{\mathrm{Sn}} \cdot \left(v_{\mathrm{Sn0}}^2 - (\alpha \cdot n\,V_{\mathrm{out}})^2\right) = 0. \tag{4.82}$$

During the resonance interval 4, v_{Sn} decreases to v_{Sn0} and the corresponding energy is transferred to the leakage inductance L_σ,

$$\frac{1}{2}\,L_\sigma \cdot (I_3^2 - I_4^2) + \frac{1}{2}\,C_{\mathrm{Sn}} \cdot \left((\alpha \cdot n\,V_{\mathrm{out}})^2 - v_{\mathrm{Sn0}}^2\right) = 0. \tag{4.83}$$

Eq. (4.83) is redundant for the analytical model and is given for completeness.

Finally, the overall energy balance applied to the complete switching cycle can be established. The load power demand $\bar{p}_{\mathrm{out}}$ over a switching period T_{P}, i.e. the energy delivered to the load, is equal to the product of voltage and charge in the output capacitor C_{out}. The charge delivered to the output is the integral of the secondary current i_{S} evaluated over one switching cycle,

$$\bar{p}_{\mathrm{out}}(t) \cdot T_{\mathrm{P}} = V_{\mathrm{out}} \cdot \int_0^{T_{\mathrm{P}}} i_{\mathrm{S}}(t) \cdot \mathrm{d}t = V_{\mathrm{out}} \cdot \int_0^{T_{\mathrm{P}}} n \cdot (i_{\mathrm{M}}(t) - i_{\mathrm{P}}(t)) \cdot \mathrm{d}t, \tag{4.84}$$

whereas $\bar{p}_{\mathrm{out}}$ is the local average output power of the converter defined by v_{n1}, cf. (4.53). Eqs. (4.82) and (4.84) complete the set of equations for the analytical model.

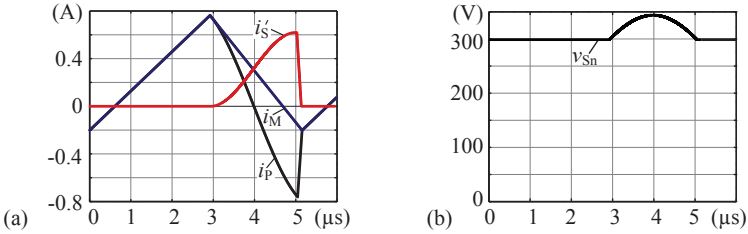


Fig. 4.20: (a) Calculated current waveforms of i_P, i_M, and i'_S which is referred to the primary side. (b) Calculated voltage applied to the snubber capacitor, v_{Sn}, for the parameters given in **Tab. 4.5**.

Tab. 4.5: Input parameters of the numerical calculation of the converter waveforms.

L_M	=	790 µH	v_{n1}	=	230 V
L_σ	=	80 µH	V_{out}	=	20 V
C_{Sn}	=	50 nF	$\bar{p}_{out}$	=	38 W
n	=	13			

Results of the numerical solver

A steady-state solution of the converter for a given input parameter set can be obtained by numerically solving the equations (4.73), (4.74), (4.76), (4.78)-(4.82), and (4.84). By way of an example, the converter current waveforms have been calculated for the input parameter set listed in **Tab. 4.5**. With the resulting parameters given in **Tab. 4.6**, the waveforms depicted in **Fig. 4.20** are obtained.

In order to determine the current and voltage values with respect to the mains period the numerical procedure is evaluated at discrete time instants over one quarter of the mains period and the integrals given in Section 4.4.1, e.g. (4.66), are evaluated numerically. The RMS currents can then be determined by geometric sums using a discrete interval Δt:

$$I = \sqrt{\frac{1}{1/4\, T_m} \cdot \sum_i i^2_{rms,i} \cdot \Delta t}; \tag{4.85}$$

$i_{rms,i}$ denotes the local RMS currents at $t = t_i$, respectively, and is calculated using the results of the numerical solver, i.e. the waveforms

Tab. 4.6: Results of the numerical calculation for the parameters given in **Tab. 4.5**.

I_0	=	−201 mA	d	=	0.554
I_1	=	785 mA	T_2	=	5 ns
I_3	=	780 mA	T_3	=	2.18 µs
I_4	=	−780 mA	T_4	=	133 ns
v_{Sn0}	=	297 V	T_{P}	=	5.2 µs
I_{P}	=	456 mA	I_{Sn}	=	318 mA
I_{S}	=	3.4 A	I_{S1}	=	328 mA

Tab. 4.7: Comparison between the calculated RMS currents of the converter obtained for PFC operation at $P_{\mathrm{out}} = 38\,\mathrm{W}$ by the analytical model and by the simplified model presented in Section 4.4.1.

Analytical model			Simplified model		
I_{P}	=	417 mA	I_{P}	=	415 mA
I_{S}	=	4.3 A	I_{S}	=	3.8 A
I_{Sn}	=	370 mA	I_{Sn}	=	292 mA
I_{in}	=	370 mA	I_{in}	=	296 mA

depicted in **Fig. 4.20**, at discrete time instants t_i ($t_i = 0 \ldots T_{\mathrm{m}}/4$ with $\Delta t = 250\,\mu\mathrm{s}$).

Tab. 4.7 lists a comparison between the calculated RMS currents obtained by the analytical model and the simplified model evaluated over a mains period. Obviously, the simplified model underestimates the RMS values of the currents due to the piecewise linear approximation of the waveforms. For the design of the converter components, however, the simple model is accurate enough particularly with the included safety margins. A final comparison of all calculated and measured results is presented in **Tab. 4.8**.

4.5 Control structure

This section describes the control structure and the controller design of the ultra-flat single-phase flyback-type AC-DC PFC rectifier. A digital

signal processor (DSP) (TMS320F2808 by TI [88]) is employed for the control. With this DSP all the analog to digital conversions and the control calculations can be performed.

4.5.1 PFC control structure

The control circuit fulfills two tasks. The first task is to achieve PFC functionality of the converter, which means that the input current i_{n} must be proportional to the mains voltage v_{n}:

$$i_{\mathrm{n}} = G_{\mathrm{in}} \cdot v_{\mathrm{n}}, \tag{4.86}$$

(G_{in} denotes the converter's input conductance). The second task of the controller is to regulate the output voltage V_{out}.

In order to achieve these goals a control structure according to **Fig. 4.21** is applied for the *Power Sheet*. The input quantities of the control are:

- Rectified input voltage v_{n1},
- Reference value of the output voltage $V_{\mathrm{out,ref}}$,
- Actual value of the output voltage V_{out},
- Rectified input current i_{n1}.

The outputs of the controller are the switching frequency f_{S} and the duty cycle for the power switch S_1 and the snubber switch S_{Sn}. In the following each block is described:

- $G(s)$ is the small-signal model of the flyback converter.
- The A/D blocks denote 12-bits analog-to-digital converters provided by the DSP.
- $H_{\mathrm{Vi}}(s)$ accounts for the time delay and the filtering of the input voltage measurement.
- $H_{\mathrm{I}}(s)$ accounts for the time delay and the filtering of the input current measurement.
- $K_{\mathrm{ff}}(s)$ represents the transfer function of the feedforward controller.

- $K_{\mathrm{I}}(s)$ is the transfer function of the inner loop current controller.
- $K_{\mathrm{V}}(s)$ is the outer loop output voltage controller.
- The topmost block represents a look-up table which maps the input voltage v_{n1} to a corresponding switching frequency f_{S}.

The input current i_{n} has a sinusoidal shape for constant G_{in}. The input conductance G_{in} determines how much energy is transferred to the load. With a given specified output voltage $V_{\mathrm{out,ref}}$, the difference between $V_{\mathrm{out,ref}}$ and the actual output voltage V_{out} is used to adjust G_{in} in order to control V_{out}.
This output voltage control loop is superimposed on an input current control loop. The bandwidth of the output voltage control loop needs to be considerably lower than $(2 \cdot f_{\mathrm{m}})$ to avoid the voltage controller to compensate the inherent output voltage ripple imposed by a single-phase system, which would distort the input current and thus result in a high THD value.

The DSP further adjusts the switching frequency f_{S} according to the input voltage v_{n1} in order to achieve operation close to BCM. This is realized with a look-up table.

4.5.2 Converter model

In order to design a feedback controller a small-signal model of the converter is required. Based on the converter modeling presented in [87] (the basic AC modeling approach) and the simplified converter model depicted in **Fig. 4.22** the small-signal model of the converter can be determined. The input voltage v_{n1} is assumed to be constant during a switching cycle. As already discussed in Section 4.3, the small-signal model is identical for CCM or DCM which facilitates a controller design without consideration of different operation modes.

Transfer function of the duty cycle to the input current

The averaging of the inductor voltage v_{Lm} and the capacitor current i_{C} with respect to a switching cycle based on the waveforms shown in **Fig. 4.22** yields

$$\bar{v}_{\mathrm{Lm}}(t) = L_{\mathrm{M}} \frac{\mathrm{d}\bar{i}_{\mathrm{M}}(t)}{\mathrm{d}t} = \frac{v_{\mathrm{n1}}(t)}{\alpha} \cdot d(t) - (1 - d(t)) \cdot n\, \bar{v}_{\mathrm{out}}(t), \qquad (4.87)$$

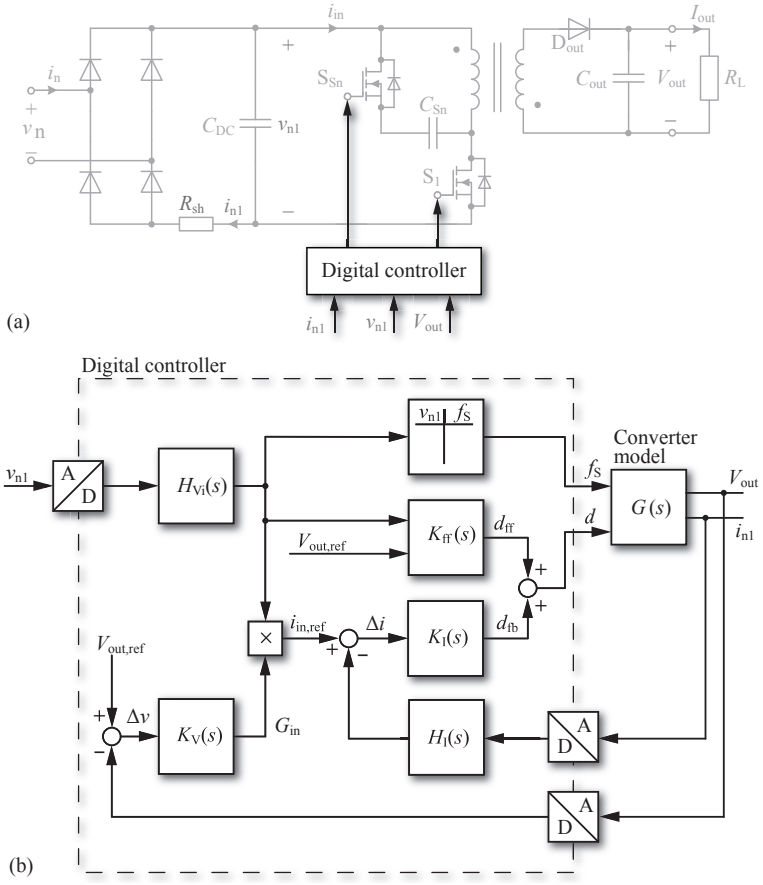


Fig. 4.21: (a) Schematic and control block of the flyback PFC rectifier which shows all required measurements. The rectified input current i_{n1} is measured using a shunt resistor R_{sh}. (b) Control structure of the PFC rectifier.

$$\begin{aligned}\bar{i}_{\mathrm{C}} &= C_{\mathrm{out}}\frac{\mathrm{d}\bar{v}_{\mathrm{out}}(t)}{\mathrm{d}t} = (1-d(t))\,\bar{i}_{\mathrm{S}} - \frac{\bar{v}_{\mathrm{out}}(t)}{R_{\mathrm{L}}} = \\ &= (1-d(t))\cdot\frac{n\,v_{\mathrm{n1}}(t)}{2\cdot\alpha\,L_{\mathrm{M}}}\cdot d(t)T_{\mathrm{P}}(t) - \frac{\bar{v}_{\mathrm{out}}(t)}{R_{\mathrm{L}}},\end{aligned} \tag{4.88}$$

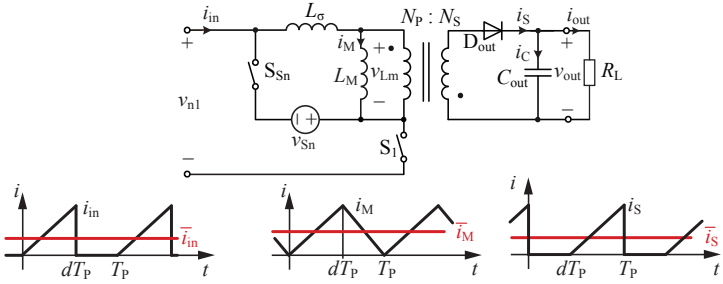


Fig. 4.22: Simplified converter model and current waveforms considered in the small-signal modeling.

with α according to (4.27).

These equations are nonlinear as multiplications with time-varying quantities are involved. In order to apply a linear feedback control to the converter a small-signal model, linearized at a given operating point[5], has to be evaluated. Therefore, each quantity is considered to be composed of a quiescent value $\bar{X}$ and a small deviation of the quantity $\hat{x}$ to the operating point,

$$\bar{x}(t) = \bar{X} + \hat{x}(t). \tag{4.89}$$

This approximation is based on the assumption that the deviation to the operating point is small which is reasonable considering the high switching frequency f_S compared to the mains frequency f_m. Applying the linearization of each time dependent quantity to (4.87) yields

$$L_M \frac{\mathrm{d}(\bar{I}_M + \hat{i}_M(t))}{\mathrm{d}t} = \frac{v_{n1}}{\alpha}(\bar{D} + \hat{d}(t)) - n\,(\bar{V}_{out} + \hat{v}_{out}(t))(1 - \bar{D} - \hat{d}(t)), \tag{4.90}$$

The collection of time-independent quantities in (4.90) leads to the steady-state solution,

$$L_M \frac{\mathrm{d}\bar{I}_M}{\mathrm{d}t} = 0 = \frac{v_{n1}}{\alpha} \cdot \bar{D} - (1 - \bar{D}) \cdot n\,\bar{V}_{out}, \tag{4.91}$$

[5]Since the operating point of a PFC rectifier changes proportionally to the sinusoidally-shaped input voltage several operating points of the converter have to be considered in order to analyze the local stability. The most critical operation point with respect to the stability is then considered for the design of the controllers.

which is identical to (4.50). This equation is based on the fact that in steady-state the inductor current is constant. The collection of linear terms results in the linearized small-signal model of the converter,

$$L_{\mathrm{M}} \frac{\mathrm{d}\hat{i}_{\mathrm{M}}(t)}{\mathrm{d}t} \approx \hat{d}(t) \cdot \left(\frac{v_{\mathrm{n1}}}{\alpha} + n\,\bar{V}_{\mathrm{out}} \right) - n\,\hat{v}_{\mathrm{out}}(t) \cdot (1 - \bar{D}). \tag{4.92}$$

The higher order terms are considered to be very small and thus negligible.

Transforming (4.92) into the Laplace domain and rearranging the terms gives the transfer function of the duty cycle $\hat{d}$ to the magnetizing current $\hat{i}_{\mathrm{M}}$,

$$\hat{i}_{\mathrm{M}}(s) = \frac{v_{\mathrm{n1}}}{s \cdot \alpha\, L_{\mathrm{M}} \cdot (1 - \bar{D})} \cdot \hat{d}(s). \tag{4.93}$$

In (4.93) it is assumed that the output voltage control loop regulates V_{out} tightly so that $\hat{v}_{\mathrm{out}}$ is small and can be neglected.
In order to control the input current $i_{\mathrm{in}}(t)$ of the converter a relation between d and i_{in} is required. The local average value of the input current $\bar{i}_{\mathrm{in}}$ can be calculated with the average magnetizing current,

$$\bar{i}_{\mathrm{in}}(t) = \bar{d}(t) \cdot \bar{i}_{\mathrm{M}}(t), \tag{4.94}$$

and a linearization yields

$$\hat{i}_{\mathrm{in}}(t) \approx \hat{d}(t) \cdot \bar{I}_{\mathrm{M}} + \bar{D} \cdot \hat{i}_{\mathrm{M}}(t). \tag{4.95}$$

Combining (4.93) with (4.95) results in the transfer function between the change in duty cycle, $\hat{d}(t)$, and the input current $\hat{i}_{\mathrm{in}}(t)$,

$$\begin{aligned} G_{\mathrm{id}}(s) = \frac{\hat{i}_{\mathrm{in}}(s)}{\hat{d}(s)} &= \frac{s \cdot \alpha\, L_{\mathrm{M}} \cdot (1 - \bar{D}) \bar{I}_{\mathrm{M}} + \bar{D} \cdot v_{\mathrm{n1}}}{s \cdot \alpha\, L_{\mathrm{M}} \cdot (1 - \bar{D})} = \\ &= \frac{s \cdot \alpha\, L_{\mathrm{M}} \cdot (1 - \bar{D}) \frac{\bar{I}_{\mathrm{in}}}{\bar{D}} + \bar{D} \cdot v_{\mathrm{n1}}}{s \cdot \alpha\, L_{\mathrm{M}} \cdot (1 - \bar{D})}. \end{aligned} \tag{4.96}$$

The transfer function $G_{\mathrm{id}}(s)$ can be evaluated at a certain operating point defined by the steady-state quantities $\bar{D}$, $\bar{I}_{\mathrm{in}}$, and v_{n1}. The operating point varies over the mains period as the input voltage v_{n1} and therefore also $\bar{I}_{\mathrm{in}}$ and $\bar{D}$ vary, cf. (4.53) and (4.50), respectively. In order to design a current controller which is stable for all input values,

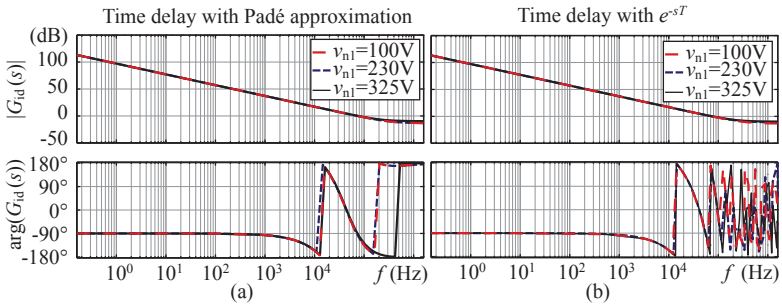


Fig. 4.23: (a) Bode plot of $G_{\mathrm{id}}(s)$ for several input voltages v_{n1} whereas the time delay induced by measurements and the DSP control is considered applying a Padé approximation. (b) Bode plot of $G_{\mathrm{id}}(s)$ where the time delay is modeled with a transcendental function $e^{-s\,T_{\mathrm{d,min}}}$. In each plot a time constant of $T_{\mathrm{d,min}} = 18.7\,\mu\mathrm{s}$ is used. The Padé approximation fits well up to a frequency of $f = 40\,\mathrm{kHz}$.

$G_{\mathrm{id}}(s)$ has to be evaluated for several operation points; the operating point with the lowest crossover frequency then needs to be considered for the controller design.

To consider time delays imposed by the measurement, the filtering, and the signal processing, a 3$^{\mathrm{rd}}$-order Padé approximation is included in the design,

$$G_{\mathrm{delay}}(s) = \frac{a_0 + a_1\,s + a_2\,s^2 + a_3\,s^3}{1 + b_1\,s + b_2\,s^2 + b_3\,s^3} \approx e^{-s\,T_{\mathrm{delay}}}. \tag{4.97}$$

In the control diagram shown in **Fig. 4.21** these time delays are modeled with $H_{\mathrm{I}}(s)$ and $H_{\mathrm{Vi}}(s)$ for the measurements of i_{in} and v_{n1}, respectively.

The DSP adjusts the duty cycle d and the switching frequency f_{S} every third switching cycle and thus, the resulting maximum time delay imposed by the control occurs at the minimal switching frequency,

$$T_{\mathrm{d,max}} = \frac{3}{f_{\mathrm{min}}} = 18.7\,\mu\mathrm{s}. \tag{4.98}$$

The Padé approximation is employed to consider $T_{\mathrm{d,max}}$ which yields for (4.97)

$$a_0 = 1, \qquad a_1 = -b_1 = -6.4\mathrm{e}5,$$
$$a_2 = b_2 = 1.71\mathrm{e}11, \qquad a_3 = -b_3 = -1.82\mathrm{e}16.$$

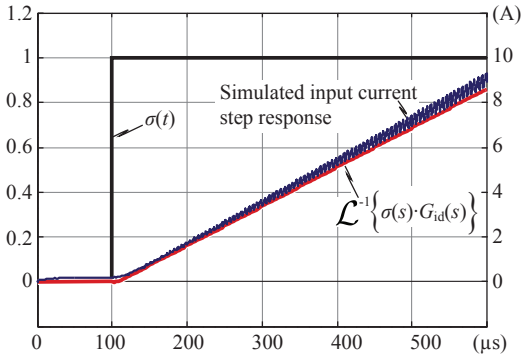


Fig. 4.24: Calculated and simulated step response of the open loop duty cycle to input current transfer function $G_{\mathrm{id}}(s)$. Parameters: $v_{\mathrm{n1}} = 100\,\mathrm{V}$, $V_{\mathrm{out}} = 20\,\mathrm{V}$, $\bar{I}_{\mathrm{in}} = 72\,\mathrm{mA}$, Step: from $\hat{d} = 0.75$ to $\hat{d} = 0.8$.

Fig. 4.23 (a) presents the Bode plot of $G_{\mathrm{id}}(s)$ for several input voltages including the time delay modeled with a Padé approximation. In order to proove validity of the approximation, **Fig. 4.23** (b) gives a Bode plot with transcendental time delay ($G_{\mathrm{delay}}(s) = e^{-s\,T_{\mathrm{d,max}}}$). The Padé approximation fits well up to a frequency of 40 kHz which is sufficient considering a current controller bandwidth lower than 10 kHz. The Bode plots show that the bandwidths at different operating points are between 107 kHz (100 V) and 115 kHz (325 V); for the design the lower bandwidth operation point, i.e. $v_{\mathrm{n1}} = 100\,\mathrm{V}$ has been considered. **Fig. 4.24** presents the calculated and the simulated open loop step response of $G_{\mathrm{id}}(s)$ and it can be seen that the simplified analytical model fits well to the simulation.

Transfer function of the input current to the output voltage

The output voltage controller $K_{\mathrm{V}}(s)$ determines the input conductance of the converter, G_{in}, and thus the amplitude of the sinusoidally shaped input current. To design an output voltage controller the transfer function of the input current to the output voltage has to be determined. Contrary to the determination of $G_{\mathrm{id}}(s)$, the applied small-signal approximation is done with respect to the mains peroid (for the input current control the approximation is applied with respect to a switch-

ing cycle).

The output power of the converter, represented with the RMS values of input voltage and input current, is given with

$$P_{\mathrm{out}}(t) = \eta \cdot V_{\mathrm{n1,rms}}(t) \cdot I_{\mathrm{in,rms}}(t). \tag{4.99}$$

Applying the linearization to (4.99) yields

$$\bar{P}_{\mathrm{out}} + \hat{P}_{\mathrm{out}}(t) = \eta \cdot (\bar{V}_{\mathrm{n1,rms}} + \hat{V}_{\mathrm{n1,rms}}(t)) \cdot (\bar{I}_{\mathrm{in,rms}} + \hat{I}_{\mathrm{in,rms}}(t)). \tag{4.100}$$

Since the averaging is done with respect to the mains period, the quiescent values of the output power, the output voltage, and the input voltage are

$$\bar{P}_{\mathrm{out}} = P_{\mathrm{out}}, \quad \bar{V}_{\mathrm{out}} = V_{\mathrm{out}}, \text{ and } \quad \bar{V}_{\mathrm{n1,rms}} = V_{\mathrm{n}}.$$

With it, the steady-state solution is $P_{\mathrm{out}} = \eta \cdot V_{\mathrm{n}} \cdot \bar{I}_{\mathrm{in,rms}}$ and the small-signal approximation is given by

$$\hat{P}_{\mathrm{out}}(t) = \eta \cdot V_{\mathrm{n}} \cdot \hat{I}_{\mathrm{in,rms}}(t). \tag{4.101}$$

In (4.101) it is assumed that the RMS value of the input voltage has no small-signal component $\hat{v}_{\mathrm{n1,rms}}$ but is constant.

The output power averaged over a mains period can be defined at the output of the converter:

$$\bar{P}_{\mathrm{out}}(t) = \bar{V}_{\mathrm{out}}(t) \cdot \bar{I}_{\mathrm{S}}(t), \tag{4.102}$$

whereas $\bar{I}_{\mathrm{S}}(t)$ is the secondary current averaged over a mains period. The small-signal model is defined with

$$\hat{P}_{\mathrm{out}}(t) \approx V_{\mathrm{out}} \cdot \hat{I}_{\mathrm{S}}(t) + \hat{V}_{\mathrm{out}}(t) \cdot \bar{I}_{\mathrm{S}}. \tag{4.103}$$

Considering **Fig. 4.22**, the current $\hat{I}_{\mathrm{C}}$ is determined by

$$\hat{I}_{\mathrm{C}}(t) = \hat{I}_{\mathrm{S}}(t) - \frac{\hat{V}_{\mathrm{out}}(t)}{R_{\mathrm{L}}} = s\, C_{\mathrm{out}} \cdot \hat{V}_{\mathrm{out}}(t); \tag{4.104}$$

this results in

$$\hat{I}_{\mathrm{S}}(s) = \left(s\, C_{\mathrm{out}} + \frac{1}{R_{\mathrm{L}}} \right) \cdot \hat{V}_{\mathrm{out}}(s). \tag{4.105}$$

Taking into account that (4.101) and (4.103) are equal for a mains period and with substitution of (4.105) yields the desired transfer function:

$$G_{\mathrm{vi}}(s) = \frac{\hat{V}_{\mathrm{out}}(s)}{\hat{I}_{\mathrm{in,rms}}(s)} = \eta \cdot \frac{V_{\mathrm{n}}}{V_{\mathrm{out}}} \cdot \frac{R_{\mathrm{L}}}{2 + s\, C_{\mathrm{out}} \cdot R_{\mathrm{L}}}, \tag{4.106}$$

considering

$$I_{\mathrm{out}} = \bar{I}_{\mathrm{S}} = \frac{V_{\mathrm{out}}}{R_{\mathrm{L}}}. \tag{4.107}$$

4.5.3 Design of the feedback control

Input current controller

With the converter plant being known, a PI current controller can be designed [87]. The bandwidth of the current control loop is chosen to be $f_{\mathrm{I}} = 2\,\mathrm{kHz}$ which is a reasonable trade-off between good control dynamics and stability, i.e. achievable phase margin. The symmetrical optimum controller design method has been applied to obtain the control parameters [113]. The control parameters resulting for the PI controller,

$$K_{\mathrm{I}}(s) = \frac{d_{\mathrm{fb}}(s)}{\Delta i_{\mathrm{n1}}(s)} = K_{\mathrm{Pi}} \cdot \frac{1 + s \cdot T_{\mathrm{Ni}}}{s \cdot T_{\mathrm{Ni}}}, \tag{4.108}$$

are $K_{\mathrm{Pi}} = 0.004\,\mathrm{A}^{-1}$ and $T_{\mathrm{Ni}} = 10\,\mathrm{ms}$, which results in the closed loop step response given in **Fig. 4.25**. The phase margin for this design is 75.5° which ensures stability for all other operating points as well.

Output voltage controller

The cut-off frequency of the output voltage control loop, f_{V}, has to be well below twice the mains frequency as otherwise the input current would be distorted. Therefore, f_{V} is set to $f_{\mathrm{V}} = 2f_{\mathrm{m}}/40 = 2.5\,\mathrm{Hz}$. Due to the slow control dynamics the time delay imposed by the current control loop is neglectable. The parameters of the applied PI control are determined by compensation of the plant dynamics, i.e. compensation of the denominator in (4.106), and to obtain the desired bandwidth. Thus, the controller is

$$K_{\mathrm{V}}(s) = \frac{G_{\mathrm{in}}(s)}{\Delta v(s)} = K_{\mathrm{Pv}} \cdot \frac{1 + s \cdot T_{\mathrm{Nv}}}{s \cdot T_{\mathrm{Nv}}}, \tag{4.109}$$

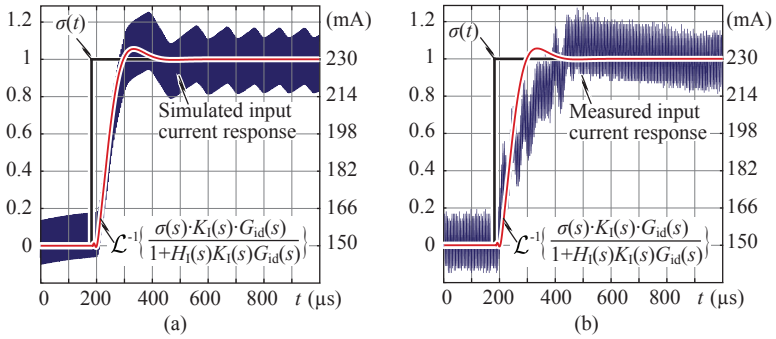


Fig. 4.25: (a) Calculated and simulated response of the closed-loop current control to a step $\sigma(t) = \mathscr{L}^{-1}\{1/s\}$. (b) Calculated and measured result of input current response. For both cases the reference current is changed from 150 mA to 230 mA. The difference between the simulation and the measurement is due to parameter tolerances and because the small-signal circuit synthesis is based on a simplified and lossless model.

with $K_{\mathrm{Pv}} = 0.0031\,\mathrm{S/V}$ and $T_{\mathrm{Nv}} = 6.82\,\mathrm{ms}$. **Fig. 4.26** (a) depicts the Bode plots of the plant $G_{\mathrm{vi}}(s)$, the PI compensator $K_{\mathrm{V}}(s)$, and the open-loop transfer function; as can be seen the desired bandwidth of 2.5 Hz is obtained. This results in a slow step response presented in **Fig. 4.26** (b).

4.5.4 Feedforward control

In a single-phase PFC rectifier system, the operating point of the small-signal model varies over the mains period. Thus, the feedback control has to compensate the control error Δi while the operating point is changing according to the sinusoidally-shaped input voltage v_{n1}.

In order to ensure a low control error a feedforward compensator can be applied, cf. [113], which presets the operating point with respect to the input voltage v_{n1},

$$d_{\mathrm{ff}}(v_{\mathrm{n1}}) = \frac{\alpha \cdot nV_{\mathrm{out,ref}}}{v_{\mathrm{n1}} + \alpha \cdot nV_{\mathrm{out,ref}}}. \tag{4.110}$$

The duty cycle d is the sum of the feedforward and the feedback value,

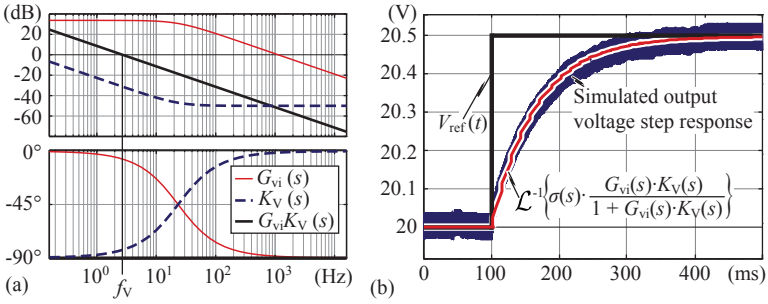


Fig. 4.26: (a) Bode plot of output voltage transfer function $G_{\mathrm{vi}}(s)$, the output voltage compensator $K_{\mathrm{V}}(s)$, and the open-loop system $G_{\mathrm{vi}}\,K_{\mathrm{V}}(s)$. (b) Calculated and simulated response of the closed-loop output voltage control loop to a output reference step from $V_{\mathrm{ref}} = 20\,\mathrm{V}$ to $20.5\,\mathrm{V}$.

cf. **Fig. 4.21** (b)

$$d = d_{\mathrm{ff}} + d_{\mathrm{fb}}. \tag{4.111}$$

4.5.5 Adjustment of the switching frequency

The switching frequency f_{S} is varied with respect to the input voltage v_{n1} according to

$$f_{\mathrm{S}}(v_{\mathrm{n1}}) = \frac{v_{\mathrm{n1}}^2}{2\cdot\alpha\,L_{\mathrm{M}}}\cdot\frac{\eta\cdot d^2}{P_{\mathrm{out}}\cdot(1-\cos(2\,\omega_{\mathrm{m}}t))}, \tag{4.112}$$

where

$$d(v_{\mathrm{n1}}) = \frac{\alpha\cdot n\,V_{\mathrm{out,ref}}}{v_{\mathrm{n1}}+\alpha\cdot n\,V_{\mathrm{out,ref}}} \qquad \text{and} \qquad \omega_{\mathrm{m}}t = \arcsin\frac{v_{\mathrm{n1}}}{\hat{V}_{\mathrm{n1}}} \tag{4.113}$$

have to be substituted into (4.112). In the DSP the relation between v_{n1} and f_{S} is implemented using a look-up table. This results in a low computational effort for the DSP compared to an analytical function.

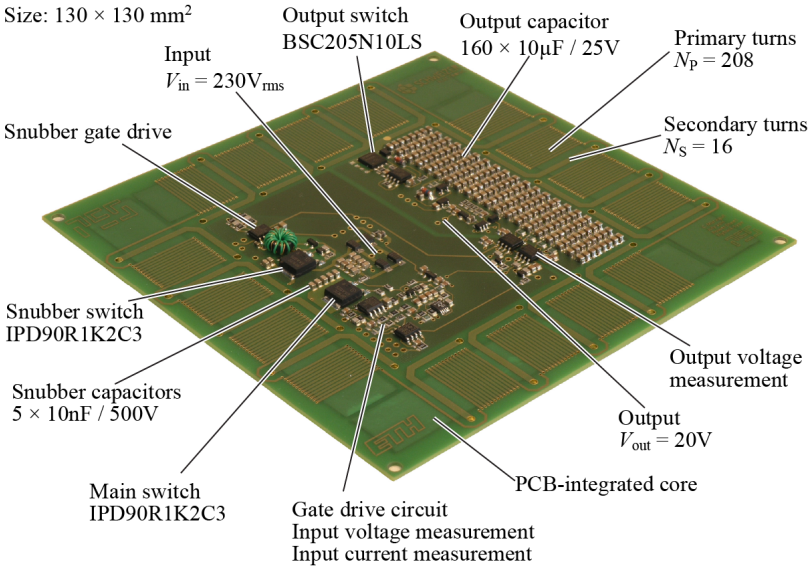


Fig. 4.27: Prototype of the flyback-type *Power Sheet* with PCB-integrated flyback transformer.

4.6 Experimental results

4.6.1 Prototype

Based on the design procedure presented in Section 4.4, a prototype of a single-phase flyback-type PFC rectifier has been realized. **Fig. 4.27** depicts the converter which has the size of $130 \times 130\,\mathrm{mm}^2$ and a power rating of $P_{\mathrm{out}} = 38\,\mathrm{W}$. The core of the flyback transformer is integrated into the PCB which results in a 1 mm thin transformer. The design of the flyback transformer is detailed in Chapter 5. All other components are conventional SMD chips which could also be embedded into the PCB. However, in order to test the circuit and measure voltages and currents the discrete setup has been preferred.

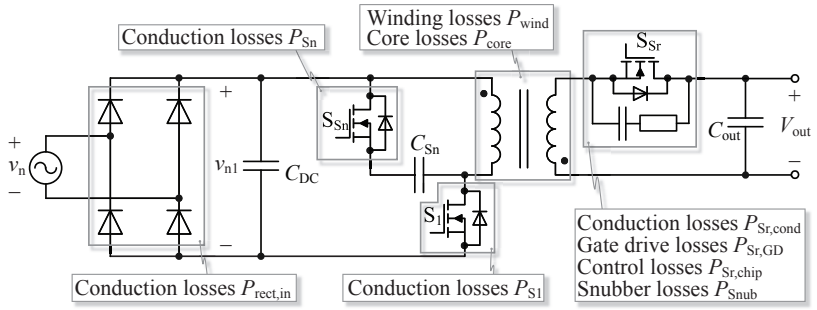


Fig. 4.28: Considered losses of the converter.

4.6.2 DC-DC operation

In order to validate the design process the loss contribution of each component is calculated in the analytical models and compared to simulated and measured results. **Fig. 4.28** indicates the considered losses of the converter:

- Conduction losses in the input diode bridge $P_{\mathrm{rect,in}}$,
- Conduction losses in the main switch S_1, P_{S1},
- Conduction losses in the snubber switch S_{Sn}, P_{Sn},
- Winding losses in the flyback transformer P_{wind},
- Core losses of the flyback transformer P_{core},
- Conduction losses in the output rectifier switch S_{Sr}, $P_{\mathrm{Sr,cond}}$,
- Gate driver losses in the output rectifier $P_{\mathrm{Sr,GD}}$,
- Losses of the gate driver control chip $P_{\mathrm{Sr,chip}}$,
- Losses in the *RC*-snubber circuit of S_{Sr}, P_{Snub}[6].

The soft-switching capability of the converter results in low switching losses and therefore, they are neglected in the loss balance. The

[6] The implemented prototype needs a snubber circuit over the output switch $\mathrm{S}_{\mathrm{out}}$ due to occuring voltage spikes caused by the reverse recovery charge of the body diode of $\mathrm{S}_{\mathrm{out}}$. The design of the snubber circuit is detailed in Appendix C.

prototype shown in **Fig. 4.27** is connected to a DSP board which controls the converter. This control board and the gate drives of S_{Sn} and S_{S1} are externally powered ($P_{aux,tot} = 1.5\,W$) and thus these losses do not show up in the loss balance. Furthermore, losses in the capacitors C_{DC}, C_{Sn}, and C_{out} are negligible as paralleled ceramic capacitors with a low ESR are applied.

Tab. 4.8 lists the calculated and simulated results for an input voltage of $v_{n1} = 230\,V$ and an output power of $P_{out} = 38\,W$. Compared to the simplified model, the analytical model yields a more accurate description of the converter currents. Nonetheless, for the design of the converter the simplified model offers an efficient and direct way to determine each component with reasonable accuracy.

Due to the rather low converter efficiency, however, a considerable power is required to cover the losses from input to output and this additional energy is not considered in the calculation model. **Fig. 4.29** (a) shows a comparison between calculated and measured primary current i_P and secondary current i'_S (primary referred). The calculated currents consist of piecewise linear and sinusoidal waveforms whereas the measurement currents are influenced by lossy and parasitic components in the converter. In particular, the winding capacitance causes the steep current drop in the measured primary current i_P and the steep current increase in the secondary current i'_S, cf. $t = 2\,\mu s$ and $t = 4\,\mu s$, which are not taken into account by the analytical model.

An analytical estimation of the converter which includes the parasitics, e.g. the winding resistance, core losses, and conduction resistances of the switches, is difficult to achieve due to the numerical effort. Therefore, a simulation which considers all loss elements and the transformer's capacitances has been applied and the results fit very well to measurement results as can be seen in **Tab. 4.8** and in **Fig. 4.29** (b). The snubber losses in the simulation are $P_{Snub} = 1\,W$. This value has been measured and is applied to the simulation in order to obtain an accurate simulation result. The impact of the winding capacitance is also included in the simulation.

Fig. 4.30 presents the pie charts of the loss distribution for each model. As can be seen, the core losses have a major impact on the total losses. Therefore, an increase of the converter's efficiency requires a reduction of the core losses which can be achieved with a more efficient (but larger) transformer design according to the Pareto Front. This issue is adressed in Section 5.3.

Tab. 4.8: Comparison between the simplified model, the analytical model, simulation results, and measurements for the *Power Sheet* operated as DC-DC converter.

$v_{n1} = 230\,V$	$V_{out} = 20\,V$		$P_{out} = 38\,W$	
	Simplified model	**Analytical model**	**Simulation**	**Measurement**
I_P	378 mA	456 mA	455 mA	430 mA
I_S	3.28 A	3.4 A	3.42 A	3.2 A
I_{Sn}	252 mA	318 mA	324 mA	
I_{S1}	281 mA	328 mA	347 mA	
P_{core}	5.57 W	6.5 W	6.6 W	
P_{wind}	1.96 W	2.3 W	2.9 W	
P_{S1}	115 mW	156 mW	157 mW	
P_{Sn}	80 mW	127 mW	131 mW	
$P_{Sr,cond}$	270 mW	285 mW	292 mW	
$P_{Sr,GD}$	88 mW	95 mW	90 mW	
$P_{Sr,chip}$	270 mW	270 mW	270 mW	
P_{Snub}	570 mW	560 mW	1.0 W	
$P_{rect,in}$	260 mW	280 mW	260 mW	
$\sum P_{loss}$	9.18 W	10.66 W	11.80 W	12.25 W
η_{calc}	80.5 %	78.1 %	76.3 %	75.2 %

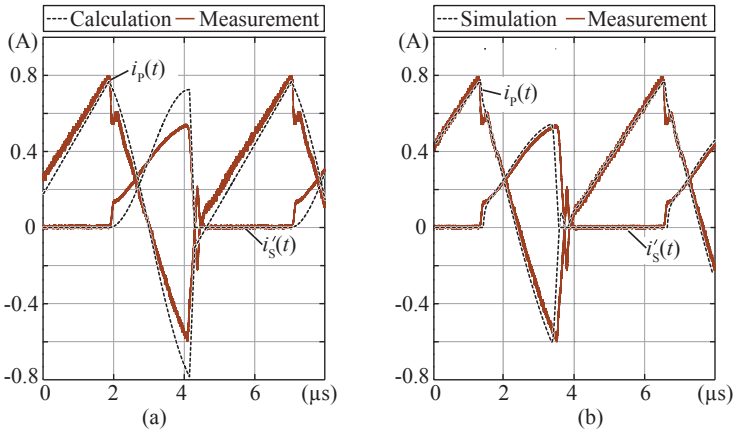


Fig. 4.29: (a) Comparison between calculated and measured transformer currents, i_P and i'_S. (b) Comparison between simulation and measurement of the transformer currents. The *Power Sheet* operates as DC-DC converter at $v_{n1} = 230\,V$, $V_{out} = 20\,V$, $P_{out} = 38\,W$.

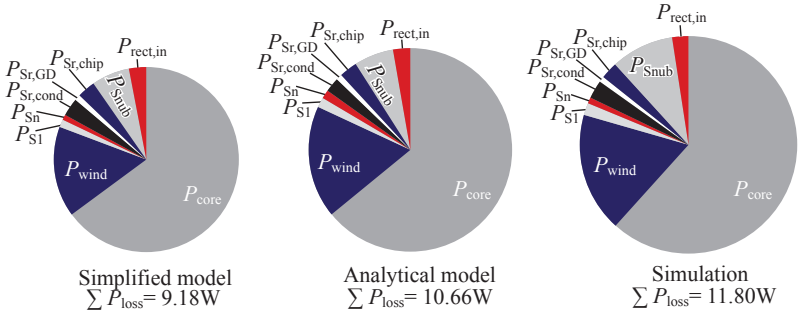


Fig. 4.30: Pie chart of the loss distribution of the *Power Sheet* for different loss models.

4.6.3 AC-DC operation

Fig. 4.31 illustrates the converter operation in AC-DC mode at nominal input voltage of $V_n = 230\,V$ and at full output power $P_{out} = 38\,W$. During the zero crossing of the input voltage v_n the modulation is turned OFF as the input current i_n cannot be shaped sinusoidally because the switching frequency is limited to 320 kHz. Besides, at low input volt-

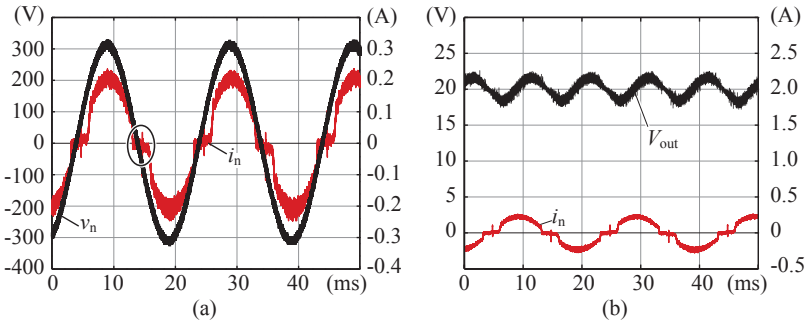


Fig. 4.31: (a) Measured mains voltage and input current of the *Power Sheet* operated as AC-DC converter at $V_n = 230\,V$, $V_{out} = 20\,V$, and at full power of $P_{out} = 38\,W$. (b) Measured output voltage V_{out} and input current i_n.

ages the duty cycle would converge to one, cf. (4.50), and interlocking delays as well as the interval to recycle the leakage energy could not be maintained. As a consequence, the duty cycle has an upper limit of 0.8. The current spikes indicated in **Fig. 4.31** (a) originate from the integral controller action.

The converter achieves a power factor of PF = 98.4 % and an efficiency of $\eta = 76.8\,\%$ at full power. The dependency of the efficiency on the output power is illustrated in **Fig. 4.32**. Publications on galvanically isolated single-phase PFC rectifiers [107, 114–118] report efficiencies of typically $\eta = 80 \ldots 90\,\%$. Compared to these values the achieved efficiency is lower. This is the prize to be paid for the ultra-flat realization of the converter.

4.7 Conclusion

In this chapter the design of a flyback-type PFC rectifier is detailed. The topology is considered to be most appropriate for a single-stage architecture because of its simple circuitry which basically only requires two active switches and the simple control structure needed to achieve the PFC functionality and the output voltage control. Besides, contrary to alternative topologies, only one magnetic element is required. Moreover, the high voltage DC link capacitor which is difficult to integrate

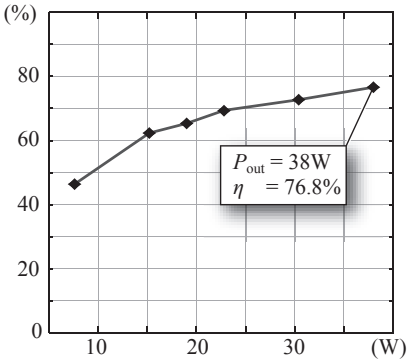


Fig. 4.32: Measured efficiency as a function of the output power P_{out}.

into the PCB only needs a very small capacitance value ($C_{\text{DC}} = 100\,\text{nF}$).

The PCB integration of the flyback transformer implies a considerable leakage inductance. Although an interleaved winding configuration reduces the leakage flux, the spacial dimensions of the transformer still impose a high leakage inductance. Reasonable values of the leakage coefficient can only be obtained if the converter is divided into several subsystems. This also allows for a distributed heat dissipation and utilizes the excellent heat removal capabilities of the ultra-flat shape.

The energy stored in the large leakage inductance needs to be recycled as otherwise the efficiency of the converter would be unacceptably low. An active snubber circuit is considered which not only recycles the leakage energy but also allows for a modulation which enables ZVS of the power switch and the snubber switch.

The design of each component is done based on a simplified model which allows for a direct and straight-forward way to calculate the currents and the voltages of the converter. In order to verify the simplifications made, an analytical model is also presented which calculates the converter's waveforms with an numerical solver. A comparison between the two models show that the simplified model underestimates the currents but is still accurate enough to design the components if a reasonable safety margin is included.

The crucial element of the converter is the flyback transformer. A thorough description of the flyback transformer design is given in Section 5.3. Based on the present results a flyback transformer is realized

with a calculated efficiency of $\eta_{\mathrm{tr}} = 84.3\,\%$.

Measurement results of the flyback converter are presented for DC-DC and AC-DC operation. Since the calculation models do not account for parasitic effects of the components the analytical waveforms and the measurement results differ. In order to verify the theoretical analysis, a simulation model including the parasitic components of the converter has been implemented and the results agree well with the measurements.

In PFC operation, the *Power Sheet* employing the designed PCB-integrated transformer achieves an efficiency of $\eta = 76.8\,\%$ and a power factor $\mathrm{PF} = 98.4\,\%$. The balance of losses illustrates that the core losses of the transformer have major impact on the overall losses. A significant increase of efficiency can only be achieved if the core losses are reduced. Thus, the PCB-integrated flyback transformer determines the achievable efficiency for the PFC rectifier and truly identifies the performance limit resulting from the extreme converter shape factor.

5

Design of PCB-integrated magnetic components

In Chapter 1 it has been pointed out that the realization of PCB-integrated magnetic components is a major challenge to realize an ultra-flat converter system with a targeted height of 1 mm. In this chapter, several integration methods already presented in the literature are briefly introduced. Based on the state-of-art of ultra-flat magnetic components and on the applicability of core materials to the ultra-flat realization, an integration method is presented whereas the core is embedded into the PCB and the windings are realized as track and vias. The chaper details the specific implications imposed by the PCB-integration and introduces a multi-objective optimization procedure with respect to the efficiency and the area-related power density of the magnetic component. The theoretical results are validated with measurements on a PCB-integrated flyback transformer designed for a PFC rectifier system with an output power of 38 W.

5.1 Introduction

In an initial step for the realization of ultra-flat inductive components, power SMD inductors could be considered. However, the total height of the flattest available power SMD inductors is roughly 3 mm [2, 60]. As an alternative, planar magnetic cores and a multilayer PCB could be used to realize ultra-flat magnetic components [119]. Still, the realization of the required ultra-flat magnetic components is unfeasible, since the minimal total height of available planar cores is 5 mm, e.g.

ELP 14/3.5/5 by [43].

In a different approach, flat magnetic components are implemented with PCB inductors consisting of spiral windings on several layers, which are covered with magnetic material on top and bottom of the PCB [120]. Based on this integration method, a transformer for a 60 W power converter is realized in [38] (PCB thickness: 4 mm). The implemented core employs a ferrite polymer compound with a low relative permeability (typ. $\mu_r = 10 \ldots 20$); therefore, a large area is required in order to obtain the desired inductance value. Accordingly, this technique facilitates the realization of thin inductors, however, the energy density of the inductors is low due to the inherently large air gap length imposed by the PCB.

A reduced air gap length and an increased energy density is achieved if the core of the magnetic component is integrated into the PCB. In [121], the PCB integration of highly permeable magnetic materials ($Ni_{80}Fe_{20}$) is discussed; PCB-integrated inductors with a thickness of 1.3 mm have been implemented and are used as inductors for a 1.5 W buck converter. A comparison between closed core structures and air inductors is given and it is shown that closed core assemblies provide the highest inductance and efficiency values per area. Since the employed magnetic cores are very thin ($10 - 20\,\mu m$), a large area is required to avoid saturation for a given current and to achieve a required inductance value. Furthermore, in [61], the eddy current losses in the magnetic cores are large due to the selected arrangement of the winding and the core.

[62] presents a comprehensive review of integrated magnetics for power converters and describes several integration methods for inductors. However, the discussion focuses on HF ($1\,MHz - 100\,MHz$) point-of-load buck converters, e.g. for mobile phones, or multicore processors, with high current and low voltage capability. For an AC-DC rectifier where the isolation between the windings is crucial and the switching frequency is typically limited below 1 MHz these integrated inductors are not applicable.

In [122], a ferrite core (3F3 by Ferroxcube [123]) is integrated into a PCB and applied to a buck converter (3.3 V/20 A). The inductance value is 1 µH and the integrated core has a thickness of 2 mm. Ferrite materials feature low core losses but they are very brittle and as the required magnetic cores are extremely thin (< 1 mm) the production of ferrite cores is very difficult. Therefore, ferrites are not considered as

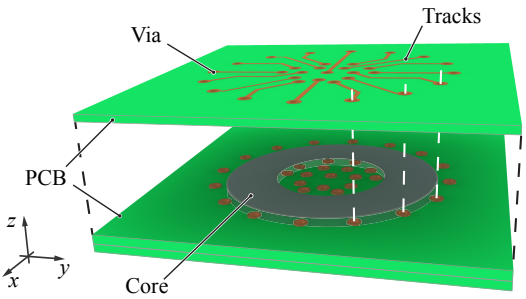


Fig. 5.1: PCB-integrated core; windings are realized with PCB tracks and vias.

an appropriate choice. Amorphous and nanocrystalline soft magnetic materials remain, which enable a simpler manufacturing of ultra-thin cores compared to ferrite cores.

[124] presents the realization of a 200 W Dc-Dc converter with PCB-integrated transformer. **Fig. 5.1** illustrates the principle of the PCB-integrated core ($h = 1.6\,\mathrm{mm}$) which is made of amorphous material. The modeling of the transformer, however, only accounts for eddy current losses and the geometry is restricted to toroidal cores.

This chapter investigates the applicability of nanocrystalline and amorphous soft magnetic materials for the realization of ultra-flat magnetic components with almost arbitrary shape. This is illustrated on the example of the high frequency (HF) transformer of a single-phase flyback-type PFC rectifier with a total converter height of 1 mm.

The design of a PCB-integrated core differs from the design of conventionally shaped cores. Therefore, Section 5.2 discusses the specific requirements that need to be considered in the design and Section 5.3 subsequently presents the optimization of ultra-flat magnetic components with respect to minimum total footprint area and/or minimum losses. The results of the multi-objective optimization are presented as η-α-Pareto Front, which shows the trade-off between the area-related power density α (W/cm^2) and the efficiency η for a given magnetic core material.
Section 5.4 presents measurement results obtained from a selected flyback transformer design that are used to verify the theoretical considerations.

5.2 Design considerations for ultra-flat magnetic components

The PCB-integration of the core implies several specific properties and restrictions on the design of an inductor or transformer. This section discusses these implications required for the multi-objective design procedure presented in Section 5.3 and is divided into the following subsections and/or main objectives:

5.2.1 summarizes the properties of the considered magnetic materials and discusses possible core constructions.

5.2.2 emphasizes the importance of the isolation between the core tapes as otherwise the core losses increase vastly.

5.2.3 focuses on the anisotropy of nanocrystalline and amorphous materials.

5.2.4 proposes a limit of the power loss per area in order to restrict the core temperature.

5.2.5 presents an accurate reluctance model required for the inductance calculation of specific core geometries.

5.2.6 details an interleaved winding arrangement for transformer applications.

5.2.1 Core geometry and materials

In order to integrate an inductor or a transformer into a PCB, the setup of the core has to be taken into consideration. There are basically two possible constructions for PCB-integrated magnetics employing nanocrystalline and amorphous materials. The core can either be composed of a stack of thin magnetic foils, cf. **Fig. 5.2** (a), or it consists of a thin toroidally wound magnetic foil, cf. **Fig. 5.2** (b). However, an air gap, which offers the designer an additional degree of freedom, can only be easily realized for stacked assemblies as toroidally wound cores would fall apart. Only with a sophisticated core attachment inside the PCB an air gap can be implemented. The integration of the core into

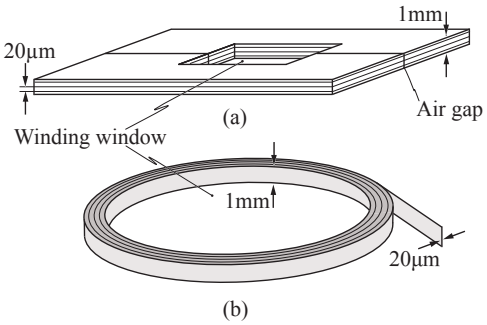


Fig. 5.2: Core configurations applicable to PCB-integrated transformers and inductors: (a) Two C-shaped core halves with stacked magnetic foils, and (b) toroidal core with a wound magnetic foil; in the latter setup (b) an air gap can only be inserted with considerable effort after embedding the core into the PCB.

the PCB requires additional manufacturing efforts compared to standard PCB production. However, the technology is already available, e.g. by [125], and hence not in the scope of this thesis.

As mentioned in the introduction, nanocrystalline and amorphous materials are beneficial as ultra-thin tapes of these materials are available that are suitable to realize the geometries in **Fig. 5.2**. These tapes feature a thickness of 20 µm or less and are applicable to HF applications. However, the width of the tapes, a, cf. **Fig. 5.3**, is limited due to manufacturing reasons. This is a limitation in the design process of an integrated inductor and causes the cores to be either composed of several core legs or of a monolithic core with rather rectangular, cf. **Fig. 5.4**, than quadratic shape, cf. **Fig. 5.3** (b), as otherwise the winding window, cf. **Fig. 5.3** (a), would be too small to provide space for the windings.

Nanocrystalline materials are typically annealed in order to feature specified magnetic properties. However, after the annealing process these materials are very brittle, which makes a further mechanical treatment impossible. On the contrary, amorphous materials remain processable after being annealed. Amorphous materials are thus considered in this chapter as they are beneficial for prototyping whereas nanocrystalline cores need to be produced by the material manufacturer.

In this thesis the materials VITROVAC 6155 F [126] and 2714A [127]

are investigated. Both materials are Cobald-based alloys whereas VITROVAC 6155F is field-annealed contrary to 2714A which is no-field annealed. Amorphous cores are typically employed for HF transformer and inductor applications and are available by various manufacturers [45, 126–129].

5.2.2 Core lamination

Lamination of magnetic cores is widely used for high frequency transformers and inductors as eddy currents and thus eddy current induced losses in the core material can be reduced. Therefore, the isolation between the magnetic foils is crucial to achieve low core losses in HF applications. Amorphous materials feature an inherent oxidation layer which reduces the conductance between two foils. However, measurement results show that the isolation provided by the oxide layer is insufficient. Two prototypes have been built up where in the first one the magnetic foils are loosely embedded into the PCB and in the second one the core is tightly pressed into the PCB. It turns out that the losses increase with increasing pressure on the stack of foils (which increases the conductivity between the magnetic foils). The measurements have shown that the pressed setup generates three times higher losses than the loose realization ($\Delta B = 0.4\,\mathrm{T}$, $f_\mathrm{S} = 100\,\mathrm{kHz}$: $P_\mathrm{loose} = 8.9\,\mathrm{W}$, $P_\mathrm{tight} = 29.25\,\mathrm{W}$).

To increase the resistance between the magnetic foils either isolation tapes or isolation lacquer layers have to be employed. The addition of the isolation decreases the core filling factor k_fe which defines the ratio between the magnetically effective core cross-section area and the total cross-section of the core. This has to be considered in the design procedure. Throughout this chapter, the core foils are isolated using an isolation laquer in order to obtain minimal core losses while keeping the core filling factor high.

5.2.3 Core losses

An alternating magnetic flux in the core results in eddy current losses and hysteresis losses. A comparison between stacked and wound cores, cf. **Fig. 5.2**, however, shows that equal eddy current losses result for both configurations; the respective explanation is presented in Appendix A.

Hysteresis losses, however, show different behavior for both core configurations as nanocrystalline and amorphous materials are generally

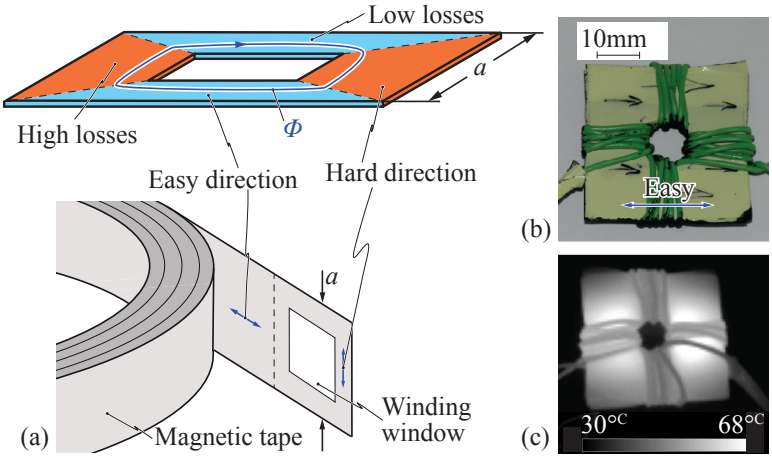


Fig. 5.3: (a) Magnetic sheets are cut out of a long band of magnetic foil. (b) A square inductor with a magnetic core formed by stacking 10 sheets (VITROVAC 6155F by VAC [126]) is shown. (c) The temperature rise in the hard direction is much higher compared to the preferential (easy) direction ($f_S = 100\,\text{kHz}$, $\Delta B = 1.5\,\text{T}$, $P_{loss} = 2.2\,\text{W}$).

anisotropic and there is a preferential (easy) and a hard direction of the foils. The terminology of easy and hard direction are chosen with regard to the power loss generation of each axis rather than the more physical interpretation presented e.g. in [130]. In toroidally wound cores the flux is always in the tangential and, therefore, easy direction, cf. **Fig. 5.3** (a). In magnetic cores consisting of a stack of magnetic foils, the flux is forced to penetrate into the hard direction as well. **Fig. 5.3** (a) shows that each sheet of the core is cut out of a magnetic tape and the winding window is considered in the middle. The magnetic flux Φ flows as indicated in **Fig. 5.3** (a) and higher losses in the hard direction have to be expected.

Fig. 5.3 (b) shows a square prototype inductor which consists of a stack of ten VITROVAC 6155F foils (each 20 µm thick) with a side length of 35 mm. **Fig. 5.3** (c) illustrates that a HF magnetic flux applied to the core results in different core losses for each direction; the temperature in the hard direction is higher compared to the easy direction.

It is therefore crucial that the increased losses in the hard direction are considered in the design of a PCB-integrated core. Otherwise, the

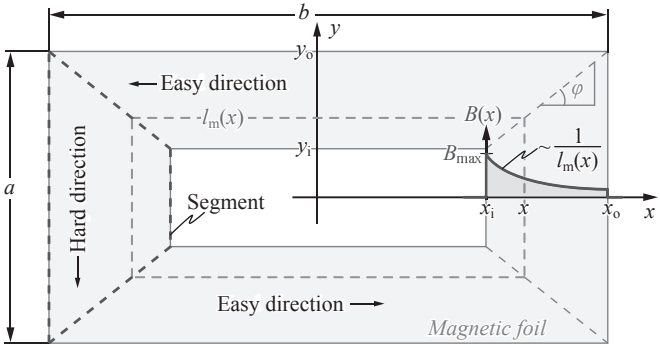


Fig. 5.4: Core geometry for the flux density calculation. To calculate the flux density and to determine the Steinmetz parameters for the hard direction a rectangular-shaped core without air gap is considered.

core could be thermally damaged. Since core loss data for the easy direction is generally provided by manufacturers the respective Steinmetz parameters (k_e, α_e, and β_e) can easily be extracted. Thus, in order to be able to estimate the total core losses, the Steinmetz parameters for the hard direction remain to be determined. For it, a segmentation of the core according to **Fig. 5.4** is assumed. The flux density in the core, $B(x)$, will decrease proportionally to the inverse of the magnetic length $l_m(x)$ whereas the maximum flux density B_{max} is at the inner border of the core (x_i or y_i).

Referring to Ampère's law and considering **Fig. 5.4**, the ratio of the flux density at the outer and the inner edge is

$$\frac{B(x = x_i)}{B(x = x_o)} = \frac{l_m(x = x_o)}{l_m(x = x_i)} = \frac{4 \cdot (x_o + y_o)}{4 \cdot (x_i + y_i)}. \tag{5.1}$$

With

$$\begin{aligned} l_m(x) &= 4 \cdot (x + y_i + (x - x_i) \cdot \tan\varphi) \\ &= 4 \cdot \left(x + y_i + (x - x_i) \cdot \frac{y_o - y_i}{x_o - x_i} \right) \end{aligned}$$

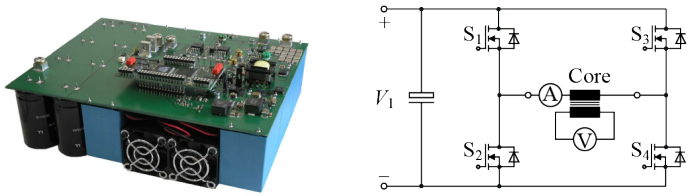


Fig. 5.5: (a) Photography and (b) circuit of the used core loss measurement system [131].

the flux density at an arbitrary position x can be determined and is thus

$$B(x) = B_{\max} \cdot \frac{x_\mathrm{i} + y_\mathrm{i}}{x + y_\mathrm{i} + (x - x_\mathrm{i}) \cdot \frac{y_\mathrm{o} - y_\mathrm{i}}{x_\mathrm{o} - x_\mathrm{i}}}. \tag{5.2}$$

The core losses can be calculated with the Steinmetz equation which has to be integrated over either an easy or a hard direction segment. For the two segments in hard direction the core losses are thus

$$P_\mathrm{v} = 2\, d_\mathrm{core}\, k_\mathrm{fe} \int_{x_\mathrm{i}}^{x_\mathrm{o}} \int_{-y_\mathrm{i}-(x-x_\mathrm{i})\tan\varphi}^{y_\mathrm{i}+(x-x_\mathrm{i})\tan\varphi} k_\mathrm{h} \cdot f_\mathrm{S}^{\alpha_\mathrm{h}} \left(\frac{\Delta B(x)}{2} \right)^{\beta_\mathrm{h}} \mathrm{d}y\, \mathrm{d}x, \tag{5.3}$$

with the core thickness d_core and the core filling factor k_fe. Equations similar to (5.2) and (5.3) can be determined for the easy direction, i.e. $\Delta B(y)$, in the same way.

With this analytical background, the Steinmetz parameters related to the hard direction can be extracted from measurement results. For it, the core losses P_core of a given core under test (CUT) are measured at a certain operating point (ΔB, f_S) using the core loss measurement system shown in **Fig. 5.5** [131]. The core losses are obtained by applying a HF current to the core and by measuring the induced voltage on an auxiliary winding. The time integral of the induced voltage is proportional to the magnetic flux density in the core and the applied current is proportional to the magnetic field. Thus, the core losses are extracted from the obtained hystersis curve.

The core losses in easy direction, P_easy, can be calculated by applying the known Steinmetz parameters and the geometry of the CUT to

Tab. 5.1: Estimation of the losses in hard direction based on core loss measurements and calculations for the core depicted in **Fig. 5.3** (b).

	$f_S = 200\,\text{kHz}$		
ΔB	0.2 T	0.4 T	0.6 T
Calculated P_{easy}, cf. (5.3)	0.05 W	0.20 W	0.47 W
Measured P_{core}, cf. [131]	0.55 W	1.76 W	3.27 W
$\Rightarrow P_{\text{hard}}$, cf. (5.4)	0.50 W	1.56 W	2.80 W

Tab. 5.2: Parameters of magnetic materials for integrated cores.

	a (mm)	B_{sat} (T)	ρ (kg/m^3)	Steinmetz parameters Easy (W/m^3)	Hard (W/m^3)
VITROVAC 6155F [126]	35	1.0	7920	$k_e = 0.0043$ $\alpha_e = 1.84$ $\beta_e = 2.04$	$k_h = 0.074$ $\alpha_h = 1.71$ $\beta_h = 1.64$
2714A [127]	50	0.57	7590	$k_e = 0.035$ $\alpha_e = 1.71$ $\beta_e = 1.91$	$k_h = 2.99$ $\alpha_h = 1.33$ $\beta_h = 2.24$

(5.3). The difference between P_{core} and P_{easy} are the losses in the hard direction parts,

$$P_{\text{hard}} = P_{\text{core}} - P_{\text{easy}}. \tag{5.4}$$

Tab. 5.1 presents the calculated and measured core losses for the CUT depicted in **Fig. 5.3** (b). In order to increase the accuracy of the Steinmetz parameter extraction, several square CUTs have been measured with different values of ΔB (0.2 T ... 1.8 T) and f_S (50 kHz ... 200 kHz). The obtained parameter sets (P_{hard}, ΔB, f_S, core geometry) are then applied to (5.3) which gives a set of equations. Finally, this over-determined set of equations is solved for the Steinmetz parameters (k_h, α_h, and β_h) using a least-square algorithm.

Fig. 5.6 presents a comparison between the amorphous materials VITROVAC 6155F [126] and 2714A [127] based on the extracted Stein-

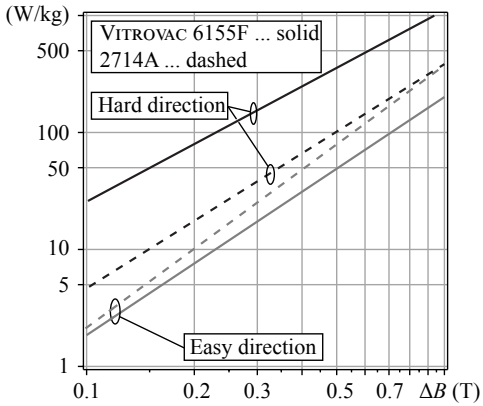


Fig. 5.6: Comparison of core losses between VITROVAC 6155F [126] and 2714A [127] at $f_S = 100\,\text{kHz}$. VITROVAC 6155F features low core losses in the easy direction whereas 2714A is better regarding the losses in the hard direction.

metz parameters listed in **Tab. 5.2**. It is shown that VITROVAC 6155F has very low losses in the easy direction but high losses in the hard direction. 2714A exhibits a more isotropic behavior. For a quadratically shaped core, 2714A is beneficial as with VITROVAC 6155F the losses in the hard direction would dominate the core losses. VITROVAC 6155F is the material of choice if long core geometries are required as there 2714A suffers from comparably high losses in the easy direction. **Fig. 5.7** shows the losses in each direction for both materials whereas the length of the core x_o, cf. **Fig. 5.4**, is varied while the width of a rod $(x_o - x_i)$ is kept constant. **Fig. 5.7** points out that the losses in the hard direction keep constant while the losses in the easy direction increase due to the increased volume. Up to a core length of $x_o = 62\,\text{mm}$ 2714A would be the material of choice and above VITROVAC 6155F features lower losses.

5.2.4 Core loss per area limitation

For PCB-integrated magnetic components thermal issues are important as the generated heat has to be transferred through the PCB to the ambient. In order to keep the core temperatures within reasonable limits a maximum power loss per area, p_{loss}, has to be specified. Considering the area related Steinmetz equation

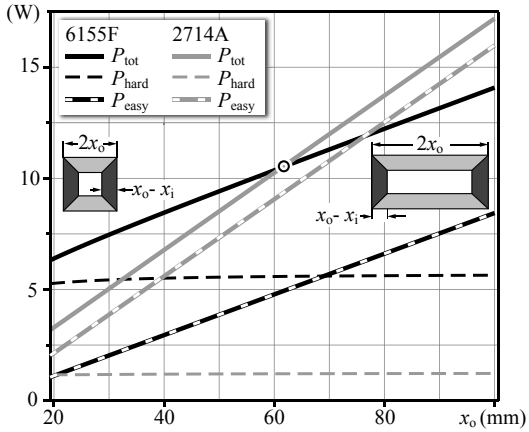


Fig. 5.7: Comparison between the losses in 2714A and VITROVAC 6155F. As can be seen for rectangular-shaped cores with a large x_o, 6155F exhibit lower losses whereas for quadratic cores 2714A is beneficial. The point where 6155F becomes better is indicated in the figure (Parameters: $d_{core} = 0.8\,mm$, $x_i = x_o - 11.8\,mm$, $y_i = 6.5\,mm$, $y_o = 17.5\,mm$, $f_S = 160\,kHz$, $\Delta B = 0.8\,T$).

$$p_{loss} = k_{fe} \cdot d_{core} \cdot k(H_{dc}) \cdot f_S^{\alpha} \cdot \left(\frac{\Delta B}{2}\right)^{\beta(H_{dc})} \quad (W/m^2), \tag{5.5}$$

the maximum allowable flux density swing ΔB can be determined at a certain frequency f_S and for a chosen material which ensures the p_{loss} limitation. In (5.5) the impact of a DC offset H_{dc} can also be considered [83]. However, for the considered materials (VITROVAC 6155F and 2714A), measurement results show almost no impact of the DC offset. With negligible impact of H_{dc} on p_{loss}, the closed form solution for ΔB is

$$\Delta B = 2 \cdot \left(\frac{p_{loss}}{k_{fe} \cdot d_{core} \cdot k \cdot f_S^{\alpha}}\right)^{1/\beta}. \tag{5.6}$$

Fig. 5.8 illustrates the calculation result of (5.6) for VITROVAC 6155F in easy direction; for a frequency of $f_S = 160\,kHz$ and a power loss per area of $p_{loss} = 0.33\,W/cm^2$ the flux density swing ΔB

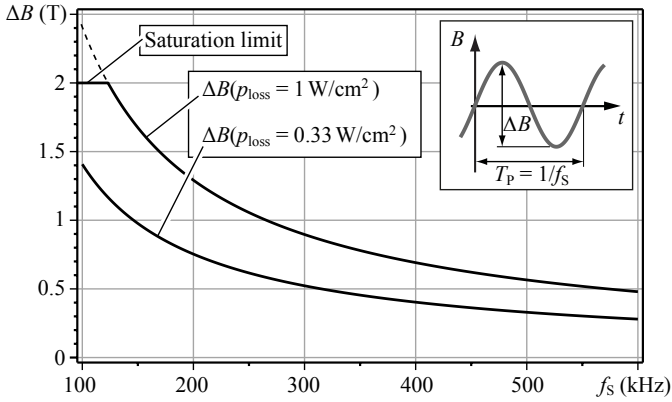


Fig. 5.8: Allowable ΔB for a specified power loss per area p_{loss} of a 1 mm thick core without DC offset of B (Material: VITROVAC 6155F, easy direction). Considering a DC offset of B changes the saturation limit, however, the losses are almost offset independent for the considered material.

must not exceed 920 mT. In the proposed design procedure the flux density is thus limited to the minimum of either ΔB or the saturation flux density B_{sat}. Therefore, the geometry of the core has to be designed to keep the maximum flux density within this limit for a given flux value.

A reasonable value for the power loss per area, p_{loss}, is obtained using measurements whereas core losses are generated by proper excitation of the core and the temperature on the PCB is measured using an infrared camera. **Fig. 5.9** (a) shows the measurement setup and **Fig. 5.9** (b) presents the resulting temperatures for given power losses per area, p_{loss}.

As the glass transition temperature for FR4 is 135 °C [132], the design procedure presented in Section 5.3 is performed with conservative value of $p_{\text{loss}} = 0.3\,\text{W/cm}^2$ which results in an expected temperature of $T_{\text{PCB}} = 62\,°\text{C}$ at 40 °C ambient temperature as specified in **Tab. 1.2**.

5.2.5 Reluctance model

The calculation of the desired inductance value of a PCB-integrated magnetic component requires the determination of the air gap length

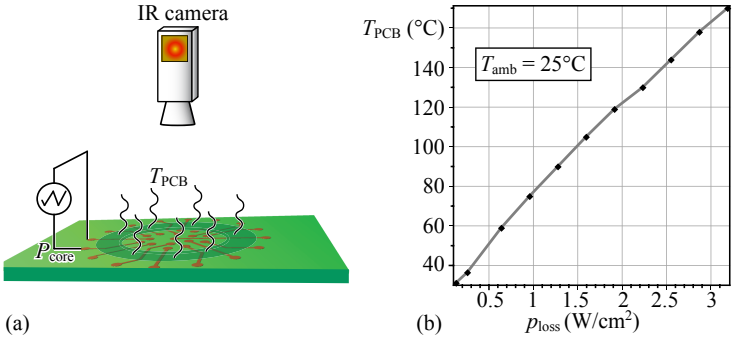


Fig. 5.9: (a) Setup of the thermal measurement for PCB-integrated cores. The measurement system presented in [83] has been applied to generate a core excitation and/or corresponding core losses. (b) Resulting temperatures for given power losses per area, p_{loss}.

based on the known core reluctance. Depending on the shape and the size of the PCB-integrated core, the total core reluctance cannot be assumed to be lumped but rather consists of a mesh of reluctances. In order to be able to consider arbitrary shapes of PCB-integrated cores, an appropriate reluctance model is required to determine the air gap length and thus to adjust the inductance value.

For monolithic or two-parts core configurations, the length of the core, b, cf. **Fig. 5.10** (a), is determined by the required winding window size because the width of the magnetic tape, a, is limited. **Fig. 5.10** (a) shows a typical two-parts setup where the windings are divided into n_{w} packages as this allows an interleaving with a secondary winding for transformer applications where a low leakage flux between the windings is crucial.

For $b \gg a$, the reluctance between the horizontal branches, the window reluctance $\mathcal{R}_{\sigma}$, is not negligible. Furthermore, due to the ultra-flat core, the fringing of the flux in the air gap l_{air} and between the horizontal rods is vastly decreasing the reluctances $\mathcal{R}_{\mathrm{air}}$ and $\mathcal{R}_{\sigma}$. An accurate analytical inductance calculation can only be achieved if the 3-D fringing factors are considered. In [133] an analytical air gap calculation method including 3-D fringing effects is presented, which is based on the Schwarz-Christoffel transformation. The consideration of these effects leads to an accurate reluctance model as illustrated in **Fig. 5.10** (b).

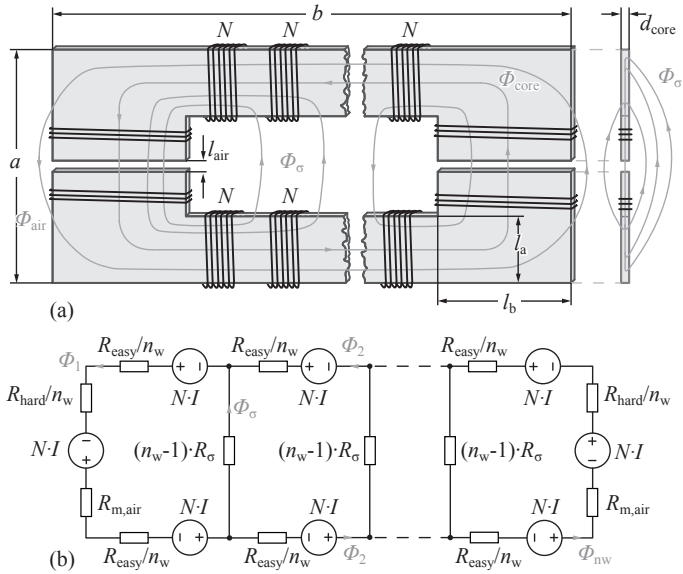


Fig. 5.10: (a) Setup of a PCB-integrated inductor with a two-parts core; n_w winding packages, each with N turns, are placed around the core in order to later facilitate an interleaving with a secondary winding. (b) Reluctance model of the setup presented in (a). The reluctances $\mathcal{R}_\sigma$ between the long magnetic rods have to be considered as they have considerable impact on the inductance for large ratios between core length and width, b/a.

The respective reluctances can be calculated with

$$\mathcal{R}_\mathrm{hard} = \frac{a - l_\mathrm{a}}{\mu_0\,\mu_\mathrm{r} l_\mathrm{b}\,d_\mathrm{core}\,k_\mathrm{fe}}, \quad \mathcal{R}_\sigma = \sigma_\mathrm{s} \cdot \frac{(a - 2\,l_\mathrm{a} - l_\mathrm{air})}{\mu_0 (b - 2\,l_\mathrm{b})\,d_\mathrm{core}\,k_\mathrm{fe}}$$
$$\mathcal{R}_\mathrm{easy} = \frac{b - l_\mathrm{b}}{\mu_0\,\mu_\mathrm{r} l_\mathrm{a}\,d_\mathrm{core}\,k_\mathrm{fe}}, \quad \mathcal{R}_\mathrm{air} = \sigma_\mathrm{a} \cdot \frac{l_\mathrm{air}}{\mu_0 l_\mathrm{b}\,d_\mathrm{core}\,k_\mathrm{fe}}, \quad (5.7)$$

whereas σ_s and σ_a are the 3-D fringing factors of the window reluctance $\mathcal{R}_\sigma$ and the air gap reluctance $\mathcal{R}_\mathrm{air}$, respectively. The reluctance model in **Fig. 5.10** (b) can then be solved with standard electrical circuit analysis methods which yield the air gap length l_air.

Tab. 5.3 presents the calculation and simulation results with and without considering fringing effects and the magnetic field in the wind-

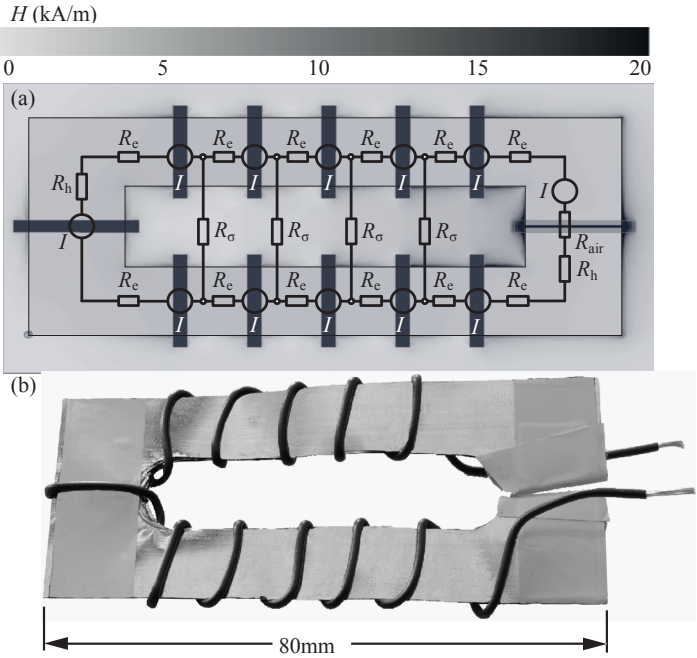


Fig. 5.11: (a) Reluctance model of an ultra-flat inductor and 3-D FEM simulation result of the magnetic field. The reluctances $\mathcal{R}_e$ and $\mathcal{R}_\sigma$ in the magnetic model are scaled with n_w and $(n_w - 1)$, respectively. The parameters are given in **Tab. 5.3** together with the calculated and simulated inductance values. (b) Prototype of the core consisting of ten stacked VITROVAC 6155F foils.

ing window for the core geometry shown in **Fig. 5.11** (b). A conventional inductance calculation method would result in a large error of $\epsilon = -78.85\,\%$, whereas

$$\epsilon = \frac{L_{calc} - L_{meas}}{L_{meas}}. \tag{5.8}$$

However, considering the fringing effects allows an accurate analytical calculation method for arbitrary core shapes. The results in **Tab. 5.3** show that the impact of the $\mathcal{R}_\sigma$ is rather small for this core setup which is also noticeable in the 3-D simulation presented in **Fig. 5.11** (a) as except for the air gap no significant field is in the wind-

Tab. 5.3: Inductance calculation comparison including the calculation error ϵ (Parameters: $a = 35\,\text{mm}$, $b = 80\,\text{mm}$, $l_\text{a} = 11\,\text{mm}$, $l_\text{b} = 13\,\text{mm}$, $l_\text{air} = 0.5\,\text{mm}$, $d_\text{core} = 0.2\,\text{mm}$, $N = 12$, $\mu_\text{r} = 1900$).

Calc. w/o window field and fringing	0.81 µH	$\epsilon = -78.9\,\%$
Calc. w/ fringing but w/o window field	3.58 µH	$\epsilon = -6.5\,\%$
Calc. w/ fringing and window field	3.87 µH	$\epsilon = +1.0\,\%$
3-D FEM simulation	3.60 µH	$\epsilon = -6.0\,\%$
Measurement result	3.83 µH	

ing window. However, if the ratio between b and a, cf. **Fig. 5.10** (a), increases, the window reluctance dominates the inductance calculation and a proper reluctance model is crucial [103].

Beside monolithic or two-parts core configurations, PCB-integrated cores can also be composed of several separate core legs. This allows for almost arbitrarily shaped core with the distance between two core legs being independent of the tape width a. The flexibility of the core construction, however, comes on the expense of a more complicated integration process as all core legs have to be aligned accurately to each other. **Fig. 5.12** (a) shows the setup of a 3-D FEM simulation for a PCB-integrated core composed of four legs with an air gap in each corner. **Fig. 5.12** (b) illustrates that for the large distance between two parallel core legs the stray field in the winding window is negligible and the magnetic field is concentrated in the air gaps. The distributed air gaps further yield a constant flux distribution in the core legs, cf. **Fig. 5.12** (c). This simplifies the core loss calclulation considerably.

For the core setup shown in **Fig. 5.12** (a), the window reluctance $\mathcal{R}_\sigma$ can be neglected and a simple reluctance model can be applied. Whether a more complex reluctance model is required can be determined with a simple 2-D FEM simulation showing the stray field distribution.

5.2.6 Interleaved windings

In many transformer applications, e.g. flyback transformers, a low leakage inductance is crucial for a proper operation of the converter. In

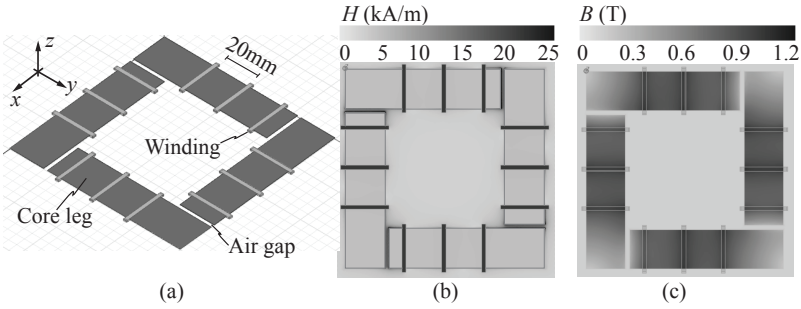


Fig. 5.12: (a) Simulation setup of a PCB-integrated core consisting of four legs. (b) Simulated magnetic field. (c) Simulated magnetic flux. Due to the air gaps in each corner the flux distribution is almost constant with regard to the core width.

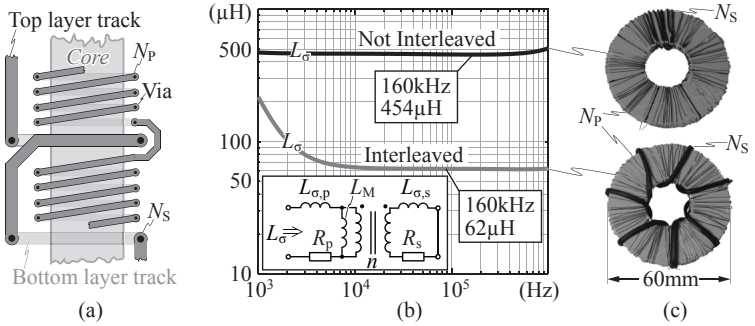


Fig. 5.13: (a) Interleaved winding arrangement. (b) Measurement result of the leakage inductance for an interleaved and a non-interleaved winding arrangement. (c) Prototypes used for the measurements: Ferrite N87, 1.5 mm thick, $N_P = 91$, $N_S = 7$. Measured primary inductance $L_P = 6.2$ mH.

conventional transformers, the primary and the secondary windings are therefore wound closely to each other and in many cases interleaved to maximize the coupling between the windings. In a PCB-integrated transformer, the windings are placed around the outlines of the core which implies that primary and secondary windings cannot be wound tightly together and therefore these transformers exhibit an inherently large leakage inductance.

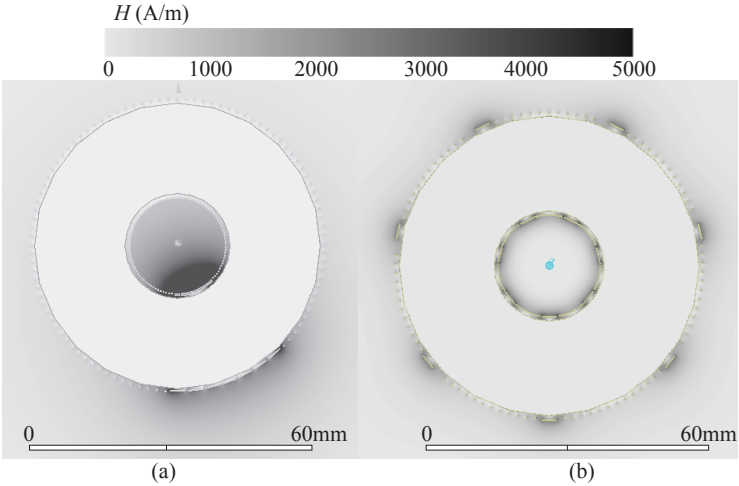


Fig. 5.14: Top view 2-D FEM simulations of the transformer in **Fig. 5.13**. (a) No interleaving between primary and secondary winding; (b) Interleaved winding arrangement. The primary current is $I_P = 1\,A$ and the secondary current is $I_S = 13\,A$.

In order to reduce the leakage inductance, an additional copper layer can be considered for the secondary winding which is placed on top of the primary winding. However, the extra copper layer comes at the expense of a thinner core as the overall thickness of the transformer is limited to 1 mm.

The coupling between the windings can be increased employing an interleaving of the windings, cf. **Fig. 5.13** (a), without compromising the thickness of the core. Applying the Double-2-D FEM simulation method [134] enables an efficient and simple way to estimate the leakage inductance of specific 3-D problems, e.g. toroids or EI cores, with two 2-D FEM simulations.

The simulations show that the interleaved winding arrangement reduces the leakage inductance by a factor of 7.2 (non-interleaved: $L_\sigma = 377.6\,\mu H$, interleaved: $L_\sigma = 52.5\,\mu H$). **Fig. 5.14** (a) and (b) depict the magnetic field distribution of a winding configuration without and with interleaving, respectively; due to the interleaving the window field is considerably reduced.

In order to validate the simulations, measurements on a protoype

core, cf. **Fig. 5.13** (c), have been performed with both winding arrangements. **Fig. 5.13** (b) presents the results which show a considerable improvement with the interleaved configuration. The measured primary inductance is $L_\mathrm{P} = 6.2\,\mathrm{mH}$. The analytical expression of the primary inductance L_σ with shorted secondary winding is

$$L_\sigma = L_{\sigma,\mathrm{p}} + \frac{n^2\,L_\mathrm{M}\cdot(n^2\,R_\mathrm{s}^2 + \omega^2\,n^2\,L_{\sigma,\mathrm{s}}^2 + \omega^2\,L_{\sigma,\mathrm{s}}\,L_\mathrm{M})}{n^4\,R_\mathrm{s}^2 + \omega^2\,n^4\,L_{\sigma,\mathrm{s}}^2 + 2\,\omega^2\,n^2\,L_{\sigma,\mathrm{s}}\,L_\mathrm{M} + \omega^2\,L_\mathrm{M}^2}. \tag{5.9}$$

For low frequencies, the measurement result of L_σ in **Fig. 5.13** (b) is determined by L_M,

$$\omega \to 0: \qquad L_\sigma = L_{\sigma,\mathrm{p}} + L_\mathrm{M} \approx L_\mathrm{M}, \tag{5.10}$$

whereas for high frequencies the measurement shows the total leakage inductance,

$$\omega \to \infty: \qquad L_\sigma = L_{\sigma,\mathrm{p}} + \frac{L_\mathrm{M}\cdot n^2\,L_{\sigma,\mathrm{s}}}{L_\mathrm{M} + n^2\,L_{\sigma,\mathrm{s}}} \approx L_{\sigma,\mathrm{p}} + n^2\,L_{\sigma,\mathrm{s}}. \tag{5.11}$$

Between 1 kHz and 5 kHz the measurement result in **Fig. 5.13** (b) shows an inductance drop according to (5.9).

Due to the reduced L_σ the prototype of the flyback transformer is realized employing the proposed interleaved winding arrangement.

5.3 Multi-objective design procedure for an ultra-flat flyback transformer

After the specific implications imposed by the ultra-thin PCB-integrated core have been discussed in the previous section, this section presents the design and the optimization of a flyback transformer (a two-winding inductor) employing a stacked core configuration which is integrated into the PCB, cf. **Fig. 5.2** (a).

The proposed multi-objective design procedure which is depicted in **Fig. 5.15** (a) can easily be adapted for an inductor or for different core configurations, e.g. toroidal cores, cf. **Fig. 5.2** (b).

Given all the input parameters listed in the flowchart, this step-by-step procedure leads to an optimal flyback transformer design with respect to a desired transformer efficiency η_tr or area-related power density α_tr,

$$\eta_{\mathrm{tr}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{loss}}}, \tag{5.12}$$

$$\alpha_{\mathrm{tr}} = \frac{P_{\mathrm{out}}}{A_{\mathrm{tot}}}, \tag{5.13}$$

whereas A_{tot} is the total required footprint area[1]. Each equation discussed in the following is given in **Fig. 5.15** (a).

The considered core geometry consists of four rectangular-shaped core legs configured as indicated in **Fig. 5.15** (b) with an air gap, l_{air}, in each corner. The length b and the width a are identical for each core leg, so that the outline of the transformer is quadratic. An advantage of this core configuration is that, due to the four separate core legs, the flux is mostly directed towards the easy direction, cf. **Fig. 5.15** (b) and so less core losses are obtained compared to a core setup in which the hard direction is more utilized, cf. **Fig. 5.10** (a).

The core could also be rectangular-shaped to reduce the winding window; thus, the aspect ratio between core length and width could be a further optimization parameter. Appendix B discusses the reduction of the required footprint area as a function of the aspect ratio.

Due to the air gaps in each corner of the core, the flux density can be assumed to be homogeneous in the core legs which can be seen in the simulation result of **Fig. 5.12** (c). This simplifies the core loss calculation; a design procedure for an inhomogenous flux density distribution is presented in [103].

In a first step the geometries of the windings, cf. **Fig. 5.15** (b), are determined; based on the track thicknesses $d_{\mathrm{tr1,2}}$ and the maximum allowable current density J_{max}, the track widths $b_{\mathrm{tr1,2}}$ and the via diameters $d_{\mathrm{via1,2}}$ of both windings can be calculated (including the via pad annular ring d_{vp} which is typically $> 0.15\,\mathrm{mm}$).

In the next design step the maximal allowable flux densities in the core, $B_{\mathrm{max,e}}$ and $B_{\mathrm{max,h}}$, are calculated for the easy and the hard directions with respect to the maximum allowable power loss per area, p_{loss}, and the saturation flux density B_{sat} according to (5.6)[2]. Then the procedure queries whether the applied flux density exceeds $B_{\mathrm{max,e,h}}$ or

[1] The optimization goal could easily be changed in order to consider only the area occupied by magnetics by defining a different area in (5.13).

[2] Since the core losses of the considered material are independent of a dc offset, we have $B_{\mathrm{max,e/h}} = \Delta B$. For other materials, the average current would also be an input parameter of the design procedure.

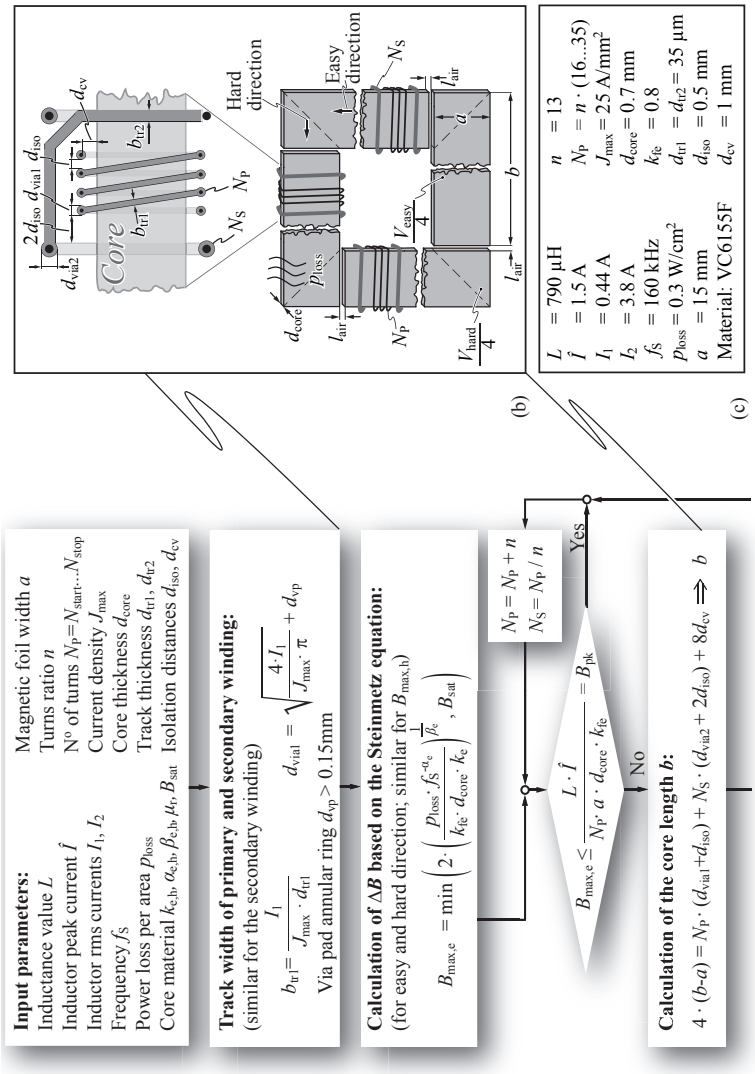


Fig. 5.15: (a) Block diagram of the design procedure of a flyback transformer with PCB-integrated core. (b) Illustration of the core and winding geometries. (c) Input parameter set. (d) Losses as a function of the number of turns for the parameters given in (c).

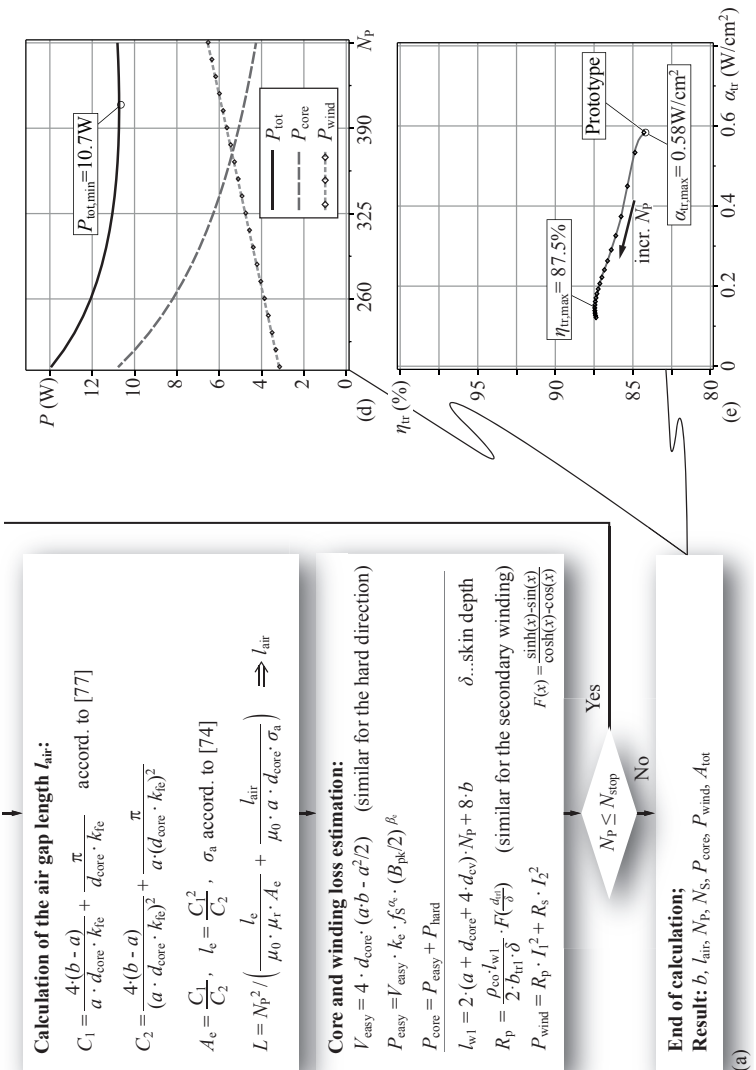
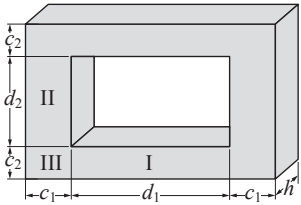


Fig. 5.15: (e) η-α-Pareto Front; a trade-off between the efficiency η_{tr} and the area-related power density α_{tr} has to be found for a given inductor or transformer. The realized prototype is indicated in the figure.



	l_i	A_i
I	d_1	$c_2 \cdot h$
II	d_2	$c_1 \cdot h$
III	$\frac{\pi}{4} \cdot (c_1 + c_2)$	$\frac{h}{2} \cdot (c_1 + c_2)$

$$C_1 = \sum \frac{l_i}{A_i} \qquad C_2 = \sum \frac{l_i}{A_i^2}$$

Fig. 5.16: Segmentation and corresponding equations of a rectangular-shaped core [135].

not. If $B_{\mathrm{pk}} > B_{\mathrm{max,e,h}}$, the next iteration step starts with an increased number of turns N_{P}; otherwise the procedure continues.

The perimeter of the winding window, $4 \cdot (b - a)$, has to be large enough to provide the space for all tracks and vias of primary and secondary winding including the isolation distances between the tracks, d_{iso}, and the distance between the core and the vias, d_{cv}. Solving this equation yields the required core leg length b.

Since the core geometry is already determined, the inductance value L can now be adjusted by calculation of the required air gap length l_{air}. As mentioned in Section 5.2.5, the fringing flux of the air gap must be considered in the air gap reluctance calculation. However, contrary to a setup composed of a monolithic or a two-parts core, e.g. in **Fig. 5.10** (a), in the chosen core configuration the distance between two parallel core legs is large so that the window stray reluctance $\mathcal{R}_{\sigma}$ is negligible which has been confirmed using 3-D FEM simulations, cf. **Fig. 5.12** (b). Thus, a simple reluctance model composed of the core reluctance and the air gap reluctance can be applied.
According to [135], an accurate reluctance model of a rectangular core can be obtained by considering the segmentation in **Fig. 5.16**. The coefficients C_1 and C_2, cf. **Fig. 5.16**, are used to calculate the effective magnetic length l_{e} and the cross-sectional area A_{e} which define the reluctance of the core. The sum of core reluctance and air gap reluctance determines the inductance value L and thus, the air gap length l_{air} can be calculated.

With all core and winding parameters being known, the core and winding losses can be determined. The core losses are evaluated using the Steinmetz equation applied to the easy and the hard directions, cf. **Fig. 5.15** (b).

The track thicknesses of the primary and secondary windings are lower than the skin depth for the considered switching frequency ($\delta = 167\,\mu\text{m}$ at $160\,\text{kHz}$) and thus, the impact of an eddy current caused increase of the winding resistance is low. Nonetheless, the calculation of the winding resistance,

$$R_\text{W} = R_\text{p} + n^2 \cdot R_\text{s}, \tag{5.14}$$

is based on the 1-D model presented in [136] which takes the skin effect into account. For applications or geometries where the proximity effect has significant impact on the winding resistance either sophisticated calculation methods [135, 137] or FEM simulations are required. In the case at hand, however, the simulations have been used to confirm that the proximity effect is negligible.

The design procedure is iterated over a specified range of $N_\text{P} = N_\text{start} \ldots N_\text{stop}$ with a step size of n which allows for integer values of N_S. **Fig. 5.15** (d) shows the core losses P_core and the winding losses P_wind as a function of N_P based on the parameters given in **Fig. 5.15** (c); minimal losses of $P_\text{tot,min} = 10.7\,\text{W}$ are obtained for $N_\text{P} = 403$ and $N_\text{S} = 31$. **Fig. 5.15** (e) depicts a η-α-Pareto Front which shows that a compromise between the transformer efficiency η_tr and the area-related power density α_tr has to be made. The maximal power density for the considered design is $\alpha_\text{tr,max} = 0.58\,\text{W/cm}^2$ and the maximal efficiency of the transformer is $\eta_\text{tr,max} = 87.5\,\%$. The power density α_tr considers the total required area; however, the winding window can also be utilized to place components which would increase the compactness of the converter system.

In the presented design procedure, the width of the magnetic foil, a, is chosen to be 15 mm due to the availability of the material. However, a is also a free design parameter which can be optimized. **Fig. 5.17** shows the Pareto Front of VITROVAC 6155F and 2714A for several values of $a = 0.5 \ldots 26\,\text{mm}$ (with a step size of $\Delta a = 0.5\,\text{mm}$) and of $N_\text{P} = 13 \ldots 455$ (with a step size of $n = 13$).
As can be seen, VITROVAC 6155F allows for higher efficiencies compared to 2714A. This is because in the chosen core configuration the hard direction, which causes high losses in VITROVAC 6155F, is barely utilized. Furthermore, the saturation flux density of 2714A is lower compared to VITROVAC 6155F, cf. **Tab. 5.2**, which explains the lower achievable power density of 2714A. However, for other core configurations and specifications 2714A might be the material of choice.

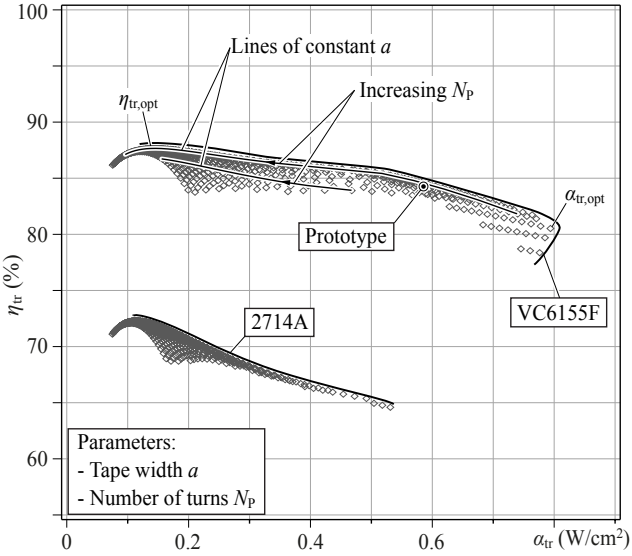


Fig. 5.17: Pareto Front for several values of N_P and a for the materials VITROVAC 6155F and 2714A. The maximum efficiency achievable is $\eta_{tr,opt} = 87.7\,\%$ ($a = 21.5\,mm$, $N_P = 325$) and the maximum power density is $\alpha_{tr,opt} = 0.79\,W/cm^2$ ($a = 20.5\,mm$, $N_P = 130$). The realized prototype is indicated in the figure.

Fig. 5.17 shows that α_{tr} increases with decreasing N_P for constant values of a due to the reduced area requirement of the winding. At $\alpha_{tr,opt} = 0.79\,W/cm^2$ the maximal power density is reached ($a = 20.5\,mm$ and $N_P = 130$, transformer size: $97 \times 97\,mm^2$) and a further decrease of N_P at constant a is not possible due to the limitation of the maximal flux density in the core. N_P can only be further decreased when a is increased (which increases the core cross-section). This required increase of a is proportionally higher than the achieved reduction of the winding window and thus the total required footprint area increases. Consequently, a further power density increase is not possible anymore.
Starting from $\alpha_{tr,opt}$, an increase of N_P and/or an increase of a decreases the flux density in the core which results in lower core losses. Thus, for increasing N_P and/or increasing a the Pareto Front shows higher efficiencies at the expense of a lower α_{tr}. The decrease of core

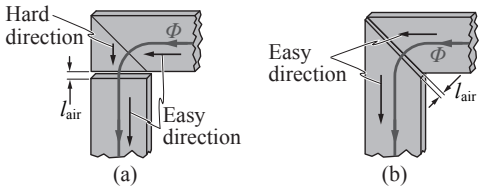


Fig. 5.18: PCB-integrated core composed of (a) rectangular legs and (b) trapezoidal legs.

Tab. 5.4: Comparison between rectangular and trapezoidal shape of the core legs for a PCB-integrated flyback transformer rated with $P_{\mathrm{out}} = 76\,\mathrm{W}$.

	Rectangular shape	Trapezoidal shape
P_{core}	10.8 W	9.2 W
P_{wind}	3.2 W	3.2 W
α_{tr}	0.58 W/cm^2	0.58 W/cm^2
η_{tr}	84.3 %	85.8 %

losses, however, is compromised by an increase of winding losses as the track lengths increase. Thus, the efficiency reaches a maximum where the decrease of core losses is equal to the increase of winding losses. The maximal efficiency is $\eta_{\mathrm{tr,opt}} = 87.7\,\%$ at $a = 21.5\,\mathrm{mm}$ and $N_{\mathrm{P}} = 325$ (transformer size: $220 \times 220\,\mathrm{mm}^2$). A further increase of N_{P} or a results in a lower efficiency as the increase of winding losses exceeds the decrease of core losses.

The design procedure is carried out for rectangular core legs. Although this core configuration is beneficial as the hard direction is barely utilized, cf. **Fig. 5.18** (a) the power losses could be further reduced employing trapezoidal core legs, cf. **Fig. 5.18** (b). With this setup the hard direction is basically avoided. The presented design procedure can easily be modified for trapezoidal core legs whereas a homogenous magnetic flux distribution in the core is assumed. **Tab. 5.4** compares the results obtained for rectangular and trapezoidal core legs for the prototype design indicated in **Fig. 5.17**. While the winding losses are identical since the same number of turns is considered the core losses are reduced by 1.6 W which increases the transformer's efficiency by

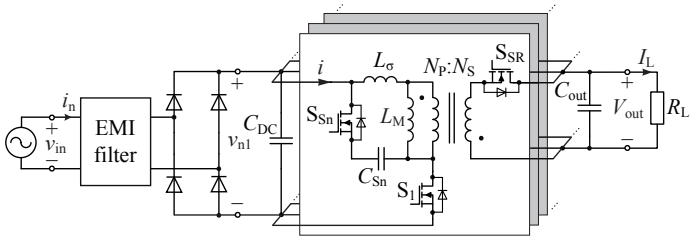


Fig. 5.19: Flyback-type single-phase PFC rectifier system, specified in **Tab. 1.2**. The system is split up into six parallel interleaved modules ($N_{\mathrm{mod}} = 6$) in order to reduce the input and output capacitor currents. Each one of the parallel modules is referred as a *Power Sheet*.

1.5 %. The power density is constant because the core size is similar in both cases. Only the air gap is slightly higher for the trapezoidal leg as the core cross-sectional area at the air gap is larger compared to the rectangular case.
Due to the simpler core manufacturing, however, the design procedure and the implemented prototype are based on rectangular core legs.

5.4 Experimental results

In order to verify the presented design procedure a prototype of a flyback transformer for a flyback PFC rectifier has been implemented. The PFC rectifier system specified in **Tab. 1.2** features an output power of 200 W. In order to obtain a flyback transformer with reasonable footprint size and performance this system is split up into six subsystems with $P_{\mathrm{out}} = 38\,\mathrm{W}$ each. The prototype of the flyback transformer is thus designed with respect to one of the six converter cells, cf. **Fig. 5.19**.

For the flyback converter a compact transformer design has been chosen as indicated in **Fig. 5.15** (e). **Fig. 5.20** depicts the PCB-integrated flyback transformer and the respective parameters are listed in **Tab. 5.5**.

Fig. 5.21 (a) presents measurement results of the primary inductance which matches well with the desired value (calculated: 790 µH, measured: $L_{\mathrm{P}} = 772\,\mu\mathrm{H}$ at 100 Hz). At the switching frequency of $f_{\mathrm{S}} = 160\,\mathrm{kHz}$ the inductance decreases to $L_{\mathrm{P}} = 741\,\mu\mathrm{H}$. Although

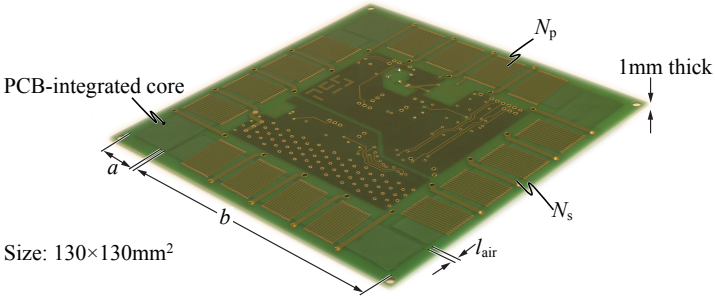


Fig. 5.20: Prototype of the PCB-integrated flyback transformer. Due to the large winding window components of the converter can be placed in the flyback transformer window area.

Tab. 5.5: Resulting parameters of the design procedure for the realized PCB-integrated flyback transformer in DC-DC operation rated with $P_{out} = 76\,\mathrm{W}$, according to the maximum power occuring in AC-DC operation of a PFC rectifier specified for an output power of 38 W (cf. **Fig. 4.14** (b)).

a	=	15 mm	P_{core}	=	10.8 W
b	=	100 mm	P_{wind}	=	3.2 W
l_{air}	=	0.8 mm	η_{tr}	=	84.3 %
d_{core}	=	0.7 mm	α_{tr}	=	0.58 W/cm²
k_{fe}	=	0.8	A_{tot}	=	139 cm²
N_P	=	208	B_{pk}	=	0.7 T
N_S	=	16			

primary and secondary windings are interleaved the large spacial dimension of the transformer results in a rather high leakage inductance of $L_\sigma = 140\,\mu\mathrm{H}$ which is in good agreement with simulation results. Due to the high L_σ an active snubber is employed in the flyback converter which recycles the energy stored in the leakage inductance [106].

The primary winding capacitance is 25 pF and the interwinding capacitance is 106 pF. The resulting resonance frequency is 1.1 MHz which

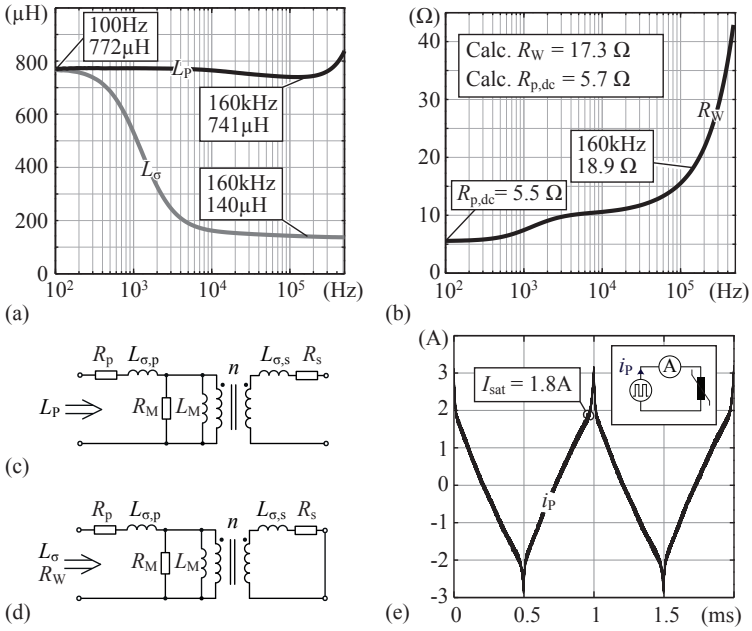


Fig. 5.21: (a) Total inductance L_P and leakage inductance L_σ over the frequency. (b) Total winding resistance $R_\mathrm{W} = R_\mathrm{p} + n^2 \cdot R_\mathrm{s}$ refered to the primary side over the frequency. (c) Equivalent circuit of the transformer used to measure L_P. (d) Equivalent circuit of the transformer used to measure L_σ and R_W. (e) Saturation measurement results which confirms the specified saturation current of 1.5 A.

is sufficient for the operation of the converter.

Fig. 5.21 (b) shows the winding resistance R_W, cf. (5.14), over the frequency. The calculation and the measurement at 160 kHz agree reasonably well (calc. $R_\mathrm{W} = 17.3\,\Omega$, meas. $R_\mathrm{W} = 18.9\,\Omega$). Notice, that at low frequencies only the primary resistance R_p (not R_W) is measured which confirms the calculation. The transformer configurations employed for the impedance measurements are indicated in **Fig. 5.21** (c) and (d). **Fig. 5.21** (e) illustrates the result of a saturation measurement; a current of $\hat{I} = 1.5$ A can be applied to the flyback transformer without causing saturation which has been specified in the design procedure.

In order to verify the loss calculation and thus the calculated effi-

Tab. 5.6: Efficiency comparison between calculation, simulation, and measurement of the *Power Sheet* in Dc-Dc operation.

		Calculation	Simulation	Measurement
$V_{in} = 230\,V$, $V_{out} = 20\,V$	P_{out}	38.0 W	38.0 W	38.0 W
	P_{in}	48.7 W	49.8 W	50.2 W
	P_{core}	6.5 W	6.6 W	
	P_{wind}	2.3 W	2.9 W	
	P_{res}	1.9 W	2.3 W	
	η_{tr}	81.2 %	80.0 %	
	η	78.1 %	76.3 %	75.2 %
$V_{in} = 325\,V$, $V_{out} = 20\,V$	P_{out}	76.3 W	76.1 W	76.3 W
	P_{in}	97.2 W	98.0 W	98.7 W
	P_{core}	9.4 W	9.7 W	
	P_{wind}	8.3 W	8.3 W	
	P_{res}	3.2 W	4.3 W	
	η_{tr}	81.2 %	80.9 %	
	η	78.5 %	77.4 %	77.3 %

ciency of the flyback transformer, η_{tr}, the flyback converter is operated in Dc-Dc mode at different input voltages V_{in}. **Tab. 5.6** lists a comparison between the calculations, simulations, and measurements for $V_{in} = 230\,V$ and $325\,V$. The calculated losses of the converter are too low as the analytical model used to calculate the voltage and current waveforms is considered to be lossless. In order to consider the resistive and parasitic converter components a simulation model implemented with Simplorer [138] is used in which the analytical core loss model according to **Fig. 5.15** (a) is still applied. **Tab. 5.6** shows that the balance of losses fits well to the measured efficiency and the estimated core and winding losses, P_{core} and P_{wind}, together with the calculated residual converter losses, P_{res} (semiconductor losses, snubber losses, gate drive losses), cover the measured converter losses.

Compared to the efficiency calculated by the design procedure, cf. **Tab. 5.5**, the estimated values in **Tab. 5.6** deviate because the de-

sign procedure calculates the core losses P_{core} for the maximum expected peak current of $\hat{I} = 1.5\,\text{A}$. However, at nominal DC-DC operation of $V_{\text{in}} = 325\,\text{V}$ and $P_{\text{out}} = 76\,\text{W}$ the applied peak current is 1.3 A which yields lower core losses compared to result of the design procedure. Similarly, the primary and the secondary currents of the design procedure are specified for AC-DC operation at $P_{\text{out}} = 38\,\text{W}$ while **Tab. 5.6** lists the result of DC-DC operation.

A detailed discussion about the converter model, the calculated, simulated, and measured waveforms of the flyback converter in DC-DC and AC-DC operation is presented in Chapter 4.

5.5 Conclusion

For the realization of a 1 mm thin PFC rectifier, the PCB-integration of magnetic components is a key issue. This chapter presents a multi-objective design procedure for ultra-flat magnetic components employing PCB-integrated cores which facilitates an optimized inductor or transformer design. Therefore, it is crucial to identify the magnetic material properly.

Depending on the material and the shape of the core, anisotropic core losses, the need for isolation between the magnetic foils, or a proper reluctance model have to be considered in order to be comply with a specified power loss per area limit and to obtain a required inductance value. All these issues are elaborated and shown by example of two amorphous materials (VITROVAC 6155F and 2714A).

The proposed design procedure considers several electrical, magnetic, and geometrical parameters in order to determine the component's configuration that is optimal with respect to minimum losses and/or minimum footprint area. The resulting Pareto Front is a vivid representation of the trade-off and it allows for a fair comparison between different materials. The design procedure can be adapted for different core shapes or aspect ratios and is therefore a universal design tool for a PCB-integrated inductor or transformer.

In order to verify the theoretical considerations a prototype of a flyback transformer for a 38 W single-phase flyback PFC rectifier has been implemented. The chosen shape of the transformer is beneficial for an anisotropic core material (VITROVAC 6155F) as almost only the easy magnetization axis is utilized. This might differ for other core shapes. Measurements to verify the core and winding losses have been

performed by operating the transformer in a Dc-Dc flyback converter. All measurements show good agreement with the results of the design procedure. The achieved efficiency of the transformer is $\eta_{\mathrm{tr}} = 80\,\%$ which identifies a performance limit for an ultra-flat converter system resulting from the extreme converter shape factor.

6

Design of an Ultra-flat EMI Filter

The EMI filter is an essential part of a PFC rectifier and considerable effort has been made to investigate this topic. The filter significantly determines size, weight, and costs of the rectifier system [84]. For that reason, the implications imposed by the PCB-integration of each component on the filter characteristics needs to be investigated in order to design a filter that fulfills the specified standards. This section emphasizes on the proof-of-concept that an EMI filter can be realized with a targeted thickness of 1 mm. The optimization of each component would be the next step and is not detailed herein. The filter design is discussed with respect to the flyback-type PFC rectifier presented in Chapter 4. However, the presented statements are also valid for other topologies.

6.1 Introduction

The flyback-type PFC rectifier presented in Chapter 4 operates with a variable switching frequency between 160 kHz and 320 kHz. The rectifier is connected to the grid and the generated HF currents could interfere with surrounding electronic equipment and/or could disturb the desired operation. The converter therefore requires an input filter in order to suppress the emitted HF current harmonics and to be immune to interference generated by electronic equipment in the surroundings. The filter has to be designed in order to fulfill electro-magnetic interference (EMI) standards, e.g. Class A or Class B limits from CISPR [30, 70]. The nature of noise mode for conducted emission (CE) EMI can be divided into two noise sources, differential mode (DM) noise and common

mode (CM) noise [139]. For each type a separate filter can be designed which simplifies the EMI noise modeling and the filter synthesis. Still, the filter design imposes challenges to the designer as several partly opposed requirements have to be fulfilled [140]:

- The required filter attenuations for both DM and CM filters have to be obtained.
- The filter has to be optimized with regard to the filter size and/or the losses.
- To prevent the filter resonances to be excited from disturbances in the grid the filter needs sufficient damping [84].
- The reactive power consumption of the filter should be as small as possible. This means the DM filter capacitors are limited in capacitance.
- The filter resonances may not interfere with the dynamics of the converter's control. So, the output impedance of the filter has to be minimized by proper design and damping to prevent stability problems [84, 141].
- The current through the CM capacitors is limited due to IT safety regulations which limits the allowable CM capacitance [31].

The EMI noise is measured using a Line Impedance Stabilization Network (LISN) connected between the grid and the converter. The LISN, which is illustrated in **Fig. 6.1**, allows for reproducible measurements regarding different grid impedances and serves as interface from the converter to the EMI test receiver [84]. For the considered frequency range of 150 kHz ... 30 MHz, the LISN basically consists of the 50 Ω input impedance of the test receiver which measures the voltage v_{rec}. The aforementioned EMI standards define limits with respect to the average detection or the quasi-peak detection [84, 142]. For the case at hand, the quasi-peak detector is considered and corresponding limits are given in **Fig. 6.2**.

In the past, the design of the EMI filter has often been based on trial-and-error approaches which are time consuming and do not allow for a filter optimization [84]. Since the EMI filter allocates up to one third of the overall converter volume for conventional converter systems,

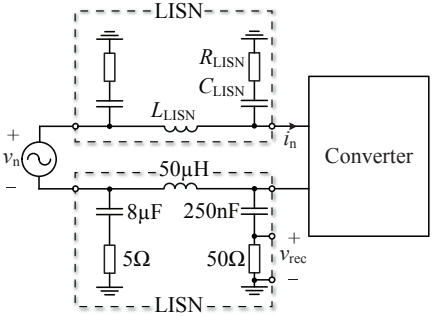


Fig. 6.1: Line Impedance Stabilization Network (LISN).

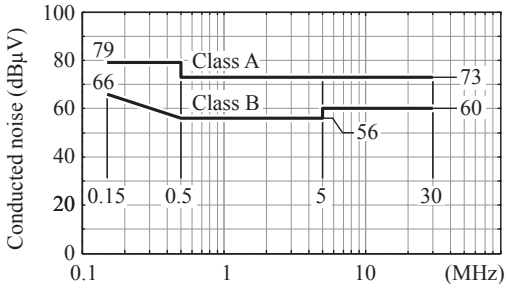


Fig. 6.2: Quasi-peak limits for conducted emissions according to CISPR Publications 11 and 22.

cf. [22], the focus of research has been laid on the optimization of the filter size [85, 142–144].

The required filter attenuation has to be determined either with calculations, simulations, or with measurements. The filter design based on measurements is not very efficient as a prototype is already needed before the filter is built. Moreover, an overall system optimization, as e.g. shown in [145], is not possible.

To overcome the drawback of the measurement-based filter synthesis, sophisticated models for DM and CM noise sources and the respective propagation paths have been proposed [146–148] which allow for an analytical description of the EMI noise. The calculation based design of an EMI filter can be simplified by applying reasonable assumptions. [85] and [143] present a DM filter design which assumes that the

total DM noise occurs at a certain design frequency f_d. Based on this noise level the filter attenuation is determined. Still, the calculation of the EMI noise is difficult if parasitic components need to be included in the model.

Contrary to calculations, simulations offer an easy and direct way to obtain the spectrum which includes the parasitic behavior of the elements and transients imposed by the control. Since the test receiver and in particular the detector have significant impact on the measured EMI spectrum [84, 142] it is crucial to consider the test receiver and the detector properly in the simulation model. The simulation software Gecko [149] offers an EMI test receiver model which considered the effect of the chosen detector type on the EMI spectrum. For that reason, in the case at hand, the EMI noise is determined using a simulation model.

In order to prevent the excitation of the filter resonances from disturbances in the grid voltage and to avoid interactions between the filter and the rectifier stage control, damping of the filter is required [150]. Several methods to introduce a damping branch into the filter and the optimization of the damping resistance are presented in [87, 151]. The elaboration, however, is carried out for a single-stage filter. It is well known, that multi-stage filters yield smaller designs as the filter attenuation of an LC filter with n stages is $n{\cdot}40\,\mathrm{dB/decade}$ at high frequencies. The cut-off frequency f_c is hence shifted to higher frequencies which allows for smaller filter components [84]. However, the optimal damping branches determined for a single-stage filter may not be optimal with respect to a multi-stage filter anymore. To overcome this problem, [141] proposes a damping optimization which allows for an optimal design of arbitrary stage filter structures.

In this chapter, the design of an ultra-flat EMI filter is presented for the example of the flyback-type PFC rectifier. The filter synthesis is based on simulations for both noise types (DM and CM) and the PCB-integrated filter inductors are designed according the method presented in Section 5.3.

6.2 Design of the differential mode filter

6.2.1 Determination of the DM capacitance

A capacitor connected between the line and the neutral wire of the grid consumes reactive power. For a low power Ac-Dc converter already

Tab. 6.1: Applied DM capacitors from Murata [41].

Capacitance	56 nF / 250 V_{rms}
Size	$5.7 \times 5.0 \times 2.9\,mm^3$
Rating	Class X2 [152]
Testing	Impulse (1.2/50 µs): 2.5 kV
	1000 h test: 1312.5 V / 100 ms every hour

small values of those X capacitors cause a considerable contribution to the total reactive power consumption. For instance, a DM capacitance of 1 µF would cause a reactive power flow at mains frequency of

$$Q = V_n^2 \cdot \omega_m C = (230\,V)^2 \cdot 2\pi\,50\,Hz \cdot 1\,\mu F = 16.6\,VAr. \tag{6.1}$$

Considering a flyback PFC rectifier cell with a rated power of 38 W, this would result in a displacement factor of DF = 0.91. For that reason, EMI filters designed for conventional power supplies employ only small DM capacitors and rather use large filter inductors to achieve the desired attenuation.

The displacement factor imposed by the DM EMI filter for the flyback-type PFC rectifier is specified to be over 0.975. For the power level of a flyback cell the maximum total DM capacitance is thus 500 nF. Since the capacitor $C_{DC} = 100\,nF$, cf. **Fig. 6.5**, is basically part of the EMI filter and also contributes to the reactive power consumption it has to be considered in this calculation. Thus, the capacitance available for the DM filter design is

$$C_{DM,tot} = 400\,nF. \tag{6.2}$$

DM filter capacitors for the EMI filter board have to fulfill safety requirements according to IEC 60384-14 [152] and the accordingly rated capacitors are referred to as X capacitors. With respect to the ultra-flat design of the filter ceramic SMD chip capacitors have been considered [41]. Although the height of X2 chip capacitors still exceeds 1 mm the package size is decreasing continuously [41] and X2 chip capacitors with a height of less than 1 mm are expected in future. For the design of the EMI filter the capacitor specified in **Tab. 6.1** is considered.

Ceramic capacitors are prone to lose their capacitance value at high voltage levels. Therefore, the applied capacitors have been tested at

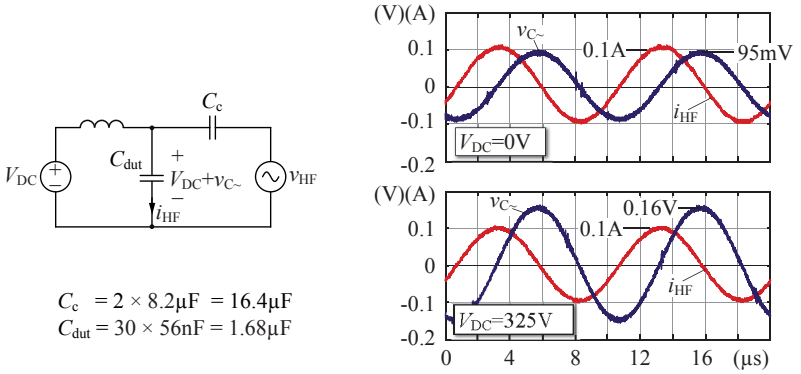


Fig. 6.3: Circuit and waveforms for the voltage stability measurement of the applied X2 ceramic capacitor chips.

high voltage to check their voltage stability. **Fig. 6.3** illustrates the measurement circuit where a DC source is superimposed by a small signal AC source via a coupling capacitor C_c. The coupling capacitor employed is composed of two parallel connected foil capacitors ($2 \times 8.2\,\mu F/K305\,V\sim$, B32926 [43]) and the capacitor under test C_{dut} consists of 30 parallel X2 capacitor chips specified in **Tab. 6.1**. The figure further shows the measurement waveforms at $V_{DC} = 0\,V$ and $V_{DC} = 325\,V$. As can be seen, the ratio between the amplitudes of the AC voltage $v_{C\sim}$ and the current i_{HF} changes with the applied DC voltage. At $V_{DC} = 325\,V$ the capacitance loses 41 % of its value at $V_{DC} = 0\,V$. This capacitance drop has to be considered in the design of the DM filter.

6.2.2 Magnetic materials applicable to PCB-integrated cores

The core materials used for conventional EMI filter inductors are typically iron powder [123, 153, 154], ferrite [43, 123, 153], or amorphous magnetic materials [126, 127]. Among them, iron powder is most popular as the maximum flux density is high (up to 1 T), the permeability is constant over a wide frequency range [84], and the low permeability allows for a toroidal core shape without air gap. For high permeability materials, an air gap is typically necessary which increases the complex-

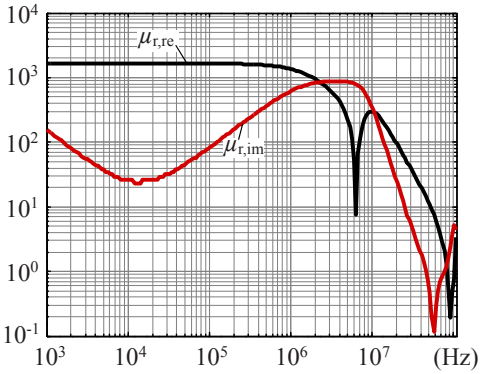


Fig. 6.4: Measured complex permeability of VITROVAC 6155F.

ity of manufacturing and the resulting fringing field is prone to couple the noise to other parts of the filter [84].

Ferrite and iron powder cores, however, are not easily applicable to the PCB-integration process as they are very brittle and the thinnest available custom ferrite cores are reported to show a height of 1.5 mm [43]. Therefore, these materials are not suited for the realization of a PCB-integrated core.

Amorphous materials remain to embed the filter inductor. Unfortunately, compared to powder cores and ferrites, the available information given in the datasheets of amorphous materials is rather poor. In particular, the permeability as a function of the applied frequency is rarely documented.

VITROVAC 6155 F (VC 6155F) by Vacuumschmelze [126] has been chosen as core material of the DM filter inductors as the material features a high saturation flux density, cf. **Tab. 5.2**, a well-defined permeability of $\mu_r = 1900$, and because of the availability of the material.

Since the frequency behavior of the permeability for VITROVAC 6155F is not available in datasheets, measurements with an impedance analyzer (Agilent 4291A [155]) have been conducted on a toroidal core ($d_o = 33.8\,\text{mm}$, $d_i = 31\,\text{mm}$, $h = 35\,\text{mm}$, $N = 20$). The resulting decomposition into real and imaginary part is depicted in **Fig. 6.4**. As can be seen, the real part of the permeability, which corresponds to the inductance value, is constant up to several hundreds of kHz.

6.2.3 Required DM filter attenuation

In a first step of the DM filter design, the DM noise level has to be determined. The noise level corresponds to the quasi-peak detected voltage v_{rec}, cf. **Fig. 6.1**, at the EMI test receiver input [84]. v_{rec} is defined by the HF component of the input current i_{n} which flows through $R_{\mathrm{LISN}} = 50\,\Omega$.

As already mentioned, the noise level determination is done using simulations. **Fig. 6.5** (a) shows the simulation model of the flyback-type PFC rectifier with the LISN and the EMI filter connected between the grid and the converter. For the determination of the DM EMI noise level, the EMI filter block indicated in **Fig. 6.5** (a) is shorted and the earth wire is opened ($\mathrm{S_{CM}}$ open). The measured voltage v_{rec} is then applied to an EMI test receiver, cf. **Fig. 6.5** (d), which calculates the noise according to the quasi-peak method. A detailed description of the quasi-peak method is given in [84].

In order to get a accurate estimation of the noise the degrading effect of the applied voltage on the capacitance C_{DC} is considered. For it, the capacitance is considered to feature only 65 % of the specified value. Furthermore, the parasitic capacitances of the full bridge diodes are also included which can be found in the datasheet.

Fig. 6.6 shows the resulting DM noise spectrum up to a frequency of 30 MHz. The highest noise component is observed at the lowest switching frequency $f_{\mathrm{min}} = 160\,\mathrm{kHz}$ as the maximum power is transferred with lowest switching frequency, cf. **Fig. 4.15** (b). Although the switching frequency is specified up to 320 kHz, the noise spectrum ends at approximately 260 kHz because at low input voltages the modulation of the converter is turned OFF in order to achieve a smoother zero crossing of the input current. Note that at low input voltages the switching frequency f_{S} would be high. The spectrum of the variable switching frequency is repeated at multiples of the baseband, i.e. at 320 kHz, 480 kHz, etc.

The design frequency for the filter design is related to the maximum noise level and thus

$$f_{\mathrm{d}} = 160\,\mathrm{kHz} \qquad \text{with} \qquad NL = 134\,\mathrm{dB\mu V}. \tag{6.3}$$

Fig. 6.7 presents the determination of the required attenuation which is the difference between the EMI noise without filter and the limit including a safety margin:

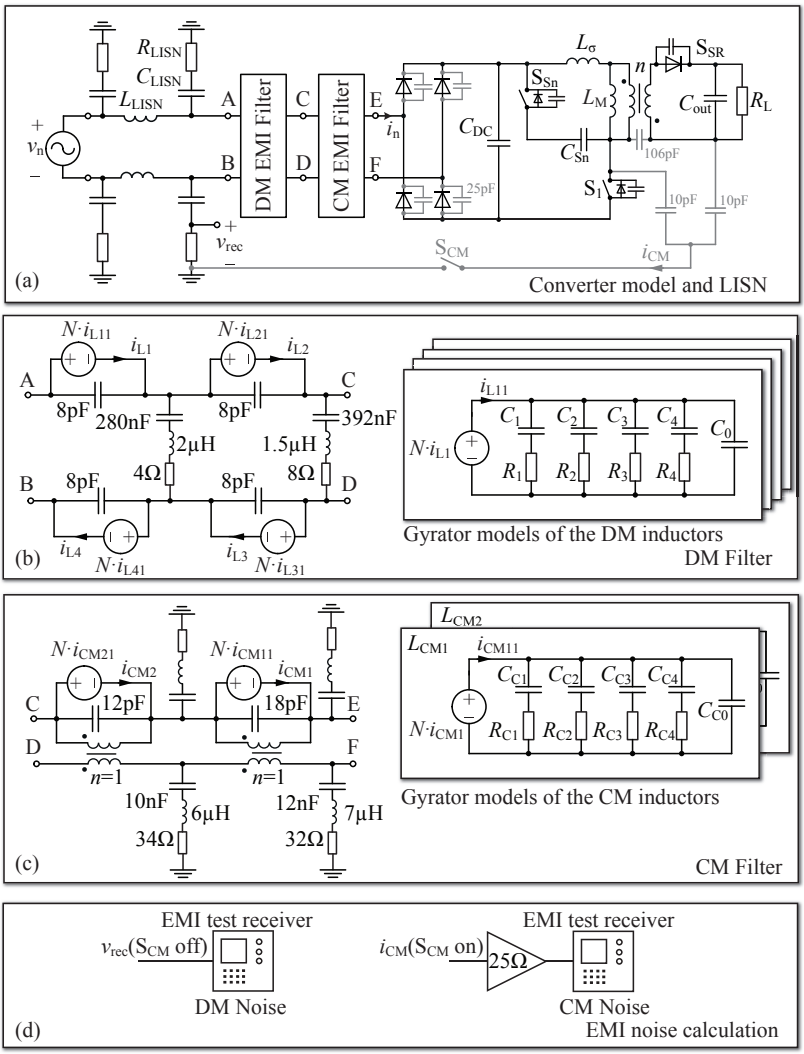


Fig. 6.5: Simulation model of the flyback-type PFC rectifier: (a) Power circuit with EMI filter and LISN, (b) DM filter, (c) CM filter, (d) principle of the EMI noise determination. The total EMI noise has been calculated according to (6.22). The converter control discussed in Section 4.5 has been applied. The simulation time is $T_{\text{end}} = 40\,\text{ms}$ and the step size is $\Delta t = 8\,\text{ns}$.

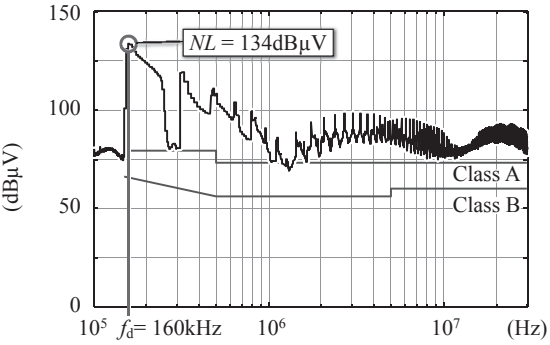


Fig. 6.6: Simulated DM noise based on the circuit in **Fig. 6.5** (a). The highest noise level of $NL = 134\,\mathrm{dB\mu V}$ occurs at $f_{\min} = 160\,\mathrm{kHz}$. Therefore, the design frequency is $f_\mathrm{d} = 160\,\mathrm{kHz}$.

$$\begin{aligned} Att_\mathrm{req}(f_\mathrm{d})[\mathrm{dB}] &= NL(f_\mathrm{d})\,[\mathrm{dB\mu V}] - \\ &- Limit(f_\mathrm{d})\,[\mathrm{dB\mu V}] + \\ &+ Margin\,[\mathrm{dB}]. \end{aligned} \tag{6.4}$$

For the case at hand, Class B and a safety margin of 8 dB have been considered which results in a required filter attenuation of

$$Att_\mathrm{req}(160\,\mathrm{kHz}) = 134\,\mathrm{dB\mu V} - 66\,\mathrm{dB\mu V} + 8\,\mathrm{dB} = 76\,\mathrm{dB}. \tag{6.5}$$

6.2.4 DM filter topology

The design of an EMI filter for a desired attenuation always raises the question of the number of stages that should be employed. In [156] it is shown, that the minimum size of a multi-stage filter is obtained when the components of each stage are identical. Based on this assumption, a single-stage, a 2-stage, and a 3-stage filter are compared to each other to determine the most suitable topology.

The total DM capacitance is limited to $C_\mathrm{DM,tot} = 400\,\mathrm{nF}$ and the corresponding filter inductors are designed in order to obtain an attenuation of $Att_\mathrm{req} = 76\,\mathrm{dB}$ at $f_\mathrm{d} = 160\,\mathrm{kHz}$. The filter inductance of each

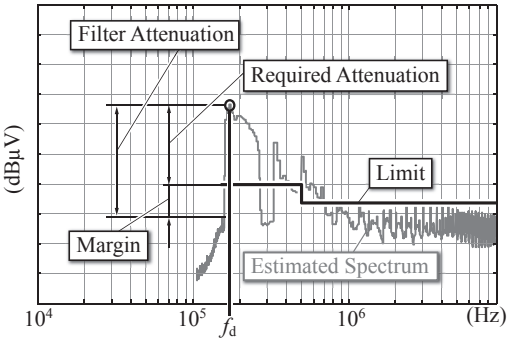


Fig. 6.7: Illustration of the determination of the required filter attenuation.

stage can be calculated with

$$2 \cdot L_{\mathrm{DM}} = \frac{1}{(2\pi f_{\mathrm{c}})^2 \cdot C_{\mathrm{DM}}}, \tag{6.6}$$

(the factor 2 accounts for the partitioning of the inductor to the line and the neutral wire) with the cut-off frequency f_{c}

$$f_{\mathrm{c}} = f_{\mathrm{d}} \cdot \sqrt{10^{-Att_{\mathrm{req}}/20}}. \tag{6.7}$$

Fig. 6.8 presents the considered filters. The resonances of the filters may result in instabilities of the converter [87] and, thus, in practice a damping branch has to be considered [87, 141, 151]. For the comparison of the different filter stage numbers, the damping branch can be neglected as the required filter inductor size is the decisive argument for the selection. Each filter in **Fig. 6.8** is symmetrical with respect to line and neutral wires and hence an additional stage always requires two more inductors.

The single-stage filter, cf. **Fig. 6.8** (a), requires two large inductances ($L_{\mathrm{DM}} = 8.9\,\mathrm{mH}$) as the attenuation only increases by 40 dB/decade. The filter transfer function is also depicted in the figure which shows that the cut-off frequency of the filter is very low ($f_{\mathrm{c}} = 1.9\,\mathrm{kHz}$) and may interfere with the current control, due to a control bandwidth of 2 kHz, cf. Section 4.5. In a 2-stage filter, cf. **Fig. 6.8** (b), the required inductance is significantly reduced

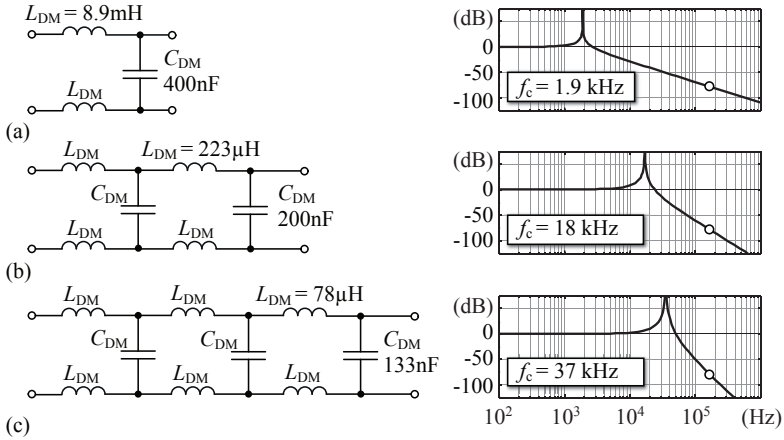


Fig. 6.8: Comparison between different numbers of stages for the DM filter. Each filter is designed for the desired attenuation of $Att_{\mathrm{req}} = 76\,\mathrm{dB}$ at $f_{\mathrm{d}} = 160\,\mathrm{kHz}$ with a total DM capacitance of $C_{\mathrm{DM,tot}} = 400\,\mathrm{nF}$.

($L_{\mathrm{DM}} = 223\,\mu\mathrm{H}$) which simplifies the PCB-integration considerably. Furthermore, the cut-off frequency is shifted to $f_{\mathrm{c}} = 18\,\mathrm{kHz}$. However, these benefits come at the expense of two more inductors. The inductors of a 3-stage filters require an inductance value of only $L_{\mathrm{DM}} = 78\,\mu\mathrm{H}$.

Considering that the volume of an inductor is proportional to the inductance value [84],

$$V_{\mathrm{L}} \propto L, \tag{6.8}$$

it can be seen that the six inductors of the 3-stage filter require half the volume compared to inductors of a 2-stage filter and with a sophisticated and automatic manufacturing and integration process the cores can easily be embedded into the PCB. In the case at hand, however, where the available material has been limited in type and quantity of the magnetic tape and the core construction has been kept as simple as possible the lower number of cores has been argument enough to go for a 2-stage filter. Therefore, the chosen number of stages for the DM filter is 2 and the required filter inductance is

$$L_{\mathrm{DM}} = 223\,\mu\mathrm{H}. \tag{6.9}$$

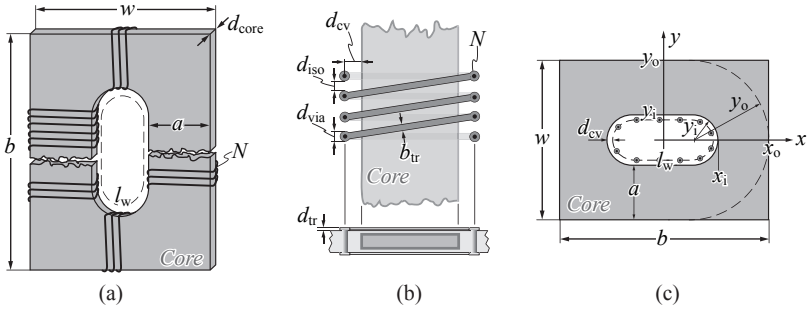


Fig. 6.9: Illustration of the model used to design the DM inductor. (a) Core shape, (b) winding structure, and (c) model and denominations of the geometrical properties of the design.

6.2.5 Design of the DM filter inductor

The inductor design of a filter choke is different compared to the design presented in Chapter 5 because the objectives change. For the boost inductor and the flyback transformer the major concerns are core losses, due to large HF flux excitations of the cores. These core losses define the efficiency and the required sizes of the components. The current in a DM EMI filter inductor, however, primarily consists of the mains frequency component [84, 111]. Therefore, contrary to HF inductors, the magnetic design is determined by the saturation flux density rather than by a thermal limit imposed by high core losses which simplifies the design of the filter inductor considerably.

The scalable model used to design the DM inductor is shown in **Fig. 6.9**. The width w of the employed VITROVAC 6155F tape is 35 mm and in order to simplify the manufacturing of the cores, it is considered to be constant and thus no design parameter. Due to the symmetrical core geometry, the remaining design parameters are

- the core length b,
- the leg width a, and
- the number of turns N.

Since no air gap is considered in order to prevent the resulting fringing flux to couple the EMI noise to filter elements close to the inductor an important parameter to adjust the core reluctance is missing.

Furthermore, an increase in the core length b would result in a large inductor and thus, b will be set to the minimal possible value which is determined by the minimal required winding window size. The leg width a and the number of turns N remain to determine the desired inductance.

The leg width a can be varied between two boundaries. The lower bound is defined by the saturation flux density $B_{\max}$. For it, the minimal required a, $a_{\min}$, is calculated similar to the approach presented in Section 5.2.3. The upper bound $a_{\max}$ is determined by the core width w and the minimum required winding window to place two vias next to each other in the y-axis, cf. **Fig. 6.9** (c),

$$a_{\max} = \frac{1}{2} \cdot (w - (2\,d_{\mathrm{cv}} + 2\,d_{\mathrm{via}} + d_{\mathrm{iso}}))\,. \tag{6.10}$$

The design procedure is presented in **Fig. 6.10** which is a simplified version of the procedure presented in Chapter 5. In a first step, the track width b_{tr} and the via diameter d_{via} are determined by the applied RMS current I, the allowable current density $J_{\max}$, and the track thickness d_{tr}, cf. **Fig. 6.9** (b). Then, the maximum allowed leg width $a_{\max}$ is calculated according to (6.10). The next step determines the parameters y_{i} and x_{i} as a function of x_{o} in order to provide enough space for the vias in the winding window. Now the minimal leg width $a_{\min}$ can be derived with respect to the maximum allowed flux density $B_{\max}$ and finally, the reluctance of the core, $\mathcal{R}_{\mathrm{c}}$, is calculated by using the model presented in **Fig. 5.16** [135]. With it, the required a for a given N is determined and if $a_{\min} \leq a \leq a_{\max}$ holds true the design is valid.

The design procedure of **Fig. 6.10** is executed for the input parameters defined in **Tab. 6.2** and for $N = 32 \ldots 50$. For a lower number of turns no solution can be found as a would be too large and thus the winding window too small. **Fig. 6.11** (a) plots the core length over the number of turns and it can be seen that the minimal required length $b_{\min} = 55.63\,\mathrm{mm}$ can be found for $N = 34$.

The reason why there is a minimum is that with increasing N the leg width a can be reduced for a given L_{DM} ($L_{\mathrm{DM}} \propto N^2 \cdot a$). A smaller a increases the winding window and the core length b is thus decreasing for $N = 32 \ldots 34$. For $N > 34$ and for constant b, the relevant circumference in the winding window, cf. **Fig. 6.9** (c), still increases due to the smaller a, however, this increase is insufficient to place the additional vias and therefore b needs to be increased. However, it should be noted that $b_{\min}$ is only slightly smaller than the core length $b = 55.76\,\mathrm{mm}$ at

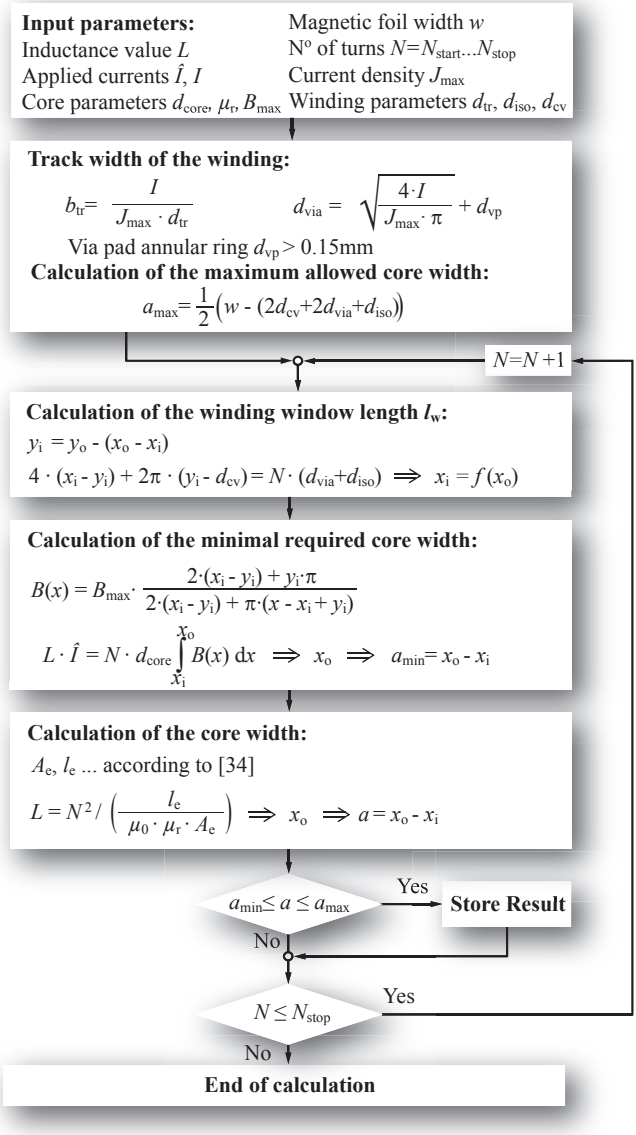


Fig. 6.10: Design procedure of the DM inductor. The corresponding model is depicted in **Fig. 6.9**.

Tab. 6.2: Input parameters for the design procedure of the DM filter inductor.

L_{DM}	=	223 µH	w	=	35 mm
$\hat{I}$	=	400 mA	N	=	32 . . . 50
I	=	250 mA	$J_{\max}$	=	40 A/mm^2
d_{core}	=	0.6 mm	d_{tr}	=	35 µm
$B_{\max}$	=	800 mT	d_{iso}	=	0.5 mm
μ_{r}	=	1900	d_{cv}	=	1.2 mm

Tab. 6.3: Resulting parameters of the DM filter inductor.

$b_{\mathrm{tr,calc}}$	=	0.18 mm	$d_{\mathrm{via,calc}}$	=	0.25 mm
$b_{\mathrm{tr,appl}}$	=	0.7 mm	$d_{\mathrm{via,appl}}$	=	0.9 mm
a	=	14.23 mm	b	=	56 mm
N	=	32	Size:		39 × 60 mm

$N = 32$ and, since the cores are manually manufactured, this difference is within the tolerance of the implementation. Since the parasitic capacitance increases with the number of turns, the lowest number of turns, $N = 32$, is considered to be most suitable.

The EMI filter board has been manufactured in-house and therefore the tight limits which would be possible for professional PCB manufacturing could not be applied. The track width b_{tr} and the diameter of the vias, d_{via}, are thus determined by the manufacturing limits; the calculation would allow for a smaller track width and a smaller via diameter. **Tab. 6.3** lists the resulting parameters including the calculated and the applied values for b_{tr} and d_{via}. Thus, the prototype inductor is larger than actually necessary. With cutting-edge PCB manufacturing limitations the DM inductor would require a footprint size of only

$$A = 39 \times 36\,\mathrm{mm}^2. \tag{6.11}$$

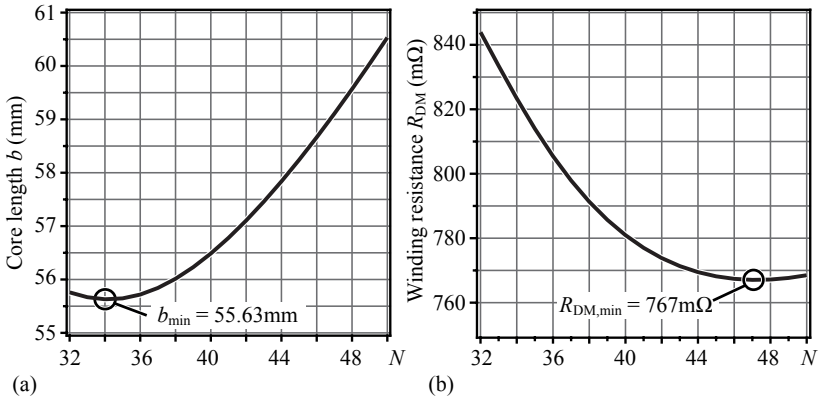


Fig. 6.11: (a) Core length and (b) winding resistance of the DM filter inductor as a function of the number of turns.

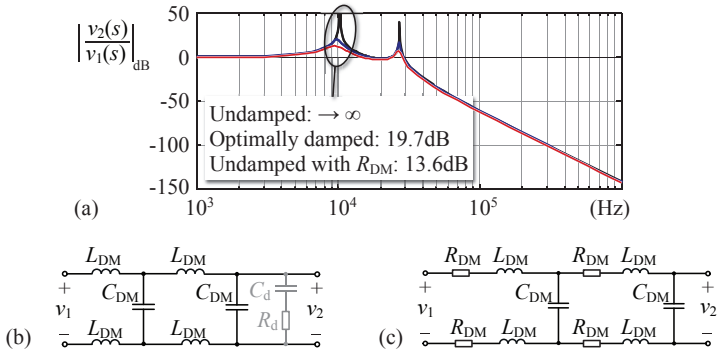


Fig. 6.12: (a) Transfer function of the filter without, with optimal, and with parasitic damping. (b) Filter structure without and with (indicated in gray) damping branch. (c) Filter structure which considers the resistances of the windings as damping elements.

6.2.6 Damping of the DM filter

A DM filter requires sufficient damping, e.g. for being immune against disturbances or distortions in the grid which could excite the filter resonances. Numerous publications deal with this issue in order to obtain the optimal damping with respect to a certain goal [87, 141, 151].

The inductors of the PCB-integrated EMI filter consist of a winding which is realized as tracks and vias, cf. **Fig. 6.9** (b). Due to the small cross-sectional area of the tracks the resistance of the winding is considerably larger compared to conventional EMI inductors composed of either solid copper or litz wire windings. **Fig. 6.11** (b) plots the winding resistance over the number of turns. The occuring minimum is for the same reason as the minimum of the core length b, i.e. the reduction of a for an increasing N decreases the winding length and compensates the length of the additional windings. At $N = 47$, the minimal winding resistance $R_{\mathrm{DM,min}} = 767\,\mathrm{m\Omega}$ is obtained and for $N > 47$ the winding length and thus R_{DM} increases.

For the designed inductor the calculated Dc resistance is $R_{\mathrm{DM}} = 843\,\mathrm{m\Omega}$ and the measurement shows a resistance of $1.15\,\Omega$ which is slightly higher due to soldering connections. The calculation is based on the applied winding parameters $b_{\mathrm{tr,appl}}$ and $d_{\mathrm{tr,appl}}$, cf. **Tab. 6.3**.

In order to investigate the impact of the large R_{DM} on the filter's transfer function, the undamped filter, an optimally damped filter, cf. **Fig. 6.12** (b), and the parasitically damped filter, cf. **Fig. 6.12** (c), are compared to each other. For it, the damped filter has been optimized with respect to maximize the mains side input impedance according to [141]. The damping branch consisting of $C_{\mathrm{d}} = 100\,\mathrm{nF}$ and $R_{\mathrm{d}} = 200\,\Omega$ are therefore, considered at the first filter stage, cf. **Fig. 6.12** (b).

Fig. 6.12 (a) presents the obtained transfer functions. As can be seen, the damping due to R_{DM} results in an already well damped transfer function and no additional damping branch is needed for the PCB-integrated EMI filter. The winding losses imposed by the DM filter inductors are reasonably small due to the small input current of $I = 250\,\mathrm{mA}$,

$$P_{\mathrm{v,DM}} = 4 \cdot R_{\mathrm{DM}} \cdot I^2 = 290\,\mathrm{mW}. \tag{6.12}$$

6.3 Design of the common mode filter

The design of the CM filter is similar to the design of the DM filter. The considerations required for the DM stage have also to be made for the CM filter in order to obtain a proper filter topology and the parameters of the components.

6.3.1 Determination of the CM capacitance

The maximum current allowed to flow through CM capacitances at 110 % of the input voltage is limited to be $I_{\mathrm{Gnd}} \leq 3.5\,\mathrm{mA}$ [31]. The total CM capacitance is thus restricted to be

$$C_{\mathrm{CM,tot}} \leq \frac{I_{\mathrm{Gnd}}}{1.1 \cdot V_{\mathrm{n}} \cdot \omega} = \frac{3.5\,\mathrm{mA}}{1.1 \cdot 230\,\mathrm{V} \cdot 2\pi \cdot 50\,\mathrm{Hz}} = 44\,\mathrm{nF}. \qquad (6.13)$$

The capacitors applied between the line or the neutral wire to the earth wire are referred to as Y capacitors and they must be rated in order to fulfill the safety standards specified in [152]. Class Y ceramic chip capacitors are commercially available [41]; however, the height of the chips exceeds 1 mm. The SMD chips specified in **Tab. 6.4** have been applied for the realized EMI filter.

6.3.2 Magnetic material applied for the CM inductors

As already mentioned in Section 6.2.2, only amorphous or nanocrystalline materials remain for the PCB-integration of the core. CM chokes are typically realized like transformers with a large but finite magnetizing inductance. Assuming an ideal coupling between the two windings the flux components caused by the comparably large DM currents cancel each other and therefore only the CM current imposed flux has to be considered for the design of the choke. Since CM currents are small with respect to the amplitude of DM currents a highly permeable material can be employed without causing the core to be saturated.

VITROPERM 500F by VACUUMSCHMELZE is a nanocrystalline core material and is widely used for CM chokes due to its good HF behavior and the high saturation flux density. Although nanocrystalline

Tab. 6.4: Applied CM capacitors from Murata [41].

Capacitance	4.7 nF / 250 $\mathrm{V_{rms}}$
Size	$5.7 \times 5.0 \times 2.0\,\mathrm{mm^3}$
Rating	Class Y2, X1/Y2 [152]
Testing	Impulse: 5 kV
	1000 h test: 1425 V / 100 ms every hour

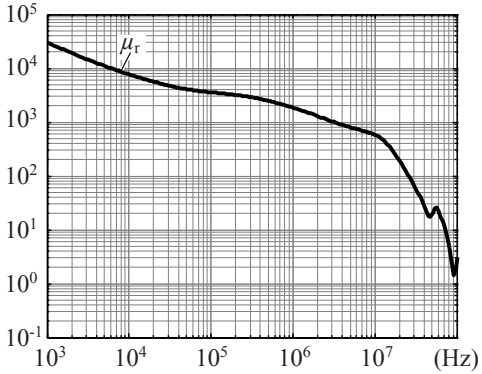


Fig. 6.13: Measured real part of the permeability of 2714A by Metglas [127].

materials come in thin tapes and are applicable to a PCB-integration process, they need to be annealed and after the annealing they are very brittle and not processable anymore. Only the manufacturer could shape the core prior to the annealing process which, however, is very elaborate for small-scale production.

Due to its availability cobalt-based 2714A by Metglas [127] has been chosen as core material of the CM chokes which is aimed for HF applications. **Tab. 5.2** lists important parameters of the material including the saturation flux density of $B_{\mathrm{sat}} = 570\,\mathrm{mT}$. The frequency behavior of the permeability is given in the datasheet for different flux densities. According to the datasheet, a permeability $\mu_{\mathrm{r}} = 5000$ has been considered in the design of the CM inductors. However, the measurement of the permeability on a toroidal core ($d_{\mathrm{o}} = 33\,\mathrm{mm}$, $d_{\mathrm{i}} = 32\,\mathrm{mm}$, $h = 50\,\mathrm{mm}$, $N = 20$) depicted in **Fig. 6.13** only shows a value of $\mu_{\mathrm{r}} = 2000$ at $f_{\mathrm{d}} = 160\,\mathrm{kHz}$ and the permeability drops considerably with increasing frequency. As will be shown, the CM filter inductors feature a too small inductance which is also based on the overrated permeability. In a redesign, the measured values have to be applied instead of the information given in the datasheet.

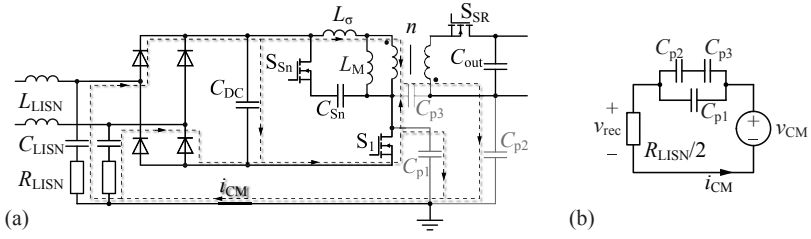


Fig. 6.14: (a) Propagation paths of the CM noise and CM capacitances included in the simulation model (indicated in gray). (b) Resulting simplified CM equivalent circuit.

6.3.3 Required CM filter attenuation

The determination of the required filter attenuation for the common mode filter is done similar to the DM filter. The CM noise is obtained using a simulation. For it, the CM propagation paths, i.e. the parasitic capacitances to the earth wire, need to be included in the simulation model.

For the CM noise determination the simulation model depicted in **Fig. 6.5** (a) has been applied whereas S_{CM} is closed. **Fig. 6.14** (a) details the propagation paths of the CM current i_{CM}. The parasitic capacitors C_{p1} and C_{p2} are each assumed to be 10 pF which is a reasonable choice considering that no heat sink is used. The interwinding capacitance of the flyback transformer, $C_{p3} = 106\,\text{pF}$, has been measured with an impedance analyzer.

Fig. 6.14 (b) shows a simplified CM equivalent circuit where the LISN is modeled with a 25 Ω resistance [146]. The voltage v_{rec} applied to $R_{LISN}/2$ defines the CM noise level. Thus, in the simulation the current i_{CM} is multiplied with 25 Ω and applied to the EMI test receiver model, see **Fig. 6.5** (d). The resulting noise spectrum is depicted in **Fig. 6.15**. Analogous to the DM filter design, the design frequency is $f_d = 160\,\text{kHz}$ where a noise level of $NL = 103\,\text{dB}\mu\text{V}$ is estimated. In order to meet Class B and including a safety margin of 8 dB the required attenuation, cf. (6.4), is

$$Att_{req}(160\,\text{kHz}) = 103\,\text{dB}\mu\text{V} - 66\,\text{dB}\mu\text{V} + 8\,\text{dB} = 45\,\text{dB}. \qquad (6.14)$$

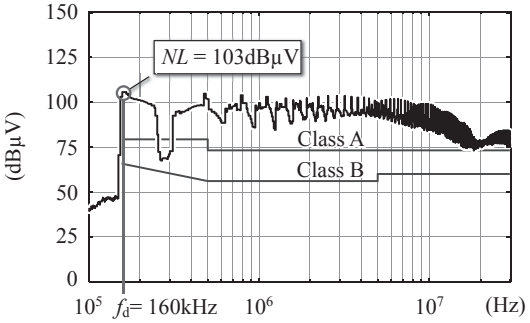


Fig. 6.15: Simulated common mode noise.

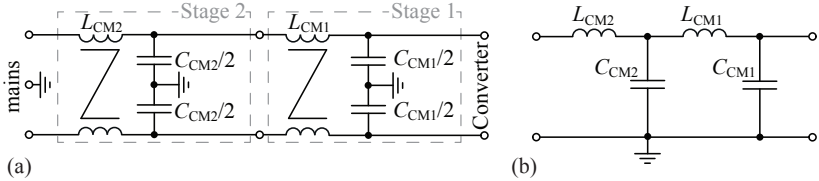


Fig. 6.16: (a) 2-stage common mode filter. (b) Equivalent circuit of the CM filter used to design each component.

6.3.4 CM filter topology

The number of stages is determined similar to the DM filter where the size of the inductors and the number of PCB-integrated cores are the decisive arguments. The analysis shows that a 2-stage CM filter results in reasonable inductor sizes at only two cores to be integrated into the PCB, cf. **Fig. 6.16**.

Contrary to the DM filter, the CM stages are not identical but different attenuation levels for the first and the second filter stage are employed. This allows for two different CM inductors and thus different parasitic capacitances. The smaller CM choke will have a higher resonance frequency due to the lower number of turns and the HF noise will be attenuated mostly by this filter stage.

The attenuation of each stage is chosen with respect to reasonable CM choke sizes:

$$Att_{\mathrm{CM1}} = 30\,\mathrm{dB}, \qquad Att_{\mathrm{CM2}} = 15\,\mathrm{dB}. \tag{6.15}$$

The spreading of the CM capacitance is also to be chosen and in order to reduce the choke size of filter stage 1 the capacitance C_{CM1} is slightly larger than C_{CM2}:

$$C_{\mathrm{CM1}} = 24\,\mathrm{nF}, \qquad C_{\mathrm{CM2}} = 20\,\mathrm{nF}. \tag{6.16}$$

With (6.7) and

$$L_{\mathrm{CM}i} = \frac{1}{(2\pi f_{\mathrm{c}})^2 \cdot C_{\mathrm{CM}i}}, \tag{6.17}$$

the required CM filter inductances are:

$$L_{\mathrm{CM1}} = 1.5\,\mathrm{mH}, \qquad L_{\mathrm{CM2}} = 323\,\mu\mathrm{H}. \tag{6.18}$$

6.3.5 Design of the CM filter inductor

Similar to the DM inductor design, CM inductors have been designed according to **Fig. 6.10**. The tape width of the 2714A material is $w = 50\,\mathrm{mm}$. Since the setup of a CM choke is similar to a 1:1 transformer, enough space needs to be allocated in the winding window for both windings. Therefore, the required winding window size is determined by double the number of turns contrary to the DM inductor design. The transformer setup allows for the cancellation of the DM currents and the resulting magnetizing current $\hat{I}$ is much lower than for the DM inductors. $\hat{I}$ has been determined using the simulation model presented in **Fig. 6.5**. The RMS current of the CM inductor, I, is basically the input current of the converter and thus identical to the DM inductor design.

Tab. 6.5 lists the input parameters for the design procedure and **Tab. 6.6** shows the obtained parameters for the core. The results for the track width and the via diameter are identical for the DM and the CM inductors.

The Dc resistances of the CM inductors are calculated to be $R_{\mathrm{CM1}} = 3.6\,\Omega$ and $R_{\mathrm{CM2}} = 2.2\,\Omega$ (measured: $R_{\mathrm{CM1}} = 4.8\,\Omega$, $R_{\mathrm{CM1}} = 2.9\,\Omega$). The losses in the CM chokes, calculated with measured resistances, are

$$P_{\mathrm{v,CM}} = I^2 \cdot (R_{\mathrm{CM1}} + R_{\mathrm{CM2}}) = 481\,\mathrm{mW}. \tag{6.19}$$

Tab. 6.5: Input parameters for the design procedure of the CM filter inductors $L_{\mathrm{CM},1}$ and $L_{\mathrm{CM},2}$.

$L_{\mathrm{CM}i}$	=	1.5 mH/323 µH	w	=	50 mm
$\hat{I}$	=	50 mA	N	=	$2 \cdot (15 \ldots 52)$
I	=	250 mA	$J_{\max}$	=	40 A/mm^2
d_{core}	=	0.6 mm	d_{tr}	=	35 µm
$B_{\max}$	=	570 mT	d_{iso}	=	0.5 mm
μ_{r}	=	5 000	d_{cv}	=	1.2 mm

Tab. 6.6: Resulting parameters of the CM filter inductors.

L_{CM1}	a	=	20 mm	b	=	70 mm
	N	=	$2 \cdot 52$			
L_{CM2}	a	=	18 mm	b	=	50 mm
	N	=	$2 \cdot 24$			

6.4 Measurement results

After each component of the EMI filter is designed the filter has been implemented. **Fig. 6.17** shows the filter board which has been realized based on the circuit diagram also indicated in the figure. Each core is integrated into the 2-layer PCB and the DM capacitors are composed of five parallel connected 56 nF chip capacitors, i.e. $C_{\mathrm{DM,appl}} = 280\,\mathrm{nF}$ is applied instead of $C_{\mathrm{DM}} = 200\,\mathrm{nF}$, in order to partly compensate the capacitance drop of 41 % at high voltages. The transfer functions of the DM and the CM stages have been measured using a frequency response analyzer (Bode100 by Omicron Lab [157]).

DM filter

The measured DM transfer function is compared to an analytical model, see **Fig. 6.18** (c), which includes the parasitic components of the DM capacitors and the Dc resistance of the DM inductors. The values of the parasitic components are obtained by fitting the calculated transfer function to the measured curve. **Fig. 6.5** (b) shows the obtained values

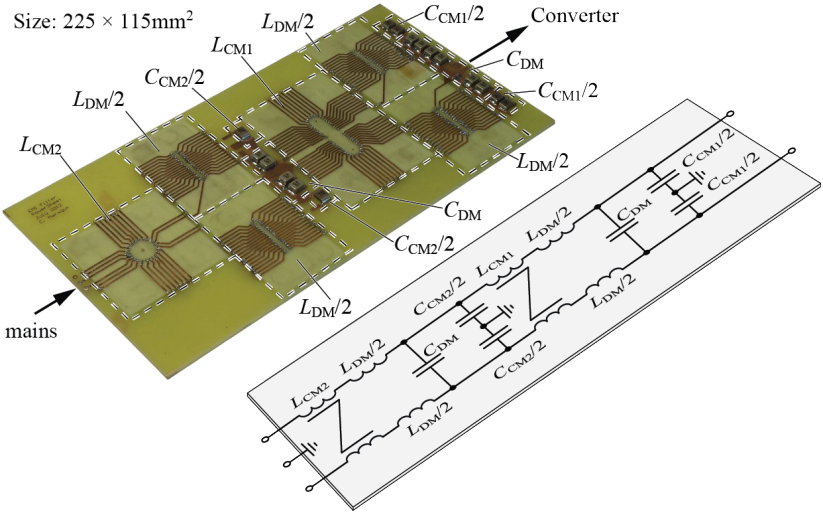


Fig. 6.17: Photography and schematic of the implemented EMI filter.

for the DM capacitor.

Comparing the measured DM transfer function with the result of the model shows good agreement for frequencies up to 500 kHz, cf. **Fig. 6.18** (a). For higher frequencies, the measured waveform deviates considerably from the analytical model which is caused by the frequency dependency of the filter inductors L_{DM}. At $f_{\mathrm{d}} = 160\,\mathrm{kHz}$ the filter attenuation is only $-70.15\,\mathrm{dB}$, cf. $Att_{\mathrm{req}}(f_{\mathrm{d}}) = -76\,\mathrm{dB}$, and at frequencies above 500 kHz the attenuation is decreasing.

In order to include the frequency dependency of the permeability a gyrator model can be applied [158], cf. **Fig. 6.18** (d). The gyrator model depicted in **Fig. 6.19** models a magnetic circuit with capacitances, resistances, and controlled sources. Contrary to a conventional reluctance model, the dependency of the reluctance on the frequency or the applied current can be considered. As indicated in **Fig. 6.19**, the permeance $\mathcal{P}$ is modeled as a capacitance; $\mathcal{P}_0$ denotes the permeance of the core without matter, i.e. $\mu_{\mathrm{r}} = 1$, and the other four branches are used to model the frequency dependend permeability with different time constants which are matched to an impedance measurement of

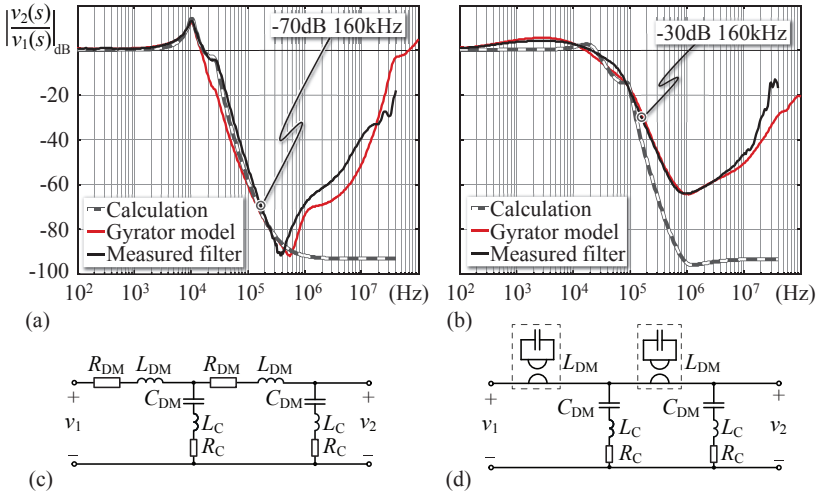


Fig. 6.18: Transfer function of (a) the DM filter and (b) the CM filter. The measurement is compared to a conventional model which includes parasitic effects and to a gyrator model which considers the frequency dependency of the permeability. (c) Schematics of the conventional filter model and (d) the gyrator model.

L_{DM}. The admittance of the $\mathcal{P}-R$ circuit is

$$Y(s) = s \cdot \mathcal{P}(s) = \frac{\dot{\Phi}(s)}{N \cdot I_{\mathrm{L}}(s)} = s\,\mathcal{P}_0 + \sum_{i=1}^{4} \frac{s\,\mathcal{P}_i}{1 + s\,\mathcal{P}_i\,R_i}. \tag{6.20}$$

The transformation to the electrical side of the model reveals that the model indeed represents a frequency dependent inductor,

$$Y(s) = \frac{s \cdot \Psi(s)}{N^2 \cdot I_{\mathrm{L}}(s)} \quad \Rightarrow \quad L(s) = N^2 \cdot \mathcal{P}(s) = \frac{\Psi(s)}{I_{\mathrm{L}}(s)}. \tag{6.21}$$

For the case at hand, a fourth order gyrator model has been considered to achieve a good match between model and impedance measurement. Applying the parameters listed in **Tab. 6.7** yields the approximation of the DM filter inductor depicted in **Fig. 6.20** (a). The gyrator model also allows an estimation of the parasitic capacitance of the inductor, C_{p}, indicated in **Fig. 6.19**. Fitting the gyrator model with C_{p} to the measured impedance yields the capacitance values for C_{p} listed in **Tab. 6.7**.

Tab. 6.7: Parameters of the gyrator models of the filter inductors. The permeances $\mathcal{P}_i$ are listed in the corresponding capacitance value which have been applied in the simulation model.

	L_{DM}	L_{CM1}	L_{CM2}
$\mathcal{P}_0 \sim C_0$	128 pF	118 pF	152 pF
$\mathcal{P}_1 \sim C_1$	54.55 nF	500 nF	875 nF
$\mathcal{P}_2 \sim C_2$	41.35 nF	10 nF	7 nF
$\mathcal{P}_3 \sim C_3$	6.28 nF	40 nF	350 nF
$\mathcal{P}_4 \sim C_4$	3.97 nF	40 nF	28 nF
R_1	0.76 Ω	6 Ω	28.6 Ω
R_2	121.2 Ω	1.6 Ω	0.43 Ω
R_3	90.94 Ω	10 Ω	2.86 Ω
R_4	15.15 Ω	20 Ω	2.28 Ω
C_{p}	8 pF	18 pF	12 pF

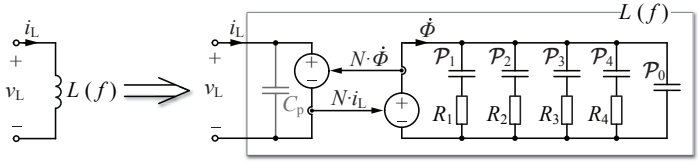


Fig. 6.19: Fourth order gyrator model of the inductor to model the frequency dependency of the core material's permeability [158].

As can be seen in **Fig. 6.20** (a), an ideal inductor overestimates the impedance already for frequencies around the design frequency f_{d}. This indicates that eddy currents in the core partly compensate the magnetic field and compromise the impedance of the inductor [159]. Although the magnetic foils are isolated using an isolation lacquer short-circuits between the sheets may still occur either at spots where the isolation of the lacquer is broken or at the edges of the core due to a burr which results from the stamping of the winding window, cf. **Fig. 6.21**. This burr can only be avoided with sophisticated core manufacturing techniques, e.g. laser cutting of each separate sheet. It has to be noted, that the permeability measurement of VITROVAC 6155F, cf. **Fig. 6.4**,

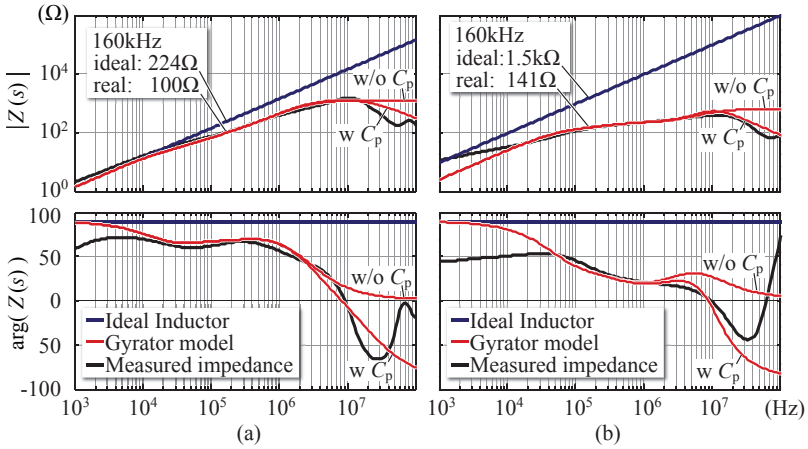


Fig. 6.20: Approximation of the impedance with the gyrator model: (a) DM inductor (Material VITROVAC 6155F, $L_{DM} = 223\,\mu H$). (b) CM choke (Material 2714A, $L_{CM1} = 1.5\,mH$). The characteristic resulting from the gyrator model is shown with and without considering a parasitic capacitance C_p, cf. **Fig. 6.19**.

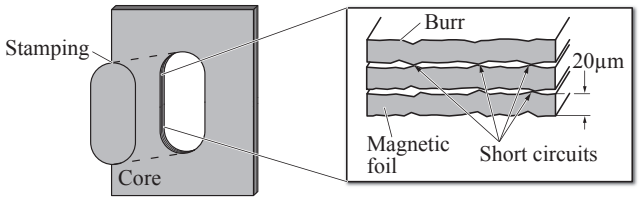


Fig. 6.21: Short circuits between the magnetic foils may occur at the edge of the winding window.

shows an about constant permeability up to almost 1 MHz and therefore a significantly better frequency behavior than material 2714A.

Fig. 6.22 (a) presents an inductor setup employing a toroidally wound core, cf. **Fig. 5.2** (b), made of VITROVAC 6155F. The inductor has actually been designed for a SEPIC converter, however, the specifications are similar to the required DM inductor. Contrary to the DM filter chokes presented in **Fig. 6.20** (a), the frequency behavior of an ideal and the measured toroidal inductor agree very well only up to a

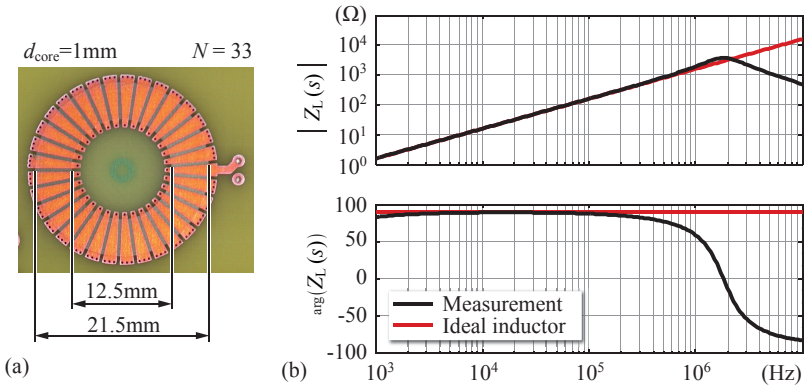


Fig. 6.22: (a) Implementation of a toroidally wound core (VITROVAC 6155F, $L = 252\,\mu H$, $I_{sat} = 0.8\,A$). (b) Impedance measurement.

frequency of 1 MHz, cf. **Fig. 6.22** (b). So, the permeability of the implemented DM filter inductors must be compromised by eddy currents in the sheets.

Toroidally wound cores (cf. **Fig. 5.2** (b)) are implemented with sophisticated cutting and winding techniques by the material manufacturer. The technique itself is proprietary but it is known that the magnetic tape is laminated with a specific isolation layer which allows for a high core filling factor of $k_{fe} = 0.9$ and the cutting method does not yield a burr. Thus, the resulting cores do not suffer from an eddy current caused impedance degradation and would be beneficial for the implementation of an ultra-flat EMI filter. Therefore, Section 6.5 presents a redesign of the EMI filter considering toroidally wound cores.

CM filter

The same measurements and investigations like for the DM filter have been conducted for the CM filter stage and the respective transfer functions are printed in **Fig. 6.18** (b). As can be seen, the frequency dependency of the inductances is even more pronounced than for the DM inductors and is caused by the vast decrease of the permeability for increasing frequencies for the material 2714A, cf. **Fig. 6.13**.

Fig. 6.20 (b) shows the impedance measurement of L_{CM1} and

the approximation obtained by the gyrator model (parameters listed in **Tab. 6.7**). The deviation between ideal and real inductor is large (over a factor of ten at f_d) and, thus, the attenuation of the filter is too low to meet the specifications. Instead of the targeted attenuation of $Att_\mathrm{req} = -45\,\mathrm{dB}$ at $f_\mathrm{d} = 160\,\mathrm{kHz}$ the CM filter only features $-30\,\mathrm{dB}$. The approximation of the parasitic capacitance yields the values $C_\mathrm{p1} = 18\,\mathrm{pF}$ and $C_\mathrm{p2} = 12\,\mathrm{pF}$ for the two CM chokes.

Fig. 6.20 (b) indicates that 2714A is not an appropriate material for a PCB-integrated CM choke. Therefore, it is proposed to use VITROPERM 500F [126] for an improved version of the CM choke. This material features a high permeability over a wide frequency range, cf. **Fig. 6.29**, and would thus be considerably more suitable for PCB-integrated CM filter inductors. A redesign of the CM filter employing VITROPERM 500F is presented in Section 6.5.

EMI simulations and measurements

The simulations of DM and CM noise without filter have already been applied to determine the required filter attenuation. For the sake of completeness, **Fig. 6.23** (a) and (b) show the respective simulations and (c) presents an estimation of the total conducted EMI noise which is calculated with

$$\text{Total noise}\,[\mathrm{dB\mu V}] = 20 \cdot \log_{10}\left(\frac{\text{DM noise}\,[\mathrm{V}] + \text{CM noise}\,[\mathrm{V}]}{1\,\mu\mathrm{V}}\right). \tag{6.22}$$

In **Fig. 6.23** (c) also the measured EMI noise is presented on top of the simulation result. As can be seen, the measured noise at 160 kHz is 8 dB higher than the value predicted by the simulation model. The deviation is mainly caused by the underestimation of the voltage dependend capacitance derating of C_DC (cf. **Fig. 6.5** (a)) which is similar to the derating discussed in Section 6.2.1. For that reason the difference between simulation and measurement is maximal at 160 kHz because the maximum voltage applied to C_DC occurs at $f_\mathrm{S} = 160\,\mathrm{kHz}$ (cf. **Fig. 4.15** (b)).

Fig. 6.24 presents the EMI spectra of the converter with applied EMI filter. The simulation of the EMI filter is based on the gyrator model, see **Fig. 6.5**. As can be seen in **Fig. 6.24** (a), the DM noise is slightly violating the Class B limit due to the reduced attenuation. The simulation result indicates that the CM noise is causing the high EMI

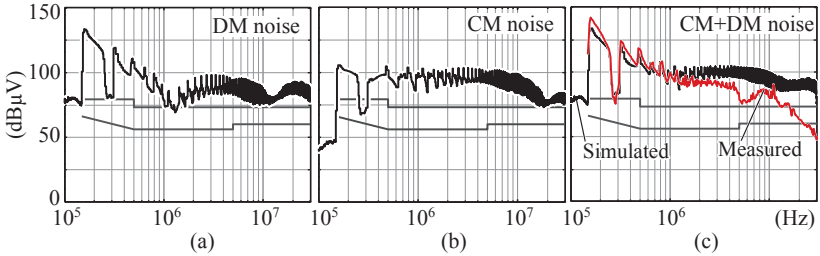


Fig. 6.23: (a) Simulated DM EMI noise, (b) simulated CM EMI noise, and (c) simulated and measured total EMI noise. The simulations and the measurement are done without the filter applied.

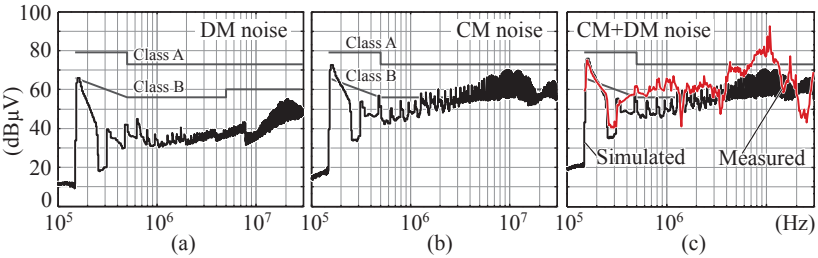


Fig. 6.24: (a) Simulated DM EMI noise, (b) simulated CM EMI noise, and (c) simulated and measured total EMI noise. The simulations and the measurement are done with the EMI filter applied. The simulation is based on the gyrator model for the filter inductors.

noise level, cf. **Fig. 6.24** (b) and (c). At f_d the simulation fits well to the measurement but with increasing frequencies the model underestimates the noise. In order to obtain a better match, the CM model must also include the connection between filter and converter, the cable to load, and the load itself [84, 146].

For the sake of integrity the EMI measurements over the entire frequency range between 150 kHz and 30 MHz is depicted in **Fig. 6.25**.

6.5 Redesign of the EMI filter

The implemented EMI filter fails to comply with the required standard because the filter inductors feature a too low impedance at high fre-

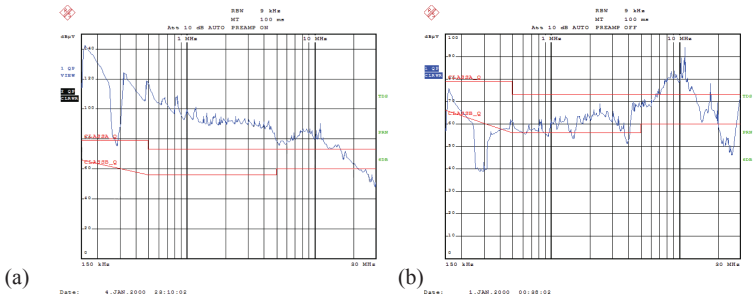


Fig. 6.25: (a) Measured EMI noise without filter. (b) Measured EMI noise with applied filter.

quencies. In this section the results and the experience obtained from the first prototype is used to redesign the EMI filter. Up-to-date PCB manufacturing techniques are considered and sophisticated cores implementation methods offered by the manufacturer are assumed to be available which obviously yields a much better inductor performance, cf. **Fig. 6.22**. The design process is done similary to the prototype design.

The voltage applied to the EMI test receiver, v_{rec}, cf. **Fig. 6.1**, consists of the DM noise voltage and the CM noise voltage:

$$v_{\mathrm{rec}}(f) = v_{\mathrm{DM}}(f) + v_{\mathrm{CM}}(f). \tag{6.23}$$

If both noise voltages, $v_{\mathrm{DM}}(f)$ and $v_{\mathrm{CM}}(f)$, are equally high the worst case of superposition with regard to the phase between the two voltages is

$$|v_{\mathrm{rec}}| = |v_{\mathrm{DM}}| + |v_{\mathrm{CM}}| = 2 \cdot |v_{\mathrm{CM}}| = 2 \cdot |v_{\mathrm{DM}}|. \tag{6.24}$$

This might result in a violation of the specified limit although DM and CM noise separately fulfill the limit. Therefore, in the redesign of the EMI filter an additional safety margin of 6 dB (corresponding to a factor 2) is considered.

DM filter

The simulation model depicted in **Fig. 6.5** has been improved by considering the degradation of C_{DC} and the resulting DM noise level is

$NL = 138\,\mathrm{dB\mu V}$ at 160 kHz. Referring to (6.4) and including the additional safety margin of 6 dB yields the required attenuation of

$$Att_{\mathrm{req,DM}}(160\,\mathrm{kHz}) = 138\,\mathrm{dB\mu V} - 66\,\mathrm{dB\mu V} + 8\,\mathrm{dB} + 6\,\mathrm{dB} = 86\,\mathrm{dB}. \tag{6.25}$$

For the redesign a 3-stage filter topology has been considered as it allows for smaller filter inductors, cf. Section 6.2.4. The total DM capacitance is still $C_{\mathrm{DM,tot}} = 400\,\mathrm{nF}$ and thus, each filter stage features $C_{\mathrm{DM}} = 133\,\mathrm{nF}$. Considering (6.7) and (6.6), the DM inductance value results to be

$$L_{\mathrm{DM}} = 115\,\mu\mathrm{H}. \tag{6.26}$$

Applying the design procedure depicted in **Fig. 6.10** to a toroidally wound core for the input parameters listed in **Tab. 6.2** but for an inductance of 115 µH yields the inductor design given in **Tab. 6.8**, where r_{i} and r_{o} account for the inner and the outer radius of the toroid, respectively.

Tab. 6.8: Result of the DM filter inductor design calculated for a toroidally wound core (cf. **Fig. 5.2** (b)). Material: VITROVAC 6155F.

$L_{\mathrm{DM}} = 115\,\mu\mathrm{H}$	
$r_{\mathrm{i}} = 5.5\,\mathrm{mm}$	$R_{\mathrm{DM}} = 1.2\,\Omega$
$r_{\mathrm{o}} = 10\,\mathrm{mm}$	$A = 4.5\,\mathrm{cm}^2$
$N = 29$	$d_{\mathrm{core}} = 0.6\,\mathrm{mm}$

The simulation model of the DM filter is shown in **Fig. 6.26** and the calculated transfer function is presented in **Fig. 6.27**. The calculation is based on the measured permeability of VITROVAC 6155F. A gyrator model is not required as the inductor can accurately be modeled with a parallel connection of an inductor, a resistor, and a capacitor, cf. **Fig. 6.26**. The parasitic capacitance of the inductors is assumed to be $C_{\mathrm{p}} = 30\,\mathrm{pF}$ which is based on measurements on inductors with similar size, cf **Fig. 6.22**. Since the footprint size of the inductors is considerably reduced compared to the implemented filter, the parasitics of the layout will also be reduced. For comparison reasons, however, parasitic components of the CM capacitor (R_{C} and L_{C}) are similar to the filter model of the prototype depicted in **Fig. 6.18** (c).

As can be seen, the designed filter achieves the required attenuation and shows an improved damping behavior compared to the implemented

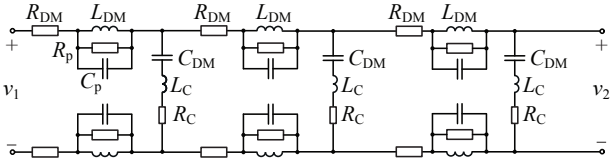


Fig. 6.26: Schematic of the considered 3-stage filter. The components in each stage are identical. (Parameters: $R_{DM} = 4\,\Omega$, $L_{DM} = 115\,\mu H$, $R_p = 5\,k\Omega$, $C_p = 30\,pF$, $C_{DM} = 133\,nF$, $R_C = 3\,\Omega$, $L_C = 1\,\mu H$).

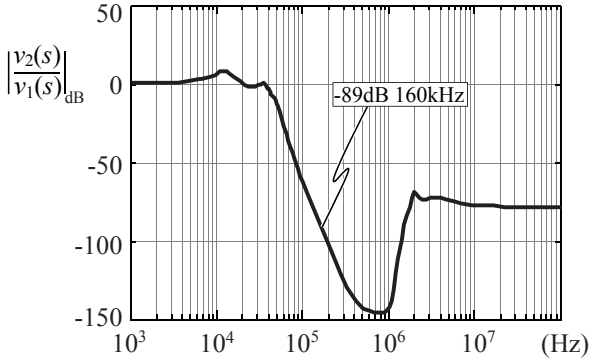


Fig. 6.27: Calculated transfer function of the 3-stage DM filter with toroidally wound cores. The calculation includes the frequency dependency of the permeability. The parasitic capacitance of the inductors is $C_p = 30\,pF$.

filter. Applying the designed filter to the simulation yields the DM noise presented in **Fig. 6.28** (a). Obviously, the DM noise is significantly reduced compared to the implemented filter, cf. **Fig. 6.24**.

CM filter

The required attenuation of the CM filter is also calculated including the additional safety margin of 6 dB,

$$Att_{req,CM}(160\,kHz) = 103\,dB\mu V - 66\,dB\mu V + 8\,dB + 6\,dB = 51\,dB. \tag{6.27}$$

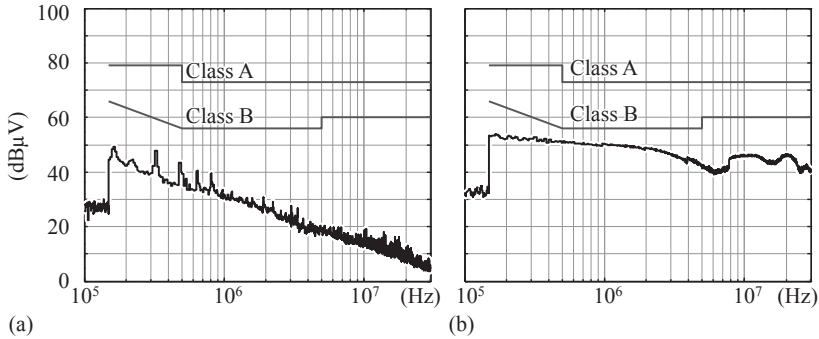


Fig. 6.28: (a) Simulated DM noise with the redesign of the EMI filter applied. (b) Simulated CM noise.

Similar to the DM filter, a three-stage filter topology is chosen. The maximum allowable CM capacitance is still $C_{\mathrm{CM,tot}} = 44\,\mathrm{nF}$. The partitioning of the required CM attenuation and the CM capacitance is chosen to be

$$\begin{aligned} &\text{Stage 1:} \quad Att_1 = 25\,\mathrm{dB}, && C_{\mathrm{CM1}} = 22\,\mathrm{nF}, \\ &\text{Stage 3:} \quad Att_2 = 15\,\mathrm{dB}, && C_{\mathrm{CM2}} = 12\,\mathrm{nF}, \\ &\text{Stage 3:} \quad Att_3 = 11\,\mathrm{dB}, && C_{\mathrm{CM3}} = 10\,\mathrm{nF}. \end{aligned}$$

Referring to (6.7) and (6.17), the CM inductances result to be

$$L_{\mathrm{CM1}} = 910\,\mu\mathrm{H}, \qquad L_{\mathrm{CM2}} = 530\,\mu\mathrm{H}, \qquad L_{\mathrm{CM3}} = 500\,\mu\mathrm{H}.$$

For the design of the CM filter inductance VITROPERM 500F is considered due to the high permeability at high frequencies. **Fig. 6.29** depicts the permeability obtained from the datasheet. Applying the inductor design procedure, cf. **Fig. 6.10**, to a toroidally wound core with a permeability of $\mu_{\mathrm{r}}(160\,\mathrm{kHz}) = 19000$ and the input parameters listed in **Tab. 6.5** yields the CM core parameters given in **Tab. 6.9**.

Since the permeability of VITROPERM 500F varies over the frequency a gyrator model according to **Fig. 6.19** has been applied to calculate the transfer function of the filter. The filter circuit is depicted in **Fig. 6.30** and the calculated transfer function is shown in **Fig. 6.31**. Similar to the DM inductor, the parasitic capacitance of the inductors are chosen based on measured results on comparable PCB-integrated

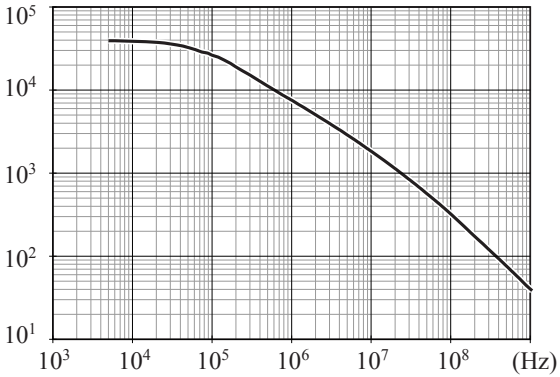


Fig. 6.29: Permeability of the VITROPERM 500F obtained from the datasheet [126].

Tab. 6.9: Result of the CM filter inductor design calculated for toroidally wound cores (Material: VITROVAC 6155F).

	L_{CM1}	L_{CM2}	L_{CM3}
L	910 µH	530 µH	500 µH
r_{i}	7.8 mm	6.4 mm	6.4 mm
r_{o}	12.5 mm	9.6 mm	9.4 mm
N	$2 \cdot 28$	$2 \cdot 22$	$2 \cdot 22$
R_{DC}	$2 \cdot 1.25\,\Omega$	$2 \cdot 0.85\,\Omega$	$2 \cdot 0.8\,\Omega$
A	$6.6\,\mathrm{cm}^2$	$4.2\,\mathrm{cm}^2$	$4.1\,\mathrm{cm}^2$

inductors. The parasitic elements of the CM capacitors are assumed to be similar to the model of the implemented CM filter. The attenuation is high even for high frequencies and the simulated CM noise, depicted in **Fig. 6.28** (b), is well suppressed.

The simulation of the filtered CM and DM EMI noise indicates that the specified Class B limit can be fulfulled with the redesigned EMI filter. The total EMI filter including all PCB-integrated inductors and the wiring would require a footprint size of

$$A = 100\,\mathrm{cm}^2. \tag{6.28}$$

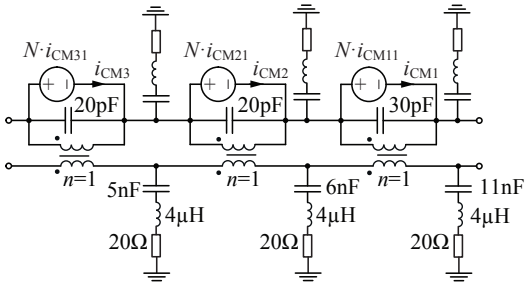


Fig. 6.30: Circuit of the calculated CM filter based on the gyrator model of the CM inductors, see **Fig. 6.19**.

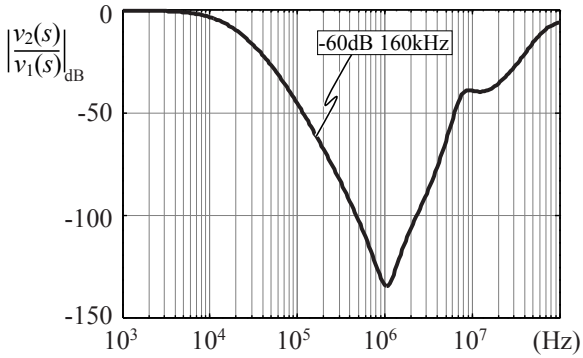


Fig. 6.31: Calculated transfer function of the CM filter with toroidally wound cores.

6.6 Conclusion

In this chapter the design of an ultra-flat EMI filter has been detailed. The filter synthesis is based on a simulation model which predicts the DM and the CM noise. The simulation based filter design offers the advantage of considering the transients during the zero-crossing of the mains voltage and allows an easy implementation of parasitic elements. Nevertheless, a proper model which includes e.g. the voltage caused capacitance degrading or an accurate EMI model of the load is necessary as otherwise the noise levels of CM and DM are underestimated.

Due to the height limitation SMD chip capacitors have to be applied

for the DM and the CM filter capacitors. Ceramic capacitors, however, suffer from a capacitance decrease with increasing applied voltage. To compensate the capacitance drop, the employed capacitors have to be checked for their voltage stability as appropriate data is usually not available. The considered ceramic chips show a capacitance drop of 40 % at 325 V and correspondingly more capacitance has to be employed. The capacitances of the DM and CM stages are limited; the DM capacitance has been limited in order to obtain a specified minimum displacement factor and the CM capacitance is limited by regimentation concerning the maximum earth current. Both limits shift the burden of the required attenuation to the filter inductors.

The material of the filter inductor core is an important issue for the PCB-integrated EMI filter. The specified filter thickness of 1 mm can only be achieved if the cores are integrated into the PCB. Conventionally used materials for EMI filter inductors, e.g. powder cores, are not applicable to the PCB-integration process and only amorphous and nanocrystalline materials remain. Due to the lack of available data for amorphous or nanocrystalline materials measurements need to be conducted to determine the permeability as a function of the frequency. Also the dependency of the permeability on the applied current might be an important issue that should be considered in the design [84].

For the DM filter inductors the core material VITROVAC 6155F has been applied which proved to show good properties up to several hundred kHz. The implementation of the core is crucial as short-circuits at the edges of the sheets may induce eddy currents which compromise the impedance of the inductor. The realized DM inductors suffer from eddy currents due to the manual manufacturing of the cores. Nonetheless, it is shown on the example of a toroidally wound core that with a sophisticated manufacturing technique the filter inductor preserves its inductance value.

The chosen material of the CM chokes is 2714A due to availability and because it is intended for HF applications. The measurement of the permeability, however, shows a continuous permeabililty drop over the frequency and the manual manufacturing resulted in short-circuits between the sheets. Thus, the impedance behavior of the implemented inductors deviates considerably from the required values. Accordingly, the filter attenuation is degraded significantly and the Class B limit of the CM noise is violated by 8 dB at 160 kHz and even more for higher frequencies. In a redesign of the filter board another material should be

employed. Among others, the nanocrystalline VITROPERM 500F would be a preferable material which features a high permeability up to several MHz.

The filter has been implemented on a 2-layer PCB board, i.e. only top and bottom layers are used for the wiring. A multi-layer board would increase the flexibility concerning wiring and shorter tracks could be placed. Since the PCB was manufactured in-house professional limits concerning tracks, clearances, and vias could not be utilized and the implemented inductors are larger than theoretically required.

Employing professionally manufactured toroidally wound cores for the filter inductors and applying VITROPERM 500F as core material for the CM inductors would allow to fully comply with the specified standard and reduce the overall size of the EMI filter to $A = 125 \times 80\,\mathrm{mm}^2$.

In summary, it can be concluded that the realization of an ultra-flat EMI filter featuring the PCB-integration of all filter inductors would comply with the EMI standards if the following steps are considered:

- Implementation of a sophisticated simulation model to accurately predict CM and DM EMI noise levels.
- Consideration of the capacitance derating at higher voltages in the design.
- Application of a sophisticated core manufacturing method in order to prevent short-circuits of between the laminations.
- Selection of a material for the CM filter choke which preserves its permeability over a wide frequency range, e.g. VITROPERM 500F.
- Selection of a low number of turns for the inductors in order to achieve a high resonance frequency.

Finally, it should be noted that a height limitation of the filter is imposed by the available Class X and Class Y capacitors which are currently 2.9 mm and 2 mm, respectively.

7 Conclusion and Outlook

7.1 Conclusion

This thesis focuses on the realization of ulta-flat converter systems aiming for a thickness of only 1 mm. In order to achieve this goal several components need to be integrated into the PCB. Apart from magnetic components and EMI filter capacitors, ultra-flat packages with $h \leq 1\,\text{mm}$ exist for power semiconductors and chip capacitors which can be directly embedded into the PCB.

Ultra-flat magnetic components for a single-phase PFC rectifier pose a major challenge to the design. In this work, a integration method is presented which is based on the PCB-integration of the core and the realization of the windings with tracks and vias. A thorough discussion about the implications imposed by the PCB-integrated core is given and a multi-objective design procedure which determines the optimal core and winding configuration with respect to the efficiency and/or the area-related power density is described. The presented procedure is a universal design tool as it is applicable to different material and different core shapes and can be used to design inductors and transformers.

Besides the PCB-integration of each component, also a proper topology selection is important. It has been concluded that a converter consisting of several subsystems is beneficial as the excellent heat removal capabilities of the ultra-flat shape can be utilized. Soft-switching is a further desired property of an ultra-flat converter as higher switching frequencies and thus smaller passive components are feasible. In that context, two systems with different component requirements are detailed: a boost-type PFC rectifier and a flyback-type PFC rectifier.

The topology and the modulation of the boost-type rectifier has been adapted in order to enable ZVS over the entire mains period. The proposed modulation, entitled *Triangular Current Mode* (TCM), requires for a detailed characterization of the switching cycle which also depends on the nonlinear output capacitance of the employed MOSFETs. In that regard, a simplified capacitance model is derived which enables a closed-form description and an analytical optimization of the TCM PFC rectifier. The results of the optimization show that the core losses of the boost inductors account for approximately 70 % of the overall losses and thus determine the efficiency and the power density of the rectifier. The discussion further addresses the implementation of the interleaving control of the inductor currents. All analytical models are validated using measurement results on a prototype of a 200 W 3-cell single-phase PFC rectifier system. The achieved efficiency and the power factor at a footprint size of $A = 347\,\mathrm{cm}^2$ are $\eta = 94.6\,\%$ and PF $= 0.993$, respectively. The thickness of the prototype is $h = 5\,\mathrm{mm}$.

The design of the flyback converter has to account for the implications of the PCB-integrated flyback transformer. In order to obtain a reasonable transformer size and particularly a reasonably low leakage inductance the system is split into six subsystems each consisting of a flyback cell. Still, the inherently large leakage inductance requires for an active snubber to recycle the energy stored in the leakage field. The applied modulation of the converter allows for ZVS of the switches. A simplified design is presented which has been aproved using an accurate analytical model, a simulation model, and measurements on a prototype of a 38 W single-phase flyback-type PFC rectifier. Similar to the TCM PFC rectifier, the transformer losses account for 80 % of the total losses. The measured efficiency and the power factor at a footprint size of $169\,\mathrm{cm}^2$ are $\eta = 76.8\,\%$ and PF $= 0.984$, respectively. All components are still placed on top of the prototype which results in a thickness of $h = 3\,\mathrm{mm}$. Embedding the chips into the PCB would allow for the required thickess of 1 mm.

The design of the EMI filter is similar to conventional converter systems. The implemention of the filter, however, poses a major challenge as the manufacturing of the cores has significant impact on the performance of the filter inductance. Measurements on an implemented prototype show that short-circuits between the magnetic foils result in an eddy-current causing inductance degradation. Employing a professionally implemented and integrated core, however, yields a good inductor

performance and would allow the EMI filter to comply with the required standards. Taking all collected experience and cutting-edge-technology manufacturing into consideration, the EMI filter for the flyback-type PFC rectifier would require a footprint area of $A = 100\,\mathrm{cm}^2$.

7.2 Outlook

For both considered converter systems, the losses and the size of the magnetic components determine the overall performance of the rectifier. The Pareto Front for either the flyback transformer or the boost inductor are thus representative for the converter efficiency and power density. An improvement of the performance can only be achieved with a corresponding improvement of the magnetic element.
The power density and the efficiency of the converter could be increased with an additional PCB layer which is available for tracks and buried vias. Although the core height d_{core} is compromised, the extra layer doubles the number of turns to be placed in the winding window. Thus, either the flux density and therefore, the core losses can be significantly reduced or a much smaller footprint size is feasible. The design procedure could be adapted in order to include the numbers of copper layers as a design parameter. Future work might also include a thorough thermal modeling of PCB-integrated components. Cutting-edge cooling methods, e.g. thermal vias, could further shift the limits of PCB-integrated systems towards a higher power density and thus, should be included in the overall system design.

The PCB-integration of the core is basically compatible to a standard PCB manufacturing process and thus, a large-scale production would be possible. Up to now ultra-flat cores, the design of the magnetic components, and the PCB-integration have not yet been investigated for the considered output power and therefore, the recognition for ultra-flat cores has been low. The achieved performance with respect to the low thickness may change this and apart from the extremely low thickness, the PCB-integration also features a robust setup with respect to applications where vibrations may deteriorate the reliability of power converters, e.g. automotive applications, because no solder connections for inductors are required which typically are the bottleneck in that regard. With the automotive industry as driving force it would be just a matter of time until PCB-integrated converter systems become off-the-shelf products.

A

Eddy current losses in stacked and toroidally wound cores

This appendix shows that for both integrated core constructions, cf. **Fig. 5.2** (a) and (b), the eddy current losses are equal. onsidering a magnetic flux in a magnetic foil of a thickness d_{foil} and a width l, cf. **Fig. A.1** (a), and following Faraday's law,

$$V = A_{\mathrm{foil}} \cdot N \cdot \frac{\mathrm{d}B}{\mathrm{d}t} \propto A_{\mathrm{foil}} = l \cdot d_{\mathrm{foil}}, \tag{A.1}$$

a voltage will be induced in the magnetic material. This voltage will cause an eddy current as indicated in **Fig. A.1**. The current depends on the resistance of the magnetic foil which is proportional to

$$R_{\mathrm{foil}} \propto \frac{l}{d_{\mathrm{foil}}}. \tag{A.2}$$

Thus, the losses caused by these eddy currents are proportional to

$$P_{\mathrm{loss}} \propto \frac{V^2}{R_{\mathrm{foil}}} \propto \frac{l^2 \cdot d_{\mathrm{foil}}^2}{l/d_{\mathrm{foil}}} = l \cdot d_{\mathrm{foil}}^3. \tag{A.3}$$

This expression gives a relation between the eddy current losses and the core geometry and will be applied to both cases of PCB-integrated inductors.

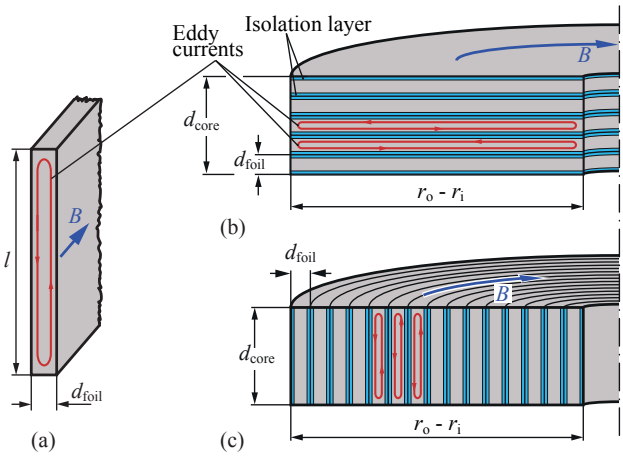


Fig. A.1: (a) Eddy currents in a simple magnetic sheet. (b) Eddy currents in a core consisting of stacked magnetic foils; (c) eddy currents in a core setup with a toroidally wound magnetic foil.

A.1 Core consisting of stacked magnetic foils

Considering **Fig. A.1** (b), the number of stacked foils for a given core thickness d_{core} can easily be calculated with

$$N_{\text{foil}} = \frac{d_{\text{core}}}{d_{\text{foil}}}. \tag{A.4}$$

This can be substituted into (A.3) and considering that the losses will now occur in N_{foil} sheets the power loss is determined with

$$P_{\text{loss}} \propto \frac{d_{\text{core}}}{d_{\text{foil}}} \cdot l \cdot d_{\text{foil}}^3 = d_{\text{core}} \cdot d_{\text{foil}}^2 \cdot (r_{\text{o}} - r_{\text{i}}). \tag{A.5}$$

A.2 Core consisting of a wound magnetic foil

For cores with a toroidally wound magnetic foil, cf. **Fig. A.1** (c), the same procedure can be applied. In order to obtain the required core width, $r_{\text{o}} - r_{\text{i}}$, whereas r_{i} and r_{o} are the inner and the outer radius of

the core, respectively, N_{foil} layers of magnetic tape are required,

$$N_{\mathrm{foil}} = \frac{r_{\mathrm{o}} - r_{\mathrm{i}}}{d_{\mathrm{foil}}}, \tag{A.6}$$

which can subsequently be substituted into (A.3):

$$P_{\mathrm{loss}} \propto \frac{r_{\mathrm{o}} - r_{\mathrm{i}}}{d_{\mathrm{foil}}} \cdot l \cdot d_{\mathrm{foil}}^3 = (r_{\mathrm{o}} - r_{\mathrm{i}}) \cdot d_{\mathrm{foil}}^2 \cdot d_{\mathrm{core}}. \tag{A.7}$$

By comparison of (A.5) with (A.7), it can be seen that the eddy current losses for both constructions are the same. This result has also been verified with 3-D FEM simulations.

B

Comparison between square and rectangular core shapes

The design procedure presented in Section 5.3 is carried out for a quadratic core shape, shown in **Fig. B.1** (a). As can be seen, the winding window is large and there might be applications where it cannot be utilized for the placement of components and the winding window space is lost.

A rectangular-shaped core configuration according to **Fig. B.1** (b) allows for a setup with smaller winding window area and the question arises how much smaller the rectangular inductor or transformer becomes. Therefore, the two core shapes are compared to each other with respect to the required footprint size.

In order to keep the analysis simple the following assumptions are considered:

- The magnetic field is concentrated in the core; i.e. no stray flux occurs in the winding window.
- The air gap length is neglected as it has minor impact on the overall size.
- The vias of the winding around the core are not considered in the determination of the footprint size.

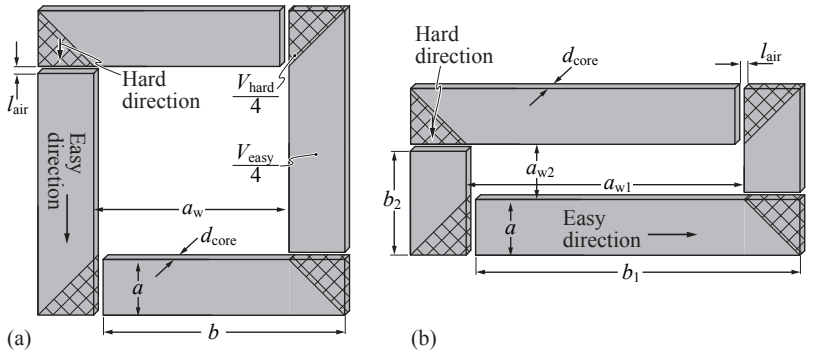


Fig. B.1: Setup of a PCB-integrated core with (a) quadratic outline and (b) rectangular outline.

B.1 Quadratic core shape

According to **Fig. B.1** (a) the overall footprint of the PCB-integrated component is

$$A_{\mathrm{tot}} = (a+b)^2, \tag{B.1}$$

whereas

$$b = a + a_{\mathrm{w}}. \tag{B.2}$$

The perimeter of the winding window,

$$l_{\mathrm{w}} = 4 \cdot a_{\mathrm{w}}, \tag{B.3}$$

has to be large enough to allocate all turns and is therefore constant for a given number of turns. Substitution of (B.2) and (B.3) into (B.1) yields

$$\begin{aligned} A_{\mathrm{tot}} &= a_{\mathrm{w}}^2 + 4\,a_{\mathrm{w}} \cdot a + 4\,a^2 \\ &= \left(\frac{l_{\mathrm{w}}}{4}\right)^2 + a \cdot l_{\mathrm{w}} + 4\,a^2. \end{aligned} \tag{B.4}$$

B.2 Rectangular core shape

A similar analysis can be done for the core setup depicted in **Fig. B.1** (b). The total area is

$$A_{\mathrm{tot}} = (a + b_1) \cdot (a + b_2), \tag{B.5}$$

with the core lengths of

$$b_1 = a_{\mathrm{w1}} + a, \qquad b_2 = a_{\mathrm{w2}} + a. \tag{B.6}$$

The winding window has again to be large enough for the placement of the windings

$$l_{\mathrm{w}} = 2 \cdot (a_{\mathrm{w1}} + a_{\mathrm{w2}}). \tag{B.7}$$

Substitution of (B.6) and (B.7) into (B.5) results in

$$A_{\mathrm{tot}} = a_{\mathrm{w1}} \cdot a_{\mathrm{w2}} + 2\,a \cdot (a_{\mathrm{w1}} + a_{\mathrm{w2}}) + 4\,a^2. \tag{B.8}$$

Introducing the ratio

$$k = \frac{a_{\mathrm{w2}}}{a_{\mathrm{w1}}}, \tag{B.9}$$

which defines the aspect ratio between the length and the width of the core yields

$$\begin{aligned} A_{\mathrm{tot}} = & \quad k \cdot a_{\mathrm{w1}}^2 + 2\,a \cdot a_{\mathrm{w1}} \cdot (1 + k) + 4\,a^2 \\ = & \quad l_{\mathrm{w}}^2 \cdot \frac{k}{4 \cdot (1 + k)^2} + a \cdot l_{\mathrm{w}} + 4\,a^2. \end{aligned} \tag{B.10}$$

B.3 Discussion

A comparison between (B.4) and (B.10) shows that for $k = 1$ the equations are equal and that the total required area can be modelled with

$$A_{\mathrm{tot}} = A_0 + A_1 \cdot \frac{k}{4 \cdot (1 + k)^2}, \tag{B.11}$$

with

$$A_0 = 4\,a^2 + a \cdot l_{\mathrm{w}}, \qquad A_1 = l_{\mathrm{w}}^2. \tag{B.12}$$

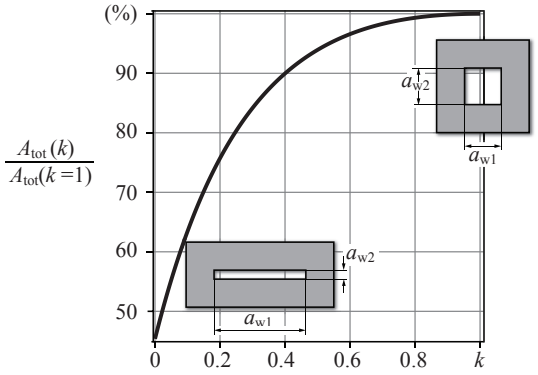


Fig. B.2: Relative required footprint area of PCB-integrated core for different ratios $k = a_{\text{w2}}/a_{\text{w1}}$. Parameters: $a = 15\,\text{mm}$, $l_{\text{w}} = 340\,\text{mm}$.

Fig. B.2 presents the dependency of the total required footprint area on the ratio k. The footprint size is thereby scaled to the required area of the quadratic configuration with the parameters of the implemented prototype in Section 5.3, i.e. $a = 15\,\text{mm}$, $l_{\text{w}} = 340\,\text{mm}$.

As can be seen, the reduction of required area is less that 10 % for $k > 0.4$. For smaller k, the magnetic component is prone to the occurance of winding flux which requires for an appropiate reluctance model, cf. Section 5.2.5, and might degrade the coupling factor for transformer applications. Nevertheless, with an accurate design the required area of a PCB-integrated inductor could be reduced with a rectangluar shaped core configuration.

C

Snubber design for the output diode of the flyback-type PFC rectifier

The flyback-type PFC rectifier presented in Chapter 4 features high currents on the secondary side of the flyback transformer ($I_S = 3.8\,A$). In order to reduce the conduction losses of the output rectifier, an actively switched semiconductor device with a low ON-resistance, e.g. a MOSFET, can be considered instead of a passive diode.

Accordingly, the output rectifier switch S_{out} emulates the diode and before the secondary current i_S reaches 0 A, S_{out} must be turned OFF and i_S commutates to the body diode of the switch. The turn-OFF transition of the body diode, however, causes a voltage spike over S_{out} due to the reverse-recovery charge and the parasitic inductance of the commutation circuit $L_{\sigma S}$. In order to reduce this voltage spike a *RC*-snubber circuit[1] is connected in parallel to S_{out}, as indicated in **Fig. C.1** (a).

Fig. C.1 (b) shows the equivalent circuit on the secondary side with a parasitic inductance $L_{\sigma S}$ which is composed of the leakage inductance of the transformer referred to the secondary side and the parasitic inductance caused by the wiring.

After turn-OFF of the body diode, the equivalent circuit given in **Fig. C.1** (c) can be considered. C_D takes the output capacitance of the switch into account. The design procedure of the *RC*-snubber is detailed in [112].

The transfer function of the voltage applied to S_{out}, $V_{Sout}(s)$, to the

[1] If the converter is operated only in DCM the snubber circuit is not necessary, however, operation close to the boundary of CCM and DCM imposes the voltage spikes caused by the reverse recovery of the diode due to parameter variations. Therefore, the snubber circuit is considered.

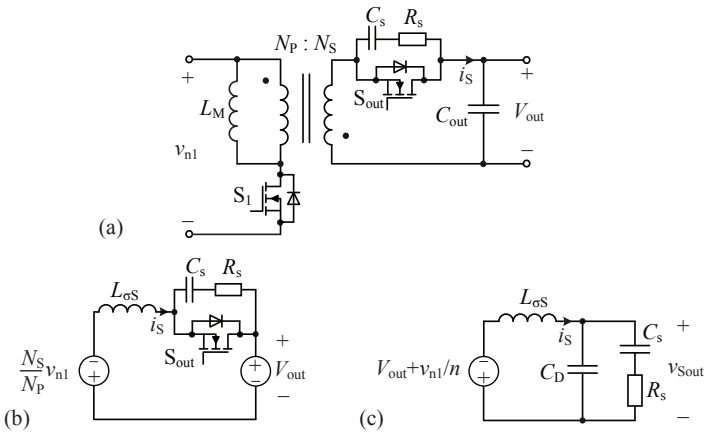


Fig. C.1: (a) Simplified flyback converter with the considered *RC*-snubber in the output. (b) Equivalent circuit on the secondary side when the power switch S_1 is ON. (c) Simplified circuit after turn-OFF of the body diode of S_{out}.

voltage $V_1(s) = V_{out} + v_{n1}/n$, is

$$G(s) = \frac{V_{Sout}(s)}{V_1(s)} = \frac{1 + s\,R_s\,C_s}{1 + s\,R_s\,C_s + s^2\,L_{\sigma S}\,(C_s + C_D) + s^3\,L_{\sigma S}\,C_D\,R_s\,C_s}. \tag{C.1}$$

The denominator polynom of $G(s)$,

$$\begin{aligned} H(j\omega) &= 1 + j\omega R_s\,C_s - \omega^2\,L_{\sigma S}\,(C_s + C_D) - j\omega^3\,L_{\sigma S}\,C_D\,R_s\,C_s = \\ &= 1 + j\omega a - \omega^2 b - j\omega^3 c, \end{aligned} \tag{C.2}$$

can be designed to obtain a Butterworth characteristic of the transfer function [160]. Thus, the coefficients must fulfill

$$\begin{aligned} a^2 &\hat{=} 2 \cdot b, \\ b^2 &\hat{=} 2 \cdot a \cdot c, \end{aligned} \tag{C.3}$$

which results in

$$\begin{aligned} R_s &= \sqrt{\frac{8}{9}} \cdot Z_0 \\ C_s &= 3 \cdot C_D, \end{aligned} \tag{C.4}$$

with

$$Z_0 = \sqrt{\frac{L_{\sigma S}}{C_D}}. \tag{C.5}$$

Assuming a parasitic inductance of $L_{\sigma S} = 900\,\text{nH}$ and considering the energy equivalent output capacitance of S_{out}, $C_D = 730\,\text{pF}$, results in

$$C_s = 2.7\,\text{nF} \quad \text{and} \quad R_s = 33\,\Omega. \tag{C.6}$$

The losses of the snubber circuit can be calculated according to [161]

$$P_{Snub} = f_S \cdot \left(\frac{Q_{oss}}{2} + Q_{rr} \right) \cdot \left(V_{out} + \frac{N_S}{N_P} \cdot v_{n1} \right), \tag{C.7}$$

whereas Q_{oss} and Q_{rr} are the output charge and the reverse recovery charge of the body diode, respectively. The output charge can be obtained from the datasheet but Q_{rr} depends on several parameters and is not specified in datasheets. A reasonable value of the recovery charge is assumed to be $Q_{rr} = 60\,\text{nC}$ [161]. Thus, the snubber losses are estimated to be $P_{Snub} = 650\,\text{mW}$.

Bibliography

[1] "SolarThinFilms Inc." 2012. [Online]. Available: www.solarthinfilms.com.

[2] R. Erickson and A. Rogers, "A microinverter for building-integrated photovoltaics," in *Proc. of the 24th Annual IEEE Applied Power Electronics Conference and Exposition, APEC*, 2009, pp. 911–917.

[3] U.S. Department of Energy, "A plan for the integrated research, development, and market transformation of solar energy technologies," *Solar American Initiative draft plan, SETP-2006-0010*, Feb. 2007.

[4] Fraunhofer institute for solar energy systems, ISE, "Photovoltaics report," Jun. 2012. [Online]. Available: www.ise.fraunhofer.de.

[5] D. Ge and Z. Chen, "On-chip boost DC-DC converter in color OLED driver & controller ICs for mobile application," in *Proc. of the 6th International Conference on ASIC, ASICON*, vol. 1, 2005, pp. 459–463.

[6] J. Jacobs, D. Hente, and E. Waffenschmidt, "Drivers for OLEDs," in *Conference Record of the 42nd IEEE Industry Applications Conference, IAS*, 2007, pp. 1147–1152.

[7] J. Yoo, S. Jung, Y. Kim, S. Byun, J. Kim, N. Choi, S. Yoon, C. Kim, Y. Hwang, and I. Chung, "Highly flexible AM-OLED display with integrated gate driver using amorphous silicon TFT on ultrathin metal foil," *Journal of Display Technology*, vol. 6, no. 11, pp. 565–570, 2010.

[8] D. G. Lamar, J. S. Zuniga, A. R. Alonso, M. R. Gonzalez, and M. M. Alvarez, "A very simple control strategy for power factor correctors driving High-Brightness LEDs," *IEEE Transactions on Power Electronics*, vol. 24, no. 8, pp. 2032–2042, Aug. 2009.

[9] "Osram GmbH," 2012. [Online]. Available: www.osram.com.

[10] G. Sauerlander, D. Hente, H. Radermacher, E. Waffenschmidt, and J. Jacobs, "Driver electronics for LEDs," in *Conference Record of the 41st IEEE Industry Applications Conference, IAS*, vol. 5, 2006, pp. 2621–2626.

[11] "Royal Philips Electronics," 2012. [Online]. Available: www.lighting.philips.com/main/.

[12] "LG Electronics," 2012. [Online]. Available: www.lg.com.

[13] "Smarttable," 2012. [Online]. Available: www.smarttable.org.

[14] E. Waffenschmidt, B. Ackermann, E. Langkabel, M. Wille, H. Marczinske, and S. Schuh, "Integral manufacturing of embedded passives integrated circuits for power electronics," in *Proc. of the 25th International Conference for Power Electronics, Intelligent Motion, and Power Quality, PCIM Europe*, 2004.

[15] E. Waffenschmidt, "Design and application of thin, planar magnetic components for embedded passives integrated circuits," in *Proc. of the 35th IEEE Annual Power Electronics Specialists Conference, PESC*, vol. 6, 2004, pp. 4546–4552.

[16] I. Josifovic, J. Popovic-Gerber, and J. A. Ferreira, "A PCB system integration concept for power electronics," in *Proc. of the 6th International IEEE Power Electronics and Motion Control Conference, IPEMC*, 2009, pp. 756–762.

[17] S. Waffler and J. W. Kolar, "Efficiency optimization of an automotive multi-phase bi-directional DC-DC converter," in *Proc. of the 6th IEEE International Power Electronics and Motion Control Conference IPEMC*, May 2009, pp. 566–572.

[18] M. Hartmann, J. Miniboeck, H. Ertl, and J. W. Kolar, "A Three-Phase delta switch rectifier for use in modern aircraft," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 9, pp. 3635–3647, Sep. 2012.

[19] M. Hartmann and J. W. Kolar, "Analysis of the trade-off between input current quality and efficiency of high switching frequency PWM rectifiers," in *Proc. of the International Power Electronics Conference, IPEC & ECCE Asia*, Jun. 2010, pp. 534–541.

[20] U. Badstuebner, J. Biela, D. Christen, and J. W. Kolar, "Optimization of a 5-kW telecom phase-shift DC-DC converter with magnetically integrated current doubler," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 10, pp. 4736–4745, Oct. 2011.

[21] J. Biela, U. Badstuebner, and J. W. Kolar, "Impact of power density maximization on efficiency of DC-DC converter systems," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 288–300, Jan. 2009.

[22] J. W. Kolar, J. Biela, and J. Miniboeck, "Exploring the pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2% efficiency vs. 7kW/dm^3 power density," in *Proc. of the 6th IEEE International Power Electronics and Motion Control Conference, IPEMC*, 2009, pp. 1–21.

[23] C. Marxgut, J. Biela, and J. W. Kolar, "Design of a multi-cell, DCM PFC rectifier for a 1 mm thick, 200 W off-line power supply – The Power Sheet," in *Proc. of the 6th International Conference on Integrated Power Electronic Systems, CIPS*, Nuremberg, 2010.

[24] F. C. Lee, M. Xu, and S. Wang, "High density approaches of AC to DC converter of distributed power systems (DPS) for telecom and computers," in *Proc. of the 4th Power Conversion Conference, PCC, Nagoya*, 2007, pp. 1236–1243.

[25] K. Raggl, T. Nussbaumer, G. Doerig, J. Biela, and J. W. Kolar, "Comprehensive design and optimization of a high-power-density single-phase boost PFC rectifier," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2574–2587, 2009.

[26] "Lenovo," 2012. [Online]. Available: www.lenovo.com.

[27] "Samsung," 2012. [Online]. Available: www.samsung.com.

[28] "abalight GmbH," 2012. [Online]. Available: abalight.de.

[29] "Derun Lighting," 2012. [Online]. Available: www.derunledlights.com.

[30] *DIN EN 55011; VDE 0875-11: Industrial, scientific and medical equipment - Radio-frequency distrubance characteristics - Limits and methods of measurement (IEC/CISPR 11: 2009)*, DIN Deutsches Institut für Normungen e.V. und VDE Verband der Elektrotechnik, Elektronik, Informationstechnik, e.V. Std., Apr. 2009.

[31] *DIN EN 60950-1; VDE 0805-1: Information technology equipment - Safety - Part 1: General requirements*, DIN Deutsches Institut für Normungen e.V. und VDE Verband der Elektrotechnik, Elektronik, Informationstechnik, e.V. Std., Dec. 2005.

[32] S. Pawel and J. Thalheim, "1700V planar transformers for high power gate drives," in *Proc. of the International Conference for Power Electronics, Intelligent Motion and Power Quality, PCIM Europe*, 2009, pp. 753–758.

[33] ——, "1700V fully coreless gate driver with rugged signal interface and switching-independent power supply," in *Proc. of the 20th International Symposium on Power Semiconductor Devices and IC's, ISPSD*, May 2008, pp. 319–322.

[34] J. Müller and D. Josip, "Integrated capacitors using LTCC," *Proceedings of MicroTech, Manchester, UK*, Jan. 2002.

[35] R. Aparicio and A. Hajimiri, "Capacity limits and matching properties of integrated capacitors," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 3, pp. 384–393, 2002.

[36] R. K. Ulrich and L. W. Schaper, *Integrated passive component technology*, 1st ed. IEEE Press, Wiley-Interscience, 2003.

[37] E. Waffenschmidt and B. Ackermann, "Power converter with printed circuit board integrated passive components," in *Proc. of the 10th European Conference on Power Electronics and Drives, (EPE)*, Toulouse, 2003, p. 119.

[38] E. Waffenschmidt, B. Ackermann, and J. A. Ferreira, "Design method and material technologies for passives in printed circuit board embedded circuits," *IEEE Transactions on Power Electronics*, vol. 20, no. 3, pp. 576–584, 2005.

[39] J. A. Ferreira, E. Waffenschmidt, J. Strydom, and J. D. van Wyk, "Embedded capacitance in the PCB of switchmode converters," in *Proc. of the 33rd IEEE Annual Power Electronics Specialists Conference, PESC*, vol. 1, 2002, pp. 119–123.

[40] Y. Rao and C. P. Wong, "Novel ultra-high dielectric constant polymer based composite for embedded capacitor application," in *Proc. of the 2nd International IEEE Conference on Polymers and*

Adhesives in Microelectronics and Photonics, (POLYTRONIC), 2002, pp. 196–200.

[41] "Murata Manufacturing Co., Ltd," 2012. [Online]. Available: www.murata.com.

[42] "Holystone International," 2012. [Online]. Available: www.holystonecaps.com.

[43] "Epcos AG," 2012. [Online]. Available: www.epcos.com.

[44] "Novacap," 2012. [Online]. Available: www.novacap.com.

[45] "TDK Corporation," 2012. [Online]. Available: www.tdk.com.

[46] "Venkel - Surface Mount Components," 2012. [Online]. Available: www.venkel.com.

[47] "Johanson Companies," 2012. [Online]. Available: www.johanson-caps.com.

[48] "Yageo," 2012. [Online]. Available: www.yageo.com.

[49] S. Dieckerhoff, S. Guttowski, and H. Reichl, "Performance comparison of advanced power electronic packages for automotive applications," in *Proc. of the 1st Automotive Power Electronics Conference and Exhibition, APE*, 2006.

[50] A. Ostmann, D. Manessis, J. Stahr, M. Beesley, M. Cauwe, and J. D. Baets, "Industrial and technical aspects of chip embedding technology," in *Proc. of the 2nd Electronics System-Integration Technology Conference, ESTC*, 2008, pp. 315–320.

[51] Z. Liang, J. D. van Wyk, F. C. Lee, D. Boroyevich, E. P. Scott, Z. Chen, and Y. Pang, "Integrated packaging of a 1 kW switching module using a novel planar integration technology," *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 242–250, 2004.

[52] K. Becker, E. Jung, A. Ostmann, T. Braun, A. Neumann, R. Aschenbrenner, and H. Reichl, "Stackable system-on-packages with integrated components," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 2, pp. 268–277, 2004.

[53] S. Dieckerhoff, T. Kirfe, T. Wernicke, C. Kallmayer, A. Ostmann, E. Jung, B. Wunderle, and H. Reichl, "Electric characteristics of planar interconnect technologies for power MOSFETs," in *Proc. of the 38th IEEE Annual Power Electronics Specialists Conference, PESC*, 2007, pp. 1036–1042.

[54] Z. Liang, J. D. van Wyk, F. C. Lee, D. Boroyevich, E. Scott, Z. Chen, and Y. Pang, "Integrated packaging of a 1 kW switching module using planar interconnect on embedded power chips technology," in *Proc. of the 18th IEEE Annual Applied Power Electronics Conference and Exposition, APEC*, vol. 1, 2003, pp. 42–47.

[55] J. Bai, G. Lu, and X. Liu, "Flip-chip on flex integrated power electronics modules for high-density power integration," *IEEE Transactions on Advanced Packaging*, vol. 26, no. 1, pp. 54–59, 2003.

[56] "Infineon Technologies," 2012. [Online]. Available: www.infineon.com.

[57] T. Wernicke, S. Dieckerhoff, T. Kirfe, G. Feix, S. Guttowski, and H. Reichl, "Experimental characterization methods for power MOSFET assemblies," in *Proc. of the 12th European Conference on Power Electronics and Applications, EPE*, 2007, pp. 1–9.

[58] "IR International Rectifier," 2012. [Online]. Available: www.irf.com.

[59] "STMicroelectronics," 2012. [Online]. Available: www.st.com.

[60] "Vishay," 2012. [Online]. Available: www.vishay.com.

[61] M. Ludwig, M. Duffy, T. O'Donnell, P. McCloskey, and S. C. O'Mathuna, "Design study for ultraflat PCB-integrated inductors for low-power conversion applications," *IEEE Transactions on Magnetics*, vol. 39, no. 5, pp. 3193–3195, 2003.

[62] S. C. O'Mathuna, N. Wang, S. Kulkarni, and S. Roy, "Review of integrated magnetics for power supply on chip (PwrSoC)," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4799–4816, Nov. 2012.

[63] J. W. Kolar, U. Drofenik, J. Biela, M. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM converter power density barriers," in *Proc. of the 4th Power Conversion Conference, PCC, Nagoya*, Apr. 2007, pp. 9–29.

[64] S. D. Round, P. Karutz, M. L. Heldwein, and J. W. Kolar, "Towards a 30 kW/liter, three-phase unity power factor rectifier," in *Proc. of the 4th Power Conversion Conference, PCC, Nagoya*, Apr. 2007, pp. 1251–1259.

[65] U. Drofenik and J. W. Kolar, "Thermal power density barriers of converter systems," in *Proc. of the 5th International Conference on Integrated Power Systems, CIPS*, Mar. 2008.

[66] O. Garcia, P. Zumel, A. de Castro, and A. Cobos, "Automotive DC-DC bidirectional converter made with many interleaved buck stages," *IEEE Transactions on Power Electronics*, vol. 21, no. 3, pp. 578–586, May 2006.

[67] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved triangular current mode (TCM) resonant transition, single-phase PFC rectifier with high efficiency and high power density," in *Proc. of the International Power Electronics Conference, IPEC & ECCE Asia*, 2010, pp. 1725–1732.

[68] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muehlethaler, T. Nussbaumer, and J. Miniboeck, "Extreme efficiency power electronics," in *Proc. of the 7th International Conference on Integrated Power Electronic Systems, CIPS*, Nuremberg, 2012.

[69] M. M. Jovanovic and D. E. Crow, "Merits and limitations of full-bridge rectifier with LC filter in meeting IEC 1000-3-2 harmonic-limit specifications," *IEEE Transactions on Industry Applications*, vol. 33, no. 2, pp. 551–557, Apr. 1997.

[70] *DIN EN 61000-3-2; VDE 0838-2: Elektromagnetische Verträglichkeit (EMV) - Teil 3-2: Grenzwerte für Oberschwingungen (Geräte-Eingangsstrom kleiner gleich 16 A je Leiter)*, DIN Deutsches Institut für Normungen e.V. und VDE Verband der Elektrotechnik, Elektronik, Informationstechnik, e.V. Std., Jun. 2011.

[71] A. Fernandez, J. Sebastian, M. M. Hernando, P. Villegas, and J. Garcia, "Helpful hints to select a power-factor-correction solution for low- and medium-power single-phase power supplies," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 46–55, 2005.

[72] U. Badstübner, "Ultra-High Performance Telecom DC-DC Converter," *PhD thesis no. 20354, ETH Zurich*, 2012.

[73] M. Daniele, P. Jain, and G. Joos, "A single stage single switch power factor corrected AC/DC converter," in *Proc. of the 27th IEEE Power Electronics Specialists Conference, PESC*, vol. 1, Jun. 1996, pp. 216–222.

[74] F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "Evaluation and efficiency comparison of front end AC-DC plug-in hybrid charger topologies," *IEEE Transactions on Smart Grid*, vol. 3, no. 1, pp. 413–421, Mar. 2012.

[75] B. Lu, R. Brown, and M. Soldano, "Bridgeless PFC implementation using one cycle control technique," in *Proc. of the 20th IEEE Annual Applied Power Electronics Conference and Exposition, APEC*, vol. 2, 2005, pp. 812–817.

[76] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1381–1390, 2008.

[77] P. Kong, S. Wang, and F. C. Lee, "Common mode EMI noise suppression for bridgeless PFC converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 291–297, 2008.

[78] H. Ye, Z. Yang, J. Dai, C. Yan, X. Xin, and J. Ying, "Common mode noise modeling and analysis of dual boost PFC circuit," in *Proc. of the 26th Annual International Telecommunications Energy Conference, INTELEC*, 2004, pp. 575–582.

[79] L. Huber, B. T. Irving, and M. M. Jovanovic, "Effect of valley switching and switching-frequency limitation on line-current distortions of DCM/CCM boundary boost PFC converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 2, pp. 339–347, 2009.

[80] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM," *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 427–435, Feb. 2011.

[81] E. Firmansyah, S. Tomioka, S. Abe, M. Shoyama, and T. Ninomiya, "A critical-conduction-mode bridgeless interleaved boost power factor correction," in *Proc. of the 31st International Telecommunications Energy Conference, INTELEC*, Oct. 2009, pp. 1–5.

[82] F. Krismer, "Modeling and optimization of bidirectional dual active bridge dc–dc converter topologies," *PhD thesis no. 19177, ETH Zurich*, 2010.

[83] J. Mühlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Core losses under the DC bias condition based on Steinmetz parameters," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 953–963, Feb. 2012.

[84] M. Heldwein, "EMC filtering of three-phase PWM converters," *PhD thesis no. 17554, ETH Zurich*, 2007.

[85] K. Raggl, T. Nussbaumer, and J. Kolar, "Guideline for a simplified differential-mode EMI filter design," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 3, pp. 1031–1040, Mar. 2010.

[86] J. Biela, D. Hassler, J. Miniboeck, and J. W. Kolar, "Optimal design of a 5kW/dm3 / 98.3% efficient TCM resonant transition single-phase PFC rectifier," in *Proc. of the International Power Electronics Conference, IPEC & ECCE Asia*, 2010, pp. 1709–1716.

[87] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Springer, Jan. 2001.

[88] "Texas Instruments," 2012. [Online]. Available: www.ti.com.

[89] "Lattice Semiconductor," 2012. [Online]. Available: www.latticesemi.com.

[90] Y. Jang and M. M. Jovanovic, "Light-load efficiency optimization method," *IEEE Transactions on Power Electronics*, vol. 25, no. 1, pp. 67–74, Jan. 2010.

[91] C. Wang, M. Xu, F. C. Lee, and Z. Luo, "Light load efficiency improvement for multi-channel PFC," in *Proc. of the 39th IEEE Annual Power Electronics Specialists Conference, PESC*, 2008, pp. 4080–4085.

[92] L. Huber, J. Zhang, M. Jovanovic, and F. Lee, "Generalized topologies of single-stage input-current-shaping circuits," *IEEE Transactions on Power Electronics*, vol. 16, no. 4, pp. 508 –513, Jul. 2001.

[93] H.-F. Liu and L.-K. Chang, "Flexible and low cost design for a flyback AC/DC converter with harmonic current correction," *IEEE Transactions on Power Electronics*, vol. 20, no. 1, pp. 17–24, Jan. 2005.

[94] R. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," in *IEEE Transactions on Industrial Applications*, vol. 27, no. 1, 1991, pp. 63–73.

[95] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Switching control strategy to minimize dual active bridge converter losses," in *IEEE Transactions on Power Electronics*, vol. 24, no. 7, 2009, pp. 1826–1838.

[96] F. Krismer, J. Biela, and W. Kolar, J. "A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range," in *Conf. Rec. of the 40th IEEE Industry Application Society Conference, IAS*, 2005, pp. 599–606.

[97] F. Krismer, S. Round, and J. W. Kolar, "Performance optimization of a high current dual active bridge with a wide operating voltage range," in *Proc. of the 37th IEEE Power Electronics Specialists Conference, PESC*, 2006, pp. 909–915.

[98] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge dc-to-dc converter," *IEEE Transactions on Industrial Applications*, vol. 28, no. 6, 1992.

[99] N. Schibli, "Symmetrical multilevel converters with two quadrant DC-DC feeding," *PhD thesis no. 2220, EPFL Lausanne*, 2000.

[100] M. T. Zhang, M. M. Jovanovic, and F. C. Lee, "Design considerations and performance evaluations of synchronous rectification in flyback converters," *IEEE Transactions on Power Electronics*, vol. 13, no. 3, pp. 538–546, 1998.

[101] B. T. Bucheru and I. D. Jitaru, "High efficiency adapter using dual switch PFC flyback single stage," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion and Power Quality, PCIM Europe*, May 2008, pp. 703–708.

[102] B. T. Bucheru, M. A. Davila, and I. D. Jitaru, "ZVS and ZCS high efficiency low profile adapter," in *Proc. of the 6th International Conference for Power Electronics, Intelligent Motion and Power Quality, PCIM China*, Mar. 2007, pp. 30–35.

[103] C. Marxgut, J. Mühlethaler, F. Krismer, and J. W. Kolar, "Multi-objective optimization of ultra-flat magnetic components with a PCB-integrated core," in *Proc. of the 8th IEEE International Conference on Power Electronics, ICPE & ECCE Asia*, Jun. 2011, pp. 460–467.

[104] J. W. Kolar, *Skriptum zur Vorlesung Leistungselektronik.* Swiss Federal Institute of Technology Zurich (ETH Zürich), Herbstsemester 2010.

[105] L. Huber and M. M. Jovanovic, "Evaluation of flyback topologies for notebook AC/DC adapter/charger applications," in *Proc. of the High Freq. Power Conversion Conference, HFPC*, 1995, pp. 284–294.

[106] G. Spiazzi, L. Rossetto, and P. Mattavelli, "Design optimization of soft-switched insulated DC/DC converters with active voltage clamp," in *Conference Record of the 31st IEEE Industry Applications Conference, IAS*, vol. 2, 1996, pp. 1169–1176.

[107] R. Watson, G. C. Hua, and F. C. Lee, "Characterization of an active clamp flyback topology for power factor correction applications," *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 191–198, 1996.

[108] R. Watson, F. C. Lee, and G. C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters,"

IEEE Transactions on Power Electronics, vol. 11, no. 1, pp. 162–169, 1996.

[109] C. P. Henze, H. C. Martin, and D. W. Parsley, "Zero-voltage switching in high frequency power converters using pulse width modulation," in *Proc. of 3rd IEEE Applied Power Electronics Conference and Exposition, APEC*, Feb. 1988, pp. 33–40.

[110] M. Zhang, M. Jovanovic, and F. Lee, "Design considerations and performance evaluations of synchronous rectification in flyback converters," in *Proc. of the 12th IEEE Applied Power Electronics Conference and Exposition, APEC*, vol. 2, 1997, pp. 623–630.

[111] M. Hartmann, "Ultra-compact and ultra-efficient three-phase PWM rectifier systems for more electric aircraft," *PhD thesis no. 19755, ETH Zurich*, 2011.

[112] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed. Wiley, Oct. 2002.

[113] O. Föllinger, *Regelungstechnik*, 10th ed. Hüthig, 2008.

[114] J. Alonso, M. Dalla Costa, and C. Ordiz, "Integrated buck-flyback converter as a high-power-factor off-line power supply," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1090–1100, 2008.

[115] B. Lin, H. Chiang, K. Chen, and D. Wang, "Analysis, design and implementation of an active clamp flyback converter," in *Proc. of IEEE International Conference on Power Electronics and Drive Systems, PEDS*, vol. 1, 2005, pp. 424–429.

[116] J. Baek, J. Kim, and B. Cho, "Low-profile AC/DC converter for laptop adaptor," in *Proc. of the 26th IEEE Applied Power Electronics Conference and Exposition, APEC*, Mar. 2011, pp. 60–64.

[117] G. Spiazzi, S. Buso, and D. Tagliavia, "A low-loss high-power-factor flyback rectifier suitable for smart power integration," in *Proc. of the 31st IEEE Annual Power Electronics Specialists Conference, PESC*, vol. 2, 2000, pp. 805–810.

[118] C. Wang, C. Lin, and T. Yang, "High-power-factor soft-switched DC power supply system," *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 647–654, Feb. 2011.

[119] Z. Ouyang, Z. Zhang, O. C. Thomsen, and M. A. E. Andersen, "Planar-integrated magnetics (PIM) module in hybrid bidirectional DC-DC converter for fuel cell application," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3254–3264, Nov. 2011.

[120] E. Waffenschmidt, "Performance limits of ultra-thin printed circuit board inductors," in *Proc. of the 37th IEEE Power Electronics Specialists Conference, PESC*, 2006, pp. 1–7.

[121] M. Ludwig, M. Duffy, T. O'Donnell, P. McCloskey, and S. C. O'Mathuna, "PCB integrated inductors for low power DC/DC converter," *IEEE Transactions on Power Electronics*, vol. 18, no. 4, pp. 937–945, 2003.

[122] Q. Chen, Z. Gong, X. Yang, Z. Wang, and L. Zhang, "Design considerations for passive substrate with ferrite materials embedded in printed circuit board (PCB)," in *Proc. of the 38th IEEE Annual Power Electronics Specialists Conference, PESC*, 2007, pp. 1043–1047.

[123] "Ferroxcube," 2012. [Online]. Available: www.ferroxcube.eu.

[124] Y. Zhang and S. Sanders, "In-board magnetics processes," in *Proc. of the 30th Annual IEEE Power Electronics Specialists Conference, PESC*, vol. 1, 1999, pp. 561–567.

[125] "Schweizer Electronic AG ," 2012. [Online]. Available: www.schweizer.ag.

[126] "Vacuumschmelze AG, VAC," 2012. [Online]. Available: www.vacuumschmelze.de.

[127] "Metglas," 2012. [Online]. Available: www.metglas.com.

[128] "Toshiba," 2012. [Online]. Available: www.toshiba.com.

[129] "Hitachi Metals," 2012. [Online]. Available: www.hitachi-metals.co.jp.

[130] C. R. Sullivan and S. R. Sanders, "Design of microfabricated transformers and inductors for high-frequency power conversion," *IEEE Transactions on Power Electronics*, vol. 11, no. 2, pp. 228–238, 1996.

[131] J. Mühlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Improved core-loss calculation for magnetic components employed in power electronic systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 964–973, Feb. 2012.

[132] L. Coppola, D. Cottet, and F. Wildner, "Investigation on current density limits in power printed circuit boards," in *Proc. of the 23rd IEEE Annual Applied Power Electronics Conference and Exposition, APEC*, 2008, pp. 205–210.

[133] J. Mühlethaler, J. W. Kolar, and A. Ecklebe, "A novel approach for 3D air gap reluctance calculations," in *Proc. of the IEEE 8th International Conference on Power Electronics, ICPE & ECCE Asia*, 2011.

[134] R. Prieto, J. A. Cobos, O. Garcia, P. Alou, and J. Uceda, "Study of 3-D magnetic components by means of "double 2-D" methodology," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 1, pp. 183–192, Feb. 2003.

[135] E. C. Snelling, *Soft Ferrites - Properties and Applications*, 2nd ed. PSMA Reprint, 2005.

[136] J. Qiu and C. Sullivan, "Inductor design for VHF tapped-inductor DC-DC power converters," in *Proc. of the 26th Annual IEEE Applied Power Electronics Conference and Exposition, APEC*, 2011, pp. 142–149.

[137] I. Lope, C. Carretero, J. Acero, J. Burido, and R. Alonso, "Practical issues when calculating ac losses for magnetic devices in PCB implementations," in *Proc. of the 27th Annual IEEE Applied Power Electronics Conference and Exposition, APEC*, 2012, pp. 1017–1022.

[138] "Ansys, Inc," 2012. [Online]. Available: www.ansys.com.

[139] C. R. Paul, *Introduction to Electromagnetic Compatibilty*, 2nd ed. John Wiley, Jan. 2006.

[140] T. Nussbaumer, M. Heldwein, and J. Kolar, "Differential mode input filter design for a three-phase buck-type PWM rectifier based on modeling of the EMC test receiver," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1649–1661, Oct. 2006.

[141] L. Xing and J. Sun, "Optimal damping of multistage EMI filters," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1220–1227, Mar. 2012.

[142] T. Nussbaumer, K. Raggl, and J. W. Kolar, "Design guidelines for interleaved single-phase boost PFC circuits," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2559–2573, 2009.

[143] J. Muehlethaler, H. Uemura, and J. W. Kolar, "Optimal design of EMI filters for single-phase boost PFC circuits," in *Proc. of the 38th IEEE Conference of Industrial Electronics, IECON*, 2012.

[144] V. Vlatkovic, D. Borojevic, and F. Lee, "Input filter design for power factor correction circuits," *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 199 –205, Jan. 1996.

[145] J. Mühlethaler, M. Schweizer, R. Blattmann, J. W. Kolar, and A. Ecklebe, "Optimal design of LCL harmonic filters for three-phase PFC rectifiers," in *Proc. of the 37th Annual Conference on the IEEE Industrial Electronics Society, IECON*, Nov. 2011, pp. 1503–1510.

[146] F. Giezendanner, J. Biela, J. W. Kolar, and S. Zudrell-Koch, "EMI noise prediction for electronic ballasts," *IEEE Transactions on Power Electronics*, vol. 25, no. 8, pp. 2133 –2141, Aug. 2010.

[147] P. Kong, Y. Jiang, and F. C. Lee, "Common mode EMI noise characteristics of low-power AC-DC converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 731–738, Feb. 2012.

[148] P. Meng, J. Zhang, H. Chen, Z. Qian, and Y. Shen, "Characterizing noise source and coupling path in flyback converter for common-mode noise prediction," in *Proc. of the 26th Annual IEEE Applied Power Electronics Conference and Exposition, APEC*, Mar. 2011, pp. 1704 –1709.

[149] "Gecko Research," 2012. [Online]. Available: www.gecko-research.com.

[150] Y. Jang and R. W. Erickson, "Physical origins of input filter oscillations in current programmed converters," *IEEE Transactions on Power Electronics*, vol. 7, no. 4, pp. 725–733, Oct. 1992.

[151] R. Erickson, "Optimal single resistors damping of input filters," in *Proc. of the 14th Annual IEEE Applied Power Electronics Conference and Exposition, APEC*, vol. 2, Mar. 1999, pp. 1073–1079.

[152] *Fixed capacitors for use in electronic equipment - Part 14: Sectional specification - Fixed capacitors for electromagnetic interference suppression and connection to the supply mains. DIN EN 60384-14*, DIN Deutsches Institut für Normung e. V., DIN German Institute for Standardization Std., 2010.

[153] "Magnetics," 2012. [Online]. Available: www.mag-inc.com.

[154] "Micrometals, Inc." 2012. [Online]. Available: www.micrometals.com.

[155] "Agilent Technologies," 2012. [Online]. Available: www.agilent.com.

[156] M. L. Heldwein and J. W. Kolar, "Design of minimum volume EMC input filters for an ultra compact three-phase PWM rectifier," in *Proc. of the 9th Brazilian Power Electronics Conference, COBEP*, Sep. 2007.

[157] "Omicron Electronics GmbH," 2012. [Online]. Available: www.omicron-lab.com.

[158] D. C. Hamill, "Lumped equivalent circuits of magnetic components: The gyrator-capacitor approach," *IEEE Transactions on Power Electronics*, vol. 8, no. 2, pp. 97–103, Apr. 1993.

[159] M. K. Kazimierczuk, *High-Frequency Magnetic Components*, 1st ed. Wiley, 2009.

[160] O. Tietze and C. Schenk, *Halbleiter-Schaltungstechnik*, 13rd ed. Springer Berlin Heidelberg, 2009.

[161] C. Mösslacher and L. Görgens, "Improving efficiency of synchronous rectification by analysis of the MOSFET power loss mechanism," in *Proc. of the International Conference for Power*

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