Eidgenössische Technische Hochschule Zürich
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Indirect Matrix Converter

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Schedule

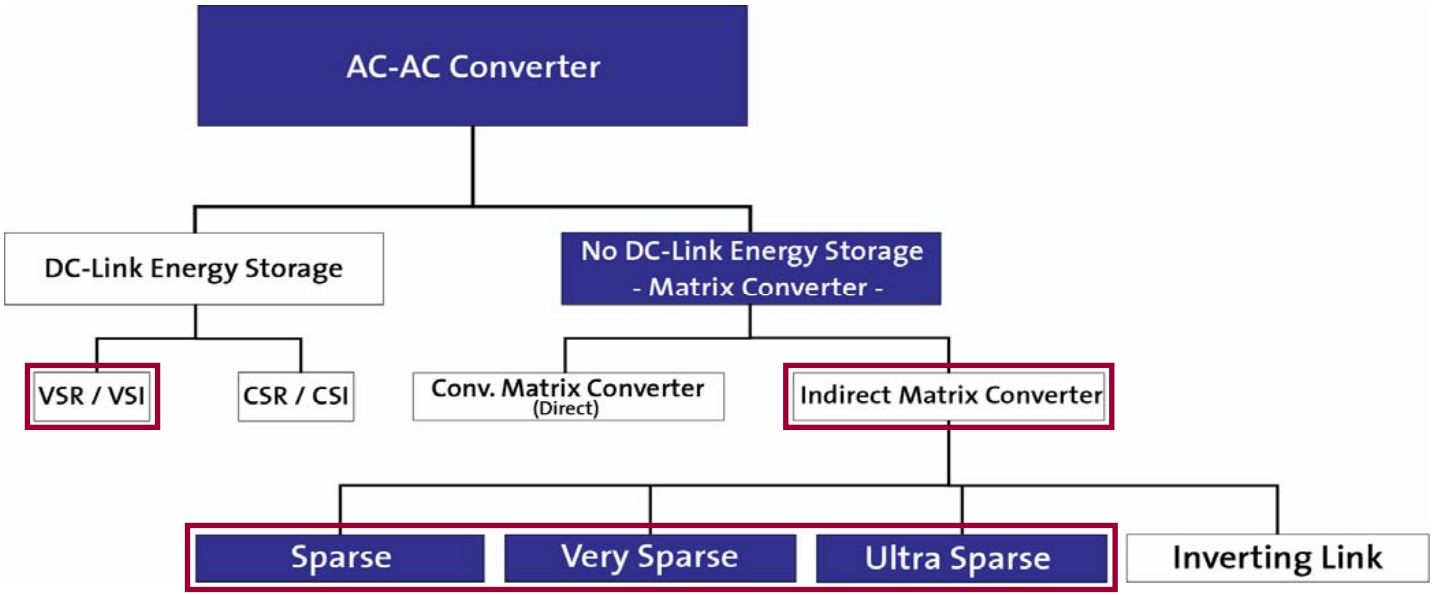
- Indirect Matrix Converter (IMC)
  Johann W. Kolar, Thomas Friedli
  - Basics
  - Comparison with Conventional (Direct) MC
  - IMC Modulation Schemes
  - Dimensioning
  - EMI Filter Design
  - Hardware Implementation
  - Experimental Results

Coffee Break

- Indirect Matrix Converter vs. Back-To-Back Converter
  Johann W. Kolar, Thomas Friedli

- Future Research and Development, Discussion
  Johann W. Kolar, Patrick Wheeler

Classification of AC-AC Converter Topologies



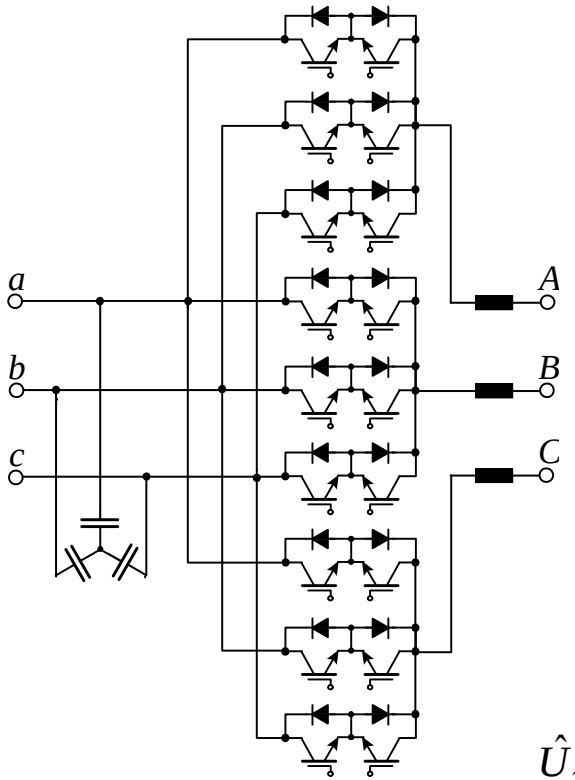
MC Features:

- Sinusoidal input and output currents
- Unity power factor at the input
- No energy storage elements: size and weight reduction

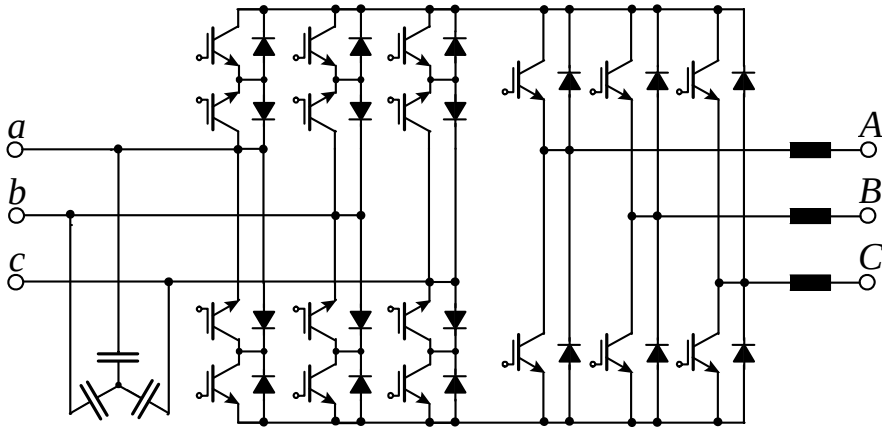
Indirect Matrix Converter (IMC)

Basic Matrix Converter Topologies

Conventional Matrix Converter



Indirect Matrix Converter



$$\hat{U}_{2,\max} = \frac{\sqrt{3}}{2} \cdot \hat{U}_1 = 0.866 \cdot \hat{U}_1$$

Conventional Matrix Converter (CMC)

Mathematical Description of the Basic Operating Behavior

Voltage Conversion

$$\begin{pmatrix} u_A \\ u_B \\ u_C \end{pmatrix} = \begin{pmatrix} sAa & sAb & sAc \\ sBa & sBb & sBc \\ sCa & sCb & sCc \end{pmatrix} \cdot \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix}$$

$$\underline{u}_{ABC} = \underline{S} \cdot \underline{u}_{abc}$$

u_a, u_b, u_c : Input voltages

u_A, u_B, u_C : Output voltages

Current Conversion

$$\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \begin{pmatrix} sAa & sBa & sCa \\ sAb & sBb & sCb \\ sAc & sBc & sCc \end{pmatrix} \cdot \begin{pmatrix} i_A \\ i_B \\ i_C \end{pmatrix}$$

$$\underline{i}_{abc} = \underline{S}^T \cdot \underline{\mathrm{i}}_{\mathrm{ABC}}$$

i_a, i_b, i_c : Input currents

i_A, i_B, i_C : Output currents

Conventional → Indirect Matrix Converter (IMC)

Voltage Conversion Split into Rectifier and Inverter Stage

$$\begin{pmatrix} u_A \\ u_B \\ u_C \end{pmatrix} = \begin{pmatrix} spA & snA \\ spB & snB \\ spC & snC \end{pmatrix} \cdot \begin{pmatrix} sap & sbp & scp \\ san & sbn & scn \end{pmatrix} \cdot \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix}$$

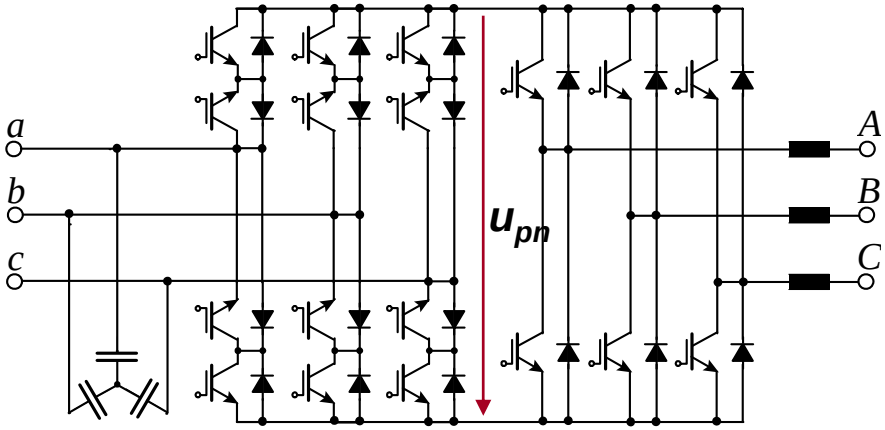
$$\underline{u}_{ABC} = \underline{S}_{\text{Inv}} \cdot \underline{S}_{\text{Rect}} \cdot \underline{u}_{abc}$$

$$\underline{u}_{DC} = \begin{pmatrix} u_p \\ u_n \end{pmatrix} = \underline{S}_{\text{Rect}} \cdot \underline{u}_{abc}$$

- Introduction of a fictitious rectifier and inverter stage
- Fictitious DC link voltage and DC link current
- Modulation as for DC link converters

Indirect Matrix Converter can be considered as a physical implementation of a mathematical concept

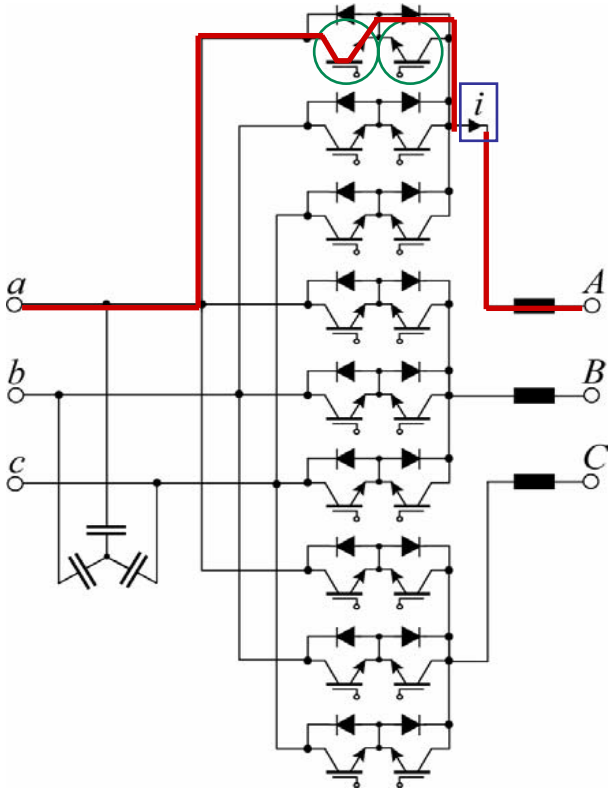
Functional Equivalence of the IMC and the CMC



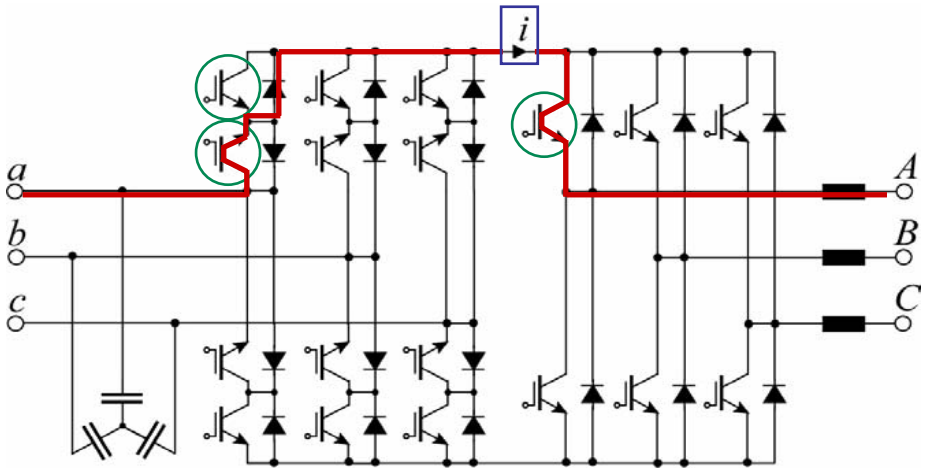
- Operation of the IMC is restricted to $u_{pn} > 0$
- Remaining switching states identical to those of CMC

No.	A	B	C	s_{Aa}	s_{Ab}	s_{Ac}	s_{Ba}	s_{Bb}	s_{Bc}	s_{Ca}	s_{Cb}	s_{Cc}	u_{AB}	u_{BC}	u_{CA}	i_a	i_b	i_c
1	a	a	a	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0
2	b	b	b	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0
3	c	c	c	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0
4	a	c	c	1	0	0	0	0	1	0	0	1	$-u_{ca}$	0	u_{ca}	i_A	0	$-i_A$
5	b	c	c	0	1	0	0	0	1	0	0	1	u_{bc}	0	$-u_{bc}$	0	i_A	$-i_A$
6	b	a	a	0	1	0	1	0	0	1	0	0	$-u_{ab}$	0	u_{ab}	$-i_A$	i_A	0
7	c	a	a	0	0	1	1	0	0	1	0	0	u_{ca}	0	$-u_{ca}$	$-i_A$	0	i_A
8	c	b	b	0	0	1	0	1	0	0	1	0	$-u_{bc}$	0	u_{bc}	0	$-i_A$	i_A
9	a	b	b	1	0	0	0	1	0	0	1	0	u_{ab}	0	$-u_{ab}$	i_A	$-i_A$	0
10	c	a	c	0	0	1	1	0	0	0	0	1	u_{ca}	$-u_{ca}$	0	i_B	0	$-i_B$
11	c	b	c	0	0	1	0	1	0	0	0	1	$-u_{bc}$	u_{bc}	0	0	i_B	$-i_B$
12	a	b	a	1	0	0	0	1	0	1	0	0	u_{ab}	$-u_{ab}$	0	$-i_B$	i_B	0
13	a	c	a	1	0	0	0	0	1	1	0	0	$-u_{ca}$	u_{ca}	0	$-i_B$	0	i_B
14	b	c	b	0	1	0	0	0	1	0	1	0	u_{bc}	$-u_{bc}$	0	0	$-i_B$	i_B
15	b	a	b	0	1	0	1	0	0	0	1	0	$-u_{ab}$	u_{ab}	0	i_B	$-i_B$	0
16	c	c	a	0	0	1	0	0	1	1	0	0	0	u_{ca}	$-u_{ca}$	i_C	0	$-i_C$
17	c	c	b	0	0	1	0	0	1	0	1	0	0	$-u_{bc}$	u_{bc}	0	i_C	$-i_C$
18	a	a	b	1	0	0	1	0	0	0	1	0	0	u_{ab}	$-u_{ab}$	$-i_C$	i_C	0
19	a	a	c	1	0	0	1	0	0	0	0	1	0	$-u_{ca}$	u_{ca}	$-i_C$	0	i_C
20	b	b	c	0	1	0	0	1	0	0	0	1	0	u_{bc}	$-u_{bc}$	0	$-i_C$	i_C
21	b	b	a	0	1	0	0	1	0	1	0	0	0	$-u_{ab}$	u_{ab}	i_C	$-i_C$	0
22	a	b	c	1	0	0	0	1	0	0	0	1	u_{ab}	u_{bc}	u_{ca}	i_A	i_B	i_C
23	a	c	b	1	0	0	0	0	1	0	1	0	$-u_{ca}$	$-u_{bc}$	$-u_{ab}$	i_A	i_C	i_B
24	b	a	c	0	1	0	1	0	0	0	0	1	$-u_{ab}$	$-u_{ca}$	$-u_{bc}$	i_B	i_A	i_C
25	b	c	a	0	1	0	0	0	1	1	0	0	u_{bc}	u_{ca}	u_{ab}	i_C	i_A	i_B
26	c	a	b	0	0	1	1	0	0	0	1	0	u_{ca}	u_{ab}	u_{bc}	i_B	i_C	i_A
27	c	b	a	0	0	1	0	0	1	1	0	0	$-u_{bc}$	$-u_{ab}$	$-u_{ca}$	i_C	i_B	i_A
⋮																		
70	b	b	c	0	1	0	0	0	1	1	1	0	0	u_{bc}	$-u_{bc}$	u_{bc}	0	$-i_C$	i_C
71	b	b	a	1	0	0	0	1	0	0	0	1	0	$-u_{ab}$	u_{ab}	u_{ab}	i_C	$-i_C$	0
72	b	b	a	0	1	0	1	0	0	1	1	0	0	$-u_{ab}$	u_{ab}	$-u_{ab}$	i_C	$-i_C$	0

Multi-Step Commutation for CMC / IMC



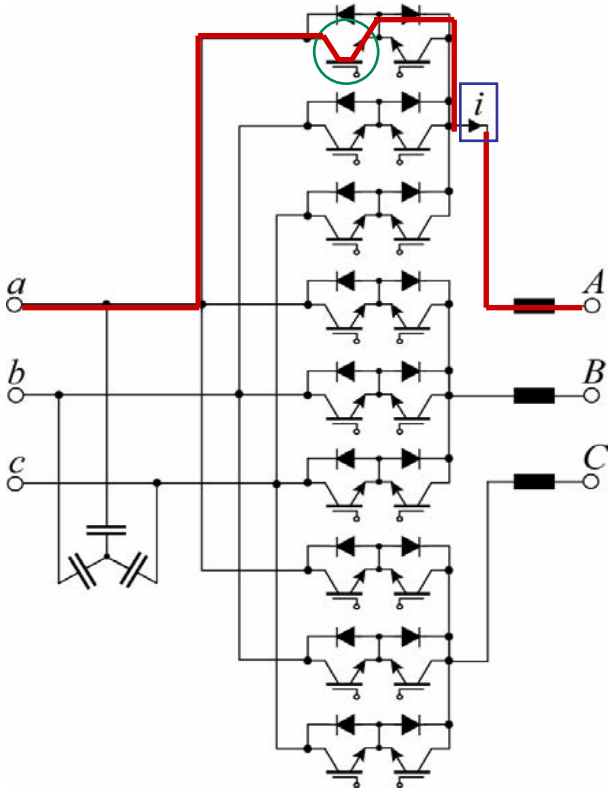
Example: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$



Constraints:

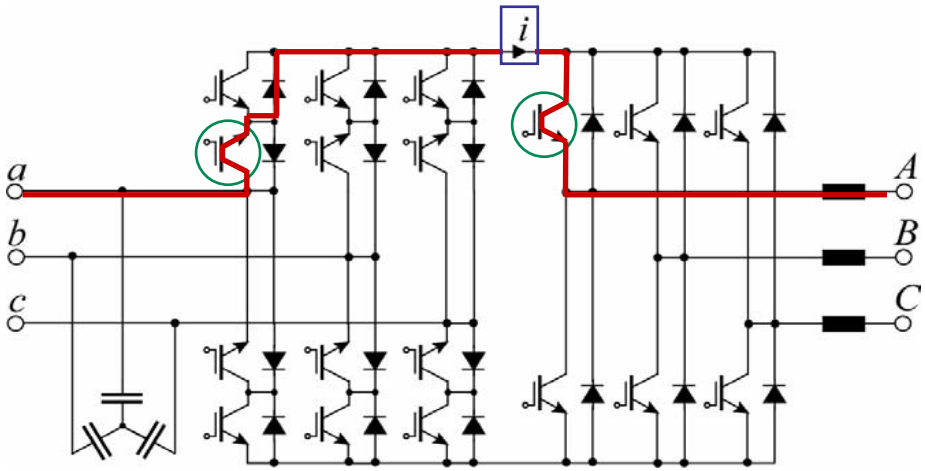
- No mains phases short-circuited
- No interruption of *i*

Multi-Step Commutation for CMC / IMC



Example: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

1st step: off



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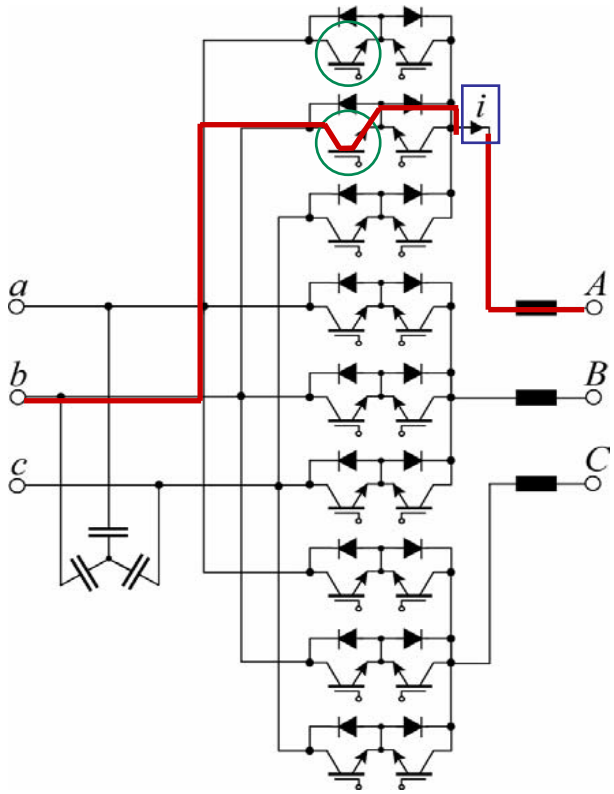
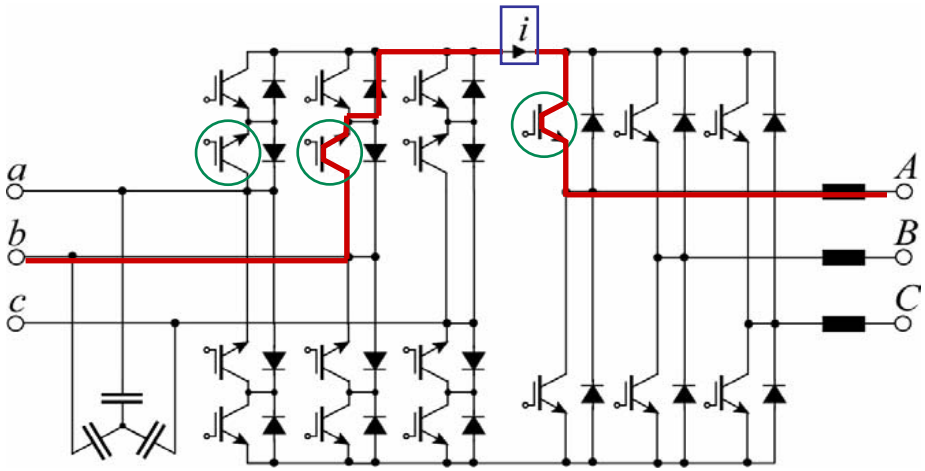
Multi-Step Commutation for CMC / IMC



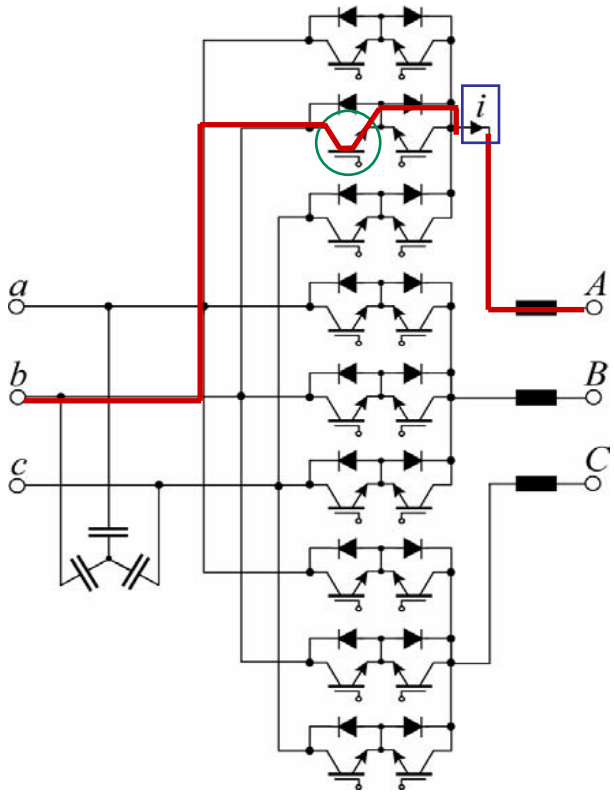
1st step: off
2nd step: on



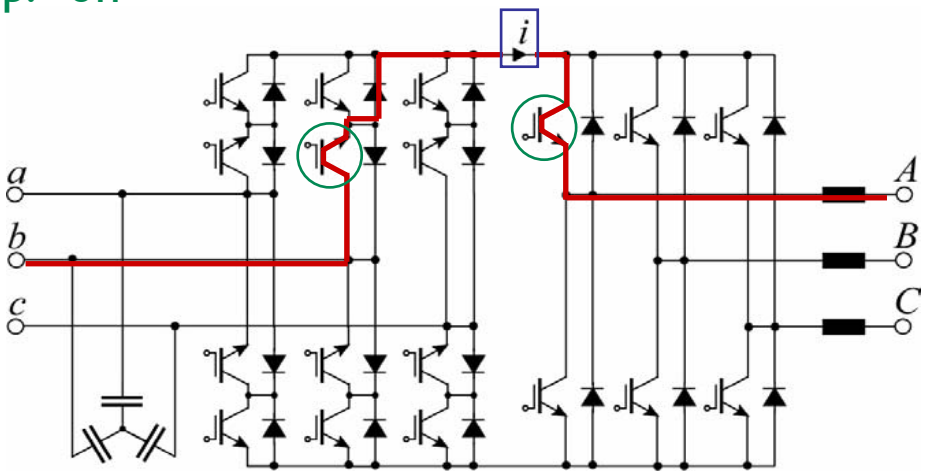
Example: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

Constraints:
- No mains phases short-circuited
- No interruption of *i*

Multi-Step Commutation for CMC / IMC



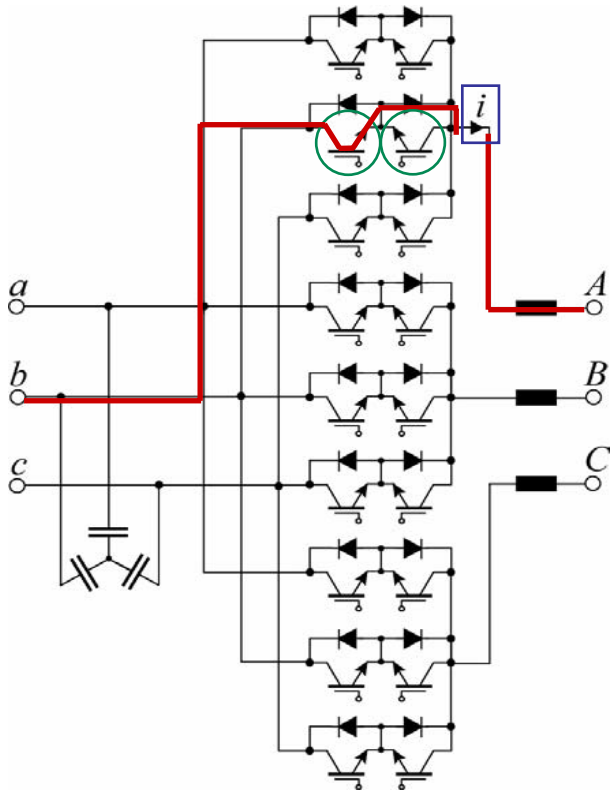
1st step: off
2nd step: on
3rd step: off



Example: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

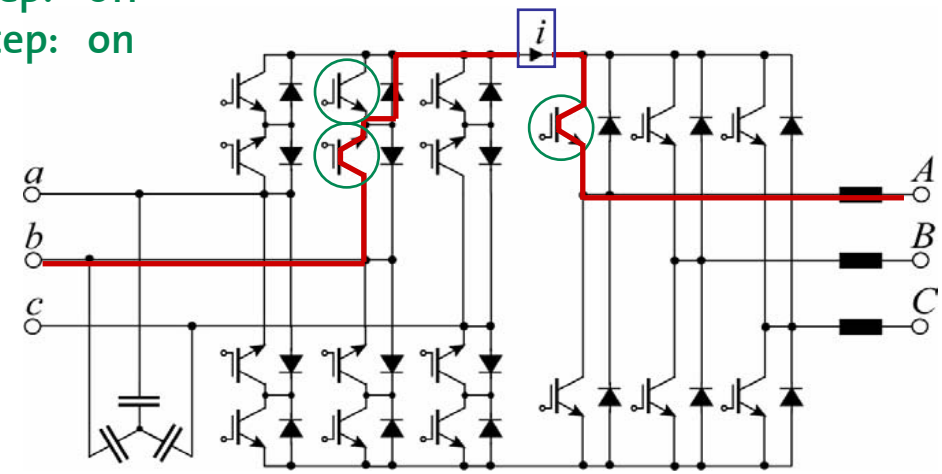
Constraints:
- No mains phases short-circuited
- No interruption of *i*

Multi-Step Commutation for CMC / IMC



1st step: off
2nd step: on
3rd step: off
4th step: on

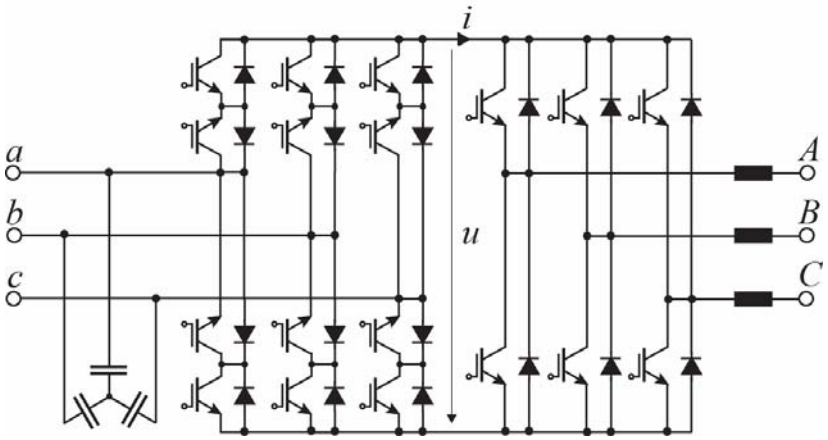
Sequence depends on current sign!

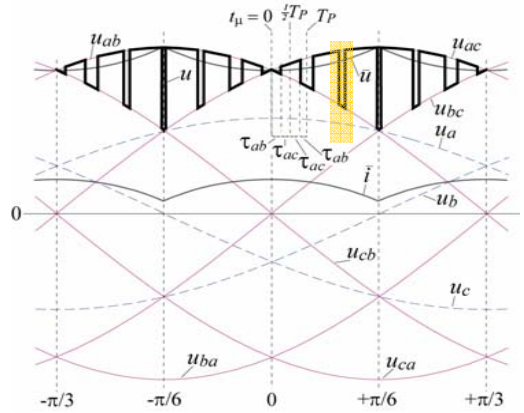


Example: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

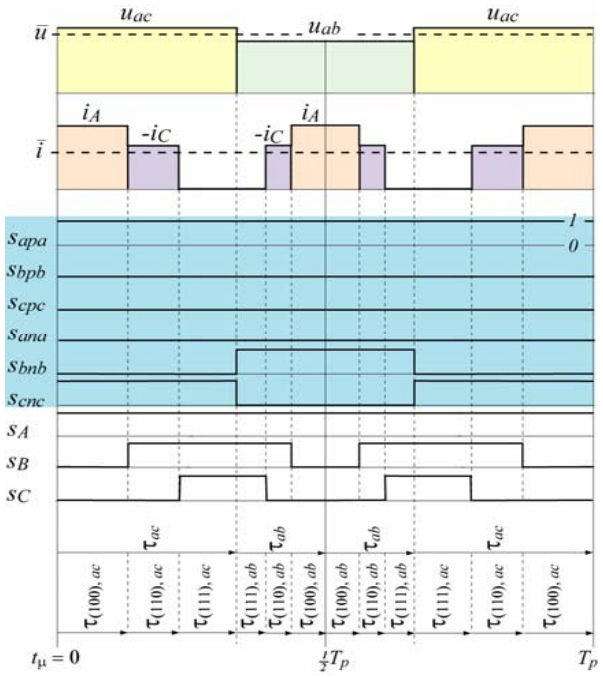
Constraints:
- No mains phases short-circuited
- No interruption of i

Zero DC Link Current Commutation for IMC





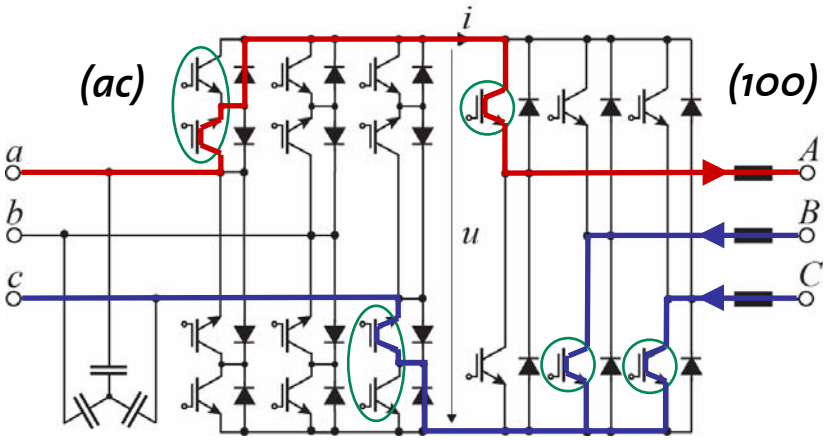
1/3 mains period



DC link voltage & current

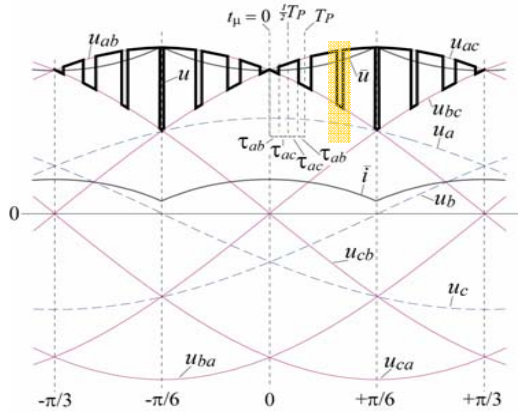
PWM pattern

Zero DC Link Current Commutation for IMC

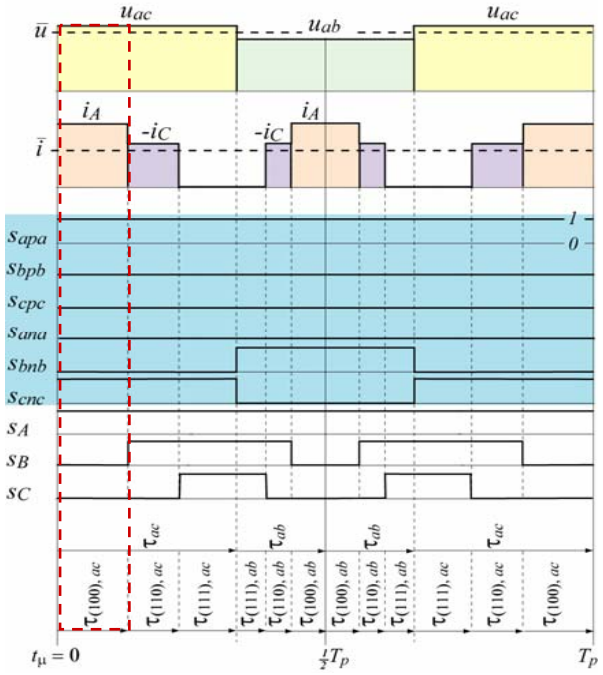


$u = u_{ac}$

$i = i_A$



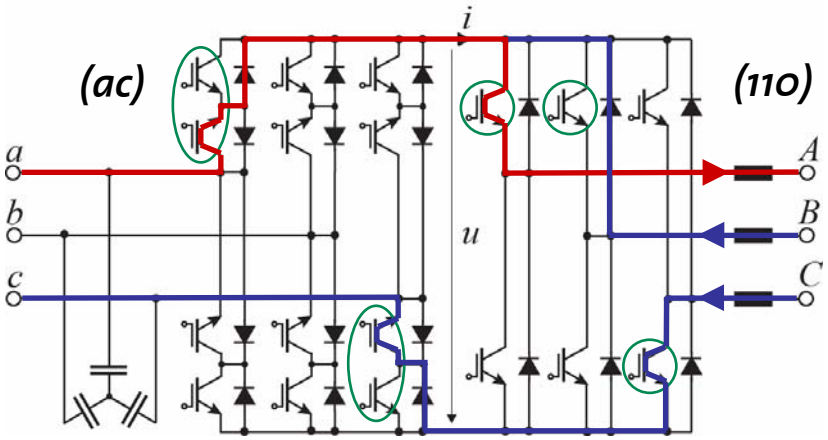
1/3 mains period



DC link voltage & current

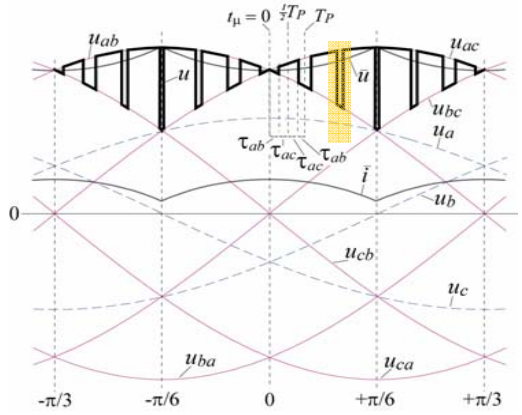
PWM pattern

Zero DC Link Current Commutation for IMC

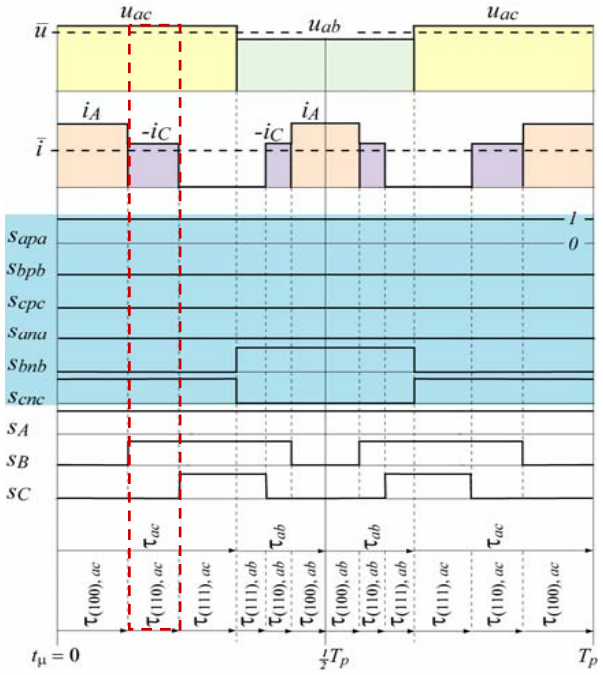


$u = u_{ac}$

$i = -i_C$



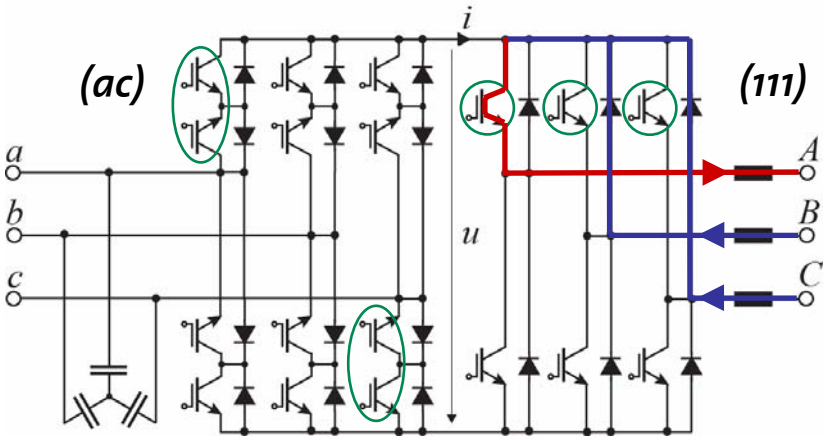
1/3 mains period



DC link voltage & current

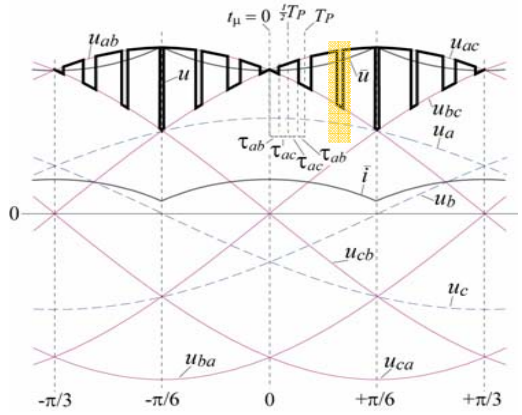
PWM pattern

Zero DC Link Current Commutation for IMC

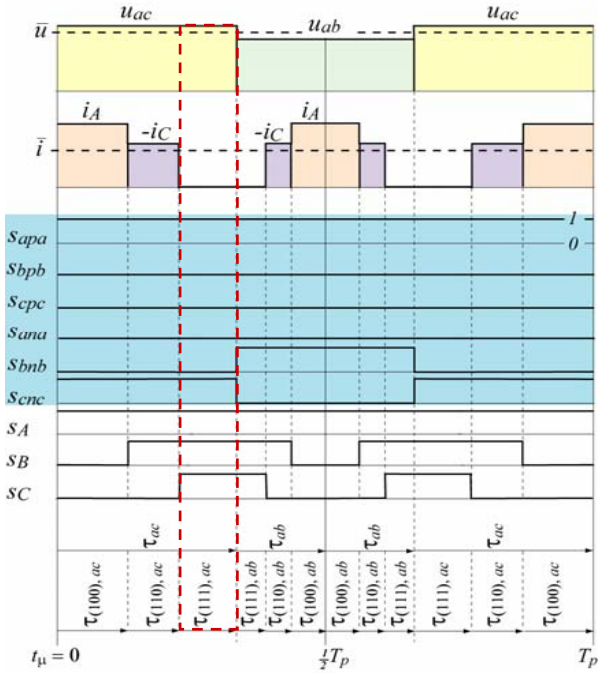


$u = u_{ac}$

$i = 0$



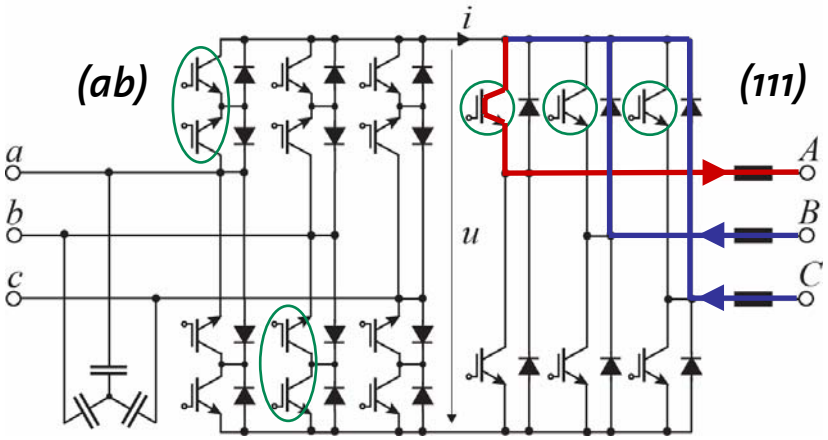
1/3 mains period



DC link voltage & current

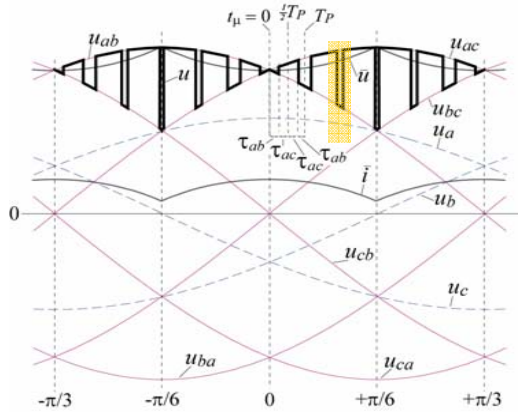
PWM pattern

Zero DC Link Current Commutation for IMC

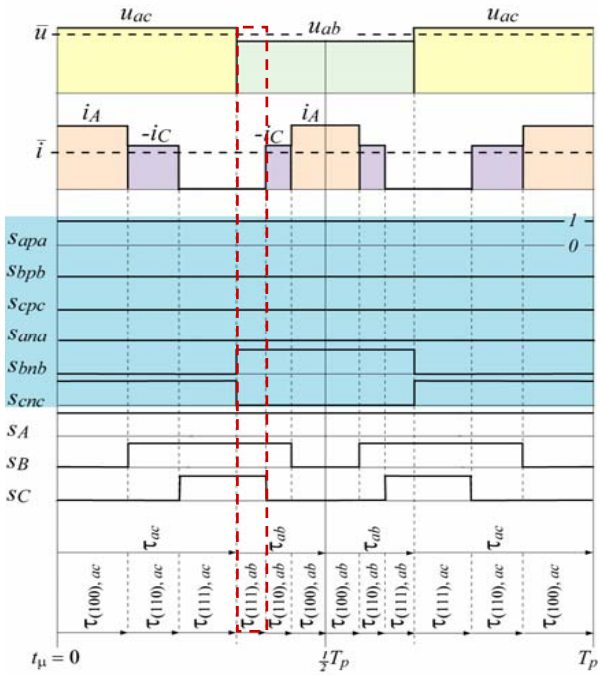


$u = u_{ab}$

$i = 0$



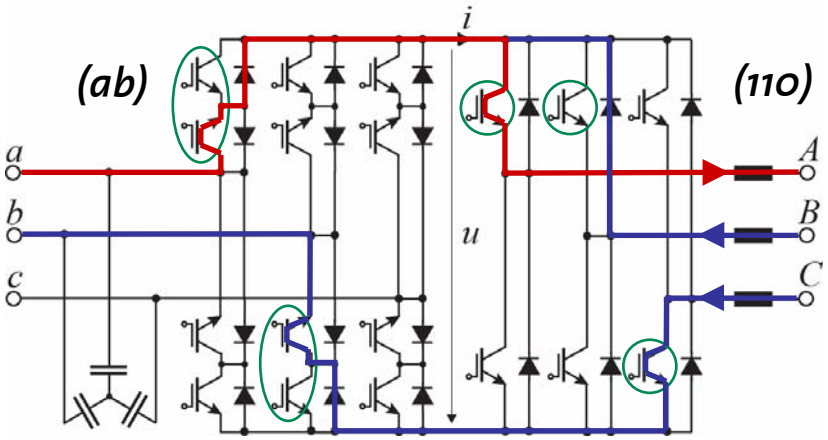
1/3 mains period



DC link voltage & current

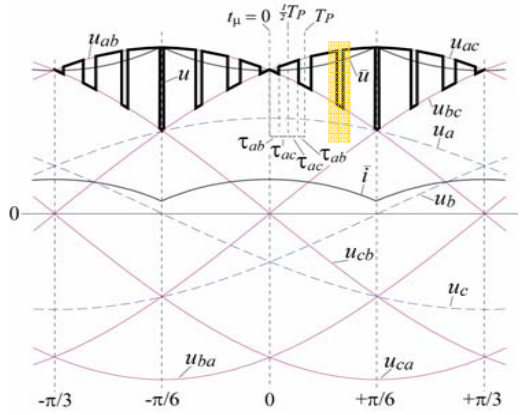
PWM pattern

Zero DC Link Current Commutation for IMC

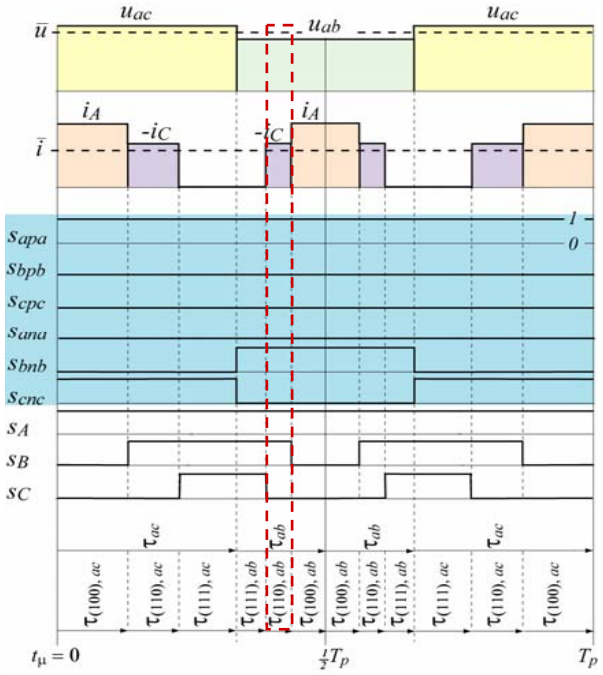


$u = u_{ab}$

$i = -i_C$



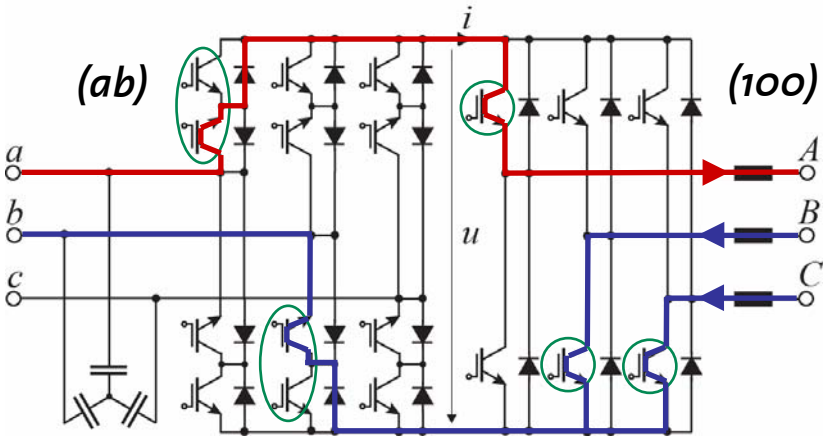
1/3 mains period



DC link voltage & current

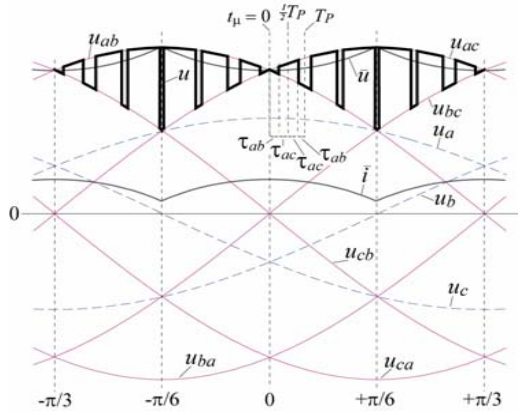
PWM pattern

Zero DC Link Current Commutation for IMC

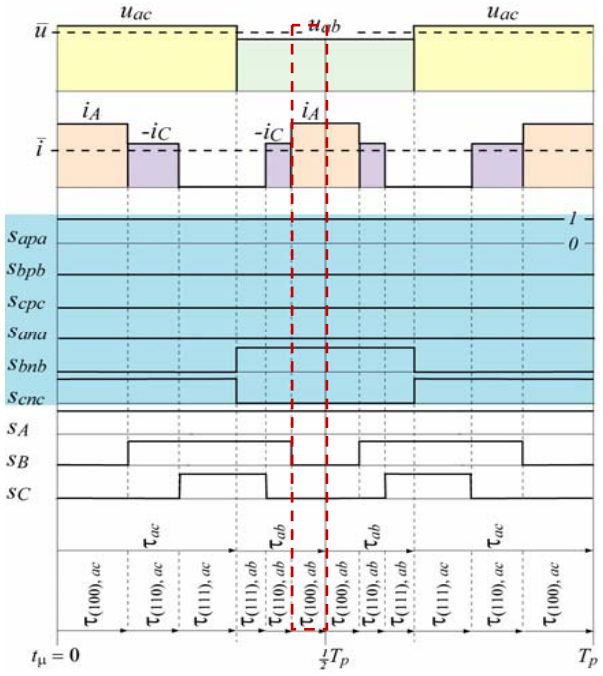


$u = u_{ab}$

$i = i_A$



1/3 mains period



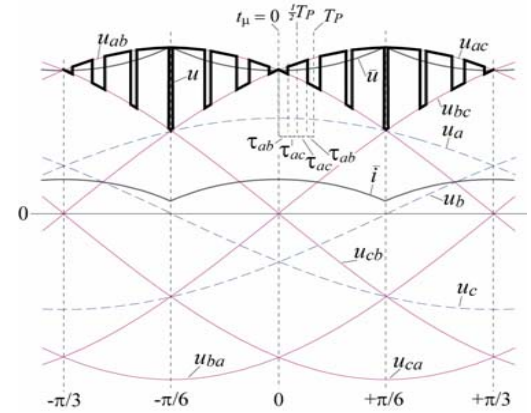
DC link voltage & current

PWM pattern

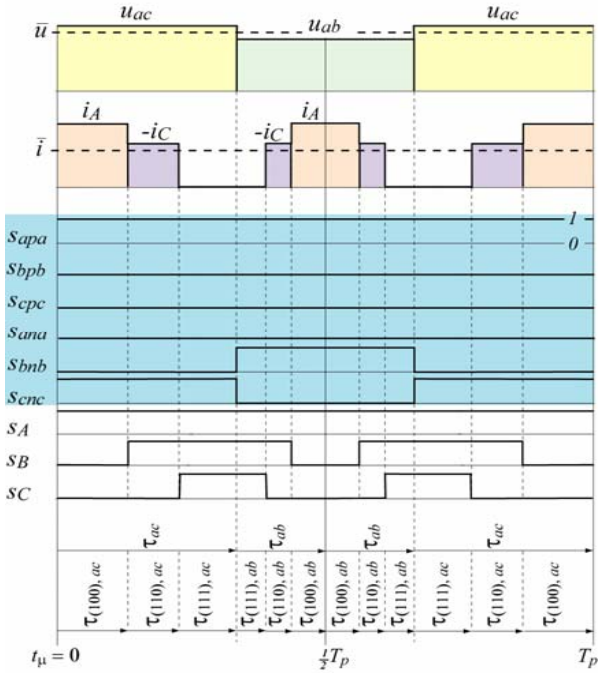
Zero DC Link Current Commutation for IMC

Summary

- Simple and robust modulation scheme as it is independent of voltages and currents (sign)
- Negligible rectifier switching losses due to zero current commutation of the rectifier stage



1/3 mains period



DC link voltage & current

PWM pattern

Space Vector Modulation

Derivation

Intervals considered

$\varphi_1 = 0...\pi/6$ $\varphi_2 = 0...\pi/6$

Free-wheeling limited to Inverter Stage

$d_{ab} + d_{ac} = 1$

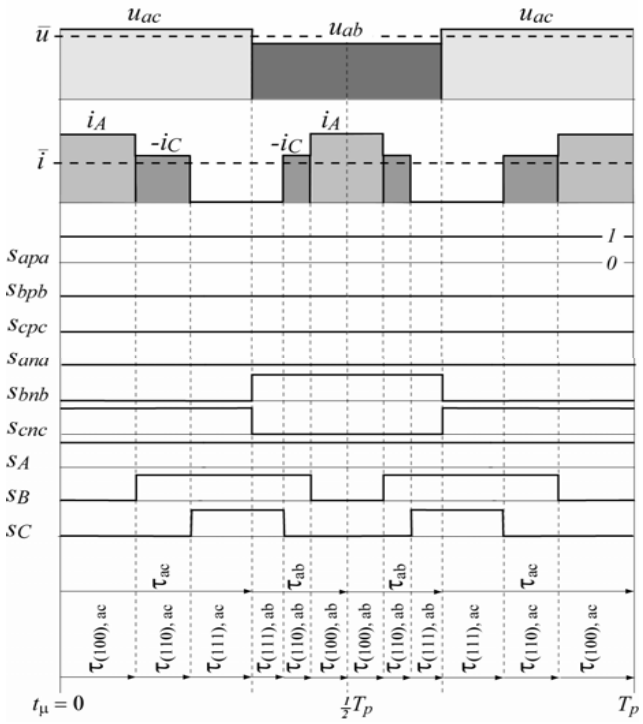
Local Average Value of Input Currents

$\bar{i}_a = (d_{ab} + d_{ac})\,\bar{i}, \quad \bar{i}_b = d_{ab}\,\bar{i}, \quad \bar{i}_c = d_{ac}\bar{i}$

Ohmic Fundamental Mains Behavior

$\cos\Phi_1 = 1$

$\bar{i}_a \sim u_a; \quad \bar{i}_b \sim u_b; \quad \bar{i}_c \sim u_c$



Relative Turn-on Times

$$d_{ac} = -\frac{\bar{i}_c}{\bar{i}_a} = -\frac{u_c}{u_a}; \qquad d_{ab} = -\frac{\bar{i}_b}{\bar{i}_a} = -\frac{u_b}{u_a}$$

Time Intervals

$\tau_{ac} = d_{ac}T_P/2 \qquad \tau_{ab} = d_{ab}T_P/2$

Identical Phase/Duty Cycle of Active Inverter Switching States (100), (110) in τ_{ac} and τ_{ab}

$$\delta_{(100),ac} = \frac{\tau_{(100),ac}}{\tau_{ac}} = \delta_{(100),ab} = \frac{\tau_{(100),ab}}{\tau_{ab}} = \delta_{(100)} \qquad \underline{u}_{(100)} = \tfrac{2}{3}u$$

$$\delta_{(110),ac} = \frac{\tau_{(110),ac}}{\tau_{ac}} = \delta_{(110),ab} = \frac{\tau_{(110),ab}}{\tau_{ab}} = \delta_{(110)} \qquad \underline{u}_{(110)} = \tfrac{2}{3}ue^{j\frac{\pi}{3}}$$

Generated Output Voltage Space Vector

$$\underline{u}_2^* = \frac{\frac{2}{3}}{\frac{T_P}{2}}(u_{ac}\tau_{(100),ac} + u_{ab}\tau_{(100),ab} + u_{ac}e^{j\frac{\pi}{3}}\tau_{(110),ac} + u_{ab}e^{j\frac{\pi}{3}}\tau_{(110),ab})$$

$$\underline{u}_2^* = \frac{\frac{2}{3}}{\frac{T_P}{2}}(u_{ac}\tau_{ac}\delta_{(100)} + u_{ab}\tau_{bc}\delta_{(100)} + u_{ac}\tau_{ac}\delta_{(110)}e^{j\frac{\pi}{3}} + u_{ab}\tau_{bc}\delta_{(110)}e^{j\frac{\pi}{3}}$$

$$= \tfrac{2}{3}(u_{ac}\frac{\tau_{ac}}{\frac{1}{2}T_P} + u_{ab}\frac{\tau_{ab}}{\frac{1}{2}T_P})\delta_{(100)} + \tfrac{2}{3}(u_{ac}\frac{\tau_{ac}}{\frac{1}{2}T_P} + u_{ab}\frac{\tau_{ab}}{\frac{1}{2}T_P})e^{j\frac{\pi}{3}}\delta_{(110)}$$

$$= \tfrac{2}{3}(u_{ac}d_{ac} + u_{ab}d_{ab})\delta_{(100)} + \tfrac{2}{3}(u_{ac}d_{ac} + u_{ab}d_{ab})e^{j\frac{\pi}{3}}\delta_{(110)}.$$

Local Average Value of the DC Link Voltage

$$\bar{u} = u_{ab}d_{ab} + u_{ac}d_{ac}$$

Output Voltage Space Vector

$$\underline{u}_2^* = \tfrac{2}{3}\bar{u}\,\delta_{(100)} + \tfrac{2}{3}\bar{u}e^{j\frac{\pi}{3}}\delta_{(110)}$$

Therefore, Calculation of the Relative On-Times of the Active Switching States of the Output Stage can be Directly Based on $\bar{u}$

$$\delta_{(100)} = \frac{\sqrt{3}}{2}\frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}}\cos(\varphi_2^* + \tfrac{\pi}{6})$$

$$\delta_{(110)} = \frac{\sqrt{3}}{2}\frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}}\sin\varphi_2^*$$

→ Absolute On-Times

$$\tau_{(100),ac} = -\frac{1}{\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_c\cos(\varphi_2^* + \tfrac{\pi}{6})$$

$$\tau_{(100),ab} = -\frac{1}{\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_b\cos(\varphi_2^* + \tfrac{\pi}{6})$$

$$\tau_{(110),ac} = -\frac{1}{\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_c\sin\varphi_2^*$$

$$\tau_{(110),ab} = -\frac{1}{\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_b\sin\varphi_2^*$$

Local Average Value of the DC Link Voltage

$$\bar{u} = \tfrac{3}{2}\hat{U}_1\frac{1}{\cos(\omega_1 t)} \qquad \bar{u}_{\min} = 3/2\,\hat{U}_1$$

Output Voltage Formation

Output Voltage System

$$u_A^* = \hat{U}_2^* \cos(\omega_2 t + \varphi_0)$$

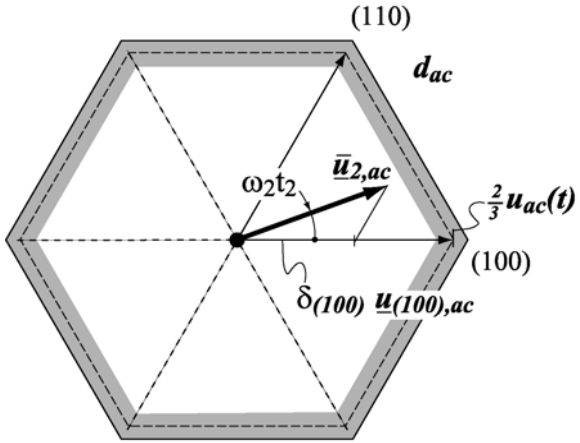
$$u_B^* = \hat{U}_2^* \cos(\omega_2 t - \tfrac{2\pi}{3} + \varphi_0)$$

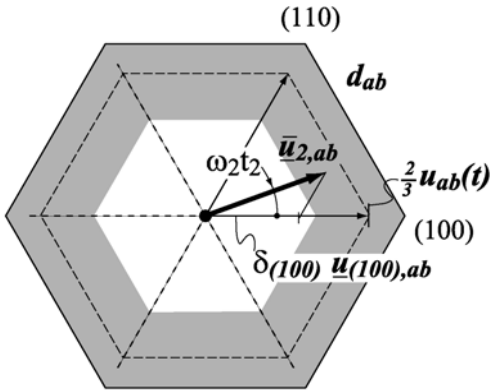
$$u_C^* = \hat{U}_2^* \cos(\omega_2 t + \tfrac{2\pi}{3} + \varphi_0)$$

Voltage Transfer Ratio

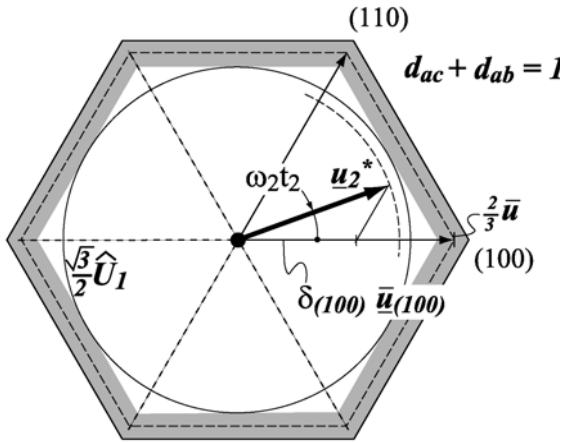
$$M = \frac{\hat{U}_2^*}{\hat{U}_1} \le \frac{\sqrt{3}}{2}$$

$$\hat{U}_{2,\max} = \frac{\sqrt{3}}{2} \cdot \hat{U}_1 = 0.866 \cdot \hat{U}_1$$





Inverter Output Voltage Space Vectors



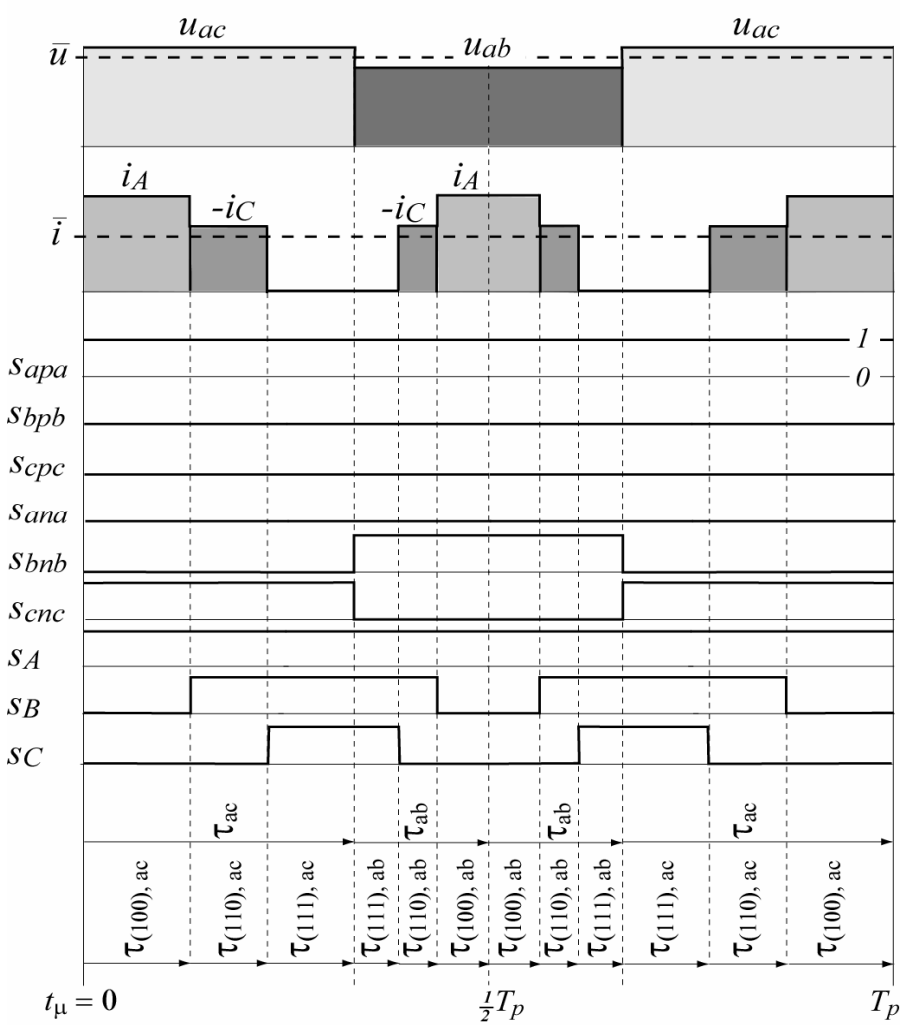
Average Output Voltage

Variation of $\bar{u}$ requires a Variation of the Inverter Modulation Index

$$m_2 = \frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}} = \frac{4}{3}\frac{\hat{U}_2^*}{\hat{U}_1}\cos(\omega_1 t)$$

Clamping

- Clamping of each output phase over a $\pi/3$-wide interval to minimize switching losses
- Switch conducting the largest current is clamped



Clamping over an Output Period

$\varphi_2=\omega_2 t$	u_A	u_B	u_C
0 ... $\pi/6$	u_p	u_p, u_n	u_p, u_n
$\pi/6$ ... $\pi/2$	u_p, u_n	u_p, u_n	u_n
$\pi/2$ ... $5\pi/6$	u_p, u_n	u_p	u_p, u_n
$5\pi/6$ ... $7\pi/6$	u_n	u_p, u_n	u_p, u_n
$7\pi/6$ ... $3\pi/2$	u_n, u_p	u_p, u_n	u_p
$3\pi/2$ ... $11\pi/6$	u_n, u_p	u_n	u_p, u_n
$11\pi/6$ ... 0	u_p	u_n, u_p	u_p, u_n

Input Current Formation

Load Phase Currents

$$i_A = \hat{I}_2 \cos(\omega_2 t + \Phi_2)$$

$$i_B = \hat{I}_2 \cos(\omega_2 t - \tfrac{2\pi}{3} + \Phi_2)$$

$$i_C = \hat{I}_2 \cos(\omega_2 t + \tfrac{2\pi}{3} + \Phi_2)$$

Verify Equal Local Average Value $\bar{i}$ of the DC Link Current in τ_{ac} and τ_{ab}

$$\bar{i}_{ac} = \frac{1}{\tau_{ac}}(i_A \delta_{(100),ac} \tau_{ac} - i_C \delta_{(110),ac} \tau_{ac}) = i_A \delta_{(100)} - i_C \delta_{(110)}$$

$$\bar{i}_{ab} = \frac{1}{\tau_{ab}}(i_A \delta_{(100),ab} \tau_{ab} - i_C \delta_{(110),ab} \tau_{ab}) = i_A \delta_{(100)} - i_C \delta_{(110)}$$

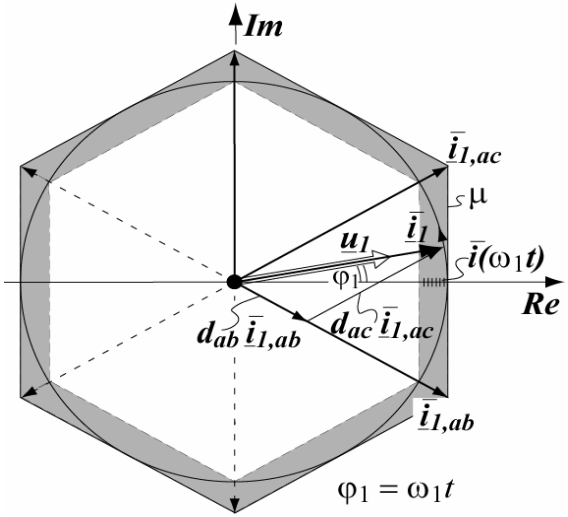
$$\bar{i} = \bar{i}_{ac} = \bar{i}_{ab} = \tfrac{3}{4} m_2 \hat{I}_2 \cos\Phi_2 = \hat{I}_2 \frac{\hat{U}_2^*}{\hat{U}_1} \cos\Phi_2 \cos(\omega_1 t)$$

Variation of Input Stage Modulation Index due to Varying $\bar{i}$

$$m_1 = \frac{|\underline{\bar{i}}_1|}{\bar{i}} = \frac{1}{\cos\omega_1 t}$$

Resulting Input Current Space Vector

$$|\underline{\bar{i}}_1| = \bar{i}\, m_1 = \hat{I}_2 \frac{\hat{U}_2^*}{\hat{U}_1} \cos\Phi_2 \cos(\omega_1 t) \frac{1}{\cos\omega_1 t} = \hat{I}_1$$



Resulting Input Phase Currents

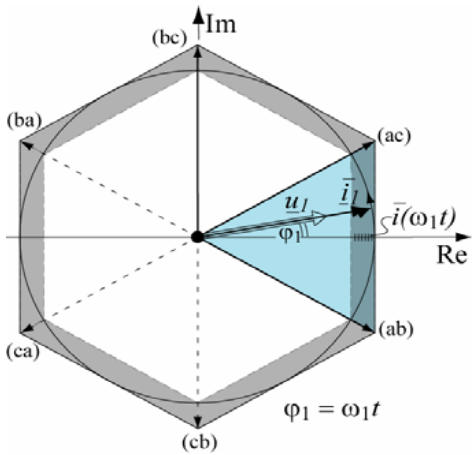
$$\bar{i}_a = \hat{I}_1 \cos(\omega_1 t)$$

$$\bar{i}_b = \hat{I}_1 \cos(\omega_1 t - \frac{2\pi}{3})$$

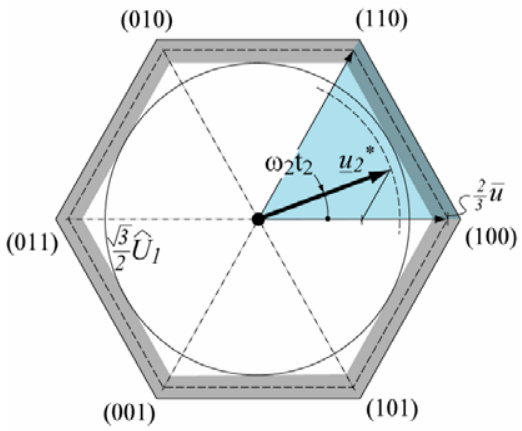
$$\bar{i}_c = \hat{I}_1 \cos(\omega_1 t + \frac{2\pi}{3})$$

Space Vector Modulation Summary

- Phase of resulting input vector is adjustable
- Output voltage vector u_2^* is adjustable
- PWM pattern is specific for each combination of input and output stage sectors



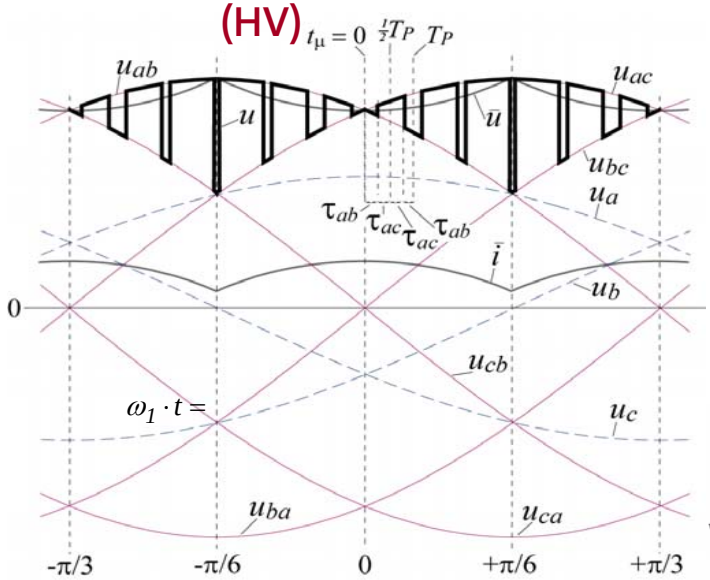
Rectifier (input) stage



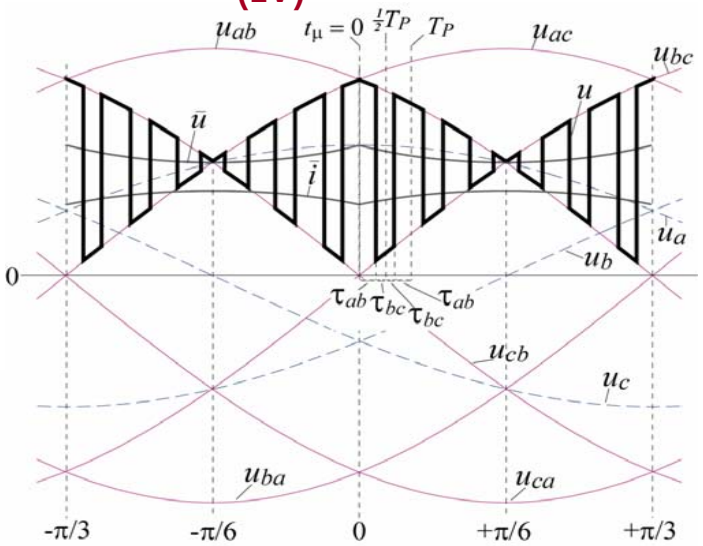
Inverter (output) stage

Conventional vs. Low Output Voltage Modulation

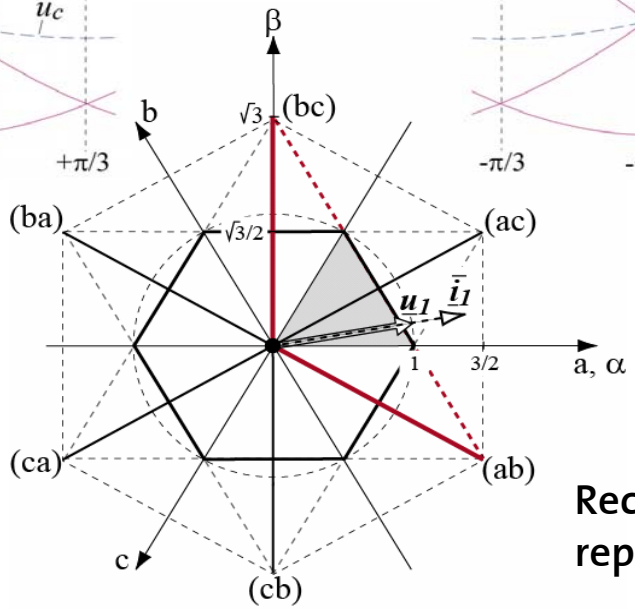
Conventional Modulation (HV)



Low Output Voltage Modulation (LV)



$$\hat{U}_{2,max,I} = \frac{\sqrt{3}}{2}\hat{U}_1 \approx 0.86 \cdot \hat{U}_1$$

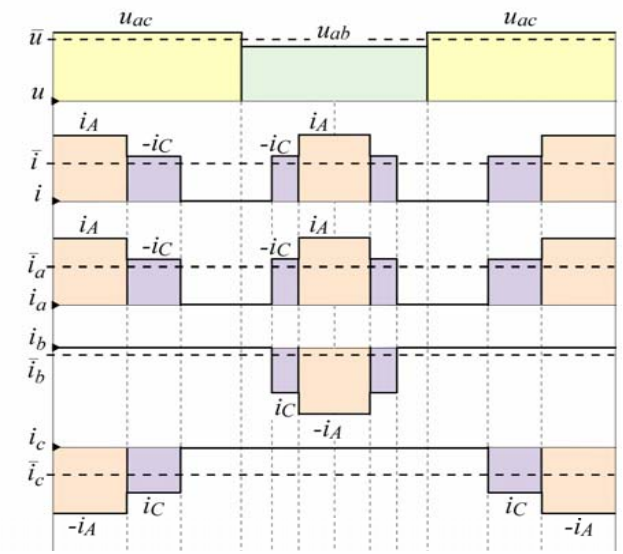


$$\hat{U}_{2,max,II} = \frac{1}{2}\hat{U}_1 = 0.5 \cdot \hat{U}_1$$

Rectifier space vector representation

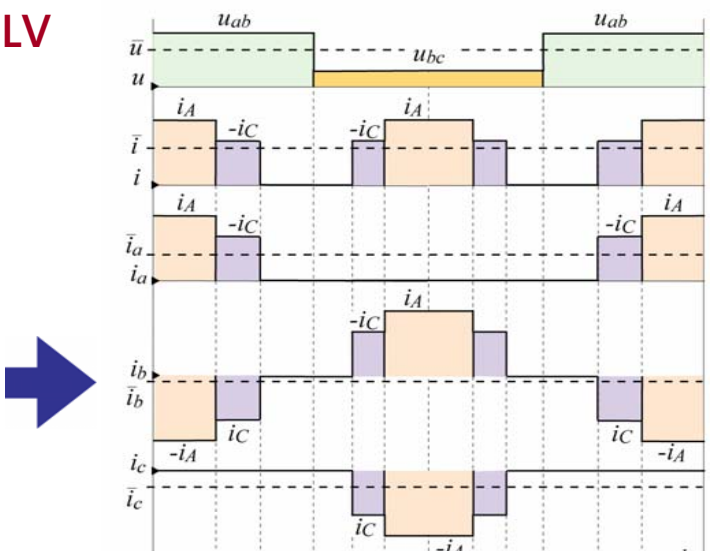
Conventional vs. Low Output Voltage Modulation

HV



- One input phase (*a*) is clamped to one DC link bus (*p*)
- Other input phases (*b*, *c*) are switched to the remaining DC link bus (*n*)

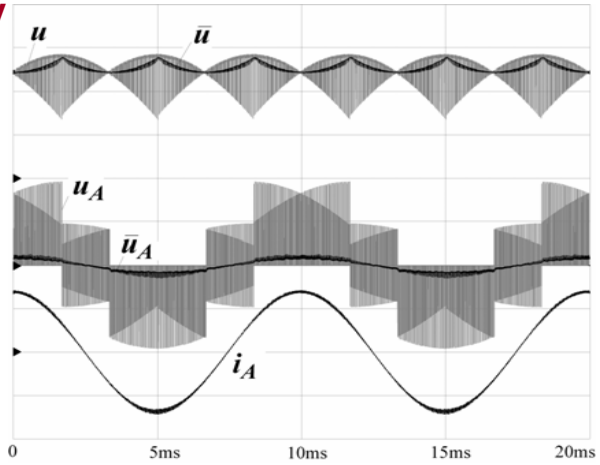
LV

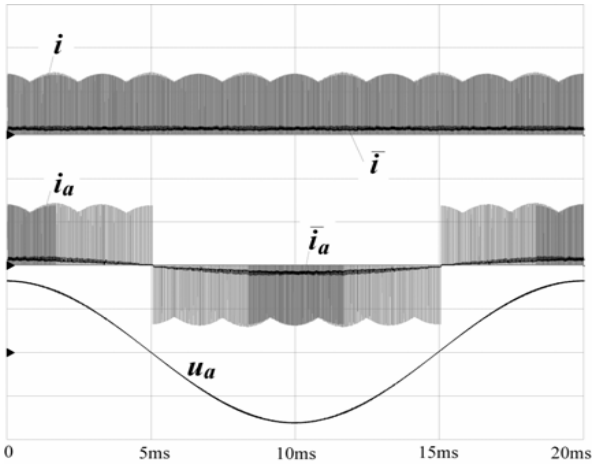


- No input phase is clamped to the DC link bus
- One input phase (*b*) is switched between the positive (p) and the negative (*n*) bus
- Current blocks of both polarities appear in one input phase (*b*)

Conventional vs. Low Output Voltage Modulation

HV





Output Voltage Generation

Parameters:

f_1 = 50 Hz

f_2 = 100 Hz

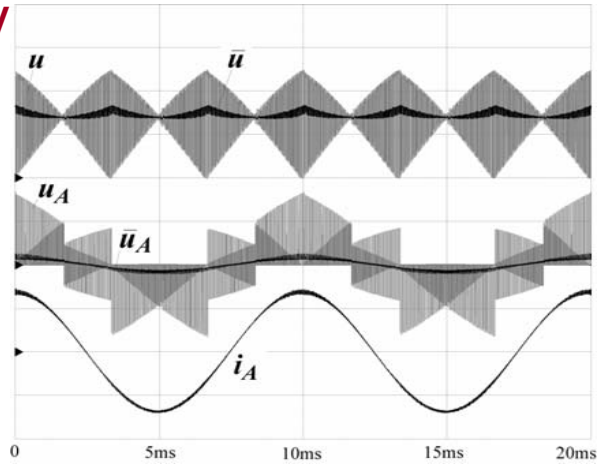
f_P = 20 kHz

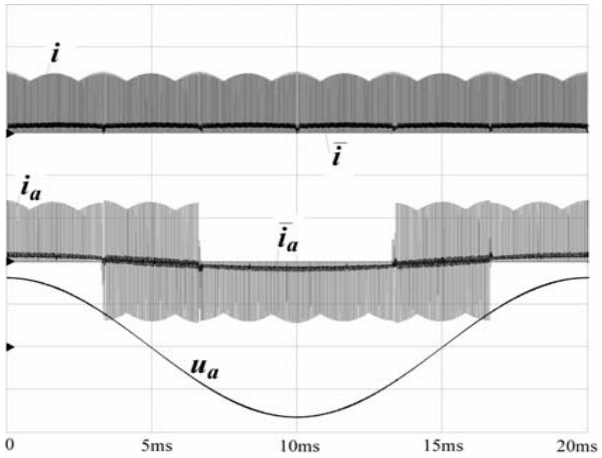
L = 1 mH

C = 9 µF

Input Current Generation

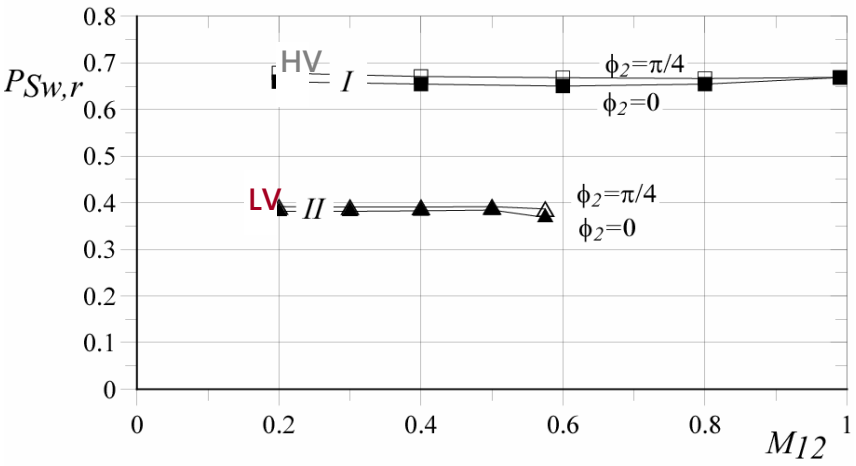
LV



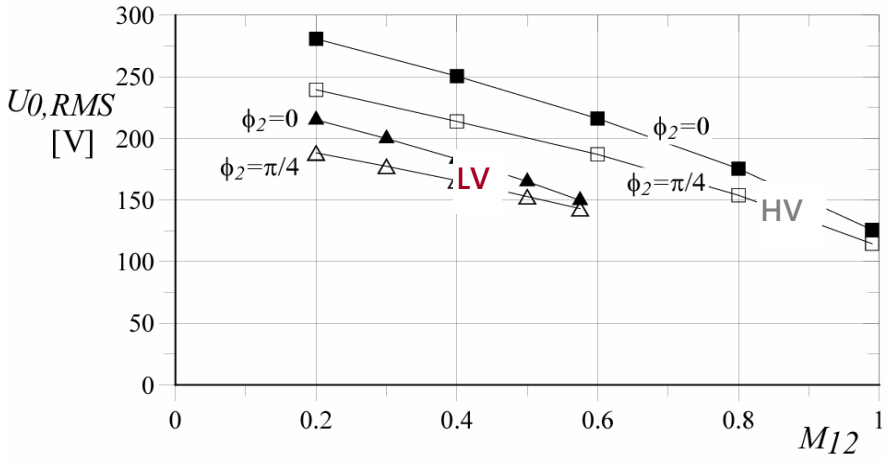


Conventional vs. Low Output Voltage Modulation

Switching Losses



Output Common Mode Voltage

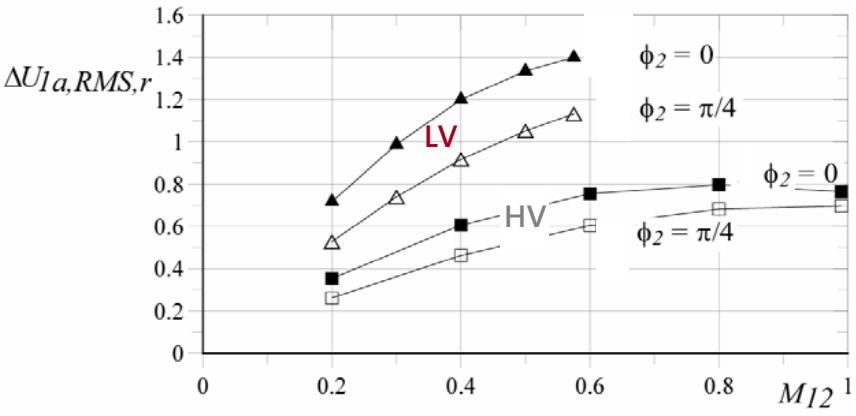


Reduction of switching losses of approximately 58%

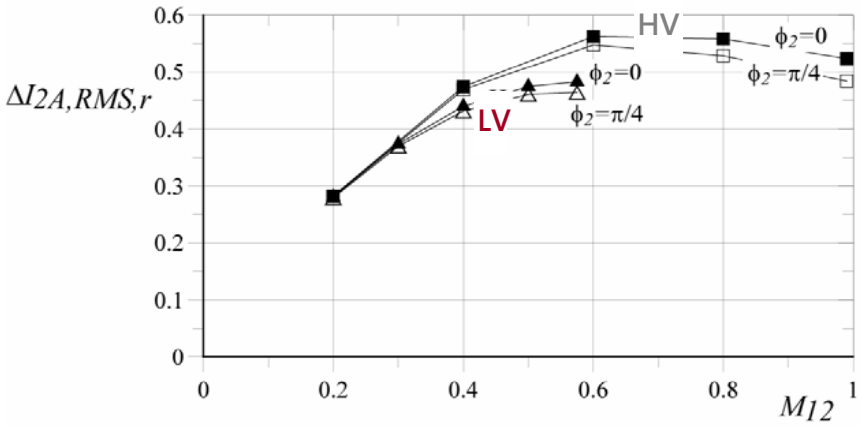
Output common mode voltage is reduced to approximately 75%

Conventional vs. Low Output Voltage Modulation

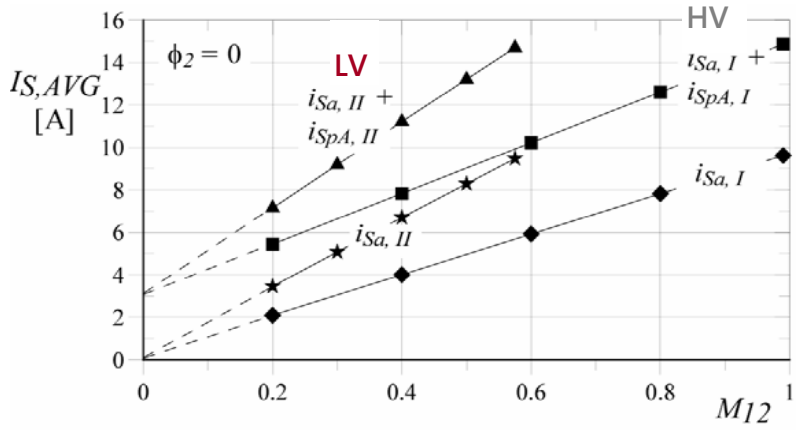
Switching Losses



Output Current Ripple



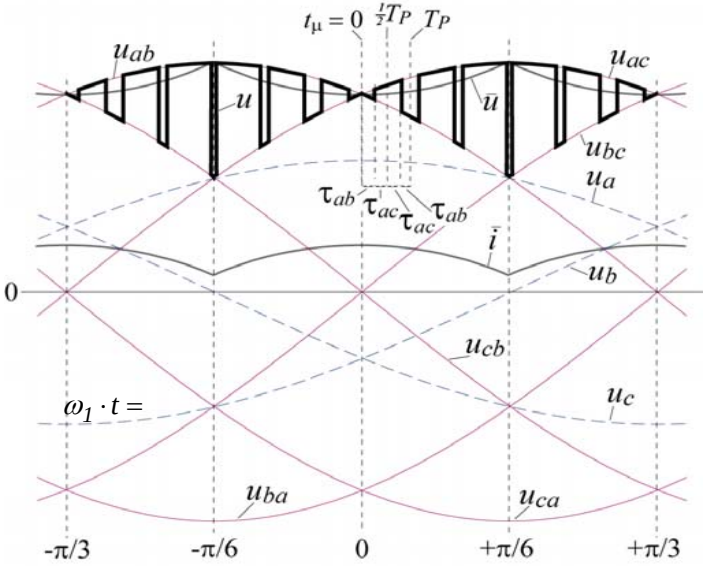
Current Stresses



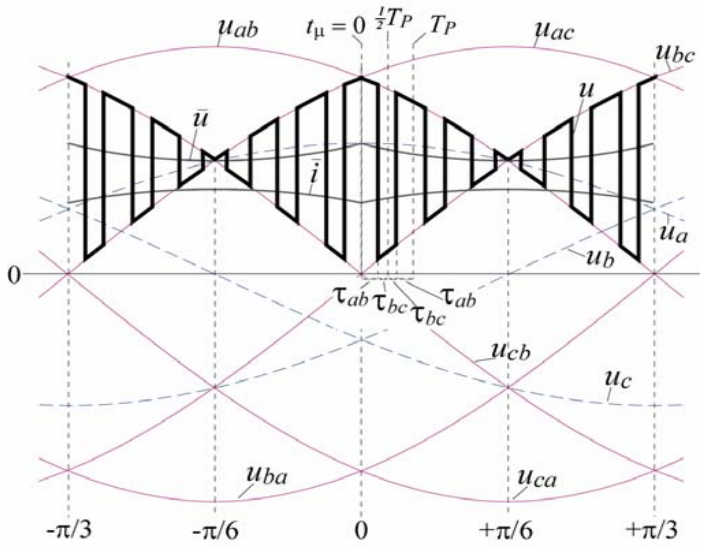
- Input voltage ripple doubles
- Output current ripple slightly reduced
- For given $\hat{U}_2$ (M_{12}) the component current stress increases (conduction losses)

3-Level Modulation Scheme

Conventional Modulation (HV)



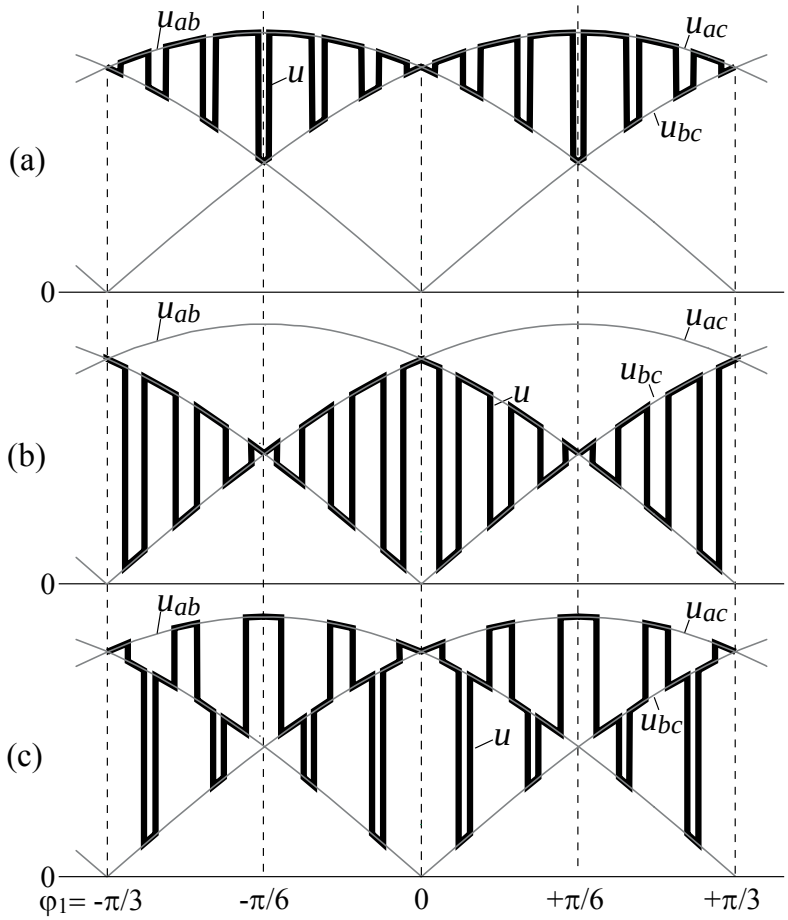
Low Output Voltage Modulation (LV)



3 Output Voltage Level Modulation (3LV)

- Weighted combination of HV and LV modulation
- Lowers output current ripple
- Reduction of the output common voltage

3-Level Modulation Scheme



Conventional / High Output Voltage Modulation (HV)

$$\hat{U}_2 = 0 \ldots \frac{\sqrt{3}}{2} \cdot \hat{U}_1$$

Low Output Voltage Modulation (LV)

$$\hat{U}_2 = 0 \ldots \frac{1}{2} \cdot \hat{U}_1$$

3 Output Voltage Level Modulation (3LV)

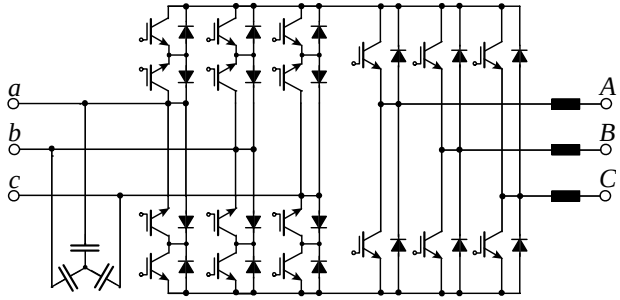
$$\hat{U}_2 = \frac{1}{2} \ldots \frac{\sqrt{3}}{2} \cdot \hat{U}_1$$

Advanced Modulation Schemes

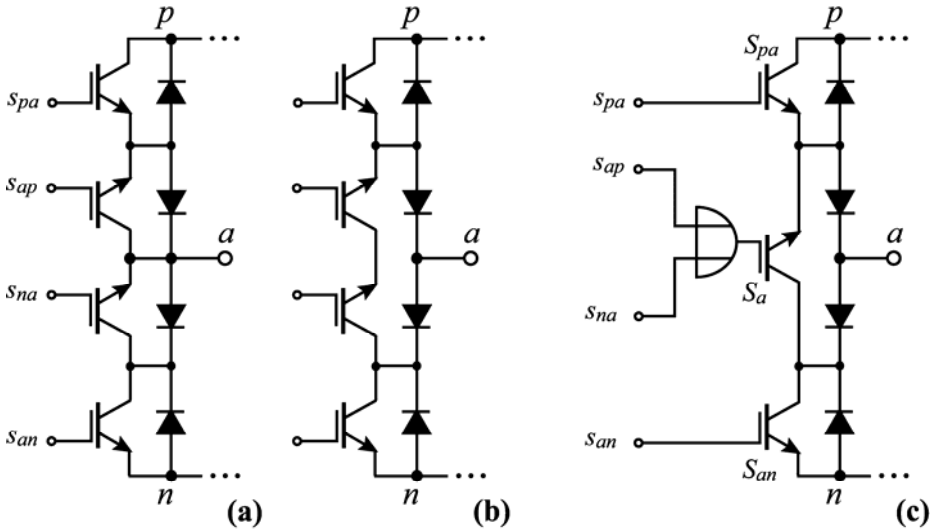
Conventional:	*Modified:*	*Modulation Differs for:*
High Output Voltage Modulation	**Low Output Voltage Modulation** + Reduced Switching Losses - Max. Output Voltage is Reduced	Input Stage (Formation of DC-link Voltage)
Switching Losses in Output Stage Only	**Switching Loss Shifting to Input Stage** + Shifting & Splitting Switching Losses - Works for Output Phase Displacement $\phi_2 < \pi/6$ & High Output Currents Only	Input- & Output Stage (Commutation Interaction)
None Reactive Power Coupling	**Input & Output Reactive Power Coupling** **RPC I** **RPC II** + Purely Reactive Output Power can be Coupled to Purely Reactive Input Power - Works with "Switching Loss Shifting" in Special Cases Only	Input- & Output Stage (Formation of Reactive Input Current / Output Voltage)

Sparse Matrix Converter (SMC)

Standard IMC Topology with 18 Switches



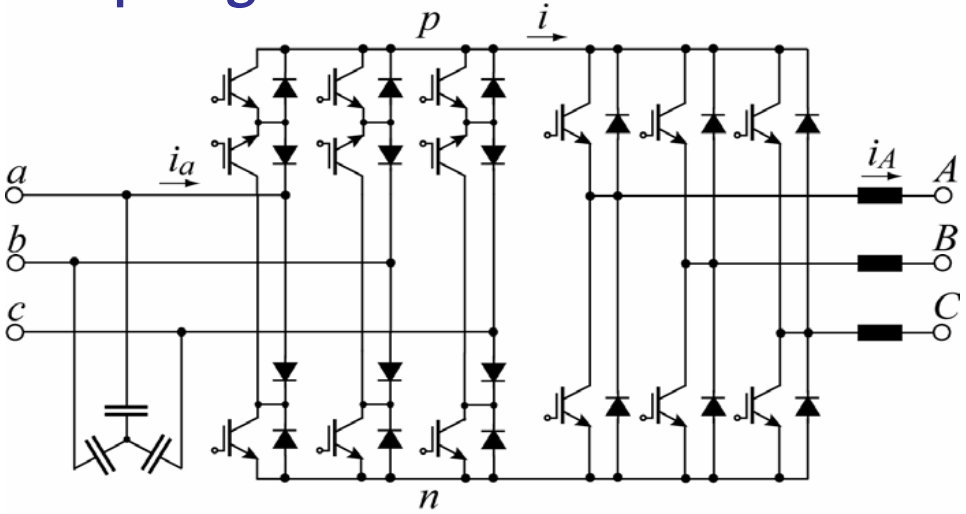
Derivation of the SMC Bridge Leg Configuration



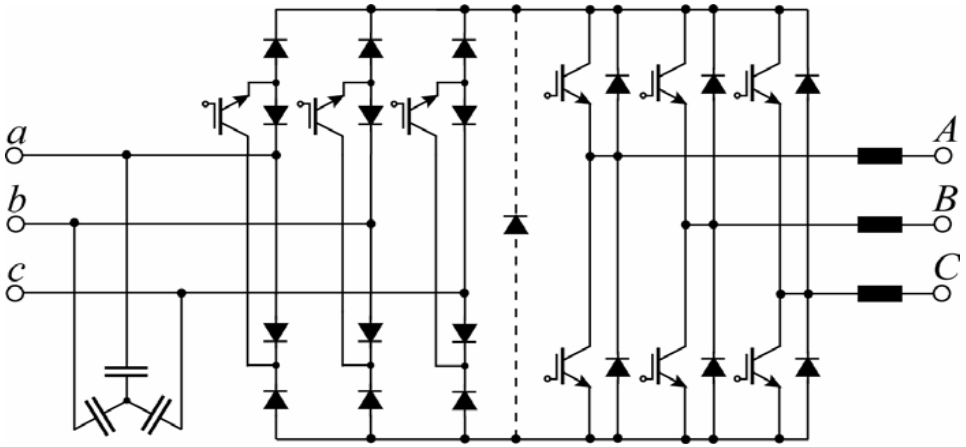
As the operation is restricted to $u_{pn} > 0$, blocking of S_{na} within the turn-on interval of S_{ap} is not required and both transistors are combined into a single transistor S_a

Sparse Matrix Converter Topologies

Sparse Matrix Converter (SMC)
Bidirectional



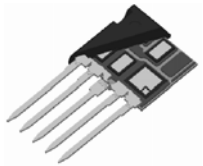
Ultra Sparse Matrix Converter (USMC)
Unidirectional



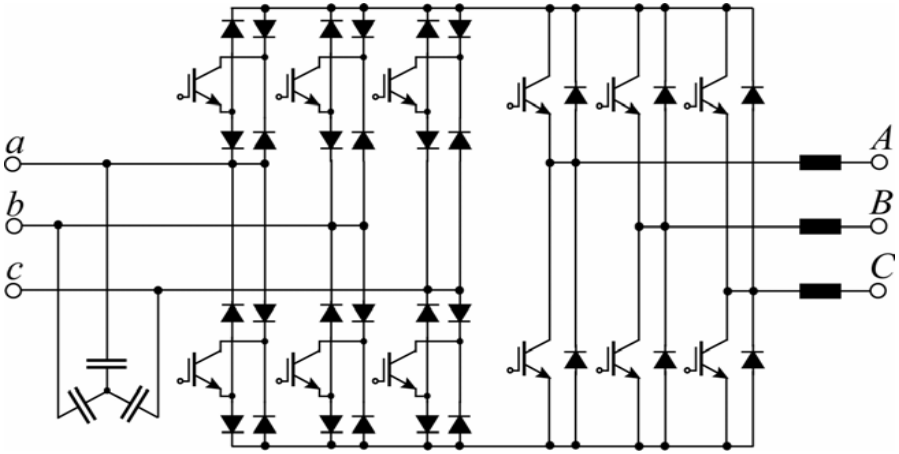
$$\Phi_1 \in (-\tfrac{\pi}{6}, +\tfrac{\pi}{6})$$
$$\Phi_2 \in (-\tfrac{\pi}{6}, +\tfrac{\pi}{6})$$

Sparse Matrix Converter Topologies

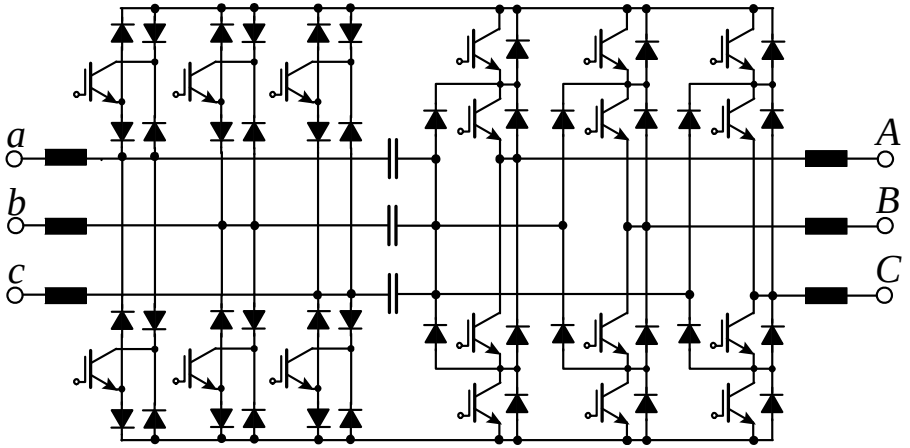
Very Sparse Matrix Converter (VSMC)
Bidirectional



Four-Quadrant Switch
IXYS FIO 50-12BD



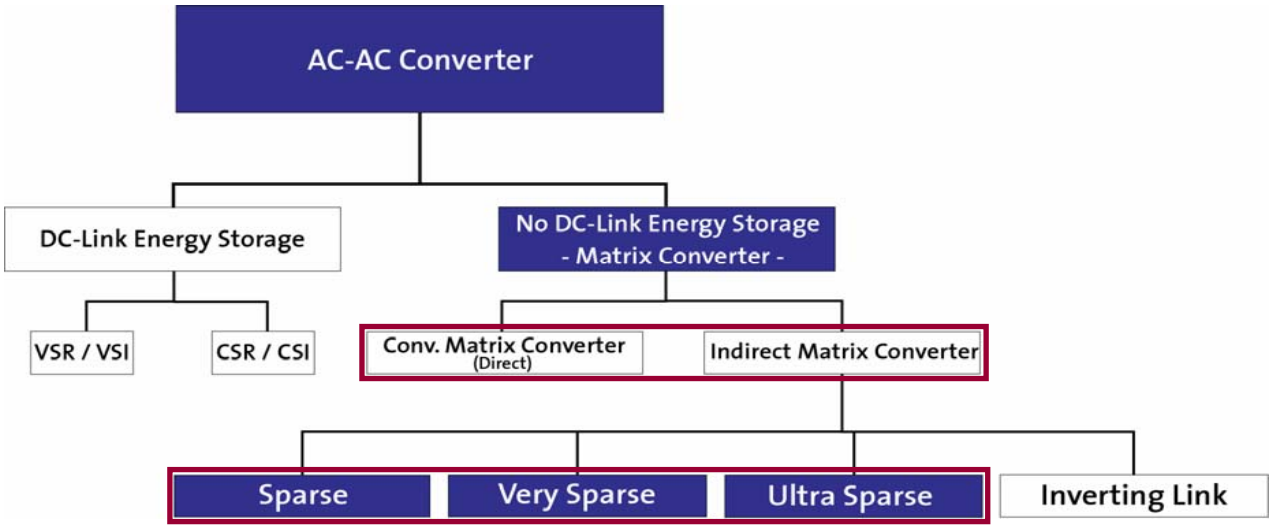
Three-Level Output Sparse Matrix Converter
Bidirectional



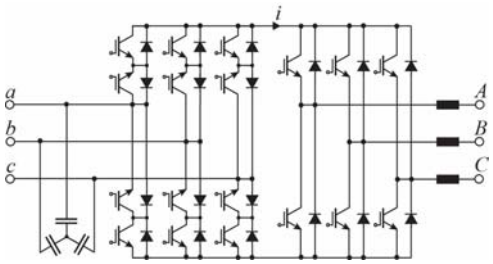
Realization Effort of Matrix Converters

Number of Transistors, Diodes and Isolated Driver Potentials

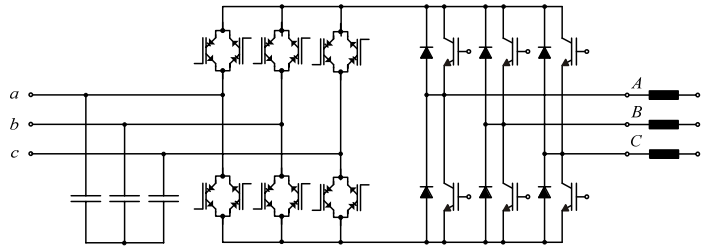
Converter Type	Transistors	Diodes	Isolated Driver Potentials
CMC	18	18	6
IMC	18	18	8
SMC	15	18	7
VSMC	12	30	10
USMC	9	18	7



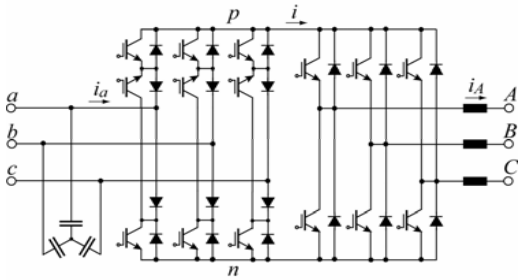
Indirect Matrix Converter Topology Overview



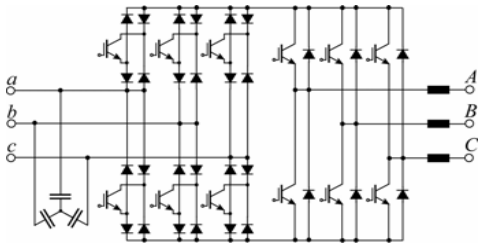
Indirect Matrix Converter (IMC)



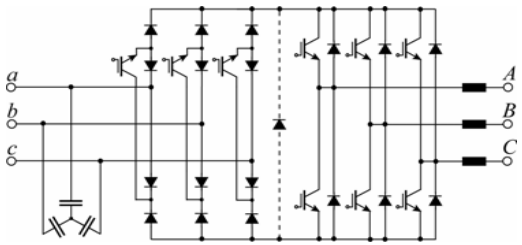
RB-IGBT Indirect Matrix Converter



Sparse Matrix Converter (SMC)



Very Sparse Matrix Converter (VSMC)

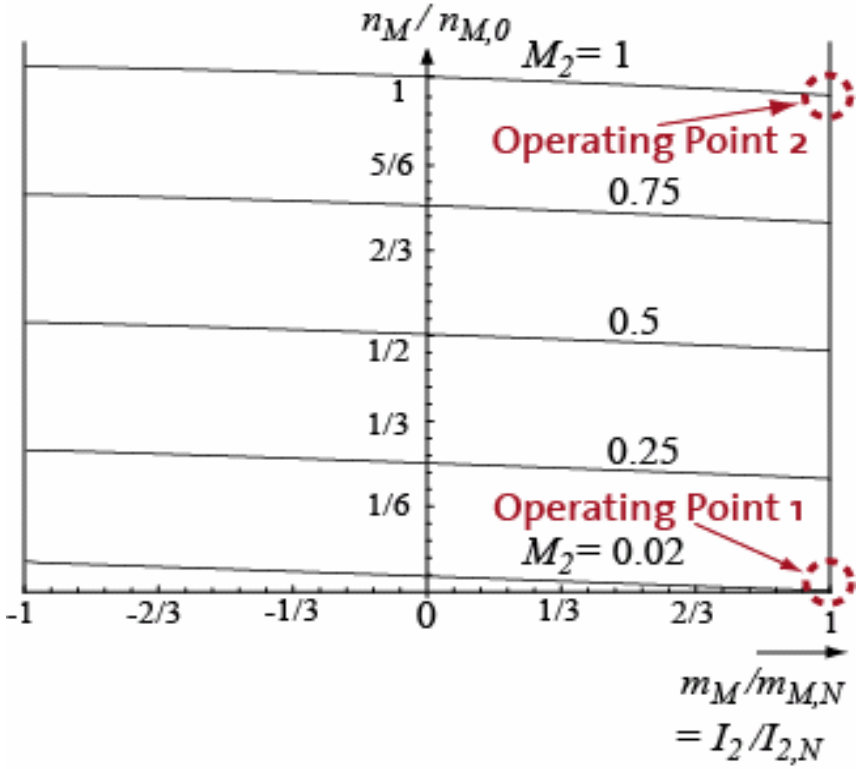


Ultra Sparse Matrix Converter (USMC)

Dimensioning Procedure

Dimensioning

Basic Considerations for Drive Application



Example of a steady state torque-speed characteristic of a PMSM

Operating Point 2

Nominal load torque: $m_M = m_{M,N}$,

Nominal speed: $n_M \approx n_{M,o}$

Output phase displacement: $\Phi_2 < 10°$

Operating Point 1

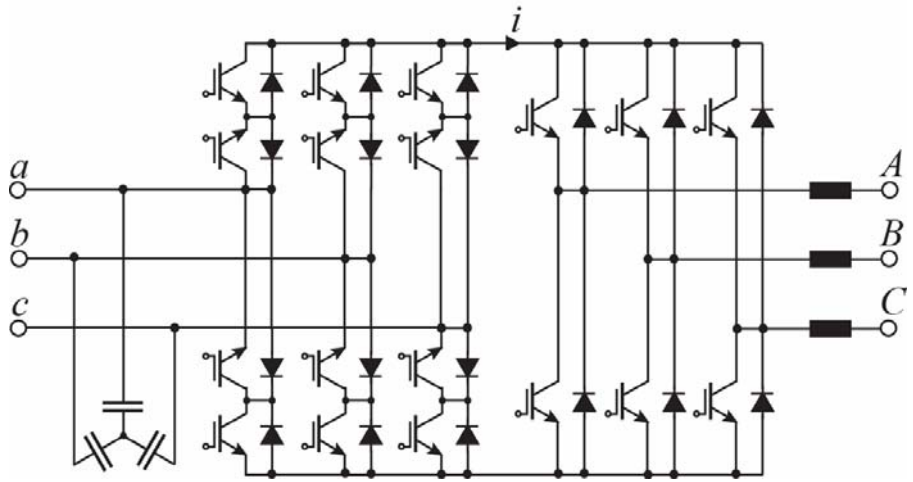
Nominal load torque: $m_M = m_{M,N}$,

Speed near zero: $n_M \approx 0$

Output phase displacement: $\Phi_2 \approx 0°$

Dimensioning

Loss Distribution

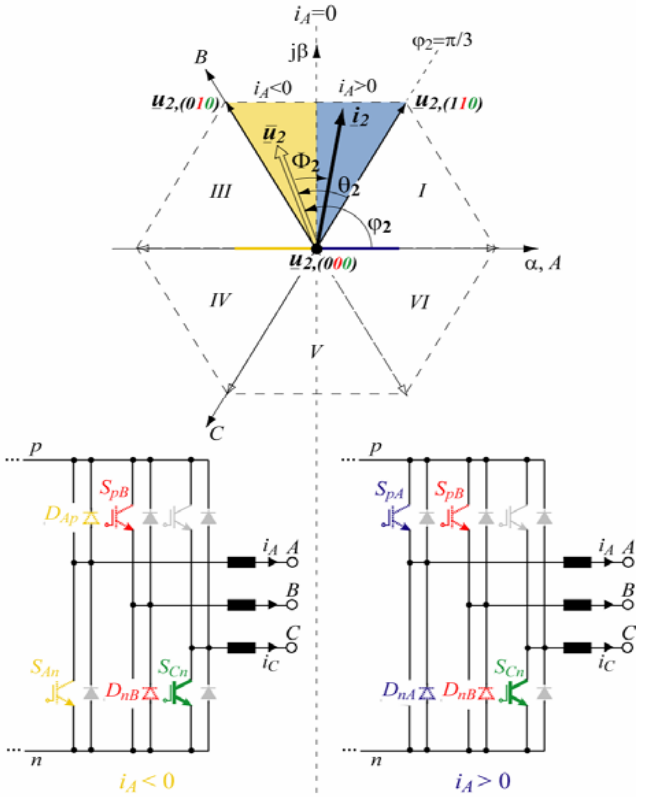


Input Stage

- Conduction losses
- Due to zero DC link current commutation, switching losses are negligible

Output Stage

- Conduction losses
- Switching losses



Positions of $\underline{\bar{u}}_2$ and $\underline{i}_2$ determine which semiconductors are subject to power losses

Dimensioning

Procedure for Loss Calculation

- Conduction and switching loss measurement on high performance test setup
- Determination of a set of parameters by a given interpolation approach (polynomial parameters)

$$\boldsymbol{K_i}\ ,i=1\ldots5$$

- **2** "Universal" analytic expressions for semiconductor dimensioning at

  Operating point 1 (local maxima): $\overline{\boldsymbol{p}}_{\boldsymbol{Dev,max}} = f\,(f_p\,,\hat{U}_1\,,\hat{I}_2\,,\boldsymbol{K_i})$

  Operating point 2 (global average): $\boldsymbol{P_{Dev}} = f\,(f_p\,,\hat{U}_1\,,\hat{I}_2\,,\boldsymbol{K_i})$

- Limitation of the output current and overall converter efficiency

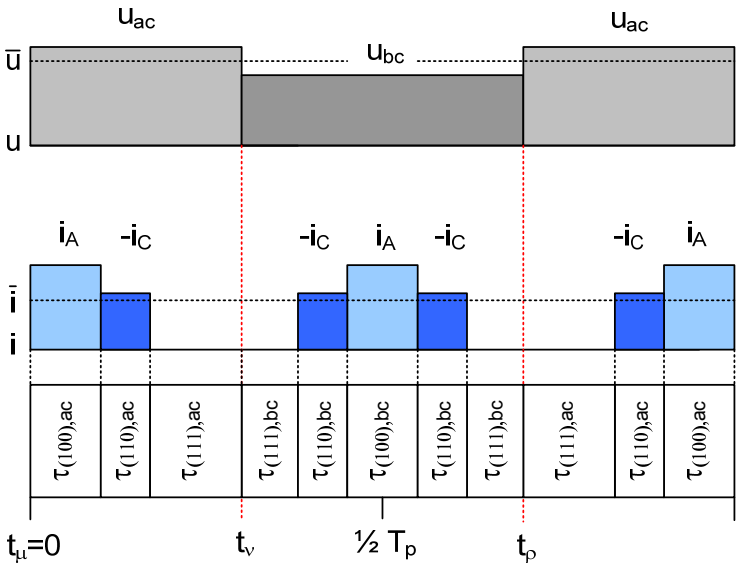
$$\hat{I}_{2,max,OP1} = f\,(\overline{\boldsymbol{p}}_{\boldsymbol{Dev,max}}\,,R_{th}\,,T_j\text{-}T_H),\quad \hat{I}_{2,max,OP2} = f\,(\boldsymbol{P_{Dev}}\,,R_{th}\,,T_j\text{-}T_H)$$

$$\eta_{,OP1} = f\,(\overline{\boldsymbol{p}}_{\boldsymbol{Dev,max}}\,,\hat{I}_{2,max,OP1}),\qquad \eta_{,OP2} = f\,(\boldsymbol{P_{Dev}}\,,\hat{I}_{2,max,OP2})$$

Switching Loss Measurements

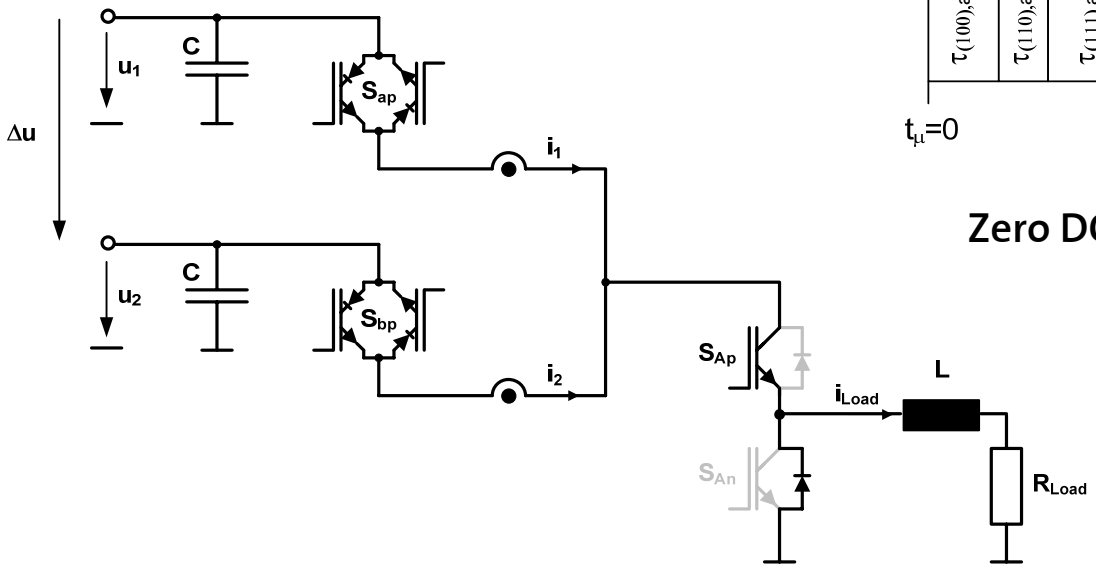
Four Commutation Cases

- $\Delta u > 0$ and $\Delta u < 0$
- $i_{Load} > 0$ and $i_{Load} < 0$



Zero DC link current commutation

Measurement setup for an IMC, using RB-IGBTs in the input stage



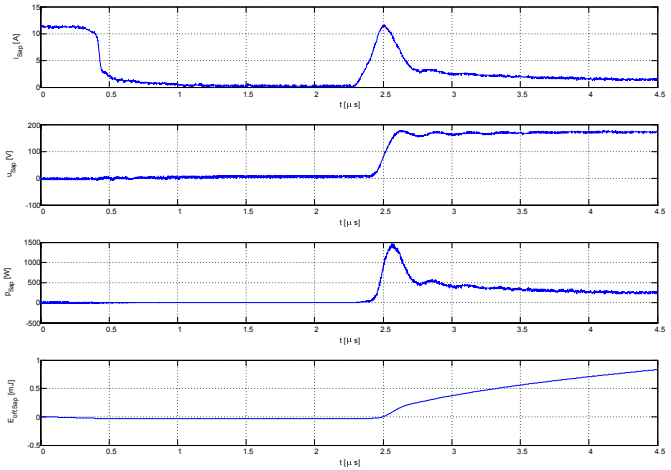
Switching Loss Measurements

Measurement Data Processing

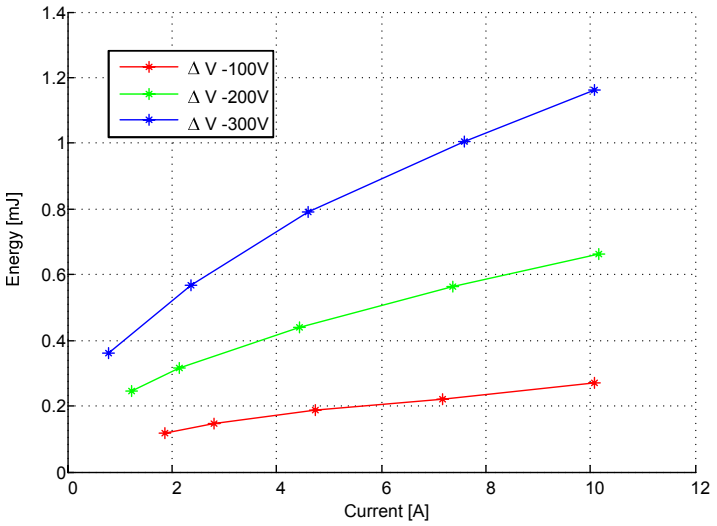
- Use of switching loss polynomial

$$w_S(u,i) = K_1 \cdot u \cdot i_2 + K_2 \cdot u \cdot i_2^{\,2} + K_3 \cdot u^2 + K_4 \cdot u^2 \cdot i_2 + K_5 \cdot u^2 \cdot i_2^{\,2}$$

- Coefficients are derived by least square approximation of the measured data
- Coefficients are used for analytical loss calculation

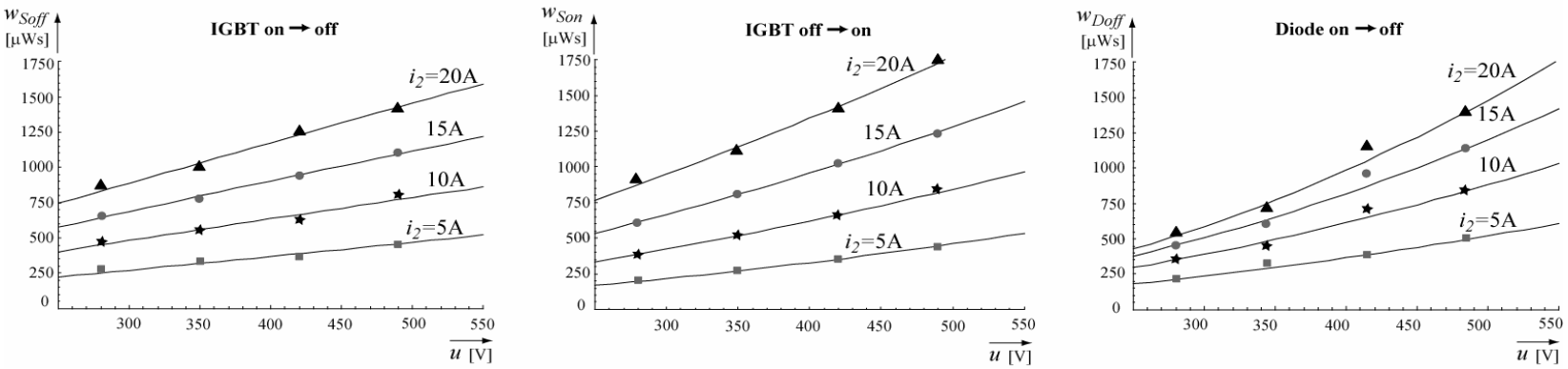


Example of fitted curves, $E_{off,\Delta u<0}$



Switching Loss Measurements

Example of Measurement Data Output



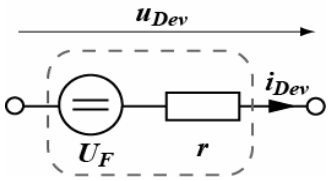
$$w_{Son}(u,i) = K_{Son1} \cdot u \cdot i_2 + K_{Son2} \cdot u \cdot {i_2}^2 + K_{Son3} \cdot u^2 + K_{Son4} \cdot u^2 \cdot i_2 + K_{Son5} \cdot u^2 \cdot {i_2}^2$$

IGBT- Switching Loss Parameter						
T_j		K_1	K_2	K_3	K_4	K_5
25°C	S_{off}	129	$-947\ 10^{-3}$	$471\ 10^{-3}$	$-84.1\ 10^{-3}$	$2.52\ 10^{-3}$
	S_{on}	41.6	1.75	$308\ 10^{-3}$	$60.7\ 10^{-3}$	$-923\ 10^{-6}$
	D_{off}	66.6	-2.54	$332\ 10^{-3}$	$95.4\ 10^{-3}$	$2.90\ 10^{-3}$
120°C	S_{off}	179	-1.31	$650\ 10^{-3}$	$-116\ 10^{-3}$	$3.48\ 10^{-3}$
	S_{on}	70.0	2.94	$518\ 10^{-3}$	$102\ 10^{-3}$	$-1.55\ 10^{-3}$
	D_{off}	97.9	-3.73	$488\ 10^{-3}$	$140\ 10^{-3}$	$4.27\ 10^{-3}$
Units		$nWs(VA)^{-1}$	$nWs(VA^2)^{-1}$	$nWs(V^2)^{-1}$	$nWs(V^2A)^{-1}$	$nWs(V^2A^2)^{-1}$

Used for analytical calculation

Analytical Loss Calculation

Conduction Losses – Model, Parameters



IGBT- On-State Parameter			
T_j		U_F	r
25°C	S	940	52.4
	D	1250	8.04
120°C	S	768	78.7
	D	732	38.0
Units		mV	mVA^{-1}

u corresponds to switched voltage of output stage devices

Conduction Losses (in general)

$$\frac{1}{T_P}\int_{T_P} dt$$

$$p_{Dev,C} = u_{Dev} \cdot i_{Dev} = (U_F + r \cdot i_{Dev}) \cdot i_{Dev} = U_F \cdot i_{Dev} + r \cdot i_{Dev}^2$$

$$\bar{p}_{Dev,C} = U_F \cdot \bar{i}_{Dev} + r \cdot i_{Dev,rms}^2$$

Local Conduction Losses in Sector II (exemplary of S_{pB})

$$\bar{p}_{SpB,C} = \underbrace{\left(\delta_{(110)} + \delta_{(010)}\right) \cdot i_B}_{\bar{i}_{SpB}} \cdot U_{FS,Inv} + \underbrace{\left(\delta_{(110)} + \delta_{(010)}\right) \cdot i_B^2}_{i_{SpB,rms}^2} \cdot r_{S,Inv}$$

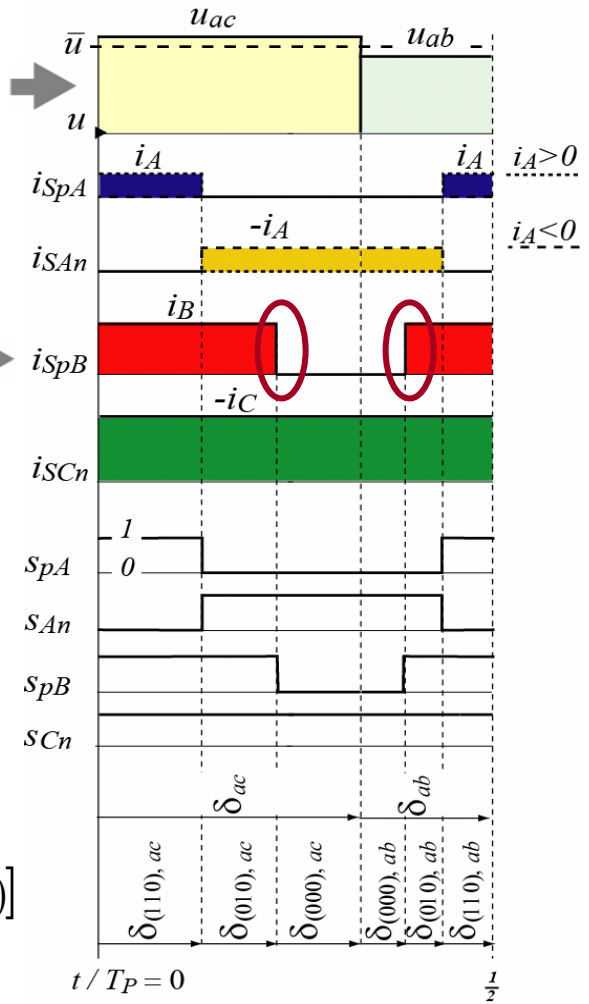
Local Switching Losses in Sector II (exemplary of S_{pB})

$$\bar{p}_{SpB,Sw} = f_P \cdot \left[w_{S,Off}(u_{ac}, i_B) + w_{S,On}(u_{ab}, i_B) + w_{S,Off}(u_{ab}, i_B) + w_{S,On}(u_{ac}, i_B)\right]$$

Local Total Losses in Sector II (exemplary of S_{pB})

$$p_{SpB} = \bar{p}_{SpB,Sw} + \bar{p}_{SpB,C}$$

Transistor Currents in Half Pulse Period of Sector II



$$\delta_{(110)} = \delta_{(110),ac} + \delta_{(110),ab}$$

$$\delta_{(010)} = \delta_{(010),ac} + \delta_{(010),ab}$$

Conduction Losses (Example for Inverter)

Operating Point 1
(Local Loss Maximum)

Equation

$$\overline{p}_{Dev,C,\max} = \frac{3}{16} M \ \hat{I}_2 \cdot \left(2\sqrt{3} \cdot U_{F,Dev} + r_{Dev} \cdot 3\hat{I}_2\right)$$

$$OP\,1 \Rightarrow M \approx 0$$

Transistor

$$M \rightarrow M \approx 0$$

$$\overline{p}_{S,Inv,C,\max} = 0$$

Diode

$$M \rightarrow \left(\frac{4}{3} - M\right) \approx \frac{4}{3}$$

$$\overline{p}_{Dev,C,\max} = \frac{1}{4} \hat{I}_2 \cdot \left(2\sqrt{3} \cdot U_{F,Dev} + r_{Dev} \cdot 3\hat{I}_2\right)$$

Operating Point 2
(Global Loss Average)

Equation

$$P_{Dev,C} =$$

$$= \hat{I}_2 \left(U_{F,Dev} \frac{4 + 2\sqrt{3} M \cos\Phi_2}{8\pi} + r_{Dev} \frac{3\pi^2 + 16\sqrt{3} M \cos\Phi_2}{24\pi^2} \hat{I}_2 \right)$$

$$OP\,2 \Rightarrow M_2 = 1$$

Transistor

$$M_2 \rightarrow M_2 = 1$$

Diode

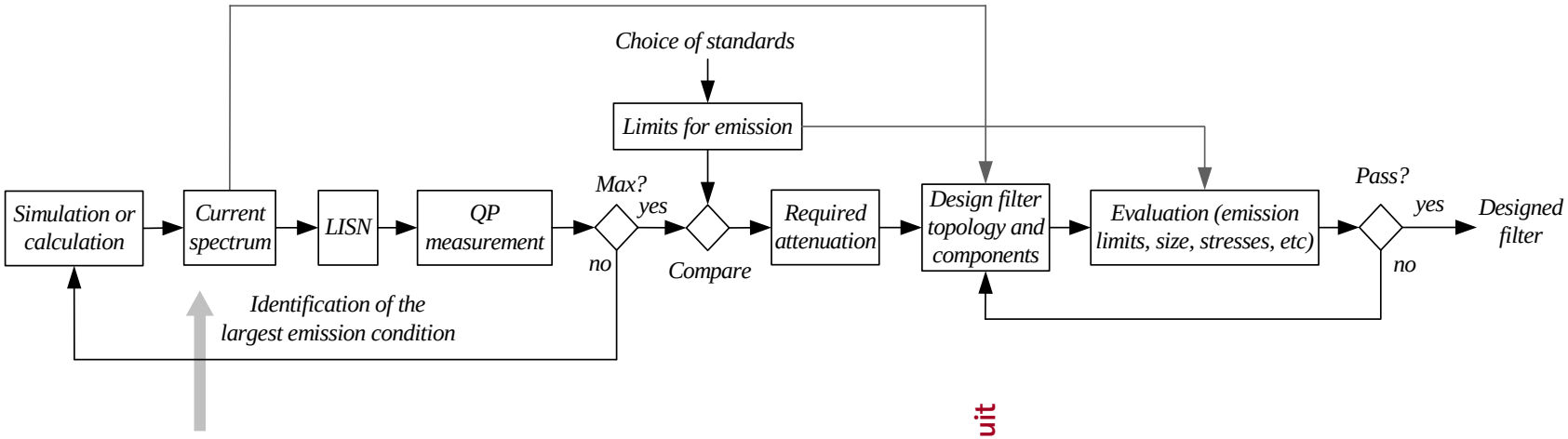
$$M_2 \rightarrow -M_2 = -1$$

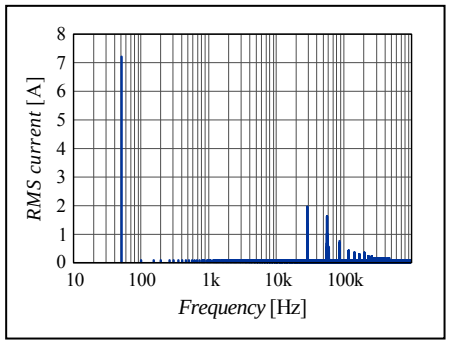
Total Inverter Stage ($P_{Inv,C}$):

$$P_{Inv,C} = 6 \cdot (P_{S.Inv,C} + P_{D.Inv,C})$$

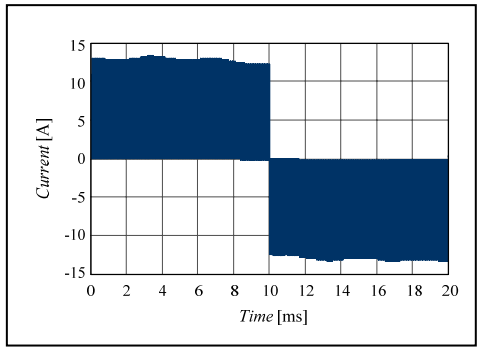
EMI Input Filter Design

Filter Design Procedure

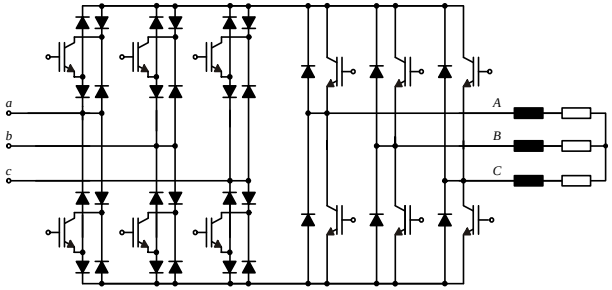




FFT calculation



Electric circuit simulation



Input current spectrum

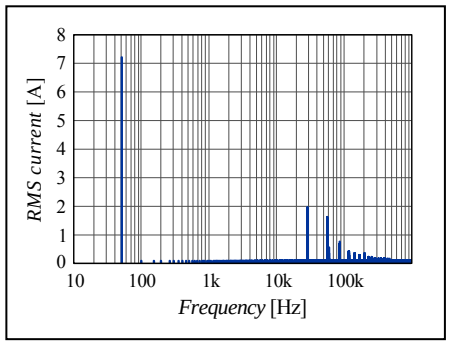
Input current

VSMC

EMI Input Filter Design

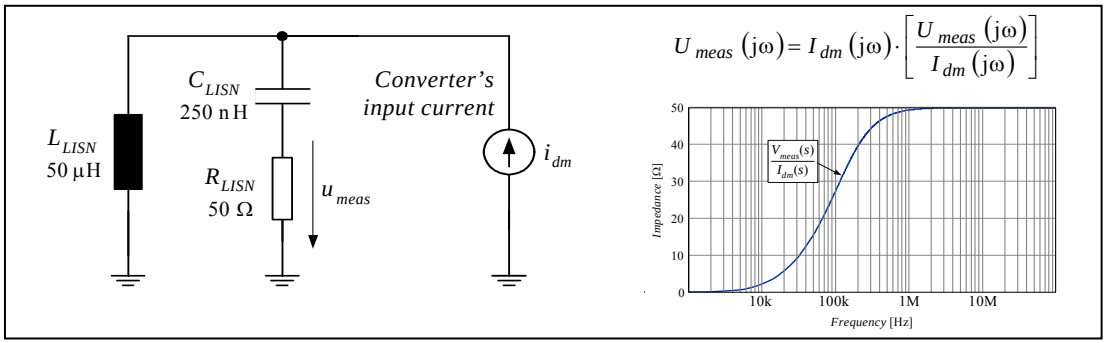
Modeled Spectral Measurement (Chain 01)

Input current spectrum

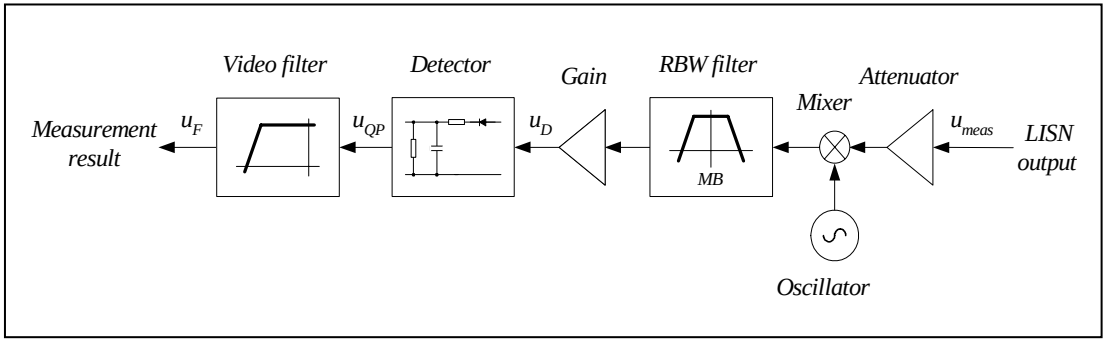


Calculation in frequency domain

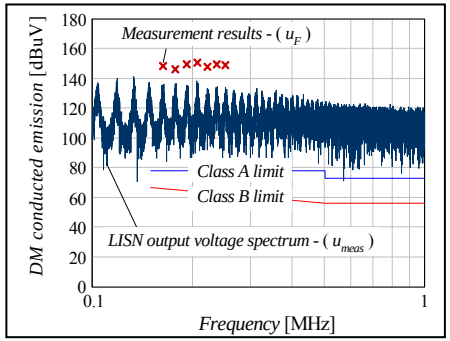
LISN simplified high frequency model



Calculations in frequency and time domains



Spectral measurement modeled chain

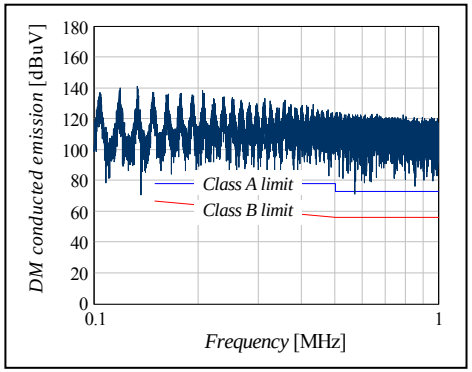


Measurement values

EMI Input Filter Design

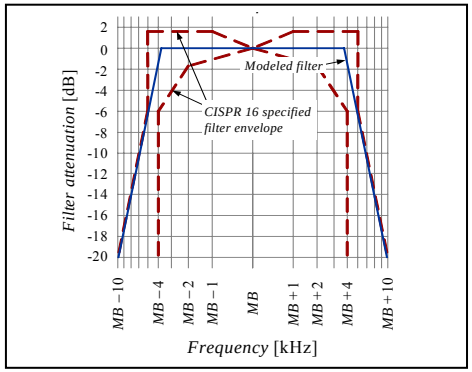
Modeled Spectral Measurement (Chain 02)

LISN output voltage spectrum

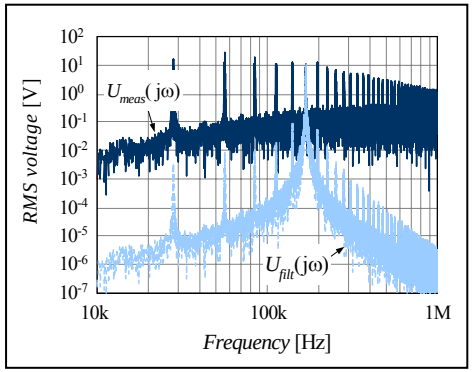


Calculation in frequency domain

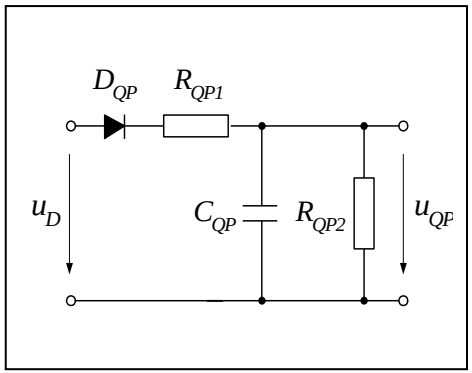
RBW filter



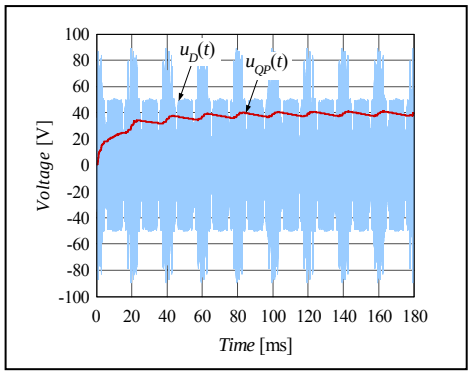
Effect of the RBW filtering



Calculations in time domain

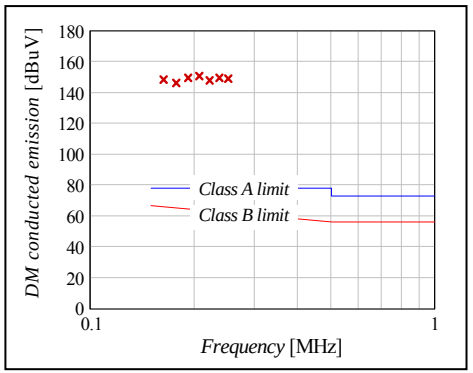


Quasi-Peak detector



Effect of the QP detector

Averaging of the QP output voltage

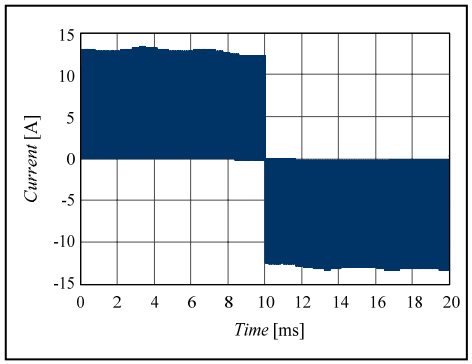


Averaged values

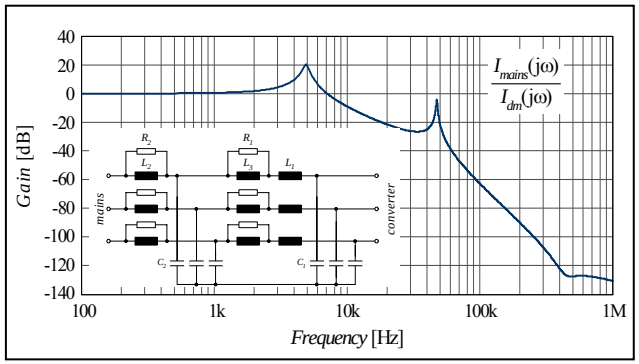
EMI Input Filter Design

Three-phase Filter (Topology and Function) and Final Result

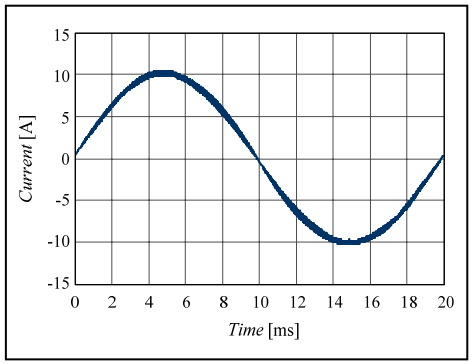
VSMC input current

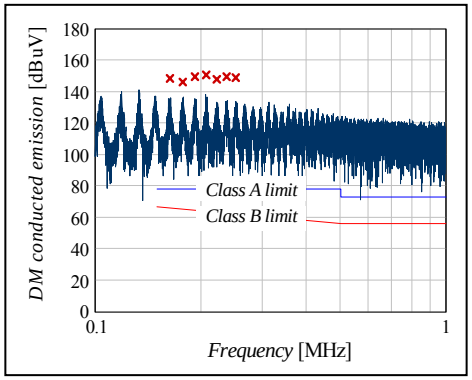


Designed three-phase filter

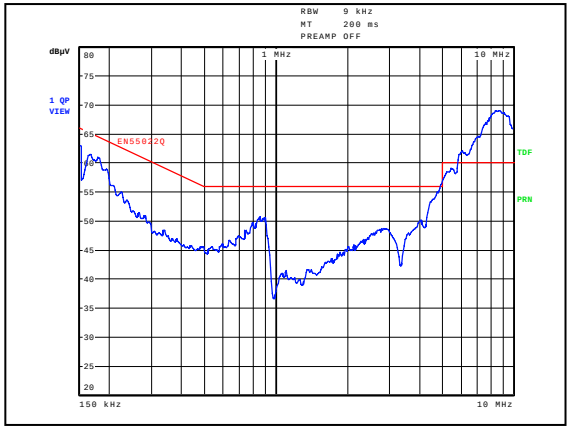


Input filtered current

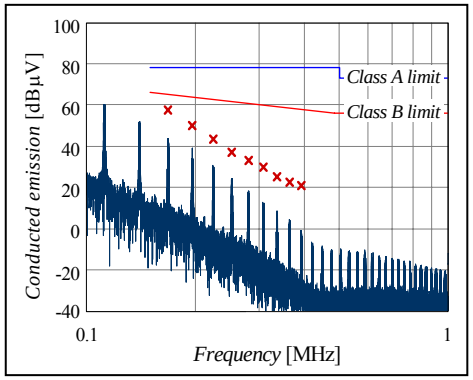




Measurement without filter



Experimental result (DM conducted emission)



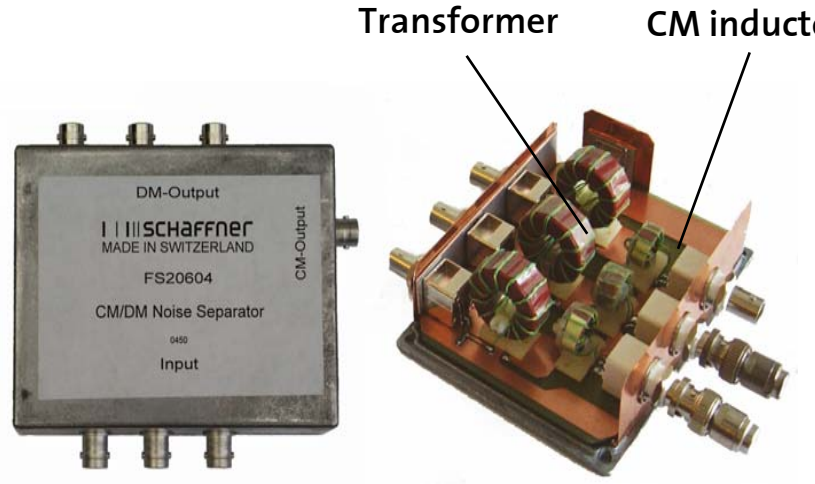
Final measurement

EMI Input Filter Design

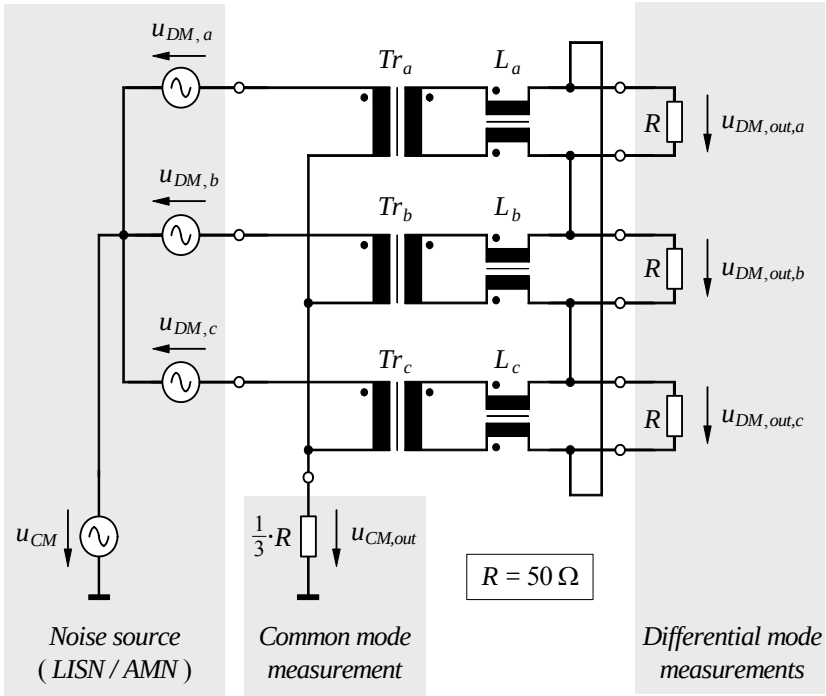
Three-phase CM / DM Noise Separator

Function

Enables separate measurement of DM and CM noise in order to properly evaluate the performance of the designed filters



Basic Noise Separator Schematic



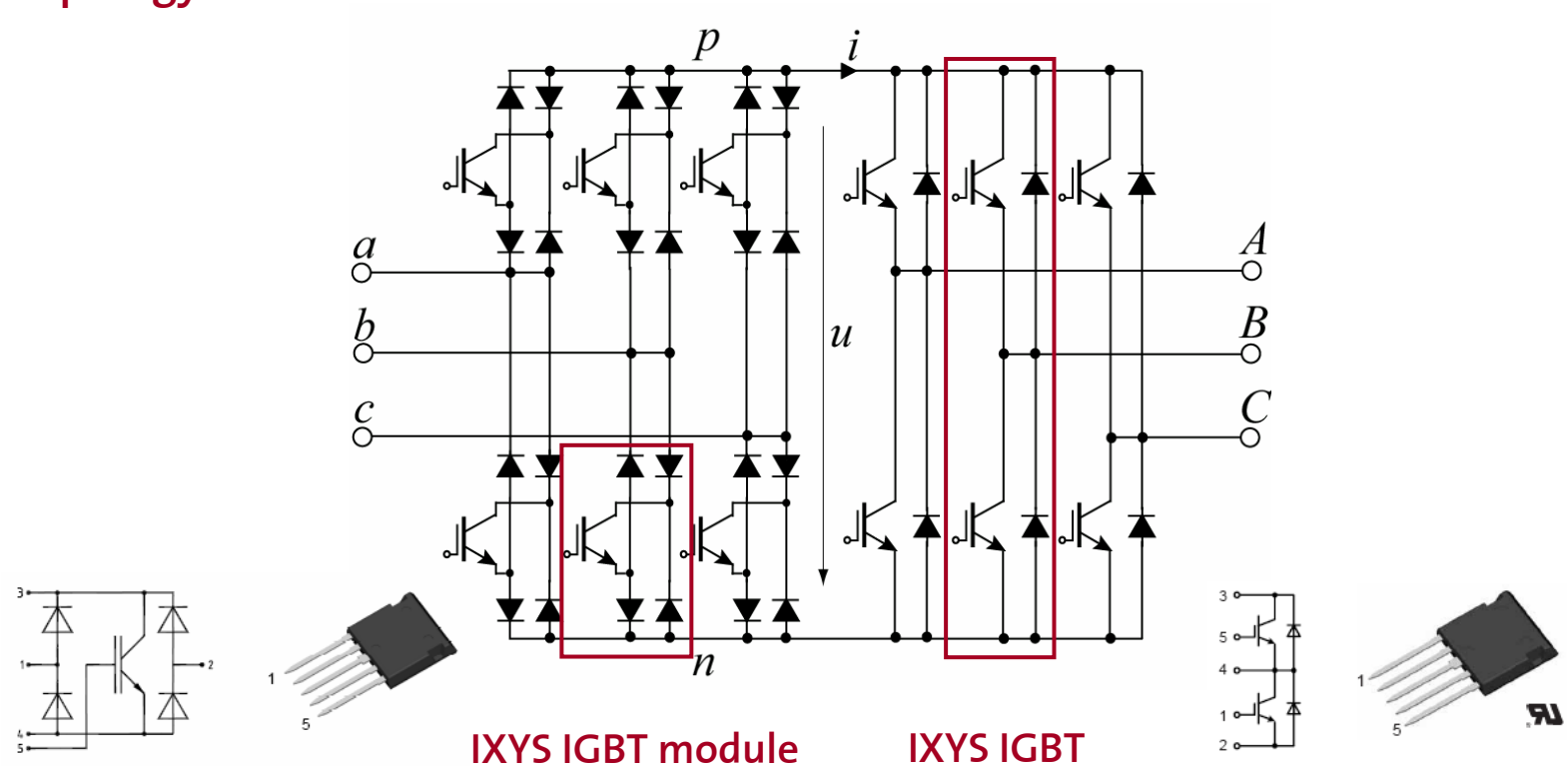
Dimensions: 12.0 x 9.5 x 5.7 cm (4.75 x 3.75 x 2.25 in.)

Hardware Prototypes

Experimental Results

Very Sparse Matrix Converter

Topology and Power Semiconductors



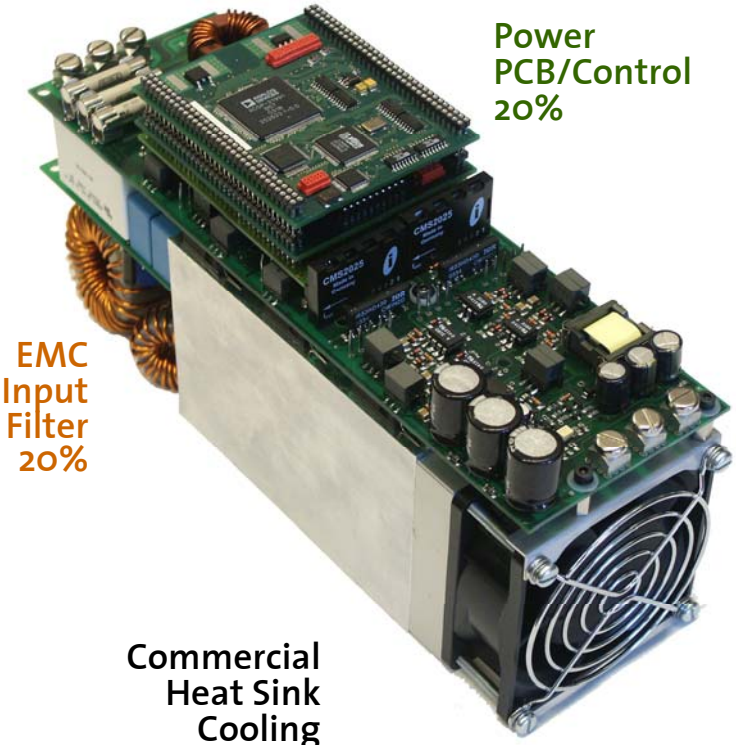
IXYS IGBT module
FIO 50-12BD
1200 V, 50 A

IXYS IGBT
FII 50-12E
1200 V, 50 A

Bidirectional power flow

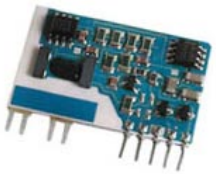
Very Sparse Matrix Converter

Hardware Construction



Input RMS voltage	230 V
Output power	6.8 kVA
Rectifier switching frequency	12.5 kHz
Inverter switching frequency	25 kHz

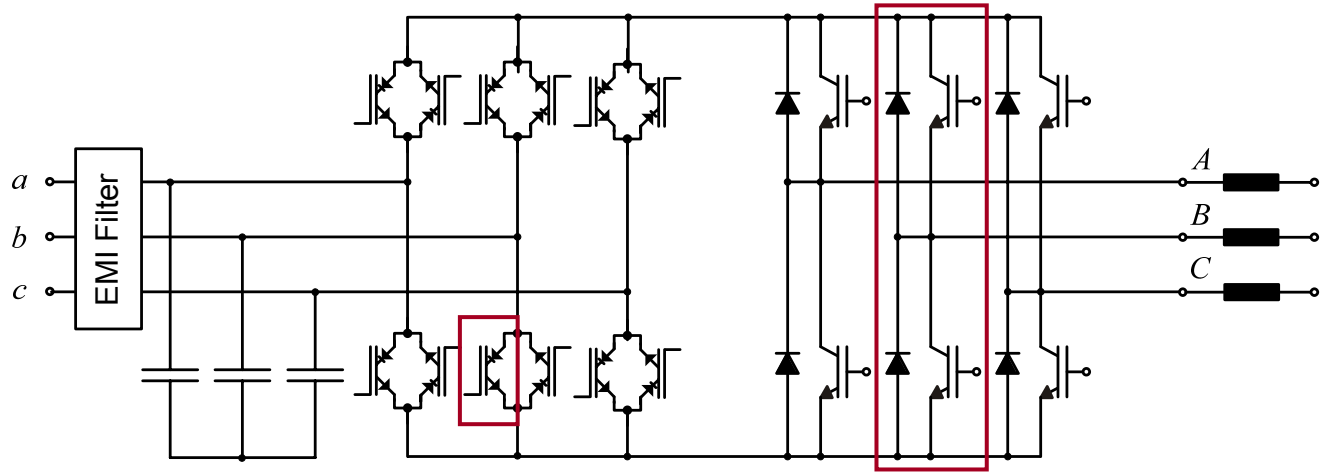
Power density	2.8 kW/dm³
	46 W/in³
Efficiency	94.5%



Magneto resistive output current sensors from Sensitec

RB-IGBT Indirect Matrix Converter

Topology and Power Semiconductors



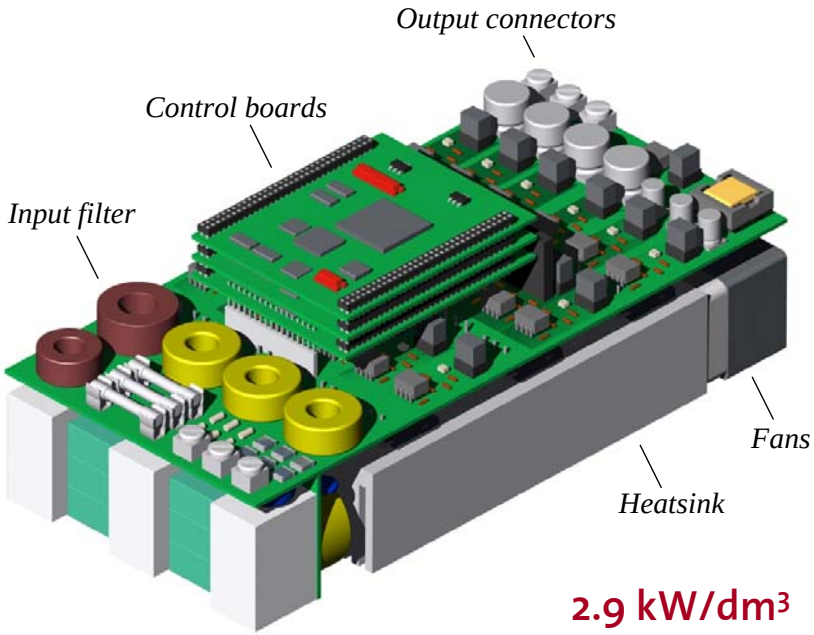
IXYS RB-IGBT
IXRH40N120
1200 V, 40 A

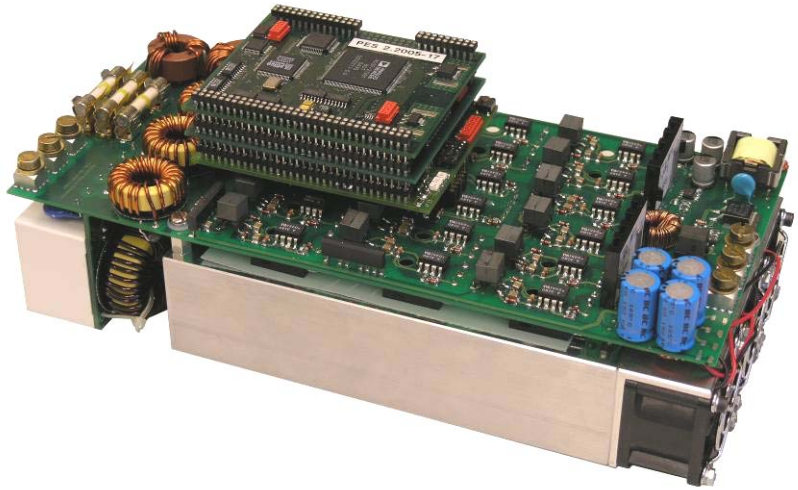
IXYS bridge-leg
FII50-12E
1200 V, 50 A

Bidirectional power flow

RB-IGBT Indirect Matrix Converter

Hardware Construction





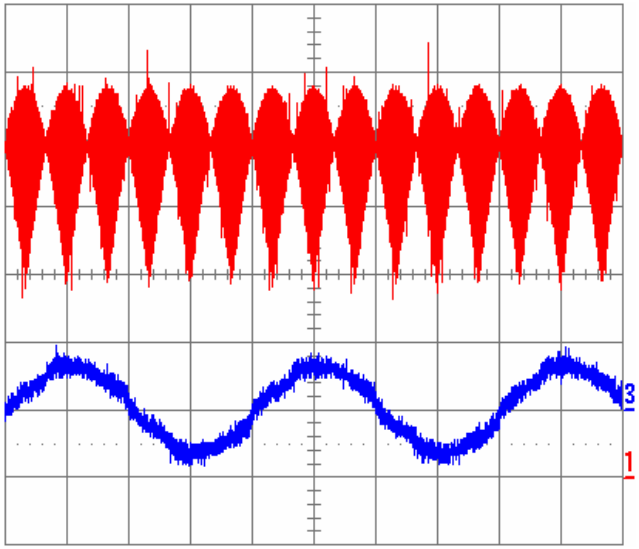
2.9 kW/dm³
48 W/in³

Efficiency: 95.5%

Input RMS voltage	230 V
Output power	6.8 kVA
Rectifier switching frequency	12.5 kHz
Inverter switching frequency	25 kHz

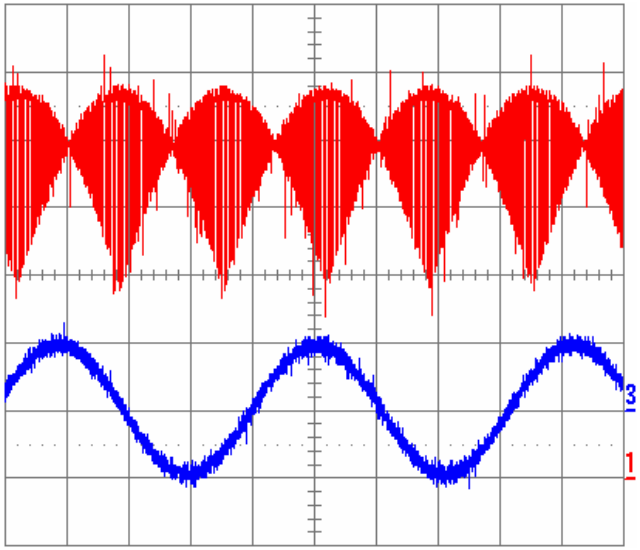
RB-IGBT Indirect Matrix Converter

Measurement Results



DC link voltage 100 V/div

Input current 5 A/div



DC link voltage 100 V/div

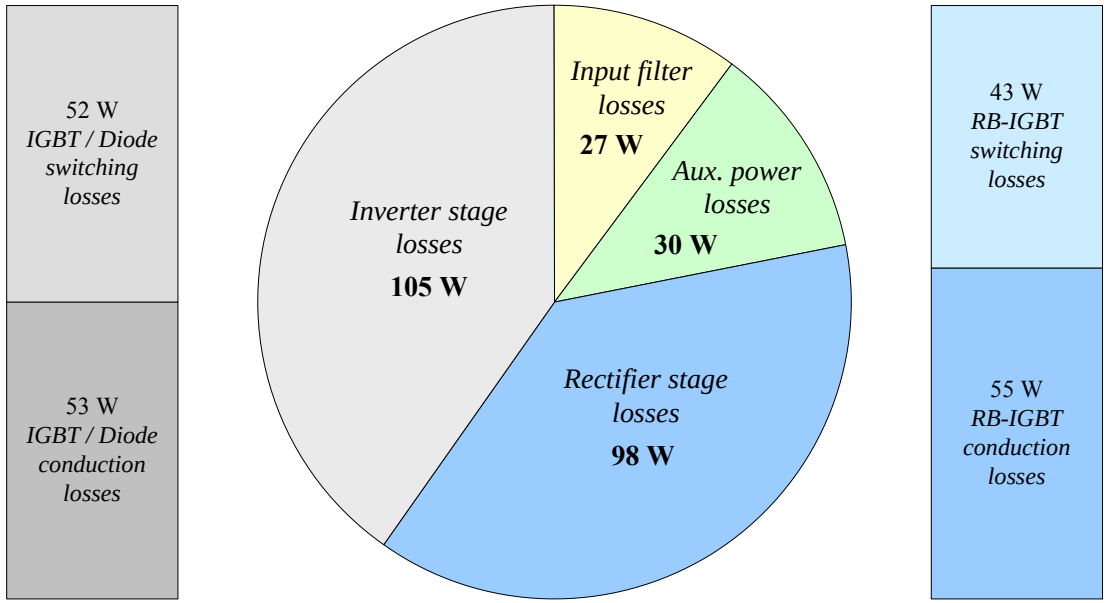
Output current 5 A/div

Operating point: U_1 = 230 V, P_{out} = 1.5 kW, f_{out} = 120 Hz

Measured efficiency: $\eta \approx 95\ \%$

RB-IGBT Indirect Matrix Converter

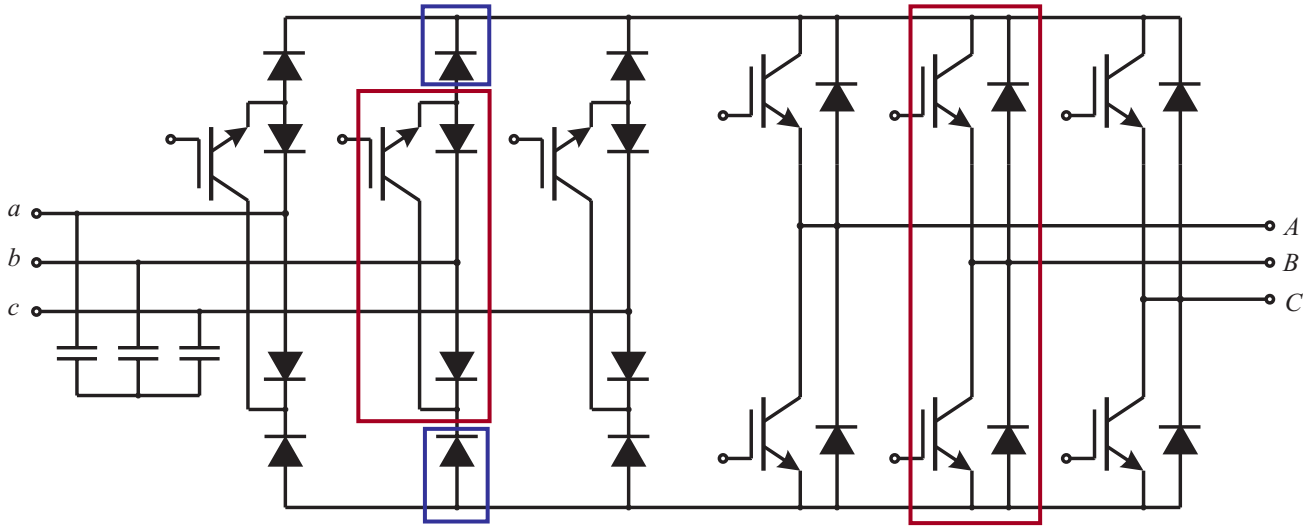
Overall Losses



Calculated losses distribution at the maximum output power of 6.8 kVA, U_1 = 230 V, $M = M_{max}$, and Φ_2 = 0°; shown for T_j = 25°C

Ultra Sparse Matrix Converter

Topology and Power Semiconductors



IXYS IGBT module
FIO 50-12BD
1200 V, 50 A

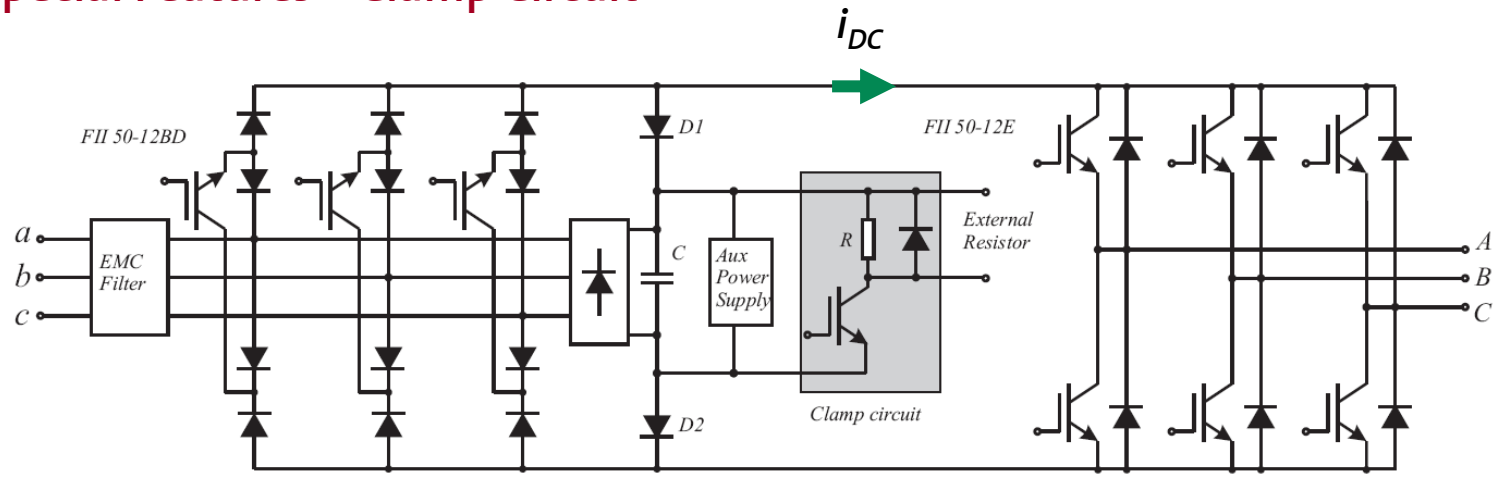
IXYS diode
DSEP 60-12AR
1200 V, 60 A

IXYS bridge-leg
FII 50-12E
1200 V, 50 A

Unidirectional power flow

Ultra Sparse Matrix Converter

Special Features – Clamp Circuit



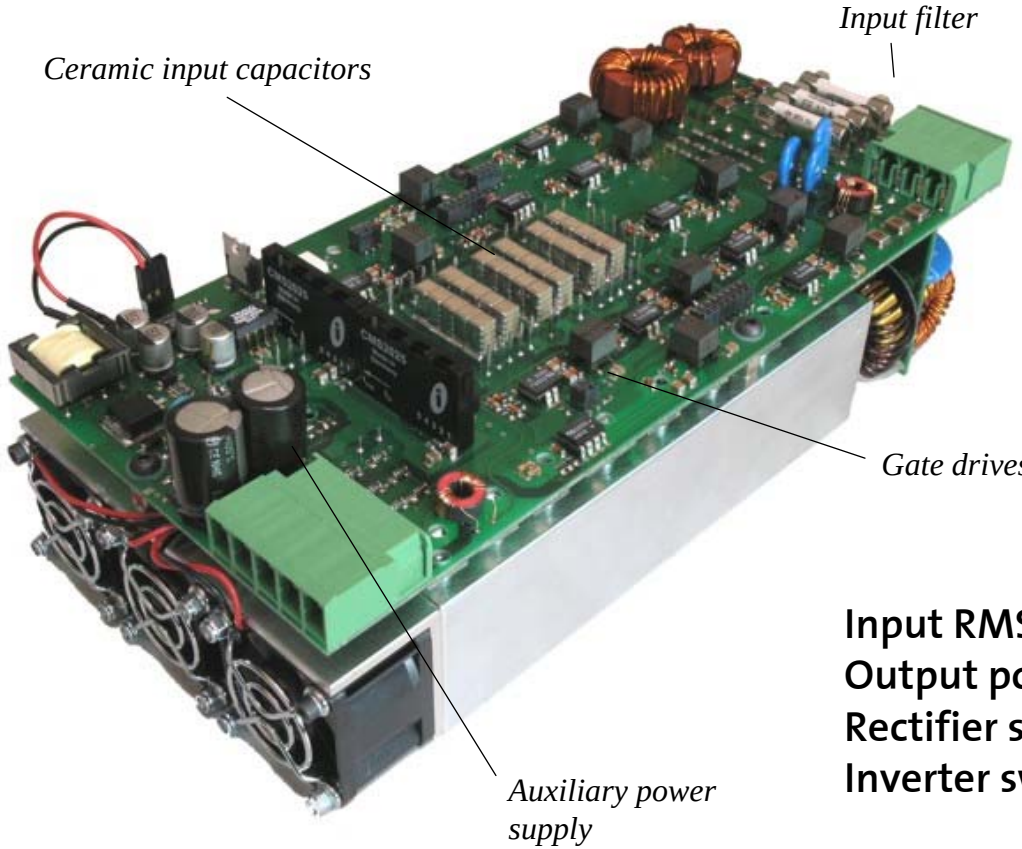
- Auxiliary power supply connected to DC link
- Clamping circuit with resistor combination to dissipate the energy of a load machine in braking mode

Output displacement angle: $\Phi_2 \in (-\frac{\pi}{6}, +\frac{\pi}{6})$ $i_{DC} > 0$

$\Phi_2 \notin (-\frac{\pi}{6}, +\frac{\pi}{6})$ $i_{DC} < 0 \rightarrow$ Clamp activation

RB-IGBT Indirect Matrix Converter

Hardware Construction

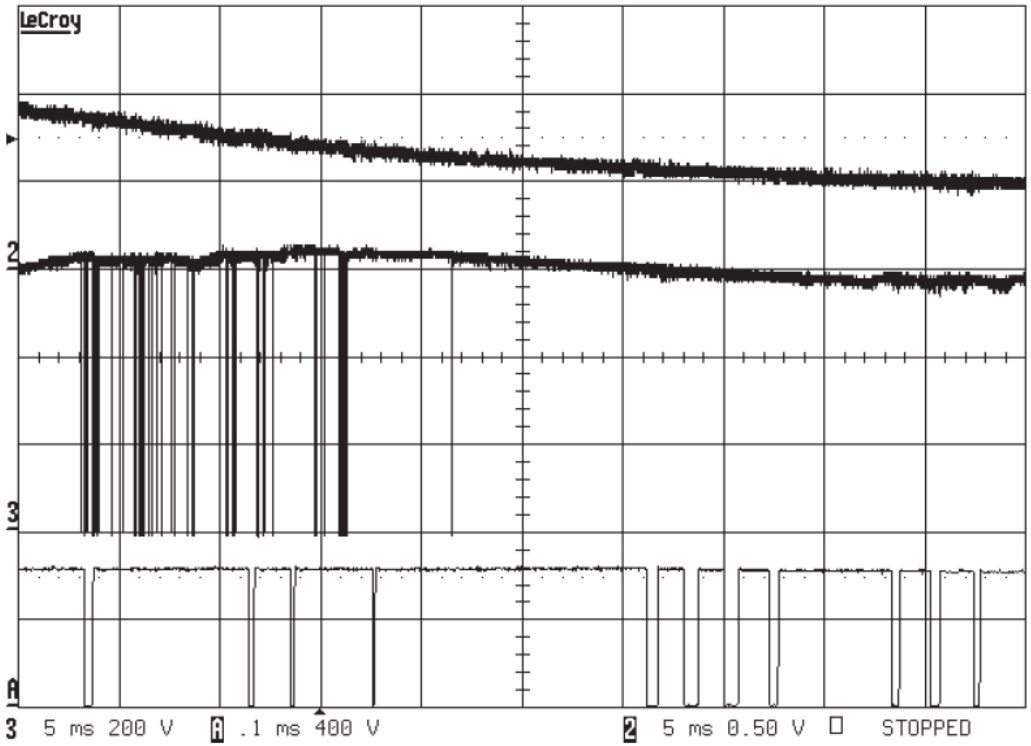


- Si USMC
- Si / SiC USMC
  SiC free-wheeling diodes in inverter stage

Input RMS voltage	230 V
Output power	5.5 kVA
Rectifier switching frequency	25 (37.5) kHz
Inverter switching frequency	50 (75) kHz

Ultra Sparse Matrix Converter

Measurement Results Showing Clamp Operation

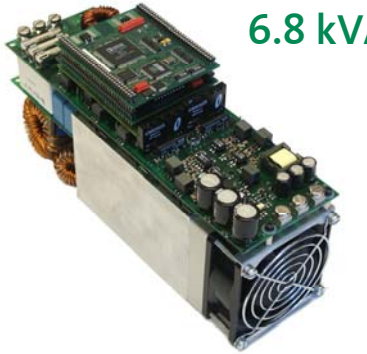


Motor speed
500 rpm/div

Voltage across
the clamp switch
200 V/div

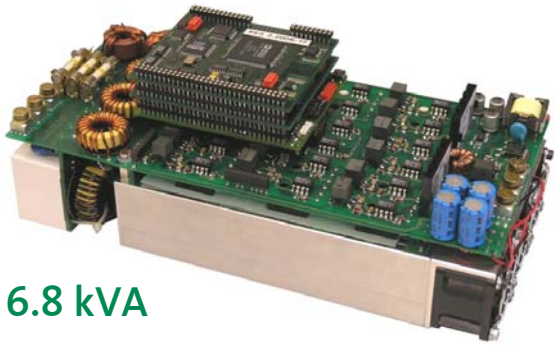
Zoomed voltage across
the clamp switch
400 V/div

Overview of Hardware Prototypes



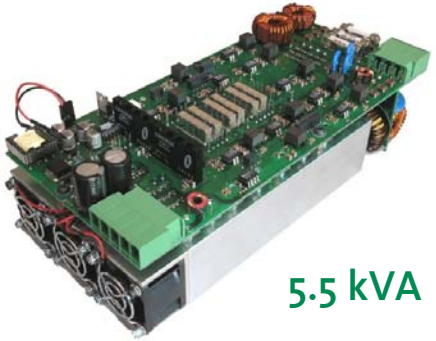
6.8 kVA

Si IGBT VSMC



6.8 kVA

Si RB-IGBT IMC

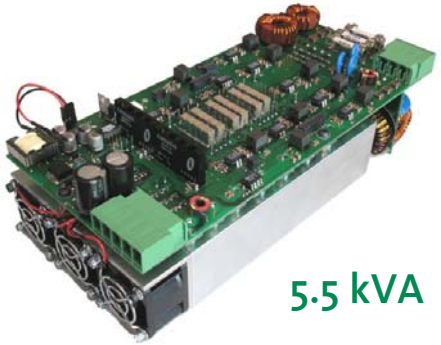


5.5 kVA

Si IGBT USMC

1.5 kVA

Si MOSFET SiC JFET
Cascode SMC



5.5 kVA

Si IGBT USMC with
SiC output stage diodes

Comparison of Back-to-Back Voltage DC-Link Converter and Indirect Matrix Converter

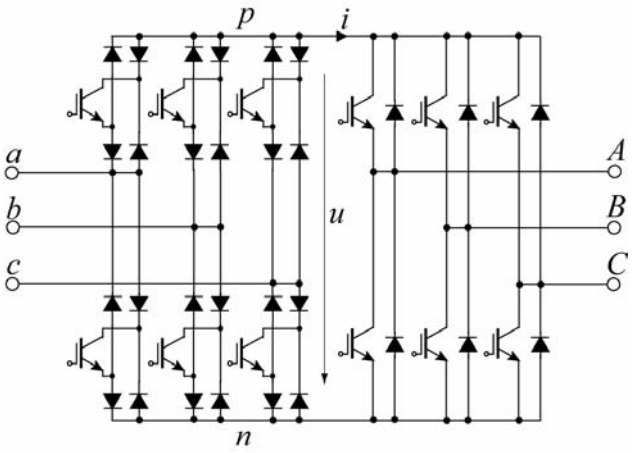
Criteria for Comparison

- **Comparison of the Realization Effort**
  Assumptions, design and losses
- **Losses and Efficiency dependent on Operating Point**
  Theoretical limits
- **Power Density**
  Physical layout, dimensions and power density
- **EMI Filtering Effort**
  Design procedure, components, structure and volume

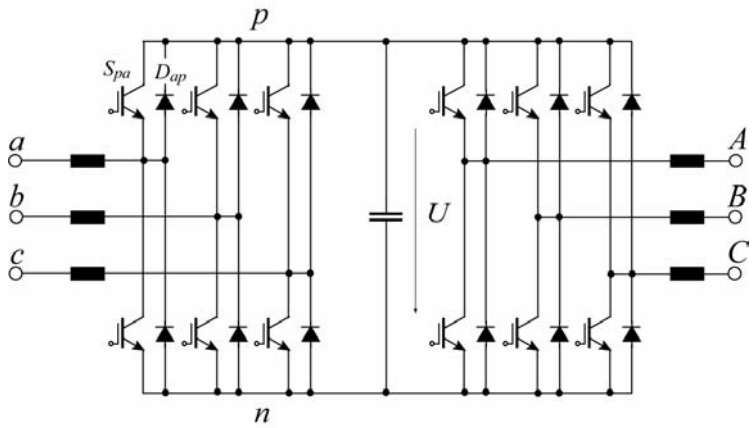
Comparison of Realization Effort

Specifications

Input (3~AC)	400 V, +10%, -15%, 50 Hz
Output (3~AC)	S_2 = 6.8 kVA at T_{amb} = 45°C
Switching frequency	*SMC*: Input f_p = 20 kHz / Output f_p = 40 kHz *BBC*: Input f_p = 40 kHz / Output f_p = 40 kHz
Dynamic Modulation Margin	ΔM_{min} = 5%
Load	PM Synchronous Motor (PMSM)



Very Sparse Matrix Converter



Back-To-Back Converter

Comparison of Realization Effort

Assumption for comparison:

Ideally designed motors for each of the topologies

VSMC

$$U_{2,N} = \frac{\sqrt{3}}{2}(1-\Delta M_{\min})\cdot U_{1,\min} = 280V$$

$$I_{2,N} = \frac{P_{2N}}{\sqrt{3}\cdot U_{2,N}} = 14A$$

BBC

$$U_{dc} = (1+\Delta M_{\min})\cdot\sqrt{2}\cdot U_{1,\max} \approx 655V$$

$$U_{2,N} = (1-\Delta M_{\min})\cdot\frac{1}{\sqrt{2}}U_{dc} = U_{1,\max} = 440V$$

$$I_{2,N} = 8.9A$$

U_1 : Input RMS voltage
U_2 : Output RMS voltage
U_{dc} : DC-link voltage
I_1 : Input RMS current
I_2 : Output RMS current
P_2 : Output power

Comparison of Realization Effort

Choice of DC-link Capacitor for the BBC

$$C_{DC-link,\min} = \frac{L_{in} \cdot P_2^2 \left[\left(E_{dc} - U_{dc}\right)^2 - \left(E_{dc} + U_{dc}\right)^2 \right]}{E_{dc}^2 \cdot U_{dc}^2 \left(\left(\min(u_{dc}) + E_{dc}\right)^2 - \left(U_{dc} + E_{dc}\right)^2 \right)}$$

E_{dc} : Peak input voltage
U_{dc} : DC-link voltage
L_{in} : Boost inductor
U_1 : Input RMS voltage
$i_{1,ripple}$: Input current ripple, peak-to-peak

$$C_{DC-link,\min} \cong 31\mu F$$

Capacitor is selected such that the voltage does not fall below a defined minimum value during the transient from full regeneration to full motor operation

Choice of Boost Inductors for the BBC

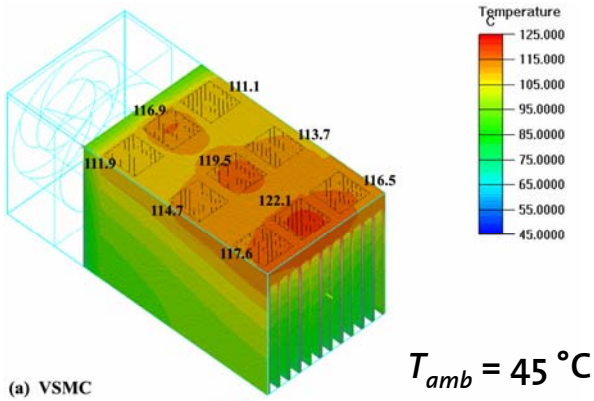
$$L_{in,\min} = \frac{U_1 / \sqrt{3}}{2 \cdot \sqrt{6} \cdot f_P \cdot i_{1,ripple}}$$

$$L_{in,\min} \cong 1mH$$

Inductors are chosen such that the current ripple at the switching frequency is lower than 20% of the input current amplitude (minimum EMI filter volume)

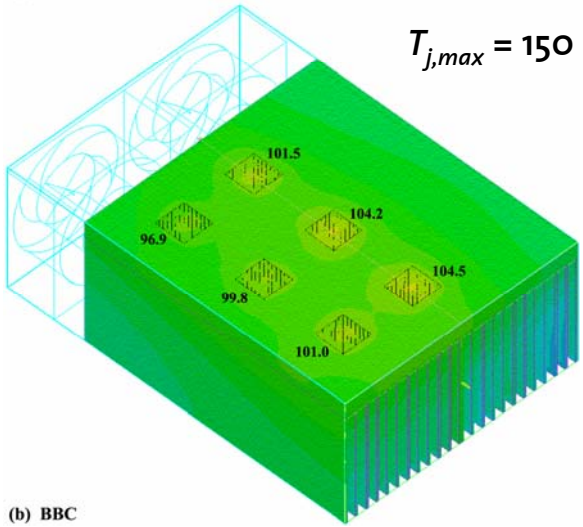
Comparison of Realization Effort

Thermal Simulation and Main Components



T_{amb} = 45 °C

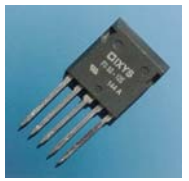
$T_{j,max}$ = 150 °C



Description	BBC		Very Sparse Matrix	
Semiconductors Input	3	IXYS FII 50-12E	6	IXYS FIO 50-12BD
Semiconductors Output	3	IXYS FIO 50-12E	3	IXYS FII 50-12E
Boost Inductors	3	1 mH (toroidal)		Not used
DC-Link Capacitors	4	8 µF, foil, 400 V_{AC}		Not used

BBC requires larger heat sink due to lower efficiency

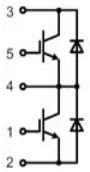
IXYS FIO 50-12E

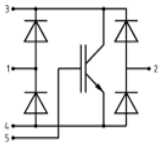


IXYS FIO 50-12BD

$R_{th,diodes}$ = 1.3 °C/W

$R_{th,IGBTs}$ = 0.6 °C/W

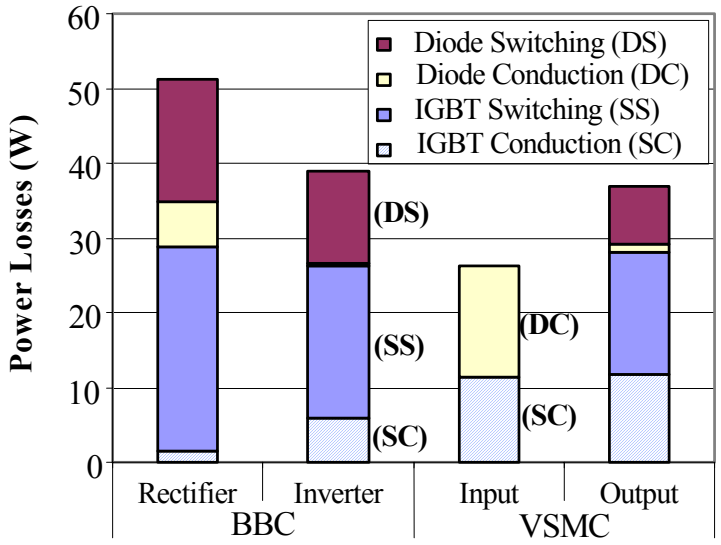




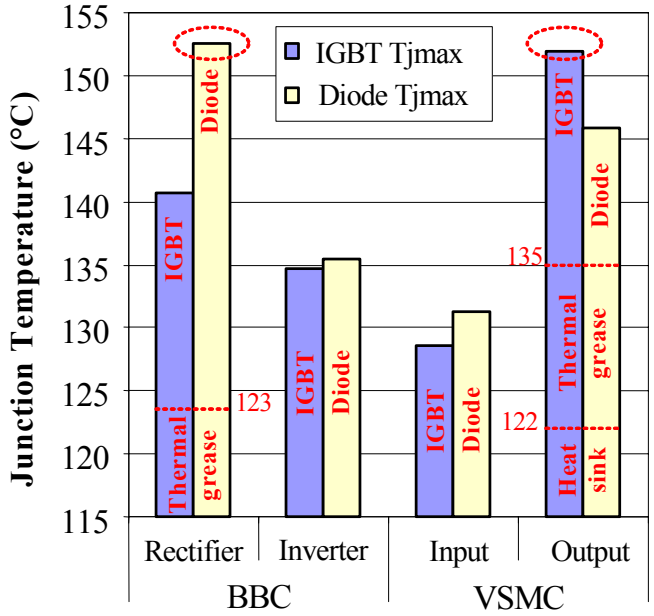
Comparison of Realization Effort

Losses and Thermal Limits – Comparison at Nominal Conditions

Losses Distribution



Junction Temperature



VSMC: No switching losses in input stage

BBC: Switching losses in both stages

Limiting device VSMC: Output IGBT

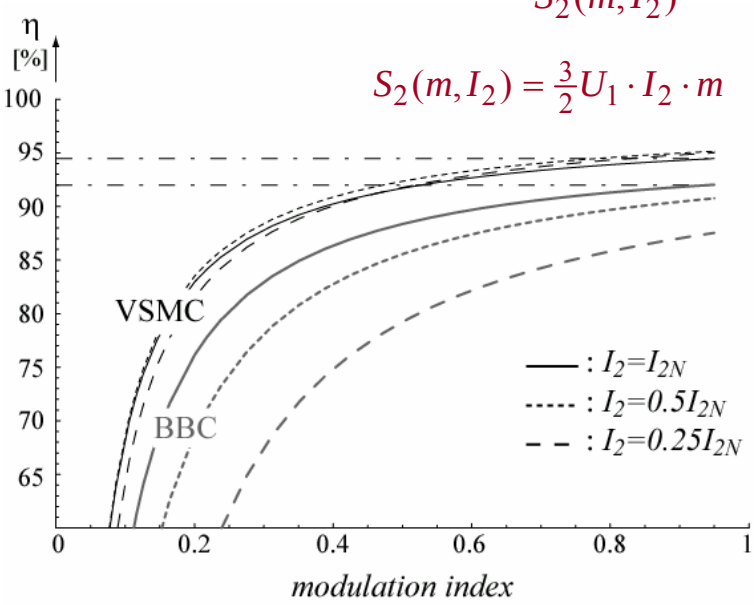
Limiting device BBC: Rectifier diode

Losses and Efficiency dependent on Operating Point

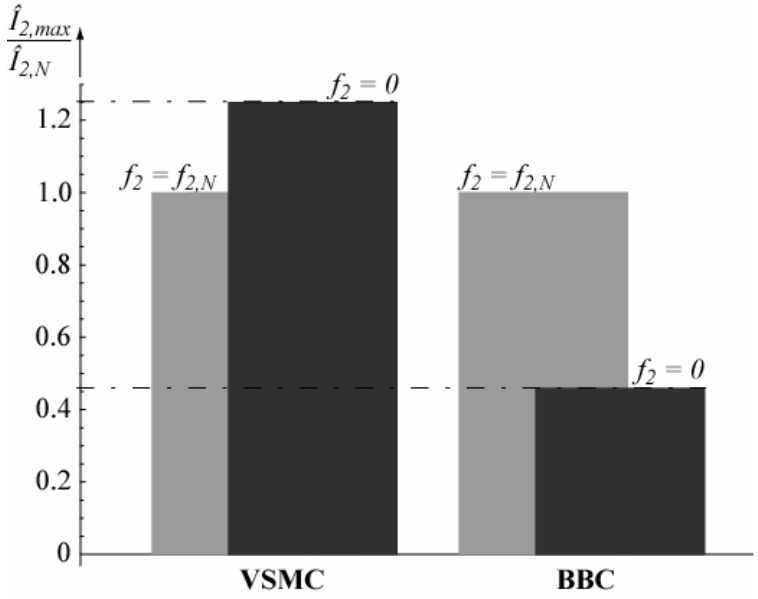
Efficiency

$$\eta = 1 - \frac{P_{Loss}(m, I_2)}{S_2(m, I_2)}$$

$$S_2(m, I_2) = \frac{3}{2} U_1 \cdot I_2 \cdot m$$



Max. Output Current for f_2 = 0 (Standstill: Most Critical OP)



Max. Efficiency at Max. Modulation Index

VSMC: 94.5%

BBC: 92.0%

Max. Output Current Amplitude

VSMC: 1.25 $\hat{I}_{2,N}$ (due to special modulation)

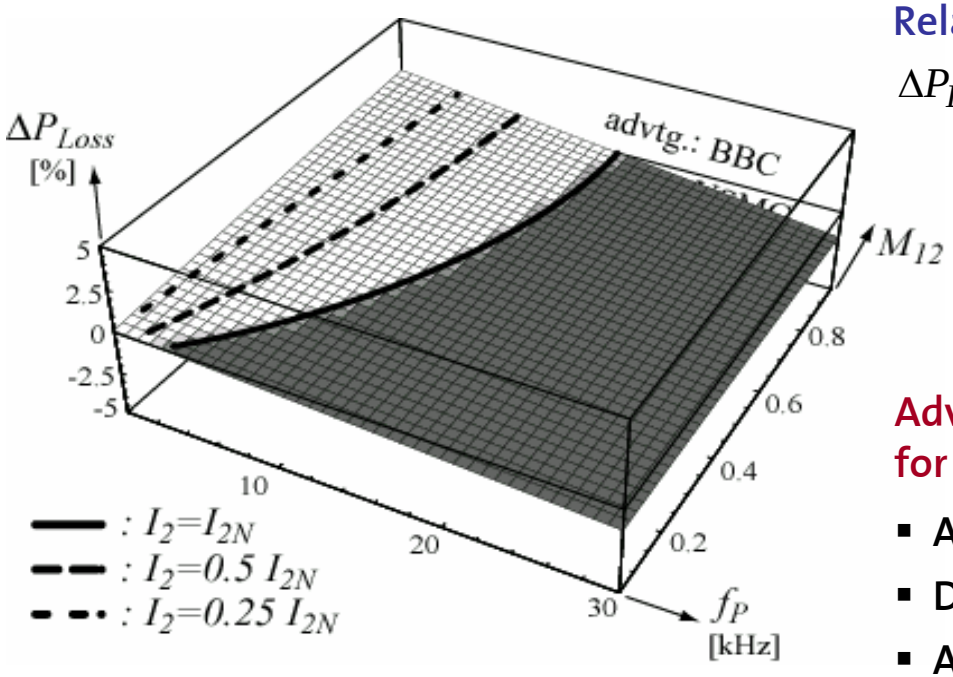
BBC: 0.46 $\hat{I}_{2,N}$

Losses and Efficiency dependent on Operating Point

Relative Loss Difference – Dependence on Load and Switching Frequency

Under rated load condition the critical f_p is about 14 kHz

→ VSMC is advantageous in efficiency within whole speed-torque plane beyond 14 kHz



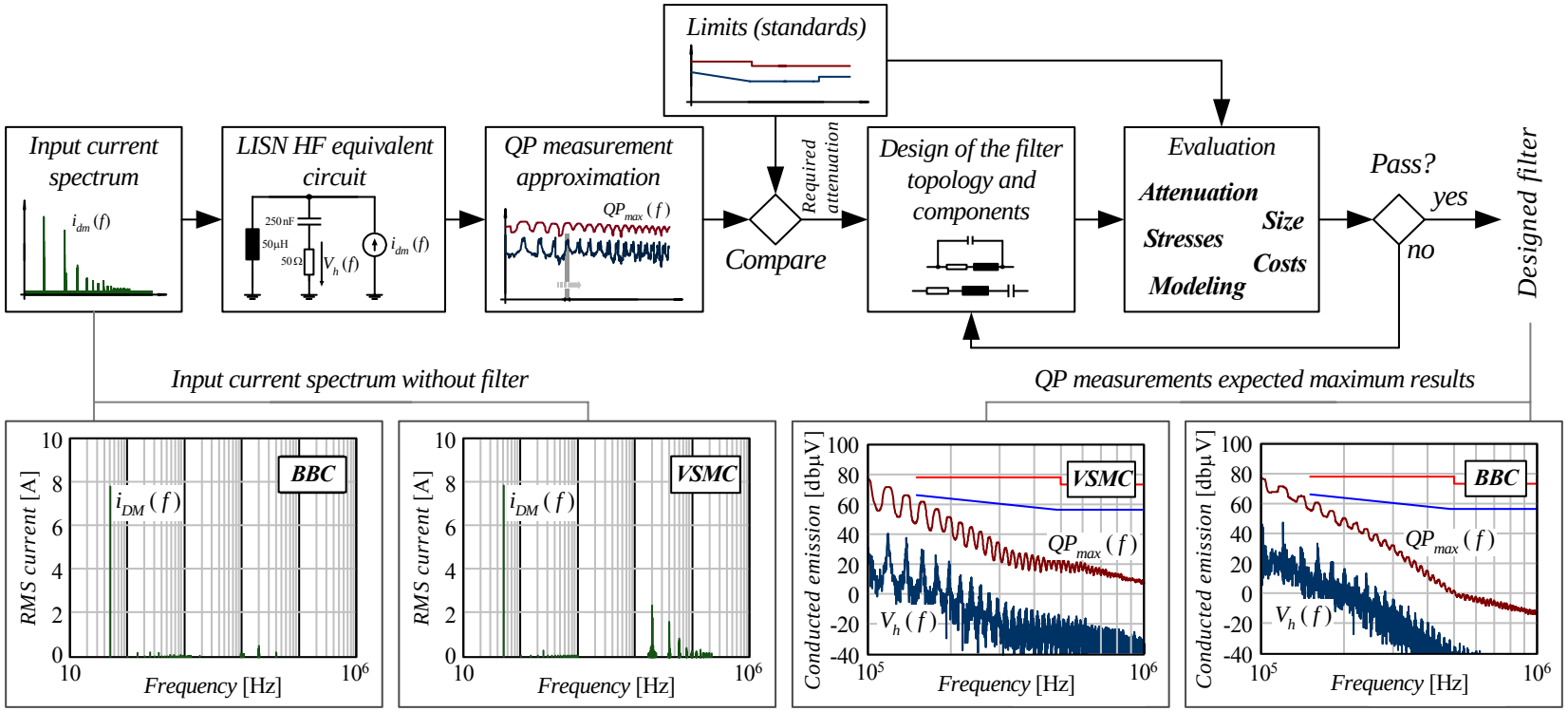
Relative Loss Difference

$$\Delta P_{Loss} = (P_{Loss,VSMC} - P_{Loss,BBC}) / P_{2N}$$

Advantageous Applications for VSMC (IMC)

- Applications requiring an output filter
- Drives operated at partial load
- Aircraft applications (400 – 800 Hz)
- Low inductance machines

EMI Filtering Effort



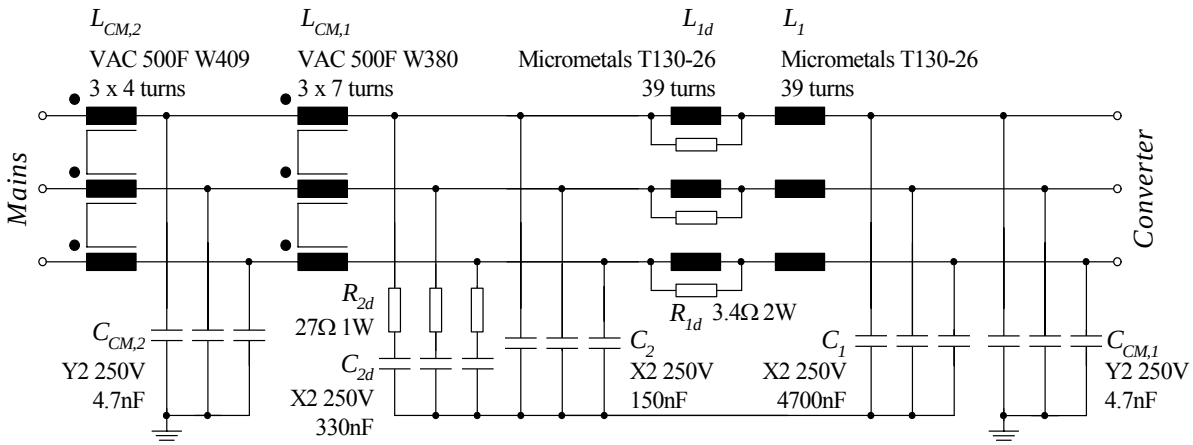
EMI Filtering Effort

Comparison

	Back-to-back	VSMC
Total DM capacitance (for all three-phases)	15.54 mF	36 mF
Total DM inductance (10 kHz)	1.20 mH	1.29 mH
Total CM capacitance	28.2 nF	28.2 nF
Total CM inductance (10 kHz)	36 mH	36 mH
Total filter components volume	325 cm^3	360 cm^3

Filter volume for the VSMC is 10% larger

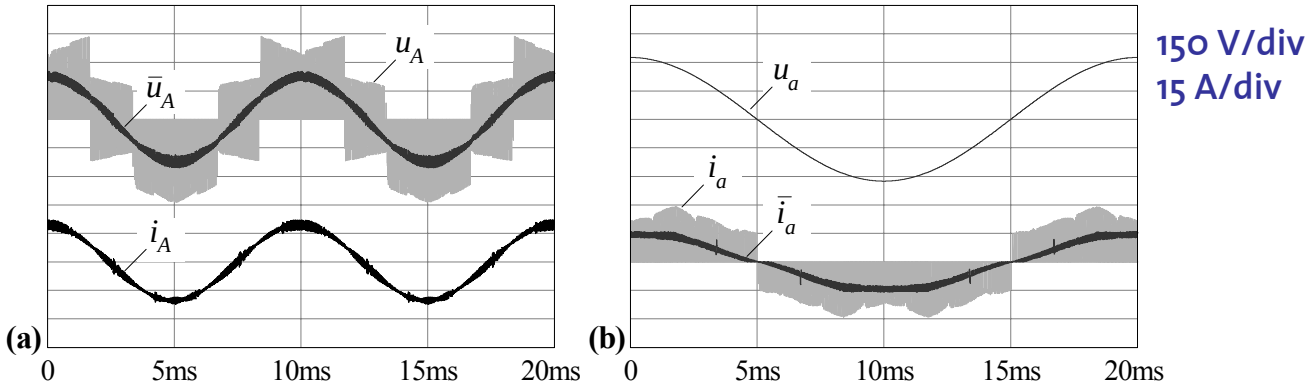
Filter Structure for the BBC



Characteristic Waveforms

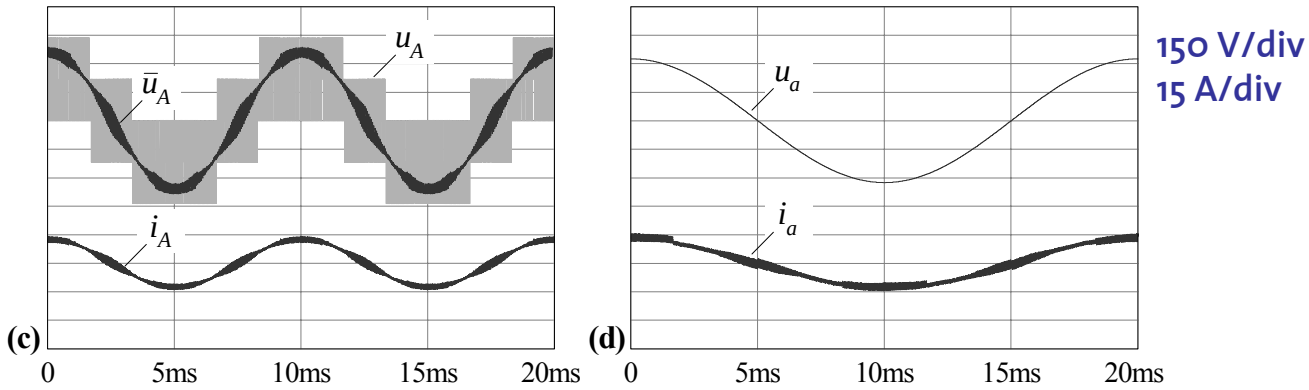
Nominal Operation (6.8 kW)

VSMC



150 V/div
15 A/div

BBC

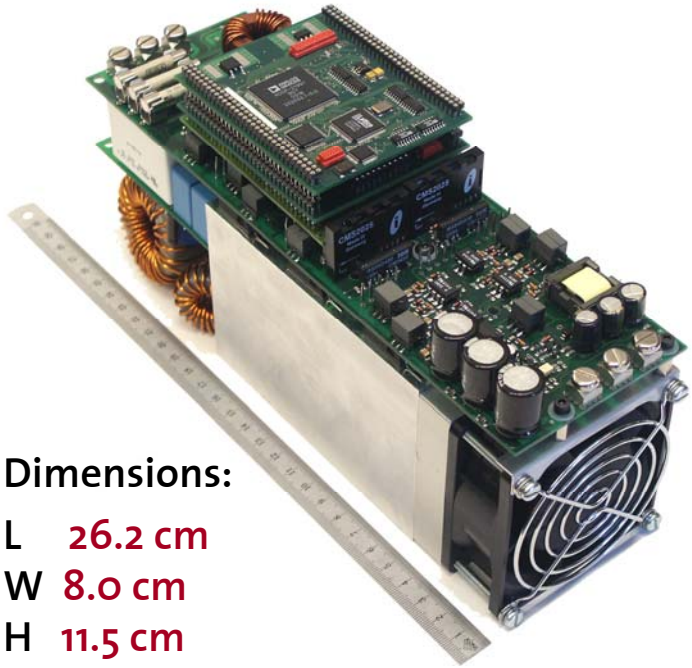


150 V/div
15 A/div

BBC Features:
- Constant DC link voltage at higher level (boost capability)
- Lower output currents due to higher output voltage level

Power Density

VSMC



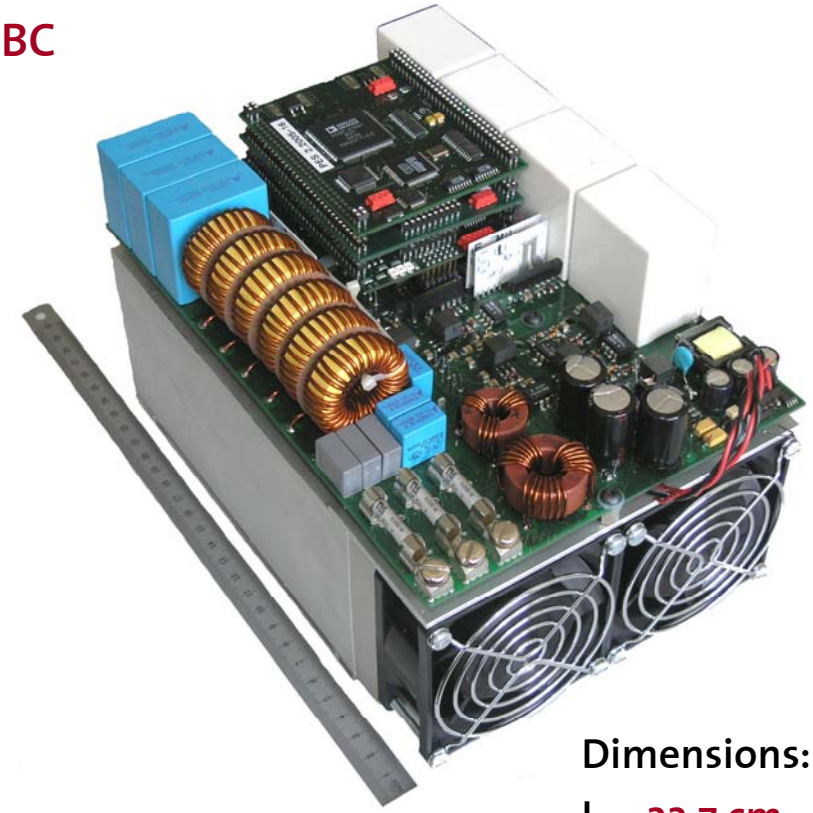
Dimensions:

L 26.2 cm
W 8.0 cm
H 11.5 cm

Volume: 2.4 liters
Power density:

≈ 2.8 kVA/liter
≈ 46 W/in³

BBC



Volume: 4.6 liters
Power density:

≈ 1.5 kVA/liter
≈ 25 W/in³

Dimensions:

L 22.7 cm
W 16.0 cm
H 13.4 cm

Conclusions

CMC and IMC / SMC proven to be competitive to BBC / Voltage DC Link System

+ Efficiency:	Typically 1-2% higher dependent on operating point for same semiconductor effort (especially, lower switching losses at high switching frequencies)
+ Volume:	Typically 20% lower for forced air cooling
o Modulation:	Comparable complexity of modulation and control, USMC clearly advantageous for unidirectional power flow
- Output Voltage:	Lower output voltage range, therefore mainly suited to applications requiring a non-standard motor anyway

Future Research

- Comparative evaluation of MC concepts and BBC for equal / optimally utilized semiconductor effort
- EMI performance (common mode filtering)
- Applicability for highly dynamic drives
- Sensorless control down to zero frequency
- Modulation for low pulse number / high power applications

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[1] **Carlson, A.:** „The back-to-back converter“, Master Thesis, Lund Institute of Technology Lund, Sweden, (1998).

[2] **Kolar, J.W., Baumann, M., Schafmeister, F., and Ertl, H.:** *Novel Three-Phase AC-DC-AC Sparse Matrix Converter. Part I - Derivation, Basic Principle of Operation, Space Vector Modulation, Dimensioning.* Proceedings of the 17th Annual IEEE Applied Power Electronics Conference and Exposition, Dallas (Texas), USA, March 10 - 14, Vol. 2, pp. 777 - 787 (2002).

[3] **Schafmeister, F., Baumann, M., and Kolar, J.W.:** *Analytically Closed Calculation of the Conduction and Switching Losses of Three-Phase AC-AC Sparse Matrix Converters.* Proceedings of the 10th International Power Electronics and Motion Control Conference, Dubrovnik, Croatia, Sept. 9 - 11, CD-ROM, ISBN: 953-184-047-4 (2002).

[4] **Schafmeister, F., Herold, S., and Kolar, J.W.:** *Evaluation of 1200V-Si-IGBTs and 1300V-SiC-JFETs for Application in Three-Phase Very Sparse Matrix AC-AC Converter Systems.* Proceedings of the 18th Annual IEEE Applied Power Electronics Conference and Exposition, Miami Beach (Florida), USA, February 9 - 13, Vol. 1, pp. 241 - 255 (2003).

[5] **Kolar, J.W., and Schafmeister, F.:** *Novel Modulation Schemes Minimizing the Switching Losses of Sparse Matrix Converters.* Proceedings of the 29th Annual Conference of the IEEE Industry Electronics Society, Roanoke (VA), USA, Nov. 2 - 6, pp. 2085 - 2090 (2003).

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[6] **Heldwein, M.L. , Nussbaumer, T. , and Kolar, J.W.:** *Differential Mode EMC Input Filter Design for Three-Phase AC-DC-AC Sparse Matrix PWM Converters.* Proceedings of the 35th IEEE Power Electronics Specialists Conference, Aachen, Germany, June 20 - 25, CD-ROM, ISBN: 07803-8400-8 (2004).

[7] **Heldwein, M.L. , Nussbaumer, T. , Beck, F., and Kolar, J.W.:** *Novel Three-Phase CM/DM Conducted Emissions Separator.* Proceedings of the 20th Annual IEEE Applied Power Electronics Conference and Exposition, Austin (Texas), USA, March 6 - 10, Vol. 2, pp. 797 - 802 (2005).

[8] **Friedli, T., Heldwein, M.L., Giezendanner, F., and Kolar, J. W.:** *A High Efficiency Indirect Matrix Converter Utilizing RB-IGBTs.* Proceedings of the 37th Power Electronics Specialists Conference, Jeju, Korea, June 18 - 22, CD ROM, ISBN: 1-4244-9717-7, (2006).

[9] **Round, S., Schafmeister, F., Heldwein, M.L., Pereira, E., Serpa, L., and Kolar, J.W.:** *Comparison of Performance and Realization Effort of a Very Sparse Matrix Converter to a Voltage DC Link PWM Inverter with Active Front End.* IEEJ Transactions of the Institute of Electrical Engineers of Japan, Volume 126-D, Number 5, May 2006, pp. 578 - 588.

Thank you very much for your attention !