

Performance Evaluation of Future T-Type PFC Rectifier and Inverter Systems with Monolithic Bidirectional 600 V GaN Switches

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Abstract—Three-phase PFC rectifier and inverter systems can be realized using identical main converter stages (MCSs) that comprise three three-level T-Type (TT) bridge-legs and a DC-bus referenced LC-filter stage. TT bridge-legs advantageously realize three output voltage levels by extending a half-bridge with the possibility to connect the switch node to the capacitive DC-link midpoint. To do so, a switching device with bipolar voltage blocking and bidirectional current carrying capability is required. A novel monolithic bidirectional 600 V/140 mΩ GaN e-mode transistor is an ideal candidate to realize the required midpoint connection in a chip-area efficient way. We therefore comprehensively characterize this monolithic bidirectional switch (M-BDS) in an 800 V DC TT bridge-leg realized with two additional 1200 V/140 mΩ SiC MOSFETs. Continuous operation of the M-BDS in all four voltage/current quadrants is demonstrated at ± 400 V, and results of calorimetric measurements of the hard- and soft switching losses are provided. This facilitates the evaluation of the TT MCS’ achievable performance in CCM and TCM rectifier and inverter designs regarding efficiency and power density. For MCSs with (three-phase) nominal power ratings of up to 2 kW, we find efficiencies of $> 99\%$ for power densities of up to about 15 kW/l.

I. INTRODUCTION

Bidirectional three-phase AC/DC or DC/AC converters with power ratings in the kilowatt range and a DC-bus voltage of 800 V are key components of a wide range of applications such as industrial power supply solutions, interfacing PV power generation to the AC grid, and efficient variable-speed

operation of electric motors. **Fig. 1** highlights the close similarity of rectifier and inverter applications: the main converter stages (MCSs), which consist of the power semiconductor switching stage (bridge-legs) and a first low-pass LC-filter stage, are identical. The converter stage must be complemented by further differential-mode (DM) and common-mode (CM) EMI filter stages in case of a grid-connected converter to meet limits given by EMI regulations. In case of motor drives, only an additional CM filter may be necessary for limiting radiated EMI in case of unshielded motor cables (not shown). A phase-modular, i.e., DC-bus referenced, realization of the LC-filter [1] advantageously provides integrated DM and CM filtering, facilitates paralleling of bridge-legs to increase the power rating, simplifies control, and enables a per-phase analysis, thus simplifying the design.

To reduce the harmonic content of the switching stage output voltage, three-level bridge-legs can preferably be used instead of standard two-level bridge-legs. The T-Type (TT) topology introduced in [2] and analyzed in detail in [3], [4] realizes the third voltage level by adding the possibility to connect the bridge-leg’s switch-node terminal to the capacitive DC-bus midpoint, see **Fig. 1**. To do so, the corresponding switching device must provide the capability to block half the DC-bus voltage in both polarities and to conduct current in both directions, i.e., bidirectional switches (BDSs) are required.

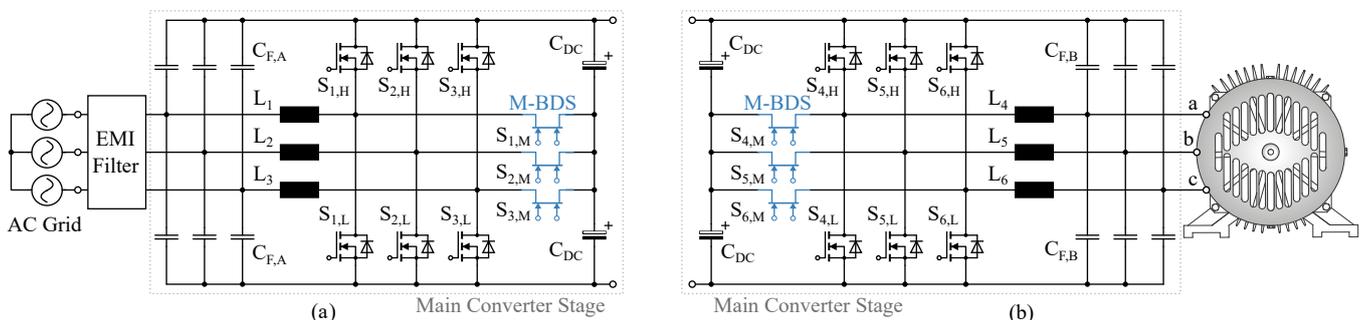


Fig. 1. Main converter stages (MCSs) of bidirectional three-phase AC/DC converters consisting of three-level T-Type (TT) bridge-legs and a first LC-filter stage referenced to the DC-bus. MCSs are universal building blocks for, e.g., (a) three-phase PFC rectifier and (b) three-phase motor inverter systems. Note the monolithic bidirectional GaN switches, $S_{X,M}$.

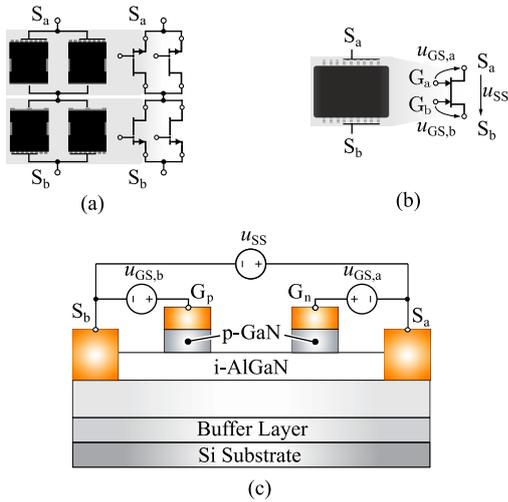


Fig. 2. (a) Realization of a BDS using four discrete unipolar GaN devices to achieve a total on-resistance equal to the on-resistance of a single device. The overall arrangement requires $4 \times$ the chip area of an individual device. (b) Alternative realization using a GaN M-BDS. (c) Structure of the GaN M-BDS, which integrates two switches in common-drain configuration, sharing a common drain-gate region.

BDSs can be realized by connecting two unipolar devices in anti-series. However, by doing so the total on-state resistance doubles. To achieve again the on-state resistance of a single device, a second anti-series configuration must be placed in parallel, i.e., in total, the required chip area increases by a factor of four (see **Fig. 2a**). Thus, recent research on *monolithic* bidirectional switches (M-BDSs), specifically GaN M-BDSs [5]–[8], see **Fig. 2b**, is of high interest regarding TT converter topologies (in addition to current-source or matrix converter topologies that also rely on devices with bipolar blocking and bidirectional current carrying capability [9]–[13]).

In this paper we present and experimentally characterize a TT MCS that employs novel monolithic bidirectional GaN e-mode 600 V/140 m Ω transistors [14]. **Fig. 2c** shows a schematic cross section of this M-BDS, which highlights the common-drain configuration and the two gate connections. As the same drain-gate region is used to take over the electric field for either blocking voltage polarity, the total chip area is expected to be small compared to that of a realization with discrete unidirectional devices discussed above. In addition, a single package facilitates improved PCB layouts.

Considering a typical DC-bus voltage of 800 V, the M-BDS employed in a TT bridge-leg operates at a blocking voltage of ± 400 V. We therefore demonstrate continuous high-frequency switching operation of the 600 V GaN M-BDS at ± 400 V, i.e., in all four voltage/current quadrants, without any external circuitry (except for the gate drives), see **Section II-A**. This facilitates the accurate calorimetric measurement of hard-switching and soft-switching losses of the TT bridge-leg’s power semiconductors, and ultimately the experimentally validated evaluation of the achievable efficiency and power density of a TT MCS designed for a rectifier or for an inverter application, and operating in continuous-conduction mode

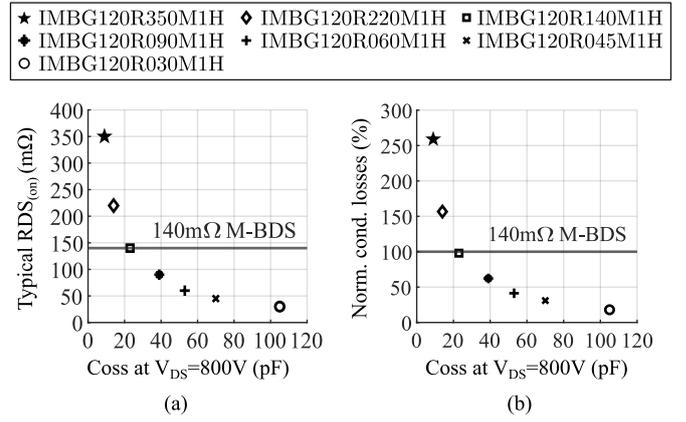


Fig. 3. (a) Typical on-state resistance and charge-equivalent output capacitance of the considered series of 1200 V SiC MOSFETs. (b) Conduction losses in a TT bridge-leg normalized to those of the 140 m Ω GaN M-BDS for an exemplary operating point (800 V DC-bus voltage, 230 V AC RMS phase voltage, and an RMS phase current of 7 A).

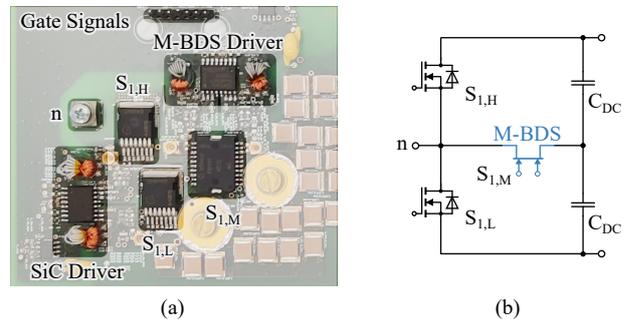


Fig. 4. (a) TT bridge-leg characterization PCB with the 600 V GaN M-BDS, the two 1200 V SiC MOSFETs (IMBG120R140M1H), and the gate drives highlighted. (b) Corresponding circuit diagram of the three-level TT bridge-leg consisting of the M-BDS $S_{1,M}$ and two SiC MOSFETs $S_{1,H}$ and $S_{1,L}$.

(CCM) or in zero voltage switching (ZVS) triangular-current mode (TCM).

II. CHARACTERIZATION OF THE M-BDS TT BRIDGE-LEG

To evaluate the performance of the M-BDSs S_{xM} in the TT bridge-legs operating with an 800 V DC-bus, suitable high- and low-side transistors S_{xH} and S_{xL} according to **Fig. 1** have to be selected, which we do by demanding similar conduction losses for each of these transistors as resulting for the M-BDSs. With very limited availability of 1200 V GaN devices, we consider SiC MOSFETs. **Fig. 3a** compares the $R_{DS(on)}$ of a series of 1200 V SiC transistors against the $R_{DS(on)}$ of the GaN M-BDS.

However, due to the different position in the TT bridge-leg, similar $R_{DS(on)}$ of the SiC devices does not necessarily imply conduction losses similar to those of the M-BDS. Thus, **Fig. 3b** shows simulated conduction losses for the upper or lower 1200 V SiC MOSFET considering an 800 V DC-bus voltage, 230 V AC RMS phase voltage and an RMS phase current of 7 A. Furthermore, the temperature-dependency of $R_{DS(on)}$ is considered for a fixed case temperature (90 $^{\circ}$ C) and switching losses are neglected in a first step. The results

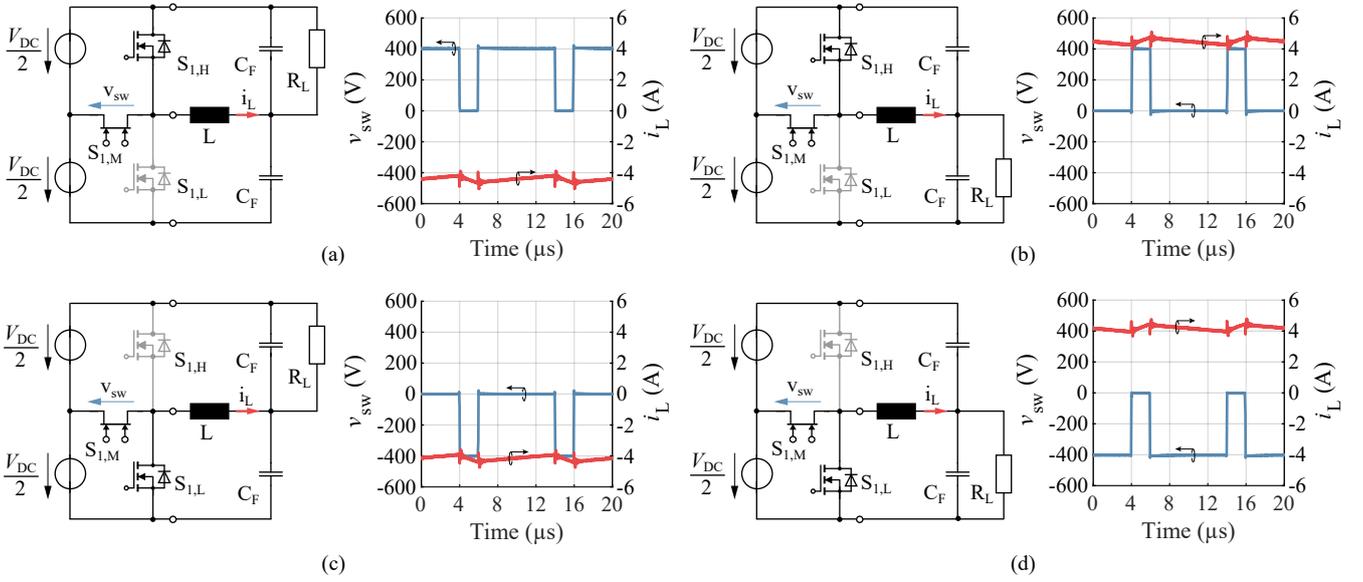


Fig. 5. Experimental verification of the continuous operation of the new GaN M-BDS with a DC voltage of ± 400 V and both current directions, i.e., in all four quadrants of the blocking voltage/on-state current plane. Except for the gate drive, the M-BDS does not require any external circuitry. The figures show the measurement circuit configurations and the corresponding CCM inductor current and switch-node voltage waveforms for switch $S_{1,M}$ operating in the (a) first, (b) second, (c) third, and (d) fourth quadrant.

confirm that the best pairing for the $140\text{ m}\Omega$ GaN M-BDS is a $140\text{ m}\Omega$ SiC MOSFET device (IMBG120R140M1H), which we thus select for the realization of the TT bridge-leg to be characterized.

A. Demonstration of GaN M-BDS Four-Quadrant Operation

The novel GaN M-BDS features an internal common-drain structure with two source and gate connections (see **Fig. 2c**). Each gate controls the device's blocking capability for one of the two possible polarities of the source-to-source voltage u_{SS} ; the device can thus operate in all four quadrants of the blocking voltage/on-state current plane. Note that the two gate connections are not referred to the same source terminal, i.e., need to be isolated from each other and two dedicated signal isolators and gate-drive power supplies are required. Owing to the non-isolating p-doped GaN layer beneath the gate connection (see **Fig. 2c**), p-n junction diodes are formed, which makes the device a Gate Injection Transistor (GIT). This implies that once the device is turned-on with a gate-source voltage u_{GS} higher than its threshold voltage u_{th} , a constant gate current of a few mA must flow through each gate to modulate the conductivity of the conducting channel. Thus, the considered GIT-type M-BDS requires a corresponding gate driver, which has been implemented on a test PCB (see **Fig. 4**) used for the calorimetric loss measurements of the TT bridge-leg semiconductors.

Using this test setup, we first operate the novel GaN M-BDS in all four quadrants with a DC voltage of ± 400 V as required from the BDS in a 800 V DC-bus TT converter. **Fig. 5** shows the corresponding equivalent circuit diagrams and the measured switch-node voltage v_{sw} and inductor current i_L waveforms for CCM operation. This demonstrates that the GaN M-BDS can continuously operate in all four quadrants with a

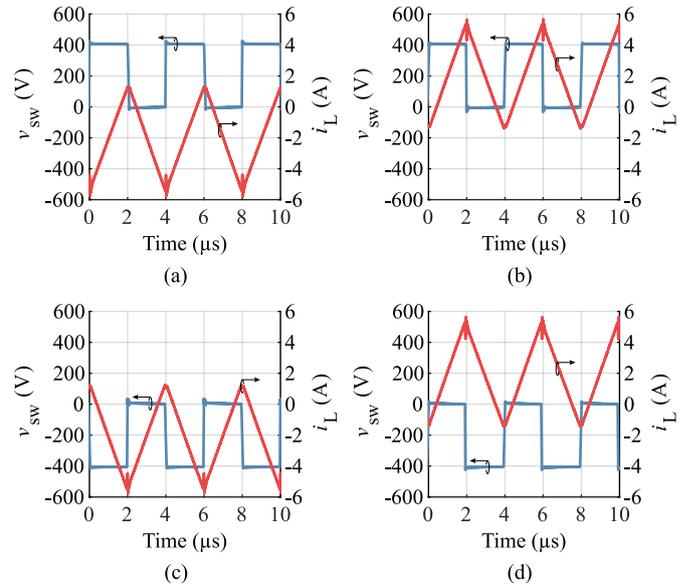


Fig. 6. Measured TCM inductor current and switch-node voltage waveforms for switch $S_{1,M}$ operating in the (a) first, (b) second, (c) third, and (d) fourth quadrant (see **Fig. 5** for the circuit configurations). Note: the characteristic fundamental-frequency time behavior of the filter inductor current in case of TCM operation is shown in **Fig. 12b**.

blocking voltage of ± 400 V and does not require any external circuitry (except for the gate drives). To the knowledge of the authors, this has not been shown for 600 V GaN M-BDSs before.

Similarly, the bridge-leg can also operate in TCM mode (see **Fig. 12b**) to achieve zero-voltage switching (ZVS) for all transitions, see, e.g., [15], [16]. To do so, a different inductor and an appropriate selection of the switching frequency and

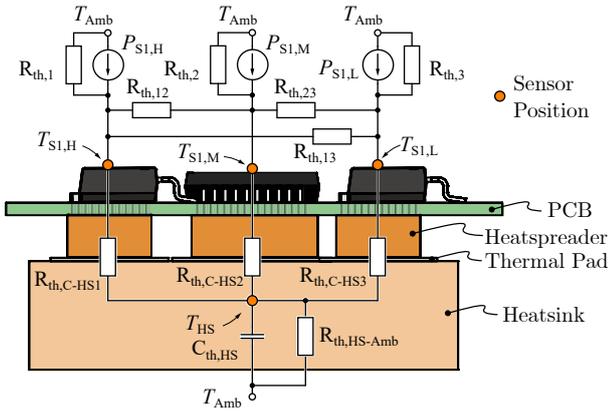


Fig. 7. Cross sectional view of the calorimetric measurement setup showing the thermal equivalent circuit and the positions of the NTC temperature sensors (Littlefuse PS104J2). The heat sink temperature is obtained by averaging the readings of two sensors attached laterally on either side of the heat sink at half height. Note that the ambient temperature sensor, the second heat sink temperature sensor, and an additional cover that reduces the external air flow near the setup, are not shown. The heat sink (60 mm×88 mm×30 mm) and the heat spreaders for the SiC MOSFETs (12 mm×10 mm×5 mm) and for the M-BDS (7 mm×15 mm×5 mm) are made out of brass. The heat spreaders are electrically isolated from the heat sink with a 0.5 mm thermal pad (Bergquist SIL PAD TSP A3000).

of the interlock delay time have been used. **Fig. 6** shows the corresponding waveforms that confirm successful TCM operation of the M-BDS-based three-level TT bridge-leg in all four quadrants.

B. Calorimetric Switching Loss Measurement Method

To measure the losses of the M-BDS and the two SiC MOSFETs in the TT bridge-leg, we employ a transient calorimetric measurement method to avoid the difficulties and inaccuracies found for electrical measurement methods (double-pulse testing), which are a consequence of the very fast-switching transients of wide-bandgap power semiconductors [17], [18]. Essentially, the total power dissipation of a power semiconductor can be measured by continuously switching the device at a current of interest, and then measuring the time it takes to increase the temperature of an attached thermal capacitance (i.e., a heat sink) by a certain amount, e.g., by 10 K. The relationship between temperature increase and power dissipation can be calibrated by injecting known losses into the power semiconductor with a controlled DC current, which facilitates highly accurate electrical reference measurements (DC voltage and DC current). Inherently, the approach measures total semiconductor losses. To separate the switching losses from the total losses, the conduction losses must be subtracted. These can be calculated from the measured current and the temperature-dependent on-state resistance (which follows from the calibration measurements, too). For further details, please refer to [17]–[19].

1) *Loss Separation:* A typical two-level half-bridge configuration consists of two identical power semiconductors. Therefore, it is sufficient to measure the total power dissipation

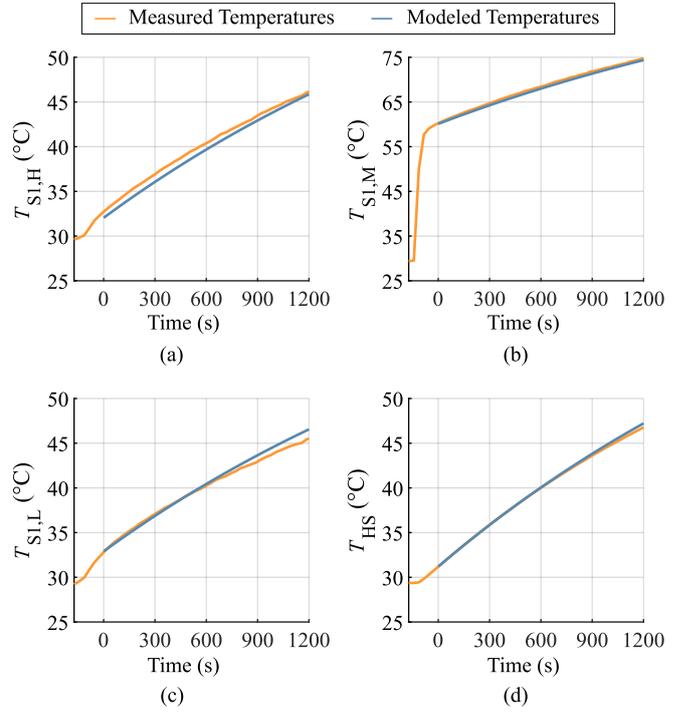


Fig. 8. Measured and modeled temperature transients when injecting 9.55 W of losses into the M-BDS: (a) high-side SiC MOSFET, (b) GaN M-BDS, (c) low-side SiC MOSFET, and (d) heat sink.

TABLE I
PARAMETERS OF THE THERMAL MODEL FROM **FIG. 7**
OBTAINED FROM CALIBRATION MEASUREMENTS.

Parameter	Value	Parameter	Value
$R_{th,1}$	21.0 K/W	$R_{th,C-HS1}$	3.35 K/W
$R_{th,2}$	30.8 K/W	$R_{th,C-HS2}$	3.69 K/W
$R_{th,3}$	20.7 K/W	$R_{th,C-HS3}$	3.68 K/W
$R_{th,12}$	126 K/W		
$R_{th,13}$	49.2 K/W	$R_{th,HS-amb}$	16.1 K/W
$R_{th,23}$	52.8 K/W	$C_{th,HS}$	495.4 J/K

of both switches into a common heat sink, as during hard-switching the total switching losses (turn-on plus turn-off) are of interest, and during soft-switching operation (symmetric TCM), both devices experience identical residual [20] turn-off losses. The three-level TT bridge-leg, however, contains two different types of semiconductors. The transient calorimetric method must thus be extended by the capability of separating the losses generated by the individual devices. However, the need for a low commutation loop inductance and hence close proximity of the switches renders the obvious solution of dedicated heat sinks per device impractical.

Instead, we use the approach illustrated in **Fig. 7**. The test board shown in **Fig. 4** is thermally connected to a brass block acting as a heat sink by conducting the dissipated heat from the switches first through the PCB using thermal vias, then through individual brass heat spreaders and finally a mechanically reinforced and electrically isolating thermal pad (Bergquist SIL PAD TSP A3000). This setup allows the separation of

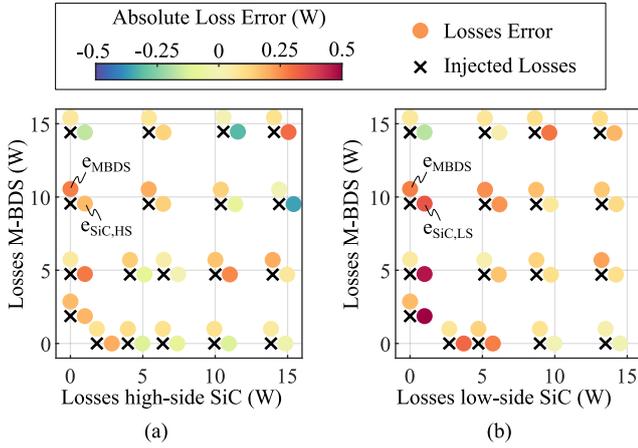


Fig. 9. Absolute deviation (colored dots) of calorimetrically measured losses from injected DC losses (black crosses). (a) Injection of DC losses in the GaN M-BDS and/or in the high-side SiC MOSFET; (b) injection of DC losses in the GaN M-BDS and/or in the low-side SiC MOSFET. The absolute error e_{MBDS} for the M-BDS is indicated by the colored dot above each black cross, whereas the errors for the high-side, $e_{\text{SiC,HS}}$, or for the low-side SiC MOSFET, $e_{\text{SiC,LS}}$, are shown on the right, respectively.

the heat fluxes of the different semiconductors by means of not only measuring the temperature rise of the (common) heat sink (T_{HS}), but also the rise of the individual semiconductor case temperatures ($T_{\text{S1},x}$), as indicated by **Fig. 7** that shows the cross section of the test setup and the corresponding thermal RC network. As mentioned, the switches are placed close to each other to minimize the commutation loop inductance, which however leads to thermal cross-couplings between the switches. The thermal resistances $R_{\text{th},xy}$ consider this effect. In addition, some heat is dissipated directly to the ambient via the surface of the switches and the PCB, represented by $R_{\text{th},x}$. To sense the temperatures of the switches, the heat sink and the ambient air, we use precision NTC temperature sensors (Littlefuse PS104J2). Note that in contrast to other reported calorimetric measurement approaches (e.g., [17], [18]) we do not thermally isolate the heat sink from the ambient as the heat dissipation of the PCB directly to the ambient is significant and unavoidable in any case because of the employed SMD power devices.

2) *Calibration:* The thermal network describing the test setup has 11 degrees of freedom (see **Fig. 7**). The corresponding model parameters must be identified with an initial calibration process. To do so, known¹ and constant DC power is dissipated in one or two of the TT bridge-leg's switches and the temperature response of the sensors recorded. **Fig. 8** shows an exemplary transient where 9.55 W of losses are dissipated in $T_{\text{S1},M}$ starting from $t = -140$ s. This results in a rise of the measured temperatures of all switches and of the heat sink. Based on the measured temperature transients for various operating points (power levels, heated devices), we fit the model parameters using a particle swarm algorithm. **Fig. 8** shows the measured temperatures and the predictions

¹Note that it is possible to electrically measure DC power with very high accuracy. Equipment used: Fluke 189.

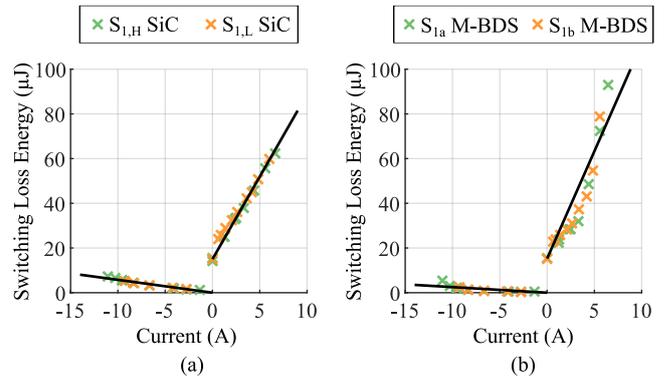


Fig. 10. Calorimetrically measured switching losses of the TT bridge-leg according to **Fig. 5** for (a) high- and low-side SiC MOSFETs and (b) for both integrated switches of the GaN M-BDS. Positive currents imply hard-switching and negative currents imply soft-switching. **Tab. II** contains the fitting coefficients for the shown linear approximations.

TABLE II
COEFFICIENTS OF THE LINEAR FIT OF MEASURED
HARD-SWITCHING AND SOFT-SWITCHING LOSSES OF THE
GaN M-BDS AND THE SiC MOSFET IN THE TT BRIDGE-LEG.

Power Semiconductor	hard-switching		soft-switching	
	k_0 (μJ)	k_1 ($\text{V}\mu\text{s}$)	k_0 (μJ)	k_1 ($\text{V}\mu\text{s}$)
600 V GaN M-BDS	15.27	9.6	0	0.25
1200 V SiC MOSFET	15.01	7.382	0	0.576

of the calibrated model for the mentioned exemplary operating point. **Tab. I** summarizes the obtained model parameters. Note that since the model does not capture the thermal capacitances of the switches, the PCB, the heat spreaders, and the NTC sensors, it cannot capture the initial, fast transient, and consequently the fit starts after this first transient has subsided. Even though the power is injected only into the M-BDS $S_{1,M}$, the temperatures of the other two switches (see **Figs. 8ac**) are correctly predicted, which proves the model's ability to capture the thermal cross-couplings.

The accuracy of the thermal model has been characterized by injecting known DC losses into one or two switches at the time. **Fig. 9** shows the deviation of the losses measured with the calorimetric method (i.e., obtained via the measured temperature transients and the thermal model parametrized with the values from **Tab. I**) from the injected DC losses (black crosses) as absolute errors, which are indicated by the adjacent colored dots. In general, we find good agreement between electrical and calorimetric measurements. The maximum absolute error of about 0.5 W occurs for the loss measurement of the low-side SiC MOSFET in case power is injected into the M-BDS only. Typical errors are lower, however, and the figure indicates that the accuracy of the calorimetric measurement of the M-BDS losses is slightly better compared to that of the SiC MOSFETs.

C. Switching Loss Measurement Results

The calibrated calorimetric loss measurement setup is used to measure the switching losses for various operating points

(top and bottom commutation cell, both current directions, and various load current levels). The respective conduction losses are calculated from the measured load current and the temperature-dependent on-state resistance of the devices (measured in advance), and then subtracted from the calorimetrically measured total losses to obtain the switching losses only. Thus, operating a commutation cell in CCM yields the total hard-switching losses of the involved devices (M-BDS and either the high-side or the low-side SiC MOSFET)². Similarly, operating the commutation cell in TCM yields the residual [20] turn-off switching energies only (soft-switching). **Fig. 10** shows the measured hard-switching and soft-switching losses of the GaN M-BDS and the SiC MOSFETs in the considered TT bridge-leg. As expected, the switching losses obtained from the two commutation cells are similar. We fit the data with linear models, i.e.,

$$E(I_{sw}) = k_0 + k_1 I_{sw}, \quad (1)$$

to be used in the performance evaluation described in the next **Section III**. **Tab. II** provides the model coefficients for hard-switching and soft-switching losses.

III. PERFORMANCE EVALUATION

The calorimetric in-situ switching loss measurements of the novel 600 V/140 mΩ GaN M-BDS and the 1200 V/140 mΩ SiC MOSFETs in a prototype TT bridge-leg facilitates an accurate estimation of the achievable performance of full three-phase TT MCSs (see **Fig. 1**) in terms of efficiency and power density. To do so, we employ a simulation-based optimization procedure that makes use of the measured semiconductor losses and models known from literature for the passive components.

A. CCM Operation

Assuming a fixed junction temperature of 125 °C, we calculate the semiconductor losses for a set of designs, each characterized by a switching frequency and a rated three-phase nominal power, considering PFC operation (designs for rectifiers) or resistive load behavior (designs for inverters) and CCM operation. For each design, the corresponding heat sink volume is estimated based on a typical cooling system performance index (CSPI) [23] of 15 W/K dm³ [11] and assuming an ambient temperature of 45 °C. The LC-filter stage (see **Fig. 1**) is dimensioned with a maximum inductor current ripple of ±30 % and for an overall attenuation of about 40 dB, i.e., a maximum peak value of the capacitor voltage ripple of ±1 %. The inductor losses and volumes are obtained using the method described in [24], considering N87 (ferrite) and Kool-Mμ (iron powder) E-, ETD-, and U-cores combined with flat or round solid wires or litz wires. To select an inductor from the resulting multitude of possible designs, we choose a minimum-volume design whose losses do not exceed 1/3 of the total semiconductor losses. Finally, we consider ceramic capacitors for the DC-bus and AC-side filter capacitors, neglect their

²Note that also the SiC MOSFET not directly involved in the commutation contributes to losses because of the current required to charge or discharge its output capacitance [21], [22].

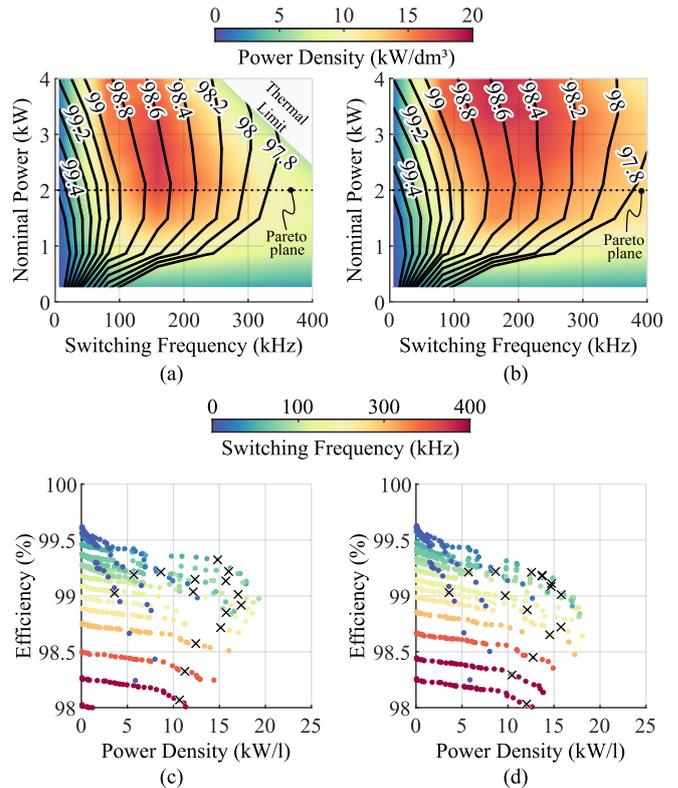


Fig. 11. Power density and efficiency for three-phase TT MCSs designed for various nominal power levels and switching frequencies, (a) for rectifier and (b) for inverter operation in CCM. The inductor designs are selected such that their losses do not exceed 1/3 of the semiconductor losses. (c) and (d) show the corresponding full (i.e., including all possible inductor designs for a given power level and switching frequency) sets of possible MCS designs with a nominal three-phase power of 2 kW, again designed for rectifier or inverter operation, respectively. The crosses indicate the designs that lie on the dashed lines in (a) and (b), i.e., where the mentioned inductor selection criteria applies.

losses, and model the volume based on an empirical survey of commercially available parts [25].

Fig. 11a gives a first overview on the dependence of the achievable power densities and efficiencies on the switching frequencies and the nominal design power ratings of TT MCSs for PFC rectifier applications. Designs with a low switching frequency achieve high efficiencies of well above 99 %, but suffer regarding power density (calculated as the sum of the main components' volumes and considering an overall volume utilization of 66 %) due to larger inductors. Maximum power density designs are achieved with a switching frequency of 150 kHz and a nominal three-phase power rating of 2 kW. Designs beyond the thermal limit indicated in the figure are not possible because the temperature rise between the M-BDSs' case and junction becomes too high (regardless of the external heat sink). Similarly, **Fig. 11b** shows the same overview for MCS designs for inverter applications, indicating that a maximum power density can be achieved with a switching frequency of 200 kHz for a design with a nominal power of 3.5 kW.

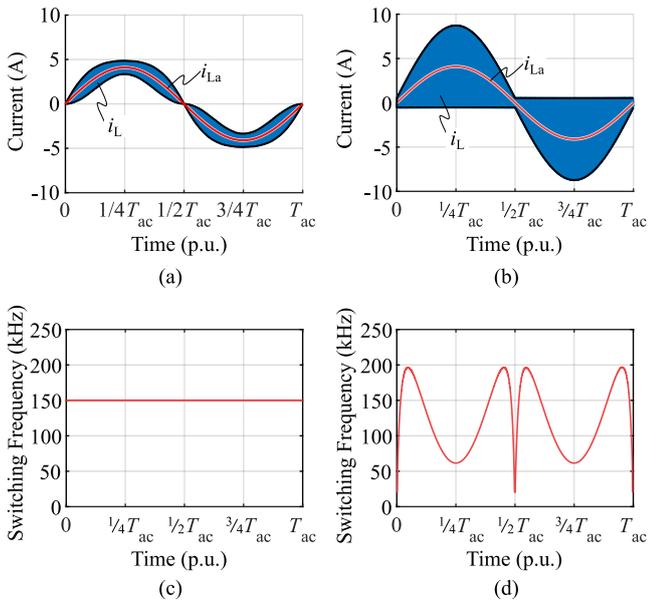


Fig. 12. Exemplary average phase current i_{La} and inductor current i_L containing a high-frequency ripple for (a) CCM and (b) TCM operation of a TT bridge-leg as shown in Fig. 1. The corresponding switching frequency is shown in (c) for CCM and in (d) for TCM operation for exemplary designs with a power rating of 2 kW.

Whereas the above analysis indicates the sweetspots in terms of power ratings, the ultimately arbitrary criteria for selecting a certain inductor design must be relaxed to reveal the full performance limits. Therefore, **Figs. 11cd** show the set of valid designs of a MCS with a nominal power rating of 2 kW in the efficiency/power density performance space for a rectifier and for an inverter application, respectively. These results include all feasible inductor designs that the employed method [24] finds for the given specifications. The crosses indicate those designs featuring inductors that meet the initial selection criterium mentioned above, and which thus lie on the dashed lines in **Figs. 11ab**. Clearly, the selection criteria emphasizes compact designs (crosses close to the actual Pareto front for higher power densities). Note that **Figs. 13ab** show the Pareto fronts in the efficiency/power density performance space for MCS designs with two additional nominal power levels.

B. TCM Operation

The phase-modular three-phase TT MCSs can also operate in TCM, see, e.g., [15], [16], in order to achieve soft-switching of the power semiconductors at the expense of higher device RMS currents ($\approx 30\%$ higher conduction losses [20]). **Fig. 12** qualitatively illustrates the inductor current waveforms and the corresponding switching frequency variation over a grid period for the two operating modes. In general, TCM operation of a TT bridge-leg shows a variation of the switching frequency that is comparable to that of a single-phase totem-pole PFC rectifier operated in TCM, see [20]. As the three-level bridge-leg features a true zero-volt output state, the switching frequency can become very low for applications where low mod-

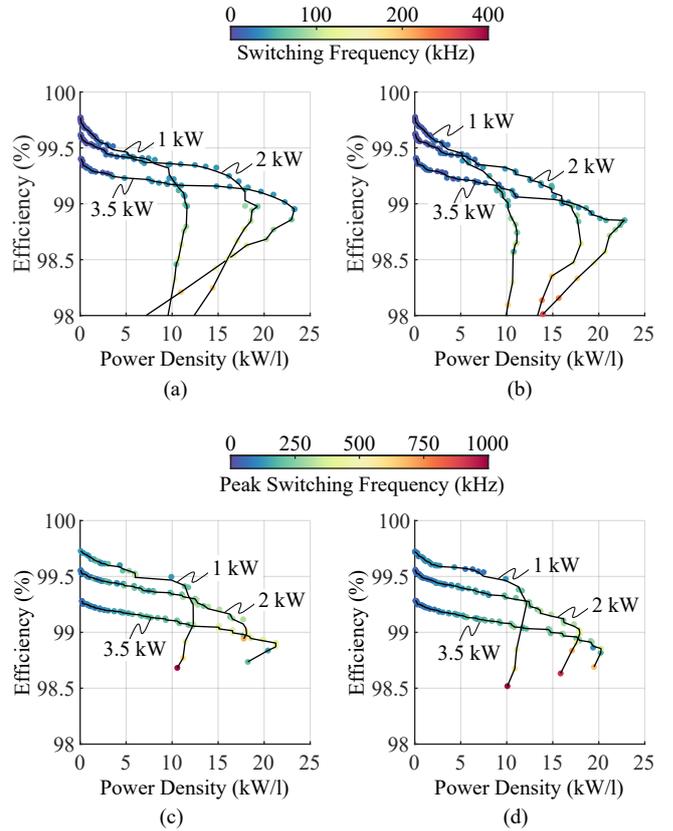


Fig. 13. Pareto fronts in the efficiency/power density performance space for MCS designs for (a) CCM rectifier, (b) CCM inverter, (c) TCM rectifier, and (d) TCM inverter applications with different nominal power ratings (and considering a phase shift of the MCS output voltage and current of 0° or 180° , respectively). Note that the 3.5 kW CCM rectifier designs in (a) reach the thermal limit of the M-BDS' package for high switching frequencies, which explains the different slope of the corresponding curve's lower branch.

ulation indices are required (e.g., motor drive applications), resulting in undesirable acoustic noise. For such applications special considerations are necessary, e.g., temporary operation in CCM, which we do not investigate further here.

Note, however, that TCM operation of TT MCSs is well suited for applications using high modulation indices such as grid-tied converters like PFC rectifiers and PV inverters. Therefore, we adapt the optimization procedure described above for TCM operation and consider the same component models and boundary conditions (e.g., DC- and AC-side capacitor voltage ripples) to obtain the Pareto fronts shown in **Figs. 13cd**, again for rectifier or inverter designs, respectively.

C. Discussion

Comparing the results for rectifier operation, TCM designs slightly outperform CCM designs for the lowest considered nominal power rating of 1 kW. Due to the low currents and hence low conduction losses, TCM facilitates high average switching frequencies without a significant efficiency reduction, but with lower inductor volumes. In contrast, in case of higher nominal power ratings, e.g., 3.5 kW, CCM designs achieve higher efficiency at similar power density. This indicates that at these power (current) levels, the conduction losses

of the switches start to dominate when TCM is employed. Considering an intermediate nominal power rating of 2kW, TCM and CCM designs will give similar performance.

The importance of selecting matching switches for the different positions in the TT bridge-leg (see **Section II**) can be observed by comparing the achievable performances of TCM rectifier and inverter designs, which are very similar (see **Figs. 13cd**). This is a consequence of the dominating conduction losses and the chosen switch pairing such that the on-state resistances of the M-BDS and the SiC MOSFETs are about equal. Note that also the performances of the CCM rectifier and inverter designs are comparable, because the hard-switching losses of the GaN M-BDS and of the SiC MOSFETs are similar, too.

IV. CONCLUSION

This paper presents the experimental characterization of a novel 600 V/140 mΩ monolithic bidirectional GaN e-mode transistor (monolithic bidirectional switch, M-BDS) in a T-Type (TT) three-level bridge-leg in combination with two 1200 V/140 mΩ SiC MOSFETs and with a DC voltage of 800 V. We demonstrate continuous operation of the M-BDS in all four voltage/current quadrants at ±400 V without any external circuitry (except for the gate drives), which facilitates accurate calorimetric measurements of the hard- and soft-switching losses of the TT bridge-leg's power semiconductors.

Based on these experimental results, we analyze the achievable efficiency and power density of a three-phase main converter stage (MCS) that employs three TT bridge-legs and a DC-bus referenced LC-output filter, being suitable for the realization of both, PFC rectifier and inverter systems. The calculated Pareto fronts in the efficiency/power density performance space enable a comparison of different nominal power ratings and different operating modes, i.e., CCM and TCM. TCM designs are favorable for lower nominal power ratings, e.g., 1 kW only. In terms of power ratings, we identify a sweet spot at 2 kW, where MCS designs achieve efficiencies of > 99 % for power densities of up to about 15 kW/l.

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