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Abstract

The trend towards higher computation power per server rack has lead to an increased interest in high density server power supplies with high efficiency and low cost. This paper analyzes how the specific features of planar magnetics as transformers and inductors can be best utilized in combination with GaN power semiconductors to reach unprecedented system performance both for power supplies with 12 V and with 48 V output voltage. Based on the optimization results a hardware demonstrator with an ultra-high power density (350 W/in^3) of a 3 kW DC/DC converter stage with a wide-input voltage range of 300 V-430 V and an output voltage of 12 V is presented.

1 Introduction

The large demand for cloud computing, initiated by ever more data traffic, has resulted in a strong increase of hyper-scale datacenter installations. Hyper-scale datacenters are different in terms of architecture in several central aspects: Instead of having a dedicated battery room for the whole server farm to provide an uninterruptible power supply (UPS) as in the legacy server architecture, hyper-scale data centers have batteries locally in each server rack, which leads to a higher overall efficiency by omitting additional conversion stages in the power flow. Furthermore, the hyper-scale architectures feature rack based power supply units (which can feed multiple server boards) instead of power supplies on each server board. This allows to change the redundancy scheme from $1+1$ to $N+1$ for additional cost saving.
Furthermore, it is estimated that the power per rack for the 12 V ecosystem will grow from currently 8...10 kW to 12...16 kW and beyond in the future. High power applications with up to 4 kW power consumption are a reality for specific AI tasks. The increase of power in a given form factor to cope with the rising computation demands brings several advantages, such as

- reduced capital expenditures (CAPEX): By moving from a $1+1$ to a $N+1$ redundancy scheme, the system integrator can buy e.g. 6 times a 3 kW supply instead of 60 times a 500 W supply for a 15 kW server;
- reduced operating costs (OPEX): By removing the UPS and installing local back up power, the additional losses of the UPS stage are omitted;
- increased return on investment (ROI) through better usage of the existing data center footprint .

In order to support this trend towards high density servers, power supplies featuring unprecedented power densities with high efficiency are required. In this paper it is shown, how enhancement mode (e-mode) GaN HEMTs in combination with planar magnetics can push the performance boundaries of state-of-the-art Si-based power supplies. The remainder of the paper is structured as follows. In **Sec. 2** the characteristic differences between planar and litz wire magnetics are analyzed, on the one side for high-frequency transformers and on the other side for PFC boost inductors. Based on the results of this analysis on component level, in a second step system level optimizations results for server supplies with 12 V and 48 V output voltage are presented in **Sec. 3** for Si and GaN semiconductor. As an essential building block for future high density power supplies, in **Sec. 4** the hardware design of an ultra-high density regulated 400 V-to-12 V DC/DC converter stage employing GaN semiconductors and a "Snake" core transformer is presented together with measurement results. Finally, **Sec. 5** presents conclusions and outlook on future work.

2 Theoretical Analysis of Planar Magnetics

In order to utilize planar magnetics with PCB-integrated windings in the most optimal way, the specific properties of these devices have to be understood in comparison to alternative winding types, such as litz or round wires. For this comparison, two different use cases of magnetic components are examined: a transformer of a series resonant converter operating in resonance (i.e. DCX converter), and a boost inductor in a totem-pole PFC converter. These two applications are very different with respect to the usage of the magnetic devices. In the case of the transformer the (peak) flux density B_{peak} within the core is independent of the load current and just influenced by the applied voltage-

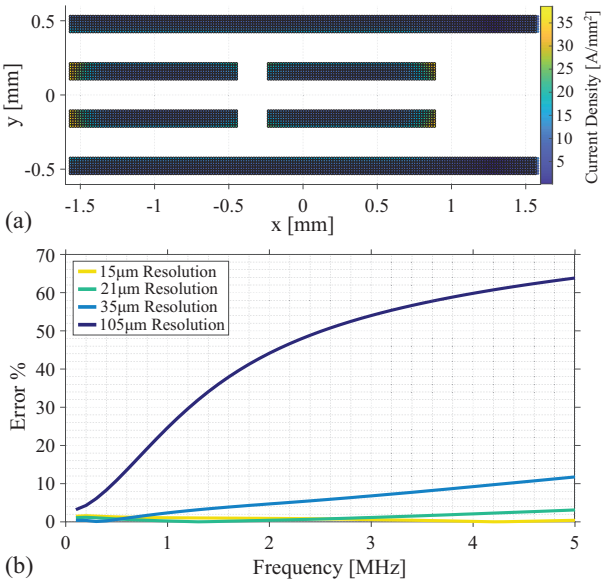

Figure 1 (a) Example of the PEEC method applied to a 4-layer center-tapped 4 : 1 transformer (outer layers: secondary windings; inner layers: primary windings) showing the discretization of the windings into sub-conductors. (b) Influence of sub-conductor resolution on loss calculation accuracy as a function of frequency.

time area,

$$B_{\text{peak,tr}} = \frac{V_{\text{p}}}{N_{\text{p}} \cdot A_{\text{core}} \cdot f_{\text{sw}} \cdot 4} \tag{1}$$

with N_{p} being the number of turns on the primary side and A_{core} the core area. In contrast, in the inductor the flux density is directly proportional to the current I_{ind} inside the inductor

$$B_{\text{peak,ind}} = \frac{L_{\text{ind}} \cdot I_{\text{ind}}}{N \cdot A_{\text{core}}}. \tag{2}$$

Another difference between these two magnetic components is the inductance value. For the boost inductor, the inductance value is a design variable which is typcially determined by the outcome of the overall system optimization process. Thus, in most of the cases an air-gap is employed in the inductor in order to allow a design with a specific inductance value without saturating the core. In the transformer, however, it is assumed for this analysis that no air-gap is inserted in order to minimize the circulating magnetizing current.

For an accurate calculation of the magnetic device losses, models for the electric, magnetic, and thermal domain have to be coupled, as described for magnetic components employing litz wires in [1] and [2]. For the calculation of planar winding losses, the partial-element-equivalent-circuit (PEEC) method is selected, since it offers an accuracy close to the finite-element-method (FEM) method at substantially lower computational efforts [3]. The method is based on a discretization of the windings into a set of sub-conductors (see **Fig. 1(a)** for an example of a transformer with 4 PCB layers). The relevant governing effects in power electronics can be captured already with the simplified (R,L_{p})PEEC model (by ignoring capacitive couplings) in the form of

$$\begin{bmatrix} \mathbf{A} & -(\mathbf{R}+j\omega\mathbf{L}) \\ 0 & -\mathbf{A}^T \end{bmatrix} \begin{bmatrix} \mathbf{V} \\ \mathbf{I} \end{bmatrix} = \begin{bmatrix} 0 \\ \mathbf{I}_S \end{bmatrix} \tag{3}$$

where $\mathbf{A}$ is the connectivity matrix defining the connections of the sub-conductors, $\mathbf{R}$ is the resistance matrix, $\mathbf{L}$ is the self and mutual inductance matrix, $\mathbf{V}$ is the vector of the unknown node voltages potential, $\mathbf{I}$ is the vector of the unknown currents flowing in each sub-conductor, and $\mathbf{I}_{\text{s}}$ is the current source vector. For the case of PCB integrated planar windings with typical thicknesses in the range of 35...105 μm the reluctance-based approach ([4]) with reluctance matrix $\mathbf{K} = \mathbf{L}^{-1}$ and subsequent sparsification ([5]) was found to provide considerable performance improvements in terms of calculation speed. As a determining factor for the size of matrices in the PEEC formulation of the circuit, the meshing resolution plays an important role, since it also influence the modeling accuracy. For the frequency range commonly found in power electronic systems of 10 kHz...5 MHz (including higher harmonics of the switching frequency) volume cells with edge lengths of 35 μm offer an acceptable relative error in the single-digit range (compared to a FEM analysis), as shown in **Fig. 1(b)**.

2.1 Transformer Analysis

For the magnetic analysis of transformers in an LLC (operated at resonance, i.e. DCX), a system power of $P_{\text{out,rat}} =$ 3 kW is selected. The primary side consists of a half-bridge operating at a DC-bus voltage of 400 V whereas for the sec-

Table 1 Magnetic optimization settings.

General Settings	
Ambient temperature	40 °C
Cooling	Forced convect. with 2 m/s
Transformer Settings	
Resonant frequencies	[50, 100, 150, ..., 1000]kHz
Nr. of XFRM in matrix	[1, 2, 3, 4]
Nr. of parallel stages	[1, 2]
Inductor Settings	
Switching frequencies	[50, 100, 150, ..., 1000]kHz
Current ripples	[2, 4, 6, ..., 18]A
Nr. of parallel stages	[1, 2, 3]
Litz Wire Magnetics	
Core shapes	RM4,...,RM14 (incl. LP)
Strand diameters	[71, 100, 200, 355]μm
Nr. of strands	no limits set
Core material	Ferrite N87 & N49
Planar Magnetics	
Core shapes	PQI16,...,PQI26
Nr. of layers	[4, 6, 8, 10, 12]
Copper thickness	[35, 70, 105[1]]μm
Core material	Ferrite N87 & N49

[1] up to 8 layers

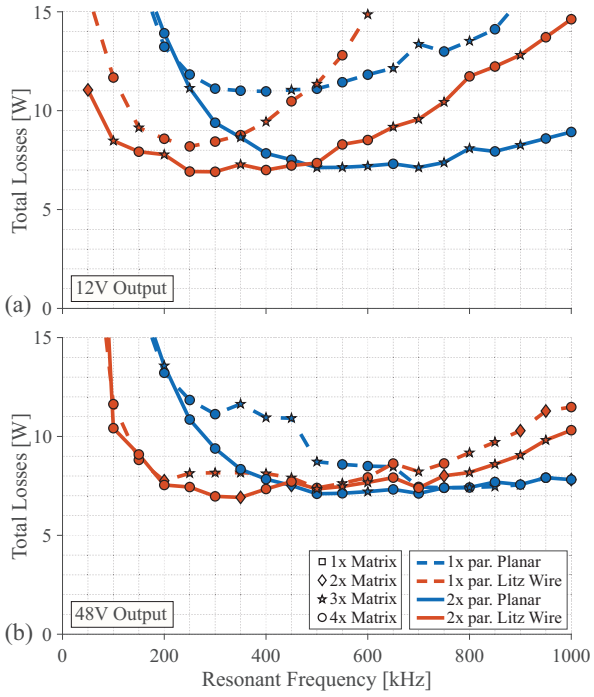

Figure 2 Optimzation results of 3 kW DCX-transformers (at 50 % load) for (a) 12V and (b) 48V output voltage for planar and litz wire designs. The results show the lowest achievable losses for single and two-times interleaved transformer stages with the number of sub-transformers being an optimization output parameter.

ondary side two different cases are studied: first, an output voltage of 12 V with center-tapped rectification, and, second, an output voltage of 48 V with full-bridge rectification. The transformer arrangement can consist of either a single transformer or of multiple individual transformers in matrix arrangement, i.e. in input-series output-parallel connection with individual synchronous rectification stages, and constitutes a free optimization parameter. The full set of optimization parameters can be found in **Tab. 1**.

The comparison between litz and planar windings is conducted by optimizing for all resonant frequencies between 50 kHz and 1 MHz (divided in 50 kHz steps) each winding type individually within the design space of **Tab. 1** for a part load operating point of $P_{\text{load}} = 50\% P_{\text{out,rat}}$. For planar windings no interleaving is assumed, because this heavily increases the coupling capacitance between primary and secondary side and can distort the converter operation and/or lead to excessive EMI noise. Also not considered in this analysis is the possibility of magnetically integrating planar matrix transformers into a single magnetic structure, as in [6] or [7].

The optimization results for an output voltage of $V_{\text{out}} = 12\,\text{V}$ are shown in **Fig. 2(a)** and indicate that depending on the resonant frequency either litz wire or planar winding can achieve the lowest losses. For frequencies below $f_{\text{res}} < 500\,\text{kHz}$ the lowest losses are reached with litz wire, while above $f_{\text{res}} > 500\,\text{kHz}$ planar windings can attain the lowest losses. In this application with high output currents at $V_{\text{out}} = 12\,\text{V}$, both concepts benefit from paralleling two

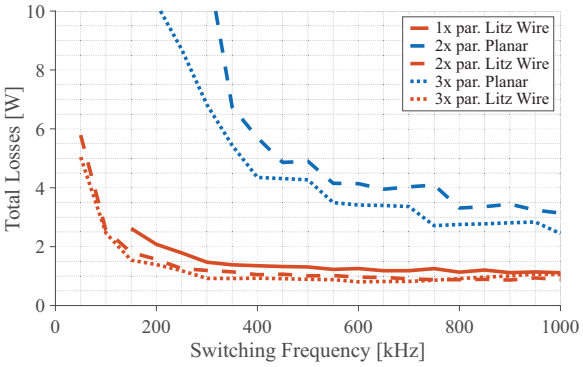

Figure 3 Optimzation results of 3 kW boost inductors (at 50 % load) for planar and litz wire inductors in dependency of the switching frequency.

transformer stages (with individual primary and secondary sides) and preferably use matrix configurations with either 3 or 4 sub-transformers. The results can be explained by the fact, that the winding window filling factor of planar magnetics is typically lower than for litz or round wires, since the maximum copper thickness of a single track is limited and so is also the number of layers. Thus, at low frequencies, where the skin depth is high, the litz wire setup is at an advantage since it can utilize larger strand diameters and achieve higher filling factors. At high frequencies, however, small strand diameters are required which also reduce the filling factor and, moreover, the proximity effect starts to play a more significant role. Here, planar windings in a transformer with co-planar arrangement of the turns can limit the impact on the losses, while litz wires have external (i.e. form neighbouring turns) and inner proximity effects (i.e. from the strands within the same turn).

A very similar picture can be observed for the $V_{\text{out}} = 48\,\text{V}$ transformers, as depicted in **Fig. 2(b)** . The cross-over between the losses of planar and litz wire transformers are again at around $f_{\text{res}} = 500\,\text{kHz}$. Different to 12 V systems, however, is that paralleling does not significantly reduce the total transformer losses anymore. This can be attributed to the fact that the output current is reduced by a factor of four compared to 12 V systems, such that paralleling the converters, which reduces the winding but increases the core losses, has a minor effect.

2.2 PFC Boost Inductor

For the analysis of inductors the case of a boost PFC operated in continous conduction mode (CCM) at an input voltage of $V_{\text{in}} = 230\,\text{V}$ at $f_{\text{g}} = 50\,\text{Hz}$ is selected. The parameters of system power ($P_{\text{out,rat}} = 3\,\text{kW}$), selected operating point (at 50 % load), and magnetic design space are the same as in the transformer analysis. The range of switching frequencies, current ripples, and number of parallel stages is selected as summarized in **Tab. 1**.

The optimization results (cf. **Fig. 3**) show that planar inductors cannot achieve the same level of losses as litz wire inductors. Additionally, at least two PFC stages have to be paralleled before planar inductors can be used, as no so-

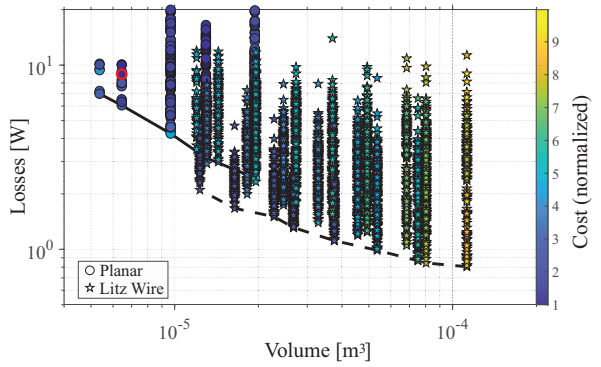

Figure 4 η-ρ Pareto-front of boost PFC inductors for planar (solid line) and litz wire (dashed line) inductors. The costs of all designs are normalized to the value of the cheapest design (red circle).

lution was found for single planar inductors for the given application. Interestingly, the total losses of litz wire inductors remain overall relatively constant with the number of parallel stages as well as with the switching frequency if operated above $f_{sw} = 300\,\text{kHz}$. For planar inductors, however, the losses decrease with increasing switching frequency. The results indicate that the large first harmonic current at f_g poses a challenge for planar inductors and viable solutions in terms of overall system efficiency are found only above around $f_{sw} > 400\,\text{kHz}$ where the losses are still between two to three times higher than for litz wire inductors.

Up to this point, the analysis has focused on the comparison of the losses between the two winding types as a function of operating frequency. By extending the scope to include also the cost and volume dimensions, a more comprehensive view can be obtained, as shown for the case of PFC inductors in **Fig. 4**. Planar inductors are dominating the region of lowest volume, at the expense of higher losses, and vice versa for litz wire inductors. The costs of the inductors have been normalized to the cheapest inductor (red circle) which is a planar inductor.

As a general statement for inductors with (quasi) DC current, one can derive that for lowest volume and/or lowest cost planar inductors should be selected, but for an overall balanced trade-off between cost, volume, and losses litz wire inductors are a better choice. For transformers, however, depending on the operating frequency, planar magnetics can even provide the lowest losses in addition to cost and volume benefits.

3 Server Supply Optimizations

Based on the inductor and transformer investigations of the previous section, full system optimizations of server supplies have been performed and the results are presented in this section.

The trend in data centers towards higher power levels per rack has lead to an increased interest in 48 V distribution rails within the rack. This reduces the distribution losses and/or facilitates the use of smaller profile copper bars. Therefore, in this section not only server power supplies with 12 V output voltage, which are nowadays dominating the market, are considered, but also supplies with 48 V (Range: $43\,\text{V} - 58\,\text{V}$) output are analyzed, both for Si and GaN power semiconductors. The specification of GaN or Si refers to the high-frequency (HF) bridge legs of the totem-pole PFC and the primary side of the LLC. The low-frequency (LF) bridge-leg in the PFC is always Si since it can be optimized for lowest conduction losses while facing negligible switching losses. The capability of GaN to operate in hard-switching allows for a CCM operation of the HF totem-pole switches and, if combined with a larger current ripple by selecting a small inductance value, natural soft-switching is achieved over a wide range of the mains period [8]. In contrast, the Si totem-pole can only be operated with zero-voltage switching (ZVS) and therefore has to be modulated in triangular current mode (TCM).

For a fair and comprehensive analysis, each power supply is optimized with respect to efficiency (η), power density (ρ), and cost (σ), compliant with the specifications listed in **Tab. 2**. The Pareto-optimal designs are identified with a systematic multi-objective optimization procedure by mapping the design space, which contains all design degrees of freedom, into the performance space of efficiency, power density and cost [9, 10]. The considered degrees of freedom are on both system and component level and are covered by sweeping through all possible converter designs, i.e. all combinations of design variables. The performance of each design is calculated with detailed analytical system and component models, which are often multi-physic models considering the electrical, thermal domain, and if applicable also the magnetic domain. For the cost calculations, the employed models are based on [10] with modifications based on commercially available cost tear-downs of industrial data center power supplies. The calculations include also the cooling system (heat sink and fan [11]), PCB, auxiliary supply, control, casing, and the cost of manufacturing. For the calculation of the power density it is assumed that due to non-ideal component placement, the sum of all calculated boxed volumes of the individual components is increased by 20% and some additional volume for the control board and auxiliary supply is included (based on a previous laboratory prototype), and also an increase in volume due to stand-off distances, casing, and IEC C14 connector is taken into account.

After all designs have been evaluated, the Pareto-front (for two performance dimensions) or the Pareto-surface (for

Table 2 Main specifications of investigated server power supplies.

Parameter	Variable	Value
Input Voltage Range	V_{in}	1ϕ, $176\,\text{V} - 265\,\text{V}_{RMS}$
Rated Output Power	$P_{out,rat}$	3 kW
Nominal Output Voltage	V_{out}	12.3 V or 48 V
Hold-up Time	$T_{hold\text{-}up}$	10 ms
EMI Compliance		Class B
Ambient Temperature	T_{amb}	40°

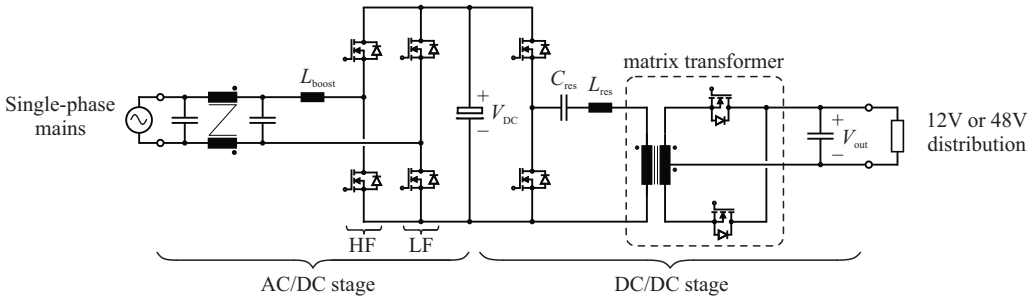

Figure 5 Schematic of a typical single-phase server supply for 12 V or 48 V output voltage. The supply consists of a totem-pole PFC stage and an LLC DC/DC stage which can consist of one or more transformers in matrix configuration.

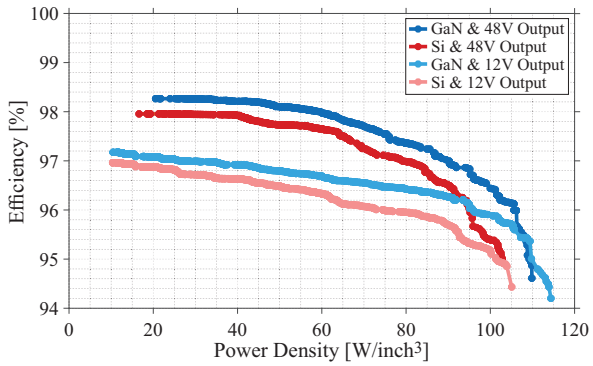

Figure 6 η-ρ Pareto optimization results for 3 kW server supplies (at 50 %) load for output voltages of 12 V and 48 V with either GaN or Si semiconductors.

three or more performance dimensions) can be extracted, which quantifies the achievable performance trade-off between the different dimensions.

The η-ρ (efficiency vs. power density) Pareto fronts for the different power level of 48 V and 12 V are comparatively shown in **Fig. 6**. At an output voltage of 48 V the system level efficiency can reach around 98.3 % with GaN semiconductors at power densities of around 35 W/in^3, whereas systems with Si semiconductors can achieve around 97.9 % at these power densities. The efficiency gap between the two semiconductor technologies tends to increase with higher power densities. This is due to the fact that more power dense designs typically require higher switching frequencies for smaller passive components. This amplifies the advantage given by lower output and gate charges of GaN switches and accordingly lower switching losses.

A reduction of the output voltage level to 12 V and thus a shift to higher output current leads to an efficiency drop of roughly 1 % at state-of-the-art power density levels. Interesting to note is that the maximum power density that can be achieved is less dependent on the output voltage but more on the semiconductor technology. This means, that regardless of output voltage, the maximum power densities with GaN and Si switches are both at around $110-115$ W/in^3 and $100-105$ W/in^3, respectively. Further volume reductions can be achieved by lowering the hold-up time (e.g. to $6-7$ ms) and/or reducing the EMI requirement (e.g. to Class A). The former one could be a viable path forward considering the recent trend of equipping the server racks with batteries, while the latter one is dependent upon the EMI immunity of the other loads connected to the same mains.

A closer inspection of the results in **Fig. 7** reveals the areas where some or all of the considered magnetic components (i.e. transformer, resonant inductor, and PFC inductor) are planar magnetics. The systems with all planar magnetics are positioned in the very high power density region where where however the efficiency already starts to drop significantly. For the 12 V systems it is more advisable to implement both the transformer and the resonant inductor with planar windings but the PFC inductor with litz wire. This enables outstanding power densities above 80 W/in^3 at reasonable efficiencies of around 96 % with GaN semiconductors. In general, also with Si semiconductors planar transformer and even full planar systems can be realized, at around 0.4...0.6 % lower efficiency than comparable GaN designs.

4 Hardware Results

Based on the findings of the previous section, a hardware demonstrator (cf. **Fig. 8(a)**) of an ultra compact DC/DC converter stage (350 W/in^3) for 12 V output voltage is presented in this section. Such a converter with a wide input voltage range will be an essential building block for future high density server supplies.

The specifications of the converter prototype are listed in **Tab. 3**. For high density single-phase server supplies the choice of the DC-link capacitance is an important value, because it not only influences the size of the entire converter but also the input voltage range of the DC/DC converter stage. In order to shrink the DC-link capacitance size for a given hold-up time, the DC/DC stage has to be

Table 3 DC/DC converter design specifications

Parameter	Variable	Value
Output voltage	V_o	12 V
Full-load output power	P_o	3 kW
Full-load output current	I_o	250 A
Nominal input voltage range	$V_{link,nom}$	370 V-430 V
Fault input voltage	$V_{link,fault}$	300 V

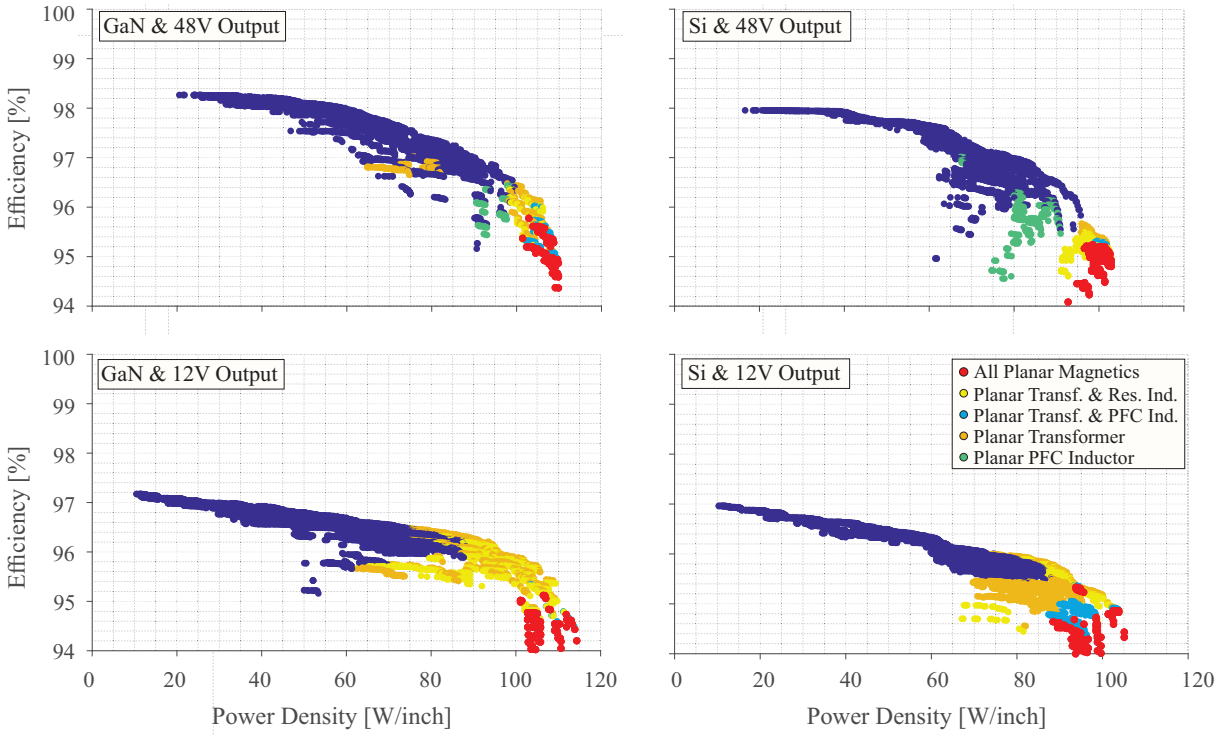

Figure 7 Detailed analysis of the individual Pareto optimization results of **Fig. 6**. The design points with one or more planar magnetic components are highlighted.

capable of working with a very wide input voltage range, i.e. from 300 V to 430 V in the case of the presented prototype, even though the nominal operating range is only from 370 V to 430 V. This poses a challenge for the control concept and the overall system optimization. For such a wide input voltage range the commonly used LLC topology, operated with frequency modulation, and with the design constraints imposed by the gain requirements, might lead to sub-optimal converter designs. Thus, a series resonant converter (cf. **Fig. 8(b)**) with a more flexible modulation scheme with frequency and phase-shift modulation is selected for this prototype ([12]). The choice of operating frequency range is selected to best utilize the employed CoolGaN^{TM}semiconductors and the planar transformer. The optimal frequency range for planar transformers (in matrix configuration) is in the range of 500 kHz and above, as shown in **Fig. 2(a)**, which is also a well suited frequency range for GaN devices due to their lower Q_{oss} and Q_{gate} charges than Si devices. This leads to a modulation scheme as visualized in **Fig. 9(a)**. For the nominal operating range (green shaded area) below around half of the rated power the converter is operated in discontinous conduction mode (DCM) by modulating the phase-shift with a constant switching frequency of $f_{sw} = 700$ kHz. Above that power level the converter enters boundary conduction mode (BCM) by varying both the phase-shift and the switching frequency at the same time. Two measured waveforms for BCM and DCM operation are shown in **Fig. 9(b)** and **Fig. 9(c)**, respectively.

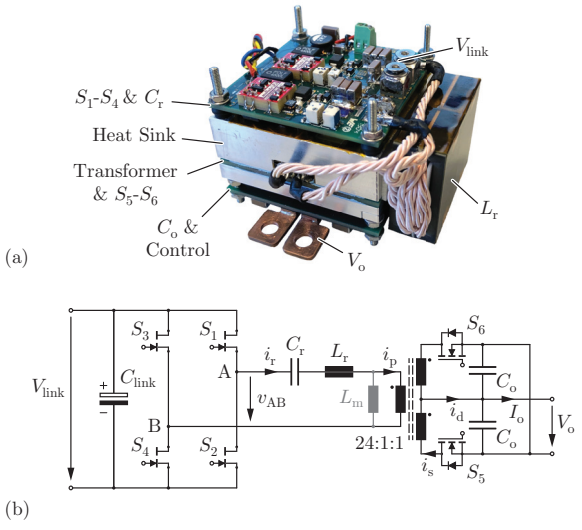

Figure 8 **(a)** Implemented 3 kW hardware prototype of the B/DCM converter, measuring 51 mm x 68 mm x 40 mm (21.6 kW/L, 350 W/in^3). **(b)** Simplified power circuit topology of the current prototype, with the transformer implemented as the snake-core matrix transformer from [7] with 4 parallel-connected synchronous rectifier stages.

For the transformer design of this converter a novel Snake-core matrix transformer has been proposed in [7]. This transformer concept eliminates any possible circulating currents on the parallel connected secondary sides of matrix transformers. For cost and realization reasons a 4-layer PCB with 105 μm copper thickness is selected, which potentially allows to manufacture the transformer on the same power PCB as the PFC stage. Compared to a litz-wire realization, this concept offers several advantages at for high

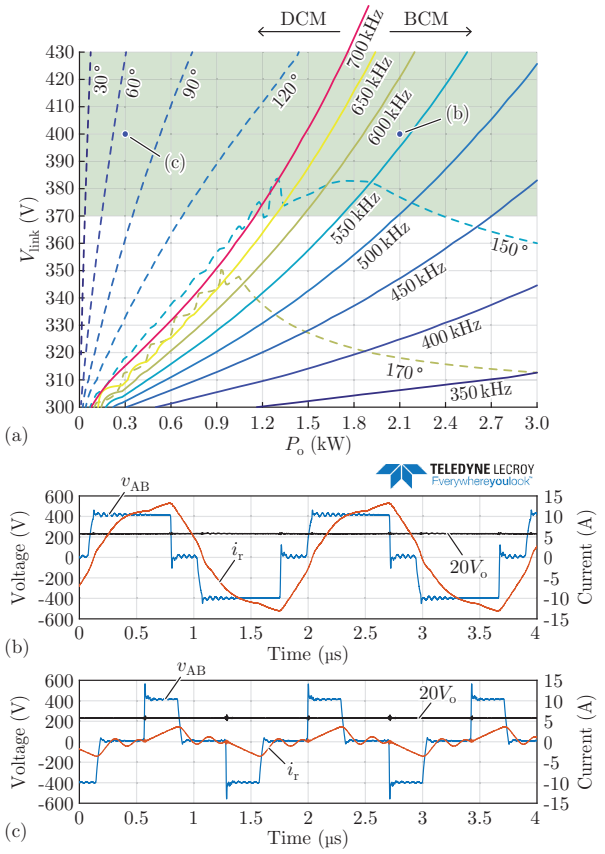

Figure 9 Visualization of converter operating modes in discontinuous conduction mode (DCM) and boundary conduction mode (BCM): (a) Phase-shift and frequency modulation pattern over entire operating range (green area indicates nominal operating range). Measured waveforms of converter operation in (b) BCM and (c) DCM.

density designs:

- Optimal trade-off between losses and volume, as shown in **Fig. 10** due to lower R_{AC} to R_{DC} ratio.
- Reduction of termination losses by assembling the synchronous rectifiers directly on the same PCB as the transformer winding.
- Enhanced thermal management due to larger surface-to-volume ratio.
- Reduction of potential circulating currents within litz wire strands due to imperfect twisting especially on the single-turn secondary sides with short wire lengths [13].
- Cost reduction by automatization of PCB assembly.

The AC-resistance of the snake-core transformer windings has been measured with an impedance analyzer and the results of **Fig. 11** show an increase of resistance for the switching frequencies encountered during nominal operation compared to the DC-resistance of about +27 % to +62 %. This is higher than predicted by the PEEC simulation but can be mainly explained by the transformer termination where the tracks are routed horizontally to

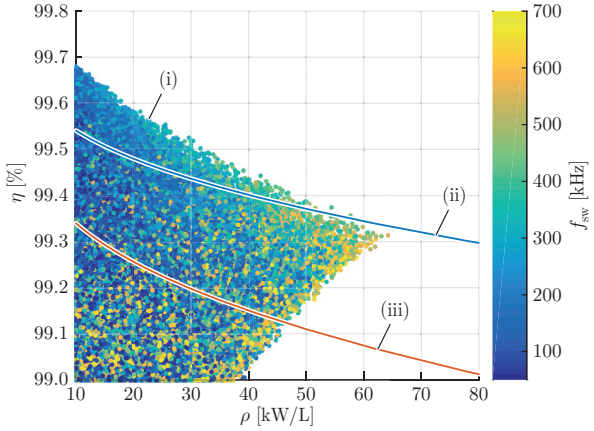

Figure 10 η-ρ Pareto-front analysis of litz-wire and 4-layer planar transformer designs. Litz-wire designs (i) are thermally limited at power densities above 65 kW/L whereas planar designs with 105 µm copper thickness (iii) achieve higher power densities at the cost of lower efficiencies, as the larger transformer surface of planar magnetics allows for enhanced thermal management. Increasing the secondary-winding copper thickness to 210 µm (ii) allows to extend the Pareto-front of the planar transformer design and outperform litz-wire designs in efficiency at power densities above 55 kW/L.

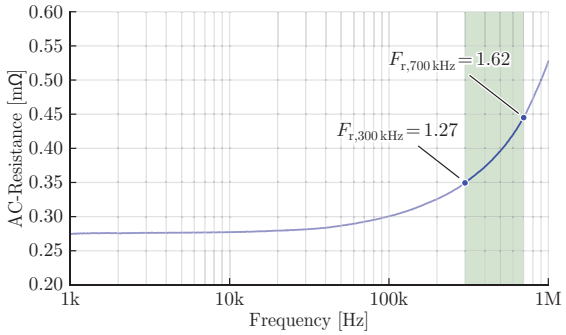

Figure 11 Snake-core transformer [7] AC-resistance measured from the primary side with secondary-side windings short-circuited. The transformer windings are built in a 4-layer PCB with 105 µm of copper thickness. The frequency operating range is highlighted in green, where for the lowest $f_{sw} = 300$ kHz and highest $f_{sw} = 700$ kHz, the correspondent AC-to-DC resistance ratios ($F_r = R_{ac}/R_{dc}$) are pointed.

each other instead of co-planar, which would lead to lower losses.

5 Conclusions and Outlook

The market introduction of GaN HEMTs with superior Figure-of-Merit has opened up the possibility to increase the switching frequency of power converters. This enables the use of planar magnetics which show a superior performance compared to standard litz wire based magnetics in the case of transformers for frequencies above

500 kHz. For the application as inductor with large (quasi)-DC current component, litz wire magnetics are the preferred choice for lowest losses, but planar magnetics allow for highest power density and lowest cost. For the realization of server power supplies with very high power density, the system level analysis shows that especially for 12 V output voltage the implementation of a planar transformer with a planar resonant inductor in combination with GaN power semiconductors is the most promising combination. In a second step, for even higher power densities and/or cost reduction, the PFC inductor might also be realized as a planar magnetic component.

For a complete SMD assembly of the entire power supply in the future it will also be necessary to implement the EMI filter with planar magnetics, which should be analyzed in-depth in a future work. In addition, the analysis of this paper can also be extend to coupled inductors and/or more complex magnetic structures where the resonant inductor and the transformer are integrated into a single magnetic component.

6 Literature

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