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Analysis and Design of Fixed Voltage Transfer Ratio DC/DC Converter Cells for Phase-Modular Solid-State Transformers

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***Abstract*—Many Solid-State Transformer (SST) concepts employ cascaded AC/DC converter cells to handle the comparatively high medium-voltage (MV) grid voltages, resulting in a phase-modular structure. Accordingly, each cell—formed by an AC/DC input stage and an isolated DC/DC output stage—processes a power fluctuating with twice the grid frequency. The series resonant converter (SRC) operated in the half-cycle discontinuous-conduction-mode (HC-DCM) is a highly attractive choice for the isolated DC/DC converter because of its high efficiency. However, this converter does not offer any control possibilities; instead, it couples the two DC voltages through certain dynamics with fixed voltage transfer ratio. This leads to a propagation of the input side power fluctuations through the SRC to the common LV bus, which has certain consequences on the converter design. The paper therefore re-derives a dynamic model of the SRC's terminal behavior in a generic way, which also covers the case of comparatively small DC link capacitors. The experimentally verified dynamic model is then used to discuss and optimize the choice of the input and output side capacitances of the DC/DC converter cell with respect to the placement of the converter's system level resonances, such as to obtain minimum volume and losses. Finally, aspects related to the design of a scaled demonstrator system featuring similar dynamic behavior as the full-scale system are addressed and first measurement results are presented.**

I. Introduction

The roots of the Solid-State Transformer (SST) concept can be traced back to the 1970s [1], however, only on the basis of more recent developments in power semiconductors and other component technologies it has started to attract significant interest from both, research and industry. SSTs are nowadays envisioned as an enabling technology for lightweight and efficient traction solutions [2]–[5], and for Smart Grid applications [6]–[10], especially for the coupling of DC microgrids to an AC distribution system.

While direct matrix-type AC-DC-AC converter structures have been discussed in literature, the majority of all proposed SST concepts relies on a modular approach to handle high grid voltages on the medium voltage (MV) side. Cascading several converter cells, each consisting of an active rectifier unit (ARU) and a series connected isolated DC/DC converter with fixed voltage transfer ratio, allows to generate a filter-friendly multilevel output waveform; furthermore, using an input-series, output-parallel (ISOP) configuration of the cells (cf. **Fig. 1a**) contributes significantly to the overall voltage scaling between MV and low-voltage (LV) side.

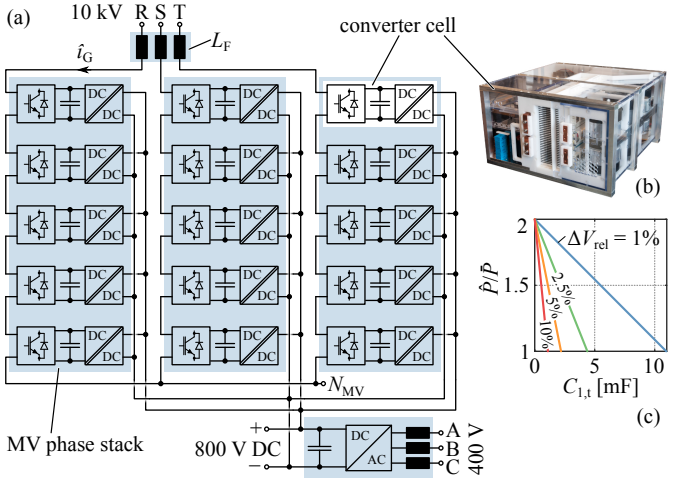

Fig. 1. (a) Topology of the considered AC/AC SST; (b) protoype of a 80 kW converter cell (cf. **Fig. 3a** for the power circuit schematic); (c) trade-off between MV side capacitance and ripple of the power processed by the DC/DC converter.

TABLE I. Main parameters of the SST and the converter cell.

Rated SST power	1 MVA	LV DC voltage	800 V
Rated cell power	83.3 kW	Turns ratio, n	11 : 8
ARU sw. freq., $f_{s,i}$	1 kHz	MV DC cap., $C_{1,t}$	660 µF
DC/DC sw. freq., $f_{s,d}$	7.4 kHz	LV DC cap., C_2	140 µF
Zero-current interval, T_z	12.8 µs	Stray ind., L_{sigma}	9 µH
MV DC voltage (per cell)	2.2 kV	Resonant cap., C_r,	79 µF

However, such designs are phase-modular on the MV side, meaning that they consist of three individual single-phase systems. Assuming the phase angle between grid voltage and current, φ, to be zero, neglecting the ARU switching, denoting the modulation index with M, and the MV DC link voltage with V_{MV}, the input power of one cell is given by $p(t) = 0.5\hat{i}_G M V_{MV} \cdot (1 - \cos(2\omega_G t))$.

This single-phase power ripple at twice the grid frequency could be propagated through the cells' DC/DC converters to the low-voltage (LV) side, where the instantaneous power contributions of the three MV phases ideally add up to a

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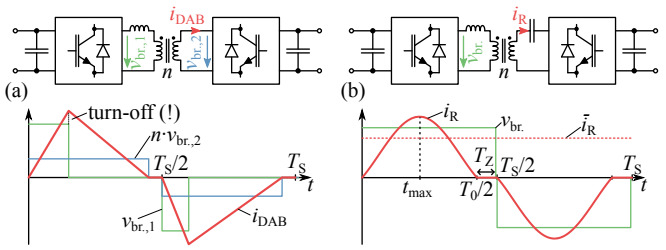

Fig. 2. (a) Basic operating principle of a DAB with triangular current mode [11], [12]; and (b) as HC-DCM series resonant converter.

constant value. Doing so allows to reduce the capacitance on the cell's MV side as illustrated by **Fig. 1c**, but on the other hand increases the losses in the DC/DC converter due to increased rms currents.

A. Realization as Triangular Current Dual Active Bridge

If the DC/DC converter is realized as a Dual Active Bridge (DAB) (cf. **Fig. 2a**), an arbitrary choice in the aforementioned trade-off can be made by suitable control of the power flow in the DC/DC converter. On the other hand, e. g., a triangular current modulation scheme of a DAB inevitably involves turning off the peak transformer current (cf. **Fig. 2a**) [11], [12], which causes high switching losses if heavy duty silicon power devices are used, and hence is contrary to achieving a high efficiency.

B. Realization as DAB HC-DCM Series Resonant Converter

From the large family of resonant converters [13], especially the SRC operated in the half-cycle discontinuous-conduction-mode (HC-DCM), is of high interest for high-power applications, since it provides ZCS for all switching transitions (cf. **Fig. 2b**). This operating mode has been described first in the early 1970s for thyristor switches [14], [15]. Since the turn of the millennium the concept has been applied also to higher power ranges, specifically in SST systems for traction applications [2], [4], [5], [16], [17]. Several publications deal with the modeling of the switching losses that arise despite having ZCS as a result of the stored-charge dynamics of silicon IGBTs [16], [18], [19], and the optimization of the converter with respect to efficiency and power density [20], illustrating very high efficiencies of around 99 % in pure DC/DC applications.

Fig. 3a shows the power circuit of an SST cell with the SRC highlighted, and **Fig. 2b** shows the key SRC waveforms. For power transfer from the MV to the LV side, the MV side bridge is applying a 50 % duty cycle voltage to the resonant tank, which consists of the transformer's stray inductance, L_σ, and a resonant capacitor, C_r, while the LV side bridge operates passively as a diode rectifier, preventing the current from crossing zero. The resulting zero-current interval, T_z, can be increased to reduce switching losses by allowing for the stored charges in the IGBTs to (partly) recombine prior to the actual switching, however, at the expense of a higher rms current, $\tilde{i}_\mathrm{R}$, such that a T_z resulting in minimum losses can be found [16], [20].

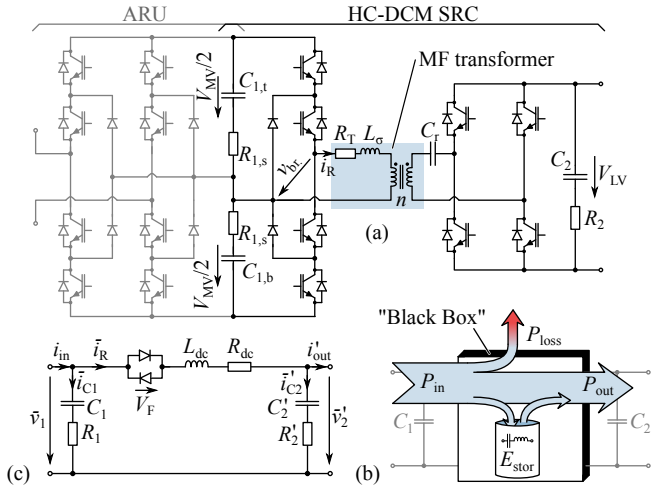

Fig. 3. (a) SST cell power circuit consisting of an active rectification unit (ARU) and a HC-DCM SRC; (b) energy- and loss-based modeling concept visualization; (c) resulting MV-referred dynamic equivalent circuit.

The amplitude of the current pulse is given by the exciting voltage step, which is in steady state defined by the voltage difference of the two DC voltages (referred to the same side of the transformer). Basically, when a load increase creates a voltage sag in the load-side DC bus, the exciting voltage increases, leading to higher peak currents and hence to an increase of the power transfer through the converter. Thus, the power flow through the converter adjusts automatically such that the (transformed) DC voltages on either side stay equal (except for some deviation due to losses). The reader is referred to the literature (e. g., [20], [21]) for a more detailed description of the converter's operating principle.

Note that there is no control possibility; the system basically acts as a "DC transformer" with a certain dynamic behavior, which leads to a number of consequences regarding the design and operation of SST converter cells based on the HC-DCM SRC, which will be addressed in the following.

II. Dynamic Model of the HC-DCM SRC

In order to better understand the dynamics of the HC-DCM SRC, and also for facilitating the design of the DC link capacitors, etc. (cf. Section IV), a non-switching model that accurately mimics the converter's terminal behavior is beneficial. A common approach to obtain such a model consists of averaging currents and voltages over a switching period (or half a switching period, for that matter), i. e., the current flowing in the model is the local average current, $\bar{i}_\mathrm{R}$, of the real converter current, i_R (cf. **Fig. 2b**). Such an equivalent circuit capturing the converter dynamics with respect to its terminal voltages and currents has been proposed already in 1990 [22], [23] (in German) for sinusoidal currents (cf. **Fig. 4a**), and was then refined later [2], [17] (both in German) (cf. **Fig. 3c**), considering piece-wise sinusoidal currents (cf. **Fig. 4b**).

In the following, the equivalent circuit will be re-derived in a generic way using a power- and energy-based approach, which yields the known results for the two mentioned cases.

In addition, here the validity is extended to the case of small DC link capacitors, where the current shape deviates from a pure sine [21], which is then verified with measurements of a full-scale SST converter cell.

A. Dynamic Model Derivation

Generally, a given amount of power transfer through the converter is associated with certain losses and a certain amount of stored energy in the SRC's resonant tank (cf. **Fig. 3b**). In order to yield the same terminal behavior as the real converter, an equivalent model must correctly capture these two phenomena, i. e., losses and stored energy in the system as functions of the transferred power must be equal. In the following, this generic conditions are used to re-derive the dynamic equivalent circuit [2] shown in **Fig. 3c**, whereby all quantities are referred to the MV side.

1) Half-Bridge to Full-Bridge Transformation: In the considered example SST converter cell, the MV side topology is a half-bridge structure, whereas the LV side topology is a full-bridge (cf. **Fig. 3a**). This combination yields a factor of two in the voltage gain, allowing for a lower turns-ratio of the medium-frequency transformer. To model this in the equivalent circuit, the following transformation is carried out,

$$\overline{v}_1 = V_{\mathrm{MV}}/2, \quad C_1 = 2C_{1,\mathrm{t}}, \quad \text{and } R_1 = 1/4 \cdot R_{1,\mathrm{t}}, \tag{1}$$

resulting in equal stored energy and losses in the MV DC link assembly.

2) Losses: The major share of the load-dependent losses occurs in the power semiconductors, which are modeled as a constant voltage drop, v_0, and an on-state resistance, r_{on}, as well as in the transformer windings, R_{T}.

Losses resulting from v_0 depend on the average current through the semiconductors. Since the local average current, $\overline{i}_{\mathrm{R}}$, is flowing in the equivalent circuit (cf. **Fig. 3**), these losses can be represented by anti-parallel diodes with an equivalent voltage drop, V_{F}, corresponding to the sum of the voltage drops of the semiconductors in the current path,

$$\overline{i}_{\mathrm{R}} V_{\mathrm{F}} \overset{!}{=} \overline{i}_{\mathrm{R}}(2v_{0,1} + 2v'_{0,2}) \quad \Rightarrow \; V_{\mathrm{F}} = 2v_{0,1} + 2v'_{0,2}, \tag{2}$$

where $v_{0,1}$ and $v_{0,2}$ denote the constant part of the voltage drops of the conducting semiconductors on either side of the transformer. Note that these values might change depending on the power flow direction (diode vs. IGBT).

On the other hand, losses resulting from the series resistances depend on the rms current. Therefore, the equivalent resistance, R_{dc}, that only sees the average current, needs to be adapted,

$$\overline{i}_{\mathrm{R}}^2 R_{\mathrm{dc}} \overset{!}{=} \tilde{i}_{\mathrm{R}}^2 R_{\mathrm{total}} \quad \Rightarrow \; R_{\mathrm{dc}} = \frac{\tilde{i}_{\mathrm{R}}^2}{\overline{i}_{\mathrm{R}}^2} R_{\mathrm{total}} = \beta^2 R_{\mathrm{total}}, \tag{3}$$

where R_{total} is the sum of all series resistances in the current path (R_{T}, r_{on} of conducting semiconductors, etc.).

Series resistances of the DC link capacitors can directly be inserted into the equivalent model; they retain their effect on the terminal currents, however, in reality they would also see the resonant current (i. e., its rms value), not only its average value. To account for this, R_{dc} needs to be adapted [2]:

$$R_{\mathrm{dc}} = \beta^2 R_{\mathrm{total}} + (\beta^2 - 1)(R_1 + R'_2). \tag{4}$$

In the DCM operating mode, switching and core losses do not depend strongly on the transferred power, and therefore do not contribute to the converter dynamics. It would be possible to model them as shunt resistors in the equivalent circuit, though.

3) Stored Energy: The energy stored in the resonant tank, E_{stor}, depends on the transferred power,

$$E_{\mathrm{stor}} = \frac{1}{2} L_\sigma \hat{i}_{\mathrm{R}}^2 \quad \left(= \frac{1}{2} C_{\mathrm{r}} \hat{v}_{\mathrm{Cr}}^2 \right). \tag{5}$$

Since the equivalent model is based on the average resonant current, an inductor, L_{dc}, is used to model the current-dependency of the stored energy,

$$\overline{i}_{\mathrm{R}}^2 L_{\mathrm{dc}} \overset{!}{=} \hat{i}_{\mathrm{R}}^2 L_{\mathrm{sigma}} \quad \Rightarrow \; L_{\mathrm{dc}} = \frac{\hat{i}_{\mathrm{R}}^2}{\overline{i}_{\mathrm{R}}^2} L_\sigma = \alpha^2 L_\sigma. \tag{6}$$

4) Summary: The elements of an equivalent circuit according to **Fig. 3c** can directly be calculated, for arbitrary waveform shapes, by means of the two ratios

$$\alpha := \frac{\hat{i}_{\mathrm{R}}}{\overline{i}_{\mathrm{R}}} \quad \text{and} \quad \beta := \frac{\tilde{i}_{\mathrm{R}}}{\overline{i}_{\mathrm{R}}}. \tag{7}$$

Fig. 4a and **b** show the resulting values for the case of (piece-wise) sinusoidal current, as derived earlier in [22] and [2], respectively. For the case of piece-wise sinusoidal current we have

$$\alpha = \frac{\pi}{2} \frac{f_0}{f_{\mathrm{s}}} \quad \text{and} \quad \beta^2 = \frac{\pi^2}{8} \frac{f_0}{f_{\mathrm{s}}}, \tag{8}$$

where f_{s} denotes the switching frequency and f_0 the resonant frequency of the pulse, which is linked to the zero-current interval duration, T_{z}, as $f_0 = 1/2 \cdot (1/(2f_{\mathrm{s}}) - T_{\mathrm{z}})^{-1}$.

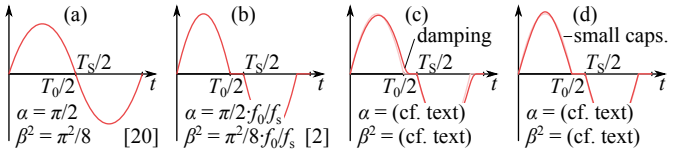

Fig. 4. SRC current shapes: (a) pure sinusoidal current; (b) piece-wise sinusoidal current; (c) effect of damping; (d) deviation caused by small DC capacitors.

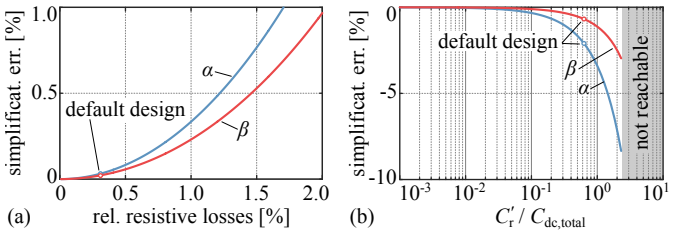

Fig. 5. Deviation of the simplified α and β (cf. **Fig. 4b**) from the correct calculation for (a) the influence of damping on the waveform (cf. **Fig. 4c**), and (b) for the case of small DC capacitors with $C_{\mathrm{dc,tot.}} := C_1 C'_2/(C_1 + C'_2)$ (cf. **Fig. 4d**).

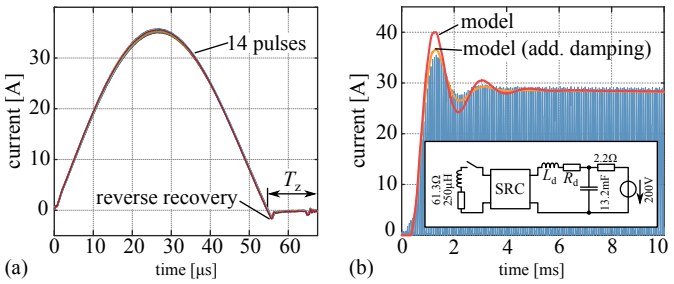

Fig. 6. (a) Measured resonant pulses used to determine α and β; (b) measured step response compared with results from the dynamic model.

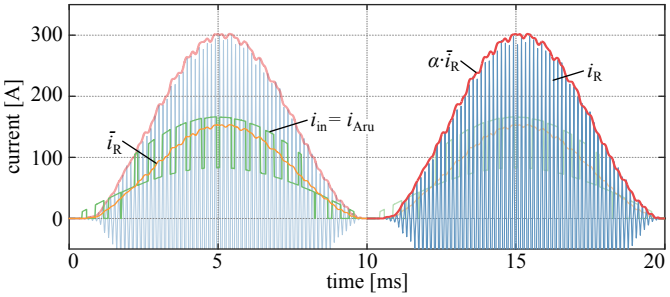

Fig. 7. Simulated waveforms of the circuits shown in **Fig. 3a** and **b** for pure active power transfer from the grid.

TABLE II. VERIFICATION FOR SMALL DC LINK CAPACITORS.

	Calc. (11)	Measured	Meas. w/o RR	Simpl. cal. (8)
α	1.971	1.991 (−1.7 %)	1.984 (−0.7 %)	1.938
β	1.240	1.248 (−0.6 %)	1.243 (−0.2 %)	1.234

5) Damping Distortion: In reality, the series damping in the resonant circuit causes a deviation from the purely sinusoidal shape, as is indicated in **Fig. 4c**. While it is still possible to find an analytic expression for α and β, it is omitted here because **Fig. 5a** illustrates that the deviation from the idealized values remains below $0.5\,\%$ as long as rms losses stay below $1\,\%$, which is generally desired for reasons of system efficiency.

B. α and β for Small DC Link Capacitors

The current shape also deviates from a sinusoid if the DC link capacitors are chosen to be comparatively small with respect to the resonant capacitor, C_r, as is illustrated in **Fig. 4d** [21]. **Fig. 5b** shows that the error introduced by not considering this effect can be quite high.

Starting from the normalized current shape in that case,

$$\begin{aligned} i_\mathrm{R}(t) &= A\sin(\omega_0 t) + B(1-\cos(\omega_0 t)), \text{ where} \\ \omega_0 &= \sqrt{\frac{C_{1,\mathrm{t}}C_2' + C_{1,\mathrm{t}}C_\mathrm{r}' + C_2'C_\mathrm{r}'}{C_{1,\mathrm{t}}C_\mathrm{r}'C_2'L_\sigma}}, \\ A &= \frac{1}{\omega_0 L_\sigma}\left(\frac{1/2\cdot T_\mathrm{s}+T_\mathrm{Z}}{2C_{1,\mathrm{t}}} + \frac{T_\mathrm{S}}{2C_\mathrm{r}'} + \frac{T_\mathrm{Z}}{C_2'}\right), \text{ and} \\ B &= \frac{2}{\omega_0^2 L_\sigma}\left(\frac{1}{C_2'} + \frac{1}{2C_{1,\mathrm{t}}}\right), \end{aligned} \tag{9}$$

first the required resonant capacitor, C_r', for a desired T_z needs to be calculated by solving

$$\left(\frac{T_\mathrm{s}}{2} - T_\mathrm{z}\right) - \frac{2\pi - 2\arctan\left(A(C_\mathrm{r}')/B\right)}{\omega_0(C_\mathrm{r}')} \stackrel{!}{=} 0, \tag{10}$$

which is only possible numerically because both, A and ω_0, are functions of C_r'. For an in-detail discussion of the derivation of the current shape, etc., the reader is referred to an earlier publication [21]. Now that T_z and C_r' are matching, α and β can be found as

$$\begin{aligned} \alpha &= \frac{\omega_0\left(A^2+B^2+B\sqrt{A^2+B^2}\right)}{2f_\mathrm{S}\sqrt{A^2+B^2}\,(BE+\pi B+2A)}, \text{ and} \\ \beta^2 &= \frac{\omega_0\left((A^2+3B^2)E + A^2\pi + 3B^2\pi + 6AB\right)}{4f_\mathrm{S}\,(BE+B\pi+2A)^2}, \\ &\text{with } E = \arctan\left(\frac{2AB}{A^2-B^2}\right) \text{ and } A > B. \end{aligned} \tag{11}$$

Note that the expressions in (11) become equal to those in (8) for $C_{1,\mathrm{t}},\ C_2' \to \infty$.

C. Experimental Verification

Using the prototype SST converter cell (cf. **Fig. 1b**) with the specifications detailed in **Tab. I** and the topology shown in **Fig. 3a**, the validity of the above derivation can be evaluated. Thus, **Fig. 6a** shows several measured current pulses plotted on top of each other. From each individual measurement, α and β are extracted and then averaged to improve accuracy. **Tab. II** shows the corresponding results, where the deviation of the calculated from the measured values is given in brackets. The waveforms clearly show the effect of diode reverse recovery, which leads to a negative contribution to the local average value of the current pulse, which in turn needs to be compensated by a higher peak current for a given power transfer. Both effects increase the α of the measured waveform—setting the measured current to zero after its first zero crossing during post-processing results in α and β values that match even better with the calculation. In any case, α and β calculated assuming a piece-wise sinusoidal current, i. e., with (8), clearly deviate from the measurements, as was to be expected considering **Fig. 5b**.

Furthermore, **Fig. 6b** compares a measured step response of the SST cell prototype and the prediction obtained from a simulation of the equivalent circuit in order to illustrate the model's capability of accurately describing the SRC converter's dynamic behavior. Note that the voltage and power levels are reduced from the nominal values in order to facilitate these measurements. The measurement circuit uses the converter cell's ARU switches to turn-on an RL-load, and a large capacitor on the LV DC side to exclude influences of the supplies' current limiter. L_d serves as a decoupling inductor

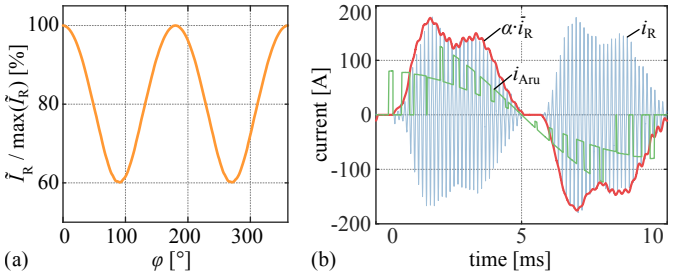

Fig. 8. (a) Relative $\tilde{I}_R$ for various grid current phase angles; (b) simulated example for $\varphi = 90°$ (note that $\alpha \tilde{i}_R < 0$ corresponds to reversed power flow).

to prevent a spreading of the SRC's switching harmonics (cf. Section IV), and R_d models its series resistance (specifically, an external coreless 17.9 µF inductor with a high R_d of 35 mΩ is used). It can be noticed that the damping of the real system is higher than that of the model, which could be explained (cf. orange curve) by the presence of about 25 mΩ of additional series resistance in the LV DC side connections (cabling, contacts, etc.). Obviously, in a direct comparison of the equivalent circuit and a switched simulation model, where all component values are precisely known, almost perfect agreement can be achieved (cf. also **Figs. 7** and **8b**).

III. The HC-DCM SRC in Three-Phase SST Cells

As described in Section II, the HC-DCM SRC couples the MV and the LV DC link voltage tightly but passively with certain dynamics. There is no control possibility and the power transfer is mainly determined by the difference of the two DC voltages. As indicated above, the power contributions of the three MV phases ideally add up to a constant value at the common LV DC bus, which means that, assuming system-wide power balance and neglecting switching frequency components, this LV DC voltage is constant, whereas the MV side voltage inevitably shows a ripple at twice the grid frequency for finite capacitances. Therefore, the full power ripple is transferred through each DC/DC converter cell (cf. **Fig. 7**), increasing the maximum peak transformer current, $\hat{I}_R$, by a factor of 2, and the rms current (considering a whole grid period), $\tilde{I}_R$, by a factor of $\sqrt{3/2} = 1.225$ with respect to constant transmission of the average power.

An important aspect is the behavior in the case of reactive power compensation on the MV side: essentially, reactive power compensation is shifting instantaneous power between the MV phases, which, in a phase-modular SST, means through the DC/DC converters and via the LV side DC link. **Fig. 8a** shows $\tilde{I}_R$ as a function of the grid current phase angle, φ, assuming a constant grid current amplitude. Even at $\varphi = \pm 90°$, $\tilde{I}_R$ still amounts to 60 % of its value for full active power transfer. The simulated waveforms from **Fig. 8b** illustrate that the power flow direction alternates with twice the grid frequency. On the other hand, there is no basic need to provide sufficient capacitance on the MV side to buffer the full power ripple (cf. **Fig. 1c**), thereby trading capacitor volume against losses. As an aside, note that the control unit needs to change the actively switched bridge (i. e., MV or LV side) twice per grid period according to the power flow direction. To do so, the low-pass filtered DC voltages (to remove switching-frequency components), $V_{MV}/2$ and V'_{LV} (cf. **Fig. 3a**), are compared and the bridge with the higher voltage is actively switched.

In the following, three approaches to cope with and/or to mitigate the power ripple transmission through the HC-DCM SRC cells in phase-modular SSTs are discussed and compared.

A. Adapted Design

For the case of constant transfer of the average power, i. e., without any grid-frequency power fluctuation, the solid curves (index $_{...,A}$) in **Fig. 9a** show the dependence of loss components in the SRC on the zero-current interval duration, T_z; the mentioned optimum being clearly visible. The switching losses arising in IGBTs even under ZCS conditions due to the stored charge dynamics are estimated using the stored charge model introduced in [19], [20]. Conduction losses are modeled based on datasheet information for 150 A/1700 V silicon IGBT modules on the MV side and 200 A/1200 A devices on the LV side. Transformer core losses are calculated, transformer winding losses are obtained using AC resistance measurements of a fully rated prototype transformer.

The dotted curves (index $_{...,NC}$) indicate the corresponding losses for full propagation of the power fluctuation through the SRC. Whereas the switching losses do not change because they are proportional to the peak currents and therefore average out to the same value over a grid period, rms-related losses in the transformer winding and also in the power semiconductors increase considerably; note that the optimum T_z therefore becomes shorter.

Recalling that the peak current increases by a factor of 2 for pulsating power transfer, clearly the power semiconductor modules must be upgraded such that the peak currents remain below their ratings, i. e., in the case at hand an upgrade to 300 A/1700 V and 450 A/1200 A types is required. The dashed curves (index $_{...,US}$) in **Fig. 9a** show the resulting losses, which in case of upgrading are in total more or less the same as in the case of averaged power transfer, since the reduction of semiconductor conduction losses overcompensates the increased transformer copper losses. Of course, it would also be possible to additionally also adapt the transformer design in order to accommodate more copper cross section for the windings, but it is not necessary to retain the initial efficiency.

B. Absorption Circuit

An option to achieve again averaged power transfer through the HC-DCM SRC consists of connecting an absorption circuit in parallel to the MV side DC link (cf. **Fig. 9b**), as it is known from traction applications. This resonant circuit can be tuned to twice the grid frequency, thus providing a shunt path for the corresponding power fluctuation. The elements L_a and C_a are related via $2\omega_G = 1/\sqrt{L_a C_a}$, but their ratio can be varied to optimize different targets as is illustrated in the figure. Capacitor volume and mass are modeled assuming a constant energy

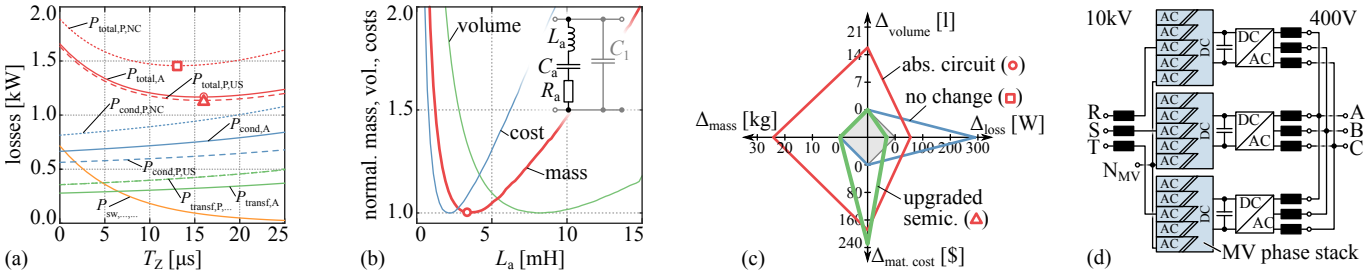

Fig. 9. (a) Converter losses for average and pulsating power transfer (cf. **Tab. I** for specifications); (b) optimization of the absorption circuit; (c) comparison of the two approaches; (d) overview schematic of a fully phase-modular SST system.

density of $6.33\,\mathrm{cm^3/Ws}$ (found from averaging datasheet values of film capacitors from different manufacturers). For each L_a value, an inductor is locally optimized by sweeping over a wide range of core and winding geometries, considering laminated steel cores and solid copper conductors, the minimum volume design for each inductance value is then used.

However, as can be seen from the comparison shown in **Fig. 9c**, where material costs are estimated using [24], the absorption circuit approach is not competitive and hence not considered further, since it contributes additional mass and volume (consider here also that the SST consists of 15 cells in total!), while not reducing costs nor losses when compared to simply upgrading the power semiconductors as described before.

C. Full Phase Modularity

The main reason for the complete transmission of the power ripple through the HC-DCM SRC is that the LV side DC voltage is constant because of the three-phase power being constant, as has been pointed out earlier. By changing the overall SST structure to a fully phase-modular variant, as is shown in **Fig. 9d** (note that then one of these phase assemblies corresponds to a traction application), the LV side DC link voltages are not necessarily constant anymore, they can also vary at twice the MV grid frequency. It can be shown that the amount of transferred power ripple then depends mainly on the ratio between the MV side capacitance and the effective LV side capacitance (which is a combination of the cell's own capacitance and the common inverter capacitance). While in the case of full phase-modularity there is thus at least the option to influence (not control!) the share of the power ripple propagated through the DC/DC converter, it suffers from other shortcomings: Besides the comparatively high price in terms of capacitance requirements to gain (limited) influence on power ripple propagation, the main disadvantage is the more complicated and less efficient symmetrization of asymmetric loading on the LV side grid towards the MV grid because there is no common LV DC link.

D. Conclusion

All in all, the above considerations show that the transmission of the full single-phase power ripple through the DC/DC converter cannot be avoided in a feasible way when a HC-DCM SRC is employed, but on the other hand can be handled without compromising the high efficiency, provided a simple upgrade of the power semiconductors is carried out.

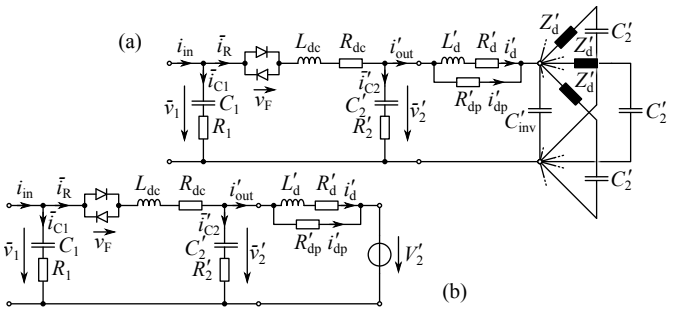

Fig. 10. Equivalent circuits of an SST cell, with (a) including a model of the LV side DC bus assembly including the other converter cells, and (b) with simplification $C_{inv} \to \infty$.

IV. Design Considerations

Thus, the HC-DCM SRC is well suited for application in the converter cells of phase-modular SSTs. In this section, some design aspects are explored based on the derived dynamic equivalent circuit.

A. Analysis Based on Transfer Functions

So far it is clear that the converter design must be able to handle transmission of the power ripple at twice the grid frequency, which has some implications on the proper choice of the DC link capacitors in addition to voltage ripple considerations alone. Starting from the dynamic equivalent circuit introduced above, **Fig. 10a** and **b** show extended versions that include additional parts of the overall SST, namely a decoupling inductor, L_d, a damping resistor, R_{dp}, the common LV inverter DC link capacitor, C_{inv}, and the other converter cells' LV sides. The LV side busbar assembly interconnecting the cells and the inverter stage inevitably features parasitic inductances, which can easily be in the order of magnitude of several hundred nH, creating a parasitic resonance with the DC link capacitors. Providing a dedicated decoupling inductor in each cell prevents the propagation of high-frequency currents across the busbar assembly and offers an additional degree of freedom to place the resonances of the converter dynamics such as not to coincide with, e. g., the switching frequency harmonics.

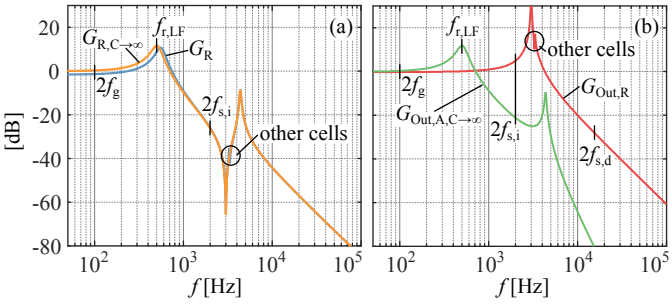

Fig. 11. Key transfer functions of the equivalent circuits shown in Fig. 10. Note that the R'_{dp} damping is chosen very low in order to highlight the resonances caused by the other cells' DC link assemblies.

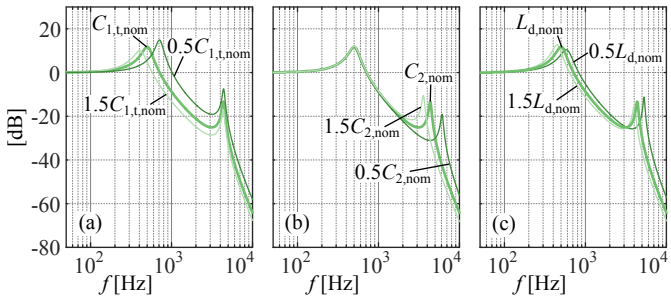

Fig. 12. Influence of the main parameters on the transfer function $G_{\mathrm{Out,A,C}\to\infty}$: (a) MV capacitor, $C_{1,t}$; (b) LV capacitor, C_2; and (c) decoupling inductor, L_d.

In essence, the HC-DCM SRC couples the two DC links through a multi-resonant network. The corresponding transfer functions can be calculated analytically, but the expressions become very complicated. Therefore, **Fig. 11** shows the magnitudes of the transfer functions $G_R = \bar{i}_R/i_{in}$, $G_{R,C\to\infty}$, and $G_{\mathrm{Out,A,C}\to\infty} = i_{out}/i_{in}$, the latter two assuming an infinite C_{inv} (cf. **Fig. 10b**). This assumption is required at $2f_g$ anyway as discussed earlier (no voltage ripple in the LV DC voltage at $2f_g$, i. e. "infinite capacitance", since the contributions of the three MV phases add up to zero), but does also not affect the high-frequency region of the transfer functions, as can be seen from the figure; although the minor parasitic resonance caused by the presence of the other cells is then neglected.

Note that since damping corresponds to losses, the system resonances shown in **Fig. 11** are as lightly damped as possible in the interest of high efficiency, making it mandatory to carefully choose their locations in the frequency spectrum in order to prevent them from being excited by harmonics of the processed currents. The input current to the DC/DC converter consists, apart from its DC component, of major AC components at $2f_g$, but resulting from the interleaved switching of the ARU stage's two bridge legs (cf. **Fig. 7**), also at $2f_{s,i}$, where $f_{s,i}$ is the ARU switching frequency. To avoid excess current stress in the DC/DC converter, it is essential to place the low-frequency resonance of G_R at $f_{r,LF}$, which is mainly given by C_1 and the sum of L_{dc} and L_d (cf. also **Fig. 12a**, and eq. (12)), such that the gain is close to 0 dB at $2f_g$, and clearly negative at $2f_{s,i}$. It should be highlighted that this implies an upper limit for C_1 (or for $C_{1,t}$, respectively), unless it would be chosen large enough to move the resonance sufficiently below $2f_g$, which is not possible with realistic capacitor values. Note that L_d can be used as a second degree of freedom to place $f_{r,LF}$. Furthermore, the high-frequency resonances of G_R and $G_{\mathrm{Out,A,C}\to\infty}$, which depends mainly on L_d and C_2, should not coincide with the main ARU switching frequency component at $2f_{s,i}$.

In addition, **Fig. 11b** shows the transfer function $G_{Out,R} = i_{out}/i_R$, which is valid for the actual (i. e., switched) resonant current, i_R, flowing into the LV side DC bus. Its resonance must be significantly below twice the DC/DC converter switching frequency, $2f_{s,d}$, which can be achieved by proper selection of L_d and C_2. Note that an adjustment of L_d affects also the low-frequency resonance (whose location is quite critical as discussed above), whereas this is not the case when C_2 is adjusted to obtain a desired attenuation at $2f_{s,d}$ (cf. **Figs. 12b** and **c**).

B. Design Optimization

Assuming a given transformer and given power semiconductors, R_{dc} and L_{dc} are fixed. In addition, it is assumed that for reasons of efficiency the resistors R_1, R_2, and R_d are comparatively small and not actively used as damping elements; specifically, they are set to 1 mΩ each for the optimization. Then, there are still four degrees of freedom left to influence the transfer function resonances, namely the two DC link capacitors, $C_{1,t}$ (or C_1) and C_2, the decoupling inductor, L_d, and also the damping resistor, R_{dp}. By sweeping those over wide ranges, a large number of designs with specifications according to **Tab. I**

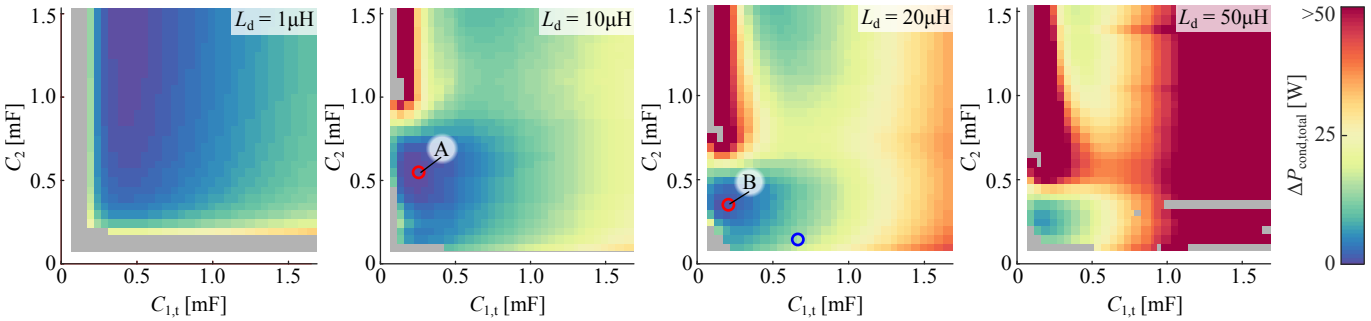

Fig. 13. Grid search result overview where the color encodes the overall conduction loss increase, $\Delta P_{cond,total}$, with respect to the design with lowest losses.

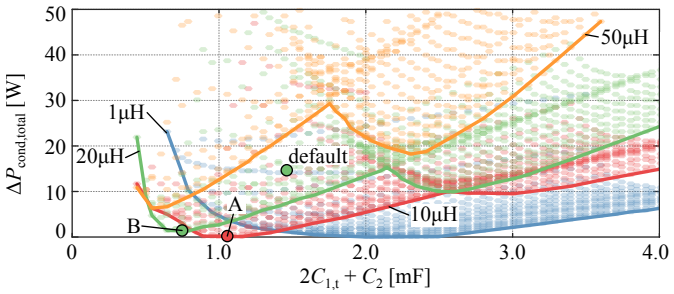

Fig. 14. Loss-increase-vs.-capacitance Pareto fronts for four different L_d values with the two designs A and B from **Fig. 13** indicated.

TABLE III. OPTIMIZATION RESULTS.

	$C_{1,\mathrm{t}}$	C_2	L_d	cap. vol.
Default	660 µF	140 µF	20 µH	5.34 l
Optimized (B)	200 µF	350 µF	20 µH	2.24 l

is calculated by utilizing the transfer functions, each design featuring specific losses, voltage ripples, etc.

In **Fig. 13**, the increase of overall conduction losses (V_F, R_dc, R_d, R_dp, etc.) with respect to the best design is plotted for all combinations, where for each tuple $\{C_{1,\mathrm{t}}, C_2, L_\mathrm{d}\}$ the R_dp resulting in lowest losses has been considered. To establish lower limits for the capacitors, all designs that result in a relative DC voltage ripple of more than 7.5 % are grayed out. It can be seen that with small L_d values (1 µH) larger capacitors are required to achieve low losses, while very large L_d values (50 µH) are not interesting, too. However, for intermediate values there is a region (note that too large capacitances are also suboptimal, as expected from the transfer functions), within which designs with minimum losses can be found (cf. markings A and B, respectively). **Fig. 14** shows the corresponding losses-vs.-capacitance Pareto fronts for the four considered L_d values, which confirms that intermediate L_d values offer the best trade-off between capacitance requirements, which translate into volume, and losses. Considering the much lower capacitor values, B would be the recommended design, featuring the element values given in **Tab. III**. The total capacitor volume can roughly be halved with respect to the default design while the overall system losses can be reduced slightly, too.

Note, however that the optimum is quite flat with respect to losses, e. g., the default design's (cf. Table I, blue circle in **Fig. 13**) conduction losses are less than 1.5 % higher than those of design B, although larger capacitors are used because of other system-level design considerations. On the other hand, even though the sensitivity to the parameters is low in the vicinity of the optimum, **Fig. 13** clearly shows that there are parameter combinations that can lead to high losses because of badly placed resonances of the converter dynamics.

Finally, in order to illustrate the achievable performance, the power density of the built converter cell from **Fig. 1a** is roughly 1.5 kW/l, including the ARU stage, isolation system (note that isolation considerations contribute significantly to the entire volume), air-cooling, all auxiliary systems, as well as

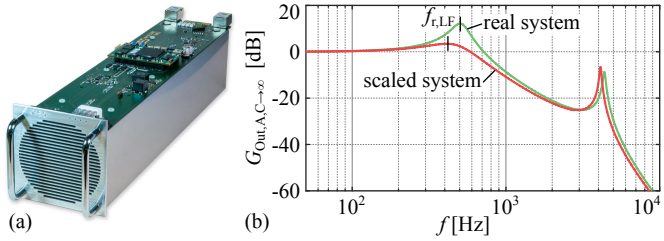

Fig. 15. (a) Scaled demonstrator SST cell providing a 100 V "MV" AC input (note that four cells will be cascaded to interface the 400 V grid) and an isolated 800 V LV DC output; (b) comparison of the main transfer function, $G_{\mathrm{Out,A,C}\to\infty}$, of the full-scale and the built scaled SST cell.

structural parts. By reducing the capacitor volume as indicated in **Tab. III** it would be possible to improve the power density by adapting the mechanical design accordingly. The estimated full-load efficiency when transferring power (with single-phase fluctuation) from the MV to the LV side is roughly 98.6 % for the DC/DC converter part, and roughly 98 % for the entire SST cell, i. e., including the ARU stage.

V. SCALED DEMONSTRATOR

In order to analyze control-related issues of the SST, a scaled demonstrator system featuring a full control system and the same power circuit structure as the real SST shown in **Fig. 1a**, but scaled to a lab-compatible power level (15 kVA, 400 V three-phase AC to 800 V DC to 400 V three-phase AC), is currently being developed and constructed (cf. **Fig. 15a**).

In principle, the scaled system would show equal dynamics as the real system if all components were scaled such that the stored energy as well as the losses, both relative to the respective rated powers, would stay equal. While the first is easily achieved, usually a lower power system shows higher relative losses, which means higher damping. Since for low frequencies $G_{\mathrm{Out,A,C}\to\infty}$ can be approximated as

$$G^{\mathrm{simplified}}_{\mathrm{Out,A,C}\to\infty} \approx \frac{1}{C_1(L'_\mathrm{d} + L_\mathrm{dc})s^2 + C_1(R_\mathrm{dc} + R'_\mathrm{d})s + 1}, \tag{12}$$

which leads to the damping being defined as

$$\delta \approx \frac{R_\mathrm{dc} + R'_\mathrm{d}}{2(L_\mathrm{dc} + L'_\mathrm{d})}, \tag{13}$$

there is a degree of freedom to compensate the scaled system's higher relative resistance by means of increasing either L_σ or L_d. However, this also shifts the low-frequency resonance, resulting in a trade-off between achieving similar resonance frequencies, $f_{\mathrm{r,LF}}$, or similar damping.

Fig. 15b shows the two transfer functions of the full-scale SST cell and the actually realized scaled version. In addition, **Fig. 16a** compares the measured step responses of the two systems, where it is clearly visible that the scaled system's response is somewhat slower and much better damped. Note that the temporary L_d used in the real system features a significantly higher R_d than what would be feasible during continuous full-power operation, therefore the measurement

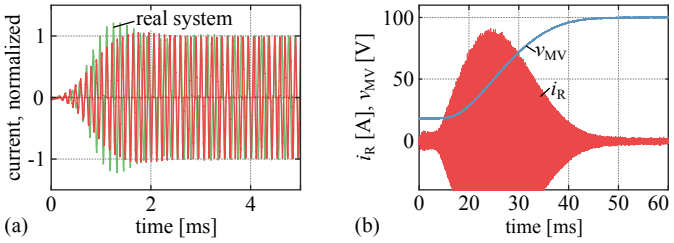

Fig. 16. (a) Comparison of the measured step responses of the real and the scaled system; (b) measurement of the system startup with an empty MV side DC link (b).

of the real system is better damped than the transfer function suggests.

Nevertheless, the dynamics are matching quite well, allowing to use the scaled system to perform experiments that would be too expensive or cumbersome with a full-scale system. As an application example, the startup process is looked at: if one DC link is charged while the other is not, the voltage excitation of the first resonant pulse would be high enough to excite destructive peak currents. Hence, one option to start the system is to start switching the HC-DCM SRC's active bridge before voltage is applied to any DC link, cf. e. g., [2], [5]. However, **Fig. 16b** shows measurements obtained from the scaled converter cell's startup with a charged LV DC link and an intially uncharged "MV" DC link. Here, the duty cycle of the switching LV bridge is ramped up very slowly from zero to about $50\,\%$ in steady-state, i. e., hard-switching transitions are used to crop the pulses at safe current levels. Thus it can be shown that HC-DCM SRC start-up with only one energized DC link is possible. Note, however, that this kind of duty-cycle control would not be feasible in steady-state operation due to the associated switching losses.

VI. Conclusion

The HC-DCM SRC is a very suitable realization option for the isolated DC/DC converter with constant voltage transfer ratio that is required in the converter cells of phase-modular SSTs, since it's ZCS feature allows high efficiencies. However, the power flow through this type of converter is not controllable. Instead, the HC-DCM SRC couples the two DC voltages with certain dynamics that can be described by means of a passive dynamic equivalent circuit. A generic derivation of this equivalent circuit and an experimental verification for the special case of small DC link capacitors has been presented.

In addition, the consequences of this dynamic coupling, e. g., the propagation of the single-phase power fluctuation through the HC-DCM SRC, corresponding mitigation strategies, and design pitfalls resulting from the resonances of the converter dynamics have been discussed, and an optimization of the capacitance selection to result in small volume and low losses has been presented. If considered carefully during the design, the lack of controllability and the system dynamics of the HC-DCM SRC are not detrimental to its application in SST converter cells.

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