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Integrated Isolation and Voltage Balancing Link of 3-Phase 3-Level PWM Rectifier and Inverter Systems

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***Abstract*—For a 3-phase pulse width modulated high-bandwidth AC voltage source, this paper presents a series resonant DC–DC converter (SRC) with a high-frequency transformer operated by only two half-bridges interconnecting a 3-phase 3-level rectifier and 3-phase plus neutral conductor 3-level inverter stage. On the primary side, one terminal of the transformer is connected through the resonant capacitor and inductor to one bridge-leg output and the other terminal is connected to the DC-link midpoint. On the secondary side, both terminals directly connect to the second bridge-leg output and the DC-link midpoint. With the proposed SRC, the galvanic isolation and the balancing of the capacitor voltages of the inverter-side split DC-link can be achieved also for an unequal loading of the DC-link capacitors. The AC source needs to supply not only passive symmetrical 3-phase loads, but also passive or active single-phase, 2-phase, DC and asymmetrical 3-phase loads. Hence, the unequal loading of the DC-link capacitors can be generated, for example, in case a DC load is connected to the 4-wire inverter stage.**
The operation principle of the SRC is described in detail for an unequal loading of the DC-link capacitors. Moreover, design guidelines for the suggested SRC are derived and finally the theoretical analysis is successfully verified by measurements conducted on a 1 kW proof-of-concept SRC prototype.

Keywords: *Galvanic Isolation, DC-Link Voltage Balancing, Series Resonant Converter, Dual Active Bridge, PWM Converter.*

I. Introduction

For bidirectional mains connected AC voltage sources consisting of a mains-side rectifier and a load-side inverter stage, a galvanically isolated DC–DC converter is inserted between the two stages to avoid a ground current in the case of grounded loads. International standards, e.g. IEC 60335-1, IEC 60950-1 and IEC 61140, limit the ground current for safety reasons; the maximum allowed ground current (e.g. $3.5\ \mathrm{mA_{rms}}$) depends on the rated nominal current and on the specific application, in which the power converter is utilized. Commonly, the DC–DC converter is realized with a Dual Active Bridge Converter (DABC) [1]–[4] employing two active full-bridges as shown in **Fig. 1**, which depicts the simplified equivalent circuit of the considered 3-phase Pulse Width Modulated (PWM) high-bandwidth AC voltage source [5]–[7]. In **Table I** the electrical specifications of the AC source are summarized. A 3-phase plus neutral conductor inverter stage is utilized to not only power passive symmetrical 3-phase loads, but also passive as well as active single-phase, 2-phase, DC and asymmetrical 3-phase loads. The choice of the inverter stage switching frequency of $f_{\mathrm{s,os}} = 48\ \mathrm{kHz}$ is motivated in [8] and the rectifier stage switching frequency of $f_{\mathrm{s,is}} = 20\ \mathrm{kHz}$ is chosen to be higher than the highest audible frequency. For such switching frequencies, it is shown in [9] that a 3-level Neutral Point Clamped (NPC) bridge-leg realized with 600 V IGBTs has lower losses than a standard 2-level bridge-leg built with 1200 V IGBTs. Thus, 3-level NPC bridge-legs are employed for the rectifier and the inverter stage, requiring also split DC-links.
The alternative isolation option, to insert a 50 Hz or 60 Hz line-frequency transformer between the mains and the rectifier stage [10], is typically discarded as it would significantly increase the size and the weight of the system [11].

As mentioned above, the AC source is also used to power DC loads. For example, a grounded DC load connected between phase A and the (grounded) neutral conductor N (cf. **Fig. 1**), which requires a positive voltage, takes its energy only from the upper DC-link capacitor $C_{\mathrm{dc,3}}$ because the neutral conductor N is directly connected to the inverter-side DC-link midpoint. This leads to an unequal average loading of $C_{\mathrm{dc,3}}$ and $C_{\mathrm{dc,4}}$, and accordingly to an increasing positive voltage difference between $U_{\mathrm{dc,4}}$ and $U_{\mathrm{dc,3}}$ over time. Thus, to avoid this voltage difference and to ensure balanced DC-link voltages $U_{\mathrm{dc,3}}$ and $U_{\mathrm{dc,4}}$ in all operating points and for all loads, a balancer circuit with controlled current i_{bal}, as depicted in **Fig. 1**, is typically provided [12]. Balanced rectifier-side DC-link voltages $U_{\mathrm{dc,1}}$ and $U_{\mathrm{dc,2}}$ can be achieved with proper control of the rectifier stage, consisting of a 3-level NPC converter which allows to control the neutral-point potential [13], [14].

TABLE I Electrical specifications of the high-bandwidth AC source depicted in **Fig. 1**.

Nominal power P_{nom}	10 kW
Nominal mains voltage U_{mains}	$400\ \mathrm{V_{ll,rms}}$
Nominal rectifier stage current I_{nom}	$14.5\ \mathrm{A_{rms}}$
Nominal DC-link voltage $U_{\mathrm{dc,nom}}$	700 V
Mains frequency f_{mains}	50 Hz
Rectifier stage switching (carrier) frequency $f_{\mathrm{s,is}}$	20 kHz
DC–DC converter switching frequency $f_{\mathrm{s,dc}}$	20 kHz
Inverter stage switching (carrier) frequency $f_{\mathrm{s,os}}$	48 kHz

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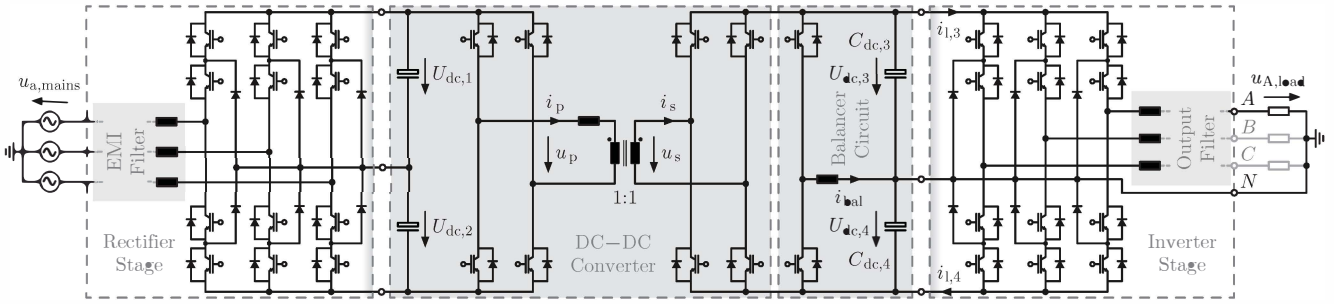


Fig. 1 Simplified equivalent circuit of the considered high-bandwidth AC source [5]–[7] with an integrated isolated DC–DC converter for galvanic isolation of the rectifier and inverter stage, and a balancer circuit to ensure equal DC-link voltages $U_{dc,3}$ and $U_{dc,4}$ also in case asymmetrical loads are supplied by the inverter stage.

As shown in **Fig. 1**, to achieve the galvanic isolation and the DC-link voltage balancing, typically two full-bridges and a half-bridge for the balancer circuit are employed. To reduce the number of power semiconductors and gate drive units from ten to four, the topology presented in **Fig. 2** is proposed [15]. Instead of a DABC, a Series Resonant Converter (SRC) [3], [16]–[19], with the resonant elements C_{res} and L_{res} is employed. In this topology, on the primary side, one terminal of the transformer is connected through the resonant capacitor and inductor to primary-side bridge-leg output and the other terminal is connected to the DC-link midpoint. On the secondary side, both terminals directly connect to the secondary-side bridge-leg output and the DC-link midpoint. The system is operated in a half-cycle discontinuous-conduction mode as further explained in **Section II**. Even though two active bridge-legs are used to allow a bidirectional power flow in all operating points, only one bridge-leg is switched and the other one operates as a diode rectifier. This reduces the complexity to run the converter compared to a DABC and motivates the selection of the SRC concept.

The load and the inverter stage are in **Fig. 2** represented by R_{34} and R_4 such that the same power flows through the DC–DC converter occur as if the inverter stage would be connected. The possible unequal average loading of the DC-link capacitors $C_{dc,3}$ and $C_{dc,4}$, as explained previously, is represented by the additional resistor R_4. The resistor R_{34} loads both capacitors $C_{dc,3}$ and $C_{dc,4}$ equally.

For an unequal average loading of the DC-link capacitors $C_{dc,3}$ and $C_{dc,4}$, the average values of the load currents $i_{l,3}$ and $i_{l,4}$ are different and the high-frequency transformer establishes a magnetizing current which is in average equal to the average of $i_{l,4} - i_{l,3}$ as further elaborated in **Section II**. Thus, the transformer is realized with an air-gap and integrates the galvanic isolation and DC-link voltage balancing.

For the DC–DC converter depicted in **Fig. 2**, 2-level half-bridges are employed instead of 3-level NPC bridge-legs as used for the rectifier and the inverter stages. A 2-level

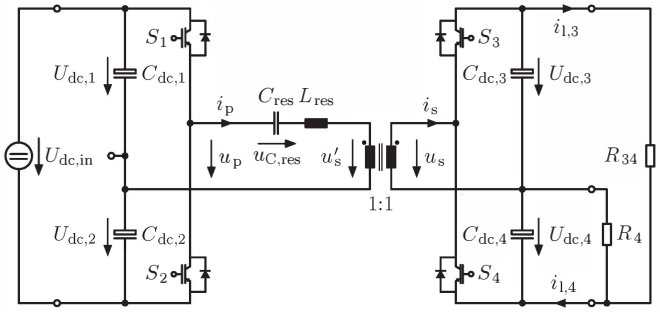


Fig. 2 Proposed DC–DC converter to achieve a galvanic isolation and a DC-link voltage balancing for split DC-links [15]. A series resonant converter (SRC) topology with only two active half-bridges is employed to reduce the number of power semiconductors and gate drive units compared to the standard solutions (cf. **Fig. 1**). Illustratively, the lower DC-link capacitor $C_{dc,4}$ is additionally loaded by R_4. It is assumed that the voltages $U_{dc,1}$ and $U_{dc,2}$ are balanced by the rectifier stage [13], [14].

bridge-leg with two 1200 V IGBTs has lower conduction losses but higher switching losses than a 3-level bridge-leg with four 600 V IGBTs [20], [21]. However, to reduce the number of power semiconductors and gate drive units, 2-level bridge-legs are selected. Furthermore, thw switching losses can be kept low due to the SR operation. The principle of operation for the proposed SRC with 3-level NPC bridge-legs can be found in [15].

Section II analyzes in detail the operation of the proposed SRC for an unequal loading of $C_{dc,3}$ and $C_{dc,4}$. The design guidelines for a 1 kW proof-of-concept SRC prototype are presented in **Section III**. The theoretical analysis of the converter is supported by measurements in **Section IV** and **Section V** concludes the paper.

A high-bandwidth AC source is the targeted application of the analyzed DC–DC converter shown in **Fig. 2**. However, the isolated DC–DC converter could also be used for mobile systems such as trains [22], electric cars [22], [23] and aerospace applications [2].

II. Operation Principle of the Half-Cycle Discontinuous-Conduction-Mode Series Resonant DC–DC Converter with Half-Bridges and Unequal Loading

The operation principle of a SRC run in Half-Cycle Discontinuous-Conduction Mode (HCDCM) with a half-bridge at the input and a full-bridge at the output, i.e. without the proposed DC-link balacing feature, is investigated in [19]. For analyzing the proposed system, in a first step, a symmetrical loading of the inverter-side DC-link capacitors is assumed, i.e. $R_4 \to \infty$ in **Fig. 2**. Moreover, the magnetizing current and the transformer stray inductance are neglected ($L_\mu \to \infty$). With these assumptions, the primary and the secondary currents are identical for a transformer turns ratio of 1:1. The voltage source $U_{dc,in}$ depicted in **Fig. 2** represents the DC-link voltage controlled rectifier stage; the partial rectifier-side DC-link voltages $U_{dc,1}$ and $U_{dc,2}$ are balanced by the 3-level NPC rectifier stage.

For a power flow from the rectifier to the inverter stage, the primary-side bridge-leg with switches S_1 and S_2 (cf. **Fig. 2**) is actively switched with a duty-cycle d of 50% (including the interlocking time). The gate signals for S_1 and S_2 are phase-shifted by 180°. This leads to the primary voltage u_p depicted in **Fig. 3(a)** over two switching periods $T_s = 1/f_{s,dc}$. Because of the switching, a resonant current pulse is generated. The positive resonant pulse is denoted by $i_{s,pp}$ and charges the upper DC-link capacitor $C_{dc,3}$; the negative pulse is denoted by $i_{s,np}$ and charges the lower DC-link capacitor $C_{dc,4}$. These pulses are shown in **Fig. 3(a)** and defined as

$$i_{s,pp} = \begin{cases} i_s & \text{if } i_s \geq 0 \\ 0 & \text{else} \end{cases}, \quad i_{s,np} = \begin{cases} i_s & \text{if } i_s \leq 0 \\ 0 & \text{else} \end{cases}. \tag{1}$$

On the secondary side, the switches S_3 and S_4 are not operated or operated with synchronous rectification, i.e. the secondary-side bridge-leg acts as a diode rectifier. In HCDCM, the resonant current pulses reach zero before a new current pulse is excited, i.e. $t_{psz} \leq T_s/2$ [cf. **Fig. 3(a)**], i.e. the SRC is operated below the resonant frequency $f_{res} = 1/\left(2 \cdot \pi \cdot \sqrt{L_{res} \cdot C_{res}}\right)$. Because of the diode rectification, once the current pulses reach zero at t_{psz}, the diodes avoid that the currents reverse direction. Accordingly, the secondary current is zero until a new current pulse is excited.

For a finite magnetizing inductance, with the equivalent circuit of the transformer referred to the primary side as depicted in **Fig. 3(e)** and for an unequal loading of $C_{dc,3}$ and $C_{dc,4}$, the primary voltage u_p, the secondary voltage u_s, and the secondary current i_s are depicted in **Fig. 3(b)**. In steady-state, the average values of $i_{s,pp}$ and $i_{s,np}$ over T_s are equal to the positive average load current $i_{l,3,avg}$ of $C_{dc,3}$ and the negative average load current $i_{l,4,avg}$ of $C_{dc,4}$ over the same period respectively. Thus,

$$i_{s,pp,avg} = i_{l,3,avg}, \quad i_{s,np,avg} = -i_{l,4,avg} \tag{2}$$

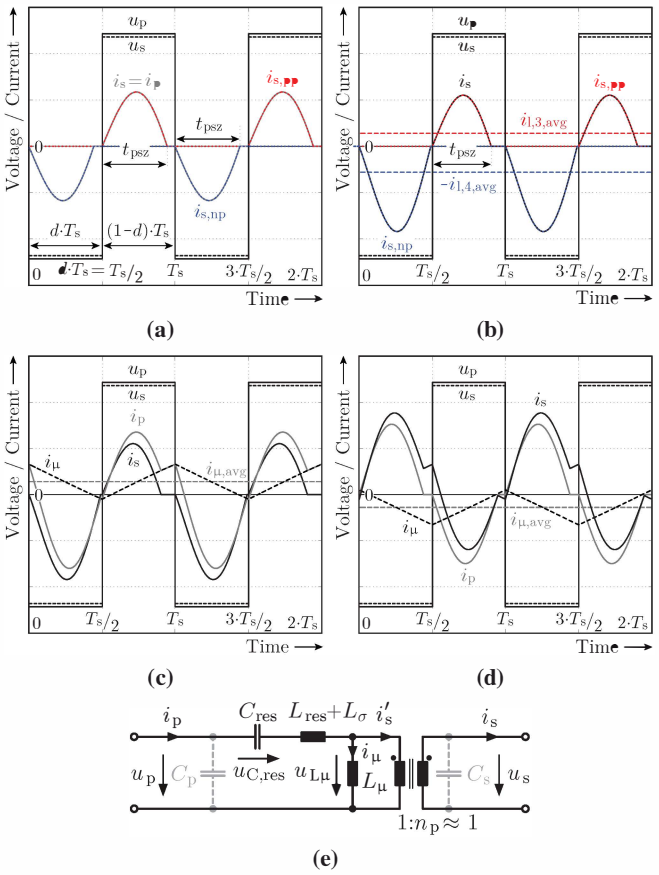


Fig. 3 Exemplary primary voltage u_p, secondary voltage u_s, primary current i_p and secondary current i_s of the SRC given in **Fig. 2** for $L_\mu \to \infty$ and equal average load currents $i_{l,3,avg} = i_{l,4,avg}$ **(a)**; u_p, u_s and i_s **(b)** and additionally i_p and magnetizing current i_μ **(c)** for a finite magnetizing inductance and an unequal *loading* of the inverter-side DC-link capacitors. Exemplary u_p, u_s, i_p, i_s and i_μ for an unequal power *fed* into the inverter-side DC-link capacitors **(d)**. T_s denotes the switching period and the equivalent circuit of the resonant components and the high-frequency transformer referred to the primary side is given in **(e)**.

and accordingly the average of the secondary current $i_{s,avg}$ over T_s is given by (discontinuous-conduction-mode)

$$i_{s,avg} = i_{s,pp,avg} + i_{s,np,avg} = i_{l,3,avg} - i_{l,4,avg}. \tag{3}$$

In the following, the averages of currents and voltages of the SRC are always taken over one switching period T_s what is not explicitly mentioned any more.

For the case shown in **Fig. 3(b)**, $i_{l,4,avg}$ is larger than $i_{l,3,avg}$ and accordingly $i_{s,avg}$ is negative [cf. Eq. (3)]. On the primary side, the average of the primary current i_p is zero in steady-state; otherwise, C_{res} would be continuously charged or discharged:

$$i_{p,avg} = i_{\mu,avg} + i'_{s,avg} = 0. \tag{4}$$

This means that an average magnetizing current $i_{\mu,avg}$ flows which compensates the average value of the secondary current

i_s, and hence

$$i_\mathrm{\mu,avg} = -i'_\mathrm{s,avg} = i'_\mathrm{l,4,avg} - i'_\mathrm{l,3,avg}, \tag{5}$$

as depicted in **Fig. 3(c)**. In the above equation the secondary-side load currents are transformed to the transformer primary side and accordingly assigned by a " $'$ ". This notation is used throughout the rest of the paper.
In steady-state, the voltage

$$u_\mathrm{L\mu} = \frac{L_\mu}{L_\mu + L_\sigma + L_\mathrm{res}} \cdot \begin{cases} U_\mathrm{dc,1} - u_\mathrm{C,res} & 0 \leq t < \frac{T_\mathrm{s}}{2} \\ -U_\mathrm{dc,2} - u_\mathrm{C,res} & \frac{T_\mathrm{s}}{2} \leq t < T_\mathrm{s} \end{cases}, \tag{6}$$

applied to the transformer magnetizing inductance L_μ [cf. **Fig. 3(e)**] is because of (4) also zero.

Thus, DC-link voltage balancing is achieved by the average magnetizing current $i_\mathrm{\mu,avg}$ and accordingly the magnetizing inductance of the high-frequency transformer takes over the functionality of the balancer inductance shown in **Fig. 1**. Therefore, the SRC integrates the DC-link voltage balancing and the galvanic isolation. In the case at hand, no voltage step-down or step-up is required, thus, a transformer turns ratio of 1:1 is employed.
Because of the average magnetizing current $i_\mathrm{\mu,avg} \neq 0$, the transformer needs to store energy and accordingly is preferably built with a low-permeability material or with a discrete air-gap. Alternatively, an inductor could be placed in parallel to the transformer primary or secondary winding which would take over a large part of the magnetizing current [cf. (5)] flowing through the transformer without the additional inductor.

For an ideal switching, the average rectifier-side DC-link voltages $U_\mathrm{dc,1,avg}$ and $U_\mathrm{dc,2,avg}$ are with the help of the magnetizing current equal in average. Based on the more detailed analysis carried out in **Section III**, it is observed that the higher the load currents the lower the average inverter-side DC-link voltages for fixed rectifier-side DC-link voltages. The reason is that the average values of the resonant current pulses [cf. Eq. (1)] increase with the higher load currents. Accordingly, to generate resonant pulses with higher average values, larger voltage excitations are required [19] meaning lower average inverter-side DC-link voltages. Thus, for unequal load currents $i_\mathrm{l,3}$ and $i_\mathrm{l,4}$, different average DC-link voltages $U_\mathrm{dc,3,avg}$ and $U_\mathrm{dc,4,avg}$ result.
Ideally, i.e. without including the parasitic capacitances C_p and C_s [cf. **Fig. 3(e)**] between the bridge-leg outputs and the corresponding midpoints, the largest average inverter-side DC-link voltage difference is reached for $i_\mathrm{l,3,avg} \neq 0$ and $i_\mathrm{l,4,avg} = 0$ or vice versa. Including the mentioned capacitors, an oscillatory charge reversal of these capacitances occurs during a switching transient. If during the transient the voltage across C_s is in absolute value larger than the DC-link voltage $U_\mathrm{dc,3}$ or $U_\mathrm{dc,4}$ plus the diode forward voltage drop u_df, the DC-link capacitor $C_\mathrm{dc,3}$ or $C_\mathrm{dc,4}$ is slightly charged. Thus, $C_\mathrm{dc,3}$ or $C_\mathrm{dc,4}$ charges to the value of the transient peak voltage across C_s minus u_df. This problem can be diminished by placing symmetrizing resistors across all DC-link capacitors which are loading the capacitors just enough to compensate the slight charging. As demonstrated by measurements (cf. **Section IV**), symmetrizing resistors of $22\,\mathrm{k\Omega}$ could be employed for the $1\,\mathrm{kW}$ prototype which are increasing the losses by only about $1\,\mathrm{W}$.
Another way to go around the issue is to actively switch the secondary-side bridge-leg in-phase with the primary-side bridge-leg, which would increase the total losses only by a few percent, as could be shown by a more detailed analysis. In case only a unidirectional power flow from the rectifier to the inverter stage is required, the secondary-side bridge-leg could be realized with only diodes and therefore symmetrizing resistors would be necessary[1].

Concluding, ideally a perfect DC-link voltage balancing is given on the rectifier side but not on the inverter side. However, because large resonant current pulses can be generated with a small excitation voltage, the voltage difference between $U_\mathrm{dc,3,avg}$ and $U_\mathrm{dc,4,avg}$ is for example at maximum 10% of $(U_\mathrm{dc,3,avg} + U_\mathrm{dc,4,avg})/2$ for the built prove-of-concept converter (cf. **Section IV**).

For feeding power back from the inverter to the rectifier side, the secondary-side bridge-leg is switched and the primary-side bridge-leg is operated as diode rectifier. In this case, again the magnetizing inductance of the transformer directly acts as a balancer inductor. Illustratively, the primary and secondary voltages as well as the primary and secondary currents are depicted in **Fig. 3(d)** for this case.
It is important to note that the resonant capacitor C_res needs to be placed on the side of the transformer where the DC-link capacitors are equally loaded (i.e. the rectifier side for the case at hand).

III. Design Guidelines for the Series Resonant DC–DC Converter with Unequal Loading

The resonant current pulses [cf. **Fig. 3(b)**] are computed analytically in this section to provide physical insight into the operating behavior of the SRC depicted in **Fig. 2**. For the sake of brevity, the subsequent equations are shown for the positive current pulse $i_\mathrm{s,pp}$ of the secondary current [cf. **Fig. 3(a)**] and for a power flow from the rectifier to the inverter stage. The negative current pulse can be computed analogously.
By superimposing the magnetizing current i_μ and the secondary current i'_s, the primary current i_p is obtained. The average of i_μ is given by the average difference between the load current $i_\mathrm{l,3,avg}$ and $i_\mathrm{l,4,avg}$; the peak-to-peak

[1] A further option would be to control the duty-cycle d of the switches of the primary-side bridge-leg [cf. **Fig. 3(a)**] as presented in [15], which would allow to equalize the inverter-side DC-link voltages $U_\mathrm{dc,3}$ and $U_\mathrm{dc,4}$ in average.

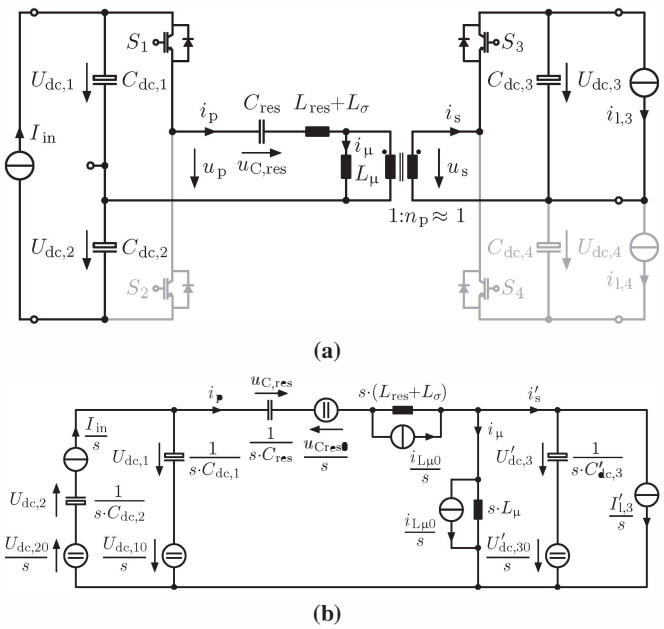


Fig. 4 Equivalent circuit employed for the theoretical analysis of the SRC of **Fig. 2** for a positive resonant current pulse [cf. **Fig. 3(b)**] **(a)**, and resulting equivalent circuit in the frequency domain based on the approach described in [19] **(b)**. The equivalent circuits are only valid for $0 \leq t \leq t_{psz}$ [cf. **Fig. 3(b)**]. The constant voltage and current sources in **(b)** result from the initial conditions (especially $i_{L\mu 0} \neq 0$), which are marked with an additional "0". The input current $I_{in} = P_{in}/U_{dc,in}$ and the load current $i_{l,3} = I_{l,3}$ are assumed to be constant.

current ripple of i_μ can be assessed using (6) while setting $U_{dc,1}(t) = U_{dc,2}(t) = U_{dc,in}/2$ and neglecting $u_{C,res}(t)$ for $U_{dc,in}/2 \gg u_{C,res}(t)\ \forall\ t$.

As described in the last section, the SRC depicted in **Fig. 2** differs from standard SRC (cf. [19] for example) by its much lower magnetizing inductance. Thus, the magnetizing inductance needs to be included into the modeling of the converter. Based on the approach explained in [19], the equivalent circuit in the frequency domain depicted in **Fig. 4** can be employed to compute the secondary current $i'_s(s)$. Adding the magnetizing inductance in the modeling enforces to set an initial condition on the magnetizing current, i.e. $i_{L\mu 0}$, and thus also on the primary current.

In the frequency domain, the current $i'_s(s)$ can be computed using nodal and mesh equations. Transforming $i'_s(s)$ into the time domain and assuming a constant load current, $i_{l,3} = I_{l,3} =$ const., leads to

$$\begin{aligned} i'_s(t) = \ & I'_{l,3} + \\ & I_{s,1} \cdot \sin(\omega_1 \cdot t) + I_{c,1} \cdot \cos(\omega_1 \cdot t) + \\ & I_{s,2} \cdot \sin(\omega_2 \cdot t) + I_{c,2} \cdot \cos(\omega_2 \cdot t). \end{aligned} \tag{7}$$

In the above equation the two angular frequencies depend only on the circuit parameters and are with the simplification of $C_{dc,1} = C_{dc,2}$ given by

$$\begin{aligned} \omega_1 = & \sqrt{\frac{1}{2 \cdot C_{1res} \cdot L_{\sigma res}} + \frac{L_{\sigma res} + L_\mu - \tilde{L}}{2 \cdot C'_{dc,3} \cdot L_{\sigma res} \cdot L_\mu}}, \\ \omega_2 = & \sqrt{\frac{1}{2 \cdot C_{1res} \cdot L_{\sigma res}} + \frac{L_{\sigma res} + L_\mu + \tilde{L}}{2 \cdot C'_{dc,3} \cdot L_{\sigma res} \cdot L_\mu}}, \end{aligned} \tag{8}$$

where $L_{\sigma res} = L_\sigma + L_{res}$, $C_{1res} = C_{dc,1} \cdot C_{res}/(C_{dc,1} + C_{res})$ and

$$\tilde{L} = \sqrt{L_{\sigma res}^2 - 2 \cdot \tilde{C}_{f1} \cdot L_{\sigma res} \cdot L_\mu + \tilde{C}_{f2}^2 \cdot L_\mu^2} \tag{9}$$

with the scaling factors

$$\begin{aligned} \tilde{C}_{f1} = & \ \frac{C_{dc,1} \cdot (C'_{dc,3} - C_{res}) + C'_{dc,3} \cdot C_{res}}{C_{dc,1} \cdot C_{res}} \text{ and} \\ \tilde{C}_{f2} = & \ \frac{C_{dc,1} \cdot (C'_{dc,3} + C_{res}) + C'_{dc,3} \cdot C_{res}}{C_1 \cdot C_{res}}. \end{aligned} \tag{10}$$

The coefficients $I_{s,1}$, $I_{c,1}$, $I_{s,2}$ and $I_{c,2}$ are a function of the initial conditions:

$$\begin{aligned} I_{s,k} = & \frac{C'_{dc,3} \cdot \left(\frac{U'_{dc,30}}{C_{1res}} + \left(L_\mu \cdot u_{dc,p} - (L_{\sigma res} + L_\mu) \cdot U'_{dc,30} \right) \cdot \omega_k^2 \right)}{2 \cdot L_{\sigma res} \cdot L_\mu \cdot C'_{dc,3} \cdot \omega_k^3 - \left(L_{\sigma res} + L_\mu \cdot \tilde{C}_{f2} \right) \cdot \omega_k}, \\ I_{c,k} = & \frac{L_\mu \cdot \left(\frac{C_{dc,1}}{C_{res}} \cdot \left(i'_{l,3} + i_{L\mu 0} \right) + \left(i'_{l,3} \cdot \left(1 - C_{dc,1} \cdot L_{\sigma res} \cdot \omega_k^2 \right) - \Delta i_{in} \right) \right)}{\frac{C_{dc,1}}{C'_{dc,3}} \cdot \left(2 \cdot L_{\sigma res} \cdot L_\mu \cdot C'_{dc,3} \cdot \omega_k^2 - \left(L_{\sigma res} + L_\mu \cdot \tilde{C}_{f2} \right) \right)}, \end{aligned} \tag{11}$$

where $k = 1, 2$, $u_{dc,p} = u_{Cres0} + U_{dc,10}$ and $\Delta i_{in} = I_{in} - i_{L\mu 0}$. $I_{s,k}$ depends only on the initial conditions of the voltages and $I_{c,k}$ only on the initial conditions of the currents.

Moreover, it is noted that the resonant current pulses contain two frequency components. For the built hardware (cf. **Section IV**), the frequencies are $f_1 = \omega_1/(2 \cdot \pi) \approx 1$ kHz and $f_2 = \omega_2/(2 \cdot \pi) \approx 24$ kHz. Furthermore, $i'_{l,3} + I_{c,1} + I_{c,2} = 0$ follows directly from the fact that the current on the secondary side cannot reverse direction after a current pulse because of the secondary-side diodes. Moreover, (7) can be simplified to

$$i'_s(t) = I'_{l,3} + I_1 \cdot \sin(\omega_1 \cdot t + \phi_1) + I_2 \cdot \sin(\omega_2 \cdot t + \phi_2) \tag{12}$$

with $I_k = \sqrt{I_{s,k}^2 + I_{c,k}^2}$ and $\phi_k = \text{atan2}(I_{c,k}, I_{s,k})$.

The time t_{psz} [cf. **Fig. 3(b)**, exemplary shown for the positive resonant current pulse $i_{s,pp}$] when the secondary current $i_s(t)$ reaches zero can be computed numerically by equating (12) to zero. t_{psz} increases with the load current $i_{l,3}$ and thus the resonant elements C_{res} and $L_{\sigma res}$ can be selected such that for the chosen switching frequency and for the maximum load current $i_{l,3,max}$ or $i_{l,4,max}$ (i.e. for loading only $C_{dc,3}$ or $C_{dc,4}$), the resonant current pulses reach zero before a new current pulse is generated, i.e. $t_{psz} \leq T_s/2$[2].

In conclusion, a first design of the SRC, which is supported by circuit simulations, can be obtained as follows. To reduce

[2] It is noted that the shape of the resonant current pulses and the time t_{psz} depend also on the parasitic resistive parts between one and the other split DC-links and the symmetrizing resistors connected across the DC-link capacitors.

the switching losses, the switching frequency $f_{s,dc}$ can be chosen such that it is just higher than the highest audible frequency. For the prototype (cf. **Section IV**), $f_{s,dc} = 20$ kHz is selected. In a next step, the maximum difference in the load current [cf. (5)] needs to be determined, which is given by the application in which the converter is employed. For the built 1 kW hardware, this maximum difference is set to 333 W. The capacitances of the DC-link capacitors can be determined such that the DC-link voltage ripple across one capacitor is limited, e.g. to 2.5% of $U_{dc,in}/2$.

On the one hand, the larger the value of the transformer's magnetizing inductance the smaller the peak-to-peak ripple of i_μ and accordingly the lower the high-frequency copper losses. On the other hand, there is also an advantage in having a reduced magnetizing inductance, especially in case the switches are implemented with MOSFETs. For a power flow from the rectifier to the inverter stage [cf. **Fig. 3(c)**], a good option is, as it is done for the 1 kW prototype, to choose the magnetizing inductance L_μ just large enough that soft-switching (zero-voltage switching) can be achieved in all operating points. Therefore, the magnetizing current has to become negative before the positive voltage is applied at the output of the primary-side bride-leg as exemplary shown in **Fig. 3(c)** and vice versa. Thus, the peak-to-peak magnetizing current ripple $\Delta i_{\mu,pp}$ needs to be slightly larger than two times the maximum average magnetizing current $i_{\mu,avg,max}$, i.e.

$$\Delta i_{\mu,pp} > 2 \cdot |i_{\mu,avg,max}| = 2 \cdot \left| i'_{l3,avg,max} - i'_{l4,avg,min} \right| . \quad (13)$$

With the above condition, also soft-switching is obtained in all operating points for an inverse power flow from the inverter to the rectifier stage as exemplary given in **Fig. 3(d)**.

To transfer the same amount of energy, the shorter the time t_{psz} the larger the peaks of the resonant current pulses for the same average DC-link voltages and switching frequency $f_{s,dc}$. This increases the primary and secondary rms currents and therefore also the copper losses. Accordingly, $t_{psz} = T_s/2$ is selected for the longest duration of the resonant current pulses. In a next step, the resonant elements can be determined. To achieve a compact converter, L_{res} should be as small as possible. Therefore, $L_{\sigma res}$ can be realized by only the stray inductance L_σ of the high-frequency transformer, i.e. $L_{\sigma res} = L_\sigma$, as it is done for the prototype. L_σ is fixed depending on the transformer design and hence C_{res} can be calculated. For a compact realization of the converter, the values of L_σ and C_{res} should be determined simultaneously to avoid high C_{res} values resulting for low L_σ.

IV. Experimental Verification

To verify the theoretically analyzed operation principle of the proposed SRC with integrated DC-link voltage balancing and galvanic isolation, a 1 kW proof-of-concept prototype is built. The electrical specifications and the circuit parameters of the system are summarized in **Table II**. The switched bridge-leg is realized with 200 V MOSFETs (OptiMOS™3 IPP320N20N3 G from Infineon Technologies AG) and the secondary-side diode rectifier stage is implemented with Schottky Diodes (MBR40250TG from On Semiconductor®). MOSFETs are selected because the relatively large forward voltage drops of IGBTs in comparison to the DC-link voltage levels. Additionally, due to the zero-voltage switching, less switching losses are expected for MOSFETs than for IGBTs.

TABLE II Electrical specifications and circuit parameters of the 1 kW SRC prototype with integrated DC-link voltage balancing and galvanic isolation.
*): To assess $L_{\sigma res}$ (cf. **Section III**), the inductances of the connecting wires, connectors and PCB tracks need to be accounted as well. For the built hardware these inductances were calculated to 0.31 µH.

Electrical Specifications	
Nominal power	1 kW
Max. asym. loading	333 W
Total DC-link voltage	150 V
Switching freq. $f_{s,dc}$	20 kHz
Circuit Parameters	
DC-link capacitors $C_{dc,x}$, $x = 1, 2, 3, 4$	
Measured capacitance	133 µF (2×68 µF)
Type	EPCOS MKT 100 V_{DC}
Resonant capacitor C_{res}	
Measured capacitance	30.2 µF (7×4.7 µF)
Type	WIMA MKS 2 30 V_{AC}
High-frequency transformer	
Core	$3 \times 2 \times$ E 42/21/15, EPCOS N27
Number of turns	$N_1 = N_2 = 17$ (bifilar windings)
Air-gap / coupling	1.7 mm / $k = 0.994 \rightarrow n_p = 0.994$
Magnetizing / stray inductance	$L_\mu = 153.1$ µH / $L_\sigma = 1.8$ µH*)

For the measurements, the equivalent circuits depicted in **Fig. 5** are employed. Five cases are investigated: for the cases $I-IV$, the power flow is from the rectifier to the inverter stage [cf. **Fig. 5(a)**]; for case V, the power flow is in the opposite direction [cf. **Fig. 5(b)**].

- *Case I* - Operation at "no load" [cf. **Fig. 6(a)**]: as mentioned in **Section II**, a minimum loading of $C_{dc,3}$ and $C_{dc,4}$ is necessary, which is achieved by setting $R_3 = R_4 \rightarrow \infty$ and $R_{34} = 22$ kΩ. This case represents the idle case, when no load is connected to the output of the SRC.
- *Case II* - Symmetrical operation at 1 kW [cf. **Fig. 6(b)**]: the inverter-side DC-link capacitors are loaded with $R_3 = R_4 = 22.5$ Ω ($R_{34} \rightarrow \infty$).
- *Case III* - Asymmetrical operation at 1 kW [cf. **Fig. 6(c)**]: $C_{dc,3}$ and $C_{dc,4}$ are loaded with $R_3 = 16.8$ Ω ($\rightarrow 330$ W) and $R_4 = 8.4$ Ω ($\rightarrow 660$ W) respectively ($R_{34} \rightarrow \infty$).
- *Case IV* - Asymmetrical operation at 330 W [cf. **Fig. 6(d)**]: the inverter-side DC-link capacitors

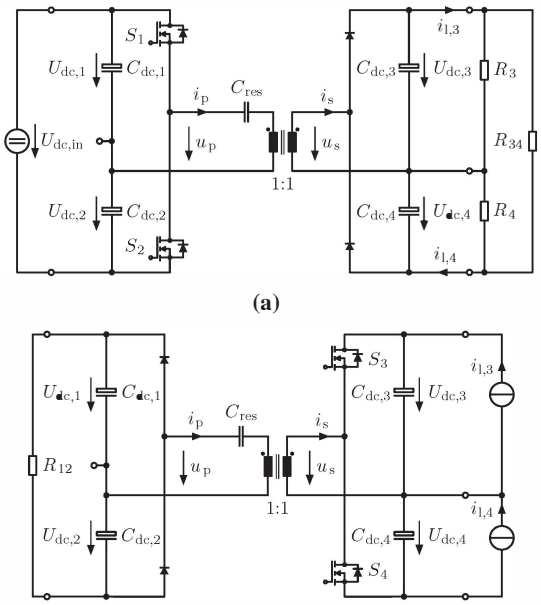
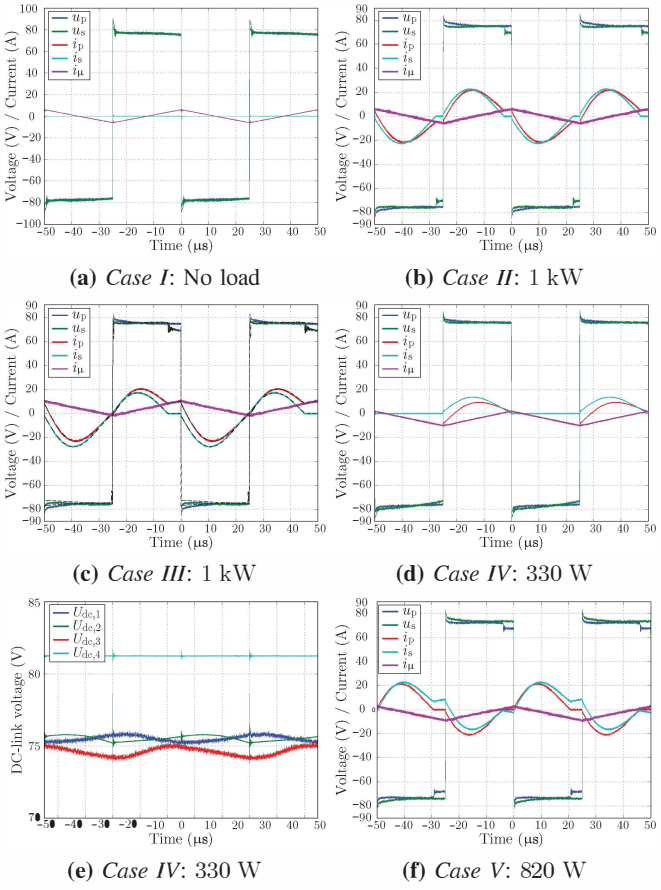


Fig. 5 Equivalent circuits of the measurement setups: for a power flow from the inverter stage to the rectifier stage **(a)**, and for a power flow from the inverter stage to the rectifier stage **(b)**.



(a) *Case I*: No load **(b)** *Case II*: 1 kW

(c) *Case III*: 1 kW **(d)** *Case IV*: 330 W

(e) *Case IV*: 330 W **(f)** *Case V*: 820 W

Fig. 6 On the 1 kW prototype (cf. **Table II**) measured primary voltage u_p, primary current i_p, secondary voltage u_s and secondary current i_s (cf. **Fig. 5**) for the five cases mentioned in the text: case I **(a)**, case II **(b)**, case III **(c)**, case IV **(d)** and case V **(f)**. For case IV, the DC-link voltages ($U_{\mathrm{dc,1,avg}} = 75.5$ V, $U_{\mathrm{dc,2,avg}} = 75.3$ V, $U_{\mathrm{dc,3,avg}} = 74.6$ V, $U_{\mathrm{dc,4,avg}} = 81.2$ V) are given in **(e)**. The transformer magnetizing current was calculated as $i_\mu = i_\mathrm{p} - i'_\mathrm{s}$.

are loaded with $R_3 = 16.8\,\Omega$ ($\rightarrow$ 330 W) and $R_4 = 22\,\mathrm{k}\Omega$ ($R_{34} \rightarrow \infty$). Because of the issue mentioned in **Section II**, $C_{\mathrm{dc,4}}$ was slightly loaded.

- *Case V* - Asymmetrical operation at 820 W [cf. **Fig. 6(f)**]: $i_{\mathrm{l,3}} = 4$ A ($\rightarrow$ 300 W) and $i_{\mathrm{l,4}} = 7.1$ A ($\rightarrow$ 520 W) is set. On the rectifier side, $C_{\mathrm{dc,1}}$ and $C_{\mathrm{dc,2}}$ are equally loaded by $R_{12} = 25\,\Omega$.

For the above mentioned cases, the measurements are shown in **Fig. 6**. Comparing the experimental results to **Fig. 3**, the measured voltages and currents are in good agreement with the theoretical analysis conducted throughout this paper. Furthermore, as exemplary depicted in **Fig. 6(c)**, the measurements are matching with the simulations (dashed black curves) carried out in GeckoCIRCUITS.

For case IV, the DC-link voltages $U_{\mathrm{dc,1}}$, $U_{\mathrm{dc,2}}$, $U_{\mathrm{dc,3}}$ and $U_{\mathrm{dc,4}}$ on the rectifier side and on the inverter side are given in **Fig. 6(e)**. As explained in **Section II**, the maximum DC-link voltage unbalance on the inverter side occurs when only one DC-link capacitor is loaded. The average voltage difference between $U_{\mathrm{dc,4}}$ and $U_{\mathrm{dc,3}}$ is 6.6 V and therefore 8.5% referred to $(U_{\mathrm{dc,3,avg}} + U_{\mathrm{dc,4,avg}})/2 = 77.9$ V.

V. Conclusion

In this paper, a series resonant DC–DC converter (SRC) integrating the split DC-link voltage balancing for unequal loadings of the DC-link capacitors and the galvanic isolation is presented for a high-bandwidth AC voltage source. The SRC interconnects a 3-phase 3-level rectifier stage with a 3-phase plus neutral conductor 3-level inverter stage which needs also to supply asymmetrical loads. The galvanic isolation is required to avoid a ground current and is achieved with a high-frequency transformer.

The proposed SRC is operated in half-cycle discontinuous-conduction-mode and consists of two half-bridges, from which only one is switched depending on the power flow direction. The bridge-leg output and the DC-link midpoint on the primary side are connected through the resonant capacitor, the resonant inductor and the primary winding of the transformer; on the secondary side, they are directly connected through the transformer secondary winding.

Supplying asymmetrical loads, the inverter-side DC-link capacitors are not equally loaded simultaneously. In this case, the voltage balancing across the DC-link capacitors is achieved by establishing an average (over one switching cycle)

magnetizing current which is equal to the difference of the load currents. Accordingly, the high-frequency transformer integrates the DC-link voltage balancing and the galvanic isolation. It needs to store energy and hence should be realized with an air-gap or a low-permeability material for a compact realization.

For standard solutions, the DC-link voltage balancing is achieved with an explicit balancer circuit and the galvanic isolation with a dual active bridge converter employing two full-bridges. Thus, the proposed SRC reduces the number of power semiconductors from 10 to 4 compared to the conventional topology.

Ideally, the DC-link voltage balancing on the rectifier side can be achieved perfectly. On the inverter side, the difference of the DC-link voltages depends on the average load currents. However, this voltage difference can be restricted to less than 10%, referred to the voltage across one DC-link capacitor.

Design guidelines are presented showing that the SRC can achieve soft-switching (zero-voltage switching) in all operating conditions if the peak-to-peak magnetizing current ripple is slightly larger than two times the maximum average magnetizing current (which corresponds to twice the maximum load current difference).

The theoretical analysis is supported by measurements conducted on a 1 kW proof-of-concept prototype matching very well with the theory and the simulations for no load, symmetrical loading and asymmetrical loading for a bidirectional power flow.

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