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4D-Interleaving of Isolated ISOP Multi-Cell Converter Systems for Single Phase AC/DC Conversion

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Abstract

The multi-cell converter approach allows to break the performance barriers of conventional systems by leveraging the advantages of using multiple interleaved low voltage and/or low current converter cells. In this digest, a fourth dimension of interleaving is proposed which considers the time dependent degrees of freedom in the control of the entire multi-cell converter system. This new control concept is based on the possibility to decouple the operation of the series connected input stages from the parallel connected output stages by using the energy storage capability of the DC-link capacitors. This digest shows how the 4D-interleaving concept improves the system performance such as the efficiency which will be demonstrated with measurement results on a hardware prototype system in the final paper.

1. Introduction

Driven by the rising demand for highly efficient telecom and server power supplies resulting from the global trend of cloud computing, the industry research efforts for new converter topologies with improved performance concerning efficiency and power density have been considerably increased. A very promising approach described in (1) (cf. **Fig. 1(b)** and **Fig. 2(a)**) towards a hyper-efficient and super-compact telecom rectifier ($\eta = 98\%$, $\rho = 2.2\text{kW/dm}^3$, $V_{\text{in,RMS}} = 230\,\text{V}, V_{\text{out}} = 48\,\text{V}, P_{\text{rat,tot}} = 3.3\,\text{kW}$) is based on a multi-cell converter concept with ISOP arrangement of the converter cells. Each converter cell contains an AC/DC rectifier input stage which is a full-bridge operated with Totem-Pole modulation and an isolated DC/DC converter output stage consisting of a phase-shifted full bridge converter. This multi-cell ISOP configuration allows to share the input voltage among the converter cells and thus enables the use of low-voltage semiconductors with superior Figure-of-Merits throughout the converter cells. In addition, the cells can be operated in an interleaved fashion in order to increase the effective switching frequency of the entire system up to a multiple of a single converter cell's switching frequency. These advantages of the ISOP converter approach provide significant benefits in terms of reduced conduction and switching losses and smaller volumes of inductive components and heat sinks (2).

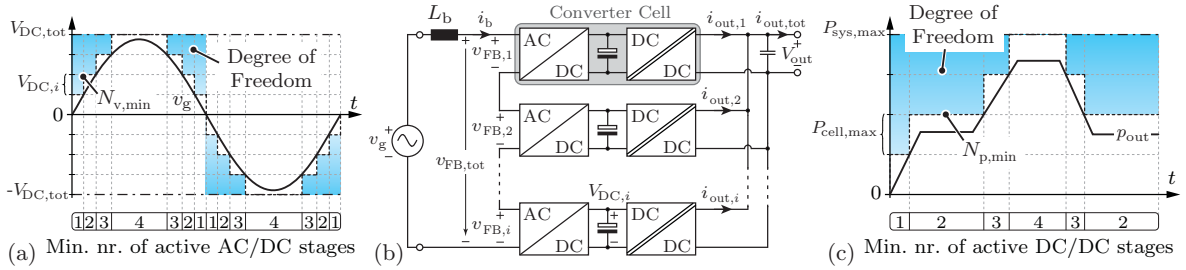

Fig. 1: 4D interleaving concepts (**(a)** and **(c)**) for an ISOP multi-cell telecom power supply module **(b)**. The available degrees of freedom in the operation of the system arise from the fact, that for each operating point of input voltage and output power only a certain minimum number of active AC/DC and DC/DC converter stages - $N_{\text{v,min}}$ and $N_{\text{p,min}}$ - is required. Any number of stages between the minimum and the maximum available number of cells can be operated at the **(a)** AC/DC and **(c)** DC/DC stages. Furthermore, the number of active cells can be different for both stages, as the DC-link capacitors employed in the cells decouple the power flow between the input and the output stages.

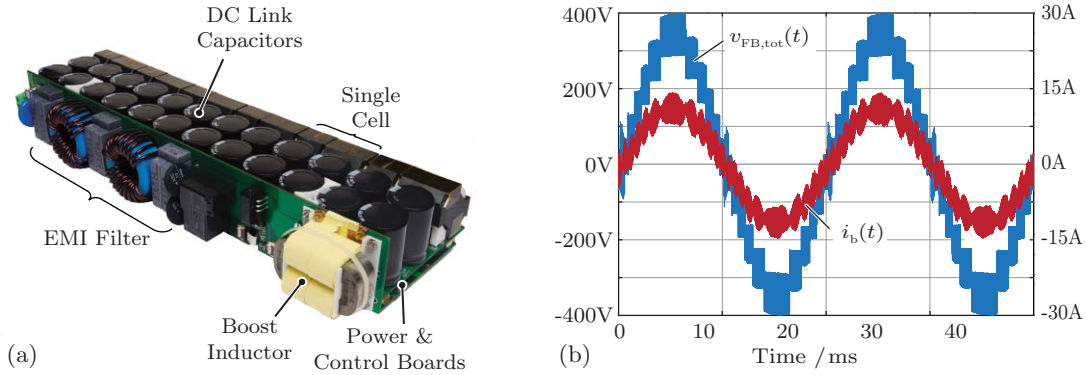

Fig. 2: (a) Hardware demonstrator of a multi-cell telecom power supply module (3) with $N_{\text{cells}} = 6$ cells and (b) measured waveform of the converter input voltage $v_{\text{FB,tot}}$ and the current i_{b} in the input side boost inductor for the operation with $N_{\text{PWM}} = 6$ PWM cells at a power level of $P_{\text{out}} = 1.5\,\text{kW}$.

The ISOP configuration itself can be considered as a spatial, i.e. 3-dimensional interleaving of multiple converter cells, where the cells are operated with a fixed operation mode and/or constant time-invariant interleaving. In this paper, a 4$^{\text{th}}$ dimension (4D) of interleaving the converter cells is introduced, where the operation mode (PWM vs. fundamental frequency modulation) and/or the number of active cells is varied over time depending on the input voltage and the load power level. In **Sec. 2** the basic degrees of freedom in the operation of the multi-cell converter of **Fig. 1(b)** which provide the possibility for 4D-interleaving are introduced. Furthermore, different 4D-interleaving concepts are proposed for the series connected AC/DC input stages and the parallel connected DC/DC output stages of the multi-cell system. In **Sec. 3** the best suited 4D-interleaving concepts are identified for both stages by means of a comprehensive Pareto-optimization and analytical derivations, respectively. Furthermore, the performance improvements are quantified in comparison to a conventional system control and a balancing scheme for the DC-link voltages is introduced.

2. 4D-Interleaving of ISOP Converters

For conventional 3D-interleaving multi-cell converter systems with ISOP configuration are usually operated with a common duty cycle for all AC/DC rectifier stages and all DC/DC converter stages, since this ensures an equal voltage sharing at the series connected inputs and an equal current sharing at the parallel connected outputs of the converter cells (4; 5).
However, this modulation scheme, does not take into account that the time-varying input voltage and load power in addition to the presence of large DC-link capacitors provide additional degrees of freedom for the operation of the system. Depending on the input voltage and output power, the number of active rectifier stages and output stages can vary over time as long as the following three conditions are fulfilled:

- *Input voltage*: At any given time the AC/DC rectifier stages have to provide a voltage $v_{\text{FB,tot}}(t)$ which is defined by the grid voltage, i.e. $v_{\text{g}}(t) \approx \overline{v}_{\text{FB,tot}}(t)$ over a switching period, where $\overline{v}_{\text{FB,tot}}(t) = \sum_{i=1}^{N_{\text{cells}}} \overline{v}_{\text{FB},i}(t) = \sum_{i=1}^{N_{\text{cells}}} V_{\text{DC},i} \cdot m_i(t)$ with m_{i} denoting the modulation index of a cell. This allows to derive a minimum number of active rectifier stages $N_{\text{v,min}}$ that are required for the operation of the system: $N_{\text{v,min}} = \left\lceil \frac{v_{\text{g}}(t)}{V_{\text{DC},i}} \right\rceil$ (cf. **Fig. 1(a)**).
- *Output current*: The total output current $i_{\text{out,tot}}(t)$ which is provided by the parallel connected DC/DC converters has to be equal to the load current, i.e. $i_{\text{load}}(t) = i_{\text{out,tot}}(t) = \sum_{i=1}^{N_{\text{cells}}} i_{\text{out},i}(t)$. Since each converter cell has a maximum power and thus also a maximum current rating $I_{\text{DC/DC,max}}$, a minimum number $N_{\text{p,min}}$ of converter cells required for the power transfer can be derived as $N_{\text{p,min}} = \lceil \frac{i_{\text{load}}(t)}{I_{\text{DC/DC,max}}} \rceil$ (cf. **Fig. 1(c)**).
- *DC link capacitors*: The DC-link capacitance is typically sized for a hold-up time requirement.

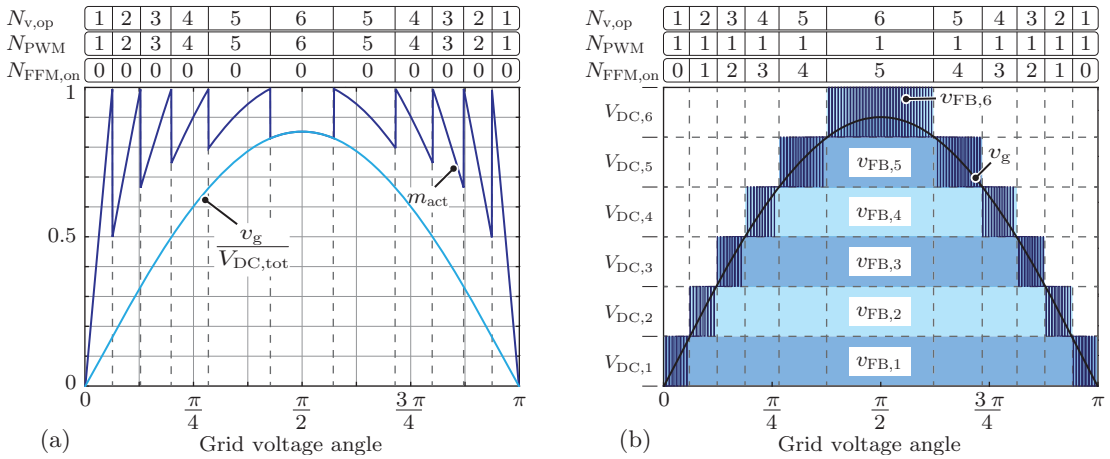

Fig. 3: Examples of the 4D-interleaving concepts for the series connected AC/DC rectifier stages: (a) operation with a variable number of PWM modules where all active rectifier stages ($N_{\text{v,op}}$) are operated with PWM with the same modulation index m_{act}. The minimum number of active PWM stages is set to $N_{\text{PWM,min}} = 1$; (b) operation with a fixed number of PWM stages (i.e. $N_{\text{PWM}} = 1$) where the remaining cells are operated with fundamental frequency and are either turned on or off ($N_{\text{FFM,on}} = N_{\text{v,op}} - N_{\text{PWM}}$).

Therefore, especially at low-power levels, this capacitance allows to have a power flow of the AC/DC rectifier stages that is different from the power flow of the DC/DC converters. The difference in the power flow is then stored in or supplied by the DC-link capacitors. This means, that the number of active AC/DC rectifier stages $N_{\text{v,op}}$ at a given time can be different from the number of active DC/DC converter stages $N_{\text{p,op}}$ as long as the net power flow of the DC-link capacitors of each cell is zero over a certain time interval, e.g. some milliseconds.

Based on the above mentioned degrees of freedom, a selection of modulation schemes making use of the 4th dimension of interleaving is presented in the following paragraphs.

2.1. AC/DC Rectifier Input Stages

The total sinusoidal cell input voltage $v_{\text{FB,tot}}$ can be distributed among the AC/DC rectifier stages in different ways. Apart from the number of active modules ($N_{\text{v,op}} \in [N_{\text{v,min}}, N_{\text{cells}}]$) the mode of operation of each active module can also be chosen. Namely, an active module can be either operated with PWM modulation or with fundamental frequency modulation (ON-OFF). Based on these degrees of freedom, two essentially different modulations schemes can be identified:

- *Variable number of PWM cells*: In this modulation scheme only the minimum number $N_{\text{v,op}} = N_{\text{v,min}}$ of required cells is operated with PWM while the remaining cells are turned off, as shown in **Fig. 3(a)**. This means, that the number of active cells, $N_{\text{v,op}}$, changes with the time-varying value of the grid voltage. All active cells are operated with a fixed frequency PWM, i.e. $N_{\text{PWM}} = N_{\text{v,op}}$, with the same modulation index and a phase shift between the cells which depends on the number of active cells, $\phi = 360°/N_{\text{PWM}}$. This leads to a varying effective switching frequency due to the varying number of active cells. In order to limit the difference between the maximum and minimum effective switching frequency, a lower limit for the number of active PWM cells, $N_{\text{PWM,min}}$, can be defined.
- *Fixed number of PWM cells*: Instead of changing the number of PWM cells during a grid cycle, this modulation scheme operates with a defined number of PWM cells at all times ($N_{\text{PWM}} = \text{const}$), as depicted in **Fig. 3(b)** for the case of a single PWM cell ($N_{\text{PWM}} = 1$). The remaining cells are operated with fundamental frequency which means they are either turned on or off ($N_{\text{FFM,on}} = N_{\text{v,op}} - N_{\text{PWM}}$). As a result, in this operation mode only a fixed number of cells (N_{PWM}) exhibits switching losses, whereas the other cells only have conduction losses. A disadvantage, however, is the reduced effective switching frequency which requires an increase of the boost inductance value in order to limit the peak-to-peak current ripple of the

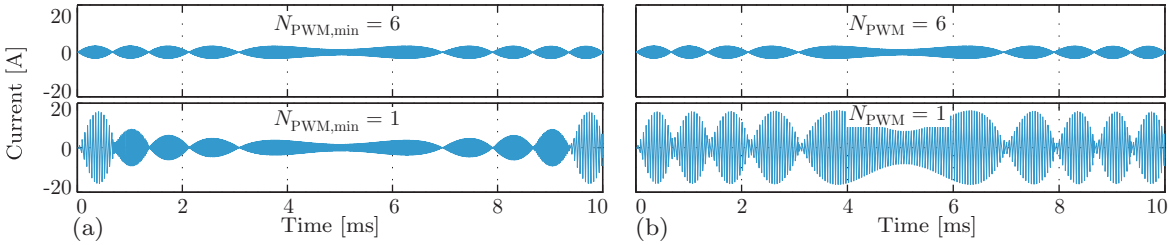

Fig. 4: Comparison of simulated boost inductor current ripple waveforms (i.e. current i_{b} without the $50\,\mathrm{Hz}$ low frequency component) for different 4D-interleaving schemes: (a) variable number of PWM modules ($N_{\mathrm{PWM,min}}$ denotes the minimum number of active PWM modules); (b) fixed numbers N_{PWM} of PWM modules where the remaining cells are operated as fundamental frequency modules. (System with 6 cells and a switching frequency of the PWM cells of $f_{\mathrm{sw,PWM}} = 20\,\mathrm{kHz}$, a boost inductance of $L_{\mathrm{b}} = 25\,\mu\mathrm{H}$, and a DC-link voltage of each cell of $V_{\mathrm{DC,cell}} = 66\,\mathrm{V}$.)

input current.

For all of the above cases, the instantaneous cell power values are unequal and the individual DC-link capacitor voltages inherently fluctuate. Thus, it is required to properly permute the operation of the cells, e.g. by cyclically changing the selection of PWM cells. Especially, in order to achieve an accurate cancellation of harmonics by interleaving multiple PWM cells, the DC-link voltages of these PWM cells should be kept as close as possible to the same value.

2.2. DC/DC Converter Output Stages

Similarly to the voltage distribution among the input side series connected AC/DC converter stages the output current can be distributed in different ways among the parallel connected DC/DC converter output stages:

- *Equal current sharing*: The number of active DC/DC stages varies depending on the output current. All cells are operated with the same current reference value and therefore equally share the output current. The current reference of a single cell can be calculated by dividing the total output current by the number of active cells. As a drawback, however, the current reference of each cell will exhibit a step change every time the number of active cells changes, which requires a highly dynamic current controller in each cell.
- *Unequal current sharing*: In this modulation scheme the output current is unequally divided among the active cells. This might be achieved e.g. if an additional cell is only activated when the previously actived cell has reached its maximum current value. This has the advantage that the current reference values of all cells are continuously changed over time without any step changes (under the assumption that there are no load steps). As a drawback, the stress on the DC-link capacitors is heavily unbalanced as some cells operate at their maximum power levels while others are in stand-by mode.

A minimum number of DC/DC converter stages can be defined to reduce the total current ripple at the output by interleaving the active DC/DC converter stages. This can be applied to both concepts, since the current ripple at the output of an individual cell is independent from the current level of the cell (i.e. the average value of the output current). Thus, even the interleaving of two cells with unequal current sharing reduces the output current ripple.

3. Simulation and Optimization Results

In this chapter the different 4D-interleaving modulation schemes are comparatively evaluated in order to identify the best possible modulation schemes for the AC/DC and the DC/DC converter stages. In the following, the 4D-interleaving modulation schemes are applied to an ISOP multi-cell telecom power supply module with $N_{\mathrm{cells}} = 6$ converter cells where each cell has a rated power

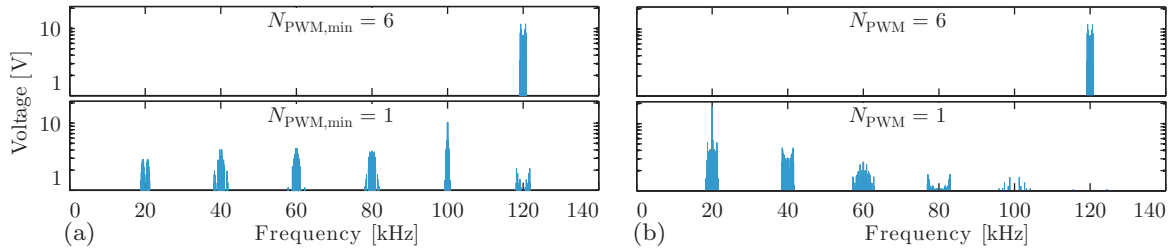

Fig. 5: Comparison of the harmonic spectrum of the input voltage $v_{\text{FB,tot}}$ of the series connection of AC/DC converter cells (without the $50\,\text{Hz}$ low frequency component) for different 4D-interleaving schemes: (a) variable number of PWM modules ($N_{\text{PWM,min}}$ denotes the minimum number of active PWM modules); (b) fixed numbers of PWM modules N_{PWM} where the remaining cells are operated as fundamental frequency modules. (System with 6 cells and a switching frequency of the PWM cells of $f_{\text{sw,PWM}} = 20\,\text{kHz}$ and a DC-link voltage of each cell of $V_{\text{DC,cell}} = 66\,\text{V}$.)

level of $P_{\text{rat}} = 550\,\text{W}$ and a DC-link capacitance of $C_{\text{DC}} = 8.8\,\text{mF}$ with a nominal DC-link voltage of $V_{\text{DC,cell}} = 66\,\text{V}$.

3.1. AC/DC Converter Stages

The modulation scheme of the AC/DC stages takes direct influence on the harmonic spectrum of the input current waveform, the RMS value of the input current, and also on the total switching losses. The effect of the selected modulation scheme on the input current waveform is shown for both modulation schemes (variable and fixed numbers of PWM cells) in **Fig. 4** for two selected scenarios. The modulation with a variable number of PWM modules and a value of $N_{\text{PWM,min}} = 6$ is equal to the operation with a fixed number of $N_{\text{PWM}} = 6$ cells which is the standard 3D interleaving operation as measured in **Fig. 2(b)**.
The harmonic spectrum of the generated converter input voltage is shown for both of the aforementioned modulation schemes in **Fig. 5**. It can be seen that the modulation with the variable number of PWM modules (**Fig. 5(a)**) leads to a more even distribution of the switching frequency harmonics over the frequency range, due to its varying effective switching frequency.
As a remark, for the generation of the plots in **Fig. 4** and **Fig. 5** the DC/DC stages were operated with conventional (3D) modulation where all stages are activated and equally share the total output power.
Since the choice of the modulation scheme affects several system parameters, a comprehensive optimization of the entire input stage comprising the EMI filter, the boost inductor and the MOSFET chip area of the AC/DC full bridges has to be performed to take into account the dependencies between the different elements and the modulation schemes. This optimization allows to identify the Pareto-limit of the trade-off between efficiency and power-density of the entire rectification stage by considering all available degrees of freedom given for the design:

- *EMI filter*: Regardless of the selected modulation scheme, the system has to comply with the CISPR Class B directive which specifies limits for the noise emissions in the frequency range of $f_{\text{CISPR}} = 150\,\text{kHz} - 30\,\text{MHz}$. This requires the calculation of the harmonic spectrum for each modulation scheme and the identification of the Pareto-optimal filter designs which can be found by considering different degrees of freedom like the number of filter stages and the choice of different values for the filter elements.
- *Boost Inductor*: The value of the boost inductance is another optimization parameter since a small value leads to a large input current ripple which increases the RMS value and also the losses of the inductor and conduction losses of the MOSFETs. However, a large current ripple also results in lower switching losses of the MOSFETs as the hard-switching instants occur at lower current levels. In addition, the design of the boost inductor represents a Pareto-optimization problem by itself as for a given set of electrical parameters different inductor designs can be found due to the possibility of employing e.g. different types of core material, core shapes, winding types (e.g. litz or foil windings), number of turns and air gap lengths.

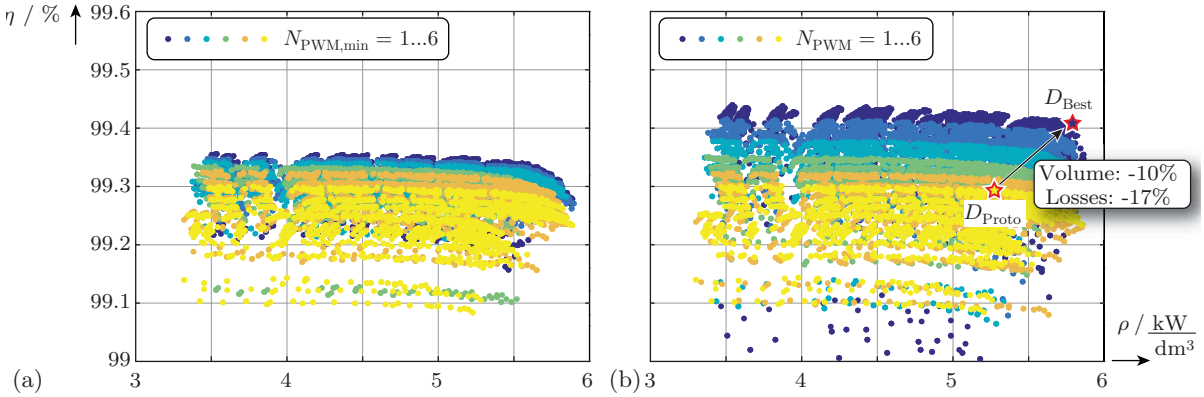

Fig. 6: η-ρ efficiency vs. power-density Pareto-optimization results of the entire rectification stage (incl. EMI filter, boost inductor, AC/DC full bridges, and DC-link capacitors): (a) Performance trade-off with a variable number of PWM cells for different minimum numbers $N_{\text{PWM,min}}$ of PWM cells, and (b) performance space for a fixed number N_{PWM} of PWM cells where the remaining cells are operated with fundamental frequency modulation. Compared to a conventional approach employed in the prototype system (D_{Proto}, $N_{\text{PWM}} = 6$) a selected design on the Pareto-front (D_{Best}, $N_{\text{PWM}} = 1$) shows 10% lower total volume and 17% lower losses.

- *Switching Frequency*: The switching frequency directly impacts the switching losses but also the shape of the input current for a given boost inductance. This also has an effect on the inductor design and the EMI filter design. Regarding the MOSFETs, a high switching frequency leads to larger switching losses but to a lower current ripple and thus to a lower current RMS value which decreases the conduction losses.
- *MOSFET Chip Areas*: The chip area selection of the MOSFETs allows to trade-off conduction losses which decrease with a larger chip area and (turn-on) switching losses which increase with a larger chip area.

The results of the Pareto-optimization of the entire rectification stage, including the EMI filter, boost inductor, full-bridge MOSFETs of the AC/DC stages, DC-link capacitors (selected for a hold-up time of $t_{\text{holdup}} = 10\,\text{ms}$), resistive PCB losses, and constant control losses, for operation at rated power ($P_{\text{rat}} = 3.3\,\text{kW}$) are plotted in **Fig. 6(a)** and **6(b)** for the modulation scheme with a variable number of PWM modules and the modulation scheme with a fixed number N_{PWM} of PWM modules, respectively. It can be concluded that the highest performance can be achieved by operating only one cell with PWM and the remaining cells with fundamental frequency modulation. Compared to the design of the hardware demonstrator (D_{Proto})(3) with a continuous operation of $N_{\text{PWM}} = 6$ cells, the 4D-interleaving concept allows to simultaneously improve the efficiency and the power density of the rectification stage; the losses are reduced by -17% and the volume by -10%, as shown for design D_{Best} in **Fig. 6(b)**. More details about both designs can be found in **Tab. 1**.

3.2. DC/DC Converter Stages

For the parallel connected DC/DC converter stages the most efficient 4D interleaving modulation scheme can be analytically derived by assuming a generic loss function of each DC/DC converter

Tab. 1: Comparison of the parameters of the AC/DC converter stages of the prototype design D_{Proto} and the Pareto-optimal 4D-interleaving design D_{Best} (cf. Fig. 6).

Variable	D_{Proto}	D_{Best}
N_{PWM}	6	1
$f_{\text{sw,PWM}}$	$20\,\text{kHz}$	$24\,\text{kHz}$
L_{b}	$25\,\mu\text{H}$	$90\,\mu\text{H}$
EMI Filter Stages	3	3
Parallel MOSFETs	2	5

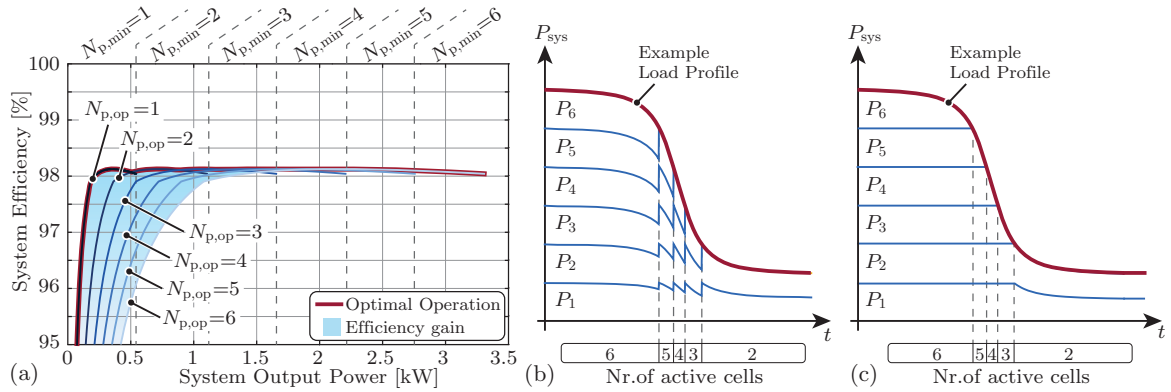

Fig. 7: 4D-interleaving of the parallel connected DC/DC converter stages of an ISOP system with $N_{\text{cells}} = 6$ converter cells which leads to a higher part-load efficiency (cf. (a)) by always operating only a subset of converter cells. (b) Operation mode with equal power reference values for all active cells which results in discontinuous changes of the power levels of the individual active cells. (c) Alternative operation with unequal power levels of the converter cells but smooth changes of the power levels of the individual cells.

depending on the output power as

$$p_{\text{loss},i} = k_0 + k_1 \cdot p_{\text{out},i} + k_2 \cdot p_{\text{out},i}^2 \tag{1}$$

where k_0 models the constant losses (e.g. auxiliary power), $k_1 \cdot p_{\text{out},i}$ the linearly dependent losses (e.g. a diode voltage drop) and $k_2 \cdot p_{\text{out},i}^2$ the quadratically dependent losses (e.g. resistive losses). The total losses of the DC-DC converter stage comprising N DC/DC converters can thus be written as

$$p_{\text{losses,tot}} = N \cdot k_0 + k_1 \cdot \sum_{i=1}^{N} p_{\text{out},i} + k_2 \cdot \sum_{i=1}^{N} p_{\text{out},i}^2 \,. \tag{2}$$

By applying the Lagrangian method to the minimization problem of (2) under the constraint of $p_{\text{out,tot}}(t) = \sum_{i=1}^{N_{\text{cells}}} p_{\text{out},i}(t)$ following solution can be found for the general case

$$p_{\text{out,1,opt}} = p_{\text{out,2,opt}} = \ldots = p_{\text{out,N,opt}} = \frac{p_{\text{out,tot}}}{N} \tag{3}$$

under which the total losses are minimized. By inserting the solution of (3) in (2) the total losses can be calculated as

$$p_{\text{losses,tot}} = N \cdot k_0 + k_1 \cdot p_{\text{out,tot}} + k_2 \cdot \frac{p_{\text{out,tot}}^2}{N} \,. \tag{4}$$

The remaining optimization parameter is the optimum number of active DC-DC converters $N = N_{\text{opt}} \in [N_{\text{p,min}}, N_{\text{cells}}]$ used for the power transfer for maximum efficiency. By differentiating (4) with respect to N and setting the derivative equal to zero, the optimal number of active cells can be found as

$$N_{\text{opt}} = \sqrt{\frac{k_2}{k_0}} \cdot p_{\text{out,tot}} \,. \tag{5}$$

Since the number N_{opt} is typically a rational number, the two nearest integer values have to be considered and the integer value which still satisfies $N_{\text{opt,int}} \in [N_{\text{p,min}}, N_{\text{cells}}]$ and leads to lower losses according to (4) has to be considered. If none of the nearest integer values satisfies the condition of $N_{\text{opt,int}} \in [N_{\text{p,min}}, N_{\text{cells}}]$ (typically for systems with larger constant losses than quadratic losses, i.e. $k_0 \gg k_2$), the value of $N_{\text{opt,int}} = N_{\text{p,min}}$ has to be chosen.
As a conclusion, this means, that the most efficient 4D-interleaving modulation scheme for the parallel connected DC/DC stages is obtained by equally sharing the total power and/or the total output current among the active DC/DC cells. This allows to extend the level of highest efficiency also to very low power levels as shown in **Fig. 7(a)** for the multi-cell telecom rectifier of **Fig. 2(a)**.

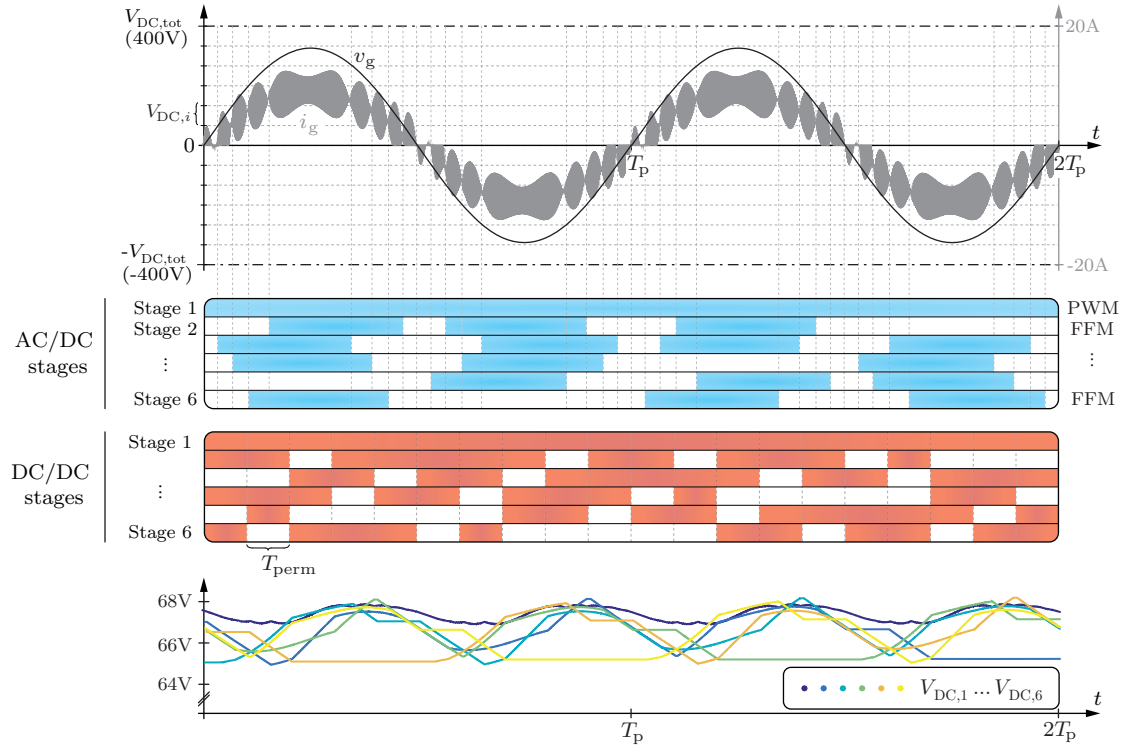

Fig. 8: Simulation results of the 4D-interleaving modulation of the ISOP multi-cell telecom rectifier system with $N_{\text{cells}} = 6$ at the operating point of $P_{\text{out}} = 1.5\,\text{kW}$. At the input side only one AC/DC stage (Stage 1) is modulated with PWM while the remaining five stages are operated with fundamental frequency modulation (FFM). At the selected power level of $P_{\text{out}} = 1.5\,\text{kW}$ the most efficient operation of the DC/DC stages is achieved with $N_{\text{p,op}} = 4$ active DC/DC stages. The balancing algorithm selects the active AC/DC and DC/DC stages based on the DC-link voltages of the cells. The permutation time interval for the DC/DC stages is chosen as $T_{\text{perm}} = 2\,\text{ms}$.

Compared to the standard modulation where all six DC/DC stages are operated at all power levels, significant efficiency gains can be achieved at power levels below 30% of the rated power $P_{\text{rat,tot}}$. In order to avoid step changes of the power reference values of the cells every time the number of cells changes (cf. **Fig. 7(b)**) it is preferable to allow unequal reference values during transient load changes (cf. **Fig. 7(c)**).

3.3. DC-Link Voltage Balancing

The 4D-interleaving modulation schemes lead to an unequal stress of the DC-link capacitors since, on the one hand, at low input voltages and output power only a fraction of the AC/DC stages and DC/DC stages is active at a given time and, on the other hand, the number $N_{\text{v,op}}$ of active AC/DC input stages can be different from the number $N_{\text{p,op}}$ of active DC/DC output stages. Thus, in order to balance the DC-link voltages during the operation with 4D-interleaving a proper permutation algorithm has to be employed which activates/deactivates the AC/DC and DC/DC stages of the cells in such way that a minimal voltage ripple on the DC-link capacitors is obtained.
One possible permutation algorithm for the AC/DC stages is described below for a system with $N_{\text{cells}} = 6$ converter cells and a fixed number of $N_{\text{PWM}} = 1$ PWM AC/DC stages and $N_{\text{FFM}} = 5$ AC/DC stages with fundamental frequency modulation (FFM). In contrast to the balancing scheme proposed in (6), the AC/DC stage which is selected for PWM operation is always the uppermost cell in the stack of converter cells, i.e the cell which is connected to the input side boost inductor L_{b}, since this minimizes the common-mode currents in the system caused by the switching operation of the PWM cell. The proposed permutation algorithm works in such way, that an additional FFM AC/DC stage is activated every time the modulation index of the PWM cell reaches its upper limit and is deactivated when the lower limit of the modulation index of the PWM stage is

reached, similar to the concept shown in **Fig. 3(b)**. The decision about which FFM AC/DC stage to activate/deactivate is based on the deviation of the DC-link voltages of the cells from the set-point voltage ($V_{\text{DC,set}} = 400\,\text{V}/N_{\text{cells}}$) in such a way that the AC/DC stage of the cell with the lowest DC-link voltage is always the next one to be activated and the AC/DC stage of the cell with the highest voltage is the next one to be deactivated.
Apart from the AC/DC stages of the cells the DC/DC stages can also be utilized for DC-link voltage balancing by means of permutation. For a system which operates at a constant power level, however, there is no natural event when DC/DC stages have to be activated/deactivated like there is for the AC/DC stages, due to the time-varying input voltage. Thus, a constant time interval of e.g. $T_{\text{perm}} = 2\,\text{ms}$ is chosen after which the selection of active stages is re-evaluated based on the DC-link voltage values of the cells. This means, that the DC/DC stages of the $N_{\text{p,op}}$ cells with the highest DC-link voltages are activated.
Consequently, the balancing of the DC-link voltage is achieved by permutation of the active AC/DC and DC/DC stages which is shown in **Fig. 8** for the operation at a constant output power level of $P_{\text{out,tot}} = 1.5\,\text{kW}$ where the most efficient operation is achieved with $N_{\text{p,op}} = 4$ active DC/DC stages. As can be seen, the ISOP system can be operated in a stable condition with 4D-interleaving at the AC/DC and DC/DC stages while the DC-link voltages are effectively balanced with only small deviations of around a maximum of $\Delta V_{\text{DC}} \approx 3\,\text{V}$.

4. Conclusions

A new dimension of interleaving the operation of the converter cells of an ISOP multi-cell telecom power supply module is presented. The proposed concept is based on a time-varying activation/deactivation of individual AC/DC input and DC/DC output stages of different cells and utilizes the decoupling of the input and output sides of the cells provided by the energy storage capability of the DC-link capacitors. Different 4D-interleaving operation schemes are discussed for the series connected AC/DC stages and the parallel connected DC/DC stages and evaluated by means of a comprehensive η-ρ Pareto optimization and analytical calculations. Compared to the standard 3D-interleaving the losses of the entire rectifier stage can be reduced by 17% and the volume can be decreased by 10% and a very flat efficiency vs. output power characteristic of the parallel connected DC/DC converter stages can be achieved.
Considering the increasing importance of higher part-load efficiency of telecom power supplies, the multi-cell converter approach in combination with the proposed 4D-interleaving concept therefore provides an interesting solution for future implementations.

5. References

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