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Synergetic Control of a Three-Phase Buck-Boost Current DC-Link Bidirectional EV Battery Charger Considering Wide Output Range and Irregular Mains Conditions

D. Zhang,
M. Guacci,
J. W. Kolar,
J. Everts

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Synergetic Control of a 3-Φ Buck-Boost Current DC-Link EV Charger Considering Wide Output Range and Irregular Mains Conditions

Daifei Zhang*, Mattia Guacci*, Johann W. Kolar*, and Jordi Everts§
*Power Electronic Systems Laboratory, ETH Zurich, Switzerland
§Prodrive Technologies B.V., Son, The Netherlands

***Abstract*—A wide output voltage range EV charger employing a three-phase (3-Φ) buck-type current source rectifier (CSR)-stage and a series-connected boost-type DC/DC-stage is introduced. The system employs a novel control structure, enabling robust operation even under heavily unbalanced 3-Φ mains conditions. It is verified how the proposed concept achieves PFC operation while regulating the output voltage in a wide range, which requires both buck and boost functionality. This includes a synergetically combined control of the 3-Φ CSR input stage and of the subsequent DC/DC output stage. In this context, a variable DC-link current control strategy referred to as 2/3-PWM is implemented, which allows to switch only two out of the three phases of the CSR-stage. Moreover, seamless transitions between the different operating modes and modulation schemes are demonstrated for different output voltage regions. Finally, the performance of the proposed synergetic control structure is comprehensively validated with closed-loop circuit simulations, focusing on buck-boost operation and on irregular 3-Φ mains conditions, including harmonics distortion, phase loss (phase open-circuit or phase zero-voltage faults), and voltage spikes.**

***Index Terms*—Three-Phase Buck-Boost Current DC-Link PFC Rectifier System, Three-Phase Buck-Type Current Source Rectifier, Synergetic DC-Link Current Control, Irregular Mains Conditions, Mains Voltage Failures, Mains Overvoltage.**

I. Introduction

EFFICIENT and robust battery charging power converters are key enablers to accelerate the world's transition to emission-free road transport [1]. In particular, DC fast (or Level 3) charging technologies, where the high-voltage (HV) DC battery of an EV is directly connected to a DC charging station bypassing the on-board battery charger, are conveniently reducing the charging times to few minutes, since charging power levels up to hundreds of kW are available off-board [2]. In order to allow the use of standard AC protection devices [3], typical Level 3 EV charging stations are employing an AC power distribution bus, which is supplied by the low-voltage secondary windings of a three-phase (3-Φ) medium-voltage distribution transformer. Each charging port consists of a 3-Φ AC/DC Power Factor Correction (PFC) rectifier front-end and a downstream isolated DC/DC converter which finally impresses the EV battery charging current. Since different EV manufactures adopt different nominal battery voltages, e.g. 360 V [4] or 800 V [5], commercial Level 3 charging stations must cover a wide output voltage range, e.g. from 150 V to 920 V [6]. However, when the isolated DC/DC converter is conveniently realized as series resonant converter, which offers high-efficiency but limited output voltage controllability [7], the sole 3-Φ AC/DC front-end must cover the required output voltage range, i.e. must necessarily offer both buck and boost functionality considering a 400 V (line-to-line, RMS) supplying mains. Additionally, the PFC rectifier system must generate a stable DC output voltage and supply the required output power, possibly also under irregular 3-Φ mains conditions, e.g. in case of harmonics distortion, voltage spikes, under-voltage events, or even voltage dips and phase loss [8]. Finally, according to the developing vehicle-to-grid (V2G) trend [9], where EVs should serve as distributed energy storage elements to support the grid operation, the 3-Φ AC/DC front-end should allow bidirectional power transfer.

The resilient operation of a 3-Φ buck-boost (bB) current DC-link PFC rectifier system (see **Fig. 1**), formed by a 3-Φ buck-type current source rectifier (CSR) [11] input stage and a subsequent boost-type DC/DC output stage, has been discussed in [12] for heavily unbalanced 3-Φ mains conditions. The 3-Φ buck CSR-stage offers several advantages compared to a conventional boost-type approach, hence, it is of high interest for robust EV chargers requiring a wide output voltage range. In particular, it tolerates overvoltage transients occurring in the 3-Φ mains, employs a reduced number of magnetic components, and features a sinusoidally varying switched voltage which reduces the occurring switching losses [13]. Furthermore, the boost-type DC/DC output stage enables a variable DC-link current control strategy (2/3-PWM) [14], [15], where sinusoidal 3-Φ input currents are generated by switching only two out of the three phases of the CSR-stage, resulting in a significant efficiency improvement. Moreover, a three-level (3-L) characteristic of the boost stage extends the output voltage range with reduced switching losses and minimized DC-link inductor size.

These findings motivate the analysis of a synergetic control structure (cf. **Fig. 2**) which ensures the robust operation of the 3-Φ bidirectional bB current DC-link PFC rectifier system as subject of this paper. The focus is on the applicability of 2/3-PWM under different unbalanced and distorted 3-Φ mains conditions and on the seamless transition between different operating modes, i.e. buck and boost mode, and corresponding modulation schemes, i.e. conventional PWM (3/3-PWM) and 2/3-PWM. The converter topology and its operating principle are briefly introduced in **Section II**. The proposed control concept, which satisfies all mentioned requirements without switching between different feedback structures, is described in **Section III** and its performance is validated in **Section IV** with the support of simulation results.

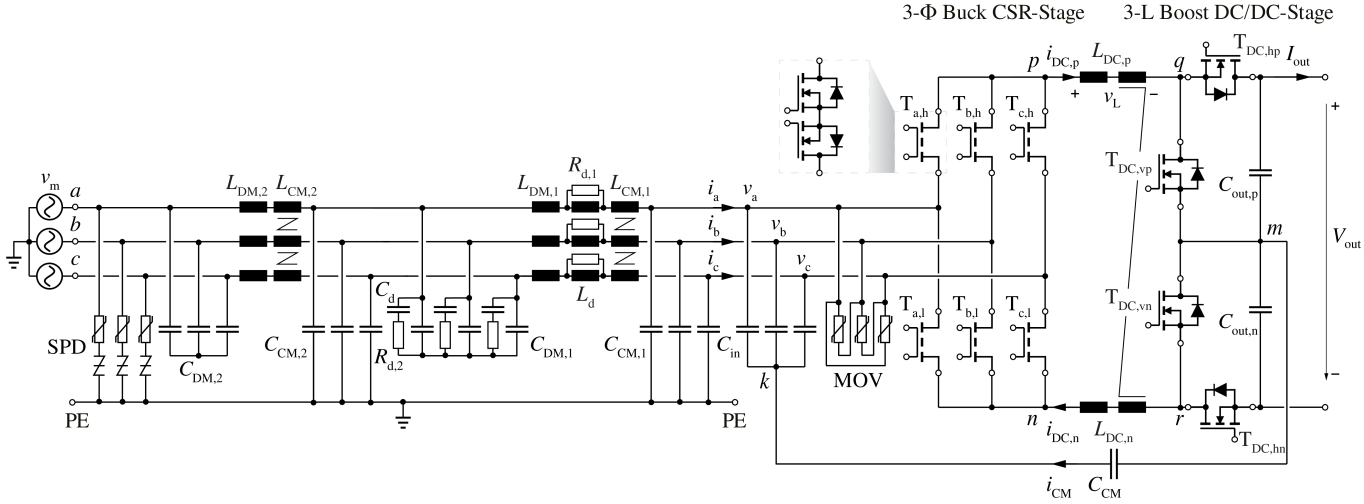

Fig. 1: Analyzed three-phase (3-Φ) bidirectional buck-boost (bB) current DC-link PFC rectifier system (specifications according to **Tab. I**). A TN-C mains structure, where the protective earth and the neutral conductors are combined, is considered [10].

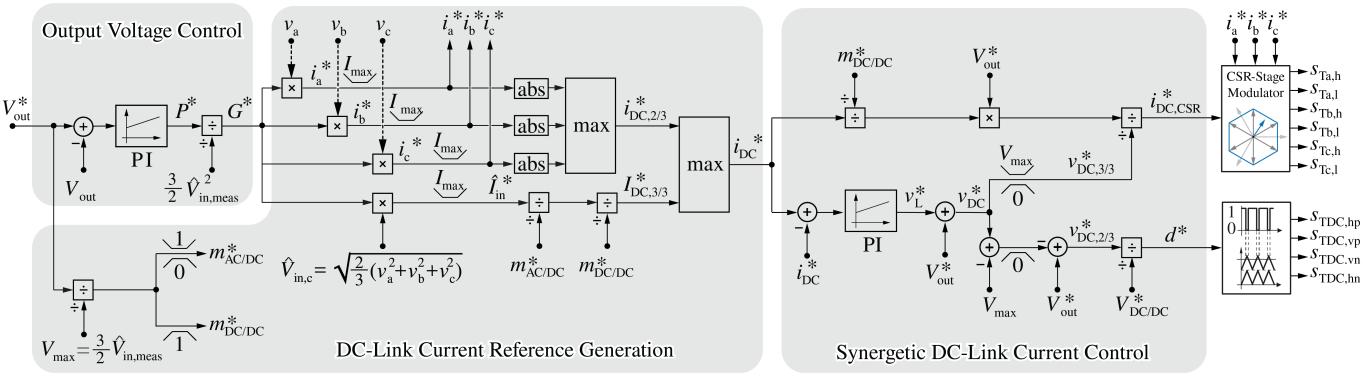

Fig. 2: Block diagram of the proposed synergetic control of the converter system shown in **Fig. 1** (voltages v_a, v_b, and v_c measured with reference to the star point of the input filter capacitors C_{in}). The three main blocks forming the control structure, i.e. the *Output Voltage Control*, the *DC-Link Current Reference Generation*, and the *Synergetic DC-Link Current Control*, enable PFC operation with sinusoidal 3-Φ input currents i_a, i_b, and i_c in phase with the sinusoidal 3-Φ mains voltages $v_{m,a}$, $v_{m,b}$, and $v_{m,c}$, regulation of V_{out}, control of the DC-link current i_{DC} with synergetic operation of the 3-Φ CSR-stage and of the boost-type DC/DC-stage, and seamless transitions between the different operating modes, i.e. buck and boost mode, and the corresponding modulation schemes, i.e. conventional PWM (3/3-PWM) and 2/3-PWM.

Finally, **Section V** concludes this paper.

II. Converter Topology and Operating Principle

The analyzed 3-Φ bidirectional bB current DC-link PFC rectifier system, connecting the 3-Φ AC mains to a DC load, features a two-stage converter structure (see **Fig. 1**, specifications according to **Tab. I**), includes a two-stage EMI filter, and employs a 3-L boost-type DC/DC output stage. Each phase of the supplying 3-Φ mains is modeled as a voltage source, which is connected directly to the input of the EMI filter, together with an overvoltage protection network consisting of surge protection devices (SPDs) [16] and metal-oxide varistors (MOVs) [17]. The CSR-stage is realized with six switches offering bidirectional voltage blocking capability and controlled bidirectional current flow, obtained each with an anti-series connection of two 1200 V SiC power MOSFETs. The DC-link inductor connects the CSR-stage with the 3-L DC/DC-stage. Both stages operate with the same switching frequency, $f_{sw} = 100\,\text{kHz}$ [18]. Finally, the artificial 3-Φ neutral point k formed by the CSR-stage input filter capacitors C_{in} and the DC output voltage mid-point m are connected through a common-mode (CM) filter capacitor C_{CM} to ensure low CM noise emission at the output.

The two stages operate synergetically to cover the wide output voltage range, as shown in **Fig. 3** [19]. The converter starts operating in ***Boost-Mode*** $\left(V_{out} > \hat{V}_{m,ll}\right)$ at $t = 0$. The DC-link current (**(b)** - black) is shaped and/or regulated by the DC/DC-stage (see **(c)** and **(d)**). The CSR-stage operates with 2/3-PWM (only two out of three phases are switching within one switching period) to reduce the switching losses [15], while the DC/DC-stage continuously switches to step up the 3-Φ mains voltage. When the output voltage (**(a)** - blue) decreases from 1000 V to 200 V, the controller seamlessly transitions to ***Buck-Mode*** $\left(V_{out} < \frac{\sqrt{3}}{2}\hat{V}_{m,ll}\right)$, where the DC-link current (**(b)** - black) is regulated only by the CSR-stage, which continuously switches to step down the 3-Φ mains voltage (see **(c)**) operating with 3/3-PWM (all three phases are switching during one switching period), while the DC/DC-stage is clamped ($T_{DC,hp}$ and $T_{DC,hn}$ are permanently conducting, see **(d)**), hence, no switching losses occur in the DC/DC-stage.

In summary, the synergetic operation of the two stages enables a significant performance improvement, since either the DC/DC-stage is clamped (***Buck-Mode***) or the CSR-stage is

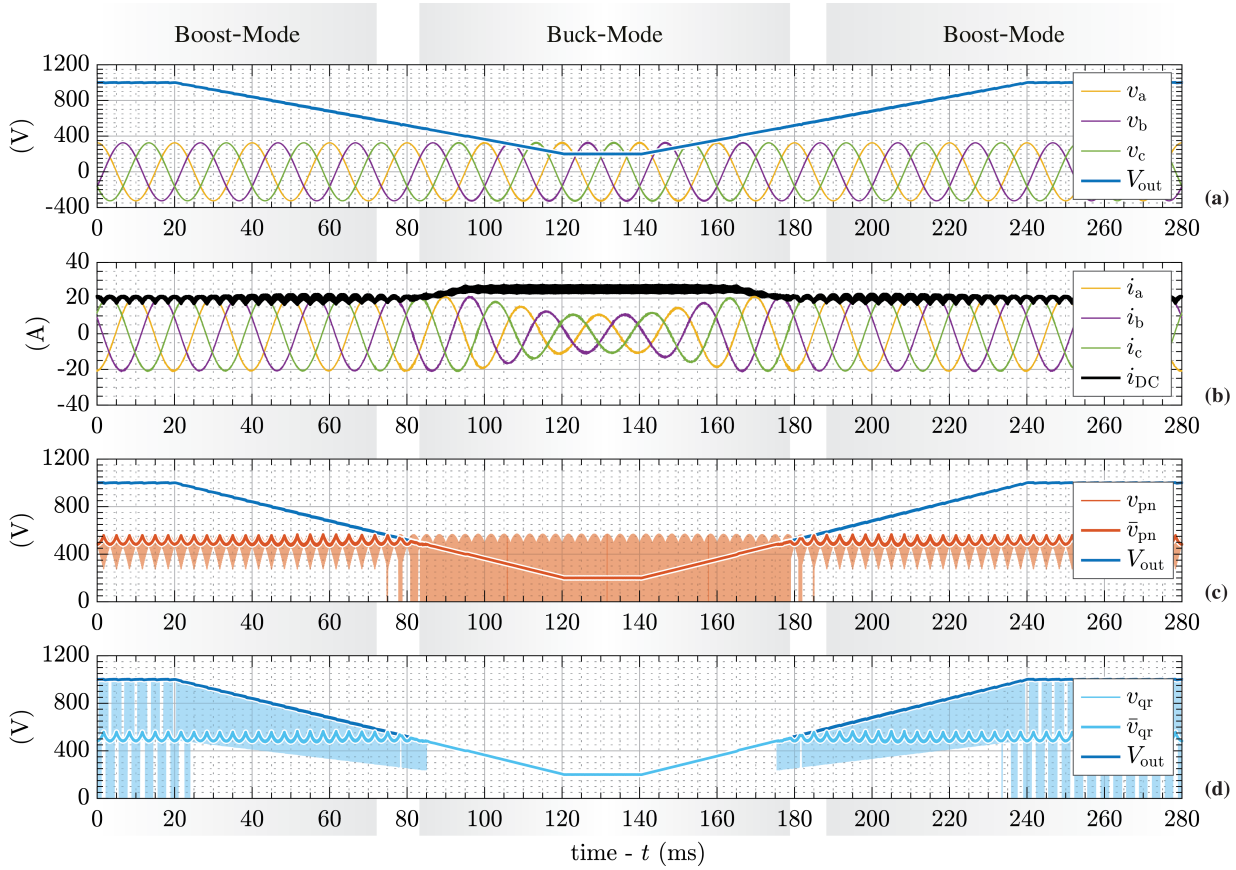

Fig. 3: Simulated waveforms of the analyzed converter (cf. **Fig. 1** and **Fig. 2**) in case of widely varying output voltage ($P_{out} = 10\,\text{kW}$ operation for $400\,\text{V} < V_{out} < 1000\,\text{V}$, $I_{out} = 25\,\text{A}$ for $V_{out} < 400\,\text{V}$). In particular, in **(a)** the 3-Φ sinusoidal input voltages v_a, v_b, and v_c, and the output voltage V_{out}, in **(b)** the 3-Φ sinusoidal input currents i_a, i_b, and i_c, and the DC-link current i_{DC}, in **(c)** the switched v_{pn} and average $\bar{v}_{pn}$ output voltage of the CSR-stage, and in **(d)** the switched v_{qr} and average $\bar{v}_{qr}$ input voltage of the DC/DC-stage are shown. The simulation covers a wide output voltage range forcing the converter to operate in different modes, and thus presents the synergetic operation of the CSR-stage and the DC/DC-stage.

operated with 2/3-PWM (***Boost-Mode***). Moreover, the CSR-stage always operates with the largest possible modulation index, minimizing the overall conduction losses.

Besides nominal 3-Φ mains conditions, the converter is also required to operate with unbalanced and/or distorted mains, and even should tolerate a phase loss, i.e. the controller should also guarantee stable 1-Φ (two line) operation. For all these conditions, uncontrolled DC-link currents, which potentially could damage the switches and trigger protection circuits, should be avoided, while the nominal output power should be continuously supplied and the desired output voltage level should be maintained. Detailed requirements and specifications for a converter operation with irregular mains conditions are listed in different standards, e.g. for harmonics distortion in *IEC 61000-2-4* [20], for mains voltage dips in *IEC 61000-4-34* [21], and for mains overvoltages in *IEC 61000-4-5* [22] (see **Section IV**).

III. Synergetic Control Structure

The proposed synergetic control structure, shown in **Fig. 2**, is described in this section highlighting its three main functional blocks, i.e. the *Output Voltage Control*, the *DC-Link Current Reference Generation*, and the *Synergetic DC-Link Current Control*. The control ensures an automatic selection of, and a natural transition between the individually optimal operating modes and/or modulation schemes, which minimizes the overall conduction and switching losses for each operating condition. For simplicity, even though this converter system could operate for any phase displacement of mains voltage and mains current and/or power factor, only ohmic mains behavior, i.e. PFC rectifier operation, is discussed herein.

A. Output Voltage Control

The first control block implements the *Output Voltage Control* (cf. **Fig. 2**), which defines the input power reference P^* through a PI-controller considering the difference between the actual V_{out} and the reference output voltage V_{out}^*. Hence, by measuring the peak value of the 3-Φ mains voltages $\hat{V}_{in,meas}$ (constant over one mains period even for unbalanced mains conditions), the converter input conductance reference

$$G^* = \frac{P^*}{\frac{3}{2}\hat{V}_{in,meas}^2}, \tag{1}$$

is calculated and fed into the following block responsible for the *DC-Link Current Reference Generation*.

B. DC-Link Current Reference Generation

In order to achieve PFC rectifier operation, the 3-Φ mains current references i_a^*, i_b^*, and i_c^* are set proportional to the corresponding 3-Φ input voltages v_a, v_b, and v_c ($v_i \approx v_{m,i}$, $i = a, b, c$, for symmetrical sinusoidal mains), and are limited to I_{max} to ensure safe operation of the power semiconductors

and to avoid a saturation of the DC-link inductor L_{DC}. The instantaneous values i_{a}^*, i_{b}^*, and i_{c}^* provide the sector information for the space vector modulator of the CSR-stage [15], while the upper envelope of the absolute values,

$$i_{\mathrm{DC,2/3}}^* = \max\{|i_{\mathrm{a}}^*|, |i_{\mathrm{b}}^*|, |i_{\mathrm{c}}^*|\}, \tag{2}$$

which defines the varying DC-link current reference for 2/3-PWM operation. At the same time, multiplying G^* with the calculated peak value of the 3-Φ mains voltages,

$$\hat{V}_{\mathrm{in,c}} = \sqrt{\frac{2}{3}\left(v_{\mathrm{a}}^2 + v_{\mathrm{b}}^2 + v_{\mathrm{c}}^2\right)}, \tag{3}$$

differs from $\hat{V}_{\mathrm{in,meas}}$ only in case of unbalanced mains conditions, provides the peak value $\hat{I}_{\mathrm{in}}^*$ of the 3-Φ mains current references. If the mains voltages are unbalanced, $\hat{V}_{\mathrm{in,c}}$ shows a time-dependent behavior within one mains period, ensuring the sinusoidal shape of $\hat{I}_{\mathrm{in}}^*$ during 1-Φ operation (see **Section IV**).

Dividing $\hat{I}_{\mathrm{in}}^*$ by the current conversion ratio of the AC/DC-stage $m_{\mathrm{AC/DC}}^* = \hat{I}_{\mathrm{in}}^*/\hat{I}_{\mathrm{DC}}^*$ and subsequently by the conversion ratio of the DC/DC-stage $m_{\mathrm{DC/DC}}^* = \hat{I}_{\mathrm{DC}}^*/I_{\mathrm{out}}$, the DC-link current reference for 3/3-PWM operation $I_{\mathrm{DC,3/3}}^*$, which shows a constant value over a 3-Φ mains period for nominal mains conditions, is calculated. $m_{\mathrm{AC/DC}}^*$ and $m_{\mathrm{DC/DC}}^*$ are derived from V_{out}^* and $\hat{V}_{\mathrm{in,meas}}$ to operate with the minimum DC-link current i_{DC}, i.e. to minimize the overall conduction losses. Finally, the DC-link current reference

$$i_{\mathrm{DC}}^* = \max\{i_{\mathrm{DC,2/3}}^*, I_{\mathrm{DC,3/3}}^*\}, \tag{4}$$

provides the input for the *Synergetic DC-Link Current Control*. In particular, if $i_{\mathrm{DC,2/3}}^*$ is larger than $I_{\mathrm{DC,3/3}}^*$, the converter operates with 2/3-PWM in ***Boost-Mode***. If smaller, the DC/DC-stage is clamped, $\mathrm{T_{DC,hp}}$ and $\mathrm{T_{DC,hn}}$ are permanently conducting, and the CSR-stage operates with 3/3-PWM in ***Buck-Mode***, resulting in identical currents flowing through L_{DC} and at the DC output. Importantly, the method for determining i_{DC}^* described by (4) ensures a seamless transition from 3/3-PWM to 2/3-PWM and vice versa, and minimum overall conduction losses.

C. Synergetic DC-Link Current Control

In the *Synergetic DC-Link Current Control* block, i_{DC}^* is first compared with the measured DC-link current i_{DC}, i.e. the average of the positive and negative DC-link currents,

$$i_{\mathrm{DC}} = \frac{1}{2}(i_{\mathrm{DC,p}} + i_{\mathrm{DC,n}}). \tag{5}$$

Depending on the control deviation, the DC-link current PI-controller provides the voltage v_{L}^*, which needs to be generated across L_{DC} by switching the CSR-stage and eventually the DC/DC-stage. The sum of v_{L}^* and V_{out}^* results in the virtual DC-link voltage reference v_{DC}^*. Feeding v_{DC}^* into two voltage limiters, the virtual DC-link voltage references for 3/3-PWM $v_{\mathrm{DC,3/3}}^*$ and for 2/3-PWM $v_{\mathrm{DC,2/3}}^*$ are calculated. This is the core of the synergetic operation; in fact, when the 3-Φ mains voltages are large enough to generate the necessary v_{DC}^* without operating the DC/DC-stage, i.e. $V_{\mathrm{max}} = \frac{3}{2}\hat{V}_{\mathrm{in,meas}} > V_{\mathrm{out}}^*$, the latter is permanently clamped to avoid switching losses, while the CSR-stage provides the required voltage gain (***Buck-Mode***), but operates with 3/3-PWM. In this case, we have $v_{\mathrm{DC,3/3}}^* = V_{\mathrm{DC}}^* = v_{\mathrm{pn}}^*$ (the reference output voltage of the CSR-stage) and $v_{\mathrm{DC,2/3}}^* = V_{\mathrm{out}}^*$. Differently, when V_{out}^* is large enough to balance the volt-seconds applied to L_{DC} by the CSR-stage for $m_{\mathrm{AC/DC}} = 1$, i.e. $V_{\mathrm{out}}^* > \frac{2}{\sqrt{3}}V_{\mathrm{max}}$, the CSR-stage operates with 2/3-PWM and the DC/DC-stage is actively switched with PWM (***Boost-Mode***); specifically, $v_{\mathrm{DC,3/3}}^* = V_{\mathrm{max}}$ and $v_{\mathrm{DC,2/3}}^* = v_{\mathrm{qr}}^*$ (the reference input voltage of the DC/DC-stage) applies.

Accordingly, the current controller regulates i_{DC} by operating always only one stage: when operating with 3/3-PWM, the CSR-stage is controlled by modifying $v_{\mathrm{DC,3/3}}^*$ and $v_{\mathrm{DC,2/3}}^*$ has no influence, while, when operating with 2/3-PWM, the DC/DC-stage is controlled by modifying $v_{\mathrm{DC,2/3}}^*$ and $v_{\mathrm{DC,3/3}}^*$ is clamped to V_{max}. Finally, for $V_{\mathrm{max}} < V_{\mathrm{out}}^* < \frac{2}{\sqrt{3}}V_{\mathrm{max}}$ (***Transition-Mode***), the current controller naturally alternates 2/3-PWM and 3/3-PWM (depending on v_{L}^*).

D. Modulator and Gate Signals

To ultimately operate the two stages, $v_{\mathrm{DC,3/3}}^*$ and $v_{\mathrm{DC,2/3}}^*$ are fed to the corresponding modulators. For the CSR-stage, the reference DC-link current $i_{\mathrm{DC,CSR}}^*$ utilized in the modulator is determined based on $v_{\mathrm{DC,3/3}}^*$ ($i_{\mathrm{DC,CSR}}^* = i_{\mathrm{DC}}^*$ in steady state). In particular, in 3/3-PWM operation, V_{out}^* coincides with $v_{\mathrm{DC,3/3}}^*$ and $m_{\mathrm{DC/DC}}^* = 1$ because $\mathrm{T_{DC,hp}}$ and $\mathrm{T_{DC,hn}}$ are permanently conducting. Differently, in 2/3-PWM operation, $m_{\mathrm{DC/DC}}^*$ must be considered due to the operation of the DC/DC-stage. For

$$V_{\mathrm{out}}^* = m_{\mathrm{DC/DC}}^* \cdot V_{\mathrm{max}}, \tag{6}$$

the CSR-stage operates with the maximum modulation index, and i_{DC}^* is regulated by the DC/DC-stage only.

The switching signals for the CSR-stage are calculated from i_{a}^*, i_{b}^*, i_{c}^*, and $i_{\mathrm{DC,CSR}}^*$ as in [15], and appropriately distributed to the twelve gate terminals. An example of this procedure is given in the following, considering the 60°-wide sector of a 3-Φ mains period where phase *c* has the minimum current value. In particular

$$\delta_{[\mathrm{ac}]} = \frac{i_{\mathrm{a}}^*}{i_{\mathrm{DC,CSR}}^*},\ \delta_{[\mathrm{bc}]} = \frac{i_{\mathrm{b}}^*}{i_{\mathrm{DC,CSR}}^*}, \tag{7}$$

are the duty cycles of the two active states, while

$$\delta_{[\mathrm{cc}]} = 1 - \delta_{[\mathrm{ac}]} - \delta_{[\mathrm{bc}]} \tag{8}$$

holds for the zero state, where $\delta_{[\mathrm{xy}]}$ indicates the duty cycle of the state [xy], having terminal *p* connected to phase *x* and terminal *n* connected to phase *y*.

On the other hand, the duty cycle reference of the DC/DC-stage,

$$d^* = \frac{v_{\mathrm{DC,2/3}}^*}{V_{\mathrm{DC/DC}}^*} = \frac{v_{\mathrm{qr}}^*}{V_{\mathrm{DC/DC}}^*}, \tag{9}$$

is compared with a triangular carrier to generate complementary switching signals. $V_{\mathrm{DC/DC}}^*$ in (9) is assigned to balance the DC voltage mid-point *m*. Specifically, when $v_{\mathrm{qr}} = 0\,\mathrm{V}$ or V_{out}, the two output capacitors $C_{\mathrm{out,p}}$ and $C_{\mathrm{out,n}}$ are simultaneously discharged or charged by the same current, thus, their voltage difference remains constant. When $v_{\mathrm{qr}} = \frac{1}{2}V_{\mathrm{out}}$, instead, either $C_{\mathrm{out,p}}$ or $C_{\mathrm{out,n}}$ can be alternatively (e.g. one switching period each) connected to the input of the DC/DC-stage and *m* can be balanced if d^* is calculated correctly. For example, considering $\bar{v}_{\mathrm{qr}} > \frac{1}{2}V_{\mathrm{out}}$, when $C_{\mathrm{out,p}}$ is connected, $V_{\mathrm{DC/DC}}^* = V_{\mathrm{Cout,n}}$, while, when $C_{\mathrm{out,n}}$ is connected, $V_{\mathrm{DC/DC}}^* = V_{\mathrm{Cout,p}}$. Accordingly, if $V_{\mathrm{Cout,p}} > V_{\mathrm{Cout,n}}$, $d_{\mathrm{p}}^* > \frac{2v_{\mathrm{qr}}^*}{V_{\mathrm{out}}} > d_{\mathrm{n}}^*$ results (d_{x}^* is the duty cycle associated to $C_{\mathrm{out,x}}$), i.e. $C_{\mathrm{out,n}}$ is connected for longer time than $C_{\mathrm{out,p}}$; in other words, $C_{\mathrm{out,n}}$ is discharged

TABLE I: System specifications and simulation parameters.

	Description	Value
V_{m}	mains RMS phase voltage	230 V
V_{out}	DC output voltage range	200 V∼1000 V
P_{out}	rated output power	10 kW
$I_{\mathrm{out,max}}$	output current limit	25 A ($V_{\mathrm{out}} < 400$ V)
f_{sw}	switching frequency	100 kHz (both stages)
$L_{\mathrm{DC,DM}}$	DC-link DM inductance	270 µH
$L_{\mathrm{DC,CM}}$	DC-link CM inductance	23 mH
C_{in}	input filter capacitor	3× 7 µF
C_{out}	output capacitor	2×10 µF (3-Φ operation) 2×1 mF (1-Φ operation)
C_{CM}	integrated filter capacitor	48 nF
$L_{\mathrm{DM,1}} = L_{\mathrm{DM,2}}$	EMI DM inductor	4.8 µH
$C_{\mathrm{DM,1}} = C_{\mathrm{DM,2}}$	EMI DM capacitor	4 µF
L_{d}	damping inductor	1 µH
$R_{\mathrm{d,1}}$	damping resistor 1	6.6 Ω
C_{d}	damping capacitor	1 µF
$R_{\mathrm{d,2}}$	damping resistor 2	4.9 Ω
$L_{\mathrm{CM,1}} = L_{\mathrm{CM,2}}$	EMI CM inductor	780 µH
$C_{\mathrm{CM,1}} = C_{\mathrm{CM,2}}$	EMI DM capacitor	17 nF

less than $C_{\mathrm{out,p}}$, which increases $V_{\mathrm{Cout,n}}$ and decreases $V_{\mathrm{Cout,p}}$. This method provides a simple way to balance m, without the need for an additional PI controller.

IV. Simulation Results

In this section, the operation of the proposed synergetic control structure is further validated observing the most significant waveforms, i.e. the 3-Φ input currents i_{a}, i_{b}, and i_{c}, the DC-link current i_{DC}, the 3-Φ voltages of the input capacitors v_{a}, v_{b}, and v_{c}, and the output voltage V_{out}, resulting from circuit simulations of the analyzed power converter (specifications and design parameters according to **Tab. I**) operating with 2/3-PWM under irregular 3-Φ mains conditions, e.g. in case of harmonics distortion, phase open-circuit, voltage dips, and mains overvoltage. In particular, it is highlighted how, even under these conditions, the nominal output power of P_{out} = 10 kW and an output voltage of V_{out} = 800 V are provided. Furthermore, once the faults occur or are cleared, i_{DC} is limited to relatively low values, hence the ratings of L_{DC} and of the power semiconductors are not exceeded, since the spikes superimposed to the sinusoidal 3-Φ mains currents are partially attenuated by the input filter and the protection network. Saturable inductors are considered in the simulation to more accurately model their real behavior, i.e. the DM inductance values are assumed to gradually drop to 50% of their nominal value when the current reaches 45 A [23], [24].

A. Harmonics Distortion

Harmonics distortion could prevent delivering the nominal output power P_{out}, and could introduce control instability because of a jitter of the sector detector output signal. Thus, the harmonics distortion compatibility of the converter is investigated in this subsection [20]. As shown in **Fig. 4**, at $t = 20$ ms several higher-order harmonics of the 50 Hz 3-Φ mains voltages, i.e. a 5th, 7th, 11th, 13th and 17th harmonic are superimposed to the ideal sinusoidal 3-Φ mains voltages. Their amplitudes and mutual phase shifts are opportunely selected to introduce multiple crossings of the 3-Φ mains voltages (three crossings instead of only one every 60°). Since the clamped phase in 2/3-PWM is determined according to the largest absolute value of the 3-Φ input currents, additional sector transitions (see **Fig. 2** and zoom in **Fig. 4**) occur. However, the proposed controller structure handles these conditions, i.e. PFC rectifier operation is maintained and V_{out} remains at its nominal value. Finally, when the higher-order harmonics are removed at $t = 100$ ms, the converter returns to normal operation.

B. Phase Open-Circuit Fault

The converter operation in case of a phase open-circuit fault is tested, and the related simulation results are shown in **Fig. 5**. An open-circuit fault, i.e. an interruption of phase c of the 3-Φ mains voltages is assumed to occur at t = 20 ms. However, the converter continues to operate and automatically transitions to 1-Φ operation without any modification of the control structure, draws approximately sinusoidal phase currents from the remaining phases, and delivers the nominal P_{out}.
The seamless transition is achieved by the proposed control structure. After the fault occurs, a current is initially drawn from phase c to discharge $C_{\mathrm{in,c}}$ until $v_{\mathrm{c}} = 0$ V. Afterwards, zero average current is drawn from the faulty phase, and the system operates with the two remaining phases like a 1-Φ rectifier, i.e. according to the modified modulation the CSR-stage is showing the behavior of a passive rectifier operating at the mains frequency. Meanwhile, the DC/DC-stage shapes i_{DC} and regulates V_{out}. According to the pulsation of the power drawn from the mains, V_{out} shows a ripple with twice the mains frequency, but the nominal P_{out} is still supplied to the load. At $t = 100$ ms, phase c is reconnected, and the converter returns to 3-Φ operation.
The derivation of the DC-link current reference i^*_{DC} during

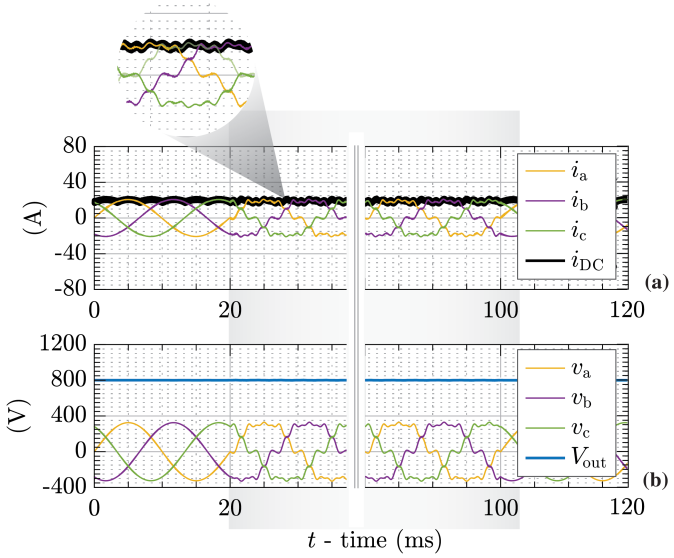

Fig. 4: Simulated waveforms of the analyzed converter in case of sinusoidal mains (up to $t = 20$ ms) and harmonics distortion of all 3-Φ mains phase voltages. In particular, in **(a)** the 3-Φ input currents i_{a}, i_{b}, and i_{c}, and the DC-link current i_{DC}, and in **(b)** the 3-Φ input voltages v_{a}, v_{b}, and v_{c}, and the output voltage V_{out} are shown.

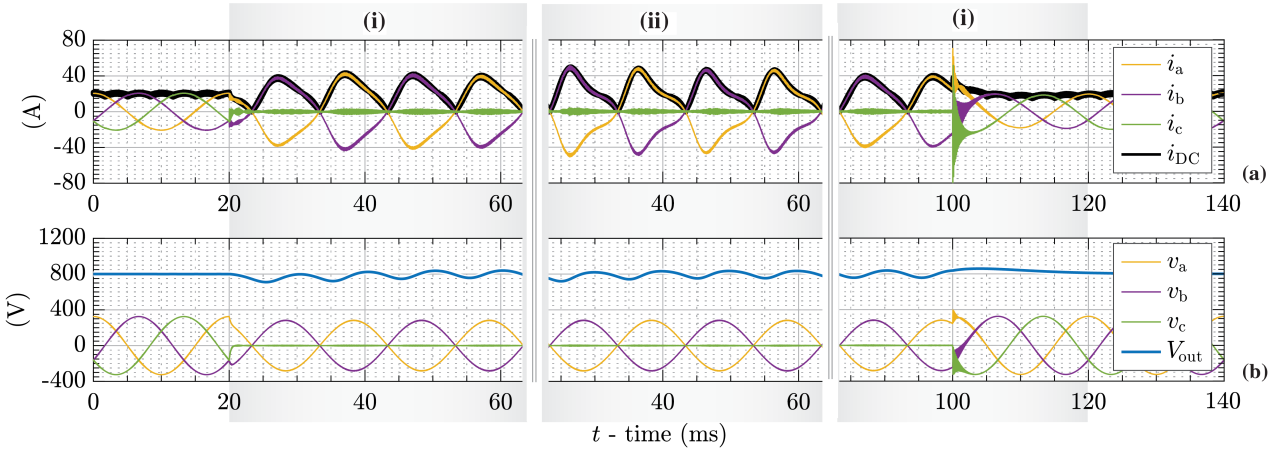

Fig. 5: Simulated waveforms of the analyzed converter (cf. **Fig. 1**, **Fig. 2**, and **Tab. I**) in case of a phase open-circuit fault considering different parameters of the output voltage PI controller. In particular, in **(a)** the 3-Φ input currents i_a, i_b, and i_c, and the DC-link current i_{DC}, and in **(b)** the 3-Φ input voltages v_a, v_b, and v_c, and the output voltage V_{out} are shown. Two sets of control parameters are utilized: in **(i)** certain values of K_P and K_I are considered, while in **(ii)** $2K_P$ and $2K_I$ are used.

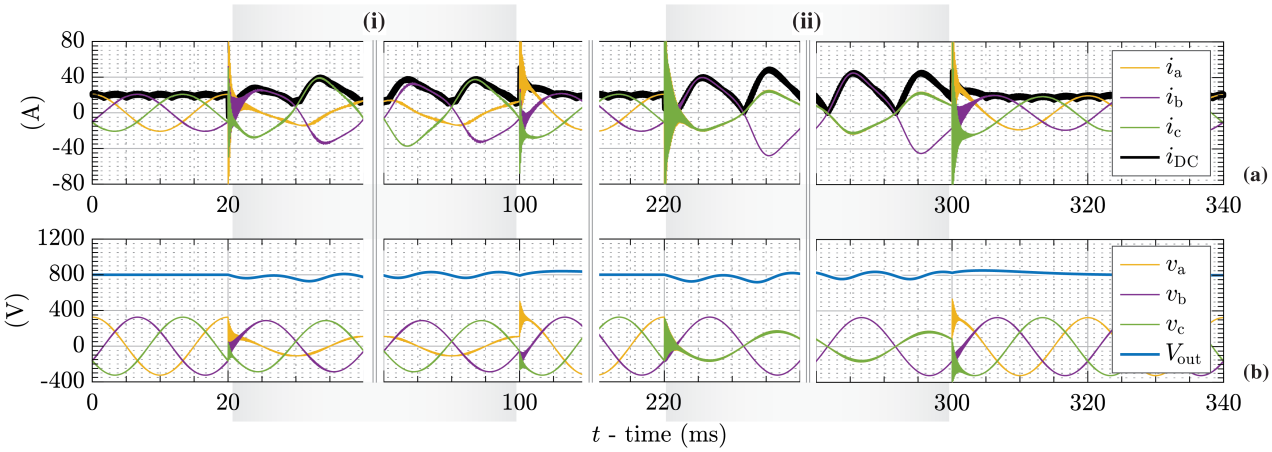

Fig. 6: Simulated waveforms of the analyzed converter (cf. **Fig. 1**, **Fig. 2**, and **Tab. I**) in case of mains voltage dips, i.e. **(i)** a phase zero-voltage fault and **(ii)** a line-to-line voltage dip. In particular, in **(a)** the 3-Φ input currents i_a, i_b, and i_c, and the DC-link current i_{DC}, and in **(b)** the 3-Φ input voltages v_a, v_b, and v_c, and the output voltage V_{out} are shown.

1-Φ operation is further discussed in the following. Assuming a constant G^*, $i^*_{DC,2/3}$ follows the shape of the positive envelope of the sinusoidal input capacitor voltages. Also $I^*_{DC,3/3}$ is sinusoidal because $\hat{V}_{in,c}$ calculated in (3) varies over the 3-Φ mains period. However, the value of $\hat{V}_{in,c}$ is always smaller than the instantaneous amplitude of the phase voltages ($v_a = -v_b$). Thus, $i^*_{DC} = i^*_{DC,2/3}$, and stable 1-Φ operation is achieved through the automatic deactivation of the mode selection function described by (4). Differently, if $\hat{V}_{in,m}$ would be utilized instead of $\hat{V}_{in,c}$ to calculate $I^*_{DC,3/3}$, the latter would be constant, and i^*_{DC} would alternatively assume the value of $i^*_{DC,2/3}$ and $I^*_{DC,3/3}$, leading to unnecessary conduction and switching losses in the CSR-stage.

In reality, the shape of $i^*_{DC,2/3}$ is strongly influenced by G^*, i.e. by the parameters of the output voltage PI controller, cf. **Fig. 5 (i)** and **(ii)**. A lower controller gain ensures less distortion of the sinusoidal mains currents, but also results in lower dynamics of the control of V_{out}.

C. Mains Voltage Dips

Simulation results describing the converter operation in case of mains voltage faults are shown in **Fig. 6**. Two types of mains voltage dips are discussed in this subsection, i.e. a mains phase zero-voltage fault (cf. **Fig. 7(a)**) and a line-to-line voltage dip (cf. **Fig. 7(b)**). At $t = 20\,\text{ms}$ (cf. **Fig. 6(i)**), $v_{m,a}$ drops to $0\,\text{V}$, but phase a remains connected to the CSR-stage input phase terminal such that i_a can flow. According to the phasor diagram of **Fig. 7(a)**, we then have $v_{m,b} = -v_{m,ab} \approx -v_{ab}$ and $v_{m,c} = v_{m,ca} \approx v_{ca}$. The input capacitors C_{in} are forming a voltage divider of v_b and v_c, thus $v_a \neq 0\,\text{V}$. Since the mains current references are determined by v_a, v_b, and v_c, $i^*_a \neq 0$ results, i.e. phase a still draws a

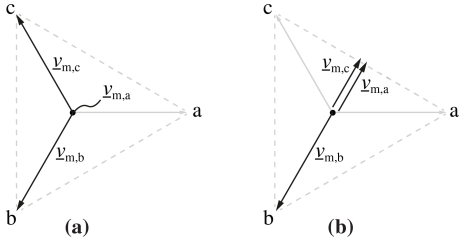

Fig. 7: 3-Φ mains voltage phasor diagram in case of **(a)** a phase zero-voltage fault occurring in phase a ($v_{m,a} = 0$, $v_{m,ab} = -v_{m,b}$, and $v_{m,ca} = v_{m,c}$), and **(b)** a line-to-line voltage dip between phase a and phase c ($v_{m,ca} = 0$).

current from the mains. The DC-link current reference i^*_{DC} is the envelope of the absolute values of i^*_a, i^*_b, and i^*_c. V_{out} shows a ripple with twice the mains frequency, i.e. varies around its nominal value, but the nominal P_{out} is still supplied to the load. At $t = 100\,\text{ms}$, phase a returns to its nominal condition, and the converter returns to regular 3-Φ operation. In **Fig. 6(ii)**, a line-to-line voltage dip is considered to occur at $t = 220\,\text{ms}$ which causes the amplitudes of $v_{m,a}$ and $v_{m,c}$ to drop to half of their nominal values, and their angles to coincide (see **Fig. 7(b)**). The DC-link current reference i^*_{DC} is determined by the unchanged phase b which features the largest phase voltage amplitude after the fault occurred. Even though V_{out} varies around its nominal value with twice the mains frequency, the nominal P_{out} is maintained. When the fault is cleared at $t = 300\,\text{ms}$, the converter operates normally again.

Each fault triggers a weakly damped resonance of the EMI filter, which causes visible ringing superimposed to the 3-Φ sinusoidal input currents. Although the worst case of stiff 3-Φ mains (no inner mains impedance) is considered, this current oscillation has no impact on the converter control and performance. Nevertheless, active damping concepts [25] could be adopted if necessary, in addition to the already present EMI filter passive damping network.

D. Mains Overvoltage

Two types of mains overvoltage are considered in the following according to [22], i.e. a line-to-line test and a line-to-ground test are performed. The test set-up is shown in **Fig. 8**; it includes the combination wave generator (CWG), the coupling network to connect the device under test (DUT) with the CWG, and the decoupling network between the CWG

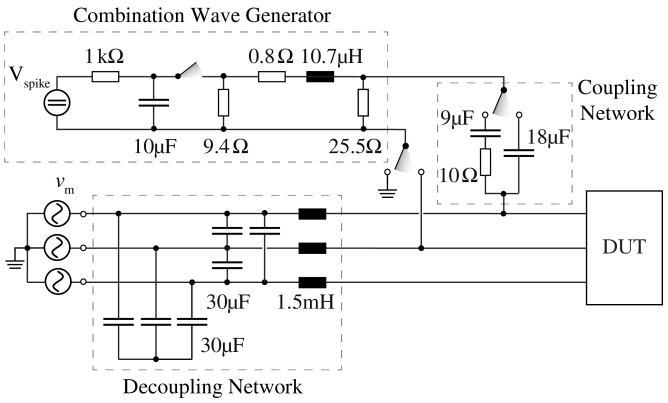

Fig. 8: Mains overvoltage test setup, including the combination wave generator (CWG), the coupling network to connect the device under test (DUT) with the CWG, and the decoupling network between the CWG and 3-Φ mains. The component values are provided, highlighting different coupling network configurations for line-to-line and line-to-ground tests.

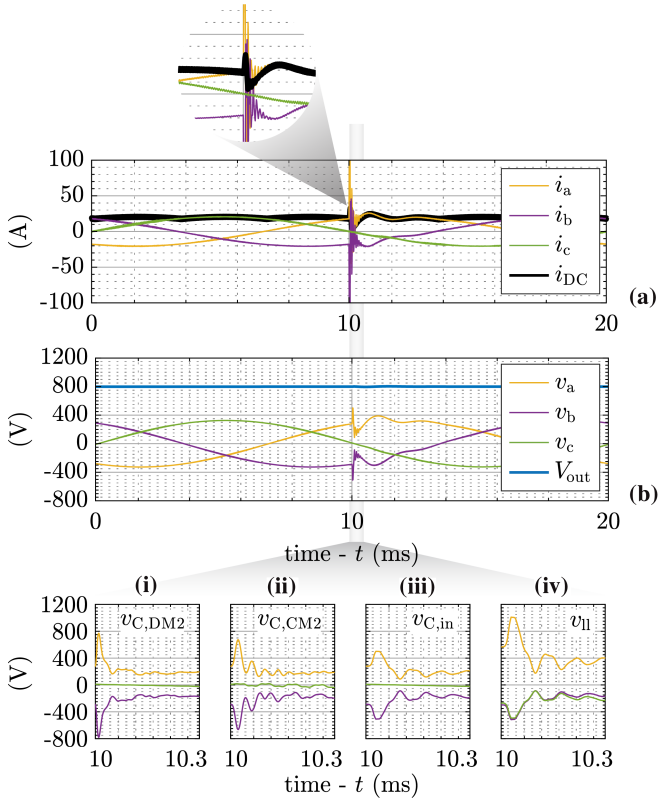

Fig. 9: Simulated behavior of the analyzed converter in case of a line-to-line overvoltage occurring between phase a and phase b. In particular, in **(a)** the 3-Φ input currents i_a, i_b, and i_c, and the DC-link current i_{DC}, and in **(b)** the 3-Φ input voltages v_a, v_b, and v_c, and the output voltage V_{out} are shown. The zoomed voltage waveforms across **(i)** the EMI filter capacitors $C_{DM,2}$ (voltages $v_{C,DM2}$), **(ii)** the EMI filter capacitors $C_{CM,2}$ (voltages $v_{C,CM2}$), **(iii)** the input filter capacitors C_{in} (voltages v_{Cin}), and **(iv)** the line-to-line voltages v_{ll} at the input terminal of the CSR-stage, occurring after the fault are additionally illustrated.

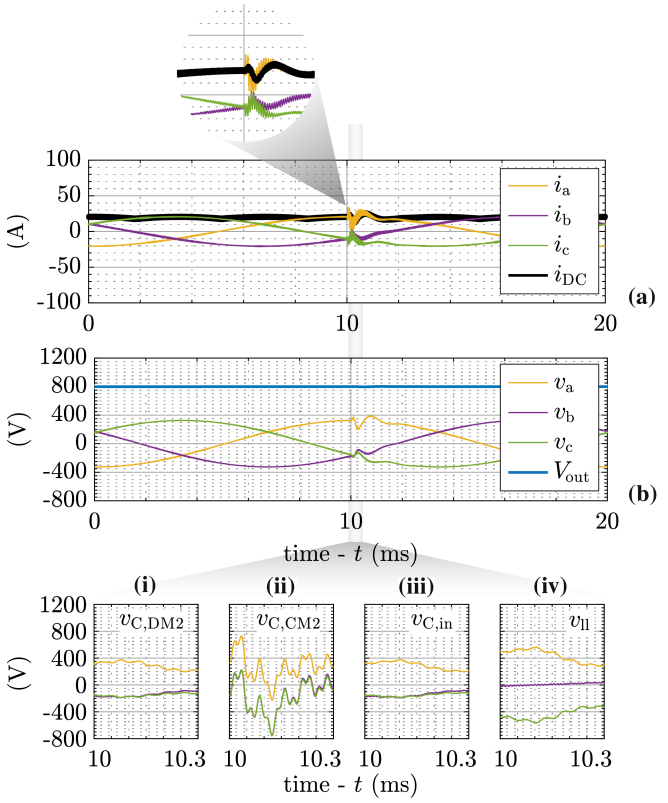

Fig. 10: Simulated behavior of the analyzed converter in case of a line-to-ground overvoltage occurring between phase a and ground. In particular, in **(a)** the 3-Φ input currents i_a, i_b, and i_c, and the DC-link current i_{DC}, and in **(b)** the 3-Φ input voltages v_a, v_b, and v_c, and the output voltage V_{out} are shown. The zoomed voltage waveforms across **(i)** the EMI filter capacitors $C_{DM,2}$ (voltages $v_{C,DM2}$), **(ii)** the EMI filter capacitors $C_{CM,2}$ (voltages $v_{C,CM2}$), **(iii)** the input filter capacitors C_{in} (voltages v_{Cin}), and **(iv)** the line-to-line voltages v_{ll} at the input terminal of the CSR-stage, occurring after the fault are additionally illustrated.

and mains. In the line-to-line test a voltage $V_{\text{spike}} = 2\,\text{kV}$ is applied and the coupling network is realized as $18\,\mu\text{F}$ capacitor, while in the line-to-ground test $V_{\text{spike}} = 4\,\text{kV}$ and the coupling network consists of a $9\,\mu\text{F}$ capacitor in series with a $10\,\Omega$ resistor.

To protect the converter from excessive overvoltage, which potentially could damage e.g. the power semiconductors of the CSR-stage, a two-stage surge protection network is installed (cf. **Fig. 1**). Surge protection devices (SPDs) i.e. a surge protection thyristor, *P3500SDLRP* [16], in series with a varistor, *V20E130P* [26], in each phase are serving as line-to-ground protection, while metal-oxide varistors (MOVs), *V420LA40BP* [17], are ensuring line-to-line protection. The selected SPDs are preferred over MOVs because of the low clamping and high continuous operating voltages, the steep dynamic characteristic, and the low leakage current [23]. For even higher continuous operating voltages, several surge protection thyristors could be connected in series. Moreover, a suppressor diode could be included for additional safety [27]. The line-to-line test simulation result is shown in **Fig. 9**, where an overvoltage spike generated by the CWG between phase *a* and *b* occurs at $t = 10\,\text{ms}$. The line-to-ground test simulation result, instead, is shown in **Fig. 10**, where an overvoltage spike generated by the CWG in phase *a* occurs at $t = 10\,\text{ms}$. Thanks to the surge protection network, the EMI filter capacitors and the semiconductors of the CSR-stage do not experience significant overvoltages. In particular, the EMI filter and input capacitors are protected by the SPDs, while the voltages across the semiconductors are clamped at $1\,\text{kV}$ thanks to the line-to-line protection MOVs. Additionally, low-pass filtering the input filter capacitor voltages v_{a}, v_{b}, and v_{c} (not shown in **Fig. 2**) with a cut-off frequency $f_{\text{c}} = 100 f_{\text{m}}$ limits the influence of the overvoltage on the peak value of i^*_{DC}, which avoids the propagation of the spike to i_{DC}.

V. Conclusion

An efficient and reliable distributed battery charging infrastructure is required to facilitate the widespread adoption of electric vehicles (EVs). Hence, a three-phase (3-Φ) bidirectional buck-boost (bB) current DC-link PFC rectifier system for DC off-board EV chargers is introduced in this paper in combination with a new control structure and overvoltage protection means. The power converter is formed by a 3-Φ buck-type current source rectifier (CSR) input stage and a subsequent boost-type DC/DC output stage, and covers a wide output voltage range of $200\,\text{V}$ to $1000\,\text{V}$. Its operation is verified by circuit simulations of a $10\,\text{kW}$ prototype employing SiC power MOSFETs and operating at a switching frequency $f_{\text{sw}} = 100\,\text{kHz}$. The proposed synergetic control concept allows to operate even under heavily unbalanced 3-Φ mains conditions, as well as harmonics distortion, undervoltage events, and phase loss. In all cases PFC rectifier operation is ensured and the DC-link current is controlled with synergetic operation of the CSR- and DC/DC-stage, which allows to reduce the number of switching actions and/or increases the power conversion efficiency. All mentioned features are achieved without changeover between different control structures for operation in different modes and with different modulation schemes. Accordingly, the analyzed power converter, in combination with the proposed synergetic control concept, represents a promising approach for realizing efficient and robust 3-Φ AC/DC PFC rectifier systems of EV charging stations.

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