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Comparative Evaluation of Isolated Front End and Isolated Back End Multi-Cell SSTs

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***Abstract*—Solid-state transformers (SSTs) are power electronic interfaces between medium voltage (MV) and low voltage (LV) systems that provide galvanic isolation by means of medium frequency (MF) transformers, making them suitable for MVAC to LVDC conversion in environments where weight and volume constraints apply. This paper discusses an isolated front end (IFE) SST concept that allows to reduce the complexity and physical size of the MV side converter assemblies compared to the well-known isolated back end (IBE) SST topologies. The IFE approach performs the entire grid current and output voltage control on the LV side using standard non-isolated |AC|-DC boost converter stages. A generic comparison of the IFE and the IBE concepts reveals that the lower complexity of the IFE, e. g., a lower total MV blocking voltage requirement (number of cascaded cells), comes along with higher device RMS currents and hence slightly higher chip area requirements. On the other hand, a case study considering a 25 kW, 6.6 kV AC to 400 V DC SST shows advantages of the IFE in part-load operation due to lower switching and transformer core losses. This makes the IFE approach interesting for applications where MF isolation instead of low frequency isolation is required because of space and weight constraints (e. g., traction, subsea or aircraft environments), and where low system complexity is desirable.**

I. Introduction

There are many emerging low voltage (LV) DC applications that could benefit from a power electronics interface to the medium voltage (MV) AC distribution grid due to higher power requirements. Such applications include, e. g., datacenters with internal 400 V DC power distribution architectures, larger PV plants, fuel cell or battery storage systems, UPS systems, or DC microgrids in general. However, in such stationary applications, the efficiency, robustness and costs of solutions based on conventional line frequency transformers (LFTs) are difficult to attain with power electronic replacements [1]. In contrast, especially in environments where volume and weight constraints apply, such as in, e. g., traction, subsea, or future aerospace applications, an increase of the isolation stage operating frequency from the grid frequency into the medium frequency (MF) range by adding power electronic conversion stages is a competitive approach to meet these requirements (cf., e. g., [2]). Such power electronic systems acting as a link between a MV and a LV system and employing MF isolation stages and providing a control input and/or a communication port are commonly denominated as solid-state transformers (SSTs). Depending on the application, such MVAC-LVDC SSTs operate either as a rectifier, as an inverter, or allow a bidirectional power flow. In either case, the power factor at the MV grid should be close to unity, i. e., isolated power factor correction (PFC) functionality must be provided.

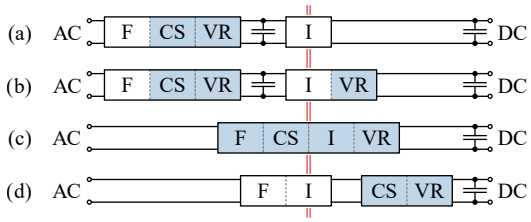

Fig. 1. Partitioning of the tasks required to perform isolated PFC: folding (F), current shaping (CS), isolation (I), and output voltage regulation (VR). A shaded background indicates a controllable stage.

A. Isolated PFC Functionality Partitioning

An isolated (single-phase) PFC system performs four distinct tasks: folding (rectification) of the AC grid voltage into a |AC| voltage, shaping of the input current (current shaping, CS), galvanic isolation (I), and output voltage regulation (VR). **Fig. 1** illustrates different variants of how these functional blocks can be partitioned and/or combined.

Variant **(a)** interfaces the AC grid with a folding and a boost stage that draws an appropriately shaped current from the grid to generate a regulated DC voltage, which is then processed by an unregulated isolated DC-DC converter stage, which could be realized as a half-cycle discontinuous-conduction-mode (HC-DCM) series-resonant converter (SRC) [2]–[4]. Since the isolation stage is positioned after the main controlling stage, this concept can be referred to as an *isolated back end* (IBE) system.

If, as in variant **(b)**, the isolation stage is realized as a regulated converter, e. g., as a dual active bridge (DAB) topology, complexity but also controllability increases, and it becomes possible to buffer the AC side power fluctuation on the primary side by controlling the power transfer through the isolation stage to be constant, providing a regulated DC output voltage with very low low-frequency ripple without requiring a large output capacitor [5]–[7].

The IBE concepts can be realized as multi-cell input-series output-parallel (ISOP) systems in order to cope with MV voltage levels on the AC side, as is shown in **Fig. 2a**. Each

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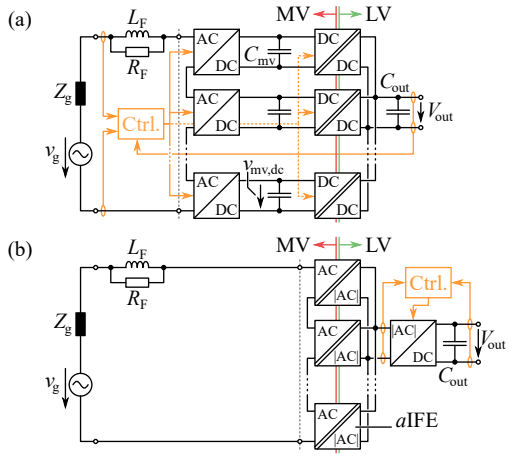

Fig. 2. **(a)** IBE and **(b)** IFE systems in ISOP configuration.

converter cell consists of a controlled AC-DC rectification stage, a DC buffer capacitance, and an isolated DC-DC converter (cf., e. g., [2], [4], [6]). Hence, a large share of the system complexity (power semiconductors, measurement and control electronics, etc.) is located on the MV side of the isolation barrier.

In a third variant of the PFC and voltage regulation task partitioning, **(c)**, all four functional blocks can be integrated into a single converter stage, which essentially directly switches the (possibly folded) mains voltage to generate a high-frequency AC voltage that is then applied to a high-frequency isolation transformer, as has initially been proposed in 1970 for an "electronic transformer" [8]. In such approaches, the shaping of the grid current as well as the output voltage control functionality are integrated into the isolation stage (cf., e. g., [9]–[17]), which further increases its complexity and hence renders the approach less feasible for ISOP configurations.

The fourth variant, **(d)**, is an inversion of the concepts (a) and (b): a folding and isolation stage is directly connected to the mains, but the current shaping and voltage regulation process is performed by a controlled |AC|-DC conversion stage on the secondary side. Hence, this arrangement is referred to as an *isolated front end* (IFE) system. This has first been proposed in 1985 for a traction application, where the rectified and then chopped line voltage was used to directly feed a 400 Hz transformer and where the current shaping was realized using a (forced-commutated thyristor-based) boost stage connected in series to the secondary side rectifier of the isolation stage [18]. The concept was later extended to a cascaded input structure featuring a transformer with multiple primary windings [19], also for a traction application. The secondary side active rectification unit was used to control the current in the transformer stray inductance and hence in the grid. Recently, this idea has been applied to low-voltage three-phase applications [20] and to a MV system [21], both employing three-phase multi-winding transformers. In contrast to these IFE realizations that use hard-switched isolation stages, an IGBT-based IFE with soft-switching, resonant isolation stages in ISOP configuration, but with individual LC filter elements at each cell's AC side, has been proposed in 2013 [22], [23].

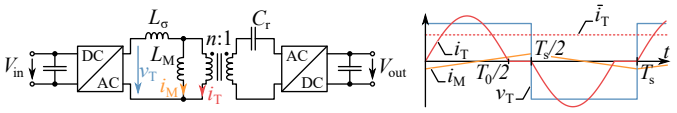

Fig. 3. HC-DCM series resonant converter (SRC) and its key waveforms.

With the goal of minimizing the complexity and employing interleaved switching in a multi-cell ISOP configuration, the IFE structure discussed in this paper does not employ such filter elements at each cell's AC side but only a common (damped) filter inductance, as shown in **Fig. 2b** [24]. A large share of the system complexity, especially the control and measurement circuitry, has been moved to the LV side when compared to the ISOP IBE system. All the regulation tasks, i. e., CS and VR, are provided by a non-isolated boost-type |AC|-DC conversion stage on the LV side, whereas the cascaded isolation stage can act as an autonomous AC-|AC| isolation front end (*a*IFE), whose only task is to provide isolation by means of a MF transformer, i. e., to tightly couple its input and output voltages without requiring control nor providing regulation, which is conceptually similar to the original "electronic transformer" proposed by McMurray in 1971 [25], and in addition provides natural balancing of the converter cell's input voltages.

B. The aIFE: Review of the HC-DCM SRC

Proposed in the 1970ies [25], [26], the HC-DCM SRC (cf. **Fig. 3**) provides exactly the desired *a*IFE functionality, because in short, the converter acts as a "DC transformer" that couples the input and output voltages tightly (with certain dynamics). For power transfer from input to output, the input bridge switches at full duty ratio and no additional control is required, since the dependence of the resonant pulses' amplitudes on the excitation voltage steps, which in turn depend on the voltage difference between input and output, adjusts the power transfer through the converter automatically such that the input and output voltages are tightly coupled. Because of this autonomous operation (no control is required), and because zero-current and zero-voltage switching (ZCS and ZVS) can be achieved for all switching transitions, the converter has been applied in numerous high-power ISOP IBE systems for SST applications, such as, e. g., described in [2], [3], [27].

C. Overview of Performed Analysis

Section II derives the structure and the operating principle of the IFE system considered in this paper, detailing also on the dynamic modeling and ISOP configurations. Based on this, section III presents a comparative analysis of the IFE and the IBE concept, and section IV contains a brief case study considering a 25 kW, 6.6 kV AC to 400 V DC SST system. After a conclusion, an appendix briefly describes additional topological variants of the IFE concept, i. e., three-phase and AC-AC configurations.

II. IFE Derivation and Operating Principle

In this section, the IFE topology considered for the comparison in section III will be derived and explained on the basis of a single converter cell, considering also a dynamic model. In a next step, the extension to an ISOP configuration will be discussed.

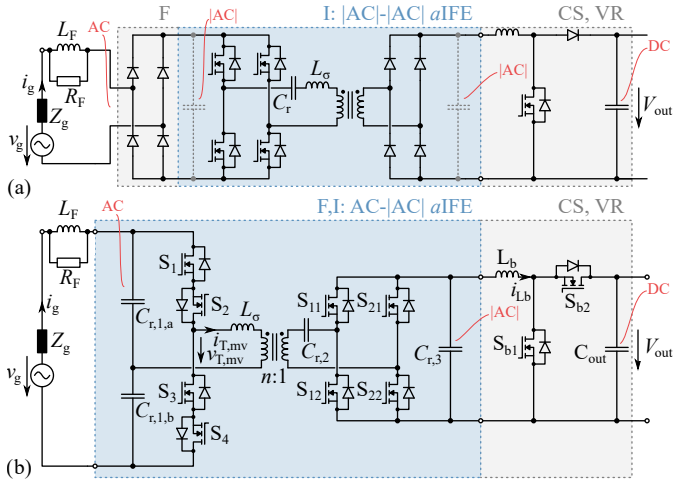

Fig. 4. **(a)** Unidirectional and **(b)** bidirectional single-cell IFE power circuit topologies. Note that $C_{\mathrm{r},1,\mathrm{a}}$, $C_{\mathrm{r},1,\mathrm{b}}$, $C_{\mathrm{r},2}$, and $C_{\mathrm{r},3}$ are resonant capacitors, not DC link capacitors.

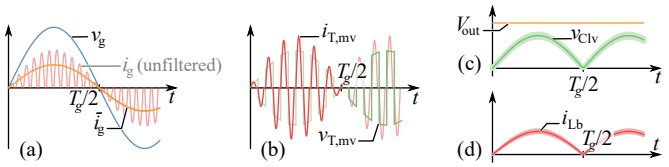

Fig. 5. Key waveforms (simplified) of the IFE topology shown in **Fig. 4b**, where a very low switching frequency is assumed for illustration purposes.

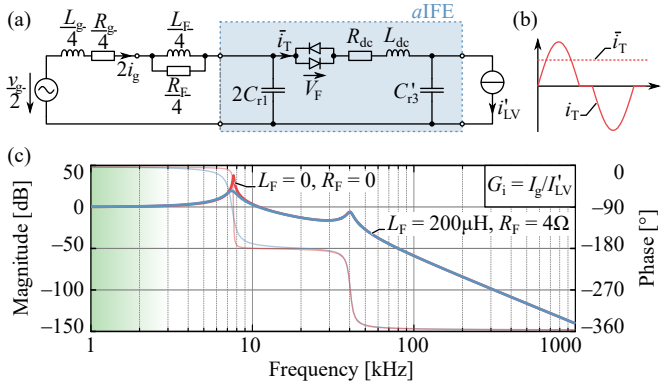

Fig. 6. **(a, b)** Dynamic equivalent circuit of the aIFE (HC-DCM SRC) including filter and grid impedances, and **(c)** corresponding transfer function from the boost stage inductor current to the grid current, $G_{\mathrm{i}}(s)$, using the data from **Tbl. IV** and $L_\sigma = 10\,\mu\mathrm{H}$.

A. IFE Topology and Key Waveforms

Fig. 4a shows a unidirectional, single-cell variant of the considered IFE topology, where the folding of the (single-phase) grid voltage is realized by means of a diode rectifier. The circuit can be extended to facilitate bidirectional operation by either replacing the rectifier diodes on the grid side by switches (indirect matrix converter topology), or by integrating the folding/unfolding operation in the aIFE's primary-side half-bridge leg using bidirectional switches (direct matrix converter approach), as shown in **Fig. 4b**. Note that in both cases all capacitors (except for the output capacitor, C_{out}) are only commutation or resonant capacitors, i. e., no energy storage elements. Since in the bidirectional topology the split resonant capacitors $C_{\mathrm{r},1,\mathrm{a}}$ and $C_{\mathrm{r},1,\mathrm{b}}$ consume capacitive reactive power from the grid (which could be compensated by suitable adaption of the boost stage current reference), high switching frequencies (and therefore high resonance frequencies and small capacitors, cf. **Fig. 3**) are desirable.

Referring to the bidirectional topology, **Fig. 5** shows the IFE's key waveforms for unity power factor rectifier operation, i. e., power flow from the AC to the DC side: the bidirectional switches are modulated with (almost) full duty ratio to chop the grid voltage and to excite resonant current half-cycles in the aIFE transformer. On the secondary side, the transformer voltage is rectified (possibly using active synchronous rectification to reduce conduction losses) to recover a folded (and scaled by the turns ratio, $1/n$, and by a factor $1/2$ due to the primary side half-bridge realization) version of the grid voltage across the LV resonant capacitor $C_{\mathrm{r},3}$—the aIFE thus acts as an isolated AC-|AC| converter.

The boost stage, in contrast, operates as a |AC|-DC converter and controls the current in the boost inductor, L_{b}, to be proportional to the |AC| voltage across $C_{\mathrm{r},3}$. Because the aIFE does not contain any significant energy storage elements (no DC link buffering capacitors), the instantaneous power flow drawn from the grid is equal to the power flow dictated by the boost stage on the LV side—the aIFE simply translates the input characteristics of the controlled boost stage to the grid without requiring feedback control by itself. In terms of currents, this means that the local average value of the current pulses in the transformer corresponds to the boost inductor current, and that the same is true for the local average of the grid current (modified by the turns ratio, etc.). Note that the operating mode of the boost stage is identical to that of a non-isolated single-phase PFC rectifier circuit, where it would be directly connected to an input diode rectifier. This illustrates how the IFE approach extends standard load-side converters to interface MV levels without requiring a bulky and heavy line frequency transformer.

B. Dynamic Behavior and Modeling

The transfer behavior, i. e., the dynamics of the aIFE stage with respect to terminal voltages and currents can be modeled by a passive equivalent circuit (cf. **Fig. 6a**), which illustrates the "DC transformer" behavior of the HC-DCM SRC [4], [28]. The current flowing in the equivalent circuit, $\bar{i}_{\mathrm{T}}$, corresponds to the local average of the real transformer current (cf. **Fig. 6b**). Assuming the current pulses to be of piecewise sinusoidal shape, the equivalent circuit elements can be calculated as

$$R_{\mathrm{dc}} = \frac{\pi^2}{8}\frac{f_0}{f_{\mathrm{s}}}R_{\mathrm{total}} \quad \text{and} \quad L_{\mathrm{dc}} = \frac{\pi^2}{4}\frac{f_0^2}{f_{\mathrm{s}}^2}L_\sigma, \tag{1}$$

where R_{total} is the sum of all series resistances in the current path (i. e., on-state resistances of the switches, winding resistances of the transformer, etc.), and where f_{s} and f_0 denote the switching and the resonant frequency, respectively. Please refer to [4] for a more detailed derivation and explanation of the dynamic model.

Using the equivalent circuit, the transfer function from the (controlled) boost inductor current to the grid current, $G_{\mathrm{i}}(s) = I_{\mathrm{g}}(s)/I'_{\mathrm{LV}}(s)$, can be calculated (cf. **Fig. 6c**). The

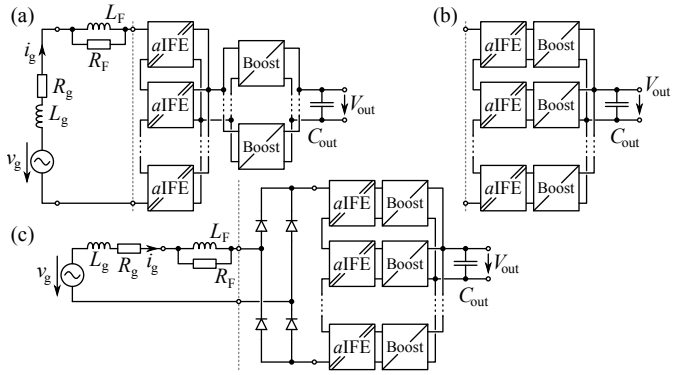

Fig. 7. Three ISOP configuration variants of the IFE topology; **(a)** common |AC| bus and single boost stage employing interleaved sub-units, **(b)** one boost stage per aIFE cell, and **(c)** common input rectifier using high-voltage semiconductors (possibly realized as an active rectifier by adding anti-parallel switches to the diodes).

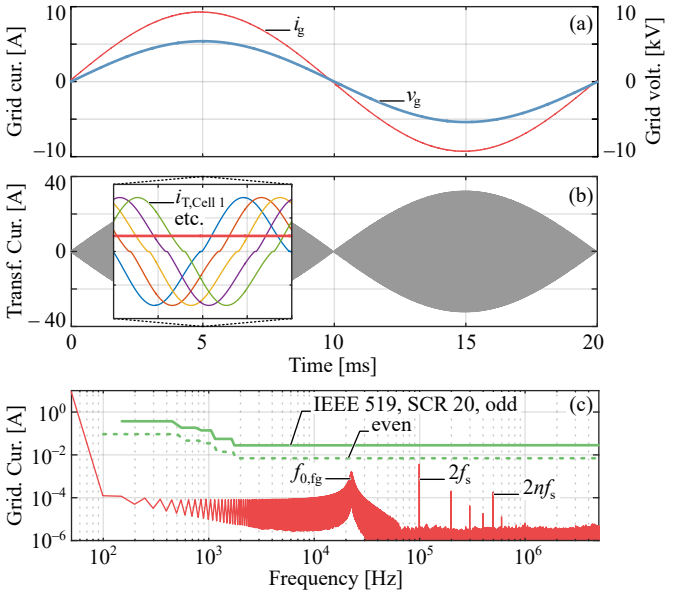

Fig. 8. Simulation results of a single-phase ISOP system (cf. **Fig. 7a**), where the boost stage is modeled as a current source, and with $L_g = 690\,\mu H$, $R_g = 22\,m\Omega$, $L_F = 200\,\mu H$, and $R_F = 10\,\Omega$.

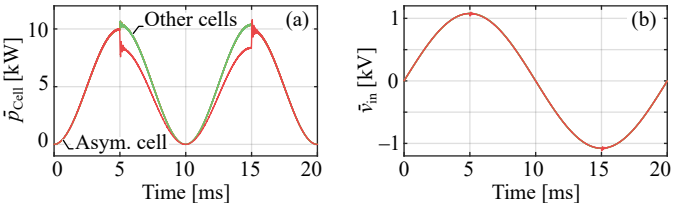

Fig. 9. Simulated self-balancing of the cells in ISOP configuration; **(a)** shows the power distribution between the cells, and **(b)** shows the sharing of the input voltage. Note that the waveforms show local average values.

gain of $G_i(s)$ being unity at low frequencies, e. g., at the grid frequency, illustrates that the aIFE is a "transparent" isolation stage, in essence similar to an LFT, although featuring significant volume and weight benefits, allowing to interface a standard boost converter to the MV grid. Note that the resonance with the highest amplitude in $G_i(s)$ occurs between the input capacitances and the filter (and inner grid) inductance. Since this resonance may be excited by load steps, appropriate damping, e. g., by using a damped RL input filter, is required.

The aIFE dynamics are not infinitely fast, which limits the IFE's capability to source or sink reactive power. As there is no intermediate energy storage on the MV side, the power flow direction through the aIFE then would need to change twice per grid period. In case of reactive power operation and/or a phase displacement of voltage and current, the *rectified* grid current would need to undergo step changes—which can be easily performed by the boost converter and its control. However, such very fast current changes are limited in bandwidth by the aIFE dynamics according to $G_i(s)$, causing disturbances in the grid current. In many applications, only operation at a power factor close to unity is required, though.

C. Input-Series Output-Parallel (ISOP) System Configuration

In order to interface a MV grid, input-series output-parallel (ISOP) configurations of the aIFE can be considered in order to employ LV semiconductors. **Fig. 7** shows three possible ISOP variants of the considered IFE topology. Since the cells are connected directly in series on the MV side, and because the grid current consists of the superposition of the *rectified* transformer current pulses of the individual cells, interleaving of the SRC carrier signals by $\Delta\varphi_{aIFE} = 180°/N_{IFE}$, with N_{IFE} denoting the number of cascaded aIFE cells, can be employed to shift the switching frequency harmonics to higher frequencies. However, due to interactions between the resonant circuits via their respective initial conditions on the MV and on the LV side (cf. [29]), the expected canceling of harmonics is not fully achieved as can be seen from the simulation results shown in **Fig. 8** for a system according to **Fig. 7a** and with specifications given in **Tbl. IV**. A detailed analysis of this phenomenon is beyond the scope of this paper. Note also that the harmonics of the boost converter stages are attenuated by the transfer characteristic of the aIFE if the (equivalent) boost stage switching frequency is chosen high enough.

As discussed earlier, the HC-DCM SRC has the property of tightly coupling its two terminal voltages. Since in an ISOP structure the voltages on the secondary side are equal for all cells—either because a direct coupling between the LV outputs of the aIFEs exists (cf. **Fig. 7a**), or because the boost stages are controlled such that they provide the same input resistance to their aIFE cell (cf. **Fig. 7b**)—equal voltage sharing among the cells is ensured on the MV side. This self-balancing feature is illustrated by simulation results of a system according to **Fig. 7a**, where in one cell a resistor consuming $10\,\%$ of the cell's nominal power ($1\,kW$) is connected in parallel to the MV input terminals at $t = 5\,ms$ and removed after one mains period (cf. **Fig. 9** and **Tbl. Ia**). Balancing is also ensured for deviations of the nominal capacitance values of the primary side resonant capacitors, as can be seen from the results in **Tbl. Ib** (one input capacitor of one cell $20\,\%$ smaller). Note that this voltage balancing is achieved without active control of the aIFEs. In addition, **Fig. 14** illustrates the system's stability during transients.

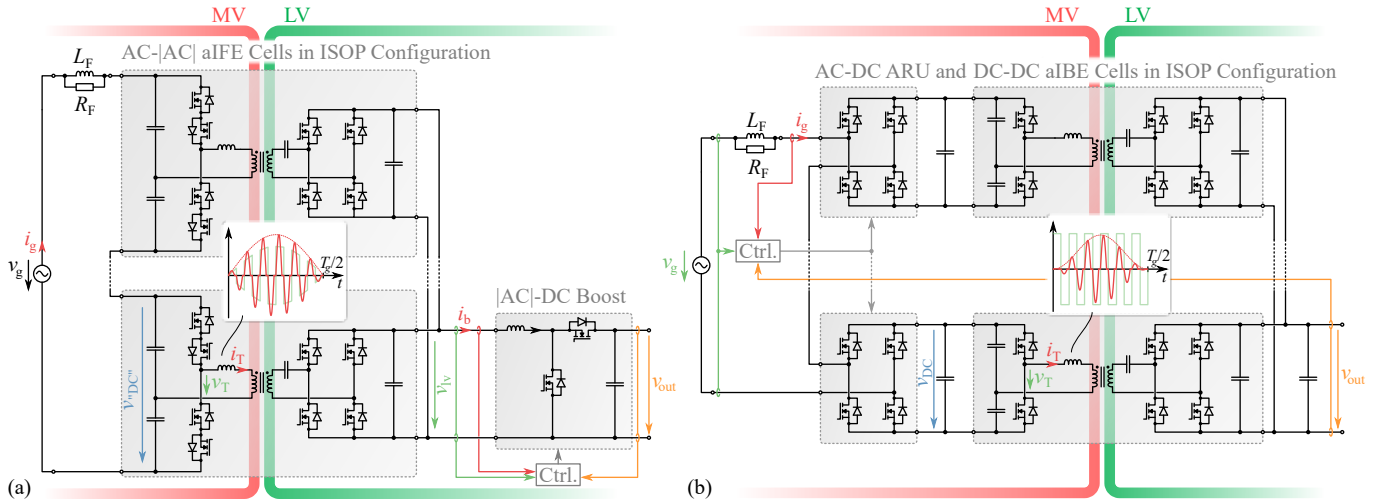

Fig. 10. Power circuits of the IFE (a) and the IBE (b) MVAC-LVDC SSTs considered in the comparative evaluation. Note that the number of cascaded cells is different for the two systems in practice (cf. (2)), and that the boost stage of the IFE system would be realized from several smaller boost stages using interleaving.

TABLE I. Effect of cell asymmetries.

	(a)			(b)		
	P	$\tilde{I}_\mathrm{T}$	$\hat{v}_\mathrm{in}$	P	$\tilde{I}_\mathrm{T}$	$\hat{v}_\mathrm{in}$
Cell with asym.	0.84	0.84	0.99	1.00	1.03	1.01
Other cells	1.04	1.04	1.01	1.00	1.00	1.00

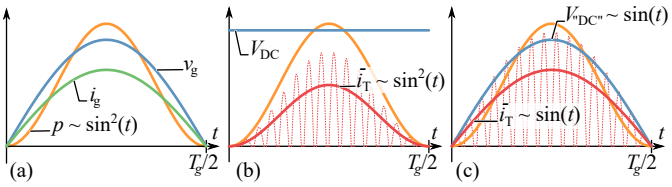

Fig. 11. Power transfer in **(a)** a single-phase grid, **(b)** in an IBE, and **(c)** an IFE system.

III. Comparative Evaluation of IFE and IBE SSTs

In the following, a generic comparison of an IFE MVAC-LVDC SST (cf. **Fig. 10a**) and a corresponding IBE system with resonant isolation stages (cf. **Fig. 10b**) will be provided, considering the realization effort for the main components (power semiconductors and transformers) and their stresses. A brief case study will be presented after this theoretical comparison in order to render the discussion more tangible.

A. Number of Cascaded Cells

In a cascaded cells system, the number of required cells follows from the peak phase voltage, $\sqrt{2}V_\mathrm{ph}$, the semiconductor voltage blocking capability, $V_\mathrm{b,MV}$, its utilization, u, and the nominal modulation index, M_N, as

$$N_\mathrm{IFE} = \frac{\sqrt{2}V_\mathrm{ph}}{uV_\mathrm{b,MV}} \qquad N_\mathrm{IBE} = \frac{\sqrt{2}V_\mathrm{ph}}{M_\mathrm{N}uV_\mathrm{b,MV}}. \tag{2}$$

Thus, $N_\mathrm{IFE}/N_\mathrm{IBE} = M_\mathrm{N} < 1$ highlights the IFE's advantage in terms of the required total MV blocking voltage (or number of cascaded cells), which is a result of shifting the boost function to the LV side. Note that for a physical realization of course $\lceil N_\mathrm{IFE} \rceil$ and $\lceil N_\mathrm{IBE} \rceil$ needed to be considered.

B. Transformer

A key difference between the IFE and the IBE system is the envelope of the switched transformer voltage. Assuming unity power factor operation, the power in single-phase systems (or also in phase-modular three-phase ISOP systems) is proportional to a $\sin^2$ function, as is illustrated in **Fig. 11a**. In an IBE system based on resonant isolation stages such as considered here, this power fluctuation is transferred through the transformers [4]. Because the DC voltage is rather constant, the local average value of the transformer current also follows a $\sin^2$ function (cf. **Fig. 11b**). However, this is different in the IFE system, where the envelope of the transformer voltage is proportional to a sine function, resulting in the local average of the transformer current also being proportional to a sine function (cf. **Fig. 11c**). Hence, the transformer RMS current of the IFE system can be derived starting with the relation

$$\bar{i}_\mathrm{T,IFE}(t) \cdot \bar{v}_\mathrm{T,IFE}(t) \stackrel{!}{=} \frac{\bar{p}_\mathrm{g}(t)}{N_\mathrm{IFE}}, \tag{3}$$

where $\bar{x}$ denotes a local average value over half a switching cycle. With

$$\bar{p}_\mathrm{g}(t) = 2P\sin(2\pi f_\mathrm{g}t)^2 \tag{4}$$

and, in the case of a half-bridge configuration (factor $1/2$),

$$\bar{v}_\mathrm{T,IFE}(t) = \frac{\sqrt{2}}{2N_\mathrm{IFE}}V_\mathrm{ph}\sin(2\pi f_\mathrm{g}t), \tag{5}$$

the local average value of the MV side transformer current in a single cell becomes

$$\bar{i}_\mathrm{T,IFE}(t) = \frac{2\sqrt{2}P}{V_\mathrm{ph}}\sin(2\pi f_\mathrm{g}t), \tag{6}$$

where P denotes the rated power of a single-phase system and V_ph the phase RMS voltage. Assuming piecewise sinusoidal

TABLE II. Expressions for the semiconductor currents and the transformer turns ratio in the IFE and IBE converter cells.

	$\tilde{I}_{\mathrm{ARU}}$	$\tilde{I}_{\mathrm{SRC,MV}}$	n	$\tilde{I}_{\mathrm{SRC,LV}}$	$\tilde{I}_{\mathrm{B,Shunt}}$	$\tilde{I}_{\mathrm{B,Ser}}$
IFE		$\frac{\pi P}{2V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}}$	$\frac{uV_{\mathrm{b,MV}}}{2V_{\mathrm{LV}}M_{\mathrm{N}}}$	$n_{\mathrm{IFE}} \cdot \tilde{I}_{\mathrm{SRC,MV,IFE}}$	$\frac{2\sqrt{3}Pn_{\mathrm{IBE}}}{3V_{\mathrm{ph}}} \cdot \sqrt{3 - \frac{4\sqrt{2}V_{\mathrm{ph}}}{\pi N_{\mathrm{IFE}} n_{\mathrm{IFE}} V_{\mathrm{LV}}}}$	$\frac{4\sqrt{3}P}{3} \cdot \sqrt{\frac{\sqrt{2}n_{\mathrm{IFE}}}{\pi V_{\mathrm{ph}} N_{\mathrm{IFE}} V_{\mathrm{LV}}}}$
IBE	$\frac{2\sqrt{2}P}{V_{\mathrm{ph}}}$	$\frac{\sqrt{3}\pi P M_{\mathrm{N}}}{4V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}}$	$\frac{uV_{\mathrm{b,MV}}}{2V_{\mathrm{LV}}}$	$n_{\mathrm{IBE}} \cdot \tilde{I}_{\mathrm{SRC,MV,IBE}}$		

transformer current pulses, the relation between local average and local RMS values is given by (cf. [4])

$$\tilde{i}_{\mathrm{T,IFE}}(t) = \sqrt{\frac{\pi^2}{8} \cdot \frac{f_0}{f_{\mathrm{s}}}} \cdot \bar{i}_{\mathrm{T,IFE}}(t), \tag{7}$$

where f_0 and f_{s} are the resonant and the switching frequency of the SRC stage, respectively. The transformer RMS current over a grid period can then be calculated with

$$\tilde{I}_{\mathrm{T,IFE}} = \sqrt{2f_{\mathrm{g}} \int_0^{\frac{1}{2f_{\mathrm{g}}}} \tilde{i}_{\mathrm{T,IFE}}(t)^2 dt} = \frac{\sqrt{2}}{2} \cdot \frac{\pi P}{V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}}. \tag{8}$$

Likewise, the transformer current for the IBE system becomes

$$\tilde{I}_{\mathrm{T,IBE}} = \frac{\sqrt{6}M_{\mathrm{N}}}{4} \cdot \frac{\pi P}{V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}}. \tag{9}$$

Note that a direct comparison of the results for the IFE and for the IBE transformer current is not meaningful, since the rated power per transformer is lower for the IBE system, because $N_{\mathrm{IBE}} > N_{\mathrm{IFE}}$; i. e., the currents differ because $\bar{i}_{\mathrm{T,IBE}} \propto \sin(2\pi f_{\mathrm{g}} t)^2$ and $\bar{i}_{\mathrm{T,IFE}} \propto \sin(2\pi f_{\mathrm{g}} t)$, but also because of M_{N} and hence the different number of cascaded cells.

Instead, the area products of the transformers can be calculated according to

$$(A_{\mathrm{c}}A_{\mathrm{w}})_{\mathrm{IFE}} = \frac{\sqrt{2}V_{\mathrm{ph}}}{2N_{\mathrm{IFE}}} \cdot \frac{\tilde{I}_{\mathrm{T,IFE}}}{k f_{\mathrm{s}} B_{\max} J_{\mathrm{rms}}} \quad \text{and} \tag{10}$$

$$(A_{\mathrm{c}}A_{\mathrm{w}})_{\mathrm{IBE}} = \frac{\sqrt{2}V_{\mathrm{ph}}}{2M_{\mathrm{N}}N_{\mathrm{IBE}}} \cdot \frac{\tilde{I}_{\mathrm{T,IBE}}}{k f_{\mathrm{s}} B_{\max} J_{\mathrm{rms}}}. \tag{11}$$

Considering (2), the area product of a single IFE transformer is larger than that of an IBE transformer because of the difference in RMS currents only; however, the IBE system requires more transformers. The "total" area products of the IFE and the IBE concept compare as

$$\frac{N_{\mathrm{IFE}} \cdot (A_{\mathrm{c}}A_{\mathrm{w}})_{\mathrm{IFE}}}{N_{\mathrm{IBE}} \cdot (A_{\mathrm{c}}A_{\mathrm{w}})_{\mathrm{IBE}}} = \frac{2}{\sqrt{3}} \approx 1.15, \tag{12}$$

and the ratio of the total transformer volumes accordingly as

$$\frac{V_{\mathrm{T,IFE}}}{V_{\mathrm{T,IBE}}} \propto \frac{N_{\mathrm{IFE}} \cdot (A_{\mathrm{c}}A_{\mathrm{w}})_{\mathrm{IFE}}^{3/4}}{N_{\mathrm{IBE}} \cdot (A_{\mathrm{c}}A_{\mathrm{w}})_{\mathrm{IBE}}^{3/4}} = \left(\frac{2^3 M_{\mathrm{N}}}{3\sqrt{3}}\right)^{\frac{1}{4}} \approx 1.05, \tag{13}$$

where $M_{\mathrm{N}} = 0.8$ has been assumed to obtain a numerical result. The total usage of active materials is thus comparable.

In order to analyze the transformer losses, it is now assumed that identical transformers are used in both systems. Core loss densities can be estimated using the Steinmetz equation, $p_{\mathrm{c}} = k f^{\alpha} \hat{B}^{\beta}$, where $\beta \approx 2 \ldots 2.5$ for typical core materials suitable for MF transformers. Whereas in the IBE system, $\hat{B}$ is constant and hence the transformer core loss density is given by $p_{\mathrm{c,IBE}} = k f_{\mathrm{s}}^{\alpha} B_{\max}^{\beta}$, it varies with the grid voltage in the IFE system (cf. **Fig. 11c**), i. e., $\hat{B}_{\mathrm{IFE}}(t) = B_{\max} \sin 2\pi f_{\mathrm{g}} t$, if the same maximum flux density, $B_{\max}$ is allowed in both systems. Therefore, the core loss density in the IFE system can be found by averaging over a grid period,

$$p_{\mathrm{c,IFE}} = \frac{2}{T_{\mathrm{g}}} \int_0^{T_{\mathrm{g}}/2} k f_{\mathrm{s}}^{\alpha} B_{\max}^{\beta} \sin(2\pi f_{\mathrm{g}} t)^{\beta} dt. \tag{14}$$

For $\beta = 2$, this integral can be solved analytically, resulting in $p_{\mathrm{c,IFE}} = 1/2 \cdot k f_{\mathrm{s}}^{\alpha} B_{\max}^{\beta}$, i. e., $p_{\mathrm{c,IFE}}/p_{\mathrm{c,IBE}} \leq 1/2$ for $\beta \geq 2$. In contrast, the winding loss densities scale with the current densities squared and since the same core geometries are assumed, with the transformer RMS currents according to

$$\frac{p_{\mathrm{w,IFE}}}{p_{\mathrm{w,IBE}}} = \left(\frac{\tilde{I}_{\mathrm{T,IFE}}}{\tilde{I}_{\mathrm{T,IBE}}}\right)^2 = \frac{4}{3M_{\mathrm{N}}^2} \approx 2.08. \tag{15}$$

Assuming further that the IBE transformers are designed with a 1:1 ratio between core and winding losses at rated power, the total transformer losses compare as

$$\frac{p_{\mathrm{T,IFE}}}{p_{\mathrm{T,IBE}}} = \frac{N_{\mathrm{IFE}} \cdot \left(\frac{1}{2}\frac{p_{\mathrm{c,IFE}}}{p_{\mathrm{c,IBE}}} + \frac{1}{2}\frac{p_{\mathrm{w,IFE}}}{p_{\mathrm{w,IBE}}}\right)}{N_{\mathrm{IBE}} \cdot \left(\frac{1}{2} + \frac{1}{2}\right)} = \left(\frac{M_{\mathrm{N}}}{4} + \frac{2}{3M_{\mathrm{N}}}\right), \tag{16}$$

resutling in 1.03 for $M_{\mathrm{N}} = 0.8$. The total transformer losses are comparable, although with the assumption of using the same core and winding arrangement, the total transformer volume of the IFE amounts to only M_{N} (< 1) times that of the IBE. An optimized IFE transformer would thus use a slightly different core geometry, offering a larger winding window and a smaller core cross section, because a higher utilization of the core (with sufficient margin towards saturation) could be tolerated.

C. Power Semiconductors

A comparison of the semiconductor requirements of two different converter topologies can be based on the sum of all devices' RMS currents [30], since

$$\sum \tilde{I}_{\mathrm{x,MV}} \propto A_{\mathrm{Chip,MV}} \propto P_{\mathrm{cond,MV}}. \tag{17}$$

The RMS currents of the power semiconductors in the SRC isolation stages can be calculated from the transformer currents, and, on the LV side, the transformer turns ratio, n. The RMS currents of the IBE cells' active rectification units (ARUs) follow from the grid current, and the RMS currents of the IFE's boost stage switches (considering one boost stage per IFE cell) can be analytically calculated, too. **Tbl. II** contains the corresponding expressions. Note that it is assumed that all rectifier stages operate actively, i. e., only FETs are considered.

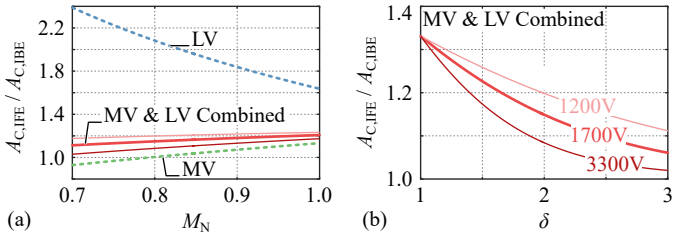

Fig. 12. Ratio of the chip area requirements of IFE and IBE systems as a function of the nominal modulation index, M_N in **(a)**, and in **(b)** as a function of δ in $r_\mathrm{on} \propto V_\mathrm{B}^\delta$ for $M_\mathrm{N} = 0.8$. For the combined metric, $u = 0.66$, $f_\mathrm{s} = f_0$, $V_\mathrm{LV} = 400\,\mathrm{V}$ is assumed, and three different MV semiconductor blocking voltages are considered.

TABLE III. Summary of the comparative analysis for $M_\mathrm{N} = 0.8$ and $f_\mathrm{s} = f_0$, and for the aggregated A_Chip ratio also assuming $\delta = 2$, $u = 0.66$, $V_\mathrm{LV} = 400\,\mathrm{V}$, and $V_\mathrm{B} = 1700\,\mathrm{V}$.

	IFE	IFE*	IBE
N	0.80	0.80	1.00
$N \cdot (A_\mathrm{c} A_\mathrm{w})$	1.15	1.15	1.00
V_T	1.05	1.05	1.00
n_Switch	0.80	0.96	1.00
Rel. *VA*-rating	1.30	1.17	1.00
A_Chip	1.15	1.11	1.00

Using the number of devices according to **Fig. 10** and N_IFE and N_IBE, respectively, the sums of the MV side and of the LV side semiconductor RMS currents can be compared (assuming $f_\mathrm{s} = f_0$ and $M_\mathrm{N} = 0.8$ for the numerical result):

$$\frac{\sum \tilde{I}_\mathrm{x,MV,IFE}}{\sum \tilde{I}_\mathrm{x,MV,IBE}} = \frac{4\pi M_\mathrm{N}}{\sqrt{3}\pi M_\mathrm{N} + 4\sqrt{2}} \approx 1.00 \qquad (18)$$

$$\frac{\sum \tilde{I}_\mathrm{x,LV,IFE}}{\sum \tilde{I}_\mathrm{x,LV,IBE}} = f(M_\mathrm{N}) \approx 2.08 \qquad (19)$$

Fig. 12a shows these ratios, which according to (17) correspond to the ratios of the required chip area, as a function of M_N, which is the only variable these metrics depend on. The semiconductor area requirement on the LV side is thus significantly larger for the IFE than for the IBE.

In order to merge the ratios for the MV and for the LV side into a single characteristic value, the theoretical scaling of the specific on-state resistance with the blocking voltage is considered, which for SiC FETs is given by [31], [32]:

$$r_\mathrm{on} \propto V_\mathrm{B}^\delta \qquad \delta \approx 2 \ldots 2.5 \qquad (20)$$

In order to account for the lower specific on-state resistance, and the hence lower chip area requirement for the same loss density (as implied by the linear sum of device RMS currents in (17)) of the LV side power devices, the contributions of the LV devices' RMS currents need to be scaled according to

$$\tilde{I}'_\mathrm{x,LV,\cdot} = \left(\frac{V_\mathrm{B,LV}}{V_\mathrm{B,MV}}\right)^\delta \cdot \tilde{I}_\mathrm{x,LV,\cdot}, \quad \text{where } V_\mathrm{B,LV} = \frac{V_\mathrm{LV}}{u_\mathrm{LV}}, \qquad (21)$$

and where u_LV denotes the blocking voltage utilization of the LV side semiconductors, which is assumed to be equal to u on the MV side. From that, an aggregated ratio of the total chip area requirements of both concepts can be derived as

$$\frac{A_\mathrm{Chip,IFE}}{A_\mathrm{Chip,IBE}} \propto \frac{\sum \tilde{I}_\mathrm{x,MV,IFE} + \sum \tilde{I}'_\mathrm{x,LV,IFE}}{\sum \tilde{I}_\mathrm{x,MV,IBE} + \tilde{I}'_\mathrm{x,MV,IBE}} \approx 1.15, \qquad (22)$$

where the numerical value is for $\delta = 2$, $M_\mathrm{N} = 0.8$, $u = 0.66$, $V_\mathrm{LV} = 400\,\mathrm{V}$, $V_\mathrm{B} = 1700\,\mathrm{V}$, and $f_\mathrm{s} = f_0$. Hence, the IFE system requires about $15\,\%$ more chip area than the IBE, generating also higher conduction losses. Note that this ratio, in addition to M_N, also depends on the utilization, $u = u_\mathrm{LV}$, the LV output DC voltage, V_LV, and the MV side device blocking voltage, V_B; however, it does not depend on the rated power, P, nor on the voltage level, V_ph. **Fig. 12a** and **b** show the dependency of this ratio on M_N, and on δ, respectively, where also three different values for V_B are considered. In the scope of further analysis, additional effects such as the dependence of the permissible loss density in the semiconductors on the blocking voltage as well as costs per chip area should be included into the considerations.

Another performance index to compare the semiconductor effort is the required relative VA rating [30], which is given by

$$\frac{1}{P} \cdot \sum i_\mathrm{x,max,IFE} u_\mathrm{x,max,IFE} = \frac{4(2\pi M_\mathrm{N} + \pi + 1)}{M_\mathrm{N}}, \qquad (23)$$

$$\frac{1}{P} \cdot \sum i_\mathrm{x,max,IBE} u_\mathrm{x,max,IBE} = \frac{8(\pi M_\mathrm{N} + 1)}{M_\mathrm{N}}, \qquad (24)$$

where $i_\mathrm{x,max}$ and $v_\mathrm{x,max}$ denote the peak current and the maximum switching voltage of the individual devices. Note that for the analytic expression again $f_\mathrm{s} = f_0$ has been assumed. The ratio between this performance indices then becomes

$$\frac{\frac{1}{P} \cdot \sum i_\mathrm{x,max,IFE} u_\mathrm{x,max,IFE}}{\frac{1}{P} \cdot \sum i_\mathrm{x,max,IBE} u_\mathrm{x,max,IBE}} = \frac{2M_\mathrm{N}\pi + \pi + 1}{2(M_\mathrm{N}\pi + 1)} \approx 1.3, \qquad (25)$$

which means that the total installed switching power is about 30% higher in the IFE (for $M_\mathrm{N} = 0.8$).

In addition to conduction losses, also switching losses arise in the IFE's boost stage and in the IBE's active rectification units, which will be briefly addressed in the case study in section IV. In contrast, the isolation stages operate with ZVS—although not over the entire grid period in the IFE case due to the varying voltage, which will be analyzed in the scope of a further publication [33].

Since each switch requires a separate gate drive unit (GDU), the total switch count is an interesting characteristic. From **Fig. 10** it follows that the total number of switches becomes $n_\mathrm{Switch,IFE} = (4+4+2) \cdot N_\mathrm{IFE}$ (assuming one boost stage per cell) and $n_\mathrm{Switch,IBE} = (4+2+4) \cdot N_\mathrm{IBE}$, respectively. Thus, the IFE system requires only M_N (< 1) times the number of individual switches and GDUs compared to the IBE.

D. Summary of Theoretical Considerations

Tbl. III summarizes the key results of the generic comparative analysis of an IFE and an IBE SST system. The IFE system requires less series connected cells, approximately the same total transformer volume, but clearly a higher effort in terms of power semiconductors. However, this additional effort is on the LV side, and typically semiconductor prices scale

with blocking voltage. Also the reduced number of individual switches and hence GDUs might alleviate the result of the chip area comparison to some extent.

In addition to the IFE system discussed above and shown in **Fig. 10a**, also the results for an IFE* system are shown in **Tbl. III**. The converter cells of an IFE* system do not use bidirectional switches, but a dedicated active full-bridge rectifier on the AC side and a simple half-bridge on the SRC's MV side, i. e., their MV side structure is identical to that of an IBE cell—with two important differences: the capacitor is only a resonant capacitor, and the active rectifier is not used to shape the current but switches only at grid frequency to fold the grid voltage. Such an approach would slightly lower the semiconductor effort in terms of chip area requirement and relative VA rating, but on the other hand the complexity and the number of semiconductors, GDUs, etc. would increase.

E. Further Aspects

1) Other Magnetic Components: In addition to the transformer, the IFE requires boost inductors on the LV side and a smaller grid filter inductor on the MV side, whereas the IBE only requires a single boost/filter inductor on the MV side. Discussing the design trade-offs is beyond the scope of this paper; however, it should be mentioned that the IFE boost stages could operate in TCM mode [34] or with higher current ripple, because the aIFE acts as a low-pass filter towards the grid if the (effective) boost stage switching frequency is chosen high enough, whereas on the other hand, the current stress seen by the IBE boost inductor is lower, and also the HF content of the current, since the input current quality must already comply with grid harmonic standards.

2) Capacitors: The IFE requires only small resonant capacitors on the MV side of the cells, reducing the physical size of the assemblies on floating potential, and one larger capacitor to buffer the single-phase power fluctuation on the LV side (which could be made smaller in case of a three-phase configuration). In contrast, the IBE requires a certain amount of the energy buffering to be performed on the MV side in order to provide a reasonably constant DC voltage for the ARU stage, which is the case even in a three-phase configuration. If a controllable isolation stage (e. g., a DAB) would be used in the IBE, the energy buffering could be forced to take place on the MV side where a comparatively high voltage ripple could be tolerated, while the isolation stage would transfer only DC power, reducing RMS currents and enabling a perfectly flat DC output voltage without significant capacitance on the LV side.

3) Common-Mode Currents and Isolation Stress: In an IBE system, the entire MV side assemblies of the cascaded cells change their potential with respect to earth at a dv/dt defined by the switching actions of the cells in the stack, which may give rise to very high common-mode currents to ground, possibly requiring appropriate countermeasures [35], and which would also increase the dv/dt stress seen by the isolation barrier [36]. The IFE system's cells, however, are essentially connected to each other by means of a capacitive voltage divider. The maximum dv/dt depends on the value of $C_{\mathrm{r},1}$ and the transformer currents; it is in any case orders of magnitudes lower than that of switching edges. This is beneficial with respect to converter EMI emissions and isolation material stress.

TABLE IV. Specifications for the case study.

Grid voltage (line to line RMS), V_{ll}	6.6 kV
Power, P	25 kW
Nom. mod. index, M_{N}	0.8
SRC switching freq., f_{s}	50 kHz
SRC resontant freq., f_0	$\approx$ 52 kHz
ARU/Boost sw. freq., f_{s}, h	25 kHz
DC output voltage	400 V
N_{IFE}, n_{IFE}	5, 1.75:1
N_{IBE}, n_{IBE}	6, 1.40:1

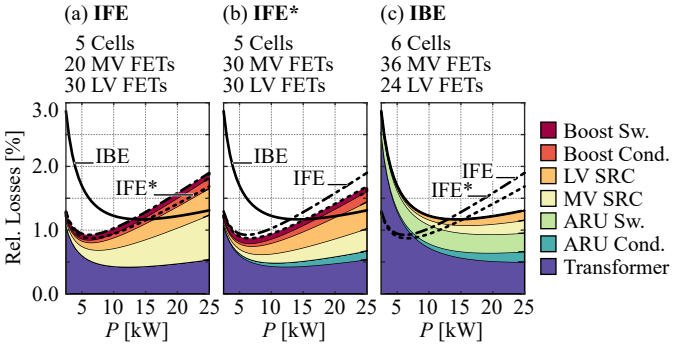

Fig. 13. Relative semiconductor and transformer losses for the three systems considered in the case study.

IV. Case Study: The Swiss SST (S^{3}T)

In order to exemplify the above theoretical considerations, this section briefly considers a 25 kW, 6.6 kV AC (line-to-line) to 400 V DC all-SiC realization of an IFE-based SST that is developed in the scope of a research program funded by the Swiss government [37], and accordingly denominated as Swiss SST (S^{3}T). **Tbl. IV** shows additional specifications considered for this case study, where Wolfspeed's upcoming 1700 V/45 mΩ and 900 V/11.5 mΩ SiC FETs are considered [38] (no paralleling, 125 °C junction temperature). ZVS switching losses are neglected, and hard switching losses of the ARU or the boost stages are modeled using datasheet values. It is assumed that the same transformers are used for all systems, and that the IBE transformers feature an efficiency of 99.5 % at rated power with an 1:1 distribution of core and winding losses.

Fig. 13 shows a comparison of calculated semiconductor and transformer losses of the three concepts discussed in the last section (IFE, IFE*, and IBE) as a function of the output power. The IBE system benefits from its lower RMS currents at high output power levels, which could be further improved at the cost of higher complexity by using a controllable DAB isolation stage, whereas the IFE system realizes lower part-load losses due to lower switching and transformer core losses. Note also that the realization effort of the IFE system is lower, because only 50 power semiconductors and GDUs are required compared to 60 in the IBE, and because the number of (identical) transformers is lower (5 instead of 6), too. In contrast, the IFE* system uses the same number of semiconductors as

the IBE system, and the changed MV side circuit structure helps to reduce conduction losses compared to the IFE. Note that additional losses of the boost and filter inductors, the capacitors, the control circuitry, etc. are not considered here but will be subject of further publications containing a more detailed, hardware-based comparison of the S^{3}T-IFE SST and a corresponding IBE realization.

V. Conclusion

This paper provides a detailed description of an isolated front end (IFE) concept for MVAC-LVDC SSTs, and provides a very generic comparison of the IFE with the mostly used isolated back end (IBE) concept. The IFE approach allows to minimize complexity on the MV side, since all control and measurement tasks can be performed by a secondary side non-isolated boost-type |AC|-DC stage, whereas a resonant autonomous isolation front end (aIFE) provides isolation by means of medium frequency transformers, thereby reducing size and weight compared to a line frequency transformer. Because the boost stage is moved to the secondary side, the total MV side blocking voltage, i. e., the number of cascaded cells, can be reduced. Also, the cells' MV side assemblies do not change their potential at high dv/dt, reducing issues with common-mode ground currents. However, this comes at the cost of a higher effort in terms of required power semiconductor chip area (factor 1.15) and higher RMS currents in the isolation stage, including the MF transformers, when compared to an IBE system. On the other hand, results of a case study considering the 25 kW, 6.6 kV AC to 400 V DC all-SiC Swiss SST (S^{3}T) show that the IFE generates lower switching and transformer core losses, resulting in lower total losses for part load operation. Thus, following an SST development vector pointing towards maximum simplification instead of maximum performance (and maximum complexity), the IFE concept might have advantages in applications where weight and volume constraints are the main driver to move from line frequency to medium frequency isolation stages and where low complexity is desirable, and where part-load operation is dominant. Such an application could, e. g., be auxiliary supplies in traction applications, as, e. g., used for climate control units, lighting, etc. of individual coaches. The IFE approach would allow to interface these auxiliary supplies directly to a MV bus running along a train and thereby removing the need for additional LV buses.

Appendix

A. Three-Phase Configurations

By connecting three single-phase IFE systems (cf. **Fig. 7**) either in a star or possibly also in a delta configuration, a three-phase IFE SST can be realized. Such a configuration allows to reduce the output buffer capacitance requirement, since ideally the power contributions of the three phases add up to a constant value at the common LV output. In contrast to an IBE system, also no energy buffering is required on the MV side of the cascaded cells. **Fig. 14** shows simulation results of a three-phase IFE SST (considering the specs from **Tbl. IV** for each phase) in star configuration with one boost stage per cell (cf. **Fig. 7b**) switching at 75 kHz (with interleaving between the boost stages) and implementing average current control,

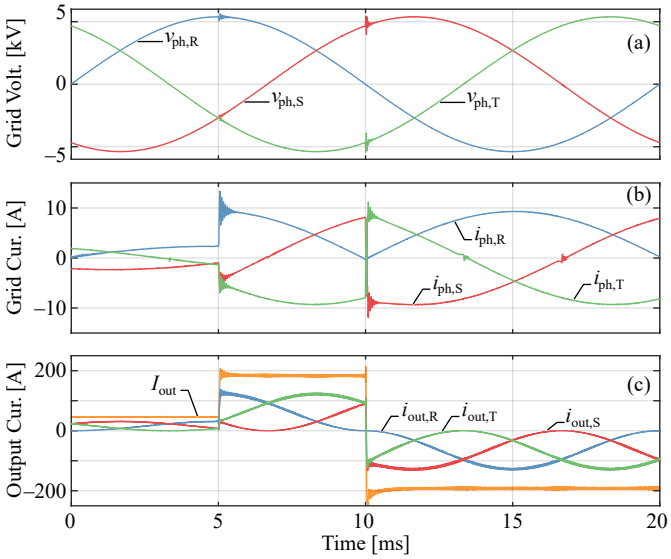

Fig. 14. Simulation of a three-phase IFE SST system including transients.

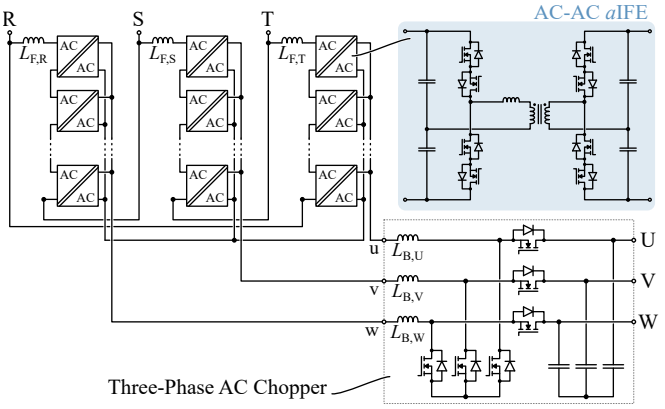

Fig. 15. Three-phase IFE SST for AC-AC applications.

which is used to perform step changes of the output current and also a transition from rectifier to inverter operating mode.

B. AC-AC Operation

In one of the first publications mentioning an "electronic transformer" [25], the HC-DCM SRC has also been used in an AC-AC configuration. **Fig. 15** shows a three-phase ISOP arrangement using such AC-AC aIFEs. If output voltage control is required, a three-phase AC chopper can be connected on the LV side (cf. [39] for a review of AC choppers). Of course, also a single-phase configuration could be realized.

C. Scott Transformer Configuration

A Scott transformer configuration as shown in **Fig. 16a** allows to transform a symmetrical three-phase voltage system into a two-phase system with 90° phase shift between the voltages [40]. This two-phase system can be interfaced using only two appropriately controlled non-isolated single-phase PFC stages to generate two DC output voltages while ensuring balanced three-phase currents on the input side [41]. In order to reduce weight and volume, the magnetic Scott transformer windings could be replaced by IFE stacks as shown in **Fig. 16b**,

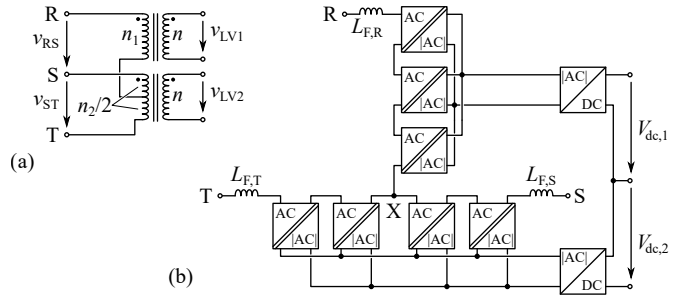

Fig. 16. **(a)** Magnetic Scott transformer, **(b)** IFE-based Scott transformer configuration.

where the number of cells, the MF transformer turns ratios and the control of the two |AC|-DC stages must be such that the voltage sharing as well as Ampère's Law of the magnetic Scott transformer are emulated. Please refer to [24] for a more detailed description of the concept.

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