A New Concept for Reconstruction of the Input Phase Currents of a Three-Phase/Switch/Level PWM (VIENNA) Rectifier Based on Neutral Point Current Measurement

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Abstract. A novel concept utilizing the neutral point current information which is gained by an AC current sense transformer or a shunt for observer-based continuous reconstruction of the input phase currents of a three-phase/switch/level boost-type PWM (VIENNA) rectifier system is proposed. The basic principle of operation and the dimensioning of the observer circuit which in modified form also could feature an output voltage earth fault detection are discussed in detail. Furthermore, results of a practical application of the system in connection with a highly dynamic ramp comparison mains current control of a 10kW laboratory model of the VIENNA rectifier are given.

1 Introduction

The DC-link current of three-phase voltage-source PWM rectifier systems is formed by sections of the input phase currents which are impressed by inductors connected in series on the AC side dependent on the switching state of the power transistors (Fig.9 in [1]). Therefore, it is obvious to reconstruct the input phase currents (which are required for the current control of the rectifier system) based on a measurement of the DC link current. Thereby, as compared to a direct measurement of two input phase currents (the third phase current can be calculated since the sum of all three mains phase currents is forced to zero for missing connection of the rectifier output voltage center point and the mains star point) the measurement effort is reduced and problems concerning different current transducer gains or DC offsets of the measured phase currents are eliminated.

In the literature this concept so far has been discussed only for three-phase *two-level* PWM *inverter* systems. E.g., in [2]-[7] two phase currents are determined within each pulse half period by sampling of the DC-link current. There, the PWM signals have to be adjusted for operating conditions where the time for which one or both phase currents appear in the DC link may fall below a minimum value beyond which reliable sampling is not possible as, e.g., in the case of low modulation index or overmodulation. Alternatively, for ensuring a reliable current information under all operating conditions one also could employ a state observer and/or machine model [8], [9]. There, the estimated phase current samples are corrected in a closed loop manner in case samples of the currents can be directly measured in the DC link otherwise the observer continues to provide phase current information in open loop.

In this paper a new concept for an observer-based reconstruction of the mains phase currents of a three-phase *three-level* PWM *rectifier* system (VIENNA rectifier) is proposed. There, in contrast to sampled data based concepts as discussed in the literature so far a *continuous* mains phase current information is derived for a ramp comparison control of the input phase currents which is realized in analogue technique because of the high switching frequency $f_p \approx 30...50$kHz. In **section 2** the basic function of the VIENNA rectifier and the formation of the neutral point current are discussed. In **section 3** the reconstruction of the input phase currents based on neutral point current measurement (as gained by an AC current sense transformer) and information about the rectifier switching state (cf. **Fig.1** and/or [11]) is treated in detail. Furthermore, in **section 4** the practical realization of the current observer system is discussed. Finally, in **section 5** guidelines for dimensioning the observer components are given and experimental results as gained from an application of the system in a 10kW laboratory model of the VIENNA rectifier are shown.

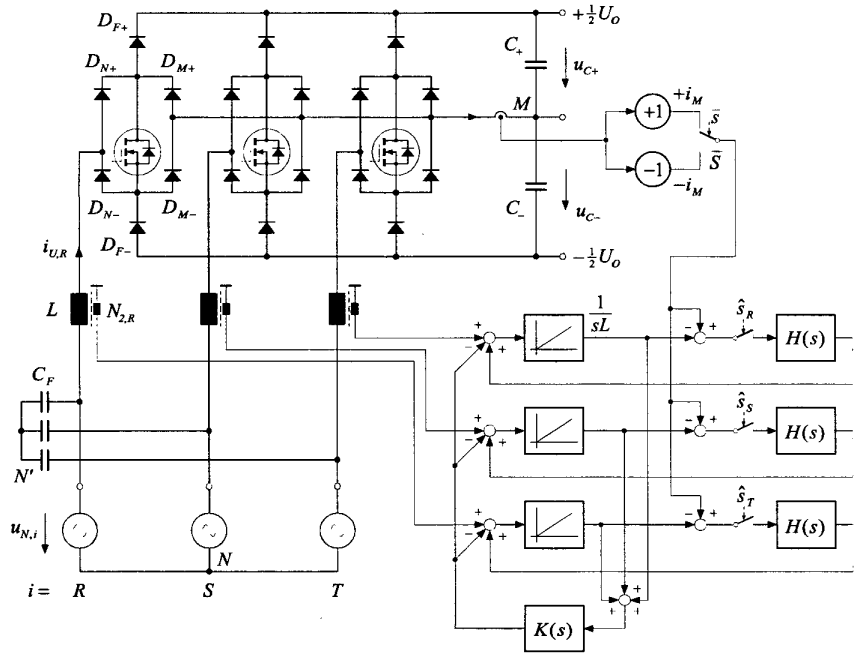

Fig. 1: Structure of the power circuit of the VIENNA rectifier (three-phase/switch/level PWM rectifier system) [10] and of the proposed circuit for the reconstruction of the mains phase currents based on measurement of the center point current i_M [11].

2 Basic Function of the VIENNA Rectifier

2.1 Control of the Rectifier Input Voltage

In the turn-off state of a power transistor S_i the current $i_{U,i}$ of a phase $i = R, S, T$ which is impressed by the respective input side inductor L is flowing via the diodes $D_{N+,i}$ and $D_{N-,i}$ into the positive (upper) DC link rail for $i_{U,i} > 0$; for $i_{U,i} < 0$ the current flow is via $D_{F-,i}$ and $D_{N-,i}$ out of the negative (lower) DC link rail. Accordingly, on the input side of the rectifier bridge leg a voltage $u_{U,i} = +\,^1/_2\, U_O$ or $u_{U,i} = -\,^1/_2\, U_O$ will appear with reference to the output voltage center point M. In contrast, for S_i in the turn-on state a bidirectional connection of the input side of a phase leg and M is given and the current flow is via $D_{N+,i}$, S_i, $D_{M-,i}$ or $D_{N-,i}$, S_i, $D_{M+,i}$, i.e. we have for the rectifier input voltage $u_{U,i} = 0$ independent of the direction of the phase current flow (cf. **Fig.2**). Accordingly, besides the binary switching function s_i ($s_i = 1$ denotes the turn-on state and $s_i = 0$ the turn-off state of a power transistor S_i) also the sign sign($i_{U,i}$) of a phase current $i_{U,i}$ takes influence on the resulting rectifier input voltage

$$u_{U,i} = \begin{cases} \frac{U_O}{2} \cdot \mathrm{sign}(i_{U,i}) & \text{if} \quad s_i = 0 \\ 0 & \text{if} \quad s_i = 1 \end{cases} . \tag{1}$$

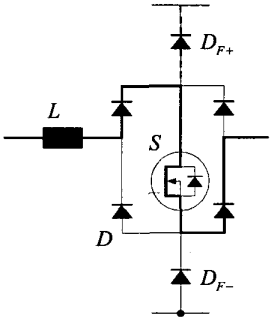

Fig.2: Conduction states of a bridge leg for positive and negative input current (current path for power transistor S in the turn-off state shown by a dashed line).

By considering the phase symmetry of the converter structure for the assumption of a purely sinusoidal mains voltage system a detailed analysis of the rectifier system can be constrained to a $^\pi/_3$-wide interval, e.g., to $\varphi_N \in (-^\pi/_6, +^\pi/_6)$ of the mains period $f_N = 1/T_N$, where $i_{U,R} > 0$, $i_{U,S} < 0$, $i_{U,T} < 0$ is valid. As discussed in [12] in this case the $2^3 = 8$ possible combinations $j = (s_R, s_S, s_T)$ of phase switching functions result in the rectifier input voltage space vectors shown in **Fig.3**.

In order to achieve a purely sinusoidal input current one would have to form a rectifier input voltage space vector

$$\underline{u}_U^* = \hat{U}_U^* \exp j\varphi_U = \underline{u}_N - j\omega_N L \underline{i}_{U,(1)} = \underline{u}_{U,(1)} \tag{2}$$

($\underline{u}_N = \hat{U}_N \exp j\varphi_N$, $\varphi_N = \omega_N t$) of constant magnitude and constant angular speed ω_N, $\underline{i}_{U,(1)}$ denotes the space vector and/or phasor of the input current fundamental, $\underline{u}_{U,(1)}$ designates the space vector and/or phasor of the rectifier input voltage fundamental). Since, however, only 8 discrete voltage space vectors $\underline{u}_{U,j}$ are available (cf. Fig.3) the actual voltage formation is in a discontinuous manner, i.e. the space vector $\underline{u}_U^*$ is formed in the average over a pulse half period $\frac{1}{2}\, T_P$ by a sequence of rectifier switching states j and/or voltage space vectors $\underline{u}_{U,j}$. There, the continuous rotation of the space vector $\underline{u}_U^*$ is approximated by shifting the reference voltage vector in phase for a respective following pulse half period $\underline{u}_{U,n}^* = \underline{u}_U^*(t_n) = \underline{u}_U^*(n.\frac{1}{2}T_P)$, $\underline{u}_{U,n+1}^* = \underline{u}_U^*(t_n + \frac{1}{2}T_P)$, (the discrete time t_n defines the position of a pulse half period within the mains period T_N).

As Fig.3 shows, there are 7 input voltage space vectors available for the approximation of $\underline{u}_{U,n}^*$. With regard to a best possible approximation one applies only those rectifier voltage space vectors $\underline{u}_{U,j}$ lying in the immediate vicinity of the vector tip $\underline{u}_{U,n}^*$ or those switching states j which are assigned to the corner points of that triangular region of the space vector plane into which the tip of the vector $\underline{u}_{U,n}^*$ points [14].

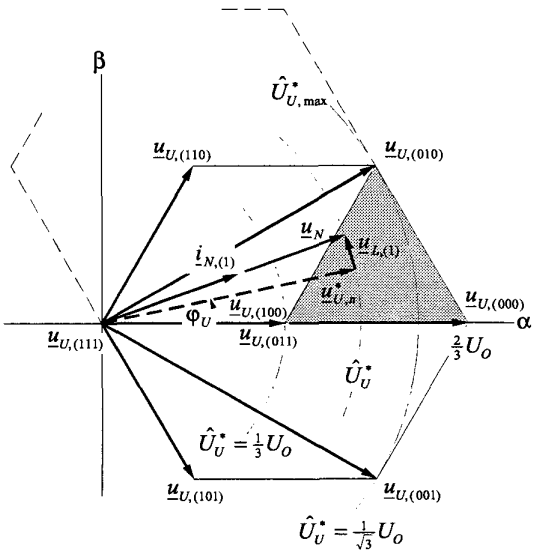

Fig.3: Rectifier input voltage space vectors $\underline{u}_{U,j}$ being available for the formation of a reference input voltage space vector $\underline{u}_{U,n}^*$ (space vector of the rectifier input voltage fundamental) for $i_{U,R} > 0$, $i_{U,S} < 0$, $i_{U,T} < 0$. Furthermore shown are the mains voltage space vector $\underline{u}_N$, the space vector $\underline{i}_{U,(1)}$ of the input current fundamental and the space vector $\underline{u}_{L,(1)}$ of the fundamental voltage drop across the rectifier input inductors L (ohmic resistance of the inductor windings neglected).

In order to minimize the switching frequency of the system we now arrange the switching states within each pulse half period in such a way that a subsequent state can always be obtained by switching of only one bridge leg. If we select arbitrarily (100) as initial switching state there results for the conditions of Fig.3 a switching sequence

$$\left|_{t_n=0}(100) \rightarrow (000) \rightarrow (010) \rightarrow (011)\right.$$
$$\left|_{t_n=\frac{1}{2}T_P}(011) \rightarrow (010) \rightarrow (000) \rightarrow (100)\right|_{t_n=T_P} \ldots \tag{3}$$

Due to the requirement of a minimum number of switchings one has to reverse the sequence of the voltage space vectors $\underline{u}_{U,j}$ after each pulse half period.

In the case at hand the switching state sequence Eq.(3) is formed by a ramp comparison current controller [14] (with superimposed output voltage control) by direct intersection of the phase current control error $\Delta i_{U,i}$ with a triangular-shaped carrier signal i_D (being common for all three phases) of switching frequency f_P (cf. **Fig.4**). This current control concept shows a low realization effort and ensures high dynamics and a constant switching frequency in contrast to, e.g., a tolerance band control [10] of comparable dynamic quality. The stationary current control error can be limited to very low values also for employing simple P-type controllers $R(s)$ by a mains voltage pre-control m_i [13]. By extending the pre-control by a third harmonic of amplitude $\frac{1}{4}\hat{U}_N$ a modulation range of $\hat{U}_U^* = 0...1/\sqrt{3}\, U_O$ (as being given, e.g., for space vector modulation of significantly higher complexity [14]) is available and/or overmodulation can be avoided also in case of relatively high amplitudes $\hat{U}_U^*$ of the rectifier input voltage fundamental.

2.2 Formation of the Center Point Current

As Fig.2 clearly shows, by turning on the power transistor of a phase ($s_i \rightarrow 1$, $i = R, S, T$) the corresponding phase current $i_{U,i}$ is fed into the neutral point M. For the total center point current being formed there by all phases we therefore have [12]

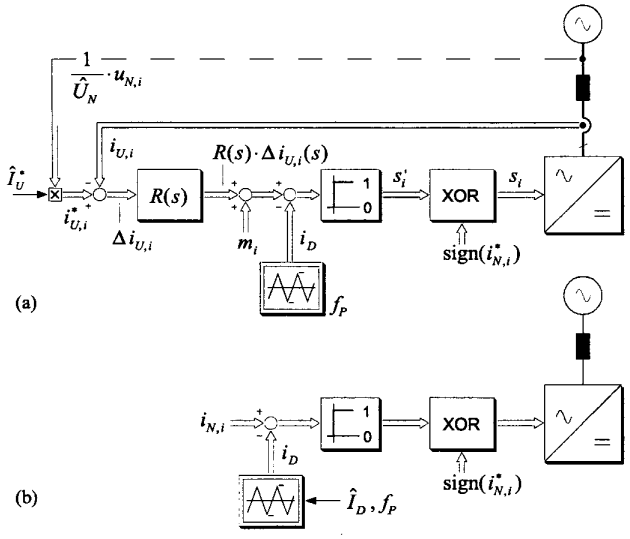

Fig.4: Block diagram of a conventional ramp comparison input current control [13] (cf. **(a)**). The amplitude $\hat{I}_U^*$ of the phase current reference values $i_{U,i}^*$ is set by an outer output voltage controller (not shown). For the sake of clarity signal paths being equivalent for all phases are combined into double lines for all phases. In the case at hand $R(s)$ is realized by a P-type controller. The switching decisions s_i' of the phase comparators have to be inverted for sign($i_{N,i}$) = -1 [13] due to the dependency of the rectifier input voltage formation on the sign of the phase currents (cf. Eq.(1)). Furthermore shown: modified ramp comparison current controller (cf. **(b)**) being characterized by low realization effort (no need to sense the mains voltage, no analog multipliers for determining the phase current reference values, no mains voltage pre-control). There, the control of the amplitude of the input current fundamental is performed via the amplitude $\hat{I}_D$ of the carrier signal i_D.

$$i_m = s_R i_{U,R} + s_S i_{U,S} + s_T i_{U,T} \,. \tag{4}$$

Accordingly, the switching states of the rectifier system lead to center point currents i_M as compiled in **Tab.1**.

s_R	s_S	s_T	i_M
0	0	0	0
0	0	1	$+i_{U,T}$
0	1	0	$+i_{U,S}$
0	1	1	$-i_{U,R}$
1	0	0	$+i_{U,R}$
1	0	1	$-i_{U,S}$
1	1	0	$-i_{U,T}$
1	1	1	0

Tab.1: Center point current i_M in dependency on the rectifier switching state (s_R, s_S, s_T).

3 Reconstruction of the Mains Phase Currents based on Center Point Current Measurement

According to **Tab.2** the center point current i_M within each pulse half period is formed by sections of in any case two input phase currents $i_{U,i}$. In order to minimize the measuring effort it therefore is near at hand to employ only a single current sensor in the connection to the output voltage center point (instead of a direct measurement of at least two input phase currents) and to reconstruct the phase current shapes under consideration of the the actual converter switching state (s_R, s_S, s_T).

switching state sequence	i_M
(100) → (101) → (001) → (011)	$+i_{U,R}$ → $-i_{U,S}$ → $+i_{U,T}$ → $-i_{U,R}$
(100) → (000) → (001) → (011)	$+i_{U,R}$ → 0 → $+i_{U,T}$ → $-i_{U,R}$
(100) → (000) → (010) → (011)	$+i_{U,R}$ → 0 → $+i_{U,S}$ → $-i_{U,R}$
(100) → (110) → (010) → (011)	$+i_{U,R}$ → $-i_{U,T}$ → $+i_{U,S}$ → $-i_{U,R}$

Tab.2: Switching state sequences and corresponding formation of i_M by sections of input phase currents $i_{U,i}$ for $\varphi_N \in (-\pi/6, +\pi/6)$ The consideration is based on the assumption of a high modulation index, i.e. $\hat{U}_U^* > 1/3\ U_O$, as typically given for the PWM rectifier systems with high output voltage utilization.

Therefore, in analogy to [8] and [9] the time-continuous phase current information which is required for a ramp comparison input current control can be derived by a state observer modeling the rectifier system AC side and the estimation error can be corrected based on measuring values of the center point current i_M (basic principle of the Luenberger observer).

The estimated value $\hat{i}_{U,i}$ of a phase current $i_{U,i}$ is calculated by integration of the voltage drop $u_{L,i}$ across the respective input inductor L. In time intervals where the center point current i_M is formed by the input current $i_{U,i}$ of a phase i (cf. Tab.1), a correction control $H(s)$ is activated in this phase ($\hat{s}_i \rightarrow 1$). As a result the estimated phase current $\hat{i}_{U,i}$ is corrected to the actual phase current shape $i_{U,i}$. (An estimation error $i_{U,i} - \hat{i}_{U,i}$ could result, e.g., due to inaccurate parameters of the system model or an inaccurate measurement of the voltage drop across the input inductors.) There, according to Tab.1 one has to perform an inversion of the measured center point current i_M for the switching states j = (011), (101) and (110) (cf. **Tab.3**) before comparing it with the estimated phase current $\hat{i}_{U,i}$.

s_R	s_S	s_T	$\hat{s}_R$	$\hat{s}_S$	$\hat{s}_T$	$\bar{s}$
0	0	0	0	0	0	x
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	1	0	0	1
1	0	0	1	0	0	0
1	0	1	0	1	0	1
1	1	0	0	0	1	1
1	1	1	0	0	0	x

Tab.3: Gating signals $\hat{s}_R$, $\hat{s}_S$, $\hat{s}_T$ of the switches S_R, S_S, S_T closing the feedback loops provided for the correction of the estimation $i_{U,i} - \hat{i}_{U,i}$ of the phase models in dependency of the rectifier switching state j=(s_R, s_S, s_T). The auxiliary signal $\bar{s}$ is employed for controlling the inversion of i_M which has to be performed for j= (011), (101), (110). The switching states (000) and (111) result in $i_M = 0$, accordingly, no correction of the observer outputs is possible ($\hat{s}_i = 0$) and the value of $\bar{s}$ is of no meaning.

Remark: The inductor voltages $u_{L,i}$ can be measured directly by differential amplifiers or by auxiliary secondary windings on the input inductors. Alternatively, the voltages also could be derived with low effort from the mains phase voltages $u_{N,i}$ (as available from the calculation of the phase current reference values, cf. Fig.4), the converter switching state j = (s_R, s_S, s_T) and the output voltage u_O (which in any case has to be measured in connection with the output voltage control or could be assumed here to be identical with the output voltage reference value for high quality output voltage control) based on

$$\begin{aligned} u_{L,i} &= u_{N,i} - (u_{U,i} - u_0) \\ u_0 &= \tfrac{1}{3}\left(u_{U,R} + u_{U,S} + u_{U,T}\right) \end{aligned} \tag{5}$$

and/or

$$\hat{u}_{L,i} = u_{N,i} - \text{sign}(\hat{i}_{U,i})(1-s_i)\frac{U_0}{2} + \hat{u}_0$$
$$\hat{u}_0 = \tfrac{1}{3}\sum_{i=R,S,T} \text{sign}(\hat{i}_{U,i})(1-s_i)\frac{U_0}{2} \quad (6)$$

(the common-mode voltage component u_0 of the rectifier input voltages has no influence on the current formation because of the missing connection between the mains star point N and the rectifier output voltage center point M). However, due to the dependency of the input voltage formation on the sign of the corresponding input current (cf. Eq. (1)) the quality of the input current reconstruction based on Eq.(6) could be impaired in the vicinity of the phase current zero crossings.

Due to the missing connection between mains star point N and the center point M of the rectifier output voltage the sum of the input phase currents is forced to zero, i.e.

$$i_{U,R} + i_{U,S} + i_{U,T} = 0\,, \quad (7)$$

which means that only 2 of the 3 rectifier input inductors represent independent energy storage devices. The current in the third input inductor is defined unequivocally if the currents of the other two phases are known and, therefore, does not represent a state variable. Therefore, the system model basically could be limited to two phases. The advantage of providing a model for each phase (cf. **Fig.1**) is the resulting phase symmetry of the observer which gives the opportunity of a direct correction of a phase model output for each switching state resulting in a center point current. However, there a system of second order is represented by a model of third order. Therefore, in order to ensure Eq. (7) also for the estimated phase currents $\hat{i}_{U,i}$ an additional controller $K(s)$ has to be provided which corrects a deviation $\varepsilon_0 = \hat{i}_{U,R} + \hat{i}_{U,S} + \hat{i}_{U,T}$ of the sum of the estimated phase current values from zero. Since during each pulse half period in any case the estimated current values of two phases are corrected by the respective controllers $H(s)$ due to $K(s)$ also the estimation of the third phase current is with low error.

4 Practical Realization of the Observer

As shown in Fig.1 the measurement of the voltage $u_{L,i}$ across an input inductor is realized advantageously by an auxiliary secondary winding $N_{2,i}$. For high resistance termination of the auxiliary winding there an output signal $u_{L,i,m}$ results which directly is proportional to the rate of change $di_{U,i}/dt$ of the respective input phase current. The reconstruction of the phase current therefore can achieved with low effort by integration of $u_{L,i,m}$ (cf. **Fig.5**, integrators Q_1, Q_2, Q_3). There, in contrast to measuring the total voltage occurring across the inductors

$$u_{L,i} = R_L i_{U,i} + \frac{\mathrm{d}Li_{U,i}}{\mathrm{d}t} \quad (8)$$

(e.g., by using a differential amplifier) the parasitic ohmic component $i_{U,i}R_L$ of $u_{L,i}$ must not be taken into account by the circuit model. As further advantage this form of voltage measurement provides galvanic isolation from the power circuit.

Remark: As shown in section 5 for rectifier systems in the power range of 5kW...20kW the input inductors typically show a lower limit of the inductive behavior (i.e., change from inductive to resistive behavior) at frequencies $f_L = {}^1/_{2\pi}\, R_L / L \approx 10$ ... 15Hz which is quite close to the mains frequency f_N. (f_L could be considered in the reconstruction of the current by a resistor connected in parallel to the capacitor C_I of the integrator).

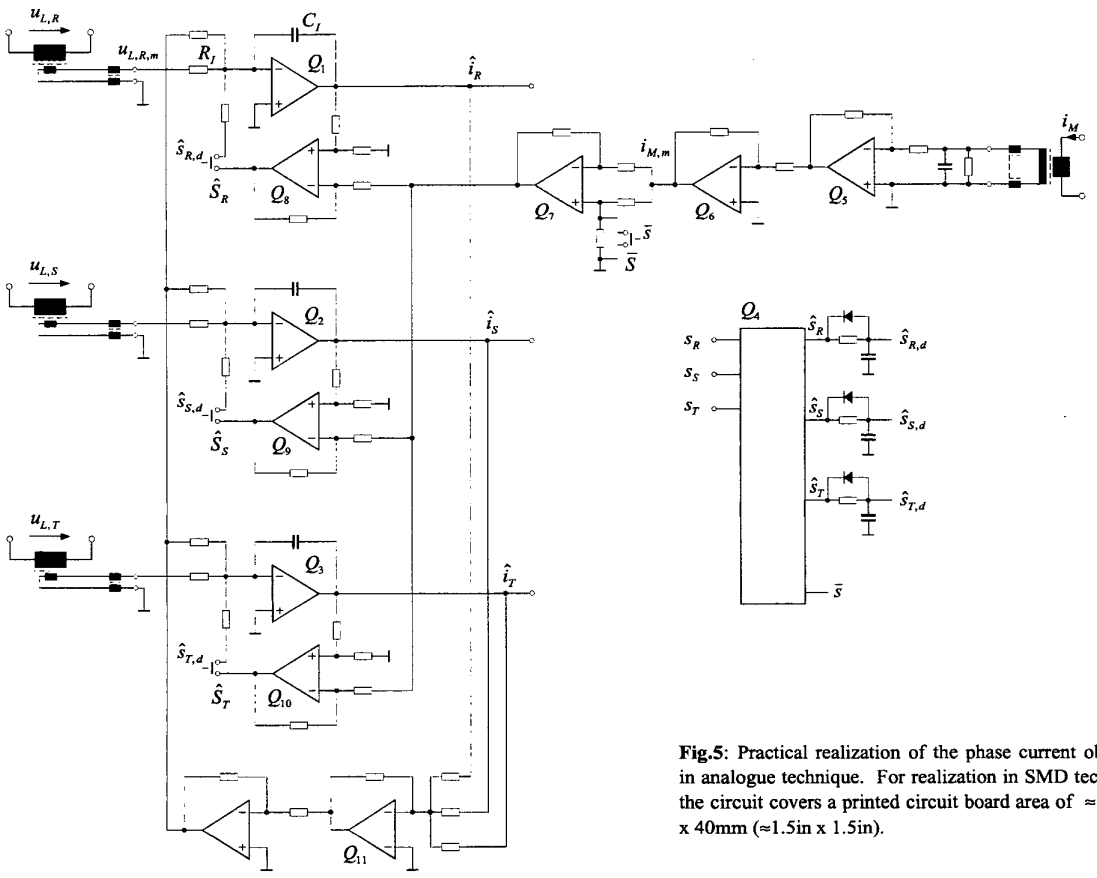

Fig.5: Practical realization of the phase current observer in analogue technique. For realization in SMD technique the circuit covers a printed circuit board area of ≈ 40mm x 40mm (≈1.5in x 1.5in).

4.1 Circuit Structure

The analogue circuit shown in Fig.5 is a direct translation of the block diagram of the input current observer depicted in Fig.1 into hardware, a detailed description therefore should be omitted for the sake of brevity.

However, it is important to note that the turn-on of the analog switches $\hat{S}_i$ is delayed by RC-elements R_D, C_D (t_d in Fig.7) with reference to the signals $\hat{s}_i$ which are derived by a 256-bit TTL-PROM Q_4 (e.g., AMD, AM27S19ACP) according to Tab.3 from the switching functions s_i. This realizes a blanking of the measured center point current $i_{M,m}$ for the correction control loops $H(s)$ in the time period required for the transition of $i_{M,m}$ to the actual signal level after a change of the rectifier switching state has occurred. The width of this transition period is defined by the time delay of the gate drive circuits of the power transistors and by the bandwidth and/or rise time of the amplifiers Q_5 and Q_6.

Contrary, the control of the inversion Q_7 of $i_{M,m}$ is without delay directly by $\bar{s}$. Accordingly, the total blanking interval t_d is available for the settling of the output of Q_7 which due to the large step change in the input signal is with limited dynamic as defined by the slew-rate of the operational amplifier employed.

5 Experimental Analysis

The theoretical considerations are verified in the following by a practical application of the observer for the determination of the instantaneous phase current values for a ramp comparison input current control of a prototype of the VIENNA Rectifier I.

Operating parameters of the VIENNA Rectifier I:

mains voltage:	U_N = 400 V_{rms} (line-to-line)
rated power:	P_O = 10 kW
output voltage:	U_O = 670 V
switching frequency:	f_P = 25 kHz .

The input inductors of the system are realized with toroidal iron powder cores MICROMETALS T184-40 having N_1=72 turns of litz wire 20x 0.355CuL. The ohmic resistance of the winding amounts to R_L=60mΩ @ 75°C. In connection with an initial inductance value of L = 700μH (for low current and/or low magnitude of the magnetization of the inductor core) there results a lower frequency limit of the inductive behavior of f_L= 13.6Hz.

In order to decouple the input inductors and the inner mains impedance at the switching frequency filter capacitors C_F =1μF are provided at the mains input.

5.1 Observer Dimensioning

Center Point Current Measurement

The dimensioning of the AC current sense transformer employed for measuring i_M has to consider a harmonic with three times the mains frequency being contained in i_M. This harmonic typically shows an amplitude of 10% of the amplitude of the input current fundamental [15] (in the case at hand ≈2A). Furthermore, a transient DC component $i_{M,avg}$ = 1...2A as occurring for a correction of an unbalance of the partial output voltages u_{C+} and u_{C-} [10] has to be taken into account. For details of the dimensioning of a current sense transformer we would like to refer here to [16] for the sake of brevity.

In the case at hand the current transformer is realized in through-hole technique by using a toroidal ferrite core SIEMENS R23/9 with a single primary turn and a current transfer ratio of 100:1. By using a power PCB for wiring the power components of the rectifier system and by doing a careful layout minimizing parasitic wiring inductances the insertion of the current transformer in the connection to the output voltage center point results in an only insignificant increase of the switching overvoltages of the power transistors. The current transformer output voltage is set to a relatively low level of 100mV@10A primary current. The following amplification is performed in two stages (amplifiers Q_5 and Q_6) in order to achieve a high bandwidth. Therefore, the amplifiers can be employed in equal form also in case a shunt resistor (10mΩ and/or 100mV@10A corresponding to a power loss of 1W) is used for current sensing in place of the current transformer.

5.2 Measurement of the Input Inductor Voltage

The measurement of the inductive component of an inductor voltage (i.e. of the component of the input inductor voltage which is proportional to the rate of change of the current) is performed by an auxiliary winding with two turns, N_2=2. According to the number of turns of the main winding of N_1 = 72 this results in a voltage transformation ratio of 36:1.

Remark: For the measurement of the inductor voltage as well as for the center point current measurement common-mode inductors are provided in the measuring lines. For high-frequency common-mode currents these inductors represent a high impedance and therefore prevent capacitive earth leakage currents (occurring due to the common-mode voltage with switching frequency of the connection to the output voltage center point and of the main windings of the input inductors) from flowing via the signal electronics. Furthermore, with respect to the relatively low level of the current measuring signal an electrostatic shield (copper foil) is introduced between the transformer core and the center point conductor and connected to the artificial mains star point N' (cf. Fig.1) which is formed by the star connection of the AC side filter capacitors C_F.

Integrators and Controllers H(s) and K(s)

The dimensioning of the components R_I and C_I of the integrators has to be under consideration of the offset voltage and the offset current and the maximum output current of the operational amplifiers employed [17].

The current dependency of the inductance $L = L\{i_U\}$ of the iron powder core input inductors (typically the inductance in the vicinity of the maxima of an input current differs by a factor of 2 from the initial inductance value given at the current zero crossings) cannot be considered in a simple form for the integration of the inductor voltages

$$u_{L,i,m} = \frac{N_2}{N_1}\left[L\{i_{U,i}\}\frac{\mathrm{d}\,i_{U,i}}{\mathrm{d}t} + i_U\frac{\mathrm{d}\,L\{i_{U,i}\}}{\mathrm{d}\,i_{U,i}}\cdot\frac{\mathrm{d}\,i_{U,i}}{\mathrm{d}t}\right]. \qquad (9)$$

Accordingly, the dimensioning of the integrators Q_1, Q_2 and Q_3 is based on an average inductance value.

Aiming for a low realization effort the correction controllers $H(s)$ and/or Q_8, Q_9 and Q_{10} are realized by simple proportional amplifiers. The amplification is selected such that the time constant of the first-order system behavior resulting for closed control loop in connection with the respective integrator is in the range of τ_H = 0.25...0.5 T_P. Because the feedback loop is closed always only in sections of the pulse periods then the actual time constant will be τ'_H = 2...5 T_P. Accordingly, the reconstructed phase currents $\hat{\imath}_{U,i}$ will show a correct fundamental amplitude independent of inaccuracies of the system model. The remaining deviation of the time behavior of the ripple components of the currents $\hat{\imath}_{U,i}$ from the actual shape of the input current ripple is of no significance for a ramp comparison control of the input phase currents.

Independent of the non-linear behavior of the input inductors $\Sigma\hat{\imath}_{U,i}$ has to be fulfilled by the reconstructed phase current values. If with respect to the continuous action of $K(s)$ the gain of Q_{11} is set to be a factor of 10 below the gain of $H(s)$ (and/or of the amplifiers Q_8, Q_9 and Q_{10}) both correction feedback loops show approximately equal dynamic and a high quality of the phase current reconstruction is achieved despite the interruption of the action of $H(s)$ in ≈ $\pi/6$-wide intervals of a mains period (cf. Figs.9 and 11(a)).

It is important to note that the correction of the integrator outputs is not connected to an operation of the rectifier power circuit, but is in a continuous manner also in intervals with zero output power and/or in case of intermittent operation (as occurring for low output power levels). In this case the switching functions resulting from the intersection of the pre-control

functions m_i and the carrier signal i_D are not applied to the gate drive circuits of the power transistors S_i but are applied to the input of Q_4. In connection with $i_{M,m} = 0$, as given for missing center point current (no load condition) therefore also $\hat{\imath}_{U,i} = 0$ is guaranteed by the correction controllers $H(s)$ and $K(s)$, and/or an influence of the offset quantities of the operational amplifiers Q_1, Q_2, Q_3 on the current reconstruction is suppressed.

5.3 Measuring Results

Figure 6 verifies the theoretical considerations given in section 2.2; for (s_R, s_S, s_T) = (110) the center point current i_M and the phase current $-i_T$ show identical time behavior.

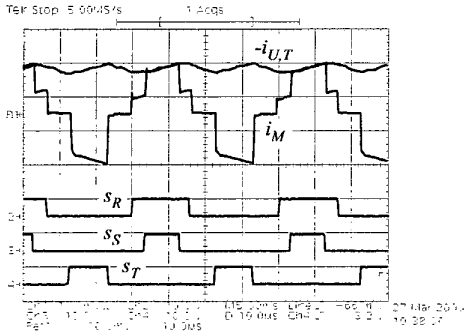

Fig.6: Center point current i_M, input phase current $-i_{U,T}$ and phase switching functions s_i; scales: 5A/div, 10V/div, 10µs/div.

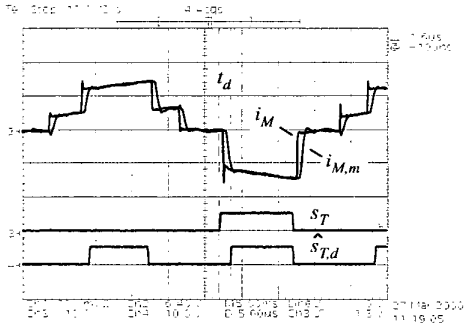

Fig.7: Actual shape of the center point current i_M and measurement signal $i_{M,m}$ (cf. Fig.5), control signal s_T of the power transistor in phase T and control signal $\hat{s}_{T,d}$ of the analog switch S_T closing the associated observer correction control loop; scales: 5A/div, 10V/div, 5µs/div.

As **Fig.7** shows the change of i_M is delayed with reference to the rising edge of s_T due to the time delay of the gate drive circuit and the switching time of the power transistor S_T The rate of rise of $i_{M,m}$ is relatively low due to the limited bandwidth of the amplifiers Q_5 and Q_6 as caused by the high gain of a=10. The transition period is suppressed for the observer correction by activating the correction control loop with a time delay (R_D, C_D in Fig.5); contrary, the interruption of the correction at the falling edge of s_T is without delay.

A change of the switching state of the rectifier results in a step change of the line-to-line input voltages and of the common-mode component u_0 of the rectifier input phase voltages (and/or of the output voltage center point with

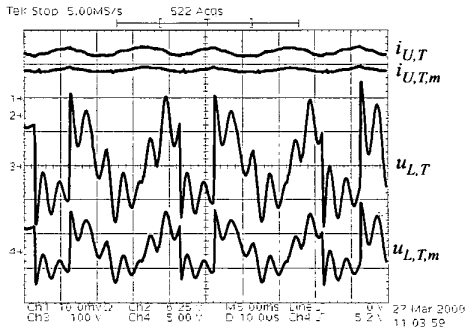

Fig.8: Actual shape of the voltage $u_{L,T}$ (300V/div) across the inductor in phase T and output voltage $u_{L,T,m}$ of the inductor auxiliary secondary winding (5V/div). Furthermore shown: time behavior of $i_{U,T}$ (5A/div) and of the corresponding reconstructed phase current $\hat{\imath}_{U,T}$; for facilitating a direct comparison of the signals $\hat{\imath}_{U,T}$ is adjusted in amplitude to $i_{U,T}$ by selection of a proper scale; time scale: 10µs/div.

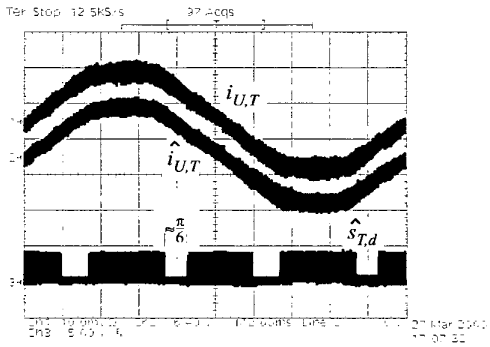

Fig.9: Time behavior of the actual and of the reconstructed phase current, $i_{U,T}$ (5A/div) and $\hat{\imath}_{U,T}$, within a mains period. Furthermore shown: control signal $\hat{s}_{T,d}$ (5V/div) of analog switch S_T activating the observer correction control loop in Phase T.

reference to earth). This stimulates a resonant circuit formed by parasitic earth capacitances $C_E \approx$ 500pF...1nF of the load circuit and of the power semiconductors and by the input inductors L and/or results in a synchronous oscillation of the voltages across the input inductors L as depicted in **Fig.8** for Phase T. The corresponding common-mode currents remain limited to relatively low values due to the high characteristic impedance of the resonant circuit and therefore cannot be identified in the shape of the phase currents.

According to **Fig.9** within a mains period the correction of a phase current observer is interrupted only in intervals of a width of $\approx\pi/6$ (for high modulation index) lying symmetrical to the maxima of the corresponding phase current. Within these intervals the correction of the phase current observer is in an indirect manner via Q_6 and/or $K(s)$ and the phase current observers of the other two phases operating with activated correction control (cf. **Fig.10**(b)). This ensures a high quality of the current reconstruction throughout the whole mains period.

We would like to point out that the very good coincidence of the actual and of the reconstructed current shape is maintained also in the vicinity of the phase current zero crossings (cf. Fig.10(c)) which could be considered being critical due to the dependency of the formation of the rectifier input phase voltage $u_{U,i}$ on the sign of the respective phase current (cf. Eq.(1)).

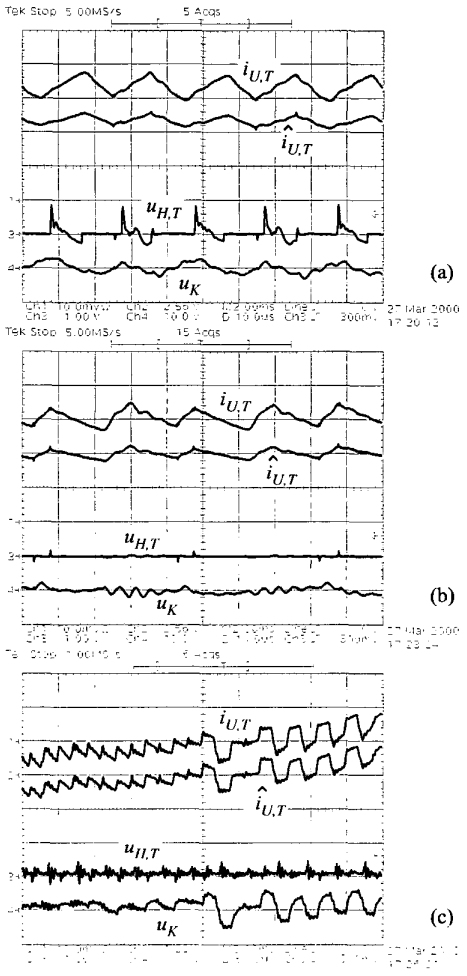

Fig.10: Output signal $u_{H,T}$ of the P-type controller Q_{10} ($H(s)$ in Fig.1) correcting the output of integrator Q_3 and output signal u_K of the P-type controller Q_{11} ($K(s)$ in Fig.1) ensuring $\Sigma\hat{\imath}_{U,i} = 0$. Furthermore shown are the time behavior of the actual and the reconstructed input current of phase T within a section of the mains period **(a)** for active (direct) observer output correction via $H(s)$, i.e. closed loop operation of the phase current observer Q_3 (2A/div, 10μs/div), **(b)** for only indirect correction of the integration of $u_{L,T}$ via $K(s)$ and/or $\hat{s}_T$ remaining at 0 (2A/div, 10μs/div), and **(c)** in the vicinity of the zero crossing of $i_{U,T}$ (1A/div, 50μs/div); The scaling of $u_{H,T}$ (1V/div) and u_K (10V/div) considers the different gains of the controllers $H(s)$ and $K(s)$; therefore, equal magnitudes of the signals shown result in an equal influence on the output of the integrator Q_3.

Figure 11 clearly verifies the insensitivity of the phase current reconstruction to inaccuracies of the system model. There, the time behavior of the actual phase current $i_{U,T}$ (5A/div) is compared to the time behavior of the reconstructed phase current $i_{U,i}$ for an increase of the time constant $R_I C_I$ of the integration of the voltages $u_{L,i,m}$ by a factor of 2 (according to a change of the inductance value considered by the system model from L to $2L$, cf. **(a)** and **(b)**) for closed loop zero sequence current correction and for $K(s)$ =0. As already discussed in connection with Fig.9 within each pulse half period in any case two phase current observers are operating with direct correction via

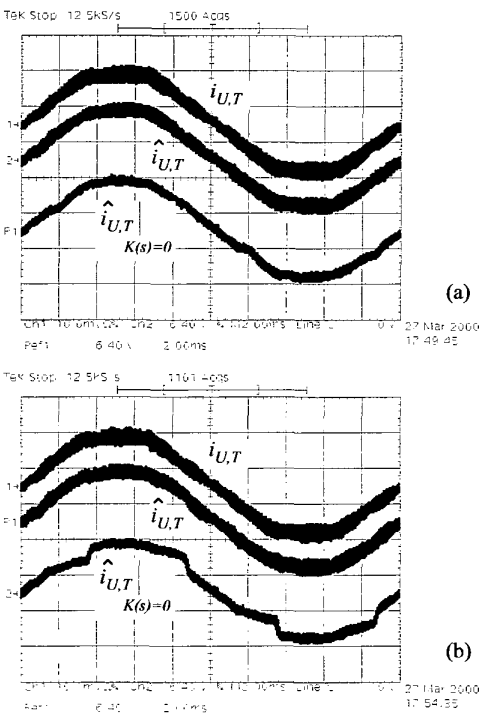

Fig.11: Sensitivity of the phase current reconstruction concerning inaccuracies of the inductance value on which the integration of the voltages $u_{L,i,m}$ is based. **(a)**: zero sequence current correction activated, **(b)**: no zero sequence current correction, i.e. $K(s) = 0$.

$H(s)$. Accordingly, also the output of the observer of the third phase shows a low estimation error due to the indirect correction via the zero sequence current controller $K(s)$. In case the zero sequence component correction is disabled, i.e. $K(s) = 0$, the reconstruction of a phase current is in sections where the correction via $H(s)$ is interrupted (cf., e.g., sections with $\hat{s}_{T,d} = 0$ in Fig.9) independent of the other phases. This results in a relatively high deviation of the reconstructed phase current $i_{U,i|K(s)=0}$ from the actual current shape $i_{U,i}$ in case the inductance considered by the system model (integrator) is different from the actual inductance value.

6 Conclusions

In this paper a simple concept for observer-based reconstruction of the continuous shape of the input phase currents of a VIENNA Rectifier is proposed. For current measurement there only a single AC current sensor in the connection to the output voltage center point is employed and the realization costs (on a single component price basis) for deriving the phase current information are reduced by about a factor of 4 as compared to employing compensated Hall-effect current transducers in two input lines. Additionally, problems resulting from an offset of the measured current signals or a different gain or drift of two current transducers are avoided inherently. Furthermore the concept is insensitive to a non-linear behavior of the input inductors and therefore can be used advantageous for realizing a highly dynamic ramp comparison phase current control also for application of input inductors with iron powder cores.

In case the reference potential (ground) of the signal electronics is connected to the center point M of the rectifier output voltage the AC current sensor can be replaced by a shunt what results in an additional reduction of the realization costs. According to the lower rms value of i_M as compared to

the rms value of the phase current (typ. $I_{M,rms} \approx 0.25...0.5\ I_{N,rms}$) there also the losses occurring for equal magnitude of the sensor output signal are reduced. However, there is a potential risk of a disturbance of the signal and control electronics by capacitive leakage currents to earth occurring due to the common mode voltage of M with switching frequency (cf. Fig.5(b) in [18]).

Aiming for a further reduction of the realization effort of the control of the VIENNA Rectifier I the continuation of the research will be on a simplified concept of the ramp comparison current control (cf. Fig.4(b), [19]) which can be realized without analog multipliers for phase current reference value generation and does not require input voltage information. The approach is known from single-phase power factor correction [20] and has been treated in different form for three-phase rectifier systems in [21].

Furthermore, the application of a modified version of the center point current measurement [22] featuring a detection of an earth-fault of the rectifier output voltage (similar to the concept for earth fault detection known for two-level inverter systems in connection with DC link current based phase current reconstruction [5], [23]) shall be investigated.

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