Self-Adjusting Input Current Ripple Cancellation of Coupled Parallel Connected Hysteresis-Controlled Boost Power Factor Correctors

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Abstract - As this paper shows, the magnetic coupling of the inductances of two hysteresis-controlled single-phase AC-to-DC boost converters connected in parallel leads in connection with a delayed switching of the power transistors to a self-adjusting staggered switching of the the partial systems. Thereby, a significant reduction of the ripple of the resulting mains current as compared to the uncoupled case is obtained. Based on the analytic description of the current shapes within a pulse period the dependency on the circuit parameters of the occurring phase displacement of the switching functions of the partial systems is calculated. Furthermore, the effect of an unsymmetry of the converters on the system behavior is analyzed and the automatic adjustment of the phase shift within a mains period is investigated by digital simulation. The theoretical considerations are verified by measurements on a laboratory model. Finally, the possibility of a substitution of the magnetic coupling of the input inductances of the partial systems by a coupling of the current controls of the converters is discussed.

1 Introduction

As described in [1], [2], [3], [4], the realization of a single-phase AC-to-DC boost converter with high power can be achieved advantageously by a parallel connection of phase-shifted partial systems. This is especially true where high power density and high efficiency is required. If a number of n sequentially controlled parallel systems (with a phase shift of $\frac{2\pi}{n}$ for each partial system) is used,

- the maximum amplitude of the ripple of the entire system input current is reduced by a factor of n^2 and
- the fundamental frequency of the ripple current is increased from f to nf (without increasing the switching losses).

These results are made in comparison to $n = 1$ (or to phase-synchronous switching) and for overall energy storage capability (and/or for an entire volume of the input inductances) being independent of n in a first approximation. Therefore, for equal maximum value of the input current ripple amplitude one can reduce the switching frequency and, therefore, one can increase the efficiency of the converter. Or, for equal switching frequency one can reduce the inductivity value of the input inductances and the filtering effort for avoidance of EMI of other electric power users. Thereby, for equal efficiency an increase of the power density of the converter can be obtained (cf. section II-E in [2]).

When the number of parallel operating partial systems is determined, one has to make compromises between a possible increase of the power density and/or the efficiency and the thereby increased system complexity (and the connected increase of manufacturing cost and reduction of reliability). Also, one has to keep in mind that the matching requirements between the inductors are increased with n, as well as the phase accuracy of the control signals of the partial systems (cf. p. 3-137 in [1] or p. D1-9 in [5]).

As shown in [1] (cf. p. 3-138) based on the optimization of a system with 3 kW output power (input voltage: $230\,V_{rms} + 15\%/-20\%$) where the dimensioning of the input filter is included and as is proven in [4] (cf. section I), the paralleling of two partial systems results in a technical/economical optimum for high output power. Thereby, for high utilization of the power handling capability of the power semiconductor devices the partial systems are operated in the continuous-conduction mode [4].

The control of the input current has to be realized by a control method with constant switching frequency (peak current mode control or average current mode control, [6], [7]) as required by the operating principle. Due to the higher control accuracy (especially in the vicinity of the mains voltage zero crossings) and to the reduced susceptibility to EMI (cf. p. 65 in [8] or p. 9-457 in [9]), one has to prefer the control of the local current mean value (average current mode control) as compared to controlling the local current peak value (peak current mode control). Thereby, the control error (being dynamically weighted and locally averaged by the current control amplifier) is

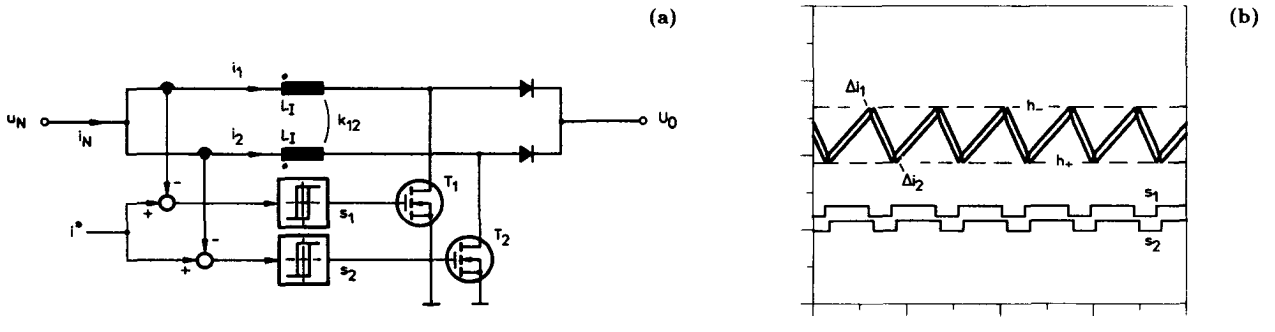

Fig.1: Analysis of the operating behavior of a parallel connection of hysteresis-controlled DC-to-DC boost converters for magnetic coupling of the input inductances of the partial systems. **(a):** basic system structure; **(b):** shape of the ripples Δi_1 and Δi_2 of the input currents i_1 and i_2 and of the switching functions s_1 and s_2 (control signals of the power transistors T_1 and T_2) of the partial systems for positive coupling k_{12}. h_+: positive switching threshold of the hysteresis controllers, h_-: negative threshold; simulation parameters: $u_N = 130\,V$, $L_I = 1.33\,mH$, $k_{12} = 0.25$, hysteresis band width $h = 4\,A$, $U_O = 380\,V$, switching delay times of the active components are neglected. Time scale: 100 ns/div. Independent of the sign of the coupling factor k_{12} (sense of winding of the partial inductances) no change of the initially existing phase shift of the switching functions in direction of an opposite-phase operation of the converters results.

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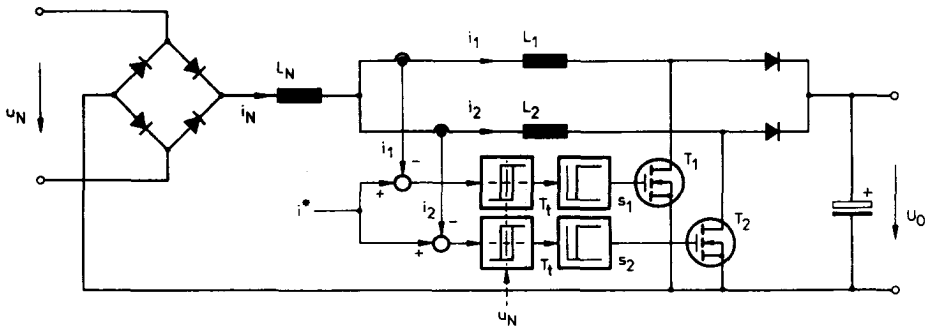

Fig.2: Basic structure of the power and control circuits of a single-phase AC-to-DC boost power factor corrector according to Fig.1 where the circuit part on the DC side is realized as a parallel connection of coupled current controlled partial systems and the switching of the power transistors is delayed by T_t. The (positive) magnetic coupling (as marked in Fig.1(a)) of the input inductances of the boost converters is illustrated by a T-equivalent circuit. There, the relations $L_N = k_{12}L_I$ and $L_1 = L_2 = (1 - k_{12})L_I$ are valid. The control signals s_1 and s_2 of the power transistors T_1 and T_2 are delayed by T_t as compared to the control signals of the hysteresis switching elements of the current controls. The dead time T_t includes the in reality always existing delay time of the control stages ond of the power transistors. It can be given in a defined manner for practical system realization by insertion of time elements into the current control loops.

transformed by comparator stages into phase-shifted pulse width modulated control signals of the power transistors of the partial systems. As becomes clear, e.g., for pre-control of the current controller output by the instantaneous value of the mains voltage, basically a control method with impressed voltage (and not with impressed current) is given here; for insuring a symmetrical current consumption of the partial systems one has to add a special control loop, therefore (cf. section VI in [4]).

A direct control and symmetrization of the partial currents could be achieved by using a control method impressing the currents. Based on this consideration, the basic question arises in connection with the already mentioned disadvantages of the peak current mode control if one can obtain a synchronization or a locking of the partial systems into an operation with opposite phase (or, at least, an operation which reduces the ripple of the total input current as compared to the algebraic sum of the ripple contributions of the partial systems) also if a control method is applied which is not linked to a constant pulse frequency, e.g., variable hysteresis control [10], [11], [12].

Methods for a staggered switching of parallel, hysteresis current controlled converters are described in the literature in connection with the reduction of the effects on the mains of input PWM rectifiers (single-phase four-quadrant choppers [14]) of high-power traction equipment. There, basically one tries to achieve a synchronization of the pulse frequencies (which vary time-dependently and in dependency on the load condition of the power circuit) and a phase shift of the switching status changes of the partial systems by (1) coupling of the current controls or, by (2) coupling of the power circuits.

The control-oriented coupling (as proposed in [15] and [16]) of several partial systems (hierarchically organized hysteresis control) involves a relatively high complexity and a relatively high realization effort of the control system. Therefore, it shall not be treated in more detail here. A specific coupling of the power circuits of parallel working systems is described in [17]. Via appropriate choice of the leakage inductances of the input main transformer of an electric locomotive feeding two four-quadrant choppers from separate secondary windings one obtains a significant reduction of the harmonic content of the transformer primary current drawn from the overhead line. Based on this, it is obvious in the case at hand to investigate the influence of a magnetic coupling of the input inductances of the AC-to-DC boost converters on the shape and harmonic content of the total input current. There, the mains voltage and the hysteresis width can be assumed constant over several switching cycles. This is due to the fact that the system pulse frequency lies substantially above the mains frequency. This in turn is required for a practical realization of the system in order to minimize the filtering effort. Therefore, one can investigate the basic system behavior using the example of two hysteresis controlled magnetically coupled DC-to-DC boost converter stages connected in parallel (cf. **Fig.1**(a)).

A digital simulation based on the assumption of ideal components leads to the current ripple shape shown in Fig.1(b). One can notice a coupling of the partial systems. However, the phase shift of the ripple currents Δi_1 and Δi_2 is not influenced thereby; especially no staggered switching of the partial systems is obtained. If, for investigating the real system behavior a switching delay time of the power transistors is introduced into the simulation (cf. **Fig.2**), one would expect only a small basic change of the operating behavior (e.g., a minor increase of the ripple amplitude). Surprisingly, however, there results a high amplification of the mutual influence of the partial systems acting in the direction of a shift of the ripple currents (or, of the switching functions characterizing the switching states of the power transistors) by one half switching period (cf. **Fig.3**). Therefore, in a first approximation there exist relations

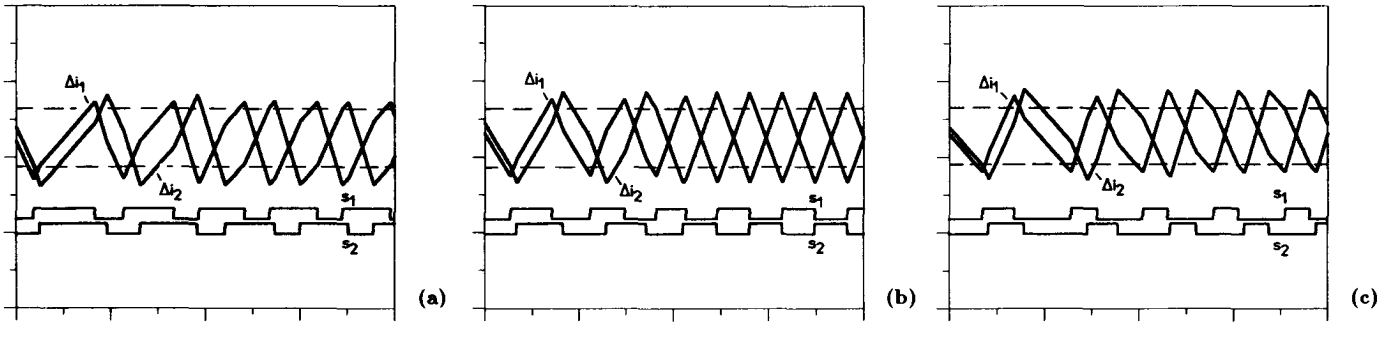

Fig.3: Operating behavior of the circuit according to Fig.2 for constant input voltage u_N and for different values of the voltage transfer ration $m = \frac{u_N}{U_0}$. Representation of the current ripples Δi_1 and Δi_2 of the input currents and of the switching functions of the partial systems. Simulation parameters: **(a):** $u_N = 130\,\mathrm{V}$ or $m = 0.34$; **(b):** $u_N = 190\,V$ or $m = 0.5$; **(c):** $u_N = 250\,\mathrm{V}$ or $m = 0.66$. Simulation parameters according to Fig.1(a): $L_N = 0.33\,\mathrm{mH}$, $L = 1\,\mathrm{mH}$ and $T_t = 6.5\,\mu\mathrm{s}$, however. Time scale: 100 ns/div. Independent of the specific value of the voltage transfer ratio one obtains (in the stationary case) an operation of the partial systems in approximately opposite phase (or a phase shift of the switching functions of approximately half a pulse period). Ideal phase opposition is given for $m = 0.5$ (cf. **(b)**).

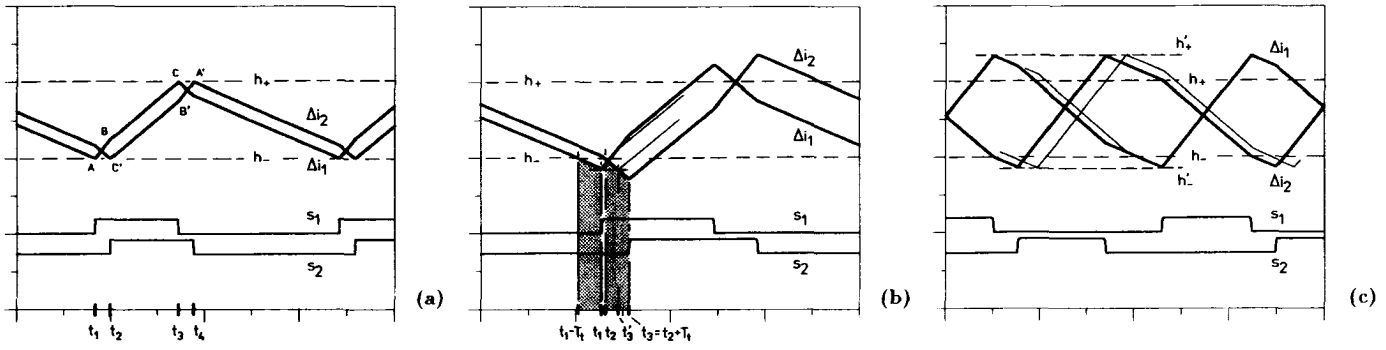

Fig.4: Shape of the current ripples Δi_1 and Δi_2 and of the switching functions s_1 and s_2 of the circuit according to Fig.2 for $T_t = 0$ (cf. **(a)**) and $T_t = 6.5\,\mu s$ (cf. **(b)** and **(c)**); the remaining simulation parameters are equal as for Fig.1(b) or Fig.3(c); time scale: $27.5\,\mu s$/div.

for the stationary case which correspond to a control method with impressed voltage and/or a forced-staggered switching. This fact motivates a further investigation of the system shown in Fig.2.

In this paper a detailed analysis of the operating behavior of a parallel connection of two variable hysteresis current controlled single-phase AC-to-DC boost converters with coupled input inductances and delayed switching of the power transistors is given. In **section 2** the self-adaptive locking of the partial systems into an operation with approximately opposite phase of the switching functions is analyzed based on the assumption of a time-constant input voltage and hysteresis width. The characteristic current shapes are described analytically. The dependency (as a function of time) of the change of the phase displacement of the switching functions occurring during the locking process is calculated for a switching sequence in dependency on switching delay time, degree of coupling and voltage transformation ratio. Based on these basic considerations, in **section 3** the global operating behavior of the power factor corrector within a mains voltage half cycle is investigated by digital simulation. In **section 4** the theoretical considerations are verified by measurements on a laboratory circuit. Finally, in **section 5** a coupling of the current controls of the partial systems replacing the coupling of the input inductances is discussed. With this one can obtain a self-adjusting staggered switching of two converters without explicite coupling of the power circuits. This gives a broad applicability of the proposed concept.

2 Theory of Operation

In the following in section 2.1 we try to give a clear explanation of the locking of the partial systems of the circuit shown in Fig.2 into an operation with opposite phase. The resuls of the detailed mathematical description of the system behavior are compiled in section 2.2. The influence of the system parameters on the lock-in process is discussed in section 2.3.

2.1 Basic Function

Figure 4(a) shows a segment of the signal shapes as shown in Fig.1(a). As already described in section 1, due to $T_t = 0$ no influence of the coupling of the partial systems on the phase shift of the switching functions s_1 and s_2 is given. The phase shift occurring in $t = 0$ is maintained. The delay $t_2 - t_1$ of the positive edge of s_2 with respect to the positive edge of s_1 shall be denoted in the following by $\tau_{n,0\to1}$, the delay of the negative edges by $\tau_{n,1\to0}$. As becomes immediately clear by inspection of the equivalent circuit of the coupled inductor arrangement (cf. L_N and L_1 and L_2 in Fig.2), the rate of change of *both* systems is influenced by each switching state change via the inductive voltage drop across L_N. We have:

s_1	s_2	$\frac{di_1}{dt}$	$\frac{di_2}{dt}$
0	0	$-k_-$	$-k_-$
0	1	$-k_{--}$	k_{++}
1	0	k_{++}	$-k_{--}$
1	1	k_+	k_+

Tab.1: Rate of change of the partial currents i_1 and i_2 in dependency on switching state combinations of the partial systems.

with

$$k_+ = \frac{u_N}{2L_N + L} \qquad k_{++} = \frac{u_N + U_O \frac{L_N}{L}}{2L_N + L}$$
$$k_- = \frac{(U_O - u_N)}{2L_N + L} \qquad k_{--} = \frac{(U_O - u_N) + U_O \frac{L_N}{L}}{2L_N + L} \,. \tag{1}$$

Because, according to **Tab.1** there exist identical current rates of change for the switching state combinations $(s_1, s_2) = (10)$ and (01), the shape of Δi_1 related to the negative switching threshold h_- and the shape of Δi_2 related to the positive threshold h_+ show the symmetry conditions indicated in Fig.4(a) (cf. A, B, C and A', B', C'). Therefore, a phase shift measured at h_- of $\tau_{n,0\to1}$ is reproduced according to $\tau_{n,1\to0} = \tau_{n+1,n,0\to1}$ at h_+. For ideal symmetry of the partial systems there remains an initial phase shift or, also, each change of this phase shift of the ripple currents caused by a disturbance as a stable condition. Therefore, the switching functions can be shifted with respect to each other freely by disturbances (or by unsymmetries of the partial systems).

A negative coupling $k_{12} < 0$ of the partial systems (reversal of the sense of winding of L_1 or L_2) results in no basic change of the operating behavior. Therefore, a more detailed discussion is omitted here. *Remark:* We want to point out in connection with $k_{12} < 0$ that a negative coupling for a practical realization could not be modelled by a T-equivalent circuit which neglects the potential separation of the partial windings. $k_{12} < 0$ is basically only possible for magnetic coupling of L_1 and L_2.

For a time delay T_t of the output signals of the hysteresis switching elements (cf. Fig.2) there results (as a comparison of Fig.4(a) and of a segment of Fig.3(a), Fig4(b), clearly shows) a basic change of the operating behavior of the circuit. By turning on T_1 in t_1 (having a delay of T_t as compared to intersecting h_-) the current rate of change of the partial current in L_2 is increased from $-k_-$ to $-k_{--}$ (cf. Tab.1). The intersection of h_- in t_2 (due to the time delay T_t of the output signals of the hysteresis switching elements Δi_1 and Δi_2 are not held within the tolerance band $h = h_+ - h_-$) occurs with a larger rate of change therefore. At the end of the delay interval T_t a current value of $\Delta i_{2,t=t_3} < i_{1,t=t_1}$ is obtained thereby. Accordingly, the phase difference of Δi_1 and Δi_2 is increased. For maintaining the phase relation existing before t_1, in analogy to Fig.4(a) a switching over would have to occur already in t_3'. There, a shape of Δi_1 and Δi_2 as shown in Fig.4(b) would result.

The phase difference is now further increased for each intersection of a switching threshold until the dead time intervals to be considered after falling below h_- will lie completely at the switching state $s_1 = 0$, $s_2 = 0$. The same is true for intervals T_t corresponding to h_+ if they will lie completely at switching states $s_1 = 1$, $s_2 = 0$ or $s_1 = 0$ and $s_2 = 1$. According to Tab.1, the partial currents then show the same rate of change when a switching threshold is crossed; this means that a stationary operation of the system is obtained. As shown in Fig.4(c), the effect of the dead time corresponds to an apparent increase of the hysteresis band width in the stationary case (switching thresholds h_+' and h_-' in connection with $T_t' = 0$).

Therefore, after an initial steady increase of the phase difference of s_1 and s_2 the segments $s_2 = 1$ of the pulse pattern s_2 are locked in the intervals $s_1 = 0$ of the pulse pattern s_1 (or the intervals $s_1 = 1$ of the pulse pattern s_1 are locked in the intervals $s_2 = 0$ of the pulse pattern s_2) after several switching cycles. (*Remark:* If the pulse $s_{2,n} = 1$ would move to the end of $s_{1,n} = 0$, s_1 would have to be regarded as lagging phase; based on the previous considerations also in this case a synchronizing reaction of the system is given which moves $s_2 = 1$ back into the region $s_1 = 0$). As also Fig.3(c) shows, it is

inherent to the system that a synchronization and an approximate opposite-phase operation of the partial systems results. Therefore, the system behavior corresponds to that of a phase-locked loop which synchronizes the switching functions in approximately opposite phase.

Remark: For negative values of the coupling factor, an initially existing phase difference of s_1 and s_2 is reduced to 0 within a few switching cycles. (This can be shown easily by digital simulation.) In this case, the stationary condition is represented by switching functions being in phase. Therefore, for the total input current no compensation of the harmonic contributions of the input currents of the partial systems is given. A more detailed analysis of this effect (which could be of advantage under certain circumstances with respect to other conditions) shall be omitted for the sake of brevity.

The considerations made so far have been related to voltage transfer ratios $m > 0.5$,

$$m = \frac{u_N}{U_O} , \tag{2}$$

or to relative on-times of the power transistors of $\alpha_T < 0.5$,

$$\alpha_T = 1 - m , \tag{3}$$

(assuming system operation in the continuous-conduction mode). If an input voltage $m < 0.5$ and/or $\alpha_T > 0.5$ exists, there results no basic change of the system operating behavior as compared to $m > 0.5$. However, the stationary condition is then characterized by the absence of the switching state combination $s_1 = 0, s_2 = 0$; the blocking intervals $s_1 = 0$ and $s_2 = 0$ are locked in the conduction intervals $s_2 = 1$ and $s_1 = 1$) of the partial systems. In connection with the previous considerations for $m > 0.5$ then also the ideally opposite-phase switching occuring for $m = 0.5$ (cf. Fig.3(b)) can be explained clearly.

In the following section we want to give a mathematical description of the behavior during the locking process. The aim is to clarify the dependency of the increase of the phase shift occuring within a switching cycle on the operating parameters and to obtain a conclusion concerning the phase relation between s_1 and s_2 actually being present in the stationary operation.

2.2 Mathematical Analysis

2.2.1 Assumptions

For the mathematical analysis we want to assume:

- operation of the partial systems in continuous-conduction mode
- ideal symmetry of the partial systems (equal switching delay times, neglection of component tolerances, etc.)
- positive coupling $k_{12} > 0$ of the input inductors of the partial systems
- constant value within a switching cycle of the input voltage u_N, the output voltage U_O and the hysteresis band width h and
- minimum on- or off-times of $2T_t$ of the power transistors (or a corresponding value of the hysteresis band width).

By the assumption of minimum on- or off-times it is possible to reduce the number of cases to be distinguished for the calculation of the lock-in process concerning the initial shift τ_n of s_1 and s_2. The operating behavior not being included hereby for $u_N \approx 0$ and $u_N \approx U_O$ is of negligible importance. This is the case because for practical realization one has to provide always a minimum value of the difference $U_O - u_N$ for sufficient system dynamics. Furthermore, the partial currents for AC voltage supply of the system for $u_N \approx 0$ (in the vicinity of the zero-crossings of the mains voltage) cannot be held by the control within the hysteresis bands (cf. Fig.8 or e.g., Figs.2(b) and 2(c) in [18] or Fig.5 in [11]). Therefore, the lock-in to the opposite-phase operation can only occur for higher voltage values.

The relations are being described at first for $m > 0.5$. As given in section 2.2.3 one can derive from this the system behavior for $m < 0.5$ by symmetry considerations.

The coupling of the partial systems is characterized in the following by

$$k_L = \frac{L_N}{L} ; \tag{4}$$

as compared to the degree of coupling k_{12} of the input inductances L_I of the partial systems there exists the relation

$$k_{12} = \frac{k_L}{1 + k_L} . \tag{5}$$

2.2.2 Analysis for $0.5\ U_O < u_N < U_O$

In dependency on the relative time-position of the switching functions s_1 and s_2 during the lock-in process (or on the overlapping of the delay intervals occurring there) one has to distinguish six regions $\tau_{n,min} \leq \tau_n \leq \tau_{n,max}$ (cf. **Fig.5**). τ_n denotes the phase shift of the switching state change $s_{2,n} = 0 \rightarrow 1$ related to $s_{1,n} = 0 \rightarrow 1$ at the beginning of a switching cycle (cf. Fig.5(d)). For the increase of the phase shift within a switching cycle we set

$$\Delta\tau_{n+1,n} = \tau_{n+1} - \tau_n . \tag{6}$$

In the following the results of the mathematical analysis are summarized briefly according to partial regions and to their sequence during the lock-in process.

Region A:

Definition region:

$$0 < \tau_{n,A} \leq \frac{m(1-m)}{m(1-m) + 2k_L(1+2k_L)} T_t . \tag{7}$$

The system behavior at the beginning of the locking process (for the region between switching functions s_1 and s_2 being in phase and a maximum phase shift *after* a switching cycle of $\tau_{n+1} = T_t$) is covered. Increase of the phase shift of s_1 and s_2 per switching cycle:

$$\Delta\tau_{n+1,n,A} = \frac{2k_L(1+2k_L)}{m(1-m)} \tau_{n,A} . \tag{8}$$

Maximum increase of the phase shift (at the upper region boundary):

$$\Delta\tau_{n+1,n,A,\max} = \frac{2k_L(1+2k_L)}{m(1-m) + 2k_L(1+2k_L)} T_t . \tag{9}$$

Region B:

Definition region:

$$\frac{m(1-m)}{m(1-m) + 2k_L(1+2k_L)} T_t \leq \tau_{n,B} \leq \frac{m}{m + 2k_L} T_t . \tag{10}$$

At the upper region boundary the phase difference of the negative switching edges $s_{2,n} = 1 \rightarrow 0$ and $s_{1,n} = 1 \rightarrow 0$ becomes equal to T_t. Increase of the phase shift of s_1 and s_2 per switching cycle:

$$\Delta\tau_{n+1,n,B} = \frac{k_L}{1 - m + k_L} T_t + \frac{2k_L(1+2k_L) - mk_L}{m(1-m+k_L)} \tau_{n,B} . \tag{11}$$

Maximum increase of the phase shift (at the upper region boundary):

$$\Delta\tau_{n+1,n,B,\max} = \frac{2k_L(1+3k_L)}{(1-m+k_L)(m+2k_L)} T_t . \tag{12}$$

See region A regarding the increase of the phase shift at the lower region boundary.

Region C:

Definition region:

$$\frac{m}{m + 2k_L} T_t \leq \tau_{n,C} \leq T_t . \tag{13}$$

There remains (as compared to A and B) only a partial overlapping of the time delays T_t corresponding to the switching state changes $s_{1,n} = 0 \rightarrow 1$ and $s_{2,n} = 0 \rightarrow 1$. Increase of the phase shift of s_1 and s_2 per switching cycle:

$$\Delta\tau_{n+1,n,C} = \frac{k_L(1+m+3k_L)}{(1-m+k_L)(m+k_L)} T_t + \frac{k_L}{1+k_L} \tau_{n,C} . \tag{14}$$

Maximum increase of the phase shift (at the upper region boundary):

$$\Delta\tau_{n+1,n,C,\max} = \frac{2k_L(1+2k_L)}{(1-m+k_L)(m+k_L)} T_t . \tag{15}$$

See region B regarding the increase of the phase shift at the lower region boundary.

Region D:

Definition region:

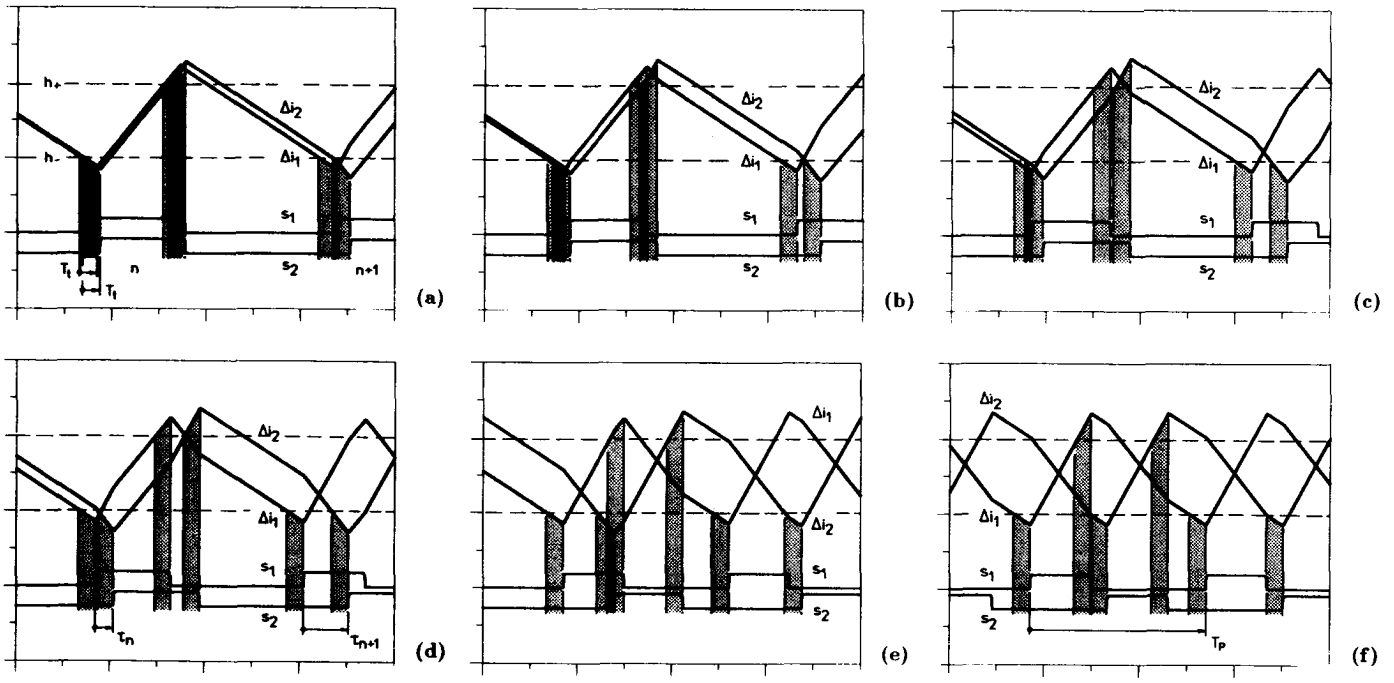

Fig.5: Representation of the shapes of the current ripples Δi_1 and Δi_2 and switching functions s_1 and s_2 as being characteristic for the cases A – F to be distinguished for the mathematical analysis of the locking process. The denomination of the figures corresponds to the related calculation region. E.g., **(a)** corresponds to region A, **(f)** corresponds to the region of stationary operation F.

$$T_t \;\le\; \tau_{n,D} \;\le\; \frac{1+2k_L}{m+k_L}\,\frac{Lh}{U_O} + \frac{1-m}{m+k_L}\,T_t \;. \tag{16}$$

Increase of the phase shift of s_1 and s_2 per switching cycle:

$$\Delta\tau_{n+1,n,D} = \frac{2k_L(1+2k_L)}{(1-m+k_L)(m+k_L)}\,T_t \;. \tag{17}$$

As Eq.(17) shows clearly (and as already qualitatively treated in section 2.1), the occurrence of a self-adjusting staggered switching is linked to a coupling k_L *and* a switching delay T_t. There, the effect of a delay time T_t on the increase of the phase shift per switching cycle $\Delta\tau_{n+1,n,D}$ is also determined by the ratio of the input and output voltages m.

Remark: As opposed to $\Delta\tau_{n+1,n,D}$, the values of $\Delta\tau_{n+1,n,(A,B,C)}$ show also a dependency on the initial shift $\tau_{n,(A,B,C)}$. This could lead to the assumption that in the regions A, B and C a phase-shifting effect could be given also without a switching delay time T_t. However, according to Eq.(7), Eq.(10) and Eq.(13) also the width of the regions A, B, and C approaches 0 for $T_t \to 0$. Therefore, the conclusion based on Eq.(17) (as given before) is valid in general.

Region E:

Definition region:

$$\frac{1+2k_L}{m+k_L}\,\frac{Lh}{U_O} + \frac{1-m}{m+k_L}\,T_t \;\le\; \tau_{n,E} \;\le\; \frac{1+2k_L}{m+k_L}\,\frac{Lh}{U_O} + \frac{1+m+2k_L}{m+k_L}\,T_t \;. \tag{18}$$

This region is defined by the occurrence of switching state changes $s_{2,n} = 0 \to 1$ within a region $\pm T_t$ around $s_{1,n} = 1 \to 0$. Increase of the phase shift of s_1 and s_2 per switching cycle:

$$\Delta\tau_{n+1,n,E} = \frac{k_L(1+2k_L)^2}{(1-m+k_L)(m+k_L)^2}\,\frac{Lh}{U_O} + \frac{k_L(1+2k_L)^2 + mk_L(1+2k_L)}{(1-m+k_L)(m+k_L)^2}\,T_t - \frac{k_L(1+2k_L)}{(1-m+k_L)(m+k_L)}\,\tau_{n,E} \;. \tag{19}$$

Increase of the phase shift at the upper region boundary:

$$\Delta\tau_{n+1,n,E} = 0 \;. \tag{20}$$

See region D regarding the increase of the phase shift at the lower region boundary.

According to Eq.(20) the phase shifting effect becomes 0 at the upper region boundary. This means that the limit of the locked or stationary condition (region F) is reached at the upper region boundary.

Region F:

Definition region:

$$t_{T,\mathrm{on}} + T_t \;\le\; \tau_{n,F} \;\le\; T_P - t_{T,\mathrm{on}} - T_t \tag{21}$$

or

$$\frac{1+2k_L}{m+k_L}\,\frac{Lh}{U_O} + \frac{1+m+2k_L}{m+k_L}\,T_t \;\le\; \tau_{n,F} \;\le\; \frac{m(1+2k_L)}{(1-m)(m+k_L)}\,\frac{Lh}{U_O} + \frac{m(m+2k_L)-k_L}{(1-m)(m+k_L)}\,T_t \;. \tag{22}$$

Increase of the phase shift of s_1 and s_2 per switching cycle:

$$\Delta\tau_{n+1,n,F} = 0 \;. \tag{23}$$

Within a switching cycle no change of the initially existing phase shift of s_1 and s_2 occurs. Within the region of τ_n defined by Eq.(21) a stationary system operation is given.

As can be seen by rewriting of Eq.(21), the switching state change $s_{2,n} = 0 \to 1$ is being held in a minimum distance from $s_{1,n} = 1 \to 0$ and the switching state change $s_{2,n} = 1 \to 0$ is being held in a minimum distance from $s_{1,n+1} = 0 \to 1$), where the minimum distance is defined by T_t. According to the explanations given in section 2.1, the stationary operation is characterized therefore by locking of the switching status regions $s_2 = 1$ in the regions $s_1 = 0$.

For the length of a switching period T_P there follows:

$$T_P = \frac{1+2k_L}{(1-m)(m+k_L)}\,\frac{Lh}{U_O} + \frac{1+k_L}{(1-m)(m+k_L)}\,T_t \;. \tag{24}$$

For the relative turn-on time (duty cycle of the transistors) there results, as can be expected from the operation of the system in continuous-conduction mode

$$\alpha_T = \frac{1}{T_P}\,t_{T,\mathrm{on}} = 1 - m \;. \tag{25}$$

2.2.3 Analysis for $0 < u_N < 0.5\ U_O$

As will be shown in the following, the system description for $m < 0.5$ can simply be derived from the analysis given in section 2.2.2 for $m > 0.5$.

Based on Eq.(1) there follows

$$k_+ = \frac{m}{1+2k_L}\frac{U_O}{L}\,, \qquad k_{++} = \frac{m+k_L}{1+2k_L}\frac{U_O}{L}\,,$$
$$k_- = \frac{1-m}{1+2k_L}\frac{U_O}{L}\,, \qquad k_{--} = \frac{1-m+k_L}{1+2k_L}\frac{U_O}{L}\,, \tag{26}$$

where definitions according to Eqs.(2) and Eq.(4) are considered. For a change of the voltage transfer ratio from m to $m' = 1-m$ a relation of the current rates of change

$$k'_+ = k_- \qquad k'_{++} = k_{--} \qquad k'_- = k_+ \qquad k'_{--} = k_{++} \tag{27}$$

is given accordingly. E.g., for voltage transfer ratio m and switching state $s_1 = 1$ and $s_2 = 0$ the same absolute values of the current rates of change of the partial currents as for $m' = 1-m$ and switching state $s'_1 = 0$ and $s'_2 = 1$ are valid; according to Eq.(27) we have for i_1: $k_{++} = k'_{--}$, for i_2: $k_{--} = k'_{++}$. Under consideration of the different signs of the actual current change we can therefore obtain the shape of $\Delta i'_1$ and $\Delta i'_2$ by using the mirror image of Δi_1 and Δi_2 with reference to the center of the hysteresis band. The corresponding switching functions s'_1 and s'_2 are to be obtained by inversion of the switching functions s_1 and s_2.

If we assume now that the analysis of the system behavior is related for m' to h_+ (and not to h_- as for m), the results derived thereby can be given directly by referring to the relations given in section 2.2.2 for $m > 0.5$. There, a replacement of the current rates of change according to

$$k_+ \rightarrow k'_- \qquad k_{++} \rightarrow k'_{--} \qquad k_- \rightarrow k'_+ \qquad k_{--} \rightarrow k'_{++} \tag{28}$$

has to be made. From this there follows the length of a pulse period of the region F' (corresponding to the region F for $m > 0.5$) via

$$T_{P,F} = \frac{k_{++}+2k_- - k_{--}}{k_{++}k_-}(h + T_i(k_{++}+k_-)) \tag{29}$$

(according to Eq.(24), cf. section 2.2.2, region F) as

$$T_{P,F'} = \frac{k'_{--}+2k'_+ - k'_{++}}{k'_{--}k'_+}(h + T_i(k'_{--}+k'_+))\,. \tag{30}$$

A further transformation leads to

$$T_{P,F'} = \frac{1+2k_L}{m'(1-m'+k_L)}\frac{Lh}{U_O} + \frac{1+k_L}{m'(1-m'+k_L)}T_i\,. \tag{31}$$

Equation(31) can be obtained also directly from Eq.(24) by the replacement

$$m \rightarrow 1-m'\,. \tag{32}$$

In the same manner there follows, e.g., the increase of the phase shift (to be measured between the *negative* switching edges $s'_2 = 1 \rightarrow 0$ and $s'_1 = 1 \rightarrow 0$) of the switching functions s'_1 and s'_2 per cycle from the relation for m and region D

$$\Delta\tau_{n+1,n,D} = \frac{1}{k_{--}}(k_{++} - k_+ + k_{--} - k_-)(1 + \frac{k_{--}}{k_{++}})T_i \tag{33}$$

(modified form of Eq.(17)) for m' and region D' as

$$\Delta\tau_{n+1,n,D'} = \frac{1}{k'_{++}}(k'_{--} - k'_- + k'_{++} - k'_+)(1 + \frac{k'_{++}}{k'_{--}})T_i\,. \tag{34}$$

Based on this there results

$$\Delta\tau_{n+1,n,D'} = \frac{2k_L(1+2k_L)}{(m'+k_L)(1-m'+k_L)}T_i \tag{35}$$

where Eq.(26) is considered. For the sake of brevity further details have to be omitted here.

2.2.4 Analysis for $u_N \approx 0.5\ U_O$

As a more detailed analysis shows, the description of the system behavior as given in section 2.2.2 and section 2.2.3 for $m > 0.5$ for

$$t_{T,\mathrm{on}} \le t_{T,\mathrm{off}} + 2T_i \tag{36}$$

and correspondingly for $m < 0.5$ for

$$t_{T,\mathrm{off}} \le t_{T,\mathrm{on}} + 2T_i \tag{37}$$

is valid here. The operating behavior for $m \approx 0.5$ is not included, therefore.

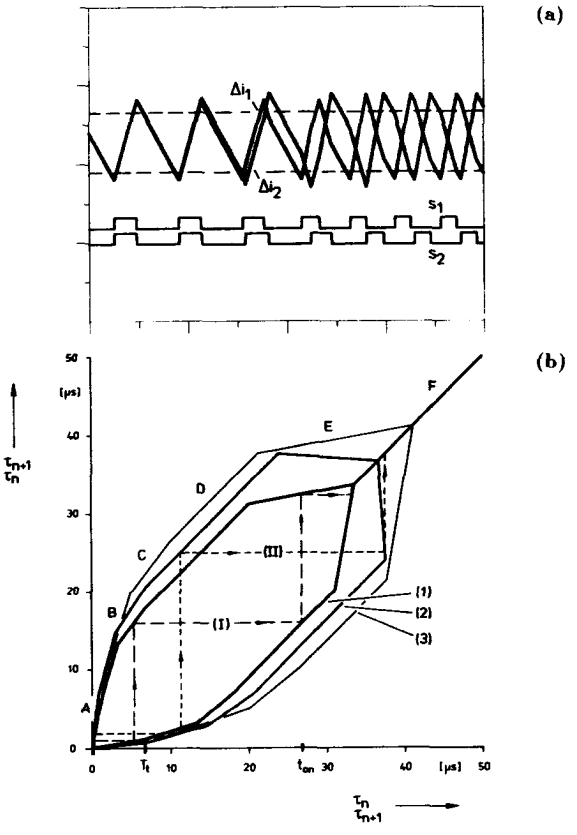

Fig.6: Representation of the opposite-phase lock-in process based on the time shapes of the current ripples Δi_1 and Δi_2 and of the corresponding switching functions s_1 and s_2 (cf. (a)) and of the lock-in characteristic (cf. (b)). Operating parameters for (a) and characteristic (1) equal to those for Fig.3(c), especially $m > 0.5$, $T_i = 6.5\,\mu s$ and $k_L = 0.33$; characteristic (2): operating parameters as for (1), but $k_L = 0.5$; characteristic (3): operating parameters as for (1), but $T_i = 10\,\mu s$; the time marks shown along the abscissa are related to characteristic (1). The phase shift of the negative switching edges $s_1 = 1 \rightarrow 0$ and of the positive switching edges $s_2 = 0 \rightarrow 1$ (as being present in the stationary case, cf. Fig. 5(f)) can also reach values $> T_i$. This is evident from the lock-in process (II) as shown for (2).

If now for $m > 0.5$ the on-time becomes larger than the maximum on-time (as defined by Eq.(36)) or, if the input voltage becomes smaller than the minimum input voltage corresponding to this maximum relative on-time, there results (as can be checked by digital simulation) a locking of the pulses $s_2 = 1$ in the center of the off-intervals $s_1 = 0$ and therefore an ideal phase shift $\tau_n = \frac{1}{2}T_P$ of s_1 and s_2. Equal conditions are valid for relative off-times becoming larger than their maximum value given for $m < 0.5$.

The extremly involved description of this case would go beyond the scope of this paper. It is important to note that also in the vicinity of the operating point $m = 0.5$ or $\alpha_T = 0.5$ (and not only and exclusively in operating point $m = 0$) there results a phase displacement of s_1 and s_2 by half a pulse period. Therefore, in this region for the self-adjusting staggered switching the same conditions are given as also for constant switching frequency and force staggered switching. For $m > 0.5$ and $m < 0.5$ only an approximate correspondence of force and self-adjusting staggered switching is given.

2.3 Opposite-Phase Lock-In Characteristic

The entering of the system into the opposite-phase mode can be represented clearly graphically based on the results derived in the previous sections. For this purpose one has to draw the time-shift τ_{n+1} of the switching functions (given after one switching cycle has elapsed) over the displacement τ_n at the beginning of the switching cycle. For the further considerations $m > 0.5$ is assumed. There, one has to distinguish among the regions A – F according to the analysis in section 2.2.2. If the mirror image with respect to the line $\tau_{n+1} = \tau_n$ of the characteristic $\tau_{n+1} = \tau_{n+1}\{\tau_n\}$ ($\tau_n = \tau_n\{\tau_{n+1}\}$) is added, we

obtain the opposite-phase lock-in characterisitc shown in **Fig.6**(b) where each end point τ_{n+1} can be interpreted as a new initial time-shift τ'_n. From this one can directly gain $\tau'_{n+1} = \tau_{n+2}$. A step-by-step continuation of this procedure (until the line $\tau_{n+1} = \tau_n$ is reached) covers the entire lock-in process (cf. (I) and (II) in Fig.6(b)).

The influence of parameter changes on the lock-in process is especially clearly described by the lock-in characteristic. As an example there is shown in Fig.6 besides the characteristic (1) for $T_t = 6.5\,\mu s$ and $k_L = 0.33$ (remaining parameters cf. Fig.3(c)) also the characterisitc for $T_t = 6.5\,\mu s$ and $k_L = 0.5$ (cf. (2)) and for $T_t = 10\,\mu s$ and $k_L = 0.33$ (cf. (3)). The increase of the switching delay time T_t as well as the increase of the coupling k_L results in an increase of the phase shifting effect or in a widening of the lock-in characteristic. Therefore, the stationary phase shift is obtained within a reduced number of switching cycles.

Remark: For initial phase equality $\tau_n = 0$ of the switching functions and ideal symmetry theoretically no phase shift of switching functions would occur. However, due to the unsymmetries (practically always given) and/or due to a disturbance in the current measurement signals i_1 and i_2 there is always given a minor lag of s_2 as compared to s_1 which initiates the lock-in process.

2.4 Sensitivity to Unsymmetries

Because of the assumption of ideal symmetry for the mathematical description of the system behavior we have to pose the question concerning the sensitivity of the locked-in state with respect to an unsymmetry of the partial systems (tolerances $\pm\Delta T_t$, $\pm\Delta h$, $\pm\Delta i^*$, $\pm\Delta L$). This question is important regarding practical realization.

In the following we will analyze the influence of a tolerance $\Delta T_t = \pm\delta T_t$ of the switching delay times of the partial systems

$$\begin{aligned} T_{t,1} &= (1-\delta)T_t \\ T_{t,2} &= (1+\delta)T_t \,. \end{aligned} \tag{38}$$

This should work as an example for the effects of an unsymmetry on the system behavior. There, $m > 0.5$ is assumed and only the region E (cf. section 2.2.2) is considered. Thereby also the boundary of the stationary operation (region F) is covered.

As an involved calculation shows, there results (as a consequence of the unsymmetry) a reduction of the phase-shift of s_1 and s_2 per switching cycle

$$\Delta\tau_{n+1,n,E,\delta} = \Delta\tau_{n+1,n,E,\delta=0} - \frac{(1+2k_L)(2+3k_L)}{(1-m+k_L)(m+k_L)}\,kT_t \,. \tag{39}$$

($\Delta\tau_{n+1,n,E,\delta=0}$ denotes the phase shift per switching cycle as being present for ideal symmetry $\delta = 0$, cf. Eq.(38)). According to Eq.(39) this reduction is proportional to the relative tolerance δ.

The phase shift per switching cycle $\Delta\tau_{n+1,n,E,\delta}$ becomes 0 already for a shift of $s_{2,n} = 0 \to 1$ and $s_{1,n} = 1 \to 0 \;< T_t$. The unsymmetry is therefore compensated by a reduction of the phase shift in the stationary operation. For extreme unsymmetry there remains an overlap of the regions $s_1 = 1$ and $s_2 = 1$ of the switching functions s_1 and s_2. As compared to ideal conditions there results a higher ripple of the total input current $i_N = i_1 + i_2$.

As a closer analysis shows, the boundary of the system-inherent synchronization of s_1 and s_2 in opposite phase (or of a locking of the pulse frequencies of the partial systems) is reached independently of m for

$$\delta_{\max} = \frac{k_L}{1+\frac{3}{2}k_L} \,. \tag{40}$$

For a typical value $k_L = 0.33$ this means (theoretically) a maximum admissible tolerance of the switching delay times $T_{t,1}$ and $T_{t,2}$ of $\delta_{\max} \approx 0.2$ or $T_{t,1} = 0.67\,T_{t,2}$. For the unsymmetry $\delta < 0.05$ to be expected at the most for practical relaization therefore a sufficient robustness of the self-adjusting ripple compensation is given.

By digital simulation also the insensitivity of the locked-in state with regard to further unsymmetries (as to be expected for practical realization) of the partial systems (tolerances $\pm\Delta h$, $\pm\Delta i^*$, $\pm\Delta L$) has been checked and proven. The detailed investigation of the robustness is the topic of further research at present. The results shall be published in a further paper in connection with an optimization of the system behavior (via a proper choice of the parameters k_L and T_t).

3 Digital Simulation

For supplying the system shown in Fig.2 from the AC mains

$$u_N = \hat{U}_N \sin\omega_N t \tag{41}$$

there is a continuous variation of the voltage transfer ratio

$$m = M\sin\omega_N t \qquad M = \frac{\hat{U}_N}{U_O} < 1 \,. \tag{42}$$

For a switching frequency f_P being high as compared to the mains frequency f_N ($\omega_N = 2\pi f_N$) one can assume, however, that the input voltage is constant over several switching cycles. Therefore, no basic change of the operating behavior (as described in the previous sections for $m < 0.5$, $m \approx 0.5$ and

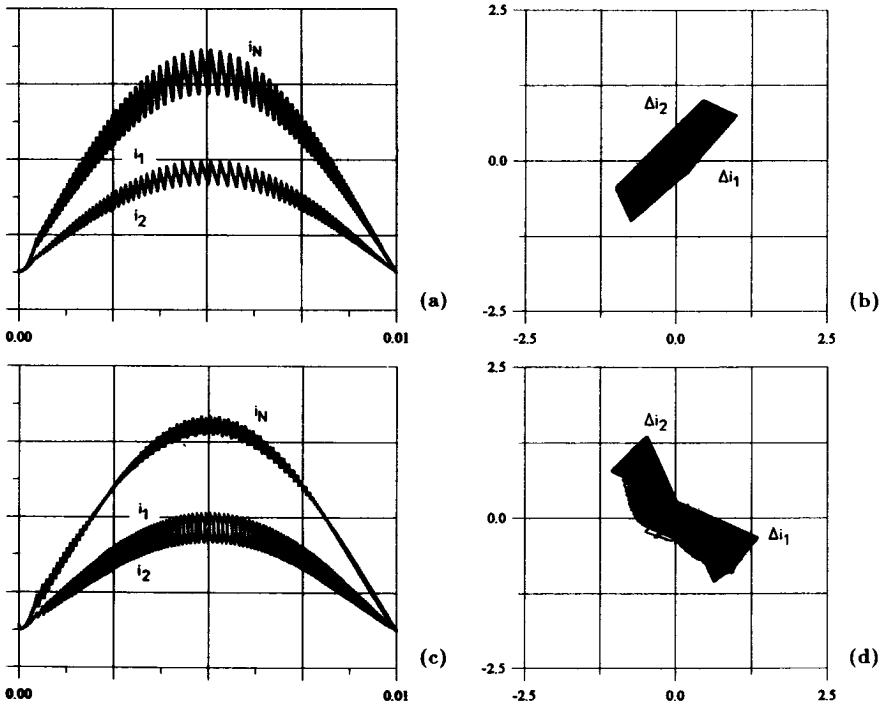

Fig.7: Results of a digital simulation of the operation behavior of the system shown in Fig.2 for sinusoidal input voltage for $T_t = 0$ (cf. **(a)** and **(b)**) and for $T_t = 6.5\,\mu s$ (cf. **(c)** and **(d)**). Representation of the partial currents i_1 and i_2 and of the total current i_N (6 A/div) within half a mains period (cf. (a) and (c)) and of the corresponding phase diagrams $\Delta i_2 = \Delta i_2\{\Delta i_1\}$ (1.25 A/div) of the ripples of the partial currents. Time scale: 2.5 ms/div; simulation parameters: $\hat{U}_N = 311\,\mathrm{V}, U_O = 380\,\mathrm{V}, \hat{I}_N^* = 8\,\mathrm{A}, h_{\max} = 2\,\mathrm{A}, L_N = 1.6\,\mathrm{mH}, L_1 = L_2 = 4.8\,\mathrm{mH}$.

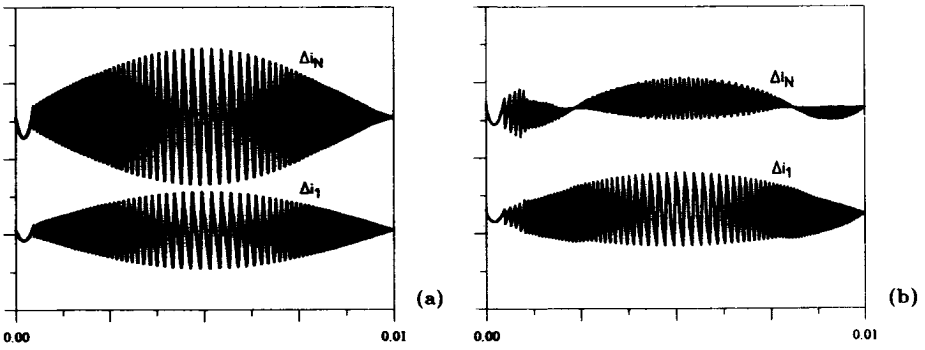

Fig.8: Time shapes (corresponding to Fig.7) of the ripple Δi_1 of the partial current i_1 and of the ripple Δi_N of the total current i_N. **(a):** $T_t = 0$ (cf. Fig.7(a) and (b)); **(b):** $T_t = 6.5\,\mu s$ (cf. Fig.7(c) and (d)); scales: 2.5 ms/div, 2.5 A/div.

$m > 0.5$ and for constant input voltage and constant hysteresis band width) can be expected.

As a digital simulation proves, in anaolgy to the considerations in connection with Fig.4(a) a self-adjusting staggered switching of the partial systems also for AC supply (besides coupling k_L of the partial systems) is linked to a delay T_t of the control signals of the power transistors. For switching ideally without delay ($T_t = 0$) of T_1 and T_2 no phase shift of the ripple currents occurs. This means also, that no cancellation of the harmonics of the partial currents i_1 and i_2 results (cf. time shape of i_N shown in **Fig.7**(a)).

By insertion of a switching delay time T_t there results a phase-shifted operation of the partial systems in wide intervals of the mains period. This reduces the ripple of the total current (cf. Fig.7(c)). The phase shift occurring there can be seen clearly for orthogonal plotting of the ripple currents Δi_1 and Δi_2 (cf. Fig.7(d)) in the phase plane. The trajectory $\Delta i_2 = \Delta i_2\{\Delta i_1\}$ shows an inclination angle of $-\frac{\pi}{4}$ with respect to the abscissa. Accordingly, an opposite phase operation of the partial systems is present. The trajectory of the ripple currents for $T_t = 0$ shows an inclination angle of $+\frac{\pi}{4}$ (cf. Fig.7(b)) according to the then in phase variation of the currents i_1 and i_2.

For low values of T_t (and variable hysteresis control) the partial currents are forced into phase when the mains voltage approaches 0. Therefore, as the representation of the ripple of a partial current and of the total current shows (cf. **Fig.8**(b)) there results an in-phase operation of the partial systems over several switching cycles after each zero-crossing of the mains voltage. Due to the rounding errors in the simulation (or, in practice, caused by a minor asymmetry of the partial systems or by disturbances) there occurs finally a minor phase shift of the switching state changes of the partial systems. This initiates the lock-in into opposite-phase operation as described in section 2.3.

The ripple Δi_N of the mains current (shown in Fig.8(b)) shows the shape being characteristic also for force staggered switching of the partial systems (cf. Fig.13 in [4]). In consistency with the considerations of section 2.2.4 the partial systems are synchronized idealy in opposite phase for $m \approx 0.5$. Accordingly, in the points $m = 0.5$ (cf. Fig.3(b)) or for $u_N = \frac{1}{2}U_O$ (the inductive fundamental voltage drops across L_N and L_1 or L_2 are neglected) $\Delta i_N = 0$ is obtained. Because of this contraction of the ripple current shape in $m = 0.5$ there remains only a relatively low ripple of the mains current also for $m > 0.5$ (in the vicinity of the mains voltage maximum) despite the larger hysteresis band width being present there for variable hysteresis control.

4 Experimental Results

The experimental analysis of the operating behavior of the circuit shown in Fig.2 has been performed at the University of Minnesota. The realization of the laboratory model has been based on the following operational parameters (nominal values) and specifications of the circuit elements

$$P_O = 500\,\mathrm{W} \quad U_O = 206\,\mathrm{V} \quad \hat{U}_N = 150\,\mathrm{V} \quad f_N = 60\,\mathrm{Hz}$$
$$h_{\max} = 1\,\mathrm{A} \quad L_N = 2\,\mathrm{mH} \quad L = 5\,\mathrm{mH} \quad T_t \approx 3.5\,\mu s$$

(h denotes the width of the hysteresis band at the maximum of the mains voltage). The values of the inductances being relatively high as compared to a dimensioning for industrial application (and the low average switching frequency $f_{P,\mathrm{avg}} \approx 9\,\mathrm{kHz}$) have been chosen for making a clear representation of the system function possible. Furthermore, due to the easier adjustability of the coupling factor k_L the magnetic coupling of the partial systems has been replaced by the arrangement corresponding to a T-equivalent circuit (cf. Fig.2). For the realization of the current control (realized as variable hysteresis control) of each partial system integrated control circuits CS-322 (Cherry Semiconductor Corp.) have been used. The current reference values have been derived directly from the input voltage. The switching delay time T_t (being adjusted to the relatively low pulse frequency) has been obtained in connection with the threshold voltage of the power MOSFETs by series resistances at the gate and an increase of the gate capacitance by paralleling of capacitors.

As becomes immediately clear by comparing Fig.7(c) and **Fig.9** the theoretical considerations are proven by measurement results. There remains only a very low ripple in the total current i_N. The low-frequency distortion of the input current corresponds to the distortion of the mains voltage u_N. It is caused by the derivation of the reference values of the partial currents from the mains voltage.

5 Simplification of the System Structure

From an engineering point-of-view finally the question has to be posed if for obtaining a certain operating behavior (i.e., actually for the solution of a *control-oriented* problem), in fact a coupling of the *power circuits* of the partial systems would be required.

When the circuit shown in Fig.2 is represented as a control-oriented block structure, the influence of L_N occurs in the form of a coupling of voltage differences formed dependent on the respective switching state. As can be seen by transformation of the block structure via transposition of the branching and summation points, the coupling can be realized also based on partial currents, however. If this consideration is applied to the actual circuit, there results the system structure as given in **Fig.10**.

As a digital simulation proves, the circuits according to Fig.2 and Fig.10 show an identical operating behavior with respect to the lock-in of the switching functions s_1 and s_2 in opposite phase. There, the relations

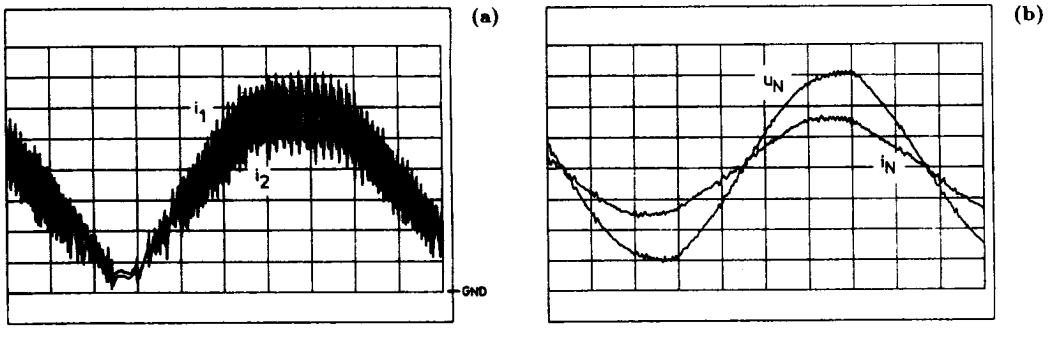

Fig.9: Experimental analysis of the self-adjusting staggered switching of an AC-DC boost power factor corrector according to Fig.2. **(a):** input currents i_1 and i_2 of the partial systems (0.5 A/div); **(b):** total input current i_N of the system (4 A/div) and mains voltage u_N (50 V/div). Time scale: for (a): 1 ms/div, for (b): 2 ms/div.

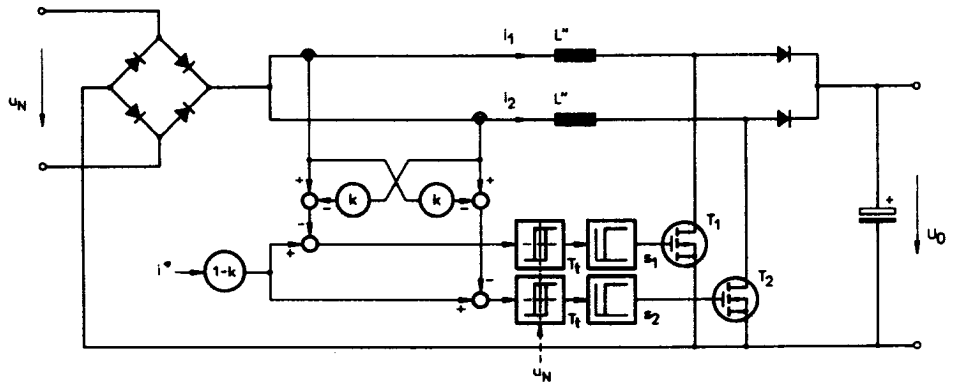

Fig.10: Structure of the circuit according to Fig.2 if the inductance L_N (coupling the partial systems) is replaced by a coupling k of the current control loops. The apparent reduction (due to the coupling) of the partial currents has to be considered by a factor $(1-k)$ in the reference value path of the current control.

$$k = \frac{k_L}{1+k_L} \tag{43}$$

and

$$L'' = \frac{1+2k_L}{1+k_L} L \tag{44}$$

have to be considered. A detailed investigation of the operating behavior and a comparison of the realization efforts of the circuits is the topic of further research at present.

6 Conclusions

The staggered switching of partial systems connected in parallel becomes of special importance increasingly also for the realization of converter systems of lower power, high efficiency and high power density (cf. e.g., [20] or [21]). (The importance for higher power systems, e.g., for traction application, has been already stressed very much in the past.)

As this paper shows, a staggered operation can be obtained not only via a direct voltage control with constant switching frequency of the partial systems (force staggered operation) but also for hysteresis control of the partial currents (variable switching frequency) by coupling of the power circuits of the partial systems in connection with delaying the control signals of the power transistors.

There result the following advantages and disadvantages as compared to force staggered switching:

Advantages:

+ simple realizabiltiy (especially for replacing L_N (cf. Fig.2) by coupling of the current control loops (cf. Fig.10))
+ insensitivity of the current control regarding the shape of the input voltage (if a not direct mains-dependent current reference value is given)
+ highly dynamic current control
+ due to the not constant pulse frequency a more even distribution of the spectrum of the harmonic power as compared to force staggered switching (constant pulse frequency) is obtained; this means that there exists the possibility of reducing the filtering effort [22]
+ direct guidance of the partial currents, direct overcurrent limitation, no additional provisions required for symmetrization of the input currents of the partial systems; the self-adjusting staggered switching is linked only to a locally equal width of the current hysteresis band of the partial currents, but not to an equal value of the current reference values; this means that the possibility of a specific unsymmetric load distribution for redundant parallel connection is possible.

Disadvantages:

– due to the fact that the phase shift of the partial systems usually deviates from π, the total input current shows a slightly higher harmonic content as compared to force staggered switching; e.g., for $m > 0.5$ a phase shift of the switching functions of at least $\tau_n = t_{T,\mathrm{on}} + T_t$ is present in the stationary case; especially for values $\alpha_T \to 0$ this does not correspond to the ideal phase shift of half a switching period $\frac{1}{2}T_P$. Therefore, the self-adjusting staggered switching (or input current ripple cancellation) can be set directly equal to a force staggered switching only for voltages $u_N \approx U_O$ and/or in the vicinity of $\alpha_T = 0.5$.
– presence of low-frequency harmonics in the mains current for high switching delay time T_t (cf. shape of Δi_1 in Fig.8(b))
– so far limitation to two partial systems
– limited applicability (concerning the self-adjusting ripple cancellation) for wide input voltage region
– limitation to continuous conduction mode.

Basically, with the proposed concept a significant reduction of the input current harmonics of a converter built up by parallel connection of two partial systems is obtained, where the advantages of simple hysteresis control are maintained. A limitation of the applicability is given only where a wide input voltage region and heavily changing load (including open load condition) are to be expected.

6.1 Future Research

The aim of this paper has been to introduce the basic features of a new circuit and control concept. There exist a multitude of tasks for further research projects:

- optimization of the operating behavior via appropriate choice of k_L and T_t where the unsymmetries of the partial systems (tolerances $\pm\Delta T_t$, $\pm\Delta h$, $\pm\Delta i^*$, $\pm\Delta L$, etc.) as they occur in practical realization have to be considered; as optimization criteria there are to be seen $\Delta I_{N,\mathrm{rms}}$, $\Delta I_{i,\mathrm{rms}}$ $(i = 1, 2)$ and the amplitude of possibly existing low-frequency mains current harmonics
- analysis of the applicability of the concept for other basic converter structures; according to investigations performed so far an applicability is also possible for buck-converters
- based on the duality of a circuit structure formed by paralleling two buck converters and of a three-level boost converter (cf. Fig.1 in [23] or [24]) the transfer of the concept to three-level converters should be tried
- comparison of the realization effort for magnetic coupling of the input inductances L_I (cf. Fig.1) and for replacement of the coupled winding arrangement by a T-equivalent circuit (cf. Fig.2)
- it should be tried to extend the control-oriented coupling of partial systems (cf. Fig.11) to more than two partial systems
- investigation of the applicability of the concept to three-phase converters; here, especially the efffect of the mutual influence of the phases for simple hysteresis current control (cf. p. 297 in [25]) is of interest.

The optimization of the operating behavior and the question of the applicability of the concept to buck converters for the case of control-oriented coupling of the partial systems is the topic of further research at the University of Minnesota and the Technical University of Vienna at present.

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