Identifying and Addressing
Important Developments of Power Electronics
Core Technologies

Future of Power Electronics Circuits

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FEPPCON 2019

Tromsö / Norway / June 26-28/2019

IEEE POWER ELECTRONICS SOCIETY
Powering a Sustainable Future

26/06/2019

IEEE
Advancing Technology for Humanity

Identifying and Addressing
Important Developments of Power Electronics
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Future of Power Electronics

Topology
Components
Control
Design
Manufacturing

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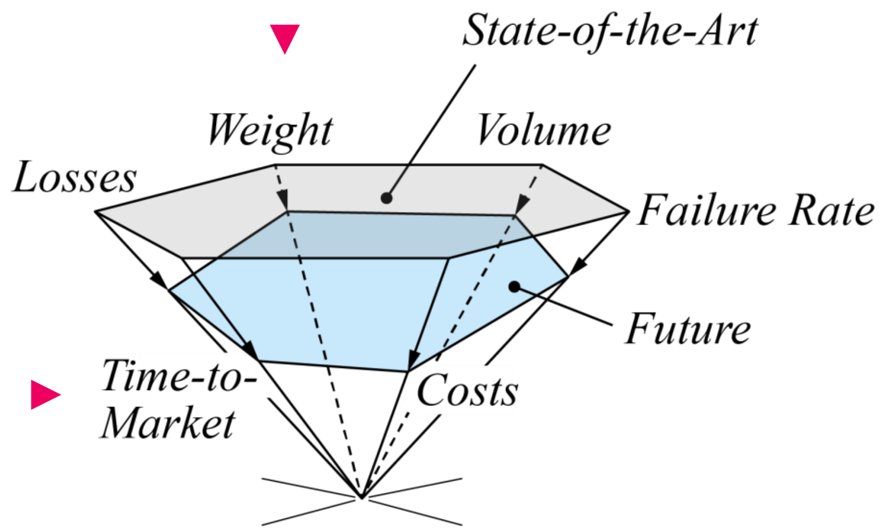
Outline

- ► *Performance Trends*
- ► *X-Concepts / "Moon-Shot" Technologies*
- ► *Power Electronics 4.0*

Required Performance Improvements

Environmental Impact... $[kg_{Fe}\ /kW]$ $[kg_{Cu}\ /kW]$ $[kg_{Al}\ /kW]$ $[cm^2_{Si}\ /kW]$

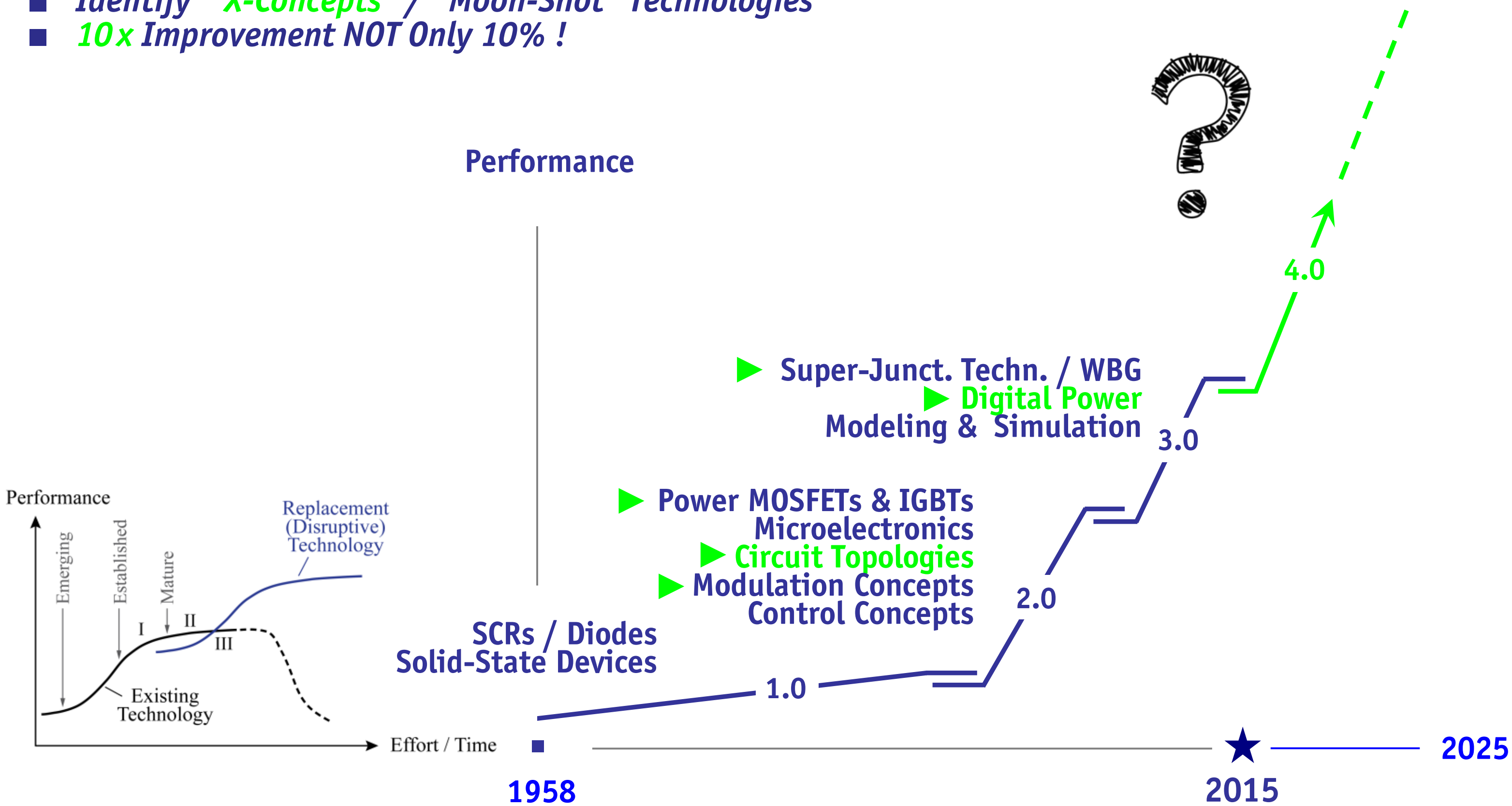
- Power Density [kW/dm^3]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Relative Losses [%]
- Failure Rate [h^{-1}]



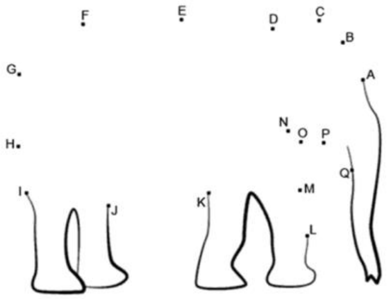
- Future → Cost / Cost / Cost & Robustness & Availability & Recyclability

S-Curve of Power Electronics

- *Power Electronics 1.0 → Power Electronics 4.0*
- *Identify "X-Concepts" / "Moon-Shot" Technologies*
- *10x Improvement NOT Only 10% !*



Topologies
Modulation & Control



History and Development of the Electronic Power Converter

E. F. W. ALEXANDERSON
FELLOW AIEE

E. L. PHILLIPI
NONMEMBER AIEE

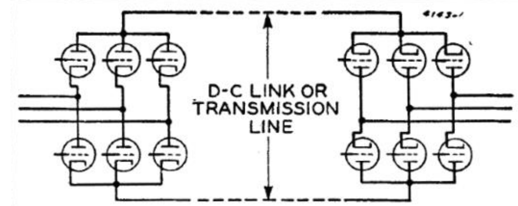


Figure 1. Electronic converter, dual-conversion type

THE TERM "electronic power converter" needs some definition. The object may be to convert power from direct current to alternating current for d-c power transmission, or to convert power from one frequency into another, or to serve as a commutator for operating an a-c motor at variable speed, or for transforming high-voltage direct current into low-voltage direct current. Other objectives may be mentioned. It is thus evidently not the objective but the means which characterizes the electronic power converter. Other names have been used tentatively but have not been accepted. The emphasis is on electronic means and the term is limited to conversion of power as distinguished from electric energy for purposes of communication. Thus the name is a definition.

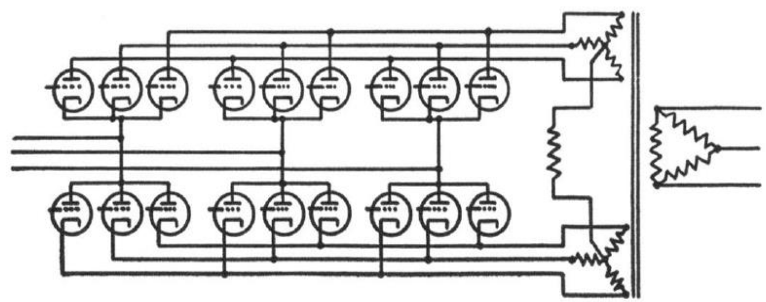
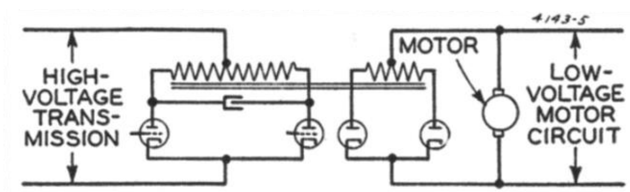


Figure 4 (left). Single-conversion-type frequency changer

Figure 5 (below). D-c transformer



Paper 44-143, recommended by the AIEE committee on electronics for presentation at the AIEE summer technical meeting, St. Louis, Mo., June 26–30, 1944. Manuscript submitted April 25, 1944; made available for printing May 18, 1944.

E. F. W. ALEXANDERSON and E. L. PHILLIPI are with the General Electric Company, Schenectady, N. Y.

1944 !

United States Patent [19] [11] **4,412,277**

Mitchell [45] **Oct. 25, 1983**

1983 !

[54] **AC-DC CONVERTER HAVING AN IMPROVED POWER FACTOR**

[75] Inventor: **Daniel M. Mitchell,** Cedar Rapids, Iowa

[73] Assignee: **Rockwell International Corporation,** El Segundo, Calif.

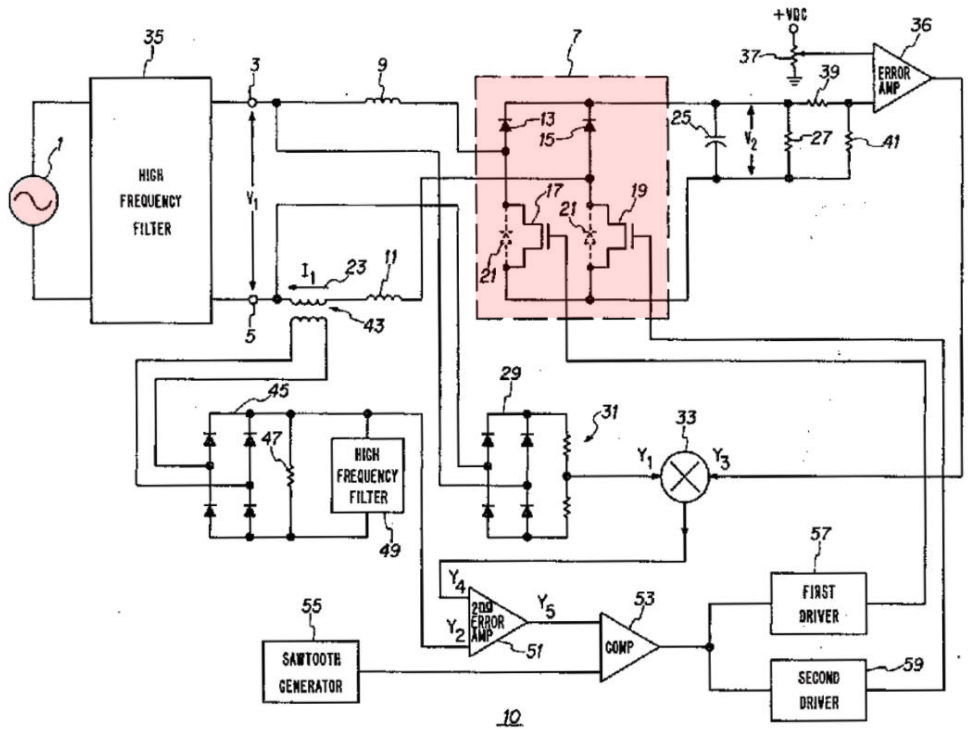
[21] Appl. No.: **414,757**

[22] Filed: **Sep. 3, 1982**

[57] **ABSTRACT**

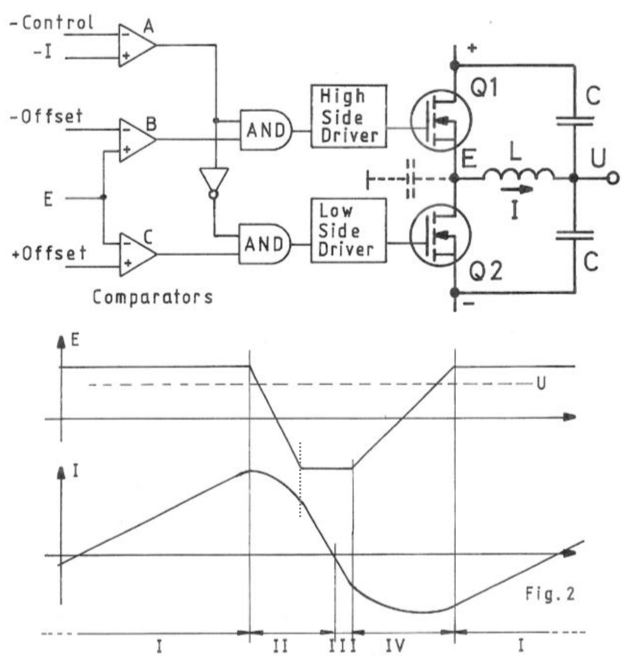
An AC to DC converter utilizes a first power converter for converting an AC signal to a DC signal under the control of a control signal. The control signal is generated by a control circuit that includes a first analog generator that provides a first signal that is analogous to the voltage of the AC signal that is to be converted. A second analog generator generates a second signal that is analogous to the current of the AC signal that is to be converted and a third analog generator generates a third signal that is analogous to the voltage of the DC output signal. The third signal and the first signal are multiplied together to obtain a fourth signal. The control signal is generated from the fourth signal and the second signal and is used to control the power converter such that the waveform of the current of the AC signal is limited to a sinusoidal waveform of the same frequency and phase as the AC signal.

8 Claims, 2 Drawing Figures



▶ ZVS/TCM Operation of Bridge-Legs

- *Avoids Utilization of Slow Internal Diodes of Si MOSFETs*
- *Enables High Sw. Frequency → Low Filter Inductor Volume*



Source: Joensson

PCIM'88

(POWER CONVERSION)

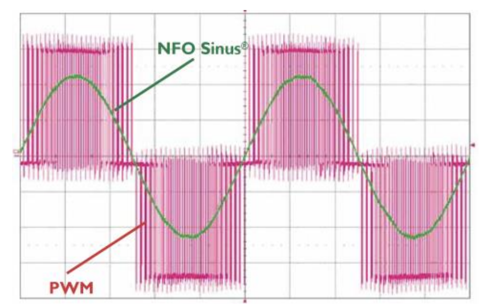
CONFERENCE

DECEMBER 8-10, 1988
TOKYO, JAPAN

← **1988 !**

Source: NFO Sinus

NFO Sinus® is available in size 0,37 kW up to 22 kW



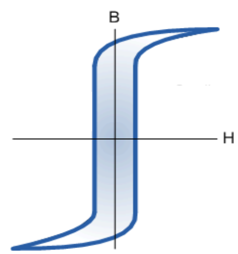
- *Generation of Continuous / Sinusoidal Motor Voltage w/o CM-Component*

— *Basic Topologies Known > 30…40 Years*
— *Min. Complexity Circuits Used in Industry*
— *Optimization of Modulation / Control Completed*
— *Several Solutions of Equal Performance*

SCC … Switched Capacitor Converters

***… "Refinements"** & Hybrid SCCs*
& Comparative Evaluation (!)

Passive Components



Source: www.electronics-tutorials.ws

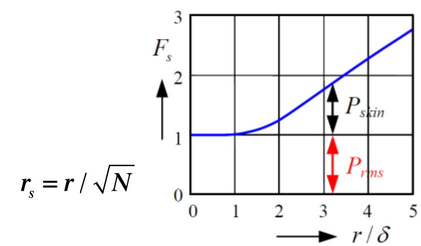
Magnetics as Example

Operation Frequency Limit (1)

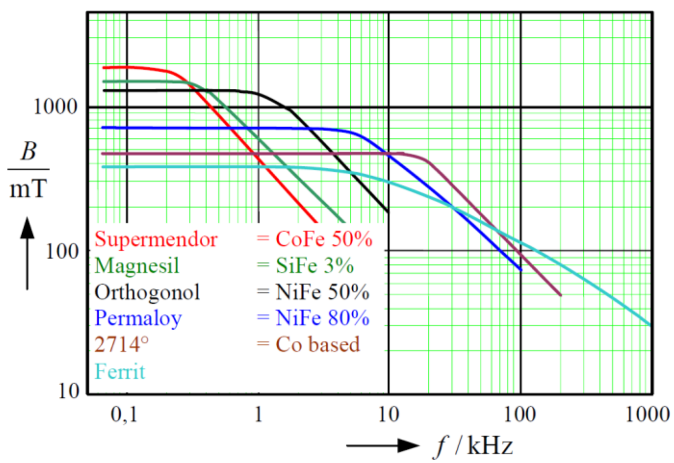
- ***Serious Limitation of Operating Frequency by HF Losses***

Source: Prof. Albach, 2011

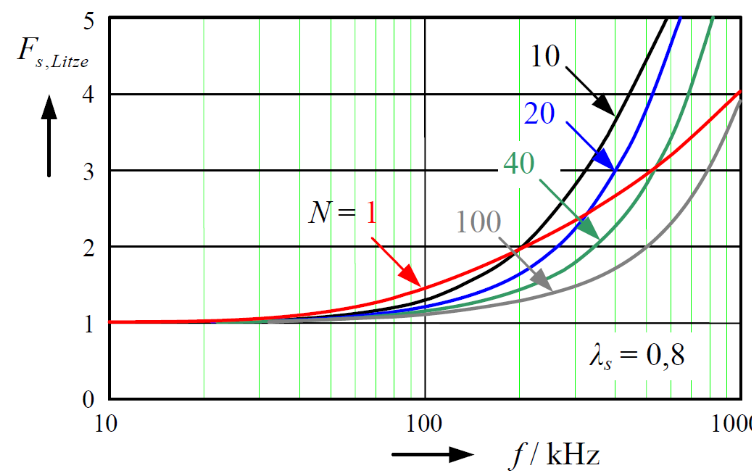
- Core Losses (incr. @ High Frequ. & High Operating Temp.)
- Temp. Dependent Lifetime of the Core
- Skin-Effect Losses
- Proximity Effect Losses



$$p_{VE} = \frac{\Delta P_{VE}}{\Delta V_E} = k\, f^{\alpha} \hat{B}^{\beta} = \text{const.}$$



- Adm. Flux Density for given Loss Density



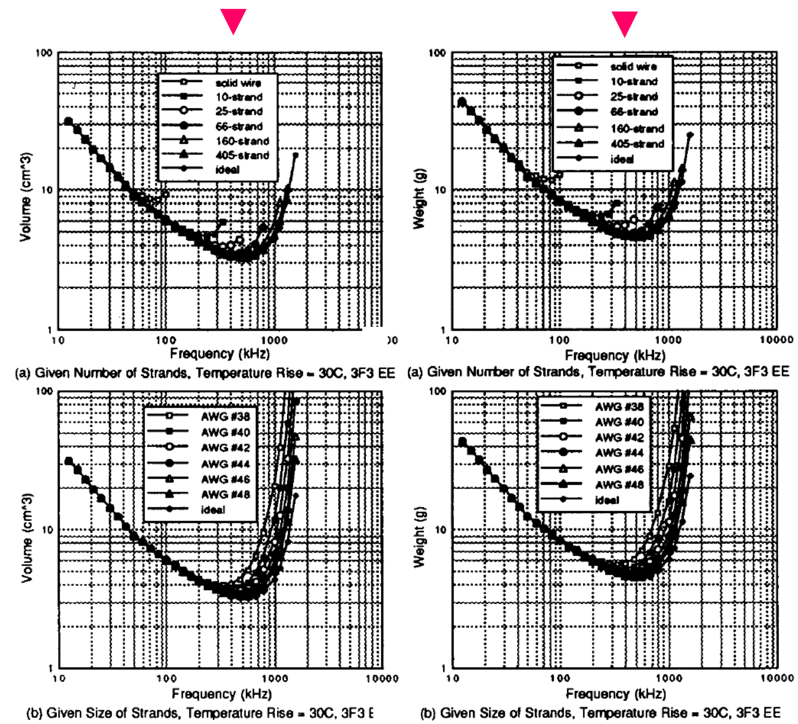
- Skin-Factor F_s for Litz Wires with N Strands

Operation Frequency Limit (2)

- *Higher Frequency Results in Smaller Size only Up to Certain Limit (for MnZn Core-Based Designs)*
- *Optimal Converter Operating Frequencies < 1MHz*
- *Difficult to Manufacture*

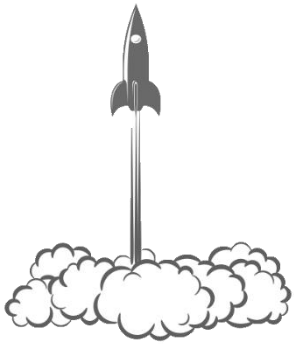
Source: Philips

Transformer Volume & Weight vs. Frequency



- *Automated Manufacturing → Magnetic Integration / PCB-Windings / Planar Shapes*

X-Technology **#1**



Wide Bandgap
Power Semiconductors

Low $R_{DS(on)}$ High-Voltage Devices (1)

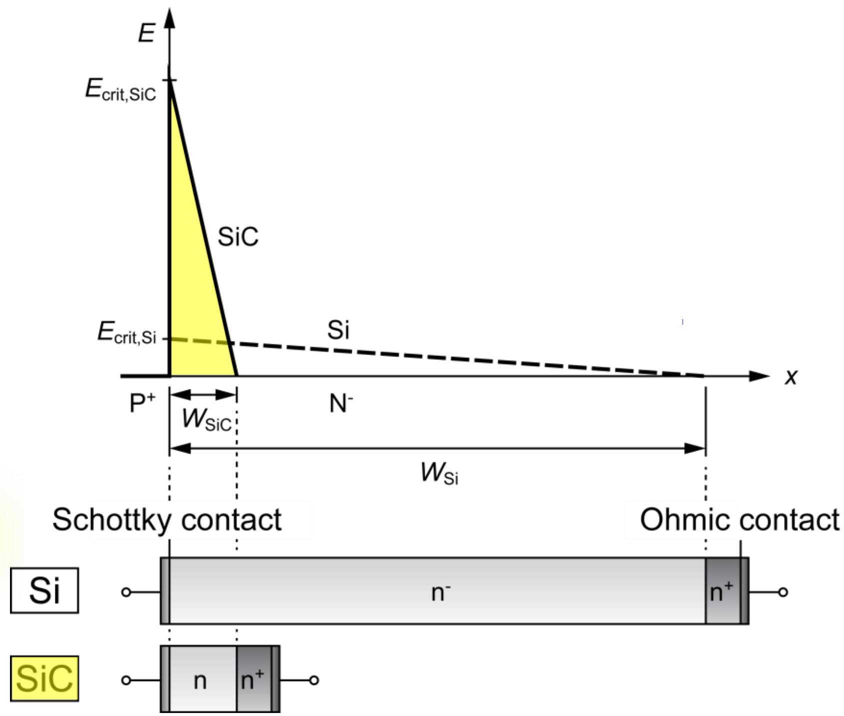
- **High Critical E-Field of SiC → Thinner Drift Layer**
- **High Maximum Junction Temperature $T_{j,max}$**

at 300 K	Si	GaAs	4H/6H-SiC	GaN
E_g (eV)	1.12	1.4	3.0-3.2	3.4
E_c (MV/cm)	0.25	0.3	2.2-2.5	3
μ_n (cm²/Vs)	1350	8500	100-1000	1000
ε_r	11.9	13	10	9.5
v_{sat} (cm/s)	1×10^7	1×10^7	2×10^7	3×10^7
λ (W/cmK)	1.5	0.5	3 - 5	1.3

$$R_{on}^{*} = \frac{4V_B^2}{\varepsilon\mu_n E_C^3} \leftarrow$$

For 1kV:	Si	SiC
W (μm)	100	10
N_D (cm⁻³)	10^{14}	10^{16}

$$R_{on,SiC}^{*} \approx \frac{1}{300} R_{on,Si}^{*}$$

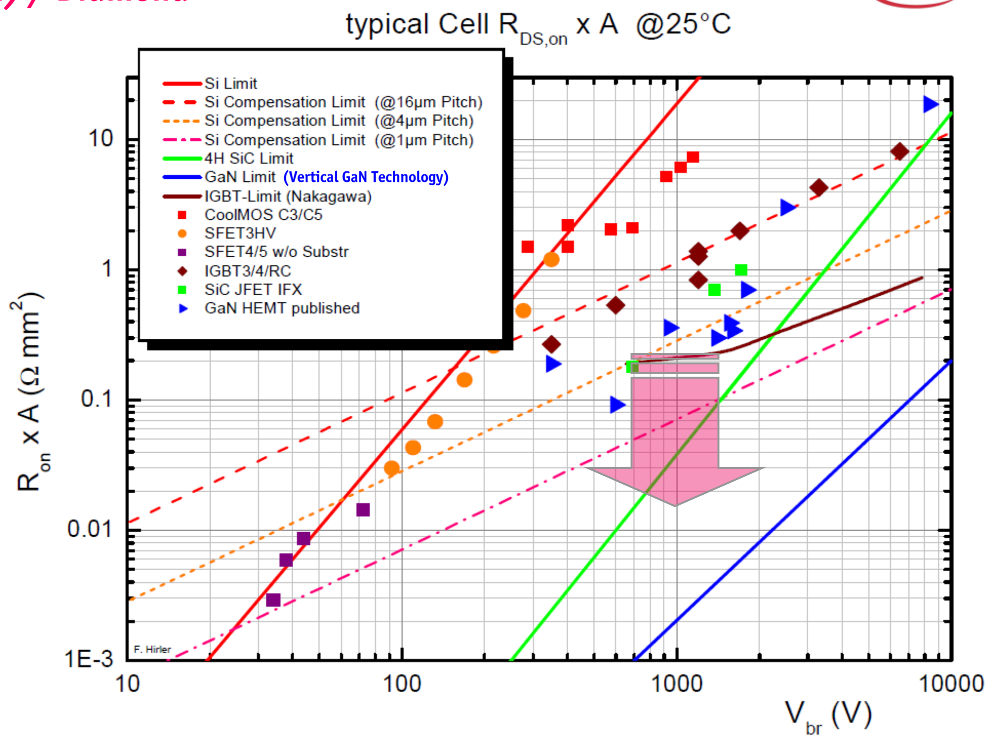


- **Massive Reduction of Relative On-Resistance → High Blocking Voltage Unipolar Devices**

Low $R_{DS(on)}$ High-Voltage Devices (2)

- Low Circuit Complexity
- High Power Conversion Efficiency
- SiC / GaN (Monolithic AC-Switch) / Diamond

Source: Infineon



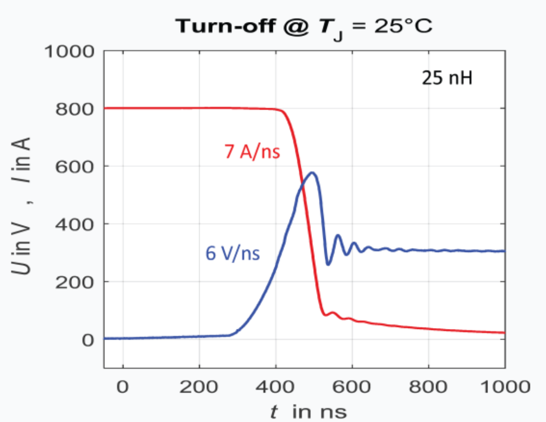
- *High Heat Conductivity* & *Excellent Switching Performance*

Low Switching Losses

- *Si-IGBT → Up to 6.5kV / Rel. Low Switching Speed*
- *SiC-MOSFETs → Up to 15kV (1st Samples) / Factor 10…100 Higher Sw. Speed*

Source: M. Bakran / ECPE 2019

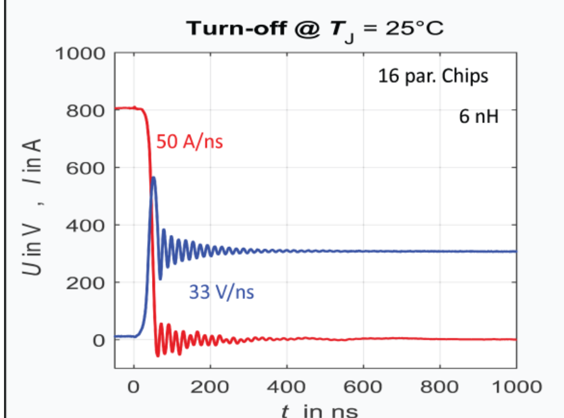
Si-IGBT / Hybrid-Pack 2



E_{off} = 45900 µJ

-> 8 kV/µs at 400V

SiC-MOSFET / (scaled for low inductance)

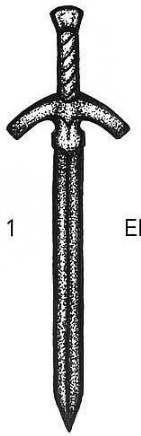


E_{off} = 4672 µJ

-> 44 kV/µs at 400 V

- *Extremely High di/dt & dv/dt → Challenges in Packaging / EMI*

Challenges



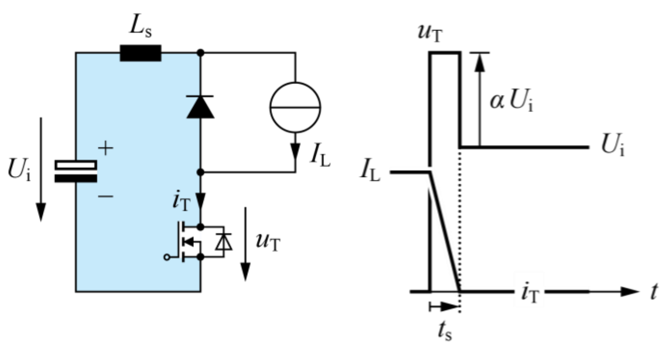
Idea: F.C. Lee

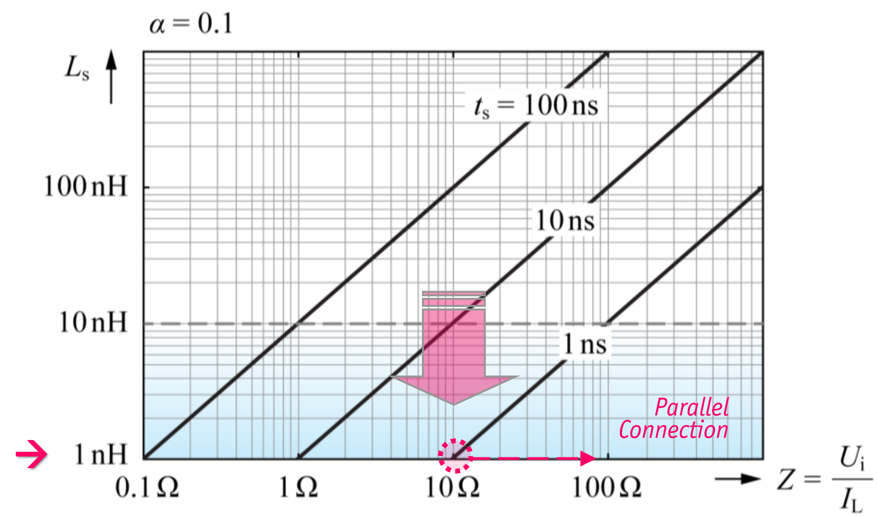
Circuit Parasitics (1)

$$L\frac{di}{dt} = u$$

- *Extremely High di/dt*
- *Commutation Loop Inductance L_s*
- Allowed L_s Directly Related to Switching Time t_s →

$$L_s \leq \frac{\alpha U_i}{\frac{I_L}{t_s}} = \alpha t_s \underbrace{\frac{U_i}{I_L}}_{Z}$$





- *Advanced Packaging & Parallel Interleaving for Partitioning of Large Currents*

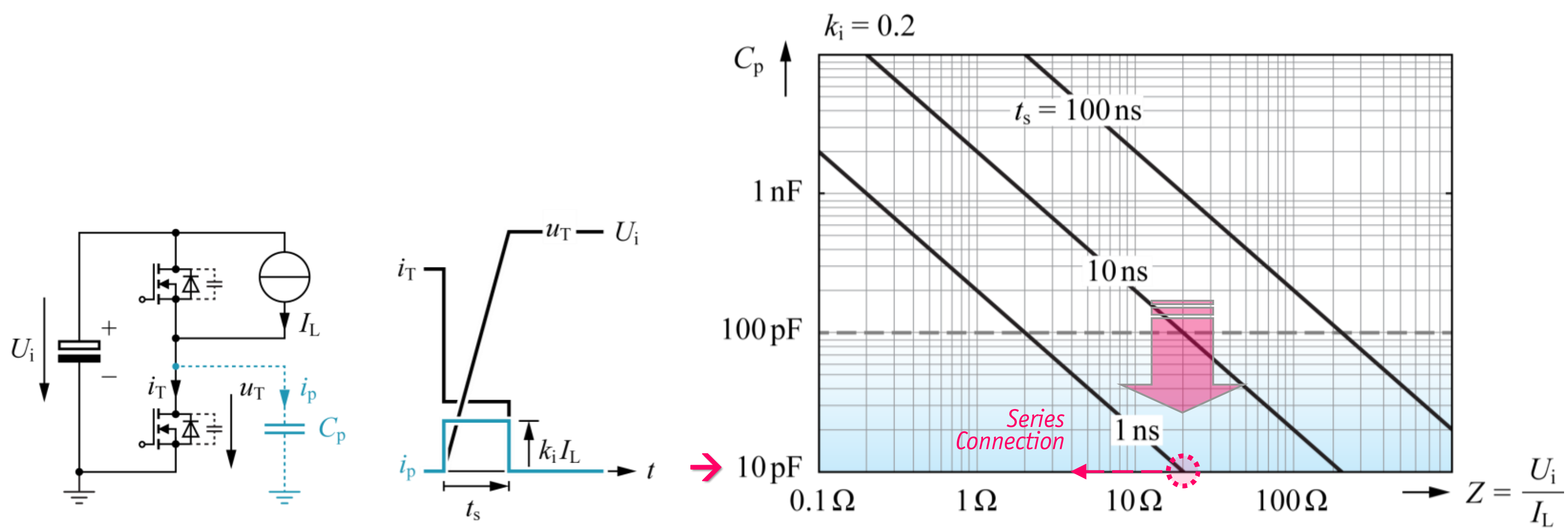
Circuit Parasitics (2)

$$C\frac{du}{dt}=i$$

- Extremely High dv/dt
- Switch Node Capacitance
- Allowed C_p Directly Related to Switching Time t_s →

$$C_p \le \frac{\alpha I_i}{\frac{U_i}{t_s}} = \alpha t_s \left(\frac{U_i}{I_i}\right)^{-1}$$

Z



- Advanced Packaging & Series Interleaving for Partitioning of Large Voltages

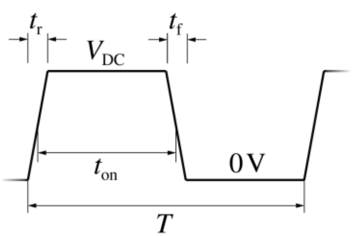
EMI Emissions

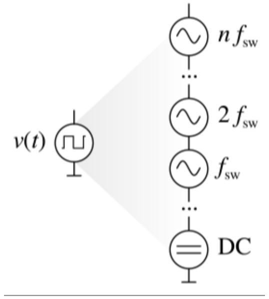
- Higher dv/dt → Factor 10
- Higher Switching Frequencies → Factor 10
- EMI Envelope Shifted to Higher Frequencies

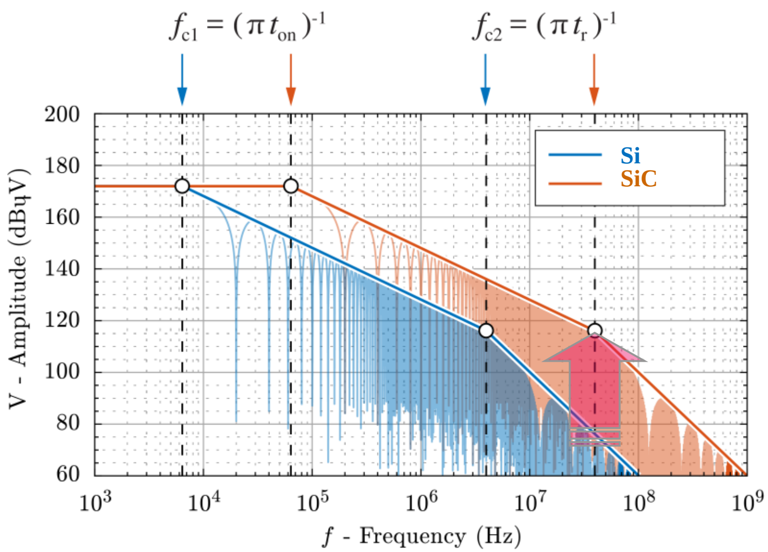
Idea: M. Schutten

f_S= 10kHz & 5 kV/us for (Si IGBT)
f_S= 100kHz & 50 kV/us for (SiC MOSFET)

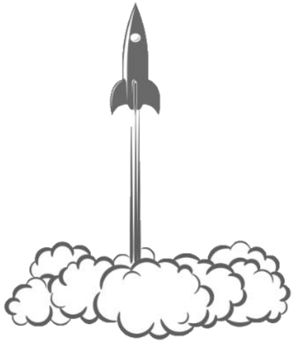
V_{DC} = 800V
DC/DC @ D= 50%







- Higher Influence of Filter Component Parasitics and Couplings → Advanced Design

X-Technology **#2**  Interleaving & Modularity

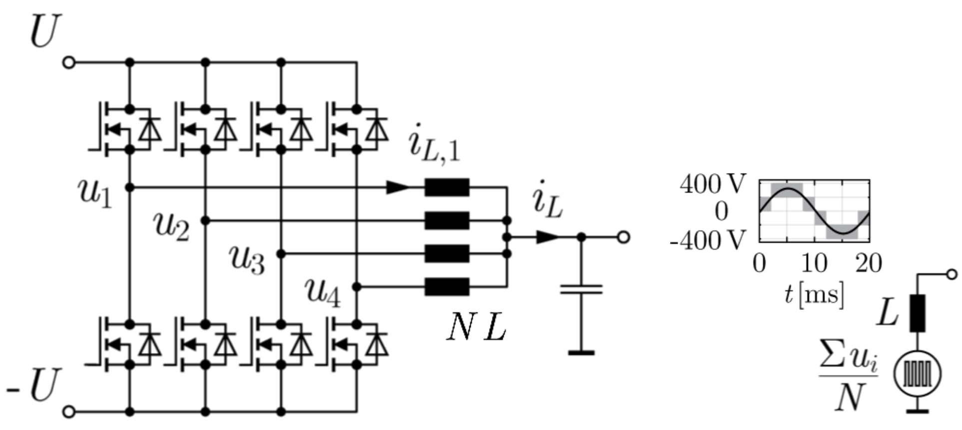
Parallel Interleaving (1)

- **Loss-Neutral Multiplication of Switching Frequency**
- **Reduced Ripple @ Same (!) Switching Losses**

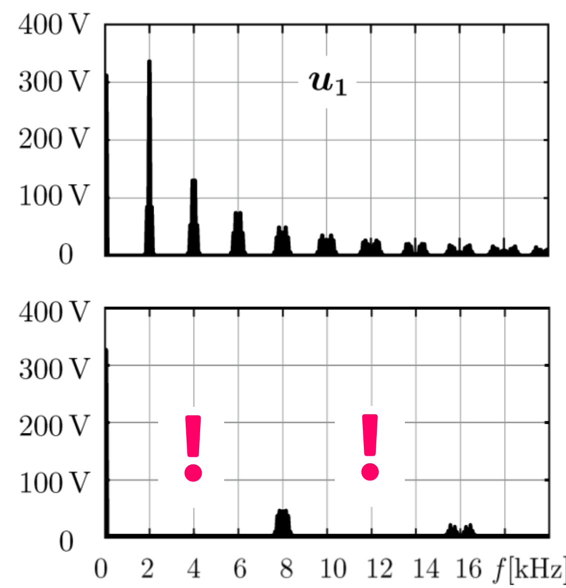
$$f_{S,\mathrm{eff}} = N \cdot f_S$$

$$\Delta I_{\max,N} = \frac{1}{N^2}\Delta I_{\max,N=1}$$

$$\Delta U_{\max,N} = \frac{1}{N^3}\Delta U_{\max,N=1}$$



N = 4



- **Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy**

Parallel Interleaving (2)

- Loss-Neutral Multiplication of Switching Frequency
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$$f_{S,\mathrm{eff}} = N \cdot f_S$$

$$\Delta I_{\max,N} = \frac{1}{N^2} \Delta I_{\max,N=1}$$

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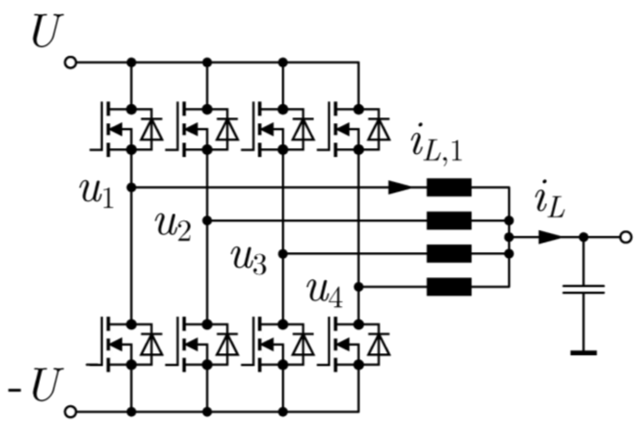
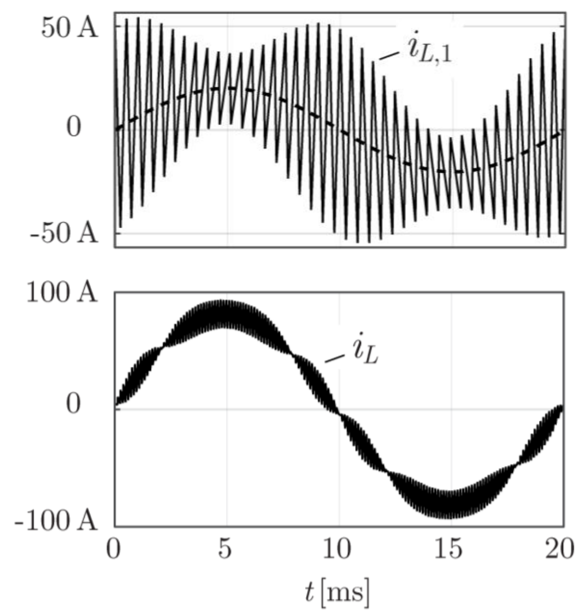


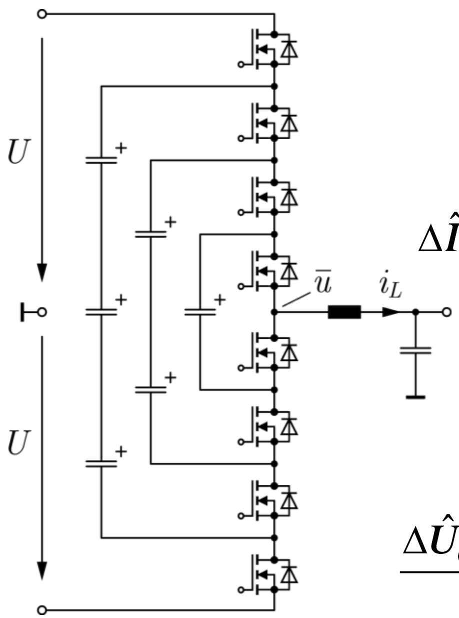
N = 4



- Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy

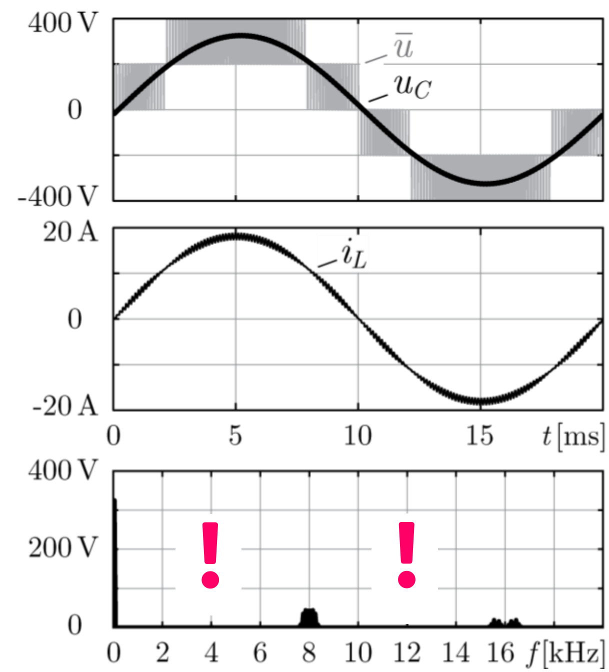
Series Interleaving (1)

- *Reduced Ripple @ Same (!) Switching Losses*
- *Lower On-Resistance @ Given Blocking Voltage → 1+1=2 NOT 2 ^{2} = 4 (!)*
- *Extends LV Technology to HV*



$$\Delta\hat{I}_{\mathrm{max},N} = \frac{1}{N^2}\overbrace{\Delta\hat{I}_{\mathrm{max},N=1}}^{\frac{U}{8 f_s L}}$$

$$\frac{\Delta\hat{U}_{\mathrm{C,max},N}}{U} = \frac{\pi^2}{32}\left(\frac{f_O}{f_S}\right)^2\frac{1}{N^3}$$

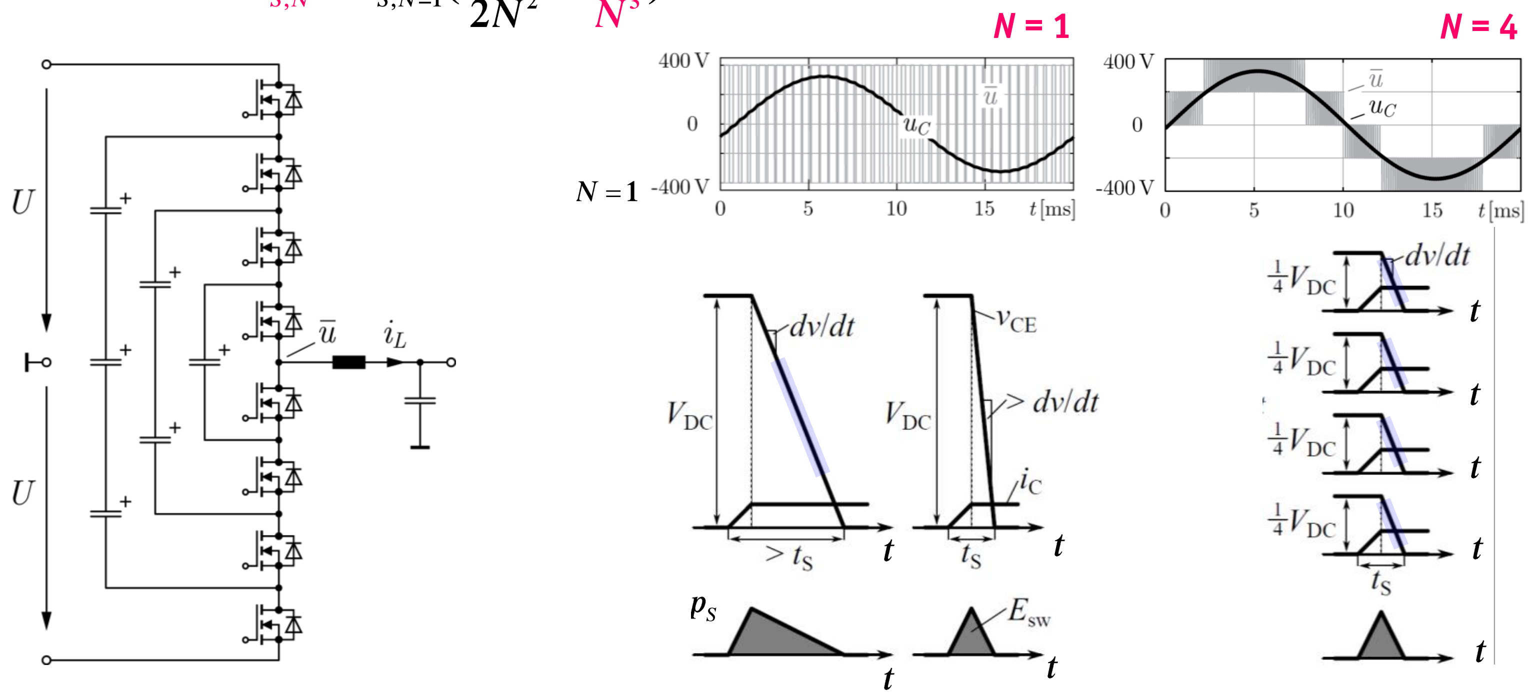


- Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy

Series Interleaving (2)

- Dramatically Reduced Switching Losses (or Harmonics) for Equal $\Delta i/I$ and dv/dt

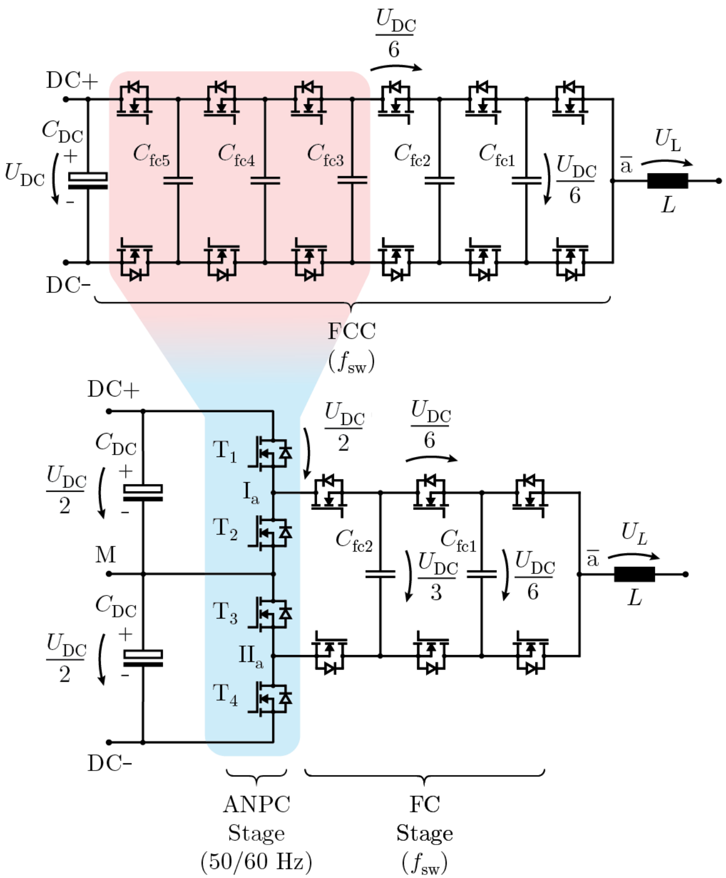
$$P_{S,N} \approx P_{S,N=1}\left(\frac{1}{2N^2} \dots \frac{1}{N^3}\right)$$

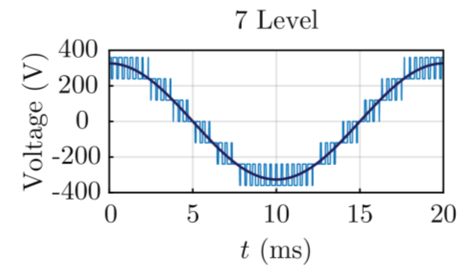


- High Efficiency @ High Effective Switching Frequency → High Power Density

Series Interleaving – Example #1

- ***Realization of a 99%++ Efficient 10kW 3-Φ 400V$_{rms,ll}$ Inverter System***
- ***7-Level Hybrid Active NPC Topology / LV Si-Technology***

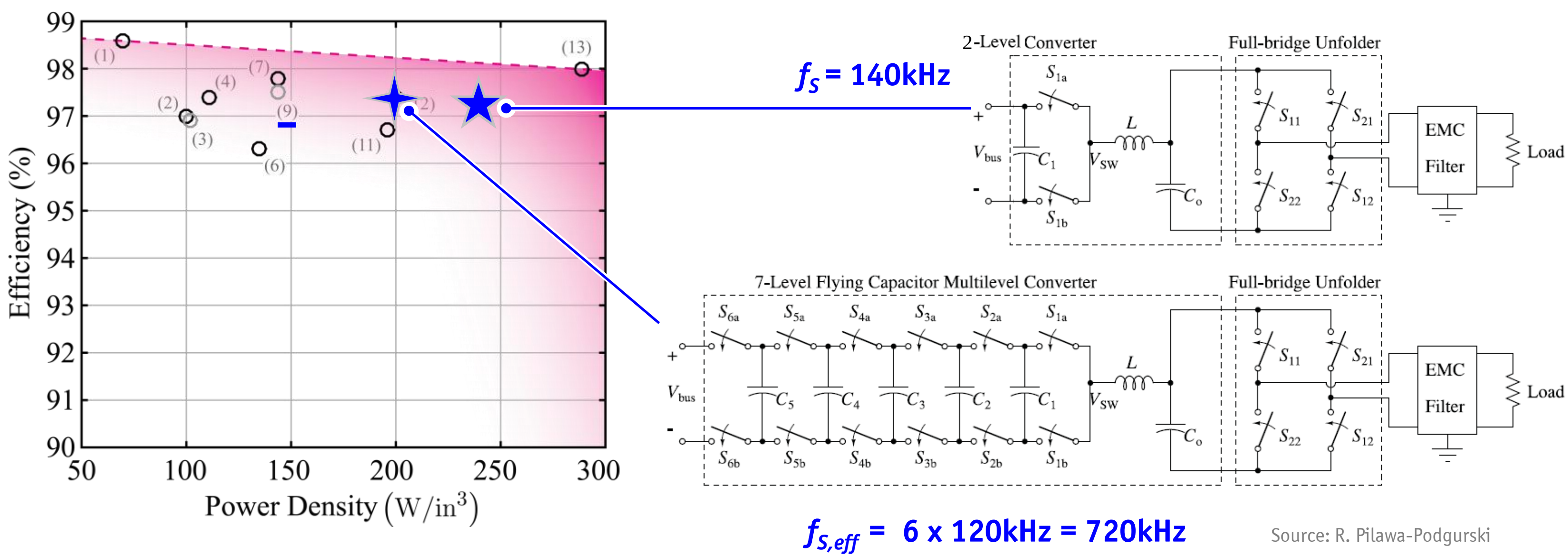




99.35%
2.6kW/kg
56 W/in^3

Series Interleaving – Example #2

- *Example of Google Little Box Challenge*
- Target: *2kW 1-Φ Solar Inverter with Worldwide Highest Power Density*
- *Comparative Analysis of Approaches of the Finalists*



Source: R. Pilawa-Podgurski

- *3D-Packaging / Integration Highly Crucial for Utilizing Multi-Level Advantages (!)*

Series Interleaving – Example #2

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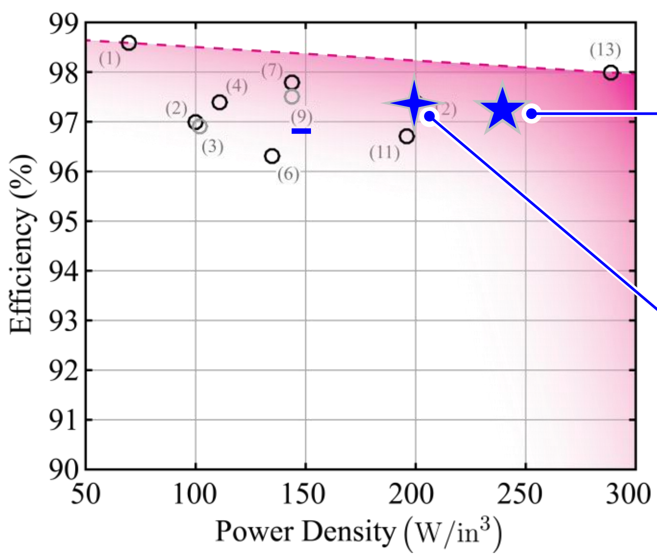
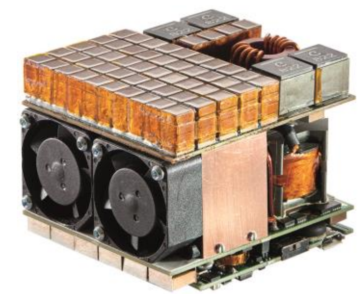
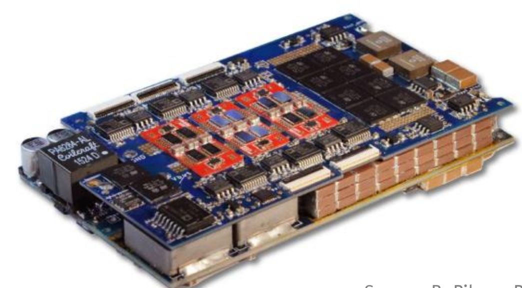


ETH zürich
Little-Box 2.0
240 W/in^3
97.4%



ILLINOIS
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

215 W/in^3
97,6%

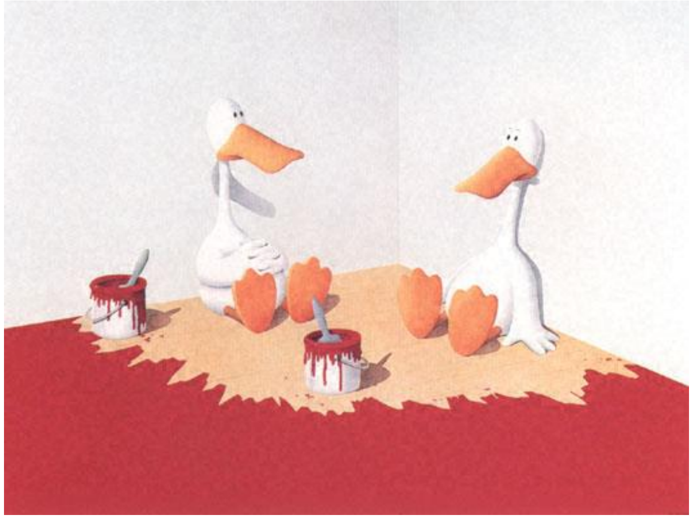


Source: R. Pilawa-Podgurski

- *3D-Packaging / Integration Highly Crucial for Utilizing Multi-Level Advantages (!)*

Observation

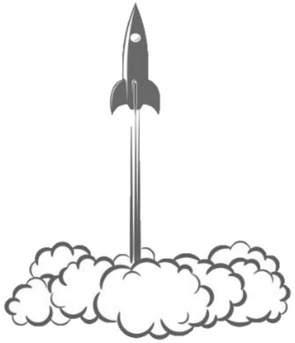
Efficiency



Power Density

** Conventional Packaging * → Very Limited Room for Performance Improvement (!)*

X-Technology **#3**

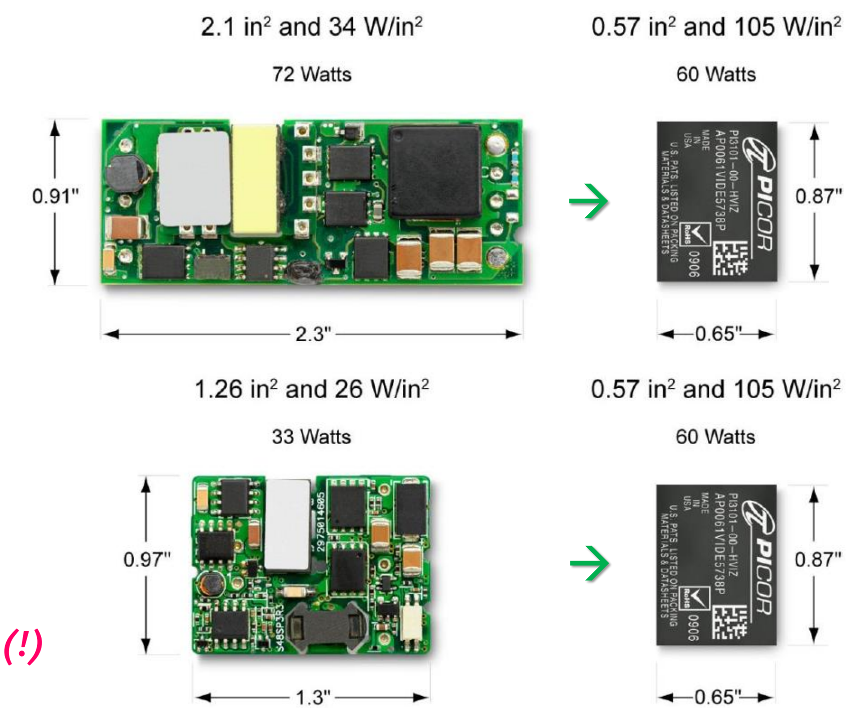


3D-Packaging
Automated Manufacturing

3D-Packaging / Heterogeneous Integration

- System in Package (SiP) Approach
- Minim. of Parasitic Inductances / EMI Shielding / Integr. Thermal Management
- Very High Power Density (No Bond Wires / Solder / Thermal Paste)
- Automated Manufacturing

Source: VICOR



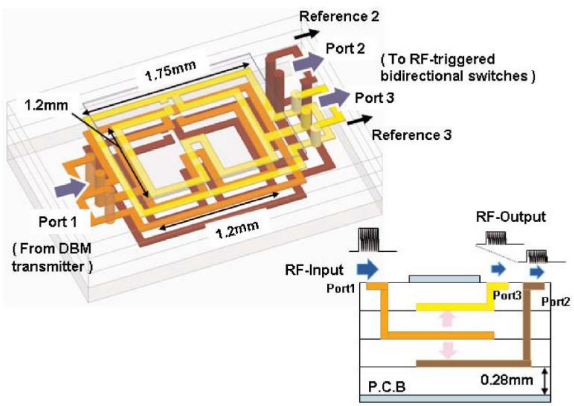
- Future Application Up to 100kW (!)
- New Design Tools & Measurement Systems (!)

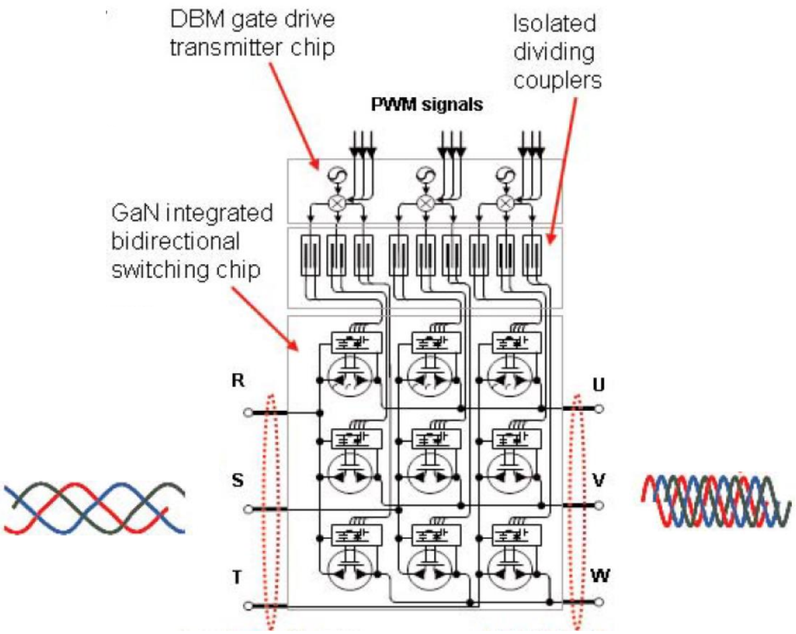
Monolithic 3D-Integration

Source: Panasonic ISSCC 2014

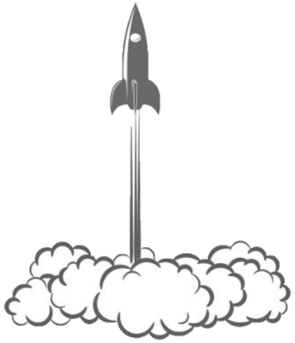
- GaN 3x3 Matrix Converter Chipset with Drive-By-Microwave (DBM) Technology
  - 9 Dual-Gate GaN AC-Switches
  - DBM Gate Drive Transmitter Chip & Isolating Couplers
  - Ultra Compact → 25 x 18 mm² (600V, 10A – 5kW Motor)

5.0GHz Isolated (5kVDC) Dividing Coupler





X-Technology #4

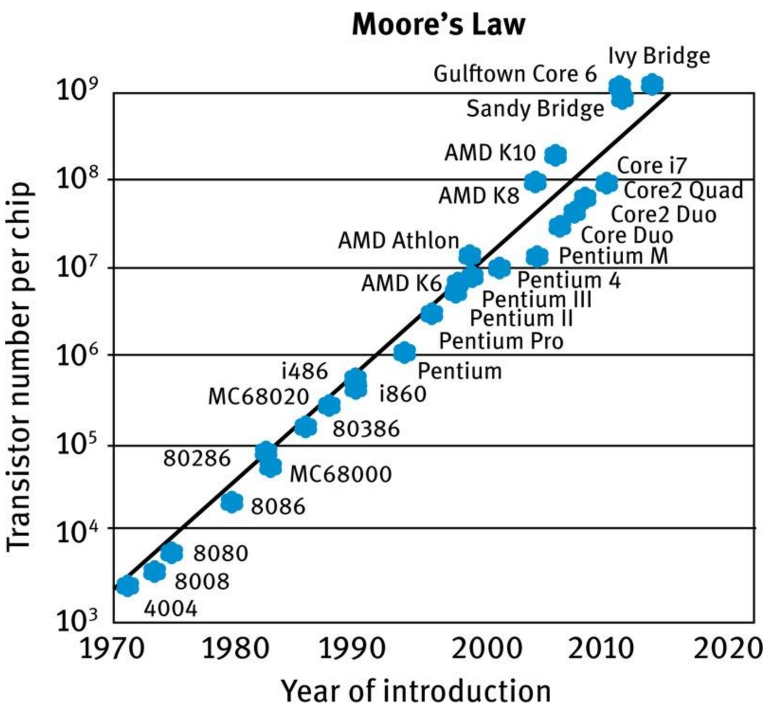


Automated Design
Digital Twin / Industry 4.0

Digital Integrated Circuits

- *Exponentially Improving uC / Storage Technology (!)*

— *Extreme Levels of Density / Processing Speed*
— *Software Defined Functions / Flexibility*
— *Cont. Relative Cost Reduction*



Source: Ostendorf & König /DeGruyter

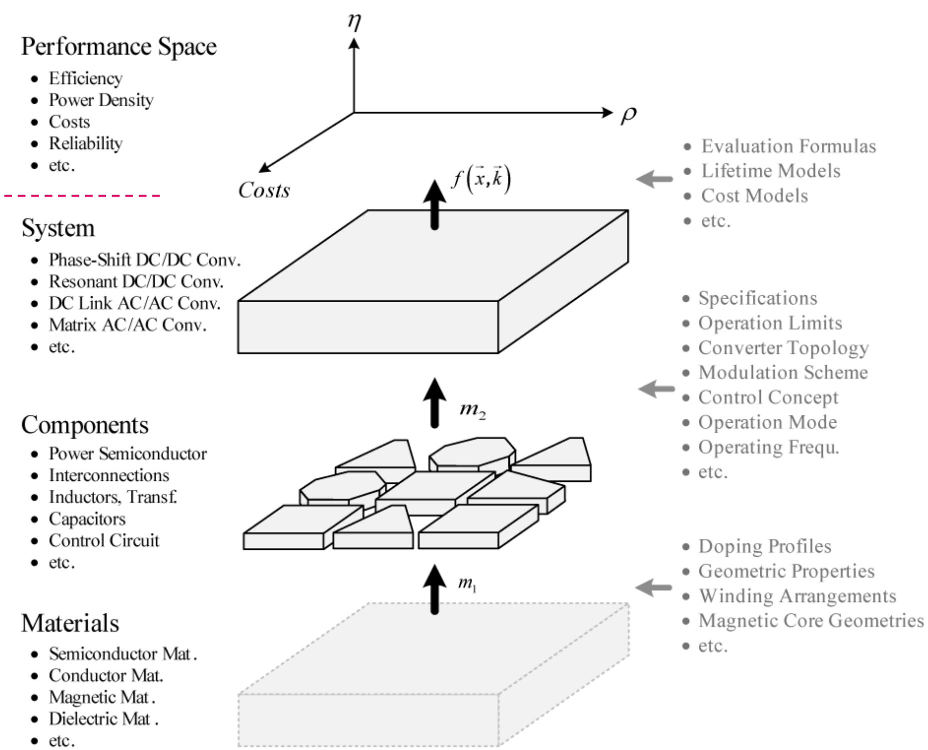
- *Fully Digital Control of Complex Systems*
- *Massive Computational Power → Fully Automated Design & Manufacturing / Industrial IoT (IIoT)*

Automated Design

Automated Design (1)

Performance Space

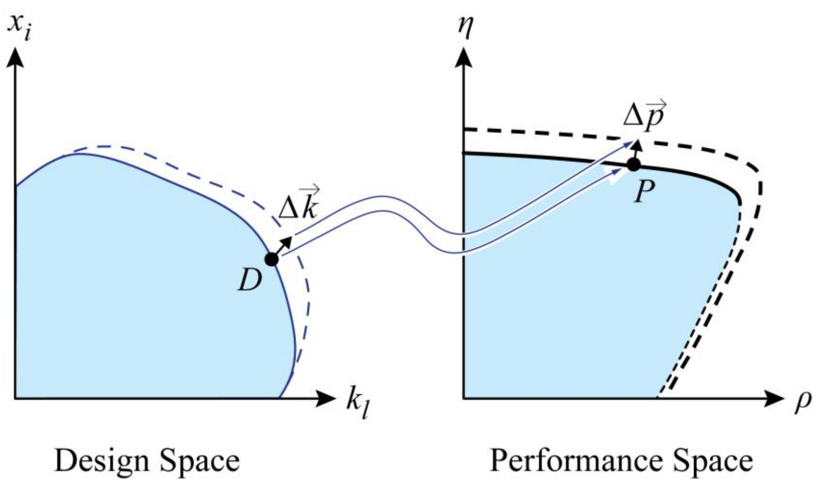
Design Space

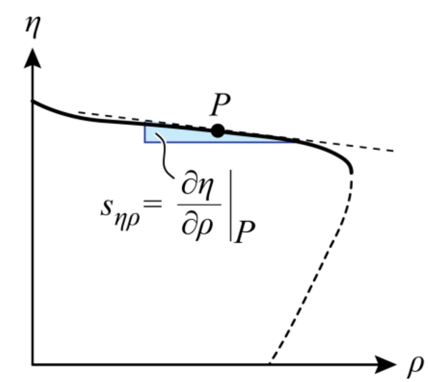


- *Mathematical Description of the Mapping* *"Technologies" → "System Performance"*

Automated Design (2)

- *Based on Mathematical Model of the Technology Mapping*
- *Multi-Objective Optimization → Best Utilization of the "Design Space"*
- *Identifies Absolute Performance Limits → Pareto Front / Surface*





- Clarifies *Sensitivity $\Delta\vec{p}\,/\,\Delta\vec{k}$* to Improvements of Technologies
- *Trade-Off Analysis*

Automated Design Roadmap

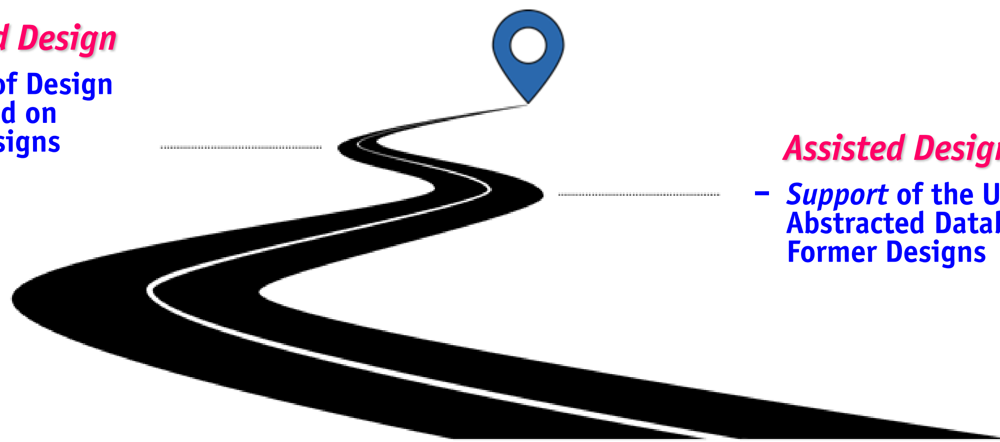
- *End-to-End Horizon of Modeling & Simulation*
- *Design for Cost / Volume / Efficiency Target / Manufacturing / Testing / Reliability / Recycling*

Autonomous Design → Design 4.0
– *Independent* Generation of Full Designs for Final Expert Judgement

Augmented Design
– *Suggestion* of Design Details Based on Previous Designs

Assisted Design
– *Support* of the User with Abstracted Database of Former Designs

State-of-the-Art
– *User Defined* Models and Simulation / Fragmented

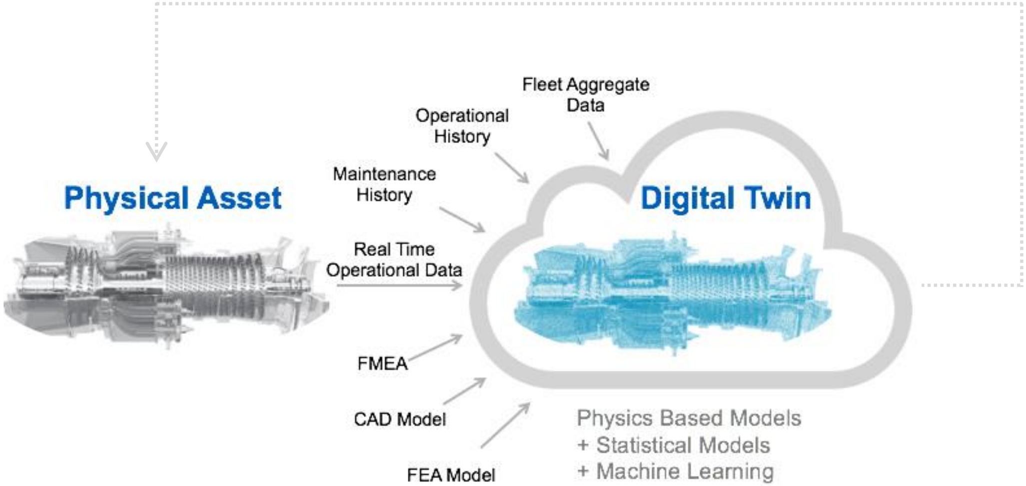


- *AI-Based Summaries → No Other Way to Survive in a World of Exp. Increasing # of Publications (!)*

Digital Twin / Industry 4.0

IIoT in Power Electronics

- *Digital Twin → Physics-Based Digital Mirror Image*
- *Digital Thread → "Weaving" Real/Physical & Virtual World Together*



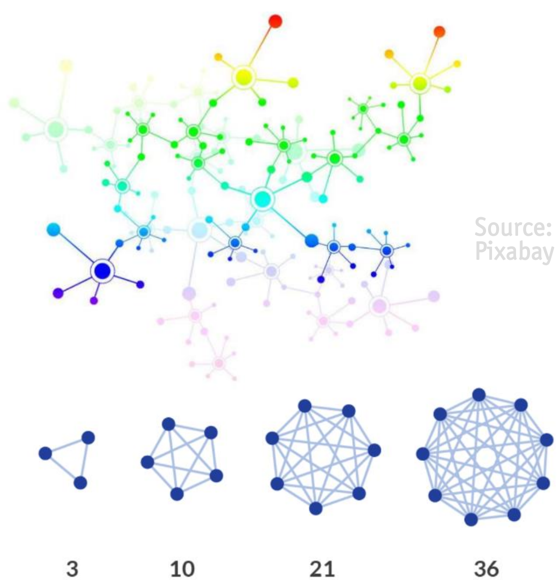
Source: www.railwayage.com

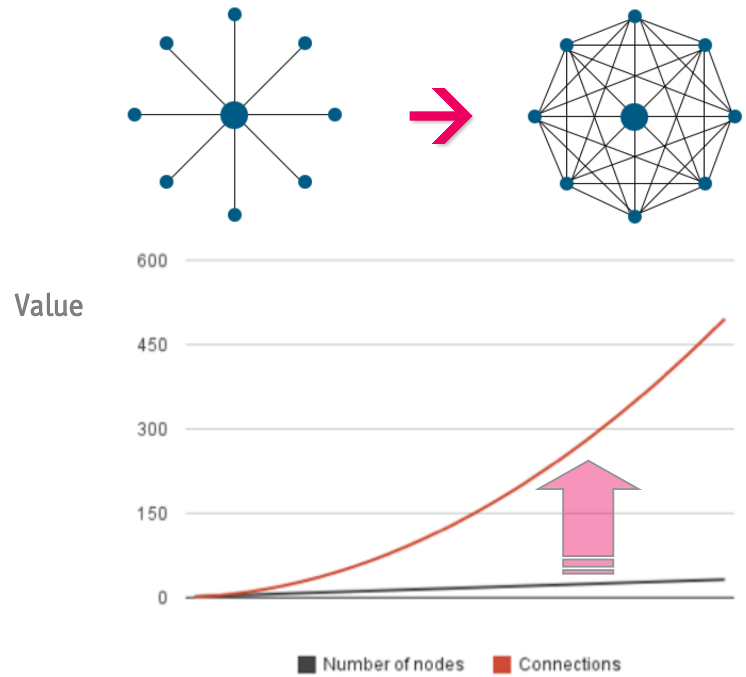
- *Model of System´s Past/Current/Future State → Design Corrections / Prev. Maintenance etc.*

Scaling Law of Digitalization

- **Metcalfe's Law**

  – *Moving from Hub-Based Concept to Community Concept Increases Value Exponentially (~n(n-1) or ~n log(n))*





- *Automated Design / Digital Control / Digital Twin / Industry 4.0*

Conclusions

Topologies → Technologies

- *Only Incremental Improvements from Topologies / Control Methods etc.*
- *Consider Converters like "ICs"*

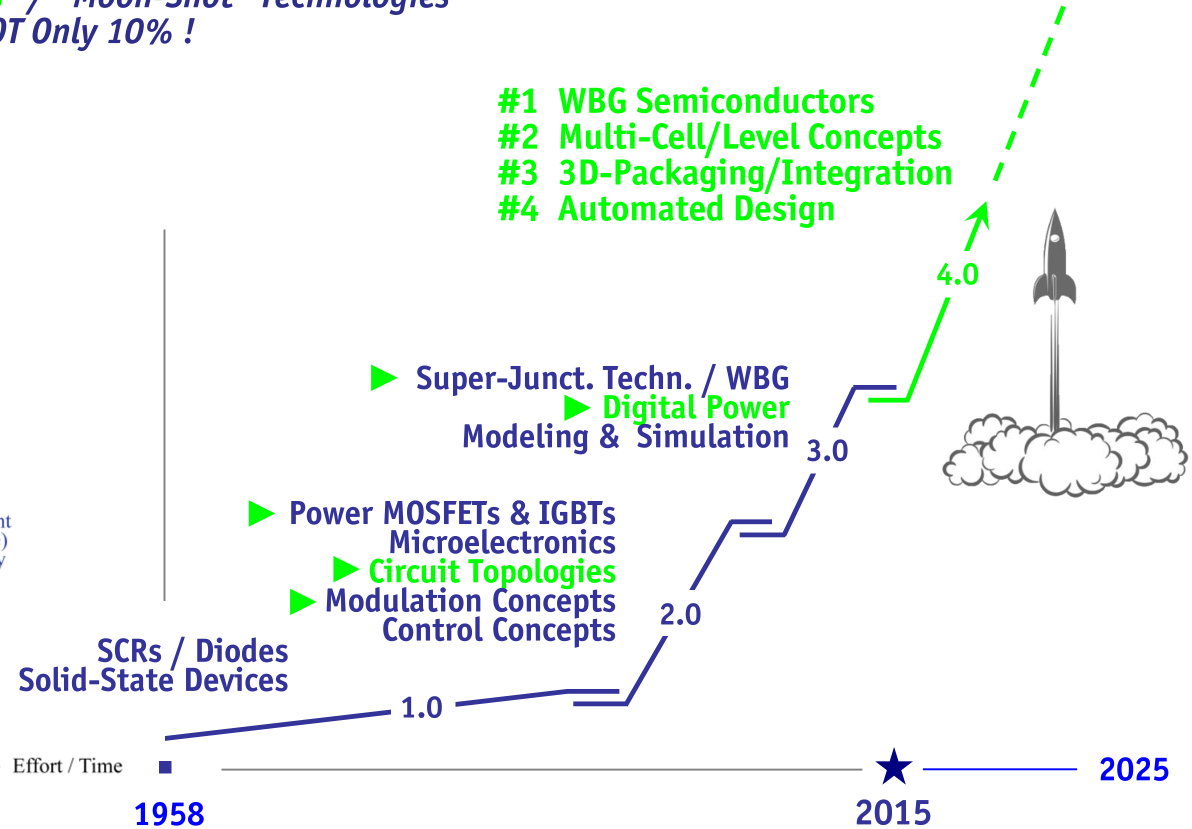
Shift to New Paradigm !

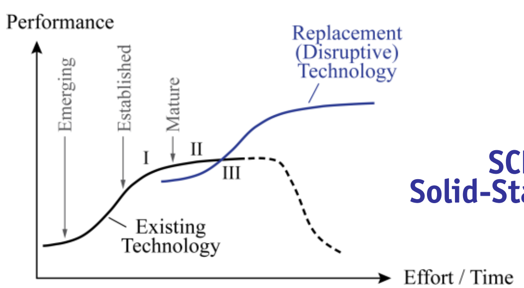
— *New Textbooks*
— *New Design Tools*
— *New Manufacturing Processes*
— *New Measurement / Testing Devices*

- *University Research → Technology Partnership OR "Fab-Less" Power Electronics*

S-Curve of Power Electronics

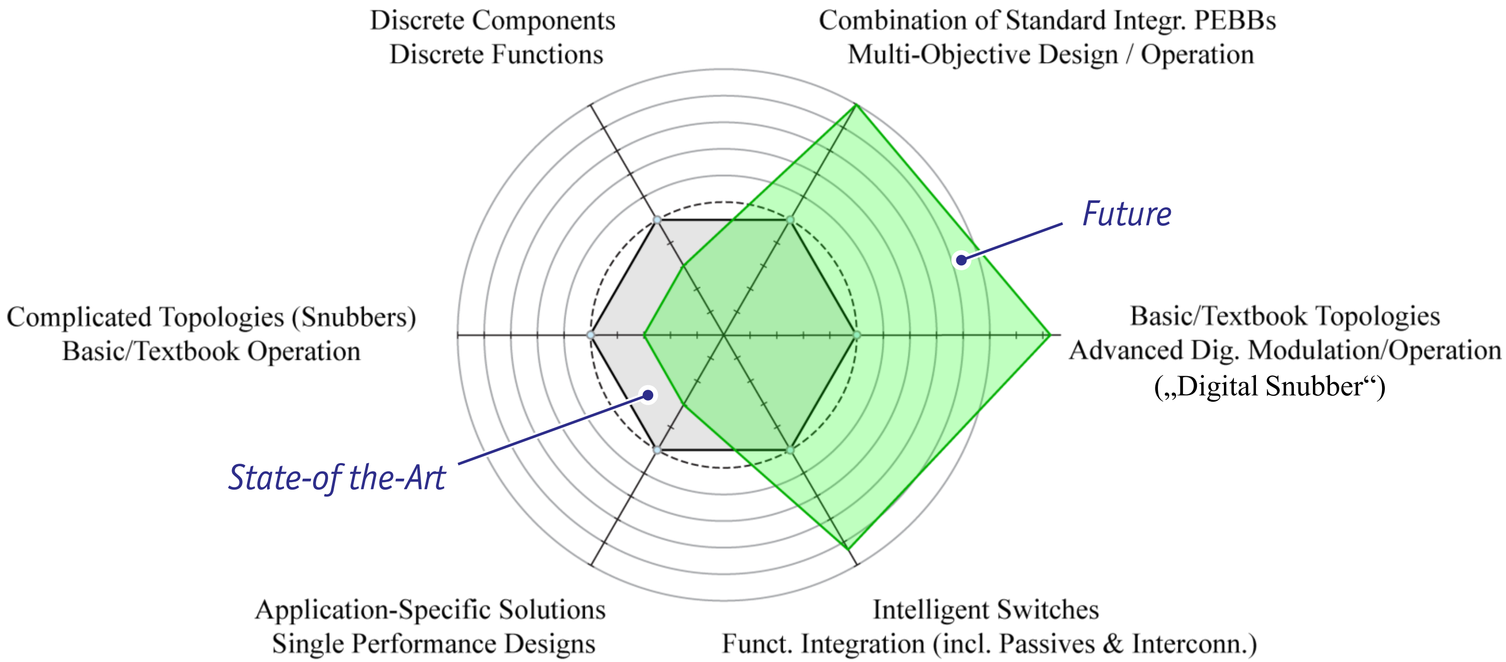
- *Power Electronics 1.0 → Power Electronics 4.0*
- *Identify "X-Concepts" / "Moon-Shot" Technologies*
- *10x Improvement NOT Only 10% !*





Future Standardization / Integration

- *Complicated → Basic/Standardized*
- *Discrete → Integrated*
- *Single-Obj. → Multi-Objective*



- *Main Driver → Cost Minimization by Automated High-Volume Manufacturing*
- *Main Enabler → Computer-Based Design Providing Insight & Digital Control for Flexibility*

Thank you!