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Detailed Analysis and Design of a Three-Phase Phase-Modular Isolated Matrix-Type PFC Rectifier

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***Abstract*—Phase-modular isolated PFC rectifiers are an interesting alternative to phase-integrated three-phase rectifiers. The use of a matrix-type converter allows to achieve isolation with a single-stage energy conversion. This paper presents a phase-modular isolated matrix-type rectifier, which can be connected to the mains either in star (Y) or delta (Δ), enabling a wide input voltage range. A detailed analysis of the operating principles and switching behavior of the converter is presented. Then, the design of the active and passive components is discussed considering a 7.5 kW, 400 V output voltage system. Different implementation alternatives are evaluated regarding efficiency and realization effort.**

I. Introduction

In today's power electronic systems, which are powered from the three phase mains, rectifier systems with an active PFC are indispensable in order to comply with directives which specify a maximum level of the noise injected back into the mains [1], [2]. Depending on the underlying application, a galvanic isolation or adaption of the output voltage is needed, which is typically realized with an additional DC/DC-converter. The major disadvantages of this converter cascading are the reduction of the overall efficiency, the large component count and the increasing control complexity. The use of three-phase matrix-type isolated PFC rectifiers has been already proposed as an alternative for single-stage conversion [3]–[6]. In comparison to the conventional two-stage PFC converter systems, the proposed phase-modular indirect matrix-type PFC rectifier system, which can be connected to the mains either in star (Y) or delta (Δ) – enabling a wide input voltage range (IMY/Δ-rectifier) – can perform the PFC functionality and the galvanic isolation in a single-stage (cf. **Fig. 1**).

Due to the phase-modularity of the IMY/Δ-rectifier, according to single-phase rectifier systems, to each phase module only the phase voltage and not the phase-to-phase voltage is applied [7], [8]. Thus, semiconductor devices with a blocking voltage of 600 V can be used, which feature a lower on-state resistance and better switching performance compared to 1200 V-devices, hence leading to even higher efficiency. The phase module, consisting of an input diode rectifier and a full bridge, is basically an indirect single-phase matrix converter and converts the low frequency mains input voltage to a high frequency AC voltage [9]. As already presented in [10], the IMY/Δ-rectifier's full bridges can be controlled with a simple phase-shift modulation where each bridge leg is switched with 50% duty cycle, thus reducing the control complexity compared to conventional two-stage PFC converter system. Furthermore, since the IMY/Δ-rectifier is a buck-type PFC rectifier and due to the missing DC-link capacitors (only a small DC-link capacitor C_{dc} is needed for each phase module during the commutation interval), on the one hand, the inrush currents at startup are strongly reduced since only the input filter capacitors have to be charged. On the other hand, with a buck-type topology the voltage level can be slowly ramped up to the desired output voltage with the ability to operate the converter with output current limitation, thus also providing an inherent short-circuit protection.

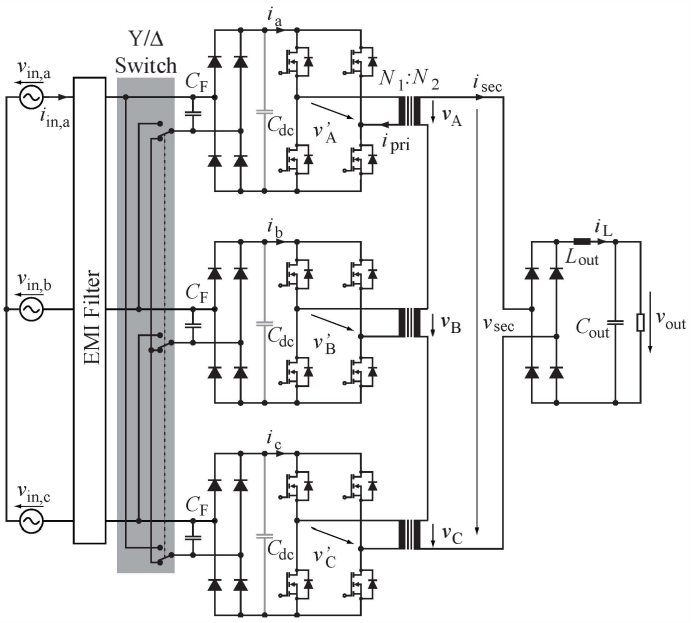

Fig. 1 Circuit diagram of the three-phase phase-modular isolated matrix-type PFC Y/Δ-Rectifier (IMY/Δ-Rectifier).

In this paper a comprehensive analysis of the basic operation, the design and limits of the proposed phase-modular indirect matrix-type PFC rectifier system (IMY/Δ-rectifier) is given.

In **Section II** the basic operation of the IMY/Δ-rectifier is explained. Based on this analysis and the given specifications of **Table I**, in **Section III** the design of a 7.5 kW converter prototype is performed. The selection of the input and output diodes, the switches of the full bridge converters, the design of the input EMI filter and of the output filter are included in this section. The built prototype is finally described in **Section IV**.

TABLE I Electrical specifications of the IMY/Δ-rectifier.

Parameter	Value
Mains voltage, nominal (rms,phase)	230 V
Mains voltage, min-max (rms,phase)	185...306 V
Mains frequency	50 Hz
Output DC voltage	400 V
Nominal power	7.5 kW
Switching frequency	72 kHz

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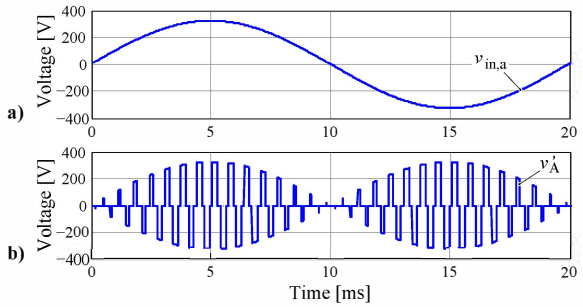

Fig. 2 Schematic waveform of **a)** the phase input voltage $v_{\mathrm{in,a}}$ and **b)** the output voltage v'_{A} of the full bridge of phase A applied to the corresponding single-phase transformer.

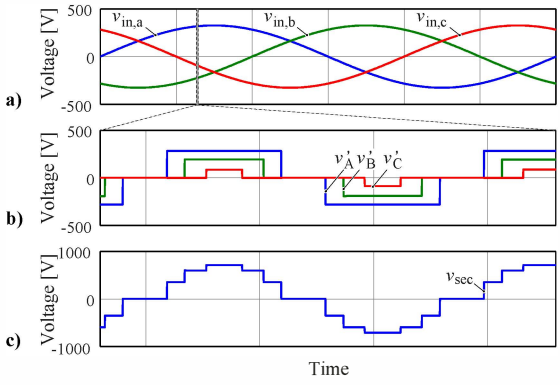

Fig. 3 Schematic waveform of **a)** the phase input voltages $v_{\mathrm{in,a}}$, $v_{\mathrm{in,b}}$ and $v_{\mathrm{in,c}}$, **b)** the resulting output voltage of the full bridge v'_{A}, v'_{B} and v'_{C} if the symmetric modulation scheme is applied and **c)** the resulting output voltage v_{sec} which is the sum of all three secondary voltages v_{A}, v_{B} and v_{C}.

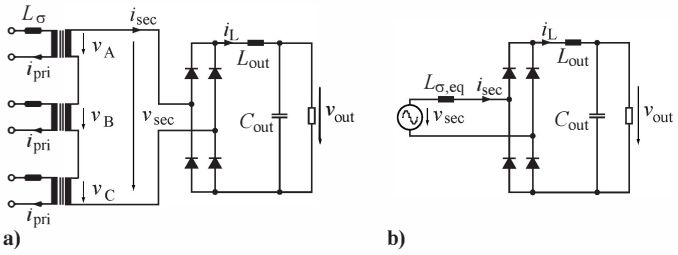

Fig. 4 a) Circuit diagram of the IMY/Δ-rectifier's secondary and **b)** its equivalent circuit which basically is a buck-type converter with input voltage v_{sec}.

II. Principle of Operation

The circuit diagram of the proposed phase-modular indirect matrix-type PFC rectifier system (IMY/Δ-rectifier) is shown in **Fig. 1**. As can be noticed, the IMY/Δ-rectifier features a phase-modular structure, whereat each phase module consists of a input diode rectifier and a full bridge. According to single-phase rectifiers, where only the phase-to-neutral instead of the phase-to-phase voltage is processed, 600 V-devices instead of 1200 V-devices can be used in each phase module, which typically have a lower on-state resistance and show an improved switching behavior compared to 1200 V-devices. Thus, lower overall semiconductor losses can be achieved. In addition, depending on the input voltage range, the voltage applied to the phase modules can be adjusted by connecting the IMY/Δ-rectifier either in star or in delta connection to the mains. With an additional relay the IMY/Δ-rectifier can automatically change the type of connection to the mains (cf. **Fig. 1**). In case of a low input voltage, the delta connection is selected in order to apply a higher voltage to each phase module and thus decreasing the input current and the overall conduction losses. Basically, each phase module is an indirect single-phase matrix converter that converts the low frequency mains input voltage to a high frequency AC voltage (**Fig. 2**). As described in [10], each phase module is controlled with a simple phase shift modulation where each bridge leg is switched with a 50% duty cycle, resulting in the high-frequency waveform shown in **Fig. 2 b)**. In order to enable a galvanic isolation, each phase module applies this high frequency AC voltage directly to an individual single-phase transformer.

On the secondary side, the windings of the three single-phase transformers are directly connected in series, thus the output voltages of the individual transformers is summed up. Based on the proposed modulation scheme in [10], where the duty cycle or phase shift respectively is proportional to the corresponding rectified input voltage, a staircase shaped output voltage is generated as shown in **Fig. 3**. Due to the 120° phase displacement between the input voltages $v_{\mathrm{in,a}}$, $v_{\mathrm{in,b}}$ and $v_{\mathrm{in,c}}$ the fundamental component of the secondary voltage v_{sec} shows a constant magnitude over the whole mains period as described in [10]. This high frequency voltage is then rectified by the output diode bridge and filtered by the output inductor L_{out} and capacitor C_{out} in order to provide a constant output voltage v_{out}. Actually, the resulting output voltage v_{out} is equal to the average value of v_{sec},

$$v_{\mathrm{out}} = \overline{|v_{\mathrm{sec}}|} = \frac{3}{2} M \frac{N_2}{N_1} \hat{v}_{\mathrm{in}}. \tag{1}$$

By only considering the secondary part of the IMY/Δ-rectifier where v_{sec} is the input voltage of this circuit (cf. **Fig. 4**), it can be noticed that the IMY/Δ-rectifier has the same structures as a conventional DC/DC buck converter. Consequently, the IMY/Δ-rectifier can be controlled with the same duty cycle M, where

$$M = \frac{2}{3} \frac{N_1}{N_2} \frac{v_{\mathrm{out}}}{\hat{v}_{\mathrm{in}}}, \tag{2}$$

and the same simple control scheme (cascaded control of output current i_{L} and output voltage v_{out}) as can be used for the conventional buck converter.

Assuming a large output inductor L_{out}, the output current i_{L} is almost constant. The same current is also flowing through all secondary windings of the transformers, with the only difference that the current through the secondary windings has a rectangular shape which is then rectified by the output diode bridge. Based on Ampere's law and assuming a large magnetizing inductance, the current in the primary as well as in the full bridge has also a rectangular shape with constant magnitude $\hat{i}_{\mathrm{pri}}$, which is given by the transformer's winding ratio $\frac{N_1}{N_2}$, $\hat{i}_{\mathrm{pri}} = \frac{N_2}{N_1} \hat{i}_{\mathrm{sec}} = \frac{N_2}{N_1} i_{\mathrm{L}}$.

Hence, in order to achieve sinusoidal input currents $i_{\mathrm{in,a}}$, $i_{\mathrm{in,b}}$ and $i_{\mathrm{in,c}}$, which are in phase with the corresponding phase voltages $v_{\mathrm{in,a}}$, $v_{\mathrm{in,b}}$ and $v_{\mathrm{in,c}}$ - thus achieving the required PFC operation - the constant current has to be pulse-width modulated sinusoidally, which means that the duty cycle is proportional to the actual input current or voltage value respectively. The resulting voltages v'_{A}, v'_{B} and v'_{C} which are applied to the primary of each single-phase transformer are shown in **Fig. 3 b)**. As can be noticed, based on the modulation scheme proposed in [10], the duty cycles of the three individual phase modules are synchronized in such a way that the resulting output voltages are symmetrically distributed.

For the sake of completeness, it has to be mentioned that it is also possible to slightly shift the input current out of phase with the input voltage in order to enable reactive power compensation.

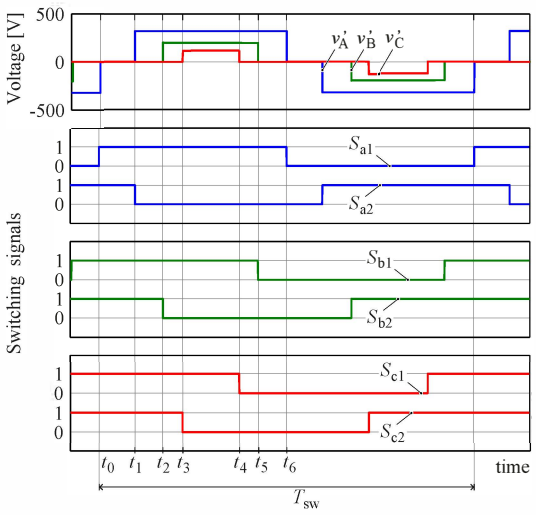

Fig. 5 Resulting voltages v'_A, v'_B and v'_C, which are applied to the individual single-phase transformers and corresponding control signals of the three full bridges for the case $v_{in,a} > v_{in,b} > v_{in,c}$.

III. Converter Design

In order to be able to properly design the IMY/Δ-rectifier with respect to the specifications given in **Table I** and to perform an accurate loss analysis, first the switching behavior of the full bridge of a phase during each switching transition has to be analyzed.

A. Full bridge converter switches

As already mentioned, the bridge legs of each full bridge are switched with a 50 % duty cycle whereat the phase current and the resulting output voltage of the full bridge v'_A, v'_B and v'_C are controlled with the phase shift between the two bridge legs. The control signals of the switches for the three full bridges and the resulting output voltages are illustrated in **Fig. 5** for the case $v_{in,a} > v_{in,b} > v_{in,c}$.

Remark: during the intervals where at least from one of the three full bridges a voltage is applied to the corresponding single-phase transformer, i.e. the full bridge is turned on, the output current impressed by the large output inductor L_{out} is flowing through the secondary windings of all three transformers which are connected in series; accordingly, current is flowing also through the other full bridges, independently of their switching states.

At the beginning of the switching period t_0 the full bridge with the largest input voltage is turned off and all phase modules are now in a freewheeling state, thus no voltage is applied to any transformer's primary winding (cf. **Fig. 6 a**)). Since before that time instant ($t < t_0$) the full bridge with the largest input voltage was conducting the negative load current ($i_{sec} = -i_L$) and the fact that the secondary windings are connected in series, the same negative load current was also flowing through the other full bridges even if they were already in the freewheeling state. If it is assumed that each transformer has a certain leakage inductance L_σ, during the time interval $t_0 - t_1$, the leakage inductances L_σ still force the negative load current to freewheel through the high-side switches S_{1p} and S_{2p} of all full bridges. The corresponding current path during the time interval $t_0 - t_1$ is shown in **Fig. 6 a)** for one full bridge.

At the time instant t_1, the switch S_{2p} of the phase module with the largest input voltage is turned off. Due to the leakage inductance L_σ the current in the primary continues to flow in the same direction, thus the parasitic output capacitance of S_{2p} is charged and the output capacitance of S_{2n} discharges until the current can flow through

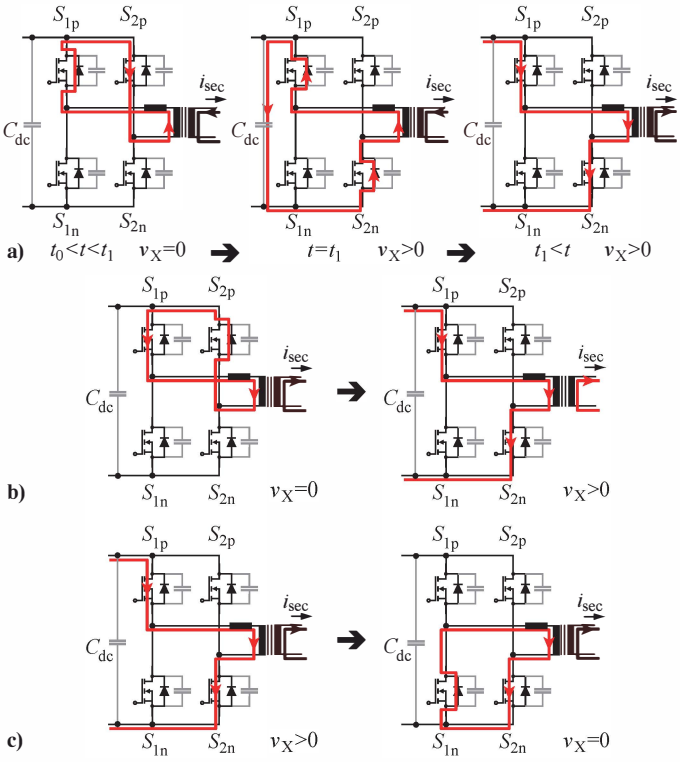

Fig. 6 Current path at different switching transitions: **a)** switching transition at t_1, when the first full bridge is switched from freewheeling to a positive output voltage, **b)** during turn on transitions at t_2 and t_3, when the second and third full bridge are turned on, and **c)** during turn off transitions at t_4, t_5 and t_6, when the full bridges return to the freewheeling state.

the anti-parallel diode of S_{2n} and the small DC-link capacitor (cf. **Fig. 6 a**)). It has to be noticed that the energy stored in the leakage inductance has to be large enough to charge/discharge the output capacitances of the bridge leg. After this commutation, S_{2n} is turned on at zero voltage (ZVS). In addition, the positive input voltage is now fully applied to the leakage inductance L_σ of the transformer, resulting in an almost linear increase of the primary current where the current changes its sign until the positive load current ($i_{sec} = i_L$) is reached.

This can be easily explained with the simplified circuit diagram shown in **Fig. 7**. Before t_1, when $v_{sec} = 0$ V, the current is flowing in negative direction through the leakage inductance $L_{\sigma,eq}$ and the output diodes D_{1n} and D_{2p} (cf. **Fig. 7 a**)). At $t = t_1$, v_{sec} changes to a positive voltage which forces D_{1p} into conduction and then occurs across the leakage inductance $L_{\sigma,eq}$, since the output diode D_{2p} is still conducting, and thus clamps the negative terminal B of v_{sec} to the positive terminal A' of the output rectifier (cf. **Fig. 7 b**)).

Due to the relatively small leakage inductance L_σ, the current rapidly decreases and changes its sign until the load current i_L is flowing in positive direction through the primary and secondary winding of the transformer (cf. **Fig. 7 c**)). Consequently, with the described transition at t_1 and the series connection of the secondary windings, the current direction is also changing in the other phase modules which are still in the freewheeling state (cf. **Fig. 6 b**), left).

At the time instant t_2, the phase module with the second highest input voltage applies a positive voltage to the corresponding transformer by switching on S_{2n}. Since the current has changed its sign already at t_1, during the switching transition at t_2, the current is forced to

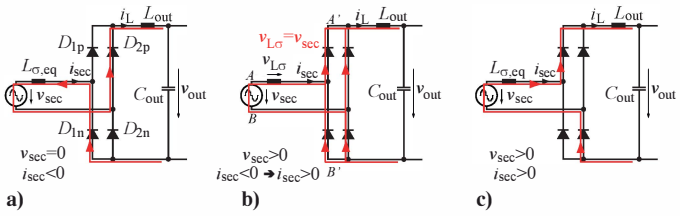

Fig. 7 Equivalent buck-type circuit of the secondary side of the IMY/Δ-Rectifier with the current path **a)** before t_1, when the full bridge is in freewheeling state, **b)** during the switching transition at t_1, when voltage is applied to the leakage inductance and **c)** after t_1, when the current has changed its direction.

commutate from the anti-parallel diode of S_{2p} to the MOSFET S_{2n}, resulting in hard switching with typically high reverse recovery losses (cf. **Fig. 6 b)**). The same hard switching transition occurs also at the time instant t_3, when the phase module with the lowest input voltage is turned on to a positive voltage.

At t_4, t_5 and t_6 the phase modules are again switched off back to the freewheeling state in reverse order, starting with the phase module having the lowest input voltage applied. During these transitions S_{1p} is turned off, thus the current impressed by the leakage inductance L_σ charges/discharges the parasitic output capacitance of the bridge leg until the anti-parallel diode of S_{1n} is conducting; accordingly, the MOSFETs S_{1n} of all three full bridges can be turned on at zero voltage (cf. **Fig. 6 c)**). After t_6 all phase modules are back again in the freewheeling state and the same kind of transitions as described above will take place in the second half of the switching period, when negative voltages are applied to the transformers. In summary, hard switching occurs always during the transition from freewheeling to an active state, but only in the two phase modules which do not block the maximum input voltage within the considered switching interval. In all other switching transitions ZVS is achieved.

Due to the hard switching transitions in the full bridge, MOSFETs with a low reverse recovery charge Q_{rr}, e.g. the CFD2-CoolMOS series from Infineon, have to be used in order to keep the switching losses reasonably low. Unfortunately, such MOSFETs typically feature a higher on-state resistances $R_{ds,on}$ – e.g. compared to MOSFETs of the C7-CoolMOS series (also from Infineon); for example, the on-state resistance $R_{ds,on}$ of the CFD2-MOSFET is approximately two times larger - thus leading to higher conduction losses which also represent a substantial share of the total converter losses as will be explained later.

In order to keep the conduction losses also with the CFD2-CoolMOS low, several MOSFET devices could be connected in parallel. At the same time, however, the reverse recovery charge is proportionally increased with the number of parallel MOSFETs and thus, even if the current per device is lowered, a higher total reverse recovery charge results in higher switching losses. In addition, also the output capacitance is increased linearly, which means that more energy has to be stored in the leakage inductance in order to charge/discharge the output capacitance during the switching transitions and to still achieve soft switching.

Another option to almost avoid any switching losses is to use Si-MOSFET devices in an OR-ing configuration as shown in **Fig. 8**. The series connected Schottky diode D_S prevents the body diode of the Si-MOSFET to conduct current (reverse recovery losses in the body diode are thus avoided), while the anti-parallel silicon carbide (SiC) diode D_P is conducting the current in negative direction through the OR-ing configuration. Consequently, the reverse recovery behavior

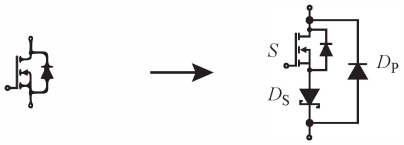

Fig. 8 MOSFETs with high reverse recovery charge can be used in an OR-ing configuration with series connected Schottky diode D_S and anti-parallel SiC-diode D_P to prevent high reverse recovery losses.

of the MOSFET's body diode is no more crucial, and instead of the CFD2-CoolMOS now the C7-CoolMOS with lower on-state resistance $R_{ds,on}$ can be used resulting in lower conduction losses. However, the additional conduction losses of the series connected low voltage Schottky diode D_S during turn-on, which are typically small due to the low forward voltage drop of Schottky diodes, and the higher conduction losses of the SiC-diode compared to the MOSFET internal parasitic Si-diode during the freewheeling interval have to be taken into account.

As an alternative to Si-MOSFETs, the utilization of semiconductor devices based on new technologies like SiC-MOSFETs or GaN-transistors would be possible. However, on the one hand SiC-MOSFETs are only available with voltage ratings of 1200 V (CMF20120D, 105 mΩ at $T_j = 150\,°C$, CREE), where the best state of the art products show around three times higher on-state resistances compared to the C7-CoolMOS (IPW65R019C7, 40 mΩ at $T_j = 150\,°C$, Infineon) and on the other hand, 600 V GaN-transistors are not commercially available yet.

As proposed in [10], the control signals of each full bridge are synchronized to each other in such a way that the voltages applied to transformers (v_A, v_B and v_C) are symmetrically distributed, resulting in a symmetric secondary voltage v_{sec} (symmetric modulation). As described above, however, in the first turn on switching transition of the full bridge with the largest input voltage at t_1 - switching from freewheeling state to either a positive or negative voltage - the current direction is changed in all full bridges due to the series connection of the secondary windings, thus resulting in hard switching during the turn on transition of the other two full bridges (cf. **Fig. 6 b)**). In order to avoid these hard switching transitions, the modulation scheme can be modified in such a way that the control signals of the individual full bridges are synchronized to each other with respect to simultaneous turn on transitions, which results in an asymmetric secondary voltage v_{sec} (asymmetric modulation) as shown in **Fig. 9**. Consequently, the freewheeling current impressed by the leakage inductances L_σ will simultaneously charge/discharge the output capacitances of the bridge legs in all three full bridges, thus in each phase module ZVS is achieved during turn on. The turn off transitions are not affected by this modification. It has to be mentioned, that even if the shape of secondary voltage v_{sec} is changed, the output current ripple in the output inductor L_{out} is hardly changed, since the voltage time integral applied to L_{out} stays the same.

With this modified modulation scheme the above stated OR-ing configuration wouldn't be needed anymore and the C7-CoolMOS with low on-state resistance $R_{ds,on}$ could be used, since now in all transitions ZVS is achieved, provided that the energy stored in the leakage inductance ($\hat{E}_{L_\sigma} = 1/2 L_\sigma \cdot \hat{i}^2_{pri}$) is high enough to fully charge/discharge all output capacitances during the simultaneous turn on transition. At low load conditions when the current through the transformer is small, however, the energy stored in the leakage inductance $\hat{E}_{L,\sigma}$ could be too low resulting in hard switching. Even if in that case the currents are low, the total converter losses could be considerably increased and under certain circumstances the MOSFETs

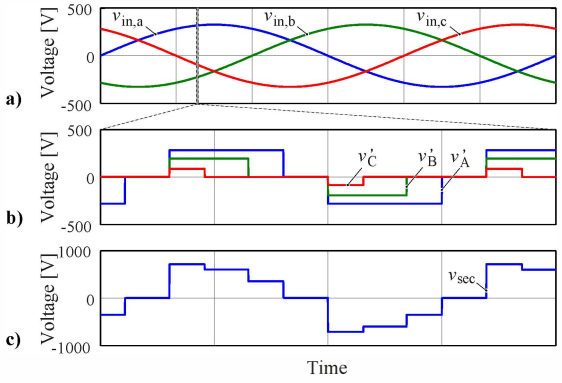

Fig. 9 Schematic waveform of **a)** the phase input voltages $v_{\mathrm{in,a}}$, $v_{\mathrm{in,b}}$ and $v_{\mathrm{in,c}}$, **b)** the resulting output voltage of the full bridge v'_{A}, v'_{B} and v'_{C} if the asymmetric modulation scheme is applied and **c)** the resulting output voltage v_{sec} which is the sum of all three secondary voltages v_{A}, v_{B} and v_{C}.

could be destroyed.

Therefore, the full bridges of the laboratory prototype are designed with MOSFETs of the C7-CoolMOS series in OR-ing configuration, with the possibility to short circuit the series connected Schottky diode and to experimentally compare the operation as well as the converter efficiency for the built OR-ing configuration with a conventional full bridge under soft switching condition.

B. Input and output diode rectifier

As already mentioned, due to the phase modularity of the IMY/Δ-rectifier, the voltage stress of all semiconductor devices of the phase modules is defined by the maximum magnitude of the mains phase-to-neutral voltage $\hat{v}_{\mathrm{in}}$ (cf. **Table I**). Thus, for the input rectifier bridges of the IMY/Δ-rectifier, which are just needed to rectify the low frequency input voltage, Si-diodes with a low forward voltage drop and with a blocking voltage of at least 600 V have to be selected.

The needed blocking voltage capability of the output diode bridge, which rectifies the high-frequency secondary voltage v_{sec}, is basically also given by $\hat{v}_{\mathrm{in}}$, however, the turns ratio of the transformer N_2/N_1 and the superposition of the voltages v_{A}, v_{B} and v_{C} has to be considered. The secondary voltage v_{sec} reaches its maximum when e.g. the input voltage of phase A reaches its maximum $v_{\mathrm{A}} = \hat{v}_{\mathrm{in}}$ and the other two phases B and C are at half the voltage $v_{\mathrm{B}} = v_{\mathrm{C}} = -\frac{1}{2}\hat{v}_{\mathrm{in}}$. Then, the maximum voltage can easily be calculated as $\hat{v}_{\mathrm{sec}} = 2 \cdot N_2/N_1 \cdot \hat{v}_{\mathrm{in,max}}$.

According to the switching behavior of the conventional DC/DC buck converter, due to the hard commutation of the diodes, the output diodes of the IMY/Δ-rectifier have to be realized either with SiC-diodes for secondary voltages higher than approximately 200 V or with Schottky diodes for voltages below this value.

As already described in detail, if one of the three full bridges is turned on, due to the series connection of the secondary windings the load current also has to flow through all primary windings and all full bridges independent of their switching state. Consequently, this results in high conduction losses in the IMY/Δ-rectifier, especially if the OR-ing configuration is used, since in the freewheeling state the current can't flow through the MOSFET but has to flow through the anti-parallel SiC-diode with its large forward voltage drop.

In order to be able to reduce the conduction losses in the primary side of the IMY/Δ-rectifier, the individual single-phase transformers could be decoupled, which could be achieved by extending the modular structure of the IMY/Δ-rectifier also to the secondary side by using

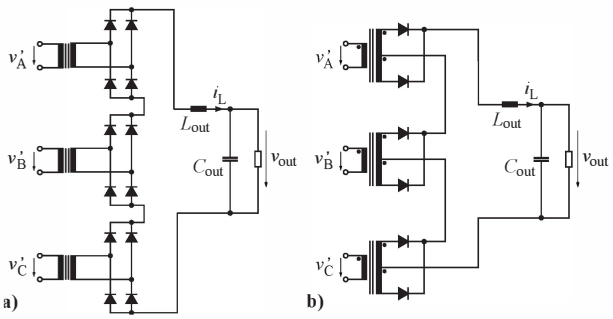

Fig. 10 Possible realization of the IMY/Δ-rectifier's secondary with **a)** either three separate full bridge output rectifiers or **b)** half bridge output rectifiers and transformers with center-tapped secondary windings.

three series connected individual output rectifiers (cf. **Fig. 10**). With this extension, during the freewheeling interval, the current in each full bridge can be forced to zero independently. Thus, the conduction losses in the primary side of the IMY/Δ-rectifier can be significantly reduced. Unfortunately, due to the missing freewheeling current during the turn on switching transition (from freewheeling state to either a positive or negative voltage) ZVS is lost. Although the turn on transition can be performed at zero current (ZCS), the stored energy in the MOSFET output capacitance is dissipated.

In addition, if the individual output rectifiers are realized as full wave rectifiers, the conduction losses are increasing, since now the load current is freewheeling through six instead of two diodes (cf. **Fig. 10 a**)). However, the output rectifiers can also be realized as half bridge rectifiers in combination with transformers having a center tapped secondary winding as shown in (cf. **Fig. 10 b**)). Then the load current is only freewheeling through three output diodes, but also has to flow through both secondary windings of the transformer.

C. Single-phase transformers

The single-phase transformers can basically be designed as the transformer of a DC/DC full bridge forward converter, with the only difference that the input voltage is varying in time. Since the duty cycle of the full bridge and the voltage applied to the transformer are proportional to the input voltage v_{in}, the envelope $B_{\mathrm{en}}(t)$ of the flux density in the transformer over one mains period is

$$B_{\mathrm{en}}(t) = \hat{B} \cdot \sin^2(\omega_{\mathrm{in}} t), \tag{3}$$

where the maximum flux density $\hat{B}$ is reached when the maximum input voltage $\hat{v}_{\mathrm{in}}$ is applied to the transformer (with a core cross section A_{core}) during one half period $T_s/2$

$$\hat{B} = \frac{\hat{v}_{\mathrm{in}} \cdot T_s/2}{N_1 \cdot A_{\mathrm{core}}}. \tag{4}$$

Finally, based on (1), the turns ratio of the transformer

$$\frac{N_1}{N_2} = \frac{3}{2} M_{\mathrm{max}} \frac{\hat{v}_{\mathrm{in,min}}}{v_{\mathrm{out}}} \tag{5}$$

can be easily found with the minimum input voltage amplitude $\hat{v}_{\mathrm{in,min}}$ and the maximum modulation index M_{max}, which typically is set around 0.9 in order to leave a certain margin for the control. As already mentioned, if the output rectification is realized with three independent rectifier bridges, the secondary winding of each single-phase transformer has to be realized as a center-tapped winding, however, the turns ratio N_2/N_1 stays the same. Concerning the loss calculation it has to be considered that the voltage applied to the transformer is independent whether one common or three separate

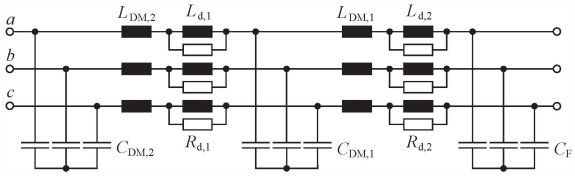

Fig. 11 Circuit diagram of the two-stage EMI input filter.

output rectifier bridges are used. Consequently, for both options the flux excitation as well as the core losses stay the same. The copper losses, however, have to be calculated differently. With one common output rectifier, the same load current with the same rectangular waveform - the pulse width is defined by the phase with the maximum duty cycle - is flowing through all three transformers. With three separate output rectifiers, however, the load current's pulse width is given by the duty cycle of the corresponding full bridge.

D. Input and output filter

The input filter has to be designed in such a way that the EMC directive (CISPR, class B) concerning conducted noise emission in the range of 150 kHz-30 MHz is fulfilled. In order to keep the input filter effort as low as possible, typically the switching frequency is limited below 150 kHz, because then the spectral component at the switching frequency doesn't have to be considered for the input filter design. Unfortunately, buck-type PFC rectifiers feature discontinuous input currents, thus compared to boost-type systems typically a higher filter attenuation is needed resulting in an increased EMI filter effort, e.g. a two-stage filter instead of a single-stage filter has to be built (cf. **Fig. 11**). Due to the discontinuous input currents, usually large filter capacitors C_F are selected which have to be closely placed to the phase module in order to achieve a low commutation inductance. In addition to the filter capacitors C_F also a small dc-link capacitor C_{DC} is provided between the input diode rectifier and the full bridge, which further improves the switching behavior, especially during the turn on transition from freewheeling to either positive or negative voltage (cf. **Fig. 6 a)**. However, since the power factor λ is reduced with increasing filter capacitance, the differential mode capacitors shouldn't be selected too large; $\lambda > 0.9$ for the whole input voltage range and a wide output power range is a reasonable value. It should be also noted again that the IMY/Δ-rectifier is capable of slightly shifting the input current out of phase with the input voltage, thus enabling reactive power compensation. Besides the differential mode capacitors, also the common mode capacitors have to be provided, where the capacitance is limited by the maximum ground currents drawn from the mains, which have to be below 3.5 mA.

Based on the specified output voltage and current ripple, the output filter components L_{out} and C_{out} can be designed. Due to the continuous current impressed by the output inductor L_{out}, the current ripple capability of the output capacitor is not as crucial as e.g. with boost-type PFC rectifiers. Assuming a constant output voltage v_{out}, based on the rectified voltage v_{sec} which is applied to the filter inductor, the maximum current ripple is obtained as

$$\Delta i_{\mathrm{L,pp,max}} = \frac{\hat{v}_{\mathrm{in}}}{L_{\mathrm{out}}} \frac{3M}{4 f_{\mathrm{sw}}} \frac{N_2}{N_1} \left(1 - \frac{\sqrt{3}}{2} M\right). \tag{6}$$

With the given specifications in **Table I**, now the achievable efficiency, and the loss and volume distribution of the IMY/Δ-rectifier are calculated and the following realization options are compared:

- **R1,CFD2 (sym. mod.)**: where the full bridge is realized with MOSFETs of the CFD2-CoolMOS series, which are controlled based on the symmetric modulation scheme and for the output rectifier only one common diode bridge is used,
- **R1,CFD2 (asym. mod.)**: where compared to **R1,CFD2 (sym. mod.)** only the modulation scheme is changed to the asymmetric modulation,
- **R3,CFD2 (sym. mod.)**: where compared to **R1,CFD2 (sym. mod.)** only the output rectifier is realized with three separate diode bridges and finally,
- **R1,C7+OR-ing**: where the full bridge is realized with MOSFETs of the C7-CoolMOS series, operated in an OR-ing configuration with the symmetric modulation scheme and common diode rectifier.

The comparative evaluation of the mentioned realization options has been done for different design, where per switch also a parallel connection of multiple discrete MOSFET devices (up to four devices per switch) is considered. For the additional diodes in the OR-ing configuration, however, there are no discrete devices placed in parallel, due to the negative temperature coefficient of Schottky diodes; a parallel connection of Si or Schottky diodes should be only used if the diode chips are already available in the same package, thus the chips are thermally well coupled. SiC-diodes, however, feature from a certain current level on a positive temperature coefficient. Therefore, a parallel connection of these diodes would be feasible. Nevertheless, due to the given forward voltage drop, with a parallel connection of diodes the reduction of the conduction losses is limited.

In **Fig. 12** the achievable efficiencies with respect to the resulting converter costs are shown. As can be noticed, for the same costs the realization option **R1,CFD2 (asym. mod.)** shows the highest efficiencies. With four parallel connected MOSFETs of the CFD2-CoolMOS series (IPW65R041CFD, $V_{\mathrm{ds}} = 650\,\mathrm{V}$, $R_{\mathrm{ds,on}} = 41\,\mathrm{m\Omega}$) a maximum efficiency of 96.7 % is achieved at nominal input voltage and nominal load. Since for the laboratory prototype an efficiency of at least 96 % is targeted, the design point DP_1 **R1,CFD2 (asym. mod.)**, where two MOSFETs of the CFD2-CoolMOS series (IPW65R041CFD, $V_{\mathrm{ds}} = 650\,\mathrm{V}$, $R_{\mathrm{ds,on}} = 41\,\mathrm{m\Omega}$) are connected in parallel per switch, is selected as the reference design (96.0 %) and the costs are normalized with respect to this design.

If the reference design is operated with the symmetric modulation scheme (**R1,CFD2 (sym. mod.)** at design point DP_2), where two of the six switching transitions result in hard switching, the efficiency is drastically reduced to 95.0 %, which is a difference of 1 % ($= 75\,\mathrm{W}$). If per switch even more MOSFETs are connected in parallel, the discrepancy between the two modulations schemes is even more pronounced; while the efficiency of the asymmetric modulation scheme is monotonically increasing, the losses with symmetric modulation are increasing due to the higher recovery losses. This is clearly shown in **Fig. 13**, where the loss distribution of the different designs is given. The only difference in the loss distribution and thus in the efficiency of design point DP_1 and DP_2 is found in the additional switching losses of DP_2. Consequently, the realization option **R1,CFD2 (sym. mod.)** is no more considered.

Another possibility is to built the reference design with three separate half bridge output rectifiers and transformers with center-tapped secondary winding, which should result in reduced conduction losses in the full bridge and in the primary windings of the transformers (**R3,CFD2 (asym. mod.)**). As illustrated in the loss distribution of **Fig. 13**, the conduction losses in the switches can be reduced, however, the conduction losses in the output rectifier are increasing disproportionately, resulting in a lower total converter efficiency and in even higher costs. Surprisingly, the total transformer losses are hardly influenced. This can be explained by the fact that with three

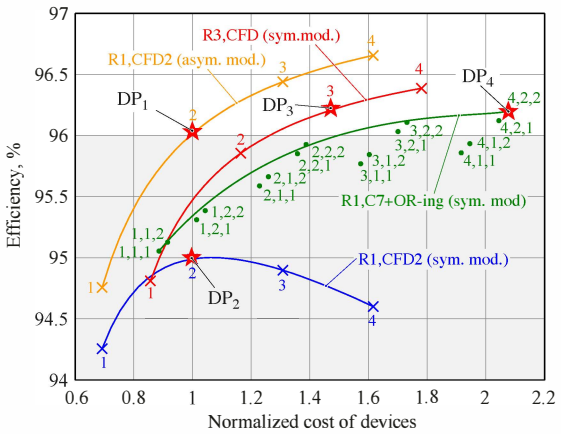

Fig. 12 Comparison of the achievable efficiencies for the different realization options with respect to the resulting converter costs. The numbers indicate how many parallel MOSFETs are used per switch. In the case of the realization option (R1,C7+OR-ing), the number of MOSFETs S, parallel diodes D_P and series diodes D_S is indicated (S,D_P,D_S). The costs are normalized with respect to the reference design (design point DP_1) that achieves an efficiency higher than 96 %.

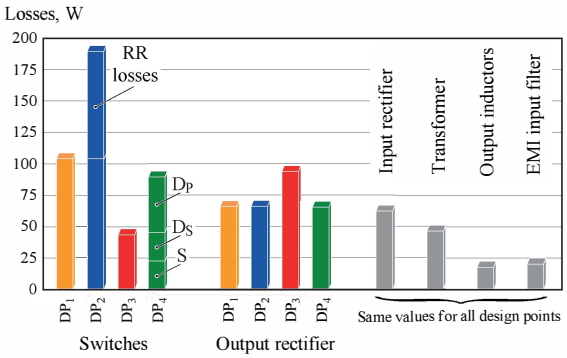

Fig. 13 Loss distribution for the different realization options at the design points DP_1, DP_2, DP_3 and DP_4. In addition to the conduction losses in the MOSFET for DP_2 the reverse recovery losses and for DP_4 the conduction losses in the Schottky diodes D_S and in the SiC-diodes D_P have to be considered.

output rectifiers the losses in the primary winding are effectively reduced, however the losses in the secondary winding are increased by approximately the same amount since now two instead of one secondary winding has to be arranged in the same winding window. Thus, a smaller wire diameter has to be selected which results in higher conduction losses in the secondary windings.

In order to compensate the additional losses in the three output rectifiers and to achieve approximately the same efficiency as with the reference design, now for the design point DP_3 (96.2 %) three instead of two parallel MOSFET are needed per switch (cf. **Fig. 12**). As one might expect, if the output rectifier would be realized as a full bridge rectifier, the conduction losses in the output diodes would be even higher. Such a solution would only be reasonable if Schottky diodes with low forward voltage drop, e.g. at lower output voltages, could be used. Therefore, since for the realization option with three rectifiers **R3,CFD2 (sym. mod.)** the hardware effort and thus the costs ($\sim$ 1.8 times more expensive) are strongly increased, this design is also dropped.

As a fourth option, the full bridges of the IMY/Δ-rectifier can be realized with MOSFETs of the C7-CoolMOS series in OR-ing configuration, thus the reverse recovery losses can be discarded and both modulation schemes can be used (**R1,C7+OR-ing**). Due to the superior low on-state resistance of the C7-MOSFET (IPW65R019C7), the conduction losses in the switch can be drastically reduced. However, this efficiency improvement is again overcompensated by the additional conduction losses in the series Schottky diode and especially in the anti-parallel SiC-diode, which shows a higher forward voltage drop (cf. **Fig. 13**). In design point DP_4 with four parallel connected MOSFETs and two Schottky/SiC-diode per switch a similar efficiency (96.2 %) is achieved as with the reference design.

Although the costs with this realization option are more than doubled compared to the reference design - due to the high number of semiconductor devices - it offers the flexibility to verify the dimensioning and the achievable efficiencies of the different realization options explained above in just one laboratory prototype; e.g. both modulation schemes can be implemented or the series connected Schottky diodes can be shorted in order to verify the reference design point DP_1.

IV. Laboratory Prototype

Based on the specifications given in **Table I**, a 7.5 kW laboratory prototype is built with full bridges in OR-ing configuration as described in the previous section.

Each phase module, containing the input diode bridge and the full bridge where discrete devices in D2PAK package are used, is realized on a single-layer insulated metal substrate (IMS) board that improves the heat transfer from the semiconductors to the heatsink. The conduction losses in the input rectifier diodes can be easily calculated based on the average and rms current ratings, which for nominal operating conditions are 4.9 A and 10.24 A, respectively. For the selected rectifier diodes (DSP45-12A), conduction losses of 5 W per diode are expected. Accordingly, the conduction losses in the MOSFETs (IPB65R045C7), Schottky diodes (VBT6045C) and SiC-diode (IDK12G65C5) are found to be 1.8 W, 1.9 W and 3.7 W per switch.

Due to the hard commutation of the output rectifier diodes, SiC Schottky barrier diodes (C4D40120D) are selected, where 16.3 W of conduction losses are expected per diode.

The design of the single-phase transformers is performed with an optimization algorithm, where different cores and turn numbers are evaluated. There, a compromise between volume and losses has to be made. For a selected switching frequency of 72 kHz transformers based on two stacked E55-cores (EPCOS) were realized. The windings with $N_1 = 8$ and $N_2 = 9$ were made of 3 mm litz wire with 840 insulated strands.

Due to the mechanical design, the filter inductor $L_\mathrm{out} = 2 \cdot 195\,\mu\mathrm{H}$ is split in two separate output inductors one of each placed in the positive and negative output rail. Each inductor is also built with two stacked E55-cores, and because of the almost constant output current, the winding is realized with 14 turns of a 2 mm thick solid copper wire. A list of the main components is given in **Table II** and the corresponding volume distribution is shown in **Fig. 14**. More than 50 % of the volume is already captured by the heatsinks, which together with the magnetic components consumes 70.8 %.

The calculated efficiencies of the designed IMY/Δ-rectifier for different input voltages and load conditions is shown in **Fig. 15**. As can be noticed, the efficiency should be maintained over 96 % for all operating conditions. The IMY/Δ-rectifier prototype, on which now the experimental measurements will be performed, is shown in **Fig. 16**.

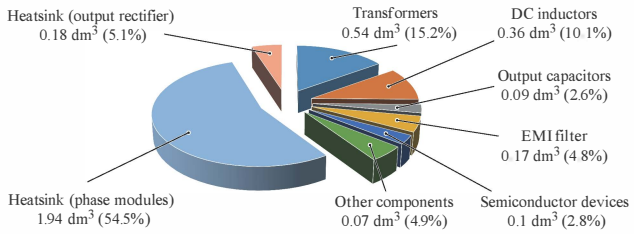

Fig. 14 Volume distribution of the main components.

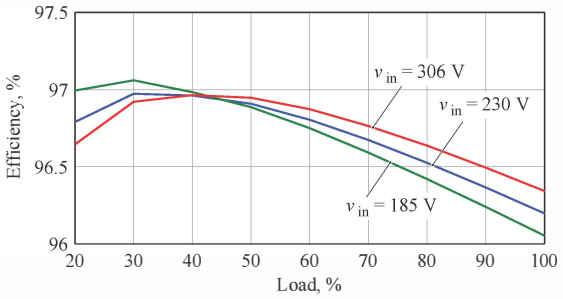

Fig. 15 Calculated efficiency of the IMY/Δ-rectifier at different load and input voltage conditions.

V. Conclusions

IMY/Δ-rectifier presents an interesting alternative to three-phase integrated PFC rectifiers. It provides the PFC functionality and the galvanic isolation in a single-stage energy conversion. Due to its phase-modularity, only the phase voltage determining the required blocking capability of the semiconductors, thus 600 V instead of 1200 V semiconductor devices can be used, which typically feature lower on-state resistances and improved switching behavior.

The IMY/Δ-rectifier can be controlled with a simple phase shift modulation, and due to its buck-type topology the same control structure and duty cycle calculation concept as for a conventional DC/DC buck converter can be implemented. In addition, with the presented modified modulation scheme in each switching transition soft switching (ZVS) can be achieved without any additional circuitry.

In this paper a comprehensive analysis of the basic operation and the design of the IMY/Δ-rectifier, including the selection of semiconductor devices and magnetic components, is presented. The built laboratory prototype is designed to achieve an efficiency of more than 96 % under different load and input voltage conditions. In the further research, experimental measurements will be performed in order to verify the presented theoretical investigations.

TABLE II Main components of the IMY/Δ-rectifier prototype.

Component	Value/details
MOSFETs S	650 V CoolMOS C7 series (IPB65R045C7)
Series diodes D_S	45 V/30 A Schottky barrier (VBT6045C)
Parallel diodes D_P	650 V/12 A SiC Schottky barrier (IDK12G65C5)
Input diodes	1200 V/45 A rectifier diodes (DSP45-12A)
Output diodes	1200 V/54 A SiC diodes (C4D40120D)
Isolation transformers	Stack of two E55 N87 cores, $N_1/N_2 = 8/9$, 3 mm/840 strands Litz wire
Filter inductor L_{out}	2x195 µH, 2 stacked E55 N87 cores, 0.6 mm airgap, 14 turns of 2 mm solid copper wire
Filter capacitor C_{out}	7x82 µF

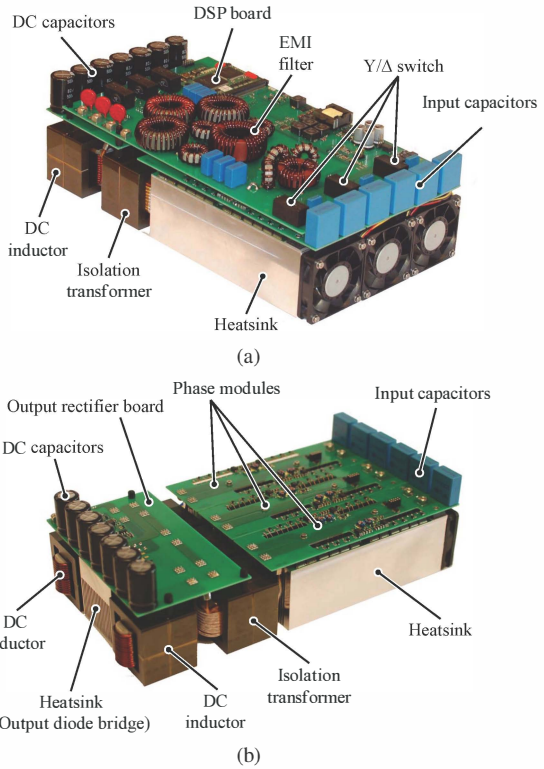

Fig. 16 Realized 7.5 kW IMY/Δ-rectifier prototype. **a)** fully assembled and **b)** without the main board, in order to show the phase modules and the output rectifier board.

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