Power Electronic Systems
Laboratory

Proceedings of the 8th International Power Electronics and Motion Control Conference (IPEMC 2016-ECCE Asia), Hefei, China, May 22-25, 2016

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Comprehensive Evaluation of GaN GIT in Low- and High-Frequency Bridge Leg Applications

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***Abstract*—In power electronics applications with power ratings around several kilowatts, wide band gap semiconductors are more and more replacing state-of-the-art Si MOSFET. SiC MOSFETs with blocking voltage rating up to $1200\,\mathrm{V}$ and low-voltage GaN devices are already commercially available on the market since a couple of years. Now also $600\,\mathrm{V}$ GaN devices are entering the market, which are a cost-effective solution in many $400\,\mathrm{V}$ key applications in order to increase the system performance in terms of achievable efficiencies or power density. Besides the employed semiconductor devices also the design of the appropriate gate drive circuit is important. In this paper a simple and reliable gate drive circuit for driving GaN switches is presented. In addition, the proposed gate drive is used to evaluate the switching performance of a GaN Gate Injection Transistor (GIT) under soft- and hard-switching condition, which provides a basis for further optimization of totem-pole converter systems.**

I. Introduction

In power electronics applications with power ratings around several kilowatts, Wide Band Gap semiconductors (WBG) like SiC or GaN are progressively replacing state-of-the-art Si MOSFET, especially in hard-switching applications [1], [2], due to the improved switching performance and lower switching losses, which e.g. with Si MOSFETs are mainly caused by the large output capacitance and the typically bad reverse recovery behavior of the body diode. In contrast, for the same voltage and current ratings, WBG devices feature a much smaller output capacitance per chip area [3] and do not or hardly suffer from reverse recovery, thus higher efficiencies can be achieved. Even in soft-switching topologies, e.g. with Triangular Current Mode (TCM) modulation, WBG semiconductors are a reasonable choice since on the one hand WBG devices also feature a lower on-state resistance per chip area than Si devices [3] and on the other hand the energy stored in the large output capacitance of Si devices cannot be fully retrieved [4]. This is to some extend also true for WBG devices, but there the output capacitance is much smaller.

SiC MOSFETs with blocking voltage rating up to $1200\,\mathrm{V}$ and low-voltage GaN devices up to $200\,\mathrm{V}/450\,\mathrm{V}$ are already commercially available on the market since a couple of years. Now also $600\,\mathrm{V}$ GaN devices are entering the market. There are mainly two types of GaN switches available: the High-Electron-Mobility Transistor (HEMT) GaN MOSFET, which is internally built as a cascode of a low-voltage Si-MOSFET and a high-voltage normally-on GaN switch (JFET) in order to emulate it externally as a normally off device, and the GaN Gate Injection Transistor (GIT) MOSFET, which is an inherently normally-off device. The major disadvantages of the cascode structure are that with the intermediate Si-MOSFET it is not possible to directly control the switching behavior of the GaN device, as well as the more complex manufacturing process and the additional bond wires between Si-MOSFET and GaN device which further increase the parasitic inductances [5]. However, as already described in the literature [2], both GaN types can definitely compete with $650\,\mathrm{V}$ SiC devices with respect to switching performance and achievable converter efficiency. In addition, due to the fact, that GaN devices can be build based on Si devices (eGaN, enhancement-mode GaN transistor), it is a cost-effective solution e.g. in many $400\,\mathrm{V}$ key applications like single-phase PFC rectifers [6], single and three-phase inverters or even isolated and non-isolated dc/dc converter [7], [8]. Typically, all these circuit topologies consist of several bridge legs, the so called totem-pole structure (cf. **Fig. 1**). Thus, independently of the system operation (PWM or TCM / hard- or soft-switching) beside the magnetic components, the bridge leg is a basic element which mainly defines the system performance in terms of achievable efficiency or power density.

Since GaN devices are not avalanche rated, they are most suitable for half-bridge applications, where based on a good layout almost no over-voltage is expected. The achievable performance of GaN GIT was already analyzed in the literature [1], [7], [9], however, no loss data for soft-switching is given. Therefore, in this paper a comprehensive evaluation of the $600\,\mathrm{V}$ GaN GIT MOSFET (IFX 5893, Samples from Infineon) in a hard- and soft-switched half bridge configuration is

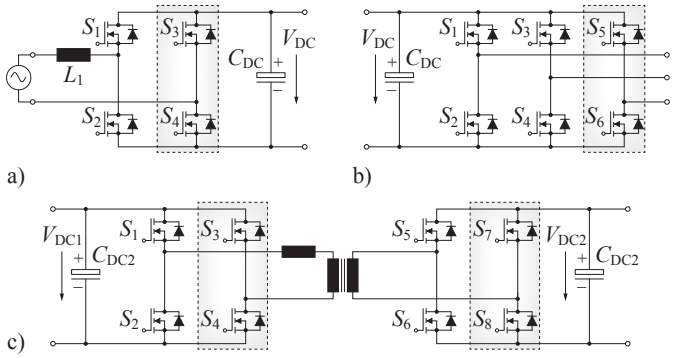

Fig. 1: Typical bridge leg applications: **a)** Totem-pole PFC full-bridge rectifier, **b)** Totem-pole full-bridge inverter, **c)** DC-DC dual active bridge.

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performed. Furthermore it will be shown that the determination of the soft-switching losses is very crucial, thus a calorimetric measurement setup, similar to the one presented in [1], is used. In addition to the proper selection of the semiconductor device and the modulation scheme, for the design of a reliable half-bridge also the selection of the appropriate gate drive circuit is important. Beneficially, since WBG devices, especially SiC and clearly also the HEMT GaN with its cascode structure, are voltage controlled devices and feature similar gate input characteristics with a capacitive behavior as Si-MOSFETs (C_{gs} and C_{dg}), the same simple and widely used push-pull gate drive circuit with separate turn-on and turn-off gate resistances can be employed (cf. **Fig. 2**). Another possible gate drive topology would for example be a resonant gate drive circuit [10], which however is not in scope of this paper.

Beside the needed dynamic performance during the switching transitions, the gate drive should also keep the switching device safely on or off during steady state. For GaN devices, the off-state is very crucial, since these devices feature a much lower threshold-voltage than their Si counterparts, typically in the range of 1 -2 V or even less. Consequently, GaN devices are sensitive to disturbances at the gate and a negative turn-off voltage at the gate is absolutely necessary, in order to prevent a parasitic turn-on of the GaN switch, e.g. in a totem-pole configuration when the complementary switch is turning-on and the gate capacitance C_{gs} is charged via the Miller capacitance C_{dg} due to a high $\mathrm{d}v/\mathrm{d}t$ voltage transition. As a drawback, the negative gate voltage is typically realized with a bipolar gate drive supply, which on the one hand makes the gate drive circuit's power supply, e.g. the isolation transformer, more complex and on the other hand also increases the parasitic inter-winding capacitance leading to higher common mode currents flowing through the gate drive. Furthermore, beside the typical capacitive behavior (C_{gs} and C_{dg}), the gate input characteristic of the GaN GIT also features a diode forward characteristic with a forward voltage of around 3.5 V (cf. **Fig. 2 b)**. Thus, in order to limit the gate current through the internal gate diode D_{gs} during the on-state interval, the positive gate drive voltage has to be either limited close to this value, which would limit the dynamic performance of the gate drive, or has to be decoupled from the gate input, which consequently also makes the driving part more complex. In practice, however, due to cost, efficiency, power density and reliability aspects, the gate drive circuit should be as safe, small and simple as possible. Following this reasoning, in [11] a gate drive circuit is proposed, where just a series capacitor C_{s} is added to the conventional resistive gate drive circuit, in order to overcome the mentioned drawbacks (cf. **Fig. 3 a)**). A similar gate drive concept with a bipolar power supply is also presented in [9]. On the one hand, the proposed gate drive in [11] enables a negative gate voltage even with a unipolar supply voltage, and on the other hand decouples the gate supply voltage from the gate input during steady state while it still allows for fast switching transitions. However, as will be shown in the following, this gate drive still shows drawbacks regarding a safe turn-off of the device, especially in the mentioned totem pole configuration. Therefore, in Section II, the operation of the gate drive presented in [11] is shortly described and based on that an improved and more reliable gate drive circuit for GaN devices is presented. Furthermore, the proper dimensioning of the gate drive circuit is described in detail and its reliability and performance is verified for different switching frequencies up to 1 MHz and voltage slopes above 500 kV/µs. Afterwards, the designed gate drive circuit is used to perform a comprehensive evaluation of the GaN GIT's switching performance under hard- and soft-switching condition in Section III. This finally provides a sound basis for the optimization of different converter systems.

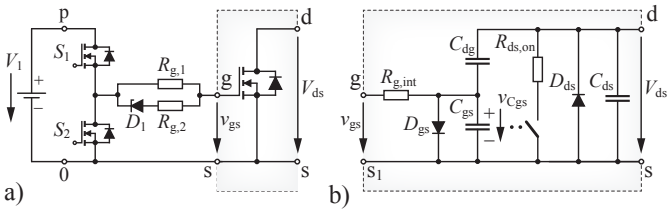

Fig. 2: a) Conventional gate drive circuit for voltage controlled semiconductor devices with separate gate resistance for on- and off-transition and **b)** simplified equivalent circuit of the GaN GIT describing the gate input behavior.

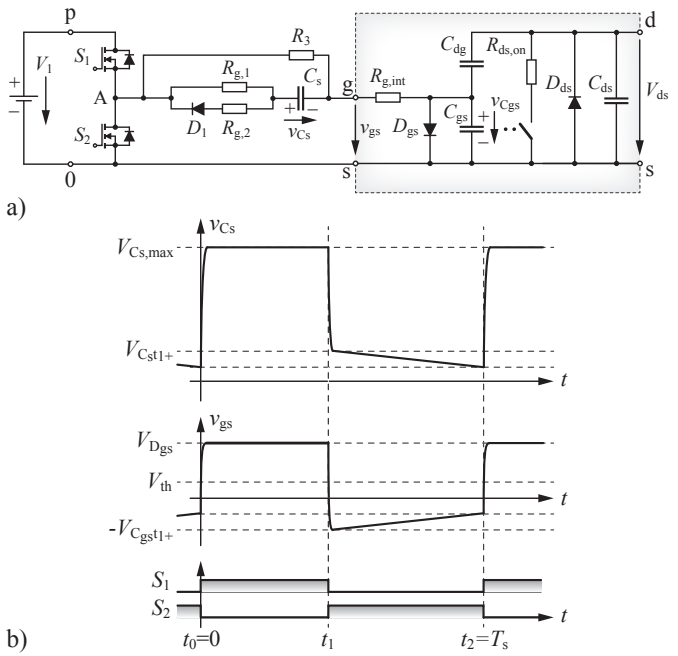

Fig. 3: a) GaN gate drive circuit with decoupling capacitor C_{s} as proposed in [11] and **b)** corresponding waveforms during one switching cycle.

II. Proposed GaN Gate Drive Circuit

A. Gate Drive Operation

The turn-on switching transition is initiated by turning-on switch S_1 at t_0 (cf. **Fig. 3 b)**). A current will flow through the typically small turn-on gate resistor $R_{\mathrm{g,1}}$, the series capacitor C_{s} and the internal gate resistance $R_{\mathrm{g,int}}$ which exponentially charges the gate capacitance C_{gs} with the time constant $\tau_{\mathrm{on,1}} = C_{\mathrm{gs}} \cdot (R_{\mathrm{g,1}} + R_{\mathrm{g,int}})$ if $C_{\mathrm{s}} \gg C_{\mathrm{gs}}$. Assuming a positive gate voltage V_1 which is larger than the forward voltage V_{Dgs} of the internal gate diode D_{gs}, the

gate capacitance C_{gs} is only charged to $V_{\mathrm{Cgs,max}} = V_{\mathrm{Dgs}}$, since then the current commutates to the internal gate diode until the series capacitance C_{s} is exponentially charged to $V_{\mathrm{Cs,max}} = V_1 - V_{\mathrm{Dgs}}$ with $\tau_{\mathrm{on},2} = C_{\mathrm{s}} \cdot (R_{\mathrm{g},1} + R_{\mathrm{g,int}})$. During the on-state interval $t_0 - t_1$ the series capacitor C_{s} is blocking and only a small current is flowing through R_3 in order to keep the GaN GIT in on-state safely. As described in [9], the on-state resistance $R_{\mathrm{ds,on}}$ can be influenced by this on-state quiescent current I_{q}, however, the influence is only marginally and increases slightly with temperature. To turn-off the GaN GIT first S_1 is opened and then S_2 is closed at t_1. Since C_{s} is still charged, the capacitor voltage $v_{\mathrm{Cs}} = V_{\mathrm{Cs,max}}$ is now applied to the gate in negative direction. Consequently, the gate capacitance C_{gs} is again exponentially discharged through the internal gate resistance $R_{\mathrm{g,int}}$, the turn off resistance $R_{\mathrm{g,off}}$ which is defined by the parallel connection of $R_{\mathrm{g},1}$ and $R_{\mathrm{g},2}$, and the series capacitor C_{s} with the time constant $\tau_{\mathrm{off}} = C_{\mathrm{gs}} \cdot (R_{\mathrm{g,off}} + R_{\mathrm{g,int}})$ until C_{s} and C_{gs} reach the same voltage. Assuming again $C_{\mathrm{s}} \gg C_{\mathrm{gs}}$, the voltage at C_{s} will almost stay constant, hence, a negative voltage is applied to the gate during this turn-off transition even though a unipolar supply voltage is used. During the off-state interval $t_1 - t_2$, however, the series capacitance C_{s} as well as the gate capacitance C_{gs} are continuously discharged through R_3 towards 0 V.

At $t_2 = T_{\mathrm{s}}$ the GaN GIT is again turned-on by opening S_2 and closing S_1. C_{gs} is again exponentially charged to $V_{\mathrm{Cgs,max}}$, however, now the initial value of the gate current depends on how much the series capacitance C_{s} was discharged during the off-state interval. This means that depending on the duration of the off-state time interval the dynamic performance of the gate drive circuit changes. Advantageously, the resistor R_3 shouldn't be too large in order to quickly discharge C_{s} and to guarantee a fast switching transition even after short off-state intervals. In this case, however, during long off-state intervals the capacitances C_{s} and C_{gs} will be discharged completely. Due to the low threshold voltage, this could now lead to safety problems. In a half-bridge configuration, for example, the high voltage slope ($\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$) occuring the turn-on transition of the complementary switch leads to a proportional current flowing through the Miller capacitance C_{dg}, which could charge the capacitances C_{s} and C_{gs} above the threshold voltage V_{th} and would parasitically turn-on the switch, even if the gate drive circuit is trying to keep the switch off. Alternatively, if the described gate drive circuit is used with a bipolar supply voltage as presented in [9], during the turn-off interval, the gate voltage would always remain at a negative level even if the series capacitor is fully discharged, and thus eliminating the reliability problem. However, since R_3 not only discharges the capacitance C_{s} and C_{gs} during the off-state interval but also defines the quiescent current I_{q} during the on-state interval, which is clearly limited to a certain maximum value, the dependency of the gate drive's dynamic performance on the duration of the off-state interval is still unremedied. Instead of changing the gate drive's supply part, the following modifications in the driving part are proposed, in order to guarantee a safe gate drive operation with consistent performance.

In order to avoid a complete discharge of the capacitances C_{s} and C_{gs} during the off-state interval, the Zener diode ZD_1 with a Zener voltage V_{ZD1} is added in series to the resistor R_3

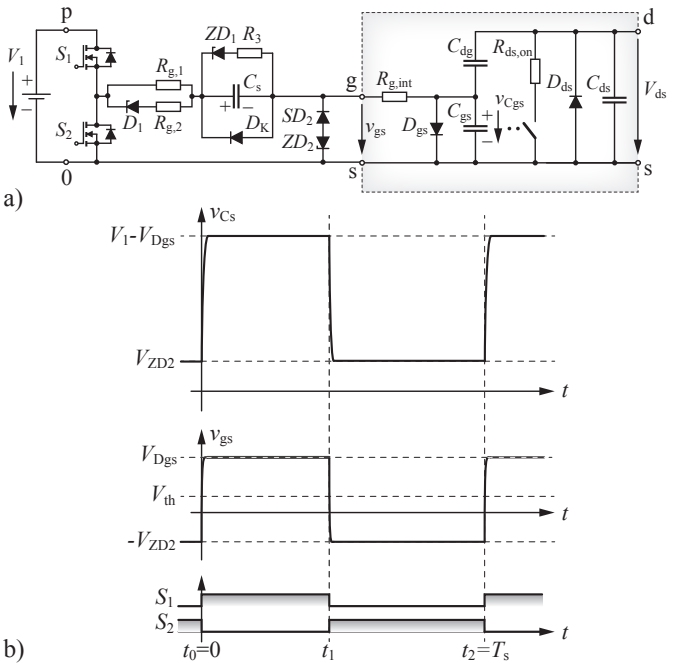

Fig. 4: a) Improved GaN gate drive circuit showing the proposed modification in the gate drive's driving part in order to guarantee a safe gate drive operation with consistent performance and **b)** corresponding waveforms during on switching cycle.

which allows to define a minimum steady state voltage for C_{s} and C_{gs} (cf. **Fig. 4 a)**). As long as the voltage of C_{s} and C_{gs} is larger than V_{ZD1}, both capacitors are discharged through R_3 and for voltages smaller than V_{ZD1} the Zener diode will block any current flow. For the dimensioning of R_3, which determines the quiescent current I_{q}, it has to be considered that with the additional Zener diode ZD_1 the voltage across R_3 is now reduced to $V_1 - V_{\mathrm{Dgs}} - V_{\mathrm{ZD1}}$. Typically the quiescent current I_{q} is in the mA-range resulting in a large resistance R_3 and in a slow discharge of C_{s} and C_{gs}. Hence, the anti-series connection of the Zener diode ZD_2 and the Schottky diode SD_2 is added, to quickly discharge C_{s} and C_{gs} through the small turn-off gate resistance $R_{\mathrm{g},1} || R_{\mathrm{g},2}$ to a maximum voltage V_{ZD2}, neglecting the forward voltage drop of SD_2. Advantageously, both Zener voltages of ZD_1 and ZD_2 are selected to be equal ($V_{\mathrm{ZD1}} = V_{\mathrm{ZD2}}$), whereby C_{s} and C_{gs} are directly discharged to a defined voltage and a further discharge through R_3 is prohibited. This also guarantees always the same dynamic performance independently from the off-time duration.

It has to be mentioned that after start-up of the converter system the capacitor C_{s} is not charged before the first turn-on sequence. Therefore, a Schottky diode D_{k} featuring a low forward voltage drop is placed in parallel to C_{s} which prevents C_{gs} to be charged to voltages above the threshold voltage V_{th}, e.g. due to the Miller current or any other distortion. After the first turn-on C_{s} is charged to its nominal value and D_{k} remains in blocking state, hence having no influence on the gate driver's operation anymore. Alternatively, the described gate drive circuitry can be moved from the gate to the source

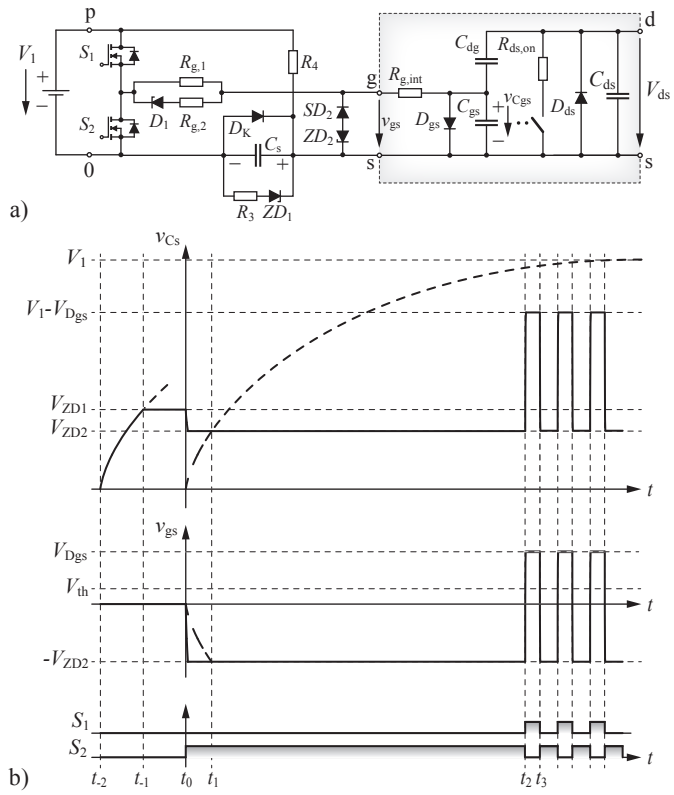

Fig. 5: a) Moving the described gate drive circuitry from the gate to the source connection and swapping the polarity of D_k, ZD_1 enables a simple charging of C_s through R_4 before the first turn-on sequence at t_2 is taking place and **b)** corresponding waveforms during start up.

connection, enabling a simple charging of C_s even before the first turn-on action takes place (cf. **Fig. 5 a)**). Keeping in mind that the polarity of all components has to be swapped, the capacitor C_s can be easily charged from the gate drive supply V_1 through R_4. As shown in **Fig. 5 b)**, as soon as the supply voltage V_1 is applied to the gate drive circuit at t_{-2}, the capacitor voltage V_Cs starts to rise exponentially with the time constant $\tau_\mathrm{charge} = C_\mathrm{s} \cdot R_4$, where R_4 should actually have a high resistance in order not to influence the regular gate drive operation. Assuming a long initialization time of the gate drive controller IC, which in reality only takes a few nanoseconds, the switches S_1 and S_2 are uncontrolled, i.e. both switches are in the off-state. Consequently, the capacitor voltage V_Cs further increases until the Zener diode ZD_1 starts to conduct at the time instant t_{-1} and prevents C_s from further charging. It has to be mentioned that during this time intervals the gate-source voltage v_gs always stays at 0 V. At t_0, the initialization of the gate drive controller IC is finished and since at start up of a converter system typically all power switches are turned-off, also the corresponding gate drives immediately change to the off-state, i.e S_2 is turned-on. Accordingly, assuming $V_\mathrm{ZD2} < V_\mathrm{ZD1}$, the series capacitor C_s is quickly discharged through the small turn-off gate resistance $R_{\mathrm{g},1} || R_{\mathrm{g},2}$ and S_2 to $V_\mathrm{Cs} = V_\mathrm{ZD2}$. Furthermore, the capacitor voltage is directly applied to the power MOSFET's gate and charges C_gs in negative direction to $v_\mathrm{gs}(t_{+0}) = -V_\mathrm{Cs}$, thus keeping the switch safely off. Afterwards, the converter system can be operated in a safe condition already from the first turn-on sequence at t_2 as described previously. For the sake of completeness, in reality the initialization time of the gate drive controller IC is in the ns-range ($t_{-2} \approx t_0$), thus during the time interval $t_0 ... t_1$ the gate source voltage v_gs directly decreases with the time constant τ_charge to $-V_\mathrm{ZD2}$ as indicated with dashed lines in **Fig. 5 b)**.

B. Gate Drive Design and Performance Analysis

In the following the proposed gate drive circuit is dimensioned for the selected GaN GIT (IFX 5893, Samples from Infineon). The GaN GIT's most important parameters needed for the design of the gate drive circuit are given in **Table I**. For the realization of the gate drive's push pull stage the LM5114 half-bridge gate driver from Texas Instruments is selected. Due to its absolute maximum rated supply voltage of 14 V as well as the maximum allowable voltage range at the gate (cf. **Table I**), the driver's supply voltage is set to $V_1 = 12\,\mathrm{V}$ taking a certain voltage margin into account. Based on this assumption and considering the given forward voltage V_Dgs of the internal gate diode, during the turn-on interval the decoupling capacitor C_s is charged to $V_\mathrm{Cs} = 7.8 ... 9.2\,\mathrm{V}$ (typ. 8.5 V). Thus, in order to achieve always the same dynamic performance during the turn-on transition, the Zener voltage $V_\mathrm{DZ1} = V_\mathrm{DZ2}$ has to be below the minimum voltage of V_Cs. A reasonable choice for the Zener voltage $V_\mathrm{DZ1} = V_\mathrm{DZ2}$ would be 6.8 V or 7.5 V. It has to be considered that with the selected Zener voltage the negative gate voltage level $V_\mathrm{gate,min} = -V_\mathrm{ZD1} = -V_\mathrm{ZD2}$ and the positive gate voltage level $V_\mathrm{gate,pos} = V_\mathrm{in} - V_\mathrm{ZD1} = V_\mathrm{in} - V_\mathrm{ZD2}$ are directly determined, thus, with the selection of the Zener voltage a compromise between fast turn-on as well as safe and fast turn-off may be needed.

On the one hand, the positive gate voltage $V_\mathrm{gate,pos}$ and the on-state gate resistance $R_\mathrm{g,on}$ (which in this case is strongly influenced by the high internal gate resistance $R_\mathrm{g,int}$) define how fast the gate is charged (charging a RC-element from $V_\mathrm{gate,neg}$ to V_th with $\tau = R_\mathrm{g,on} \cdot C_\mathrm{gs}$), which in general influences the switching delay and the hard-switching losses. Often the optimum value of the on-state gate resistance is identified in the application or in switching loss measurements, since small values namely enable faster switching times and typically lower switching losses (which still depends on the reverse recovery behavior of the anti-parallel diode), but can also lead to ringing caused by layout and packaging dependent inductances, especially by the common source inductance.

TABLE I: Characteristics of the GaN GIT needed for the dimensioning of the proposed gate drive.

Parameter	*Ratings*
V_gs	$-10 ... 4.5\,\mathrm{V}$
V_th	$0.7 ... 1.6\,\mathrm{V}$ (typ. $1.2\,\mathrm{V}$)
V_Dgs	$2.8 ... 4.2\,\mathrm{V}$ (typ. $3.5\,\mathrm{V}$)
$R_\mathrm{g,int}$	$5.3\,\Omega$
$C_\mathrm{gs,eq}$	400 pF
$C_\mathrm{gd,Qeq}$ ($V_\mathrm{gd} = 0 ... 400\,\mathrm{V}$)	7 pF
$C_\mathrm{ds,Qeq}$ ($V_\mathrm{ds} = 0 ... 400\,\mathrm{V}$)	114 pF

For soft-switching, however, a fast turn-on transition is not mandatory, since in this case the current only commutates from the anti-parallel diode to the MOSFET channel slightly reducing the conduction losses. On the other hand, in order to minimize the turn-off losses especially for soft-switching, a fast discharge of the gate capacitance C_{gs} is desired so that the MOSFET channel is already switched-off before the drain-source voltage drastically rises, thus keeping the overlapping of the voltage transient and MOSFET channel current transient small. This actually demands a large gate current I_{g}, which means a large negative gate voltage $V_{\mathrm{gate,neg}}$ and a low total off-state gate resistance $R_{\mathrm{g,off,tot}} = R_{\mathrm{g,int}} + R_{\mathrm{g,off}}$

$$I_{\mathrm{g}}(t) = (V_{\mathrm{Cgs}}(t) - V_{\mathrm{gate,neg}})/R_{\mathrm{g,off,tot}}. \tag{1}$$

For the given specifications in **Table I**, even if an external gate resistance of $R_{\mathrm{g,off}} = 0\,\Omega$ and a Zener voltage of $V_{\mathrm{DZ1}} = V_{\mathrm{DZ2}} = 6.8\,\mathrm{V}$ is selected, the high internal gate resistance $R_{\mathrm{g,int}}$ strongly limits the maximum gate current to a moderate value of $I_{\mathrm{g}} = 1.5\,\mathrm{A}$ ($V_{\mathrm{Cgs}}(t) \approx V_{\mathrm{th}}$ assumed). Consequently, as it is shown in the following, since the current in the Miller capacitance C_{dg} increases proportionally with the load current I_{L}, a fast discharge of the gate capacitance C_{gs} is not anymore. This could result in a large overlapping of the voltage and MOSFET channel current transient and thus in increased soft-switching losses. Considering the capacitive MOSFET model in **Fig. 6 a)** and assuming that the gate-source capacitance C_{gs} is already discharged before the voltage v_{ds} across the MOSFET rises, the gate current I_{g} has to be at least as large as the Miller current I_{dg} in order to prevent C_{gs} to be charged again and not to slow down the voltage slope $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$. Since the MOSFET channel is already off during the voltage transient, the load current I_{L} has to flow through the output capacitance $C_{\mathrm{oss}} = C_{\mathrm{dg}} + C_{\mathrm{ds}}$ of the upper and lower switch in the half-bridge. Hence, the Miller current I_{dg} can be calculated depending on the load current I_{L} and the capacitances C_{dg} and C_{ds} as

$$I_{\mathrm{dg}}(t) = c \cdot I_{\mathrm{L}} \cdot C_{\mathrm{dg}}/(C_{\mathrm{dg}} + C_{\mathrm{ds}}), \tag{2}$$

where c is the share of the load current I_{L} between the upper and lower switch in a bridge-leg, which actually depends on the non-linear voltage dependent output capacitance. As shown in **Fig. 6 a)**, the output capacitance of the switch S_2, which was conducting and now is turned-off, can be magnitudes larger than the output capacitance of the complementary switch S_1, which was actually blocking the full input voltage ($C_{\mathrm{oss}}(0V) \gg C_{\mathrm{oss}}(V_{\mathrm{in}})$). Thus, at the beginning of the switching transient almost the full load current I_{L} is flowing through the switch which is turning-off. This statement is also strengthened by the fact that the commutation loop inductance L_{σ} prevents the current to flow through S_1 until a positive voltage is applied to L_{σ}, which enables the current to commutate to S_1. Hence, as a worst case approximation either $c = 1$ can be assumed or the more realistic voltage dependent output capacitance values given in the manufacturer's datasheet at around $0\,\mathrm{V}$ and V_{in} can be used in order to calculate the factor c.

In reality, as soon as the gate voltage v_{gs} is falling below the Miller voltage $V_{\mathrm{Cgs,Miller}}$, the MOSFET channel current

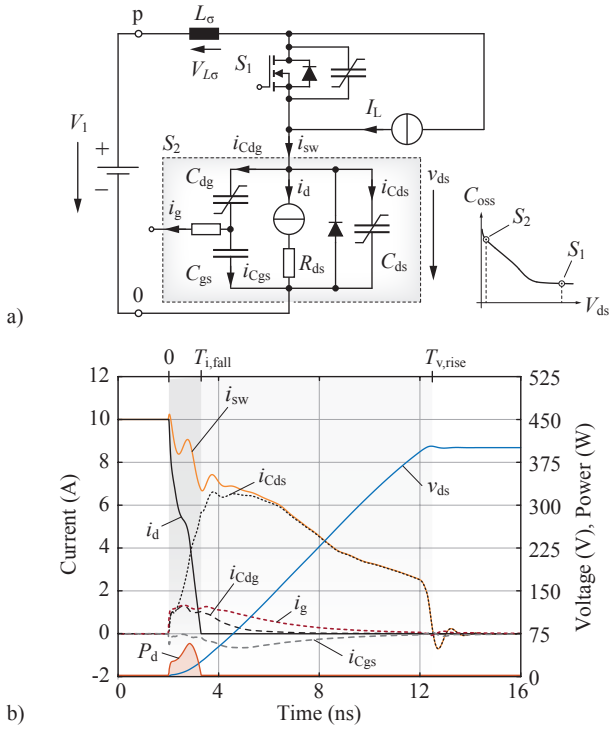

Fig. 6: Analysis of the soft-switching turn-off transition with **a)** the capacitive model of the MOSFET and **b)** the turn-off transition simulated with Gecko Circuits considering the non-linear MOSFET capacitances and parasitic inductances.

will become smaller than the load current I_{L}, thus the current difference has to flow through the output capacitances C_{dg} and C_{ds} leading to an immediate increase of the switch voltage V_{ds}. Consequently, a certain overlapping of the voltage and MOSFET channel current transient cannot be avoided (cf. **Fig. 6 b)**) and during this time interval the gate driver not only has to carry the Miller current I_{dg} but also has to further discharge C_{gs} from $V_{\mathrm{Cgs,Miller}}$ to V_{th} with the gate-source current

$$I_{\mathrm{gs}}(t) = (V_{\mathrm{Cgs,Miller}} - V_{\mathrm{th}}) \cdot C_{\mathrm{gs}}/T_{\mathrm{i,fall}}, \tag{3}$$

where $T_{\mathrm{i,fall}}$ is the current fall time in the MOSFET channel. The Miller voltage $V_{\mathrm{Cgs,Miller}}$ can either be determined from the measured characteristics provided in the datasheet or can be calculated with the transconductance g_{m} as $V_{\mathrm{Cgs,Miller}} = I_{\mathrm{ds}}/g_{\mathrm{m}} + V_{\mathrm{th}}$. As can be noticed, since I_{dg} increases proportionally with the load current I_{L}, based on Kirchhoff's law ($I_{\mathrm{g}} = I_{\mathrm{dg}} + I_{\mathrm{gs}}$) the discharge of C_{gs} is slowed down, i.e. $T_{\mathrm{i,fall}}$ is prolonged. With the given specifications, for example, it is found that $c \approx 0.75$ and that for a load current of around $I_{\mathrm{L}} = 10\,\mathrm{A}$ the Miller current I_{dg} already reaches the calculated maximum gate current $I_{\mathrm{g,max}}$. This means that for $I_{\mathrm{L}} > 10\,\mathrm{A}$ the Miller current I_{dg} would exceed the $I_{\mathrm{g,max}}$ and would recharge C_{gs}. Consequently, with the increasing gate voltage v_{gs} also the MOSFET channel current rises, which keeps the Miller current I_{dg} below $I_{\mathrm{g,max}}$. In other words, the Miller current I_{dg} is limited by the maximum gate drive current $I_{\mathrm{g,max}}$ and the voltage slope of v_{ds} is slowed down resulting in a larger overlapping of the voltage and MOSFET channel current transient. However, this limitation of I_{dg} typically only

takes place at low drain-source voltages (cf. $0...T_{\mathrm{i,fall}}$ in **Fig. 6 b)**), since the Miller capacitance C_{dg} - and hence also I_{dg} - strongly decrease with increasing v_{ds} and at higher drain-source voltages I_{dg} becomes negligible compared to I_{ds} (cf. $T_{\mathrm{i,fall}}...T_{\mathrm{v,rise}}$ in **Fig. 6 b)**). Accordingly, for the calculation of the voltage rise time $T_{\mathrm{v,rise}}$, where the output capacitances of both switches have to be charged/discharged from 0 V to V_{in} and vice versa, the voltage dependent capacitances C_{ds} and C_{dg} can be substituted by their charge equivalent capacitances $C_{\mathrm{ds,Qeq}}$ and $C_{\mathrm{dg,Qeq}}$ (cf. **Table I**), thus $c = 0.5$. In a first approximation the resulting voltage rise time is then $T_{\mathrm{v,rise}} = V_{\mathrm{in}} \cdot (C_{\mathrm{ds,eq}} + C_{\mathrm{dg,eq}})/(c \cdot I_{\mathrm{L}})$. Assuming that during $T_{\mathrm{i,fall}}$ the current linearly decreases from I_{L} to 0 A and the voltage V_{ds} linearly rises from 0 V to $V_{\mathrm{ds}}(T_{\mathrm{i,fall}}) = T_{\mathrm{i,fall}}/T_{\mathrm{v,rise}} \cdot V_{\mathrm{in}}$, the switching energy which is lost due to the overlapping can be approximated as

$$E_{\mathrm{overlap}} = \frac{1}{6} \cdot V_{\mathrm{in}} \cdot I_{\mathrm{L}} \cdot \frac{T_{\mathrm{i,fall}}^2}{T_{\mathrm{v,rise}}}. \tag{4}$$

For the selected dimensioning of the gate drive and a load current of $I_{\mathrm{L}} = 10$ A this would lead to only $E_{\mathrm{overlap}} \approx 100$ nJ of additional soft switching losses, which is orders of magnitudes lower than the measured soft-switching losses as shown later. Clearly, it has to be mentioned that this calculation is only used as a rule of thumb for the dimensioning of the gate drive circuit. However, even in the circuit simulation (Gecko Circuits), where the non-linearity of the MOSFET capacitances as well as possible parasitic inductances due to layout or device packages were considered, the simulated switching losses were at similar low levels (cf. **Fig. 6 b)**). Hence, the soft-switching losses can not only be assigned to the overlapping of voltage and MOSFET current transient and thus other loss mechanisms, e.g. output capacitance related losses during charging and discharging, are presumed and are still subject of research.

In contrast to the soft turn-off, the hard turn-off transient is much less critical because the current is only commutating from the MOSFET channel to the anti-parallel diode. However, a sufficiently negative gate voltage $V_{\mathrm{gate,neg}}$ and a low off-state gate resistance $R_{\mathrm{g,off,max}}$ are also required in order to guarantee a safe and reliable operation of the half-bridge. In analogy to soft-switching, the hard turn-on transient of the half-bridge's complementary switch causes a high voltage slope $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ and a Miller current I_{dg} charging the gate capacitance C_{gs} of the switch which is actually in the off-state. With a suitable selection of $V_{\mathrm{gate,neg}}$ and $R_{\mathrm{g,off,max}}$, a possible charging of C_{gs} above V_{th} (parasitic turn-on) has to be prohibited. Assuming constant $\mathrm{d}V_{\mathrm{ds}}/\mathrm{d}t = \Delta V_{\mathrm{ds}}/\Delta t$, constant charge equivalent capacitances $C_{\mathrm{ds,Qeq}}$ and $C_{\mathrm{dg,Qeq}}$ (cf. **Table I**), $C_{\mathrm{s}} \gg C_{\mathrm{gs}}$, $V_{\mathrm{Cgs}}(0) = V_{\mathrm{neg}}$, and neglecting any inductances, the voltage $v_{\mathrm{gs}}(t)$ as well as the final value at the end of the voltage slope $v_{\mathrm{Cgs}}(T_{\mathrm{v,rise}} = V_{\mathrm{in}} \cdot \Delta V_{\mathrm{ds}}/\Delta t)$ can be calculated based on the capacitive MOSFET model (cf. **Fig. 3 b)**) depending on a given $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ as

$$V_{\mathrm{Cgs}}(t) = V_{\mathrm{neg}} + I_{\mathrm{dg}} \cdot R_{\mathrm{g}} \cdot (1 - \mathrm{e}^{\frac{-t}{R_{\mathrm{g}} \cdot C_{\mathrm{gs}}}}). \tag{5}$$

Still enabling a reliable half-bridge operation, with the selected negative gate voltage of $V_{\mathrm{gate,neg}} = V_{\mathrm{DZ1}} = V_{\mathrm{DZ2}} =$ 6.8 V and the internal gate resistance $R_{\mathrm{g,int}} = 5.3\,\Omega$, the maximum allowed voltage slope during hard switching is $\mathrm{d}v_{\mathrm{ds,max}}/\mathrm{d}t \approx 600\,\mathrm{kV/\mu s}$ at $V_{\mathrm{in}} = 400$ V. So far for the calculation of the maximum $\mathrm{d}v_{\mathrm{ds,max}}/\mathrm{d}t$ it was always assumed that $C_{\mathrm{s}} \gg C_{\mathrm{gs}}$, since in this case C_{s} emulates an ideal bipolar gate drive supply. It also has to be considered, however, that the gate drive losses are mainly defined by C_{s}. During the turn-on transient C_{s} is charged to $V_{\mathrm{in}} - V_{\mathrm{Dgs}}$ and during turn-off it is discharged to $V_{\mathrm{DZ1}} = V_{\mathrm{DZ2}}$, which means that in each switching cycle $T_{\mathrm{s}} = 1/f_{\mathrm{s}}$ the source V_{in} has to supply the charge difference $\Delta Q = C_{\mathrm{s}} \cdot ((V_{\mathrm{in}} - V_{\mathrm{Dgs}}) - V_{\mathrm{DZ1}})$. Thus, the resulting gate drive losses can be calculated as

$$P_{\mathrm{gd}} = \Delta Q \cdot V_{\mathrm{in}} \cdot f_{\mathrm{s}}. \tag{6}$$

Consequently, in order to keep the gate drive losses low, either the voltage difference or the capacitance C_{s} has to be small, where the minimum series capacitance C_{s} should be an order of magnitude larger than C_{gs}. Considering C_{gs} of the selected GaN GIT (cf. **Table I**), the series capacitance is set to $C_{\mathrm{s}} = 10$ nF, which e.g. for a switching frequency of $f_{\mathrm{s}} = 1$ MHz results in $P_{\mathrm{gd}} = 288$ mW. A summary of the selected gate drive values is given in **Table II**. In **Fig. 7 a)** and **b)** the measured gate voltages for the two switching frequencies $f_{\mathrm{s}} = 10$ kHz and $f_{\mathrm{s}} = 1$ MHz are shown, confirming the described operation of the gate drive circuit

TABLE II: Selected values for the proposed and realized gate drive circuit shown in **Fig. 5 a)**.

Component	*Value*
$R_{\mathrm{g,1}}$	5 Ω
$R_{\mathrm{g,2}}$	0 Ω
R_3 (for $I_{\mathrm{q}} = 10$ mA)	170 Ω
R_4	100 kΩ
V_1	12 V
$V_{\mathrm{DZ1}} = V_{\mathrm{DZ2}}$	6.8 V

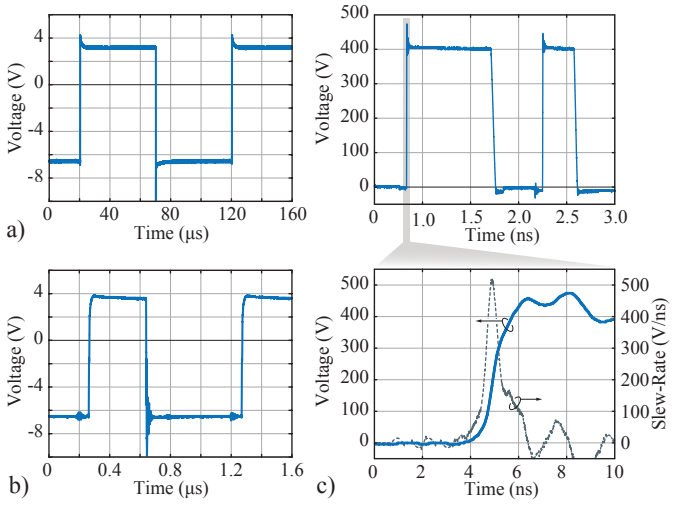

Fig. 7: Measured gate voltages for the two switching frequencies **a)** $f_{\mathrm{s}} = 10$ kHz and **b)** $f_{\mathrm{s}} = 1$ MHz and **c)** the measured maximum voltage slope of above $500\,\mathrm{kV/\mu s}$ achieved with hard switching.

with the correct voltage levels. In addition, the gate drive circuit's reliability was tested under hard switching condition with $\mathrm{d}v_{\mathrm{ds,max}}/\mathrm{d}t$ above $500\,\mathrm{kV/\mu s}$ as shown in **Fig. 7 c)**.

III. Switching Loss Measurements

A. Measurement Setups

The designed gate drive is also used to evaluate the hard- and soft-switching performance of the GaN GIT in half-bridge configuration. Usually, switching loss measurement are performed with a double pulse test where both, the hard- and soft-switching losses, can be measured in one sweep by electrically measuring the device voltage and current during a turn-on and turn-off transient. For the evaluation of devices featuring slow switching transients, e.g. in the range of hundreds of ns, this method allows to obtain reliable switching loss data. However, for fast switching transients in the ns- or tens of ns-range, which can be achieved with WBG devices, the accuracy of the measured switching losses already suffers e.g. from offsets, from improper deskew and jitter between current and voltage probes, from limited bandwidths of the passive or active probes, or from any other measurement distortion like common mode. Furthermore, not only the measurement itself but also the processing and evaluation of the measured data is crucial, like how the offsets are treated and especially in which time interval the measured power is integrated in order to extract the loss energy, e.g. is any ringing present after the switching transient accounted for the switching losses or not. This applies regardless of whether hard- or soft-switching measurements are performed, since due to the small output capacitance of WBG devices already with small load currents also in soft-switching transitions large current and voltage slopes can be achieved.

However, the double pulse test is almost the only way to measure the hard-switching losses for different voltage and current values, because a continuous operation would definitely lead to an overheating and damage of the Device Under Test (DUT); or the repetition rate is reduced in such a way that the DUT is operated in a thermally uncritical level and the continuous power is e.g. measured with a calorimetric setup at constant temperature. Nevertheless, since most semiconductor materials show temperature dependent hard-switching losses and therefore a large number of measurements has to be performed at different currents, voltages and temperatures as well as the fact that calorimetric measurements can take a considerable amount of time until the thermal equilibrium is reached, in the following the hard-switching losses are performed with the double pulse setup shown in **Fig. 9 a)**.

Another aggravating factor in measuring the soft-switching losses with the double pulse test is the fact that in contrast to the hard-switching measurements, where in both switching transitions energy is lost and the total switching losses is the sum of these losses, in soft-switching measurements in one switching transition energy is stored in the DUT's output capacitance and in the other is retrieved. This means that the resulting and typically small soft-switching losses is the difference of two large values, and thus can lead to tremendously wrong loss calculation results. Assuming that for example the soft-switching losses make up to $10\,\%$ of the energy stored during one transition and that due to some reason the stored and retrieved energy are measured with an error of $\pm 10\,\%$, the error in the energy difference in the worst case could result either in three times larger soft-switching losses or even to an energy gain. In contrast, for the hard-switching losses the error of the sum would still stay below $10\,\%$. Another disadvantage of the double pulse measurement is that in order to measure the device current, a shunt or a current transformer has to be introduced into the commutation loop, which compared to the final layout increases the commutation inductance significantly, and thus has a negative influence on the measured waveforms and losses, e.g. because of ringing due to increased common source inductance which could demand higher gate resistances and consequently leads to higher losses [12].

Due to the mentioned drawbacks a indirect measurement approach is followed in this paper in order to accurately measure the soft-switching losses of the GaN GIT. Based on the buck converter topology shown in **Fig. 8 a)**, the GaN GIT bridge leg is continuously operated in triangular current mode with a duty cycle of $50\,\%$ considering an appropriate dead time T_{dt} (**Fig. 8 b)**). Since no load is applied to the converter, only the power loss is supplied from the input and only reactive power is transferred between the DC-link and the output capacitor which in combination with the symmetric bridge voltage v_{T2} leads to a symmetric current excitation in the output inductor i_{L} and a constant output voltage of $V_{\mathrm{out}} = V_{\mathrm{in}}/2$. The measurements were performed with an input voltage of $V_{\mathrm{in}} = 400\,\mathrm{V}$. In order to determine the soft-switching losses at different current levels, the current ripple in the output inductor is controlled by varying the switching frequency. This means that a small current ripple requires a high switching frequency and vice versa, thus, the product of the current ripple times the switching frequency is constant. Based on the assumption that in a first approximation the soft-switching losses are proportional to the switched current, this

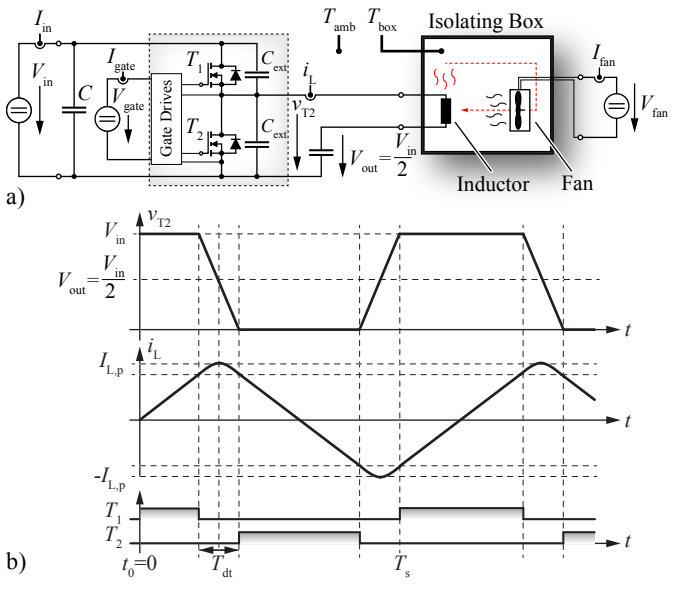

Fig. 8: a) Calorimetric measurement setup used to determine the soft-switching losses and **b)** waveforms of the bridge voltage v_{T2}, the inductor current i_{L} and the appropriate gate signals of the two switches T_1 and T_2.

relation has the advantage that independently from the selected switching frequency or switched current the same losses are expected and the DUT is always operated at similar thermal conditions and thus also at similar $R_{\mathrm{ds,on}}$.

The soft-switching losses are indirectly deduced from the DC-input power P_{in} minus the losses in the output inductor P_{L} and the gate drive circuits P_{gd}. The input and output capacitors are realized with ceramic capacitors (CERALink), which feature an extremely low ESR making the resulting losses negligibly small. This is also proven by the fact that there is no noticeable temperature rise during operation. The input power P_{in} can be precisely measured based on the DC-values V_{in} and I_{in}. This also applies to the losses in the gate drive circuits $P_{\mathrm{gd}} = U_{\mathrm{gate}} \cdot I_{\mathrm{gate}}$, which are fed in by an auxiliary power supply. The losses of the output inductor P_{L} are measured with a calorimetric setup, i.e. the inductance is placed into a thermally insulated box and its dissipated heat is measured based on the the temperature difference between the temperature in the box T_{box} and the ambient temperature T_{amb} times the thermal resistance R_{th} of the insulated box ($P_{\mathrm{box}} = R_{\mathrm{th}}(T_{\mathrm{box}} - T_{\mathrm{amb}})$). The thermal resistance $R_{\mathrm{th}} = \Delta T/P$ can easily be determined by feeding a certain DC-power P_{heat} into an separate heating resistor R_{heat} and measuring the resulting temperature difference $\Delta T = T_{\mathrm{box}} - T_{\mathrm{amb}}$. In order to guarantee an homogeneous temperature distribution inside the box, an additional fan is circulating the hot air. The losses of the fan, which are also fully dissipated inside the box, correspond to the fan's DC-input power $P_{\mathrm{fan}} = U_{\mathrm{fan}} \cdot I_{\mathrm{fan}}$. The inductor losses are then $P_{\mathrm{L}} = P_{\mathrm{box}} - P_{\mathrm{fan}}$.

For the sake of completeness, since calorimetric measurements can take a considerable amount of time until the thermal equilibrium is reached, the inductor losses could also be measured more quickly if an air coil is used. Since in this case only copper losses are expected, the inductor losses can be calculated based on the AC-resistance $R_{\mathrm{ind,AC}}(f)$, which can be measured with an impedance analyzer, and the Fourier transform of the measured inductor current $I_{\mathrm{ind,AC}}(f)$. In order to achieve a more precise estimation of the inductor losses, the inductor's AC-resistance could be measured also at different temperatures $R_{\mathrm{ind,AC}}(f, T)$. Alternatively, both methods can be combined i.e. placing the air coil into the insulated box, in order to further increase the measurement accuracy.

Nevertheless, the total semiconductor losses consisting of conduction and switching losses can now be deduced from $P_{\mathrm{semi}} = P_{\mathrm{in}} - P_{\mathrm{L}}$. To obtain only the switching losses P_{switch}, the conduction losses P_{cond} have to be subtracted from the total semiconductor losses P_{semi}. The conduction losses can be calculated based on the rms-value of the current $I_{\mathrm{semi,rms}}$ in the switches and the on-state resistance $R_{\mathrm{ds,on}}$ of the GaN GIT ($P_{\mathrm{cond}} = R_{\mathrm{ds,on}} \cdot I^2_{\mathrm{semi,rms}}$), where $I_{\mathrm{semi,rms}}$ is quasi equal to the output inductor's rms-value $I_{\mathrm{L,rms}}$. Assuming that at the beginning of the turn-off sequence the MOSFET channel is already blocking before the drain-source voltage increases, it only has to be considered that during the dead time interval the inductor current $I_{\mathrm{L,rms}}$ is not flowing through $R_{\mathrm{ds,on}}$ but is charging the output capacitances, which means that $I_{\mathrm{semi,rms}}$ is slightly smaller than $I_{\mathrm{L,rms}}$. For low switching frequencies where the dead time is considerably shorter than the switching period, this mismatch can be neglected ($I_{\mathrm{semi,rms}} \approx I_{\mathrm{L,rms}}$); for higher switching frequency, however, it has to be considered in the current calculation. In addition, in each loss measurement the actual case temperature $T_{\mathrm{semi,c}}$ is measured in order to determine the actual $R_{\mathrm{ds,on}}$ from the temperature dependent on-state resistance $R_{\mathrm{ds,on}}(T)$ given in the manufacturer's data sheet.

B. Experimental Results

As already mentioned, the hard-switching losses are determined with the double pulse setup shown in **Fig. 9 a)**. For the current measurement a coaxial shunt (SDN-414-10 from T&M Research Products, $R_{\mathrm{s}} = 0.1\,\Omega$, DC-2 GHz rated bandwidth) is used. The total commutation loop inductance loop is around $6 - 7\,\mathrm{nH}$, where the major contribution is coming from the coaxial shunt's leads. Each switch T_1 and T_2 is realized with one GaN GIT (IFX 5893, Samples from Infineon). In **Fig. 9 b)** the measured hard-switching losses for a voltage range of $100{-}400\,\mathrm{V}$ and a current range of $2{-}18\,\mathrm{A}$ at $25\,^{\circ}\mathrm{C}$ are shown. As expected, the losses of both switching transients increase with the switched voltage and the total switching losses are dominated by the turn-on losses which also increase with the switched load current. Furthermore, the measured hard-switching losses match really well the experimental results found in [9].

The soft-switching losses are determined with the described calorimetric setup. The loss measurements are performed for four different half-bridge configurations. First, the soft-switching losses were evaluated for the two cases where the half bridge is either realized with one GaN GIT per switch or two parallel GaN GITs per switch. The corresponding measured soft-switching losses are shown in **Fig. 10**. As can be noticed, up to around $11\,\mathrm{A}$ the soft-switching losses with one GaN GIT are lower than with two GaN GITs in parallel per switch. At higher currents for one GaN GIT the losses

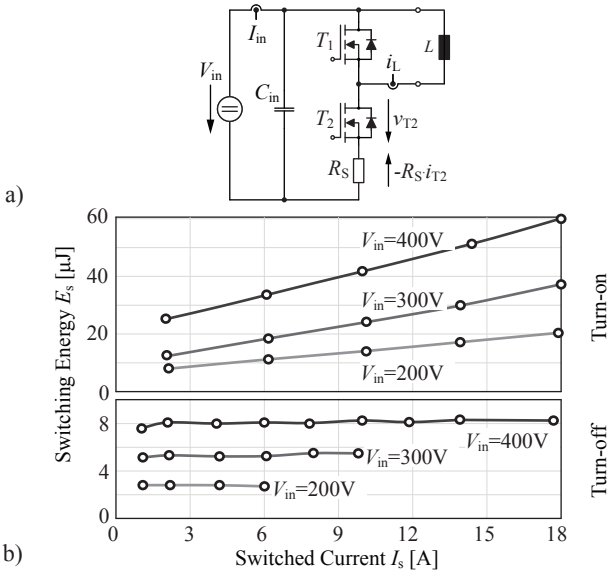

Fig. 9: a) Double pulse test setup used to perform the hard-switching loss measurements and **b)** measured hard-switching losses E_{s} (turn-on and turn-off) depending on the switched current I_{L} and the input voltage V_{in}.

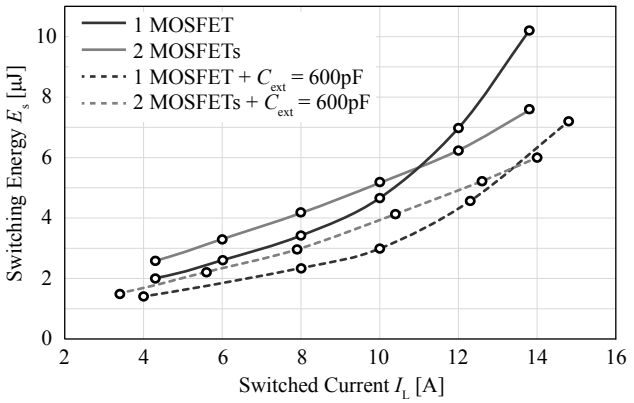

Fig. 10: Measured soft-switching losses E_s depending on the switched current I_s for four different half-bridge assemblies.

TABLE III: Coefficients of the polynomial interpolation for the current range from $4\,\mathrm{A}$ to $14\,\mathrm{A}$ where $E_\mathrm{s}(I_\mathrm{s}) = k_0 + k_1 \cdot I_\mathrm{s} + k_2 \cdot I_\mathrm{s}^2 + k_3 \cdot I_\mathrm{s}^3$.

	1 MOSFET	*2 MOSFETs*	*1 MOSFET +* $C_\mathrm{ext} = 600\,\mathrm{pF}$	*2 MOSFETs +* $C_\mathrm{ext} = 600\,\mathrm{pF}$
$k_0[\mu\mathrm{J}]$	1.0812	1.0933	0.7307	0.7435
$k_1[\mu\mathrm{J/A}]$	0.4106	0.3549	0.2689	0.1942
$k_2[\mu\mathrm{J/A^2}]$	-0.064	-0.0034	-0.0348	0.0099
$k_3[\mu\mathrm{J/A^3}]$	0.0059	0.0008	0.0031	0.0002

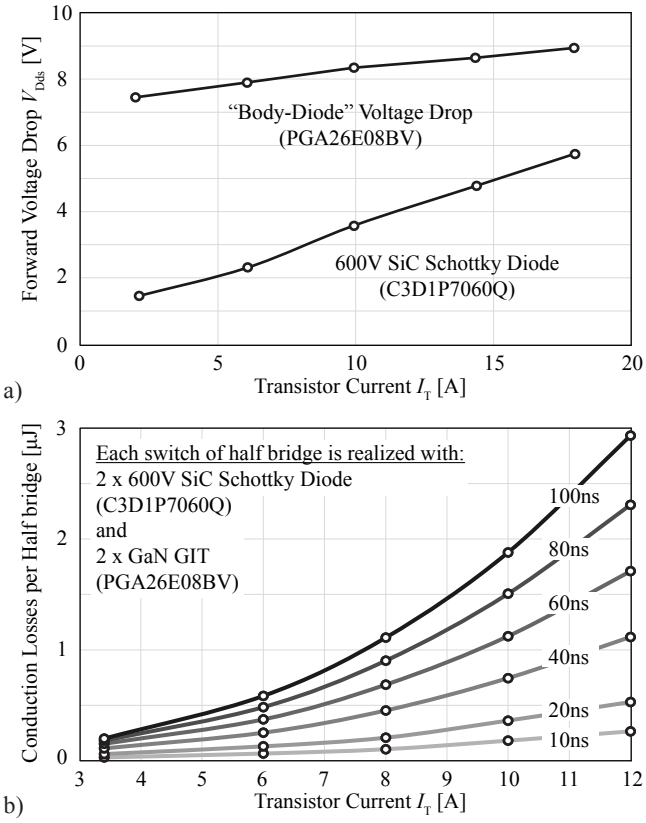

Fig. 11: Measured conduction losses due to the additional conduction of the anti-parallel diode during the commutation interval.

strongly increase, while for two GaN GITs the losses show an almost linear current dependency.

The same measurement have been evaluated for different turn-on and turn-off resistance and also the series capacitance in the gate drive circuit was modified ($C_\mathrm{s} = 100\,\mathrm{nF}$ instead of $10\,\mathrm{nF}$), however, no influence on the switching losses could be noticed. Since even with a turn-off resistance of $R_{\mathrm{g},2} = 0\,\Omega$ the switching losses are not decreasing, it is expected that the switching losses are primarily turn-off losses, which on the one hand arise due to the high internal gate resistance of $R_{\mathrm{g,int}} = 5.3\,\Omega$ which inhibits a fast discharge of the gate-source capacitance and an abrupt commutation of the switch current from the MOSFET channel to the output capacitance and on the other hand due to potential output capacitance related losses during charging and discharging. Therefore, in order to prevent the drain-source voltage to noticeably increase before the GaN GIT is completely turned-off, an external output capacitance C_ext is placed in parallel to the switches slowing down the voltage transient (cf. **Fig. 8 a)**). As a result, by increasing the external output capacitance in steps of $100\,\mathrm{pF}$ the switching losses steadily decrease. At the same time, however, increasing the output capacitance also demands either a higher charging current (higher conduction losses) or results in longer dead times at the same current (higher reactive power and duty cycle limitations) in order to ensure soft-switching. Therefore, as a trade-off an additional capacitance of $C_\mathrm{ext} = 600\,\mathrm{pF}$ is selected and the measurement for the two mentioned configuration with either one or two GaN GITs per switch is repeated. As shown in **Fig. 10**, compared to the measurement without external capacitance C_ext, the switching losses still show the same current dependency but now are strongly decreased. For the current range from $4\,\mathrm{A}$ to $14\,\mathrm{A}$ the measured losses are interpolated with a third order polynomial, which allows a simple calculation of switching losses e.g. in an optimization procedure of a converter system. The corresponding coefficients are listed in **Table III**.

Furthermore, it has to be mentioned that the GaN GIT shows a large voltage drop in reverse conduction mode, which could lead to falsified switching loss measurements (cf. **Fig. 11 a)**). Therefore, on the one hand external SiC-diodes (C3D1P7060Q, CREE) are placed in anti-parallel to the GaN GIT in order to keep the forward voltage drop low, and on the other hand the dead time is adjusted in such a way that after the soft-switching transition these SiC-diodes do not or just hardly conduct. In real system operation, however, this current dependent dead time usually cannot be measured but is calculated. Hence, to avoid a possible half-bridge shoot through, a certain margin is added to the calculated dead time resulting in additional conduction losses of the anti-parallel diode. Therefore, this loss penalty is also analyzed for different load currents by increasing the dead time in steps of $20\,\mathrm{ns}$. In **Fig. 11 b)** the measured conduction losses for two parallel GaN GIT's with two parallel connected SiC-diodes (2 x C3D1P7060Q, CREE) are shown. As can be noticed, this additional conduction losses only make a small contribution to the switching losses; e.g. if the diode conduction time can be held below $40\,\mathrm{ns}$, the additional losses are around $1\,\mu\mathrm{J}$ at $12\,\mathrm{A}$.

IV. Conclusion

In this paper a simple and reliable gate drive circuit for driving GaN switches is presented. In spite of a unipolar supply voltage, the proposed gate drive circuit enables a bipolar gate voltage by means of a decoupling capacitance. On the one hand, the gate drive circuit features a duty cycle independent high dynamic performance during switching transients and on the other hand guarantees a reliable operation during on- and off-states prohibiting parasitic turn-on even during fast switching with highest voltage slopes. Its reliability and proper operation is verified for different switching frequencies up to $1\,\mathrm{MHz}$ and voltage slopes up to $500\,\mathrm{kV/\mu s}$. In addition, the proposed gate drive was used to evaluate the switching performance of a GaN GIT under soft- and hard-switching conditions. While the hard-switching losses are measured with a conventional double pulse test, the soft-switching losses are evaluated with a calorimetric measurement setup, since the achievable accuracy of soft-switching loss measurements in a double pulse test is poor. Thus, in addition to the presented gate drive circuit, the performed evaluation of the GaN GIT provides a basis for further optimization of different converter systems.

Acknowledgment

The authors would like to thank Infineon Technologies Austria AG for providing the GaN GIT devices used in this study.

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