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***Abstract*—Global energy consumption in AI-related data centers is expected to double by 2026. This rapid growth necessitates an upgrade in their power supply architecture, where isolated three-phase (3-Φ) ac/dc converters serve as fundamental building blocks. However, state-of-the-art two-stage ac/dc-dc/dc converter concepts suffer from limited power conversion efficiency and power density. This paper proposes a novel three-phase integrated active filter isolated matrix-type rectifier (IAF-iMR) that enables high-efficiency, direct (single-stage) ac/dc conversion with high power density, while maintaining reduced modulation and control complexity compared to conventional isolated matrix-type ac/dc converters. By incorporating bipolar bidirectional switches, the proposed IAF-iMR directly converts low-frequency three-phase mains line-to-line voltages into a high-frequency switched ac voltage across the transformer's primary-side winding, eliminating one power conversion stage compared to two-stage or quasi-single-stage configurations and enhancing power conversion efficiency.**

The paper first explains the operating principle of the IAF-iMR using equivalent circuits, which are verified by detailed circuit simulations. Furthermore, component stresses are analyzed to guide component selection, followed by a qualitative comparative evaluation against alternative isolated three-phase ac/dc converter concepts. Finally, a novel matrix-type isolated-three-phase-HF-link three-phase ac/dc converter (i3X-Rectifier) is introduced as a next-generation high-power data center power supply solution. The proposed i3X-Rectifier employs a three-phase transformer to mitigate overstress limitations of single-phase isolation transformers, improving performance and compactness.

***Index Terms*—Single-Stage Isolated AC/DC Converter, Three-Phase Rectifier, Integrated Active Filter (IAF), Matrix Converter (MC), Dual Active Bridge (DAB), Third-Harmonic Current Injection, AI-Centric Data Center Power Supply**

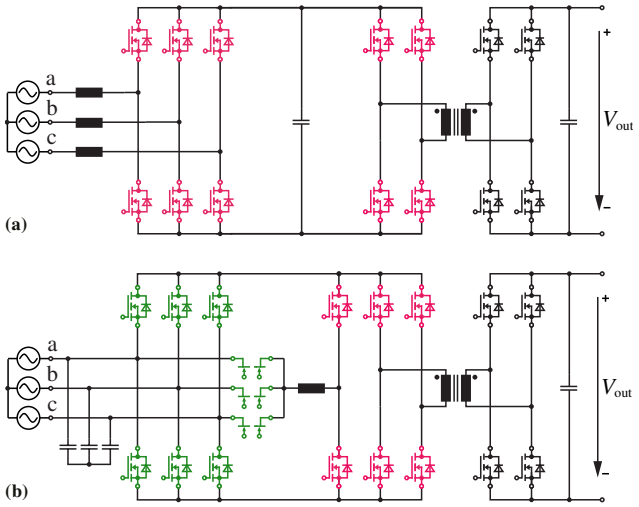

Fig. 1: (a) Schematic of a typical two-stage isolated three-phase (3-Φ) ac/dc converter, comprising a two-level Power Factor Correction (PFC) rectifier front-end and an isolated dc/dc output stage. **(b)** Schematic of a quasi-single-stage converter, featuring an integrated active filter (IAF) front-end for ac/dc conversion and a dc/dc stage for galvanic isolation. The basic operating principle of the IAF front-end is explained in **Fig. 2** [7]. Note that the transistors connected between the 3-Φ mains and the transformer's primary winding are categorized based on their switching frequencies: the green transistors operate at low switching frequencies (multiples of the mains fundamental frequency), while the pink ones operate at high frequencies (e.g., in the range of hundreds of kHz).

I. Introduction

Global energy consumption in AI-related data centers is projected to grow significantly, from 460 TWh in 2022 to over 1000 TWh by 2026—nearly doubling within four years [1]. For instance, AI model training systems, such as those used for ChatGPT, consume more than 80 kW per rack, while advanced setups like Nvidia's GB200 servers require up to 120 kW per rack [2], [3]. This rapid expansion underscores the urgent need to upgrade data centers' power architectures to enable highly efficient power conversion from medium-voltage distribution (13.2 or 25 kVac) to the chip-level voltages (below 1 Vdc) [4]–[6].

Traditional 48 Vdc rack power systems can no longer support the substantially increasing power demands of AI-related data centers, necessitating a transition to next-generation +/− 400 Vdc power distribution system [8]. Increasing the distribution voltage to +/− 400 Vdc significantly reduces power distribution losses and enables megawatt-level power feeding capability, accommodating IT payload expansions. Compared to conventional ac distribution systems, the bipolar dc distribution system offers key advantages, including easier integration of renewable energy resources and reduced raw material consumption, such as copper [9], [10], and provides a 400 Vdc supply to downstream step-down dc/dc converters.

As a result, ac/dc power conversion will shift from IT racks to sidecar power racks, enabling a single power rack to supply multiple IT payload racks with improved efficiency and flexibility [8]. Isolated three-phase (3-Φ) ac/dc converters are essential building blocks of sidecar power racks, and they must achieve high efficiency, high power density, and minimal complexity. State-of-the-art solutions typically separate the functions of sinusoidal mains current shaping and output voltage

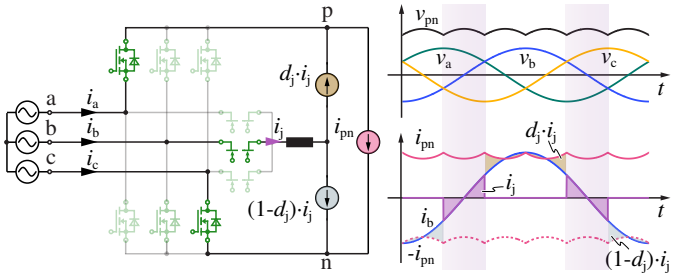

Fig. 2: Basic operating principle of the integrated active filter (IAF) front-end, considering a 60° interval of the mains period where phase voltages $v_a > v_b > v_c$. A 3-Φ unfolder rectifies the 3-Φ mains voltages and outputs a six-pulse-shaped voltage v_{pn} (the envelope of the mains line-to-line voltage) [21], [22]. For constant power transfer, the downstream dc/dc stage needs to guarantee a complementary inverse six-pulse-shaped current i_{pn}. The injection bridge-leg connects to the phase with the lowest absolute voltage, ensuring the sinusoidal shaping of all 3-Φ mains currents.

isolation/regulation by employing a power factor correction (PFC) rectifier at the front-end, followed by an isolated dc/dc output stage, resulting in a two-stage power conversion process, as shown in **Fig. 1a**. However, this two-stage approach can potentially lead to lower overall efficiency, reduced power density, and increased implementation complexity. As a result, matrix-type single-stage and quasi-single-stage converter concepts are attracting growing interest in recent research [7], [11]–[20].

For quasi-single-stage topologies, one approach is an integrated active filter (IAF)-based ac/dc converter, where a 3-Φ unfolder directly interfaces with the 3-Φ mains (see ac-side filter capacitors in **Fig. 1b**) using a diode bridge[1] and three bipolar bidirectional switches[2], along with an injection bridge-leg, eliminating the need for an intermediate capacitor. **Fig. 2** illustrates the basic operating principle of the IAF front-end, where the 3-Φ unfolder rectifies the 3-Φ mains voltages and outputs a six-pulse-shaped voltage v_{pn} (the positive envelope of the 3-Φ mains line-to-line voltages) to supply the downstream dc/dc stage [21], [22]. The dc/dc stage draws a complementary inverse six-pulse-shaped input current i_{pn}, ensuring constant power transfer. Considering a 60° interval of the mains period with a mains voltage relation $v_a > v_b > v_c$, the current i_j is injected into phase b (the phase with the lowest absolute instantaneous value) and is regulated to follow i_b, proportional to v_b in order to ensure ohmic mains behavior [26], [27]. By appropriately assigning a duty cycle d_j, the other two phase currents are given by $i_a = i_{pn} - d_j \cdot i_j$ and $i_c = -i_{pn} - (1 - d_j) \cdot i_j$. Consequently, the injection bridge-leg ensures sinusoidal shaping of all 3-Φ mains currents [27]. Note that the transistors of the injection bridge-leg conduct relatively small currents, with a maximum value of only half the phase peak current. The IAF-based ac/dc converter offers several advantages over other typical 3-Φ PFC rectifiers, including reduced switching losses, less magnetics efforts, and lower control complexity.

[1]Switches are advantageously arranged antiparallel to the diodes for synchronous rectification in order to reduce conduction losses **Fig. 1b**.

[2]Fully controllable, i.e., two-gate bipolar bidirectional switches are typically realized as inverse-series drain-drain connection of two unipolar MOSFETs, but have recently become available as samples in monolithic form (Monolithic Bidirectional Switches, MBDSs) from several power semiconductor manufacturers [23]–[25] and will be commercialized in near future.

However, this quasi-single stage concept (see **Fig. 1b**) still requires an ac/dc rectifier circuit to interface with the 3-Φ mains and generate a unipolar dc-link voltage v_{pn}, which is then converted into a high-frequency (HF) ac voltage by a full-bridge circuit. While the control complexity remains relatively low, this additional full-bridge increases overall hardware realization efforts.

To reduce realization efforts while maintaining low modulation and control complexity, the 3-Φ diode rectifier is advantageously replaced by a matrix-type front-end (see **Fig. 3a**). This topology directly converts low-frequency (LF) 3-Φ mains voltages v_a, v_b, v_c into an HF ac voltage v_x across the primary-side winding of the isolation transformer. Although all primary-side switches (including the injection bridge-leg) must be able to block bidirectional voltages, the resulting circuit topology requires one less power conversion stage than the quasi-single-stage configuration (see **Fig. 1b**), reducing the number of transistors and enhancing power conversion efficiency. This proposed configuration is called the Integrated Active Filter isolated Matrix-Type Rectifier (IAF-iMR).

Section II discusses the basic operating principle of the proposed IAF-iMR, serving as the foundation for the explanation of the control scheme presented in **Section III**. Simulation results (6.25 kW output power, 3-Φ 400 Vac mains, and 400 Vdc output) presented in **Section IV** validate the theoretical analysis by demonstrating 3-Φ sinusoidal currents drawn from the mains and a constant, isolated dc output voltage. Additionally, the rms current stresses on the transistors and the isolation transformer are provided to guide component selection. **Section V** presents a comparative analysis between the proposed IAF-iMR and the bidirectional IAF-based quasi-single-stage ac/dc converter (see **Fig. 1b**). Finally, **Section VI** concludes the paper and provides an outlook on a novel circuit topology, called the matrix-type isolated-three-phase-HF-link three-phase ac/dc converter (**i3X-Rectifier**). The i3X-Rectifier features significantly reduced stresses on both the transformer windings (current stresses) and the magnetic cores (HF magnetic flux amplitude), making it a highly competitive solution for high-power (100 kW range) AI-centric data center rack supplies.

II. Operating Principle

The proposed IAF-iMR comprises a matrix-type front-end, an integrated active filter (IAF) stage, and a DAB-type back-end, as shown in **Fig. 3a**. Its operating behavior is analyzed in this section based on the derived equivalent circuits (see **Fig. 3b**), where each of the two commutation cells in the matrix-type front-end is replaced by a three-pole switch, while the DAB-type back-end is replaced by a voltage source $v_{z'}$, which alternates in polarity with an amplitude of V_{out} in the positive or negative half cycle.

The operating principle is analyzed over a 60° interval of the mains period, considering a relation of the phase voltages $v_a > v_b > v_c$. Detailed switching signals and characteristic waveforms of the proposed IAF-iMR over two switching periods within this interval are provided in **Fig. 3c**. The analysis for the remaining intervals of a full mains cycle can be obtained by cyclically interchanging the phase quantities.

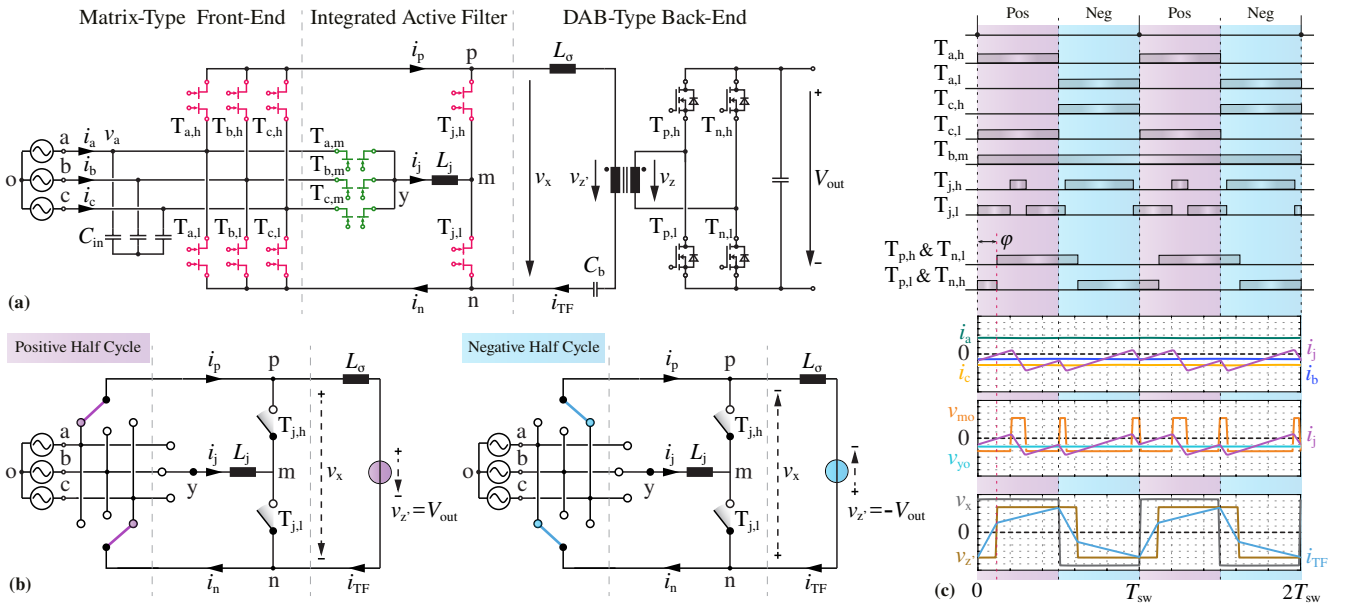

Fig. 3: **(a)** Schematic of the proposed single-stage three-phase integrated active filter isolated matrix-type rectifier (IAF-iMR). The matrix-type front-end directly convert LF 3-Φ mains voltages into an HF ac voltage v_x applied to the DAB-type back-end. The integrated active filter (IAF) stage guarantees sinusoidal shaping of all 3-Φ mains currents using the 3rd-harmonic current injection with switching of $T_{j,h}$ and $T_{j,l}$ adapted to the changing polarity of v_x. **(b)** Equivalent circuits of the proposed IAF-iMR in the positive and negative half cycles in the considered 60° interval of the mains period where phase voltages $v_a > v_b > v_c$, assuming a unity transformer turns ratio (the indicated voltages v_x and $v_{z'}$ are representing the actual physical directions). **(c)** Switching signals and characteristic waveforms of the proposed IAF-iMR over two switching periods.

A. Matrix-Type Front-End

The matrix-type front-end consists of two commutation cells, each comprising three bidirectional switches (e.g., the high-side commutation cell includes $T_{a,h}$, $T_{b,h}$, and $T_{c,h}$). At any given time, exactly one switch from each commutation cell is turned ON to form v_x with an amplitude equal to the highest line-to-line mains voltage. In the considered 60° interval, phases *a* and *c*, are always active, while the transistors ($T_{b,h}$ and $T_{b,l}$) stay OFF-state. As shown in **Fig. 3b**, during the positive half cycle, turning on $T_{a,h}$ and $T_{c,l}$ results in $v_x = v_{ac}$; during the negative half cycle, turning on $T_{a,l}$ and $T_{c,h}$ results in $v_x = -v_{ac}$. This switching scheme generates an ac voltage v_x that alternates at the switching frequency f_{sw} with an amplitude of the highest line-to-line mains voltage, as shown in **Fig. 3c**. Consequently, the amplitude (envelope) of v_x exhibits a six-puls shape over one mains period.

B. DAB-Type Back-End

The DAB-type back-end operates at the same switching frequency f_{sw} as the matrix-type front-end and regulates the power flow to the dc output by adjusting the phase shift φ applied to the carrier of the DAB-type back-end (see **Fig. 3c**). Assuming a unity transformer turns ratio, during the positive half cycle[3], turning on $T_{p,h}$ and $T_{n,l}$ generates $v_z = v_{z'} = V_{out}$; during the negative half cycle, turning on $T_{p,l}$ and $T_{n,h}$ generates $v_z = v_{z'} = -V_{out}$. Consequently, a voltage difference $v_x - v_{z'}$ is applied across the transformer stray inductance L_σ, driving a trapezoidal-shaped transformer current i_{TF} and facilitating power transfer between the transformer's primary and secondary sides.

[3]Note that the positive and the negative half cycles for the DAB-type back-end are shifted according to phase shift φ applied to the back-end carrier.

C. Integrated Active Filter (IAF) Stage

The IAF stage ensures the ohmic mains behavior of the proposed IAF-iMR, i.e., 3-Φ sinusoidal mains currents are proportional to the 3-Φ mains voltages at any given point of time. In the considered 60° mains voltage interval, a current needs to be injected into phase *b* (the phase with the minimum absolute instantaneous voltage value), and otherwise phase *b* would remain with no current, as the transistors $T_{b,h}$ and $T_{b,l}$ of the matrix-type front-end are in the OFF-state. This can be achieved by turning on $T_{b,m}$ ($T_{a,m}$ and $T_{c,m}$ remain in the OFF-state) and controlling the current i_j through the injection inductor L_j by properly gating $T_{j,h}$ and $T_{j,l}$ to shape the local average value of i_j, i.e., ensure that i_j aligns with the mains current i_b in the considered 60° interval. This guarantees an instantaneously constant power is drawn from the 3-Φ mains and delivered to the dc output, in combination with sinusoidal currents in phases *a* and *c*. This concept is known as the 3rd-harmonic current injection concept (see **Fig. 2**) [26], [27].

In the proposed IAF-iMR, the matrix-type front-end is advantageously implemented to directly convert LF 3-Φ mains voltages into an HF ac voltage v_x, enabling single-stage operation. Consequently, the potentials of *p* and *n* obtain different values during the positive and negative duty cycles within each switching period. To incorporate the 3rd-harmonic current injection concept into the proposed IAF-iMR, different duty cycles d_j of the injection bridge-leg ($T_{j,h}$ and $T_{j,l}$) must be assigned during the positive and negative half cycles such that i_j is appropriately regulated. The injection bridge-leg must operate

at $2f_{sw}$ (see **Fig. 3c**), which is twice the switching frequency of the matrix-type front-end and the DAB-type back-end.

Assuming a comparably small LF voltage over the injection inductor L_j, the local average value of switched voltage v_{mo} must be equal to $v_{yo} = v_b$ in the considered 60° interval. During the positive half cycle, $v_{po} = v_a > 0$ and $v_{no} = v_c < 0$, leading to $v_x = v_{ac} > 0$. During the negative half cycle, $v_{po} = v_c < 0$ and $v_{no} = v_a > 0$, leading to $v_x = v_{ca} < 0$. The duty cycle d_j assigned during the positive and negative half cycles must be different as shown in **Fig. 3c**.

The triangular injection current i_j is driven by the voltage different between v_{mo} and v_{yo}. v_{mo} is defined not only by the switching states of the injection bridge-leg (of the transistor $T_{j,h}$ and $T_{j,l}$) but also by the potentials of p and n. At the boundaries of the positive and the negative half cycles, v_{mo} always changes the polarity without altering the injection bridge-leg switching state. Consequently, i_j transitions from increasing to decreasing or vice versa at these boundaries, resulting in the reduced HF current ripple in i_j. In other words, a lower injection inductance L_j is required for a given current ripple level compared to conventional IAF-based rectifiers [27], which compensates for the higher switching frequency of the injection bridge-leg required in the IAF-iMR.

D. Soft-Switching Operation

The proposed IAF-iMR can potentially achieve full soft-switching operation[4], which ensures that the charge stored in the transistors' output capacitances is recycled rather than dissipated during the turn-ON transitions. This allows the use of relatively high switching frequencies for compact converter designs. Additionally, the selection of power semiconductor devices can be optimized to minimize conduction losses without increasing switching losses, enabling optimal semiconductor performance independent of the typical transistors' figure-of-merit [28]. This approach maximizes efficiency, and allows to simultaneously achieve high power densities and high power conversion efficiencies.

The soft-switching operation of the matrix-type front-end resembles that of typical isolated single-phase matrix-type rectifiers [12]. The switched currents i_p (for the upper commutation cell) and i_n (for the lower commutation cell) are the superpositions of the transformer current i_{TF} and sections of the injection current i_j. As shown in **Fig. 3c**, at switching instants of the matrix-type front-end, i_j always equals its local average value (the current in the phase with the lowest absolute instantaneous phase voltage value), while i_{TF} reaches its peak. Thus, the directions of i_p and i_n are same as that of i_{TF} at switching instants, considering the peak value of i_{TF}, which is *3 to 4 times larger* than the local average value of i_j according to circuit simulation results in **Sec. IV**.

The triangular-shaped injection current i_j allows soft switching of the injection bridge-leg ($T_{j,h}$ and $T_{j,l}$), similarly to the triangular current mode (TCM, [29]). Hysteresis control of the i_j or advanced modulation schemes can be implemented for full soft-switching operation [7].

[4]Full soft-switching operation refers to achieving soft switching for all HF switching transitions. The switching transitions $T_{a,m}$, $T_{b,m}$, and $T_{c,m}$ are excluded from this consideration, as they occur only a few times per fundamental mains cycle and contribute negligibly to the total power losses.

The transformer current i_{TF} (see **Fig. 3c**) enables the soft switching in the DAB-type back-end. Note that the soft-switching region depends on system specifications and operating conditions, such as the transformer leakage inductance L_σ, transformer turns ratio, as well as input/output voltages [30], [31].

III. Control Strategy

This section presents a control strategy for the IAF-iMR that ensures 3-Φ sinusoidal mains currents and a constant isolated dc output voltage. The proposed controller (see **Fig. 4**) includes four main functional blocks, i.e., matrix-type front-end modulation, 3rd-harmonic current injection, DAB-type back-end modulation and output voltage control. Note that the matrix-type front-end operates as an open-loop modulator without feedback regulation. In contrast, the 3rd-harmonic current injection bridge-leg and the DAB-type back-end are feedback-regulated using PI controllers. The following subsections provide a detailed explanation of each functional block.

A. Matrix-Type Front-End Modulation

The measured 3-Φ mains voltages v_a, v_b, v_c are first processed through a polarity assignment block, before being sorted into $v_{max}, v_{mid}, v_{min}$ voltage levels. Each switching period is equally divided into a positive and a negative half cycle. During the positive half cycle, a gain of +1 is applied, preserving the original measured polarities; whereas, during the negative half cycle, a gain of −1 is applied, reversing their polarities.

For example, considering a 60° mains interval where $v_a > v_b > v_c$: during the positive half cycle, $v_{max} = v_a = v_{po} > 0$ is achieved by turning on $T_{a,h}$, and $v_{min} = v_c = v_{no} < 0$ is achieved by turning on $T_{c,l}$; during the negative half cycle, $v_{max} = v_c = v_{po} < 0$ is realized by turning on $T_{c,h}$, and $v_{min} = v_a = v_{no} > 0$ is realized by turning on $T_{a,l}$.

The corresponding middle phase selector transistor (one of the transistors $T_{a,m}$, $T_{b,m}$, $T_{c,m}$) connects the phase with the minimum absolute instantaneous voltage value (phase b in this case) to the injection inductor L_j. This allows 3rd-harmonic current injection, ensuring 3-Φ sinusoidal mains currents (see **Sec. III-C**).

B. Output Voltage Control & DAB-Type Back-End Modulation

The output voltage reference V^*_{out} is tracked by providing the corresponding power reference P^*_{out} using a PI controller. The DAB-type back-end is then regulated to deliver the required output power P^*_{out} using basic phase shift modulation, as implemented in typical DAB converters [30]–[34].

The power transferred across the galvanic isolation transformer depends on the product of transformer winding voltage amplitudes, i.e., $|v_x| = |v_{max} - v_{min}|$ and $|v_z| = V_{out}$, and the phase shift in between [31]:

$$\begin{aligned} P^*_{out} &= \frac{n \cdot V_{out} \cdot |v_{max} - v_{min}|}{2\pi f_{sw} L_\sigma} \cdot \frac{\pi - |\varphi^*|}{\pi} \cdot \varphi^* \\ &= \frac{n \cdot V_{out} \cdot |v_{max} - v_{min}|}{2\pi f_{sw} L_\sigma} \cdot k_{DAB} \cdot \varphi^*, \end{aligned} \tag{1}$$

where n denotes the transformer turns ratio and a linearized constant $k_{DAB} = 0.68$ is applied considering a phase shift φ^* up to 60°.

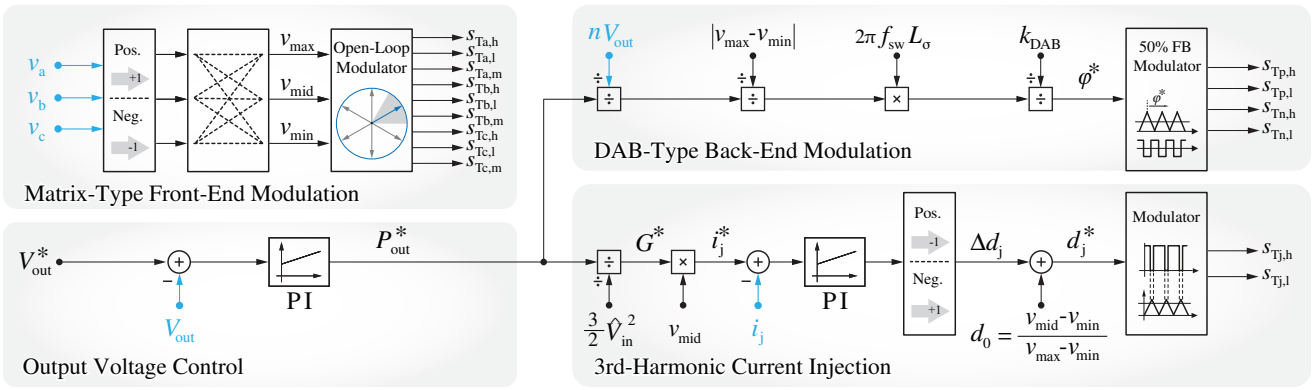

Fig. 4: Control block diagram of the proposed IAF-iMR, including four main functional blocks to ensure 3-Φ sinusoidal mains currents as well as a constant isolated dc output voltage. The matrix-type front-end generates an HF ac voltage v_x by directly converting LF 3-Φ mains voltages, requiring no feedback regulation (open-loop modulation). In contrast, both the DAB-type back-end and the 3rd-harmonic current injection bridge-leg are feedback-regulated using PI controllers. The constant power transferred through the isolation transformer to the dc output is controlled by adjusting the phase shift φ between the carriers of the matrix-type front-end and the DAB-type back-end. The 3-Φ sinusoidal mains currents are ensured by the 3rd-harmonic current injection, thereby maintaining a constant power draw from the mains.

The calculated phase shift φ^* is fed into a 50% full-bridge (FB) modulator, which generates the gating signals for the DAB-type back-end. The amplitude of the transformer's primary winding voltage, $|v_x| = |v_{max} - v_{min}|$, follows a six-pulse-shaped waveform over one mains fundamental period. Consequently, in steady-state operation, φ^* exhibits an inverse six-pulse shape (see **Fig. 5f**) for a constant output power delivery.

C. 3rd-Harmonic Current Injection

The input conductance

$$G^* = \frac{P^*}{\frac{3}{2}\hat{V}_{in}^2}, \tag{2}$$

is calculated using the power reference P^*_{out} and the measured peak phase voltage $\hat{V}_{in}$, assuming that the 3-Φ sinusoidal mains current references are proportional to the corresponding measured 3-Φ input phase voltages, ensuring purely ohmic operation of the 3-Φ mains. Thus, the injection current reference equals the phase current in the phase with the lowest absolute instantaneous voltage value, i.e., $i_j^* = G^* \cdot v_{mid}$.

The injection current deviation $i_j^* - i_j$ is fed into a PI controller to determine the required correction duty cycle Δd_j^* after assigning the appropriate polarities in the corresponding positive or negative half cycle. Specifically, to increase i_j, v_{mo} must be reduced to generate a positive correction voltage across L_j. This needs a negative Δd_j^* in the positive half cycle ($v_{po} > 0$ and $v_{no} < 0$). In contrast, in the negative half cycle, a positive Δd_j^* is required since $v_{po} < 0$ and $v_{no} > 0$.

Furthermore, to improve the controller's dynamic performance, a duty cycle feedforward d_0 is implemented:

$$v_{mid} = d_0 \cdot v_{max} + (1 - d_0) \cdot v_{min} \Rightarrow d_0 = \frac{v_{mid} - v_{min}}{v_{max} - v_{min}}. \tag{3}$$

Thus, $T_{j,h}$ and $T_{j,l}$ regulate i_j to match the 3rd-harmonic current (the current in the phase with the minimum amplitude); i_j is injected via one of the transistors $T_{a,m}$, $T_{b,m}$, or $T_{c,m}$ into the corresponding phase. This ultimately ensures 3-Φ sinusoidal mains currents.

TABLE I: Main circuit specifications and parameters for the simulations shown in **Fig. 5**. Note that L_{in} is not shown **Fig. 3**.

	Description	Value
V_{in}	RMS mains phase volt.	230 V
V_{out}	DC output volt.	400 V
P_{out}	Output power	6.25 kW
f_{sw}	Switching frequency	150 kHz
$N_p : N_s$	Transformer turns ratio	1:1
L_σ	Leakage inductance	20 µH
L_j	Injection inductance	15 µH
C_{in}	Mains filter capacitance	8 µF
L_{in}	Mains filter inductance	4 µH

IV. Simulation Results & RMS Current Stresses

In this section, the IAF-iMR's operation is validated by closed-loop circuit simulations using the proposed control strategy shown in **Fig. 4** to supply 6.25 kW to a 400 V dc load from 3-Φ 400 V mains. Main circuit specifications and parameters are listed in **Tab. I**. Note that the switching frequency f_{sw} is the carrier frequency for the matrix-type front-end and the DAB-type back-end. The injection bridge-leg ($T_{j,h}$,and $T_{j,l}$) must be switched at $2f_{sw}$.

A. Simulation Results

Fig. 5a - **Fig. 5b** confirm the basic operating principle of the proposed IAF-iMR, demonstrating that the 3-Φ sinusoidal mains currents are generated proportional to the corresponding measured 3-Φ input phase voltages, i.e., purely ohmic operation of the 3-Φ mains is achieved. In **Fig. 5c**, one of the phase selector transistors ($T_{a,m}$, $T_{b,m}$, and $T_{c,m}$) is alternatively turned ON for each 60° mains interval. Thus, v_{yo} is always equal to the phase voltage with the minimum absolute instantaneous voltage value. The voltage v_{mo} attains either the maximum or minimum phase voltage by turning ON $T_{j,h}$ or $T_{j,l}$. The voltage difference between v_{yo} and v_{mo} drives the injection current i_j, whose local average value matches the phase current with minimum absolute instantaneous value.

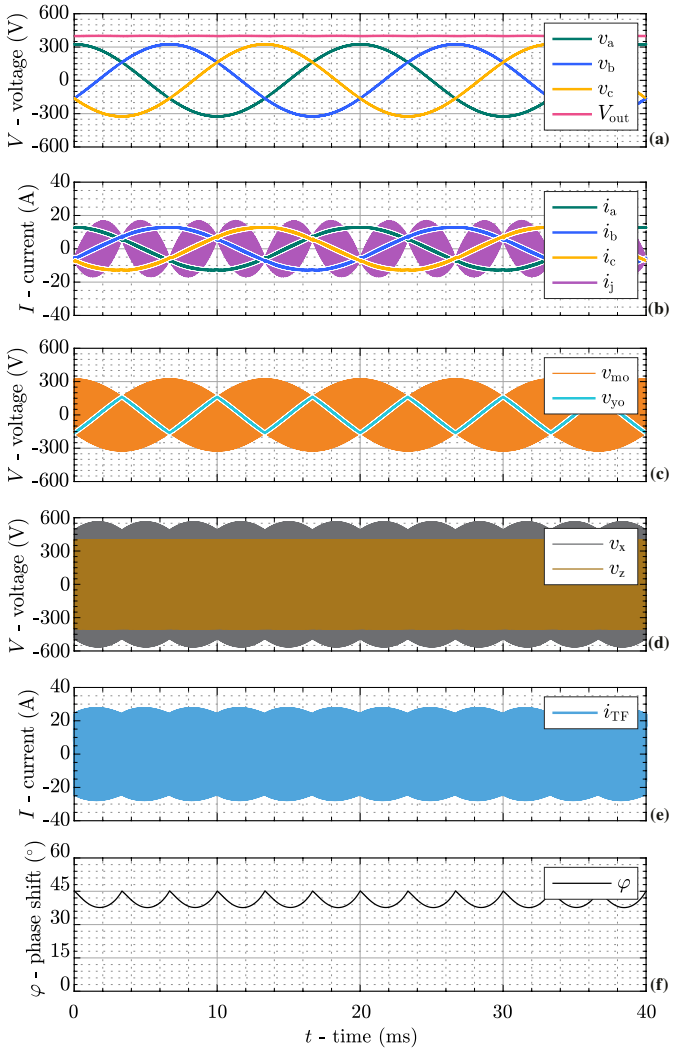

Fig. 5: Simulated key waveforms of the proposed three-phase integrated active filter isolated matrix-type rectifier (IAF-iMR) connected to 3-Φ 400 V mains to deliver a nominal power of 6.25 kW at 400 V dc output.

Fig. 5d - **Fig. 5f** illustrate the DAB-type operation, where the primary and secondary winding voltages (v_x and v_z) drive an HF trapezoidal-shaped transformer current i_{TF}. The amplitude of v_x follows a six-pulse-shaped waveform over one mains fundamental period. Consequently, in steady-state operation, the phase shift φ exhibits an inverse six-pulse shape (not constant), dynamically adjusting to maintain constant output power delivery.

B. RMS Current Stresses

The rms current stresses of the main components in the analyzed IAF-iMR are summarized in **Tab. II**, presented both as absolute values and as percentages relative to the output current. This provides guidelines for transistor selection and magnetic component design.

Specifically, the current stresses in the matrix-type front-end, DAB-type back-end, and isolation transformer are comparable to those in typical isolated single-stage matrix-type ac/dc converters [12]. Although an IAF stage is additionally required, its transistors' current stresses remain relatively low (around 30% of the output current), indicating that only a small additional chip area is needed. On the other hand, the IAF stage significantly reduces control and modulation complexity compared to the conventional matrix-type converters, i.e., with no need of complex schemes for maintaining 3-Φ sinusoidal mains currents and achieving full soft-switching operation [12].

TABLE II: RMS current stresses of the main components in the analyzed IAF-iMR, presented both as absolute values and as percentages relative to the dc output current. The IAF-iMR is connected to 3-Φ 400 V mains to deliver a nominal power of 6.25 kW at 400 V dc output.

	Description	Value	Percent
I_{out}	Output current	15.6 A	100%
$I_{in,rms}$	Mains phase current	9.1 A	58%
	Matrix-type front-end		
$I_{matrix,rms}$	Current in transistors, e.g., $T_{a,h}$ or $T_{a,l}$	10.7 A	69%
	Integrated active filter		
$I_{selector}$	Current in phase selector $T_{a,m}$, $T_{b,m}$, $T_{c,m}$	4.3 A	28%
$I_{j,rms}$	Current in injection bridge-leg $T_{j,h}$, $T_{j,l}$	5.4 A	35%
	DAB back-end		
I_{DAB}	Current in transistors, e.g., $T_{p,h}$, $T_{p,l}$	12.3 A	79%
	Isolation transformer		
$I_{TF,rms}$	Transformer current	17.4 A	112%

As conceptual alternatives to non-phase-modular three-phase IAF- and/or matrix-based approaches, phase-modular concepts have recently been extensively studied for electric vehicle (EV) charging applications due to the flexibility in interfacing both three-phase and single-phase ac inputs [35]. Compared to phase-modular approaches, the proposed IAF-iMR, which employs a matrix-type front-end, offers several advantages: it requires fewer magnetic components, utilizes a higher voltage amplitude for power transfer through the galvanic isolation transformer, and consequently experiences lower rms current stresses. These benefits contribute to a more compact, high-efficiency converter design.

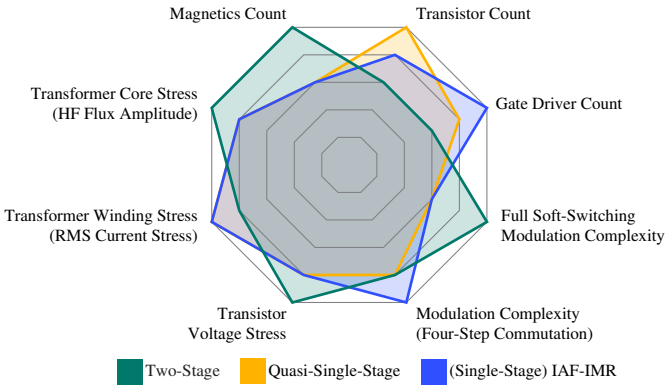

Fig. 6: Qualitative comparative analysis of isolated 3-Φ ac/dc converters: a two-stage topology comprising a two-level PFC front-end and an isolated dc/dc back-end (see **Fig. 1a**), the IAF-based quasi-single-stage topology (see **Fig. 1b**), and the proposed single-stage IAF-iMR. Note that lower values indicate more favorable characteristics.

V. Comparative Analysis

This section presents a brief comparative analysis of two typical isolated ac/dc converter topologies, i.e., the two-stage topology (see **Fig. 1a**) and the quasi-single-stage IAF-based topology (see **Fig. 1b**), to the proposed single-stage IAF-iMR. This partly quantitative and qualitative comparison covers three key aspects: component count, main component stresses, and modulation/control complexity. The results are qualitatively summarized in **Fig. 6**, where lower values (e.g., fewer components, lower stress, or simpler modulation) indicate more favorable characteristics.

In terms of component count, the two-stage topology requires fewer transistors and gate drivers but incorporates more magnetic components, due to its separation of the PFC front-end and isolated dc/dc back-end. In contrast, the IAF-based quasi-single-stage topology employs more transistors and gate drivers while reducing the number of magnetic components. This distinction arises from their fundamental topology difference: the two-stage topology operates as a voltage-source (voltage dc-link) topology, whereas the IAF-based quasi-single-stage topology operates as a current-source (current dc-link) topology. Consequently, these differences align with the inherent trade-offs between voltage-source and current-source systems [36]. The proposed IAF-iMR, which employs a matrix-type front-end, further simplifies the quasi-single-stage topology into a true single-stage topology. This design achieves a balance by reducing both magnetic (cf. the two-stage topology) and semiconductor components (cf. the quasi-single-stage topology), although it requires a relatively higher number of gate drivers due to the application of two-gate MBDSs.

The component stress follows the intrinsic trade-offs between current-source and voltage-source topologies. In the two-stage topology, front-end transistors must block a typical DC-link voltage of 720 V for a 400 V mains, which is higher than in quasi-single-stage or single-stage topologies. In these current-source configurations, the front-end transistors need to block approximately 670 V[5], considering a 10% voltage variation [37]. Since the front-end transistors' blocking voltages are equal to the transformer primary winding voltages, the two-stage topology experiences lower transformer current stress when transferring a fixed amount of power; in contrast, in quasi-single-stage and single-stage topologies, transformers potentially need to handle higher current stresses.

All three topologies can potentially achieve full soft-switching operation without requiring additional auxiliary circuits. However, two-level voltage-source rectifiers operating in triangular current mode (TCM) demand additional effort in filter design and EMI compliance [29]. In contrast, operating the IAF's injection bridge-leg with TCM requires relatively low effort [7]. Furthermore, the proposed IAF-iMR must employ a four-step commutation strategy due to the direct AC connection of the MBDSs, leading to higher modulation complexity compared to the other two topologies [38], [39].

All in all, the proposed IAF-iMR presents a compelling solution for very compact and high-efficiency data center power supplies. By minimizing the number of magnetic components and transistors, it offers a competitive advantage over traditional two-stage and quasi-single-stage topologies. As advancements in intelligent power module technology continue, the down-side limitations of the IAF-iMR, i.e., primarily related to the four-step commutation and the increased number of gate drivers, will be mitigated, making it an even more attractive candidate for next-generation AI-driven data centers.

[5]The front-end transistors must block the line-to-line voltages, meaning that a 10% variation in phase voltages can lead to a 20% variation in line-to-line voltages , i.e., $1.2 \cdot 563\,\text{V} \approx 670\,\text{V}$.

VI. Conclusion & Outlook

To enable highly efficient power conversion for next-generation AI-driven data centers, this paper proposes a novel single-stage three-phase (3-Φ) Integrated Active Filter isolated Matrix-type Rectifier (IAF-iMR), comprising a matrix-type front-end, an IAF stage, and a DAB-type back-end. The proposed IAF-iMR advantageously leverages the matrix-type front-end to achieve direct LF-ac/HF-ac conversion, replacing the conventional ac/dc-dc/ac conversion used in typical two-stage or quasi-single-stage topologies. This approach generates an HF ac voltage across the transformer's primary winding while requiring fewer magnetic components and power transistors, improving both efficiency and compactness. The IAF stage injects a third-harmonic current into the phase with the lowest absolute instantaneous voltage value, ensuring sinusoidal

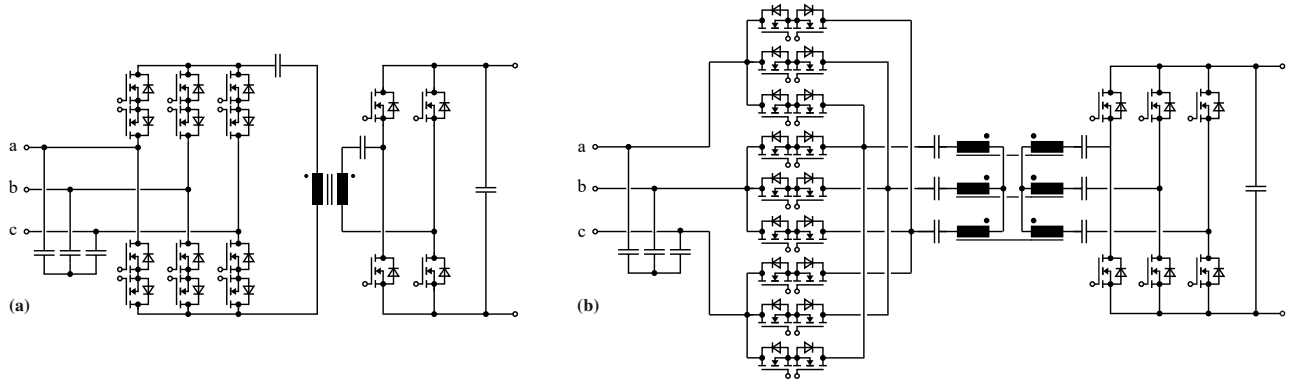

Fig. 7: Schematics of **(a)** a typical matrix-type isolated-*single-phase*-HF-link three-phase ac/dc converter and **(b)** a novel matrix-type isolated-*three-phase*-HF-link three-phase ac/dc converter, called **i3X-Rectifier**. Similar to the advantages of the three-phase DAB dc/dc converter [31], the i3X-Rectifier leverages a three-phase transformer as isolated HF-link, resulting in reduced components stresses (power transistors, isolation transformers, and filter capacitors), better transformer core utilization, lower filtering efforts, and an extended soft-switching region.

shaping of all 3-Φ mains currents. Additionally, the potential for achieving soft-switching operation in all three converter stages of the proposed IAF-iMR is explored. Circuit simulation results verify the operating principle of the IAF-iMR and validate the proposed control strategy. This is followed by a component stress analysis and a comparative evaluation against two-stage and quasi-single-stage topologies, emphasizing the IAF-iMR as a compelling solution for data center applications due to its high efficiency, optimized component utilization, and improved overall system performance.

However, the single-phase (1-Φ) transformer employed in the proposed IAF-iMR poses a bottleneck that limits the IAF-iMR for data center power supplies exceeding, e.g., 50 kW. To overcome this limitation, a novel matrix-type isolated-three-phase-HF-link 3-Φ ac/dc converter, i.e., **i3X-Rectifier** (see **Fig. 7b**), is proposed, where a 3-Φ isolation transformer is used as HF-link to replace the 1-Φ transformer in a conventional matrix-type isolated 3-Φ ac/dc converter (cf. **Fig. 7a**), which can be derived by further extending the proposed IAF-iMR concept.

Compared to an isolated-*single-phase*-HF-link, the isolated-*three-phase*-HF-link offers several advantages, including reduced rms/peak current stresses in both power transistors and transformer windings, lower high-frequency magnetic flux amplitudes in magnetic cores, better transformer core utilization, and reduced input/output filtering requirements. These improvements align with the performance benefits of 3-Φ DAB dc/dc converters over 1-Φ DAB counterparts [31]. As a result, the i3X-Rectifier emerges as a highly interesting solution for high-power applications requiring high power density and efficiency, such as future high-power (100 kW range) data center supplies in dedicated power racks.

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