Parasitic Extraction Procedures for SiC Power Modules

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Abstract

This paper presents an overview of the procedures performed both in academia and industry for estimating the parasitic behavior of power semiconductor packages. The modeling features and limitations of the state-of-the-art software tool, ANSYS Q3D Extractor, and the measurement methods typically used for the parasitic inductance analysis of silicon carbide (SiC) power modules are comprehensively analyzed on the example of a TO-247-3 package with a single 80 mΩ, 1.2 kV SiC power MOSFET, and of a half-bridge wire-bondless module with two 25 mΩ, 1.2 kV SiC power MOSFETs.

1 Introduction

Thanks to the SiC material properties, the implementation of emerging SiC semiconductor devices in advanced power converters enables engineers to increase the switching frequency, and thus, achieve higher power density and improved energy conversion efficiency in comparison to the mature silicon (Si)-based power electronics (PE). However, a one-to-one replacement of Si devices with SiC devices in PE systems is not recommended. In order to fully benefit from SiC, all benefits coming from SiC devices have to be systematically analyzed and the overall systems have to be modified and optimized accordingly. One of the requirements is the re-design of power module structures in order to exploit the fast switching and thermal capabilities of SiC devices. The trends towards the implementation of SiC devices in modern PE systems designed for harsh environments have additionally supported the development of more advanced power semiconductor packages [1]. A great effort is being made to find the best placement of dies, optimize substrate layouts and improve interconnections in order to ensure low stray inductances (L_{stray}) and capacitances, and, hence, to prevent high overvoltages, current spikes, and electromagnetic interference problems. Namely, higher slopes in voltage and current switching waveforms typically not observed in the switching transitions of Si devices point out the need for a significant minimization of the power switching loop inductance, the gate-driver inductance, the coupling between power and control loops, and the common mode capacitance. Accordingly, the correct prediction of parasitics of SiC power modules increases in importance. Advanced packaging technologies based on wire-bond-less interconnections, and on integration of power devices, drive circuitry, and decoupling capacitors [2, 3] ensure very low inductance of current commutation paths. Power modules for housing WBG devices adopting these new technologies impose requirements for the highly accurate extraction of parasitic inductances, resistances, and capacitances. Particularly, a modeling error in the estimation of the loop inductance and PCB layout inductance of more than 5 % has a much higher impact for low-inductance power modules than for Si-IGBT-modules with the commutation loop inductance in the range of several tens nH [4]. Three-dimensional (3D) numerical modeling and different measurements techniques [5, 6, 7, 8] have been employed in engineering practice to extract the parasitics of power modules and hence, characterize their high frequency performance. In this paper, we address the accuracy of these techniques for extracting the package parasitics.

2 3D Numerical Modeling

In various publications targeting the design of power modules and their dynamic behavior, authors have frequently reported only the commutation (power) loop inductance omitting the information on frequency, and/or the consideration of mutual inductive and capacitive couplings. In actual power module structures, however, the power loop inductance is distributed. It consists of mutually coupled conductive paths representing the partial inductances seen from the source, drain, and gate ports of power devices, which have different impact on the module dynamic performance [9]. An accurate prediction of the distributed power loop inductance is highly important for SiC power modules operating at high switching frequencies. In addition, the stray resistances and the capacitive couplings e.g. between the package and heatsink, and due to the external package connections [10], can have a significant impact on the dynamic performance of power semiconductor devices. 3D field simulations have been employed in engineering practice to estimate the parasitic elements of the packaging structures.

2.1 ANSYS Q3D Extractor

The well-known ANSYS software package, Q3D Extractor, has been frequently used for this purpose [11]. In comparison to pure Finite Element Method-based software tools such as COMSOL Multiphysics, Q3D takes advantage of a surface mesh to calculate the high frequency behavior of conductive structures. As a result, it enables a more efficient extraction of frequency-dependent partial inductances, resistances and capacitive couplings between

conductive nets, valid for the quasi-static field assumptions. A major advantage of Q3D is the ability to estimate these partial inductances within a power module, as well as building an equivalent circuit representing the electromagnetic behavior of the 3D modeling structure in a defined frequency range. However, some limitations of Q3D modeling were observed as stated in [10]. In this paper, we investigate the accuracy of Q3D modeling for extracting the partial inductances of SiC power modules and discrete components.

The modeling of partial inductances is based on distinguishing different current paths defined by the position of dies in the package and placing the Q3D excitations at the suitable positions. Q3D Extractor models the capacitive coupling between the nets and the self-capacitance of a net towards ground, but not the distributed capacitance inside of a single net. Q3D excitation ports are modeled as equipotential surfaces, so that every current path representing a Q3D net is defined between two excitation ports, named as *source* and *sink*. The modeling limitations due to this assumption and accuracy of the modeling in Q3D Extractor are presented in this paper on the examples of discrete TO-247 package and a planar half-bridge all-SiC power module.

2.1.1 3D Modeling of Half-Bridge (HB) Wire-bondless Power Module

A half-bridge (HB) wire-bondless power module based on a planar interconnection technology [12] shown in Fig. 1a) is used as the first modeling example. The 3D geometry model of this module structure was built in Q3D Extractor, see Fig. 1c), in order to calculate the inductance L and resistance R of the commutation loop defined by the current path between DC+ and DC- terminals. Two simulations

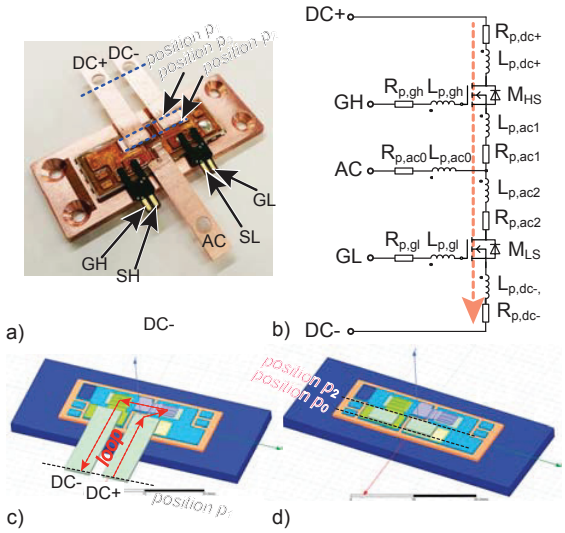

Figure 1 HB wire-bondless power module: a) photo, b) simplified equivalent circuit showing only partial inductances, and c) 3D models used in ANSYS Q3D to extract the parasitic elements of the power module for 1) position p_1, and 2) positions p_0 and p_2.

were performed to extract total and distributed L and R, respectively. The total L and R of the current path between DC+ and DC- is simulated by modeling the 25 mΩ SiC dies in the half bridge configuration as two copper blocks. For calculating the distributed L and R in Q3D, the current path has to be divided into three sub-paths, $L_{p,dc+}$, $L_{p,ac}$, and $L_{p,dc-}$, defined by equipotential excitations. The definitions of these partial inductances are shown by an equivalent circuit of the half bridge module, see Fig. 1b). The Q3D modeling results are summarized in Table 1. The simulations are done for three different positions of the DC+ and DC- excitation ports: position p_0, position p_1 and position p_2, as shown in Fig. 1a). For position p_2, the influence of the length of copper bus-bars is taken into account. As reported in Table 1, there is a mismatch between the power loop inductance calculated in Simulation A, $L_{dc+,dc-}$, and the equivalent loop inductance calculated from the partial inductances estimated by Q3D in Simulation B as $L_{loop,eq} = L_{p,dc+} + L_{p,dc-} + L_{p,ac} + 2 \cdot (M_{dc+,ac} + M_{dc-,ac} + M_{dc+,dc-})$, where $L_{ac} = L_{p,ac1} + L_{p,ac2}$, see Fig. 1b). The parasitic inductance analysis presented in [4] for a 100 kW full SiC inverter pointed out a similar Q3D modeling challenge. This difference originates from the aforementioned Q3D modeling feature of assuming that the conductor surfaces defined as excitations are equipotential regions, which is not physically correct in the real current paths. Particularly, the cuts made to calculate the partial inductances are equipotential in Simulation B; however, these surfaces are not equipotential in Simulation A, which in turn should represent the current path of the power loop more realistically. When estimating $L_{dc+,dc-}$, the difference between the Simulation A and Simulation B for the position p_0, without including the length of bus-bars is $\approx 25\%$, i.e. $L_{loop,eq} = 2.12$ nH vs. $L_{dc+,dc-} = 2.84$ nH, for position p_2, it is $\approx 7.8\%$, while for the position p_1 it is 30 %. Accordingly, the significance of this mismatch depends on the geometry of power loops within a power module, which is further shown in the following section on the example of a discrete TO-247-3 package.

From the Q3D modeling results including the insulation layer [12], the self-capacitance of the DC- net is less than 1 pF, while the self-capacitances of the DC+ and AC nets are $\approx$ 18 pF, the mutual capacitances between the AC and DC- nets and the AC and DC+ nets are $\approx$ 23 pF and $\approx$ 3 pF, respectively. These capacitances can potentially have a higher influence on the dynamic behavior of the HB power module at high switching frequencies [10].

2.1.2 3D Modeling of TO-247-3 Package

The 3D geometry of a 1.2 *kV* 80 mΩ SiC Power MOSFET in TO-247-3 package (Cree C2M0080120D) is shown in Fig. 2. The position of six bond wire pads on the die and six pads on the source terminal are extracted from a dissembled package. The modeling of the drain-source current path was performed by replacing the SiC die with a copper block in order to extract the inductance of the current path between the drain and source terminals, $L_{12} = L_{DS}$ in Q3D Extractor. In the second simulation,

Table 1 Q3D modeling results for the HB power module package at 50 MHz and the ac values of the loop inductance, $L_{dc+,dc-}$, extracted by the impedance measurements (with MOSFET channels closed).

L [nH]	L_{dc+}	L_{dc-}	L_{ac}	$M_{dc+,ac}$	$M_{dc-,ac}$	$M_{dc+,dc-}$	L_{simB}	L_{simA}	rel.diff	L_{meas}
p_0	0.8	0.88	1.51	-0.219	-0.127	-0.187	2.12	2.82	25 %	2.74
p_1	8.63	9.04	1.63	-0.36	-0.2	-3.84	10.51	11.36	7.8 %	11.51
p_2	0.19	0.23	1.4	-0.071	-0.039	-0.012	1.58	2.27	30 %	2.33

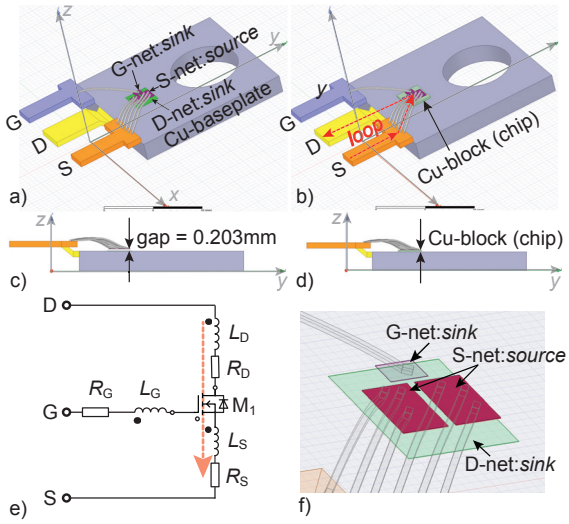

Figure 2 Q3D Modeling of a TO-247-3 package: a) 3D model for extracting partial inductances, L_D, L_S, L_G, M_{DS}, M_{DG}, and M_{GS}, referred to Simulation B, b) 3D model for extracting drain-source loop inductance L_{DS}, referred to Simulation A, c) YZ view of the 3D model in Simulation B, and d) YZ view of the 3D model in Simulation A.

referred to Simulation B, the copper block is removed to extract the partial inductances of the drain-source current loop, $L_1 = L_D$, $L_2 = L_S$, and the mutual coupling between them, $M_{12} = M_{DS}$. The same modeling approach was applied to extract partial inductances of the gate-source L_{GS} and drain-gate L_{DG} current loops. All modeling results are summarized in Table 2. The difference between $L_{12,SimA}$ and $L_{12,SimB} = L_1 + L_2 + 2 \cdot M_{12}$, where the notation 1-2 corresponds to D-S, G-S, and D-G, is smaller in comparison to the previous example of the half-bridge power module. In the TO-247-3 package, the current paths are mainly determined by the terminals, and the chip does not significantly affect the current loops. This is not the case for the planar geometry of the low-inductance HB power module where the difference is more pronounced. According to the Q3D modeling results, the self-capacitances and the capacitive coupling between the gate, source and drain nets are less than 1 pF, which means that the additional capacitive effects introduced by the TO-247-package can be neglected.

As Q3D is a powerful tool frequently used for the extraction of parasitics of power modules, which cannot be easily assessed by the measurements, there is a strong requirement to asses the accuracy of this tool for modeling power WBG semiconductor packages. Accordingly, in the next section, the verification of the previously presented Q3D modeling results is described.

Table 2 Q3D modeling results for the TO-247-3 package at 50 MHz and the ac values of the loop inductances extracted by the two-terminal impedance measurements (with the MOSFET channel closed).

L [nH]	L_1	L_2	M_{12}	L_{simB}	L_{simA}	L_{meas}
D-S	3.53	5.39	-1.58	5.76	5.98	5.54
D-G	3.53	7.38	1.59	7.74	7.95	7.38
G-S	7.34	5.39	-0.84	11.08	12.14	11.6

3 Parasitic Inductance Analysis based on Measurements

In the case when the package geometry and layout is unknown, 3D numerical modeling is not possible and engineers resort to different measurement techniques to characterize the high frequency performance of the modules. There are different measurement approaches used to characterize parasitic parameters of the integrated power electronics modules and discrete packages [5, 6, 7, 8, 13]. As the measurements are performed only from the output terminals of the power module characterizing internal current loops, it is very challenging to extract the mutual inductances of the loops existing within the power module layout. Therefore, self-inductances of power module layouts are typically estimated from the loop impedance measurements neglecting the mutual coupling effects as described in [7, 8, 13], for example. On the other hand, for discrete packages, a few publications addressed the estimation of both self- and mutual-inductances existing in the package by means of measurements. In the case of discrete power devices with three terminals (IGBTs, MOSFETs), a minimum of four impedance measurements are required to extract the existing self- and mutual-inductances within the package. This points out the requirement to define the fourth terminal inside of the package. In [6], the authors proposed a four-terminal measurement of a Si-IGBT in TO-247-3 package using a time domain reflectometry (TDR) instrumentation setup. TDR measurements are based on the wave propagation through a transmission line with inserted the device under test (DUT) and terminated by a 50 Ω resistance. From the measured reflected waves, the equivalent inductance of the current path be-

tween each two terminals can be calculated. The fourth terminal, N was positioned on the base plate, where the scanning acoustic tomography was used to set up the position of point N as close as possible to center of the IGBT die. A disadvantage of these measurement technique in comparison to the impedance measurements is the possibility to determine only a single-value inductance at high frequencies and not the inductance in a wide-frequency range. In [5], a capacitor defined by two copper plates is added to the base-plate of a SiC MOSFET in T0-247-3 package (Cree C2M0080120D) forming the fourth terminal and allowing the separate impedance measurements of the drain-side and source-side current paths. The accuracy of these measurement techniques significantly depends on the definition of the fourth terminal and the inductance calculation from the measured waveforms. The authors in [5] report the estimation of self- and mutual-inductances with an error of 10 %, however without any further clarification.

3.1 Verification

An accurate measurement approach is a necessary tool to verify the 3D modeling results. Accordingly, we combine both, impedance measurements and 3D numerical modeling using the well-established Q3D Extractor, to show the accuracy of the presented procedures for the extraction of parasitics inside of power modules and discrete packages used for housing commercial WBG semiconductor devices. The impedance measurements were performed using a Keysight Impedance Analyzer (E4990) operating from 20 Hz to 120 MHz using a 42941A pin adapter and/or a 16047E fixture.

3.1.1 TO-247-3 Package

To extract the parasitics of a TO-247-3 package, the impedance measurements were performed between drain-source, drain-gate, and gate-source terminals of three MOSFET samples. The measurements of Z_{DS} were performed with both, switch open and closed, i.e. by applying -5 V (i.e. channel closed) and 20 V (i.e. channel open) between gate and source terminals, respectively. When the channel is open, a series R_S-L_S circuit can be used to model the impedance of the D-S current path, and the frequency dependent drain-source inductance $L_{DS}(f)$ and resistance $R_{DS}(f)$ can be calculated from the measured $Z_{DS}(f)$. On the other hand, when the channel is closed, the measured impedance represents the impedance of a series R_S-L_S-C_S circuit, where R_S and L_S are the total resistance and inductance of the measured current path respectively, and C_S is the equivalent capacitance of the current path formed by the inner MOSFET's capacitances. Similarly, the measurements of Z_{GS} and Z_{DG} were performed with the channel closed, and hence, the ac values of L_{GS} and L_{DG} are calculated from the corresponding Z-measurements. The measurement results summarized in Table 2 represent the averaged measurements of three MOSFET samples. It should be emphasized that the impedance measurements, as performed in this work and also suggested in literature, e.g. [7, 8], are feasible in general only if the resonant frequency of the measured impedance curve can be captured by the measurement equipment.

Analyzing the measured impedance curves Z_{DS}, Z_{DG}, and Z_{GS}, we observe that the impedance of a series R_S-L_S-C_S network, with $C_S = \text{const}$ does not very accurately match the measured impedance in the whole frequency range from 1 kHz up to 120 MHz. Particularly, the capacitance seen from the terminals decreases with frequency above approximately 1 MHz. This frequency behavior of the MOSFET capacitances can be explained by the time response of the charge carriers in the semiconductor to the applied voltage. Namely, a relaxation time τ (referred also to time constant) can be defined for any MOSFET capacitance [14]. At higher frequencies f, when $1/\tau \ll f$, various capacitive effects become less influential, which we also verified by the measurements of MOSFET's capacitances on the die level, see Fig. 3. Accordingly, this change of MOSFET capacitances seen in C_S has to be considered in order to correctly extract the ac value of the series inductance L_S from the measured loop impedance, $Z_S(f)$. The series R_S-L_S-C_S circuit can be determined to fit the measured $Z_S(f)$ with higher accuracy either below or above the resonant frequency. As a result, the extracted series inductance between the terminals, L_S, can be expressed rather as a range than as an exact value. The importance of considering the frequency dependent C_S for accurate calculation of the parasitic inductance can be seen in Fig. 4 showing the the extraction of the parasitic inductance of the drain-source current loop in the TO-247-3 package from the $Z_{DS}(f)$ measurements. Determining the series R_S-L_S-C_S circuit to match the measured $Z_{DS}(f)$ with higher accuracy in the low frequency range, Fig. 4a), and in the high frequency range, Fig. 4b), results in the equivalent L_S of 4.37 nH and 5.53 nH, respectively. The influence of a floating terminal during the impedance measurements of three-terminal devices, as discussed in [8], has not been observed in the frequency range up to 120 MHz, and the accuracy of estimating the parasitic inductance, $L_S(f)$, from an impedance measurement, $Z_S(f)$, is mainly determined by capacitive behavior, as previously described.

The measured $Z_{DS}(f)$ with the channel opened and the parasitic inductance of the drain-source current path, $L_{DS}(f)$

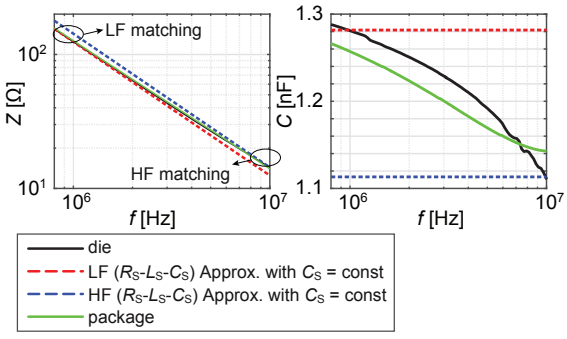

Figure 3 Measured impedance $Z_{DS}(f)$ at the die and package levels and the impedance of the series R_S-L_S-C_S circuits fitted to the measured $Z_{DS}(f)$ with higher accuracy in the range of either low (LF) or high frequencies (HF), b) the corresponding capacitive behaviors.

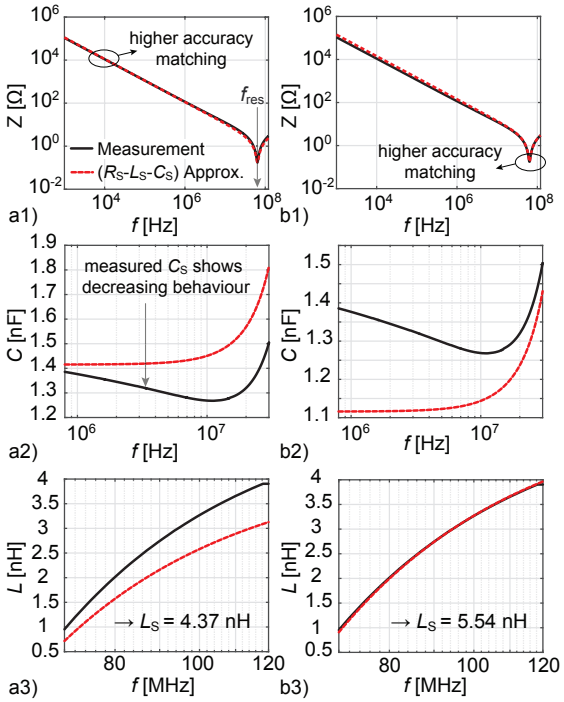

Figure 4 Extraction of the ac value of parasitic inductance of drain-source current loop in the TO-247-3 package. The series R_S-L_S-C_S circuit fitted the measured $Z_S(f)$ with higher accuracy a) below, and b) above the resonant frequency, $f_{res} \approx 50\,\text{MHz}$. a2) and b2) show the capacitive behavior of $Z_S(f)$ below f_{res}, while a3) and b3) show the inductive behavior of $Z_S(f)$ above f_{res}.

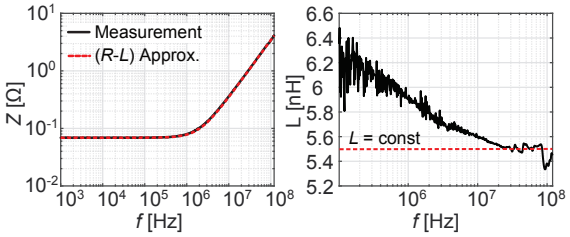

Figure 5 Extraction of the parasitic inductance of drain-source current loop in the TO-247-3 package with closed channel: a) the series R_S-L_S circuit is used to fit the measured $Z_{DS}(f)$, and b) $L_{DS}(f)$ in the frequency range from 0.1 MHZ to 120 MHz extracted from the measured $Z_{DS}(f)$.

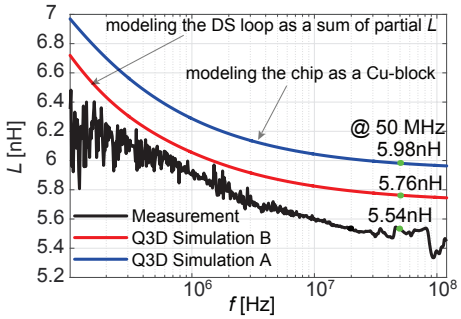

Figure 6 Verification of Q3D modeling of $L_{DS}(f)$ with the impedance measurements of the drain-source current loop inside of a TO-247-3 package, with the MOSFET channel open ($V_{GS} = 20\,\text{V}$).

calculated from $Z_{DS}(f)$ are shown in Fig. 5a) and b), respectively. Fig. 6 presents the verification of the Q3D modeling previously described with the measurement results, $L_{DS}(f)$. This comparison between the simulation results and the measurements of a TO-247-3 package demonstrates the present challenges with the electromagnetic modeling of package structures with Q3D Extractor. Even though the loop inductance calculated in Simulation A should represent the current path more realistically than the loop inductance calculated from the partial inductances in Simulation B, the Simulation B is closer to the measurements, see also Table 2.

The mutual inductance between the drain and source nets calculated by Q3D is $M_{DS} = -1.58\,\text{nH}$, i.e. the mutual coupling coefficient equals $k = M_{DS}/\sqrt{L_D \cdot L_S} = -0.362$. This is approximately two times less than the the mutual coupling coefficient extracted from the measurements in [5] for the same SiC MOSFET component, which in turn could mean that the authors calculated the coupling as $k = 2 \cdot M_{DS}/\sqrt{L_D \cdot L_S}$, as the measured source and drain self-inductances in [5] are very close to the values estimated in this paper based on Q3D and impedance measurements. On the other hand, the measurements of a discrete Si-IGBT in the TO-247-3 package presented in [6] show significantly different package inductances than the inductances calculated in this paper for discrete SiC-MOSFETs in the TO-247-3 package.

3.1.2 HB Wire-bondless Power Module

The impedance measurements between DC+ and DC- of the HB wire-bondless power module were performed using a 4991A pin adapter, which allows the measurements of the loop impedance with and without considering the length of copper bus bars, as it was previously described for the Q3D modeling of the HB power module, see Fig. 1a). In the first measurements, the channels of the SiC MOSFETs were closed. This means that the current path seen between DC+ and DC- terminals can be represented as a series R_S-L_S-C_S circuit, as previously discussed. In the second measurements, the channels of both SiC MOSFETs in the half-bridge configuration are opened by applying the 20 V across the gate-source terminals. In this way, the current path between DC+ and DC- terminals can be represented as a R_S-L_S circuit, where $R_S \approx 50\,\text{m}\Omega$ is the total resistance formed by two open channels in series with $R_{ds,on} = \approx 25\,\text{m}\Omega$ resistance each, and L_S is the total inductance of the current path formed by the top copper layout of the DBC substrate and planar interconnects. Under the measurement conditions with the channels closed, the total ac inductance approaches 2.74 nH, 11.51 nH, and 2.33 nH for the positions p_0, p_1, and p_2, respectively. The corresponding measurement results for the position p_0 are

shown in Fig. 7. Under the measurement conditions with the channels open, the total inductance L_S calculated from the measured Z_S is 2.62 nH, 11.41 nH, and 2.19 nH for the positions p_0, p_1, and p_2, respectively. The verification of Q3D modeling with the measurement results for the positions p_0 and p_2 is shown in Fig. 8.

4 Conclusion

This paper presents a comprehensive analysis of the parasitic extraction procedures typically used in engineering practice during the design process of power modules. The main aim is to evaluate the accuracy and limits of the proposed measurement methods and corresponding modeling techniques. A comparison between the modeled and measured loop impedances of the aforementioned SiC power semiconductor packages reveals the accuracy of the suggested modeling procedure as well as its applicability to power modules larger than discrete packages.

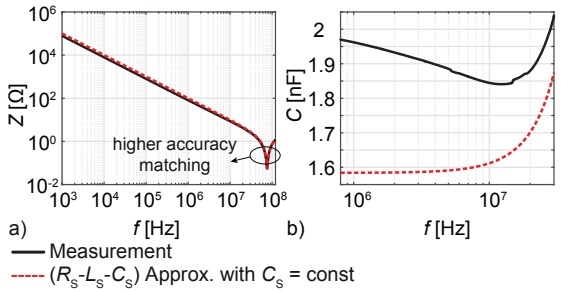

Figure 7 Extraction of the ac value of the loop inductance between DC+ and DC- terminals of the HB power module. a) The series R_S-L_S-C_S circuit fitted the measured $Z_S(f)$ with higher accuracy above the resonant frequency, $f_{res} \approx 75$ MHz, and b) show the capacitive behavior of $Z_S(f)$ below f_{res}.

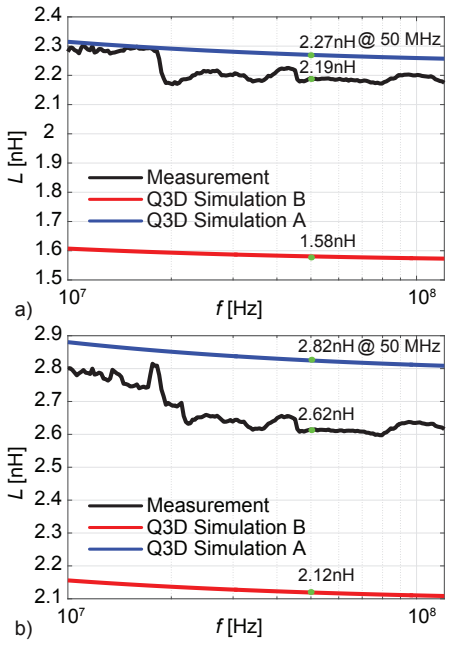

Figure 8 Verification of Q3D modeling of $L_{dc+,dc-}(f)$ with the impedance measurements of the current loop between DC+ and DC- terminals of the HB power module with the MOSFET channels open ($V_{GS} = 20$ V) for the position a) p_2 and b) p_0.

5 Acknowledgment

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