ANALYSIS OF TURN-OFF BEHAVIOR AND SWITCHING LOSSES
OF A 1200V/50A ZERO-VOLTAGE OR ZERO-CURRENT SWITCHED IGBT

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Abstract

The aim of this paper is the development of the basics for the determination of the maximum obtainable switching frequencies of a 20kW, 820V/50V full-bridge DC-DC converter designed with (second generation) 1200V/50A IGBTs.

Because the turn-on losses can be almost completely avoided by phase-shift PWM (zero-voltage turn-off of the active switches), main attention is paid to the determination of the turn-off losses. The dependencies of the switching power losses per switching cycle on the load condition and on the junction temperature etc. are investigated for the following cases: (a) simple pulse width modulation (switching without snubber), (b) switching with capacitive parallel branch (turn-off snubber network) and (c) "force commutation" of the power electronic switches using a commutation circuit (zero-current switching).

Based on the research results there follows the possibility of rating the overall effort linked to a given operating mode of the power electronic devices. Also, the limits of the operating region of the converter system can be determined.

Keywords: Full-bridge phase-shift PWM converter, zero-voltage switching, turn-off snubber, IGBT current tailing, zero-current switching.

Introduction [1],[2],[3]

In general, the development of power electronic systems is characterized more and more by the requirement of increasing power density and dynamics and by the minimization of electromagnetic influences.

The maximum power density is linked via the efficiency of the energy conversion and the size of the electrical and magnetic storage devices to the system pulse frequency. Furthermore, this frequency presents a basic limit of the obtainable system dynamics. These aspects give the motivation for this paper where the switching frequencies are discussed which can be ob-tained with a 1200V/50A IGBT as used for developing a 20kW (820V/50V, 25A/400A) full-bridge phase-shift PWM DC-DC converter (cf. Fig.1). (Resonant converter, quasi-resonant converter multi-resonant converter topologies etc. have not been considered here for the concept selection especially due to the comparatively high component stress and due to the postulated high load range (0-150%).

As shown in Fig.1, the output voltage control of the converter system (which is the basis of this research) is performed by synchronized pulsation of the bridge legs using phase displacement (this control method has already found broad application in connection with thyristor resonant inverters; it is now discussed in the literature to a growing extent for converters designed with turn-off power semiconductor devices). For the case that the electric charges of the circuit capacitances $(C_{p,1}\|C_{p,2})$, $(C_{p,3}\|C_{p,4})$, are completely reversed in polarity by the load current on the primary (which is impressed by the leakage inductance $L_{\sigma,1}$ for commutation of bridge leg I or by the load inductance L for commutation of bridge leg II) within the pause between turn-off of one transistor of a bridge leg and turn-on of the other transistor, then in general no turn-on losses of the power electronic devices result (the free-wheeling diode lying in antiparallel conducts at this turn-on point of time). For a more detailed description of the commutation process of branch I and II see later.

For given maximum allowable overall valve power losses the obtainable switching frequency is determined for the rated operating point by the energy loss per switching cycle or by the snubber networks themselves which minimize the (frequency dependent) turn-off losses. The dependency of the therefore especially interesting turn-off power loss on the

- load condition
- junction temperature and
- dimensioning of the components of the snubber circuits
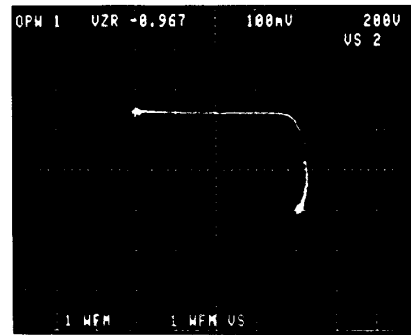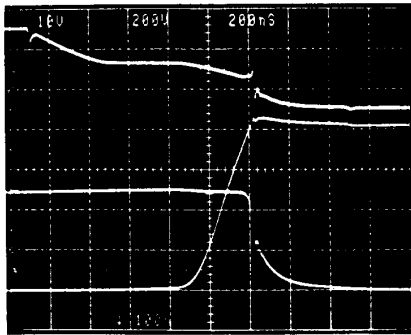
is investigated for
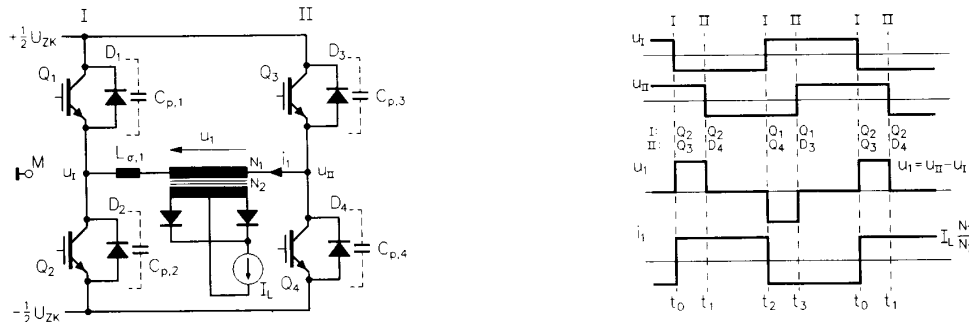
Fig.1: Structure of the power circuit of a transformer coupled DC/DC converter in full bridge configuration. Voltage formation and primary current shape for phase-shift PWM (idealized representation: output capacitances of the switches, forward voltage drops, stray inductances, magnetizing current etc. neglected.) The output current is assumed constant. The bridge legs are marked by I and II. The valves which are conducting within a time interval and the characteristic number of the commutating branch are noted at its beginning.
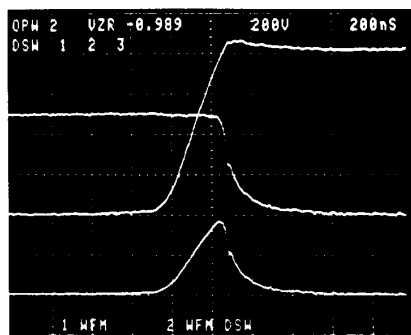
- switching without snubber

- switching with turn-off snubber by using a capacitive leg in parallel (zero-voltage switching, cf. Fig.6) and

- zero-current turn-off of the switches using a resonant commutation circuit (cf. Fig.12).
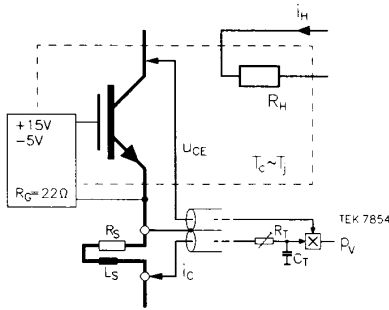
Fig.2: Circuit configuration for measurement of the turn-off losses. Current sensing via a biplanar temperature-compensated shunt whose high-pass behavior $(T_1 = \frac{L_s}{R_s})$ is compensated via a low-pass R_T, C_T of equal corner frequency $\frac{1}{T_1}$. Evaluation (integration) of the measured transistor losses p_V using the oscilloscope TEK 7854. (The measurement using a shunt has been preferred due to the then possible extremly low-inductivity design of the power circuit, as compared to using a jaw-type current probe.)

The valve control is performed by a bipolar driver circuit +15V/−5V, $R_G = 22\Omega$ (a change of the gate resistance only barely influences the turn-off losses; therefore this case is not analyzed in more detail here).

Switching without snubber

The determination of the turn-off losses can simply be performed by analysis of a step-down structure.

The current in the switch is sensed on the emitter side using a frequency compensated shunt (cf. Fig.2). The current at turn-off is defined by the turn-on time for given DC link voltage and given load time constant. The switching frequency is chosen such that the junction temperature T_j of the power electronic device under investigation lies barely above that (T_c) of the case (or of the heat sink). This temperature is given directly by a heater current i_H flowing through a resistor R_H mounted on the same heat sink. For switching without special turn-off snubber a limitation of the switching overvoltages has to be performed by using proper snubbers (used just for limitation of overvoltages) for the valve because the leakage inductances of a practical circuit cannot be totally avoided. Figure 3 shows the switching behavior of a 1200V/50A IGBT (2nd generation, Toshiba MG50Q2YS9).

The DC link voltage U_{ZK} is 820V, the junction temperature $T_j=125^\circ$C. The switching delay time of 800ns (for $R_G=22\Omega$, $U_G= +15V/-5V$) is approximately independent of the temperature. The voltage across the switch has to become larger than the DC link voltage before the switch current may decrease and commutate into the free-wheeling diode (cf.Fig.3). A considerable part (about 50%) of the turn-off energy therefore is dissipated in the switch before the current starts to decrease (cf. Fig.4). The entire turn-off energy (area beneath the instantaneous power curve in Figure 4) amounts to 9.3mJ. This corresponds to a turn-off power loss of 93W for a switching frequency of 10kHz.

Fig.3: Turn-off behavior of a 1200V/50A IGBT half-bridge module (Toshiba MG50Q2YS9) without snubber; $U_{ZK} = 820$V, $R_G = 22\Omega$, $T_j = 125^\circ$. LEFT (200ns/Div): above: bipolar gate signal (+15V/−5V, 10V/Div), below: collector emitter voltage u_{CE} (200V/Div), collector current i_C (20A/Div); RIGHT: turn-off load line (i_C vs. u_{CE}).

Fig.4: Above: as in Fig.3, below: curve showing the instantaneous turn-off power (20kW/Div); $W_{off}=9.3$mJ.

The current, DC link voltage and temperature dependencies of the turn-off losses for switching without snubber are given in Fig.5. While the turn-off energy can be calculated based on an approximately voltage-proportional behavior, it increases more than proportional in dependency on the current to be turned off. For rated current the turn-off losses for 125°C junction temperature are about twice as high as the losses for 25°C.

Switching with Capacitive Snubber (ZVS) [4], [5], [6], [7], [8]

To reduce the turn-off losses it is obvious to delay the voltage rise appropriately during turn-off by using a turn-off snubber (cf. Fig.6). The simplest method by which the dependency of the turn-off losses of the capacitance of the snubber capacitor can be determined is given by an R_B, C_B, D_B snubber for the valve.

Figure 7 shows the turn-off process of the 1200V/50A module for a snubber capacitance of 22nF. The switching delay time (about 800ns) remains due to the very much nonlinear Miller capacitance C_{GC} approximately un-
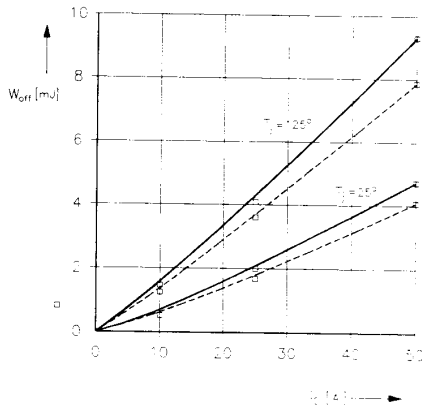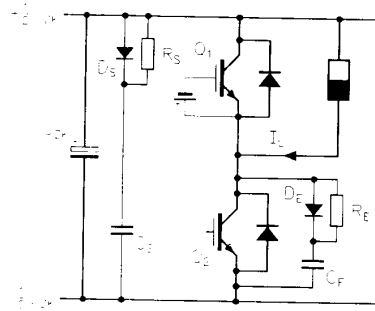
Fig.6: Circuit configuration for using a turn-off snubber network. The bridge leg works as already for the determination of the turn-off losses for switching without snubber in the step-down operating mode (negative voltage applied to the gate of Q_1 by using a 9V battery) and with very low duty ratio. The circuit R_S, D_S, C_S attached close to the terminals of the half bridge module serves to limit the switching overvoltages caused by the lead inductances.
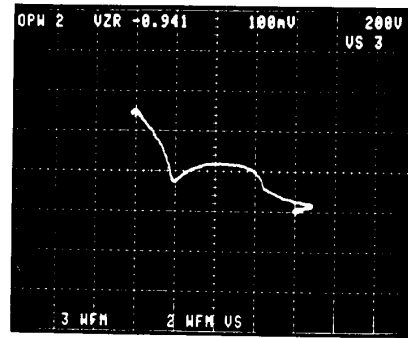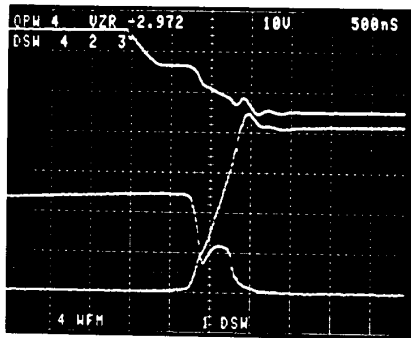
Fig.7: Zero-voltage turn-off process with C_E=22nF; scales and parameters as in Fig.3.
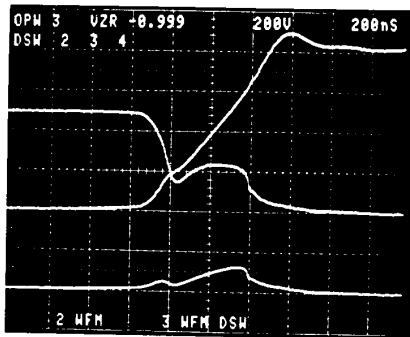
Fig.8: Zero-voltage turn-off; above: collector-emitter voltage and collector current; below: instantaneous turn-off power (C_E=22nF, W_{off}=5.7mJ); for scales and other parameters cf. Figs.3. and 4.

changed as compared to snubberless switching. The voltage across the switch rises accordingly to the commutation of the load current from the valve into the snubber capacitor C_E. Figure 7 clearly shows the reduced stress on the switch during turn-off as compared to switching without snubber (cf. Fig.3).

The switch current does not go to zero as fast as for snubberless switch-

ing, however. The minority carriers which are stored in the N- epi layer of the power electronic device lead to a considerable delay of the turn-off of the device after turn-off of the MOSFET-channel. This has to be seen in connection with the then capacitive base current of the PNP transistor part. This base current remains on within the voltage rise time. Managing of this effect is only possible via a sufficiently high capacitance of the turn-off snubber capacitor C_E. This, on the other hand, in turn will limit the maximum obtainable switching frequency.

Due to the fact that the IGBT turns on again partially during the voltage rise, the turn-off energy loss (cf. Fig.8) is reduced by a lower amount than could be expected initially.

However, the evaluation of the switching losses in dependency on the snubber capacitance shows in spite of this fact a significant reduction of the turn-off losses (c.f. Fig.9). The turn-off losses are decreased for increasing values of the snubber capacitance and reach about one third of the value of snubberless switching. There the voltage rate of rise amounts to about 450V/μs. A further reduction of the voltage rate of rise below this characteristic value results only in a small improvement.

There remains in principle a loss contribution which is determined by the life time of the minority carriers (which cannot be removed by suction from the base as possible for bipolar transistors) flowing out of the power electronic device ("tail current") and by the blocking voltage rate of rise. The duration (determined by the snubber capacitor) of the voltage rise itself (for 450V/μs and U_{ZK}=820V) allows switching frequencies of up to about 250kHz. However, the turn-off losses determine the obtainable switching frequency; the turn-off losses amount to about 90W for 820V DC link voltage and 25kHz switching frequency.

As a consequence, a further reduction of the turn-off losses is only possible
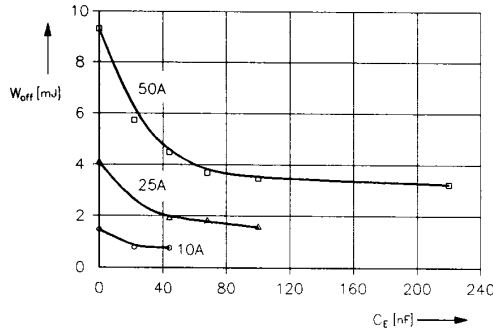
Fig.9: Turn-off losses W_{off} vs. snubber capacitance C_E ($U_{ZK} = 820V$, $U_G = +15V/-5V$, $R_G = 22\Omega$, $T_j = 125°$); parameter: switched load current. As already noted for the turn-off without snubber, the losses for $U_{ZK}=680V$ can be determined again approximately by voltage-proportional transformation.

by avoiding the tail current, i.e. by zero- current switching or turn-off of the valve by a resonant circuit (see next section).

Remark: One has to note that for a full-bridge phase-shift PWM converter the bridge legs I and II (cf. Fig.1) encounter different turn-off conditions which have to be considered for dimensioning the snubber capacitors. Bridge leg I always is switched (cf., e.g., point of time t_0 or t_2 in Fig.1) from a free-wheeling mode into an active mode (energy being transferred to the secondary side). Therefore, the primary current is impressed only by the stray inductance $L_{\sigma,1}$, and not by the load circuit. If the capacitances $C_{p,1}$ and $C_{p,2}$ (which function reducing the switching power loss) are increased
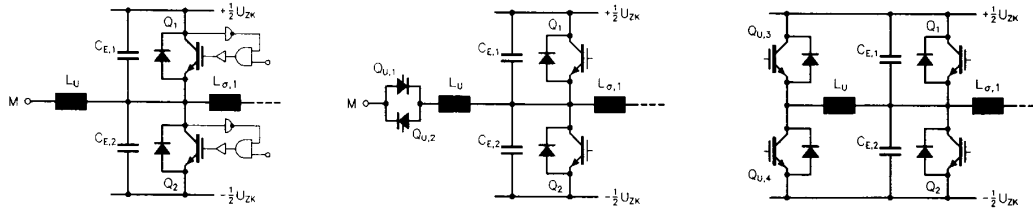
by explicit snubber capacitors there will take place a complete charging and recharging of the capacitances only for

$$i_1 \sqrt{\frac{L_{\sigma,1}}{C_{E,1} + C_{E,2} + C_{p,1} + C_{p,2}}} \geq U_{ZK} \qquad i_1 = I_L \frac{N_2}{N_1} \qquad (1)$$

(where the magnetising current is neglected) allowing the lossless turn-on of the transistor lying in opposite position of the bridge leg. The limitation of the load range (contained implicitely in Eq.(1)) for which a complete avoidance of the turn-on losses is given, can be avoided by using a charging and discharging circuit (cf. Fig.10, left-hand side). The bridge legs I and II work with a duty cycle of $\approx$50%. The triangular current flowing through the charging/discharging circuit (M: capacitive center point of the DC link voltage) allows (dis)charging of $C_{E,1}$ and $C_{E,2}$ also for no-load operation. As noted (in Fig.10) the switch is enabled only for low values of the collector-emitter voltage (dual thyristor mode). However, a higher current has to be turned off and additional conduction losses result in higher stresses on the transistors.

Further possibilities for the arrangement of (dis)charging circuits are also shown in Fig.10. The lower stress (on Q_1 and Q_2) connected with these variants (higher obtainable switching frequency as compared to the circuit described before) requires additional switching elements, however. A closer analysis and a comparison of the circuits is the topic of a future paper now in preparation.

For bridge leg II there occurs always a commutation from an active state to a free-wheeling state (commutation from Q_3 to D_4 or from Q_4 to D_3). There, the primary current is impressed by the load inductance; charging and discharging of $C_{E,3}$ and $C_{E,4}$ therefore can be described by

$$(C_{E,3} + C_{E,4} + C_{p,3} + C_{p,4}) \frac{du_{C,34}}{dt} = I_L \frac{N_2}{N_1} = i_1. \qquad (2)$$

For making no-load (or low-current) operation possible, also in this case a (dis)charging circuit has to be provided. Its dimensioning is based on other

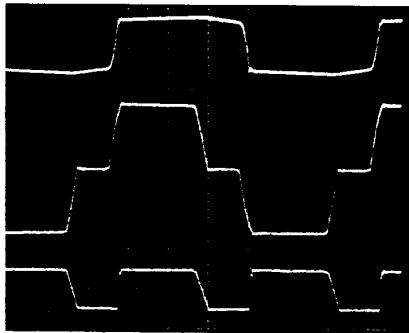**Fig.10:** For capacitive snubbing of a half bridge leg of phase-shifted PWM converter.

Fig.11: Primary current (20A/Div) and voltage (500V/Div) and secondary voltage (50V/Div) of a ZVS full-bridge phase-shifted DC/DC converter (from above to below; t: 5μs/Div). The "voltage loss" (occurring due to the transformer stray inductance and the charging and discharging of the snubber capacitances $C_{E,1}$ and $C_{E,2}$) of the secondary voltage as compared to the primary voltage (referred to the secondary) has to be considered for the determination of the capacitance of the snubber capacitors.

criterions, however, as compared to branch I; this results in a lower stress on switches Q_3 and Q_4.

The voltage and current shapes measured in a 20kW ZVS phase-shift PWM converter are shown in Fig.11. Besides the reduction of the switching losses, the application of snubber capacitors results in a considerable reduction of the EMI due to the then given trapezoidal shape of the primary voltage.

Zero Current Switching (ZCS)   [9], [10], [11], [12], [13]

Figure 12 shows the zero-current turn-off circuit (modified McMURRAY converter, known from the literature) which is treated in this paper. The function of the circuit can be described in an efficient manner by using the so-called u-Zi-diagram (state-plane analysis), cf.Fig.12.

At time t_0 the turn-off procedure of the current-carrying transistor Q_2 is initiated by turning on $Q_{L,2}$. For the commutation capacitor C there shall be $u_C(t_0) = -U_{ZK}$. At time t_1 the switch can be turned off with zero current. The current flow is given in the following by a reverse current of the power electronic device (minority carrier device) and by the current contribution $i_{D,2}$ flowing through the free-wheeling diode D_2 lying in antiparallel. At time t_2 the resonant current again reaches the load current, the free-wheeling diode starts blocking while the switch voltage jumps to the capacitor voltage given at this point of time.

Figure 13 shows switch current and voltage for the half-bridge module MG50Q2YS9 during the turn-off process for 50A switched current and an amplitude of 65A for the quenching current i_C (also cf. Fig.12). The valve therefore has to reach the blocking state within the time interval $[t_2 - t_1]$. The voltage rate of rise is essentially determined by the blocking behavior of the free-wheeling diode.

The voltage across Q_2 changes with a rate of rise of up to 8kV/μs for a junction temperature of 25°C and after all still with 4kV/μs for 125°C (cf. Fig.13). As a closer analysis shows, the turn-off losses of the free-wheeling diode without snubber (besides the du/dt-turn-on losses of Q_2) represent an essential part of those losses (of the circuit elements) which are linked to the switching frequency. With conduction of the free-wheeling diode D_1 begin-

ning in t_3 the commutation capacitor voltage is determined by an oscillation which includes the DC-link voltage. A period of time-linear charging by the load current in interval $[t_3-t_2]$ can be present before conduction of D_1. In the real circuit this period does not exist in all cases due to the reverse current flowing through Q_2 or D_2.

Figure 14 shows u_C and i_C vs. time or in the u-Zi-diagram for the turn-off process shown in Fig.13. There does not exist a time interval where i_C remains (approximately) constant and clamped to the load current I_L. Due to the high reverse current (cf. Fig.13) the commutation circuit rings back. From this instant on the voltage across Q_2 rises very fast towards U_{ZK} where the reverse current ends almost instantly (cf. Fig.13) and commutates into D_1. Therefore, one can assume for the resonant circuit that an oscillation
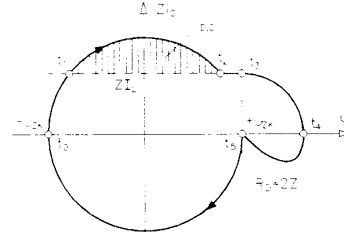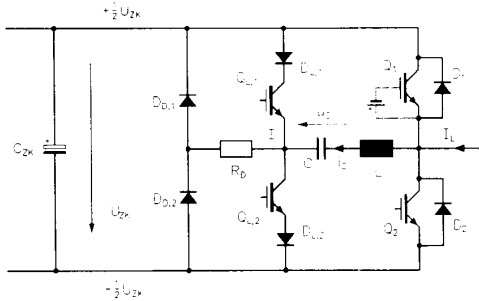

Fig.12: Structure of the power circuit for "force commutation" of the power electronic devices using a resonant circuit (step-down operation of the bridge leg Q_1, Q_2). Description of the current and voltage behavior for zero-current switching (using the so-called u-Zi-diagram, $Z = \sqrt{L/C}$).
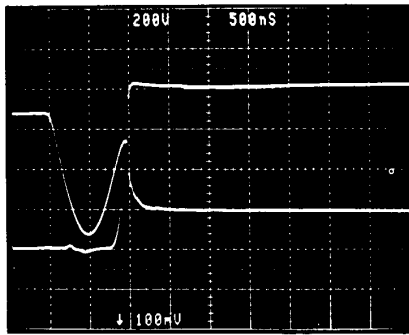

Fig.13: Zero-current turn-off behavior; $U_{ZK} = 820$V, $U_G = +15$V/-5V, $R_G = 22\Omega$, $T_j = 125^0$, U_{CE}: 200V/Div, i: 20A/Div, t: 500ns/Div.

around the DC link voltage starts immediately after the commutation period. This oscillation, the overcharging of the capacitor connected herewith, and the following discharging process can be seen clearly from Fig.14. The sudden decrease of voltage u_C immediately before the end of the commutation process is caused by a voltage being built up across circuit inductances. If one substracts the voltage across the circuit inductances from the measured voltage, one can clearly recognize the oscillation following the commutation process and its amplitude in the u-Zi-diagram.

Due to the commutation current reversal also the turn-off switch can be turned off itself with zero current. The diode $D_{L,2}$ connected in series takes over the blocking voltage $u_C(t_4) - U_{ZK}$. Via the damping circuit $R_{D,1}$ $D_{D,2}$ the commutation capacitor is discharged to the DC link voltage in the following. (Regarding other realization possibilities of this discharging circuit see Fig.15.) After a resonant process initiated by turning on $Q_{L,1}$ (immediately before turning on Q_2 again), leading through D_1, the capacitor voltage again reaches the value assumed at the beginning of this process. Due to the pulse stress of only short time duration, caused by the ringing current, IGBTs with relatively low constant current carrying ability can be used as turn-off switches. "Latching" of the turn-off switches caused by the high current amplitude does not lead to a malfunction. As described previously,
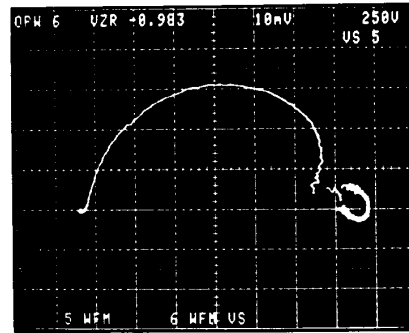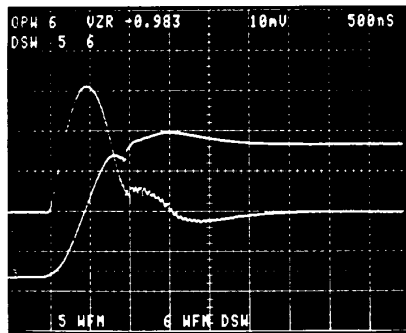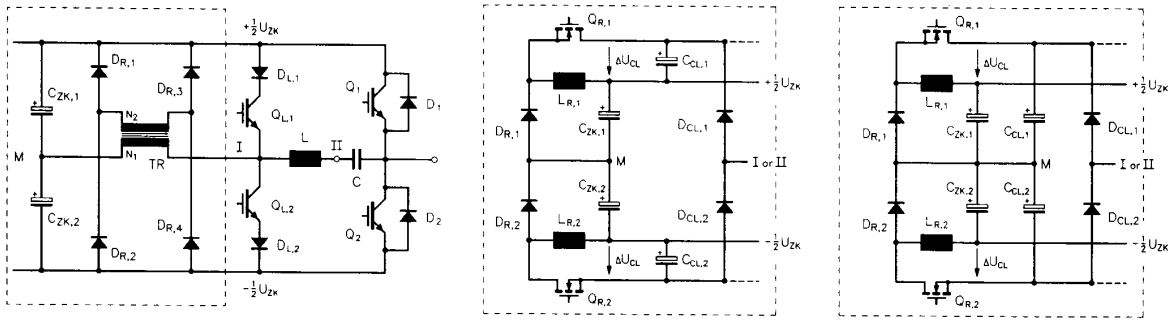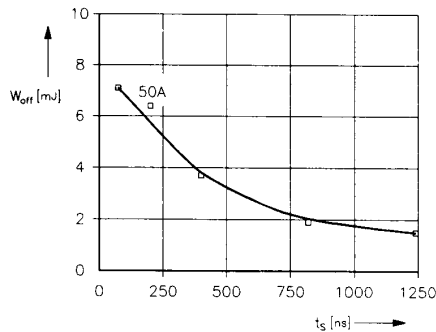

Fig.14: LEFT: Voltage u_C (500V/Div) across the capacitor and current i_C (20A/Div) of the commutation circuit; RIGHT: u-Zi-diagram of the commutation (250V/Div, 20A/Div).
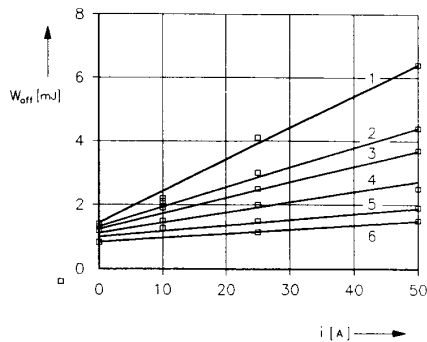
Fig.15: Basically lossless realised concepts of the damping network R_D, $D_{D,1}$, $D_{D,2}$ of a MᶜMᴜʀʀᴀʏ converter (especially of interest for power levels > 100kW). LEFT: feedback of the surplus energy of the commutation capacitor via a transformer TR; CENTER and RIGHT: energy feedback of the commutation capacitor and blocking voltage limitation to $(U_{ZK} + \Delta U_{CL})$ or ΔU_{CL}. (Center: energy feedback by buck-boost converter, right: energy feedback by buck converter.)

they are turned off in a resonant manner at the end of the ringing phase (and not via their gate).

Similarly, as already seen for the case of a capacitive snubber, also here unexpectedly high losses occur. The base charge of the PNP-transistor inside the IGBT is reduced only a little during commutation because the inverse current flows through the free-wheeling diode D_2. Therefore, only a small inverse voltage is built up. An increased commutation current (inverse current) only increases the turn-off losses in the inverse diode D_2. Furthermore, one

can see that the occurrance of the so-called "current tail" cannot be avoided. As already explained, a du/dt across the IGBT causes a partial turn-on which also occurs here after commutation (when voltage is being built up across the switch). If the voltage rise is delayed by an additional snubber, the current becomes more flat and lasts longer in a manner being characteristic for C-snubbers (see discussion in the previous section). The current in the main switch due to du/dt basically cannot be completely avoided by increasing t_S (the time where the voltage across the switch and the current are negative or zero, time for the recombination of the charge carriers, "hold-off intervall"). From Fig.16 we see the turn-off losses in the main switch Q_2 vs. t_S (hold-off interval).

One can conclude that the losses are cut in half once more as compared to applying purely capacitive snubbers. For decreasing load current the loss contribution of the main switch is decreased also on one hand, on the other hand the current-dependent loss contribution of the inverse diode is increased. For a good snubber dimensioning for the main switch the turn-off losses remain approximately constant for the entire load current region (cf. Fig.17). For this purpose there are relatively large values of t_S required, however (also, cf. Fig.16).

Fig.16: Turn-off losses W_{off} for a turn-off current i of 50A in the main switch Q_2 vs. time for recombination (hold-off interval) t_S (U_{ZK}=820V, T_j = 125°).

Fig.17: Approximation of the W_{off} vs. switched current i for different resonant circuits (1-6) with the same characteristic impedance Z = 12.3Ω. The resonant frequencies of the resonant circuits are: for circuit 1: 1MHz, 2: 667kHz, 3: 500kHz, 4: 336kHz, 5: 250kHz and 6: 168kHz (U_{ZK}=820V, T_j = 125°).

Conclusions

In this paper the turn-off losses for switching without snubber, with snubber capacitor (ZVS) and for "force commutation" (ZCS) have been investigated. The turn-off losses for ZCS become smaller than those obtained by conventional snubber circuits only for relatively long hold-off intervals. Here we have listed the best possible values which can be reached with sensible effort in the respective operating mode. The losses per switching cycle amount to 9.3mJ : 3.5mJ : 1.5mJ = 6.2 : 2.3 : 1 (9.3mJ for switching without snubber, 3.5mJ for zero voltage switching, 1.5mJ for zero current switching; switched current: 50A, U_{ZK}=820V, T_j = 125°). The obtainable switching frequencies approximately behave inversely proportional (1 : 2.7 : 6.2). Based on the results one can determine the entire power loss for different circuit concepts and their limitations (as far as no considerable turn-on losses have to be expected). This serves as basis for consideration and comparison of different circuit concepts.

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