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A Novel Switch-Mode Power Amplifier with High Output Voltage Quality Employing a Hybrid Output Voltage Filter

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Abstract — The paper presents a novel topology of a switch-mode power amplifier using a hybrid output filter consisting of a passive LC-circuit with a small linear amplifier connected in series to the capacitor of the LC-circuit. The linear amplifier compensates the voltage ripple of the capacitor resulting from the ripple of the output current of the switch-mode power stage. The design of the linear amplifier only has to be performed regarding the ripple voltage and current values of the passive filter part. The power dissipated in the linear amplifier becomes relatively small as compared to the output power of the total system and does not affect the overall efficiency significantly. Furthermore, with a proper arrangement of the linear amplifier the output impedance of the total system will be determined by the linear stage and not by the LC-filter and can therefore be kept very low. In contrary to a conventional switch-mode power amplifier the dynamic characteristic of the output filter influences the load voltage only in an implicit manner. The paper describes the operating principle of the system, analyzes the fundamental relationships for the circuit design and presents simulation results.

1 Introduction

Linear (class-A, or -AB) power amplifiers are replaced by switching (class-D) amplifiers in an increased quantity to improve the efficiency and optimize the power density of the system. However, if the output voltages have to be of very high quality (e.g., for test and measuring equipment) switching amplifiers show significant limitations. The output voltage of a class-D amplifier contains switching frequency noise of substantial amplitude which has to be reduced by a proper low-pass filter (cf. Fig.1). However, this filter – which has to be in general of higher order type – reduces the dynamic response and increases the output impedance of the total amplifier system. Furthermore, the interlock delay time of the usually applied bridge topologies and/or a ripple of the DC supply voltage and/or the on-state voltages of the power semiconductor devices (transistors and free-wheeling diodes) may result in low-frequency distortion which hardly can be reduced by the switching frequency output filter mentioned before. To avoid the disadvantages described above, circuit topologies can be applied which are formed by a parallel arrangement of a class-D switching system and a conventional linear amplifier stage [1], [2]. The essential drawback of such a system is that the linear amplifier part has to cover the full output voltage range of the system and that the remaining losses of the linear stage are about 5–10% (best case condition) of the output power, even if ripple reduction techniques are applied [3].

For a minimization of the losses the basic idea of the system presented in this paper in comparison to the systems presented in [2] is that the linear amplifier is connected to the class-D stage via a capacitive coupling element. The voltage across this capacitor would be approximately the output voltage of the system and therefore, the

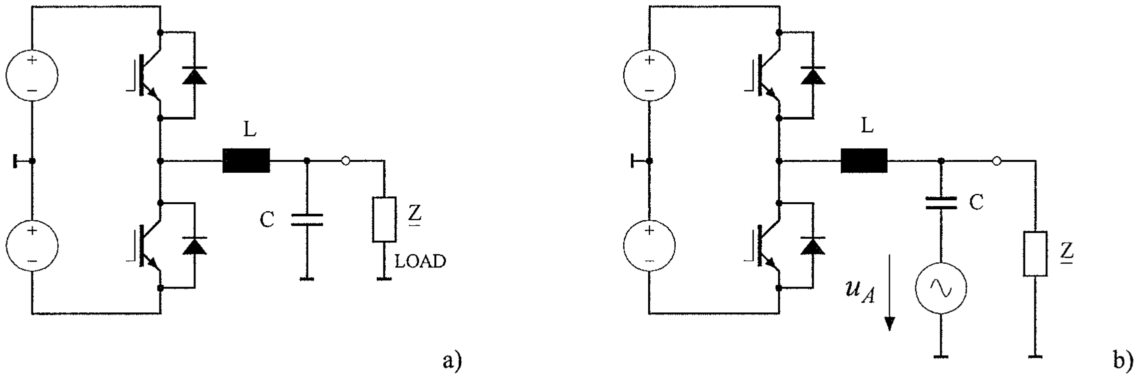


Fig.1: Circuit diagram of a conventional switch-mode power amplifier with a passive LC output filter a) and of the proposed topology employing a hybrid output filter b). There, the capacitor voltage ripple is compensated by a linear voltage source u_A.

linear stage only has to generate output voltages of a small amount as compared to the total output voltage. The presented topology can also be seen as a class-D amplifier employing a hybrid output filter consisting of a passive LC-circuit and a voltage source u_A which corrects the voltage ripple of the filter capacitor C (cf. Fig.1b). The voltage source is realized by a linear power amplifier stage whose supply voltage level can be chosen relatively low as compared to the DC link voltage of the switching stage because the linear amplifier only has to generate an output voltage which is equal to the voltage ripple of C but of opposite sign. Therefore, the total losses can be significantly reduced as compared to the amplifier systems presented in [1] and [2]. However, the control of such a system (cf. Fig.1b) becomes difficult because the total output voltage can be influenced by the duty cycle of the switching stage as well as by the output voltage of the linear amplifier. In the easiest case the linear stage could be treated as a method to increase the effective order of the passive output filter (e.g., to get a fourth order hybrid output filter applying only two passive reactance elements).

2 Basic Considerations

To overcome the drawback of defining the output voltage of the system indirectly as mentioned before, it is preferable to take advantage of the asymmetric structure of the output stage of linear power amplifiers (usually emitter followers or source followers, respectively). As can also be seen from its small-signal equivalent circuit diagram (cf. Fig.2a), a power transistor operating in linear mode is not symmetrical regarding the output impedance of the power terminals. The emitter forms a voltage-mode output with a low inner impedance defined by the transfer conductance g_m of the device, whereas the collector serves as a current terminal with a very high output impedance. Therefore, it is of significant advantage to exchange the position of the linear voltage source u_A and of the filter capacitor C (cf. Fig.2b). Now the output voltage u of the amplifier system is immediately defined by the linear stage (reference value u^* referred to GND; feedback system of the linear stage not shown in Fig.2b). The current-mode characteristic given by the collectors of the linear stage decouples the voltage ripple of the filter capacitor from the output and the voltage across the smoothing inductor L. Contrary to a class-D amplifier with a passive LC output filter as shown in Fig.1a, in the stationary case the currents i_L and i_C show a time-linear shape due to the first order transfer function given by L. According to $i_C = C \cdot du_C/dt$ there results a parabolic capacitor voltage u_C with an average value being identical to the output voltage u of the system. The voltage ripple of the capacitor does not appear at the output of the system because it is covered implicitly by the current source characteristic of the linear stage. It has to be pointed out, however, that a very low output impedance of the linear system

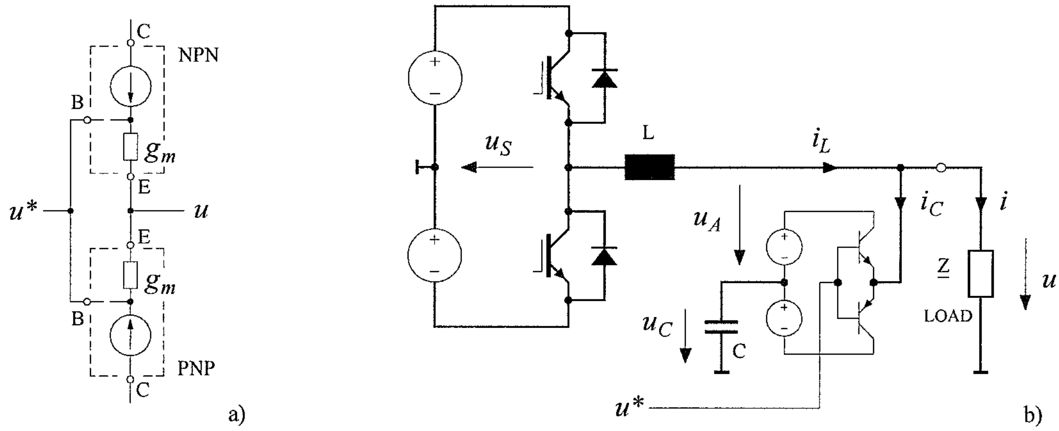


Fig.2: a) small-signal equivalent circuit of a push-pull emitter follower; b) proposed arrangement of the linear amplifier stage connected directly to the output of the amplifier system.

part is of paramount importance to get an output voltage with a high signal-to-noise ratio. This circumstance has to be considered by an appropriate design of the linear amplifier circuitry and feedback system. Concerning the control of the system it has to be mentioned that the output voltage u is defined by the linear stage. The control of the switching stage has to be performed in that way that the capacitor voltage u_C follows u as close as possible. With this the output voltage u_A of the linear amplifier and as a conclusion its necessary supply voltage level gets as small as possible which is of importance for minimizing the losses of the linear stage.

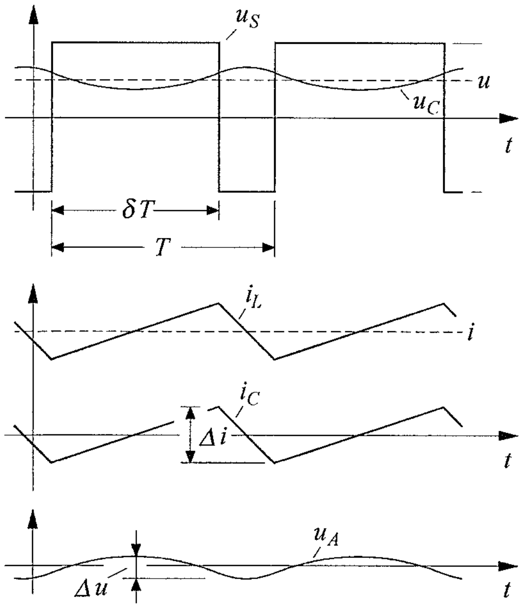
3 Stationary Operation

For analysis of the stationary operation behavior the voltage and current wave shapes within a switching interval T are calculated. For this it is assumed that the output voltage u of the system (defined by the linear stage) and, furthermore, also the load (output) current i are constant within T (i.e., the switching frequency $f_S = 1/T$ of the class-D stage is assumed high as compared to the frequency of the output signals u and i). Due to the zero average value of the voltage across the smoothing inductance L the duty cycle of the switching stage can be calculated as

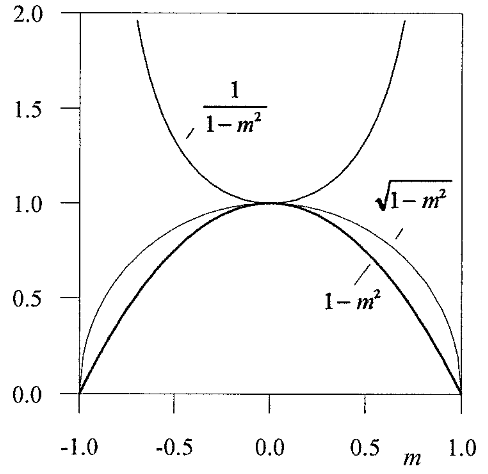
$$\delta = \frac{1+m}{2} \qquad \text{and} \qquad 1-\delta = \frac{1-m}{2}, \tag{1}$$

where the definition $m = u/U$ of a local modulation index (output voltage u related to the DC link voltage $\pm U$) is used. Considering the assumption described before we get a triangular shape for the inductor current i_L and also for the capacitor current i_C (cf. Fig.3a). As a result, the capacitor voltage shows a parabolic shape. Integrating the fundamental differential equations $u_L = L\,di_L/dt$ and $i_C = C\,du_C/dt$ within the relevant time intervals ($[0,\delta\, T]$ for i_L and $[\delta\, T/2,(1+\delta)T/2]$ for u_C) yields the two basic ripple relationships of the system:

$$\boxed{f_S \cdot \Delta i = \frac{U}{2L}\cdot\left(1-m^2\right)} \qquad \boxed{\Delta u = \frac{\Delta i}{8 f_S C}} \tag{2}$$



a)



b)

Fig.3: a) voltage and current wave shapes of the presented amplifier system of Fig.2b; b) dependency of switching frequency and ripple voltage according to Eqs.(3,4,6,7).

The further analysis of the system depends on the selected operating mode of the current control. The simplest method (A) to guide i_L can be achieved by application of a hysteresis controller with constant (i.e., independent of the modulation index m) width of the tolerance band $\Delta i = \Delta I$. With this assumption Eqs.(2) can be rewritten as

$$f_S(m) = \frac{U}{2L\Delta I} \cdot \left(1 - m^2\right) = f_{S,0,A} \cdot \left(1 - m^2\right) \qquad \Delta u(m) = \frac{\Delta I}{8 f_S(m) \cdot C} = \frac{\Delta I^2 L}{4UC} \cdot \frac{1}{1 - m^2} = \Delta U_{0,A} \cdot \frac{1}{1 - m^2} \quad (3)$$

where the abbreviations $f_{S,0,A} = U/(2L\Delta I)$ and $\Delta U_{0,A} = (\Delta I^2 L)/(4UC)$ (switching frequency and voltage ripple for zero output voltage $m = 0$) are used. The drawback of this control method is that the switching frequency becomes very small for large output voltage levels $|m| \to 1$. Due to the inverse proportional dependence of the voltage ripple on the switching frequency this results in a high voltage ripple (cf. Fig.3b). To give the linear stage the ability to compensate this ripple, its supply voltage has to be selected correspondingly high. This increases the losses of the linear stage and worsens the efficiency of the total amplifier system.

The described disadvantage could be avoided by application of a control structure (B) with a switching frequency being not dependent on m, e.g., by using a pulse width modulator or a hysteresis current controller with an adaptive width of the tolerance band. With this assumption of constant f_S the basic relationships (Eqs.(2)) yield

$$\Delta i(m) = \frac{U}{2 f_S L} \cdot \left(1 - m^2\right) = \Delta I_{0,B} \cdot \left(1 - m^2\right) \qquad \Delta u(m) = \frac{U}{16 f_S^2 LC} \cdot \left(1 - m^2\right) = \Delta U_{0,B} \cdot \left(1 - m^2\right) \qquad (4)$$

where the abbreviations $\Delta I_{0,B} = U/(2 f_S L)$ and $\Delta U_{0,B} = U/(16 f_S^2 LC)$ for $m = 0$ are used. Due to the constant switching frequency now also the ripple voltage amplitude follows the relationship $1 - m^2$ and, therefore, $\Delta u \to 0$ for $|m| \to 1$ (cf. Fig.3b). The normalization of the highest voltage ripple amplitude (peak-to-peak value) $\Delta U_{0,B}$ (valid for modulation index $m = 0$) with respect to the total DC link voltage $2U$ and substituting the resonance frequency $\omega_{res} = 1/\sqrt{LC} = 2\pi f_{res}$ of the output LC filter (which defines the large-signal bandwidth of the amplifier system) gives a fundamental relation between the voltage ripple and the switching frequency-to-bandwidth ratio

$$\frac{\Delta U_{0,B}}{2U} = \frac{1}{2\cdot 16 f_S^2 LC} = \frac{\omega_{res}^2}{32 f_S^2} = \frac{4\pi^2}{32}\frac{f_{res}^2}{f_S^2} = \frac{\pi^2}{8}\left[\frac{f_{res}}{f_S}\right]^2 = 1.23\left[\frac{f_{res}}{f_S}\right]^2 . \qquad (5)$$

If, e.g., a switching frequency of tenfold the bandwidth of the amplifier is used (as this is usually the case for conventional class-D amplifiers), there results a peak-to-peak voltage ripple of only 1.23% of the total DC link voltage. On the other hand, for a system of $2U = 600\,\text{V}$ DC link voltage and a ±15 V supply voltage of the linear stage a switching frequency of only $f_S \approx 5 f_{res}$ would be necessary.

A further control method (C) aiming for a voltage ripple $\Delta u = \Delta U$ being not dependent on the modulation index m gives an optimal utilization of the supply voltage of the linear stage. In this case there results for the switching frequency from the basic equations (2)

$$f_S(m) = f_{S,0,C}\cdot\sqrt{1-m^2} \qquad \text{with} \qquad f_{S,0,C} = \sqrt{\frac{U}{16LC\cdot\Delta U}} = \sqrt{\frac{U}{\Delta U}}\cdot\frac{\omega_{res}}{4} = \sqrt{\frac{U}{\Delta U}}\cdot\frac{\pi}{2}\cdot f_{res} \qquad (6)$$

(cf. Fig.3b). According to the right relationship of Eqs.(2) this control can be performed, e.g., by applying a hysteresis current control with adaptive width of the tolerance band:

$$\Delta i(m) = \Delta U\cdot 8\cdot C\cdot f_S(m) = \Delta U\cdot 8\cdot C\cdot f_{S,0,C}\cdot\sqrt{1-m^2} = \Delta i_{0,C}\cdot\sqrt{1-m^2} \quad \text{with} \quad \Delta i_{0,C} = \sqrt{\frac{4U\cdot\Delta U}{L/C}} . \qquad (7)$$

4 Dynamic Behavior – Control Structure

Contrary to the systems presented in [1]–[3] the full power bandwidth and the large-signal transient response of the amplifier system described in this paper is defined – as already mentioned in the previous section – by the corner frequency f_{res} of the LC output filter. However, the control structure of the system is not of the well known second order type (as this is true for conventional class-D amplifier systems) because the output voltage u of the system is determined by the linear stage with its separate feedback loop (the design of this loop is not influenced by the control of the switching stage). Considering the stationary case the control of the switching stage has to be performed such that the average value of i_L within a switching period is equal to the load current i. With this the average capacitor current becomes zero and the average capacitor voltage is equal to the output voltage u. The simplest control of the switching stage therefore would be to measure the output current i and to use this quantity as the reference value of the inductor current i_L. Considering $i_L - i = i_C$ (cf. Fig.2b), the control mentioned before

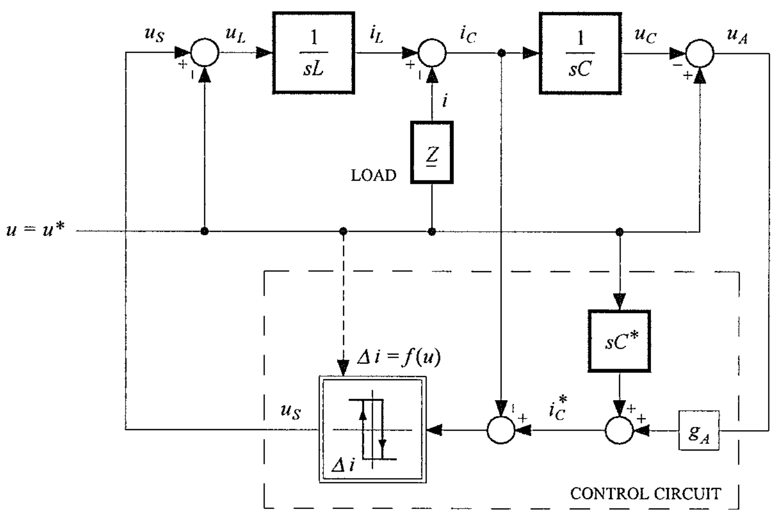


Fig.4: Control structure of the realized amplifier system; current control of the switching stage is realized by application of a hysteresis controller with adaptive width of the tolerance band.

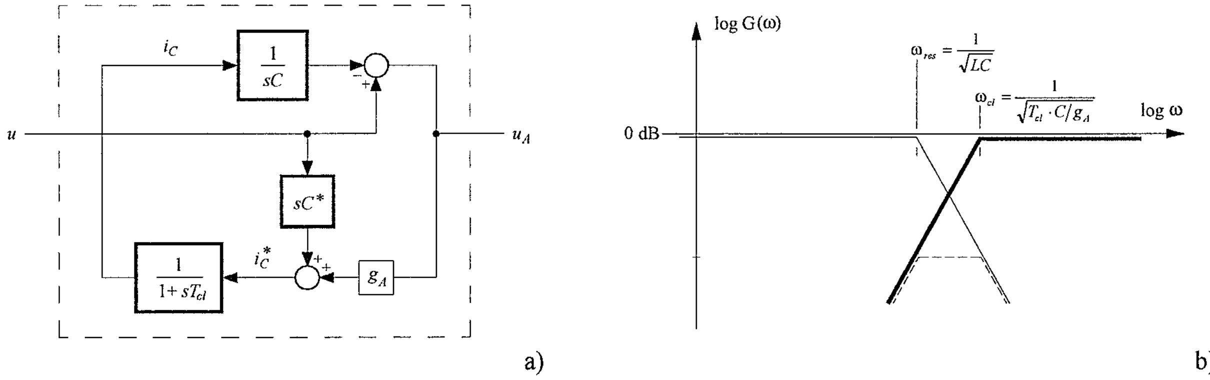


Fig.5: a) Control-oriented structure diagram defining the disturbance transfer function $G(s) = U_A(s)/U(s)$; b) Bode-diagram of $G(s)$ (bold line, corner frequency ω_{cl}) and large-signal frequency response (thin line) given by the resonance frequency ω_{res} of the LC-filter; the maximum amplitude of the linear stage output voltage appears within the region ω_{res} to ω_{cl} (dashed line).

can be realized by application of a hysteresis controller whose input is formed exclusively by the actual value of the capacitor current i_C (i.e., $i_C^* = 0$). To extend this scheme to the non-stationary case a pre-control of the capacitor current according to $i_C = C \cdot du/dt$ (in the LAPLACE-domain this results in the zero sC^* shown in Fig.4) is necessary to avoid signal frequency voltage components at the output of the linear stage. (It should be noted, that the fundamental operating principle of the presented system is given by the application of a capacitive coupling element to block the output voltage of the system from the output of the linear stage.) Assuming a perfect pre-control ($C^* = C$) the output voltage u_A of the linear stage only has to compensate the switching frequency component of the capacitor voltage caused by the ripple current through L. However, the zero average value of u_A has to be guaranteed by extending the control circuit employing a separate voltage feedback path. In the simplest case a proportional-type controller g_A generates an additional capacitor current reference value for $u_A > 0$. This additional current charges C and according to $u = u_A + u_C$ this reduces the output voltage u_A of the linear stage.

For simplification of the control-oriented analysis the dynamic performance of the current control loop is approximated by a first-order delay $I_C(s) = I_C^*(s) \cdot 1/(1+sT_{cl})$. With this the disturbance transfer function between the output voltage u of the total system and the output voltage u_A of the linear stage can be calculated according to Fig.5a as

$$G(s) = \frac{U_A(s)}{U(s)} = \frac{s^2 T_{cl} \cdot C/g_A}{1 + s \cdot C/g_A + s^2 T_{cl} \cdot C/g_A} \quad \text{and} \quad \omega_{cl} = \frac{1}{\sqrt{T_{cl} \cdot C/g_A}} \tag{8}$$

where $C^* = C$ is assumed. The relation given before describes a second order high-pass characteristic with the corner frequency ω_{cl} (cf. Bode-diagram Fig.5b). As mentioned in section 3, the power bandwidth of the system is given by the resonance frequency $\omega_{res} = 1/\sqrt{LC}$ of the LC circuit. To avoid that the linear stage will be driven into saturation it is necessary therefore to limit the bandwidth of the signal to be amplified. This can be realized using a proper input pre-filter which implicitly covers the characteristic of the LC stage. In Fig.5b, a second order low-pass with a cut-off frequency being equal to the LC-resonance frequency ω_{res} is shown. Consequently, the maximum amplitude of u_A appears in the frequency region $\omega_{res} \ldots \omega_{cl}$ (cf. dashed line of Fig.5b). The corner frequency ω_{cl} of $G(s)$ and as a result the maximum amplitude $U_{A,\max}$ can be influenced by the gain g_A of the voltage feedback path. However, it should be noted that the voltage component $U_A(\omega)$ calculated using Eq.(8) is caused exclusively by input voltage variations and does not include the switching frequency voltage ripple Δu which is calculated by Eq.(2).

5 Design Example – Simulation Results

In the following a prototype system of the proposed amplifier structure shall be calculated briefly and verified by digital simulation. The amplifier should supply a 1kHz-signal with an average power of 5kW into a purely resistive load of $\underline{Z} = R = 6.25\,\Omega$. Therefore, a load current amplitude of $\hat{I} = 40$ A and a maximum output voltage of $\hat{U} = 250$ V results. In order to guarantee a sufficient voltage margin, a total DC link voltage of $2U = 600$ V has to be chosen. Neglecting the voltage drop across the smoothing inductance L, the modulation index and the duty cycle vary in the region of $m = -\frac{5}{6}...+\frac{5}{6}$ or (according to Eq.(1)) $\delta = \frac{1}{12}...\frac{11}{12}$, respectively. Because the relatively high DC link voltage requires 1000V switching devices, ultra-fast IGBTs with explicit soft-recovery free-wheeling diodes arranged in parallel have been selected. The application of MOSFETs would not reduce the switching losses to a very large extent, because the turn-on losses of a hard switched bridge topology are essentially influenced by the reverse recovery characteristic of the free-wheeling diodes; especially the body diode of a high voltage MOSFET shows a very poor recovery characteristic. Furthermore, the $R_{DS,on}$ of a MOSFET with 1000V break-down voltage becomes very high as compared to a similar IGBT device due to the absence of minority carriers in the MOSFET. Depending on the operation mode the better turn-off behavior of the MOSFET can be neutralized by its higher on-state losses.

The dimensioning of the LC circuit considers a power bandwidth of about 5 kHz. Assuming a maximum current ripple of about 10% (4A) of the peak output current and a switching frequency of approximately 62.5 kHz ($T = 16\,\mu$s; reduced current utilization of the IGBT) results in $L = 600\,\mu$H and $C = 2\,\mu$F. The control of the system is performed according to method B of section 3, i.e., the switching frequency f_S does not depend on the modulation index m. This is achieved by application of a hysteresis current controller whose width of the tolerance band (and as a result also the capacitor voltage ripple) varies according to $1 - m^2$. With Eq.(4) the maximum voltage ripple valid for the stationary case can be calculated as

$$\Delta U_{0,B} = \frac{U}{16 f_S^2 LC} = \frac{300\,\text{V}}{16 \cdot (62.5\,\text{kHz})^2 \cdot 600\,\mu\text{H} \cdot 2\,\mu\text{F}} = 4\,\text{V}_{\text{pp}}\,. \tag{9}$$

A pre-control sC of the capacitor current as shown in Fig.4 is implemented in the control circuit; the gain of the voltage feedback path is adjusted to $g_A = 0.2$ A / V resulting in a time constant of $C/g_A = 10\,\mu$s (cf. Fig.5). As a

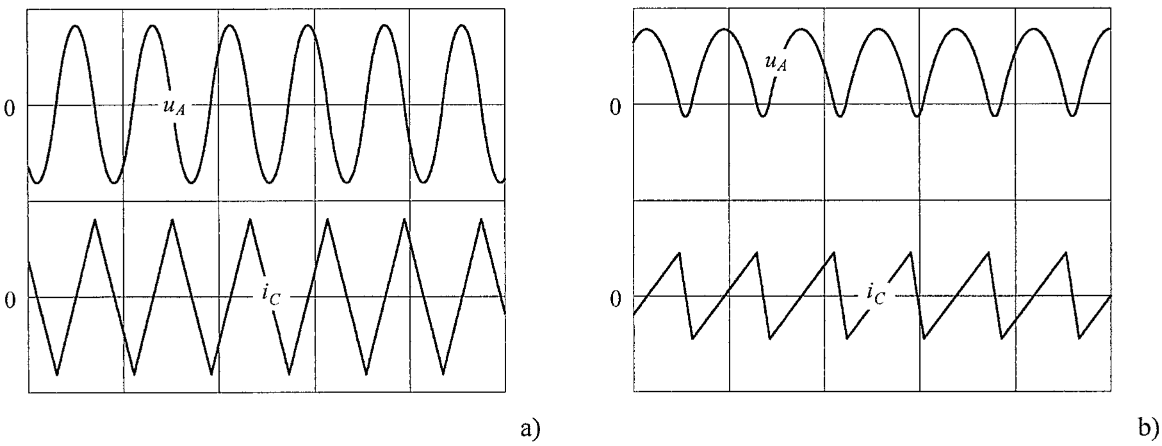
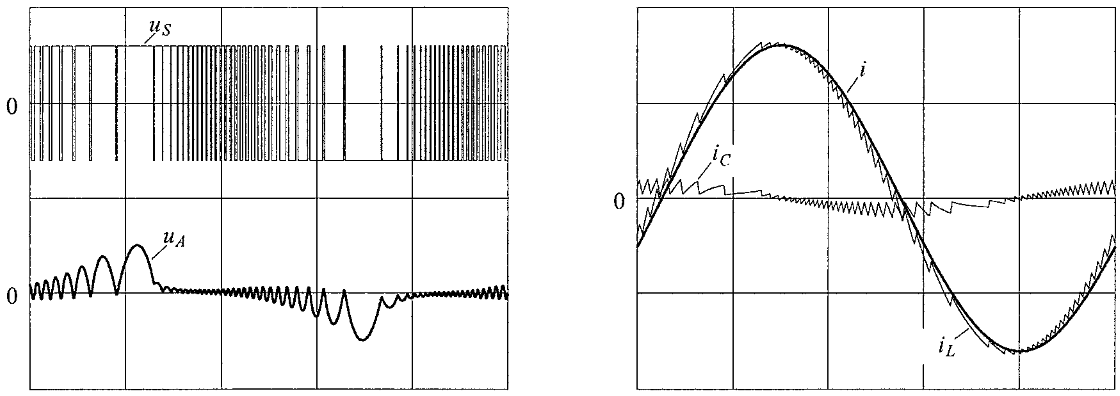


Fig.6: Stationary behavior of the output voltage u_A and of the output current i_C of the linear voltage correction stage for total output voltage of a) $u = 0$ V ($m = 0$, $\delta = 1/2$) and b) $u = 200$ V ($m = 2/3$, $\delta = 5/6$); parameters: $L = 600\,\mu$H, $C = 2\,\mu$F, $f_{res} = 4.6$ kHz, $\underline{Z} = R = 6.25\,\Omega$, $f_S = 62.5$ kHz ($T = 16\,\mu$s), $\Delta I_{0,B} = 4$A; scale: 2.5 A / div, 2.5V / div, 20μs / div.

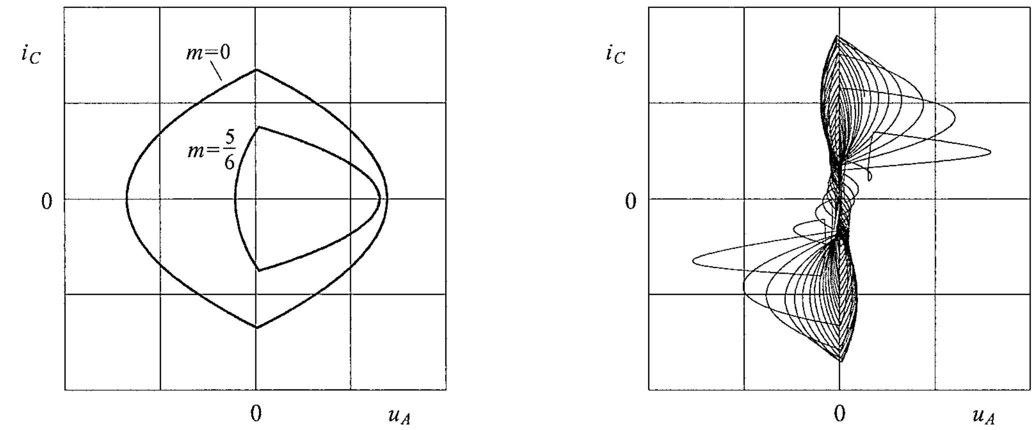


a) b)

Fig.7: 1kHz / 5kW - sine wave response of the amplifier system; a) output voltage u_S of the switching stage (500 V/div) and output voltage u_A of the linear stage (25 V/div); b) current wave shapes (25 A/div); time scale: 0.2ms / div.

closer analysis shows (not given here for the sake of brevity) and as can be seen from Fig.6b, this feedback method does not result in a zero average value of u_A if $m \neq 0$. This could be achieved if a more complex transfer function is applied instead of the simple gain g_A. However, the optimal utilization of the supply voltage of the linear stage requires symmetrical positive and negative peak values of the u_A - signal and not a signal with zero average value.

Figure 7 presents the 1kHz / 5kW sine wave response of the power amplifier. There it has to be pointed out that the switching frequency is not constant as expected from Fig.6. The reason for this is that the width of the tolerance band of the current controller is adapted according to Eq.(4) using the output voltage u (reference voltage). Due to the voltage across the inductance L this control is imperfect because the half bridge has to generate the output voltage $u + L\,di/dt$. A more precise controller therefore would have to consider the described effect. However, a pre-control of the tolerance bandwidth with $L\,di/dt$ would require a current measurement. Figure 8 shows the u_A / i_C - trajectories of the system according to the stationary case of Fig.6 (cf. Fig.8a) and to the sine wave response of Fig.7 (cf. Fig.8b). It has to be pointed out that these diagrams demonstrate the decoupled structure of this LC circuit due to the defined output voltage as compared to the circular trajectories of a conventional



a) b)

Fig.8: u_A / i_C - trajectories of the a) stationary behavior according to Fig.6 and b) of the sine wave response according to Fig.7; scale: a) u_A : 1.5V/div, i_C : 1.5A/div; b) u_A : 8V/div, i_C : 3A/div.

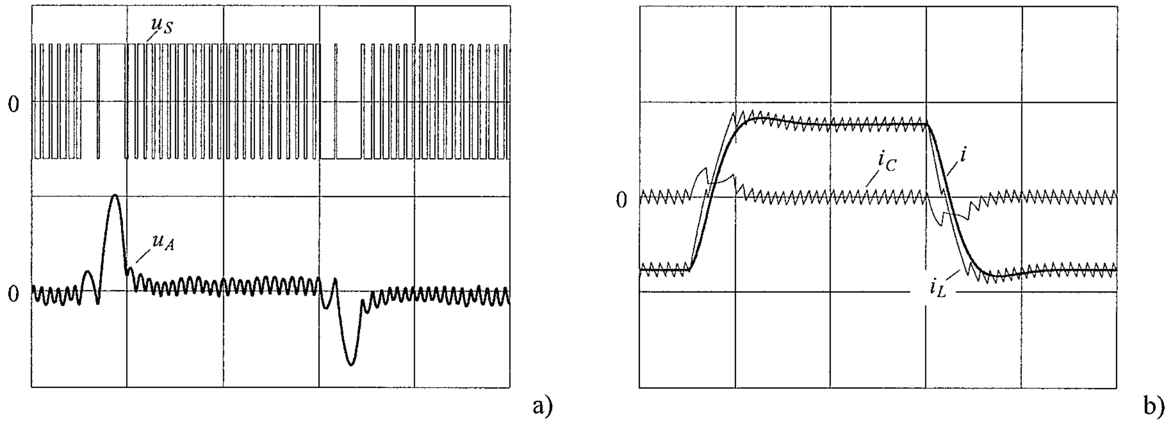


Fig.9: 1kHz - pulse response of the amplifier system; a) output voltage u_S of the switching stage (500 V/div.) and output voltage u_A of the linear stage (25 V/div); b) current wave shapes (25 A/div); time scale: 0.2ms / div.

LC resonant circuit. Especially for the pulse response of the system (cf. Fig.9) it is essential that the reference input signal shows a band width limitation according to the resonance frequency of the LC circuit. Otherwise the linear stage would have to generate voltage spikes of significant amplitude (cf. u_A in Fig.9a) which usually is not possible due to its relatively low supply voltage level. Therefore, a well damped second order input filter of equal cut-off frequency as the LC circuit is connected in series to the input of the system. Furthermore, the not perfect adaptive current controller hysteresis as a result of the neglected inductor voltage – already discussed in connection with Fig.7 – leads to a remarkable increase of u_A during rapid changes of the u. Remark: All the simulations presented in this paper have been performed with the control oriented simulation system ANA which is a versatile but easy-to-use simulation package available from a Web-server of the Technical University Vienna [4].

To conclude this section, Fig.10 shows an extended structure diagram of the system. There, the adaptive width of the tolerance band is realized by multiplying the control error $i_C^* - i_C$ by the factor $U^2/(U^2 - u^2) = 1/(1 - m^2)$. The total control system of the switching part is of relatively low complexity. Therefore, it can be implemented with relatively low effort. For sensing the capacitor current (which is the only current that has to be measured for the control) a small shunt resistor connected in series to the capacitor can be applied (i.e., the current measuring

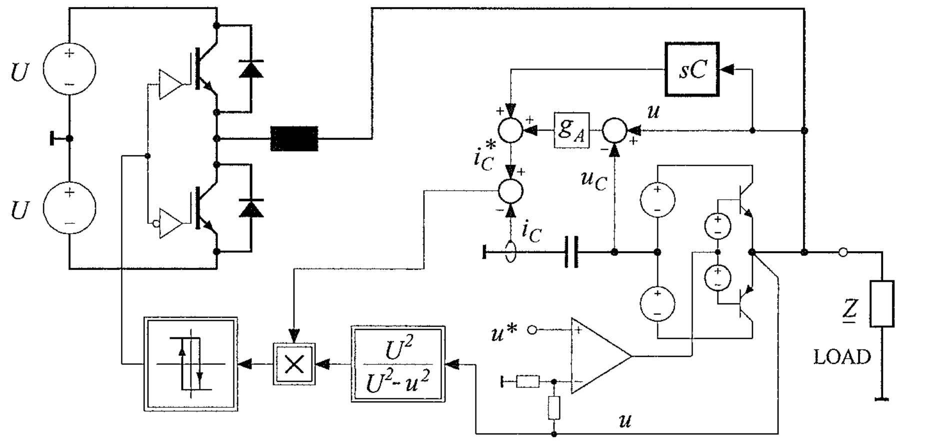


Fig.10: Extended structure diagram of the power circuit and of the control circuit of the proposed switching amplifier using a hybrid output voltage filter topology.

signal is already referenced to ground). This resistor does not influence the output impedance of the system (which is important to get a low switching frequency noise voltage component) because it is located in the high impedance current source collector path of the voltage follower stage. The total output impedance is defined by the emitter followers of the linear stage in connection with the inner impedance of the driver circuit and the loop gain of the feedback path of the linear stage. A more detailed discussion of this problem area is omitted here and can be found in [2]. The second order bandwidth limiting filter located in the input path of the system is not shown in Fig.10. However, it should be pointed out that the differentiating element sC (used for the pre-control of the capacitor current) can be realized advantageously by tapping the input of the last integrator of the second order input filter.

6 Conclusions

The power amplifier system presented in this paper can be considered as a class-D switching amplifier with a hybrid output voltage filter. This filter consists of a passive LC circuit with an active correction voltage source connected in series to the capacitor to compensate the voltage ripple. This ripple is caused by taking over the ripple current of the smoothing inductance L. The correction voltage source is realized by a linear amplifier with a relatively small power level as compared to the total output power of the system because the output voltage is blocked off by the filtering capacitor C. Due to the asymmetric structure of linear voltage followers this linear amplifier can be arranged in such a way that the output impedance of the total system is given basically by the very low impedance of the linear stage. (There, a proper design of the circuit of the output stage, of the driver stage and a sufficient loop gain of the linear amplifier is assumed.) It has to be pointed out that the main advantage of the presented system is that the total output impedance is defined by the impedance of the linear stage and that it is not given by the much higher reactance of C. From this, there results an almost ideal voltage source characteristic of the system which is also of significant importance in order to obtain a high switching frequency noise rejection of the output voltage. The drawback of the presented power amplifier structure, however, is that the total power bandwidth is given by the passive LC filter circuit (as this is the case for pure class-D structures) and cannot be extended by the linear amplifier part. Furthermore, it should be pointed out that the linear stage requires a floating power supply with respect to the ground terminal of the load. In addition, the output voltage of the driver stage of the voltage follower has to cover the full output voltage range of the system. This complicates its circuitry, especially because the very low necessary output impedance of the linear stage also requires a low impedance of the driver. Within the scope of further research a laboratory model of the circuit shown in Fig.10 is being realized at present. A summary of the results of the experimental investigations and a comparison to a system employing a hybrid output filter with grounded correction amplifier will be presented in a future paper.

References

[1] G. B. Yunt, "Series- or Parallel-Connected Composite Amplifiers," *IEEE Transactions on Power Electronic*, PE-1, Vol.1, No.1, pp. 48–54 (1986).

[2] H. Ertl, J. W. Kolar, and F. C. Zach, "Basic Considerations and Topologies of Switched-Mode Assisted Linear Power Amplifiers," *IEEE Transactions on Industrial Electronics*, IE-1, Vol.44, No.1, pp. 116–123 (1997).

[3] H. Ertl, J. W. Kolar, and F. C. Zach, "A New 1kW Class-D Supported Linear Power Amplifier Employing a Self-Adjusting Ripple Cancellation," *Proc. of the 29th International Conference on Power Conversion*, Nürnberg, Germany, May 21–23, pp. 265–274 (1996).

[4] J. W. Goldynia and J. M. Marinits, "Simulation System ANA – Version 2.12," Simulation Software and Reference Manual (PDF-file in german) can be found on http://www.iert.tuwien.ac.at .