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***Abstract*—As the demand for energy in AI-driven data centers continues to rise, there is an urgent need for innovative solutions to enhance the efficiency and power density of isolated three-phase AC/DC converters. In this context, the Integrated-Active-Filter Rectifier (IAFR) emerges as a promising solution due to its low complexity and high efficiency, achieved through the low switching frequency of all power semiconductors except for an injection leg needed to shape the three-phase sinusoidal input currents. However, the IAFR's performance limits concerning efficiency and power density, as well as its behaviour under unbalanced grid conditions, are still unclear. This paper presents a detailed analysis of the IAFR operation and introduces a Triangular-Current-Mode (TCM) operation for the injection leg, ensuring Zero-Voltage-Switching (ZVS) across the entire grid cycle. Additionally, a control strategy for the IAFR is proposed to ensure sinusoidal input currents and minimize power fluctuations under unbalanced grid conditions. The proposed control and modulation strategies are verified through simulations, while a multi-objective Pareto optimization is employed to determine the performance limits of the IAFR when paired with an isolated downstream DC/DC converter stage required for galvanic isolation and output voltage regulation.**

***Index Terms*—Three-phase, PFC Rectifier, Multi-Objective Pareto Optimization, Synergetic Control, Isolated Power Converter.**

I. Introduction

The global data center sector is a significant contributor to the world's electricity consumption, accounting for 1.7% - 2.2% of global electricity use [1]. With the rapid growth of data centers, projected to expand at an annual rate of 5% - 10%, energy demand is expected to increase substantially over the next decade [2], [3]. In this context, electricity represents 40% - 80% of the operational expenses for data centers, making it crucial to improve the efficiency of power conversion systems to lower costs and meet sustainability targets [4].

Fig. 1 illustrates a typical data center power supply system, where the AC/DC conversion is performed by multiple parallel power racks whose next-generation goal is reaching 99% efficiency while providing galvanic isolation [5], [6]. Additionally, as highlighted from the key power rack parameters in **Tab. I**, these power racks must maintain reliable operation even under unbalanced grid conditions (about 10% of phase-voltage amplitude variation, and 10° of phase-voltage displacement).

To achieve high power-conversion efficiency, efforts are being made to reduce conversion stages in AC/DC systems, leading

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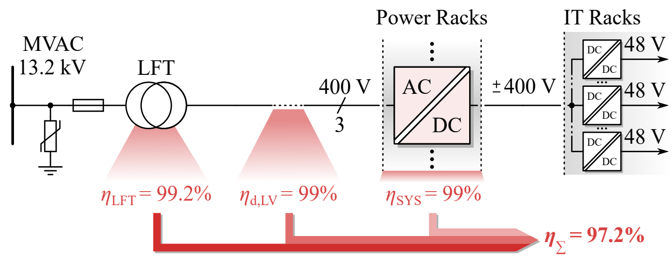

Fig. 1. Typical data center power supply system from MVAC to IT racks [5].

Table I. Key Specifications of the Power Rack.

Description	Symbol	Value	Unit
Nominal line-to-line RMS input voltage	V_{m}	400	V
Nominal input frequency	f_{m}	50	Hz
DC output voltage	V_{out}	400	V
Max. line-to-neutral amplitude unbalance	Δv	±12.5	%
Max. line-to-neutral phase unbalance	$\Delta\varphi$	±10	°

to the adoption of single-stage isolated converters that combine AC/DC conversion and output regulation [6]. These solutions enable high efficiency and, in recent studies, simplified control schemes enabled by MOSFETs in anti-series connection [7]. While these solutions show great promise, they are set to be even more competitive with the off the shelf availability of Monolithic Bidirectional Switches (MBDSs) in the near future [8]–[10].

Nevertheless, the complexity of single-stage isolated converters may compromise reliability, a critical concern given that power failures account for 43% of data center outages [11]. Therefore, reliable topologies and power converter structures remain a priority to ensure stable operation even under demanding scenarios, such as unbalanced grid conditions [12].

This paper focuses on a promising solution to these challenges: the quasi-single-stage converter, shown in **Fig. 2a**, consisting of a three-phase Integrated-Active-Filter Rectifier (IAFR) front-end coupled with an isolated DC/DC converter. The goal of this study is to assess the performance of the overall system, with a particular emphasis on the IAFR. The IAFR front-end integrates a three-phase synchronous (six-pulse) rectifier, three bidirectional switches, and an injection bridge-leg, enabling efficient AC/DC conversion while drawing sinusoidal current from the grid [13], [14]. To further enhance efficiency, this paper proposes a Triangular-Current-Mode (TCM) operation for the injection leg, enabling Zero-Voltage-

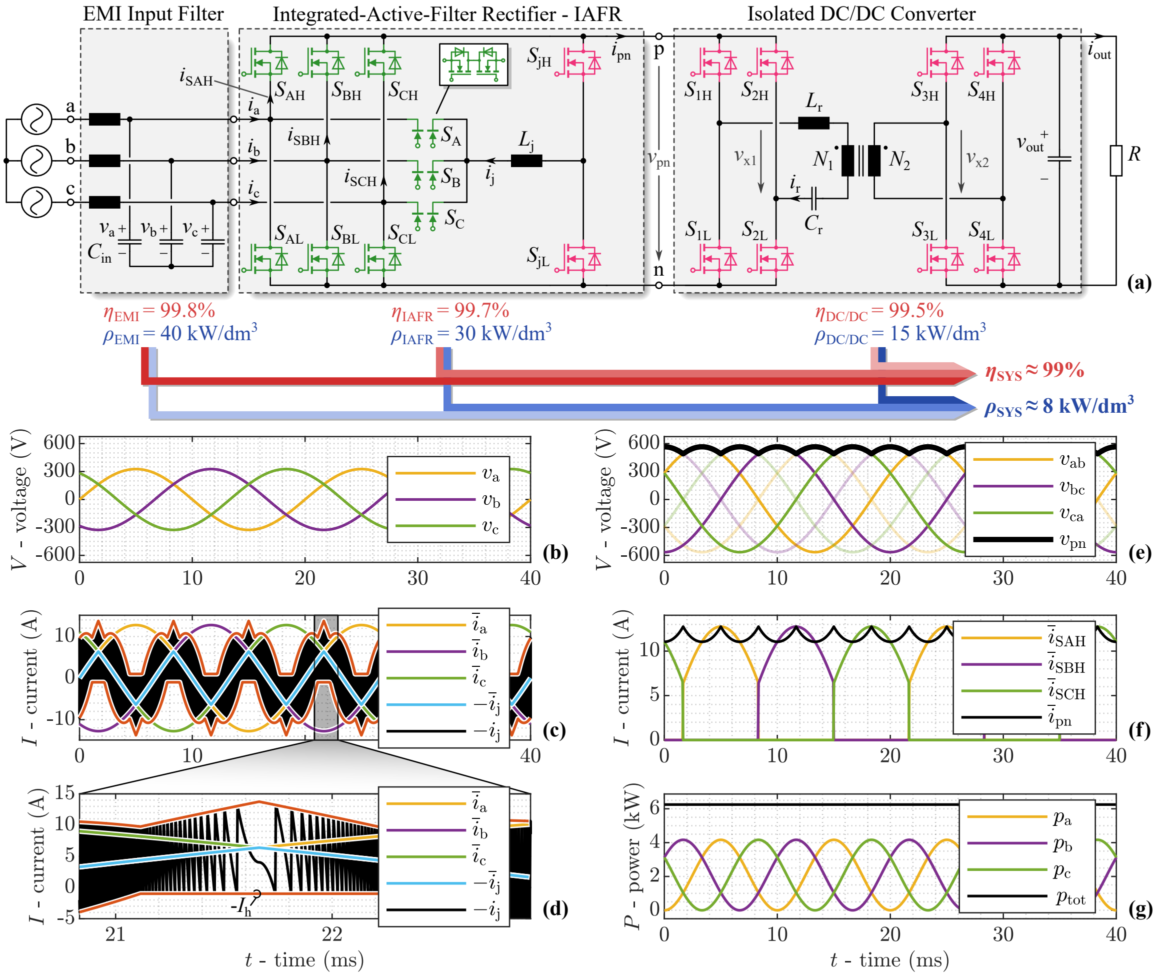

Fig. 2. **(a)** Schematic of a quasi-single-stage converter featuring a bidirectional Integrated-Active-Filter Rectifier (IAFR) for three-phase AC/DC conversion and to draw three-phase sinusoidal mains current. This is paired with an isolated DC/DC back-end stage to ensure galvanic isolation and regulate the output voltage. The transistors are categorized based on their switching frequencies: green indicates transistors with low switching frequencies (multiples of the mains fundamental frequency), while pink indicates transistors operating at high switching frequencies (typically in the range of hundreds of kHz). In **(a)** the arrows report an example of efficiency and power density targets for the different parts of the isolated AC/DC converter. **(b)-(g)** Simulated waveforms of the IAFR under balanced mains conditions, with the injection leg operated in Triangular-Current-Mode (TCM).

Switching (ZVS) and ultimately reducing the volume of the required heatsink. Moreover, the challenge of unbalanced grid operation, which can cause fluctuations in input power, is addressed by a control strategy that mitigates power oscillations, eliminating the need for large energy storage elements, while ensuring sinusoidal input currents even under unbalanced grid conditions [15].

After a detailed analysis of the IAFR operation, this paper defines its performance limits in terms of efficiency and power density through a Multi-Objective Optimization (MOO), which considers a wide range of degrees of freedom. These performance limits provide a guideline for designing the isolated DC/DC converter, specifying its performance requirements to meet the overall system's efficiency and power density targets.

The paper is organized as follows: **Section II** introduces the IAFR operating principle, followed by the TCM modulation in **Section III**, and the control strategy for unbalanced grid in **Section IV**. **Section V** presents the IAFR MOO, with its results in **Section VI**. **Section VII** defines the design guidelines for the DC/DC converter, and **Section VIII** concludes the paper.

II. Operating Principle of the IAFR

Fig. 2a presents a schematic of the IAFR, which integrates a three-phase synchronous (six-pulse) rectifier, three bidirectional/bipolar switches, and an injection bridge-leg to achieve AC/DC conversion while drawing sinusoidal current from the three-phase mains. The output voltage v_{pn} of the rectifier, shown in **Fig. 2e**, exhibits the six-pulse-shaped positive envelope of the mains line-to-line voltages. This voltage is fed to the isolated DC/DC stage, where the current i_{pn} (illustrated in **Fig. 2f**) inversely tracks the rectified voltage, ensuring constant power transfer. The injection leg shapes the three-phase sinusoidal currents by injecting the third harmonic current i_j (shown in **Fig. 2c**) into the phase not connected to nodes p or n, thanks to the bidirectional switches S_A, S_B, and S_C. Finally, **Fig. 2g** shows the power drawn from each phase, p_a, p_b, and p_c, as well as the total input power, $p_{tot} = 6.25\,\mathrm{kW}$.

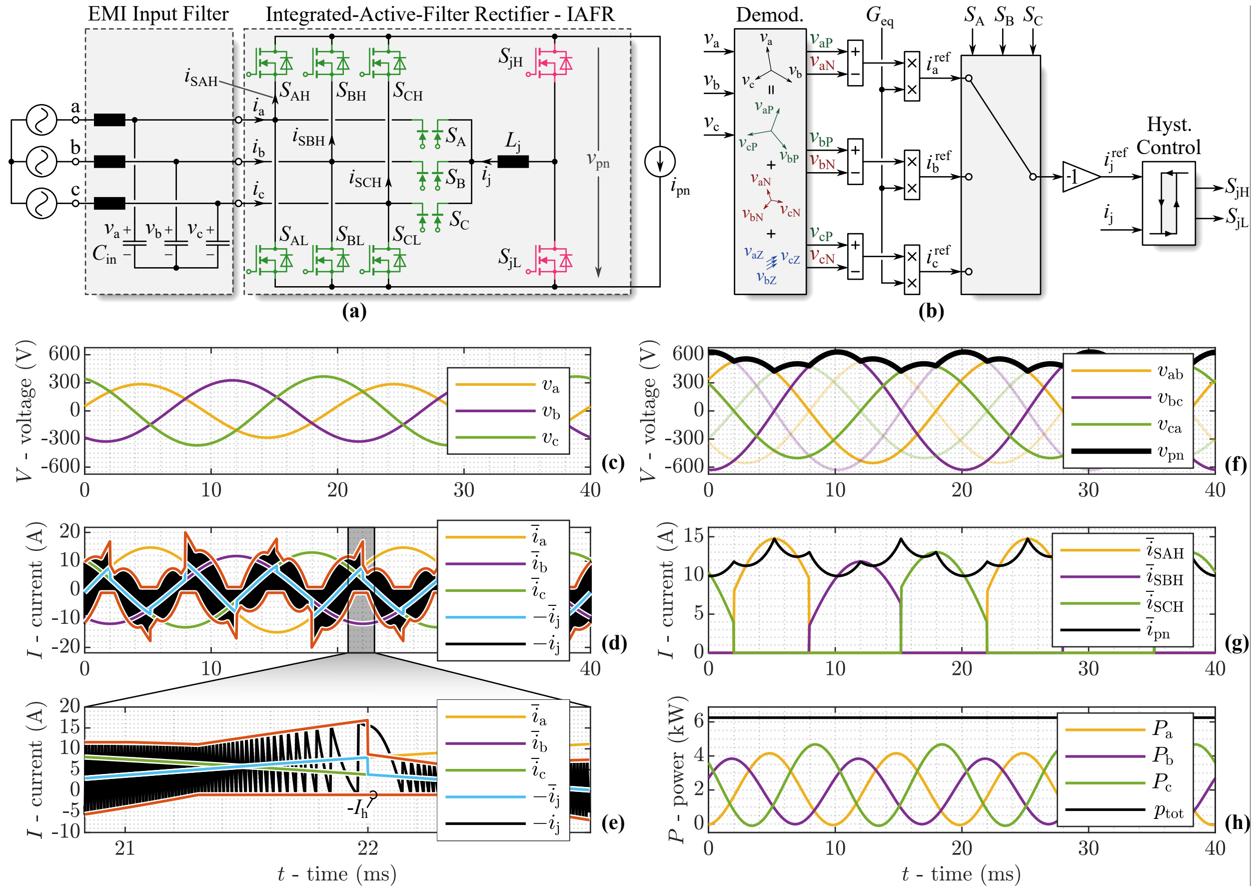

Fig. 3. **(a)** Simplified schematic of the circuit in **Fig. 2a**, where the isolated DC/DC converter is replaced with a constant-power load modeled as a current sink $i_{pn} = P_{out}/v_{pn}$, with P_{out} being the constant output power. **(b)** Control block diagram of the IAFR, designed to maintain constant input power even under unbalanced mains conditions. **(c)-(h)** Simulated waveforms of the IAFR under unbalanced mains operation.

Notably, the injection bridge-leg is the only high-switching-frequency component of the IAFR, while other devices operate at multiples of the mains fundamental frequency, allowing them to be optimized for reduced conduction losses. This separation of switching and conduction losses enables the IAFR to achieve ultra-high efficiency (>99.5%), making it well-suited for the demanding requirements of AI data center applications.

III. Proposed TCM Modulation of the IAFR

Fig. 2d provides a detailed view of the IAFR injection leg operating in Triangular-Current-Mode (TCM). In this mode, the current i_j reverses direction during each switching period, enabling Zero-Voltage-Switching (ZVS) at transistor turn-on. This mechanism minimizes switching losses, improves efficiency, and increases power density by reducing heatsink volume requirements. Looking deeper on the proposed TCM modulation for the IAFR, the current i_j is hysteretically controlled within a dynamically adjusted band. The band threshold values (orange curves in **Fig. 2c** and **Fig. 2d**) are set to ensure that the average current $\bar{i}_j$ tracks the required injection current for the selected phase. Additionally, these thresholds are adjusted to limit the maximum switching frequency of the injection leg, enabling the IAFR to operate in a Bounded TCM (BTCM) mode, balancing efficiency and switching constraints.

IV. Unbalanced Mains Operation of the IAFR

To ensure precise output regulation of the overall system under unbalanced mains conditions, the IAFR must be controlled to draw constant power from the grid. Any fluctuations in input power would lead to significant output voltage oscillations unless large energy storage elements, such as capacitors, are used [16]–[22]. For this reason, the control scheme presented in **Fig. 3b** is employed on the IAFR shown in **Fig. 3a** [15]. The control strategy begins by demodulating the input voltages v_x $(x = a, b, c)$ to extract their positive (v_{xP}) and negative (v_{xN}) sequence components [23]. The reference for the input current i_x is then chosen to eliminate input power fluctuations, resulting in $i_x^{ref} = (v_{xP} - v_{xN})\, G_{eq}$, where G_{eq} is the equivalent input transconductance, calculated from the output power reference of the DC/DC stage [24]–[31]. Finally, the current i_j is controlled to its reference i_j^{ref} (determined by the selected injection phase with S_A, S_B, and S_C) using hysteresis control, where the hysteresis thresholds are dynamically adjusted as described in **Section III** to maintain the desired BTCM operation.

Fig. 3c-h present the simulated waveforms of the IAFR in **Fig. 3a**, operating with the control strategy shown in **Fig. 3b**. As observed in **Fig. 3h**, although the power drawn from each individual phase is unbalanced, the total input power p_{tot} is constant at an average value of $p_{tot} = 6.25\,\mathrm{kW}$, without power oscillations, and sinusoidal phase currents are drawn from the mains. This constant input power eliminates the need for large energy storage elements, minimizing passive components size.

V. Multi-Objective-Optimization Framework

To assess the performance limits of the IAFR in terms of efficiency and power density, a MOO routine is employed to explore a wide range of design parameters and to determine their impact on the IAFR's performance. The implemented MOO routine is better explained using the flowchart in **Fig. 4**, where the systems specifications are also listed.

A. System Model

On the system level, the IAFR has four main degrees of freedom (DOFs): the switching frequency f_{sw}, the inductor current ripple $\Delta i_{L,n}$, the modulation (PWM or BTCM), and the hysteresis current I_h (needed for the BTCM operation detailed in **Fig. 2d**). For a given combination of the system level DOFs, the optimization routine computes the injection inductance L_j to achieve the specified ripple $\Delta i_{L,n}$, and the filter capacitance C_{in} to meet the target capacitor ripple $\Delta v_{C,n}$. Afterwards, the algorithm calculates the idealized electrical waveforms over one fundamental period at the nominal operating point, where the highest component stresses occur. Based on these waveforms, the components' losses and volumes are estimated using suitable component models.

B. Component Models

Transistors: Considering 1200 V off the shelf available devices (Infineon IMCQ120R007M2H / 7.5 mΩ, AIMCQ120R020M1T / 19 mΩ, and AIMCQ120R030M1T / 30 mΩ) the transistors for the synchronous rectifier, the phase selector, and the injection leg are selected separately. The conduction losses are modeled using the temperature-dependent on-resistance, while the switching losses are based on calorimetrically measured data [32]. Different junction temperatures are also considered, as lower temperatures facilitate lower losses but require larger heatsinks.

Heatsink: The thermal interface between transistors and heatsink is modeled with a typical thermal impedance of $0.42\,\mathrm{K\,in^2/W}$, and the heatsink volume is obtained assuming a Cooling-System Performance Index of $CSPI = 15\,\mathrm{W/(dm^3K)}$ [32], and an ambient temperature of $T_a = 40°\mathrm{C}$.

Injection inductor: The design tool from [33] is employed to optimize the inductor by varying the component-level DOFs like core material (N87, Magnetics KoolMμ), core size, winding (solid/litz wire), etc.

Filter capacitors: The capacitors C_{in} are designed for a maximum high-frequency peak-to-peak voltage ripple of 2%, and are found considering typical volumetric energy densities of commercially available film capacitors. Even though the film capacitor losses are very small, they are considered via $\tan\delta = 0.001$. It is worth mentioning that, to reduce the conduction losses in the synchronous rectifier, as well as in the phase-selector, the filter capacitors C_{in} have been moved from the AC-side to the DC-side as described in [14].

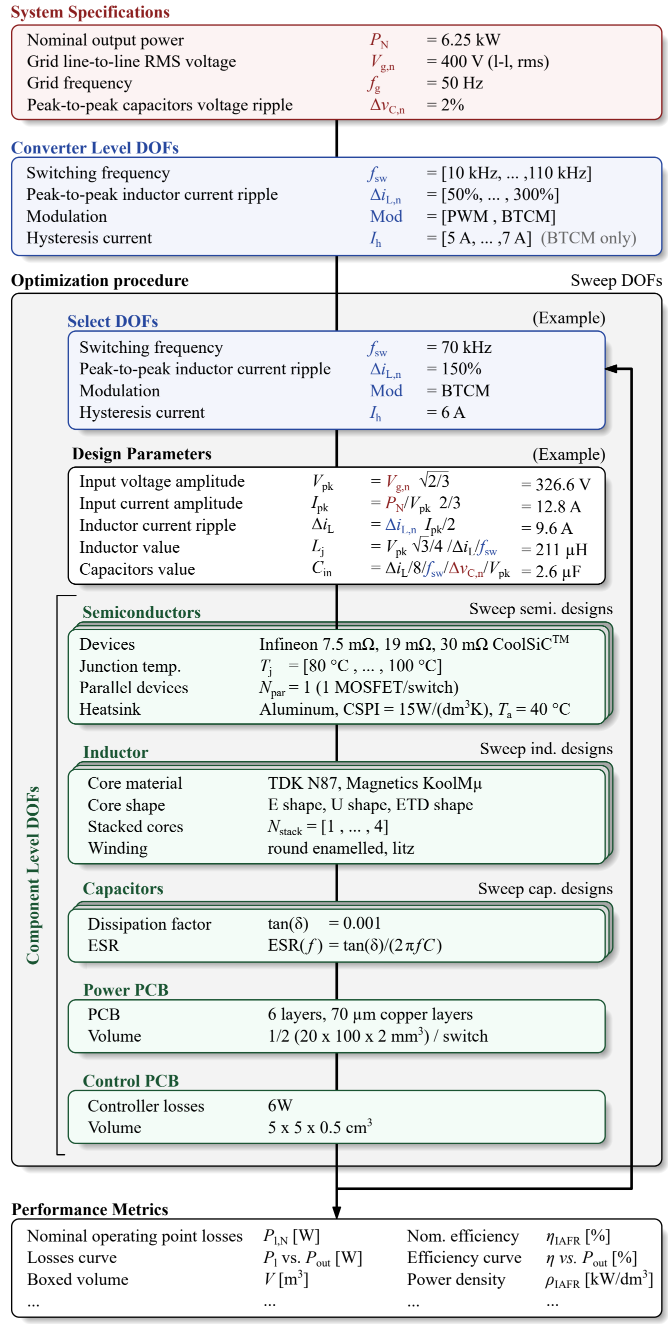

Fig. 4. Flowchart of the Multi-Objective Optimization (MOO) routine implemented in MATLAB for the IAFR optimization.

Power and Control PCBs: The power PCB area/volume depends on the number of power transistors and their package size. On the other hand, the control PCB has a fixed area based on experience, with constant controller losses estimated at 6 W.

C. Performance Evaluation

For a given combination of system-level DOFs (i.e., f_{sw}, Δi_L, modulation, and I_h) the optimization routine recombines all feasible component designs to obtain every possible converter realizations. Afterwards, to derive the efficiency curve (efficiency vs. output power), each converter is evaluated at

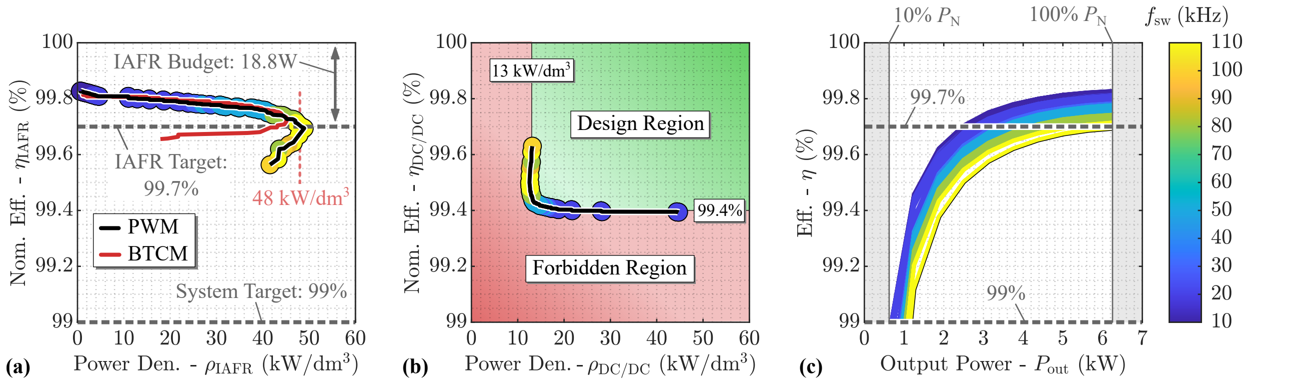

Fig. 5. Multi-Objective Optimization (MOO) results: **(a)** IAFR nominal efficiency vs. power density with color-coded switching frequency f_{sw} of the IAFR; **(b)** Isolated DC/DC converter **required** nominal efficiency vs. power density to achieve the target of η_{SYS} = 99% and ρ_{SYS} = 8kW/dm^3 for the system in **Fig. 2a**, with color-coded switching frequency f_{sw} of the IAFR (the IAFR is operated with PWM); **(c)** efficiency curve of the IAFR operated with PWM.

different output power levels, discarding designs that overstress any component. Finally, performance metrics including nominal efficiency η_{IAFR}, boxed volume V (considering 50% of air between components), power density ρ_{IAFR}, and the efficiency curve η vs. P_{out} are computed.

VI. IAFR Multi-Objective Optimization Results

Fig. 5 presents the optimization results for the 6.25 kW[1] IAFR in **Fig. 2a** composed of the synchronous rectifier (S_{XH}, S_{XL}), the phase selectors (S_X), the injection leg (S_{jH}, S_{jL}), the injection inductance (L_j), the filter capacitors (C_{in}) shifted to the DC-side as described in [14], as well as the power and control PCB. **Fig. 5a** shows the corresponding nominal efficiency vs. power density $\eta_{IAFR} - \rho_{IAFR}$ Pareto front comparing the modulations of the IAFR (PWM and BTCM), as well as the 99.7% IAFR efficiency target (detailed by the arrows in **Fig. 2a**). In the same figure, the color scale represents the switching frequency f_{sw} of the IAFR ranging from 10 kHz (blue) to 110 kHz (yellow). Interestingly, as shown in **Fig.5a**, the IAFR with BTCM achieves only a slightly higher nominal efficiency than PWM, while the latter offers greater power density. This is because, despite the reduced switching losses in BTCM (allowing for a smaller heatsink in the injection leg) it requires larger overall inductors. The reason lies in the higher saturation current required to handle the inductor current peaks that occur specifically under BTCM (see **Fig. 2c-d**). Moreover, the efficiency gap between PWM and BTCM remains minimal, as BTCM operation affects only a limited portion of the grid cycle (see **Fig. 2c-d**).

Afterwards, when considering the full-system in **Fig. 2a**, if the targets of η_{SYS} = 99% [5], [6] and ρ_{SYS} = 8kW/dm^3 of the total system should be reached, the IAFR Pareto front in **Fig. 5a** can be used to define the performance requirements for the remaining system components, i.e., the EMI filter and the isolated DC/DC converter. Assuming an EMI filter efficiency of η_{EMI} = 99.8%, and a power density of ρ_{EMI} = 40kW/dm^3 [34], the corresponding Pareto front for the DC/DC converter can be derived. This front, shown in **Fig. 5b**, defines the nominal efficiency $\eta_{DC/DC}$ and power density $\rho_{DC/DC}$ required by the DC/DC stage to meet the system targets of η_{SYS} = 99% and ρ_{SYS} = 8kW/dm^3 when combined with a specific IAFR realization from **Fig. 5a** (where the PWM Pareto front has been considered). Additionally, this DC/DC converter Pareto front, serves as a design guideline, specifying the DC/DC stage performance constraints and delineating a "forbidden region" where no DC/DC converter realization can achieve the overall system objectives. Considering the IAFR Pareto front in **Fig. 5a** and the previously specified EMI filter (η_{EMI} = 99.8% and ρ_{EMI} = 40kW/dm^3), the forbidden region is colored in red in **Fig. 5b**, and highlights how the full-system targets of η_{SYS} = 99% and ρ_{SYS} = 8kW/dm^3 can be achieved with a DC/DC converter with an efficiency of $\eta_{DC/DC}$ = 99.5% and a power density of $\rho_{DC/DC}$ = 15kW/dm^3.

Finally, **Fig. 5c** shows the efficiency curve η vs. P_{out} for the IAFR operated with PWM (similar curves can be drawn for the IAFR with BTCM). As depicted in such a figure, the IAFR can reach the targeted efficiency of 99.7% when its design switching frequency is lower than 100 kHz, with a corresponding power density (from **Fig. 5a**) of ρ_{IAFR} = 48kW/dm^3.

VII. Isolated DC/DC Converter Discussion

As detailed in **Section VI**, the IAFR optimization results can be used as guidelines for the design of the isolated DC/DC converter. As presented in **Fig. 5b**, this stage must achieve an efficiency of $\eta_{DC/DC}$ = 99.5% and a power density of $\rho_{DC/DC}$ = 15kW/dm^3. Moreover, since the input voltage v_{pn} of the DC/DC converter follows the six-pulse-shaped envelope of the mains line-to-line voltages (see **Fig. 2e**), the converter requires a high regulation bandwidth and fast dynamics to maintain a stable output voltage.

To tackle these challenges the DC/DC stage is implemented with a highly efficient and compact structure, typically an LLC resonant converter, or a Dual-Active-Bridge (DAB) converter [35]. These topologies are strong candidates for the DC/DC stage as they enable to soft-switch all power transistors, reducing switching losses and ultimately increasing efficiency

[1]The power level of 6.25 kW corresponds to a scaled-down version of ¼ of the final system (circuit in **Fig. 2a**), which is expected to operate at 25 kW or higher, with overall dimensions of 104 mm (width) × 40 mm (height) × 710 mm (length), resulting in a target power density of ρ_{SYS} > 8kW/dm^3.

and power density. Additionally, to provide the required output voltage regulation, different modulation schemes are available: the LLC resonant converter is typically operated by adjusting its switching frequency to regulate the output voltage. However this would cause the LLC converter to enter non-optimal operating regions, with increased losses and an overall lower efficiency. For this reason several studies have adopted a Quantum-Series-Resonant Converter (QSRC) operation, enabling the LLC converter to be always operated at its resonance frequency, improving efficiency while maintaining adequate output voltage regulation [36]–[38]. An alternative to the QSRC for ensuring LLC converter operation at its resonance frequency is the Extended Smart-Link (XS-link) concept proposed in [39], where an additional partial power processing converter is placed in series with the LLC stage. This configuration ensures a constant input voltage to the isolated DC/DC converter, allowing it to be optimized for a single input/output voltage transfer ratio and ultimately improving the overall system performance.

On the other hand, DAB converters regulate the output voltage by adjusting the phase-shift between the inverters' voltages, enabling precise control and fast dynamics [35]. The efficiency of the DAB converter can be further improved by using Triple-Phase-Shift (TPS) modulation, with optimally-selected phase-shift and duty cycles [35]. Moreover, in [40], the DAB converter efficiency is increased through a multilevel structure, which reduces the RMS current in the transformer's windings while ensuring precise output voltage regulation.

The above-mentioned solutions provide valuable guidelines for the design of the isolated DC/DC converter, aiming to achieve a target efficiency of $\eta_{\mathrm{DC/DC}} = 99.5\%$ and a power density of $\rho_{\mathrm{DC/DC}} = 15\mathrm{kW/dm^3}$. The referenced studies demonstrate promising performance, with results approaching these targets [37], [40]. By further optimizing the isolated DC/DC converter to meet the specific requirements of the application described in this paper, it is expected that these goals will be successfully achieved in the course of further research, currently being carried out at the University of Padova.

VIII. Conclusions

Next-generation power supply systems for AI-driven data centers requires unparalleled levels of performance in terms of efficiency, power density, and reliability. In this context the AC/DC conversion is set to achieve efficiencies exceeding 99%, power densities greater than $8\mathrm{kW/dm^3}$, galvanic isolation, and reliable operation even under unbalanced grid. To reach these targets, this paper presents a quasi-single-stage solution that combines an Integrated-Active-Filter Rectifier (IAFR), and an isolated DC/DC converter. The first stage (IAFR) provides an ultra-efficient and simple rectification achieved through the low switching frequency of all power semiconductors except for an injection leg needed to sinusoidally shape the three-phase input currents. Afterwards, the isolated DC/DC stage precisely regulates the output voltage and ensures galvanic isolation.

To enhance the IAFR's efficiency, a Bounded Triangular-Current-Mode (BTCM) modulation is introduced, ensuring Zero-Voltage-Switching (ZVS) on the injection leg throughout the entire grid cycle. While BTCM reduces switching losses and allows for a smaller heatsink, this study reveals that those benefits are counter-balanced by the need for a larger inductor due to its required higher saturation current compared to standard relatively low current ripple PWM.

Then, the system's reliable operation under unbalanced grid conditions is addressed through a control strategy that always maintains a constant input power. This approach prevents input power fluctuations and eliminates the need for large energy storage elements, thereby reducing the volume of the required passive components.

Finally, the performance limits of the IAFR, in terms of efficiency and power density, are derived through a multi-objective Pareto optimization which accounts for a wide range of design parameters. The results show IAFR efficiencies exceeding 99.7%, and power densities greater than $30\mathrm{kW/dm^3}$, making the IAFR a strong candidate for the front-end stage in isolated AC/DC converters. Additionally, these findings provide valuable insights for the design of the isolated DC/DC converter, which must achieve an efficiency of 99.5% and a power density of $15\mathrm{kW/dm^3}$, while ensuring precise output voltage regulation and input current shaping when fed with a rectifier three-phase six-pulse voltage.

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