



GENERATION SiC/GaN 3-Φ Variable Speed Drive Systems

Johann W. Kolar et al. Swiss Federal Institute of Technology (ETH) Zurich Power Electronic Systems Laboratory www.pes.ee.ethz.ch

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Source: SIEMENS





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Variable Speed Motor Drive (VSD) Systems

- Industry Automation / Robotics
 Material Machining / Processing Drilling, Milling, etc.
- Compressors / Pumps / Fans
 Transportation
- etc., etc.

.... Everywhere !



• 60...70 % of All Electric Energy Used in Industry Consumed by VSDs







Europe

Variable Speed Drive Concepts

- **DC-Link Based AC/DC/AC OR Matrix-Type AC/AC Converters Battery OR Fuel-Cell Supply OR Common DC-Bus Concepts**



• 45% of World's Electricity Used for Motors in Buildings & Industrial Applications





Europe

State-of-the-Art VSD System

- Standard 2-Level Inverter Large Motor Inductance Allows Low Sw. Frequency
- Shielded Motor Cables / Cable Length Limited / Insulated Bearings / Acoustic Noise







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Surge Voltage Reflections

- "Long Motor" Cable $l_c \ge \frac{1}{2} t_r v$ Short Rise Time of Inverter Output Voltage Impedance Mismatch of Cable & Motor \rightarrow Reflect. @ Motor Terminals / High Insul. Stress



 \rightarrow *dv/dt-Filtering OR Full-Sinewave Filtering / Termination & Matching Networks etc.*







Motor Bearing Currents

- Switching Frequency CM Inverter Output Voltage \rightarrow Motor Shaft Voltage Electrical Discharge in the Bearing ("EDM")



→ Cond. Grease / Ceram. Bearings / Shaft Grndg Brushes / dv/dt-Filter OR Full-Sinewave Filters















Low R_{DS(on)} High-Voltage Devices

- Higher Critical E-Field of SiC \rightarrow Thinner Drift Layer Higher Maximum Junction Temperature $T_{j,max}$



• Massive Reduction of Relative On-Resistance \rightarrow High Blocking Voltage Unipolar (!) Devices







Si vs. SiC

- Si-IGBT / Diode → Const. On-State Voltage, Turn-Off Tail Current & Diode Reverse Recovery Current
- SiC-MOŚFET \rightarrow Loss Reduction @ Part Load BUT Higher R_{th}



• Space Saving of >30% on Module Level (!)







Si vs. SiC Conduction Behavior

Si-IGBT → Const. On-State Voltage Drop / Rel. Low Switching Speed
 SiC-MOSFETs → Resistive On-State Behavior / Factor 10 Higher Sw. Speed



• SiC MOSFETS Facilitate Higher Part Load Efficiency







Si vs. SiC Switching Behavior

Si-IGBT → Const. On-State Voltage Drop / Rel. Low Switching Speed
 SiC-MOSFETs → Resistive On-State Behavior / Factor 10 Higher Sw. Speed



High di/dt & dv/dt \rightarrow Challenges in Packaging / EMI / Motor Insulation / Bearing Currents

















Circuit Parasitics

High di/dt

Commutation Loop Inductance L_s Allowed L_s Directly Related to Switching Time $t_s \rightarrow$





Advanced Packaging & Parallel **Interleaving** for Partitioning of Large Currents (Z-Matching)







Si vs. SiC EMI Emissions

- Higher dv/dt → Factor 1 Higher Switching Frequencies → Factor 1 EMI Envelope Shifted to Higher Frequencies \rightarrow Factor 10
- \rightarrow Factor 10



• Higher Influence of Filter Component Parasitics & Couplings \rightarrow Advanced Design





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Inverter Output Filters

dv/dt-Filters – Full-Sinewave Filters











—— dv/dt-Limitation ——







Passive | Hybrid | Active dv/dt-Limitation

- **Passive** Damped LC-Filter $f_c > f_s$ **Hybrid** Undamped LC-Filter & Multi-Step Sw. Transition **Active** Gate-Drive Based Shaping of Sw. Transients



• Connection to DC-Minus & CM Inductor \rightarrow Limit CM Curr. Spikes / EMI / Bearing Currents







Comparison of dv/dt-Filtering Techniques









Multi-Bridge-Leg dv/dt-Limitation

2-Step Switching / Resonant Transition (cf. Active dv/dt-Filter)



Source: J. Ertl et al. PCIM Europe 2018

 $V_{\rm DC}$

DC

■ Staggered Sw. Parallel Bridge-Legs → Non-Resonant Multi-Step Transition



Source: J. Ertl et al. PCIM Europe 2017

• Adv. for High Power / High Output Curr. Syst. Employing Parallel Bridge-Legs & Local Comm. Caps







Aux. Resonant Commutated Pole

- dv/dt-Limitation & Sw. Loss Red. w/ Snubber Cap. & Aux. Switches → 1 ... 1.5kV/us
 Opt. Timing of Aux. & Main Switches → Pre-FlexTM Self-Learning AI Algorithm
 Concept Proposed for BJTs by M. Lockwood & A. Fox @ IPEC 1983 (!)





Green: Lr Resonant inductor current (varies with load)

Purple: S2 Vds switch voltage (600V-0V)

Yellow: Aux + Lr ARCP and inductor voltage (-300V to +300V)

Blue: Load current varies 0-160A

- Complicated Implementation / Critical Timing for $f_{sw} > 100 \, kHz$ 99.5% Half-Load | 99.35% Full-Load Eff. @ 100 kW, 800 V_{DC}, f_{sw} = 50 kHz (1200 V/12 m Ω SiC MOSFETs)









Inverter Systems w/ Sinusoidal Output Voltages —







Inverter Sinewave Output Filter

- Measures Ensuring Longevity of Motor Insulation & Bearings / EMI Compliance
 DM-Sinus Filter OR DM & CM Full-Sinewave Filter











—— Triangular Current Mode (TCM) —— ZVS Operation





Full-Sinewave Filter & ZVS Operation

- Purely Sinusoidal Output Voltage (DM & CM Filtering) High Sw. Frequency & TCM \rightarrow Low Filter Inductor Volume
- ZVS of Inverter Bridge-Legs



- Only 33% Increase of Transistor Conduction Losses Compared to CCM (!)
- Very Wide Switching Frequency Variation







()

Frequency-Bounded TCM \rightarrow B-TCM

• Very Wide Switching Frequency Variation of TCM \rightarrow B-TCM



• $TCM \rightarrow B$ -TCM - 10% Further Increase of Transistor Conduction Losses









Continuous Current Mode (CCM) Operation ——







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$3-\Phi$ 650V GaN Inverter System (1)

Source: YASKAWA

- Transphorm 650V Normally-On GaN HEMT/30V Si-MOSFET Cascode 6-in-1 Power Module
 Sinewave LC Output Filter Corner Frequency f_c= 34 kHz (f_{sw}= 100 kHz)
- No Freewheeling Diodes



\rightarrow Comparison to Si-IGBT Drive Systems





$3-\Phi$ 650V GaN Inverter System (2)

Source: YASKAWA

Comparison of GaN Inverter w/ LC-Filter to Si-IGBT System (No Filter, f_{sw}=15kHz)
 Measurement of Inverter Stage & Overall Drive Losses @ 60Hz



 \rightarrow 2% Higher Efficiency of GaN System Despite LC-Filter (Saving in Motor Losses) !









Multi-Level / Multi-Cell Converters & Modularity







3-Level T-Type Inverter (1)

- *Higher Number of Bridge-Leg Output Voltage Levels / Lower DM & CM Voltage Steps Neutral Point Clamped* | *Flying Capacitor* | *T-Type Bridge-Leg Topologies*









3-Level Bridge-Leg

- More Complicated Bridge-Leg Structure
- **On-State-Losses of Series-Connected Switches**







3-Level T-Type Inverter (2)

- 3-Level T-Type Inverter 3-Level Phase Voltage / 5-Level Line-to-Line Voltage Lower DM & CM Voltage Steps Compared to 2-Level Converter



- *Full-Sinewave DC-Link Referenced LC-Filter Elimination of DM & CM Sw. Frequ. Voltage Harmonics T-Type Topology Ensures Low Conduction Losses Adv. Application of M-BDSs (!)*







3-Level T-Type Inverter (3)

- 3-Level T-Type Inverter 3-Level Phase Voltage / 5-Level Line-to-Line Voltage Lower DM & CM Voltage Steps Compared to 2-Level Converter



- **Full-Sinewave DC-Link Referenced LC-Filter** Elimination of DM & CM Sw. Frequ. Voltage Harmonics T-Type Topology Ensures Low Conduction Losses Adv. Application of M-BDSs (!)





SiC/GaN Figure-of-Merit

- Figure-of-Merit (FOM) Quantifies Conduction & Switching Properties
- FOM Identifies Max. Achievable Efficiency @ Given Sw. Frequ.



- Advantage of LV over HV Power Semiconductors \rightarrow Advantage of Multi-Level over 2-Level Converter Topologies







3-Level Flying Capacitor (FC) Converter

3-Level Flying Cap. (FC) Converter \rightarrow No Connection to DC-Midpoint Involves All Switches in Voltage Generation \rightarrow Eff. Doubles Device Sw. Frequency



FC Voltage Balancing Possible also for DC Output







4.8MHz GaN Half-Bridge Phase Module

- Combination of Series & Parallel Interleaving
- 600V GaN Power Semiconductors, f_{sw} = 800 kHz Volume of ~180 cm³ (incl. Control etc.) H₂O Cooling Through Baseplate



• Operation @ f_{out} = 100 kHz / $f_{sw,eff}$ = 4.8 MHz, 10 kW, U_{dc} = 800 V








_ Motor-Integrated Inverter Systems









Stacked-Multi-Cell (SMC) Inverter

- Fault-Tolerant VSD
- **Low-Voltage Inverter Modules**
- Very-High Efficiency / Power Density
- Automated Manufacturing
- Rated Power
 DC-Link Voltage
 45kW / f_{out} = 2kHz
 1kV





• Smart Motor / All-in-One / Plug & Play | Connected / Intelligent VSD 4.0



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Motor-Integrated SMC-Inverter

Rated Power
DC-Link Voltage
3-\$\Phi\$ Power Cells
Outer Diameter
9kW @ 3700rpm
650...720V
5+1
220mm



- Axial Stator Mount
- 200V GaN e-FETs
- Low-Capacitance DC-Links
- 45 mm x 58 mm / Cell

• Main Challenge — Thermal Coupling OR Thermal Decoupling of Motor & Inverter

Motivation

- General / Wide Applicability
- Adaption to Load-Dependent Battery | Fuel Cell Supply Voltage
 Operation in Wide Output Voltage / Wide Motor Speed Range

- Full-Sinewave Filtered Motor Supply Voltage
- LC Output Filter Inductor Advantageously Utilized as Buck-Boost-Inductor

Buck-Boost «Y–Inverter»

Generation of AC-Voltages Using Unipolar Bridge-Legs

- Switch-Mode Operation of Buck OR Boost Stage → Quasi Single-Stage Energy Conversion (!)
 3-Φ Continuous Sinusoidal Output / Low EMI → No Shielded Cables / No Motor Insul. Stress

3-Φ Current Source Inverter (CSI) Topology

Y-Inverter \rightarrow **Phase Modules** w/ Buck-Stage | Current Link | Boost-Stage 3- ϕ CSI \rightarrow Buck-Stage V \rightarrow I Converter | Current DC-Link DC/AC-Stage

- Single Inductive Component
- Positive DC-Side Voltage for Both Directions of Power Flow \rightarrow Future Utilization of M-BDSs

3-Ф Buck-Boost CSI (1)

■ Monolithic Bidir. Bipolar GaN Switches Featuring 2 Gates → Full Controllability

Buck-Stage for Impressing Const. DC Current / PWM of CSI for Output Voltage Control

• Conventional Control of Inverter Stage \rightarrow Switching of All 3 Phase Legs (3/3)

3-Ф Buck-Boost CSI (2)

- Monolithic Bidir. Bipolar GaN Switches Featuring 2 Gates → Full Controllability
- Buck-Stage for Impressing Const. DC Current / PWM of CSI for Output Voltage Control

• Conventional Control of Inverter Stage \rightarrow Rel. High CSI-Stage Sw. Losses

3-Ф Buck-Boost CSI (3)

- "Synergetic" Control of Buck-Stage & CSI Stage 6-Pulse-Shaping of DC Current by Buck-Stage \rightarrow Allows Clamping of One CSI-Phase

• Switching of Only 2 of 3 Phase Legs (2/3 Mode) \rightarrow Significant Reduction of Sw. Losses

3-Ф Buck-Boost CSI (4)

- "Synergetic" Control of Buck-Stage & CSI Stage 6-Pulse-Shaping of DC Current by Buck-Stage \rightarrow Allows Clamping of One CSI-Phase

• Switching of Only 2 of 3 Phase Legs \rightarrow Significant Red. of Sw. Losses (\approx -86% for R-Load)

Current Source Buck-Boost Rectifier

- Derivation Based on Bidir. Buck-Boost Current Source Inverter (CSI) \rightarrow Buck-Boost PFC Rectifier
- **Lower # of Ind. Components Compared to Boost-Buck Rectifier Approach**

- AC/DC Buck Stage Distributes DC-Link Current to Mains Phases Sinusoidal Inp. Current
- Synergetic Control/Modulation of Rectifier Stage & DC/DC Stage for Min. Sw. Losses

3-Φ Current DC-Link AC/AC Converter

DC-Side Coupling of Buck-Boost Current DC-Link PFC Rectifier & Inverter — AC/DC/AC

Full-Sinewave Filtering @ Input & Output w/ Single Magnetic Component

- Bipolar Blocking / Unidir. Switches | Unidir. DC-Link Current Sufficient for Bidir. Power Conversion
- Modulation-Based Inversion of DC-Link Voltage Polarity \rightarrow Inv. of Power Flow Direction

Remark 3-O Current DC-Link AC/AC Converter Sinusoidal Motor Voltage Achieved w/ Single Ind. Component Unidir. Valves Sufficient for Bidir. Power Conversion M-BDSs — Synchronous Rectification $L_{\rm CM}$ ⊶<mark>ٻ</mark> normally on ¥ ¥ А B h **↔**⊢

• Relation to High-Power Thyristor-Based Medium-Voltage Synchr. Machine Variable Speed Drives

Remark Self Reverse-Blocking M-BDS-Concept (1)

- **Bidir.** Curr. DC-Link Converters Unidir. I_{dc} & Bipolar U_{dc} OR **Bidir.** I_{dc} & Unipolar U_{dc}
- HV Switch + HV Diode
 M-BDS

• "Self-Switching"

HV Diode Characteristic / High Cond. Losses Ohmic Cond. Char. BUT 2 External Gate Signals / 2 Gate Drivers Ohmic Cond. Char. BUT High Local Complexity (Sensing)

SRB-MBDS Quasi-Ohmic Cond. Char. (Cascode w/ LV Si Schottky Diode) & 1 External Gate

Remark Self Reverse-Blocking M-BDS-Concept (2)

- Bidir. Curr. DC-Link Converters Unidir. I_{dc} & Bipolar U_{dc} OR Bidir. I_{dc} & Unipolar U_{dc}
- HV Switch + HV Diode M-BDS
- "Self-Switching"

HV Diode Characteristic / High Cond. Losses Ohmic Cond. Char. BUT 2 External Gate Signals / 2 Gate Drivers Ohmic Cond. Char. BUT High Local Complexity (Sensing)

SRB-MBDS Quasi-Ohmic Cond. Char. (Cascode w/ LV Si Schottky Diode) & 1 External Gate

DUA ITY(

Buck-Boost

Boost-Buck

DUA

- Current DC-Link Topology
- Application of M-BDSs
- Complex 4-Step Commutation OR SRB-MBDSs Low Filter Volume

- Challenging Overvoltage Protection
- Limited Control Dynamics

- **Standard Bridge-Legs**
- Low-Complexity Commutation
- Defined Semiconductor Voltage Stress
- Facilitates DC-Link Energy Storage

High Input / Output Filter Volume

DUA

- Current DC-Link Topology
- Application of M-BDSs
- Complex 4-Step Commutation Low Filter Volume

- Voltage DC-Link Topology
- **Standard Bridge-Legs**
- Low-Complexity Commutation Defined Semiconductor Voltage Stress
- Facilitates DC-Link Energy Storage

■ All-600V-GaN AC-AC VSDs / 1.4 kW, 200V L-L / Full EMI Filter (Grid & Motor) / 97% Nominal Eff.

$3-\Phi AC/AC$ Matrix Converter $\begin{cases} 100 \\ 000 \\ 011 \end{cases}$

Indirect & *Direct* 3- Φ AC/AC Matrix Converter

- Constant 3-Φ Instantaneous Power Flow → No Low-Frequ. DC-Link Power Pulsation Buffer Requirement (!)
 Indirect AC/DC—DC/AC OR Direct AC/AC Power Conversion → IMC OR DMC
 DMC → Switch Matrix w/ Bipolar Voltage Blocking & Current Carrying Devices

• Input-Side Cap. / Output-Side Motor Ind. \rightarrow Operation Limited to Buck-Type (Step-Down) Conversion

Indirect & *Direct* 3- Φ AC/AC Matrix Converter

Input Filter Capacitors | Sw. Stage | Motor Inductance
 Buck-Type Power Conversion Topology

pO *b* c c -0Cn

- IMC Relies on Strictly Pos. DC-Link Voltage / i=0 Input Stage Commutation
 M-BDS-Based Realization of DMC Features Lower # of Switches / 4-Step Commutation

4-Step Commutation of DMC

- No Mains Short Circuit
- No Load Current Interruption

Assumption $u_{ab} < 0$

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4-Step Commutation of DMC (1)

- No Mains Short Circuit
- No Load Current Interruption

Assumption $u_{ab} < 0$

4-Step Commutation of DMC (2)

- No Mains Short Circuit
- No Load Current Interruption

Assumption $u_{ab} < 0$

4-Step Commutation of DMC (3)

- No Mains Short Circuit
- No Load Current Interruption

Assumption $u_{ab} < 0$

4-Step Commutation of DMC (4)

- No Mains Short Circuit
- No Load Current Interruption

Assumption $u_{ab} < 0$

U1 600V 11 E 100A Sync Stc:11

12 E 100A Syme Src=11

600V 13 E 100A Sync Srct 10

ΣB(3V3A)

U4 600V 14 E 100A Sync Src: E0

05 600V 15 E 100A Sync Src: 10

U6 600V 16 E 100A Syne Src:E0

Industry Application of 3- Φ Matrix Converter

- **Fully Regenerative** \rightarrow e.g. Downhill Conveyor etc.
- Higher Power Density Compared to Voltage DC-Link System / No Front-End Boost Inductors
- Quasi Three-Level Output Characteristic
- No-Switching / Eco Operation for f₂ = f_{Mains}

Challenging Overvoltage Protection Limited Output Voltage Range (!)

Close to Unity Power Factor

WiPDA Europe

3- Φ **AC/AC** *Matrix* **Converter Comparison**

- Indirect Matrix Converter (IMC)
- GaN M-BDS AC/DC Front-End
- *ZCS Commutation of AC/DC Stage @ i_{DC}=0 No 4-Step Commutation*

- **Direct** Matrix Converter (CMC)
- 4-Step Commutation
- Exclusive Use of GaN M-BDSs

- Higher # of Switches Compared to DMC
- Lower Cond. Losses @ Low Output Voltage Thermally Critical @ $f_{out} \rightarrow 0$

• Thermally Critical @ $f_{out} \approx f_{in}$

3-Φ Current DC-Link vs. Matrix AC/AC Converter

- Current DC-Link Topology
- Application of M-BDSs | 12 Switches
- 4-Step Commutation
- Buck-Boost Functionality
- Low Filter Volume

• Challenging Overvoltage Protection

- Direct Matrix Converter
- Application of M-BDSs | 9 Switches
- 4-Step Commutation
- Complex Space Vector Modulation
- Limited to Buck-Operation (!)

• Challenging Overvoltage Protection

Monolithic 3D-Integration

Source: Panasonic ISSCC 2014

Isolated

dividing

DBM gate drive

transmitter chip

- M-BDS GaN 3x3 Matrix Converter with Drive-By-Microwave (DBM) Technology

- 9 Dual-Gate GaN AC-Switches / 4-Step Commutation DBM Gate Drive Transmitter Chip & Isolating Couplers Ultra Compact $\rightarrow 25 \times 18 \text{ mm}^2$ (600V, 10A 5kW Motor) -

Massive Space Saving Compared to Discrete Realization (!)

- Slowing Transistor Node Scaling → Vertical & Heterogeneous Integr. of ICs for Performance Gains Extreme 3D-Integrated Cube-Sized Compute Nodes Dual Side & Interlayer Microchannel Cooling

• Interposer Supporting Optical Signaling / Volumetric Heat Removal / Power Conversion

Thank you!

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Authors

Johann W. Kolar (M'89–F'10) is a Fellow of the IEEE, an International Member of the US NAE and a Full Professor and Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich. He has proposed numerous novel converter concepts incl. the Vienna Rectifier, has spearheaded the development of x-million rpm motors and has pioneered fully automated multi-objective power electronics design procedures. He has graduated 95 Ph.D. students, has published 1000+ research papers, 4 book chapters, and has filed 200+ patents. He has served as IEEE PELS Distinguished Lecturer from 2012 - 2016. He has received 45+ IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Power Electronics Society R. David Middlebrook Achievement Award, the 2016 IEEE PEMC Council Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2021 EPE Outstanding Achievement Award and 2 ETH Zurich Golden Owl Awards for excellence in teaching. The focus of his current research is on ultra-compact/efficient WBG PFC rectifier and inverter systems, ultra-high BW switch-mode power amplifiers, multi-port converters, Solid-State Transformers, multi-functional actuators, ultra-high speed / motor-integrated drives, bearingless motors, ANN-based multi-objective design optimization and Life Cycle Assessment of power electronics systems.

Jonas Huber (S'11-M'16-SM'22) received the MSc (with distinction) degree and the PhD degree from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2012 and 2016, respectively. Since 2012, he has been with the Power Electronic Systems Laboratory, ETH Zurich and became a Post-Doctoral Fellow, focusing his research interests on the field of solid-state transformers, specifically on the analysis, optimization, and design of high-power multi-cell converter systems, reliability considerations, control strategies, and applicability aspects. From 2017, he was with ABB Switzerland Ltd. as an R&D Engineer designing high-power DC-DC converter systems for traction applications, and later with a Swiss utility company as a Business Development Manager. He then returned to the Power Electronic Systems Laboratory as a Senior Researcher in 2020, extending his research scope to all types of WBG-semiconductor-based ultra-compact, ultra-efficient or highly dynamic converter systems.

• Contact Information

kolar@lem.ee.ethz.ch | huber@lem.ee.ethz.ch

