Comparison of Not Synchronized Sawtooth Carrier and Synchronized Triangular Carrier Phase Current Control for the VIENNA Rectifier I

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Abstract. Integrated control circuits being available for input current control of single-phase power factor correctors are frequently applied also for realizing a simple current control for each phase of a three-phase PWM rectifier system. There, the input currents are controlled independently although the three phases are mutually coupled, i.e., the sum of the phase currents is forced to zero for missing connection between the mains star point and the output voltage center point. However, ignoring of the coupling of the three phases results in increased amplitudes of harmonics with switching frequency and/or in a significantly higher ripple of the rectifier input current. This is shown in this paper by a detailed analysis of different current control concepts for a three-phase three-switch three-level boost-type PWM rectifier (VIENNA Rectifier I) with unity power factor. The theoretical considerations are verified by digital simulations and an experimental analysis of a laboratory prototype and are valid in general for three-phase boost-type voltage DC link PWM rectifier systems.

1 Introduction

Integrated control circuits being available for input current control of single-phase unity power factor PWM rectifiers [1] are frequently applied also for realizing a simple current control for each phase of a three-phase PWM rectifier system [2]. There, the input currents of the three-phase rectifier are controlled independently although the three phases are mutually coupled, i.e., the sum of the phase currents is forced to zero for missing connection between the mains star point and the output voltage center point. Therefore, as shown in the following there result increased amplitudes of harmonics with switching frequency and/or a significantly higher ripple of the rectifier input current. There, different ramp comparison current control concepts employing independent sawtooth-shaped and triangular-shaped carrier signals for each phase current control are considered in comparison to synchronized triangular-shaped phase carrier signals. The results of this investigation are valid in general for three-phase PWM rectifier systems, but here the detailed analysis is concentrated on a three-phase three-switch three-level boost-type PWM rectifier known as VIENNA Rectifier I [3]. In **section 2** the basic principle of operation of the VIENNA Rectifier I is described briefly, and the phase current control realized as a ramp comparison current control [4] is discussed in detail. In **section 3** a simple current control of each phase of the three-phase rectifier applying integrated single-phase control circuits with independent, i.e., not synchronized sawtooth-shaped carrier signals is analyzed theoretically. It is shown that by synchronizing the individual carrier signals the ripple of the mains phase current can be reduced significantly. Using triangular-shaped carrier signals instead of sawtooth-shaped signals results in a further reduction of the amplitudes of harmonics with switching frequency of the rectifier input current. **Section 4** gives results of a digital simulation and a comparative evaluation of the different current control concepts described in section 3. There, the harmonics rms value and the amplitudes of the harmonics of the rectifier input current serve as evaluation criterion and the comparison is on the basis of equal switching losses. Finally, in **section 5** the theoretical considerations are verified by measurements on a 10kW-laboratory prototype of the VIENNA Rectifier I.

2 VIENNA Rectifier I, Mains Current Control

2.1 Basic Considerations

The VIENNA Rectifier I, a three-phase three-switch three-level boost-type unity power factor PWM rectifier, is characterized by

- sinusoidal current consumption
- ohmic mains behaviour, unity power factor operation
- controlled output voltage
- low circuit complexity
- high power density and
- high efficiency ($\approx$ 97% at reated power).

The advantages of this system as compared to other three-phase rectifier concepts with sinusoidal input currents (e.g., the three-phase six-switch two-level converter) are especially

- a low number of power transistors
- a lower distortion of the input currents because of the three-level characteristic and
- a lower blocking voltage stress (determined by only half the output voltage) on all output semiconductors if switching transients are neglected.

Because of the three-level charactersitic three different voltages ($+\frac{U_z}{2}, 0, -\frac{U_z}{2}$) are avaliable at the rectifier input for mains phase current control which results in a low ripple and low harmonics of the input current. Low effects on the

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mains can therefore be achieved using much smaller inductors than required for a two-level converter of equal switching losses. Another distinctive advantage of the three-level structure is the reduction of the blocking voltage stress on the power semiconductors to (ideally) 50% of the DC output voltage U_Z. Since the switching losses are in good approximation proportional to the blocking stress, in a first approximation the switching frequency can be doubled as compared to a two-level system without increasing the losses. E.g., for operating the VIENNA Rectifier I in the European low voltage mains (400 V_{rms} line-to-line rms) it is possible to use power MOSFETs with a blocking capability of $U_{DSS} = 500V$ with low on-resistance and low conduction losses for realizing the power transistors. The above described advantages result in an extremely low volume and/or high power density (W/dm^3) of the VIENNA Rectifier I.

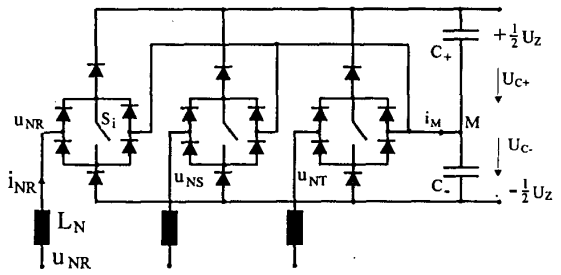

Fig.1: Structure of the power circuit of the VIENNA Rectifier I.

The analysis of the current flow in the power circuit in dependency on the switching state clearly shows the basic principle of operation of the VIENNA Rectifier I. The input current of each phase is defined by the voltage applied across the corresponding inductor L_N on the mains side (Eq.(1)). A recifier input voltage $u_{U,i}$ is determined by the switching state of the power transistor S_i and by the sign on $i_{N,i}$. **Figure 2** shows the conduction states of the power circuit for the switching states (100), (000), (010) and (011) in the interval $i_{N,R} > 0, i_{N,S} < 0, i_{N,T} < 0$. As explained in section 2.4 the other possible switching states (001), (101), (110) and (111) are not applied in this interval for using ramp comparison current control and, therefore, are not shown in Fig.2.

Positive current $i_{N,R} > 0$ flows through the positive freewheeling diode if the switch of phase R is off ($s_R = 0$). If the power transistor S_R is on ($s_R = 1$) the positive input current $i_{N,R}$ being impressed by the input inductor $L_{N,R}$ flows through the power transistor S_R into the neutral point and/or capacitive output voltage center point M of the converter. In case of $s_R = 1$ the potential $u_{U,R}$ (referred to M) is lower by $\frac{U_Z}{2}$ as compared to $s_R = 0$ (cf. switching states (011) and (100)). Therefore, because of $u_{L,R} = u_{N,R} - u_{U,R} = L_N \frac{di_{N,R}}{dt} > 0$ for $s_R = 1$ the absolute value of $i_{N,R}$ will increase; correspondingly, for $s_R = 0$ the absolute value of $i_{N,R}$ will decrease ($u_{L,R} = u_{N,R} - u_{U,R} = L_N \frac{di_{N,R}}{dt} < 0$) if a sufficiently high output voltage value U_Z is assumed.

In case of negative phase currents the situation is different as shown for the phases S and T in Fig.2 ($i_{N,S}, i_{N,T} < 0$). If power transistor S_S is on ($s_S = 1$) the input current $i_{N,S}$ flows into the neutral point M, i.e., we have $u_{U,S} = 0$. If the switch S_S is off ($s_S = 0$) the current flow $i_{N,S}$ is through the negative free-wheeling diode and via the negative bus of the recifier output voltage which results in a negative rectifier input voltage $u_{U,S} = -\frac{U_Z}{2}$. According to to $u_{L,S} = u_{N,S} - u_{U,S} = L_N \frac{di_{N,S}}{dt} > 0$, therefore, the absolute value of the negative input current $i_{N,S}$ will decrease. For increasing the absolute value of $i_{N,S}$ and/or makeing $i_{N,S}$ more negative the power switch S_S, therefore, has to be on ($s_S = 1$), as opposed to the case of positive phase current where turning on the switch results in increasing phase current.

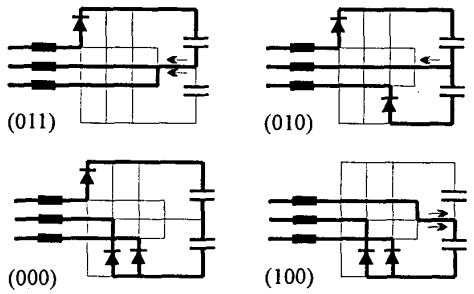

Fig.2: Conduction states for system switching states (011), (010), (000), (100) under the assumption of $i_{N,R} > 0, i_{N,S} < 0, i_{N,T} < 0$ (being valid within a $\frac{\pi}{3}$-wide interval of the mains period).

In summary, the time-behavior of each input phase current $i_{N,i}$ can be determined by the state of the corresponding switch S_i and it, therefore, is possible to achieve a sinusoidal mains current shape being distorted only by a small current errror $\Delta i_{N,i}$ according to the harmonics of $u_{U,i}$ with switching frequency. Because of the current dependency of the voltage formation the sign of the phase currents has to be considered for controlling the power transistors S_i.

Due to the phase-symmetry of the system topology and the symmetries of an ideal three-phase voltage/current system the discussion, however, can be limited to a $\frac{\pi}{3}$-wide interval and/or to a single set of signs of the mains currents. Therefore, all considerartions will be based on $i_{N,R} > 0, i_{N,S} < 0, i_{N,T} < 0$ (cf. Fig.2) in the following.

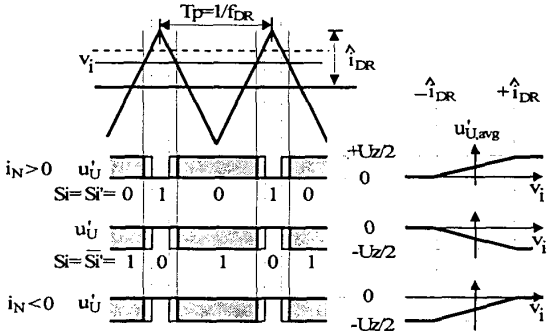

Fig.3: Generation and inversion of the switching function in case of negative input phase current $i_{N,i} < 0$ and dependency of the average rectifier input voltage $u'_{U,i}$ on the pre-control signal v_i.

Because of the dependency of the system behaviour on the signs of the mains phase currents a phase switching state s_i as generated by a conventional current control scheme has to be inverted for negative sign of the corresponding phase current. This can be explained for a ramp comparison phase current control by **Fig.3**. As shown at the left hand side of Fig.3 the intersections of a pre-control signal v_i (section 2.3) with the (here) triangular carrier signal define the swithing state $s_i = s_i'$ of the power transistor S_i. In case of $i_{N,i} > 0$ the rectifier input voltage $u_{U,i}$ is switched between $u_{U,i} = 0$ ($s_i = s_i' = 1$) and $u_{U,i} = +\frac{U_Z}{2}$ ($s_i = s_i' = 0$). The dependency of the local average value $u_{U,i,avg}$ (related to a pulse period) of $u_{U,i}$ is shown on the right hand side of Fig.3. In case of $i_{N,i} < 0$ the rectifier input voltage $u_{U,i}$ is switched between $u_{U,i} = 0$ ($s_i = s_i' = 1$) and $u_{U,i} = -\frac{U_Z}{2}$ ($s_i = s_i' = 0$). According to the characteristic $u_{U,i,avg} = u_{U,i,avg}\{v_i\}$ shown on the right hand side of Fig.3 an increase of v_i results in a decrease of $u_{U,i,avg}$ which is contrary to the behavior required for proper current control. Therefore, in the case of negative current $i_{N,i} < 0$ the output s_i of the corresponding phase current controller has to be inverted ($s_i = \overline{s_i'}$) as shown at the bottom of Fig.3, left hand side. This results in an inversion of the slope of the characteristic $u_{U,i,avg} = u_{U,i,avg}\{v_i\}$ (Fig.3, bottom, right hand side) and/or in equal gain of the current controller independent of the phase current sign.

2.2 Coupling of the Phases

As described in section 2.1 the shape of input phase current $i_{N,i}$ is defined by the voltage appearing across the input inductors

$$L_N \frac{di_{N,i}}{dt} u_{L,i} = u_{N,i} - u'_{U,i} \ . \qquad (1)$$

It is important to point out that the rectifier input voltage $u'_{U,i}$ (referred to the mains star point N) is determined not only by $u_{U,i}$ (referred to the output voltage center point),

$$u_{U,i} = \begin{cases} \text{sign}\{i_{N,i}\}\frac{U_Z}{2} & \text{if} \quad s_i = 0 \\ 0 & \text{if} \quad s_i = 1 \end{cases} , \qquad (2)$$

(and/or by the state of the switch S_i and sign$\{i_{N,i}\}$) but also by the switching states of the other phases due to the influence of the voltage u_0 between the output voltage center point M and N.

Based on

$$\begin{aligned} L_N \frac{di_{N,R}}{dt} &= u_{N,R} - u_{U,R} - u_0 \\ L_N \frac{di_{N,S}}{dt} &= u_{N,S} - u_{U,S} - u_0 \\ L_N \frac{di_{N,T}}{dt} &= u_{N,T} - u_{U,T} - u_0 \end{aligned} \qquad (3)$$

u_0 can be calculated as

$$u_0 = -\frac{1}{3}(u_{U,R} + u_{U,S} + u_{U,T}) \qquad (4)$$

where $u_{N,R} + u_{N,S} + u_{N,T} = 0$ and $i_{N,R} + i_{N,S} + i_{N,T} = 0$ and/or $\frac{di_{N,R}}{dt} + \frac{di_{N,S}}{dt} + \frac{di_{N,T}}{dt} = 0$ has to be considered.

Connecting M and N and/or short-circuiting u_0 ($u_0 = 0$) would decouple the three phases and/or would turn the three-phase rectifier into three independent single-phase rectifier systems being connected in parallel at the output side. According to Eq.(1) then the shape of a phase current $i_{N,i}$ only is determined by the switching state of the corresponding phase i.

The coupling of the phases results in an increased number of rectifier input voltage levels being available for guiding the phase currents and or allows a closer approximation of the ideal purely sinusoidal shape of $u'_{U,i}$. (cf. Eq.(1) and Fig.6(b) in [3]). Therefore, applying a current control scheme taking into account the coupling of the phases will reduce the amplitudes of input current harmonics with switching frequncy significantly as compared to independent current control of the phases (cf. section 4).

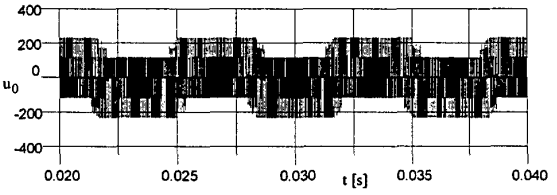

Fig.4: Time behaviour of the voltage u_0 between the output voltage center point M of the VIENNA Rectifier I and the mains star point N.

2.3 Control of the VIENNA Rectifier I (Ramp Comparison Current Control)

The block diagram of the ramp comparison current control of one phase of the VIENNA Rectifier I is shown in **Fig.5**. The sinusoidal current reference value $i^*_{N,i}$, which is in phase with the corresponding mains voltage $u_{N,i}$, is compared to the actual input current value $i_{N,i}$ and the control difference $\Delta i_{N,i}$ is added to the carrier signal which defines the switching frequency. The amplitude of the current reference value $i^*_{N,i}$ is set by an output voltage controller, which is omitted in Fig.5.

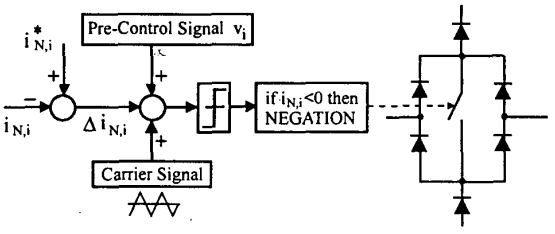

Fig.5: Block diagram of the ramp comparison control of one phase current of the VIENNA Rectifier I. The combinatorial logic considers the dependency of the rectifier input voltage formation (cf. section 2.1) on the sign of the phase current by inverting the comparator output s_i for $i_{N,i} < 0$.

By ramp comparison current control the relative on-time of a switch (and/or of the local average rectifier input voltage $u_{U,i,avg} = u_{U,i,avg}\{v_i\}$ being required for guiding the current along the sinusoidal reference) is determined by the intersection of the current control error $\Delta i_{N,i}$ with the carrier signal. Neglecting the fundamental of the voltage $u_{L_N,i} = L_N \frac{di_{N,i}}{dt}$ across the inductor L_N, in a first approximation

$$u_{U,i} \approx u_{N,i} \qquad (5)$$

has to be generated at the rectifier input. Accordingly, generating $u_{N,i}$ by a pre-control signal v_i allows to limit the

stationary current control error to very low values. Based on the characteristics $u_{U,i,avg} = u_{U,i,avg}\{v_i\}$ shown in Fig.3 there results for positive input currents $i_{N,i} > 0$

$$v_i = \hat{I}_{DR}(\frac{4u_{N,i}}{U_Z} - 1) \quad (6)$$

($\hat{I}_{DR}$ denotes the amplitude of the carrier signal); for $i_{N,i} < 0$ we have

$$v_i = \hat{I}_{DR}(\frac{4u_{N,i}}{U_Z} + 1) \; . \quad (7)$$

2.4 Switching State Sequence

As shown in **Fig.6** the intersection of the pre-control signals v_R, v_S and v_T with the carrier signal (showing sawtooth or triangular shape) defines the switching state sequence $(s'_R\, s'_S\, s'_T)$, e.g., (000) – (001) – (011) – (111) for $i_{N,R} > 0, i_{N,S} < 0, i_{N,T} < 0$ and/or $v_R > 0$ and $v_S < 0, v_T < 0$, and the relative on-time of the different switching states. As already explained in section 2.3 the switching states s'_i of phases with negative currents have to be inverted which results in the final switching states $(s_R\, s_S\, s_T)$ = (011) – (010) – (000) – (100) as shown in Fig.6. (Within one pulse-period $T_P = \frac{1}{f_P}$ the pre-control signals v_i varying with fundamental frequency can be assumed as constant.)

For the resulting switching sequence each change-over to a subsequent switching state is done by switching of always only one power transistor S_i, i.e., the switching pattern is optimized concerning the switching losses and is identical with the pattern of space vector based current control schemes (which show a considerably higher realization effort).

3 Not-Synchronized Sawtooth-Shaped versus Synchronized Triangular-Shaped Phase Carrier Signals

(1) Independent Sawtooth-Shaped Carrier Signals

For current control in single-phase PWM rectifier systems ramp comparison control as depicted in Fig.5 can be realized advantageously by using integrated single-phase control cicuits. Since for single-phase systems it does not matter if the carrier signal shows a sawtooth or triangular shape, integrated single-phase control circuits employ a sawtooth-shaped carrier signal due to the relatively low relization effort of a sawtooth generator.

Three independent integrated single-phase controllers also could be employed in a first approach for realizing a simple and inexpensive ramp comparison current control of a three-phase PWM rectifier system. However, this ignores the implicit coupling of the three phases (section 2.2) which results in increased amplitudes of harmonics with switching frequency of the rectifier input current as compared to coordinated switching of the phases.

(2) Synchronized Sawtooth-Shaped Carrier Signals

For taking advantage of the coupling of the phases the carrier signals of the phase current controllers have to synchronized, i.e. should be identical in frequency and phase. This easily can be achieved by extending the integrated control by some external components and results in a significant reduction of the ripple and of the harmonics of the input current as compared to independent phase current control.

(3) Synchronized Triangular Carrier Signal

Using a single triangular carrier signal for ramp comparison phase current control in three-phase PWM rectifier systems reduces the harmonics and the ripple of the input current theoretically to about 60% as compared to a synchronous sawtooth shaped carrier control with equal switching losses. Therefore, in order to achieve an optimized system behaviour and/or minimum mains current ripple for given transistor losses the current control has to be based on synchronized triangular carrier signals.

A clear theoretical explanation of the advantage of the use of (synchronized) triangular carrier signals as compared to using (synchronized) sawtooth signals can be given based on **Fig.6**.

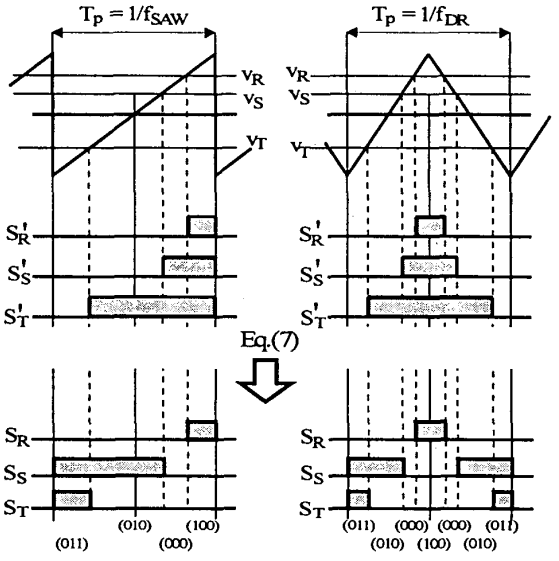

Fig.6: Determination of the switching states of the power transitors S_i of the VIENNA Rectifier I by intersecting phase pre-control signals v_i with a sawtooth-shaped or a triangular-shaped carrier signal.

Figure 6 shows the single sawtooth carrier resulting for synchronizing the phase sawtooth carriers of frequency f_{SAW} and the phase pre-control signals v_R, v_S, v_T as given within the considered $\frac{\pi}{3}$-wide interval of the mains period $(i_{N,R} > 0, i_{N,S} < 0, i_{N,T} < 0)$. The switching of the power transistors S_R, S_S and S_T is defined by the intersections of the carrier and the corresponding sum of the pre-control signal and the control error $\Delta i_{N,i}$ (not shown in Fig.6). The switching states of the rectifier system are denoted by combining the phase switching functions s_i to triples $(s_R\, s_S\, s_T)$ = (011), (010), (000) or (100). Based on a space-vector analysis of the voltage formation of the VIENNA Rectifier I [5] it can be shown that always 4 switching states have to be applied within a pulse half period T_P of the carrier signal in order to achieve a minimum ripple of the sinusoidal system input currents. The absolute input current ripple amplitude is dependent on the frequency of the carrier signal. The higher the switching frequency, the smaller is the ripple and the distortion of the input

current. But by increasing the switching frequency of the carrier signal also the switching losses are increased accordingly. In case of a triangular carrier signal, as shown at the right hand side of Fig.6, the switching states (011), (010), (000) are applied *two times* within each pulse period $T_P = \frac{1}{f_{DR}} = \frac{1}{f_{SAW}}$, although the three power transistors have exactly equal switching losses as in case of a sawtooth-shaped carrier. Applying 3 out of 4 switching states twice reduces the ripple of the input current to about 60%, as will be shown in the following by a digital simualtion.

Remark: For a triangular shaped carrier in general no simultaneous swiching of all three phases occurs at the end of each pulse period, but each subsequent switching state is reached by switching of only a single power transistor. Therefore, within each pulse period a switching state sequence consisting of 6 and not of only 4 switching states is applied. In a first approximation this is equal to increasing the effective switching frequency of a sawtooth carrier by a factor of 6/4 and/or corresponds to a reduction of the amplitude of the mains current ripple by 2/3 ($\approx 60\%$).

4 Simulation Results

4.1 Simulation Parameters

The parameters of the digital simulation have been set according to a typical practical application of the VIENNA rectifier I for the realization of the front end of a high power three-phase AC-to-DC telecommunications power supply module

$\hat{U}_N = 327\text{V}$ $\quad f_N = 50\text{Hz}$ $\quad L_N = 300\mu\text{H}$
$U_Z = 700\text{V}$ $\quad \hat{I}_N^* = 18\text{A}$ $\quad P_{IN} = 8.8\text{kW}$.

For the system switching frequency a relatively low value has been selected in order to clearly show details of the time behaviour of the mains current ripple and for limiting the simulation time. For a practical realization one typically would select a switching frequency of 30...50kHz.

(1) Not Synchronized Sawtooth Carrier Signals

Since the there is no synchronization of the three integrated single-phase control circuits the three sawtooth carrier signals will in general show slightly different frequencies due to tolerances of the passive components defining the pulse frequency. For the simulation this has been considered by selecting

$f_{SAW,R} = 15.5\text{kHz}$ (-3%)
$f_{SAW,S} = 16.0\text{kHz}$
$f_{SAW,T} = 16.5\text{kHz}$ (+3%) .

Therefore, the slope of the carrier $\frac{d}{dt} i_{SAW} = \hat{I}_{SAW} / \frac{1}{2} T_P$ has to be higher than the maximum slope of the current control error and/or of the deviation of the actual phase current $i_{N,i}$ from its reference value and/or its fundamental. For amplitudes of the mains phase voltages in the range of $\hat{U}_N \in (\frac{1}{3}U_Z, \frac{2}{3}U_Z)$ this results in a minimum required amplitude of the sawtooth carrier of

$$\hat{I}_{SAW,MIN} = \frac{U_Z}{6 f_{SAW} L_N} \tag{8}$$

if $\frac{d}{dt}\Delta i_{N,i} = \frac{1}{L_N}(u_{N,i} - u_{U,i} - u_0)$ and $u_0 = -\frac{1}{3}U_Z, -\frac{1}{6}U_Z, 0, +\frac{1}{6}U_Z, +\frac{1}{3}U_Z$ are considered [6] and/or as can be shown clearly by a space vector based analysis of the system (which has been omitted here for the sake of brevity). For the given simulation parameters there follows $\hat{I}_{SAW,MIN} = 24.3\text{A}$, for the simulation $\hat{I}_{SAW}$ has been set to 26A.

(2) Synchronized Sawtooth Carrier Signals

According to a synchronization of the phase control carriers in frequency and phase we define

$$f_{SAW,R} = f_{SAW,S} = f_{SAW,T} = 16.0\text{kHz}$$
$$\varphi_{SAW,R} = \varphi_{SAW,S} = \varphi_{SAW,T} = 0 \ .$$

The required minimum amplitude of the carrier signals is not influenced by the synchronization and, therefore, is set again to $\hat{I}_{SAW} = 26\text{A}$ (as for control scheme (1)).

(3) Synchronized Triangular Carrier Signals

There, the carrier signals are synchronized and triangular-shaped with a frequency of $f_{DR} = 16.0\text{kHz}$. The required minimum amplitude of the triangular carrier is half the value of the carrier amplitude required for a sawtooth-shaped carrier because a symmetrical triangular carrier signal $\frac{di_{DR}}{dt} = \frac{\hat{I}_{DR}}{\frac{1}{4}T_P}$ shows twice the slope of the sawtooth carrier, while the maximum slope of the current error $\frac{d}{dt}\Delta i_{N,i} = \frac{1}{L_N}(u_{N,i} - u_{U,i} - u_0)_{MAX} = \frac{1}{L_N}\frac{U_Z}{3}$ remains unchanged (cf., e.g., $U_{N,R} = \frac{1}{3}U_Z$, $U_{N,S} = -\frac{1}{6}U_Z$, $U_{N,T} = -\frac{1}{6}U_Z$, $u_{U,R} = +\frac{1}{2}U_Z$, $u_{U,S} = 0$, $u_{U,T} = -\frac{1}{2}U_Z$, $u_0 = 0$, $L_N \frac{d}{dt} i_{N,T} = \frac{1}{3}U_Z$). Therefore, there results

$$\hat{I}_{DR} > \frac{U_Z}{12 f_{DR} L_N} = 12.2\text{A} \ ; \tag{9}$$

accordingly the carrier amplitude has been set to $\hat{I}_{DR} = 13\text{A}$.

4.2 Time Behaviour of the Input Current

The simulation parameters defined in section 4.1 guarantee approximately equal switching losses of the control concepts (1), (2) and (3) and, therefore, allow to directly compare the simulation results.

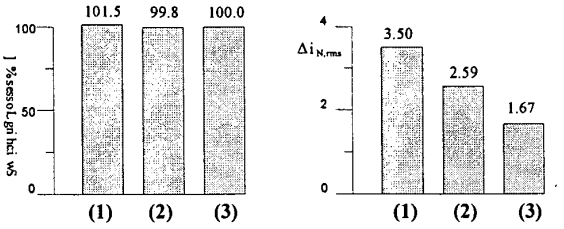

Fig.7: Switching losses (left hand side) and rms value of the ripple of the mains current for different shapes of the carrier signals of the ramp comparison current phase control; **(1)** not synchronized sawtooth carrier signals, **(2)** synchronized sawtooth-shaped carrier signals, **(3)** synchronized triangular-shaped carrier signals.

If the switching frequency f_P is constant during the mains period the total switching loss of one power transistor can be written as

$$P_V = \frac{2}{T_N} \int_0^{\frac{1}{2}T_N} k \ i_{N,i} \ f_P \ dt = \frac{2}{\pi} k \ f_P \ \hat{I}_N \tag{10}$$

[7] if the switching losses are assumed to show a linear dependency on the actual value of the current being switched ($\hat{I}_N$ denotes the amplitude of the mains phase current $i_{N,i}$, k is a factor characterizing the switching losses of the specific power transistor in dependency of the semiconductor junction temperature and of the turn-off voltage) and if only the mains current fundamental is considered. According to Eq.(10) the total switching losses are proportional to the frequency of the carrier signal and are independent of the carrier shape. For taking into account also the input current harmonics with switching frequency and/or calculating the switching losses by digital simulation minor differences of the switching losses of the different control methods result (cf. **Fig.7**, left hand side) which, however, are of no importance for the following considerations.

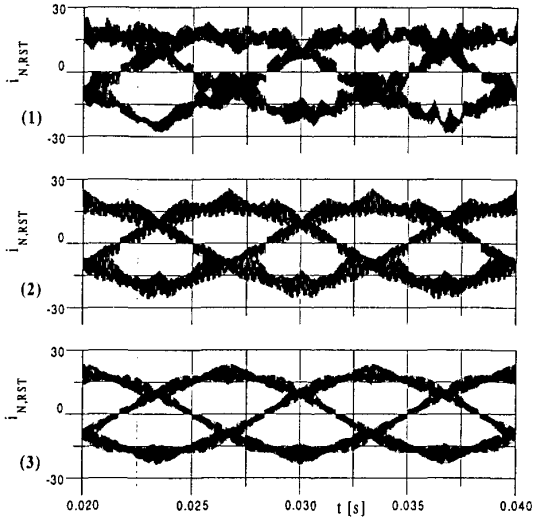

Fig.8: Digital simulation of the time behaviour of the mains phase currents of the VIENNA Rectifier I for different carrier signals of the ramp comparison phase current control; **(1)** not synchronized sawtooth-shaped carrier signals, **(2)** synchronized sawtooth-shaped carrier signals, **(3)** synchronized triangular-shaped carrier signals.

As shown in **Fig.8** and **Fig.9** the input current ripple is significantly smaller for using synchronized triangular carrier signals (3) as compared to using synchronized sawtooth-shaped carrier signals (2). Not synchronized sawtooth carriers (1) result in the largest ripple amplitude.

A numerical calculation of the averaged rms-value of the phase current ripples

$$\Delta i^2_{N,rms} = \frac{1}{3}(\Delta i^2_{N,R,rms} + \Delta i^2_{N,S,rms} + \Delta i^2_{N,T,rms}) \quad (11)$$

gives a characteristic value for describing the quality of the different current control schemes (cf. Fig.7, right hand side). According to the theoretical considerations in section 3 control scheme (3) shows the lowest averaged rms-value of the input current ripples which is reduced by a factor of approximately $\frac{2}{3}$ as compared to control scheme (2). Not synchronizing the sawtooth-shaped carrier signals and/or control scheme (1) results in an rms-value being higher by an factor of about 2 as compared to control scheme (3) due to the uncoordinated operation of the phase current controllers.

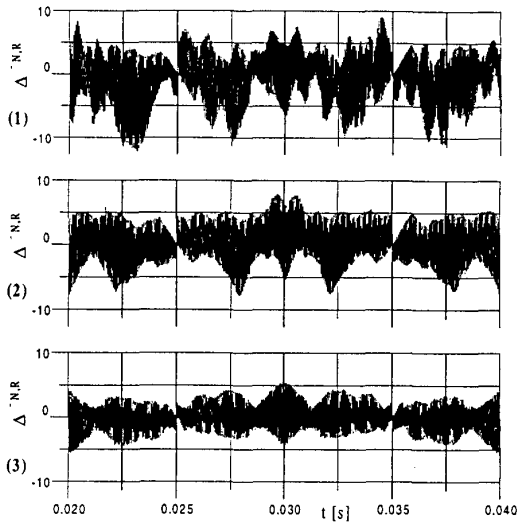

Fig.9: Digital simulation of the time behaviour of the ripple of a mains phase current of the VIENNA Rectifier I for different carrier signals of the ramp comparison phase current control; **(1)** not synchronized sawtooth-shaped carrier signals, **(2)** synchronized sawtooth-shaped carrier signals, **(3)** synchronized triangular-shaped carrier signals.

The asymmetry of the current ripple (cf. Fig.9) concerning the positive and the negative current fundamental half period occurring for control schemes (1) and (2) is due to the asymmetry of the sawtooth carrier signal. Inverting the sawtooth carrier would results in an inversion of the unsymmetry of the current ripple. Only for inverse switching sequences of successive pulse half periods a local zero average value of the current ripple, and/or no low frequency distortion of the input phase currents occurs.

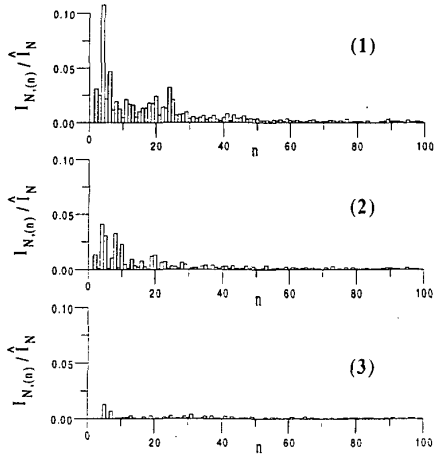

Fig.10: Normalized spectrum (related to the mains current fundamental) of a mains phase current of the VIENNA Rectifier I for different carrier signals of the ramp comparison phase current control (n denoted the ordinal number of the harmonics); **(1)** not synchronized sawtooth-shaped carrier signals, **(2)** synchronized sawtooth-shaped carrier signals, **(3)** synchronized triangular-shaped carrier signals.

4.3 Harmonics of the Mains Current

Ramp Comparison Current Control concentrates the harmonics of the input current around multiples of the switching frequency which is defined by the frequency of the carrier signal. For the operating parameters defined in section 4.1 the harmonics are grouped around 16kHz, 32kHz, 48kHz, etc. Since low-frequency harmonics are very difficult to filter this is a distinct advantage of ramp comparison control as compared to current control concepts with not constant and/or load-dependent switching frequency, e.g., tolerance band phase current control where the harmonics are distributed over a wide frequency range and subharmonics of the mains frequency could occur.

As **Fig.10** shows, the remaining harmonics with low frequency are clearly reduced in case of synchronized triangular carrier signals (3) as compared to control scheme (2) and, especially, concerning control scheme (1). This results in a significant reduction of the effort required for limiting high frequency conducted emissions to given values.

5 Experimental Results

As **Fig.11** clearly shows, the results of the theoretical considerations and digital simulations are fully verified by measurements on a 10kW laboratory prototype of the VIENNA Rectifier. There, the system operating parameters have been set as defined in section 4.

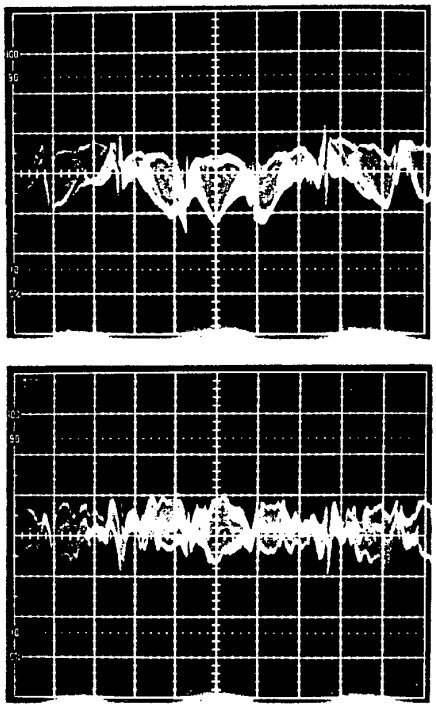

Fig.11: Experimental analysis of the VIENNA Rectifier I. Time behavior of the mains current ripple for synchronized sawtooth-shaped carrier signals (top) and synchronized triangular-shaped carrier signals (bottom) of the input phase current controllers.

6 Conclusion

On the example of the VIENNA Rectifier I it has been shown that employing three integrated single-phase control circuits for the independent control of the mains phase currents gives a very low realization effort but results in a relatively high ripple of the input currents. By changing the shape of the carrier signal from sawtooth to triangular and by synchronizing the carrier signals of the phase current controllers (and/or by coordinating the switching actions of the phases) the input current ripple is reduced by a factor of about 2 while the switching losses remain unchanged. Weight, size and cost of an input EMI-filter can be significantly reduced, therefore. This is valid in general for boost-type three-phase PWM rectifier systems.

ACKNOWLEDGMENT

The authors are very much indebted to the Jubiläumsfonds der ÖSTERREICHISCHEN NATIONALBANK which generously supports the work of the Department of Electrical Drives and Machines of the Technical University of Vienna.

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