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***Abstract*—Driven by the needs of the continuously growing fuel-cell industry, a promising three-phase inverter topology, the Y-inverter, is proposed, which comprises three identical buck-boost DC/DC converter modules connected to a common star point. Each module constitutes a phase-leg and can be operated in similar fashion to conventional DC/DC converters, independent of the remaining two phases. Therefore, a straightforward and simple operation is possible. In addition, the Y-inverter allows for continuous output AC voltage waveforms, eliminating the need of additional AC-side filtering. Due to the buck-boost nature of each phase leg, the AC voltages can be higher or lower than the DC input voltage. This is an essential feature for fuel-cell applications, which suffer from a wide DC input voltage range. This paper details the operating principle of the Y-inverter, outlines the control system design and verifies its functionality by means of simulation results. The Y-inverter performance in terms of efficiency η and power density ρ is briefly analyzed by means of a multi-objective optimization and a converter design is selected which is compared to a benchmark system realized with a conventional inverter solution.**

***Index Terms*—High-speed drives, Y-inverter, Fuel-cell application, Wide input and output voltage range, Control system**

I. Introduction

As the proliferation of industrial and automotive fuel-cell (FC) applications continues, the demand for highly efficient converters in a small form factor is intensified [1]. Typically, the oxygen needed for the fuel-cell operation, is provided by a compressor unit with a power rating of approximately 10% of the FC power. The compressor is driven by an auxiliary motor drive system which is directly powered from the FC (cf. **Fig. 1(a)**). Fuel-cells exhibit a wide voltage range and are characterized by a negative voltage coefficient, meaning that their voltage is dropping as the extracted current is increasing. This poses challenges for the design of the inverter power electronics which must be dimensioned for both the high blocking voltage under low power, as well as the high currents under full power operation. Those two design constraints are contradictory and inevitably lead to oversized converters with inferior performance. At the same time the EMI emission regulations, with respect to the AC output, are becoming progressively more stringent. For this reason, an AC-side LC filter structure usually follows the inverter in order to ensure sinusoidal high quality output currents and voltages. The bulky inductive components of the filter further add to the electronics volume and losses.

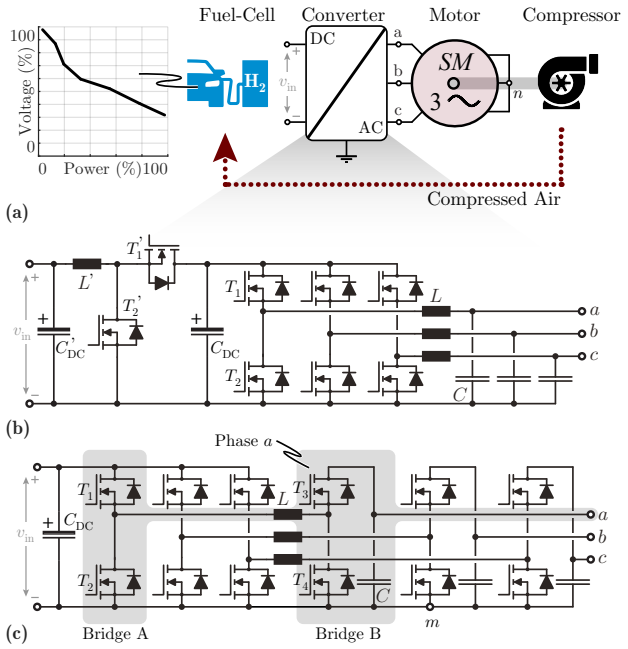

Fig. 1: In **(a)** a typical 10 kW fuel-cell (FC) application is depicted. The oxygen needed for the FC operation is provided by a high-speed compressor controlled by a FC attached motor drive. In **(b)** the conventional inverter solution, with a DC/DC boost converter followed by a voltage source inverter (boost VSI) is depicted, while in **(c)** the proposed three-phase Y-inverter featuring three identical buck-boost phase modules is illustrated.

There has been extensive research towards inverter topologies that counterbalance the inherent limitations of a varying DC input voltage. A popular solution is a DC/DC boost converter cascaded with a voltage source inverter (boost VSI) which is depicted in **Fig. 1(b)** [2]. The boost converter generates a stable, easily controllable, high DC-link voltage that mitigates the current stress of the inverter under full power operation. However, increased number of inductive components and semiconductor losses originating from the DC/DC stage degrade

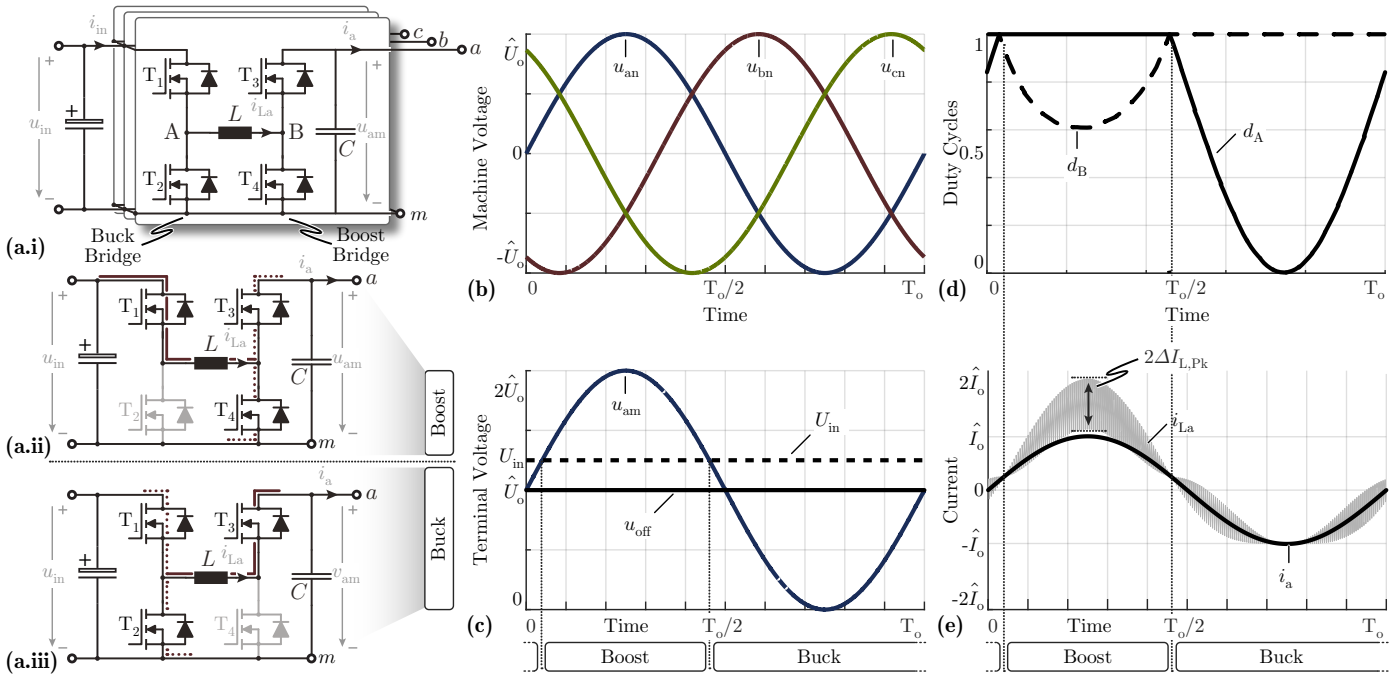

Fig. 2: Operating principle of the Y-inverter. In **(a.i)** one of the three identical bridge-leg modules comprised in the Y-inverter is depicted. In **(a.ii)** and **(a.iii)** the boost and buck operation are highlighted respectively. In **(b)** the three AC motor voltages voltages are illustrated while in **(c)** the corresponding strictly positive terminal inverter output voltage of phase a is depicted. The required buck d_{A} and boost d_{B} duty cycles are presented in **(d)** and the inductor current i_{La} is plotted on top of the motor AC current i_{a} in **(e)**.

the overall system performance. Alternative single conversion stage topologies, such as the Z-source inverter, have gained significant interest over the past decade [3] [4]. The Z-source inverter utilizes a unique impedance network and shoot-through zero states to boost the voltage of the capacitors of the Z-source network, but suffers from increased voltage stress under high boost ratios.

In response to these shortcomings, an inverter module, referenced to as Y-inverter (cf. **Fig. 1(c)**), is presented within this paper. Based on the well established idea of realizing a three-phase inverter by connecting three DC/DC converters to a common star point [5]–[10], three identical phase modules are attached to the negative DC-rail m. The Y-inverter benefits from three key features. Firstly, each phase-leg can employ simple controllers similar to conventional DC/DC converters. Secondly, the Y-inverter provides a continuous AC output voltage which eliminates the need of a dedicated output filter. Finally, due to its buck-boost characteristic, the DC input voltage can be higher or lower than the AC voltage.

In this paper, in a first step the operating principle of the Y-inverter is explained in **Sec. II**. An appropriate control scheme in introduced in **Sec. III** while the seamless and uncomplicated operation of the Y-inverter is verified by means of simulation results. **Sec. IV** is dedicated to the selection of the hardware demonstrator and the critical design aspects. Finally, the conclusions are drawn in **Sec. V**.

TABLE I: Y-inverter fundamental quantities.

Parameter	Buck Operation	Boost Operation
u_{am}	$\leq U_{\mathrm{in}}$	$\geq U_{\mathrm{in}}$
d_{A}	$\frac{u_{\mathrm{am}}(t)}{U_{\mathrm{in}}} \in [0...1]$	1
d_{B}	1	$\frac{U_{\mathrm{in}}}{u_{\mathrm{am}}(t)} \in [0...1]$
Switch signals	T_1 on : $d_{\mathrm{A}} >$ Car	T_1 on
	T_2 on : $d_{\mathrm{A}} <$ Car	T_2 off
	T_3 on	T_3 on : $d_{\mathrm{B}} >$ Car
	T_4 off	T_4 on : $d_{\mathrm{B}} <$ Car
u_{A}	$d_{\mathrm{A}} U_{\mathrm{in}}$	U_{in}
u_{B}	u_{am}	$d_{\mathrm{B}} u_{\mathrm{am}}$
u_{am}	$d_{\mathrm{A}} U_{\mathrm{in}}$	$\frac{1}{d_{\mathrm{B}}} U_{\mathrm{in}}$
Low freq. ind. current $\langle i_{\mathrm{La}} \rangle$	i_{a}	$\frac{1}{d_{\mathrm{B}}} i_{\mathrm{a}}$
$\Delta I_{\mathrm{L,Pk}}$	$\frac{1}{2} \frac{d_{\mathrm{A}}(1-d_{\mathrm{A}}) U_{\mathrm{in}}}{f_{\mathrm{s}} L}$	$\frac{1}{2} \frac{d_{\mathrm{B}}(1-d_{\mathrm{B}}) u_{\mathrm{am}}}{f_{\mathrm{s}} L}$

II. Operation Principle

The Y-inverter, presented in **Fig. 1(c)**, consists of three identical phase-legs: Each phase is comprised of two half bridges connected to the opposite terminals of an inductor L, and an output capacitance C placed between the AC output terminal a, b, c and the negative DC-rail m, which forms a

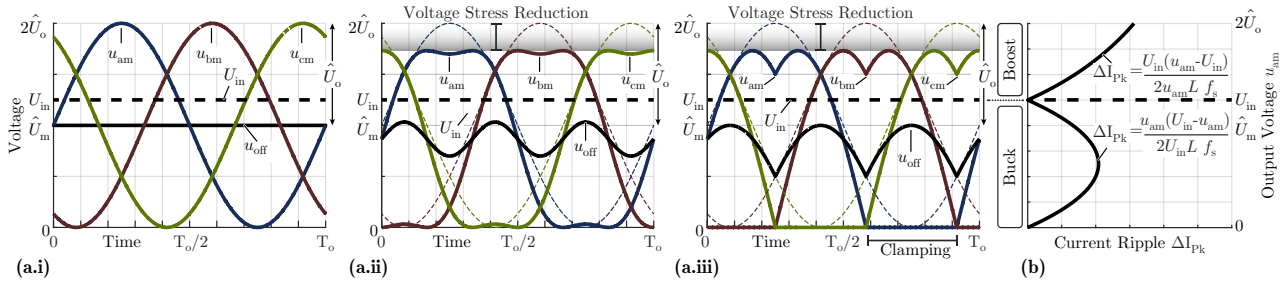

Fig. 3: Possible Y-inverter modulation schemes. In **(a.i)** the standard modulation is depicted where a constant offset $u_{\text{off}} = \hat{U}_{\text{o}}$ is added to the AC motor voltage u_{a} in order to form the strictly positive terminal inverter voltage u_{am}. In **(a.ii)** a third harmonic pattern is superimposed to the offset voltage $u_{\text{off}} = \frac{\sqrt{3}}{2}\hat{U}_{\text{o}} + \frac{1}{6}\hat{U}_{\text{o}}\sin(3\omega t)$ resulting in the same motor AC line-to-line voltage but with 13% lower voltage stress on the semiconductor devices (for the same modulation depth). In **(a.iii)** discontinuous modulation scheme applied to of the Y-inverter where the phase-leg with the most negative voltage is clamped to zero. Thereby, the switching losses are reduced up to 33%. Finally in **(b)** the dependency of the inductor current ripple over the full output voltage range is analytically derived.

common star Y-point among the three phases. The potential of each AC inverter output is strictly defined with respect to m and is independent of the remaining two phases. Each phase can be operated autonomously, as an equivalent single-phase converter. This feature significantly simplifies the converter analysis and reduces the control effort.

The focus is now shifted on phase a (cf. **Fig. 2(a.i)**), whose structure is equivalent to a non-isolated buck-boost DC/DC converter [11]. The left half-bridge (T_1, T_2) is dedicated to buck converter operation (cf. **Fig. 2(a.iii)**) while the right hand side bridge (T_3, T_4) is exclusively used for boost operation (cf. **Fig. 2(a.ii)**). The buck and boost bridges are operated in a mutually exclusive fashion, meaning that only one of the two half-bridges is pulse width modulated (PWM) at a time, while the top side switch of the second bridge is clamped to an active on-state. The duty cycles d_{A} and d_{B} control the high side switch of the buck and boost bridge-leg respectively. In buck operation, the duty cycle of the buck bridge-leg d_{A} ranges from 0 to 1, while the duty cycle of the boost bridge-leg d_{B} is kept to 1. Hence, the topology reduces to a simple buck converter (cf. **Fig. 2(a.iii)**) that yields a controllable output voltage $u_{\text{am}} = d_{\text{A}} U_{\text{in}} \leq U_{\text{in}}$. On the other hand, during boost operation, the duty cycle of the boost bridge-leg d_{B} ranges from 0 to 1, while the duty cycle of the buck bridge-leg d_{A} is maintained at 1, i.e. the switch T_1 is permanently on (cf. **Fig. 2(a.ii)**). In this case, the topology is equivalent to a boost converter where $u_{\text{am}} = \frac{1}{d_{\text{B}}} U_{\text{in}} > U_{\text{in}}$. The important system quantities are summarized in **Tab. I** for buck and boost operation.

Returning to the three-phase consideration, a sinusoidal AC voltage $u_{\text{an}} = \hat{U}_{\text{o}}\sin(\omega t)$ with respect to the load open star connection n must be formed (cf. **Fig. 2(b)**). This voltage cannot be directly reproduced by the phase leg a, since each phase leg is comprised in a bidirectional DC/DC converter with strictly positive output voltage, $u_{\text{am}} > 0$. Instead, a sinusoidal voltage with an offset $u_{\text{off}} = \hat{U}_{\text{o}}$, such that it remains always positive, can be generated, $u_{\text{am}} = \hat{U}_{\text{o}}\sin(\omega t) + u_{\text{off}}$ (cf. **Fig. 2(c)**). If this concept is extended to the remaining phases b and c, then three sinusoidal voltages with the same offset voltage are formed (with respect to the Y-inverter star point m). The DC offset $u_{\text{off}} = \hat{U}_{\text{o}}$ clearly constitutes a common mode (CM) voltage component, and thus cannot drive any current in an open star three phase load

$$\begin{aligned} u_{\text{CM}} &= \frac{u_{\text{am}} + u_{\text{bm}} + u_{\text{cm}}}{3} = \hat{U}_{\text{o}} \\ u_{\text{an}} &= u_{\text{am}} - u_{\text{CM}} = \hat{U}_{\text{o}}\sin(\omega t). \end{aligned} \tag{1}$$

The strictly positive, sinusoidally modulated, phase voltages $u_{\text{i,m}}, i \in a, b, c$, drive purely sinusoidal load currents and hence voltages $u_{\text{i,n}}, i \in a, b, c$, across the load. Depending on the instantaneous voltage reference $u^*_{\text{am}}(t)$, the inverter transitions seamlessly between buck and boost operation: When $u^*_{\text{am}}(t)$ is lower that the DC-link voltage U_{in} then the Y-inverter is operated in buck regime, while boost regime is employed when $u^*_{\text{am}}(t) > U_{\text{in}}$.

For high switching to fundamental frequency ratios ($\frac{f_{\text{s}}}{f_{\text{o}}} \gg 1$), the dynamics of the DC/DC phase-leg converter are orders of magnitude faster than the frequency of the sinusoidal currents and voltages. Thus, each point of the slowly changing fundamental voltage u_{am} can be considered as a steady state operating point from the DC/DC converter perspective. According to this local static model of the DC/DC converter, the duty cycles d_{A} and d_{B} can be calculated by considering the input to output voltage ratios during buck and boost operating regime

$$\begin{aligned} d_{\text{A}} &= \min\left[1, \frac{u_{\text{am}}(t)}{U_{\text{in}}}\right] \\ d_{\text{B}} &= \min\left[1, \frac{U_{\text{in}}}{u_{\text{am}}(t)}\right]. \end{aligned} \tag{2}$$

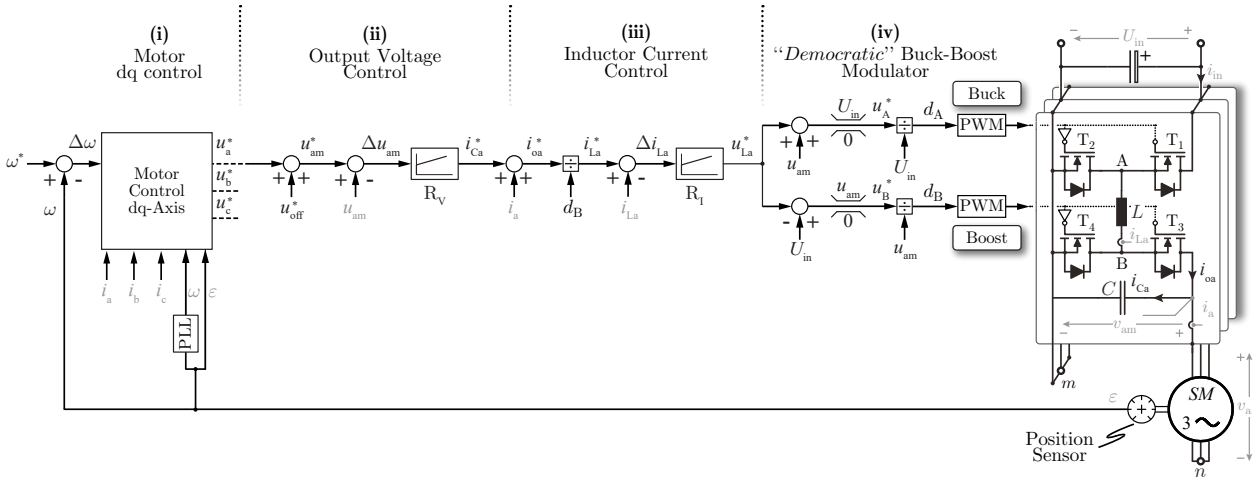

Fig. 4: Y-inverter control block diagram. In **(i)** the cascaded motor speed ω current i_{a} controller is illustrated that provides the three machine reference terminal voltages $u_{\mathrm{a}}^*, u_{\mathrm{b}}^*, u_{\mathrm{c}}^*$ which must be generated by the converter. The cascaded terminal voltage (external loop) inductor current (internal loop) controller employed by each phase module of the Y-inverter is illustrated in **(ii)**,**(iii)** respectively. The inductor reference voltage u_{La}^* derived from the cascaded control structure is translated into the corresponding buck and boost bridge-leg duty cycles $d_{\mathrm{A}}, d_{\mathrm{B}}$ by the "*democratic*" buck-boost modulator shown in **(iv)**.

The resulting duty cycle signals are visualized in **Fig. 2(d)**. Due to the switched operation of the buck or boost half-bridge, a high frequency voltage is applied across the phase-leg inductor L, which generates a current ripple with amplitude $\Delta I_{\mathrm{L,Pk}}$ (cf. **Tab. I**). The current ripple depends on both the instantaneous terminal voltage u_{am} as well as on the operating regime (i.e. buck or boost operation) as visualized in **Fig. 3(b)**. The output current of the boost half-bridge (T_3, T_4) is filtered by the terminal capacitor C resulting in a high quality, predominantly sinusoidal load voltage u_{an} and eliminating the need for additional filtering on the AC load side.

A. Modulation Techniques

The offset voltage u_{off}, which is added to the AC motor voltage u_{a} in order to maintain the terminal inverter voltage u_{am} strictly positive, is now analyzed in more detail. In the course of the Y-inverter operating principle introduction (cf. **Fig. 3(a.i)**) the offset voltage was selected to be constant $u_{\mathrm{off}} = \hat{U}_{\mathrm{o}}$ however, this is not obligatory. The offset voltage, which is equivalent to the injected common mode (CM) voltage of a three-phase system $u_{\mathrm{off}} \equiv u_{\mathrm{CM}}$, represents an essential degree of freedom which can benefit the inverter performance [12], [13]. For example the superposition of a sinusoidal third harmonic component on the constant offset voltage $u_{\mathrm{off}} = \frac{\sqrt{3}}{2}\hat{U}_{\mathrm{o}} + \frac{1}{6}\hat{U}_{\mathrm{o}}\sin(3\omega t)$ is reminiscent of the third harmonic modulation (THM) of two-level three-phase inverters [14]. Such an approach allows for better utilization of the fuel-cell DC voltage. More precisely the same output voltage can be generated as in the standard modulation case where $u_{\mathrm{off}} = \hat{U}_{\mathrm{o}}$, but with approximately 13% lower voltage stress of the semiconductor devices as highlighted in **Fig. 3(a.ii)**. An alternative approach described in literature as discontinuous modulation (DCM) [15], [16] can also be applied to the Y-inverter: The phase with the most negative voltage is clamped to the negative DC rail m ($u_{\mathrm{i,m}} = 0, \quad i \in a, b, c$), for one third of the fundamental period $\frac{T_{\mathrm{s}}}{3}$. Accordingly, the clamped phase-leg exhibits no switched operation, leading to a total reduction of the switching losses of up to 33%. The beneficial 13% semiconductor voltage stress reduction also applies for the discontinuous modulation. The described modulation scheme is visualized in **Fig. 3(a.iii)**. The switching losses can be further reduced if zero voltage switching (ZVS) is achieved: To this end a triangular current modulation (TCM) can be employed [17], [18] where the inductor current i_{La} has a negative offset at the beginning and at the end of each switching period, enabling soft switching resonant transitions. A comprehensive analysis of optimal CM modulation techniques (OCMM) suitable for three-phase modular systems referenced to a common star point m can be found in [19].

III. Control System Design

The functionality of the Y-inverter is further evaluated within the context of an auxiliary fuel-cell high-speed motor drive. An industry solution example of a high-speed motor drive, required power of $1\,\mathrm{kW}$ and rotational motor speed of $300\,\mathrm{krpm}$ [20], [21]. The specifications of the motor drive are recapitulated in **Tab. II**. A standard cascaded motor speed-phase current controller is required, referenced to the dq-axis frame, in order

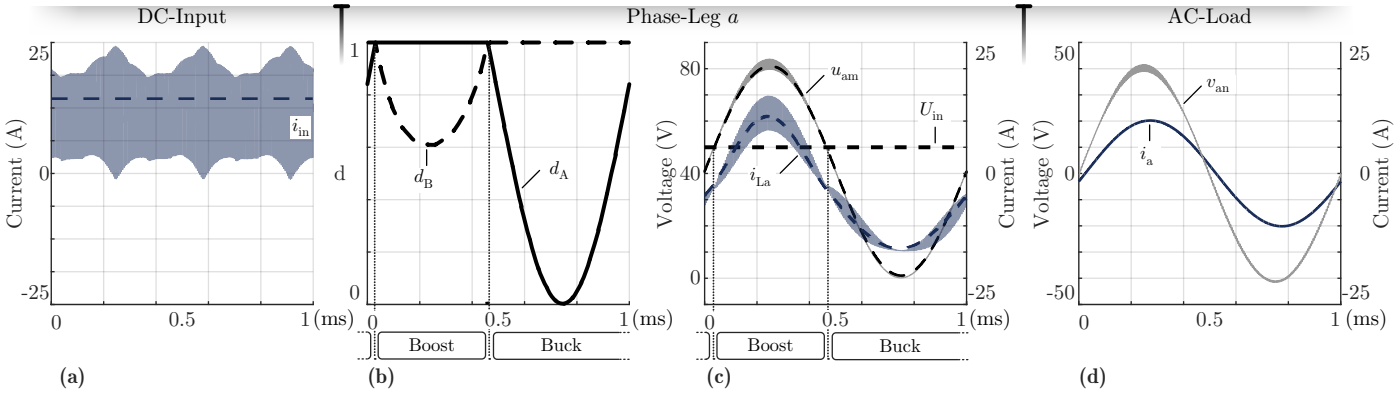

Fig. 5: Simulation results of the Y-inverter driving a high-speed motor. In **(a)** the input current drawn from the DC-link is shown. In **(b)** the buck and boost half-bridge duty cycles are illustrated, while in **(c)** the inductor current and the terminal voltage are depicted. Finally in **(d)** the output AC motor voltage and current of phase a are presented.

to drive the machine. As an input the motor controller receives the machine speed ω, angle ϵ and terminal currents $i_\mathrm{a}, i_\mathrm{b}, i_\mathrm{c}$ and in return yields the reference machine terminal AC voltages $u_\mathrm{a}^*, u_\mathrm{b}^*, u_\mathrm{c}^*$ which must be generated by the inverter (cf. **Fig. 4(i)**).

Each phase-leg is controlled independently ensuring that the output phase voltages $u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}$ follow their sinusoidal references $u_\mathrm{a}^*, u_\mathrm{b}^*, u_\mathrm{c}^*$. The controller block diagram visualized in **Fig. 4** for phase a is comprised of a cascaded output voltage u_a inductor current i_La controller. The splitting of the inductor current and the terminal voltage control, decouples the two state variables $u_\mathrm{a}, i_\mathrm{La}$ and hence allows for higher total bandwidth and superior dynamic performance. Firstly, the predetermined offset voltage u_off is added to the motor terminal voltage reference u_a^* in order to form the strictly positive inverter output voltage reference u_am^*. The output voltage error Δu_am is processed by a PI controller R_V (external output voltage control loop) and consequently added to the appropriate feed-forward terms, yielding the inductor current reference signal i_La^* (cf. **Fig. 4(ii)**). Afterwards, the inductor current error Δi_La is passed through another PI controller R_I (internal inductor current control loop) yielding the required voltage across the inductor u_{La}^* (cf. **Fig. 4(iii)**). More details of the external voltage and the internal current controller design are presented in **Tab III**. There, the transfer functions (TF) of the corresponding plants and controllers are shown, while the selected crossover frequencies and proportional gains are specified.

TABLE II: Fuel-cell powered high-speed motor drive specifications.

Parameter	Value
Motor	
Speed n	$300\,\mathrm{krpm}$
Induced voltage (EMF)	$30\,\mathrm{V_{RMS}}$ (Phase)
Power P	$1\,\mathrm{kW}$
Inductance L_m	$32.8\,\mu\mathrm{H}$
Resistance R_m	$91\,\mathrm{m}\Omega$
Fuel-cell	
Output power P_FC	$10\,\mathrm{kW}$
Compressor power P	$1\,\mathrm{kW}$
Fuel-cell voltage V_FC	40...120V

For the buck-boost modulator block there are several options how the required voltage across the inductor $u_\mathrm{La} = u_\mathrm{A} - u_\mathrm{B}$ can be generated. If for example a positive voltage $u_\mathrm{La}^* > 0$ is needed in order to increase the inductor current i_La, it can either be achieved by increasing the voltage u_A of bridge-leg A (i.e. increase d_A) or by decreasing the voltage u_B of bridge-leg B (i.e. decrease d_B). The translation of the inductor voltage u_La into the buck and boost bridge voltages $u_\mathrm{A}, u_\mathrm{B}$ and hence the duty cycles $d_\mathrm{A}, d_\mathrm{B}$ is performed by the modulator (cf. **Fig. 4(iv)**). The modulator follows a "*democratic*" strategy, in the sense that the inductor voltage formation burden is equally shared between the buck and boost bridges. Namely, if the Y-inverter is operated in buck regime (cf. **Fig. 2(a.iii)**), meaning that $u_\mathrm{am} + u_\mathrm{La}^* \leq U_\mathrm{in}$, the limiter $[0, u_\mathrm{am}]$ of the boost branch indicated in **Fig. 4(iv)** automatically saturates the duty cycle d_B

TABLE III: Cascaded terminal voltage-inductor current controller analysis. The associated transfer functions (TF) are specified, while guidelines regarding the selection of the PI controllers crossover frequency and proportional gains are provided.

Controller Type	Voltage	Current
Plant TF	$G_\mathrm{V} = \frac{\tilde{u}_\mathrm{am}}{\tilde{i}_\mathrm{Ca}} = \frac{1}{sC}$	$G_\mathrm{I} = \frac{\tilde{i}_\mathrm{La}}{\tilde{u}_\mathrm{La}} = \frac{1}{sL}$
Controller TF	$R_\mathrm{V} = K_\mathrm{V}\frac{1+sT_\mathrm{V}}{sT_\mathrm{V}}$	$R_\mathrm{I} = K_\mathrm{I}\frac{1+sT_\mathrm{I}}{sT_\mathrm{I}}$
Crossover frequency	$f_\mathrm{V} = \frac{f_\mathrm{I}}{10} = \frac{f_\mathrm{s}}{100}$	$f_\mathrm{I} = \frac{f_\mathrm{s}}{10}$
Proportional gain	$K_\mathrm{V} = 2\pi f_\mathrm{V} C$	$K_\mathrm{I} = 2\pi f_\mathrm{I} L$

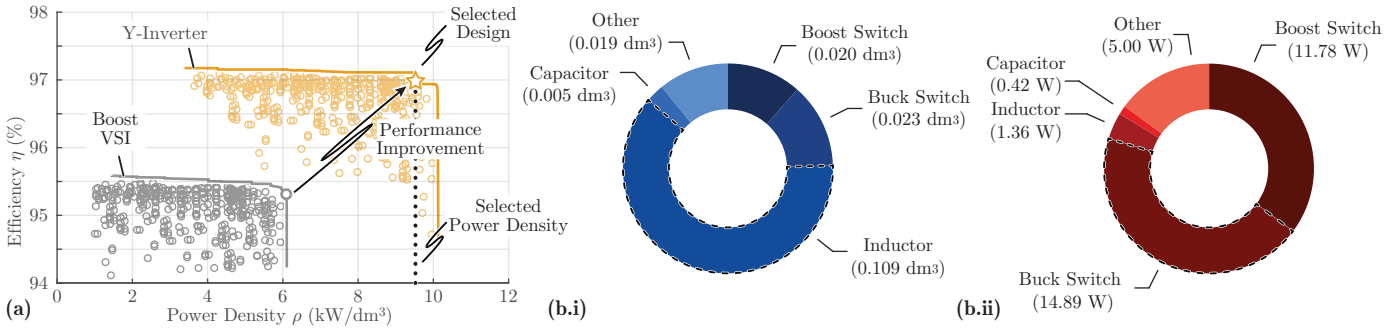

Fig. 6: In **(a)** the efficiency (η) power density (ρ) Pareto optimization results for the Y-inverter are compared against the performance of the conventional cascaded boost VSI topology shown in **Fig. 1(b)**. Two benchmark designs are indicated on the $\eta - \rho$ performance space corresponding to the conventional boost VSI and the Y-inverter concepts in order to highlight the performance difference. The specifications of those designs are given in **Tab. IV**. The break-down of the volume and the losses corresponding to the Y-inverter is visualized in **(b.i)** and **(b.ii)** respectively.

of the boost bridge-leg to 1, while the duty cycle d_A of the buck bridge-leg can vary freely in $[0, 1]$ interval. Thereby the inductor current is controlled exclusively by means of bridge-leg A. On the contrary during boost operation, where $u_\mathrm{am} + u^*_\mathrm{La} > U_\mathrm{in}$ (cf. **Fig. 2(a.ii)**), bridge-leg B (d_B) is responsible for controlling the inductor current while d_A is automatically clamped at 1 by the limiter of the buck branch shown in **Fig. 4(iv)**. The transition between the buck and the boost modulation branches is seamless.

In order to validate the proposed control strategy, a co-simulation is built within a Matlab-Simulink framework employing the Y-inverter, a static machine model and a time-discrete version of the controller shown in **Fig. 4**. The main Y-inverter waveforms, extracted from the simulation, are plotted in **Fig. 5**.

IV. Multi-Objective Optimization

In order to quantify the Y-inverter performance in terms of efficiency η and power density ρ, a multi-objective optimization routine is performed. The extracted results are then compared against the respective performance of a conventional cascaded boost VSI (cf. **Fig. 1(b)**) designed for the same specifications of **Tab. II**. There are multiple degrees of freedom in the design of the power electronics system: different abstract electrical parameters such as switching frequency and passive component values [22] can be selected, while numerous component physical implementation options exist for inductive components (e.g. core shape, core material, winding type) [23] and semiconductor devices (e.g. chip area, technology) [24], [25]. For each possible converter design, the volume and loss contributions of all the employed components are added yielding the efficiency and power density of the total converter system. By iterating this process for all the possible component combinations, the complete design space is mapped into the two dimensional performance space $\{\eta, \rho\}$. Based on the obtained performance space the Pareto-optimal designs can be identified and the associated trade-offs can be determined. Details on the models employed in the optimization and the optimization algorithm are omitted here for the sake of brevity.

The $\eta - \rho$ Pareto limits of the two converter options (i.e. boost VSI and Y-inverter) are depicted in **Fig. 6(a)**, where certain performance trends can be identified. The boost VSI exhibits an acceptable efficiency of 95.5%, since the boost DC/DC converter and the DC/AC inverter stages are decoupled and can be operated in an optimal fashion. However, the boost VSI solution quickly reaches a power density threshold at $6\,\mathrm{kW/dm^3}$ due to the volume contribution related to the DC/DC stage. At the nominal operating point, where the boost stage must step-up the FC voltage to the greatest degree, especially the boost inductor is exposed to large voltage-time areas and hence is rather bulky. Moreover, the boost type DC/DC converter provides a DC voltage which is above or equal to the maximum FC voltage with a twofold effect on the system: Power semiconductors featuring a high blocking voltage must be employed for the inverter stage with inferior figures of merit and hence higher losses. A motor with EMF compatible with the respective high DC link voltage must be employed, thus only a high voltage motor (i.e. $50\,\mathrm{V_{RMS}}$ phase voltage) can be driven by the boost VSI topology.

The Y-inverter breaks through the efficiency barriers of traditional systems, i.e. reaches 97.2% efficiency, while maintaining a very high power density of $10\,\mathrm{kW/dm^3}$, because it allows for

TABLE IV: Specifications of the Y-inverter hardware prototype and the boost VSI benchmark design that are highlighted in **Fig. 6(a)**. The current stresses of the main converter components, i.e. semiconductor devices, inductors and DC capacitors are provided for the nominal power operating point of $P = 1\,\mathrm{kW}$. The notation of the different system components can be found in **Fig. 1(b),(c)** for the boost VSI and the Y-inverter respectively.

Converter Topology	Boost VSI	Y-Inverter
DC/AC stage		
f_s	$300\,\mathrm{kHz}$	$450\,\mathrm{kHz}$
$\mathrm{EMF}_{\mathrm{Ph,RMS}}$	$50\,\mathrm{V}$	$30\,\mathrm{V}$
$I_{\mathrm{T1,RMS}}$	$7.9\,\mathrm{A}$	$11.1\,\mathrm{A}$
$I_{\mathrm{T2,RMS}}$	$7.9\,\mathrm{A}$	$9.5\,\mathrm{A}$
$I_{\mathrm{T3,RMS}}$	-	$14.2\,\mathrm{A}$
$I_{\mathrm{T4,RMS}}$	-	$3.2\,\mathrm{A}$
L	$9.7\,\mu\mathrm{H}$	$3\,\mu\mathrm{H}$
$I_{\mathrm{L,Pk}}$	$18.2\,\mathrm{A}$	$28.5\,\mathrm{A}$
C	$3.8\,\mu\mathrm{F}$	$4.8\,\mu\mathrm{F}$
C_{DC}	$11.3\,\mu\mathrm{F}$	$23\,\mu\mathrm{F}$
$I_{\mathrm{C_{DC},RMS}}$	$3.9\,\mathrm{A}$	$4.9\,\mathrm{A}$
DC/DC Stage		
f_s	$300\,\mathrm{kHz}$	-
$I_{\mathrm{T'1,RMS}}$	$11.9\,\mathrm{A}$	-
$I_{\mathrm{T'2,RMS}}$	$12.2\,\mathrm{A}$	-
L'	$23.1\,\mu\mathrm{H}$	-
$I_{\mathrm{L',Pk}}$	$19.2\,\mathrm{A}$	-
C'_{DC}	$4.6\,\mu\mathrm{F}$	-
$I_{\mathrm{C'_{DC},RMS}}$	$1.3\,\mathrm{A}$	-
Total Converter		
Semiconductor nr.	8	12
Inductor nr.	4	3
DC capacitor nr.	2	1
ρ	$6\,\mathrm{kW/dm^3}$	$9.5\,\mathrm{kW/dm^3}$
η	95.5%	97.2%

a single-stage energy transfer (no DC/DC interface converter) and hence contains a minimum number of inductive components. Moreover, only one half-bridge per phase is switched, while the second half-bridge is clamped, a fact that limits the power semiconductor losses. On the other hand, compared to the conventional boost VSI converter, the Y-inverter offers more flexibility in the sense that it can be operated with both a low or a high voltage motor as a result of its inherent buck-boost capability. Therefore, the motor EMF is considered as a degree of freedom in the optimization procedure. A motor with $30\,\mathrm{V_{RMS}}$ phase voltage is best suited for the Y-inverter.

Based on the optimization results, a prototype design with a power density of $\rho = 9.5\,\mathrm{kW/dm^3}$ (accounting only for the boxed volume of components) and a calculated efficiency of $\eta = 97.2\%$ is selected. The corresponding breakdown of its volume and losses is presented in **Fig. 6(b.i)-(b.ii)**. The detailed specifications and component current stresses of the Y-inverter

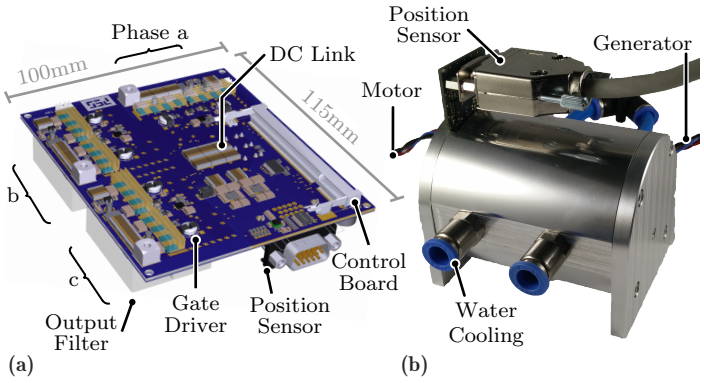

Fig. 7: Y-inverter prototype is presented in **(a)** and a custom designed ultra high-speed motor in **(b)**. The depicted systems will be used to experimentally evaluate the theoretical considerations in future publications.

prototype are provided in **Tab. IV** and are compared to the respective data of an optimized traditional boost VSI solution. A hardware demonstrator employing the latest generation of GaN devices is designed (cf. **Fig. 7(a)**) in order to validate the claimed performance benefits derived from the Y-inverter. The achieved hardware prototype power density is lower that the theoretically calculated values i.e. $\rho \simeq 7\,\mathrm{kW/dm^3}$ because of the non-ideal placement of the components and the air volume between them. The test setup in addition consists of a custom-built $300\,\mathrm{krpm}$ motor depicted in **Fig. 7(b)**. The associated controllers described in **Sec. III** are implemented within a digital signal processor, in order to drive the machine. The motor angle ϵ is provided by a hall sensor board that is directly mounted on the machine chassis. Experimental measurements will be provided in a future publication.

V. Conclusions

A promising three-phase inverter topology towards highly efficient low voltage inverters for fuel-cell applications is presented within this paper. The Y-inverter is comprised of three buck-boost DC/DC converters which are connected to a common star point. The potential of each output AC terminal is strictly defined with respect to the star point, allowing for a straightforward operation of each phase-leg as a conventional buck-boost DC/DC converter enabling a wide input and output voltage range. The Y-inverter also benefits from an integrated AC output filter hence it provides a smooth sinusoidal voltage to the motor. An appropriate control system is designed and analyzed while its functionality is verified by simulation results for a high-speed fuel-cell powered motor drive application. Finally the achievable efficiency and power density of the Y-inverter is determined through a comprehensive multi-objective

optimization and is compared against a traditional boost VSI solution. There, a clear comparative gain of 1.5% efficiency and $4\,\mathrm{kW/dm^3}$ power density in favor of the Y-inverter is deduced.

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