# A NOVEL SINGLE-SWITCH THREE-PHASE AC/DC BUCK-BOOST CONVERTER WITH HIGH-QUALITY INPUT CURRENT WAVEFORMS AND ISOLATED DC OUTPUT

# UN NOUVEAU CONVERTISSEUR AC/DC TRIPHASE BUCK-BOOST A UN SEUL COMMUTATEUR, AVEC FACTEUR DE FORME DU COURANT D'ENTREE ELEVE ET A SORTIE CONTINUE ISOLEE

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**Résumé**

Le présent exposé décrit un système convertisseur flyback AC-DC, à un interrupteur unique,triphasé. Le système opérant en mode discontinu est caractérisé par une structure simple des parties puissance et commande, par une faible distorsion du courant de réseau et par un comportement ohmique en mode fondamental du réseau et un potentiel de coupure de fréquence élevé de la tension de sortie régulée. Les relations entre la valeur de crête, de la valeur moyenne et de la valeur efficae, ainsi qu'entre la tension maximale de blocage des semi-conducteurs de puissance et les paramétres du circuit sont indiquées en plus de l'analyse du comportement en régime permanent. L'analyse théorique est vérifiée et confirmée par simulation numérique.

**Abstract**

In this paper a new three-phase single-switch AC-DC flyback converter system is presented. The system operates in the discontinuous mode. The simple structure of its power and control circuit, low mains current distortion and resistive fundamental behavior as well as the high-frequency isolation of the controlled output voltage have to be pointed out. Besides the analysis of the stationary operating behavior the dependencies of the peak values, average values and rms values of the device currents and of the maximum blocking voltages across the power electronic devices on the circuit parameters are given as analytic approximations. The theoretical analysis is verified by digital simulation.

## 1 Introduction

The topic of this paper is the development and analysis of a circuit concept for the realisation of the input unit of a unidirectional three-phase AC-DC converter. The converter shall be applied as power supply for an electronic control unit and be fed from a 115V, 400Hz three-phase AC system. Due to safety and systems aspects it has to be realised as two-stage energy converter [1]. The controlled output voltage of the rectifier input stage is converted by a DC-DC converter into the load voltage levels.

The basic development requirements which are relevant for the determination of the concept of the mains converter are defined as follows:

- high reliability (low complexity of the power and control units)
- high power density
- efficiency > 0.85
- wide input voltage range
- isolation of the AC and the DC sides
- total harmonic distortion factor < 0.05 (with the assumption of a purely sinusoidal and symmetric mains voltage system)
- fundamental displacement factor of the mains currents > 0.95
- current limited start-up, limitation of the input currents for transient mains overvoltages, limitation of the output current (overload protection)
- possibility of parallel operation of several converters.

For universal applicability of the AC-DC converter the DC link voltage is defined as $U_O$ = 280 V. This is approximately equal to the (ideal) mean output voltage for three-phase diode rectification of the 115V mains. Due to the high voltage level this can also be used for buffering of mains voltage outages with relatively low capacitances (minimisation of the size). The maximum output power of the mains converter is given by 690W.

In the following, in section 2 a new topology of a three-phase single-switch pulse rectifier system is developed via a three-phase extension of a DC-DC flyback converter. Section 3 treats the analysis of the operating principle of the system which forms the basis for the derivation of the equations for the stationary operation (section 4). With the assumption of high pulse frequency in section 5 analytic approximations of the current stresses (peak values, average values, rms values) on the system components are calculated and the blocking voltage stresses on the power electronic devices are given. The accuracy (or the limit of applicability) of the analytical approximations is derived via a comparison of the results of the calculation with the results of a digital simulation. Based on section 5, in section 6 the approach for dimensioning the converter is discussed. Furthermore, in this section the values for the component stresses resulting for the initially given operating parameters are summarised. These component stresses form the basis for the selection of the power electronic devices and can be used for an assessment of the converter within a concept evaluation.

Section 7 describes a simple extension of the converter structure which leads to an increase of the system efficiency and to a reduction of the blocking voltage stress of the power electronic devices. Finally, the advantages and disadvantages of the converter are compared and commented in section 8.

## 2 Converter Topologies

Due to requirements for low effects on the mains and for high power density, the mains converter has to be realised as pulse converter system. For high system pulse frequency the filtering effort is considerably reduced as compared to line-commutated systems [2]. Furthermore, the isolation can be included directly into the converter function and be achieved by a small size high-frequency transformer.

For the realisation of a three-phase pulse rectifier system one can apply (besides three-phase converter structures) also three single-phase AC-DC converters which are connected to a three-phase system [3]-[5].

The combination of three single-phase units makes possible the design of a fault-tolerant system due to the parallel operation on the output side of the three partial systems which are fed by the different mains phases. The dimensioning of the three converter modules has to be performed according to half of the output power of the overall system. This results in high reliability via the redundancy of one module. Furthermore, the modular design simplifies the system development and test. However, these advantages are paid for by a high device count for power and control circuits and by a reduction of the power density. A further disadvantage is the basically low utilisation of the phase modules which is due to the instantaneous phase power pulsating with twice the mains frequency. In the case at hand we want to prefer a direct three-phase realisation.

Based on [6] in [7]-[10] three-phase unidirectional pulse rectifier systems with high-frequency isolation are introduced. They show a very simple structure of the power and control circuits and satisfy the initially mentioned requirement regarding low system complexity. The converter topologies can be thought to be formed via a three-phase extension of basic DC-DC converter structures [7]. They are characterised by discontinuous input phase currents (three-phase single-switch discontinuous inductor current mode boost-type rectifier) or by discontinuous input phase voltages (three-phase single-switch discontinuous capacitor voltage mode buck-type rectifier). The mains voltage proportional control of the peak values of the converter input currents/voltages

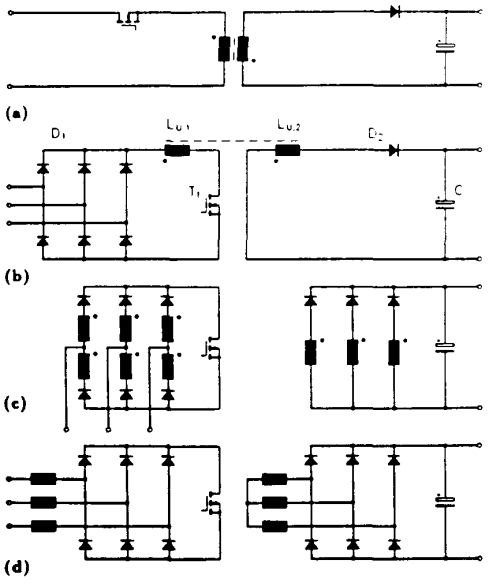


**Fig.1: Development of three-phase single-switch AC-DC flyback converter topologies (b), (c), (d) based on the basic structure of a DC-DC flyback converter (a); (c): three-phase single-switch discontinuous inductor current mode flyback rectifier (regarding the coupling of the partial windings cf. Fig.2).**

is achieved in analogy to the discontinuous operation of single-phase AC-DC pulse rectifiers having constant power transistor on-time directly by the mains voltages/currents (*automatic* current shaping, [11]). For series connection of a mains filter which suppresses input current harmonics with switching frequency, a considerable reduction of the effects on the mains is achieved, as compared to line-commutated rectification.

As a more detailed analysis of the system behavior shows, the harmonics content of the mains currents remaining after filtering the discontinuous input quantities is essentially determined by the voltage or current transformation ratio of the converter, however [7], [10], [12]. E.g., in three-phase single-switch discontinuous inductor current mode boost rectifier systems high amplitudes of low frequency harmonics are present in the mains current spectrum [12] for output voltages being low as compared to the amplitude of the line-to-line mains voltage. This leads to a small distortion factor of the mains currents only for high output voltages or for low input voltages, respectively.

Due to the required wide input voltage region one has to ask the question regarding the topologies of three-phase single-switch discontinuous-mode pulse rectifier systems with input voltage independent (ideal) sinusoidal input currents.

Discontinuous-mode single-phase AC-DC flyback converters show a purely sinusoidal shape of the filtered input currents for constant pulse frequency and constant on-time [13]. In connection with the simple structure of the power circuit and the full controllability of the power flow (as given for this converter type) this motivates the development of three-phase pulse rectifier systems based on the basic structure of a DC-DC flyback converter as described in the following.

Figure 1, (a) shows the power circuit of a DC-DC flyback converter which can be extended to a three-phase converter by connecting a three-phase diode bridge $D_1$ (cf. Fig.1, (b)) in series. However, low-frequency harmonics of high amplitude are present in the mains current of this system. This is the case because (due to the operating principle of the three-phase diode bridge) for transistor $T_1$ conducting only two phases conduct current. Therefore, the phase current shape shows $\pi/3$ wide intervals with zero current.

If one splits up $L_{U,1}$ to the valve branches (cf. Fig.1, (c)), the mains voltage system and the valve voltage system are decoupled and a simultaneous current flow in all phases is made possible. Due to splitting up the primary windings, the direction of the secondary current is not dependent on the direction of the primary phase currents. The basic secondary circuit structure of the DC-DC converter can therefore be maintained and the secondary circuits of the phases can be connected in parallel directly.

An AC-side arrangement (and split-up) of $L_{U,1}$ results in the converter structure shown in Fig.1, (d) [14] which makes possible (contrary to (c)) a combination of the phase energy storage devices to a three-phase system. For rectification of the AC currents being present on the secondary one has to connect the output diodes $D_2$ in a three-phase bridge configuration, however. Therefore, the function of the converter as flyback converter is linked to a minimum output voltage value defined by mains voltage and turns ratio.

For the case at hand, a closer analysis therefore can be limited to the circuit shown in Fig.1, (c), which will be called in the following three-phase single-switch discontinuous inductor current mode (DICM) flyback rectifier.

Remark: If one moves the power transistor $T_1$ instead of $L_{U,1}$ to the input of the three-phase bridge $D_1$, there follows a three-phase flyback converter structure which requires three turn-off power semiconductor devices. With regard to the desired minimum complexity, this variant (as analysed in [15]) and other variants of higher complexity (as given in the literature, e.g., in [16], [17]) will not be considered here.

## 3 Principle of Operation

In analogy to the three-phase single-switch discontinuous-mode pulse rectifier systems as given in the literature, the control of the system shown in Fig.2 may be performed in the stationary case with a pulse frequency $f_P$ and an on-time of the power transistor $T_1$ being constant within the mains period. A synchronisation of $f_P$ and mains frequency $f_N$ can be omitted for $f_P \gg f_N$. Due to the low-pass characteristic of the mains filter $L_N, C_N$ the mains voltage can be assumed to lie directly at the filter output.

For illustrating the operating principle Fig.3 shows the conducting states of the converter occurring during the pulse period $t_p \in [0, T_P]$. ($t_p$ denotes a local time running within the considered pulse period.) Concerning the mains phase voltages being approximately constant within the pulse period we assume $u_{N,R} > 0$, $u_{N,T} \leq u_{N,S} \leq 0$ (being valid in an interval of $\pi/6$ of

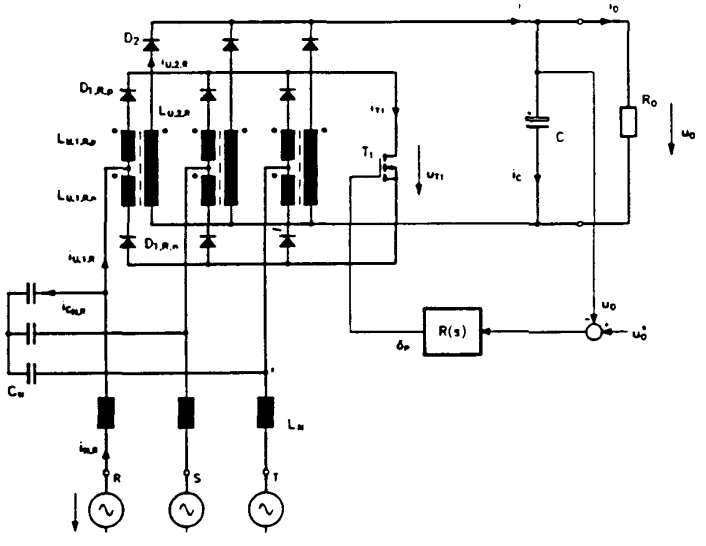


**Fig.2: Basic structure of the power and control circuits of a three-phase single-switch DICM flyback rectifier; the feeding mains is replaced by a Y-connection of ideal voltage sources $u_{N,(RST)}$; filtering of the high-frequency spectral components of the discontinuous converter input currents $i_{U,1,(RST)}$ by a mains filter $L_N$, $C_N$; $R_O$: load resistance (e.g., voltage dependent input impedance of a DC-DC converter connected to the output of the pulse rectifier); in the stationary case the control of the power transistor $T_1$ is performed by a constant pulse frequency $f_P$ and by a constant relative turn-on time $\delta_P$ being set by an output voltage control circuit.**

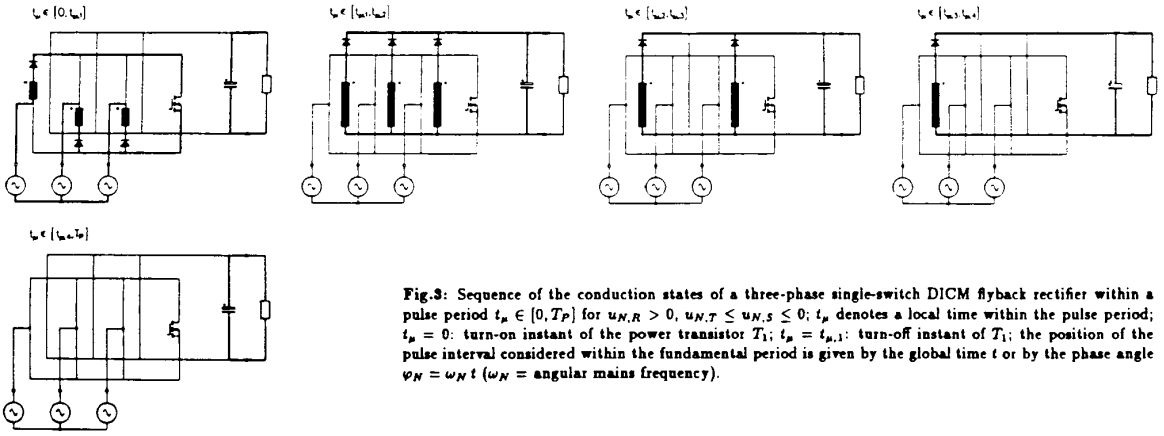

**Fig.3:** Sequence of the conduction states of a three-phase single-switch DICM flyback rectifier within a pulse period $t_\mu \in [0, T_P]$ for $u_{N,R} > 0$, $u_{N,T} \leq u_{N,S} \leq 0$; $t_\mu$ denotes a local time within the pulse period; $t_\mu = 0$: turn-on instant of the power transistor $T_1$; $t_\mu = t_{\mu,1}$: turn-off instant of $T_1$; the position of the pulse interval considered within the fundamental period is given by the global time $t$ or by the phase angle $\varphi_N = \omega_N t$ ($\omega_N$ = angular mains frequency).

the mains fundamental period, (cf. Fig.5, (a)) ). Due to the phase-symmetric structure of the converter and due to the assumption of a purely sinusoidal voltage system the analysis of this angle interval derermines the system behavior within the entire fundamental period. **Figure 4 shows the local** shape of the phase currents being related to Fig.3.

Before turning on $T_1$ we have according to the operation of the system in discontinuous mode: $i_{U,1,(RST)} = i_{U,2,(RST)} = 0$. $T_1$ is turned on at $t_\mu = 0$. The DC side short-circuit of the bridge circuit consisting of $L_{U,1,(RST),\sigma} = L_{U,1,(RST),\sigma}$ (primary inductances of the phase transformers) and $D_{1,(RST),\sigma}$, $D_{1,(RST),\sigma}$ (diodes on the primary side) results in a rate of rise of the input currents being defined by the instantaneous values of the mains phase voltages. For constant turn-on time therefore in the turn-off instant $t_\mu = t_{\mu,1}$ of $T_1$ phase current values are obtained which vary sinusoidally over the mains period and which are proportional to the respective phase voltage. The demagnetisation of the transformers is performed via the secondary diodes $D_{2,(RST)}$. For discontinuous mode we have to guarantee $t_{\mu,4} \leq T_P$ according to Fig.4. A stress on $T_1$ caused by reverse recovery currents of the diodes $D_{2,(RST)}$ is avoided therefor

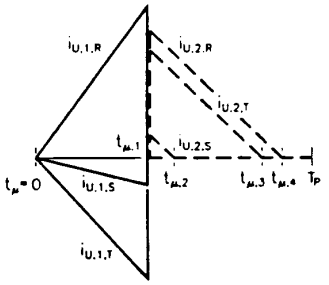


**Fig.4:** Time characteristic of the converter input currents $i_{U,1,(RST)}$ and of the output currents $i_{U,2,(RST)}$ (dashed) within a pulse period for $t_\mu \in [0, T_P]$ for $u_{N,R} > 0$, $u_{N,T} \leq u_{N,S} \leq 0$ (cf. Fig.3); $t_{\mu,4} - t_{\mu,1}$: demagnetisation interval; parameter: $\frac{N_2}{N_1} = 1.2$.

Because the demagnetisation interval does not influence the mains current shape there remain purely sinusoidal mains currents which are in phase with the mains voltages. This is due to the sinusoidal envelope of the converter input currents $i_{U,1,(RST)}$ (cf. Fig.5, (b)) for ideal filtering of the harmonics with pulse frequency (cf. section 4.2). The system shows therefore (contrary to, e.g., three-phase DICM boost-type rectifiers) low effects on the mains independently of the voltage transfer ratio as well as a high power factor and resistive mains behavior. Furthermore, independently of the output voltage level full controllability of the power flow is given. This makes a limitation of the start-up current or an overcurrent protection easily realisable.

The advantages of the proposed concept mentioned so far have to be compared to the basic disadvantages being caused by the high current stresses on the devices due to the flyback converter principle and by a high filtering effort. In order to establish an evaluation basis concerning the applicability of the proposed converter system (going beyond the special application described here) and concerning a comparison with alternative concepts, we therefore want to determine in the following (after formulation of the basic equations

# 4 System Analysis

## 4.1 Assumptions

For the analysis of the stationary operating behavior the following assumptions are made in order to concentrate on the essential:

- purely sinusoidal, symmetric mains voltage system $u_{N,(RST)}$,
- purely sinusoidal mains currents (fundamental; switching frequency components of $i_{U,1,(RST)}$ are suppressed – ideal mains filter),
- the voltage ripple of the filter capacitors $C_N$ may be neglected,
- fundamental components of the voltage across $L_N$ may be neglected as compared to the amplitude $\hat{U}_N$ of the mains phase voltages; accordingly, the filter capacitor voltage is assumed impressed and set equal to the mains voltage,
- ideal magnetic coupling of the two primary windings and of the secondary winding for each phase,
- constant output voltage $u_O$,
- constant load (output) current $i_O$,
- $f_P > 200 f_N$ or $T_P \ll T_N$, respectively (mains phase voltages approximately constant within a pulse period),
- ideal system components (especially: neglection of the system losses, switching times etc.).

Of special importance is the assumption of a pulse frequency being sufficiently higher than the mains frequency. As described in section 5.1, this assumption makes possible a very exact approximation of the current stresses on the system components being relevant for dimensioning. Therefore, one can omit a very time-consuming determination of the device stresses by digital simulation. Furthermore, the knowledge of analytical relationships has (as compared to a system analysis by digital simulation whose validity is limited to discrete parameter sets) the advantage of a deeper insight into the system behavior and allows therefore an immediate conclusion regarding the influence of parameter variations on the device stresses.

## 4.2 Basic Equations

The analysis of the basic equations of the stationary operating mode is performed for constant $f_P$ and constant local on-time $t_{\mu,1}$ of $T_1$. Furthermore, only discontinuous mode is assumed as well as a symmetric split-up of the primary windings of the transformers according to

$$L_{U,1,(RST),\sigma} = L_{U,1,(RST),\sigma} = L_{U,1} \,. \tag{1}$$

For the relation of primary and secondary inductances we have

$$\frac{L_{U,1}}{L_{U,2}} = \frac{N_1^2}{N_2^2} \tag{2}$$

according to the assumption of ideal coupling. Based on a symmetrical, purely sinusoidal mains voltage system there follows for the instantaneous input phase currents at turn-off instant $t_\mu = t_{\mu,1}$ of $T_1$ (cf. Fig.4):

$$\begin{aligned} i_{U,1,t_\mu 1,R} &= \hat{U}_N \frac{t_{\mu,1}}{L_{U,1}} \cos(\varphi_N) \\ i_{U,1,t_\mu 1,S} &= \hat{U}_N \frac{t_{\mu,1}}{L_{U,1}} \cos(\varphi_N - \frac{2\pi}{3}) \\ i_{U,1,t_\mu 1,T} &= \hat{U}_N \frac{t_{\mu,1}}{L_{U,1}} \cos(\varphi_N + \frac{2\pi}{3}) \,. \end{aligned} \tag{3}$$

There, the position of the considered pulse interval within the fundamental period $T_N$ is defined by the angle

$$\varphi_N = \omega_N t \ . \tag{4}$$

The mains currents remaining after (ideal) filtering of the spectral components with pulse frequency (cf. $L_N, C_N$ in Fig.2) of the discontinuous input currents $i_{U,1,(RST)}$ now follow directly via averaging related to the pulse period as:

$$\begin{aligned} i_{N,R} &= \frac{1}{2}\hat{U}_N \frac{T_P}{L_{U,1}}\delta_P^2 \cos(\varphi_N) \\ i_{N,S} &= \frac{1}{2}\hat{U}_N \frac{T_P}{L_{U,1}}\delta_P^2 \cos(\varphi_N - \frac{2\pi}{3}) \\ i_{N,T} &= \frac{1}{2}\hat{U}_N \frac{T_P}{L_{U,1}}\delta_P^2 \cos(\varphi_N + \frac{2\pi}{3}) \ , \end{aligned} \tag{5}$$

where

$$\delta_P = \frac{1}{T_P} t_{\mu,1} \tag{6}$$

denotes the relative turn-on time or the duty cycle of the power transistor $T_1$. As already described in section 3, no low-frequency effects of the system on the mains occur. The amplitude of the (ideally) purely sinusoidal mains currents being in phase with the mains phase voltages is given with Eq.(5) as:

$$\hat{I}_N = \frac{1}{2}\hat{U}_N \frac{T_P}{L_{U,1}}\delta_P^2 \ . \tag{7}$$

Regarding the loading of the mains the converter therefore can be assumed to be replaced by equivalent resistances

$$R_N = 2\,\frac{L_{U,1}}{T_P}\delta_P^{-2} \tag{8}$$

(for Y-connection) which can be set by the relative turn-on time $\delta_P$ of $T_1$.

Remark: This defining equation of an input equivalent resistance is also given in an identical form for DICM DC-DC (cf. [18], Eq.(13)) and for single-phase AC-DC flyback converters (cf. [11], Eq.(13.28)) and is valid approximately also for three-phase single-switch DICM boost-type input rectifiers (cf. [7], Eq.(16) or [12], Eq.(38)).

Considering the equality of input and output power (because the system has been assumed loss-free) we have for the converter output power:

$$P_O = \frac{3}{4}\hat{U}_N^2 \frac{T_P}{L_{U,1}}\delta_P^2 \ . \tag{9}$$

For ideal magnetic coupling and for discontinuous operation the entire magnetic energy being stored at instant $t_\mu = t_{\mu,1}$ in the primary inductances is transferred into the secondary within each pulse period. The power flow as averaged over one pulse period therefore is not influenced by the value of the output voltage $u_O$ and has the time-constant value

$$p_{O,avg} = P_O \tag{10}$$

for the stationary case. The system shows a constant-power behavior on the output side being also characteristic for single-phase AC-DC flyback converters operating in discontinuous mode [19]. One has to point out, however, that in the case at hand (contrary to single-phase systems) also for highly dynamic output voltage control no low-frequency distortion of the input current shape occurs. This is due to the time-constant (average) power flow for constant turn-on time.

As shown in the following section, besides the output current

$$I_O = \frac{P_O}{U_O} \tag{11}$$

and the duty ratio $\delta_P$ of $T_1$ the global maximum value of the transistor current

$$I_{T1,max} = \hat{U}_N \frac{T_P}{L_{U,1}}\delta_P \tag{12}$$

and the global maximum value of the output diode current

$$I_{D2,max} = I_{T1,max}\frac{N_1}{N_2} \tag{13}$$

are of paramount importance regarding the current stress on the system components.

Remark: In this paper, a global maximum value denotes the maximum of a signal characteristic within the fundamental period. This maximum value has to be distinguished from a local maximum value being present within a pulse interval. E.g., the current values $i_{U,1,\mu 1,(RST)}$ given in Eq.(3) represent local maximum values of the input current shape.

For the relation of the amplitude of the mains current fundamental and the maximum transistor current there follows with Eqs.(7, 12):

$$\frac{I_{T1,max}}{\hat{I}_N} = 2\delta_P^{-1} \ . \tag{14}$$

Therefore, there results, e.g., for $\delta_P = 0.5$ a current stress on $T_1$ being four times the peak value of the mains current fundamental. This clearly points out the high current stress on the devices characterising the discontinuous mode of a flyback converter.

For the (global) maximum duration of the current flow within a pulse interval there follows:

$$T = t_{\mu,4,max} = t_{\mu,1} + \Delta t_{\mu,41,max} = t_{\mu,1}(1 + \frac{\hat{U}_N}{U_O}\frac{N_2}{N_1}) \tag{15}$$

where

$$\Delta t_{\mu,41,max} = \frac{\hat{U}_N}{U_O}\frac{N_2}{N_1} t_{\mu,1} \tag{16}$$

denotes the maximum duration of the demagnetisation phase. For discontinuous mode we have to guarantee therefore:

$$T_P \geq T \ . \tag{17}$$

# 5 Component Ratings

For dimensioning and determination of the application region of the system especially the current and voltage stresses on the power electronic devices as well as of the passive components are of interest. The current and voltage characteristics to be analysed for the calculation of the component stresses are shown in Fig.5 (c), (d), (e), (f) with the exception of the mains filter and the output capacitor currents.

The calculation of the dependencies of device stresses being relevant for dimensioning (current and blocking voltage peak values, current average and rms values) on the system parameters (input voltage, output voltage, output power, turns ratio, pulse frequency etc.) as simple analytic approximations is the topic of the following sections.

## 5.1 Analysis Method

The basis of the calculation method is a quasi-continuous analytical approximation of the discontinuous system behavior [20], [21], being defined by averaging the quantities over a pulse period. The knowledge of the characteristic of a time function $i_i(t_\mu)$ within one pulse period $t_\mu \in [0, t_\mu]$ is replaced there by the (discrete) quantities which can be denoted as local mean value

$$i_{i,a\,v} = \frac{1}{T_P}\int_0^{T_P} i_i(t_\mu)\,dt_\mu \tag{18}$$

and local rms value:

$$i_{i,rms}^2 = \frac{1}{T_P}\int_0^{T_P} i_i^2(t_\mu)\,dt_\mu \ . \tag{19}$$

(Remark: the local rms value corresponds to a discrete time function having equal loss.) If these local mean values now are related to the position $\varphi_N$ (or to the global time $t = \omega_N^{-1}\varphi_N$) of the pulse interval within the fundamental period $T_N$, then there is defined a continuous (global) time characteristic of the local mean value and of the local rms value. By a second averaging related to the fundamental period

$$I_{i,avg} = \frac{1}{2\pi}\int_0^{2\pi} i_{i,avg}(\varphi_N)\,d\varphi_N \tag{20}$$

$$I_{i,rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} i_{i,rms}^2(\varphi_N)\,d\varphi_N \tag{21}$$

there follow accordingly directly the characteristic quantities global mean value and global rms value which characterise the component stresses.

In connection with a minimisation of component size and weight of the magnetic devices one has to aim in a practical realisation, by all means, for $f_P \gg f_N$. Because in the discontinuous mode a transistor stress by reverse recovery currents of the output diodes $D_2$ is avoided, $f_P \geq 200 f_N$ seems to be obtainable in the case at hand. As a digital simulation based on the assumptions made in section 4.1 shows, the derivations of the analytical expressions from exact results remain below 2% there. Therefore, the calculation results given in the following can be used as basis for dimensioning.

## 5.2 Characteristic Current Values of the Devices

**Mains filter capacitance $C_N$:**

$$I_{CN,rms}^2 = \frac{1}{6}(1 - \frac{3}{4}\delta_P)\delta_P I_{T1,max}^2 \tag{22}$$

$$I_{CN,max} = I_{T1,max} - \hat{I}_N \tag{23}$$

**Transformer $L_{U,1,p}, L_{U,1,s}, L_{U,2}$:**

**primary:**

$$I_{U,1,p,max} = I_{U,1,s,max} = I_{D1,max} \tag{24}$$

$$I_{U,1,p,rms} = I_{U,1,s,rms} = I_{D1,rms} \tag{25}$$

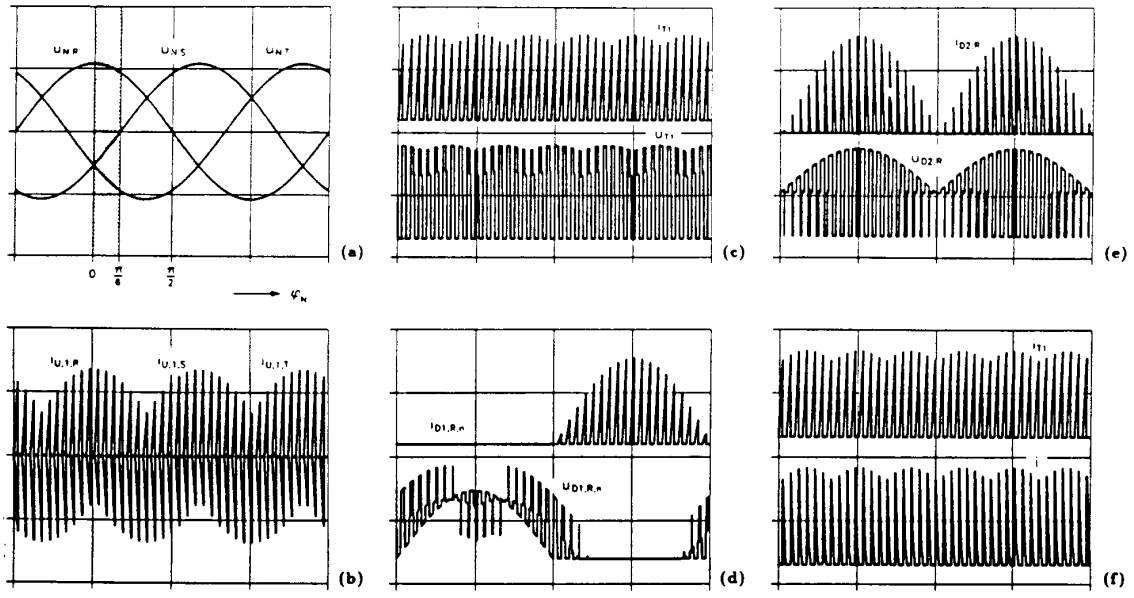


**Fig.8:** Digital simulation of a three-phase single-switch DICM flyback rectifier operating with constant switching frequency $f_P$ without mains filter $L_N$, $C_N$ connected in series based on the assumptions made in section 4.1; turn-on time $t_{p,1}$ of $T_1$ constant within the fundamental period; representation of one fundamental period $T_N$; the angle interval $\varphi_N \in [0, \frac{\pi}{6}]$ considered for the analysis of the system behavior (cf. section 3 is marked in (a) by the dotted area; (a): mains phase voltages $u_{N,(RST)}$ (150V/div); (b): converter input currents $i_{U,1,(RST)}$ (10A/div); (c): transistor current $i_{T1}$ (10A/div) and transistor blocking voltage $u_{T1}$ (400V/div); (d): primary diode current $i_{D1,R,n}$ (10A/div) and diode blocking voltage $u_{D1,R,n}$ (300V/div); (e): secondary diode current $i_{D2,R}$ (5A/div) and diode blocking voltage $u_{D2,R}$ (400V/div); (f): current $i$ feeding the output capacitor and transistor current $i_{T1}$, (10A/div); parameters: $P_O = 800$W, $U_{N,rms} = 115$V, $f_N = 400$Hz, $U_O = 280$V, $\frac{N_1}{N_2} = 0.57$, $L_{U,1} = 0.36$mH, $L_{U,2} = 1.12$mH, $f_P = 1/T_P = 15.6$kHz, $t_{p,1} = 30.8\mu$s.

secondary:

$$I_{U,2,max} = I_{D2,max} \quad (26)$$

$$I_{U,2,rms} = I_{D2,rms} \quad (27)$$

**Diodes $D_1$:**

$$I_{D1,max} = I_{T1,max} \quad (28)$$

$$I_{D1,avg} = \frac{1}{3} I_{T1,avg} \quad (29)$$

$$I^2_{D1,rms} = \frac{1}{12} \delta_P I^2_{T1,max} \quad (30)$$

**Power Transistor $T_1$:**

$$I_{T1,max} = \hat{U}_N \frac{T_P}{L_{U,1}} \delta_P \quad (31)$$

$$I_{T1,avg} = \frac{3}{2\pi} \delta_P I_{T1,max} \quad (32)$$

$$I^2_{T1,rms} = \frac{1}{6}(1 + \frac{3\sqrt{3}}{2\pi}) \delta_P I^2_{T1,max} \quad (33)$$

**Diodes $D_2$:**

$$I_{D2,max} = I_{T1,max} \frac{N_1}{N_2} \quad (34)$$

$$I_{D2,avg} = \frac{1}{3} I_O \quad (35)$$

$$I^2_{D2,rms} = \frac{16}{27\pi} I_O I_{D2,max} \quad (36)$$

**Total current of the secondary diode branches:**

$$I_{max} = 2\, I_{D2,max} \quad (37)$$

**Output capacitance $C$:**

$$I^2_{C,rms} = \frac{8}{3\pi}(\sqrt{3} - \frac{1}{3}) I_O I_{D2,max} - I^2_O \quad (38)$$

$$I_{C,max} = I_{max} - I_O \quad (39)$$

## 5.3 Blocking Voltage Stress

**Power Transistor $T_1$:**

$$U_{T1,max,i} = \sqrt{3}\hat{U}_N + 2\frac{N_1}{N_2} U_O \quad (40)$$

The voltage value given here is related to ideal magnetic coupling ($k = 1$) of the primary and secondary, according to the assumptions made in section 4.1.

For non-ideal magnetic coupling

$$k = \sqrt{1 - \sigma}$$

of the primary and the secondary (the coupling of the two primary windings $L_{U,1,(RST),P}$ and $L_{U,1,(RST),n}$ is still assumed to be ideal) there occurs contrary to ideal coupling no immediate current commutation from $L_{U,1,(RST),P}$ or $L_{U,1,(RST),n}$ to $L_{U,2,(RST)}$ when turning off $T_1$. For limiting the blocking voltage one has to provide a circuit $U_L$ in parallel to $T_1$. Its function is illustrated by an avalanche-diode in **Fig.6**. Then a maximum blocking voltage stress on $T_1$ is fixed by

$$U_{T1,max} = U_L \,, \quad (41)$$

replacing Eq.(40). The length of the current commutation interval and, therefore, the power dissipated in $U_L$ are substantially influenced by the maximum blocking voltage stress. For maximising the system efficiency one has to aim for values of $U_L$ as high as possible, where the maximum transistor voltage has to be observed.

**Diodes $D_1$:**

The maximum blocking voltage stress can only be given as a worst-case estimate:

$$U_{D1,max} \leq \max \left( \begin{cases} \frac{3}{4}\hat{U}_N + \frac{1}{2}U_L \\ \sqrt{3}\hat{U}_N + \frac{1}{2}U_L - \frac{3}{2}k\frac{N_1}{N_2}U_O \\ \sqrt{3}\hat{U}_N + k\frac{N_1}{N_2}U_O \end{cases} \right) \quad (42)$$

This is due to the relatively complex blocking voltage characteristic for non-ideal coupling and limitation of the voltage accross $T_1$ (cf. Fig.5 (d), valid only for *ideal* coupling).

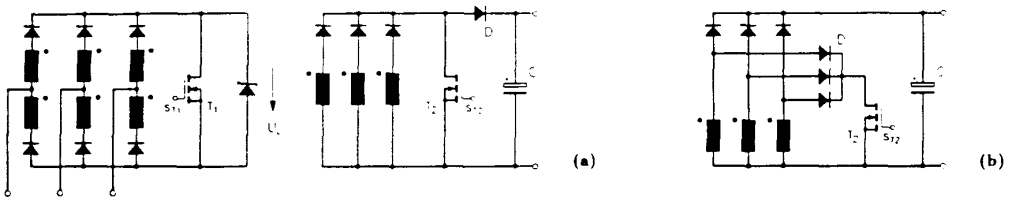


Fig.6: Reduction of the losses in the blocking voltage limitation circuit $U_L$ connected in parallel to $T_1$ (the losses occur due to non-ideal magnetic coupling of primary and secondary); (a): $T_2$ turned on in interval $t_\mu \in [t_{\mu,1}, t_{\mu,c} > t_{\mu,b}]$ (cf. Fig.7, (c)), diode $D$ prevents the shorting of the output voltage; (b): as (a), but avoidance of an increase of the conduction losses caused by diode $D$ (representation limited to the secondary systems part).

**Diodes $D_2$:**

For neglection of a small reduction of the blocking voltage stress for non-ideal coupling there follows:

$$U_{D2,max} = U_O + \frac{N_2}{N_1}\hat{U}_N \ . \tag{43}$$

# 6 Converter Design

In the following the procedure for dimensioning of the converter is outlined and an overview over the component stresses is given using a numerical example.

## 6.1 Procedure

Setting the turns ratio and the inductance of the primary of the transformer has to be done under consideration of the following: (1) blocking voltage stresses on the semiconductors occurring for maximum input voltage $\hat{U}_{N,max}$, (2) maintaining the discontinuous mode for minimum input voltage $\hat{U}_{N,min}$ and maximum output power $P_{O,max}$.

Regarding the blocking voltage stress one has to keep in mind especially the power transistor $T_1$. As outlined in connection with Eq.(41), one has to set the maximum blocking voltage $U_{T1,max,i}$ (occurring for ideal coupling) sufficiently below the maximum blocking voltage for non-ideal coupling (as defined by $U_L$). Therefore, there follows by transformation of Eq.(40) for the turns ratio:

$$\frac{N_1}{N_2} \le (U_{T1,max,i} - \sqrt{3}\hat{U}_{N,max})\frac{1}{2U_O} \ . \tag{44}$$

One has to point out that a reduction of $U_{T1,max,i}$ leads to an increase of the blocking voltage stress on the diodes $D_2$ according to

$$U_{D2,max} \ge U_O\left(1 + \frac{2\hat{U}_{N,max}}{U_{T1,max,i} - \sqrt{3}\hat{U}_{N,max}}\right) , \tag{45}$$

(cf. Eq.(43)). Using Eq.(15) and Eq.(17) there follows for guaranteeing the discontinuous mode for minimum input voltage:

$$\delta_{P,max} \le \left(1 + \frac{\hat{U}_{N,min}}{U_O}\frac{N_2}{N_1}\right)^{-1} \ . \tag{46}$$

Then, the inductance of the primary windings of the transformer results in (cf. Eq.(9)):

$$L_{U,1} = \frac{3}{4}\hat{U}^2_{N,min}\frac{T_P}{P_{O,max}}\delta^2_{P,max} \ . \tag{47}$$

The inductance of the secondary windings is given by the relation

$$L_{U,2} = L_{U,1}\frac{N_2^2}{N_1^2} \tag{48}$$

(cf. Eq.(2)).

After determination of the basic system parameters one can now (as shown in the following by using a numerical example) calculate the remaining dimensioning parameters by applying the relations compiled in sections 5.2 and 5.3.

## 6.2 Design Example

We assume (cf. section 1): $U_{N,rms}$ = 50 V ... 165 V
$f_N$ = 400 Hz
$U_O$ = 280 V
$P_{O,max}$ = 690 W ($P_{O,avg}$ = 640 W)
$f_P$ = 100 kHz ($T_P$ = 10 µs) .

The system efficiency to be expected is estimated as $\eta \approx 0.85$ in order to provide a sufficient safety margin. Therefore, $P_O$ = 810 W is the basis for dimensioning. For calculation of the maximum duty cycle the inclusion of a control margin can be omitted, therefore.

For the threshold level of the blocking voltage limitation circuit (defining the maximum voltage stress of $T_1$) we choose

$$U_L = 800\text{V}$$

or

$$U_{T1,max,i} = 600\text{V} \ ,$$

respectively. There, the realisation of $T_1$ by direct paralleling of a power MOSFET and of an IGBT (minimisation of the switching losses and the on-state losses with minimum control effort, [22]) is considered. The leakage of the transformer is estimated as

$$\sigma = 0.025 \ .$$

According to sections 6.1 and 5.3 there follows then:

$\frac{N_1}{N_2}$ = 0.35
$U_{D2,max}$ = 945 V
$U_{D1,max}$ = 606 V
$\hat{U}_{N,min}$ = 71 V : $\delta_{P,max} = 0.58$
$\hat{U}_{N,max}$ = 233 V : $\delta_{P,max} = 0.176$
$L_{U,1}$ = 15.5 µH
$L_{U,2}$ = 126.5 µH .

As mentioned already in section 4.2, the component current stress is essentially determined by the maximum values of the transistor current and the output diode current and by the duty ratio $\delta_P$. For the determination of the maximum stress on the AC-side components one has to consider the case of minimum input voltage (or maximum $\delta_P$, respectively), therefore.

Remark: Because the output power is determined directly by the maximum value of the transistor current according to

$$P_O = \frac{3}{4}\frac{L_{U,1}}{T_P}I^2_{T1,max} \tag{49}$$

(cf. Eqs.(9, 12)), for constant output power $I_{T1,max}$ and, therefore, the secondary currents are not influenced by the input voltage value. The current characteristic values of the DC-side devices are only dependent on the output power and not on the input voltage, therefore.

Via evaluating the relations given in section 4.2 and section 5.2 there follows for the current ratings:

Amplitude of the mains current fundamental:

$$\hat{I}_{N,max} = 7.6 \text{ A}$$

Mains filter capacitor $C_N$:

$I_{CN,rms}$ = 6.2 A
$I_{CN,max}$ = 19.0 A

Transformer inductances $L_{U,1,p}, L_{U,1,s}, L_{U,2}$:

Primary:

$I_{U,1,p,max} = I_{U,1,s,max}$ = 26.6 A
$I_{U,1,p,rms} = I_{U,1,s,rms}$ = 5.9 A

Secondary:

$I_{U,2,max}$ = 9.3 A
$I_{U,2,rms}$ = 2.3 A

Diodes $D_1$:

$I_{D1,max}$ = 26.6 A
$I_{D1,avg}$ = 2.5 A
$I_{D1,rms}$ = 5.9 A

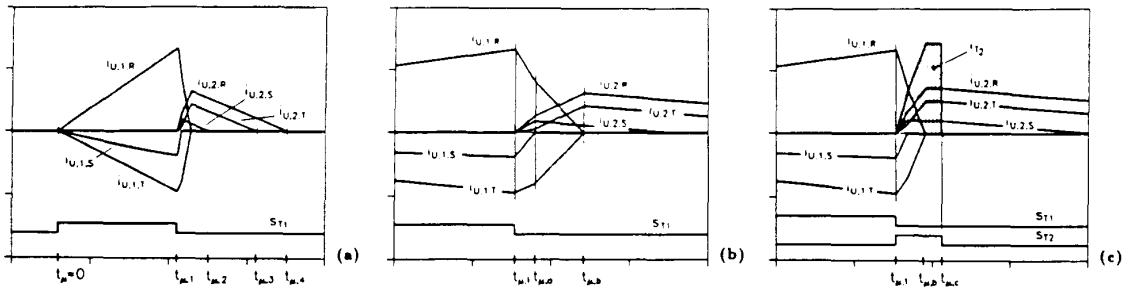


**Fig.7** : Digital simulation of the shapes of the input and output currents of the converter ($i_{U,1,(RST)}$ and $i_{U,2,(RST)}$) within a pulse period (cf. (a)); non-ideal magnetic coupling of $L_{U,1}$ and $L_{U,2}$; $s_{T1}$: switching function or control signal of $T_1$, respectively; $t_{\mu,1}$: turn-off instant of $T_1$; parameters: as Fig.5, but $\sigma = 0.0975$; $u_{N,R} > 0$, $u_{N,T} \leq u_{N,S} \leq 0$.

Power transistor $T_1$:

$$I_{T1,max} = 26.6\ A$$
$$I_{T1,avg} = 7.4\ A$$
$$I_{T1,rms} = 11.2\ A$$

Diodes $D_2$:

$$I_{D2,max} = 9.3\ A$$
$$I_{D2,avg} = 0.96\ A$$
$$I_{D2,rms} = 2.3\ A$$

Total current through diodes $D_2$:

$$I_{max} = 18.6\ A$$

Output capacitor $C$:

$$I_{C,rms} = 4.9\ A$$
$$I_{C,max} = 15.7\ A$$

Output current $I_O$:

$$I_O = 2.9\ A\ .$$

## 7 Efficiency Improvement

As mentioned in section 5.3 and as easily verifyable by digital simulation, the obtainable efficiency is influenced substantially by the difference $U_L - U_{T1,max,i}$, besides by the loss contributions of the semiconductors and the passive components. A high efficiency is inevitably linked to a high blocking voltage stress on $T_1$ (defined by $U_L$) and to low transformer leakage (connected with a high manufacturing effort).

A ficticious increase of $U_L$ (while avoiding an increase of the blocking voltage stress on $T_1$) can now be achieved by applying a second power transistor $T_2$ (on the secondary) and of an output diode $D$ (cf. Fig.6, left side). $T_2$ is turned on at turn-off instant of $T_1$ (cf. Fig.7, (c)). By shorting the secondary winding the transformatory coupling of a voltage into the primary (which would slow down the current commutation) is suppressed. Due to this, the current commutation interval is shortened and the losses in $U_L$ are reduced accordingly.

After turning off $T_2$ the magnetisation energy (stored in $L_{U,2,(RST)}$) is fed into to the output via diode $D$ which prevents shorting of the output voltage when $T_2$ is turned on. Due to its very short on-time one has to dimension $T_2$ only regarding the pulse current stress and a transistor with low average current carrying capability can be applied. The control of $T_2$ which is directly linked to the turn-off of $T_1$ furthermore allows a simple realisation of the control stage. Therefore, with a small increase of system complexity a significant converter efficiency improvement (or a reduction of the blocking voltage stress in $T_1$, respectively) is made possible.

(b): Current commutation from $L_{U,1,R,P}$, $L_{U,1,S,n}$, $L_{U,1,T,n}$ to $L_{U,2,(RST)}$ for $U_L = 800V$;

(c): as (b), but with power transistor $T_2$ on the secondary; $s_{T2}$: switching function of $T_2$, $s_{T2}$ marked by the dotted area; current commutation interval $t_\mu \in [t_{\mu,1}, t_{\mu,b}]$ significantly reduced as compared to (b), reduction of the limitation losses.

## 8 Conclusions

Based on the topology of a DC-DC flyback converter a new three-phase single-switch DICM rectifier system has been developed in this paper.

+ Ideally, complete avoidance of low-frequency effects on the mains (purely sinusoidal mains currents being in phase with the mains voltages),
+ simple structure of the power circuit and of the control circuit (constant pulse frequency and – for the stationary case – constant turn-on time of the power transistor allow the application of standard SMPS control ICs), possibility of sensing the output voltage to be controlled by a third transformer winding which also can be used for the internal supply of the system,
+ high-frequency potential separation between AC and DC sides (possibility of matching the input and output voltage levels and reduction of the component stress by proper choice of the turns ratio),
+ simple control behavior (corresponds to a DCIM DC-DC flyback system [23], [24] due to the time-constant average power flow (cf. Eq.(10))),
+ full controllability of the power flow (inrush-current limitation (start-up or transient overvoltages of the mains), output current limitation (load faults)),
+ low circuit effort when various potential separated output voltages are to be realised,
+ possibility of direct parallel operation of several converters.

- High peak current stress on the components (high conduction losses, especially if a MOSFET power transistor is used, high requirements regarding the ESR (equivalent series resistance) of the passive components (filtering and smoothing capacitors etc.) ),
- high blocking voltage stress on the power semiconductors,
- unidirectional magnetisation of the transformers (low utilisation of the cores),
- high filtering effort for avoiding conducted EMI (electromagnetic interference) – reduction of the power density of the system.

The advantages and drawbacks mentioned here correspond to a large extent to these of a DICM DC-DC flyback converter; an application of the system is especially of interest for low output power (<1kW) and low rated mains voltage.

Finally, there shall be pointed out that one can basically avoid low-frequency effects on the mains only for discontinuous mode of the system (when three-phase energy is transformed into DC energy and only a single controlled power electronic device is used). The simple system structure being paid for high current stress therefore (contrary to DC-DC converters) cannot be reduced by choosing the continuous mode.

### List of Symbols

| | |
|---|---|
| $C$ | output capacitor |
| $C_N$ | mains filter capacitor |
| $D$ | output diode |
| $D_1$ | diodes on the primary side |
| $D_2$ | diodes on the secondary side |
| $f_N$, $f_P$ | mains frequency, pulse frequency |
| $i$ | total current of the three secondary branches |
| $i_C$ | output capacitor current |
| $i_{CN}$ | current through the capacitors of the mains filter |
| $i_{D1}$ | current through $D_1$ (primary side) |
| $i_{D2}$ | current through $D_2$ (secondary side) |

| | |
|---|---|
| $i_{T1}$ | current through transistor $T_1$ |
| $i_{U,1.R}$, $i_{U,1.S}$, $i_{U,1.T}$ | input phase currents |
| $i_{U,1.R,p}$, $i_{U,1.S,p}$, $i_{U,1.T,p}$ | primary currents of the transformers (positive branches) |
| $i_{U,1.R,n}$, $i_{U,1.S,n}$, $i_{U,1.T,n}$ | primary currents of the transformers (negative branches) |
| $i_{U,2.R}$, $i_{U,2.S}$, $i_{U,2.T}$ | transformer secondary currents |
| $k$ | coupling factor between primary and secondary windings |
| $L_N$ | mains filter inductances |
| $L_{U,1}$ | inductance of a primary winding (positive or negative branch) |
| $L_{U,2}$ | inductance of a secondary winding |
| $N_1$ | number of turns of a primary winding |
| $N_2$ | number of turns of a secondary winding |
| $p_O$ | output power |
| $R_N$ | power-equivalent input resistance of the converter (Y-connection) |
| $t$ | (global) time (within a fundamental period) |
| $T$ | global maximum value of the sum of turn-on time of $T_1$ and duration of the demagnetisation phase |
| $T_1$ | main power transistor |
| $T_2$ | auxiliary power transistor for reduction of the losses in $U_L$ |
| $T_N$, $T_P$ | mains fundamental period, pulse period |
| $t_\mu$ | microscopic (local) time counted within a pulse interval |
| $U_L$ | threshold voltage of the voltage limitation circuit of $T_1$ |
| $u_{N,R}$, $u_{N,S}$, $u_{N,T}$ | mains phase voltages |
| $u_O$ | DC output voltage |
| $u_{T1,max}$ | maximum blocking voltage stress on $T_1$ for non-ideal magnetic coupling |
| $u_{T1,max,i}$ | maximum blocking voltage stress on $T_1$ for ideal magnetic coupling |
| $\delta_P$ | relative turn-on time of $T_1$, duty cycle |
| $\varphi_N$ | phase assigned to time $t$ ($\varphi_N = \omega_N t$) within the fundamental period |
| $\omega_N$ | mains angular frequency |
| $\sigma$ | transformer leakage coefficient (according to coupling $k$) |

| | |
|---|---|
| **lower case letters:** | characterising (local or global) time-dependent quantities |
| **upper case letters:** | characterising time-independent global mean or rms values |

**Indices:**

| | |
|---|---|
| **avg** | linear mean value |
| **i** | common counting subscript, ideal magnetic coupling |
| **max** | global maximum value |
| **min** | global minimum value |
| **n** | components between the phase inputs and the negative bus bar of the primary bridge |
| **p** | components between the phase inputs and the positive bus bar of the primary bridge |
| **(RST)** | phase R or phase S or phase T |
| **rms** | quadratic mean value |
| $t\mu i$ | time assignment of a local current value |
| $\mu$ | local time (within a pulse_period) |
| **1** | primary side |
| **2** | secondary side |

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