Sinusoidal Current Rectification and Ripple Cancellation in a Very WideThree Phase AC Input to Generate a Regulated DC Output

Lana Chaar, Girish Kamath, Ned Mohan
Electrical Engineering Department
University of Minnesota
Minneapolis, MN 55455
Tel: 1-612-625-3300

Chris P. Henze
Schott Power Systems, Inc.
1000 Parkers Lake Road
Wayzata, MN 55391
Tel: 1-612-475-1173

Johann W. Kolar
Technical University Vienna
Power Electronics Section 359.5
GusshausstraBe 27
Vienna A-1040, Austria
Tel: +43-1-58801-3728

Abstract

This paper represents a three-phase ac to dc rectifier topology that produces a regulated dc output voltage with low input current distortion. The novelty of this paper lies in the circuit which not only operates over a wide range of input voltages but also provides ripple cancellation in the rectifier current. Moreover, this converter utilizes the principle of third harmonic current generation and circulation through a zig-zag transformer in order to achieve power factor correction in the line current. Since simulation is a way to investigate the concept prior to any hardware realization, PSpice-based simulation has been carried out. Simulation results are presented that prove the concept.

I. Introduction

Three-phase power input presents challenges to power designers to reduce harmonic distortion and increase power factor in order to meet guidelines drafted by the IEEE-519 [1] and potentially by the IEC-555 [2]. Moreover there has been a requirement from power users to have a universal input machine [3] that is capable of operating over a wide range of input voltages. Allowing for a 20% variation in the input voltage, a universal input voltage range that a design must accommodate is 160 to 566 Vrms. It has been shown that ripple cancellation in the input current can be achieved by coupling parallel connected hysteresis-controlled Boost converters [5]. The main advantage of interleaving is that it increases the switching frequency without increasing the losses. It increases the power density without reducing the power efficiency. But one has to keep in mind that such a topology requires complex control. Thus a compromise between power density increase and system complexity will occur. This paper presents a novel topology that generates sinusoidal input current and ripple cancellation in the rectifier current, thus a low THD and a high power factor. The circuit consists of a three-phase diode bridge rectifier, a harmonic current circulation network, and two modulating circuits.

II. Description and Operation

The circuit under test consists of a three-phase diode bridge rectifier, a zig-zag transformer and two modulating circuits (fig. 1).

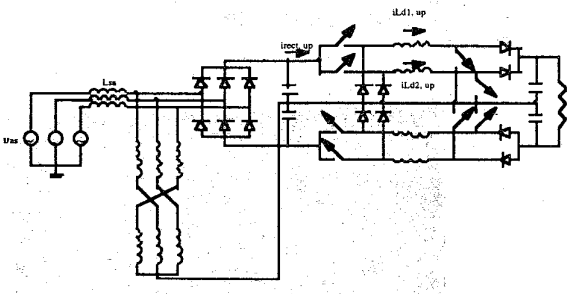

Fig. 1 Proposed Toplogy

The diode bridge and the transformer are connected to the utility. Each diode in the rectifier conducts for 120 degrees. The zig-zag transformer is used for third harmonic current circulation. The injection point is connected to the common node of the

nodulating circuits. Each of the modulating circuits consists of two parallel cascaded Buck and Boost converters. A single inductor is shared between one Buck converter and one Boost converter. The control circuit forces the current flowing in the inductor to have a dc component as well as a third harmonic component. Each modulated circuit has two switches, one for the Buck and one for the Boost. Each switch is controlled independently by means of constant band hyteresis controller. If the output voltage is above the instantaneous rectifier input voltage, the Boost converter operates to control the inductor current. Similasrly, when the output voltage is lower than the instantaneous rectifier input voltage, the Boost switch turns off and the Buck converter regulates the current. When the output voltage is between the maximum and minimum peaks of the three pulse rectifier input voltage, the circuit switches from Boost to Buck three times in a utility cycle. Such a topology is described in [6].

III. Ripple Cancellation Using a Bang-Bang Current Mode Control

Because of rapid changes in voltages and currents within a switching converter, power electronic equipment is a source of EMI [7]. There are various VDE, FCC and military standards that specify the maximum limit on the conducted EMI [8]. A major advantage of the proposed rectifier topology is that the high frequency switching takes place on the dc-side rather than the ac-side. Therefore, the filter for the EMI (which is equally, if not, more important issue as the low-order harmonic currents) is placed on the dc-side and does not draw line-frequency currents. This reduces the EMI filter.

Another method that would reduce it even further is by interleaving an n number of dc-dc converters as shown in fig.1. There is no theoretical limit for the number of interleaved stages, since eight stages were used in [9]. But the higher the interleaved number of stages, the more complicated system becomes. Thus, for a simpler system, two dc-dc converters are interleaved. In a fixed-frequency PWM operation, it is easy to provide a half-cycle phase shift between the two parallel stages in order to reduce the ripple. However, a disadvantage of interleaving [arallel connected fixed frequency PWM converters is to obtain a proper current sharing between the units. This problem can be avoided by usng hysteresis current control. Recently it has been shown that the necessary phase shift can also be provided rather easily in two parallel dc-dc converters operating in a bang-bang (tolerance band) current-mode control [5]. In this paper the above concept is applied to the converters in fig. 1, where the currents contain a dc component plus a third harmonic component.

IV. Control Circuit

The control circuit should be able to perform satisfactorily under all conditions of line and load. Moreover, parameters such as switching time delay, degree of coupling as well as voltage transformation are found to have a great effect on the behavior of the modulating circuit. Similarly, it has been shown that the paralleling of two partial systems results in a dramatic size reduction of the energy-storage inductors [4]. Therefore, for better utilization of the power handling capability of power semiconductor devices, a continuous inductor current control is needed. The coupling technique described in [5] is being used. Both types of converters are coupled via the control circuit. In both cases, whether being in the Buck mode of operation or in the Boost mode of operation, the control is very similar. All switches are controlled independently. As described in [6], in the first approach, where the inductor current in both modes of operation has a dc component and a third order harmonic component, is being used. It has been shown that in order to achieve the lowest THD in the input line current, the magnitude and phase of the third harmonic component of the reference current with respect to the dc current and phase voltage respectively are different depending on the mode of operation .

The reference currents for the upper and lower Buck Converters are shown in eq. (1) and (2) respectively:

$$I_{ref,up} = I_d + 0.85 * I_d * \sin(3 * \omega * t - 0.139) \quad (1)$$

$$I_{ref,lw} = I_d - 0.85 * I_d * \sin(3 * \omega * t - 0.139) \quad (2)$$

The reference currents for the upper and lower Boost converters are shown in eq. (3) and (4) respectively:

$$I_{ref,up} = I_d + 0.72 * I_d * \sin(3 * \omega * t - 0.245) \quad (3)$$

$$I_{ref,lw} = I_d - 0.72 * I_d * \sin(3 * \omega * t - 0.245) \quad (4)$$

In order to achieve ripple cancellation in the individual inductors, the reference current is modified by (1-k) where k is the coupling factor. This current is then compared with the actual current

that is also affected by the coupling factor as shown in the following expressions (eq. 5 & 6).

$$i_{L1,act} = i_{Ld1} - k * i_{Ld2} \quad (5)$$

$$i_{L2,act} = i_{Ld2} - k * i_{Ld1} \quad (6)$$

The resulting error signal is then supplied to a hysteresis element that would generate a gate signal (fig. 2).

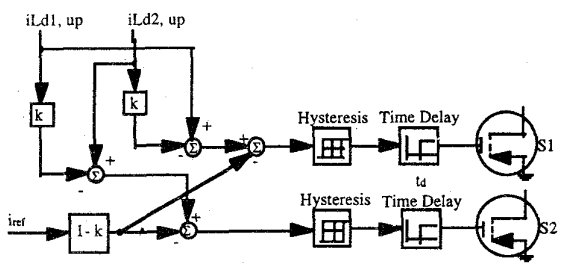

Fig. 2 Block Diagram of the Control Circuit

A dead time in any ways is neededto get a staggered switching of the parallel units. Since switching delay is found to have an effect on the control performance, the gate signal is then fed into a delay stage in order to determine the appropriate gate signals for the power transistors. In order to achieve the best result and to have a large ripple cancellation the time delays have to be equal in all cases.

In addition, in order to determine the mode of operation, a logic control is also required. It compares the output voltage with the instantaneous rectifier input voltage. If the output voltage is larger, the converter then acts as a normal Boost. If the output voltage is smaller, the converter then acts as a Buck converter.

V. Simulation Results

The proposed topology (fig. 1) is simulated using Pspice [10]. It is simulated with a three-phase, 60 Hz, 208 V (line-to-line) since both Buck and Boost modes are achieved. The load resistance was adjusted to achieve a power level of 3 kW. The dc reference current flowing in each inductor was chosen to be 8 A. A small capacitor of 1μf is placed at the input of the converters to provide circulation path for the third harmonic current. The inductor current is controlled using the fixed tolerance band control described above. The coupling factor k was chosen to be 0.25 (eq. 5 and 6). The circuit is simulated in the Buck - Boost mode of operation. Fig. 3 shows the upper rectifier voltage, the output voltage and the logic wich determines the mode of operation (Buck and Boost).

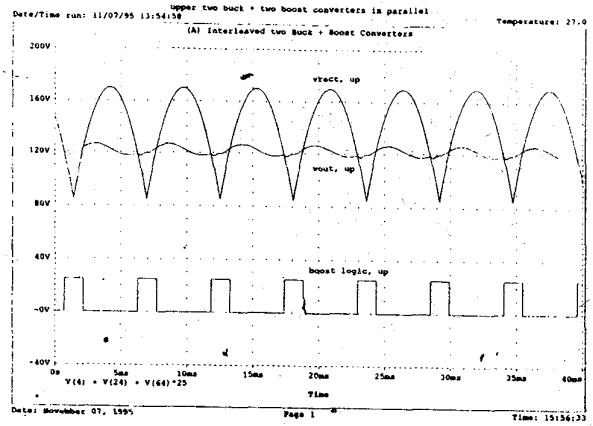

Fig. 3 Simulated output and input voltage of the upper dc-dc converter

The currents through the rectifier and upper inductor are shown in fig. 4.

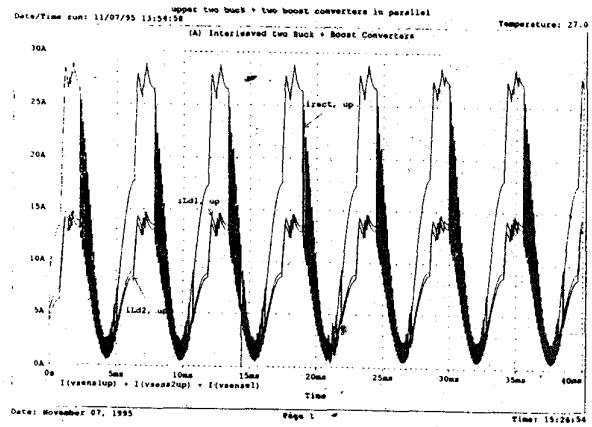

Fig. 4 Simulated rectifier and inductor Currents for the upper dc-dc converter

Fig. 5 shows one of the upper inductor currents with the corresponding reference currents in the Buck and Boost modes.

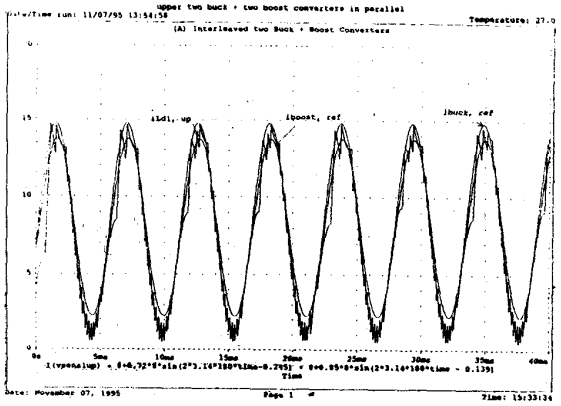

Fig. 5 Simulated reference and actual current through one of the upper inductors

Fig. 6 shows the phase difference in the upper inductor currents which causes a significant ripple cancellation, resulting in a much smoother current through the rectifier.

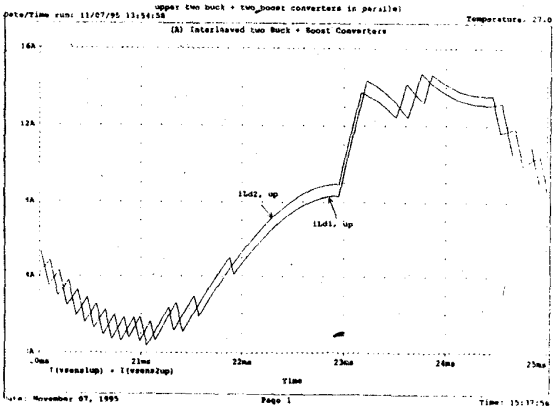

Fig. 6 Phase shift in the two upper inductor currents.

VI. Conclusion

A new circuit topology resulting in a sinusoidal input current rectification as well as a large ripple cancellation is presented. A description of the operation as well as the control circuit are given. PSpice simulation is carried out and proves the concept behind this topology. It shows that this circuit has the capability of operating over a wide range of input voltages achieving a low THD and producing a high power factor. Coupling and switching delays are used since they have a great effect on the circuit performance. Since two switches are used in each modulating circuit instead of one as in a Flyback converter, the voltage stress on the switch is reduced.

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