Analytical Calculation of the RMS Current Stress on the DC Link Capacitor of Voltage DC Link PWM Converter Systems

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Abstract. In this paper a simple analytical expression for the current stress on the DC link capacitor of a voltage DC link converter system, as caused by the load-side inverter is derived. There, a sinusoidal inverter output current and a constant value of the DC link voltage are assumed. The DC link capacitor current rms value is determined by the modulation depth and by the amplitude and the phase angle of the inverter output current. Despite the neglection of the output current ripple the results of the analytical calculation match very well with a digital simulation even if the output current ripple is relatively high as given, e.g., for low-frequency IGBT inverter systems. Thus, the approximation can advantageously be used for designing the DC link capacitor of PWM converter systems.

1 Introduction

Voltage DC link inverters are frequently fed via uncontrolled rectifier bridges from the single-phase or the three-phase mains. There, in the DC link usually aluminium electrolytic capacitors (connected in series and/or in parallel) are used

- to compensate the difference between the power requirement of the inverter (whose mean value is constant in steady state operation) and the output power of the input rectifier bridge varying with two or six times the mains frequency,
- to supply the input current of the inverter with pulse frequency,
- to reduce the spreading of current harmonics with pulse frequency into the mains,
- to supply transient power peaks and
- to protect the inverter from transient peaks of the mains voltage.

As explained, e.g., in [1] the operating voltage and especially the working temperature (in most cases the temperature of the capacitor-can is taken as reference value) take significant influence on the working life of electrolytic capacitors. If, e.g., an aluminium electrolytic capacitor is operated at 0.9 rated voltage the failure rate is lowered to 60% as compared to an operation at rated voltage (cf. Fig.7 in [1]). If the working temperature is lowered, the typical working life doubles for every 10°C below the rated temperature (Arrhenius Law, cf. p. 6 in [2]), as due to the lower temperature the diffusion of the gaseous parts of the electrolyte through the end seal is reduced and thus the drying-out of the capacitor is delayed.Therefore, in order to meet a demanded MTBF (Mean Time Between Failure) of the inverter besides selecting an appropriate rated voltage of the capacitor also the correct thermal design is of major importance.

The temperature being important for the working life is the can-temperature T_c (cf. Fig.8 in [3]). T_c is determined by the ambient temperature T_a and by the power dissipation in the capacitor as caused by the capacitor rms current $I_{C,\mathrm{rms}}$,

$$T_c = T_a + I_{C,\mathrm{rms}}^2 R_{\mathrm{ESR}} R_{th,c-a} \qquad (1)$$

(R_{ESR} denotes the equivalent series resistance of the capacitor which represents the sum of the frequency sensitive resistance of the oxid dielectric, the temperature sensitive resistance of the electrolyte and the relatively constant small contributions of the foil, the tabs and the terminals [3], [4]; $R_{th,c-a}$ denotes the heat transmission resistance between the capacitor can and the ambience).

Remark: In connection with Eq.(1) it is important to point out that an absolute maximum rating $I_{C,\mathrm{rms,max}}$ of the current stress on an electrolytic capacitor (as specified in the data sheet) is determined by the maximum allowable capacitor hot spot temperature $T_h > T_c$ (cf. Fig.8 in [3]). (With rising temperature the electric strength of the dielectric material is lowered and in addition chemical reactions between the electrolytic material and the aluminium oxide of the anode foil take place). Hence it is necessary to ensure in any case $I_{C,\mathrm{rms}} < I_{C,\mathrm{rms,max}}\{T_a\}$ even if the working life is not of special importance.

Therefore, for a correct thermal design of the capacitor the rms value $I_{C,\mathrm{rms}}$ of the DC link capacitor current is of paramount importance. The methods for calculating $I_{C,\mathrm{rms}}$ as proposed in the literature so far are based on a spectral analysis of the phase quantities (cf. [5], Fig.4(h) in [6], [7], [8], [9], [10], [11]) and/or rely on digital simulations. Besides the considerable amount of time required for establishing a simulation model one drawback of these methods is the missing possibility of demonstrating the influence of the operating point of the inverter (which is characterized by the modulation depth and by the amplitude and the phase displacement of the inverter output current and voltage fundamentals) on the capacitor current stress as the simulation is valid always only for a single set of operating parameters.

However, as shown in this paper, it is also possible to calculate the rms current of the DC link capacitor in analytically closed form in the time domain with sufficient accuracy.

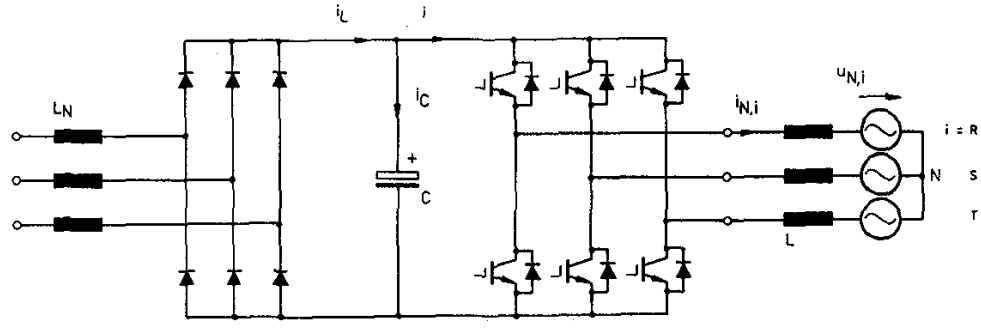

Fig.1: Basic structure of the power circuit of a voltage DC link converter. The AC machine fed by the inverter is considered by a simple equivalent circuit formed by leakage inductances L and machine counterelectromotive forces $\underline{u}_{N,i}$. The inductors L_N at the input (and/or an inductor at the output of the input rectifier bridge) have to be provided for limiting the peak values of the input currents and/or the effects on the mains and the current stress on the DC link capacitor C [12].

The effort necessary for designing the capacitor regarding the current stress thus is reduced to the evaluation of a simple mathematical expression. In addition the knowledge of the functional influence of the operating parameters on the capacitor current rms value can easily be used for determining the worst case current stress.

2 Basic Considerations

For preparing the analytical calculation of the capacitor current stress a brief review of the fundamentals of the inverter control and of the formation of the inverter input current i will be given in the following. Due to the symmetries of an ideal three-phase voltage system and due to the phase-symmetric structure of the converter power circuit there the analysis can be limited to a $\frac{\pi}{3}$-wide interval of the inverter output voltage fundamental period.

2.1 Space Vector Modulation

For stationary operation the reference value of the inverter output voltage can be represented by a space vector

$$\underline{u}_{U,(1)} = \hat{U}_U \exp(j\varphi_U) \qquad \varphi_U = \omega_N t \tag{2}$$

of constant magnitude $\hat{U}_U$ and constant angular speed $\omega_N = 2\pi f_N$ (f_N denotes the inverter output frequency). $\underline{u}_{U,(1)}$ is approximated within each pulse half period $t_\mu \in [0, T_P)$ by switching between the immediately neighbouring inverter output voltage space vectors. For the angle interval $\varphi_U \in (\frac{\pi}{3}, \frac{2\pi}{3})$ (*cf.* **Fig.2**) which is considered in the following we, therefore, have as switching state sequence

$$\begin{aligned} \ldots|_{t_\mu=0}(000) - (010) - (110) - (111)|_{t_\mu=\frac{1}{2}T_P} \\ (111) - (110) - (010) - (000)|_{t_\mu=T_P} \ldots \end{aligned} \tag{3}$$

where each inverter switching state is characterized by the triple (s_R, s_S, s_T) of the associated phase switching functions s_i, $i = R, S, T$. (We define $s_i = 1$ if the output voltage of phase i referred to the fictitious center point of the DC link is positive, $u_{U,i} = +\frac{1}{2}U_O$, and $s_i = 0$ if the output voltage of phase i is negative, $u_{U,i} = -\frac{1}{2}U_O$).

The relative on-times of the switching states (010) and (110),

$$\begin{aligned} \delta_{(010)} &= \frac{\sqrt{3}M}{2}\sin(\varphi_U + \frac{\pi}{3}) \\ \delta_{(110)} &= \frac{\sqrt{3}M}{2}\sin(\varphi_U - \frac{\pi}{3}) , \end{aligned} \tag{4}$$

can be determined by simple geometrical considerations (*cf.* Fig.2) and are defined by the location φ_U of the respective pulse half period within the fundamental period of the inverter output voltage and by the relative amplitude of the inverter output voltage fundamental and/or the modulation index

$$M = \frac{\hat{U}_U}{\frac{1}{2}U_O} \qquad M \in [0, \frac{2}{\sqrt{3}}] . \tag{5}$$

(With reference to the conditions given for a typical practical applications, the DC link voltage is assumed to be constant in the following.) In contrast the distribution of the total on-time of the non-voltage-forming (free-wheeling) switching states (000) and (111)

$$\delta_{(000)} + \delta_{(111)} = 1 - (\delta_{(010)} + \delta_{(110)}) \tag{6}$$

between the beginning and the end of each pulse half period can be freely chosen without influenzing the fundamental output voltage phasor $\underline{u}_{U,(1)}$. This degree of freedom

$$\delta_{(111),r} = \frac{\delta_{(111)}}{\delta_{(111)} + \delta_{(000)}} \qquad \delta_{(111),r} \in [0, 1] , \tag{7}$$

e.g., can be used for minimizing the rms value of the inverter output current ripple with switching frequency [13]. Alternatively, one also could use a suboptimal even distribution $\delta_{(000)} = \delta_{(111)}$ and/or $\delta_{(111),r} = 0.5$ under consideration of

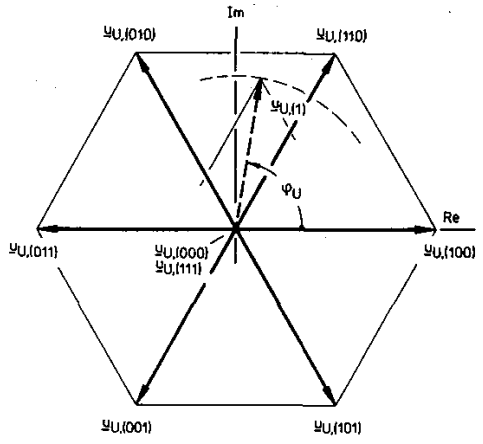

Fig.2: Space vectors of the inverter output voltage assigned to the active inverter switching states and to the non-voltage-forming switching states (000) and (111); furthermore shown: inverter output voltage reference value $\underline{u}_{U,(1)}$ which has to be formed in the average over a pulse half period of position φ_U; $\underline{u}_{U,(1)}$ is associated with the fundamentals of the pulse-width modulated inverter output phase voltages $u_{U,i}$, $i = R, S, T$.

a low realization effort of the inverter control [14].

2.2 Inverter Input Current Formation

As becomes immediately clear by considering the inverter bridge legs as two-pole switches between positive and negative DC link bus ($s_i = 1$ and/or 0) we have for the input current i of the inverter

$$i = s_R i_{N,R} + s_S i_{N,S} + s_T i_{N,T} \tag{8}$$

(for the considerations in this paper the dead-time interval which has to be considered for the gating of the transistors of a bridge leg in practice and the reverse recovery current of the freewheeling diodes which take minor influence on the shape of i [15], [16] are neglected). Dependent on the inverter switching state i is formed by segments of the inverter output phase currents $i_{N,i}$. E.g., for the switching state (010), the output terminal of phase S is connected to the positive DC bus and phases R and T are switched to the negative DC link rail, therefore, i and $i_{N,S}$ show identical time behavior (cf. **Fig.3**). For switching state (110) there results $i = -i_{N,T}$, where

$$i_{N,R} + i_{N,S} + i_{N,T} \equiv 0\,, \tag{9}$$

(as being valid due to the isolated neutral point N of the AC machine, cf. Fig.1) has to be considered. Only for the free-wheeling states (000) and (111) no current appears at the converter input. The distribution $\delta_{(111),\mathrm{r}}$ of the freewheeling states between the beginning and the end of a pulse half period therefore in a first approximation only takes influence on the position of the current conduction intervals $i = i_{N,S}$ and $i = -i_{N,T}$ within a pulse half period, but does not influence the shape of i in principle. (A further minor influence of $\delta_{(111),\mathrm{r}}$ on the shape of i is due to the ripple of the phase currents $i_{N,S}$ and $i_{N,T}$ which shows a different shape for different values of $\delta_{(111),\mathrm{r}}$).

3 Calculation of Average and RMS Value of the Inverter Input Current

For the sake of concentrating to the essentials a purely sinusoidal shape of the inverter output currents

$$\begin{aligned} i_{N,R,(1)} &= \hat{I}_N \cos(\varphi_U - \varphi) \\ i_{N,S,(1)} &= \hat{I}_N \cos(\varphi_U - \frac{2\pi}{3} - \varphi) \\ i_{N,T,(1)} &= \hat{I}_N \cos(\varphi_U + \frac{2\pi}{3} - \varphi) \end{aligned} \tag{10}$$

corresponding to a space vector

$$\underline{i}_{N,(1)} = \hat{I}_N \exp(j(\varphi_U - \varphi)) \tag{11}$$

is assumed in the following (φ denotes the phase displacement of the fundamentals of the inverter output voltage $\underline{u}_{U,(1)}$ and the inverter output current $\underline{i}_{N,(1)}$). This is equivalent to only considering the fundamentals of the phase currents which in a first approximation show a constant value within a pulse half period. The error caused by the neglection of the output current ripple will be calculated in section 5 and remains small even if the ripple amplitude reaches relatively high values (as compared to the amplitude of the phase current fundamental).

3.1 Mean Value of the Inverter Input Current

Based on the considerations in section 2.2 we have for the *local* mean value of the inverter input current (related to a pulse half period)

$$i_{\mathrm{avg}} = \frac{2}{T_P} \int_0^{\frac{1}{2}T_P} i \, \mathrm{d}t_\mu \,. \tag{12}$$

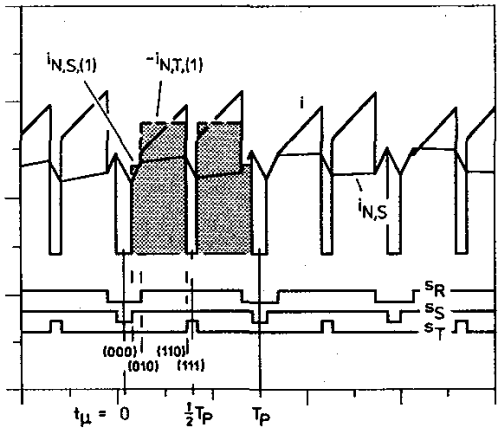

Fig.3: Illustration of the formation of the inverter input current i in dependency on the inverter switching state (s_R,s_S,s_T); local time behavior of the inverter input current i, of the inverter output phase current $i_{N,S}$ and of the phase switching functions s_R, s_S and s_T; furthermore shown: simplified shape of the inverter input current resulting for the neglection of the phase current ripple and/or exclusive consideration of the phase current fundamentals (shown dashed and pointed out by the dotted area). The simplified current shape gives the basis of the calculation of the DC link capacitor current stress in section 3.

Eq.(12) can be expressed as

$$i_{\text{avg}} = \delta_{(010)} i_{N,S} - \delta_{(110)} i_{N,T} \ . \tag{13}$$

With this, and Eqs.(4) and (10) we receive

$$i_{\text{avg}} = I_{\text{avg}} = \frac{3}{4} \hat{I}_N M \cos\varphi \ . \tag{14}$$

Corresponding to the constant power supplied by a symmetrical and sinusoidal three-phase voltage/current system the inverter input current shows a constant local average value $i_{\text{avg}} = I_{\text{avg}}$, i.e., local and *global* (related to the fundamental of the output voltage) mean value are identical. For $\cos\varphi = 0$ the inverter generates only fundamental reactive power and/or no power is supplied from the DC link (harmonic power components are neglected). Accordingly, we have $I_{\text{avg}} = 0$, the inverter input current i is defined by segments out of the vicinity of the zero crossings of the output phase currents $i_{N,i}$ with alternating signs (cf. **Fig.4**(a)).

On the contrary, for $\cos\varphi = 1$ we have purely active power operation and/or maximum current is supplied by the DC link. There, i is formed by segments of identical signs out of the vicinity of the maxima of the phase currents $i_{N,i}$ (cf. Fig.4(b)). For a given value of the fundamental displacement factor $\cos\varphi$ of the output current/voltage system I_{avg} will rise linearily with increasing modulation index M. This can be explained by considering the linear increase of the width of the current pulses (cf. Eq.(4)) appearing at the inverter input for increasing modulation index M or by the increase of the inverter output power due to the proportional increase of the fundamental output voltage as a consequence of the higher modulation index M (cf. Eq.(5)).

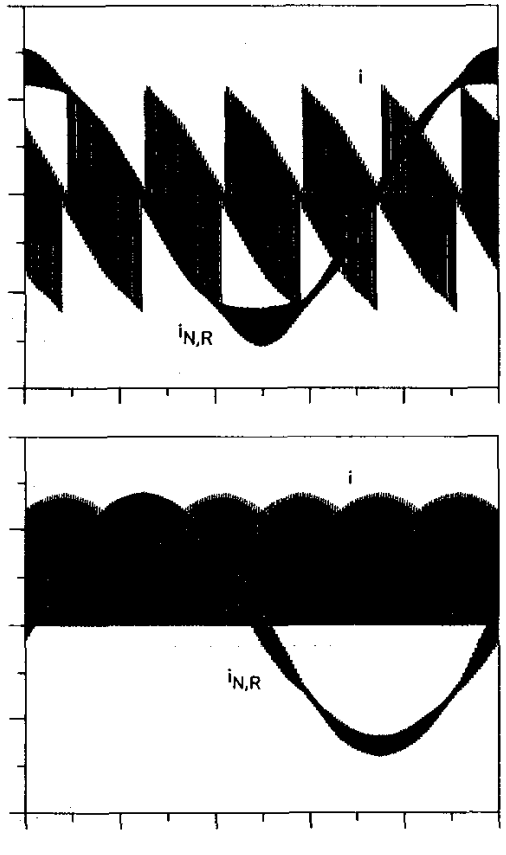

Fig.4: Time behavior of the inverter input current i and the output phase current $i_{N,R}$ within a fundamental period of the converter output voltage for $\cos\varphi = 0$ (cf. **(a)**) and $\cos\varphi = 1$ (cf. **(b)**).

It is important to note that besides the (global) mean value, i ideally does not contain any low frequency harmonics but only harmonics with switching frequency.

3.2 RMS Value of the Inverter Input Current

For the local rms value of the inverter input current

$$i_{\text{rms}}^2 = \frac{2}{T_P} \int_0^{\frac{1}{2}T_P} i^2 \, \mathrm{d}t_\mu \tag{15}$$

we have in analogy to Eq.(14)

$$i_{\text{rms}}^2 = \delta_{(010)} i_{N,S}^2 + \delta_{(110)} i_{N,T}^2 \ . \tag{16}$$

Therefore, with

$$I_{\text{rms}}^2 = \frac{3}{\pi} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} i_{\text{rms}}^2 \mathrm{d}\varphi_U \ , \tag{17}$$

and Eq.(4) there follows for the global rms value I_{rms} of i

$$I_{\text{rms}} = I_{N,\text{rms}} \sqrt{\frac{2\sqrt{3}}{\pi} M (\frac{1}{4} + \cos^2\varphi)} \ . \tag{18}$$

In connection with Eq.(18) one has to point out that the rms value of the inverter input current i in a first approximation (as calculated by exclusively considering the output phase current fundamentals) is *independent* of the inverter control scheme. Various control schemes differ only concerning the distribution $\delta_{(111),\text{r}}$ of the free-wheeling states [13] (being characterized by $i = 0$) between beginning and end of each pulse half period but not concerning the relative on-times $\delta_{(010)}$ and $\delta_{(110)}$ of the votage-forming states (cf. Eq.(4)). If the fundamentals of the output phase currents $i_{N,S,(1)}$ and $-i_{N,T,(1)}$ are assumed to be approximately constant within $t_\mu \in [0, \frac{1}{2}T_P)$, therefore, there is no influence of the actual position of the switching state intervals $\delta_{(010)}$ and $\delta_{(110)}$ on the value of i_{rms}. Therefore, the only (minor) influence of $\delta_{(111),\text{r}}$ on i_{rms} and I_{rms} is by the ripple component of $i_{N,S}$ and $-i_{N,T}$ which, however, has been neglected for the derivation of Eq.(18).

Remark: We would like to point out that the control parameter $\delta_{(111),\text{r}}$ also takes influence on the ripple with switching frequency of the DC link voltage. Therefore, alternatively to minimizing the harmonics rms value of the output phase currents $i_{N,i}$ one also could minimize the DC link voltage ripple by appropriately defining $\delta_{(111),\text{r}}$ [17]. This kind of optimization is of special importance if foil capacitors (which are characterized by a higher admissible current stress and higher service life as compared to electrolytic capacitors, but show a considerably lower capacitance) are employed for realizing the DC link capactior.

4 DC Link Capacitor Current RMS Value

The DC link capacitor current is defined by the difference

$$i_C = i_L - i \tag{19}$$

of the inverter input current i and the output current i_L of the converter input stage which in most cases is realized as uncontrolled three-phase rectifier bridge.

By splitting up i and i_L into DC and AC components (designated by subscript 'ac'),

$$\begin{aligned} i &= I_{\text{avg}} + i_{\text{ac}} \\ i_L &= I_{L,\text{avg}} + i_{L,\text{ac}} \ , \end{aligned} \tag{20}$$

one now can replace Eq.(19) by

$$i_C = i_{L,\text{ac}} - i_{\text{ac}} \ . \tag{21}$$

As is immediately obvious the load on the DC link capacitor is defined solely by the AC components of i and i_L, the DC component I_{avg} of i can be considered do be supplied directly by the input rectifier bridge.

With Eq.(20) and

$$I^2_{C,\text{rms}} = \frac{3}{\pi} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} i_C^2 \ \mathrm{d}\varphi_U \tag{22}$$

one receives for the global rms value of the DC link capacitor current

$$I^2_{C,\text{rms}} = I^2_{\text{ac,rms}} + \frac{3}{\pi} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} i_{\text{ac}} i_{L,\text{ac}} \mathrm{d}\varphi_U + I^2_{L,\text{ac,rms}} \ . \tag{23}$$

The problem with a mathematical evaluation of this equation usually cosists in the calculation of the integral being dependent on i_{ac} and $i_{L,\text{ac}}$. If, however, as in the case at hand the currents i_L and i do not contain harmonics in the same frequency range – harmonics of higher amplitudes are usually only present for ordinal numbers $n < 50$ in the output current of uncontrolled rectifier bridges (cf., e.g., Fig.13 in [18]); the frequency range being occupied by harmonics of i is defined by the inverter switching frequency and shows typically a lower bound of $n \approx 200 \ldots 500$ for a realization of the turn-off power semiconductors by IGBTs – we have

$$\frac{3}{\pi} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} i_{\text{h}} i_{L,\text{h}} \mathrm{d}\varphi_U = 0 \tag{24}$$

and we receive for the current stress on the DC link capacitor

$$I^2_{C,\text{rms}} = I^2_{\text{ac,rms}} + I^2_{L,\text{ac,rms}} \ . \tag{25}$$

Therefore, the rms value of the DC link capacitor current can clearly be divided into a contribution being determined by the mains-commutated input rectifier and a contribution caused by the PWM inverter (cf. Fig.7 in [4]). For the sake of brevity in the following only the calculation of $I_{C,\text{rms},1} = I_{\text{ac,rms}}$ will be discussed in detail. Concerning the calculation of $I_{C,\text{rms},2} = I_{L,\text{ac,rms}}$ we would like to refer to, e.g., [19].

Remark: If the DC link is fed via a self-commutated rectifier, e.g., a three-phase PWM rectifier system with high pulse frequency (cf., e.g., p. 201 in [20]) the DC link capacitor current results from a superposition of harmonics of the DC link input and output currents. The current stress on the DC link capacitor therefore is dependent on the amplitudes and on the phase relations of the harmonics of equal ordinal number resulting in a higher or lower amplitude of the respective harmonics in the DC link capacitor current. Therefore, $I_{C,\text{rms}}$ can be minimized by an appropriate coupling and/or synchronization of the rectifier

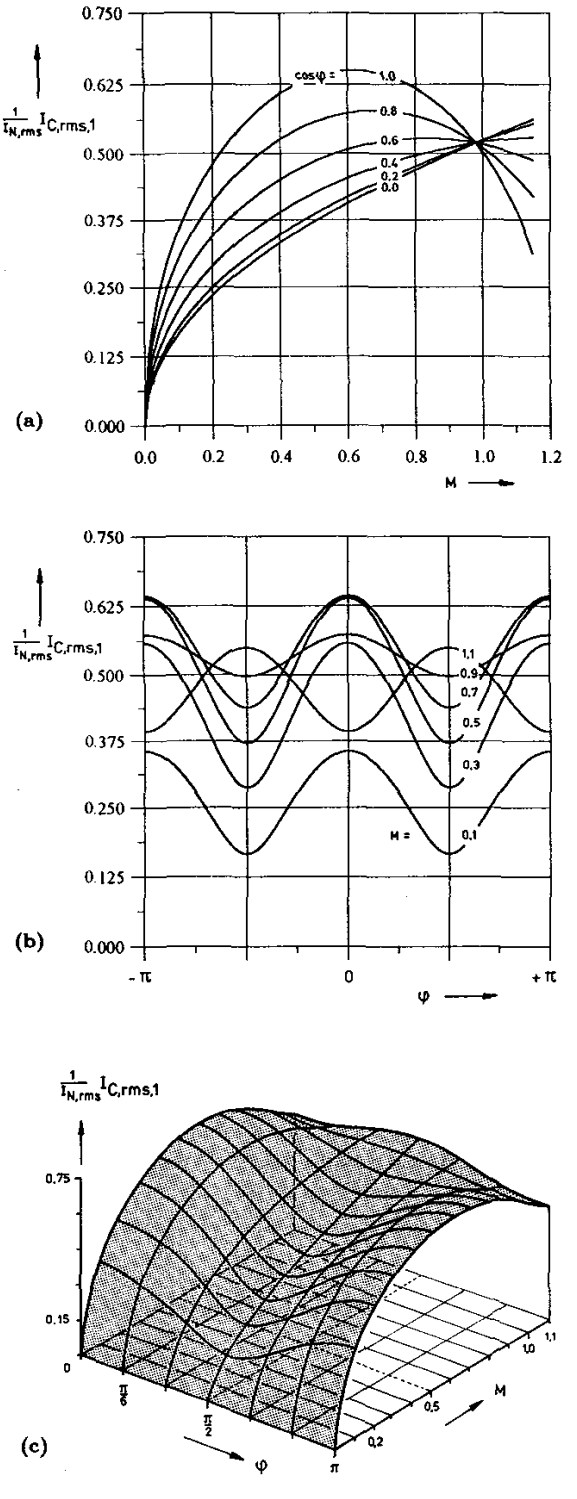

Fig.5: Dependency of the inverter-side contribution $I_{C,\text{rms},1}$ (cf. Eq.(27)) to the global DC link capacitor current rms value $I_{C,\text{rms}}$ on the inverter modulation index M and on the phase displacement φ of the fundamentals of the inverter output phase voltages $u_{U,i}$ and the associated output phase currents $i_{N,i}$. Parameters of the family of curves: $\cos\varphi$ (cf. (a)) and M (cf. (b)); (c): three-dimensional representation.

and inverter controls (cf. section 3 in [21] and [22]). The maximum current stress on the DC link capacitor current occurs for completly 'uncorrelated' operation of the input- and output-side systems (related to the power flow into and out of the DC link). As shown in [23] (cf. Eq.(50) in [23]) in this case

$$I_{C,\mathrm{rms,max}} = I_{\mathrm{ac,rms}} + I_{L,\mathrm{ac,rms}} \tag{26}$$

can be given as a worst case estimate. For a more accurate determination of $I_{C,\mathrm{rms}}$ one would have to refer to a digital simulation.

For the rms value $I_{C,\mathrm{rms},1}$ of the AC component i_{ac} of i we have in general

$$I^2_{C,\mathrm{rms},1} = I^2_{\mathrm{rms}} - I^2_{\mathrm{avg}} \; . \tag{27}$$

and with Eq.(14) [25]

$$I_{C,\mathrm{rms},1} = I_{N,\mathrm{rms}} \sqrt{2M[\frac{\sqrt{3}}{4\pi} + \cos^2\varphi(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M)]} \; . \tag{28}$$

Eq.(28) represents the wanted functional dependency of the current stress on C on the inverter operating parameters (cf. **Fig.5**). The proportional relationship of $I_{C,\mathrm{rms},1}$ and $I_{N,\mathrm{rms}}$ and/or $\sqrt{M}$ can be explained clearly by considering the fact that i is formed by segments out of the phase currents with a width being linearily dependent on the modulation index M (cf. Eq.(8)). (For $M = 0$ the inverter remains in the free-wheeling state within the entire pulse half period; therefore, we then have $i = 0$ or $i_{C,\mathrm{rms},1} = 0$, respectively).

However, if now $\cos\varphi \approx 1$ is assumed, besides I_{rms} also the DC component I_{avg} increases with increasing M, according to Eqs.(14) and (18). Therefore, according to Eq.(27) a maximum of the DC link capacitor current rms value $I_{C,\mathrm{rms}}$ occurs about in the middle of the modulation range

$$M_{I^2_{C,\mathrm{rms},1}\to\max} = \frac{8\sqrt{3}}{9\pi}(1 + \frac{1}{4\cos^2\varphi}) \; . \tag{29}$$

This can be explained clearly by considering the rms value of the AC component of a unipolar square wave signal with variable duty ratio α which reaches a maximum for $\alpha = 0.5$. For operating the inverter at maximum modulation depth $M_{\max}$ the shape of i still shows intervals with zero current (of relative width $\delta_{(000)} + \delta_{(111)}$, cf. Eqs.(4) and (6)). Accordingly, the inverter input current in any case shows a AC component i_{ac} and/or $I_{C,\mathrm{rms},1}$ does not reach 0 for values of M close to $M_{\max}$.

In the case of $\cos\varphi \approx 0$ again a sequence of phase current segments showing increasing widths for increasing M is switched into the DC link. However, there is no reduction of $I_{C,\mathrm{rms},1}$ as compared to I_{rms} due to the missing DC component I_{avg} of i (no power is supplied by the DC link and/or, as discussed in section 3.1, the phase current segments occuring within a pulse half period show opposite signs). Therefore, $I_{C,\mathrm{rms}}$ coincides with I_{rms} (cf. Eq.(18)) and the maximum of $I_{C,\mathrm{rms}}$ occurs for maximum modulation depth $M_{\max} = \frac{2}{\sqrt{3}}$ and/or turns into a boundary maximum. This is true in general for

$$\cos^2\varphi \le \frac{1}{4(\frac{3\pi}{4} - 1)} \; . \tag{30}$$

In this connection we would like to point out that for

$$M' = \frac{16\sqrt{3}}{9\pi} \tag{31}$$

the resulting current stress $I_{C,\mathrm{rms},1}$ is independent of the value of $\cos\varphi$.

According to **Fig.5** for a coarse worst case estimation of the current stress on the DC link capacitor as a basis for the capacitor dimensioning one has to start from

$$I_{C,\mathrm{rms},1} \approx \frac{1}{2}\hat{I}_N \tag{32}$$

independent of the value of the fundamental displacement factor $\cos\varphi$.

5 Accuracy Estimation

In order to be able to derive a simple expression for the inverter-side current stress $I_{C,\mathrm{rms},1}$ on C and for being independent of details of the inverter control scheme, the ripple of the inverter output currents $i_{N,i}$ has been neglected and/or only the fundamentals $i_{N,i,(1)}$ of the phase currents $i_{N,i}$ have been considered so far. Thus, a very clear approximation being independent of the absolute values of the DC link voltage U_O, the pulse frequency f_P and the stray inductance L of the AC machine (cf. Fig.1) has been derived. Now in the following the error which is caused by the neglection of the phase current ripple as compared to an exact calculation by digital simulation is determined and/or the limit of the applicability of Eq.(28) for the design of the DC link capacitor is determined.

There, for characterizing the ripple of the phase currents a parameter

$$\kappa = \frac{1}{\hat{I}_N}\frac{U_O T_P}{8L} \tag{33}$$

is defined. Thus all operating parameters being of influence on the formation of the output current ripple are combined and related to the amplitude of the output current fundamental. ($\frac{U_O T_P}{8L}$ represents the ripple amplitude resulting for the application of a symmetrical square wave voltage of frequency f_P, duty cycle $\alpha = 0.5$ and amplitude $\frac{1}{2}U_O$ to L.) Furthermore, a symmetrical distribution $\delta_{(111),\mathrm{r}} = 0.5$ of the free-wheeling switching state (cf. section 2.1) is assumed which is frequently applied in practice due to the low calculation effort required for the determination of the inverter switching instants [24].

For feeding the DC link via an uncontrolled rectifier bridge the value of the DC link voltage is determined directly by the mains voltage and usually shows a very low ripple. Therefore, for the following considerations a constant DC link voltage of $U_O = 540\,\mathrm{V}$ is assumed corresponding to the voltage value resulting for the operation of the converter system in the European low voltage three-phase mains (line-to-line voltage: $400\,\mathrm{V_{rms}}$) and ideal capacitive smoothing. For the switching frequency we define $f_P = \frac{1}{T_P} = 10\,\mathrm{kHz}$. Thus, by considering output inductance values in the range of $L = 0.3375 \ldots 1.35\,\mathrm{mH}$ in connection with an amplitude of the output phase currents being set to $\hat{I}_N = 20\,\mathrm{A}$ a range of $\kappa = 0.25 \ldots 1.0$ is inspected, where the output current shape changes form being approximately sinusoidal ($\kappa = 0.25$) to having a relatively high ripple component ($\kappa = 1$, cf. **Fig.6**). Furthermore, the conditions for $\cos\varphi = 1$ and $\cos\varphi = 0$ are investigated as in these cases qualitatively different shapes of i and/or i_{ac} (cf. Fig.4) occur.

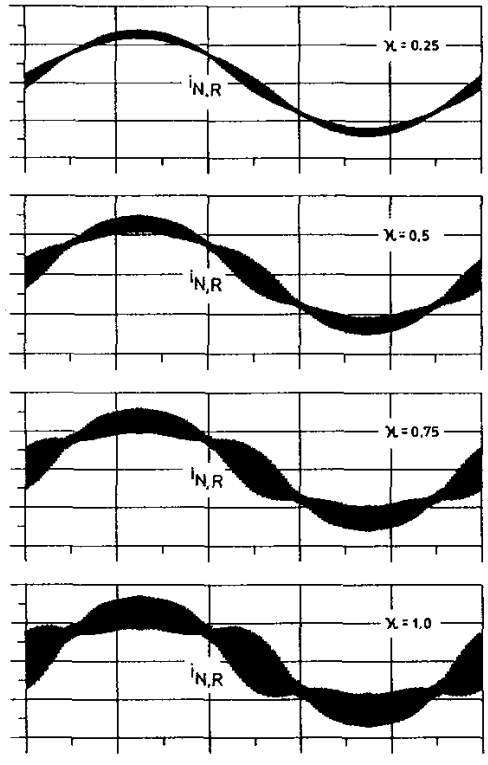

Fig.6: Time behavior of an inverter output phase current for different values of the parameter κ which characterizes the relative amplitude (related to the amplitude $\hat{I}_N$ of the output current fundamental) of the output current ripple; $\kappa = 0.25, 0.5, 0.75$ and 1.0 (cf. **(a)** - **(d)**); simulation parameters: $\cos\varphi = 1$, $M = 1.0$

The dependency of the relative error

$$f = \frac{1}{I_{C,\mathrm{rms},1,\mathrm{sim}}}(I_{C,\mathrm{rms},1,\mathrm{Eq.(28)}} - I_{C,\mathrm{rms},1,\mathrm{sim}}) \qquad (34)$$

of the analytical calculation of $I_{C,\mathrm{rms},1}$ based on Eq.(28), $I_{C,\mathrm{rms},1,\mathrm{sim}}$ denotes the inverter-side current stress on C as determined by digital simulation) on κ and M is shown in **Fig.7**. For values of M close to 0 the phase currents show a very low ripple (cf. Fig.16 in [25]). Therefore, the error caused by assuming a purely sinusoidal output current shape remains limited to very small values. For increasing modulation depth M a higher relative error of the analytical approximation occurs due to the increasing output current ripple amplitude.

In the case of $\cos\varphi = 0$ we in general have a lower accuracy than for $\cos\varphi = 1$. This can be explained clearly by the fact that for $\cos\varphi = 0$ the inverter input current (and correspondingly also i_{ac}, Eq.(21)) is formed by segments out of the vicinity of the zero crossings of the output phase currents; thus a current ripple of given amplitude κ takes a relatively higher influence on the shape of i as for forming i by segments out of the vicinity of the maxima of the phase currents and/or for $\cos\varphi = 1$ (cf. Fig.4).

In case, e.g., a minimum degree of accuracy according to $|f| < 5\ldots10\%$ is set for the dimensioning the application range of Eq.(28) is limited by $\kappa \approx 0.75$. This, however, certainly includes the conditions being typically present in practice for operating an IGBT inverter at rated power. Therefore, the dimensioning can be based on Eq.(28) and/or a time-consuming calculation of $I_{C,\mathrm{rms},1}$ by digital simulation can be omitted.

Remark: Harmonic-optimal modulation (i.e., a modulation scheme which is optimized with respect to minimum harmonic current rms value by extending simple sinusoidal modulation by addition of a third harmonic [13]) in a first approximation results in an almost identical time behavior of the output current ripple and/or an equal harmonic rms value of the phase current ripple as given for the (suboptimal) control scheme which has been taken as a basis for the considerations in this paper (cf. Fig.6 in [14]. Therefore, Fig.7 can be considered as being valid also for optimized control. For purely sinusoidal modulation there results a higher ripple of the phase currents [13], [24] and in consequence the analytical calculation shows a higher deviation from the results of the digital simulation for a given value of κ. However, as this control scheme due to its limited modulation

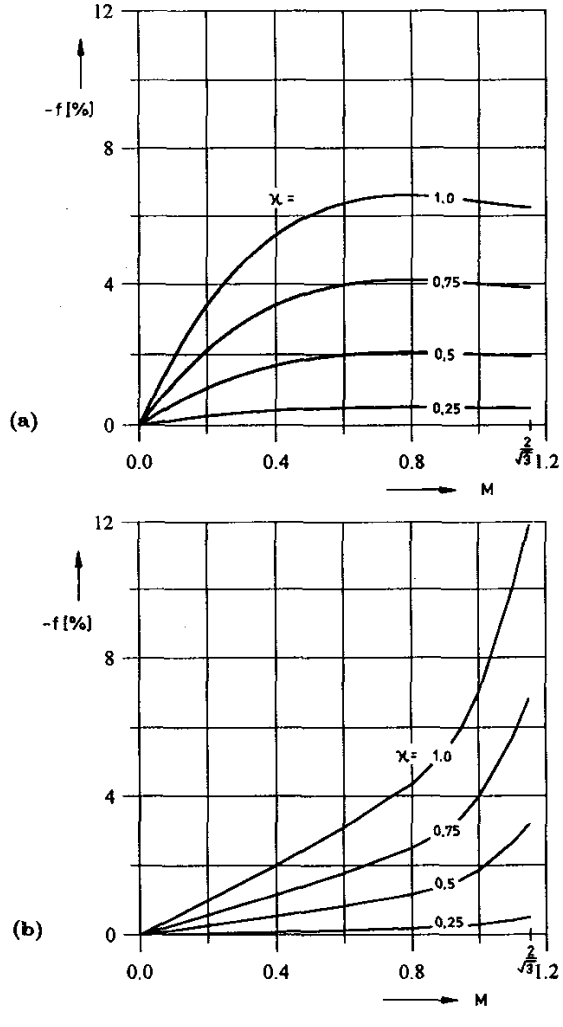

Fig.7: Relative error f of the analytical calculation of the capacitor current stress $I_{C,\mathrm{rms},1}$ as caused by the PWM inverter (cf. Eq.(28)) from the results of a digital simulation in dependency on the modulation index M and the relative amplitude κ of the inverter output current ripple for $\cos\varphi = 1$ (cf. **(a)**) and $\cos\varphi = 0$ (cf. **(b)**).

range $M \leq 1$ is of very limited practical importance this will not be discussed in more detail here.

6 Dimensioning of the DC Link Capacitor

For the dimensioning of C regarding the current stress the data sheet specifies a maximum permissible current stress $I_{C,\mathrm{rms,dim}}$ for a required working life of the aluminium electrolytic capacitor in dependency on the ambient temperature T_a. $I_{C,\mathrm{rms,dim}}$ represents a fictitious current rms value (cf. p. 9 in [26]) which considers the decrease of the R_{ESR} of an aluminium electrolytic capacitor with rising frequency. In most cases the value of this resistance is given for a frequency of $f = 100\,\mathrm{Hz}$ ($R_{\mathrm{ESR,100Hz}}$). Therefore, we have for the losses occurring in the capacitor

$$P_C = R_{ESR,100\mathrm{Hz}}\, I^2_{C,\mathrm{rms,dim}} \tag{35}$$

with

$$I^2_{C,\mathrm{rms,dim}} = \sum_{f_i} k_{f_i} I^2_{C,(f_i),\mathrm{rms}} \tag{36}$$

and

$$k_{f_i} = \frac{R_{ESR,f_i}}{R_{ESR,100\mathrm{Hz}}}\,, \tag{37}$$

where $I_{C,(f_i),\mathrm{rms}}$ denotes the rms value of the spectral component of i_C with frequency f_i; R_{ESR,f_i} defines the value of the equivalent series resistance being given for this frequency.

According to the data sheets of aluminium electrolytic capacitors, about a constant value of $k_{f_i>10\mathrm{kHz}} \approx 0.45$ is given for frequencies $f > 10\,\mathrm{kHz}$ (cf., e.g., p. 35 in [27])). For a realization of the turn-off power semiconductors of the inverter by IGBTs (as assumed in this paper) the switching frequency typically is set to values $f_P > 10\,\mathrm{kHz}$. Therefore, the effective current stress on the DC link capacitor as caused by the inverter simply can be calculated via

$$I^2_{C,\mathrm{rms,1,dim}} \approx 0.45\, I^2_{C,\mathrm{rms,1}}\,. \tag{38}$$

There, $I_{C,\mathrm{rms,1}}$ denotes the capacitor current rms value resulting for the maximum amplitude of the inverter output current. For the low frequency components of the capacitor current $I_{C,\mathrm{rms,2,dim}}$ which are caused by the uncontrolled rectifier bridge at the system input a different weighting of the harmonics has to be performed according to the capacitor data sheet (cf., e.g., Fig.3 in [4] or p.37 in [27]) and/or $I_{C,\mathrm{rms,2,dim}}$ has to be calculated by a digital simulation.

By comparing the admissible current stress of a capacitor with the actually occurring total current stress the number of capacitors to be connected in parallel can be determined and/or a capacitor having a sufficiently high capacitance and, therefore, a relatively high maximum current rating can be chosen. Due to the larger surface of capacitors of higher capacitance (and/or higher volume) the heat transmission resistance $R_{th,c\to a}$ shows a lower value. Therefore, for a given can temperature T_c a higher power loss $I^2_{C,\mathrm{rms,dim}} R_{ESR}$ of the capacitor can be tolerated (cf. Eq.(1)). In connection with this it is important to note that the capacitance of the DC link capacitor of practical systems usually is determined by the effective capacitor current stress and not, e.g., by a given maximum admissible value of the amplitude of the DC link voltage ripple. This confirms the assumption of a constant DC link voltage made in chapter 2.1.

7 Conclusions

In this paper a simple analytical expression for the current stress on the DC link capacitor of a three-phase PWM converter system as caused by the inverter stage is derived. As checked by a comparison to the results of a digital simulation the calculated expression meets the accuracy requirements for designing the DC link capacitor for practical IGBT inverter systems (switching frequency $f_P > 10\,\mathrm{kHz}$, relative ripple of the output current $\kappa < 0.75$).
The topic of further research will be the analytical calculation of the DC link capacitor current stress in the case of over-modulation and of the DC link capacitor current rms value as occurring for three-level (cf. [28] and/or [29]) and single-phase [21] PWM inverter systems.

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