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***Abstract*—DC power distribution systems for data centers, industrial applications and residential areas are expected to provide higher efficiency, reliability and lower cost compared to ac systems. Accordingly they have been an important research topic in recent years. In these applications an efficient power factor correction rectifier, supplying a dc distribution bus from the conventional three-phase ac mains is typically required. This paper analyzes the three-phase buck-type unity power factor SWISS Rectifier showing that its input current THD can be improved significantly by interleaving. The dc output filter is implemented using a current compensated Integrated Common Mode Coupled Inductor which ensures equal current sharing between interleaved half bridges and provides common mode inductance. Based on the analysis an high efficient 8 kW, 4 kW dm^{-3} (64 W in^{-3}) lab-scale prototype converter is designed using SiC MOSFETS. Measurements taken on a hardware prototype confirm a full power efficiency of 99.16 % and a peak efficiency of 99.26 %.**

I. Introduction

Over the last decades the power demand of intrinsic dc loads, such as information and communication technology equipment, data centers, electric vehicle battery charging, LED lighting, etc. increased substantially. Furthermore renewable energy sources such as PV modules, fuel cells and battery storage are also based on dc. Therefore, dc distribution systems are expected to give advantages in terms of efficiency, reliability and/or cost as the total number of conversion stages can be reduced. Consequently, dc power supply and distribution systems for information and communication technology equipment, electric vehicle traction battery fast charging and dc microgrids have been a major topic in research and industry in recent years and corresponding standards have been created [1–9].

In these applications loads, with typically tens of kilowatts or more, are supplied from a dc bus with $\approx 400\,\mathrm{V}$ which is powered from the conventional $400\,\mathrm{V}$ or $480\,\mathrm{V}$ rms three-phase ac mains. Due to the high power levels sinusoidal ac input currents, in-phase with the mains voltage are required. As the dc bus voltage is lower than the amplitude of the full-wave rectified three-phase line-to-line voltage, two-stage systems are normally used which consist of a boost-type power factor correction (PFC) rectifier front end providing $\approx 800\,\mathrm{V}$ dc and a subsequent step-down dc-dc converter. Buck-type PFC rectifiers, which allow a direct conversion from the three-phase ac mains to a dc bus with lower voltage, are an advantageous alternative offering potentially lower losses, volume and cost [11].

The schematic of the three-phase buck-type SWISS Rectifier introduced in [10] is shown in **Fig. 1(a)**. It consists of an ac-side EMI input filter, an Input Voltage Selector (IVS) and two series-connected buck-type dc-dc converters $\mathrm{S_{x\bar{p}}}$, $\mathrm{D_{y\bar{p}}}$ and $\mathrm{S_{\bar{n}z}}$, $\mathrm{D_{\bar{n}y}}$. Note that all diodes and switches in the IVS are commutated at mains frequency only, therefore basically no switching losses occur in the IVS. Hence, diodes with a low forward voltage drop, or MOSFET-based synchronous rectifiers can be used in the IVS. The IVS output voltages u_x, u_y, u_z are piece-wise sinusoidal as the input phase with highest potential is connected to node x, the one with lowest potential to z and the remaining phase to node y.

In this paper the conventional (single buck converter output stage), cf. **Fig. 1(a)**, and interleaved SWISS Rectifier, cf. **Fig. 1(b)**, are compared regarding their ac input and dc

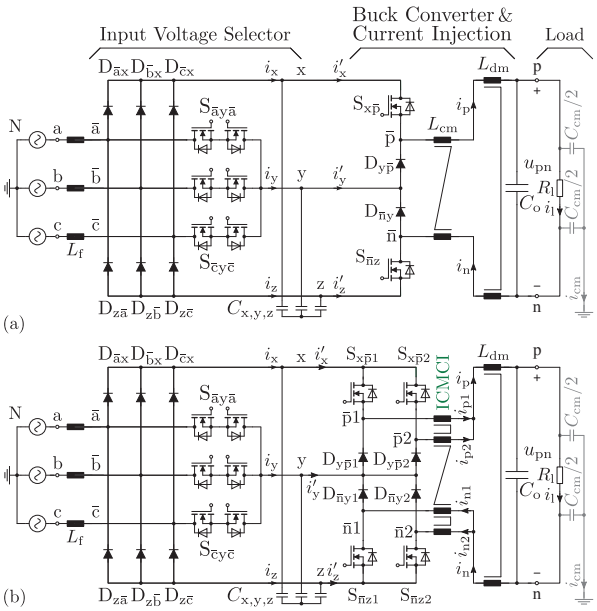

Fig. 1. **(a)** Three-phase buck-type SWISS Rectifier consisting of an EMI input filter, an Input Voltage Selector commutated at mains frequency and two dc-dc buck converters as proposed in [10]. **(b)** Interleaved SWISS Rectifier using a novel four winding current compensated Integrated Common Mode Coupled Inductor (ICMCI) which is used to ensure equal current sharing $i_{\mathrm{p1}} \approx i_{\mathrm{p2}}$, $i_{\mathrm{n1}} \approx i_{\mathrm{n2}}$ and provides common mode inductance.

TABLE I
Converter Specifications

Input Voltage (Line-to-Neutral)	$U_1 = 230\,\mathrm{V}$ rms
Input Frequency	$\omega_1 = 2\pi\,50\,\mathrm{Hz}$
Switching Frequency	$f_\mathrm{s} = 27\,\mathrm{kHz}$
Nominal Output Voltage	$U_\mathrm{pn} = 400\,\mathrm{V}$
Nominal Output Power	$P = 8\,\mathrm{kW}$
DM Output Inductance	$L_\mathrm{dm} = 350\,\mu\mathrm{H}$
CM Output Inductance	$L_\mathrm{cm} = 600\,\mu\mathrm{H}$

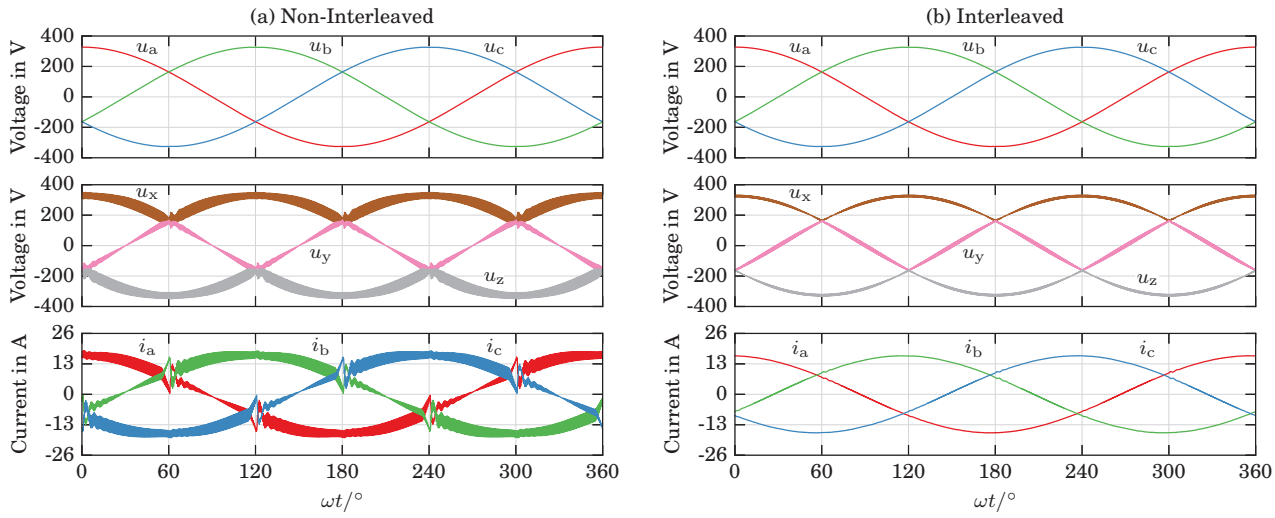

Fig. 2. Simulation results for an 8 kW SWISS Rectifier as specified in **Table I**, showing the ac input voltages $u_{a,b,c}$, the filter capacitor voltages $u_{x,y,z}$ and the resulting ac input currents $i_{a,b,c}$. **(a)** Due to the discontinuous input currents $i'_{x,y,z}$ of the non-interleaved dc-dc buck converters a high ripple in $u_{x,y,z}$ and in the ac input currents $i_{a,b,c}$ results. This also leads to significant distortions in $i_{a,b,c}$ as described in [12]. **(b)** In the interleaved SWISS Rectifier the switching frequency voltage ripples of $u_{x,y,z}$ are reduced significantly due to harmonic cancellation. Therefore the ac input current ($i_{a,b,c}$) ripple and the resulting distortion at sector boundaries are reduced as well.

output properties in **Section II**. The implemented prototype converter is presented in **Section III**, including measurement results.

II. SWISS RECTIFIER

A. Non-Interleaved SWISS Rectifier

In **Fig. 1(a)** the SWISS Rectifier with two coupled dc output inductors L_{cm} (common mode) and L_{dm} (differential mode) is shown. As the dc load is connected between output nodes p and n of the converter and has no connection to the star point N of the ac mains $i_p = i_n$ can usually be assumed and the differential mode inductor alone would be sufficient. However, this is not the case if the load is, for example, a widespread dc distribution bus, potentially including physically large backup batteries, which can have a significant capacitance C_{cm} to ground. This creates a conduction path for high frequency common mode (cm) currents i_{cm} from the output nodes p and n to the grounded star point N as shown in **Fig. 1**, which is also the case if dedicated cm capacitors are added to the converter as part of a cm filter, which is typically required to comply with EMI regulations.

Simulation results for a conventional non-interleaved 8 kW SWISS Rectifier specified in **Table I** are shown in **Fig. 2(a)**. It can be seen that the ac input currents i_a, i_b, i_c show a significant switching frequency ripple and distortions with an amplitude of $\approx 6\,A$ at every $60°$ mains voltage sector boundary. Detailed simulation results for the vicinity of the first sector boundary at $\omega t \approx 60°$ are shown in **Fig. 3(a)**. These distortions are due to the switching frequency voltage ripple on the filter capacitors $C_{x,y,z}$ as described in [12]. As u_x, u_y and u_z are piece-wise sinusoidal due to the IVS operation, $C_{x,y,z}$ create reactive power at the ac input which typically has to be limited to a few percent of the converter's rated output power, which limits the capacitance value of $C_{x,y,z}$. As the SWISS Rectifier is a buck-type topology the input currents i'_x, i'_y and i'_z of the dc-dc converter are discontinuous which, in connection with the limited capacitance of $C_{x,y,z}$ results in a high switching frequency ripple of u_x, u_y and u_z, cf. **Fig. 3(a)**.

B. SWISS Rectifier with Interleaved Output Stages

To reduce the input current and voltage ripples either the ac input filter capacitance and inductance can be increased or a higher switching frequency can be used. Both options increase volume, losses and cost of the converter system. In order to overcome these disadvantages two interleaved dc-dc converters can be used as output stage to reduce the input and output current ripples [13]. The schematic of the resulting system, denominated as *interleaved SWISS Rectifier* in the following, is shown in **Fig. 1(b)** where two individual bridge legs $S_{x\bar{p}1}$ / $D_{y\bar{p}1}$ and $S_{x\bar{p}2}$ / $D_{y\bar{p}2}$ are used for the p side dc-dc converter stage and $S_{\bar{n}z1}$ / $D_{\bar{n}y1}$, $S_{\bar{n}z2}$ / $D_{\bar{n}y2}$ are used for the n side. By using the same duty cycle but $180°$ phase shifted carriers for the pulse width modulation of $S_{x\bar{p}1}$ and $S_{x\bar{p}2}$ the high frequency components of the resulting input current i'_x have twice the frequency and half the amplitude compared to the non-interleaved case as shown in the detailed simulation results in **Fig. 3(b)**.

Simulation results of the interleaved SWISS Rectifier are shown in **Fig. 2(b)**, where it can be seen that the differential mode (dm) and cm current ripples are reduced significantly compared to **Fig. 2(a)**. Detailed simulation results for the first mains voltage intersection are shown in **Fig. 3(b)**. Due to the reduced ripple of the buck converter input currents i'_x, i'_y and i'_z, the peak-peak ripple on the filter capacitor voltages u_x, u_y and u_z reduces from 105 V without interleaving to 24 V with interleaving. Also the ripple and the distortions of the input currents i_a, i_b and i_c occurring at every $60°$ mains voltage sector boundary are reduced from $\approx 6\,A$ to $< 1\,A$.

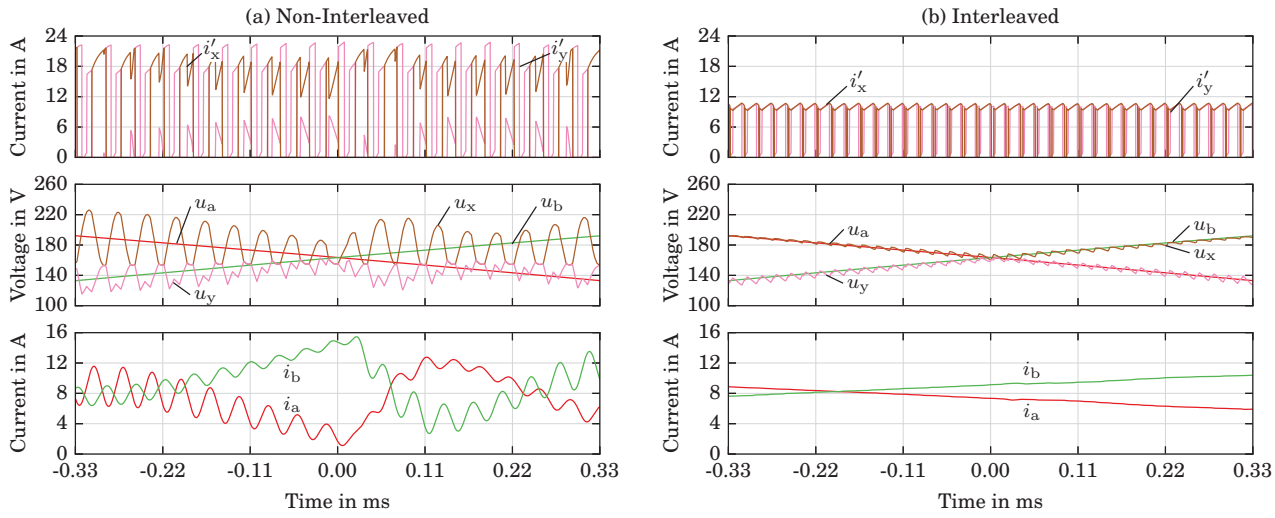

Fig. 3. Detailed simulation results of the first intersection of the mains line-to-neutral voltages u_a and u_b at $\omega t \approx 60°$: **(a)** the discontinuous buck converter input currents i'_x, i'_y of the non-interleaved SWISS Rectifier lead to high switching frequency ripples of the input filter capacitor voltages u_x and u_y. As u_x and u_y cannot intersect due to $D_{y\bar{p}}$ and $S_{x\bar{p}}$ a distortion of the mains currents i_a and i_b results [12]. **(b)** In case of an interleaved SWISS Rectifier the amplitude of i'_x, i'_y is reduced and the frequency is doubled which leads to a significant reduction of the ripples in u_x and u_y.

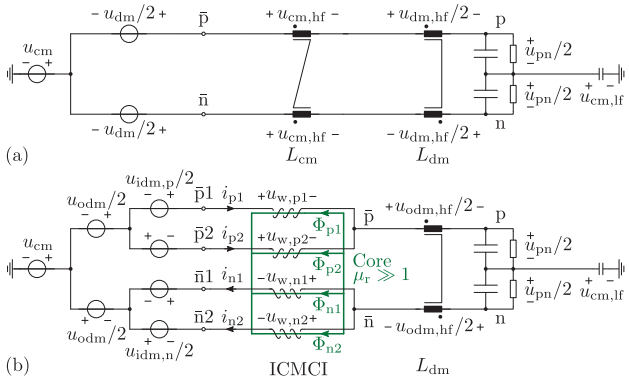

Fig. 4. Simplified circuit diagram of **(a)** the conventional and **(b)** the interleaved SWISS Rectifier where the IVS and the dc-dc converters are replaced by equivalent voltage sources split into common mode, outer- and inner differential mode.

Note that the interleaved buck converters can be controlled such that the individual dc-dc converter currents are split equally, i.e. $i_{p1} = i_{p2}$ and $i_{n1} = i_{n2}$ except for a switching frequency ripple. This implies that current compensated filtering of the dc-dc converter output voltages can be accomplished with close-coupled inductors. Ideally they carry no dc flux component and can be implemented without an air-gap, leading to a larger inductance value, similar to a cm inductor. Typically this is implemented with so called Intercell Transformers (ICTs) [14–16], were the interleaved SWISS Rectifier would require two ICTs, one for the p and one for the n side bridges. However, the two ICTs and the cm inductor L_{cm} can be integrated into a single four winding magnetic device in the following denominated as *Integrated Common Mode Coupled Inductor* (ICMCI) as shown in **Fig. 1(b)** and **Fig. 4(b)**.

C. Integrated Common Mode Coupled Inductor - ICMCI

In order to analyze the properties of the ICMCI the SWISS Rectifier's input filter, IVS and dc-dc converters are replaced by equivalent voltage sources which define the potentials of nodes $\bar{p}1$, $\bar{p}2$, $\bar{n}1$ and $\bar{n}2$ with respect to the mains star point and/or ground. Furthermore, these four voltage sources can be converted to a tree structure of a common mode (cm), an outer differential mode (odm) and two inner differential modes (idm) as shown in **Fig. 4(b)**. A similar equivalent circuit of the conventional SWISS Rectifier is shown in **Fig. 4(a)** for comparison. These equivalent voltages can be derived as

$$u_{cm} = \frac{u_{\bar{p}1} + u_{\bar{p}2} + u_{\bar{n}1} + u_{\bar{n}2}}{4} , \tag{1}$$

$$u_{odm} = \frac{u_{\bar{p}1} + u_{\bar{p}2}}{2} - \frac{u_{\bar{n}1} + u_{\bar{n}2}}{2} , \tag{2}$$

$$u_{idm,p} = u_{\bar{p}1} - u_{\bar{p}2} , \tag{3}$$

$$u_{idm,n} = u_{\bar{n}1} - u_{\bar{n}2} . \tag{4}$$

Neglecting any stray fields in the ICMCI the fluxes Φ_{p1}, Φ_{p2}, Φ_{n1}, Φ_{n2} generated by the four windings have to sum up to zero due to the ICMCI's core, cf. **Fig. 4(b)**:

$$\Phi_{p1} + \Phi_{p2} + \Phi_{n1} + \Phi_{n2} = 0 . \tag{5}$$

This implies that the voltages applied to the four windings sum to zero as well due to inverse winding direction of the p and n side ICMCI windings. Using Kirchhoff's voltage law on the circuit shown in **Fig. 4(b)** three additional equations can be found, which yields four equations that define the ICMCI's voltages

$$u_{w,p1} + u_{w,p2} + u_{w,n1} + u_{w,n2} = 0 , \tag{6}$$

$$u_{w,p1} - u_{w,p2} = u_{idm,p} , \tag{7}$$

$$-u_{w,n1} + u_{w,n2} = u_{idm,n} , \tag{8}$$

$$u_{w,p1} + u_{w,p2} - u_{w,n1} - u_{w,n2} = 4\, u_{cm,hf} . \tag{9}$$

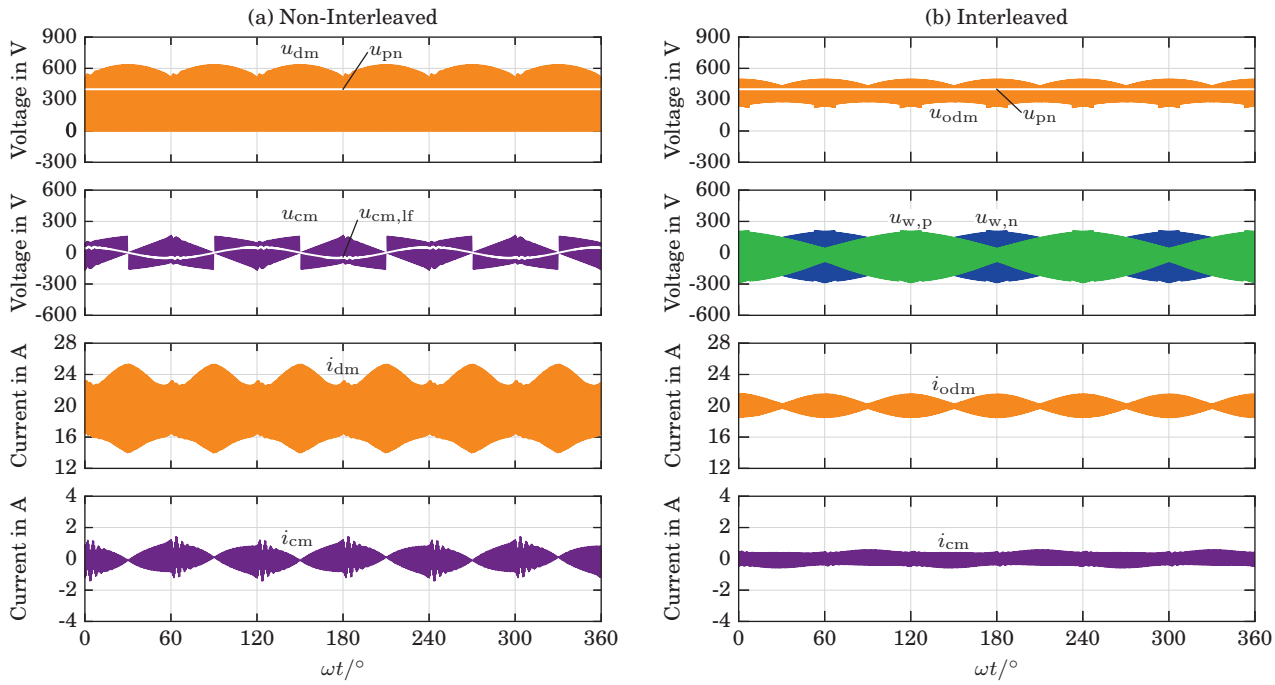

Fig. 5. **(a)** Detailed simulation results for a non-interleaved SWISS Rectifier with the same operating conditions as in **Fig. 2**, showing dm and cm voltages u_{dm} and u_{cm} created by the dc-dc converters and the resulting dm and cm currents i_{dm} and i_{cm}. **(b)** Simulation results of the corresponding quantities of an interleaved SWISS Rectifier using an ICMCI. Due to the interleaving the outer differential mode (odm) voltage u_{odm} peak-to-peak value reduces, which leads to a reduction of the ripple in the corresponding current i_{odm}.

Note that $u_{\mathrm{cm,hf}}$ is the switching frequency component of the converter's cm voltage u_{cm} as given by (1). Solving the system of equations given by (6) to (9) with respect to the ICMCI's winding voltages yields

$$u_{\mathrm{w,p1}} = \quad u_{\mathrm{idm,p}}/2 + u_{\mathrm{cm,hf}} \ , \tag{10}$$

$$u_{\mathrm{w,p2}} = -u_{\mathrm{idm,p}}/2 + u_{\mathrm{cm,hf}} \ , \tag{11}$$

$$u_{\mathrm{w,n1}} = -u_{\mathrm{idm,n}}/2 - u_{\mathrm{cm,hf}} \ , \tag{12}$$

$$u_{\mathrm{w,n1}} = \quad u_{\mathrm{idm,n}}/2 - u_{\mathrm{cm,hf}} \ . \tag{13}$$

It can be seen that the ICMCI's winding voltages are defined only by the switching frequency cm voltage and the inner dm voltages, while the outer dm voltage is applied only to the differential mode inductor L_{dm} and the dc output u_{pn}.

Simulation results of the ICMCI's winding voltages and the outer dm voltage for nominal operation are shown in **Fig. 5(b)**. Compared to a non-interleaved SWISS Rectifier, as shown in **Fig. 5(a)**, the (outer) dm voltage applied to L_{dm} is reduced which leads to a significant reduction of the peak-to-peak ripple in i_{odm} compared to i_{dm}. The same holds for the cm current i_{cm}.

A drawing of the resulting switching frequency voltage and current waveforms is shown in **Fig. 6** for $0° \leq \omega t \leq 30°$. It can be seen that the ICMCI's winding voltages $u_{\mathrm{w,p1}}$, $u_{\mathrm{w,p2}}$, $u_{\mathrm{w,n1}}$ and $u_{\mathrm{w,n2}}$ are periodic with the switching frequency, while the voltage $u_{\mathrm{odm,hf}}$ applied to L_{dm} shows twice that frequency due to harmonic cancellation.

III. Rectifier Prototype

For power supply systems which are operated 24/7, as in data centers, a high efficiency is desirable to minimize the cost of conversion losses and cooling and hence the operating costs of the system [17]. Furthermore a high efficiency over a wide range of output currents is desirable in applications where redundant supplies are used resulting in a nominal operation at half of the rated power or less. Therefore, a system which achieves an efficiency of $> 99\,\%$ for $P > P_{\mathrm{rated}}/3$ for the operating condition listed in **Table I** was designed.

TABLE II
Components used in the Hardware Prototype

	ICMCI	$\boldsymbol{L_{\mathrm{dm}}}$
Core	4 x U46/40/28-3C94	F3CC25
Wire	0.4 x 15 mm	2.4 x 6 mm
Turns	4 x 20	2 x 15
Volume	420 cm^3	249 cm^3
Losses	5.6 W	2.9 W
$\mathrm{D_{x\bar{k}}}$, $\mathrm{D_{\bar{k}z}}$	C2M0025120	$P_{\mathrm{loss}} = 1.8$ W
$\mathrm{S_{\bar{k}y\bar{k}}}$	C2M0080120	$P_{\mathrm{loss}} = 0.8$ W
$\mathrm{S_{x\bar{p}1,2}}$, $\mathrm{S_{\bar{n}z1,2}}$	C2M0025120	$P_{\mathrm{loss}} = 4.9$ W
$\mathrm{D_{y\bar{p}1,2}}$, $\mathrm{D_{\bar{n}y1,2}}$	C2M0025120[1]	$P_{\mathrm{loss}} = 1.0$ W

Silicon carbide (SiC) MOSFETs are selected due to their low conduction and switching losses and high blocking voltage rating (1.2 kV) compared to Si IGBTs and Si MOSFETs [18, 19]. Nanocrystalline core material (*FINEMET*) is used for dm inductor L_{dm} due to its high saturation flux density (≈ 1.2 T) and lower losses compared to amorphous alloys. For the current compensated ICMCI core *3C94* ferrite material is used due to its lower core losses. A symmetrical, cube-type core as shown in **Fig. 7** is used for the ICMCI. This shape is achieved by using four conventional C cores,

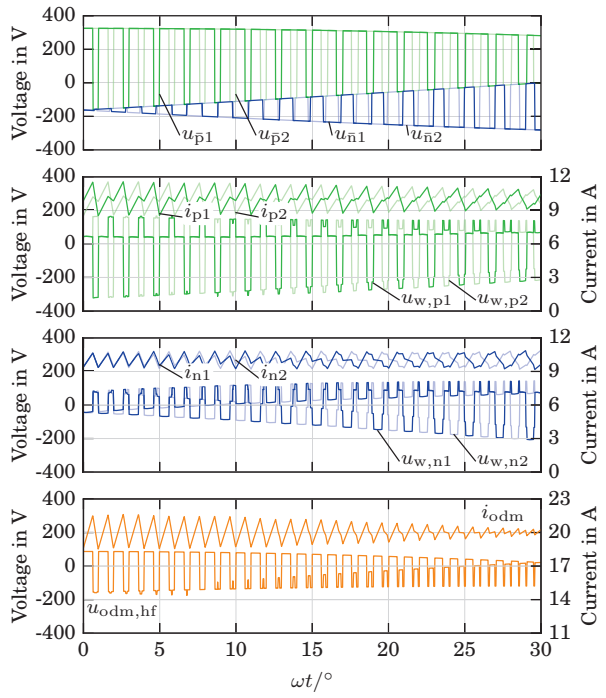

Fig. 6. Visualization of the resulting dc-dc converter output voltages $u_{\bar{p}1}$, $u_{\bar{p}2}$ and $u_{\bar{n}1}$, $u_{\bar{n}2}$ during a 30° mains voltage sector, with a reduced switching frequency of 9 kHz. This results in the ICMCI voltages $u_{w,p1}$, $u_{w,p2}$, $u_{w,n1}$ and $u_{w,n2}$ and the outer dm voltage $u_{odm,hf}$ applied to L_{dm}.

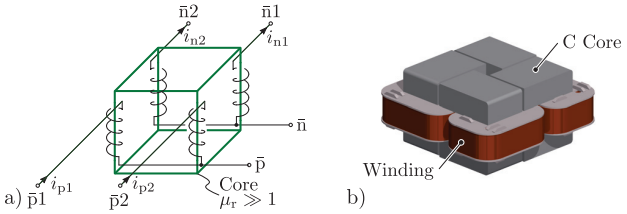

Fig. 7. **(a)** Structure of the implemented symmetrical, cube-type ICMCI core which is constructed from four C cores with one winding each as shown in **(b)**.

each carrying one winding as shown in **Fig. 7(b)**. The semiconductors and magnetic components selected for the prototype are listed in **Table II**.

The calculated losses of the selected components for nominal operation are shown in **Fig. 8(a)** with the corresponding volumes given in **(b)**. About 60 % of the total losses result from semiconductors, 13 % from the main magnetic components and 27 % from the EMI filter, control, gate drivers, auxiliary supply etc. A picture of the implemented hardware prototype, achieving a power density of 4.0 kW dm^{-3} (66 W in^{-3}) is shown in **Fig. 9**.

Measurement results of the rectifier's mains voltages and currents at nominal operation are shown in **Fig. 10**. The resulting input currents $i_{a,b,c}$ are nearly sinusoidal and free of distortions at the sector boundaries as expected from the presented simulation results. Note that the rectifier's control circuit is configured for ohmic mains behavior as described in [20]. An input current THD of 2.45 % results for a mains voltage THD of 2.29 %.

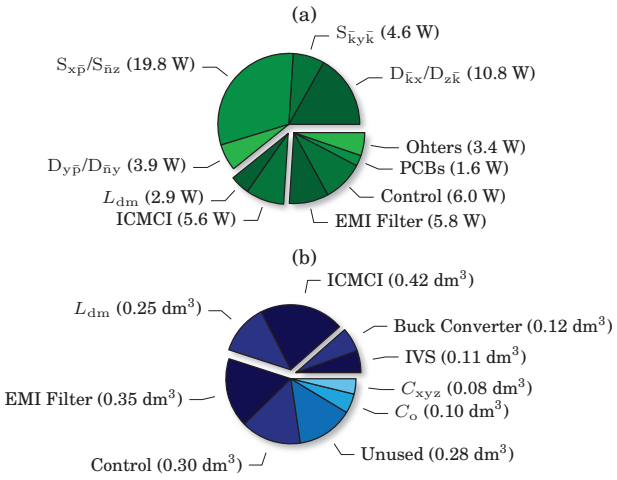

Fig. 8. Calculated losses of the rectifier's main components (cf. **(a)**) for nominal operation ($U_{pn} = 400$ V, $I_l = 20$ A). The control losses include DSP/FPGA, gate drivers, fans and auxiliary supply. The corresponding volumes in dm^3 are shown in **(b)** (1 dm^3 = 61 in^3).

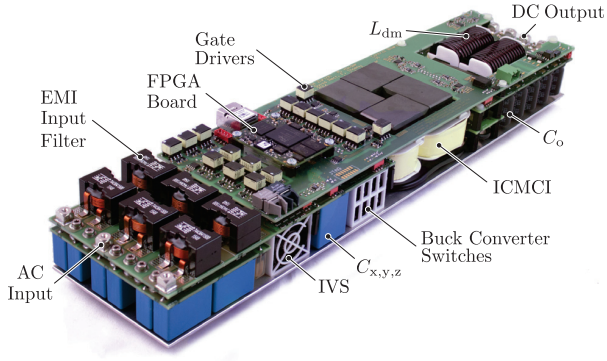

Fig. 9. Implemented 8 kW 400 V ac / 400 V dc interleaved SWISS Rectifier prototype (420 mm x 95 mm x 50 mm) with > 99 % efficiency (cf. **Fig. 11**) and a power density of 4 kW dm^{-3} (66 W in^{-3}).

The calculated efficiency of the rectifier for $U_{pn} = 400$ V as function of dc load current I_l is shown in **Fig. 11**, together with measurement results taken using a *Yokogawa WT3000* power analyzer. It can be seen that the measurement results of the prototype converter match the calculated efficiency

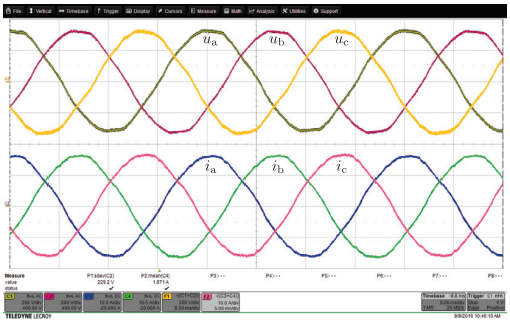

Fig. 10. Measured ac mains voltages $u_{a,b,c}$ (200 V / div.) and converter input currents $i_{a,b,c}$ (10 A / div.) for nominal operation. Note that the quantities for phases a and b were measured directly while those of phase c are created numerically as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

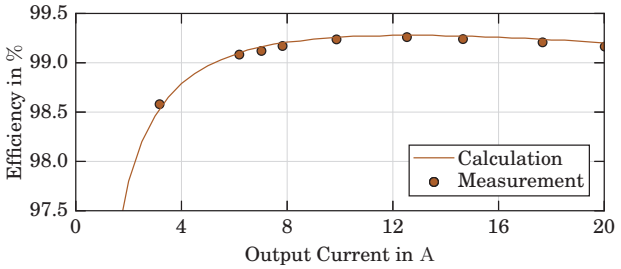

Fig. 11. Calculated and measured efficiency of the rectifier as function a of I_1, indicating that the converter achieves an efficiency above 99 % for > 30 % load with peak efficiency of 99.26 %. Measurements were taken on the prototype shown in **Fig. 9** using a *Yokogawa WT3000* power analyzer.

over a wide range of output currents. A peak efficiency of $\eta = 99.26\,\%$ (error range: 98.80 % - 99.74 %) was measured for $I_1 = 12.5\,\mathrm{A}$ and $\eta = 99.16\,\%$ (error range: 98.84 % - 99.49 %) at rated load $I_1 = 20\,\mathrm{A}$.

IV. Conclusion

This paper describes a three-phase buck-type unity power factor SWISS Rectifier with interleaved dc-dc converter output stages. The system allows a single-stage conversion from the three-phase mains to a lower dc voltage. Using interleaved dc-dc converter stages reduces the input current and voltage ripples which improves the ac input current THD and reduces the dc output current ripple. Furthermore, the required dc output inductors can be combined into a current compensated Integrated Common Mode Coupled Inductor (ICMCI) and a differential mode inductor. Based on this approach a high efficiency interleaved SWISS Rectifier for dc distribution and power supply systems is designed, achieving a power density of $4\,\mathrm{kW\,dm^{-3}}$. Measurements taken on a prototype verify an efficiency of 99.16 % (±0.32 %) at nominal operation with 8 kW dc output power and a peak efficiency of 99.26 % (±0.48 %). Note that for a similar 5 kW three-phase buck-type rectifier, based on Si MOSFETS and SiC diodes, an efficiency of 98.8 % and a power density of $2.2\,\mathrm{kW\,dm^{-3}}$ were reported in [11]. However, further research is required to assess potential benefits regarding efficiency and/or power density which could result from novel wide band-gap semiconductor devices such as monolithic bidirectional switches which could be used in the IVS [21].

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