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***Abstract*—Solid-State Transformers (SSTs) are a promising technology since they enable a reduction in weight and volume of transformers while integrating new functionalities and services in the grid. However, a new kind of electric stress for the insulation occurs in this type of power converter, given that low-frequency medium-voltage stresses are mixed with high-frequency stresses generated by the converter's switching actions. This paper analyzes, in time and frequency domains, the voltage stresses appearing in cascaded converters, employing converter cells based on two-level or three-level bridge legs. The highest electric fields occur in the medium-frequency transformers of the converter cells' DC-DC converters, which provide galvanic isolation within the SST. Numerical simulations of the electric field distributions in these transformers are presented for the different frequency components and the impact of the converter topology on the insulation stress is highlighted. Furthermore, it is shown that the dielectric losses of the transformer can be neglected despite the presence of high-frequency harmonics. Finally, a transformer insulation concept based on semiconducting tape is proposed.**

***Index Terms*—Solid-State Transformers, Multi-cell converter, Medium-frequency transformer, Electric field, Insulation.**

I. Introduction

The need to integrate renewable energy sources into the grid and the progress of the semiconductor technology has caused interest in the idea of Solid-State Transformers (SSTs). SST technology has many advantages over conventional low-frequency (LF) transformers, such as, e. g., reduced weight, availability of a low-voltage (LV) DC bus and, most important, control features such as power flow control or active filtering [1]–[3]. Various topologies are suitable for the construction of an SST, but since high-voltage semiconductors are not available yet, a series connection of medium-voltage (MV) devices or a multi-cell converter approach is required. Multi-cell converters offer a great flexibility, redundancy, a multilevel voltage waveform on the grid side [4], and can take advantage of the fast switching capabilities of new $1.7 - 3.3\,\mathrm{kV}$ SiC devices [5].

The design of SSTs has already been examined with respect to the topology [2], [3], the semiconductors [5], the isolated DC-DC converters [6], which are used to provide galvanic isolation by means of medium-frequency (MF) transformers, and the magnetic and thermal design of these transformers [7]–[10]. The concerns about the electric insulation of the SST, however, remain widely open. Specific parts of the SST need to insulate the complete grid voltage (low-frequency, high-voltage). Furthermore, an electric stress due to the converter's switching actions (medium-frequency, medium-voltage) occurs. The coexistence of these two kinds of stresses is called a mixed-frequency stress, and is a new kind of constraints for the insulation of power electronic and high-voltage systems. The mixed-frequency stress can lead to accelerated ageing of the insulation [11]–[14] or to a reduced breakdown strength [15]. However, so far only limited research has been dedicated to the insulation of an SST [16] or of MF transformers [17]–[19].

It is therefore interesting to analyze how the electric field distribution in insulation components is influenced by the presence of such mixed-frequency stresses. For this reason, a more detailed analysis of the voltage and field stresses occurring in an SST is required in order to locate the critical points in the insulation system (within the individual converter cells, between these cells, and between the cells and grounded parts such as the cabinet, etc.). These are expected to be found within the MF transformers, where the insulation thicknesses need to be small in order to improve the magnetic and thermal coupling. The MF transformer is therefore the key component of an SST with respect to the insulation coordination, and a detailed analysis is required in order to choose the insulation principle of the transformer and for the winding design.

This paper is organized as follows. First, the voltage stresses are analyzed at different points of the chosen SST designs, and the MF transformer insulation is identified as the most stressed part. Electric field simulations of the transformer are carried out, and the impact of the SST topology on the insulation stress is illustrated. The dielectric losses in the transformer are estimated. Finally, a frequency-dependent insulation system, specially adapted for mixed-frequency stress, is proposed.

II. Considered SST

The limited availability of efficient high-voltage power semiconductors (i.e. blocking voltage higher than $3.3\,\mathrm{kV}$) implies that a series connection of switches is required in order to deal with the MV grid voltages levels. Most of these topologies lead to mixed-frequency stress in the insulation. In this paper, the analysis is carried out considering cascaded full-bridges topologies, which feature input series, output parallel (ISOP) structure. However, the results can also be extended to other topologies.

The considered SST is designed for a connection to the $10\,\mathrm{kV}$ MV grid. Fig. 1 gives an overview on the converter structure. Each of the cells comprises an AC-DC stage and an

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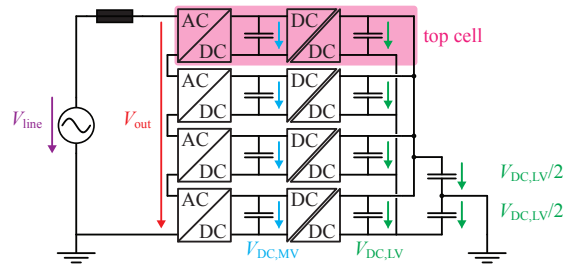

Fig. 1. One phase of the considered SST topology where each cell has an AC-DC and a DC-DC converter. The top cell is located at the MV end of the stack and is particularly important for insulation considerations.

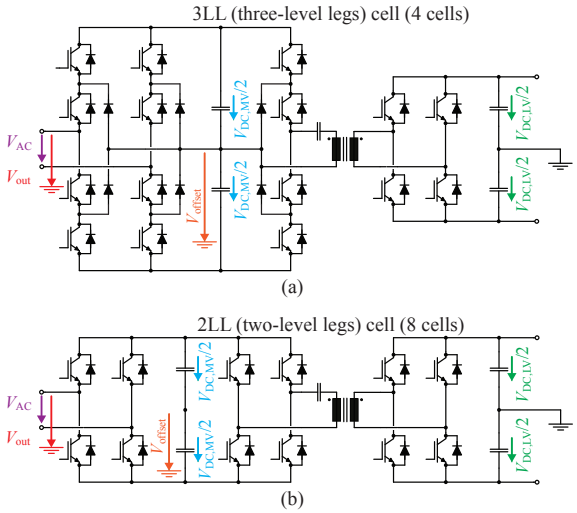

Fig. 2. Two possible realization options for the cascaded converter cells (top cell) based on three-level bridge legs (a) or two-level bridge legs (b).

isolated DC-DC converter, which provides galvanic isolation and part of the voltage adaption, the major share of which, however, is provided by the ISOP structure. All the insulation stress considerations are done with respect to the top cell, since it is subject to the highest voltage stress.

Figs. 2 (a) and (b) show different realization options for the cascaded converter cells. The first cell design employs three-level Neutral-Point Clamped (NPC) bridge legs (3LL) [20], [21] on its MV side, whereas the second design uses two-level bridge legs (2LL). Power modules with the same voltage rating are used for both variants, implying that the number of cells with 2LL is two times higher than with 3LL cells. The required DC-link voltage, $V_{DC,MV}$, is 1100 V for the variant with 2LL and 2200 V for the design using 3LL, corresponding to 8 cascaded 2LL cells and 4 cascaded 3LL cells, respectively. The blocking voltage of the semiconductor devices is 1100 V in both cases and thus the same 1700 V IGBTs can be selected. The chosen switching frequencies are 3 kHz for the AC-DC converter and 8 kHz for the DC-DC stages. The cell based on 2LL uses a full-bridge on the DC-DC converter's MV side, whereas the 3LL-based design features a half-bridge only. From the corresponding DC-link voltages, it follows that the MF transformer's MV side terminal voltage is the same in both cases (1100 V).

Since the scope of this paper is not to analyze the control and operation of an SST in the grid, a solidly grounded star-

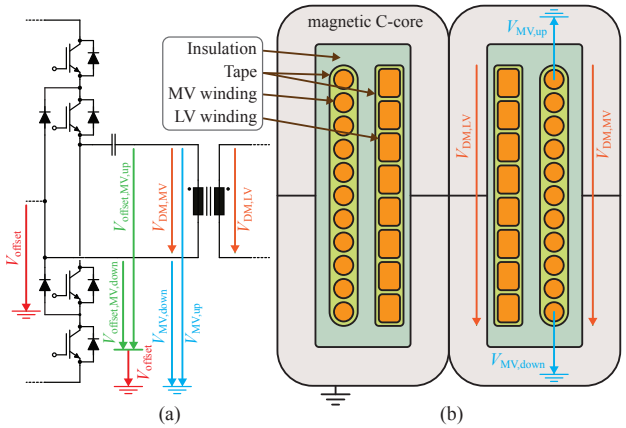

Fig. 3. Definition of the voltages within the MF transformer (top cell) (a), and cross-sectional view of the winding window of the transformer (11 : 8 ratio) with the corresponding insulation (b).

point on the MV side and a grounded DC-link midpoint on the LV side are assumed. It is thus sufficient to consider only one MV phase stack in order to assess the insulation stresses appearing within the cascaded converter structure. It should be noted that here only stresses under normal operation mode are considered. However, other constraints can arise considering a fault in the SST or a fault in the grid (lightning strike, short circuit, etc.).

III. Voltage Stresses in the SST

In order to achieve a multilevel output voltage waveform, the modulation of the cascaded cells converter is done with phase-shifted SPWM (Synchronized Pulse-Width Modulation), where the carriers are phase-shifted between the cells (interleaving) [4]. The relevant voltages for the insulation stress are defined in Fig. 2, and the voltages in the MF transformer are shown in Fig. 3 (a).

Constant DC-link voltages and ideal commutations are considered for calculating the waveforms. First, the output voltages of the individual converter cells are extracted in time and frequency domains (V_{AC}). Starting from the first cell, which features one grounded output terminal, the offset voltage, V_{offset}, i. e., the voltage between a cell's MV side DC-link midpoint and ground, of each converter cell can be computed from the superposition of the output voltages of the preceding cells (cf. Fig. 1).

A. Time Domain Waveforms

In Fig. 4, the calculated waveforms are shown for the cell placed at the top of the phase stack, where the offset voltage is maximal. The line output voltage, V_{out}, contains 17 levels with a high effective switching frequency. It can be seen that the offset voltage of the top cell contains all the switched output voltages of the series connected cells, i. e., a large 50 Hz component and high-frequency harmonics. Even though the individual cells' output voltages, V_{AC}, are different for 2LL and 3LL cells, the grid and offset voltages show a similar shape over one fundamental grid period.

B. Frequency Domain Analysis

These voltages can also be described in frequency domain. However, due to the interleaved switching and to the high

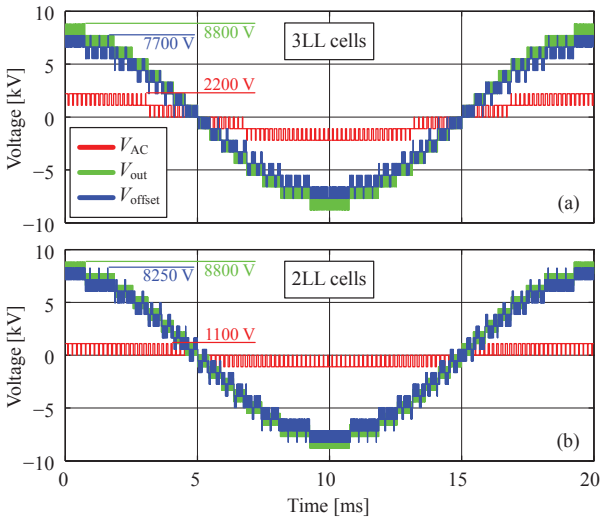

Fig. 4. Voltage waveforms in time domain for the top cell with 3LL (a) and 2LL (b) cells.

switching frequency, the gap between groups of harmonics is considerable, as shown in Fig. 5 (a) for V_{offset}. Therefore, only the total RMS value of each group of harmonics is shown in Figs. 5 (b-e). This grouping is done at frequencies where there is no aliasing between the sidebands.

The first voltage harmonics of V_{out} (cf. Fig. 5 (c)) appear at $n = 2 \cdot 4 \cdot 3000\,\text{Hz}/50\,\text{Hz} = 480$ for the design with 3LL cells and at $n = 2 \cdot 8 \cdot 60 = 960$ for the solution with 2LL cells. The amplitude of the harmonics is similar because the number of levels is the same for both designs.

The voltages appearing at the transformer's MV winding can be divided into two parts: first, there is an offset voltage between the whole winding and ground coming from all the AC-DC converter modules in the phase stack, i. e., V_{offset} (cf. Fig. 5 (b)), where it's important to notice that in contrast to the output voltage, harmonic cancellations due to interleaving do not appear for the transformer (first harmonics near $n = 60$). Secondly, the voltages resulting from the cell's own DC-DC converter, $V_{\text{offset,MV,up}}$ and $V_{\text{offset,MV,down}}$, respectively, are also present at the MV winding terminals (cf. Fig. 3 (a) and Figs. 5 (d-e)).

It should be noted that the design using a 3LL for the DC-DC converter produces an asymmetric voltage stress between the transformer terminals. One terminal is directly connected to the mid-point of the DC-link (cf. Fig. 2, $V_{\text{offset,MV,down}} = 0$), and is therefore not subject to any component from the DC-DC converter. For the DC-DC converter with 2LL, the harmonics are smaller and distributed between the two terminals due to the full-bridge configuration.

From Fig. 5, it can be seen that a mixed-frequency stress is present in the SST with a medium-voltage stress at 50 Hz, requiring an insulation voltage of 10 kV, and a medium-frequency component with insulation requirements of 2 kV (significant harmonics up to 100 kHz). With the obtained voltage stresses, the insulation stress of the SST can now be analyzed in more detail.

C. Insulation of SSTs

The cell at the top of the stack requires a higher insulation level than cells at the lower end of the stack. It would therefore be theoretically possible to adapt the cell's insulation capabilities according to their position in the stack. However, this solution is certainly impracticable regarding manufacturing and maintenance. A better option would be to make temporal permutations of the cells in order to achieve an equal ageing of the insulation among the cells. This way, the complete insulation design can be done with the top cell.

A critical point is the reference voltage of the cells. Each cell should have a ground connection due to the output parallel structure. For safety reasons, it is desired that the frame of the cell is grounded. The potential of the baseplates of the semiconductor modules is also important for the insulation stress. The MV side cooling plates of the power modules cannot be grounded because the IGBT baseplate insulation is not able to withstand 10 kV [22]. For this reason, the cooling plates need to be connected to the DC-link midpoint of the cell, thus removing the mixed-frequency stress from the semiconductors.

The remaining component is the MF transformer, where the mixed-frequency stress cannot be removed due to the ISOP structure. In order to achieve a good magnetic coupling and a good thermal conductivity, the space between the MV winding, the LV winding and the core should be as small as possible. For these reasons, the insulation within the MF transformers will experience the maximum stresses. Therefore, the next section will examine in detail the field distribution inside the MF transformer of the top cell.

IV. Electric Field in the MF Transformer

A. Transformer Design

An important aspect for the insulation of the transformer is the potential of the core. If the core has a floating potential, then both windings need to provide the complete insulation strength. Another solution is to use two C-shaped cores with an air gap. In this case, one C-core carries the MV winding and is fixed to the cell's MV side DC-link midpoint potential, the other core carries the LV winding and is grounded [18]. Consequently, no insulation between the windings and their respective cores is required. However, the insulation material needs to be placed between the cores, resulting a large air gap. The resulting spacing between the windings leads to higher leakage inductance, considerable stray field, and the large air gap creates large magnetizing currents. In addition, cooling the windings by means of metal elements results in high losses due to the high magnetic fields lying between them [7].

Therefore, a conventionally-shaped transformer based on an E-core with concentric windings has been chosen (cf. Fig. 3 (b)). The E-core is grounded and therefore the LV winding has to be isolated only for the potential of the LV DC-link, whereas the MV winding needs to withstand the full mixed-frequency MV stress. This design allows a separate manufacturing of the winding assembly, allowing a completely isolated winding bobbin to be inserted in the core.

It is important to notice that the power ratings of the transformers are different for the two types of cells (3LL or 2LL SSTs have a different number of cells). Nevertheless, both transformers have the same voltage level (cf. Fig. 5 (b)) implying that the insulation of the winding window is similar for both cases. Since the magnetic properties do not interfere with the electric field computation, it is possible to make the

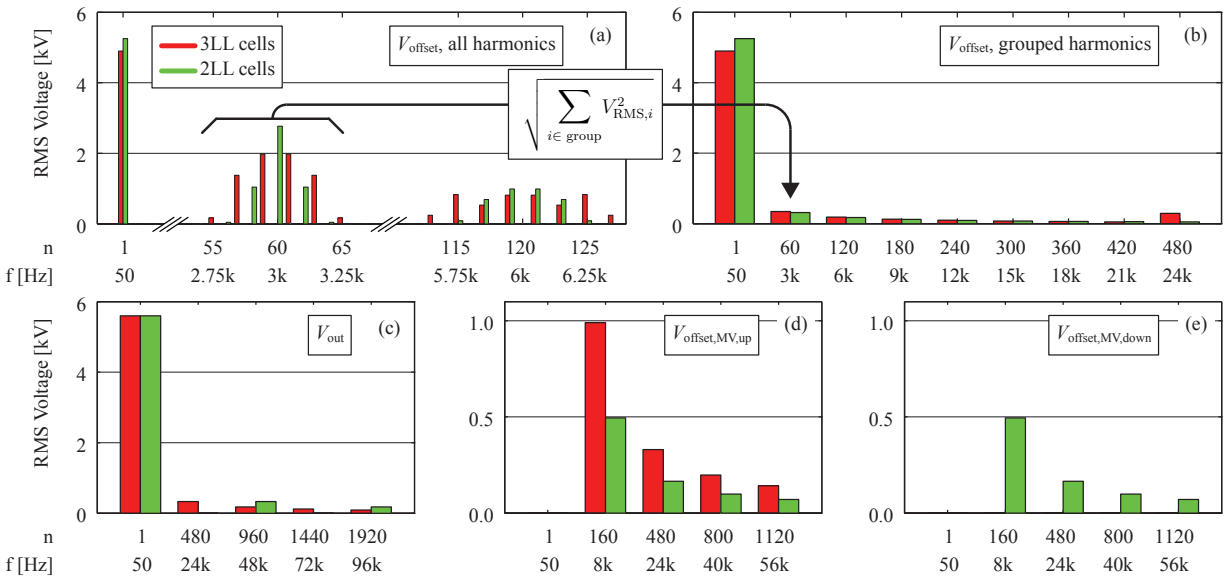

Fig. 5. RMS value of voltage harmonics for the cell placed at the top of the stack for all harmonics (a), and for grouped representation (b-e).

TABLE I
INSULATION STRESS WITH 3LL AND 2LL CELLS WITHOUT/WITH SEMICONDUCTING TAPE.

Type	Unit	without tape		with tape	
		3LL	2LL	3LL	2LL
Time Peak (space max.)	[kV/mm]	3.82	3.82	3.43	3.41
RMS LF (space max.)	[kV/mm]	2.12	2.27	1.87	2.00
RMS MF (space max.)	[kV/mm]	0.53	0.34	0.53	0.34
Losses LF (space max.)	[kW/m^3]	0.88	1.01	0.68	0.78
Losses MF (space max.)	[kW/m^3]	19.7	13.1	19.8	13.3
Losses LF (total)	[W/m]	0.17	0.19	0.18	0.21
Losses MF (total)	[W/m]	2.26	2.31	2.27	2.32
Losses (total)	[W/m]	2.43	2.50	2.45	2.53

field simulation for the same winding window. This enables a direct comparison of the electric field patterns.

The field analysis is performed for a simple transformer with epoxy ($\epsilon = 3.5$ [23]) as a homogeneous insulation material (without the tape shown Fig. 3 (b)). The resulting transformer window is analyzed be means of 2D-FEM in time and frequency domains. All the fundamental results of the next sections are summarized in Tab. I (case without tape) for allowing a comparison between the topologies.

B. Base Fields

The computation of the electric field can be split into three parts: the common mode (CM) voltage against the core of the transformer (grounded) and the differential mode (DM) voltage across the MV and LV windings (cf. Fig. 3). Since there is no CM LV excitation, the corresponding field simulation is not necessary.

From the three corresponding field distributions (base fields), it is possible to construct all the desired voltage distributions by superposition if a linear voltage distribution along the windings is assumed. This is correct if the inductances and the capacitances are equally distributed and if the resonances of the transformer are not excited. The resulting static, i.e. not frequency dependent, electric field distributions can be seen in Figs. 6 (a-c) for normalized voltage excitations. Since the winding window is symmetrical, only the upper half is shown. For the DM component, the stress is mainly located at the top of the windings and for the CM component between the winding and the core.

C. Transformer Stress in Time Domain

In order to obtain the maximal stress in time domain, the superposition of the three base fields is done for the critical instant (maximal CM and DM components with the same sign). The corresponding field is shown in Fig. 6 (d), where the maximal field is 3.82 kV/mm, which is an acceptable value for epoxy (with a margin for fault conditions [23]).

In Fig. 4, it can be seen that the maximal value of V_{offset} is 7700 V for 3LL and 8250 V for 2LL cells. However, for the 3LL cell, V_{offset} is only one part of the CM voltage that the transformer needs to withstand (cf. Figs. 5 (d-e)). The NPC half-bridge of the DC-DC converter adds half of the DC-link voltage as CM component (550 V from $V_{\text{offset,MV}}$). Then the total CM voltages are the same for both topologies. Since the DM component is also identical (1100 V), the maximal stress in time domain is exactly the same and Fig. 6 (d) is valid for both topologies.

Even if the above computation has been made with superposition of vector fields, a simple approximation of the maximal field is possible. The critical point is located at the MV winding, therefore the impact of the LV winding DM excitation can be neglected. Since the field at the winding boundary is radial, the vector sum between CM and DM components for the MV winding can be transformed into a scalar sum. With the maximal value of the base field plots and the CM/DM components as defined above the approximated maximal stress is:

$$\begin{aligned} E_{\text{max}} &\approx V_{\text{CM,MV}} \cdot E_{\text{CM,MV}} + V_{\text{DM,MV}} \cdot E_{\text{DM,MV}} \\ &\approx 8250\,\text{V} \cdot 434\,\text{kV/mm} + 1100\,\text{V} \cdot 219\,\text{kV/mm} \\ &\approx 3.82\,\text{kV/mm}, \end{aligned} \quad (1)$$

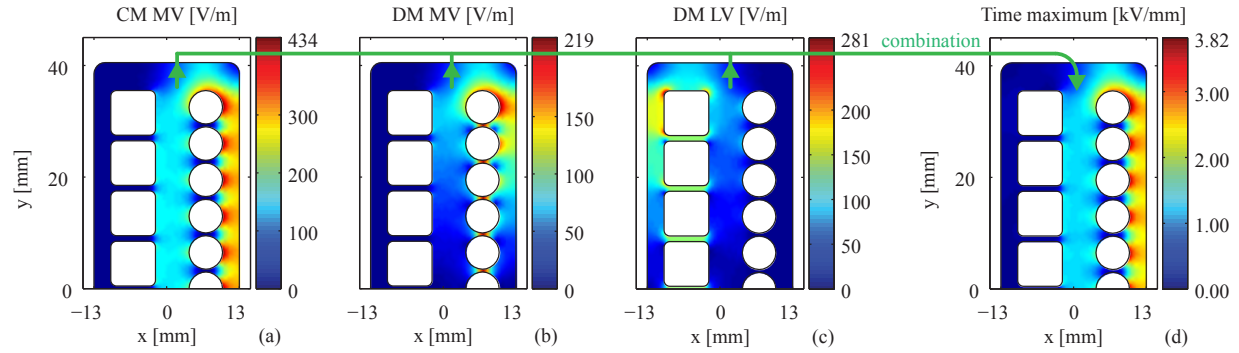

Fig. 6. Electric field for a CM excitation (1 V) of the MV winding (a), DM excitation ($[-0.5\,\mathrm{V}, 0.5\,\mathrm{V}]$) of the MV (b), and LV (c) windings. The combination of (a-c) with the voltage excitations gives the maximal field in time domain (d). Since all fields are symmetrical, only half of the winding window is shown in each case.

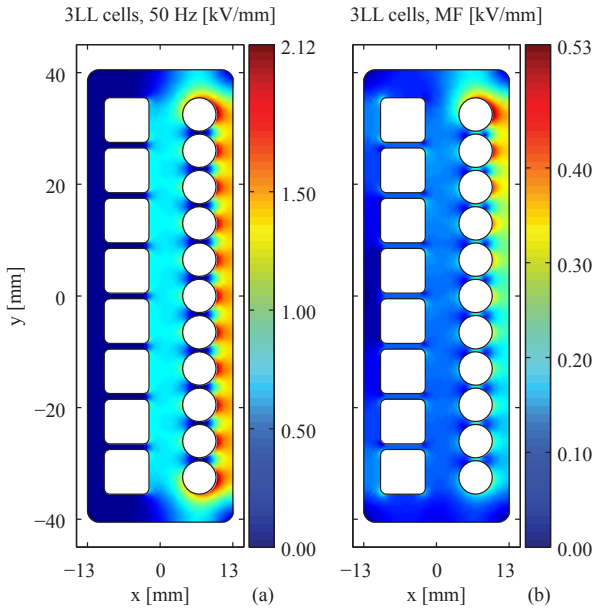

Fig. 7. RMS electric field for the grid frequency (a) and MF components (b) with 3LL cells.

where $E_{\mathrm{CM,MV}}$ and $E_{\mathrm{DM,MV}}$ are the maximum field for a normalized excitation (cf. Fig. 6). This is a good approximation of the vector sum (about $0.1\,\%$) deviation). This approximation can also be used for obtaining an estimate of the maximal field stress from FEM simulations. However, the maximal electric field is present only at a certain instant. For a comprehensive insulation stress study, the field should also be analyzed in frequency domain.

D. Transformer Stress in Frequency Domain

The high-frequency electric field can cause a premature ageing of the insulation materials [11]–[14]. For this reason, it is important to evaluate the stress at grid frequency and at higher frequencies separately. With the voltage harmonics from Fig. 5, the total RMS electric field can be computed for the grid and converter frequencies separately. The results are shown in Fig. 7 for 3LL and in Fig. 8 for 2LL cells.

The MF field contains the components from the AC-DC and from the DC-DC converter modules while the $50\,\mathrm{Hz}$ part comes only from the AC-DC converters. The $50\,\mathrm{Hz}$ voltage component

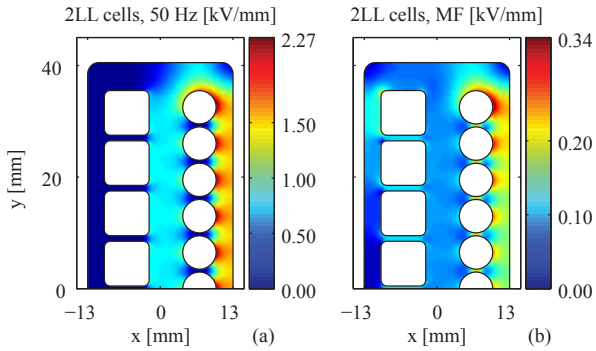

Fig. 8. RMS electric field for the grid frequency (a) and MF components (b) with 2LL cells. Since the fields are symmetrical, only half of the winding window is shown in each case.

is a pure CM voltage (from V_{offset}), but the MF components are a combination between CM and DM components (different mix for the different harmonics). This implies that the field distribution in the transformer is frequency-dependent, i.e. there are different field patterns at different frequencies, even if the base fields from Figs. 6 (a-c) are static.

It can be seen that magnitude-wise, the main stress is between the MV winding and the core. The low-frequency stress magnitude is about four times higher than the MF stress. For the MF component, the stress is not symmetrical with respect to the winding window height for a DC-DC converter based on a 3LL, due to the asymmetry of the voltage (cf. Figs. 5 (d-e)). With 2LL, the maximal MF RMS electric field is reduced by $35\,\%$, implying that this topology has a better utilization of the insulation. However, with 2LL, the fundamental harmonic of the AC-DC converters is larger with respect to the 3LL cells variant (due to the larger number of cells). This leads to a slightly higher LF field.

Please note that even if the MF RMS stress is not the same for the two examined topologies, the maximum value (in time domain) of the electric field is equal as shown above. These results are compatible with the time domain results because the RMS field does not give any information about the peak value of the electric field.

For the computation of the RMS field, all the harmonics have the same weight. However, the high frequency components can lead to an accelerated ageing due to dielectric losses or partial

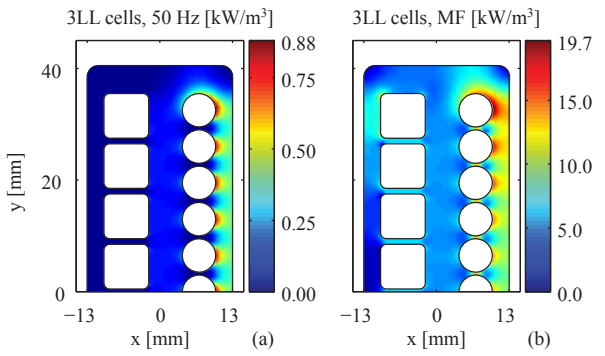

Fig. 9. Loss density for the grid frequency (a) and MF components (b) with 3LL cells. For saving space, only the upper part (where the losses are larger) of the winding window is shown even if the losses are not symmetrically distributed.

discharges [12], [14]. For this reason, the computation of the dielectric losses is also interesting.

E. Transformer Dielectric Losses

The magnetic and ohmic losses of the transformer have already been analyzed in detail [7], [8]. However, the question of dielectric losses remains open for the case of mixed-frequency stress, where the presence of MF harmonics could also lead to increased losses. The dielectric loss density can be expressed as

$$p = 2\pi f \cdot \tan(\delta) \cdot \epsilon \cdot \epsilon_0 \cdot E_{\text{rms}}^2, \tag{2}$$

where $\tan(\delta)$ is the dielectric loss tangent. The harmonics of the electric field are decreasing with $\sim 1/f$ (cf. Fig. 5) and therefore the losses are scaling with $\sim f/f^2$. The spectral distribution of the losses per length of the winding window is computed for a conservative choice of the loss factor ($\tan(\delta) = 0.02$ for epoxy [23]). For dielectric losses, the high frequencies have more impact than for the RMS field, giving an insight for the ageing of the insulation [24].

Fig. 9 shows the spatial distribution of the losses (with 3LL cells), where all the MF frequency losses are added together. Even if the LF RMS field was dominating, the MF field generates more losses showing the impact of the mixed-frequency stress. It can also be seen that the dielectric losses are mainly located near the windings, given that the losses are proportional to the square of the electric field.

The spatial losses can be integrated over the winding window in order to have the spectral distribution of the losses as shown in Fig. 10. It can be seen that the losses are mainly generated from the grid frequency and the switching of the DC-DC converter (comparison with the harmonics of Fig. 5). With 3LL cells the losses around $n = 480$ are due to the AC-DC converters (V_{offset}) while these losses are located around $n = 960$ with 2LL cells. The 3LL cell has more losses due to the DC-DC converters but less due to the AC-DC stages such that the total losses are similar for both variants (around 2.5 W/m, see Tab. I).

However, the dielectric losses are not significant when compared to the core and winding losses, which are orders of magnitude higher in typical MF transformer designs [8]. Nevertheless, the dielectric losses could be used for the design of the insulation and for the diagnostic of the insulation ageing.

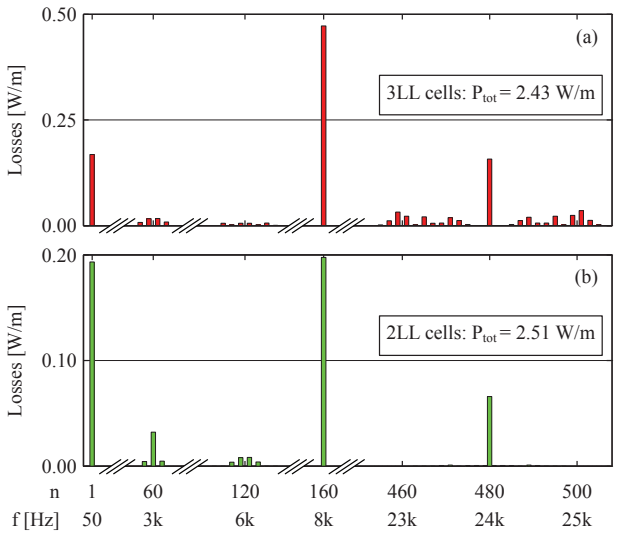

Fig. 10. Spectral distribution of the transformer dielectric losses for 3LL (a) and 2LL (b) cells.

V. Frequency Dependent Insulation

A. Insulation Concept

For the transformer insulation concept presented above, the base fields are static (cf. Fig. 6). It is possible to design a frequency dependent insulation system that is specially adapted to mixed-frequency stress. The idea is to have different responses for the grid frequency and for the switching frequencies. Such an effect can be reached with a semiconducting tape, as often done for the isolation of rotating machines [25]. A semiconducting tape features a low, but non-zero conductivity. Here, a linear tape is used (conductivity does not depend on the electric field) but similar effects could also be achieved with nonlinear tape [26]. The electrical parameters (permittivity and conductivity) are also assumed not to be frequency dependent.

At low frequencies, the tape acts as a perfect conductor, whereas for higher frequencies the displacement current dominates, implying that the tape is a dielectric. A dielectric tape has no impact on the field distribution, while a conducting tape shields the field. The proposed design is shown in Fig. 3 (b), where the two windings are surrounded by semiconducting tapes. The placement of such a tape has many advantages:

- The tape equalizes the stress near the windings, reducing the impact of some non-desired field hotspots (due to production tolerances, surface roughness of Litz wires, etc.).
- The tape can act as a barrier for partial discharges if combined with a Mica-tape.
- The stress at the grid frequency can be confined, utilizing the shielding effect, while the MF frequency stress can spread in the complete insulation.

The tape could be connected to a reference potential (typically the winding mid-point). For a MF transformer, where the dimensions are small, such a solution would lead to a complex process (field grading) for ensuring that the tape connection is not a field hotspot. For this reason, a floating tape (without reference potential) has been chosen. For the computation example shown here, a tape with a thickness of 250 µm and a conductivity of 10^{-4} S/m has been placed at

a distance of 1 mm from the windings. The computation of the field with a tape is not static anymore and needs further investigations.

B. Computation Method

The displacement and ohmic current should be now taken into account in the simulation (electrokinetics). The main challenge is the modelling of the tape. Since the tape is very thin, a meshing would lead to a high computational effort. A better solution is to model the tape as a one-dimensional object and implement the material with an additional constraint (weak formulation) on the boundary:

$$\int_{\partial\Omega} t \cdot \mathbf{J}_t \cdot \nabla_t V \, \mathrm{d}\Omega, \tag{3}$$

where t is the thickness of the tape, $\mathbf{J}_t$ the tangential current (ohmic and displacement current), V the potential (test function), and ∇_t the tangential gradient (along the tape).

An ill-conditioned matrix appears at very low frequencies, where the tape can be considered as an ideal conductor, leading to numerical problems. A solution is to detect in which frequency range the voltage drop along the tape is below a certain tolerance (0.1 % of the excitation voltage). Below this threshold, the model of the semiconducting tape is replaced with an ideally conducting tape.

In Fig. 11, the method for analyzing a frequency dependent insulation system in frequency and time domain is shown. The case of a static insulation is also illustrated (see Section IV). The fundamental ideas of the computation are:

- Computation of the base fields with FEM (CM/DM). These are independent of the excitation, such that only a reduced number of FEM simulations is required (normalized excitations).
- Compute all the fields in frequency domain since FEM is rather suited for frequency domain analysis. Since the fundamental frequency is low and since the switching transitions are fast, a time domain field simulation would be slow (cf. Fig. 4). With a frequency domain computation many harmonics can be neglected.
- Using the superposition principle, the field is computed in frequency domain (CM/DM together). Then the RMS field and the losses are extracted.
- Computation of the time domain field with inverse Fourier transform (x and y components should be treated separately). Since the fundamental frequency is very low, another inverse Fourier transforms are applied near the switching transitions for achieving a better resolution.

C. Base Fields

The voltage drop along the tape (maximum minus minimum voltages) is presented in Fig. 12 for normalized CM and DM excitations of the MV winding. The voltage drop at low frequencies is zero, implying that the tape acts as a conductor. At higher frequencies, the voltage drop converges to the value reached for the case where the tape is not activated (as done in Section IV). For a DM excitation, at high frequencies the tape follows the voltage of the different turns composing the winding, therefore the voltage drop is almost 1 V. The tape properties have been chosen such that the transition between

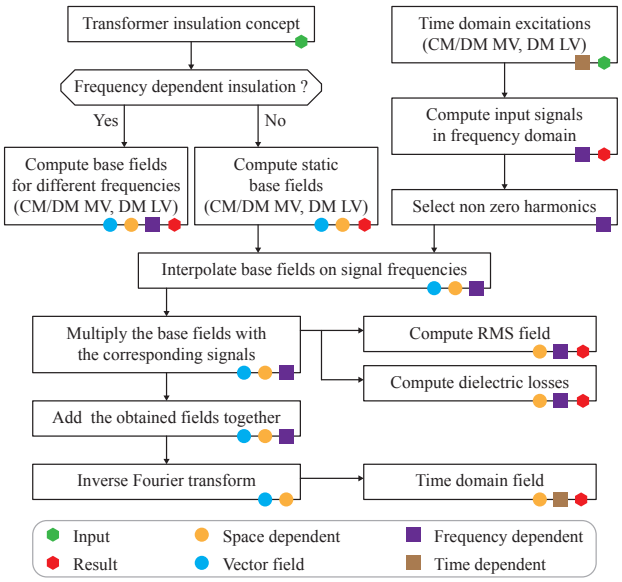

Fig. 11. Flow chart showing the computation method for analyzing a static or frequency-dependent insulation system in frequency and time domain.

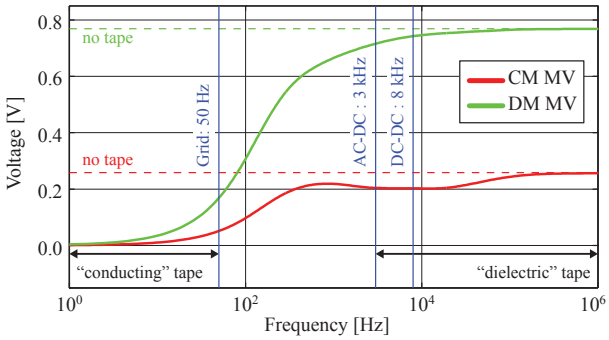

Fig. 12. Maximal voltage difference along the semiconducting tape (MV winding) for CM excitation (1 V) and a DM excitation ($[-0.5\,\mathrm{V}, 0.5\,\mathrm{V}]$). The dashed curve represents the voltage drop along the tape when it has not been activated (tape with a zero conductivity).

the conductive and dielectric domains occurs between the grid and the switching frequencies.

The base fields with the semiconducting tape are shown in Fig. 13 for the MV winding at 50 Hz and 8 kHz (DC-DC converter switching frequency). A comparison with Fig. 6 shows that the CM MV component is reduced at 50 Hz with the semiconducting tape (due to the field homogenization). The price to pay is a twice larger DM MV field at 50 Hz (because the integral of the electric field should remain equal to the applied voltage). For this reason, using a perfectly conducting tape (silver/copper tape) is not a good solution because the field pattern would look like those shown in Figs. 13 (a) and (c) for all the frequencies.

The semiconducting tape is not active anymore at 8 kHz such that the DM MV field is not higher than for the case without tape. This is the fundamental usage of a semiconducting tape for mixed-frequency stress: although the tape deteriorates the DM insulation response at the low frequencies, it has no impact because DM voltages in the MF transformer occur at higher frequencies, where the tape is not active.

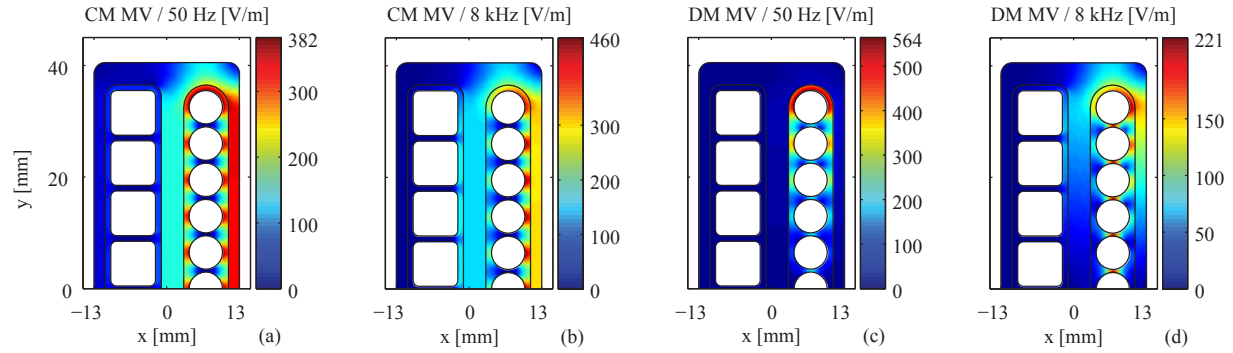

Fig. 13. Electric field for a CM excitation (1 V) of the MV winding (a-b) and DM excitation ($[-0.5\,\mathrm{V}, 0.5\,\mathrm{V}]$) of the MV winding (c-d). The insulation system with semiconducting tapes is shown at 50 Hz and 8 kHz. Since the fields are symmetrical, only half of the winding window is shown.

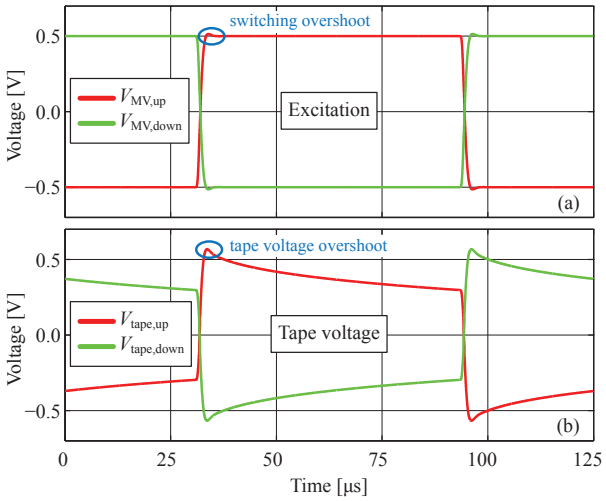

Fig. 14. DM excitation of the MV winding (a) and the corresponding voltage drop of the semiconducting tape (b). The voltages $V_{\mathrm{MV,up}}$ and $V_{\mathrm{MV,down}}$ are defined in Fig. 3, whereas $V_{\mathrm{tape,up}}$ and $V_{\mathrm{tape,down}}$ are the voltages extrema (maximum of the absolute value) along the tape near the upper and lower half of the winding window. The switching frequency is 8 kHz and the switching transitions are modeled with a small overshoot (1 µs rise time).

D. Time Domain Response

Using an inverse Fourier transform, the results in time domain can be obtained. In Fig. 14, the voltage drop across the tape of the MV winding is shown for a normalized DM excitation at 8 kHz with non-ideal switching transitions. The tape voltage follows mainly the excitation voltage, which is the goal for DM excitations as explained above. The same observation can also be made from Fig. 12 by looking at the tape voltage at 8 kHz.

After the switching transition, the tape voltage decreases because the tape is equalizing the stress of the DM component at lower frequencies. The tape voltage continues to change even if the switching transition of the excitation is completed. It is also interesting to see that the overvoltage at the tape is larger than the overshoot of the excitation. Such phenomena are possible since the problem with the semiconducting tape is not static anymore. However, with the chosen tape properties, this overvoltage is small and does not produce field hotspots.

E. Stress with SST Waveforms

The waveforms of Section III are applied to the windings with tape and the stresses are computed. All the results are summarized in Tab. I (case with tape). The comparison between the insulation with and without tape shows that the maximal stress in time domain is reduced by ca. 10 % with the tape. This reduction comes mainly from the better distribution of the LF CM voltage (as shown in Fig. 13). But as explained above, the field reduction is not the only advantage of the tape. The tape will also reduce the stress due to the non-simulated surface roughness.

The low frequency RMS stress is also reduced while the MF stress and the dielectric losses remain stable. The impact of the topologies (3LL and 2LL cells) is similar for the two proposed insulation concepts.

The insertion of a semiconducting tape should also be examined with respect to eventual ohmic losses. However, since the tape has been designed such that the ratio between the permittivity and the conductivity is very high, the corner frequency of the tape is around 1 MHz ($\omega_e = \sigma/\epsilon$). This corner frequency is the frequency where the displacement current overcomes the conduction current inside the tape and is not the transition frequency of Fig. 12, which is considerably lower. This means that there is no voltage drop in the normal direction inside the tape and that the electric field in the tape is only tangential (along the tape). This tangential field is rather small (field that makes the voltage drop along the tape) and therefore the ohmic losses are also reduced (less than 2 W/m).

The insertion of conductive elements in the insulation modifies the capacitances. Some designs with semiconducting tape are leading to an increased CM current in the transformer (for tapes with high conductivity). Since the CM disturbances are already a challenge for multi-cell SSTs [27], such an insulation system is not desired. For the presented design the increase of the CM current is less than 1 %.

With all these results, it is possible to make a recommendation for the choice of the conductivity of the tape, given that it is possible to control the electrical properties of the tape with the production process [26], [28]. The conductivity has to be chosen together with the thickness of the tape since increasing the conductivity has the same effect as increasing the thickness. For minimizing the losses, the CM current and for realizing a good MF field distribution, a tape with a low

conductivity/thickness is required. Therefore, the conductivity should be chosen as low as possible, given that the tape should still feature an almost constant voltage for the grid frequency. It can be seen in Fig. 12 that these criteria are respected for the chosen tape.

It has been shown that implementing a frequency dependent insulation concept is an interesting option for mixed-frequency stress and that semiconducting tape is a possible option to achieve this goal.

VI. Conclusion

A multi-cell SST produces voltage stresses between the cells, within the cells and between the cells and grounded parts of the SST. The insulation stress is a mixed-frequency stress, i. e., containing low-frequency MV stresses but also high-frequency components. The MF transformer isolation of the converter cell placed at the top of the phase stack is subject to the harmonics from all the other cells' AC-DC converters and from its own DC-DC converter, combined with the grid voltage.

The electric field in the transformer can be decomposed into CM and DM voltages. The superposition of the CM and DM voltages implies a frequency dependent distribution of the electric field. When compared to a DC-DC converter featuring a NPC half-bridge on its MV side, the MF electric field component can be reduced by about 35 % with a DC-DC converter using a full-bridge on its MV side, due to the resulting symmetrical stress.

Frequency dependent insulation concepts that show different responses for the grid and medium-frequency components, are a possibility for handling challenges arising from mixed-frequency stresses. A design based on semiconducting tapes has been presented. The mixed-frequency stress is also not only a constraint but also an opportunity that can be used to implement a frequency-optimized insulation coordination.

The dielectric losses can be neglected in a MF transformer; but the exact impact of the high-frequency components on the lifetime of the insulation remains unclear and will require further investigations. The knowledge of the material properties under mixed stresses will allow, with the presented electric field distribution, an optimal design of the SST isolation, and future publications will analyze this in more detail.

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