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Advanced Power Electronic Concepts for Future Aircraft and Electric Vehicle Applications

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presented by

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a Sara,

a Valeria e Antonio, i miei genitori.

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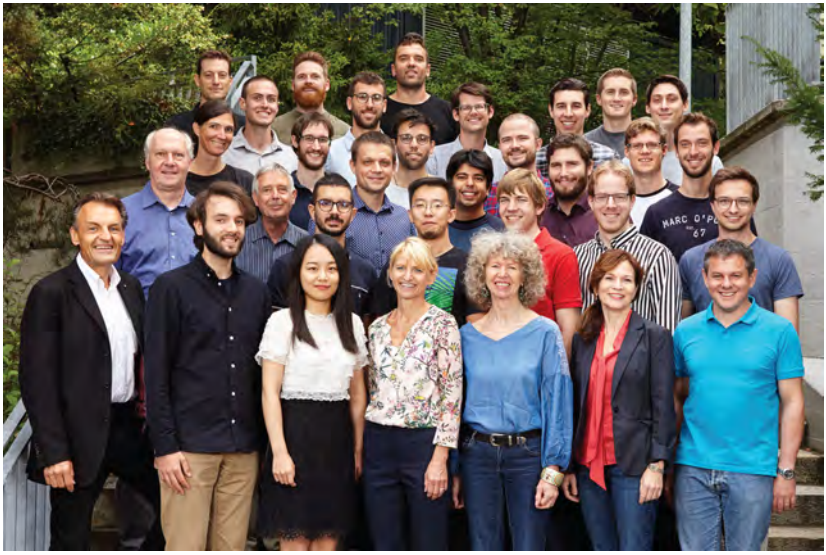
Dear Mr. Guacci,
Excellent! We are looking forward to having you as a member of our team.
Best,
Johann W. Kolar.



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Dear PES Team,
Thank you all for this unforgettable life-changing experience.
Have a nice day,
Mattia.

A beautiful body perishes, but a work of art does not.
Leonardo Da Vinci (b. 1452 in Anchiano, Italy)

Lord, grant that I may always desire more than I can accomplish.
Michelangelo Buonarroti (b. 1475 in Caprese, Italy)

Passion is the genesis of genius.
Galileo Galilei (b. 1564 in Pisa, Italy)

The best Ferrari ever built is the next one.
Enzo Ferrari (b. 1898 in Modena, Italy)

Abstract

Greenhouse gases (GHGs) produced by the transportation sector are largely responsible for the occurring climate change. Favorably, the electrification of aircraft and road vehicles can mitigate this phenomenon by improving the energy efficiency of air and road transport. The trend towards More Electric Aircraft (MEA), which embody all design solutions replacing pneumatic, hydraulic, and mechanical aircraft systems with power electronic systems, guarantees enhanced fuel economies for the air transport. On the other hand, electric vehicles (EVs) offer higher well-to-wheel efficiencies than internal combustion engine vehicles, thus also lower emissions and cost of operation. The evolution of MEA and EVs must be supported by significant advancements in the field of power electronics, since higher and higher power levels are processed on-board of electrified aircraft and road vehicles. Hence, in order to limit the energy conversion losses and the weight/volume of the power electronic systems, only converters with extreme efficiency and power density figures fulfill the requirements of these industries.

Advanced power converters employing wide-bandgap (WBG) semiconductors are identified as key enablers of the performance breakthrough desired for power electronic systems for MEA and EV applications. In particular, modular converters allow to benefit from the superior performance of low voltage power semiconductors and simultaneously ensure fault-tolerant operation, scalability, and reduced design effort. The higher switching speeds of silicon-carbide (SiC) and gallium-nitride (GaN) power transistors, instead, enable higher switching frequencies, i.e. the downsizing of the filter components, without significantly impacting the cooling requirements.

Unfortunately, beside these proven advantages, the high switching speeds of WBG semiconductors arouse several measurement and design challenges preventing the full exploitation of their potential. Moreover, still unresolved manufacturing issues translate into unexplained loss mechanisms, which compromise their high frequency operation. Accordingly, the performance limits of latest SiC and GaN devices are explored in this thesis. Also, dedicated switching and conduction loss measurement techniques are developed, and advanced design concepts are tested. The envisaged performance improvements are validated with the comprehensive analysis of advanced power converters and technologies. The ultimate goal is to identify and address the challenges inhibiting the widespread adoption of next-generation power converters based on WBG semiconductors on-board of MEA and EVs, i.e. hindering the electrification of the transportation sector necessary to limit its unbearable share of GHG emissions.

Sommario

I gas serra (GHGs) prodotti dal settore dei trasporti sono tra i principali responsabili del cambiamento climatico. Fortunatamente, l'elettrificazione di aerei e veicoli stradali può rallentare questo fenomeno migliorando l'efficienza energetica del trasporto aereo e su strada. Il trend verso i More Electric Aircraft (MEA), i quali racchiudono tutte le soluzioni progettuali volte a sostituire i sistemi pneumatici, idraulici, e meccanici di un aereo con sistemi di elettronica di potenza, assicura un risparmio di carburante per il trasporto aereo. I veicoli elettrici (EVs), invece, garantiscono un miglior bilancio energetico dal pozzo alla ruota dei veicoli alimentati da un motore a combustione interna, e quindi anche ridotte emissioni e costi operativi. Lo sviluppo di MEA e EVs richiede notevoli progressi nel campo dell'elettronica di potenza, dato che potenze elettriche sempre più elevate vengono utilizzate a bordo di aerei e automobili elettrificati. Quindi, per limitare le perdite nella conversione di energia ed il peso/volume dei sistemi di elettronica di potenza, solamente convertitori con estrema efficienza e ad alta densità di potenza soddisfano i requisiti di queste industrie.

Convertitori di potenza avanzati che impiegano semiconduttori ad ampio intervallo di banda (WBG) sono considerati elementi chiave per rivoluzionare le prestazioni dei sistemi di elettronica di potenza per MEA ed EVs. In particolare, i convertitori modulari consentono di beneficiare delle prestazioni superiori dei semiconduttori di potenza a bassa tensione, e al contempo assicurano tolleranza ai guasti, scalabilità, ed un minor sforzo progettuale. Le maggiori velocità di commutazione dei transistori di potenza al carburo di silicio (SiC) e al nitruro di gallio (GaN), invece, consentono di incrementare le frequenze di commutazione, i.e. di ridimensionare i componenti dei filtri, senza avere un impatto significativo sui requisiti di raffreddamento.

Purtroppo, al fianco di questi comprovati vantaggi, le elevate velocità di commutazione dei transistori WBG danno vita a diverse sfide progettuali e problematiche di misurazione che impediscono di sfruttare a pieno il loro potenziale. Inoltre, problemi di fabbricazione ancora irrisolti si traducono in inspiegabili meccanismi di perdita, che compromettono il loro funzionamento ad alta frequenza. Pertanto, in questa tesi vengono esplorati i limiti prestazionali dei più recenti dispositivi SiC e GaN. Vengono sviluppate, inoltre, delle tecniche dedicate alla misurazione delle perdite di commutazione e di conduzione, e vengono testati dei concetti progettuali avanzati. I miglioramenti delle prestazioni previsti vengono verificati tramite l'analisi approfondita di convertitori di potenza e tecnologie all'avanguardia. Il fine ultimo è di identificare e far fronte alle sfide che inibiscono un ampio utilizzo di convertitori

di potenza di prossima generazione basati su semiconduttori WBG a bordo di MEA ed EVs, i.e. che ostacolano l'elettrificazione del settore dei trasporti necessaria per limitare la sua insostenibile quota di emissioni di GHGs.

Abbreviations

2D	Two-Dimensional
3D	Three-Dimensional
3-Φ	Three-Phase
AC	Alternating Current
C	Carbon
Cu	Copper
DC	Direct Current
DUT	Device-Under-Test
e-mode	Enhancement-Mode (Normally-Off)
EV	Electric Vehicle
FET	Field-Effect Transistor
FoM	Figure of Merit
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistors
MEA	More Electric Aircraft
MOSFET	Metal-Oxide-Semiconductor FET
PCB	Printed Circuit Board
PFC	Power Factor Correction
PV	Photovoltaic
PWM	Pulse-Width Modulation
RMS	Root-Mean-Square
SJ	Super-Junction
Si	Silicon
SiC	Silicon Carbide
SOA	Safe Operating Area
VSD	Variable-Speed Drive
WBG	Wide-Bandgap
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Contents

1 Introduction

Burning carbon fuels produces large amounts of greenhouse gases (GHGs), which have harmful impacts on people's well-being and on the environment [1]. In fact, GHGs present in the atmosphere, such as carbon dioxide (CO_2), absorb and re-radiate solar energy to the Earth's surface, thus increasing its temperature [2]. As the concentration of GHGs climbs, climate change occurs at much higher rates than anticipated and with disastrous effects [3]. These statements are alarmist excerpts of the seventeen sustainable development goals of the United Nations [4]; particularly, of number seven "Affordable and Clean Energy" [1] and of number thirteen "Climate Action" [3].

Surpassing electricity generation and industry, the transportation sector is becoming responsible for the largest fraction of GHG emissions caused by human activities. E.g. in the US in 2017, 28.9 % of the total 6.5 Gt of CO_2 equivalent were generated by the transportation sector [5]. GHG emissions from transportation primarily originate from burning fossil fuel for road vehicles, ships, trains, and planes [5]. Given the undergoing demographic change and rapid urbanization, transport-related GHG emissions could increase at a faster rate than emissions from all other energy end-use sectors, and around 12 Gt of CO_2 equivalent per year could be reached worldwide by 2050 (compared to today's 8.1 Gt) [6]. Accordingly, sustained policies must be immediately implemented to meet the aggressive GHG emission reduction targets defined by political agenda around the world, which are essential to counteract the consequences of the occurring climate change [7, 8].

Mitigation potentials are identified in the increase of the energy intensity, i.e. in the improvement of the performance efficiency, of aircraft and road vehicles, and in the reduction of the fuel intensity, i.e. in the migration to lower carbon fuels and energy carriers, e.g. using sustainably produced elec-

tricity [7]. The latest advancements in power electronics described in this thesis are key enablers of the described strategies. In fact, they facilitate the widespread diffusion of EVs and next-generation aircraft technologies, by improving their performance. Advanced power electronic concepts for future aircraft, e.g. MEA, and EV applications are hence investigated to accelerate the advent of sustainable transport [9]. The ultimate goal of this thesis is to contribute to the reduction of GHG emissions generated by the transportation sector, i.e. to improve the environmental conditions on our planet.
Brief overviews of current and future trends in MEA and EV technologies are introduced in **Section 1.1** and **Section 1.2**, respectively. Hence, the key challenges, i.e. the desirable advancements in power electronics, motivating this work are described in **Section 1.3**. The main contributions of this thesis are presented in **Section 1.4**, before summarizing the content of each chapter in **Section 1.5**. Finally, all publications created as part of this thesis, or in the scope of related projects, are listed in **Section 1.6**.

1.1 Next-Generation Electric Aircraft

Air transport is one of the main sources of GHG emissions in the transportation sector, second only to road transport [10]. Even though civil aviation contributes to CO_2 emissions with a significantly smaller fraction than cars, e.g. 13.4 % compared to 60.7 % in Europe in 2016 [10], other data highlight the severity of the current status of this industry. First, the primacy of air transport in GHG emissions per passenger and traveled km; a long-haul flight, in fact, causes comparable GHG emissions than all its passengers potentially undertaking the same journey by car individually, i.e. with one passenger per car, and approximately thirty times more emissions than a train covering the same distance [11]. Since most of the GHG emissions occur during take-off and landing, the comparison is even worse for short-haul flights [11]. Second, there is no convenient alternative to air transport for long-haul flights in a foreseeable future, hence, at the moment, there is no possibility to mitigate these GHG emissions with a modal shift of the population [12]. Third, the continuous growth of the sector experienced in the last decades and forecast for the next ones, i.e. the 3.8 billion air travelers of 2016 are expected to become 7.2 billion by 2035 [13], is so significant that even the most optimistic scenario cannot hope to reverse the emissions growth [14]. Accordingly, air transport will be inevitably responsible for a larger and larger share of GHG emissions in the future.
Possible countermeasures to slow down, if not revert, this negative trend,

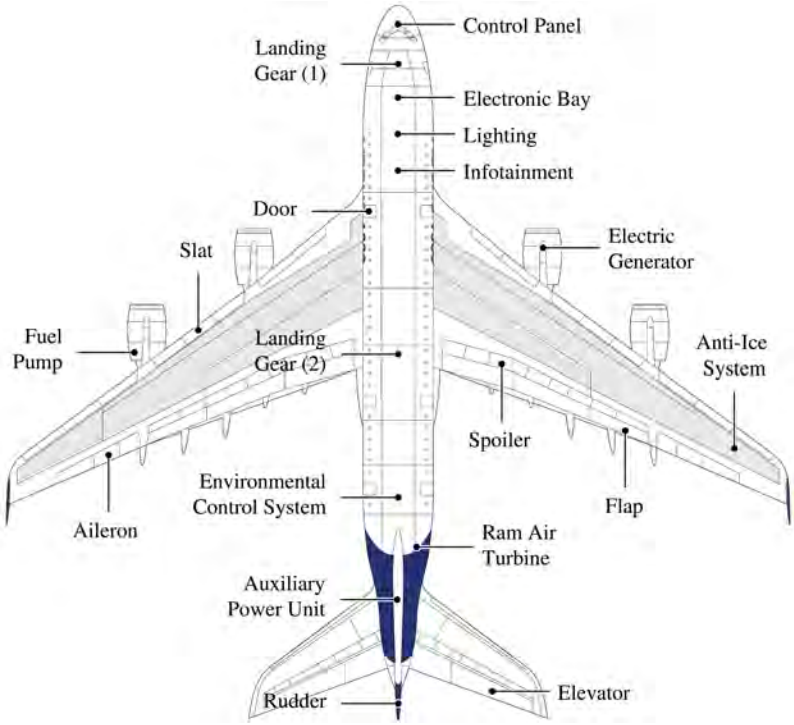


Fig. 1.1: Electric/electronic systems present in conventional aircraft and electrified systems in MEA.

require advancements in different areas, e.g. in material science to reduce the aircraft weight, in chemistry to develop low carbon fuels, in fluid dynamics to optimize the aircraft profile, etc. [15]. As well, significant improvements are desired in aircraft power architectures and engine performance technologies, aiming to significantly enhance energy utilization and fuel economy [16]. In this context, the inherently higher efficiency (and lower maintenance effort) of electric systems led, in the last two decades, to the continuous electrification of air transport [16]. This trend is often described with the concept of MEA, which embody all design solutions aiming to maximize the use of electricity for all aircraft systems, as indicated in **Fig. 1.1**. In MEA, the non-propulsive energy demand, traditionally split between pneumatic, hydraulic,

mechanical, and electric systems, is entirely provided by electric systems [17]. In particular:

- The pneumatic system (typically rated for 1.2 MW on a short-haul conventional commercial aircraft [17]) is usually supplied from bleed air extracted from the engine, and is used to power the environmental control system (ECS), and the anti-ice system [17]. In a bleed-less MEA architecture, an electro-thermal ice protection scheme replaces the flow of hot bleed air through the wings necessary to de-ice them, also reducing drag and noise [18]. Additionally, the air conditioning and cabin pressurization systems, part of the ECS, are powered by electrically driven compressors [18]. This approach significantly reduces the losses occurring in a bleed system; since all the high speed air produced by the engine is converted into thrust, excessive energy extraction is avoided, given that only enough power as needed is produced, and a more efficient secondary power extraction method is adopted [18]. Moreover, the weight of the aircraft is reduced, since the ducting used to pass the pressurized air around the airplane is removed.
- The hydraulic system (240 kW [17]) is used to move the aircraft flight control surfaces, e.g. rudder, ailerons, elevators, and flaps, in order to control the direction of flight, and to power the retraction, steering, and braking of the landing gear [17]. Inline with the trend towards MEA, parts of this system can be locally replaced by electro-mechanical and electro-hydrostatic actuators [17]. In this case, the losses originating from continuously ensuring a defined pressure level for actuation are avoided, and the weight of the aircraft is reduced given the absence of corrosive fluids.

Several other advantages are introduced by MEA concepts, i.e. by the replacement of pneumatic, hydraulic, and mechanic systems, with more flexible electric power converters and actuators. The resulting lower aircraft weight ensures expanded range and reduced fuel consumption [16]. The limited part count lowers maintenance costs, simplifies the installation, and improves the system reliability [16]. In fact, during fault conditions, electric systems are able to maintain their functionality by automatic reconfiguration, and generally provide a much faster response to changes in power demand. Finally, advanced diagnostics and prognostics is possible, since electric systems are able to provide constant monitoring during operation [16].
The interest of the aircraft industry in MEA, as well as the research progress in this area, is confirmed by the substantial growth of the overall electric

Fig. 1.2: Two prototypes testing all-electric and hybrid propulsion technologies. **(a)** The E-FaN from *Airbus* and *Siemens*, an all-electic 60 kW two-seater. **(b)** The E-FaN X from *Airbus*, *Rolls-Royce*, and *Siemens*, a flying testbed for a 2 MW electric motor.

power rating of on-board systems in commercial planes. While 100 kW were typical before 1980, 500 kW were surpassed in 2004 with the *Airbus* A380, and finally the milestone of 1 MW was achieved in 2010 with the *Boeing* B787 [16]. These values are approaching a significant fraction of the propulsive power, typically in the range of few tens of MW [17]. In these designs, the major technological breakthrough consists of replacing the current multi-modal systems with electric circuits controlling all functions of the aircraft, both on the ground and in flight [19].

The next logical step in the electrification of aircraft is the hybridization of the propulsive power, e.g. with all-electric, hybrid, and turbo-electric architectures [15]. Few manned electric aircraft prototypes were developed since 1973, and several single/two-seater airworth-like demonstrators were realized in the last decade [15]. All feature propulsive power ratings between few tens and few hundreds of kW, i.e. significantly lower than the ones of typical short-haul conventional commercial aircraft, and a limited range imposed by the physical constraints on the take-off weight (TOW) [15]. E.g. in 2014 *Siemens* developed the all-electric E-FaN (see **Fig. 1.2(a)**), a two seater with a maximum TOW weight of 600 kg, a flight time of 1 h, and a propulsive power of 60 kW provided by two electric motors supplied by 250 V batteries [15].

The most remarkable project in the electrification of a commercial aircraft is the E-FaN X (see **Fig. 1.2(b)**) [20, 21]. This is the result of a partnership among *Airbus*, *Rolls-Royce*, and *Siemens* aiming to realize an hybrid-electric flying testbed for a 2 MW electric motor supplied by a gas turbine and a large battery pack. The demonstrator is intended to explore the challenges of high power electric propulsion systems [15], and intends to make the technology to fly a hundred passenger aircraft, based on electric and hybrid technologies,

available by 2040. The final goal of the project is to halve the aviation industry's CO_2 emissions by 2050, by using alternative propulsion systems [22]. Finally, electrification enables aircraft concepts that are not currently served with conventional propulsion architectures, e.g. for noise and cost reasons [23]. An example of this new trend, which could allow point-to-point urban air mobility in a near future, is represented by electric vertical take-off and landing aircraft (eVTOLs). More than hundred eVTOL concepts have been proposed in the last years, with some already proving their operation in test flights, e.g. *Lilium* Jet and *Airbus* Vahana [23].
In general, with the established trends towards MEA and aircraft featuring hybrid or all-electric propulsion, the total on-board electric power budget, already ranging from several hundreds of kW to few MW, is bound to rapidly increase even further, e.g. to tens of MW. As a result, state-of-the-art and future aircraft electric systems face enormous challenges related to power generation, distribution, and consumption, but as well constitute the only viable option for the sustainable growth of the aircraft industry. The electric system of MEA, e.g. of the *Airbus* A380, described herein as an example, is a complex system comprised of both DC and AC architectures [16]. Several buses distribute the electric power along the aircraft, i.e. 230 V AC-buses directly supplied from the generators connected to the two propulsion engines, ±270 V high voltage DC-buses powered from AC/DC rectifier units connected to the AC-buses, and 28 V low voltage DC-buses regulated from DC/DC converters connected to the high voltage DC-buses or directly powered from batteries [16]. Hence, low power DC-loads are typically connected to the low voltage DC-bus, while high power AC-loads, requiring 115 V, are supplied either from DC/AC inverter units connected to the high voltage DC-buses, or directly through auto-transformers connected to the AC-buses [17]. Accordingly, dozens of power electronic elements, i.e. the generators and all the AC/DC, DC/DC and DC/AC power converters, as well as the cables, energy storage elements, circuit breakers, etc., are installed on-board of MEA, and are responsible for an efficient power generation and distribution [16]. This electric system, with an overall power rating of up to 1 MW, must be designed to operate at the highest possible efficiency in order to meet the reduced fuel burn and thus GHG emissions goals [24]. Additionally, components with extreme power density are required to minimize the system weight, since this helps to further reduce the fuel consumption [24]. In particular, system efficiencies raging from 98.0 % to 99.3 % and gravimetric power densities from 16 kW/kg to 23 kW/kg are identified by several studies as minimum requirements to effectively support the development of hybrid-electric propulsion

systems in commercial aircraft [25]. Similar targets are also key enablers for the further development, e.g. for the increase of range and payload, of next-generation all-electric aircraft and eVTOLs.

1.2 Electric Vehicles: Past, Present, and Future

The first prototype of road vehicle powered by an electric motor can be traced back to 1828 [26]. In the following decades, EVs were further developed and became very popular at the end of the XIX century. Even if less noisy and smelly than their gasoline powered counterparts, they suffered from a lower speed, i.e. 20 km/h, and a limited mileage caused by the low energy density, high price, and poor reliability of the battery technologies available at the time. For these reasons, EVs were completely abandoned at the beginning of the XX century in favor of traditional internal combustion engine (ICE) powered vehicles. A similar but shorter historical cycle repeated around 1960, but ended with an analogous outcome. Only in the late 1990, significant advancements in battery technologies, as well as the development of an environmental consciousness, i.e. a growing sense of environmental responsibility, motivated new interest in EVs [27, 28].
Modern research leveraged on the higher tank-to-wheel and well-to-wheel efficiencies, and on the reduced life cycle emissions of EVs compared to ICE vehicles [8]. These benefits become more significant when the electric energy necessary to recharge the battery is provided by renewable sources [29]. Despite the higher cost, inferior mileage, and the lack of adequate charging and grid infrastructures, this era is still identified as the beginning of the electric revolution of road transport, since drastic improvements in vehicles electrification coincided with a radical transformation of the understanding of mobility [8].
Tightening government GHG emission regulations and subsidies supported the continuous exponential growth of the EV market in the last two decades [27,28]. Additionally, several other advantages favored the market penetration of EVs, e.g. the reduced maintenance and cost of ownership, the fuel economy and independence, and the energy security [30, 31]. Hence, the diffusion of EVs motivated the development of a capillary charging infrastructure [32]. Moreover, economy of scale, e.g. large volume manufacturing, and large investments facilitated the cost reduction [8]. Accordingly, the cost cross-over point (between an EV and an equivalent ICE vehicle) is expected in the next five years, while the consequent sales cross-over point is forecast in the next twenty years [8, 33].

Fig. 1.3: The two most sold models of BEV and HEV in the US market in 2019 [34]: **(a)** the Tesla Model 3 and **(b)** the Toyota Prius Prime, respectively.

Two main categories of EVs are nowadays available (see **Fig. 1.3**). Battery EVs (BEVs) are fully-electric vehicles without an ICE. In these vehicles, the only source of energy used to power all on-board components, as well as the traction electric motor(s), is a high capacity battery pack [35]. This battery is charged from an external source, either directly, i.e. according to Level 3 (DC fast) charging standards, or indirectly, through an on-board battery charger, i.e. according to Level 1 or Level 2 (AC) charging standards [36]. Differently from BEVs, hybrid EVs (HEVs) have an additional on-board energy storage element, e.g. a gasoline tank, and power source, such as an ICE. An opportune control algorithm instantaneously decides, depending on the driving conditions, the power flow configuration ensuring the best vehicle performance and fuel economy [35]. E.g. in a parallel hybrid architecture, the driving power can be provided both from the electric motor and from the ICE in variable shares, while the ICE can as well charge the battery (with the electric motor operating as generator) [35]. In a series hybrid architecture, instead, the ICE is used only as a range-extender to charge the battery, i.e. it is operated as generator in a high efficiency operating point, while the driving power is provided only by the electric motor, which is directly connected to the transmission [35]. Often, regenerative braking is a second source of power and can be used to charge the battery [35]. Plug-in HEVs (PHEVs) are a variant of HEVs in which the battery can be additionally charged from an external (off-board) energy source, e.g. a power outlet, as in a BEV [35].
Almost all EVs require common power electronic elements on-board [33]. The main components of the BEV shown in **Fig. 1.3(a)** are illustrated in **Fig. 1.4** as an example. In particular:

- The traction battery is often the primary source of energy. The most widely adopted nominal battery voltages range from 350 V to 400 V, even though 48 V are still used in HEVs and 800 V are an upcoming

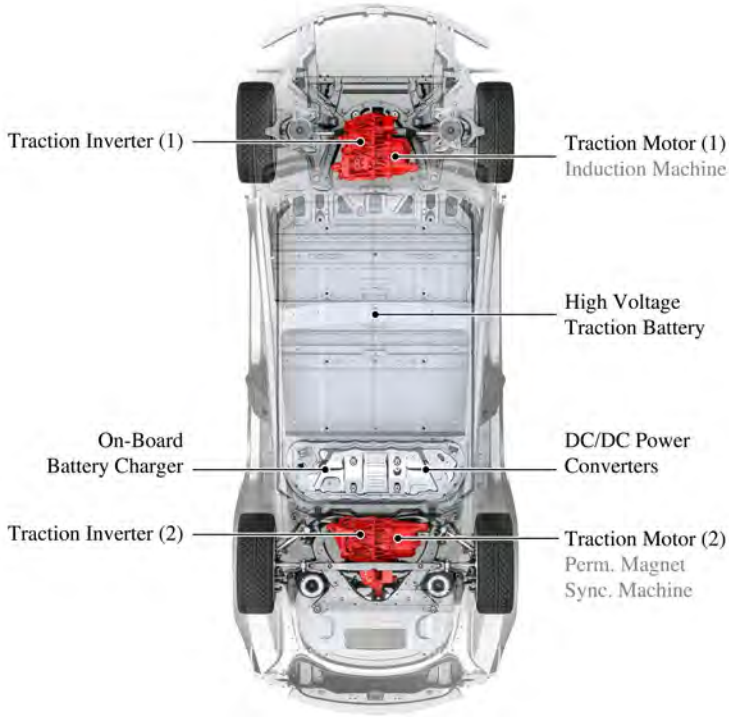


Fig. 1.4: Main power electronic components on-board of modern BEVs, i.e. DC/DC power converters, the on-board battery charger, front and rear motor drives integrated into the housing of the two traction motors, and the high voltage traction battery.

standard in high performance BEVs [34]. Typical battery capacities vary from 1 kWh to 10 kWh in HEVs, and from 10 kWh to 100 kWh in BEVs, depending on the vehicle class and on the desired mileage [34].

- The traction motor is an electric motor connected to the vehicle transmission which converts the electric energy stored in the battery into mechanical energy, i.e. it provides the speed and torque necessary to drive the EV. Its power rating varies from few tens of kW to 100 kW in HEVs, and from several tens of kW to few hundreds of kW in BEVs, depending on the vehicle class and on the desired performance [34]. Different motor technologies, e.g. induction motors, synchronous permanent magnet motors, etc., offer different advantages, e.g. regarding

cost and power density, and are possibly used independently, or in combination, e.g. with one motor per axis [33, 35].

- The traction inverter is a DC/AC power converter connected between the traction battery and the traction motor. It provides the required current and voltage waveforms at the motor terminals, and eventually recharges the battery in the regenerative braking phase (or when required in a parallel HEV). Generally, the inverter operates with both directions of power flow. Its output power capability is defined by the power rating of the motor, while its voltage rating is defined by the nominal battery voltage. Typical values for both are listed in the previous paragraph.

- Even though DC fast charging, i.e. the direct connection between an external DC power outlet and the traction battery, is becoming a predominant trend to reduce the charging times, BEVs and PHEVs are equipped with an on-board battery charger, i.e. an AC/DC power converter connected between an external power outlet and the traction battery during charging operation. On-board battery chargers are typically rated from 3.3 kW to 22 kW, depending on the vehicle class and battery capacity, in order to ensure convenient charging times [34].

- Finally, DC/DC power converters are responsible to generate low voltage levels, e.g. 12 V, from the high voltage battery. Typically, 12 V are necessary to supply ancillary loads, e.g. power steering and brake-by-wire systems, electric suspension systems, air conditioning compressors, infotainment and lighting systems, etc. Power ratings of few kW are nowadays already required [34]; nevertheless, these are increasing to fulfill the power demand of autonomous vehicles, i.e. to supply additional camera, radar, and more demanding processing units [33].

Overall, several power converters, continuously processing power levels up to hundreds of kW, are installed on-board of modern EVs. Accordingly, their power conversion efficiency and power density figures become key performance indexes of the entire vehicle [8, 37]. For example, an efficiency improvement of the traction inverter translates into an efficiency improvement of the overall powertrain, hence in a better fuel economy. Accordingly, with less losses, less battery capacity is necessary to achieve the same mileage, and a cheaper, smaller, and lighter battery can be installed by the manufacturer. On the other hand, a higher power density of the traction inverter directly allows to increase the payload of the vehicle, or to extend its mileage if the battery

capacity is increased utilizing the freed space. Moreover, compact power electronic converters facilitate the realization of skateboard chassis designs, which simplify the widespread electrification across all vehicle platforms [33]. Although also the cost reduction is a crucial aspect in the development of this industry, this topic is not discussed herein.
For the mentioned reasons, several roadmaps define the power electronic requirements, e.g. in terms of efficiency and power density, of the main components on-board of next-generation EVs (see **Fig. 1.4**). For example, state-of-the-art traction inverters feature typical efficiency and power density figures of 96 %, 12 kW/dm^3, and 15 kW/kg, respectively. However, in order to facilitate the mass market adoption of EVs, these performance indexes are required to improve to 97 %, 15 kW/dm^3, and 22 kW/kg by 2025, and to 98 %, 60 kW/dm^3, and 50 kW/kg by 2035, according to the study presented in [37]. These objectives are clearly to satisfy the needs of EV manufacturers, and to guarantee the sustainable development of this industry necessary to meet the defined GHG emission targets [38].

1.3 Challenges and Opportunities

The improvement of energy efficiency and the reduction of fuel consumption necessary to reduce the GHG emissions of the transportation industry, triggered, in the last two decades, significant investments in MEA and EV technologies. Although the increasing interest of the research community is already facilitating rapid technical advancements in these industries, a breakthrough in power electronics is still required. In fact, the electrification of transport inevitably translates into higher power levels, i.e. few MW in MEA and several hundreds of kW in EVs, to be processed on-board. Consequently, extremely high efficiency and gravimetric power density figures, e.g. higher than 99 % and 20 kW/kg, respectively, are specified for modern on-board power converters, in order to limit their losses and weight, even with significantly increasing overall power ratings.
Nowadays, the weight breakdown of power converters is dominated by the size of the passive filter components, and of the cooling system needed to dissipate the losses occurring in the power stage. Hence, conventional converter solutions, e.g. Si IGBT six-switch 3-Φ inverters in VSD applications, cannot meet the described highly ambitious targets. Differently, superior performance can be achieved through cutting-edge power electronics concepts, which exploit, at the component level, the higher switching frequencies enabled by the latest WBG power semiconductors, and at the converter level,

the most advanced converter design solutions offering reduced filtering effort, e.g. current source inverters and modular multi-phase inverters.

1.3.1 Component Level

Recently developed WBG power semiconductors, such as SiC and GaN transistors and diodes, offer unprecedented performance, i.e. significantly reduced conduction and switching losses compared to Si counterparts of same voltage and current ratings. However, to deal with the extreme switching speeds characteristics of WBG devices, several challenges must be carefully addressed. Given the inaccuracy of conventional measurement methods, new approaches are indispensable to characterize these devices, and to obtain comprehensive loss maps at the basis of power converter optimization procedures. Moreover, particular attention is required to realize power stage designs featuring extremely low parasitic elements, i.e. concepts which are able to withstand the enabled high switching speeds. For example, even though SiC power devices constitute a relatively mature technology, new power module (PM) packaging concepts with sophisticated interconnection technologies must be investigated in order to mitigate switching overvoltage phenomena. Additionally, a transition from multi-chip PMs to fully integrated PMs that can accept higher currents and temperatures, contain fewer interfaces and multifunctional subcomponents is envisaged. On the other hand, the manufacturing of GaN power devices, an even more promising WBG technology, is not yet mature and consequently not well understood loss mechanisms, with a significant influence on switching and conduction performance, occur. Nevertheless, entry industry applications for GaN power semiconductors are already identified, e.g. in DC/DC power converters and on-board chargers for EVs. Therefore, a detailed characterization of the conduction and switching behavior of these devices is needed in order to fully utilize their potential in advanced power converters.

1.3.2 Power Converter Level

Power converters employing latest semiconductor technologies are envisaged as promising solutions to achieve the mentioned efficiency and power density targets, since WBG devices guarantee enhanced performance, i.e. lower losses, while operating at higher switching frequencies. In particular, multi-level converter topologies are interesting candidates to alleviate the current limitations of conventional solutions, since their voltage waveforms of decreased harmonic content enable the downsizing of the filter components,

but on the other hand lead to increased complexity. Multi-cell topologies, instead, still benefiting from the superior performance of low voltage power semiconductors, have modular structures ensuring compactness, scalability, and reduced design effort. Therefore, modular/multi-cell power converter solutions, which can conveniently enable fault-tolerant operation through cell-redundancy, should be analyzed extensively. In order to extend the advantages of modularity also to the electric machines connected to these converters in VSD applications, machines with multiple 3-Φ winding sets should be considered in combination. Additionally, if these power electronic converters are integrated into the machine housing, several other advantages, e.g. reduction of cables length, electromagnetic (EM) emissions, design and installation costs and complexity are enabled.
As an alternative solution to the modular/multi-cell approach, the recent development of monolithic bidirectional GaN switches suggests to consider topologies featuring a low share of passive components, such as current DC-link converters, where a single DC-link inductor is required to generate continuous 3-Φ sinusoidal voltage waveforms. In fact, the bidirectional voltage blocking capability of these novel devices translates into substantially reduced system complexity, i.e. in the halving of the number of employed switches. Furthermore, new modulation strategies should be analyzed, such that converter losses and filtering effort can be minimized.

1.4 Aims and Contributions of the Thesis

Modern WBG power semiconductors are crucial for the advancements of the power electronics industry. However, although their potential has been demonstrated, several challenges still prevent the full exploitation of their performance. Accordingly, the aim of this thesis is to identify and analyze these barriers, to develop the necessary concepts to overcome them, and to demonstrate their effectiveness in power converter designs, finally proving the enablement of the efficiency and power density breakthroughs demanded in EVs and MEA, i.e. in next-generation power electronics applications. In particular, the main contributions of this thesis are recognized in:

PART 1 - **Novel Measurement Techniques for WBG Semiconductors**

Part 1 of the thesis covers the development of accurate measurement methods for the characterization of the conduction and switching performance of WBG power semiconductors in real operating conditions. The described conduction

loss measurement method allows to determine their on-state voltage during operation, and offers a very short response time, i.e. is particularly suitable for characterizing fast switching power semiconductors. The proposed switching loss measurement method, instead, is based on the observation of temperature variations, rather than on the measurement of electric quantities, but nevertheless offers comparably short measurement times.

PART 2 - **Performance Bottlenecks of WBG Semiconductors**

Part 2 details the performance analysis of WBG power semiconductors, overcoming characteristic challenges associated with their high switching speeds, thanks to the developed measurement techniques. In particular, the study of the non-ideal behaviors of GaN-on-Si HEMTs, i.e. of the unexpected switching losses originating from the charging process of their output capacitance, and of the excessive conduction losses as a results of the dynamic on-state resistance phenomenon, aims to facilitate their widespread adoption. The guideline for the optimization of a buffer network allows to maximize the switching speeds of SiC power semiconductors in PMs, i.e. to reduce the occurring losses, without compromising the system lifetime and/or increasing the overall EM noise emissions. Ultimately, the comparison in terms of conduction, switching, and thermal performance of Si versus GaN devices provides an insight on the improvement enabled by WBG power semiconductors at the converter level.

PART 3 - **Next-Generation Converters with WBG Semiconductors**

Finally, part 3 discusses the analysis of advanced power converters featuring modern WBG power semiconductors, and the optimization of their design parameters, e.g. switching frequency, supported by experimentally derived semiconductor loss models, and by a detailed understanding of their operation. Two case studies are considered for next-generation VSD applications, i.e. on-board of MEA and EVs: in particular, a modular multi-cell GaN inverter consisting of six input-series connected 3-Φ inverters, and a 3-Φ current source inverter system employing latest dual-gate monolithic bidirectional GaN e-FETs. Additionally, an in-depth analysis of current trends in power electronics describes several topics of interest for the further development of modern VSD, e.g. the trade-off between power density and reliability enabled by modular/multi-level inverters, the superior FoM of WBG power semiconductors, the advantages and challenges associated with integrated modular motor drives, etc.

1.5 Outline of the Thesis

The core part of this thesis is structured in eight chapters, whose content is summarized herein. In particular:

PART 1 - **Novel Measurement Techniques for WBG Semiconductors**

- **Chapter 2**
  The design, calibration, and experimental validation of an on-state voltage measurement circuit are described in this chapter. First, the operation of different measurement concepts is explained and these are compared. The most promising one is identified, analyzed in detail, and a hardware prototype is realized. Several considerations precede an exhaustive calibration of the developed measurement device, which meets the desired accuracy. Next, its performance is experimentally verified measuring the on-state behavior of different WBG power semiconductors. Finally, the challenges associated with the online measurement of the conduction losses in a real power converter are addressed, and described with the support of measurement results.

- **Chapter 3**
  Two calorimetric semiconductor loss measurement methods are presented in this chapter. The associated measurement procedures are described in detail, and the explanation of the physical principles underlying these methods is supported by the analysis of the thermal models of the measurement setups. A test setup is physically realized and thermally characterized to experimentally prove the applicability and the advantages of the proposed methods, which are finally compared.

PART 2 - **Performance Bottlenecks of WBG Semiconductors**

- **Chapter 4**
  The charging process of the output capacitance C_{oss} of GaN power semiconductors is analyzed in this chapter by means of calorimetric measurements in a dedicated setup. First, benchmark soft-switching loss measurements are carried out to develop an accurate measurement method; hence, the C_{oss}-loss mechanism is isolated, and experimentally characterized in a test device. After a thorough analysis of the internal device structure, a modified power semiconductor is designed and investigated, and its performance is finally compared, highlighting a substantial improvement, i.e. reduction of C_{oss}-losses.

- **Chapter 5**
  The dynamic on-state resistance dR_{on} phenomenon, i.e. the increase of on-state resistance after a turn-on switching transition characteristic of GaN-on-Si HEMTs, is the focus of this chapter. A dedicated measurement setup, suitable to characterize the dR_{on} of different DUT during operation, is first presented to provide evidence of the issue. Hence, several measurements are performed for different operating conditions to quantify the relevance of the effect on a selected device. Additionally, a framework for manufacturers of GaN HEMTs, for translating the measured dR_{on} into conduction losses, is finally proposed.

- **Chapter 6**
  In this chapter, the performance of two 200 V 10 mΩ GaN and Si power semiconductors is comprehensively characterized by means of measurements. First, a measurement setup is designed for each DUT, and the procedures to evaluate their conduction, thermal, and switching performance is described. Thus, the obtained results are extensively commented and compared. Finally, a sensitivity analysis is carried out to separately evaluate the influence of single device parameters on the overall efficiency and power density of a basic converter.

- **Chapter 7**
  The design and experimental analysis of a 1200 V SiC PM are discussed in this chapter. First, the advantages associated with the integration of a buffer-damping network are presented, together with an optimization procedure for its sizing. Measurements on a scaled PM prototype, which is also described and characterized in static conditions, are carried out to investigate the performance of the realized design in combination with the snubber. Afterwards, the design steps supporting the realization of a full-scale PM are summarized, and switching waveforms are measured, with and without the optimized network, to verify the improvement of the derived procedure in a real setup.

Part 3 - **Next-Generation Converters with WBG Semiconductors**

- **Chapter 8**
  A 3-Φ buck-boost current source inverter system for VSD applications, using monolithic bidirectional GaN switches, is analyzed in this chapter. Its detailed operation, in combination with a variable DC-link current control strategy denominated 2/3-PWM, is first explained through

analytic calculations of the component stress and comprehensive circuit simulations for different operating conditions. Afterwards, the reduction of switching and conduction losses enabled by 2/3-PWM is quantified, and the functioning of the developed control scheme is demonstrated. Finally, a hardware prototype is designed, and the performance of the monolithic bidirectional switches is verified.

- **Chapter 9**
  A modular multi-cell GaN inverter, consisting of six input-series connected 3-Φ inverters, and designed to supply an eighteen-phase electric machine, is analyzed in this chapter. The expected performance advantages of the proposed topology, compared to conventional and multi-level approaches, are quantified in an analytical study, considering the FoM of WBG power semiconductors, and focusing on the reliability function of redundant systems. Afterwards, the challenges specifically associated with the integration of the proposed power converter into the housing of the driven machine are discussed. Finally, an optimization routine for the converter design is delineated, and the results are analyzed in the efficiency-power density performance space.

Conclusion and Outlook

- **Chapter 10**
  The most significant findings of this thesis, i.e. the discussed measurement techniques and power electronic concepts enabling the full exploitation of the unprecedented performance of WBG semiconductors in power converters for next-generation MEA and EV applications, are jointly summarized in this last chapter, alongside the identified research areas and topics, which could support the rapid electrification of the transportation sector.

1.6 Publications

The most relevant documents created as part of this thesis, or in the scope of related projects, are listed in this section in chronological order.

1.6.1 Journal Papers

The main findings presented in this thesis have been published in international refereed journals, as listed in the following:

⑨ **M. Guacci**, D. Bortis, I. F. Kovačević-Badstübner, U. Grossner, and J. W. Kolar, "Analysis and Design of a 1200 V All-SiC Planar Interconnection Power Module for Next Generation More Electrical Aircraft Power Electronic Building Blocks," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 4, pp. 320–330, 2017.

⑧ **M. Guacci**, D. Bortis, and J. W. Kolar, "On-State Voltage Measurement of Fast Switching Power Semiconductors," *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 2, pp. 163–176, 2018.

⑦ **M. Guacci**, M. Heller, D. Neumayr, D. Bortis, J. W. Kolar, G. Deboy, C. Ostermaier, and O. Häberlen, "On the Origin of the C_{oss}-Losses in Soft-Switching GaN-on-Si Power HEMTs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 679–694, 2019.

⑥ **M. Guacci**, J. Azurza Anderson, K. Pally, D. Bortis, J. W. Kolar, M. Kasper, J. Sanchez, and G. Deboy, "Experimental Characterization of Silicon and Gallium Nitride 200 V Power Semiconductors for Modular/Multi-Level Converters Using Advanced Measurement Techniques," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2238–2254, 2020.

⑤ **M. Guacci**, D. Zhang, M. Tatic, D. Bortis, J. W. Kolar, Y. Kinoshita, and H. Ishida, "Three-Phase Two-Third-PWM Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 4, pp. 339–354, 2019.

Moreover, part of the research activity supported the work of others, which is reflected in the co-authorship of the following publications:

④ J. Azurza Anderson, E. J. Hanak, L. Schrittwieser, **M. Guacci**, J. W. Kolar, and G. Deboy, "All-Silicon 99.35 % Efficient Three-Phase Seven-Level Hybrid Neutral Point Clamped/Flying Capacitor Inverter," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 1, pp. 50–61, 2019.

③ G. Zulauf, **M. Guacci**, and J. W. Kolar, "Dynamic On-Resistance in GaN-on-Si HEMTs: Origins, Dependencies, and Future Characterization Frameworks," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5581–5588, 2019.

(2) G. Zulauf, **M. Guacci**, J. M. Rivas Davila, and J. W. Kolar, "The Impact of Multi-MHz Switching Frequencies on the Dynamic On-Resistance of GaN-on-Si HEMTs," *IEEE Open Journal of Power Electronics*, vol. 8, no. 3, pp. 2238–2254, 2020.

(1) D. Cittanti, **M. Guacci**, S. Miric, R. Bojoi, and J. W. Kolar, "Analysis and Performance Evaluation of a Three-Phase Sparse Neutral Point Clamped Converter for Industrial Variable Speed Drives," under review for *Springer Journal of Electrical Engineering*, 2020.

1.6.2 Conference Papers

Other core achievements presented in this thesis have been published in the proceedings of international conferences, in particular:

(12) **M. Guacci**, D. Neumayr, D. Bortis, J. W. Kolar, and G. Deboy, "Analysis and Design of a Multi-Tapped High-Frequency Auto-Transformer Based Inverter System," in *Proc. of the 17th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Trondheim, Norway, 2016.

(11) **M. Guacci**, D. Bortis, and J. W. Kolar, "High-Efficiency Weight-Optimized Fault-Tolerant Modular Multi-Cell Three-Phase GaN Inverter for Next Generation Aerospace Applications," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Portland, OR, USA, 2018.

(10) **M. Guacci**, M. Tatic, D. Bortis, Y. Kinoshita, H. Ishida, and J. W. Kolar, "Novel Three-Phase Two-Third-Modulated Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs," in *Proc. of the 10th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Xi'an, China, 2019.

Importantly, (10) has been recognized with the "Best Paper Award".
Additionally, the support in preliminary studies, experimental work, and in the writing of the final manuscript has been recognized with the co-authorship of the following papers:

(9) D. Neumayr, **M. Guacci**, D. Bortis, and J. W. Kolar, "New Calorimetric Power Transistor Soft-Switching Loss Measurement Based on Accurate Temperature Rise Monitoring," in *Proc. of the 29th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Sapporo, Japan, 2017.

⑧ I. F. Kovačević-Badstübner, R. Stark, **M. Guacci**, J. W. Kolar, and U. Grossner, "Parasitic Extraction Procedures for SiC Power Modules," in *Proc. of the 10th International Conference on Integrated Power Electronics (CIPS)*, Stuttgart, Germany, 2018.

⑦ O. Raab, **M. Guacci**, A. Griffo, K. Kriegel, M. Heller, J. Wang, D. Bortis, M. Schulz, and J. W. Kolar, "Full-SiC Integrated Power Module Based on Planar Packaging Technology for High Efficiency Power Converters in Aircraft Applications," in *Proc. of the 11th International Conference on Integrated Power Electronics Systems (CIPS)*, Berlin, Germany, 2020.

⑥ D. Zhang, **M. Guacci**, J. W. Kolar, and J. Everts, "Synergetic Control of a Three-Phase Buck-Boost Current DC-Link EV Charger Considering Wide Output Voltage Range and Irregular Mains Conditions," in *Proc. of the 9th International Power Electronics and Motion Control Conference (IPEMC - ECCE Asia)*, Nanjing, China, 2020.

⑤ D. Zhang, **M. Guacci**, D. Bortis, J. W. Kolar, and J. Everts, "Three-Phase Bidirectional Buck-Boost Current DC-Link EV Battery Charger Featuring a Wide Output Voltage Range of 200 to 1000 V," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Detroit, MI, USA, 2020.

④ M. Haider, **M. Guacci**, D. Bortis, J. W. Kolar, and Y. Ono, "Analysis and Evaluation of Active/Hybrid/Passive dv/dt-Filter Concepts for Next Generation SiC-Based Variable Speed Drive Inverter System," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Detroit, MI, USA, 2020.

③ D. Zhang, **M. Guacci**, J. W. Kolar, and J. Everts, "Three-Phase Bidirectional Ultra-Wide Output Voltage Range Current DC-Link AC/DC Buck-Boost Converter," in *Proc. of the 46th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Singapore, Republic of Singapore, 2020.

② D. Cittanti, S. Miric, **M. Guacci**, R. Bojoi, and J. W. Kolar, "Comparative Evaluation of 800 V DC-Link Three-Phase Two/Three-Level SiC Inverter Concepts for Next-Generation Variable Speed Drives," in *Proc. of the 23rd International Conference on Electrical Machines and Systems (ICEMS)*, Hamamatsu, Japan, 2020.

① J. W. Kolar, J. Azurza Anderson, S. Miric, M. Haider, **M. Guacci**, M. Antivachis, G. Zulauf, D. Menzi, P. Niklaus, J. Miniböck, P. Papamanolis, G. Rohner, N. Nain, D. Cittanti, and D. Bortis, "Application of WBG Power Devices in Future 3-Φ Variable Speed Drive Inverter Systems - "How to Handle a Double-Edged Sword"," in *Proc. of the IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2020.

1.6.3 Patents

The most innovative and original outcomes of the research, which could offer a competitive advantage if commercially exploited, have led to the filing of national and international patents. In particular:

⑦ J. W. Kolar, D. Neumayr, D. Bortis, **M. Guacci**, M. Leibl, and G. Deboy, "Power Converter Including an Autotransformer and Power Conversion Method," US Patent 10 177 681 B2, 2 017 373 608 A1, 2016.

⑥ **M. Guacci**, D. Bortis, and J. W. Kolar, "Durchlassspannung-Messschaltung," CH Patent 714 661 A2, 2018, (in German).

⑤ J. W. Kolar, D. Bortis, and **M. Guacci**, "Verfahren zum Regeln eines Dreiphasen-Pulsgleichrichtersystems mit Stromzwischenkreis," CH Patent, 2019, Application, (in German).

④ G. Deboy, J. W. Kolar, M. Kasper, D. Bortis, and **M. Guacci**, "Power Converter and Power Conversion Method," DE Patent, 2019, Application.

③ M. Haider, **M. Guacci**, D. Bortis, J. W. Kolar, and Y. Ono, "Three-Phase Supplied Modular Machines - Mesh Topology (TPSMM-I)," Patent, 2020, Application in Process.

② M. Haider, **M. Guacci**, J. W. Kolar, D. Bortis, and Y. Ono, "Three-Phase Supplied Modular Machines - Phase-Modular Approach (TPSMM-II)," Patent, 2020, Application in Process.

① D. Zhang, **M. Guacci**, J. W. Kolar, and J. Everts, "Electrical Power Converter," EU Patent, 2020, Provisional Application.

1.6.4 Workshops, Tutorials, Keynotes, etc.

The main results of the research activity have been as well disseminated in the form of oral presentations at international workshops, and in tutorial or keynote presentations at international conferences. In particular:

(14) **M. Guacci**, D. Neumayr, D. Rothmund, J. Azurza Anderson, D. Bortis, and J. W. Kolar, "Accurate Calorimetric Switching Loss Measurement of Ultra-Fast Power Semiconductors," *Presentation at the ECPE Workshop "EMC in Power Electronics: From Harmonics to MHz - Design for EMC and Fast Switching"*, Berlin, Germany, 2017.

(13) J. W. Kolar, D. Neumayr, D. Bortis, **M. Guacci**, and J. Azurza Anderson, "Google Little-Box Reloaded," *Keynote Presentation at the 10th International Conference on Integrated Power Electronics (CIPS)*, Stuttgart, Germany, 2018.

(12) D. Neumayr, D. Bortis, **M. Guacci**, J. Azurza Anderson, and J. W. Kolar, "Google Little-Box Reloaded," *Presentation at the STS (Spezial Transformatoren Stockach) Annual Seminar*, Ludwigshafen, Germany, 2018.

(11) J. Azurza Anderson, **M. Guacci**, D. Neumayr, and J. W. Kolar, "Evaluation of a Hybrid Multi-Level Flying Capacitor Bridge-Leg Topology for Beyond 99 % Power Conversion Efficiency," *Presentation at the Huawei Workshop on Highly Efficient Single Phase Power Converters in the Low Voltage Grid Connected Application*, Nuremberg, Germany, 2019.

(10) J. W. Kolar, **M. Guacci**, M. Antivachis, and D. Bortis, "Advanced SiC/GaN 3-Φ PWM Inverter Systems for VSD Applications," *Keynote Presentation at the CPES Annual Power Electronics Conference*, Blacksburg, VA, USA, 2019.

(9) D. Neumayr, J. W. Kolar, D. Bortis, **M. Guacci**, and J. Azurza Anderson, "Google Little-Box Reloaded - Advances in Ultra-Compact GaN Based Single-Phase DC/AC Power Conversion," *Tutorial at the International Wide-Bandgap Power Electronics Applications Workshop (SCAPE)*, Stockholm, Sweden, 2019.

(8) **M. Guacci**, M. Tatic, D. Bortis, J. W. Kolar, Y. Kinoshita, and I. Hidetoshi, "Novel Three-Phase 2/3-Modulated Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs," *Presentation at the International Wide-Bandgap Power Electronics Applications Workshop (SCAPE)*, Stockholm, Sweden, 2019.

⑦ D. Bortis, J. W. Kolar, M. Antivachis, **M. Guacci**, and D. Menzi, "Advanced Three-Phase PFC-Rectifiers," *Presentation at the ECPE Cluster-Seminar "Power Factor Correction (PFC)" und "Active Frontend" Schaltungen, Bauelemente, Regelung*, Augsburg, Germany, 2019, (in German).

⑥ J. W. Kolar, J. Azurza Anderson, **M. Guacci**, M. Antivachis, and D. Bortis, "Advanced 3-Φ SiC/GaN PWM Inverter & Rectifier Systems," *Presentation at the Centre for Power Electronics Annual Conference*, Loughborough, UK, 2019.

⑤ J. W. Kolar, **M. Guacci**, M. Antivachis, and D. Bortis, "Advanced 3-Φ SiC/GaN PWM Inverter & Rectifier Systems," *Tutorial at the 45th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Lisbon, Portugal, 2019.

④ J. W. Kolar, **M. Guacci**, M. Antivachis, and D. Bortis, "Next Generation 3-Φ Variable Speed Drive PWM Inverter Concepts," *Keynote Presentation at the 20th International Symposium Power Electronics (Ee)*, Novi Sad, Serbia, 2019.

③ D. Bortis, **M. Guacci**, M. Antivachis, and J. W. Kolar, "Future SiC/GaN Variable Speed Drive Inverter Topologies - "How to Handle a Double-Edged Sword"," *Presentation at the 2nd Wangener Automotive Symposium – Inverter Trends & Technology*, Wangen, Germany, 2019.

② J. W. Kolar, **M. Guacci**, M. Antivachis, and D. Bortis, "Advanced 3-Φ SiC/GaN PWM Inverter Concepts for Future VSD Applications," *Tutorial at the 35th Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020.

① J. W. Kolar, **M. Guacci**, M. Antivachis, and D. Bortis, "Next-Generation SiC/GaN 3-Φ Variable Speed Drive PWM Inverter Concepts," *Tutorial at the 9th International Power Electronics and Motion Control Conference (IPEMC - ECCE Asia)*, Nanjing, China, 2020.

1.6.5 Group-, Semester-, and Master-Theses

Finally, ten students contributed to the findings presented in this thesis in the course of Group-, Semester-, and/or Master-Theses projects. In particular:

⑪ M. Heller, "Optimization and Design of a Closed-Loop Gate Driver for SiC Planar Power Module," ETH Zurich, 2017, Semester Thesis LEM1707. Supervision: **M. Guacci**.

⑩ D. Wu, "Optimization and Design of a Current Source Gate Driver for SiC Planar Power Module," ETH Zurich, 2017, Semester Thesis LEM1708. Supervision: **M. Guacci**.

⑨ M. Heller, "Investigation of Soft Switching Losses Mechanisms in Wide Bandgap Semiconductors," ETH Zurich, 2017, Master Thesis LEM1721. Supervision: **M. Guacci**.

⑧ N. Koglin, "Design of an Intelligent Gate Driver for More Electric Aircraft SiC Power Module," ETH Zurich, 2017, Semester Thesis LEM1732. Supervision: **M. Guacci**.

⑦ A. Peloso, "Evaluation of Different Semiconductor Technologies for the Use in Modular Multilevel Converter in STATCOM Applications," ETH Zurich, 2018, Master Thesis LEM1821. Supervision: **M. Guacci**.

⑥ K. Pally, "Performance Evaluation of Low On-State Resistance 200 V Power Semiconductors for Next Generation Aerospace Power Electronics," ETH Zurich, 2018, Semester Thesis LEM1827. Supervision: **M. Guacci** and J. Azurza Anderson.

⑤ M. Tatic, "Performance Evaluation of a Novel Dual-Gate Gallium Nitride Monolithic Bidirectional Enhancement Mode Field Effect Transistor in Three-Phase Current Source Inverter Application," ETH Zurich, 2018, Semester Thesis LEM1836. Supervision: **M. Guacci**.

④ G. Kaufmann, S. Marti, and P. Sivananthaguru, "Design and Testing of a Light-Weight 1.5 kW Multi-Port DC/DC Power Converter for Underwater Robotics Applications," ETH Zurich, 2019, Group Thesis LEM1901. Supervision: **M. Guacci**.

③ K. Pally, "Optimization, Design and Testing of a High-Efficiency Fault-Tolerant Integrated Modular Multi-Phase GaN Inverter," ETH Zurich, 2018, Master Thesis LEM1902. Supervision: **M. Guacci** and M. Haider.

② M. Tatic, "Experimental Analysis of a 10 kW Integrated Modular Motor Drive," ETH Zurich, 2020, Master Thesis LEM2004. Supervision: **M. Guacci** and M. Haider.

① S. Leuch, "Integrated DM/CM Inductor Design for Three-Phase Bidirectional Buck-Boost Current DC-Link EV Battery Charger," ETH Zurich, 2020, Semester Thesis LEM2009. Supervision: D. Zhang and **M. Guacci**.

Part 1

Novel Measurement Techniques for Wide-Bandgap Semiconductors

2

On-State Voltage Measurement of Fast Switching Power Semiconductors

This chapter summarizes the most relevant findings in the context of research on the on-state voltage measurement of fast switching power semiconductors, which are also published in:

- **M. Guacci**, D. Bortis, and J. W. Kolar, "On-State Voltage Measurement of Fast Switching Power Semiconductors," *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 2, pp. 163–176, 2018.

Motivation

A new measurement device, capable of coping with the low-on state voltages and extreme switching frequencies of WBG power semiconductors, is necessary to characterize their conduction performance and to investigate not well understood loss mechanisms.

Executive Summary

The on-state resistance $R_{ds,on}$ is a key characteristic of unipolar power semiconductors, and its value depends on their operating conditions, e.g. junction temperature, conducted current, and applied gate voltage. Hence, the exact determination of $R_{ds,on}$ cannot only rely on datasheet information, but requires the measurement of current and on-state voltage during operation. Besides the determination of the conduction losses, the on-state voltage measurement enables dynamic $R_{ds,on}$ analysis, device temperature estimation, condition monitoring, and consequently time-to-failure prediction. However, in contrast to a switch current measurement, several challenges arise in the design of an on-state voltage measurement circuit (OVMC), i.e. high measurement accuracy (mV-range) during on-state, high blocking voltage capability (kV-range) during off-state, and fast dynamic response (ns-range) during switching transitions are demanded. Different OVMC concepts are known from IGBT applications, however, the more severe requirements introduced from the high switching frequency, high switching speed, and low OV characterizing the operation of WBG power semiconductors, prevent their usage. Off-the-shelf products hardly satisfy the mentioned specifications, whereas the performance of state-of-the-art OVM research prototypes requires further investigations and/or improvements. With this aim, an innovative OVMC concept is designed, analyzed, calibrated, and tested in this chapter. Furthermore, the OV of different power semiconductors is measured as function of their operating conditions to validate the performance and highlight the potential of the proposed solution.

2.1 Introduction

Today, the experimental analysis of a power converter is typically focused on the switching behavior of the power semiconductors, e.g. on switching overvoltages and voltage oscillations occurring in hard-switching transitions [39] and/or on switching voltage and current time displacement relative to ZVS [40] transitions. However, with the increasing switching speed enabled by WBG devices and/or with employing ZVS concepts, the loss contribution of the semiconductors is more and more dominated by the conduction losses. The power converter operating conditions are significantly influencing the occurring conduction losses. Junction temperature, conducted current, applied gate voltage, switching frequency, manufacturing variability, and aging take, in fact, a combined impact on the instantaneous value of the semiconductors on-state resistance $R_{ds,on}$. Despite this premise and contrary to switching loss analysis, no on-state behavior analysis and/or no experimental verification of the calculated $R_{ds,on}$ value is typically carried. Hence, worst-case

approximations, based on datasheet information, are inferred to estimate the conduction losses. Performing online $R_{ds,on}$ measurements would allow to accurately verify conduction loss calculations and hence to improve optimization procedures for the design of power converters [41, 42].
In order to achieve this, the voltage across and the current through the DUT have to be measured accurately and simultaneously. Several solutions are suitable to obtain the DUT current, i.e. it can be directly measured (e.g. with a series connected shunt resistor) or indirectly derived from the load current and the gate signals, both available for control purposes. In contrast, the usage of conventional voltage probes to accurately measure the DUT on-state voltage (OV) is prevented from the resulting dynamic range, i.e. the ratio between the maximum voltage (during the off-state) and the minimum voltage (during the on-state) applied at the input of this measurement circuit. The required extreme dynamic range limits the measurement resolution, as can be understood with the following example. If a conventional 12-bit oscilloscope is set to capture the voltage blocked (e.g. 1000 V) from a specimen power MOSFET (e.g. $R_{ds,on} = 25\,m\Omega$), the least significant bit, i.e. the measurement resolution, corresponds to $^{1000\,V}/_{2^{12}} \approx 250\,mV$. This voltage is already half the OV of the mentioned MOSFET conducting 20 A ($25\,m\Omega \cdot 20\,A = 500\,mV$) and the resulting accuracy is definitely insufficient. Ideally, in order to perform this measurement with an accuracy of 1%, the least significant bit should correspond to 5 mV ($0.01 \cdot 500\,mV$); in other words, an 18-bit oscilloscope ($^{1000\,V}/_{2^{18}} \approx 4\,mV$) would be required [43]. Alternatively, the conventional oscilloscope full-scale voltage would have to be limited to 20 V ($^{20\,V}/_{2^{12}} \approx 5\,mV$). The full-scale voltage reduces to 1 V if the same accuracy is desired while measuring only 1 A ($25\,m\Omega \cdot 1\,A = 25\,mV$, $0.01 \cdot 25\,mV = 0.25\,mV$ and $0.25\,mV \cdot 2^{12} = 1\,V$). However, if the oscilloscope range is limited to measure the sole OV (e.g. 1 V), the overdrive of the oscilloscope amplifiers, caused by the voltage blocked in the off-state, significantly distorts the measurements and could damage the instrument.
It results clear that the achievable accuracy is insufficient because of the trade-off with the excessive dynamic range. Therefore, only dedicated on-state voltage measurement circuits (OVMCs), limiting the voltage during the off-state to values within the oscilloscope input voltage range, allow accurate measurements during on-state. For example, a full-scale voltage of 10 V guarantees a measurement resolution of $^{10\,V}/_{2^{12}} \approx 2.5\,mV$, sufficient in most cases. Beside accuracy and resolution, also the bandwidth of OVMCs is of importance, since modern GaN semiconductors often present dynamic $R_{ds,on}$ effects [44, 45], i.e. a high initial (immediately after a turn-on switching transition) $R_{ds,on}$ value which slowly (with time constants varying in the µs-

range) settles to a constant value, still larger than the nominal one specified in the datasheets. In order to characterize this phenomenon, OVMCs should measure the correct OV immediately after the turn-on transition of the DUT in switching applications. The dynamic $R_{ds,on}$ is a fundamental FoM in the evaluation of GaN semiconductors, and it depends on the voltage blocked during the off-state, on the amplitude and direction of the switched current, as well as on the switching frequency, i.e. on the blocking and conducting times [45–47]. As this information is not specified in the datasheet of GaN devices, the experimental on-state behavior analysis is of fundamental importance.

In addition to dynamic and stationary OV analysis, other application areas are envisaged in literature, defining the requirements of an ideal OVMC. The OV is a promising temperature sensitive electric parameter, i.e. a circuit parameter ensuring high sensitivity and good linearity with respect to temperature variations [48]. Measuring the OV offers the potential for replacing conventional temperature measurements in application with severe volume constraints. Furthermore, the OV is identified as a favorable aging indicator. E.g. in power modules (PMs), a crack in the metallization layer and/or the lift-off of a bond-wire cause an increase of $R_{ds,on}$, i.e. of the OV [49, 50]. This establishes a positive feedback mechanism accelerating the aging process. Monitoring the OV allows a detection of the failure and potentially enables time-to-failure predictions, advantageous in reliability critical or remote applications. Accordingly, a trend towards intelligent gate drivers integrating OVMCs is traced [51] and, to facilitate this, compactness is generally demanded. As well, the mentioned bandwidth requirement, associated with a fast dynamic response of the OVMC after a switching transition, is of importance in all the foreseen application areas, if fast switching semiconductors are considered. Finally, the online measurement of conduction losses enabled by OVMCs can significantly improve the measurement accuracy of calorimetric switching loss measurement methods [52–54].

The nowadays most common OVM approaches can be traced back more than thirty years [55, 56]. Recently, the increased interest of the power electronics community in WBG semiconductors, combining reduced $R_{ds,on}$ values with increased switching speeds, motivated the interest to derive solutions offering better accuracy and higher bandwidth, e.g. [57] and [58], where also a comprehensive overview of the state-of-the-art is discussed. However, these concepts still reveal limited performance: [58] suffers significantly from noise and common-mode disturbances, and is tested only at high OV values, while [56] and [57] have an intrinsic accuracy limitation, i.e. an unknown diode forward voltage drop in the OVM path, as discussed in **Section 2.2**.

A solution to the latter issue is proposed in [50], where a novel OVMC is presented to monitor the wear-out of high power IGBT in PMs. Unfortunately, the performance of this OVMC highlighted in [50, 59, 60] and the provided design guidelines are insufficient and inadequate for fast switching power semiconductors, especially in terms of bandwidth and dynamic response. Significant distortions are introduced from this OVMC at its output for tens of µs, and the settling time of the designed analog circuitry itself is already in the range of 1 µs, i.e. comparable to the conduction period of a device operating with a switching frequency in the hundreds of kHz-range. Moreover, with respect to IGBTs, where the OV is rarely below 500 mV, when considering fast switching semiconductors with $R_{ds,on}$ values in the mΩ-range, it results significantly more challenging to guarantee the same OVM accuracy. Only limited information on the accuracy is provided in [50], and the performed OVMs are not completely validated with an alternative setup. Nevertheless, this OVMC is considered as a promising solution for the foreseen achievable accuracy enabled by the correction of the unknown diode forward voltage drop in the OVM path.
Lately, also OVM probes became commercially available [61, 62], aiming to replace OVM ICs [63]. A commercial solution is tested, but poor dynamic performance is experienced. Consequently, it results necessary to develop an OVMC able to satisfy all the mentioned requirements in order to cover all envisaged applications.
The reference setup, supporting the analysis presented in this chapter, is shown in **Fig. 2.1**. It highlights an OVMC (gray) connected to the low-side power semiconductor T_2, i.e. the DUT, of a half-bridge configuration. The same circuit could be connected to the high-side T_1, however, for simplicity, only the depicted solution is analyzed in the following. Different power semiconductors are then selected for T_2, enabling their comparison. After a discussion on the state-of-the-art of OVMCs summarized in **Section 2.2**, the proposed OVMC is presented in **Section 2.3**, where its operating principle and the achieved accuracy and bandwidth are verified through measurements on a calibrated test bench. Afterwards, the turn-on behavior of different Si, SiC and GaN power semiconductors is experimentally analyzed, validating the dynamic performance of this OVMC. Finally, the main challenges faced during the online measurement of conduction losses are commented in **Section 2.4**, before presenting the conclusions in **Section 2.5**.

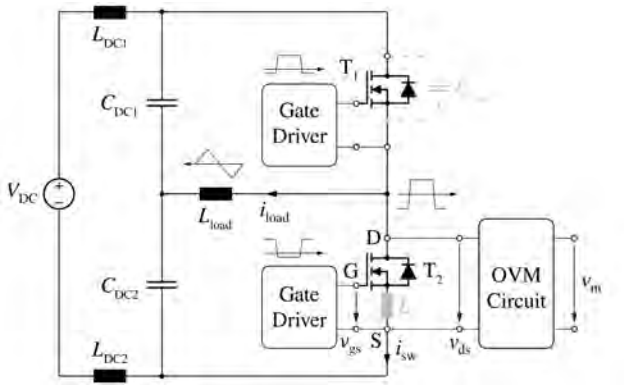


Fig. 2.1: Power converter setup considered as reference in the analysis of different OVMCs. The two power semiconductors in half-bridge configuration T_1 and T_2 are operated with complementary 50 % duty-cycles. The output inductor L_{load}, tapped to the split DC-link capacitors C_{DC1} and C_{DC2}, ensures symmetric triangular current mode (TCM) operation (blue waveforms). The parasitic inductance L_P and parasitic output capacitance C_{oss1} of T_1 are shown as well.

2.2 Conventional On-State Voltage Measurement Circuits

The schematics depicted in **Fig. 2.2** show the two most common implementations of OVMCs. The decoupling elements T_p or D_1 ideally perform as a short-circuit (i.e. $v_{ds} \approx v_{1,a}$ and $v_{1,b}$) when the power transistor T_2 (i.e. DUT, see **Fig. 2.1**) is conducting (on-state) and as an open-circuit when it is blocking the DC-link voltage V_{DC} (off-state). As explained in the introduction, the accuracy of v_1 during on-state and the dynamic performance of the transition between the two states are the most important properties of an OVMC. The two approaches are compared according to these criteria in the rest of this section. The final aim is to highlight their advantages in order to facilitate the design of a better performing solution.

The OVMC illustrated in **Fig. 2.2(a)** [56] is based on the decoupling MOSFET T_p. The gate of T_p is connected to a voltage source V_p and when $V_p > v_{1,a} + V_{th,Tp}$, T_p is in the on-state and

$$v_{1,a} = \frac{R_1}{R_1 + R_{Tp}} v_{ds}, \tag{2.1}$$

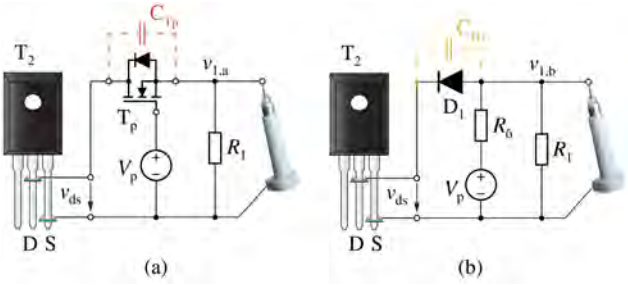


Fig. 2.2: Schematic representation of the two most common implementations of OVMCs. The input voltage v_{ds} is sensed at the DUT leads (see **Fig. 2.1**); by means of **(a)** the MOSFET T_p or **(b)** of the diode D_1, the output of the OVMC is decoupled during the DUT off-state and connected during its on-state. While the dynamic performance of the first approach is affected from C_{Tp}, the accuracy of the second one is compromised by v_{D1}.

where $V_{th,Tp}$ and R_{Tp} are the threshold voltage and the on-state resistance of T_p, respectively. Typically $R_{Tp} \ll R_1$, therefore $v_{1,a} \approx v_{ds}$. Regarding the transition between the two states, two control strategies are possible:

- *active*: V_p is switched to 0 V before T_2 is turned off and back to V_p after T_2 is completely turned on;
- *passive*: V_p is kept constant and T_p operates in its linear region during the off-state of T_2.

The active solution is intuitively effective but increases the complexity of this OVMC, e.g. logic and delay circuitry between the gate drivers of T_2 and T_p results necessary, and introduces a blanking time. Therefore, the less intuitive passive solution is preferred and herein considered, however additional challenges need to be faced [58].
The OVMC of **Fig. 2.2(b)** [55] is realized with the diode D_1 instead of the MOSFET T_p. When $v_{ds} < V_p - V_{fv,D1}$, D_1 conducts and

$$v_{1,b} = v_{ds} + v_{D1}(T_{D1}, i_{D1}), \tag{2.2}$$

where $V_{fv,D1}$, T_{D1} and i_{D1} are the forward voltage, the junction temperature and the current of D_1 respectively. During the off-state, $v_{1,b}$ is fixed from V_p and D_1 naturally blocks V_{DC}. Differently from (2.1), a significant error term (i.e. v_{D1} in the range of hundreds of mV) appears in (2.2), causing an offset on

$v_{1,b}$. As specified in (2.2), v_{D_1} is function of T_{D_1} and i_{D_1}, however, an approximate value is commonly subtracted from $v_{1,b}$ to obtain v_{ds} [56, 57]. This only partially compensates v_{D_1} and compromises the accuracy of the measurement. Nevertheless, this OVMC is often preferred (e.g. in desaturation circuits) to the one previously described, giving lower importance to the achievable accuracy than to hardware complexity and dynamic performance. The latter aspect is the focus of the following paragraph.
The transition of the DUT between on and off-state, i.e. the commutation of the half-bridge (see **Fig. 2.1**), implies charging and discharging of the parasitic output capacitances of T_1 and T_2 (i.e. C_{oss1} and C_{oss2} in **Fig. 2.1**), as well as of the input capacitance of the OVMCs. In fact, C_{Tp} and C_{D_1} (see **Fig. 2.2**) are charged to V_{DC} when T_2 is in the off-state, while are discharged when T_2 is conducting. The charging/discharging network includes the resistor R_1 or R_6, whose range of suitable values is limited from the operation of the OVMCs (e.g. R_1 defines the off-state current in the MOSFET-based solution). Consequently, C_{Tp} and C_{D_1} should be minimized:

- compared to C_{oss} in order not to affect the switching transition of the half-bridge, i.e. slowing down the voltage slope of the switch node $\mathrm{d}v_{ds}/\mathrm{d}t$ in ZVS transitions, or significantly increasing the capacitive energy dissipated in hard-switching transitions;
- accordingly minimizing the magnitude of the charging/discharging current spikes, potentially damaging measurement and/or supply circuitry;
- minimizing the time constant of the *RC*-network formed with R_1 or R_6, improving the dynamic performance of the OVMCs (see **Section 2.3.4**).

These considerations clearly address the selection of T_p and D_1 towards devices featuring a small parasitic capacitance. Additionally, a low inductance package and a short connection from the OVMC to the DUT are preferred in order to limit the voltage oscillations of v_1, inevitably excited from the switching transitions. According to these criteria, in the considered setups, a 800 V N-channel Si MOSFET [64] is selected for T_p as in [48] and a 600 V SiC Schottky diode [65] for D_1.
In order to prove the first statement, the parasitic capacitances of the selected devices are compared with the parasitic output capacitance C_{oss2} of a commercial 650 V e-mode GaN HEMT (specimen C in **Tab. 2.1**) as function of v_{ds} in **Fig. 2.3(a)**. At $v_{ds} = 25\,\mathrm{V}$, C_{D_1} is a negligible fraction (i.e. 5%) of C_{oss2}, while C_{Tp} contributes to the overall capacitance (i.e. $C_{oss2} + C_{Tp}$) for more than 30%.

Tab. 2.1: Specifications of the power semiconductors considered as DUT for the proposed OVMC.

Specimen	Power Semiconductor	$V_{ds,MAX}$	$I_{ds,MAX}$ @ 25 °C	$R_{ds,on}$ @ 25 °C
A	SiC power MOSFET	1200 V	98 A	25 mΩ
B	Si SJ MOSFET	700 V	46 A	40 mΩ
C	e-mode GaN HEMT	650 V	30 A	50 mΩ

As mentioned, this influences the switching behavior of the half-bridge where specimen C is selected for T_2, e.g. in soft-switching operation. In **Fig. 2.3(b)**, measured waveforms of v_{ds} and dv_{ds}/dt for three different conditions are shown: without any OVMC (blue), with the MOSFET-based approach (red) and with the diode-based approach (yellow) connected to T_2. While the presence of D_1 does not affect $dv_{ds}/dt \approx 20\,V/ns$, T_p slows it down especially in the first phase where C_{Tp} is comparable with C_{oss2}. This effect is clearly undesired and can be attributed to the selected T_p. However, depending on T_2, the range of suitable devices T_p (in terms of C_{Tp}) narrows, reaching a bottleneck in the case of interest of fast switching power semiconductors. Differently, parasitic capacitance of 600 V commercially available diodes can be in the range of few pF, enabling a more general OVM solution. Consequently, the approach presented in the next section is derived from the diode-based circuit. It aims to improve its accuracy, while benefiting from the reduced parasitic capacitance.

2.3 Proposed On-State Voltage Measurement Circuit

In **Section 2.2**, strengths and weaknesses of the two most common OVM approaches are highlighted. In this section, a promising solution derived from the diode-based circuit, and originally presented in [50], is analyzed in detail. As discussed in the introduction, it results significantly more challenging to perform OVMs in the case of fast switching semiconductors compared to IGBTs, e.g. due to the higher switching frequency and lower OV. Considering the design guidelines proposed herein, relative in particular to the small input parasitic capacitance, the usage of a 50 Ω output stage, the high bandwidth

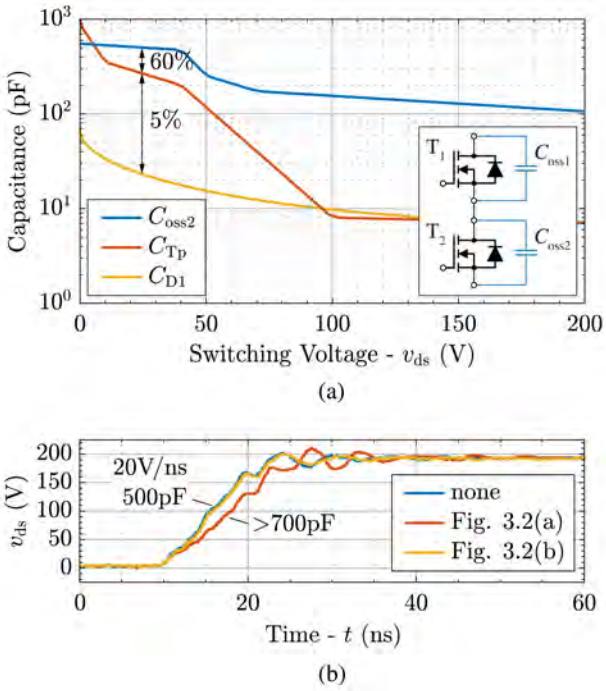


Fig. 2.3: (a) Comparison of the parasitic capacitances of the devices selected to realize the OVMCs of **Fig. 2.2**. For $v_{ds} < 100\,V$, C_{D1} is considerably smaller than C_{Tp} and, more important, negligible compared to C_{oss2}. This reflects on the switching behavior of the half-bridge **(b)**: the presence of T_p, i.e. C_{Tp} (red), significantly reduces dv_{ds}/dt during a soft-switching transition of T_2, whereas C_{D1} (yellow) does not have any influence.

conditioning circuitry, the integrated generation of the supply voltages, and the thoughtful design and calibration processes, this OVMC is improved to combine high accuracy, outstanding dynamic performance and reduced circuit complexity. This ultimately enables its usage in the mentioned application areas of interest, as verified with the described measurement results. Initially, the operating principle of the OVMC is presented to better comprehend its possible limitations, providing the basis for its improvement.

2.3.1 Operating Principle

The schematic of the proposed OVMC for fast switching power semiconductors is depicted in **Fig. 2.4(a)** (a simplified version is shown in **Fig. 2.4(c)**) together with its hardware realization (see **Fig. 2.4(b)**). The concept is derived from the approach shown in **Fig. 2.2(b)**, but now two identical diodes (i.e. D_1 and D_2) are connected in series at the input. During the on-state of T_2, the same current i_D is assumed to flow through D_1 and D_2 ($i_{D1} = i_{D2}$). Therefore, given the same operating point for the two diodes, the respective voltage drops v_D are assumed to be identical ($v_{D1} = v_{D2}$). Since thanks to the Zener diode Z_1, only D_1 blocks V_{DC}, v_{D2} can be measured and subtracted (with the operational amplifier Op_2) from v_1. Consequently, the offset v_{D1} present in (2.2) can be, with this OVMC, exactly corrected rather than roughly compensated. During the off-state, the operation is similar to the one of the OVMC shown in **Fig. 2.2(b)**.
The transfer function of the complete OVMC (see **Fig. 2.4(a)**) is herein derived. When $v_{ds} < V_p - v_{D2} - v_{D1}$, and with Op_1 and Op_2 operating linearly (always assumed from here on),

$$\begin{cases} v_+ = \dfrac{R_{1b}}{R_{1a} + R_{1b}} v_1 \\ v_3 = \dfrac{R_{2b}}{R_{2a} + R_{2b}} v_2 \\ v_m = v_- - \dfrac{R_4}{R_3}(v_3 - v_-) \end{cases} \tag{2.3}$$

holds. The system of equations given in (2.3) can be solved for the output voltage v_m if $v_+ = v_-$ is assumed, obtaining

$$v_m = \frac{R_{1b}}{R_{1a} + R_{1b}} \left(1 + \frac{R_4}{R_3}\right) v_1 - \frac{R_{2b}}{R_{2a} + R_{2b}} \frac{R_4}{R_3} v_2. \tag{2.4}$$

Defining $R_{1,b} = R_{2,b} = R$ and $R_{1,a} = R_{2,a} = \beta R$ so that

$$\frac{R_{1b}}{R_{1a} + R_{1b}} = \frac{R_{2b}}{R_{2a} + R_{2b}} = \frac{1}{1 + \beta} \tag{2.5}$$

and selecting $R_3 = R_4$, (2.4) can be simplified to

$$v_m = \frac{1}{1 + \beta}(2\, v_1 - v_2). \tag{2.6}$$

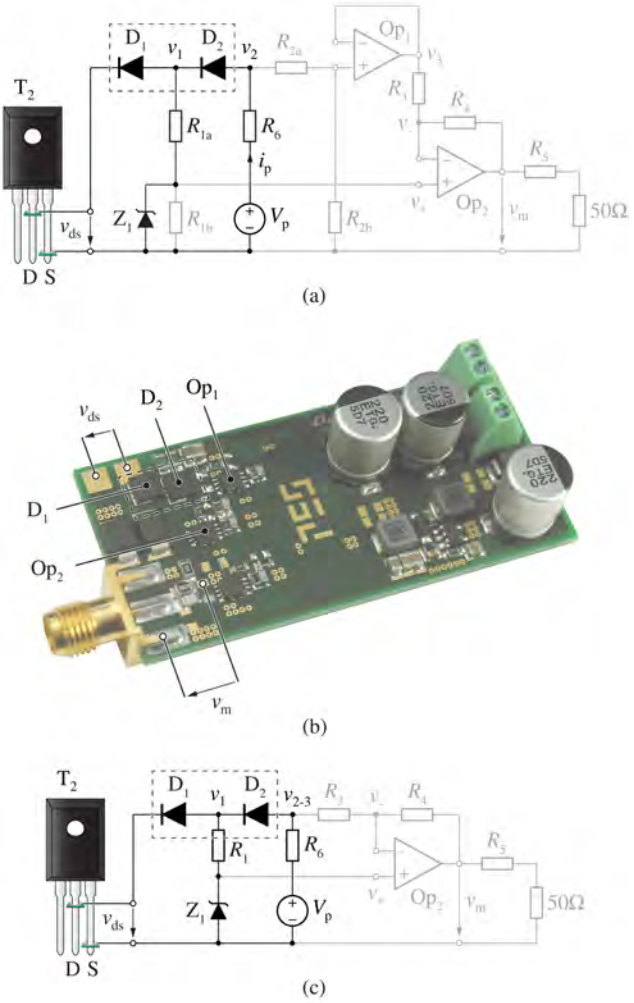


Fig. 2.4: Schematic representation of the realized **(a)** and simplified **(c)** versions of the proposed OVMC. **(b)** depicts the hardware realization of **(a)**. D_1 and D_2 are thermally well coupled (dashed box) in order to improve the measurement accuracy.

Finally, it must be noticed that the term

$$2\,v_1 - v_2 = v_1 - (v_2 - v_1) = v_1 - v_{D2}, \tag{2.7}$$

under the assumption that $v_{D2} = v_{D1}$, can be used in (2.6) to obtain

$$v_m = \frac{1}{1+\beta}(v_1 - v_{D1}) = \frac{1}{1+\beta} v_{ds}. \tag{2.8}$$

Hence, the proposed OVMC corrects the offset on v_1, i.e. v_{D1}, producing an output voltage v_m referred to the source potential of the DUT, exactly proportional to v_{ds} during its on-state.
In case the scaling of v_{ds} obtained by means of the voltage dividers formed by R_{1a}-R_{2a} and R_{1b}-R_{2b} is not needed, they can be bypassed (i.e. $R_{2,a} = 0\,\Omega$, $R_{1,b}$ and $R_{2,b}$ removed). Consequently Op_1 results unnecessary as well (see **Fig. 2.4(c)**) and the system of equations given in (2.3) reduces to

$$v_m = v_1 - \frac{R_4}{R_3}(v_2 - v_1) = v_{ds}. \tag{2.9}$$

The degree of freedom given by β is lost, i.e. the input voltage range of the circuit is reduced, but the number of required components is halved.
To provide a better understanding of the proposed OVMC, additional considerations are herein reported to conclude the section. As in the diode-based circuit presented in **Fig. 2.2(b)**, the values of V_p and R_6 fix the current in D_1 and D_2 during the on-state. $V_p = 10\,V$ (**Section 2.3.2**) and $R_6 = 750\,\Omega$ (**Section 2.2**) are selected. If the currents flowing in the voltage dividers formed by R_{1a}-R_{2a} and R_{1b}-R_{2b} are negligible (see **Fig. 2.4(a)**), the operating point of the OVMC when T_2 is in the on-state is defined by

$$i_p = \frac{V_p - v_{D2} - v_{D1} - v_{ds}}{R_6}. \tag{2.10}$$

If $v_{ds} = 0\,V$ and $v_{D1} = v_{D2} = 1\,V$ are assumed, $i_p \approx 10\,mA = I_{p,nom}$. Consequently, $P_{p,nom} = V_p\, I_{p,nom} \approx 100\,mW$ defines the power consumption of the OVMC from the main power source. It is important to limit i_p to a negligible fraction, e.g. 1%, of the current flowing through T_2 to avoid an increase and/or distortion of the OV (and to limit $P_{p,nom}$). This limit is strictly application-dependent and, if exceeded, the additional OV should at least be considered in the calculation of $R_{ds,on}$. Moreover, a lower boundary of i_p is also set from the parasitic currents circulating in the OVMC, e.g. in the voltage divider formed by R_{1a}-R_{2a} and in the input of Op_2. If i_p is reduced below a certain threshold, it would result impossible to neglect the parasitic currents and the fundamental assumption $i_{D1} = i_{D2}$ would be violated, compromising the accuracy of the measurement. V_p defines as well, together with Z_1, the value of v_{ds} at which the circuit snaps. The blocking voltage of Z_1 is selected to be

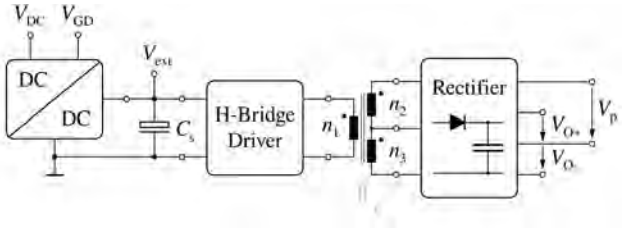


Fig. 2.5: Schematic representation of the OVMC supply circuitry. V_p, V_{O+} and V_{O-} can be generated from one of the supply voltages available in the power converter, e.g. V_{DC} and V_{GD}, facilitating the integration of the OVMC. Galvanic isolation is guaranteed and a small value of parasitic capacitance C_{it} ensures high CM rejection.

bigger than V_p to avoid its conduction during the on-state of T_2, but on the other hand low enough to limit v_1 during the off-state. Consequently the sole D_1 blocks the off-state voltage V_{DC}, protecting the measurement circuitry.
Finally, in order to facilitate the modular integration of the OVMC in a power converter (e.g. in case of intelligent gate drivers), **Fig. 2.5** illustrates different options for the generation of the required supply voltages. In the proposed solution, V_p and the supply voltages of the operational amplifiers V_{O+} and $V_{O-} = V_{O+}$ are galvanically isolated and generated from the gate driver supply voltage V_{GD}. A small value of parasitic capacitance C_{it} ensures a high common-mode (CM) rejection ratio. Thanks to the isolated supplies, the proposed OVMC can be connected, without any additional precaution, also to the high-side power semiconductor T_1 (see **Fig. 2.1**). Hence, the OV of T_1 can be measured with respect to its source potential, i.e. v_{ds}. To avoid a differential measurement and CM disturbances, it can be convenient to refer the OVM to a constant voltage, e.g. V_{DC}. To do so, the schematic of the proposed OVMC should be mirrored and referred to the drain potential of T_1. Afterwards, all the calculations performed for the low-side case remain valid.

2.3.2 Accuracy Measurement and DC Calibration

The accuracy of the proposed OVMC with respect to the assumptions made in **Section 2.3.1** is herein verified and calibration measurements support the analysis.
The first requirement for a correct operation of this OVMC is the identity $v_{D2} = v_{D1}$. First, in order to guarantee $i_{D1} = i_{D2}$, the current flowing in the voltage divider formed by $R_{1,a}$-$R_{1,b}$ (if present) must be negligible. If this cannot be achieved by increasing the value of $R_{1,a} + R_{1,b}$, an operational amplifier Op_3

can be added between v_1 and R_{1a}. However, even if $i_{D1} = i_{D2}$, the eventually different junction temperatures of the diodes (i.e. T_{D1} and T_{D2} respectively) and their manufacturing variability can cause a mismatch of v_D. T_{D1} can generally be higher than T_{D2} because D_1 is exposed to a wide input voltage excitation and is also physically closer to T_2, where the major losses are dissipated. In order to minimize the problem, the nominal operating point of the circuit can be tuned at a temperature-independent point of the *V-I* characteristic of the diodes (if existing and coinciding between them). Alternatively, two diodes in the same package can be chosen in order to maximize their thermal coupling. Unfortunately, as explained in **Section 2.2**, several constraints already drive the selection of the diodes (e.g. a small parasitic capacitance) if good dynamic performance is required, and it results difficult to find devices combining all these characteristics. More realistically, as shown in **Fig. 2.4(b)** (dashed box), a sufficient and good practice is to thermally well couple D_2 with D_1 on the OVMC PCB (and if necessary provide separation between the OVMC and T_2 without excessively increasing the parasitic inductance of their connection). Hence, a temperature difference $\Delta T_D = T_{D1} - T_{D2}$ of only 3 °C is measured in the worst-case operating conditions of interest (i.e. maximum losses of 8 W in T_2 at the highest switching frequency of 1 MHz and off-state voltage of 400 V). In particular, depending on the operating conditions of T_2, T_{D1} varies between $T_{D1,min} = 30$ °C and $T_{D1,max} = 40$ °C.
Concerning the device variability, before assembling the circuit, two diodes featuring the same v_D in the operating conditions of interest must be selected (a variability in the range of 10 mV is experienced in worst-case among several samples). To minimize this issue, it is convenient to reduce the variation of i_p from $i_{p,min} < I_{p,nom} < i_{p,max}$, caused by a variation of v_{ds} (according to (2.10)). For this reason, in [50], the voltage source V_p-R_6 is replaced with a current source I_p. However, considering the experiment presented in the introduction (i.e. a specimen power MOSFET with $R_{ds,on} = 25$ mΩ conducting ±20 A), the excursion of v_{ds} is in the range of ±500 mV and the current variation results only

$$\Delta i_p = \frac{i_{p,max}}{i_{p,min}} = \frac{V_p - v_{D2} - v_{D1} - v_{ds,min}}{V_p - v_{D2} - v_{D1} - v_{ds,max}} \approx 1.1. \tag{2.11}$$

Even a worst-case ±15% variation, i.e. ±1.5 mA, is assumed not to have any influence on the OVMC accuracy. To quantitatively support this statement, v_{D1} and v_{D2} are reported in **Tab. 2.2** as a function of i_p and T_{D1}. A worst-case mismatch in the diode voltage drops $v_{\Delta D} = v_{D1} - v_{D2} = 2$ mV and a temperature coefficient of 1 mV/°C are observed. $v_{\Delta D}$ must be negligible compared to the measured v_{ds} not to affect the OVM accuracy. This becomes more and more

Tab. 2.2: Mismatch in the diode voltage drops $v_{\Delta D}$ as function of their temperature T_D and current.

i_p	T_{D1}	v_{D1} (mV)	v_{D2} (mV)	$v_{\Delta D}$ (mV)
$i_{p,min}$	$T_{D1,min}$	831	832	-1
	$T_{D1,max}$	820	818	2
$i_{p,max}$	$T_{D1,min}$	838	839	-1
	$T_{D1,max}$	828	826	2

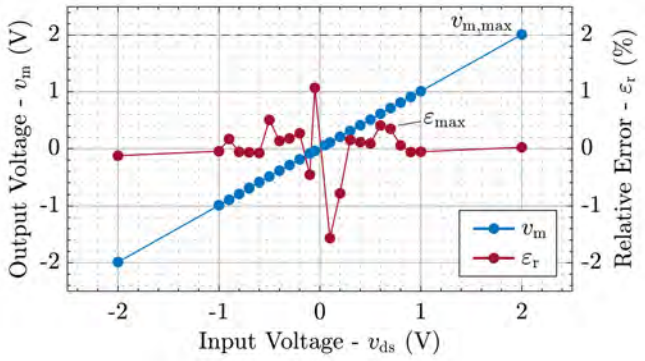


Fig. 2.6: Results of the DC calibration of the proposed OVMC. When a DC voltage $-2\,V < v_{ds} < 2\,V$ is applied at the input (x-axis), the output v_m (left y-axis) deviates less than 5 mV, corresponding to a relative error $\varepsilon_r < 2\%$ (right y-axis) in worst-case.

difficult to achieve at low OV levels, e.g. with $v_{ds} < 40$ mV, but, if desired, an even more sophisticated diode matching and/or calibration procedure can be adopted. However, also other problems arise when v_{ds} approaches 0 V and the DUT current approaches very low values, and these are discussed in **Section 2.4**. Finally, it can be noticed that, due to the small value of i_p, the diode model provided in [65] is not valid. For these reasons, the proposed calibration procedure cannot be avoided to enable the performance of the OVMC described in this section. Other interesting considerations regarding the precise tuning of the proposed OVMC are reported in **Appendix A**, as guideline for its design.

To conclude, once the crucial aspects related to the design of the proposed OVMC are clarified and taken into account, the achieved accuracy is measured. **Fig. 2.6** illustrates the relative error ε_r (right y-axis) from a DC input v_{ds} (x-

axis) to a DC output v_m (left y-axis) in a range from $-2\,V$ to $2\,V$. ε_r is confined between $\pm 2\%$ with an absolute maximum error $\varepsilon_{max} = 5\,mV$. Here, and in the rest of the analysis, the gain of the proposed OVMC is normalized to 1 for the sake of clarity.

2.3.3 Bandwidth Measurement and AC Calibration

A high bandwidth requirement is mandatory in all the application areas of OVMCs mentioned in the introduction, when fast switching semiconductors are considered. The bandwidth and the accuracy in AC operation of the proposed OVMC are verified in this section to evaluate its applicability in the conditions of interest. Measurements are preceded from a brief discussion pointing out the most significant aspects enabling its performance.
Accurately sensing a high frequency signal with a conventional oscilloscope probe (as in **Fig. 2.2(a)-(b)**) results in a challenge. In fact, when the high impedance input (i.e. $1\,M\Omega$) of the oscilloscope is used, precise tuning of the probe internal capacitance is required to have a flat gain for all the frequency range of interest. Hence, the $50\,\Omega$ input of the oscilloscope is preferred. $R_5 \approx 50\,\Omega$ is added at the output of the proposed OVMC (cf. **Fig. 2.4(a)-(c)**) to match the output impedance of Op_2 with the characteristic impedance of the used cable (i.e. $50\,\Omega$). This is possible only given the presence of Op_2, driving the necessary output current in the oscilloscope without affecting the circuit performance. Therefore, the selection range of operational amplifiers is limited from their output current and voltage capabilities. Among the available devices, a low noise 1 GHz 10 V 40 mA operational amplifier [66] is selected to maximize the achievable bandwidth of the OVMC.
The results of the high frequency calibration are described in **Fig. 2.7**. Three different triangular waveforms at 700 kHz with peak-to-peak voltage amplitudes increasing from 1 V to 7 V are generated at the input v_{ds} and plotted (red) behind the measured output v_m (blue) in **Fig. 2.7(a)**. When $v_{ds} < 2\,V$, the input and output waveforms are indistinguishable. At $v_{ds} = v_{m,max} = 2\,V$, Op_1 saturates and v_m is distorted. In **Fig. 2.7(b)-(c)**, the absolute ε and relative ε_r errors are reported for the case of 3 V peak-to-peak. ε is limited between $\varepsilon_{max} = \pm 10\,mV$ in the worst-case and has a zero mean. It must be mentioned that ε_{max} is in the range of the oscilloscope resolution. ε_r is, for the same reason, mainly in a $\pm 5\%$-range; however, when v_{ds} approaches 0 V (gray shaded area), the division between two small numbers causes a numerical issue.
Finally, with a vector network analyzer, the bandwidth of the proposed OVMC is measured exciting it at the input v_{ds} with sinusoidal waveforms up to $2\,V_{pk,pk}$. The $-3\,dB$ bandwidth is outside the measurable frequency range of

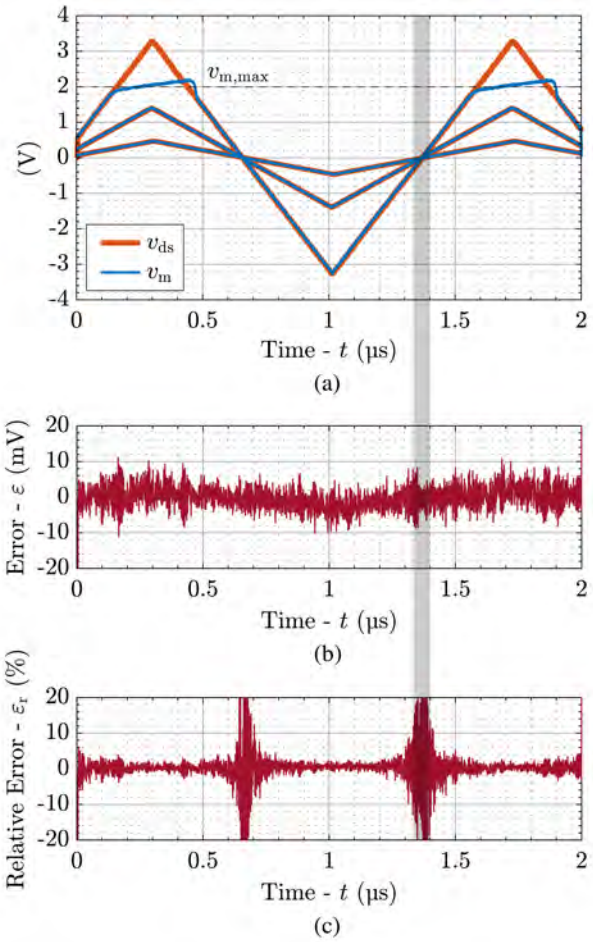


Fig. 2.7: Results of the AC calibration of the proposed OVMC. **(a)** When AC voltage waveforms of different amplitudes are applied at the input v_{ds}, the output waveforms v_m are practically indistinguishable from them. Thus, **(b)** the absolute error ε approaches the oscilloscope resolution, while **(c)** the relative error ε_r is down to ±5%.

the instrument (i.e. 50 MHz) while the normalized linear gain g_{lin} is 1.0 until 1 MHz and still 0.97 at 10 MHz, independently of the input signal amplitude (see **Fig. 2.8**). In order to guarantee the linearity in these measurements, the input signal never exceeds $v_{m,max}$. The real bandwidth of the circuit is, instead,

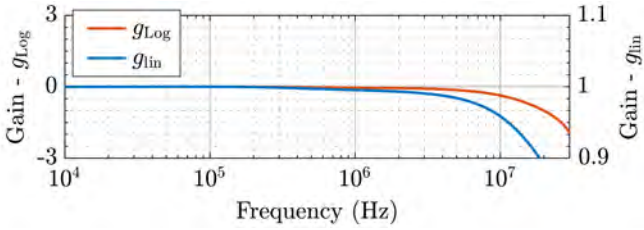


Fig. 2.8: Measured bandwidth of the proposed OVMC. The −3 dB bandwidth is above 50 MHz while $g_{\mathrm{lin}} = 1.0$ until 1 MHz and 0.97 at 10 MHz.

strongly influenced from its dynamic response after the turn-on switching transition of the DUT, which is the topic of the next section.

2.3.4 Dynamic Response

To conclude the characterization of the proposed OVMC, its outstanding dynamic response is analyzed in this section, accompanied by a discussion on the main features enabling this achievement.
As mentioned, it is important to perform accurate OVMs immediately after the turn-on transition of the DUT. This allows to capture eventual dynamic $R_{\mathrm{ds,on}}$ effects, the diode conduction phase during dead-times, and enables high frequency measurements necessary in all the mentioned application areas. In fact, the time constant of the dynamic response must be negligible compared to the duration of the DUT on-state to obtain meaningful OVMs.
In **Fig. 2.9**, the dynamic response of the proposed OVMC is compared with the one of a state-of-the-art commercial OVM probe. The two measured waveforms highlight the faster response of the proposed approach (blue). The measured signal is the on-state resistance $r_{\mathrm{ds,on}}(t)$ (the explicit reference to the time dependency is omitted from now on) of a commercial 1200 V SiC power MOSFET (specimen A in **Tab. 2.1**) for two different case temperatures. The value of $r_{\mathrm{ds,on}}$ is obtained dividing the output of the OVMCs v_{m} by the DUT current i_{sw} (see **Fig. 2.1**) and must be limited to the time window where the DUT is in the on-state (i.e. after t_{o}). The key design guidelines at the basis of the achieved performance rely on the selection of high bandwidth operational amplifiers and diodes with small parasitic capacitance, and on a low inductive PCB design (especially concerning the commutation loop).
In order to quantify the dynamic response time of the proposed OVMC, two more measurements, showing the turn-on transition of different DUT, are

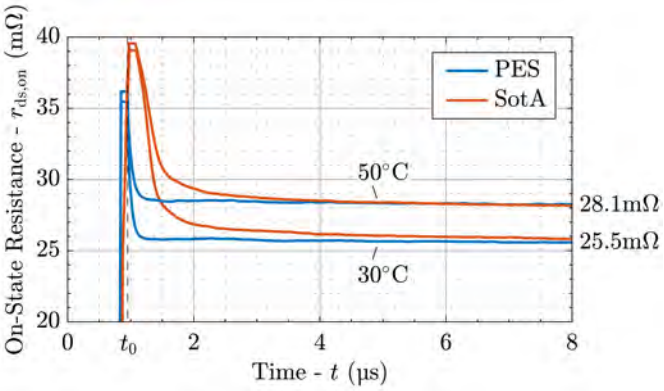


Fig. 2.9: Comparison in terms of dynamic response between the proposed OVMC (named PES) and a state-of-the-art (SotA) commercial OVM probe. When the DUT turns on at t_0, the output of the proposed OVMC immediately measures the correct OV, i.e. the nominal $r_{ds,on}$ value, whereas the commercial device features a time constant in the µs-range. A fast dynamic response increases the maximum switching frequency at which an OVMC can perform useful measurements, since the dynamic transient must be negligible compared to the duration of the DUT on-state.

performed (see **Fig. 2.10** and **Fig. 2.11**). In **Fig. 2.10**, a commercial 650V e-mode GaN HEMT (specimen C in **Tab. 2.1**) is tested. When the high-side transistor T_1 is turned off, v_{ds} drops from V_{DC} to ≈ 0 V because of a positive load current i_{load} (not shown, see **Fig. 2.1**). The anti-parallel body diode of T_2 (i.e. D_{T2}) immediately conducts and v_m accordingly shows a large negative value. When v_{gs} reaches ≈ 0 V, T_2 turns on and i_{sw} commutates from D_{T2} to the channel of T_2. Consequently v_m increases from the forward voltage of D_{T2} to $r_{ds,on} i_{sw}$. As the cursors highlight, the response time of the proposed OVMC is less than 50 ns if the real transition is assumed instantaneous. The same situation is reproduced in **Fig. 2.11** with a commercial Si SJ MOSFET (specimen B in **Tab. 2.1**). In this condition, ≈ 0.8 V can be accurately measured during all the conduction time of D_{T2}.

2.4 Online Conduction Loss Measurement

In this section, the integration of the proposed OVMC into a power converter is commented, and the associated challenges are addressed. In particular, the considered setup is equivalent to the schematic shown in **Fig. 2.1**. Assuming

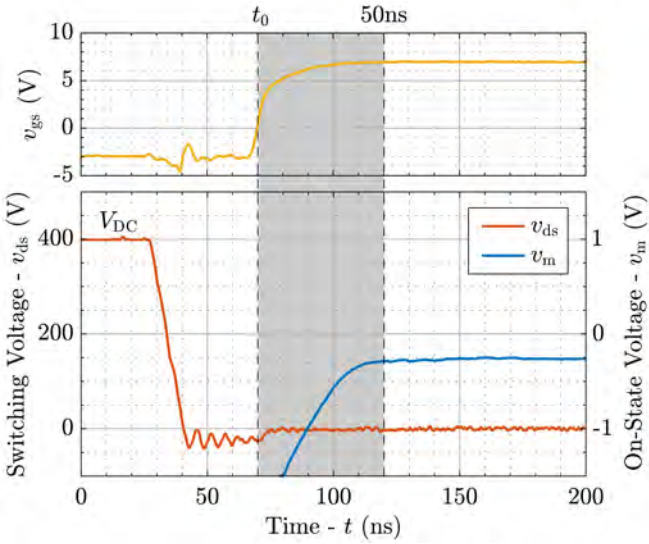


Fig. 2.10: Analysis of the dynamic response of the proposed OVMC. Less than 50 ns after v_{gs} has reached 0 V, v_m is settled to the correct value.

symmetrical triangular current mode (TCM) operation of the half-bridge (i.e. T_1 and T_2 are operated with complementary 50 % duty-cycles and no load is connected at the output), the analysis can be limited to the conduction time of T_2. All the relevant measured waveforms are shown in **Fig. 2.12(a)-(b)**. In particular, the switch node voltage v_{ds} (red), the load current i_{load} (green), the gate voltage v_{gs} (yellow), and the output of the proposed OVMC v_m (blue). Inside the time window t_1-t_2, the on-state resistance $r_{ds,on}$ of T_2 can be determined dividing v_m by $-i_{load} = i_{sw}$ (see **Fig. 2.12(c)**). The instantaneous conduction losses p_{cond} can be calculated as $r_{ds,on} i_{sw}^2$ or equivalently $v_m i_{sw}$ (see **Fig. 2.12(d)**). Finally, the average conduction losses can be obtained as average of p_{cond} during the on-state interval of T_2 (gray shaded area). Similarly, an average $R_{ds,on}$ value can be obtained as average of $r_{ds,on}$. In this case, $R_{ds,on} = 26.9\,\text{m}\Omega$ (see **Fig. 2.12(c)**) results for specimen A in **Tab. 2.1**. Consequently, the approximated conduction losses P_{cond} can be directly calculated as $R_{ds,on} i_{sw}^2$ (see **Fig. 2.12(d)**). Given the almost perfect overlap between the curves in **Fig. 2.12(d)**, when p_{cond} and P_{cond} are averaged, 3.6 W results in both cases. However, in general, the first approach is preferred, since it takes into account dynamic $R_{ds,on}$ effects and the current dependency of $R_{ds,on}$.

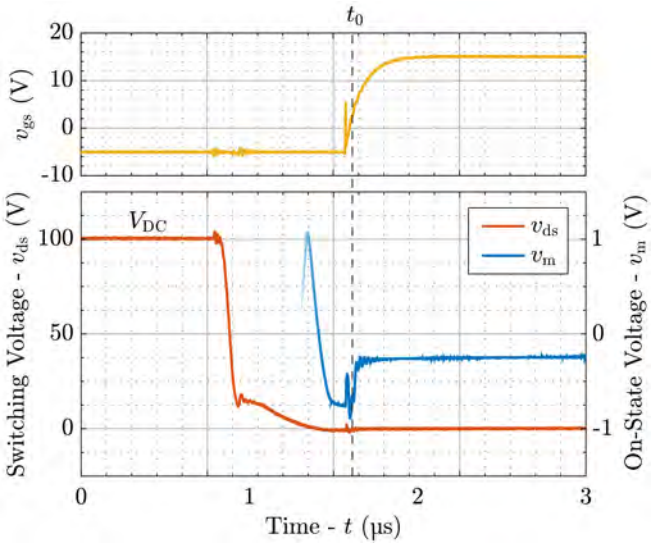


Fig. 2.11: Analysis of the dynamic response of the proposed OVMC. When v_{ds} during the conduction time of D_{T_2} is in the measurable range, the proposed OVMC allows to evaluate the dead-time conduction losses and its effective duration.

In order to perform accurate OVMs for these operating conditions, two challenges, associated in particular with the reduced OV and high current slopes that need to be measured, are faced. The first challenge to overcome is represented by the parasitic inductance L_P in series with T_2. **Fig. 2.13(a)** highlights the load current slope $\mathrm{d}i_{load}/\mathrm{d}t = -\mathrm{d}i_{sw}/\mathrm{d}t$ (up to tens of $\mathrm{A}/\mu\mathrm{s}$) that, in combination with L_P, causes a voltage offset (red) on v_m according to

$$v_m = R_{ds,on} i_{sw} + L_P \frac{\mathrm{d}i_{sw}}{\mathrm{d}t} \tag{2.12}$$

(blue). Hence, calculating $r_{ds,on}$ as

$$r_{ds,on} = \frac{v_m}{i_{sw}} = R_{ds,on} + \frac{L_P}{t} = R_{ds,on}\left(1 + \frac{\tau_{RL}}{t}\right), \tag{2.13}$$

the term $\frac{\tau_{RL}}{t}\left(\tau_{RL} = \frac{L_P}{R_{ds,on}}\right)$ distorts the result. Therefore, in contrast to a constant $R_{ds,on}$ (dashed in **Fig. 2.13(b)**), the waveform of $r_{ds,on}$, solid in **Fig. 2.13(b)**, is obtained. E.g. if $L_P = 8\,\mathrm{nH}$ and $R_{ds,on} = 50\,\mathrm{m\Omega}$, then $\tau_{RL} \approx$

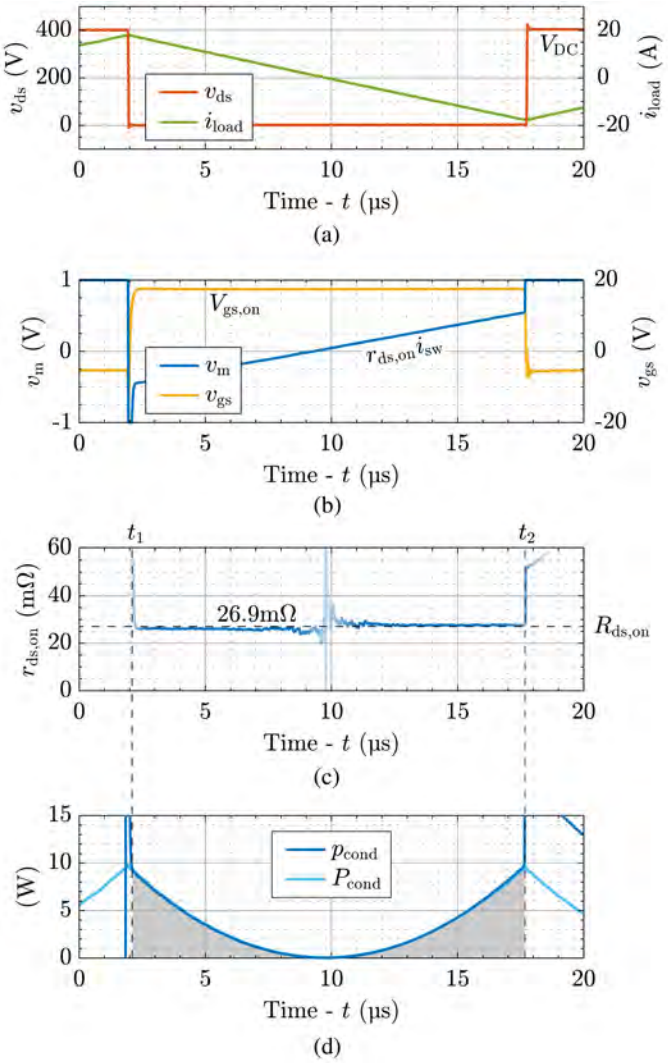


Fig. 2.12: (a)-(b) Typical waveforms measured on the half-bridge operating in triangular current mode (TCM). When $v_{gs} = V_{gs,on}$ (yellow), T_2 conducts and v_m (blue) is proportional to i_{sw} and i_{load} (green). In **(c)** $r_{ds,on}$ is calculated between t_1 and t_2 dividing v_m by i_{sw}, while in **(d)** p_{cond} is obtained multiplying v_m and i_{sw}.

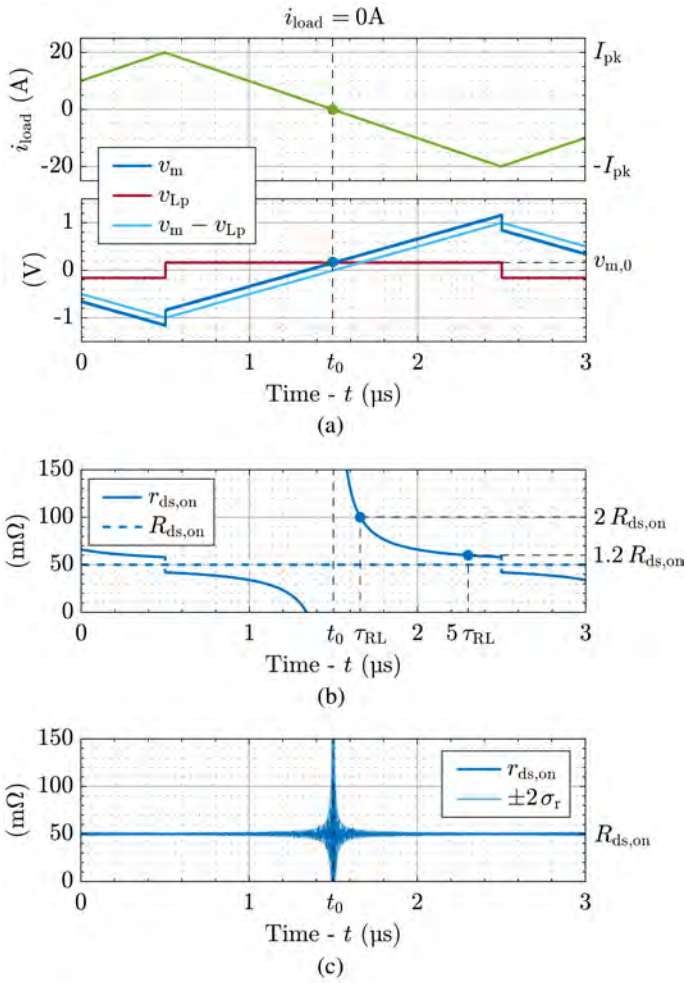


Fig. 2.13: **(a)** Typical waveforms measured on the half-bridge operating in TCM, highlighting how the combination of L_P and di_{sw}/dt causes a distortion on v_m and consequently on **(b)** $r_{ds,on}$. **(c)** A measurement error on v_m translates into an error on $r_{ds,on}$, particularly amplified for small values of i_{sw}, as in (2.15).

150 ns. Hence, after $t = 5\,\tau_{RL} = 800$ ns, $r_{ds,on} = 1.2\,R_{ds,on} = 60$ mΩ. From (2.13) it can be concluded that L_P should be minimized, i.e. the connection from the

DUT to the OVMC should start as close as possible to the drain and source terminals of T_2, excluding any additional path where i_{sw} flows. Unfortunately, part of L_P is located internally in the package of the DUT and no design expedient results helpful. A compensation network could be inserted and tuned, however it would negatively affect the dynamic performance of the proposed OVMC. Alternatively, the inductive voltage drop $v_{m,o}$ can be isolated from the resistive component taking advantage of the zero crossing of i_{sw}. I.e. measuring v_m and $\mathrm{d}i_{sw}/\mathrm{d}t$ when $i_{sw} = 0\,\mathrm{A}$, (2.12) can be solved for L_P. Formally

$$v_{m,o} = v_m|_{i_{sw}=0} = L_P \frac{\mathrm{d}i_{sw}}{\mathrm{d}t}. \tag{2.14}$$

Repeating this measurement for different $\mathrm{d}i_{sw}/\mathrm{d}t$, the obtained average value of L_P can be used to adjust v_m. From the practical point of view, this results in subtracting $v_{m,o}$ from v_m in each measurement, ensuring $v_m = 0\,\mathrm{V}$ when $i_{sw} = 0\,\mathrm{A}$. Whereas this assumption sounds legit and sufficient by itself, calculating L_P provides a physical motivation to this adjustment. Moreover, obtaining constant L_P across different measurements guarantees their correctness. This becomes more and more important when the zero crossing of i_{sw} is not present and/or measurable, and the knowledge of L_P is the only option to correct the measurement result. Alternatively, $r_{ds,on}$ can be calculated independently of L_P as the ratio between $\mathrm{d}v_m/\mathrm{d}t$ and $\mathrm{d}i_{sw}/\mathrm{d}t$ for constant $\mathrm{d}i_{sw}/\mathrm{d}t$. Even if not affected from $v_{m,o}$, this approach loses accuracy when the voltage and current slopes become flatter.
The second challenge is easily highlighted applying the propagation of uncertainty rule on $r_{ds,on} = v_m/i_{sw}$:

$$\sigma_{r_{ds,on}} = \sqrt{\left(\frac{\partial r_{ds,on}}{\partial v_m}\sigma_{v_m}\right)^2 + \left(\frac{\partial r_{ds,on}}{\partial i_{sw}}\sigma_{i_{sw}}\right)^2} = \frac{1}{i_{sw}}\sqrt{\sigma_{v_m}^2 + (r_{ds,on}\,\sigma_{i_{sw}})^2} \tag{2.15}$$

and

$$\sigma_{\%r_{ds,on}} = \frac{\sigma_{r_{ds,on}}}{r_{ds,on}} = \frac{\sigma_{v_m}}{r_{ds,on}\,i_{sw}} = \sigma_{\%v_m} \tag{2.16}$$

are obtained, assuming $\sigma_{i_{sw}} = 0\,\mathrm{A}$. σ_x and $\sigma_{\%x}$ indicate the absolute and relative error on the measured quantity x, respectively. (2.15) proves why $\sigma_{r_{ds,on}}$ and therefore $r_{ds,on}$ diverges when i_{sw} approaches 0 A (see **Fig. 2.12(c)** and **Fig. 2.13(b)-(c)**). (2.16), instead, expresses how $\sigma_{\%r_{ds,on}}$ coincides with $\sigma_{\%v_m}$ when $\sigma_{i_{sw}} = 0$. In other words, any error on v_m reflects one-to-one (relatively) on $r_{ds,on}$ (i.e. on p_{cond}). An example of $r_{ds,on}$, corrected from $v_{m,o}$, but resulting

from v_m with $\sigma_{v_\mathrm{m}} = 5\,\mathrm{mV}$ to highlight the effect, is shown in **Fig. 2.13(c)**. Since the only expedient to minimize both phenomena described from (2.15) and (2.16) is to reduce σ_{v_m}, the effort placed on the accuracy analysis of the proposed OVMC addressed in **Section 2.3** is clearly justified. Moreover, these considerations underline how measurements of low $r_{\mathrm{ds,on}}$ and/or high $\mathrm{d}i_\mathrm{load}/\mathrm{d}t$ (e.g. WBG semiconductors) introduce new challenges for OVMCs.

2.5 Conclusion

An on-state voltage measurement circuit (OVMC) for fast switching power semiconductors is presented and fully characterized in this chapter. The correction of the offset voltage present in typical OVMCs, the small input parasitic capacitance, the usage of a 50 Ω output stage, the high bandwidth conditioning circuitry, the integrated generation of the supply voltages, and the thoughtful design and calibration processes are key features and/or main improvements of the proposed approach when compared with the state-of-the-art.

The operating principle of the proposed OVMC is described and detailed design guidelines are given. Furthermore, accurate DC and high frequency calibration measurements are performed. Several challenges, e.g. measurement distortion due to the DUT parasitic inductance and noise amplification at low DUT current values, arise when the proposed OVMC is integrated into the measurement setup of interest considering fast switching power semiconductors. However, implementing the addressed precautions, the achieved accuracy ($< \pm 2\,\%$ error), bandwidth ($> 50\,\mathrm{MHz}$), and dynamic response ($< 50\,\mathrm{ns}$) finally enable precise OVMs in the case of both low $R_{\mathrm{ds,on}}$ values and at high switching frequencies, e.g. in applications featuring WBG semiconductors. In summary, the proposed OVMC generally enables on-state behavior analysis of power devices and accordingly improves the accuracy of power converter optimization procedures, loss breakdown models, and of calorimetric switching loss measurement methods. Moreover, this circuit is envisaged as fundamental feature of next generation intelligent gate drivers, including temperature and condition monitoring, as well as time-to-failure prediction circuits.

3

Calorimetric Switching Loss Measurement of Fast Switching Power Semiconductors

This chapter summarizes the most relevant findings in the context of research on a new transient calorimetric switching loss measurement method, which are also published in:

- D. Neumayr, **M. Guacci**, D. Bortis, and J. W. Kolar, "New Calorimetric Power Transistor Soft-Switching Loss Measurement Based on Accurate Temperature Rise Monitoring," in *Proc. of the 29th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Sapporo, Japan, 2017.

- **M. Guacci**, M. Heller, D. Neumayr, D. Bortis, J. W. Kolar, G. Deboy, C. Ostermaier, and O. Häberlen, "On the Origin of the C_{oss}-Losses in Soft-Switching GaN-on-Si Power HEMTs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 679–694, 2019.

- **M. Guacci**, J. Azurza Anderson, K. Pally, D. Bortis, J. W. Kolar, M. Kasper, J. Sanchez, and G. Deboy, "Experimental Characterization of Silicon and Gallium Nitride 200 V Power Semiconductors for Modular/Multi-Level Converters Using Advanced Measurement Techniques," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2238–2254, 2020.

Motivation

The extreme switching speeds of WBG power semiconductors require new non-electric switching loss measurement techniques. Transient calorimetric semiconductor loss measurement methods, relying on the developed on-state voltage measurement device for the determination of the occurring conduction losses, are promising candidates to obtain comprehensive and accurate switching loss maps.

Executive Summary

Modern GaN and SiC power semiconductors are key enablers for future advancements in power electronics and require new experimental methods for the determination of their switching losses. In fact, the widely accepted Double Pulse Test method fails to accurately capture the dissipated energy during a switching transition, because of electric measurement limitations imposed by the very fast switching speeds enabled by WBG devices. In this chapter, two calorimetric measurement principles, which rely on the temperature rise monitoring of the heat sink and/or of the package of the power semiconductors under test, are presented. Unlike traditional steady-state calorimetric methods, a single measurement can be performed in a few tens of seconds or few minutes, since thermal transients during continuous operation rather than thermal equilibria are considered. Several setups are realized to experimentally evaluate the switching performance of different fast switching devices, and to demonstrate the wide applicability of the proposed methods. The obtained results provide accurate semiconductor loss models supporting the optimization of power converters employing WBG devices, ultimately enabling the full exploitation of their performance.

3.1 Introduction

The unprecedented performance of WBG semiconductors enables a significant switching frequency increase in modern power converters, allowing to downsize the filter components when maximal power density is targeted. Nowadays, the switching losses typically dominate the loss breakdown of compact converter designs. Hence, a good knowledge of the switching performance of WBG devices is crucial for the optimization of modern power converters.

The most widely adopted approach to measure the switching losses of a power device is the Double Pulse Test [67, 68]. This method relies on the measurement of electric quantities, i.e. of the voltage across and of the current through a switch, to calculate the energy dissipated in a switching transition. The measurement accuracy of electric methods is defined by the performance, e.g.

in terms of bandwidth and intrusiveness, of the selected voltage and current probes. Accordingly, the high switching speeds of WBG semiconductors are limiting the applicability of these methods, and motivated, in the recent years, the need to investigate alternative electric [69, 70], as well as calorimetric [40, 53, 54, 71–79], switching loss measurement methods. The latter are based on the observation of thermal quantities, and are thus generally independent of the electric characteristics of the analyzed devices, e.g. the voltage and current ratings. Generally, calorimetric measurement methods can be divided into two subcategories, i.e. steady-state methods and transient methods. In steady-state methods [40, 54, 71–73] the setup is continuously operated until the thermal steady-state is reached and, only then, the occurring losses are determined from the observation of specific temperature values. Differently, transient methods [53, 74–79] analyze the thermal dynamics of the system, e.g. its thermal step response after turn-on, and, at the expense of slightly increased complexity, offer reduced measurement times and comparable accuracies [74, 75, 77].
In this chapter, after describing the realized measurement setup in **Section 3.2**, two transient calorimetric switching loss measurement methods are introduced in **Section 3.3**. In particular, the one presented in **Section 3.3.1** is based on the observation of the heat sink temperature, while the one discussed in **Section 3.3.2** relies on the analysis of the case temperature of the DUT. Since the latter approach involves much shorter thermal time constants, the measurement time can be conveniently reduced in this case. Afterwards, the thermal models associated with both methods are analytically derived, before commenting in detail the respective measurement procedures. Finally, **Section 3.4** concludes the chapter.

3.2 Measurement Setup

The calorimetric switching loss measurement methods presented in **Section 3.3** can be conveniently applied for a bridge-leg configuration of two DUT T_h and T_l (see **Fig. 3.1**). As an example, **Fig. 3.1(b)** depicts the implementation on a PCB of the circuit schematic shown in **Fig. 3.1(a)**, realized for the switching performance characterization of 200 V OptiMOS 3 FD Si power MOSFETs [80] [81]. In addition to the DUT, the DC voltage source V_{dc} and the symmetric LC output filter formed by the output inductor L_o and the output capacitors C_o, and the load resistor R_o are indicated.
The setup is operated with constant switching frequency f_{sw}, dead-time t_{dt} and duty-cycle d, such that the switch node voltage v_{sw} results in a rectangular

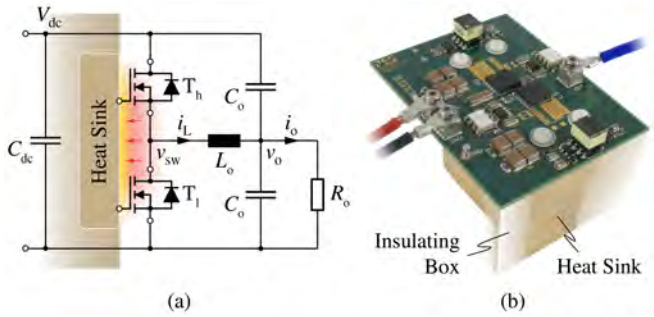


Fig. 3.1: (a) Circuit schematic of the measurement setup consisting of two switches, T_h and T_l (DUT), in bridge-leg configuration, the DC-link/commutation capacitor C_{dc}, the symmetric *LC* output filter formed by the output inductor L_o and the output capacitors C_o, and the load resistor R_o. **(b)** Realization of the power stage shown in **(a)** on a PCB. The PCB is mounted on a brass heat sink, which is closely thermally coupled with, but electrically isolated from, the power semiconductors.

waveform and, when the *LC* output filter is connected, the DC output voltage is $v_o = d\,V_{dc}$. V_{dc} is adjusted to characterize the switching performance of the DUT at the voltage level of interest; f_{sw} is varied (between hundreds of kHz and 1 MHz) to maximize the switching losses with respect to other frequency-independent losses, i.e. to increase the sensitivity of the switching loss measurements [54]; t_{dt} is set depending on I_{sw} to minimize the reverse conduction losses [79]. Finally, the configuration of the output network is modified to vary the inductor current i_L, and therefore, both the switched current I_{sw} and the operating mode of the setup, as described in the following:

- *Soft Switching - ZCS*: the switch node is left open, i.e. the *LC* output filter is not connected, forcing $i_L = I_{sw} = 0$ A.
- *Soft Switching - ZVS*: the symmetric *LC* output filter is connected to the switch node to obtain Triangular Current Mode (TCM) operation and ZVS conditions. In this case, I_{sw} corresponds to the positive and negative peaks of i_L, and can be calculated as

$$I_{sw} = \pm \frac{V_{dc}\, d(1-d)}{2\, L_o\, f_{sw}} = \pm \frac{V_{dc}}{8\, L_o\, f_{sw}}, \tag{3.1}$$

  if $d = 0.5$. The desired value of I_{sw} is obtained adjusting the value of L_o, typically between hundreds of nH and few µH, for a given f_{sw}.

- *Hard-Switching (HS)*: R_o is connected to the output node of the symmetric *LC* output filter to obtain Continuous Conduction Mode (CCM) operation and HS conditions. A sufficiently large value is selected for L_o (typically in the hundreds of µH range) to minimize the ripple on i_L, while the value of R_o is adjusted to achieve the desired and approximately constant

$$I_{sw} = \frac{d\,V_{dc}}{R_o}\,. \tag{3.2}$$

  To equally share the conduction losses between T_h and T_l, d could be fixed to 0.5 also in this case. However, when the setup is operated in CCM, the majority of the switching losses occur in T_h, which is HS (for $i_L > 0$). Hence, by utilizing the degree of freedom given by d, the major fraction of the conduction losses can be shifted to T_l, thus redistributing the total losses between T_h and T_l and equalizing their junction temperature T_j; by doing so, the maximum measurable losses are increased.

Both in ZVS and HS conditions, the maximum value of I_{sw} is reached once the conduction losses dominate the total losses (accuracy limit [54]) and/or when T_j cannot be anymore limited below 100 °C (thermal limit).

3.3 Measurement Methods

By operating the setup shown in **Fig. 3.1** as described in the previous section, the switching losses of the DUT can be measured and/or calculated according to the procedure described in the following. For this purpose, a thermal equivalent circuit of the measurement setup is first derived and calibrated determining the value of its parameters. Hence, once an accurate thermal model of the setup is obtained, calorimetric semiconductor loss measurements are performed continuously operating the setup in the conditions of interest, and estimating the occurring losses by matching measured and modeled (through the thermal equivalent circuit) thermal quantities, e.g. temperature variations. Finally, the switching losses are calculated from the results of the calorimetric loss measurements, subtracting all other loss contributions. The following analysis focuses only on the calorimetric measurement of semiconductor losses; different solutions to separate the switching losses from the measured losses (which, e.g. include the conduction losses) are discussed in [79].

3.3.1 T_{hs}-based Transient Calorimetric Switching Loss Measurement Method

A transient calorimetric measurement procedure, based on the analysis of the rise of the heat sink temperature T_{hs} over time, is originally presented in [76]. The associated thermal equivalent circuit is illustrated in **Fig. 3.2(a)**. Since this approach considers the thermal dynamics of T_{hs}, which is recorded by means of a fiber optic thermometer [82], only $C_{th,hs}$, i.e. the thermal capacitance of the solid brass heat sink thermally coupled with T_h and T_l, and $R_{th,hs\text{-}a}$, i.e. the thermal resistance between the heat sink and the ambient, mainly defined by the thermal insulating box surrounding the setup (see **Fig. 3.1(b)**), are included in the equivalent circuit. Nevertheless, particular attention must be paid to the thermal resistance from the junction of the DUT to the heat sink, since its value defines the maximum losses allowed in the setup not to exceed the maximum tolerable T_j.
In addition to a good thermal coupling between the DUT and the heat sink, also electric insulation is necessary between them, and a trade-off must be found. Since the heat sink is conductive, an insulating material must be inserted between the PCB and the heat sink to prevent a short-circuit. This feature is intrinsic in the Insulated Metal Substrate (IMS) board considered in [53], but a conventional PCB is preferred in this study to simplify the design procedure. A layer of the best-in-class thermal-pad [83] introduces an excessive thermal resistance if the vertical heat-flow from the DUT to the heat sink is constrained in the area defined by the case of the DUT. For this reason, two Cu heat-spreaders, i.e. one per DUT, are introduced in the vertical stack between the PCB and the thermal-pad. The high thermal conductivity of Cu allows the spreading of the heat-flow in the horizontal plane and the bottleneck introduced by the pad is alleviated due to the larger surface.
With the considered thermal model (see **Fig. 3.2(a)**), the differential equation

$$P_{T,tot} = C_{th,hs}\frac{dT_{hs}(t)}{dt} + \frac{T_{hs}(t) - T_{amb}}{R_{th,hs\text{-}a}}, \tag{3.3}$$

solved as

$$T_{hs}(t) = (T_o - P_{T,tot}\,R_{th,hs\text{-}a} - T_{amb})e^{-\left(t/R_{th,hs\text{-}a}\,C_{th,hs}\right)} + P_T\,R_{th,hs\text{-}a} + T_{amb}, \tag{3.4}$$

describes the evolution of $T_{hs}(t)$ (with $T_{hs}(0) = T_o$) after a step of the total semiconductor losses $P_{T,tot} = P_{T,h} + P_{T,l}$ (with $P_{T,h}$ and $P_{T,l}$ indicating the individual semiconductor losses) is applied to the system (at $t = 0$). (3.4) is of the type $y = 1 - e^{-|x|}$, with initial value T_o, steady-state value $P_T\,R_{th,hs\text{-}a} + T_{amb}$, and

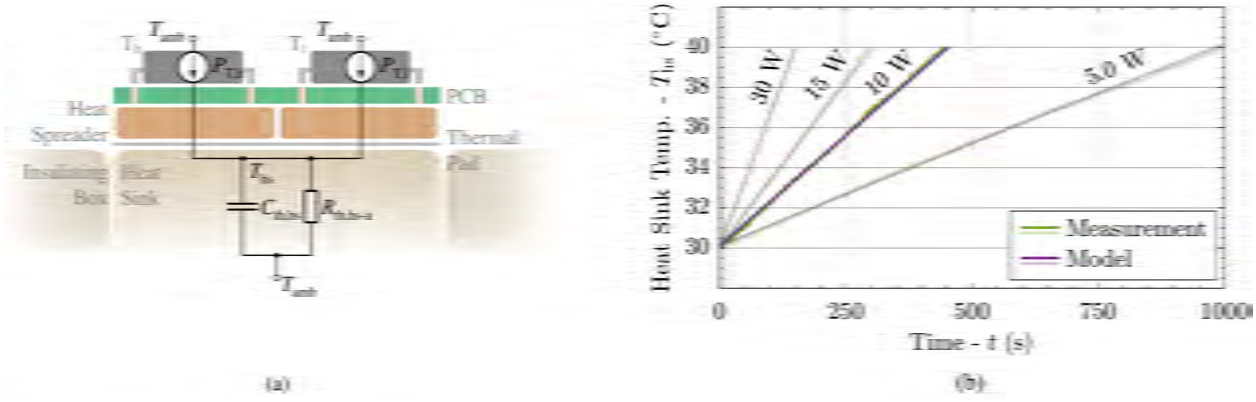


Fig. 3.2: (a) Thermal equivalent circuit of the switching loss measurement setup considered to apply the T_{hs}-based transient calorimetric measurement method. The equivalent circuit contains the heat sources $P_{T,h}$ and $P_{T,l}$ indicating the individual semiconductor losses, the thermal capacitance $C_{th,hs}$ of the heat sink connected to T_h and T_l, and the thermal resistance $R_{th,hs\text{-}a}$ between the heat sink and the ambient; T_{amb} indicates the ambient temperature. **(b)** Measured (green) and modeled (purple) waveforms of the heat sink temperature T_{hs} for different values of the total semiconductor losses $P_{T,tot}$. A variation of T_{hs} from 30 °C to 40 °C defines the duration of each measurement, function of $P_{T,tot}$.

several independent parameters. In particular, the ambient temperature T_{amb}, which can be easily measured, $R_{\text{th,hs-a}}$ and $C_{\text{th,hs}}$, dependent on the geometry and material properties of the setup, and $P_{\text{T,tot}}$, relative to the operating point. In a first calibration phase, both DUT are turned on and operated as resistors. Thus, a known constant power $P_{\text{T,tot}}$ is injected via the DUT into the thermal system at known T_{amb}, while T_{hs} is recorded from 30 °C to 40 °C. For consistency among the measurements, $T_{\text{hs}} = 30$ °C is always considered as measurement starting point. Repeating this procedure for several values of $P_{\text{T,tot}}$ yields to the set of curves illustrated in **Fig. 3.2(b)**. Hence, the values of $R_{\text{th,hs-a}}$ and $C_{\text{th,hs}}$ best fitting the measured curves according to a least-mean-square (LMS) regression performed on the model represented by (3.4) are extracted (see **Tab. 3.1**). As an example, measured (green) and modeled (purple) waveforms of T_{hs} for different values of $P_{\text{T,tot}}$ are depicted in **Fig. 3.2(b)**. The modeled waveforms are obtained inserting in (3.4) the measured values of $P_{\text{T,tot}}$ and T_{amb}, and the identified LMS optima $R_{\text{th,hs-a}}$ and $C_{\text{th,hs}}$.
In a subsequent measurement phase, i.e. when the half-bridge formed by the DUT is continuously operated in the operating point of interest, $P_{\text{T,tot}}$ is unknown but $R_{\text{th,hs-a}}$ and $C_{\text{th,hs}}$ remain unchanged. Consequently, the LMS regression can now be applied to estimate $P_{\text{T,tot}}$ from a new set of curves. The matching between the two set of curves in **Fig. 3.2(b)** ultimately guarantees accurate estimations of $P_{\text{T,tot}}$.
It is worth noticing that the measured curves associated with the highest values of $P_{\text{T,tot}}$, e.g. 30 W, are practically linear (i.e. the influence of $R_{\text{th,hs-a}}$ is not yet visible), which allows to simplify (3.3) to

$$P_{\text{T,tot}} = C_{\text{th,hs}} \frac{\mathrm{d}T_{\text{hs}}(t)}{\mathrm{d}t}. \tag{3.5}$$

In this case, once $C_{\text{th,hs}}$ is known, $P_{\text{T,tot}}$ is determined with good approximation by the ratio $^{\Delta T_{\text{hs}}}/_{\Delta t}$, where ΔT_{hs} indicates the temperature excursion within one measurement of duration Δt. Since typical resolutions of temperature and time measurements are 0.1 °C and 1 s respectively, $\Delta T_{\text{hs}} = 10$ °C and $\Delta t_{\text{min}} = 100$ s are imposed, limiting the quantization error to 1 % in both cases. To ensure $\Delta t \geq \Delta t_{\text{min}}$ with the highest value of $P_{\text{T,tot}}$, (3.5) is rearranged and an expression for the minimum feasible $C_{\text{th,hs}}$ is obtained. This parameter also defines the minimum difference in terms of Δt between measurements of similar $P_{\text{T,tot}}$, e.g. $\bar{P}_{\text{T,tot}}$ and $\bar{P}_{\text{T,tot}} + 10$ %.
In case $P_{\text{T,tot}}$ is significantly lower, the rate of change of T_{hs} over time is influenced also by $R_{\text{th,hs-a}}$. Hence, $R_{\text{th,hs-a}}$ should be maximized (e.g. through an insulating box) to increase the sensitivity of T_{hs} with respect to $P_{\text{T,tot}}$. It can still occur that T_{hs} does not reach 40 °C (never or not in reasonable time) for

Tab. 3.1: Parameters of the thermal equivalent circuit considered to perform the switching loss measurements of OptiMOS 3 FD Si power MOSFETs according to the T_{hs}-based transient calorimetric measurement method.

	Description	Value
$R_{th,j\text{-}c}$	junction-to-case thermal resistance	0.4 K/W
$R_{th,c\text{-}hs}$	case-to-heat sink thermal resistance	3.6 K/W
$C_{th,hs}$	heat sink thermal capacitance	460 J/K
$R_{th,hs\text{-}a}$	heat sink-to-ambient thermal resistance	32 K/W

very low values of $P_{T,tot}$; in this case, a maximum measurement time can be defined.
Even if this method is successfully adopted in [53, 74, 77, 79], possible improvements to it are identified in the reduction of the measurement time [75], and in the simplification of the measurement setup, which requires a dedicated heat sink. Following the proposed guideline, in fact, several (up to twenty) minutes are necessary to characterize a single operating point, not only because of the recommended lower boundary of the measurement times (necessary to ensure a satisfactory accuracy), but also because of the time required for the heat sink to cool down after each measurement. Differently, shorter measurement times are achieved in [76], but additional components are still necessary.

3.3.2 Ultra-Fast T_c-based Transient Calorimetric Switching Loss Measurement Method

If the transient behavior of the case temperature T_c of the DUT, rather than the one of T_{hs}, could be characterized, much shorter thermal time constants would be involved in the measurement procedure and no customized heat sink would be required. With this aim, the thermal equivalent circuit of the measurement setup (see **Fig. 3.1**) is extended as illustrated in **Fig. 3.3(a)** [76]. This thermal model additionally includes the thermal capacitances $C_{th,h}$ and $C_{th,l}$ of the case of T_h and T_l, and the resistive Π-network formed by $R_{th,h}$, $R_{th,l}$ and $R_{th,m}$. $R_{th,h}$ and $R_{th,l}$ indicate the thermal resistance between the heat sink and the case of T_h and T_l, respectively, while $R_{th,m}$ models the thermal coupling between T_h and T_l. The parameters of this thermal equivalent circuit, resulting from the calibration of the measurement setup, are listed in **Tab. 3.2**. From this equivalent circuit, a system of first-order linear ordinary differential

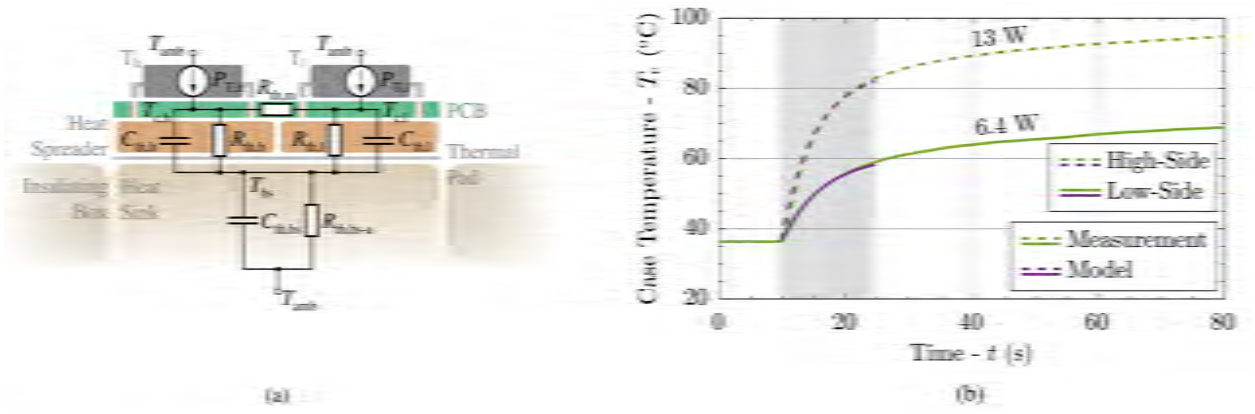


Fig. 3.3: **(a)** Thermal equivalent circuit of the switching loss measurement setup considered to apply the T_c-based transient calorimetric measurement method. The equivalent circuit contains, in addition to the elements described in **Fig. 3.2**, the thermal capacitances $C_{\mathrm{th,h}}$ and $C_{\mathrm{th,l}}$ of the case of $\mathrm{T_h}$ and $\mathrm{T_l}$, and the resistive Π-network formed by $R_{\mathrm{th,h}}$, $R_{\mathrm{th,l}}$ and $R_{\mathrm{th,m}}$. $R_{\mathrm{th,h}}$ and $R_{\mathrm{th,l}}$ indicate the thermal resistance between the heat sink and the case of $\mathrm{T_h}$ and $\mathrm{T_l}$, respectively, while $R_{\mathrm{th,m}}$ models the thermal coupling between $\mathrm{T_h}$ and $\mathrm{T_l}$. The thermal resistances from the case of the DUT to the ambient are neglected to limit the complexity of the model. **(b)** Measured (green) and modeled (purple) waveforms of the case temperatures $T_{\mathrm{c,h}}$ (dashed) and $T_{\mathrm{c,l}}$ (solid) for different values of the individual semiconductor losses $P_{\mathrm{T,h}}$ and $P_{\mathrm{T,l}}$. In this case, the measurement time is fixed to 15 s.

Tab. 3.2: Parameters of the thermal equivalent circuit considered to perform the switching loss measurements of OptiMOS 3 FD Si power MOSFETs according to the ultra-fast T_c-based transient calorimetric measurement method.

	Description	**Value**
$R_{th,h}$	$R_{th,c\text{-}hs}$ of T_h	3.9 K/W
$R_{th,l}$	$R_{th,c\text{-}hs}$ of T_l	3.3 K/W
$R_{th,m}$		30 K/W
$C_{th,h}$	$C_{th,c}$ of T_h	1.5 J/K
$C_{th,l}$	$C_{th,c}$ of T_l	1.8 J/K
$C_{th,hs}$		393 J/K
$R_{th,hs\text{-}a}$		∞

equations (ODEs) describing the evolution of the case temperatures $T_{c,h}$ and $T_{c,l}$ over time can be derived. In particular,

$$\begin{bmatrix} \dfrac{dT_{c,h}}{dt} \\ \dfrac{dT_{c,l}}{dt} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_{th,h}+R_{th,m}}{C_{th,h}\,R_{th,h}\,R_{th,m}} & \dfrac{1}{C_{th,h}\,R_{th,m}} \\ \dfrac{1}{C_{th,l}\,R_{th,m}} & -\dfrac{R_{th,l}+R_{th,m}}{C_{th,l}\,R_{th,l}\,R_{th,m}} \end{bmatrix} \begin{bmatrix} T_{c,h} \\ T_{c,l} \end{bmatrix} + \begin{bmatrix} \dfrac{P_{T,h}}{C_{th,h}} \\ \dfrac{P_{T,l}}{C_{th,l}} \end{bmatrix} \tag{3.6}$$

$$\frac{dT_{hs}}{dt} = \frac{P_{T,h}+P_{T,l}}{C_{th,hs}}\,. \tag{3.7}$$

is obtained. Solving (3.6) for $T_{c,h}$ and $T_{c,l}$ provides the expressions necessary to estimate the values of $P_{T,h}$ and $P_{T,l}$. Hence, the variations of $T_{c,h}$ and $T_{c,l}$ for given values of $P_{T,h}$ and $P_{T,l}$ can be calculated from (3.6), or unknown values of $P_{T,h}$ and $P_{T,l}$ can be estimated from the fitting on the measured variations of $T_{c,h}$ and $T_{c,l}$, as described in **Section 3.3.1**. Accordingly, measured (green) and modeled (purple) waveforms of $T_{c,h}$ (dashed) and $T_{c,l}$ (solid) for different values of $P_{T,h}$ and $P_{T,l}$ are depicted in **Fig. 3.3(b)** and in **Fig. 3.4(b)-(c)**, for the measurement setup shown in **Fig. 3.1** and **Fig. 3.4(a)**. In this case, the measurement time (highlighted in gray in **Fig. 3.3(b)**) is fixed to 15 s (counted from time $t = 10$ s, i.e. when the setup starts to operate, to $t = 25$ s), since this is sufficient to capture the transient behavior of T_c. In fact, approximately for $t > 30$ s, the variation of T_c is only determined by the variation of T_{hs} (cf. **Fig. 3.2(b)** and **Fig. 3.3(b)**). Hence, significantly shorter measurement

Fig. 3.4: (a) Photo of the measurement setup with the high frame rate and high resolution thermal imaging camera [84] and a frame captured during a measurement. **(b)-(c)** Measured (green) and modeled (purple) waveforms of the case temperatures $T_{c,h}$ (dashed) and $T_{c,l}$ (solid) for different values of the individual semiconductor losses $P_{T,h}$ and $P_{T,l}$.

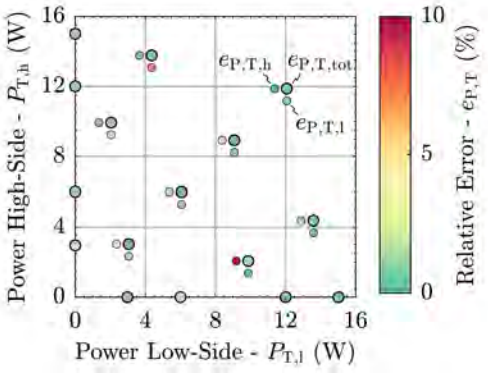


Fig. 3.5: Relative error on the T_c-based transient calorimetric loss measurement method on the estimation of $P_{T,tot}$, i.e. $e_{P,T,tot}$ (large dot of each triplet), and of $P_{T,h}$ and $P_{T,l}$, i.e. $e_{P,T,h}$ (left small dot) and $e_{P,T,l}$ (bottom small dot), in dependency of $P_{T,h}$ and $P_{T,l}$ (approximately $0\,W \leq P_{T,h} < 15\,W$ and $0\,W \leq P_{T,h} < 15\,W$). The measurement accuracy is considered satisfactory, since $e_{P,T,tot}$ is below 3 % for all calibrated cases.

times, compared to the T_{hs}-based method, can be achieved in this case. To maintain a high measurement resolution with shorter measurement times, the high frame rate (up to hundreds of frames-per-second) high resolution thermal imaging camera [84] shown in **Fig. 3.4(a)** is used to measure $T_{c,h}$ and $T_{c,l}$. In particular the camera measures the average temperature of specified areas, e.g. coinciding with the package of T_h and T_l. In the selected measurement time window (which corresponds to the window on which the fitting algorithm for determining the parameters of the thermal model is applied), the matching between measured and modeled curves is remarkable, hence accurate estimations of $P_{T,tot}$, as well as of $P_{T,h}$ and $P_{T,l}$, are expected.
This is verified for all operating points of interest, i.e. approximately $0\,W \leq P_{T,h} < 15\,W$ and $0\,W \leq P_{T,l} < 15\,W$, by comparing the estimated values of $P_{T,tot}$, $P_{T,h}$ and $P_{T,l}$ to a reference electric measurement. The comparison is performed in DC conditions, such that constant values of $P_{T,h}$ and $P_{T,l}$, supplied from a power source, can be accurately measured with precision multimeters. The obtained relative errors, both on the total power $e_{P,T,tot}$ and on the individual ones $e_{P,T,h}$ and $e_{P,T,l}$, are depicted in **Fig. 3.5**. It can be observed that $e_{P,T,tot}$ is limited below 3 % (0.8 % on average), while $e_{P,T,h}$ and $e_{P,T,l}$ are 2.3 % and 2.0 %, respectively.

3.3.3 Comparison of the Transient Calorimetric Switching Loss Measurement Methods

As anticipated, several advantages are introduced by the T_c-based approach compared with the T_{hs}-based one. First, $P_{T,h}$ and $P_{T,l}$ can be estimated separately, since both $T_{c,h}$ and $T_{c,l}$ are measured (rather than only T_{hs}). This possibility can be exploited when the loss distribution between T_h and T_l is asymmetric; however, if e.g. $P_{T,h} \gg P_{T,l}$, an excessive coupling between $T_{c,h}$ and $T_{c,l}$ can negatively affect the measurement accuracy of the individual semiconductor losses. Second, and most important, the measurement time is conveniently reduced to a few seconds, i.e. to the time sufficient to capture the transient behavior of T_c. Moreover, using the high resolution thermal imaging camera, there is no inaccuracy of the temperature measurement due to electromagnetic coupling, as could occur with thermocouples or dedicated ICs [75]. In principle, any temperature measurement device can be used, however, an excessively large sampling time inevitably penalizes the measurement accuracy. Finally, no additional component, e.g. no customized heat sink, must necessarily be installed on the power circuit to perform the measurements. Hence, this switching loss measurement method can be more easily applied to existing power converters.

3.4 Conclusion

In this chapter, two transient calorimetric measurement techniques suitable to accurately determine the switching losses of fast switching power semiconductors are presented. These methods, based on heat sink or case temperature rise monitoring, allow to quickly and accurately determine the switching losses of WBG power devices in half-bridge arrangement, at any operating point, and independent of their characteristics. At first, analytical expressions describing the time behavior of the thermal models of the realized measurement setup are derived. Then, the proposed measurement procedures are presented and critically compared. Finally, experimental results, proving the applicability and accuracy of both methods are discussed. The obtained switching loss data are key enablers for the multi-objective optimization of modern power converters, and thus can support the progress of power electronics in the realization of high efficiency and extremely compact converters.

Part 2

Performance Bottlenecks of Wide-Bandgap Semiconductors

4

On the Origin of the C_{oss}-Losses in GaN-on-Si HEMTs

This chapter summarizes the most relevant findings in the context of research on the origin of the C_{oss}-losses in GaN-on-Si HEMTs, which are also published in:

- **M. Guacci**, M. Heller, D. Neumayr, D. Bortis, J. W. Kolar, G. Deboy, C. Ostermaier, and O. Häberlen, "On the Origin of the C_{oss}-Losses in Soft-Switching GaN-on-Si Power HEMTs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 679–694, 2019.

Motivation

Losses occurring during the charging process of the parasitic output capacitance of currently available WBG power semiconductors limit the envisaged increase of switching frequency and compromise the efficiency of modern power converters. The developed accurate switching loss measurement method is a key enabler for the investigation of this phenomenon.

Executive Summary

The unprecedented performance potential of GaN-on-Si HEMTs is seen as key enabler for the design of power converters featuring extreme power density figures, as demanded in next generation power electronics applications. However, unexpected loss mechanisms, i.e. dynamic $R_{ds,on}$ phenomena and C_{oss}-losses, are appearing in currently available GaN transistors and are compromising their operation. In this chapter, measurements of C_{oss}-losses are performed in a dedicated calorimetric measurement setup and, through a systematic approach, the root cause of this loss mechanism is identified. Afterwards, with the essential support of a manufacturer of power semiconductors, a novel transistor, featuring an enhanced multi-layer III-N buffer, is developed based on the acquired knowledge. A significant reduction in terms of C_{oss}-losses, i.e. of soft-switching losses, and the absence of dynamic $R_{ds,on}$ phenomena are verified experimentally on the new device. These achievements enable a significant performance improvement for future soft-switching power converters featuring GaN-on-Si HEMTs.

4.1 Introduction

The remarkable electron mobility and breakdown electric field figures of GaN, together with a revolutionary semiconductor structure based on a 2D electron gas (2DEG) [85], enable the realization of GaN-on-Si HEMTs with outstanding switching and conduction performance [79]. Nowadays, normally-off GaN transistors are widely adopted in power density optimized converters featuring voltages up to 500 V [41] and are foreseen as promising semiconductor solutions for power converters on-board of EVs and MEA [79]. The above mentioned features guarantee high efficiencies, e.g. 99 %, even at high switching frequencies, especially when soft-switching modulation schemes and/or converter concepts are considered [41]. The excellent switching and conduction performance results in lowered cooling and filtering requirements [79], hence in unbeatable power density figures, since magnetic components and heat sink elements often dominate the volume and weight breakdowns of power converters [41].

GaN power transistors are commercially available for only about seven years, but, because of their promising performance, soon became a trending research topic in the power electronics community. Accordingly, GaN devices have been thoroughly investigated in the last years, and several unexpected, and not yet completely understood, loss mechanisms have been observed. Among them, dynamic $R_{ds,on}$ phenomena and C_{oss}-losses are of main importance,

since they can significantly limit the potential of these devices. Dynamic $R_{\mathrm{ds,on}}$ phenomena can be explained by stored and/or trapped charges in the channel of GaN devices, which lead to a temporary increase of the drain-source resistance $R_{\mathrm{ds,on}}$, i.e. of the occurring conduction losses, after the transistors are turned on. Although this issue is still not completely solved by most of the manufacturers [39, 42], it is at least well characterized in literature [44]. The expression *C_{oss}-losses*, instead, defines a loss mechanism relative to the charging/discharging process of the parasitic output capacitance C_{oss} of power transistors, particularly affecting the performance of soft-switching power converters. Soft-switching operation is ideally considered loss-less from the point of view of the power semiconductors, however, evidences of $\mathrm{d}v/\mathrm{d}t$-dependent C_{oss}-losses, i.e. of current-dependent soft-switching losses, are recently documented in literature, also for GaN devices [53, 69, 71, 86]. Accordingly, soft-switching operation of GaN power transistors is shown to be lossy, and to even compromise the operation and the efficiency of soft-switching power converters switching in the MHz-range. As an example, the measured efficiency of the soft-switching Class-Φ_2 inverter presented in [71] resulted 5 % lower than what originally estimated. The main responsible for this discrepancy was identified in the unexpected C_{oss}-losses. However, despite this substantial influence and in contrast to the case of dynamic $R_{\mathrm{ds,on}}$ phenomena, currently only few evidences of C_{oss}-losses in GaN-on-Si HEMTs are available in literature, and only unconfirmed hypotheses on their origin are speculated. This provides a solid motivation to this study, essentially aiming to identify the cause of C_{oss}-losses in GaN-on-Si HEMTs.

Loss mechanisms in capacitors, e.g. C_{oss}-losses, are typically quantified evaluating the hysteresis curve originating from charging/discharging a sample with large signal voltage waveforms. This method, based on the Sawyer-Tower (ST) circuit, has first been used in 1929 [87] to measure the ferro-electric hysteresis loop of Rochelle salt, but recently gained new attention after being applied to SJ Si MOSFETs [88], where the first evidences of C_{oss}-losses were observed. In this ST experiment, the MOSFET is kept permanently off and a sinusoidal voltage waveform is applied across its drain and source terminals, i.e. to C_{oss}. The hysteresis in the voltage-charge plane, observed during the charging and discharging processes of C_{oss}, is then providing a direct measure of the energy lost in a full charging/discharging cycle.

The underlying loss mechanism can be understood by analyzing the dynamics of charge transport within the p- and n-columns characterizing the SJ structure highlighted in **Fig. 4.1(a)** [89]. During the charging process of C_{oss}, i.e. the turn-off transition of a SJ device, the space charge region expands around the surface of the blocking pn-junction formed by the deep p-columns,

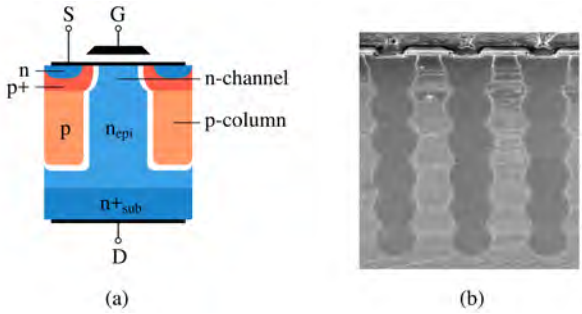


Fig. 4.1: Cross-section of a SJ Si MOSFET highlighting **(a)** the different doping concentrations and the characteristic 3D structure of p- and n-columns and **(b)** the inhomogeneity of the doping profiles as a results of the multi-epitaxy technology and subsequent implantation of p-dopants.

hence reaching far into the active area of the device. If stranded charges are left within the p-columns during the depletion, they can no longer flow as majority carriers, thus creating losses. Since this loss mechanism is largely associated with stranded charges [89], losses can only occur during the depletion process of the p-columns. The sharp variation of C_{oss} at around 50 V, typical for SJ devices, indicates that the depletion process is fully completed around this voltage. Later technology nodes (with lower area-specific on-state resistance) often achieve an even earlier, i.e. at lower voltages, depletion of the p- and n-column structure. Generally, the design of the SJ structure, e.g. in terms of doping concentration, and the technology considered for its realization have a significant influence on the formation of stranded charges [89]. **Fig. 4.1(b)** shows, as an example, a cross-section of a SJ structure created by multiple epitaxy steps and subsequent implantation of p-dopants. As this type of technology creates locally strongly varying doping concentrations in both p- and n-regions, special care is taken to ensure a seamless depletion of the p-columns. It can be concluded that the results obtained applying the ST method to SJ devices [88] provided a physical understanding and a solid basis for the reduction of the C_{oss}-losses and/or of the soft-switching losses observed in SJ Si MOSFETs [53].
Differently from SJ devices, GaN-on-Si HEMTs feature symmetric C_{oss} charging and discharging processes and have an entirely distinct device structure, i.e. dopant charges are practically not present. Hence, a different loss mechanism, investigated in the following, must be at the origin of the observed $^{dv}/_{dt}$-dependent C_{oss}-losses [69].

Conventional ST measurement setups can achieve values of $\mathrm{d}v/\mathrm{d}t$ typical for the operation of GaN devices only when high frequencies, in the range of tens of MHz, are considered. Moreover, sinusoidal voltage waveforms, common in the ST method, are generally not representative of the operating conditions of a device in a switching circuit. Additionally, several motivations discussed in [52] discourage the usage of any electric measurement method to characterize soft-switching losses, especially when high switching speeds, i.e. transitions showing $\mathrm{d}v/\mathrm{d}t$, are involved, mainly because of their limited accuracy. Given the similarity between soft-switching losses and C_{oss}-losses, for the above mentioned reasons, calorimetric measurement methods [52, 53, 90] should be preferred over electric measurement methods [91], i.e. the ST method.

In [71], a calorimetric measurement method is proposed to characterize C_{oss}-losses in GaN transistors. In particular, in order to isolate C_{oss}-losses from other sources of loss, high $\mathrm{d}v/\mathrm{d}t$ voltage waveforms are generated across the C_{oss} of several permanently turned off transistors. Hence, the steady-state temperature of each DUT is measured, and the occurring losses are estimated by means of the known thermal resistances of the system. The mentioned voltage waveform is generated by a switching circuit placed physically very close to the DUT, i.e. avoiding that parasitic elements, as otherwise introduced by an electrically long connection, could distort the signal and compromise the measurements. However, this inevitably leads to a measurement setup where self and mutual (between the DUT and the exciting circuit) thermal resistances are in the same order of magnitude. Since the losses occurring in the DUT are only a small share of the total losses occurring in the overall setup, it can be shown that a small error in the temperature measurement, and/or in the estimation of the thermal resistances, can cause a significant error in the final measurement results [69].

At the contrary, in the setup presented in [52], the DUT is thermally well isolated from the exciting half-bridge, but a significant parasitic inductance is introduced by their connection. However, the voltages at stake (around 7 kV) are significantly higher than the ones characterizing GaN transistors (up to 600 V), and allow to neglect voltage distortions, e.g. oscillations, with amplitudes up to several hundreds of volts. A novel approach, ideally combining the advantages of both [52] and [69], is developed along this chapter to accurately measure C_{oss}-losses occurring in GaN-on-Si HEMTs.

Finally, as stated in [69], it was impossible, up to now, to address the root cause of the observed C_{oss}-losses in GaN devices mainly because the detailed device constructions are proprietary to the device manufacturers, which prevents a clear understanding of the loss mechanisms. For this reason,

Tab. 4.1: Main characteristics of the IGT60R070D1 [92] *CoolGaN* e-mode GaN power transistor from *Infineon*. Subscript Q and E in C_{oss} differentiate charge equivalent and energy equivalent capacitances.

$V_{ds,MAX}$	$I_{dc,MAX}$ @ 25 °C	$R_{ds,on}$ @ 25 °C	$C_{oss,Q} - C_{oss,E}$ (pF) @ 100 V	@ 200 V	@ 300 V	@ 400 V
600 V	31 A	55 mΩ	170 − 146	131 − 104	111 − 85	101 − 79

with the aim to remedy the C_{oss}-losses observed in GaN-on-Si HEMTs, the insight of the semiconductor manufacturers is considered fundamental. Accordingly, it is preferred to focus on a single transistor, of which a variety of different prototypes and detailed information are available through the manufacturer itself, rather than characterizing transistors of different types. Because of an on-going research collaboration, the choice is guided towards the IGT60R070D1 [92] *CoolGaN* e-mode GaN power transistor from *Infineon*, whose main characteristics are reported in **Tab. 4.1**.
In **Section 4.2**, the setup initially considered to characterize the soft-switching losses of the analyzed GaN-on-Si HEMT is described from the electric and thermal point of view, whereas in **Section 4.3** the results of the soft-switching loss measurements are presented. In **Section 4.4**, a novel measurement setup, enabling the isolation of the C_{oss}-losses, is illustrated, and the results of the relative measurements are discussed. **Section 4.5** offers a detailed description of the internal structure of the considered transistor, allowing to speculate on the cause of the measured losses. Afterwards, in **Section 4.6**, a novel measurement procedure, aiming to identify the region of the transistor where the losses are originated, is described. The acquired knowledge facilitates the design of an enhanced GaN-on-Si HEMT which, as expected and confirmed in **Section 4.7**, does not exhibit any C_{oss}-losses nor dynamic $R_{ds,on}$ phenomena. **Section 4.8** concludes the work summarizing the achievements.

4.2 Calorimetric Soft-Switching Loss Measurements

The results of the soft-switching loss measurements relative to a GaN-on-Si HEMT presented in [53] are significantly higher than expected according to the device simulations performed by the semiconductor manufacturer itself. With the aim of investigating the possible reasons causing this discrepancy,

e.g. an unexpected loss mechanism like the C_{oss}-losses, a novel calorimetric measurement setup is designed and new experimental measurements are performed. The DUT is a commercial *CoolGaN* e-mode GaN power transistor IGT60R070D1 from *Infineon* [92] with the characteristics listed in **Tab. 4.1**. In this section, the measurement setup, the modified measurement procedure, and the improvements aiming to enhance the measurement accuracy (with respect to [53]) are first described; afterwards, the obtained measurement results are presented and discussed.

4.2.1 Description of the Measurement Setup

From the electric point of view, the considered measurement setup essentially consists of the DC-source V_{dc}, the input filter L_{dc}-C_{dc}, the switching half-bridge T_1-T_2 (T_1 and T_2 are, herein, the DUT) and the output inductor L_{load} connected from the switch node of the half-bridge to the mid-point of the split DC-link, as shown in **Fig. 4.2**. The half-bridge output voltage and current are denominated v_{ds} and i_{load}, respectively. L_{dc} has the only purpose of protecting the DC-source from high frequency current harmonics. As also visible in **Fig. 4.3**, C_{dc} is formed by the parallel connection of $C_{dc,h}$ and $C_{dc,l}$ with $C_{dc,hf}$; $C_{dc,h\text{-}l}$ are energy storage film-capacitors designed to maintain a constant DC-link voltage during operation of the half-bridge, whereas $C_{dc,hf}$ are low parasitics multi-layer ceramic capacitors (MLCCs) [93] installed to

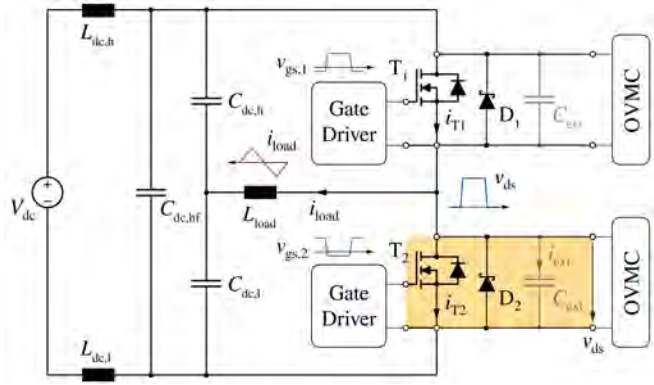


Fig. 4.2: Schematic of the realized soft-switching loss measurement setup consisting of the half-bridge formed by the two DUT T_1 and T_2. With the considered modulation scheme (see $v_{gs,1}$ and $v_{gs,2}$), the illustrated waveforms of v_{ds} and i_{load} are obtained.

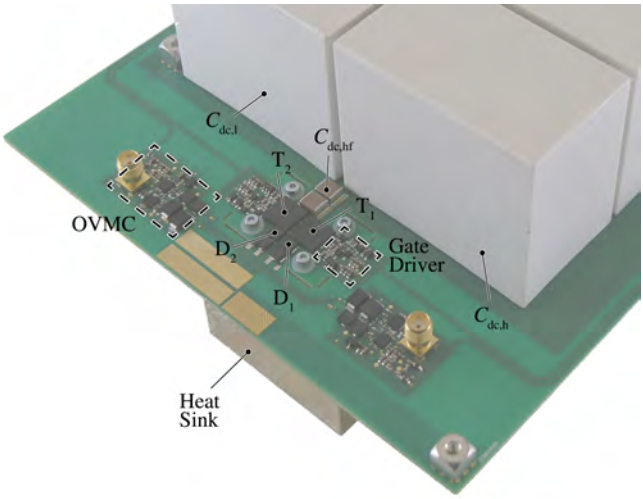


Fig. 4.3: Picture of the realized soft-switching loss measurement setup. The switching half-bridge formed by the two DUT T_1 and T_2, the anti-parallel diodes D_1 and D_2, the gate drivers, the OVMCs and the capacitors $C_{dc,h}$, $C_{dc,l}$, and $C_{dc,hf}$ are highlighted.

improve the switching performance of the half-bridge (i.e. to minimize the commutation loop inductance, thus preventing overvoltage and voltage oscillations after high speed switching transitions [39]). The combination of L_{load} with $C_{dc,h\text{-}l}$ serves as well as output voltage filter. SiC Schottky diodes [65] D_1 and D_2, featuring a much lower threshold voltage compared to the DUT in reverse conduction [92], are connected in parallel to T_1 and T_2 to reduce the conduction losses occurring during the dead-times t_{dt} of the half-bridge. C_{ext} are MLCCs [94] necessary for measurement purposes, as described in **Section 4.3**. The selected gate drivers and the on-state voltage measurement circuits (labeled OVMC in **Fig. 4.2** and **Fig. 4.3**) are thoroughly described in [40] and [95] respectively, and just adapted herein for the needs of this setup.
The adopted modulation scheme consists of a 50 % duty-cycle PWM signal with a switching frequency $f_{sw} = 1\,\text{MHz}$ (see $v_{gs,1}$ and $v_{gs,2}$ in **Fig. 4.2**). Thus, the switch node voltage v_{ds} resembles a symmetric square-wave shaped waveform of amplitude V_{dc} and, accordingly, a symmetric (with respect to 0 A)

Tab. 4.2: Circuit parameters and value of the components of the realized soft-switching loss measurement setup shown in **Fig. 4.2**.

	Description	Value	Note
V_{dc}	DC-source voltage	100 V… 400 V	
$L_{dc,h\text{-}l}$	DC-input inductor	1 mH	
$C_{dc,h\text{-}l}$	split DC-link capacitors	60 µF	
$C_{dc,hf}$	DC-snubber capacitor	4.4 µF	[93]
L_{out}	output inductor	0.6 µH… 10 µH	
$T_{1\text{-}2}$	DUT		**Tab. 4.1**
$D_{1\text{-}2}$	anti-parallel diodes		[65]
C_{ext}	external capacitor	0… 100 pF	[94]
f_{sw}	switching frequency	1 MHz	
I_{sw}	switched current	5 A… 20 A	

triangular current waveform i_{load} of peak value I_{sw},

$$\frac{V_{dc}}{2} = L_{load}\frac{2\,I_{sw}}{1/2 f_{sw}} \quad \longrightarrow \quad I_{sw} = \frac{V_{dc}}{8\,L_{load}\,f_{sw}}, \tag{4.1}$$

appears at the output of the half-bridge. Hence, V_{dc} and $\pm I_{sw}$ correspond to the switched voltage and switched current, respectively. Further details of all circuit parameters and components are provided in **Tab. 4.2**.
In order to vary the operating point of the half-bridge, V_{dc} is adjusted through the DC-source, f_{sw} is maintained constant, and L_{load} is modified according to (4.1) to obtain the desired I_{sw}. **Fig. 4.4** shows typical waveforms of v_{ds} and i_{load} for one switching period in case of $V_{dc} = 400\,\text{V}$ and $I_{sw} \approx 20\,\text{A}$. The current flowing in T_2 is additionally included in **Fig. 4.4** to highlight the conduction time of T_2 (corresponding to $v_{ds} \approx 0\,\text{V}$).
When I_{sw} and the energy stored in L_{load} during the switching transitions of the half-bridge (i.e. $\approx L_{load} I_{sw}^2/2$) are sufficient to charge and/or discharge the equivalent capacitance of the switch node ($\approx 2\,C_{oss}$) during t_{dt}, complete soft-switching operation is guaranteed, and sensible soft-switching loss measurements can be carried out.
The fundamental principle of soft-switching operation can be visualized focusing on the waveform of the calculated instantaneous power p_{T_2} at the terminals of T_2, also shown in **Fig. 4.4**. Depending on the direction of the slope of v_{ds}, C_{oss} of T_2 is charged (positive slope of v_{ds}, turn-off transition of T_2) or discharged (negative slope, turn-on) by i_{load}. Generally, i_{load} acts

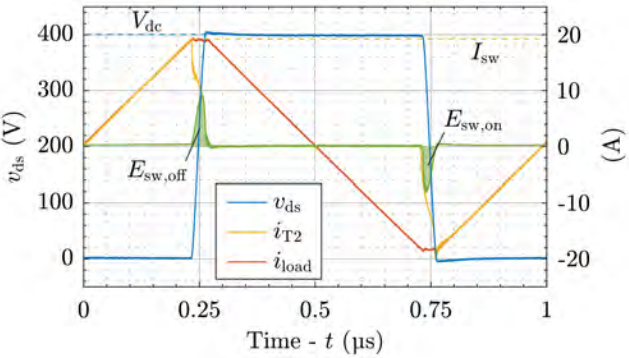


Fig. 4.4: Main waveforms characterizing the half-bridge shown in **Fig. 4.2** in soft-switching operation, i.e. v_{ds}, i_{load}, i_{T2} and p_{T2} for one switching period ($f_{sw} = 1\,\text{MHz}$) in case $V_{dc} = 400\,\text{V}$ and $I_{sw} \approx 20\,\text{A}$.

as a current source charging or discharging the parallel connection of C_{oss} of the two DUT. Consequently, a certain amount of energy (calculated as the area underlying p_{T2}) is stored $E_{sw,off}$ in or released $E_{sw,on}$ from C_{oss} of T_2 (the opposite occurs for T_1). As suggested by preceding measurements, this process causes losses and, in particular, the soft-switching losses E_{sw} can be defined as the difference between $|E_{sw,on}|$ and $E_{sw,off}$.
It is worth mentioning that the considered setup (see **Fig. 4.2**) features the advantage of emulating, for the DUT, the very same switching conditions occurring in a power converter operating in soft-switching. Hence, the results of these measurements are expected to be representative of the real switching performance, i.e. to provide accurate soft-switching loss data, e.g. useful for the multi-objective optimization of soft-switching power converters [41].

4.2.2 Description of the Measurement Procedure

The subtractive calorimetric measurement method introduced in [53] is applied in the following. Accordingly, to isolate the switching losses P_{sw}, all other loss contributions, combined in P_{ext}, are identified, estimated (measured or calculated), and subtracted from the power P_{tot} resulting from the calorimetric measurement, i.e.

$$P_{sw} = P_{tot} - P_{ext}. \tag{4.2}$$

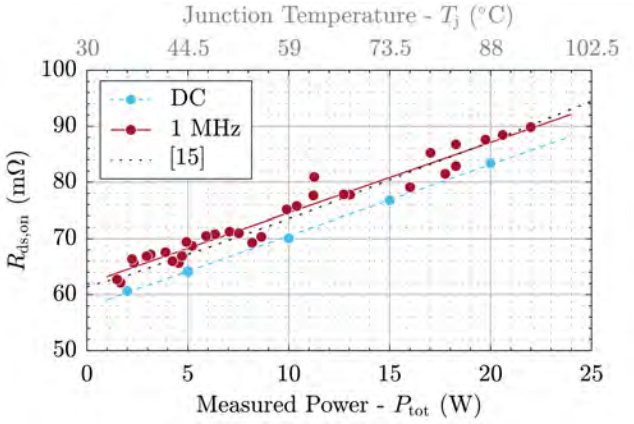


Fig. 4.5: Measured $R_{ds,on}$ in soft-switching operation (solid) compared with the values measured during calibration (dashed), and with the nominal values reported in the datasheet of the DUT [92] (dotted), as function of P_{tot} and at $T_{hs} = 30\,°C$. T_j, obtained in first approximation as $T_{hs} + P_{tot}(R_{j\text{-}c}+R_{c\text{-}hs})/2$, is additionally indicated to facilitate the comparison with the corresponding plot reported in [92].

As discussed in [95], the accuracy of P_{sw} (σ_{Psw} is e.g. the worst-case uncertainty of P_{sw}) is influenced from the accuracy of both the calorimetric measurement itself, and of the estimations defining P_{ext} (σ_{Pext}). However, intuitively (or as formally derived in [95]) the impact of σ_{Pext} on σ_{Psw} is reduced proportionally to P_{sw}/P_{ext} (see **Appendix B**). To increase this ratio, P_{sw} is maximized keeping $f_{sw} = 1\,MHz$, and attention is paid to accurately estimate all the identified contributions to P_{ext}, minimizing σ_{Pext}. In particular:

- The OVMC developed in [95] is connected to each DUT to measure the real-time value of the on-state resistance $R_{ds,on}$, and accurately calculate the occurring conduction losses P_{cond}, which are major contributors to P_{ext}. The results of these measurements are summarized in **Fig. 4.5**, where the measured $R_{ds,on}$ in soft-switching operation (solid) is compared with the values measured during calibration (dashed), and with the nominal values reported in the datasheet of the DUT [92] (dotted), as function of the measured (or estimated from T_j in the case of the datasheet) P_{tot}, and at $T_{hs} = 30\,°C$. It is worth mentioning that, different from other GaN devices analyzed in [95], these DUT do not feature any dynamic $R_{ds,on}$ phenomena [44], and there is a very good agreement between the measured and nominal $R_{ds,on}$.

- Conduction losses occur in D_1 and D_2 during t_{dt}, and are calculated and subtracted. In each operating point, t_{dt} is adjusted to ensure the completion of the switching transition, while minimizing the diode conduction time with the maximum resolution allowed by the digital control circuit. It should be noticed that, since the time resolution on setting t_{dt} is limited, and the safety margin with respect to the completion of the switching transition can be assumed constant, further increasing f_{sw} to increase P_{sw} inevitably leads to a higher impact of this loss contribution to the final measurement accuracy, because $t_{dt}f_{sw}$ increases.

- The equivalent series resistances (ESRs) of $C_{dc,h\text{-}l}$ and $C_{dc,hf}$ cause additional conduction losses during switching operation. It is challenging to measure the current flowing, e.g. through $C_{dc,hf}$, denominated $i_{Cdc,hf}$, without affecting the commutation loop inductance of the half-bridge formed by the DUT [39]. Therefore, the parasitic elements of the circuit are measured and/or estimated, and comprehensive simulations are performed to determine $i_{Cdc,hf}$. **Fig. 4.6** shows, as an example, the Fourier transform of the simulated $i_{Cdc,hf}$ (solid) in combination with the value of ESR of $C_{dc,hf}$ specified in its datasheet [93] (dashed). This information allows to calculate the occurring losses in $C_{dc,hf}$, and a similar procedure is followed also for $C_{dc,h\text{-}l}$ and C_{ext}. The losses in the PCB dielectric are calculated not to have any significant impact on P_{tot}, and are therefore neglected. This is achieved minimizing the parasitic capacitance of the PCB in the design phase, which is also of importance to maximize the achievable dv/dt for a given I_{sw}. Similarly, the losses in any other parasitic capacitor are neglected too.

- In a soft turn-off switching transition of T_2, it could happen that v_{ds} rises before the channel of T_2 is completely opened (the opposite holds for T_1). The time overlap of non-zero voltage and current creates V-I overlap losses. It is impossible to separate the current flowing in the channel of T_2 from the one flowing in its C_{oss} by means of measurements. However, the existence of V-I overlap losses is excluded in this case, since $v_{gs,2}$ is measured to reach the specified threshold, i.e. $i_{T_2} = 0$ A, before v_{ds} rises (given the presence of C_{oss}). To support this thesis, a circuit model is developed and simulations based on the measured waveforms are performed; finally, the V-I overlap losses are quantitatively evaluated and, although negligible, subtracted.

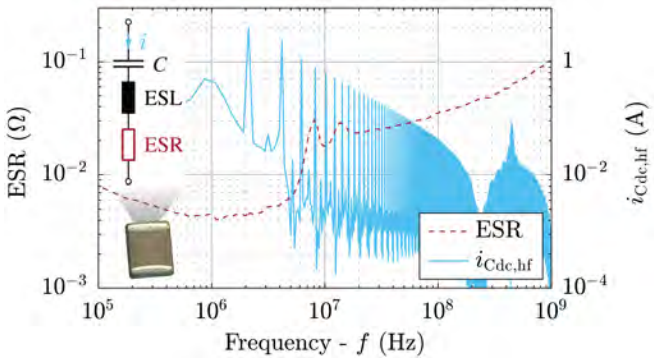


Fig. 4.6: Fourier transform of the simulated $i_{\mathrm{Cdc,hf}}$ (solid) and nominal ESR of $C_{\mathrm{dc,hf}}$ [93] (dashed) considered to calculate the losses occurring in $C_{\mathrm{dc,hf}}$ during switching operation.

- The impact of the losses occurring in the auxiliary circuits, e.g. the gate drivers and the OVMCs, is estimated operating them individually.

All the listed contributions to P_{ext} (except for P_{cond}) are generally below 20 % of P_{sw}, i.e. even a significant error on their estimation is ideally attenuated up to five times once P_{sw} is calculated [95]. However, to improve the measurement accuracy, it is important to estimate them carefully, especially benefiting of the implemented OVMCs for the calculation of P_{cond} [95], since $P_{\mathrm{sw}}/P_{\mathrm{cond}} \approx 0.5$ for the highest values of I_{sw}.

4.3 Soft-Switching Loss Measurement Results

Considering the measurement setup and procedure described in the previous section, P_{sw} is measured for different operating conditions of the DUT, i.e. with V_{dc} ranging from 100 V to 400 V (in 100 V steps) and I_{sw} from 5 A to 20 A (in 5 A steps). Assuming symmetry, the resulting P_{sw} of the half-bridge are halved to obtain the losses of a single DUT, and divided by f_{sw} to provide data independent of frequency. The obtained $E_{\mathrm{sw}} = P_{\mathrm{sw}}/(2\,f_{\mathrm{sw}})$ are plotted as function of I_{sw} in **Fig. 4.7** (dots) for different V_{dc}. The dependency of E_{sw} on V_{dc} and I_{sw} is evident. Moreover, since the data relative to a single V_{dc} are aligned, linear interpolations are performed and shown (solid). The linear model fits the measurement results except for the case of $I_{\mathrm{sw}} = 20$ A where, mainly because of P_{cond}, σ_{Psw} is more significantly affected from σ_{Pext}.

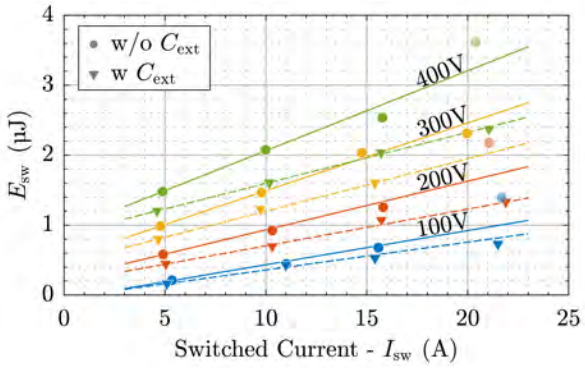


Fig. 4.7: E_{sw} as function of I_{sw} (5 A... 20 A) for different V_{dc} (100 V... 400 V). E_{sw} without (dots) and with (triangles) C_{ext} are compared.

Overall, E_{sw} summarized in **Fig. 4.7** are lower than their counterpart reported in [53], potentially because of the following reasons:

- The DUT belong to a new generation of *CoolGaN* which features 30 % reduced C_{oss}, thus improved switching performance compared to the prototype samples considered in [53].
- The enhancements brought to the measurement procedure, as described in **Section 4.2.2**, significantly improves σ_{Pext} and therefore σ_{Psw}. Moreover, carefully characterizing (and subtracting) all the contributions to P_{ext}, finally ends up reducing P_{sw} according to (4.2).
- The measurement setup considered in [53] is based on an IMS board which guarantees good thermal coupling and electric isolation between the DUT and the heat sink without additional effort. However, only a single Cu layer is available on an IMS board to route the interconnections and place and/or solder the components, thus, only sub-optimal designs in terms of parasitic capacitances, commutation loop, and gate loop inductances can be realized, inevitably worsening the switching performance of the half-bridge formed by the DUT. To overcome this, a PCB is preferred to an IMS board in this setup, since by only introducing a thermal-pad, similar thermal performance is achieved.

To further investigate the linear dependency of E_{sw} with respect to I_{sw}, the same measurements are repeated after connecting C_{ext} = 100 pF in parallel

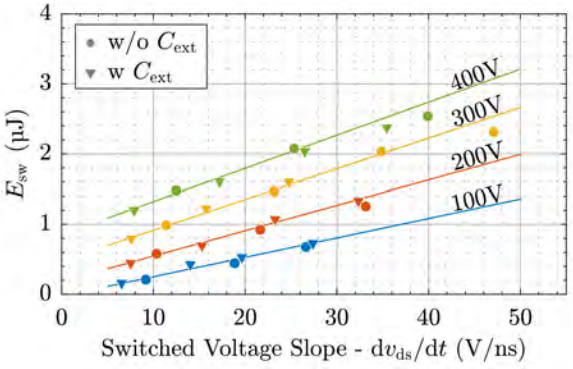


Fig. 4.8: E_{sw} as function of dv_{ds}/dt obtained with different I_{sw} (5 A... 20 A) for different V_{dc} (100 V... 400 V). E_{sw} without (dots) and with (triangles) C_{ext} follow the same interpolation lines (solid).

to each DUT (see **Fig. 4.2**). The resulting E_{sw} are also indicated in **Fig. 4.7** (triangles), accompanied by linear interpolating curves (dashed).
For the same V_{dc} and I_{sw}, E_{sw} in case of C_{ext} = 100 pF (triangles) is consistently lower than E_{sw} measured without C_{ext} (dots). Since the presence of C_{ext} reduces the fraction of I_{sw} flowing through C_{oss}, i.e. reduces the switched voltage slope dv_{ds}/dt for the same I_{sw}, it is interesting to compare the results as function of dv_{ds}/dt as in **Fig. 4.8**. dv_{ds}/dt defining the x-axis is calculated measuring the time taken from v_{ds} to rise (or fall) from $0.1\,V_{dc}$ to $0.9\,V_{dc}$ (or vice versa). Depending on the presence of C_{ext}, different dv_{ds}/dt values are measured for the same I_{sw}, however, all the measured points (dots and triangles) surprisingly align, for each V_{dc}, along the same linear interpolating curve (solid) for the whole considered dv_{ds}/dt-range, i.e. from 6 V/ns to 47 V/ns. It can be concluded that E_{sw} is not only proportional to I_{sw}, but, more precisely, to the current flowing in C_{oss} (or to dv_{ds}/dt [69]), exactly as if its charging/discharging process would be lossy.

4.4 Measurements of Permanently Turned Off Devices

To confirm the evidence of a lossy C_{oss} charging/discharging process resulting from **Section 4.3**, the setup described in **Section 4.2.1** is now modified introducing a second half-bridge T_3-T_4 connected in parallel to the switching

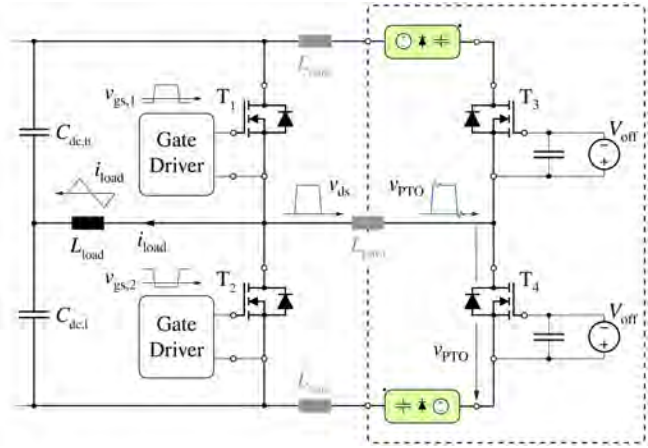


Fig. 4.9: Schematic of the realized measurement setup consisting of the half-bridge formed by the PTO DUT T_3 and T_4 (dashed box) connected in parallel to the switching half-bridge T_1-T_2. T_1 and T_2 generate high dv/dt square-wave voltage waveforms across the drain and source terminals of T_3 and T_4.

half-bridge T_1-T_2, as shown in **Fig. 4.9** (dashed box). T_3 and T_4 (i.e. the DUT) are permanently turned off (PTO) applying a negative DC-voltage V_{off} between their gate and source terminals, while the switching half-bridge is operated as described in **Section 4.2.1**. Hence, high dv/dt square-wave voltage waveforms are generated across the drain and source terminals of the PTO DUT, isolating the loss mechanism associated with C_{oss} from all the other sources of loss contributing to P_{ext} (see **Section 4.2.2**). This measurement setup for the PTO DUT, featuring voltage waveforms representative for real operating conditions (see **Section 4.2.1**), is preferred over others where sinusoidal voltage excitations are considered (see **Section 4.1**).

4.4.1 Description of the Measurement Method

In order to calorimetrically measure the occurring losses in the PTO DUT $P_{tot,PTO}$, the half-bridge formed by the PTO DUT is mounted on a separate heat sink constituting a second thermal system, as shown in **Fig. 4.10**. This heat sink is optimized for the new range of lower losses since no conduction losses occur in the PTO DUT, i.e. $P_{cond,PTO} = 0\,W$, and the whole thermal system is calibrated accordingly.
To maximize the measurement accuracy, the influence of P_{tot} on $P_{tot,PTO}$, i.e.

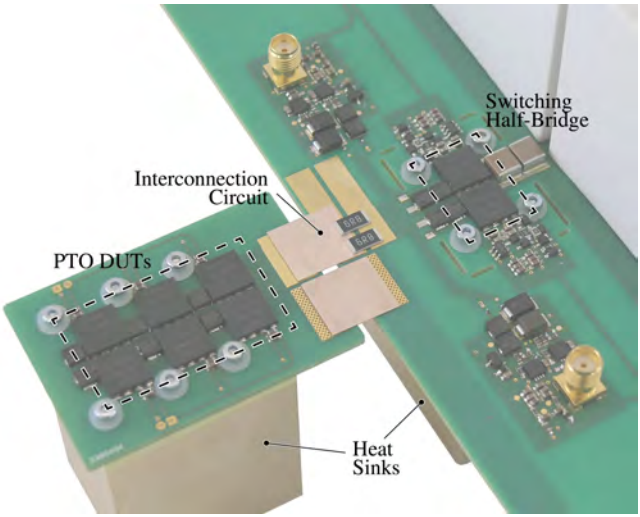


Fig. 4.10: Picture of the realized measurement setup for the PTO DUT. On the right-hand side PCB, the switching half-bridge is highlighted. On the left-hand side PCB, the half-bridge formed by the PTO DUT, separated by the interconnection circuit from the switching half-bridge, is visible (see **Fig. 4.11**).

the thermal coupling between the two half-bridges, should be minimized. For this reason, the possibility of attaching the half-bridge formed by the PTO DUT on the same heat sink of the switching half-bridge is discarded. Nevertheless, an electric connection between the half-bridges is necessary for the correct operation of the setup, i.e. their thermal coupling can, in reality, only be minimized. Long and narrow interconnections between the half-bridges would surely limit their thermal coupling, but as well introduce significant parasitic inductances L_{para}. The resonant network formed by L_{para}, in combination with C_{oss} of the PTO DUT (characteristic impedance $Z_{\text{rn}} \propto \sqrt{L_{\text{para}}/C_{\text{oss}}}$), is excited by v_{ds}. Hence, the voltage measured across T_4, labeled v_{PTO}, does not coincide with v_{ds} as desired, but is partially distorted by a super-imposed voltage oscillation, as visible in **Fig. 4.9**. Since C_{oss} is fixed from the PTO DUT, L_{para} defines a trade-off between distortion of v_{ds} and thermal coupling, and a satisfactory compromise must be achieved.
Several solutions tested to overcome the above mentioned issue, essentially consisting of different circuits suitable for the interconnection of the two half-bridges, are proposed in **Fig. 4.11**. If no precaution would be taken (i.e.

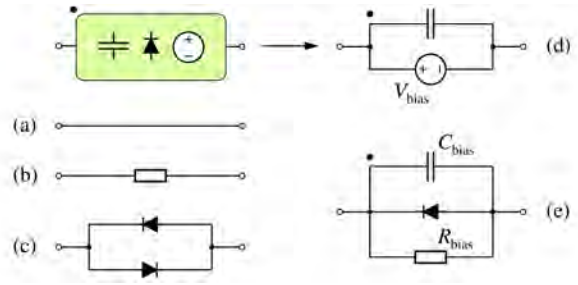


Fig. 4.11: Different solutions to interconnect the half-bridges (see **Fig. 4.9**); (d) is preferred since by properly adjusting V_{bias}, the reverse conduction of both PTO DUT is prevented.

solution (a) would be adopted) the voltage oscillation present on v_{PTO} would be clamped by the PTO DUT in reverse conduction, not only violating the assumption of PTO, but also introducing additional losses which would need to be estimated and subtracted. If a resistor (b) of sufficient value, e.g. $2\,Z_{rn}$, or diodes (c) would be connected as shown in **Fig. 4.10**, the effects of the voltage oscillation could be significantly reduced, but new sources of loss would be again introduced. An alternative solution, similar to (c), is therefore proposed herein.

Properly adjusting the voltage V_{bias} of the voltage source (d), each PTO DUT can be biased as highlighted in **Fig. 4.12** and summarized in **Tab. 4.3** for the case of T_2 and T_4. If V_{bias} is selected at least equal to the amplitude of the voltage ringing characterizing v_{PTO} after a turn-on transition of T_2 (dashed), $v_{PTO} \geq 0\,V$, i.e. the reverse conduction of T_4 is prevented. Moreover, since no passive element is present in the circuit, (d) is ideally loss-less. Although (d) is effective, two potentially negative aspects associated with its implementation have to be mentioned:

- During a turn-off transition of T_2, while v_{ds} changes from 0 V to V_{dc}, v_{PTO} changes from V_{bias} to $V_{dc} + V_{bias}$, i.e. v_{PTO} is unnecessarily shifted by V_{bias} also during a turn-off transition of T_2. This can be solved replacing V_{bias} with an accordingly modulated switched voltage source v_{bias} ($v_{bias} = 0\,V$ before T_2 turns off and $v_{bias} = V_{bias}$ before T_2 turns on) or with the passive network (e). In (e), C_{bias} is adjusted to build up the desired V_{bias} through the capacitive current caused by a turn-on transition of T_2, and R_{bias} to discharge C_{bias} before the subsequent turn-off transition.

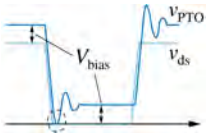


Fig. 4.12: Simplified v_{ds} and v_{PTO} waveforms highlighting the effect of V_{bias} (see **Fig. 4.11(d)**).

Tab. 4.3: Nominal v_{ds} and v_{PTO} (see **Fig. 4.12**).

T_2 state	on	off
v_{ds} (V)	0	V_{dc}
v_{PTO} (V)	V_{bias}	$V_{dc} + V_{bias}$

- Since (d) itself does neither limit nor attenuate the voltage oscillation present on v_{PTO}, a combination of (d) with (b) or (c) can be additionally considered (cf. **Fig. 4.11(e)**).

4.4.2 Discussion on the Measurement Results

$P_{tot,PTO}$ is measured with the described setup featuring (d) and for the same operating points considered in **Section 4.3**. Afterwards, E_{PTO} is calculated from $P_{tot,PTO}$ and the obtained results are provided in **Fig. 4.13** (squares) as function of dv_{PTO}/dt. Only two measurement points are recorded for $V_{dc} = 100\,V$, since, for higher dv_{PTO}/dt, the required V_{bias} (proportional to dv_{PTO}/dt exciting the resonant circuit) becomes an excessive fraction of V_{dc}. Additionally, linear interpolating curves (dashed) are reported. The range of dv_{PTO}/dt (x-axis) roughly corresponds to the one of dv_{ds}/dt in the measurements performed with $C_{ext} = 100\,pF$, since each PTO DUT has the same impact as C_{ext} on the transistors forming the switching half-bridge (and $C_{ext} \approx C_{oss}$). In fact, in order to avoid an excessive reduction of dv_{PTO}/dt, only a single PTO DUT per side forms the half-bridge T_3-T_4, as visible in the thermal image snippet of **Fig. 4.13**. More than one PTO DUT connected in parallel would increase the sensitivity of the measurements, but also further reduce the occurring dv_{PTO}/dt, unless I_{sw} is not increased. The result of the linear interpolation of E_{sw} for $V_{dc} = 400\,V$ (see **Section 4.3**) is additionally reported in **Fig. 4.13** (solid) as function of dv_{ds}/dt to compare the two experiments.
Although E_{PTO} is lower than E_{sw} in the same operating conditions (this is

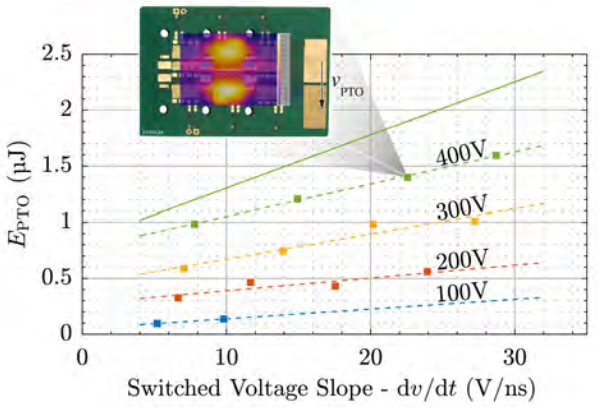


Fig. 4.13: E_{PTO} as function of $\mathrm{d}v_{PTO}/\mathrm{d}t$ obtained with different I_{sw} (5 A... 20 A) for different V_{dc} (100 V... 400 V). E_{PTO} (dashed) constitutes 70 % to 90 % of E_{sw} (solid) in the case of V_{dc} = 400 V.

consistent for all V_{dc}, cf. **Fig. 4.8**), a significant fraction of E_{sw}, generally from 50 % (from 70 % in the case of V_{dc} = 400 V) to 90 %, is still observed in the PTO DUT. It can be concluded that the C_{oss} charging/discharging process itself has a major impact on the losses occurring in soft-switching operation. These results are in good agreement with the findings presented in [69], where comparable E_{PTO} (especially if normalized with respect to C_{oss}) are measured for the same V_{dc} and $\mathrm{d}v_{PTO}/\mathrm{d}t$ on a similar PTO DUT.
The following causes can explain the discrepancy between E_{sw} and E_{PTO}:

- Additional loss mechanisms related to the conduction of i_{load} may occur in switching operation, whereas not being present in the PTO DUT.
- σ_{Pext} associated with the switching half-bridge, e.g. in the case of the V-I overlap losses, is limited. In fact, it relies on circuit simulations which potentially underestimate their impact, finally resulting in overestimating E_{sw} according to (4.2).
- As a consequence of the selected interconnection circuit (d), $v_{PTO} \approx v_{ds} + V_{bias}$ during a turn-off transition of T_2. Even if the amplitude of both v_{PTO} and v_{ds} square-wave shaped waveforms is V_{dc} (excluding the voltage oscillation), the non-linearity of C_{oss}, in combination with the voltage offset V_{bias}, might be to a large extent responsible for the loss mismatch. In fact, C_{oss} is significantly larger at low voltage, e.g.

$C_{oss}(0\,V) \approx 3\,C_{oss}(30\,V)$ [92], i.e. in the voltage range not covered by v_{PTO}. Thus, since the investigated loss mechanism involves the charging/discharging process of C_{oss}, it is legit to expect that the voltage range characterized by the highest amount of charge has the highest impact on E_{PTO}.
The previous assumption is confirmed with two experiments. First, repeating the measurements for different V_{bias} (higher than the limit defined by the voltage ringing), it results that E_{PTO} decreases inversely proportional to V_{bias} for the same V_{dc}. Second, considering the interconnection circuit (e), E_{PTO} approaches E_{sw}. However, (e) requires to adjust C_{bias} in each operating point, and the overall effort of the measurement procedure significantly increases. Employing (d), this issue is only partially mitigated in the turn-on transitions of T_2, adjusting V_{bias} such that v_{PTO} reaches 0 V (including the voltage oscillation). Nevertheless, (d) is still considered the best solution among the ones shown in **Fig. 4.11**.
At the expense of a modified dv_{PTO}/dt, a switching half-bridge generating a sinusoidal, rather than a square-wave, v_{ds} voltage waveform could as well alleviate the issue.

- The voltage oscillation visible in v_{PTO} is well damped after every switching transition from the resistance of the connections between the half-bridges (e.g. PCB Cu tracks and interconnection circuit), i.e. a second source of loss contributes to E_{PTO}. To compensate for this, the energy stored in the resonant network L_{para}-C_{oss} is estimated from C_{oss} and from the amplitude of the first peak of the voltage oscillation present on v_{PTO}, and subtracted from $P_{tot,PTO}$. This implicitly considers the worst-case assumption that all energy stored in L_{para}-C_{oss} is dissipated in the PTO thermal system, which ultimately leads to a slight reduction of E_{PTO}.

To better understand the origin of E_{PTO}, a simplified loss model can be derived. As anticipated in **Section 4.2.1**, each soft-switching transition can be described with an equivalent circuit formed by a current source I_{sw} charging/discharging the parallel connection of the C_{oss} from 0 V to V_{dc} in a time $\bar{t} = V_{dc}(dv/dt)^{-1}$. If a certain R_{oss} is assumed to justify the evidence of losses, the occurring E_{PTO} would result as

$$E_{PTO,R} \approx R_{oss}\left(\frac{I_{sw}}{2}\right)^2 \bar{t} = R_{oss}C_{oss,Q}V_{dc}\frac{I_{sw}}{2} \tag{4.3}$$

(neglecting any other capacitance present in the circuit). (4.3) is calculated computing the energy dissipated by a resistor R_{oss}, when a lossy capacitor

$C_{oss,Q}$ (calculated at V_{dc}) is charged from 0 V to V_{dc} by a current source $I_{sw}/2$. This model can explain the linear trend of E_{PTO} with respect to I_{sw} (or dv_{PTO}/dt), and the increasing slope of the interpolating curves with increasing V_{dc}. It must be noticed that $C_{oss,Q}$ decreases non-linearly with increasing V_{dc} as described in **Tab. 4.1**, thus partially compensating the increase of the slopes. Additionally, with a properly adjusted value of R_{oss}, this model can as well reproduce the hysteresis curves of C_{oss} measured in [69]. On the other hand, unfortunately, this model is too simplistic to give any insight on the non-zero intercepts of the interpolating curves (dashed), which can be visualized extrapolating them towards $dv_{PTO}/dt = 0\,V/ns$. It is obvious that E_{PTO} should be 0 J at this point, but this is not of practical interest, since outside the range of typical dv/dt of soft-switching converters.
Moreover, it is interesting to notice that, if E_{PTO} is normalized with respect to the energy stored in C_{oss} (i.e. $C_{oss,E}V_{dc}^2/2$), the dependency of E_{PTO} on V_{dc} practically disappears.
Nevertheless, the proof of a lossy C_{oss} charging/discharging process is once more confirmed, and an in depth analysis of the DUT structure is conducted in the next section to investigate the physical reasons, possibly explaining the highlighted phenomena.

4.5 Hypotheses on the Origin of the C_{oss}-Losses

Each terminal of the DUT excited by a high dv/dt voltage waveform during every switching transition, namely source, drain and substrate, must be analyzed separately to identify potential loss mechanisms in the device structure, causing the observed C_{oss}-losses.
An equivalent circuit of the DUT, including the parasitic capacitors connecting the three mentioned terminals, is shown in **Fig. 4.14(a)**. Additionally, comparing the equivalent circuit with the cross-section of the internal structure of the DUT illustrated in **Fig. 4.14(b)**, the main structural components determining these capacitors can be visualized. The drain-source capacitor $C_{d\text{-}s}$ is mainly defined by the inter-metal capacitances between source and drain metals, including the field plate and the 2DEG. $C_{d\text{-}s}$ also includes the drain-gate capacitor $C_{g\text{-}d}$, considered in parallel to $C_{d\text{-}s}$ in a first approximation. These elements are typically considered loss-less, as long as the inter-level dielectrics can be assumed nearly ideal. Also the drain p-GaN region, under the assumption of PTO, is considered loss-less, since there is no potential drop applied across it that could cause the injection of holes. Differently, in

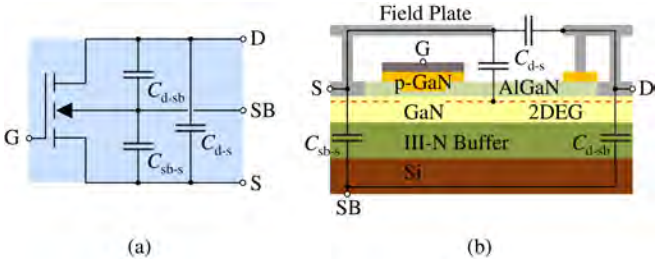


Fig. 4.14: (a) Equivalent circuit and **(b)** cross-section of the DUT illustrating the main structural components determining the parasitic capacitors $C_{\text{d-s}}$, $C_{\text{sb-s}}$ and $C_{\text{d-sb}}$.

the two capacitors from the drain and source metals to the conductive Si substrate, denominated $C_{\text{sb-s}}$ and $C_{\text{d-sb}}$ respectively, the relevant dielectric is the III-N buffer, which could in principle show intrinsic loss mechanisms in contrast to traditional dielectrics, as discussed in the following.

The basic role of the epitaxial layers forming the III-N buffer, is to provide electric insulation between the substrate (on the bottom-side) and the lateral GaN channel (on the top-side), when a non-zero v_{ds} is applied to the DUT. Therefore, the III-N buffer should ideally form a capacitor with no vertical leakage current I_{leak}. In reality, I_{leak} increases with v_{ds} but is limited well below 1 nA/mm^2 for typical static conditions below 125 °C and with $v_{\text{ds}} < 480$ V. Consequently, given a die area in the range of a few mm^2, the contribution of I_{leak} to the overall losses in static conditions can be neglected. Nevertheless, losses occurring in dynamic conditions could be more significant, depending on the technology selected to create the III-N buffer.

The complete structure of typical III-N buffers consists of several layers. At the bottom, an Aluminum-Nitride (AlN) buffer layer is typically used to nucleate on the Si substrate. On top of this, several layers are required to compensate for the thermal expansion mismatch between Si and the remaining III-N buffer (between the growth temperature of around 1000 °C and room temperature), thus providing a base of sufficiently good quality for the GaN channel [96]. Since the layers typically used are not intrinsically insulating, deep traps are introduced through foreign dopants during the growth of the III-N buffer.

The most commonly used dopant is C, which is already available from the metal-organic precursor used to grow the III-N layers and, moreover, is fully compatible with the contamination requirements of the standard fabrication process of Si CMOS. Even though it is empirically shown that layers with increased concentrations of C exhibit significantly lower I_{leak}, the responsible

mechanism is still under discussion. Additionally, the nature of C-doped GaN (GaN:C) layers is best described by a lossy (rather than a leakage suppressing) dielectric, i.e. I_{leak} is not completely eliminated [97–100]. However, this feature seems to offer an advantage in terms of dynamic conduction performance, by allowing a fast discharge of the GaN channel and of the III-N buffer from trapped and/or stored charges, hence alleviating dynamic $R_{ds,on}$ phenomena [97,98]. Recently, it has been suggested that C atoms might also segregate to the structural defects, e.g. threading dislocations or low angular grain boundaries, which are an inevitable part of III-N buffers grown on Si. The distance between these atoms could become sufficiently small to enable direct defect-to-defect interactions. The results of several electric measurements [99–101] suggest the existence of such a defect band-related transport mechanism.

Interestingly, when comparing a single GaN:C-layer, revealing the isolated leakage behavior of the defect band, with actual multi-layer III-N buffers, the same exponential dependency of I_{leak} with respect to temperature can be recognized, as illustrated in **Fig. 4.15(a)**, where the measured leakage current densities J_{leak}, obtained dividing I_{leak} by the dies area, are plotted as function of temperature for both cases. This result suggests that the same physical transport mechanism might not only act in single GaN:C-layers, but that it could also play a significant role in the real full multi-layer III-N buffer.

Moreover, comparing J_{leak} in these two cases as function of the applied electric fields as in **Fig. 4.15(b)**, an exponential field dependency on different pre-factors and offsets is visible. The presence of an offset clearly indicates that the defect band transport induced by C doping is actually not the sole mechanism causing the insulating behavior of the multi-layer III-N buffer. The offset can be best described as an additional potential drop, whose origin is assumed to be related to the different combination of layers within the buffer, comparable to a depletion region characteristic of p-n junctions. Moreover, it is verified that in reverse bias condition, a simple GaN:C/GaN:Si-layer can guarantee a voltage blocking behavior with very low I_{leak} [100].

It can be concluded that a single GaN:C-layer is not sufficient to provide the desired insulating behavior, but an optimized sequence of different layers forming the full III-N buffer is required. As a consequence, the resistive behavior of the C-related defect band, visible in **Fig. 4.15(b)**, could be responsible for a significant fraction of the losses measured in **Section 4.4**, in particular during the formation of the buffer depletion region. This hypothesis could be relevant in contrast to the trapping phenomena seen in C-doped buffers. Interestingly, both the presence of traps and of resistive layers within the buffer could cause a similar hysteresis of C_{oss}, hence explaining the losses.

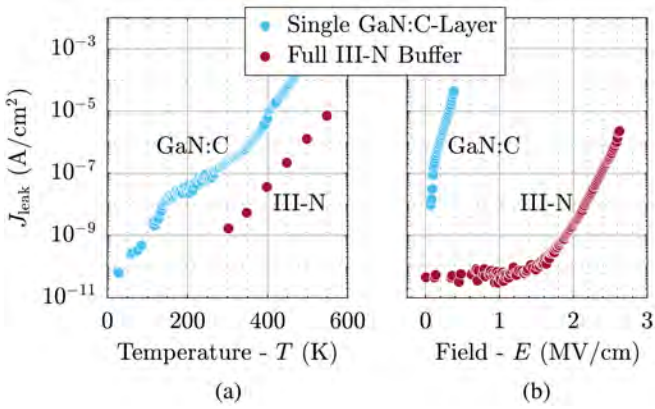


Fig. 4.15: Measured J_{leak} of a single GaN:C-layer compared to a complete multi-layer III-N buffer as function of **(a)** temperature and **(b)** vertical electric field.

4.6 Measurements of Device-Under-Test with Separate Substrate

The evidence of a lossy C_{oss} charging/discharging process, provided by the experimental results described in **Section 4.4**, is supported by the above discussed analysis of the internal structure of the DUT. Nevertheless, it is still unknown which of the three capacitors shown in **Fig. 4.14** contributes most to the observed losses. In the commercial version of the DUT, the substrate is electrically connected to the source inside the package, i.e. $C_{sb\text{-}s}$ is shorted and therefore cannot contribute to E_{PTO}. Hence, the main suspects are $C_{d\text{-}s}$, associated with the lateral structure of the DUT and to the field plate, and $C_{d\text{-}sb}$, distributed along the vertical stack.

To separate these two potential causes of E_{PTO}, two DUT, denominated separate substrate (SS) DUT, are packaged without the internal connection between substrate and source, and installed in the half-bridge T_3-T_4 replacing the PTO DUT. The PCB is modified inserting eight solder bridges (jumpers) allowing to connect the source and substrate terminals of both SS DUT to either the source or the drain terminals of the transistors forming the switching half-bridge. As an example, the four jumpers connected to the low-side SS DUT, i.e. T_4, are illustrated in **Fig. 4.16**, where the drain and source terminals of the low-side transistor of the switching half-bridge, i.e. T_2, are labeled AC and GND respectively. Ideally, each jumper can be either open (o) or

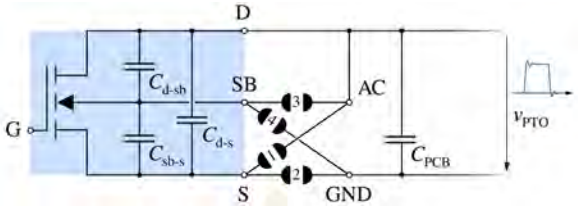


Fig. 4.16: Equivalent circuit of the DUT and schematic representation of the jumpers allowing to connect the source and substrate terminals of the low-side SS DUT to either AC or GND.

Tab. 4.4: Possible configurations of the jumpers of **Fig. 4.16** with associated binary coded states and expressions of $Q_{tot,i}$ as function of Q_j.

	Connection					
J	**1**	**2**	**3**	**4**	**Note**	$Q_{tot,i}$
	0	1	0	1	*d-s,sb*	$Q_{d\text{-}s} + Q_{d\text{-}sb} + Q_{PCB}$
	0	1	0	0	*d-s*	$Q_{d\text{-}s} + Q_{d\text{-}sb\text{-}s} + Q_{PCB}$
	0	0	0	1	*d-sb*	$Q_{d\text{-}sb} + Q_{d\text{-}s\text{-}sb} + Q_{PCB}$
	0	1	1	0	*d,sb-s*	$Q_{d\text{-}s} + Q_{sb\text{-}s} + Q_{PCB}$
	1	0	0	1	*d,s-sb*	$Q_{d\text{-}sb} + Q_{sb\text{-}s} + Q_{PCB}$
	1	0	1	0		
	0	0	0	0	*d,s,sb*	Q_{PCB}
	1	0	0	0		
	0	0	1	0		

closed (1), i.e. sixteen (2^4) symmetrical (between the low- and high-side of the half-bridge formed by the SS DUT) configurations of jumpers are possible. Several configurations connect AC to GND, causing the setup to be inoperable. Thus, only the remaining nine configurations are reported in **Tab. 4.4**, where the numbering defined in **Fig. 4.16** and the binary coded states of the jumpers are used to differentiate among them.
Each configuration of jumpers leads to a different equivalent capacitance between AC and GND, i.e. excited from the switching half-bridge, which applies v_{PTO} between AC and GND. In first approximation, the additional parasitic capacitance introduced by the open jumpers is not considered, since negligible compared to the contribution of the DUT. Hence, for example, in configuration 0101 (first row of **Tab. 4.4**) both source and substrate termi-

nals of T_4 are connected to GND and v_{PTO} is applied across its drain and source (connected to substrate) terminals, defining the notation *d-s,sb*. In this case, the capacitors $C_{d\text{-}s}$, $C_{d\text{-}sb}$ and C_{PCB} (where the latter includes all the parasitic capacitors not directly related to T_4) are connected in parallel, hence the charge $Q_{tot,1} = Q_{d\text{-}s} + Q_{d\text{-}sb} + Q_{PCB}$ characterizes this experiment. Since both SS DUT are PTO, $C_{g\text{-}d}$ is again considered in parallel to $C_{d\text{-}s}$ (and not shown explicitly). Differently, configurations 0100 and 0001 (second and third row of **Tab. 4.4**) impose the series connections ($\oplus$) of capacitors, i.e. $C_{d\text{-}sb} \oplus C_{sb\text{-}s} = C_{d\text{-}sb\text{-}s}$ and $C_{d\text{-}s} \oplus C_{sb\text{-}s} = C_{d\text{-}s\text{-}sb}$. Since these capacitors are known and/or expected to be non-linear, the corresponding charge variables $Q_{d\text{-}sb\text{-}sb}$ and $Q_{d\text{-}s\text{-}sb}$ must be defined as well. All configurations of the type 0x0x are redundant since they cause the SS DUT to float, i.e. only C_{PCB} is excited by v_{PTO}.
The occurring losses $P_{SS,i}$ can be measured in six distinguishable (non-redundant) experiments for each operating point of interest ($V_{dc} = 400\,V$ and $I_{sw} = 20\,A$ are selected), setting the appropriate configuration of jumpers i. Finally, the contribution of each capacitor to $P_{SS,i}$ can be determined.
First of all, each $Q_{tot,i}$ in $\boldsymbol{Q_{tot}}$ can be calculated as

$$Q_{tot,i} = \frac{I_{sw}\, V_{dc}}{2\ {}^{dv_{PTO,i}}/_{dt}} \tag{4.4}$$

for every experiment $i = 1, 2, \ldots 6$. $Q_{tot,i}$ is the result of the linear combination, represented by $\mathbf{A}$ and described in **Tab. 4.4**, of the six unknown charges Q_j forming $\boldsymbol{Q}$, associated with the six identified capacitors, i.e.

$$\begin{bmatrix} Q_{tot,1} \\ Q_{tot,2} \\ \vdots \\ Q_{tot,6} \end{bmatrix} = \boldsymbol{Q_{tot}} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} Q_{d\text{-}s} \\ Q_{d\text{-}sb} \\ Q_{sb\text{-}s} \\ Q_{d\text{-}sb\text{-}s} \\ Q_{d\text{-}s\text{-}sb} \\ Q_{PCB} \end{bmatrix} = \mathbf{A}\,\boldsymbol{Q}. \tag{4.5}$$

To clarify, $A_{i,j} = 1$ indicates that the charge Q_j, and therefore the associated capacitor, is involved in the experiment i (vice versa is true when $A_{i,j} = 0$). $\boldsymbol{Q} = \mathbf{A}^{-1}\boldsymbol{Q_{tot}}$ can be calculated to find the unknown Q_j. The resulting measured value $Q_{d\text{-}s} + Q_{d\text{-}sb} = 37\,nC$ differs only 10 % from the corresponding value, i.e. Q_{oss} calculated at 400 V, reported in [92], confirming the accuracy of this measurement procedure.
Afterwards, for each experiment i, the average current $I_{i,j}$ determining the

flow of Q_j in the associated capacitor can be calculated according to

$$\begin{bmatrix} 1/t_1 \\ 1/t_2 \\ \vdots \\ 1/t_6 \end{bmatrix} \boldsymbol{Q}^{\intercal} \circ \mathbf{A} = \begin{bmatrix} I_{\text{d-s},1} & I_{\text{d-sb},1} & 0 & 0 & 0 & I_{\text{PCB},1} \\ I_{\text{d-s},2} & 0 & 0 & I_{\text{d-sb-s},2} & 0 & I_{\text{PCB},2} \\ 0 & I_{\text{d-sb},3} & 0 & 0 & I_{\text{d-s-sb},3} & I_{\text{PCB},3} \\ I_{\text{d-s},4} & 0 & I_{\text{sb-s},4} & 0 & 0 & I_{\text{PCB},4} \\ 0 & I_{\text{d-sb},5} & I_{\text{sb-s},5} & 0 & 0 & I_{\text{PCB},5} \\ 0 & 0 & 0 & 0 & 0 & I_{\text{PCB},6} \end{bmatrix} = \boldsymbol{I}. \quad (4.6)$$

t_i corresponds to the time considered to calculate $\mathrm{d}v_{\text{PTO,i}}/\mathrm{d}t$, while the notation $\circ\mathbf{A}$ indicates, instead, the element-wise multiplication for $\mathbf{A}$ necessary to zero the elements of $\boldsymbol{I}$ associated with capacitors not involved in the experiment. As a verification of the procedure, $2\sum_j I_{i,j} = I_{sw}$, where 2 is necessary to account for the presence of low- and high-side SS DUT.
From the considerations reported in **Section 4.4**, it can be assumed that E_{PTO} is proportional to the current charging/discharging the lossy capacitor (neglecting the offset at $\mathrm{d}v/\mathrm{d}t = 0\,\mathrm{V/ns}$). Therefore, proportionality factors λ_j are introduced herein to describe the relationship between $I_{i,j}$ and the measured losses $P_{SS,i}$. In particular, each λ_j belonging to $\boldsymbol{\lambda}$ can be calculated as

$$\begin{bmatrix} \lambda_{\text{d-s}} \\ \lambda_{\text{d-sb}} \\ \lambda_{\text{sb-s}} \\ \lambda_{\text{d-sb-s}} \\ \lambda_{\text{d-s-sb}} \\ \lambda_{\text{PCB}} \end{bmatrix} = \boldsymbol{\lambda} = \boldsymbol{I}^{-1} \begin{bmatrix} P_{\text{SS},1} \\ P_{\text{SS},2} \\ \vdots \\ P_{\text{SS},6} \end{bmatrix} = \boldsymbol{I}^{-1} \boldsymbol{P}_{\mathbf{SS}}. \quad (4.7)$$

In the commercial version of the DUT, $C_{\text{sb-s}}$ is shorted, i.e. only $\lambda_{\text{d-sb}}$ and $\lambda_{\text{d-s}}$ are of practical interest.
Finally, since $\lambda_{\text{d-sb}} \approx 20\,\lambda_{\text{d-s}}$ results from (4.7), it can be concluded that $C_{\text{d-sb}}$, i.e. the multi-layer III-N buffer separating the Si substrate from the GaN channel, is responsible for up to 95 % of E_{PTO}. As discussed in **Section 4.5**, this is assumed to originate from the resistivity of the C-doped layers in the III-N buffer. Hence, different samples featuring different vertical internal structures are assessed in the next section, aiming to overcome the C_{oss}-losses.

4.7 Improvement of the III-N Buffer Structure

In **Section 4.6**, $C_{\text{d-sb}}$ is finally proven to be the major contributor to E_{PTO} measured in **Section 4.4** and therefore to E_{sw} measured in **Section 4.3**. Since,

as described in **Section 4.5**, $C_{\text{d-sb}}$ depends on the technology used to build the III-N buffer, a DUT featuring a different epitaxial stack is analyzed in this section. The modified epitaxial stack is denominated B to differentiate it from the original one, denominated A, considered in all the measurements discussed until this point. It is worth mentioning that the devices based on both epitaxial stacks, i.e. A and B, yield comparable performance both in terms of static lateral device and vertical buffer leakage currents, as well as concerning their dynamic behaviors, e.g. with respect to lifetime models and in terms of measured I_{leak} and dynamic $R_{\text{ds,on}}$. Additionally, the stacks are of similar thicknesses leading to the same contributions to C_{oss}.
To support the latter statements, $R_{\text{ds,on}}$ of two DUT featuring the two considered epitaxial stacks is measured under dynamic conditions and with different voltage stresses V_{s} up to 600 V (applied across the drain and source terminals of the DUT in off-state). The results are normalized with respect to $R_{\text{ds,on}}$ measured in the same setup with $V_{\text{s}} = 0\,\text{V}$ (to exclude any other possible dependency, e.g. related to temperature) and compared in **Fig. 4.17**. Both DUT, i.e. epitaxial stacks A and B, exhibit a good uniformity of $R_{\text{ds,on}}$ with respect to V_{s}, are well comparable between each other, and do not feature any increase of $R_{\text{ds,on}}$ in dynamic conditions, similarly to what already has been reported in **Fig. 4.5**. To summarize, epitaxial stack B is demonstrated to be equally good as A in terms of dynamic $R_{\text{ds,on}}$ in these conditions.
The results of $E_{\text{PTO-B}}$, i.e. E_{PTO} of the PTO DUT featuring epitaxial stack B, and the associated linear interpolating curve are reported in **Fig. 4.18** (stars and dashed line respectively) as function of $\mathrm{d}v_{\text{PTO}}/\mathrm{d}t$ for the case of $V_{\text{dc}} = 400\,\text{V}$. For comparison, also the previously measured $E_{\text{PTO-A}}$ (squares and dashed line) and $E_{\text{sw-A}}$ (solid line) with (dots) and without (triangles) $C_{\text{ext}} = 100\,\text{pF}$ are shown always for the case of $V_{\text{dc}} = 400\,\text{V}$ as function of the respective $\mathrm{d}v/\mathrm{d}t$. The modified epitaxial stack enables a reduction of E_{PTO} which amounts up to 73 %, definitely motivating the presented study.
Interestingly, epitaxial stack B shows the same C-level as A according to measurements based on secondary ion mass spectrometry (SIMS). However, it is believed that the defect band, discussed in **Section 4.5** as hypothesis for the origin of the C_{oss}-losses, might depend more on the local C-density within certain structural defects, rather than on the absolute C-level.
The remaining losses visible in **Fig. 4.18** (stars) may still arise from small residual losses in the vertical internal structure of the DUT featuring the modified epitaxial stack. However, it is also possible that the minimum absolute $E_{\text{PTO-B}}$ reaches the measurement noise floor of the considered calorimetric measurement setup and/or causes external factors, e.g. the losses occurring in the switching half-bridge, to compromise the measurement accuracy.

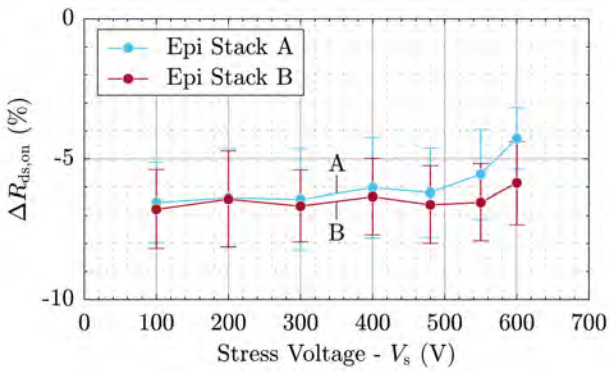


Fig. 4.17: $R_{ds,on}$ of the two DUT featuring epitaxial stacks A and B measured in dynamic conditions as function of V_s and normalized with respect to $R_{ds,on}$ measured with $V_s = 0\,V$. The vertical error bars indicate the standard deviation of $R_{ds,on}$ calculated within sixteen measurements across the whole wafer per each V_s. The measured $R_{ds,on}$ in case $V_s > 0\,V$ (dynamic) is even smaller compared to the case of $V_s = 0\,V$ (static), since a small residual amount of positive charges is present in the channel of the DUT after turn-on.

To compensate for the possible influence of external sources of loss and therefore validate the findings, a second calorimetric measurement approach, relying on the measurement of the case temperature T_c of the PTO DUT with a high definition thermal imaging camera [84], is presented in the following. **Fig. 4.18** shows, as an example, two infrared images of the two analyzed PTO DUT featuring different epitaxial stacks, and captured after approximately 10 s of their operation in identical conditions ($V_{dc} = 400\,V$ and $dv_{ds}/dt \approx 30\,V/ns$). They highlight how the PTO DUT based on epitaxial stack A (left) heats up significantly, i.e. $T_c \approx 10\,°C + T_{hs}$ because of the occurring $E_{PTO\text{-}A}$ whereas, in contrast, the PTO DUT based on epitaxial stack B (right), heats up only $1\,°C + T_{hs}$, given the negligible $E_{PTO\text{-}B}$. The remaining $P_{tot,PTO\text{-}B}$, causing the recorded minor rise of T_c in the second case, could be explained with the losses due to the voltage oscillation present on v_{PTO}. Since the parameters of the two thermal systems, i.e. of the two considered PTO DUT, are measured to be very similar (given that the two setups are physically identical), the temperature rise $T_c - T_{hs}$ is a good indicator to compare the occurring $P_{tot,PTO}$. Consequently, the improvement brought by the modified epitaxial stack, visible in the plot of **Fig. 4.18**, can be at least confirmed with this second and practically independent measurement approach.

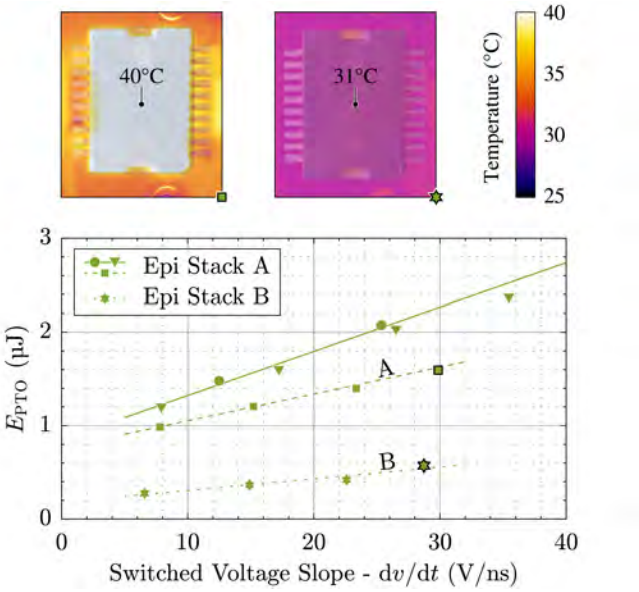


Fig. 4.18: E_{PTO} as function of $\mathrm{d}v_{PTO}/\mathrm{d}t$ obtained with different I_{sw} (5 A... 20 A) for V_{dc} = 400 V. $E_{PTO\text{-}B}$ (dotted) is more than 70 % lower than $E_{PTO\text{-}A}$ (dashed). Additionally, thermal images of the two analyzed PTO DUT featuring different epitaxial stacks: B (right) experiences only one tenth of the temperature increase of A (left).

The presented improvement, derived from the modified epitaxial stack, supports the hypothesis considering the vertical GaN-on-Si structure between the drain contact and the grounded Si substrate as main responsible for the soft-switching losses of III-N power devices. This not only justifies the conducted study, but also increases the interest towards the already existing challenge of providing highly insulating buffer layers with minimal transient response.

4.8 Conclusion

GaN-on-Si HEMTs are nowadays the best-in-class power semiconductors [95], but losses associated with their output capacitance C_{oss} severely limit their performance in soft-switching power converters [69].
In this research work, an accurate calorimetric measurement setup is devel-

oped to characterize the soft-switching losses of the IGT60R070D1 *CoolGaN* e-mode GaN power transistor from *Infineon*. Subsequently, the setup is adapted to isolate the C_{oss}-losses, which are demonstrated, by means of measurements, to constitute the main share of the observed soft-switching losses. Afterwards, the main technology components and the regions of the internal structure of the device forming C_{oss} are analyzed. With the support of experimental evidences, it is speculated that the resistive behavior of the C-related defect band present in the multi-layer III-N buffer, i.e. in the dielectric of the parasitic capacitance between the drain and the substrate of the device, could be the main responsible for the observed losses. Finally, based on this conclusion, a device featuring a modified GaN-on-Si stack is realized and measurements of C_{oss}-losses are repeated to quantify the expected improvement.
C_{oss}-losses appear to be almost entirely eliminated in the new device featuring the modified epitaxial stack. Moreover, it is verified that the enhanced device structure does not introduce any dynamic $R_{ds,on}$ phenomena. In other words, this study, not only deepened the understanding about the origin of the C_{oss}-losses, but finally resulted in the realization of a new GaN-on-Si HEMT which potentially does not exhibit any of the two loss mechanisms typically limiting the performance of GaN devices, i.e. dynamic $R_{ds,on}$ phenomena and C_{oss}-losses.

5

On the Dynamic On-State Resistance in GaN-on-Si HEMTs

This chapter summarizes the most relevant findings in the context of research on the dynamic on-state resistance in GaN-on-Si HEMTs, which are also published in:

- **M. Guacci**, D. Bortis, and J. W. Kolar, "On-State Voltage Measurement of Fast Switching Power Semiconductors," *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 2, pp. 163–176, 2018.
- G. Zulauf, **M. Guacci**, and J. W. Kolar, "Dynamic On-Resistance in GaN-on-Si HEMTs: Origins, Dependencies, and Future Characterization Frameworks," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5581–5588, 2020.

Motivation

The dynamic on-state resistance phenomenon, i.e. the increase of on-state resistance after a turn-on switching transition, translates into a substantial increase of conduction losses in power converters based on GaN power semiconductors. Similarly as for the losses occurring in the parasitic output capacitance, the described measurement setup allows to characterize this loss mechanism.

Executive Summary

The performance of GaN HEMTs is negatively affected by the dynamic on-state resistance $\mathrm{d}R_{\mathrm{on}}$ phenomenon, where the on-state resistance immediately after turn-on is higher than its DC value in the same operating conditions. A proliferation of recent literature reports inconsistent $\mathrm{d}R_{\mathrm{on}}$ measurements, with some publishing a significant increase in conduction losses, and others finding that the problem is non-existent. Hence, power electronics designers are left without accurate conduction loss estimations in converters featuring GaN HEMTs, since also no information on $\mathrm{d}R_{\mathrm{on}}$ is reported in the datasheet of these devices. Therefore, the causes underlying the $\mathrm{d}R_{\mathrm{on}}$ phenomenon are described in this chapter before analyzing the impact of the most significant circuit parameters, e.g. switching frequency and blocking voltage, on this undesired effect. Several measurements, performed on a previously calibrated on-state voltage measurement setup, confirm that each of these variables must be independently controlled, and that only steady-state $\mathrm{d}R_{\mathrm{on}}$ measurements are meaningful. Finally, the influence of the $\mathrm{d}R_{\mathrm{on}}$ phenomenon on the overall converter performance is quantified, analyzing the increase of conduction losses in two case studies.

5.1 Introduction

Compared to Si power semiconductors, GaN-on-Si HEMTs offer much lower specific on-state resistance values at a given blocking voltage, up to the maximum commercially available voltage rating of 1200 V [102]. This characteristic enables higher switching frequencies in modern power electronics converters, leading to simultaneous improvements of efficiency and power density [41]. However, GaN-on-Si HEMTs are known to exhibit the dynamic on-state resistance $\mathrm{d}R_{\mathrm{on}}$ phenomenon, where the on-state resistance $R_{\mathrm{ds,on}}$ immediately after turn-on is significantly higher than its DC value. This phenomenon can significantly affect the conduction losses of GaN-based power converters, since dynamic effects can dominate the effective $R_{\mathrm{ds,on}}$ for the entire conduction period. Its root cause can be identified in the trapping of electrons in undesired locations of the device structure. When this happens, the concentration of electrons in the 2D electron gas (2DEG) must be proportionally reduced to maintain overall charge neutrality, decreasing the drain-source current. Detrapping these electrons requires finite time with the switch in the on-state, during which $R_{\mathrm{ds,on}}$ values higher than expected are observed. Hence, it is critical, e.g. in order to properly dimension the heat sink of a power stage, or to select the optimum chip area for given converter specifications, to accurately characterize this phenomenon. Its importance

has lately resulted in a proliferation of literature [103]; however, a survey of these papers finds such widely varying values of $\mathrm{d}R_{\mathrm{on}}$ that designers cannot benefit from them to accurately determine the conduction losses of GaN-based power converters. Therefore, in this chapter, a standardized method for the characterization of the $\mathrm{d}R_{\mathrm{on}}$ phenomenon is introduced, and its impact on the converter performance is analyzed. In particular, the considered measurement setup is described in **Section 5.2**, and its accuracy is demonstrated by means of benchmark measurements. The $\mathrm{d}R_{\mathrm{on}}$ of a commercial HEMT is measured in **Section 5.3.1** to validate the impact of several circuit parameters on the magnitude of the effect. **Section 5.3.2** proposes a reporting framework for GaN HEMT manufacturers, and a methodology to translate the multi-dimensional $\mathrm{d}R_{\mathrm{on}}$ space into conduction losses. Finally, **Section 5.4** concludes the chapter.

5.2 Online Conduction Loss Measurements

An accurate and high bandwidth on-state voltage measurement circuit (OVMC), suitable to characterize the $R_{\mathrm{ds,on}}$ of fast switching power semiconductors is designed, calibrated and tested in [95]. The mentioned OVMC is considered in the next section for the characterization of the $\mathrm{d}R_{\mathrm{on}}$ phenomenon. In this section, $R_{\mathrm{ds,on}}$ of different power semiconductors, forming the low-side switch of a generic half-bridge, is measured as function of their operating conditions to prove the capabilities of the setup.
The nominal value of $R_{\mathrm{ds,on}}$ reported in the datasheet of specimen A in **Tab. 5.1** is compared in **Fig. 5.1** with the values of $R_{\mathrm{ds,on}}$ measured with the OVMC in a Double Pulse Test (DPT) setup in the same conditions as described in the datasheet. The black dashed line R_{data} is plotted as function of the junction temperature $T_{\mathrm{j,data}}$ (i.e. bottom x-axis) while the blue measurement points R_{DPT} are plotted as function of the measured case temperature $T_{\mathrm{c,DPT}}$ (i.e. top x-axis). Since the DPT has electric dynamics which are assumed to be faster than the thermal dynamics of the DUT, $T_{\mathrm{c,DPT}} \approx T_{\mathrm{j,DPT}}$ is considered and the two x-axis coincide (i.e. $T_{\mathrm{j,DPT}} \approx T_{\mathrm{j,data}}$). R_{DPT} measured with the OVMC match R_{data} with an approximation of ±3% (blue confidence bar is ±5%). The discrepancy can be attributed mainly to the device manufacturing variability. Additionally, no $\mathrm{d}R_{\mathrm{on}}$ phenomenon is observed on this SiC power semiconductor, as expected.
Fig. 5.2, instead, summarizes the values of $R_{\mathrm{ds,on}}$ measured in two different continuous operating conditions for all the specimens of **Tab. 5.1**. In particular, the orange points R_{TCM} are measured in Triangular Current Mode (TCM) operation [41] with blocking voltage $V_{\mathrm{DC}} = 400\,\mathrm{V}$, switched current

Tab. 5.1: Specifications of the power semiconductors considered as DUT for validating the performance of the OVMC.

Specimen	Power Semiconductor	$V_{ds,MAX}$	$I_{ds,MAX}$ @ 25 °C	$R_{ds,on}$ @ 25 °C
A	SiC power MOSFET	1200 V	98 A	25 mΩ
B	Si SJ MOSFET	700 V	46 A	40 mΩ
C	e-mode GaN HEMT	650 V	30 A	50 mΩ

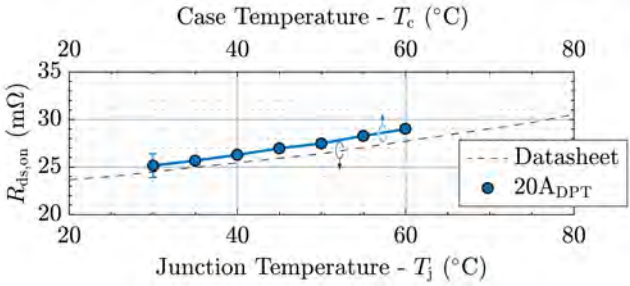


Fig. 5.1: Average value of $R_{ds,on}$ (R_{DPT}) measured with the proposed OVMC in a DPT setup for specimen A in **Tab. 5.1**, compared with the nominal $R_{ds,on}$ values reported in its datasheet R_{data}. The measured points match the nominal values within ±3%.

$I_{sw} = 20\,A$, and switching frequency $f_{sw} = 30\,kHz$, while the blue points R_{dc} are measured in DC operation. The DC current $I_{DC} = I_{pk}/(\sqrt{3}\sqrt{2}) = 8\,A$ is selected to ensure that approximately the same losses occur in the DUT in DC operation as in TCM operation (legitimately neglecting the soft-switching losses [53]), such that $T_{j,DC} \approx T_{j,TCM}$ when $T_{c,DC} = T_{c,TCM}$ is measured. All the circuit parameters are maintained the same in both experiments, in particular matching the values recommended in the datasheet. For specimen A (see **Fig. 5.2(a)**), R_{TCM} and R_{dc} are slightly higher than R_{data} and R_{DPT} (see **Fig. 5.1**). The reason behind it is the difference in T_j between the two sets of measurements ($T_{j,DC} \approx T_{j,TCM} > T_{j,data} \approx T_{j,DPT}$) due to the losses continuously occurring in the DUT. As a consequence, the positive temperature coefficient of $R_{ds,on}$ affects the result. More interesting to notice is that R_{dc} is very close, i.e. within ±4% (orange confidence bar is ±5%), to R_{TCM} as expected, since $T_{j,DC} \approx T_{j,TCM}$ and the current dependency of $R_{ds,on}$ is practically negligible in this range. The discrepancy can be attributed to the

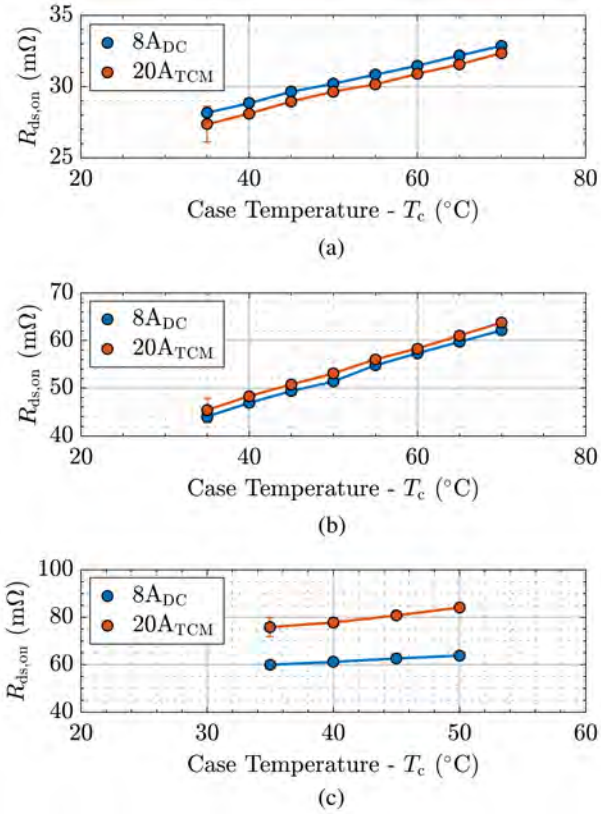


Fig. 5.2: Average value of $R_{ds,on}$ measured with the proposed OVMC for different operating conditions, for different DUT (see **Tab. 5.1**), and as a function of T_c. R_{TCM} (orange) and R_{dc} (blue) are similar (within ±5%) for **(a)** specimen A and **(b)** B when the power loss conditions are matched. **(c)** In the case of specimen C, a significant discrepancy (i.e. ≈ 50%) between the two sets of measurements is observed.

accuracy of the current measurement and of the OVMC, and to slightly different operating conditions. An equivalent set of measurements is performed on specimen B (see **Fig. 5.2(b)**) and identical conclusions can be drawn. Hence, the accuracy and the performance of the proposed OVMC are once more validated. **Fig. 5.2(c)** summarizes R_{TCM} and R_{dc} for specimen C. In this case, a significant discrepancy (i.e. ≈ 50%) between the two sets of measurements is observed. $T_{j,DC} \approx T_{j,TCM}$ is not a true assumption anymore, since more losses

are now unexpectedly occurring in the DUT in TCM operation. However, the discrepancy is attributed in this case to the DUT itself, i.e. to the $\mathrm{d}R_{\mathrm{on}}$ phenomenon [45].

5.3 Dynamic On-State Resistance Phenomenon

In this section, the analysis of the $\mathrm{d}R_{\mathrm{on}}$ of a GaN semiconductor (device parameters hidden for anonymity, with the device voltage rating indicated as BV_{ds}) is demonstrated with experimental results, considering the measurement setup validated in the previous section. The focus is on the identification of the circuit dependency of the $\mathrm{d}R_{\mathrm{on}}$ phenomenon, aiming to facilitate the design procedure of GaN-based converters.

5.3.1 Measurement Results

At first, $\mathrm{d}R_{\mathrm{on}}$, calculated as the average of $R_{\mathrm{ds,on}}$ during the on-time of the DUT, is measured in a DPT setup under hard-switching conditions with the on-time fixed to 50 µs, $I_{\mathrm{sw}} = 15\,\mathrm{A}$, and $T_{\mathrm{c}} = 35\,^{\circ}\mathrm{C}$. **Fig. 5.3(a)** reports the resulting

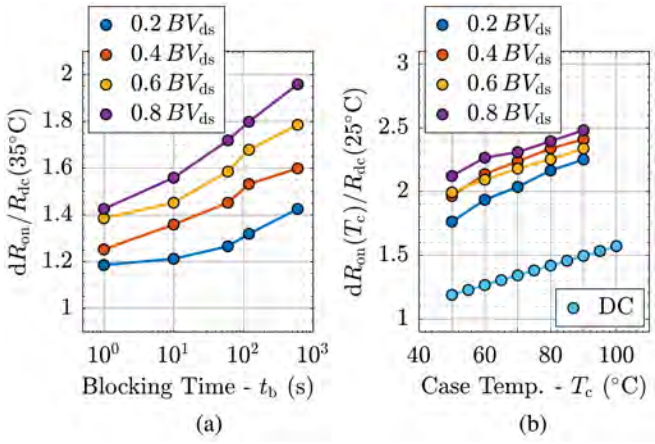


Fig. 5.3: Misleading $\mathrm{d}R_{\mathrm{on}}$ measurements and normalization. **(a)** $\mathrm{d}R_{\mathrm{on}}$ calculated for an on-time of 50 µs in a DPT setup after hard turn-on switching transition of the DUT with $I_{\mathrm{sw}} = 15\,\mathrm{A}$. **(b)** $\mathrm{d}R_{\mathrm{on}}$ calculated in steady-state hard-switching conditions with $I_{\mathrm{sw}} = 15\,\mathrm{A}$ and $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$, but normalized to $R_{\mathrm{dc}}(25\,^{\circ}\mathrm{C})$. The legend indicates V_{DC} normalized to BV_{ds}.

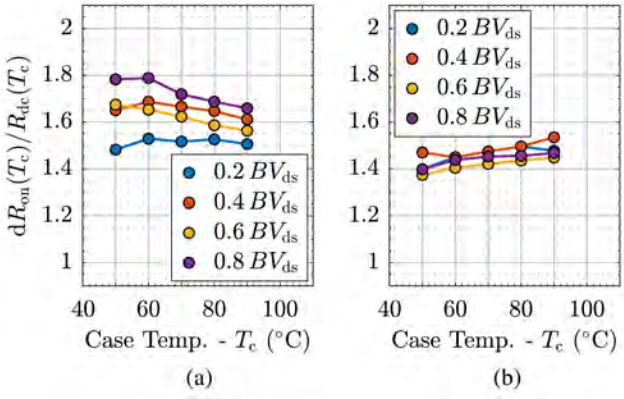


Fig. 5.4: $\mathrm{d}R_{\mathrm{on}}$ measurements, normalized to $R_{\mathrm{dc}}(T_{\mathrm{c}})$, in steady-state. **(a)** Hard-switching with $I_{\mathrm{sw}} = 15\,\mathrm{A}$ and $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$. **(b)** Soft-switching with $I_{\mathrm{sw}} = -15\,\mathrm{A}$ and $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$.

$\mathrm{d}R_{\mathrm{on}}$, where the monotonic increase with respect to blocking voltage V_{b} and blocking time t_{b} is observed. While this approach for the characterization of the $\mathrm{d}R_{\mathrm{on}}$ phenomenon is common, these results are invalid, as arbitrary blocking times heavily influence $\mathrm{d}R_{\mathrm{on}}$, and accumulated trapping is completely ignored. Overall, $\mathrm{d}R_{\mathrm{on}}$ measurements must be recorded under steady-state conditions. **Fig. 5.3(b)** shows the results obtained in steady-state conditions, but with $\mathrm{d}R_{\mathrm{on}}$ normalized to $R_{\mathrm{dc}}(25\,^{\circ}\mathrm{C})$, i.e. the value of $R_{\mathrm{ds,on}}$ observed in DC conditions at $T_{\mathrm{c}} = 25\,^{\circ}\mathrm{C}$, another common but misleading practice. This reporting method overstates the dynamic degradation, as $\mathrm{d}R_{\mathrm{on}}$ and the natural positive temperature coefficient of the DUT are lumped together in the overall increase. Hence, $\mathrm{d}R_{\mathrm{on}}$ measurements should be normalized to $R_{\mathrm{dc}}(T_{\mathrm{c}})$, as in the remainder of the chapter.

Fig. 5.4(a) shows measured $\mathrm{d}R_{\mathrm{on}}$ under hard-switching conditions for different values of V_{b} and T_{c}, with $I_{\mathrm{sw}} = 15\,\mathrm{A}$ and $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$. These measurements highlight the importance of both controlling temperature and measuring $\mathrm{d}R_{\mathrm{on}}$ at realistic operating temperatures. For example, $\mathrm{d}R_{\mathrm{on}}$ increases monotonically with higher V_{b} near 50 °C, but at higher temperatures (e.g. 90 °C), $\mathrm{d}R_{\mathrm{on}}$ is nearly flat. These trends and magnitudes directly contradict the DPT measurements, again highlighting the importance of temperature-controlled, steady-state measurements. Identical test conditions are kept in **Fig. 5.4(b)**, but the DUT is operated in ZVS conditions to eliminate hot-electron trapping. Accordingly, different trends of $\mathrm{d}R_{\mathrm{on}}$ result: e.g. the magnitude of $\mathrm{d}R_{\mathrm{on}}$ in

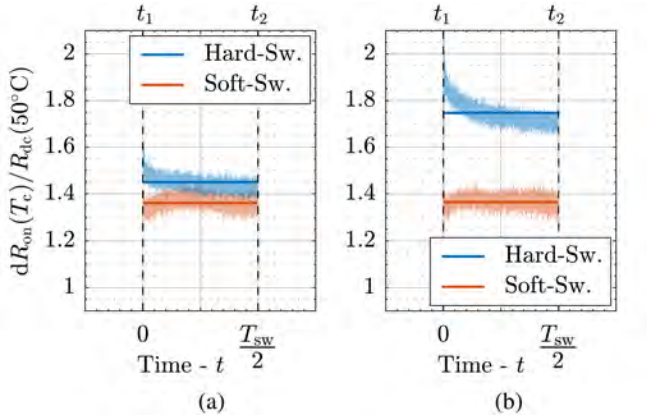


Fig. 5.5: $\mathrm{d}R_{\mathrm{on}}$ measurements, normalized to $R_{\mathrm{dc}}(50\,°\mathrm{C})$, in steady-state hard- and soft-switching conditions with $I_{\mathrm{sw}} = \pm 15\,\mathrm{A}$, $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$, and $T_{\mathrm{c}} = 50\,°\mathrm{C}$. **(a)** $V_{\mathrm{DC}} = 0.2\,BV_{\mathrm{ds}}$. **(b)** $V_{\mathrm{DC}} = 0.8\,BV_{\mathrm{ds}}$. The average values over the conduction period (shown as solid lines) match the reported values in **Fig. 5.4**.

soft-switching is lower than in hard-switching for the same I_{sw}. While there is one less trapping mechanism in soft-switching, the relative $\mathrm{d}R_{\mathrm{on}}$ magnitudes between soft- and hard-switching are impacted by specific device structures, and this relationship should not be broadly extrapolated.

By comparing $\mathrm{d}R_{\mathrm{on}}$ during the on-time between hard- and soft-switching, further insights on the detrapping mechanisms and time constants can be gained. **Fig. 5.5** plots measured $\mathrm{d}R_{\mathrm{on}}$ with $I_{\mathrm{sw}} = \pm 15\,\mathrm{A}$, $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$, and $T_{\mathrm{c}} = 50\,°\mathrm{C}$ for each operating mode. In hard-switching, there is significant detrapping (which manifests as steadily decreasing $\mathrm{d}R_{\mathrm{on}}$) during the 50 µs on-time, while in soft-switching, no measurable detrapping occurs over the same conduction period.

The measurements in **Fig. 5.6(a)** and **Fig. 5.6(b)** return to hard-switching, but vary f_{sw} and I_{sw} respectively to show the effects of each individual parameter. **Fig. 5.6(a)** highlights the expected trend of increasing $\mathrm{d}R_{\mathrm{on}}$ at higher f_{sw}, with an extra 20 % increase between 50 kHz and 200 kHz. An increase of $\mathrm{d}R_{\mathrm{on}}$ with f_{sw} is expected and observed in nearly all prior measurements, but this trend is not believed to continue monotonically. In fact, at higher frequencies, the on-time is decreased, which increases $\mathrm{d}R_{\mathrm{on}}$, but also decreases the blocking time, which is expected to reduce $\mathrm{d}R_{\mathrm{on}}$. **Fig. 5.6(b)** shows a weak increase of $\mathrm{d}R_{\mathrm{on}}$ with larger I_{sw}, following increased hot-electron trapping at higher

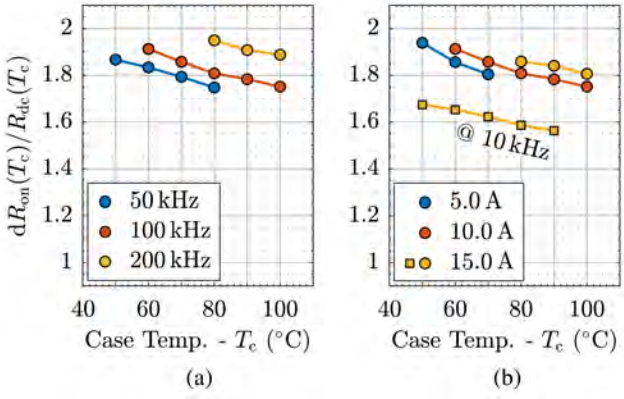


Fig. 5.6: dR_{on} measurements, normalized to $R_{dc}(T_c)$, in steady-state. **(a)** Hard-switching with $V_{DC} = 0.6\,BV_{ds}$ and $I_{sw} = 10\,A$. **(b)** Hard-switching with $V_{DC} = 0.6\,BV_{ds}$ and $f_{sw} = 100\,kHz$. Excluded temperatures for particular sweeps were not achievable with the cooling capability of the test setup.

hard-switched currents. For this particular device and operating condition, frequency is much more influential than current (cf. 10 kHz comparison in **Fig. 5.6(b)**).
To summarize, these plots demonstrate that dR_{on} is influenced by each parameter, and therefore only one can be varied at a time to understand trends. This multi-dimensional space complicates both the reporting and the translation of dR_{on} measurements to in situ conduction losses. Therefore, the following section proposes solutions to address both these aspects.

5.3.2 Practical Design Procedure

With the multi-dimensional parameter set that influences dR_{on}, care must be taken to translate measurements into conduction losses in realistic operating conditions. In this section, a reporting framework for GaN device manufacturers, and a method to include dR_{on} in the converter design process are proposed.
Fig. 5.7 shows a measurement set and a proposed mapping for GaN HEMT manufacturers to report dR_{on} in datasheets, with a four-point measurement set across duty-cycle d and I_{sw}, and the other operating parameters fixed at realistic values, e.g. $V_{DC} = 0.6\,BV_{ds}$, $f_{sw} = 100\,kHz$, and $T_c = 70\,°C$. A 2D linearization around the four measurement points to estimate dR_{on} in the

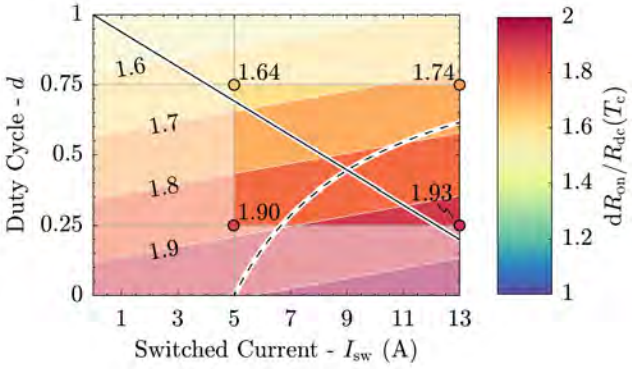


Fig. 5.7: $dR_{on}/R_{dc}(T_c)$ as a function of I_{sw} and d in hard-switching conditions with $V_{DC} = 0.6\,BV_{ds}$, $f_{sw} = 100$ kHz, and $T_c = 70$ °C. Four measured dR_{on} values are labeled, with a 2D linearization performed to interpolate and extrapolate to other values of I_{sw} and d. The solid line indicates the locus for a bridgeless totem-pole 2 kW PFC rectifier with 230 V RMS input voltage and 400 V output voltage, while the dashed line is the locus for a constant power 2 kW DC/DC buck converter with 400 V input voltage. The current ripple is neglected. For both loci, the duty-cycle refers to the low-side switch.

remainder of the operating region is then performed, achieving a worst-case relative error between measurement and fitting of 1.2 %.
With this map, designers can a priori estimate conduction losses in a wide variety of converters. For example, in a 2 kW totem-pole bridgeless PFC rectifier, whose d-I_{sw} operating region is highlighted by the solid line in **Fig. 5.7**, this method indicates an increase of conduction losses in the low-side switch of 86 % over the losses calculated with $R_{dc}(T_c)$. **Fig. 5.7** includes a similar locus (dashed line) for a constant power 2 kW DC/DC buck converter with 400 V input voltage and varying output voltage; the converter designer could appropriately weight dR_{on} by the percentage of time at each output voltage to estimate the effective dR_{on} in the considered application. Similar maps could be utilized to accurately or conservatively estimate dR_{on} in a range of converter topologies with GaN HEMTs.

5.4 Conclusion

Existing dynamic on-resistance dR_{on} measurements on GaN HEMTs give such a wide variance of test methods and results that conduction losses cannot

be accurately predicted. Hence, a simplified explanation of the key causes for the $\mathrm{d}R_{\mathrm{on}}$ phenomenon is provided in this chapter. These considerations support the development of a framework for future $\mathrm{d}R_{\mathrm{on}}$ characterization, reporting, and estimation. First, the measurement setup is described and $\mathrm{d}R_{\mathrm{on}}$ is measured in steady-state conditions with an accurate OVMC. Then it is proven that the standard DPT method does not ensure correct results, as these measurements depend strongly on an arbitrary blocking time, and ignore accumulated trapping effects. The reported sets of steady-state measurements, instead, show that different circuit parameters must be individually controlled for performing accurate comparisons, and to identify correct trends and magnitudes. $\mathrm{d}R_{\mathrm{on}}$ has a significant impact on the on-state behavior of the characterized GaN HEMT, nearly doubling the expected conduction losses for realistic switching frequency, current, and voltage values. A framework for including $\mathrm{d}R_{\mathrm{on}}$ in GaN HEMT datasheets, with a few key linearized maps forming the basis for conduction loss estimation in a wide range of common topologies, is finally proposed. Overall, understanding and standardizing $\mathrm{d}R_{\mathrm{on}}$ will expedite the mitigation of the highlighted problems, and lead to the faster adoption of WBG power semiconductors in more and more power electronics applications.

6

Experimental Characterization of 200 V Power Semiconductors for Modular/Multi-Level Converters

This chapter summarizes the most relevant findings in the context of research on the experimental characterization of 200 V power semiconductors, which are also published in:

- **M. Guacci**, J. Azurza Anderson, K. Pally, D. Bortis, J. W. Kolar, M. Kasper, J. Sanchez, and G. Deboy, "Experimental Characterization of Silicon and Gallium Nitride 200 V Power Semiconductors for Modular/Multi-Level Converters Using Advanced Measurement Techniques," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2238–2254, 2020.

Motivation

The developed semiconductor loss measurement setup, combining transient calorimetric switching loss and on-state voltage measurements, allows to comprehensively characterize the performance of different power semiconductors. Two 200 V GaN and Si devices are compared in this study, providing models for the optimization of modular/multi-level power converters, which are able to break the performance barriers of conventional approaches.

Executive Summary

The increasing demand for higher power densities and higher efficiencies in power electronics, driven by the aerospace, EV, and renewable energy industries, encourages the development of new converter concepts. In particular, modular and/or multi-level (M/ML) topologies are employed to break the performance barriers of state-of-the-art power converters by simultaneously reducing the system losses and volume/weight. These improvements mainly originate from the replacement of high voltage transistors, e.g. 1200 V, typical for two-level converters, with low voltage, e.g. 200 V, devices, offering superior electric performance. Hence, two low on-state resistance Si and GaN 200 V power semiconductors are comprehensively characterized in this chapter to support the multi-objective optimization and the design of M/ML power converters. First, the selected devices are analyzed experimentally determining their conduction, thermal and switching characteristics. In the course of this analysis, an unexpected switching loss mechanism is observed in the Si devices at hand; the physical reason of this behavior is clarified and it is proven to be solved in next generation research samples, which are also characterized by measurements. Finally, the influence of the measured power semiconductor performance on the overall efficiency and power density of a typical converter is determined through a case study analyzing a hard-switching half-bridge operated as single-phase inverter, i.e. the fundamental building block of M/ML topologies. It is concluded that, in this voltage and power class, GaN e-FETs are nowadays approximately a factor of three superior to Si power MOSFETs; however, the better heat dissipation achieved by the latter in this voltage class still makes them the preferred solution for higher power applications.

6.1 Introduction

Modern application areas of power electronics define unprecedented requirements in terms of efficiency and volumetric/gravimetric power density. In particular, the established trends towards the electrification of transport generates a strong demand for high power density converters [104, 105] since, e.g. in MEA and EVs, any additional weight reduces the payload capacity and limits the range/mileage. At the same time, the rising share of renewable energies in the electricity generation requires ultra-high efficiency power converters to minimize the losses at the interface between the renewable sources and the distribution grid [106–108].

Most of the power electronic systems in the mentioned application areas perform DC/AC energy conversion, e.g. when tied to the grid or in VSD, and have output power ratings typically ranging from several kW (e.g. VSD [109]

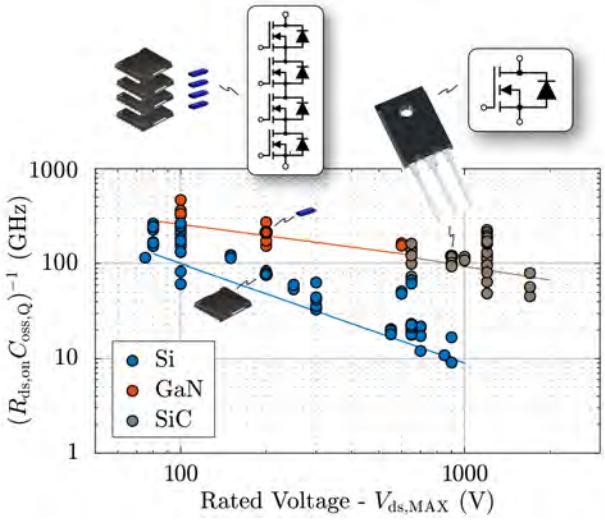


Fig. 6.1: FoM considering conduction losses and (capacitive) hard-switching losses of more than hundred commercially available Si (blue), GaN (red), and SiC (brown) power devices in dependency of their blocking voltage capability $V_{\mathrm{ds,MAX}}$. The monotonic decrease of the FoM with increasing $V_{\mathrm{ds,MAX}}$ justifies the interest towards modular and/or multi-level power converters, where typically several lower voltage devices are connected in series to replace and outperform single higher voltage devices.

or EV on-board battery chargers [36]) to few tens of kW (e.g. residential PV installations [108] or MEA power systems [110]). In fact, even converters with higher power ratings, i.e. up to hundreds of kW, are preferably realized by interconnecting smaller converters, e.g. rated for few tens of kW [111, 112], since scalable and modular approaches generally enable cost reduction and fault-tolerance, respectively [113]. Moreover, also the DC-link voltages V_{dc} at stake are comparable among these applications; e.g. 540 V and (in the future) 1000 V are typical voltage levels for DC buses in MEA [112, 114], 400 V and 800 V are the most common voltages of (fully charged) traction batteries in EVs [115], and approximately 400 V and 800 V are obtained from the active rectification of single-phase and 3-Φ grids, and/or are required to feed power into the grid.

Modular and/or multi-level (M/ML) DC/AC power converter topologies are identified as the most prominent approach to meet all the discussed performance targets. In fact, by taking advantage of the superior performance of

low voltage power semiconductors (see **Fig. 6.1**), M/ML inverters achieve reduced losses in the power stage, resulting in higher efficiencies and downsized heat sinks [108]. Additionally, a high number of voltage levels reduces the filtering effort, i.e. minimizes the volume/weight of the filter components by increasing the effective frequency of the output waveforms and/or by reducing their harmonic content [116] as highlighted in **Fig. 6.2**, where the structure and the switch node voltage v_{sw} waveform of a M/ML inverter, i.e. of a five-level Flying Capacitor converter (FCC), are compared with the ones of a conventional two-level inverter.

The remarkable potential of this class of converters is confirmed in literature; e.g. [106, 108, 112, 117] among others, prove how M/ML approaches with output power ratings up to tens of kW can outperform traditional two-level inverter solutions both in terms of efficiency and power density. Moreover, M/ML converters are already in use in successful products, confirming their market readiness [118].

Virtual prototyping and multi-objective optimization, e.g. in terms of efficiency and power density, are the key enablers to meet ambitious performance targets with minimum amount of materials and resources. Accordingly, these concepts are becoming the preferred industry approach to perfect the design of power electronic systems [119–121]. The optimization of power converters relies on an accurate performance characterization of every component, i.e. on the derivation of mathematical models which allow to determine the performance of a converter in dependence of its design parameters, e.g. the selected topology, modulation scheme, power semiconductors, switching frequency, etc.

When efficiency and power density are defined as performance indexes, accurate models of the power semiconductors become essential. In fact, the conduction losses of the power stage can have a significant impact on the overall converter efficiency and on the cooling requirements; moreover, determining the optimum switching frequency, which mostly depends on the switching losses and on the thermal performance of the selected power semiconductors, is essential to minimize the size of the passive components.

The first parameter guiding the selection of the most suitable switches for a specific power converter is their blocking voltage rating $V_{ds,MAX}$, which must fulfill

$$V_{ds,MAX} \geq V_{ds,o} = \alpha \frac{V_{dc}}{f(N)}. \tag{6.1}$$

In (6.1), α defines a safety margin, e.g. $\alpha = 1.3$, V_{dc} is the DC-link voltage of the inverter (see **Fig. 6.2(a)-(b)**), N indicates the number of voltage levels

(e.g. $N = 5$ in **Fig. 6.2(a)** and $N = 2$ in **Fig. 6.2(b)**, as visible in **Fig. 6.2(c)-(d)**, respectively) and $f(N)$ is a function associated with the selected converter topology, e.g. $f(N) = N - 1$ for N-level FCCs [116] as well as for conventional two-level inverters ($N = 2$). For example, if $V_{dc} = 540\,V$, $V_{ds,o} = 702\,V$ results from (6.1) for a two-level inverter ($f(2) = 1$), while $V_{ds,o} = 176\,V$ for a five-level FCC ($f(5) = 4$). Generally, inserting in (6.1) the mentioned values of V_{dc} and typical values of N, e.g. $3 \leq N \leq 7$, $V_{ds,MAX} = 200\,V$ is frequently obtained [108, 112] after rounding the resulting $V_{ds,o}$ to the closest voltage class of power devices available on the market (see **Fig. 6.1**). To maximize the power semiconductor performance, it is convenient to select a value of N for which $V_{ds,o}$ is close to a common voltage class, e.g. 200 V. As shown in **Fig. 6.1**, 200 V power semiconductors are nowadays available both in Si (blue) and GaN (red) technology.

A practical approach to compare different power semiconductors is based on the analysis of their FoM [122], i.e. a numeric value obtained combining several characteristics of a device, appropriately selected to represent its performance. The FoM calculated as $1/(R_{ds,on}C_{oss,Q})$ [123] is considered as a good indicator of the performance of hard-switching power stages, typical for M/ML topologies. In this FoM, $R_{ds,on}$ and $C_{oss,Q}$ are the on-state resistance and the charge-related parasitic output capacitance of a power semiconductor, respectively. **Fig. 6.1** depicts this FoM for several Si, GaN, and SiC power semiconductors in dependency of their $V_{ds,MAX}$. The monotonic decrease of the FoM with increasing $V_{ds,MAX}$ justifies the interest in M/ML converters. However, for $V_{ds,MAX} \leq 200\,V$, the FoM of GaN and Si are too similar to constitute a reliable performance metric. Additionally, the considered FoM does not include aspects determining the performance of a power device besides $R_{ds,on}$ and $C_{oss,Q}$, e.g. temperature-dependent conduction losses, heat dissipation capability, current-dependent switching losses, etc. Accordingly, even though GaN and Si 200 V power semiconductors are nowadays successfully employed in M/ML converters, an accurate evaluation of their performance, facilitating the optimization of the design parameters and the selection of the most suitable semiconductor technology in each specific application, is not yet available.

For all the above mentioned reasons, this chapter aims to comprehensively characterize, by experimental measurements, the performance of selected best-in-class 200 V power semiconductors. The results of this analysis, while also serving for a more general comparison between GaN and Si devices, provide accurate models to support the multi-objective optimization of M/ML power converters, i.e. to facilitate the achievement of the stringent perfor-

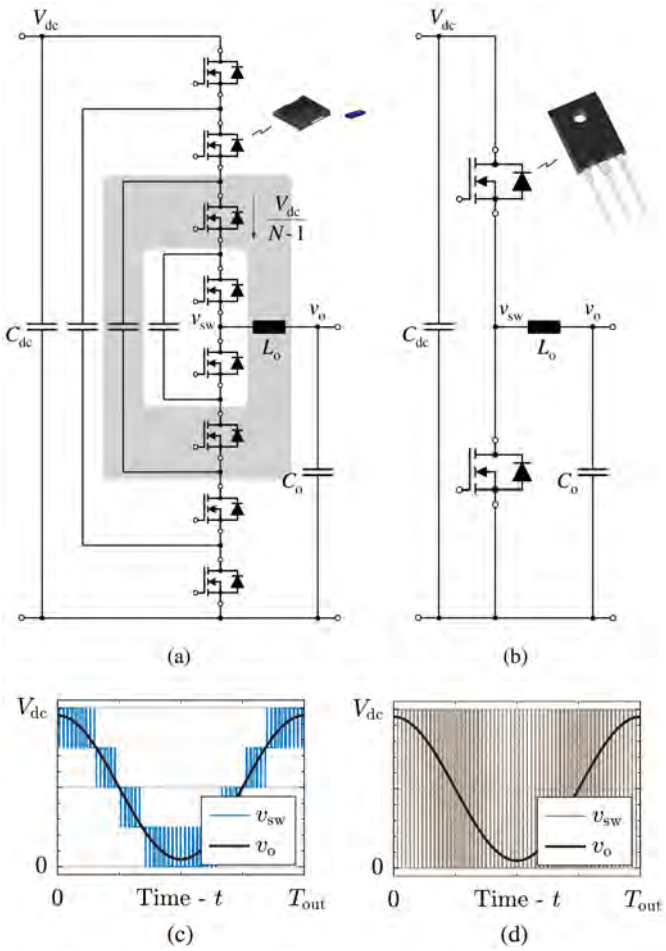


Fig. 6.2: (a) Example of a typical multi-level inverter, i.e. a Flying Capacitor converter (FCC) with five voltage levels ($N = 5$), realized with the series connection of several low voltage power semiconductors ($N-1 = 4$ per side), compared to **(b)** a conventional two-level inverter employing two higher voltage devices. The gray area in **(a)** highlights one pair of transistors (out of the $N - 1 = 4$ pairs) in bridge-leg configuration, i.e. operating with complementary gate signals, forming the FCC. **(c)**-**(d)** Idealized switch node voltage v_{sw} and output voltage v_o waveforms (measured against the negative DC bus) associated with the converters shown in **(a)** and **(b)**, respectively, within one AC output period T_{out}.

mance targets defined by the aerospace, EV, and renewable energy industries. Moreover, a guideline for the power semiconductor industry is provided by highlighting how each characteristic of the considered devices, e.g. the value of $R_{ds,on}$, affects the overall converter performance, i.e. it results evident where improvements at the device level are nowadays most required.
Considering the increasing power (and thus current) demand in the mentioned application areas, the interest in ultra-high efficiency converters, and the fact that several devices are often connected in series in the path of the load current in M/ML topologies (see **Fig. 6.2(a)**), this study focuses on the power semiconductors offering the lowest value of $R_{ds,on}$ in the 200 V voltage class, corresponding to $R_{ds,on} \approx 10\,m\Omega$.
The employed measurement setups, designed hardware prototypes and selected power semiconductors are introduced in **Section 6.2**. Their conduction, thermal and switching performance is separately evaluated in **Sections 6.3**, **6.4** and **6.5**, respectively. An anomaly observed in the switching behavior of the Si devices at hand is explained and experimentally proven to be solved in **Section 6.6**. Thereafter, the obtained data are combined in **Section 6.7** to quantify the performance limits of a basic power converter, which is identified as fundamental building block of several M/ML topologies, in dependence of the selected power semiconductors. **Section 6.8** concludes the chapter.

6.2 Devices-Under-Test and Measurement Setup

The Si and GaN 200 V power semiconductors with the lowest value of $R_{ds,on}$ on the market are the IPT111N20NFD OptiMOS 3 Fast Diode (FD) Si power MOSFET [80] and the EPC 2047 GaN e-FET [124]. For the reasons described in **Section 6.1**, these two switches, whose nominal characteristics are listed in **Tab. 6.1**, are considered as the best candidates for the performance evaluation described in this chapter. Additionally, since these benchmark devices feature similar characteristics (same voltage rating and same nominal $R_{ds,on}$ value), they offer the opportunity to fairly compare, in more general terms, GaN e-FETs against Si power MOSFETs.
In the next sections, the performance of the selected power semiconductors, named hereafter DUT, is experimentally verified in a setup mainly consisting of two DUT, T_h and T_l, in bridge-leg configuration, mounted on a heat sink. In this measurement setup, the waveforms of the voltage across and of the current flowing through the DUT can be easily adjusted in open-loop control;

Tab. 6.1: Nominal characteristics of the IPT111N20NFD OptiMOS 3 Fast Diode (FD) Si power MOSFET [80] and of the EPC2047 GaN e-FET [124].

Power Semiconductor		$V_{ds,MAX}$	$I_{ds,MAX}$	$R_{ds,on}$	$C_{oss,Q}$	$C_{rss,Q}$	$(R_{ds,on} C_{oss,Q})^{-1}$	**Package**
Manufacturer	Model		@ 25 °C	@ 25 - 150 °C	@ 120 V		@ 25 °C - 120 V	**Area**
Infineon	OptiMOS 3 FD	200 V	96 A	9 - 26 mΩ	1430 pF	49 pF	77 GHz	116 mm^2
EPC	EPC 2047	200 V	32 A	7 - 12 mΩ	540 pF	16 pF	265 GHz	7 mm^2

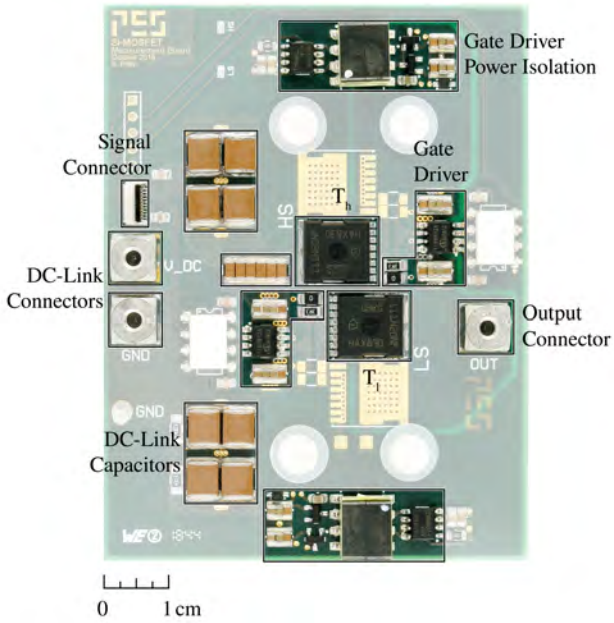


Fig. 6.3: Employed measurement setup designed to evaluate the performance of the IPT111N20NFD OptiMOS 3 Fast Diode (FD) Si power MOSFET [80] on a PCB. The setup is formed by two DUT, T_h and T_l, in bridge-leg configuration, the respective gate drivers [125] with isolated signal transmission and isolated power supply, and the DC-link/commutation capacitor C_{dc} [93]. The DC input voltage source V_{dc}, the symmetric *LC* output filter, and the load resistor R_o are connected to the PCB through screw connectors. The control board providing the switching state information is connected through the signal connector.

additionally, by modifying the network connected at the switch node and/or the value of the load resistor R_o, a comprehensive characterization of the thermal, conduction, and switching performance of the DUT is enabled for different operating conditions, regardless of their final application.
The hardware realizations of the setup are shown in **Fig. 6.3** and **Fig. 6.4** for the OptiMOS 3 FD (Si power MOSFET) and for the EPC 2047 (GaN e-FET), respectively, highlighting the most significant components soldered on the PCBs.

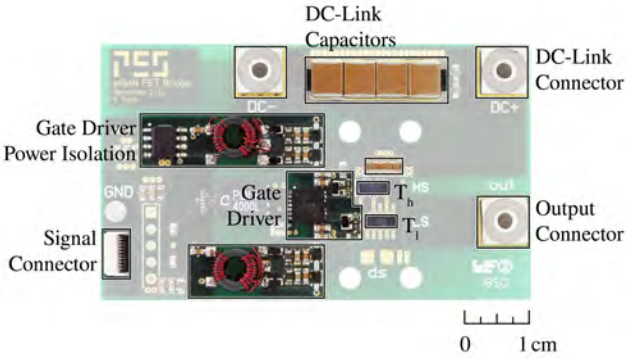


Fig. 6.4: Employed measurement setup designed to evaluate the performance of EPC 2047 GaN e-FETs [124] on a PCB. The setup is formed by two DUT, T_h and T_l, in bridge-leg configuration, the half-bridge gate driver [126] with isolated signal transmission and isolated power supply, and the DC-link/commutation capacitor C_{dc} [93].

6.3 Conduction Performance Evaluation

The selection of the optimum power semiconductors for a specific power converter is often driven by the estimated conduction losses. Hence, the conduction performance of the DUT is evaluated in this section by characterizing their $R_{ds,on}$ in dependence of their junction temperature T_j. To perform these measurements, different DC current values I_{dc} are impressed through T_h and T_l (see **Fig. 6.3** and **Fig. 6.4**) which are permanently kept in on-state, while the voltage v_{ds} across them and their case temperature T_c are accurately measured. Afterwards, $R_{ds,on}$ is calculated as v_{ds}/I_{dc} and T_j is determined using $T_c + R_{th,j\text{-}c} R_{ds,on} I_{dc}^2$, where $R_{th,j\text{-}c}$ indicates the thermal resistance between the junction and the case of the DUT (specified in their datasheets [80, 124]).
The obtained results (average between T_h and T_l) are summarized in **Fig. 6.5** for both OptiMOS 3 FD (blue) and EPC 2047 (red), comparing the measured values of $R_{ds,on}$ (solid and dots) with their datasheet (shaded) counterparts (typical and worst-case). A very good matching between measured and nominal values is generally observed. For the OptiMOS 3 FD, a discrepancy only appears for high values of T_j, and it is attributed to an unclear definition of T_c in [80]. For the EPC 2047, instead, the measured curve is consistently at the boundary defined by the worst-case curve reported in [124].
Even if the EPC 2047 outperforms the OptiMOS 3 FD under static conditions, it cannot be inferred that the EPC 2047 would as well offer superior conduction

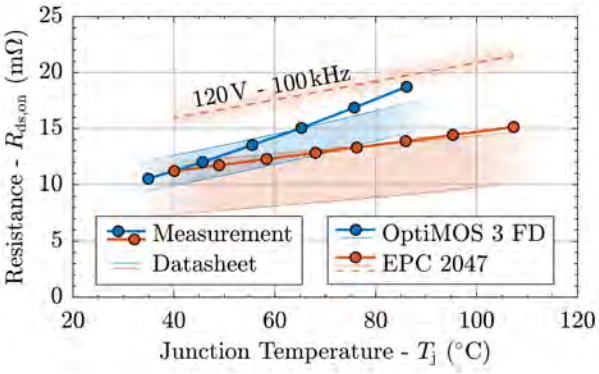


Fig. 6.5: Measured (solid and dots) and datasheet (shaded, typical and worst-case) values of $R_{ds,on}$ in dependency of the junction temperature T_j for the OptiMOS 3 FD (blue) and for the EPC 2047 (red). Additionally, estimated (dashed) values of $R_{ds,on}$ for the EPC 2047, considering the impact of the dynamic $R_{ds,on}$ phenomenon for a blocking voltage $V_{dc} = 120\,V$ and a switching frequency $f_{sw} = 100\,kHz$ [42]. Depending on the influence of the dynamic $R_{ds,on}$ phenomenon, the EPC 2047 can offer either consistently better or worse conduction performance compared to the OptiMOS 3 FD.

performance in a real power converter. In fact, GaN e-FETs typically suffer from the dynamic $R_{ds,on}$ phenomenon [42]; this effect is responsible for increasing, in switched applications, the value of $R_{ds,on}$ measured in DC conditions by a factor k_{dyn}, which mainly depends on the voltage blocked by the transistor in off-state V_{dc} and on its switching frequency f_{sw}. If $k_{dyn}(V_{dc} = 120\,V, f_{sw} = 100\,kHz) = 0.39$, i.e. a 39 % increase of $R_{ds,on}$, is considered as an example [42], the measured (solid and dots) values of $R_{ds,on}$ for the EPC 2047 can be scaled accordingly, resulting in worse conduction performance, as highlighted in **Fig. 6.5** (dashed). In general, while the information about $R_{ds,on}$ provided in the datasheets of Si MOSFETs can be sufficiently accurate, it is necessary, instead, to experimentally characterize the dynamic $R_{ds,on}$ phenomenon of each GaN e-FET individually [95].
Nevertheless, it can be concluded that, at least for f_{sw} in the hundreds of kHz-range, OptiMOS 3 FD and EPC 2047 offer comparable conduction performance, as initially expected and desired.

6.4 Thermal Performance Evaluation

The volume/weight reduction of power converters, strongly demanded in the mentioned application areas, inevitably implies higher loss densities. Accordingly, the precise understanding of the thermal characteristics of every component in the power stage becomes fundamental. Despite this, the thermal parameters of the power semiconductors indicated in their datasheets are often of no use. Accordingly, their thermal performance must be experimentally characterized, e.g. like it is done for the DUT in this section.
In a setup similar to the one described in **Section 6.3**, different DC power values P_T are injected in T_h and T_l, (see **Fig. 6.3** and **Fig. 6.4**), while T_c is measured and the heat sink temperature T_{hs} is maintained constant. After calculating T_j, the measured values of P_T (average between T_h and T_l) are plotted in **Fig. 6.6** for both OptiMOS 3 FD (blue) and EPC 2047 (red). The curves are linear as expected, and their slope yields the thermal resistance $R_{th,j\text{-}hs} = R_{th,j\text{-}c} + R_{th,c\text{-}hs}$ between the junction of the DUT and the heat sink. The absolute values of $R_{th,j\text{-}hs}$ are strictly dependent on the geometries and on the thermal properties of the setup, e.g. on the design of the heat sink and on the selected thermal interface material [83]. However, since an optimized heat sink structure is considered for both DUT for the sake of a fair

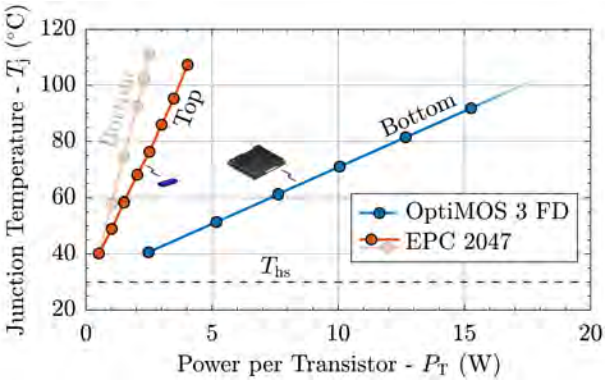


Fig. 6.6: Measured (solid and dots) values of T_j in dependency of the dissipated power P_T for the OptiMOS 3 FD (blue) and for the EPC 2047 (red), for a constant heat sink temperature T_{hs} = 30 °C (dashed). The two red curves are associated with bottom-side (through the PCB) and top-side (through the package) cooling of the EPC 2047. Since a lower thermal resistance $R_{th,j\text{-}hs}$ between the junction of the DUT and the heat sink is achieved with top-side cooling, this solution is preferred.

comparison, generally valid conclusions can be drawn. The package of the OptiMOS 3 FD features a heat-slug pad on the bottom-side enhancing the performance of bottom-side cooling concepts. Additionally, if several vias are placed in correspondence of this pad, the heat transfer through the PCB can be maximized. The package of the EPC 2047, instead, features a very dense footprint and a small size; moreover, several components must be placed nearby the GaN e-FETs to minimize parasitic inductances and capacitances in the power stage, i.e. to improve their switching performance, given the higher switching speeds. Hence, for the EPC 2047, no space is available for vias and top-side cooling concepts are preferable, as highlighted in **Fig. 6.6**. Simultaneous top and bottom-side cooling would in both cases improve the thermal performance, but on the other hand result in unpractical heat sink designs. Nevertheless, because of its larger chip area and package, approximately five times more power can be dissipated (a five times lower value of $R_{\text{th,j-hs}}$ can be achieved) for the same T_{j} and T_{hs} by the OptiMOS 3 FD compared to the EPC 2047.
This result justifies in part the significantly different current ratings $I_{\text{ds,MAX}}$ indicated in the datasheets of the DUT (see **Tab. 6.1**), and constitutes a limitation for the EPC 2047. In fact, although several GaN e-FETs can be connected in parallel in the same PCB area occupied by a single OptiMOS 3 FD to increase the overall $I_{\text{ds,MAX}}$, additional switching losses and new challenges, related to the parallelization of fast switching power semiconductors, arise simultaneously [127].

6.5 Switching Performance Evaluation

Selecting the optimum switching frequency of a specific power converter requires a comprehensive switching loss map of the employed power devices. Unfortunately, the switching loss data reported in the datasheets of power semiconductors (if present at all) are generally incomplete [80, 124]. Moreover, the design of the power stage, e.g. the selected components (gate driver IC, commutation capacitors, etc.) and their placement, strongly influences the switching behavior of the power devices. Hence, similarly to the case discussed in **Section 6.4**, meaningful switching loss data can only be obtained experimentally. In particular, the setups of **Fig. 6.3** and **Fig. 6.4**, complemented for this purpose by connecting the DC voltage source V_{dc} and, optionally, the symmetric LC output filter formed by the output inductor L_{o} and the output capacitors C_{o}, and R_{o} are considered herein.
The switching losses of both DUT, measured according to the transient calori-

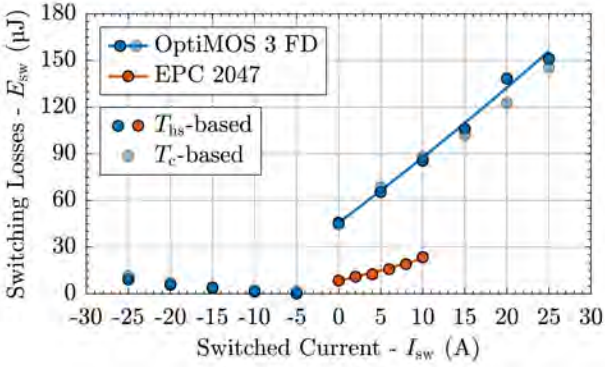


Fig. 6.7: Measured (dots) values of the switching energy E_{sw} dissipated in one switching transition by the entire half-bridge formed by either two OptiMOS 3 FD (blue) or two EPC 2047 (red), in dependency of the switched current I_{sw} in ZVS ($I_{sw} < 0$), ZCS ($I_{sw} = 0$), and hard switching (HS, $I_{sw} > 0$) conditions. Additionally, quadratic fit (solid) on the measured values in HS conditions (see **Tab. 6.2**). HS losses ($I_{sw} > 0$) are shown for both OptiMOS 3 FD (blue) and EPC 2047 (red), while ZVS losses ($I_{sw} < 0$) are depicted only for the OptiMOS 3 FD. Two different transient calorimetric switching loss measurement methods, one based on the dynamics of T_{hs}, and the other one based on the dynamics of T_c, are compared [81].

metric measurement method based on the heat sink temperature T_{hs} [79], are summarized in **Fig. 6.7**, where they are plotted in the form of the switching energy E_{sw} dissipated by the entire half-bridge in one switching transition, in dependency of I_{sw}; positive and negative values of I_{sw} along the x-axis correspond to HS and ZVS conditions, respectively. Even though these results are collected operating the measurement setups as DC/DC converters in electric steady-state, once the relation between E_{sw} and I_{sw} is determined, also the expected switching losses for different operating conditions can be readily estimated by summing the switching losses occurring in each switching period, obtained considering different switched current values in **Fig. 6.7**.
Observing the results related to the OptiMOS 3 FD, it is evident how the measured values of E_{sw} in ZVS conditions are much (between fifteen and twenty times) smaller than their HS counterparts for the same values of I_{sw}. Comparing the two DUT instead, the measured values of E_{sw} in HS conditions result significantly (between three and six times) smaller for the EPC 2047 (red), which accordingly outperforms the OptiMOS 3 FD (blue). However, the range of admissible I_{sw} of the EPC 2047 is reduced due to its inferior power

Tab. 6.2: Coefficients of the HS loss model for OptiMOS 3 FD Si power MOSFETs and EPC 2047 GaN e-FETs.

Power Semiconductor		k_0	k_1	k_2
Manufacturer	Model	(µJ)	(V µs)	(Ω µs)
Infineon	OptiMOS 3 FD	45.7	4.00	0.014
EPC	EPC 2047	8.47	1.25	0.014

dissipation capability. Although the measured values of E_{sw} significantly depends on the design of the power stage and of the gate driver, both setups are optimized to achieve the best switching performance, hence enabling a direct comparison.
The values of E_{sw} of the OptiMOS 3 FD obtained with the ultra-fast T_c-based transient calorimetric measurement method are additionally plotted in **Fig. 6.7** and compared with the ones obtained with the T_{hs}-based method. An almost perfect matching is observed between the two results.
For convenience, the quadratic polynomial

$$E_{sw}(I_{sw}) = k_0 + k_1 I_{sw} + k_2 I_{sw}^2 \tag{6.2}$$

is fit on the measured curves for $I_{sw} \geq 0$ (see **Fig. 6.7**); the derived coefficients k are reported in **Tab. 6.2** for both DUT, providing a compact expression for modeling the losses occurring in ZCS and HS conditions, and highlighting the superior performance of the EPC 2047.
The relative outcome of this comparison is expected also for other Si MOSFETs and GaN e-FETs of similar characteristics, since the beneficial properties of WBG semiconductors ensure lower values of C_{oss} (see **Tab. 6.1**), i.e. lower values of stored energy to be dissipated in every HS transition, as well as faster switching speeds. The latter statement is confirmed in **Fig. 6.8(a)**, where the measured values of the voltage switching speed dv/dt are depicted with the same notation as used in **Fig. 6.7**. While 31 V/ns is the typical dv/dt value of the EPC 2047, only 6 V/ns could be achieved with the OptiMOS 3 FD. **Fig. 6.8(a)** includes as well the measured dv/dt values in ZVS conditions; for the EPC 2047, the measured points are aligned on the slope $1/2\, C_{oss,Q}$ as expected [79].
To highlight once more the different dv/dt values between the two DUT, **Fig. 6.8(b)** and **Fig. 6.8(c)** show the measured waveforms of v_{sw} in a ZVS and in a HS transition with $I_{sw} = \pm 5$ A. In the ZVS transition, the highly nonlinear behavior of C_{oss} of the OptiMOS 3 FD can be recognized. Additionally,

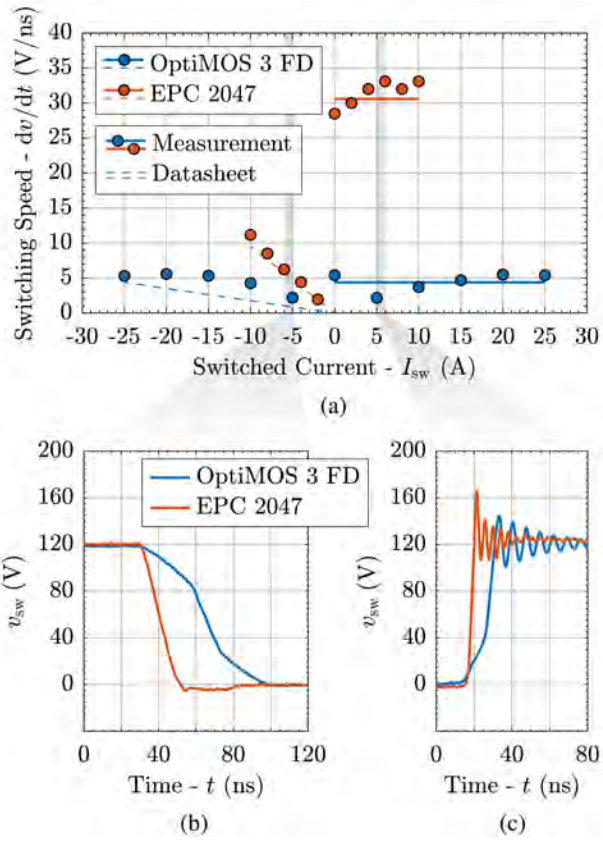


Fig. 6.8: (a) Measured (dots) values of the voltage switching speeds $\mathrm{d}v/\mathrm{d}t$ of the OptiMOS 3 FD (blue) and of the EPC 2047 (red), in dependency of I_{sw} in the conditions considered in **Fig. 6.7**. Additionally, ideal (dashed) $\mathrm{d}v/\mathrm{d}t$ values in ZVS conditions and average measured (solid) $\mathrm{d}v/\mathrm{d}t$ values in HS conditions. The $\mathrm{d}v/\mathrm{d}t$ values are calculated observing the variation of v_{sw} from 10 % (90 %) to 90 % (10 %) of V_{dc}. Finally, measured waveforms of v_{sw} in a **(b)** ZVS transition and in a **(c)** HS transition of the OptiMOS 3 FD (blue) and of the EPC 2047 (red), with $I_{sw} = \pm 5$ A.

from the resonance frequency f_r of the voltage oscillations visible in the HS transitions and the values of C_{oss} at V_{dc} [80, 124], the power loop inductance L_{pl} of the two setups can be calculated according to $1/C_{oss}\,(2\pi f_r)^2$; $L_{pl} = 3.7$ nH is obtained for the OptiMOS 3 FD and $L_{pl} = 1.2$ nH for the EPC 2047. This

difference can be attributed mainly to the smaller footprint of the package of the EPC 2047, which facilitates a more compact power stage design.

6.6 Unexptected Switching Behavior of OptiMOS 3 FD

The HS loss model described by (6.2) allows to split E_{sw} in a I_{sw}-dependent and in a I_{sw}-independent part. The latter coincides with the (capacitive) ZCS losses $E_{sw,ZCS}$, which can be estimated [128] according to

$$E_{sw,ZCS} = E_{sw}(0) = Q_{oss} V_{dc}\,, \tag{6.3}$$

where Q_{oss} indicates the parasitic output charge of the DUT at V_{dc}. Comparing the values of $E_{sw,ZCS}$ obtained with (6.3) with the measured values $E_{sw}(0)$ reported in **Fig. 6.7**, a satisfactory matching is observed for the EPC 2047, while a significant discrepancy is noticed for the OptiMOS 3 FD. This unexpected finding is further investigated measuring $E_{sw,ZCS}$ for different $\mathrm{d}v/\mathrm{d}t$ values, i.e. for different values of the turn-on gate resistance $R_{g,on}$. The results of this analysis are summarized in **Fig. 6.9** and in **Tab. 6.3**, where the measured values of $E_{sw,ZCS}$ (solid) are compared with the calculated ones (dashed) in dependency of $R_{g,on}$, for both DUT. As expected, the measured $E_{sw,ZCS}$ of the EPC 2047 (red) are independent of $R_{g,on}$ and validate (6.3), additionally confirming the accuracy of the considered measurement method. Differently, the measured $E_{sw,ZCS}$ of the OptiMOS 3 FD (blue) are, for typical values of $R_{g,on}$, e.g. $R_{g,on} \leq 10\,\Omega$, significantly higher than their nominal counterparts and strongly dependent on the $\mathrm{d}v/\mathrm{d}t$ values. This trend is ultimately responsible for compromising the switching performance of the OptiMOS 3 FD, since $E_{sw,ZCS}$ defines the lower boundary of the HS losses [128], i.e. k_o.
The observed phenomenon originates from the internal structure of the analyzed power semiconductor, as explained in the following. Modern field plate or shielded gate transistors, such as the OptiMOS 3 FD, feature a 3D structure able to simultaneously reduce gate charge Q_g and area-specific $R_{ds,on}$ values [129–131]. As shown in **Fig. 6.10(a)**, this 3D structure consists of a deep trench comprising two electrodes: one is connected to the gate potential, while the other one, i.e. the field plate, is tied to the source potential. Whereas the gate forms a vertical MOS channel along the side face of the mesa region between the trenches, the field plate buried within the trench provides countercharges allowing to increase the n-doping of the drift region, and hence to reduce the specific $R_{ds,on}$ of the MOSFET for a given voltage

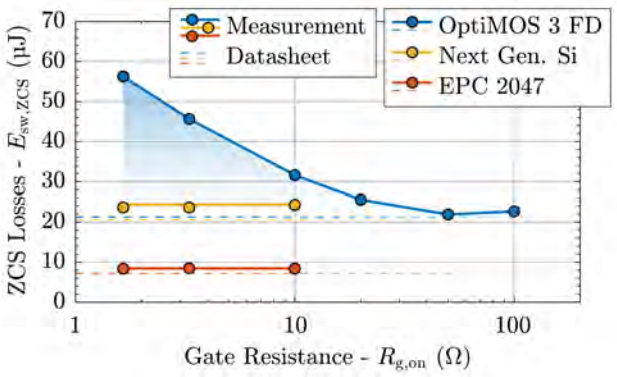


Fig. 6.9: Measured (solid and dots) and estimated (dashed) values of the energy dissipated in one ZCS transition $E_{sw,ZCS}$ by the entire half-bridge formed by either two OptiMOS 3 FD (blue), two EPC 2047 (red), or two of the next generation Si switches (yellow) in dependency of the turn-on gate resistance $R_{g,on}$. While the measured values of $E_{sw,ZCS}$ of the EPC 2047 and of the next generation Si switch are independent of the dv/dt values and approach the results of the respective calculations, the measured $E_{sw,ZCS}$ of the OptiMOS 3 FD are unexpectedly higher for low values of $R_{g,on}$, i.e. for high dv/dt values.

Tab. 6.3: Value of $R_{g,on}$ and associated measured dv/dt and $E_{sw,ZCS}$ values for OptiMOS 3 FD Si power MOSFETs.

Power Semiconductor		R_g	dv/dt	$E_{sw,ZCS}$
Manufacturer	Model	(Ω)	(V/ns)	(µJ)
Infineon	OptiMOS 3 FD	1.6	6.2	56.3
		3.3	6.0	45.6
		10	4.8	31.7
		20	3.7	25.5
		50	2.3	21.9
		100	1.6	22.7

rating [129]. Furthermore, the field plate shields the gate electrode located above the drain contact, and helps to reduce the parasitic gate-drain capacitance C_{gd}, i.e. to increase the switching speed while avoiding dv/dt induced parasitic turn-on [132]. In contrast to SJ devices, the field plate is not depleted when the transistor is in the blocking state; hence, the field plate needs to

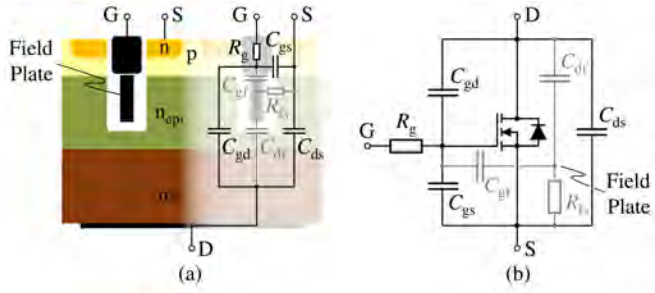


Fig. 6.10: (a) Cross section of a field plate transistor, similar to the one of the OptiMOS 3 FD; the parasitic components originating from the internal structure of the device are shown according to their physical origin. **(b)** Circuit schematic of the parasitic components highlighted in **(a)**. The parasitic elements associated with the field plate are represented in gray.

be isolated from the surrounding Si area, e.g. through a thick oxide able to withstand the breakdown voltage of the device.
However, the field plate structure introduces additional parasitic elements affecting the dynamic performance of the switch; e.g. the parasitic capacitances between the field plate and the drain C_{df}, and between the field plate and the gate C_{gf} appear, as visible in **Fig. 6.10**. The value of these capacitances is defined by the thickness of the oxide between the field plate and the Si substrate, and between the field plate and the gate electrode, respectively. Moreover, since the field plate is manufactured out of polysilicon, a non-zero resistance R_{fs} between the field plate and the source is also present [129] (see **Fig. 6.10**).
Analyzing the impedance network simplifying the internal structure of the OptiMOS 3 FD, two intrinsic *R-C* snubber circuits can be identified (see **Fig. 6.10(b)**). One is the R_{fs}-C_{gf} gate snubber that, together with the internal gate resistance R_g, damps the ringing of the gate-source voltage v_{gs} during the switching transients. The other one is the R_{fs}-C_{df} snubber, and it is designed to actively limit overvoltage spikes occurring in HS transitions on the drain-source voltage v_{ds}. Hence, by avoiding excessive ringing on v_{sw}, it reduces the electromagnetic (EM) noise emissions.
Unfortunately, the parasitic elements introduced by the field plate structure can as well have a negative impact on the switching losses. In particular, when the displacement currents generated by a HS transition cause the departing of the field plate potential from its reference source potential, the gate-source

capacitance C_{gs} is charged through C_{gd}, as well as through the series connection of C_{df} and C_{gf}. With high values of $^{dv}/_{dt}$, a partial parasitic turn-on might occur as the internal v_{gs} approaches the gate threshold voltage. This phenomenon is believed to cause the additional switching losses highlighted in **Fig. 6.9**, which are consistently occurring at high $^{dv}/_{dt}$ values.
Consequently, in the manufacturing process of field plate MOSFETs, there is a trade-off between avoiding overvoltages and excessive ringing of v_{gs} and v_{ds}, and reducing the switching losses. Whereas the OptiMOS 3 FD is optimized for the former to enable quiet EM operation of HS converter systems, the next generation 200 V transistors are optimized for the latter, i.e. towards the lowest switching losses, by entirely suppressing any coupling between gate and field plate electrodes, and by having a quasi-zero impedance connection between the field plate and the source.
To conclude this analysis, research samples belonging to the next generation of 200 V transistors are analyzed for the same conditions used for the OptiMOS 3 FD, and the measured (solid and dots) and calculated (dashed) values of $E_{sw,ZCS}$ are also shown in **Fig. 6.9** (yellow) for comparison. Supporting the previous explanation, the measured values of $E_{sw,ZCS}$ of the next generation switches are independent of $R_{g,on}$, i.e. of the $^{dv}/_{dt}$ values; hence, significantly enhanced switching performance is achieved.

6.7 Power Converter Case Study

The conduction, thermal, and switching characteristics of the DUT, i.e. OptiMOS 3 FD Si power MOSFETs and EPC 2047 GaN e-FETs, are separately evaluated in **Sections 6.3**, **6.4**, and **6.5**. These experimental results are combined herein to determine the performance limits of a basic power converter in dependency of the devices selected for the realization of its power stage (see **Fig. 6.3** and **Fig. 6.4**). Additionally, since this converter can be considered as part of a more complex system, e.g. of a 3-Φ inverter, of a modular multi-phase inverter, or of a multi-level inverter, the obtained results can be generalized. The ultimate goal of this analysis is to quantify the expected superiority of GaN 200 V over Si 200 V power semiconductors, and to identify the bottlenecks limiting further performance improvements.

6.7.1 Converter Specifications and Loss Models

Since DC/AC power converters are of most interest in the mentioned application areas, a HS half-bridge operated as single-phase inverter, which

is identified as the fundamental building block of several M/ML inverter topologies (see **Fig. 6.2(a)**), is considered in this analysis. As a performance metric, the efficiency η of the half-bridge is calculated as a function of the switching frequency f_{sw} and of the RMS value of the output current $I_{o,RMS}$. The calculations consider all the aspects mentioned in the previous sections, in particular:

- *Conduction Performance*: the conduction losses P_{cond} are calculated as $R_{ds,on}I_{o,RMS}^2$ with a sinusoidal output current i_o. The dependence of $R_{ds,on}$ on T_j (see **Fig. 6.5**) is considered for both DUT. Additionally, the dynamic $R_{ds,on}$ phenomenon is taken into account for the EPC 2047 [42].

- *Thermal Performance*: T_j is iteratively determined according to the measurement results presented in **Fig. 6.6**, and accounted for in the calculation of P_{cond}, given the dependency of $R_{ds,on}$ with T_j (see **Fig. 6.5**). The maximum T_j is fixed at $T_{j,MAX} = 100\,°C$ and $T_{hs} = 50\,°C$ is considered, similar to the specifications given in [133].

- *Switching Performance*: the switching losses P_{sw} are calculated according to **Fig. 6.7** and **Tab. 6.2**, i.e. only the HS losses are considered (the ZVS losses are neglected). In particular, an appropriate value of I_{sw} is selected for each switching period from the sampling of i_o (the current ripple is neglected); thus, E_{sw} is calculated according to (6.2) per each switching period, and all contributions in one AC output period are summed. Finally, the total switching energy is multiplied with the output frequency, determining P_{sw}.

For consistency with **Section 6.5**, the DC input voltage is $V_{dc} = 120\,V$ and the modulation index m is fixed to $m = {}^{2\,\hat{v}_o}/_{V_{dc}} = 1$, where $\hat{v}_o$ indicates the peak value of the sinusoidal output voltage v_o. Hence, assuming SI-units for all quantities, the output power $P_o = {}^{V_{dc}}/_{2\sqrt{2}}\, I_{o,RMS} \approx 42\, I_{o,RMS}$ is considered to calculate $\eta = 1 - {}^{(P_{sw}+P_{cond})}/_{P_o}$. $I_{o,RMS}$ is varied in the few tens of A-range, resulting in values of P_o of up to approximately 1 kW, apparently lower than the output power requirements of DC/AC converters in the application areas of interest. However, if 3-Φ M/ML inverters are considered, the overall output power is obtained, in first approximation, multiplying P_o by the number of phases, the number of levels, and/or the number of modules forming the converter, thus reaching several kW or few tens of kW. For example, considering $V_{dc} = 480\,V$ for a 3-Φ five-level FCC (see **Fig. 6.2(a)**), already $I_{o,RMS} = 10\,A$, i.e. $P_o = 420\,W$, translates into an output power rating of $3 \cdot 4 \cdot P_o = 5\,kW$. Additionally, more than one DUT can be employed, i.e.

several DUT can be connected in parallel to realize each switch forming the bridge-leg, but this option is not considered herein for the sake of simplicity.

6.7.2 Calculation Results

The results of the introduced analysis are shown in **Fig. 6.11**, where the calculated values of η are plotted in dependency of f_{sw} and $I_{o,RMS}$, for both DUT. The white areas in the plots indicate operating regions beyond the thermal limit of the half-bridge, and thus highlight how the superior thermal performance of the OptiMOS 3 FD enables higher values of $I_{o,RMS}$, and hence P_o, for a given f_{sw}, with respect to the EPC 2047 (cf. **Fig. 6.11(a)** and **Fig. 6.11(b)**). From an efficiency point of view, instead, the EPC 2047 outperforms the OptiMOS 3 FD in the whole operating region where the GaN design is thermally feasible, mostly because of its lower switching losses (see **Fig. 6.7**). The latter statement is confirmed in **Tab. 6.4**, where the maximum achievable switching frequencies f_{sw}^{MAX} are listed for different values of P_o and η, for both DUT. In **Fig. 6.11** and **Tab. 6.4**, it can be additionally observed how the half-bridge performance estimated through the FoM (see **Fig. 6.1**) are confirmed, at least in relative terms. In fact, approximately a three times higher f_{sw}^{MAX} can be achieved for the same η and P_o by the EPC 2047, with respect to the OptiMOS

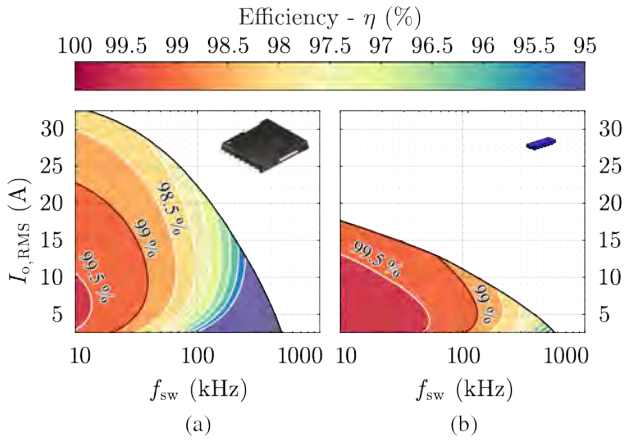


Fig. 6.11: Efficiency η of the HS half-bridge formed by either **(a)** two OptiMOS 3 FD Si power MOSFETs or two **(b)** EPC 2047 GaN e-FETs, in dependency of f_{sw} and of the RMS value of the output current $I_{o,RMS}$.

Tab. 6.4: Maximum switching frequency f_{sw}^{MAX} achievable by the HS half-bridge formed by either two OptiMOS 3 FD Si power MOSFETs or two EPC 2047 GaN e-FETs, for different values of P_o and η.

Power Semiconductor		f_{sw}^{MAX} @ P_o = 250 W		
Manufacturer	Model	η = 99 %	η = 98 %	η = 97 %
Infineon	OptiMOS 3 FD	35 kHz	77 kHz	119 kHz
EPC	EPC 2047	130 kHz	299 kHz	–

Power Semiconductor		f_{sw}^{MAX} @ P_o = 500 W		
Manufacturer	Model	η = 99 %	η = 98 %	η = 97 %
Infineon	OptiMOS 3 FD	38 kHz	97 kHz	156 kHz
EPC	EPC 2047	73 kHz	–	–

3 FD, as expected from **Tab. 6.1** [113]. However, the FoM approach neglects several aspects with a strong impact on the converter design, e.g. the thermal limit of the half-bridge. In a first step, a factor considering the typical $R_{th,j\text{-}hs}$ value of the power semiconductors could be included in the FoM definition to account for the thermal characteristics of the different devices, thus providing a more accurate insight on the converter performance limits.
Continuing with the analysis of **Tab. 6.4**, it can be observed how, e.g. for P_o = 500 W, the Si-based design achieves higher values of f_{sw} than the GaN-based design, however, at the expense of lower η. As well, the opposite variation of f_{sw}^{MAX} for increasing P_o characterizing the two DUT, i.e. an increasing f_{sw}^{MAX} for the OptiMOS 3 FD and a decreasing f_{sw}^{MAX} for the EPC 2047, indicates significantly different values of optimum P_o in the two cases. In other words, even if the two characterized power semiconductors have comparable $R_{ds,on}$ values and the EPC 2047 generally ensures better switching performance, the packaging of the OptiMOS 3 FD allows it to remain competitive for higher power applications.
Nevertheless, in a comprehensive multi-objective optimization procedure, also the chip area should be considered as a design parameter; i.e. η should be evaluated for several EPC 2047 connected in parallel (i.e. for a larger chip area) in order to increase the power rating of the GaN-based solution, and for Si power MOSFETs with a smaller chip area, since higher $R_{ds,on}$ and lower Q_{oss} values could enhance the performance of the Si-based design at low P_o and high f_{sw} values.

To conclude, the impact of f_{sw}^{MAX} on the volumetric power density of the considered single-phase inverter can be qualitatively estimated. First, the output inductor L_o can be designed according to

$$L_o = \frac{V_{dc}\, d(1-d)}{\Delta I_{o,pkpk}\, f_{sw}^{MAX}} \geq \frac{V_{dc}}{4\, k_{ripple} \sqrt{2}\, I_{o,RMS}\, f_{sw}^{MAX}}, \tag{6.4}$$

where $\Delta I_{o,pkpk}$ indicates the peak-to-peak ripple of i_o, and k_{ripple} is defined as

$$\Delta I_{o,pkpk} = k_{ripple}\, \sqrt{2}\, I_{o,RMS}. \tag{6.5}$$

Considering $k_{ripple} = 0.3$, $P_o = 500\,W$ ($I_{o,RMS} = 11.8\,A$), and the values of f_{sw}^{MAX} associated with $\eta = 99\,\%$ (see **Tab. 6.4**) as an example, $L_o = 158\,\mu H$ and $82\,\mu H$ are obtained for the Si- and GaN-based designs, respectively. The reduction by factor 1.9 in the value of L_o is directly related, i.e. inversely proportional, to the increase of f_{sw}^{MAX} achieved by the EPC 2047. Moreover, since the volume of an inductor can be assumed proportional to its inductance value for a given current rating [134], a factor 1.9 more compact design of L_o is expected in this case. Finally, since the same value of η is considered for both designs, comparable heat sink volumes can be assumed, hence leading to the GaN-based solution having a higher power density than its Si-based counterpart.

6.7.3 Sensitivity Analysis

Fig. 6.12(i-iv) summarize the sensitivity of the results shown in **Fig. 6.11** with respect to the parameters defining the conduction **(i)**, thermal **(ii)**-**(iii)** and switching **(iv)** performance of the DUT [135]. Only one parameter at a time is modified while the others are kept constant; thus, the limit values of η, f_{sw}, and $I_{o,RMS}$ are analyzed in order to understand which characteristics of each DUT constitute the major bottleneck for the performance of the power stage, i.e. which key factors should preferably be improved at the device level by the semiconductor manufacturers. In particular, the maximum achievable switching frequency f_{sw}^{η} for a given η, the maximum achievable output power P_o^{fsw} for a given f_{sw}, and the maximum achievable switching frequency f_{sw}^{Po} for a given P_o are compared.
The most relevant observations, focusing on the η, P_o, and f_{sw} values of interest, are commented in the following:

(i) Halving the value of $R_{ds,on}$ enhances the performance of both solutions, offering higher η at low f_{sw} and high $I_{o,RMS}$ values. However, already

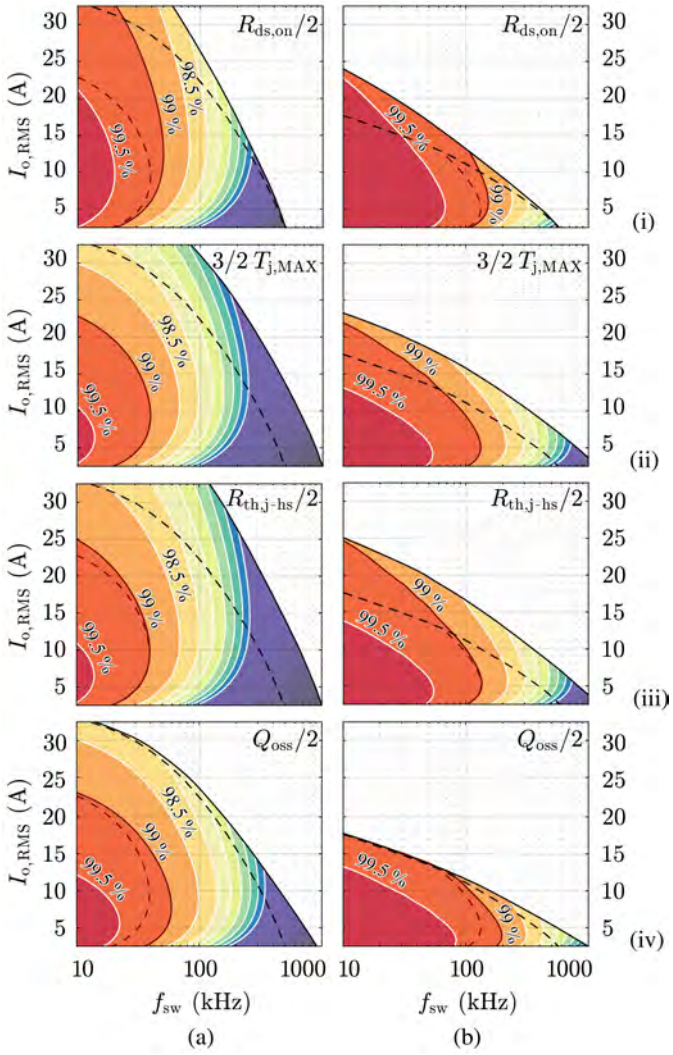


Fig. 6.12: Sensitivity analysis of η of the HS half-bridge formed by either **(a)** two OptiMOS 3 FD Si power MOSFETs or two **(b)** EPC 2047 GaN e-FETs, in dependency of f_{sw} and of $I_{o,RMS}$, for different perturbations of the parameters defining the conduction **(i)**, thermal **(ii)**-**(iii)** and switching **(iv)** performance of the DUT. The thermal limit (black, dashed) and $\eta = 99\,\%$ (red, dashed) curves of the reference designs (see **Fig. 6.11**) are reported in the corresponding plots for comparison.

at $f_{sw} = 100\,\text{kHz}$, the improvement in terms of P_o^{fsw} is almost negligible for both DUT. The reduction of conduction losses provides more room for switching losses; hence, both f_{sw}^{η} and f_{sw}^{Po} increase. The effect on f_{sw}^{Po} is stronger on the EPC 2047, since the conduction losses generally dominate its loss breakdown, particularly for low values of f_{sw}.

(ii) An increase of the allowed junction temperature $T_{j,MAX}$ from 100 °C to 150 °C does not influence η but extends the operating range of both designs. Since more conduction losses are allowed for the same f_{sw}, P_o^{fsw} increases in both cases. More significantly, since more switching losses are allowed for the same P_o, f_{sw}^{Po} doubles for the OptiMOS 3 FD and triples for the EPC 2047 if $P_o = 500\,\text{W}$ is considered.

(iii) Decreasing $R_{th,j\text{-}hs}$ has a similar effect as increasing $T_{j,MAX}$. In addition, the associated reduction of T_j, i.e. of $R_{ds,on}$, slightly improves η for every operating point. With the considered perturbation of parameters, $R_{th,j\text{-}hs}$ has the strongest influence on P_o^{fsw} and f_{sw}^{Po}, both for the OptiMOS 3 FD and for the EPC 2047.

(iv) A reduction of Q_{oss} is of particular interest for high efficiency applications. For instance, considering $\eta = 99\,\%$, halving Q_{oss} translates into approximately a 50 % increase in f_{sw}^{η} for both DUT, i.e. Q_{oss} is the parameter with the strongest influence on f_{sw}^{η}. Differently from **(i)**, the effect on f_{sw}^{Po} is more evident on the OptiMOS 3 FD, which suffers mostly from the switching losses.

Summarizing the results of this sensitivity analysis, it can be concluded that, to realize high efficiency and high power density converters at the considered voltage level and power ratings, an improvement in the switching performance is the most desirable; however, the thermal characteristics are the factor limiting a further increase of switching frequency and/or of output power rating. In particular, mainly the value of Q_{oss} defines η for high values of f_{sw}, while the value of $R_{th,j\text{-}hs}$ limits the SOA, i.e. P_o.

6.8 Conclusion

Virtual prototyping and multi-objective optimization procedures of modular and/or multi-level (M/ML) power converters support the aerospace, EV, and renewable energy industries in meeting more and more demanding requirements in terms of efficiency and volumetric/gravimetric power density. These

approaches strongly rely on accurate models of the power stage performance, which allow to identify the performance limits, and support the perfection of the design, of power converters.
Accordingly, Si and GaN power semiconductors with 200 V blocking voltage capability and the lowest value of on-state resistance $R_{ds,on}$ currently available in the market are experimentally characterized in this chapter. These devices, i.e. the OptiMOS 3 Fast Diode (FD) Si power MOSFET [80] and the EPC 2047 GaN e-FET [124], are identified as the best candidates for realizing efficient and compact M/ML inverters in the application areas of interest.
The conduction performance of both DUT (excluding the dynamic $R_{ds,on}$ phenomenon of the GaN e-FET) is comparable and in good agreement with the information provided in the respective datasheets. From the thermal point of view, given the better thermal conductivity of its package, the Si MOSFET is able to dissipate five times more power than the GaN e-FET for the same case temperature. On the other hand, the GaN e-FET offers from three to six times lower switching losses, mostly originating from its smaller parasitic output capacitance value, which results in higher voltage switching speeds. Additionally, an undesired switching behavior of the considered Si MOSFET is observed; after analyzing the internal structure of the device, this loss phenomenon is clarified, and proven to be eliminated in research samples of next generation Si devices, which are also analyzed experimentally.
In the last section, the described experimental results are combined in the performance analysis of a hard-switching half-bridge operated as single-phase inverter, enabling a comparison of the two DUT in a real converter application. Moreover, a sensitivity analysis is performed to separately evaluate the influence of the different device parameters on the overall converter performance: a reduction of the parasitic output charge has the most significant impact on the converter efficiency at switching frequencies above 100 kHz, whereas better cooling performance increases the converter output power rating. In general, considering a typical switching frequency of modern hard-switching topologies, i.e. 140 kHz, the Si-based (OptiMOS 3 FD) half-bridge offers higher power ratings (500 W) with lower efficiencies (97 %), while, at the contrary, the GaN-based (EPC 2047) design, ensures ultra-high efficiencies (99 %), but at lower power ratings (250 W).

7

Analysis and Design of 1200 V SiC Planar Interconnection Power Modules for Next-Generation Electric Aircraft

This chapter summarizes the most relevant findings in the context of research on a new 1200 V SiC power module, which are also published in:

- **M. Guacci**, D. Bortis, I. F. Kovačević-Badstübner, U. Grossner, and J. W. Kolar, "Analysis and Design of a 1200 V All-SiC Planar Interconnection Power Module for Next Generation More Electrical Aircraft Power Electronic Building Blocks," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 4, pp. 320–330, 2017.
- O. Raab, **M. Guacci**, A. Griffo, K. Kriegel, M. Heller, J. Wang, D. Bortis, M. Schulz, and J. W. Kolar, "Full-SiC Integrated Power Module Based on Planar Packaging Technology for High Efficiency Power Converters in Aircraft Applications," in *Proc. of the 11th International Conference on Integrated Power Electronics Systems (CIPS)*, Berlin, Germany, 2020.

Motivation

Low parasitics power stages are essential to fully exploit the unprecedented performance of WBG power semiconductors, e.g. to maximize their switching speeds without compromising the converter system lifetime. Planar interconnection technologies and integrated buffer capacitors are possible solutions to improve the performance of SiC power modules.

Executive Summary

Compact, light-weight, and efficient Power Electronic Building Blocks (PEBBs) are fundamental for the electrification of future aircraft. Core elements of modern PEBBs are power modules (PMs) employing solely SiC MOSFETs. However, in order to take advantage of the high switching speed enabled by SiC power semiconductors, novel PM concepts must be investigated. Low inductance planar interconnection technologies, integrated buffer capacitors and damping networks are possible solutions to mitigate switching overvoltages and oscillations at the switch node caused by the high switching speeds of SiC MOSFETs, ultimately enabling the realization of high efficiency and reliable SiC PM for MEA applications. In this chapter, the analysis and the design of novel ultra-low inductance 1200 V SiC PMs featuring an integrated buffer-damping network are discussed. First, a scaled PM prototype is described and characterized with impedance measurements. Then, a general optimization procedure guiding the sizing of the integrated components is presented, and measurements are performed to verify the analysis. Afterwards, the design and optimization of a full-scale PM, featuring an integrated buffer-damping network, are outlined. To conclude, switching waveforms are measured during operation of the second PM, proving the performance improvement enabled by the low inductance design and the derived procedure.

7.1 Introduction

The MEA concept targets the replacement of mechanic, pneumatic, and hydraulic systems of commercial aircraft with electric power converters and actuators, aiming for decreased fuel consumption and/or emissions reduction, as well as increased reliability and/or lower maintenance effort [136]. The turning point of this trend can be traced back to 2010, when the milestone of 1 MVA of electric power was reached on-board of the *Boeing* B787. An electric power requirement of 1.6 MVA is planned for the next generation of aircraft [137], motivating the increased interest of the power electronics community in MEA. In particular, the *Horizon2020* European Project 636170 - *Integrated, Intelligent Modular Power Electronic Converter* (I2MPECT) [138], building on the expertise in device packaging, thermal management, converter design, and reliability analysis of European industry and academia, intends to demonstrate significant advances in terms of power-to-weight ratio and efficiency of Power Electronic Building Block (PEBBs) for MEA. The primary goal is the realization of a $> 98\,\%$ efficient 3-Φ inverter with the specifications indicated in **Tab. 7.1**, achieving a gravimetric power density of 10 kW/kg, three times higher than nowadays available solutions [110].

Tab. 7.1: Electrical specifications of the I2MPECT PEBB.

	Description	Value
V_{dc}	input DC voltage	540 V… 700 V
f_{sw}	switching frequency	30 kHz
$V_{out,RMS}$	RMS AC output voltage	115 V
$I_{out,RMS}$	RMS AC output current	130 A
P_{out}	AC output power	15 kVA
f_{out}	output frequency	400 Hz… 2 kHz

PEBBs, i.e. power converter modules with defined functionality and simplified interfaces, employing switching stages based on power modules (PMs) using solely SiC semiconductors, can push the already strict requirements concerning compactness and light-weight established in the aircraft industry even further, while still enabling reduced complexity and costs. The PEBBs approach reduces the engineering effort both in the design and in the maintenance phase of a power electronic system, while SiC intrinsic qualities, e.g. higher switching speed, lower on-state voltage, and improved temperature withstanding capability allow a reduction of losses, output filter downsizing, and lower cooling requirements [139]. However, in order to guarantee the reliability of PEBBs, and to fully utilize the performance of SiC MOSFETs, an ultra-low inductance PM designs is required. In fact, parasitic inductances, in combination with the enabled high switching speed, could cause significant overvoltages and undesired ringing [140], ultimately compromising the lifetime of the PM and increasing its electromagnetic (EM) noise emissions [141]. To explore the state-of-the-art in terms of commutation loop inductance L_{CL} of 1200 V SiC PMs [142–146], a comprehensive analysis of commercially available PMs is conducted (see **Tab. 7.2**). Most of nowadays available designs employ bond wires to interconnect the dies and feature L_{CL} values in the range of 5 nH to 10 nH. In order to allow a fair comparison between PMs, a FoM, defined as

$$\mathrm{FoM} = \left(\frac{R_{ds}\, I_{ds}^2}{V_{dc}\, I_{ds}}\, 100\, \frac{L_{CL}}{1\,\mathrm{nH}} \right)^{-1}, \tag{7.1}$$

is calculated for the analyzed PMs, and as well reported in **Tab. 7.2**. The lower limit of L_{CL} only slightly reduces if research prototypes are considered [147–151]. Differently, when planar interconnection technologies are

Tab. 7.2: Commutation loop inductance of commercially available 1200 V SiC PMs.

Power Module		I_{ds}	$R_{ds,on}$	L_{CL}	FoM
Manufacturer	**Part Number**	@ T_j = 175 °C	@ T_j = 25 °C		
Cree	CAS325M12HM2	444 A	3.7 mΩ	5 nH	1.46
Infineon	FF6MR12W2M1	200 A	5.6 mΩ	8 nH	1.34
Microsemi	MSCMC120AM03CT6LIAG	631 A	2.5 mΩ	3 nH	2.53
Rohm	BSM300D12P2E001	300 A	7.3 mΩ	13 nH	0.42
Semikron	SKM250MB120SCTE2	249 A	7.5 mΩ	6 nH	1.07

Tab. 7.3: Commutation loop inductance of SiC PMs featuring planar interconnections.

Research Facility		V_{dc}	I_{ds}	L_{CL}
Fraunhofer IZM	[155]	-	-	0.9 nH
Semikron	[156]	1200 V	400 A	1.4 nH
University of Grenoble	[141]	1200 V	144 A	< 2 nH
University of Nottingham	[158]	2500 V	-	< 2.6 nH
University of Tennessee	[159]	1200 V	-	2.6 nH

adopted [152, 153], i.e. bond wires are replaced by wide coplanar structures [154], L_{CL} can be reduced below 2 nH [155, 156] (see **Tab. 7.3**). PMs featuring this solution provide benchmarks for the next generation of PMs. Additionally, planar interconnection technologies facilitate symmetric designs and enable double-sided cooling [141, 157] aiming towards an even increased power density. A second measure enabling the full utilization of SiC high switching speed is the integration of a buffer capacitor into the PM. It allows the decoupling of L_{CL} from the parasitic inductance L_{ext} of the connection between the PM and the external input filter capacitor [147]. If a sufficient amount of capacitance is selected, the current during the switching transient is provided from the integrated capacitor, and only the portion of inductance inside the PM L_{CL} experiences a fast current variation $^{di}/_{dt}$ [160], mitigating the overvoltage. On the other hand, the paralleling of the buffer capacitor with the external capacitor introduces an undamped resonance network. Therefore, in order to prevent prolonged oscillations, a suitable damping network must be additionally integrated.
Ultimately, the sizing of the buffer capacitor and of the optimized damping network result from a trade-off between required volume and effectiveness of the solution. Moreover, the impact of parasitic inductances, e.g. L_{CL} and L_{ext},

on the performance of the buffer-damping network is not known in advance, and therefore a widely applicable approach is desired. Accordingly, the focus of this chapter is first on the design and experimental analysis of SiC PMs with half-bridge arrangement featuring planar interconnections; second, on the design procedure for an optimized integrated buffer-damping network with low sensitivity towards parasitic inductance.
In order to experimentally validate the benefits enabled by a low inductance PM design and explore its limit, the PM prototype shown in **Fig. 7.1(a)**, featuring a planar interconnection technology, is characterized in **Section 7.2**. The effectiveness of an integrated buffer capacitor against overvoltage is proven with measurements in **Section 7.3**. Subsequently, in **Section 7.4**, the optimization of a damping network is discussed, and its performance is analyzed. Afterwards, a guideline for the design of an integrated buffer-damping network is described in **Section 7.5**. In **Section 7.6**, a second PM, based on the discussed prototype, is designed and optimized to achieve an efficiency higher than 98 % at the operating point specified in **Tab. 7.1**; afterwards, switching waveforms are presented, proving the performance improvement enabled by the low inductance design. Finally, conclusions are drawn in **Section 7.7**.

7.2 Ultra-Low Inductance Power Module

The one-to-one replacement of Si MOSFETs and IGBTs in PMs with SiC MOSFETs does not allow the full exploitation of their performance: the enabled high switching speed, in fact, sets more severe constraints on the values of parasitic elements that can be tolerated. Therefore, new challenges during the design phase of SiC PMs must necessarily be faced.
In this section, the PM prototype shown in **Fig. 7.1**, serving as test platform for the design of the integrated buffer-damping network, is characterized, stressing the importance of the placement of the dies and of the interconnection technology in order to achieve an ultra-low inductance design. Considerations are deliberately limited to a basic but modular half-bridge structure (i.e. only one die per switch), designed for the specifications reported in **Tab. 7.1** but for one sixth of the power rating. The design of the full-scale PM is discussed in **Section 7.6**, building on the acquired knowledge.

7.2.1 Planar Interconnection Technology

The PM shown in **Fig. 7.1** consists of two *Cree* CPM2-1200-0025 SiC dies [161] (4 mm × 6.4 mm) connected in bridge-leg configuration by a planar intercon-

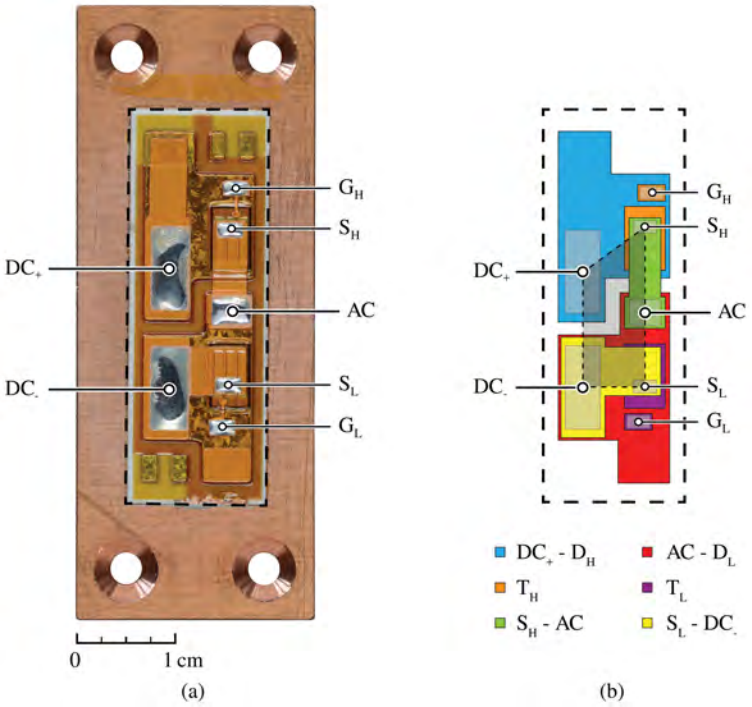


Fig. 7.1: (a) Prototype of the designed PM including two 1200 V SiC power MOSFETs. The solder pads for gate (G_L, G_H) and Kelvin source (S_L, S_H) connections are highlighted, as well as the DC and AC terminals of the half-bridge. **(b)** Structure of the PM clarified with colors: the planar interconnections (green and yellow) and the substrate Cu layer (blue and red) enable an ultra-low inductance design. The area of the average commutation loop is highlighted.

nection technology [152]. At the core of this technology, a thin insulation material separates the Cu substrate from a second metal layer. The former is realized through photo-lithography, while the latter is obtained by a Cu electro-deposition process. The insulation material between them is applied in an additive printing process, and allows for high operating temperatures, i.e. well above 150 °C. The SiC MOSFETs are attached to a Si nitride (Si_3N_4) active metal brazed (AMB) substrate by a pressure assisted silver sintering process. Moreover, the PM is covered only with a top-insulation film as final coating to provide a terminal protective layer against electric arcing, dirt and

humidity, thus there is no need for the conventional Si gel.
In **Fig. 7.1(b)**, the arrangement of dies and the terminals are highlighted. The high-side MOSFET T_H (orange) is sintered on the top (blue) Cu substrate (300 µm thick) connecting its drain D_H (on the back-side of the die) to the positive supply terminal DC_+. Similarly, the low-side MOSFET T_L (purple) is sintered on the bottom (red) substrate Cu layer connecting its drain D_L to the AC output. The source contacts of the MOSFETs (S_H and S_L on the top-side of the dies) are connected depositing the Cu layer forming the planar interconnections (100 µm thick) from S_H to AC (green) and from S_L to DC_- (yellow). A 50 µm thick polyamide-base material isolates the substrates from the interconnections.
Because of the selected technology, only one Cu layer is available, therefore it is not possible to overlap yellow and green connections aiming to a vertical design which would yield to an even lower L_{CL} [154]. The area of the horizontal commutation loop (highlighted in gray), including the DC terminals and the MOSFETs, is minimized, whereas the distances are only constrained by the manufacturing process and/or isolation requirements. The overall size of the Al_2O_3 ceramic substrate (dashed in **Fig. 7.1(a)** and **(b)**) results as 39.4 mm × 13.8 mm with an overall maximum thickness of 1.3 mm.

7.2.2 Commutation Loop Inductance

In order to verify the effectiveness of this design solution, L_{CL} is characterized with multiple impedance measurements performed with a precision impedance analyzer [162]. More in detail, when both MOSFETs are conducting, the circuit seen from the DC terminals of the PM can be approximated by a *RL* series connection, where $R = 2\,R_{ds,on}$ and $L = L_{CL}$. Differently, when both MOSFETs are in the blocking state, the impedance resemble a *LC* series connection, where $L = L_{CL}$ and

$$C = \frac{1}{2}\left(\frac{C_{gs}\,C_{gd}}{C_{gs}+C_{gd}} + C_{ds}\right) = \frac{1}{2}\left(C_{oss} - \frac{C_{rss}^2}{C_{iss}}\right) \tag{7.2}$$

is defined by the parasitic capacitances of the two SiC MOSFETs connected in series (neglecting C_p in **Fig. 7.3**). The impedance of ideal *RL* and *LC* equivalent circuits are analytically calculated in the frequency domain, and the values of *R*, *L* and *C* are selected in order to best approximate the measured curves, as shown in **Fig. 7.2**. The value of $R_{ds,on}$ is additionally measured during the conduction of a DC current where, in accordance with [161], approximately 25 mΩ results for each MOSFET; moreover, inserting in (7.2) the values of

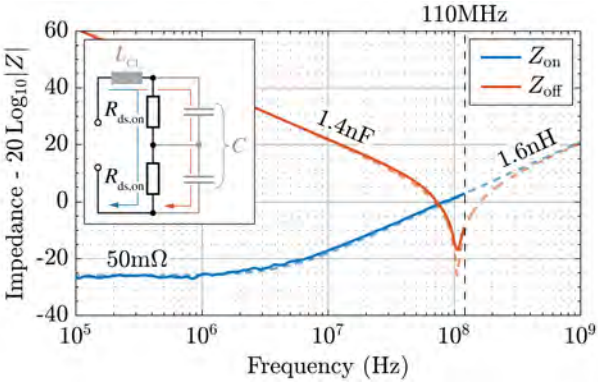


Fig. 7.2: Impedance measured from the DC terminals of the PM shown in **Fig. 7.1** when both MOSFETs are conducting (blue) or blocking (red). Series *RL* and *LC* equivalent circuits (dashed) with the component values given in the figure match the measurements, respectively. For frequencies higher than 110 MHz, only the simulated curves converging to $L_{CL} = 1.6$ nH are shown.

the parasitic capacitances specified in [161] for $v_{ds} = 0$ V, an equivalent capacitance $C = 1.4$ nF results as expected. Even if the frequency measurement range of the used instrument is limited to 110 MHz, the analytical curves clearly converge to the extrapolated value of $L_{CL} = 1.6$ nH.

7.2.3 Gate Loop Inductance

The connection from the PM to the gate driver plays an important role in the shaping of the voltage and current waveforms during a switching transient. In a first approximation, the path from the driver to the gate connection on the die can be represented with the inductance L_g shown in **Fig. 7.3**. Intuitively, L_g limits the change of the gate current, reducing the bandwidth of the driver. This consequently increases the delay time and the current rise time, ultimately increasing the switching losses [163].
Additionally, the charging process of C_{gs} excites a resonance at $f_g = 1/2\pi\sqrt{L_g C_{gs}}$ and, in order to limit v_{gs} below the gate voltage rating of the MOSFET, a lower boundary for the gate resistance $R_{g,lim}$ is set. $R_{g,lim}$ is proportional to L_g, but while being effective in damping the resonance, it also limits the maximum switching speed.
Based on the premises above, it is clear that the minimization of the gate connections length should be of main concern for the design of a PM. The in-

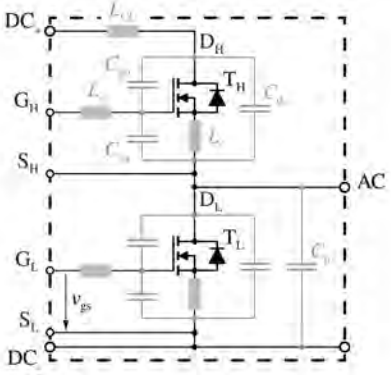


Fig. 7.3: Equivalent circuit of the PM, including the internal parasitic capacitances of the SiC power MOSFETs, and the parasitic inductances associated with the interconnections.

tegration of the gate driver into the PM is only ideally a valid option, because it requires additional effort, leads to higher costs and size, and increases the failure rate of the PM [164]. Short, wide and coplanar connections are more realistically advised as best practice. For convenience, however, gate and source terminals are typically routed all together and next to each other to one side of the PM. Adopting this approach, the value of L_g can easily reach 30 nH [147], resulting in the mentioned drawbacks.
Additionally, if the connection to the source of a MOSFET is partially shared between gate driver and bridge-leg, a fraction of L_g (L_s in **Fig. 7.3**), known as common source inductance, is shared with the path defining L_{CL}. Consequently, a change on i_{ds} directly affects v_{gs} according to

$$v_{gs} = v_{gs,o} - L_s \frac{di_{ds}}{dt}. \tag{7.3}$$

E.g. with a current slope of 10 A/ns, each 100 pH of L_s subtracts 1 V from $v_{gs,o}$ during a turn-on transition, providing a negative feedback reducing the switching speed. This issue is well known and can be avoided splitting the power source and the gate source connections, i.e. using a Kelvin source. It is less transparent, instead, that even if L_g and L_{CL} are physically independent, the magnetic coupling $M_{g,CL}$ between them basically plays the same role as L_s. Although it is difficult to experimentally quantify the impact of $M_{g,CL}$ on v_{gs}, it is important to be aware of its consequences once the gate driver is arranged in close proximity of the PM.

In the considered PM, gate and Kelvin source solder pads are directly accessible from the top of the dies (G_L, G_H and S_L, S_H indicated in **Fig. 7.1 (a)**). In particular, S_H directly contacts T_H and is separated from the Cu interconnection carrying the current to AC (yellow); the same applies for S_L, separated from DC-. Short and wide Cu connections are used to connect the solder pads to the driver, reducing L_g to only 6 nH. In this way, low values of R_g could be selected, achieving high switching speeds, therefore minimizing the switching losses, without the risk of damaging the gate dielectric. With the aim of further reducing L_g, a solution featuring overlapping gate connections on a flexible PCB could be used.

7.3 Integrated Capacitive Snubber

The amount of capacitance at the DC-side of a converter C_{dc} can vary in a wide range depending on the power rating and input voltage V_{dc}, and it typically results in a bulky structure (e.g. $C_{dc} \approx 100\,\mu F$ in the considered setup) that hardly finds place in the closest proximity of the switching stage, i.e. the PM. The inductances of the conductors connecting C_{dc} to the DC terminals of the PM significantly contribute to the total power loop inductance $L_{PL} = L_{ext} + L_{CL}$. In particular, its ideal lower boundary is limited by the parasitic inductance of C_{dc} (ESL), typically in the order of 10 nH to 20 nH. A significant L_{ext} vanishes the benefit of a low inductance PM design, therefore a possible solution, i.e. the integration of a buffer capacitor into the PM, is analyzed in this section.
The circuit supporting the first part of the following explanation is shown in **Fig. 7.4(a)**. It represents the PM of **Fig. 7.1** (dashed box) connected in a Double Pulse Test (DPT) setup and simplified for the case of a hard turn-on switching transition of the high-side MOSFET T_H. The parameters of the DPT setup and the values of the parasitic elements introduced in **Fig. 7.4(a)** are summarized in **Tab. 7.4** (herein $L_{ext} = 15$ nH and $R_g = 1.5\,\Omega$ if not differently specified).
A current step through L_{ext}, originating from the switching transition, excites the resonance between L_{PL} and C_o ($C_{dc} \rightarrow \infty$). C_o represents the parallel connection of the output capacitance C_{oss} of the low-side MOSFET T_L with the parasitic capacitance of the PM from the switch node to DC- (see C_p in **Fig. 7.3**). While the latter depends only on the geometry of the PM ($C_p = 45$ pF is assumed), C_{oss} is non-linear, i.e. $C_{oss}(v_{ds})$; however, in order to best model the resonance occurring on a DC voltage bias, $C_{oss}(V_{dc}) = 215$ pF [161] is considered. This results in $C_o = 260$ pF.
The frequency-dependent parasitic resistance $R_{ac}(f) > R_{ds,on}$ of the $L_{PL}C_o$

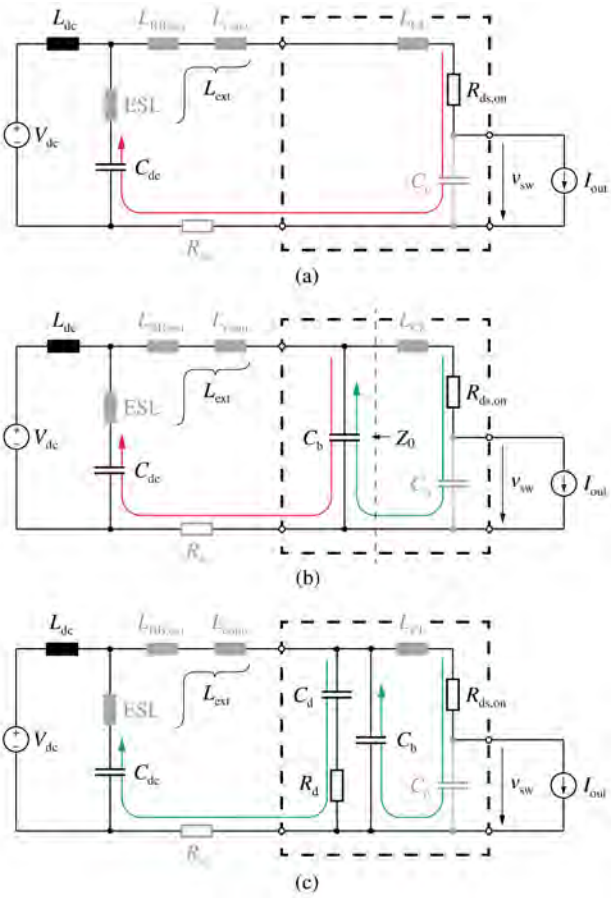


Fig. 7.4: Equivalent circuit of the analyzed half-bridge during a hard turn-on switching transition. In **(a)**, the high frequency current components excited from the switching transition flow through L_{ext}, leading to overvoltage across the low-side MOSFET T_L. With the integration of C_b into the PM **(b)**, the high frequency currents (green) are confined, but a resonance between L_{ext} and C_b is created. In **(c)**, a damping network R_dC_d is additionally integrated. Z_o indicates the output impedance of the input filter.

resonant network, typically much smaller than its characteristic impedance, i.e. $\sqrt{L_{PL}/C_o} \approx 8\,\Omega$, is the only damping element present. Consequently, a voltage spike and a prolonged oscillation at the voltage v_{sw} across T_L occurs,

Tab. 7.4: Parameters of the DPT setup and parasitic elements of the PM.

	Description	Value
V_{dc}	input DC voltage	540 V
L_{dc}	input inductor	1 mH
C_{dc}	external film capacitor	94 µF
T_H, T_L	*Cree* CPM2-1200-0025	
I_{out}	switched output current	30 A
v_{gH}	T_1 gate driver voltage	V_{on} = 20 V
v_{gL}	T_2 gate driver voltage	V_{off} = −5 V
R_g	gate resistance	1.5 Ω or 5 Ω
L_g	parasitic gate inductance	6 nH
C_b	buffer capacitor	0…24 nF
C_d	damping capacitor	0…24 nF
R_d	damping resistor	0.5 Ω… 4.7 Ω
$R_{ds,on}$	high-side MOSFET on-state resistance	25 mΩ
R_{ac}	frequency-dependent resistance	0.2 Ω… 0.7 Ω
C_o	switch node parasitic capacitance	260 pF
L_{CL}	commutation loop in the PM	1.6 nH
L_{conn}	PM connectors	6 nH
$L_{BB,ext}$	from PM connectors to C_{dc}	0 nH or 20 nH
ESL	C_{dc} parasitic inductance	9 nH
L_{ext}	L_{conn} + $L_{BB,ext}$ + ESL	15 nH or 35 nH

as shown in blue in **Fig. 7.5**. v_{sw} reaches $v_{sw,pk}$ = 896 V, more than 300 V above V_{dc}, and strongly oscillates when R_g = 1.5 Ω.
This waveform provides other information on the parameters of the equivalent circuit of **Fig. 7.4(a)**. Knowing C_o, L_{PL} can be calculated from the resonant frequency $f_{tot} = 1/2\pi\sqrt{(L_{CL}+L_{ext})C_o}$ = 77 MHz, and 16.6 nH results as expected ($L_{PL} = L_{ext} + L_{CL}$ = 15 nH + 1.6 nH).
Additionally, analyzing the exponential decay of the overvoltage envelope

$$v_{sw,env}(t) = V_{dc} + (v_{sw,pk} - V_{dc})\, e^{-t/\tau}, \tag{7.4}$$

with a time constant of τ = 48 ns, $R_{ac}(f_{tot})$ = 0.7 Ω results. The value of R_{ac} completes the linear model shown in **Fig. 7.4(a)**, enabling the simulation of the waveforms of v_{sw}; hence, the oscillation after the switching transient and its decay can be compared with measurements. However, correct initial

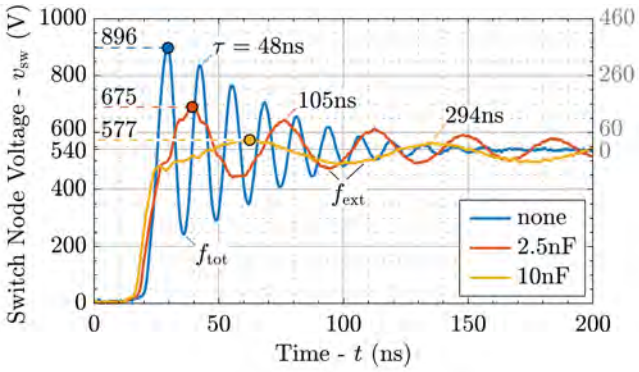


Fig. 7.5: Measured waveforms of the voltage across T_L during hard turn-on switching transitions of T_H (R_g = 1.5 Ω, L_{ext} = 15 nH) with (red and yellow) and without (blue) integrated buffer capacitor C_b. A C_b bigger than 2.5 nF already significantly reduces the peak of v_{sw}, however, without a proper damping network, a prolonged oscillation occurs.

conditions, i.e. the amplitude of the current step $i_{out,pk}$ exciting the resonance, must be set and therefore must be known in advance. For this reason, a measurements-based approach is initially preferred to optimize the buffer-damping network.

With the integration of the buffer capacitor C_b into the PM, as shown in **Fig. 7.4(b)** and **Fig. 7.6**, L_{PL} is split in L_{ext} and L_{CL}, and L_{CL} is minimized. Consequently, the high frequency current components excited during the switching transient are confined in a smaller loop (green in **Fig. 7.4(b)**) and bypass L_{ext}, significantly reducing $v_{sw,pk}$. With the final goal of quantifying the achievable improvements and dimensioning C_b, several experiments are performed.

Two measured waveforms (red and yellow) are shown in **Fig. 7.5** for two different values of C_b, i.e. 2.5 nF and 10 nF. The main resonant frequency is now shifted to $f_{ext} = 1/2\pi\sqrt{L_{ext}C_b} < f_{tot}$ (f_{ext} = 26 MHz and 13 MHz, respectively) because $C_b > C_o$ and $L_{ext} \approx L_{PL}$. Due to the lower resonant frequency, R_{ac} reduces ($R_{ac}(f_{ext}) \approx 0.1\,\Omega \ldots 0.2\,\Omega$), and τ correspondingly increases to 105 ns and 294 ns, prolonging the oscillation. Moreover, connecting C_b, a second resonant network resonating at $f_{int} = 1/2\pi\sqrt{L_{CL}C_{oss}} = 247$ MHz > f_{tot} (because $L_{CL} < L_{PL}$) is formed. The associated oscillation is only partially visible on the waveforms, given the ultra-low inductance design, and the higher value of frequency-dependent resistance. Nevertheless, if needed, it can be damped

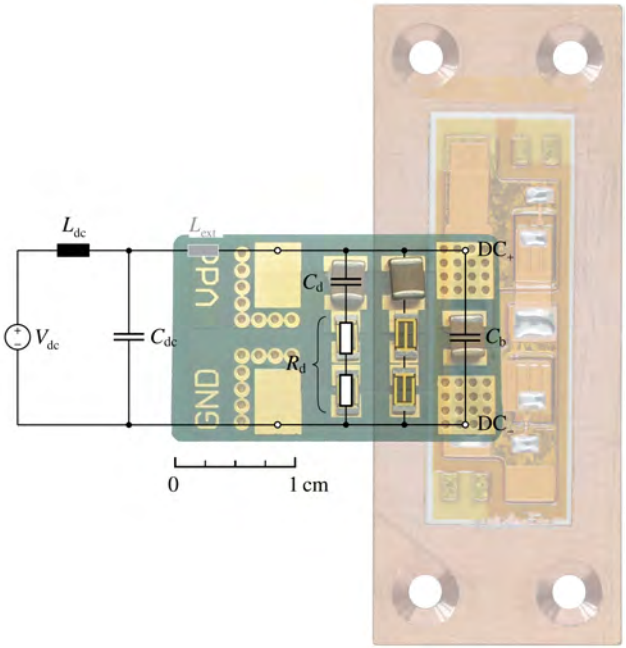


Fig. 7.6: PCB providing a practical and low inductive solution to integrate the buffer capacitor C_b and the damping network R_dC_d into the PM. One undamped and two damped ceramic capacitors find place together with power resistors of different values.

at the AC side of the PM [165]. However, it is worth noticing that, if f_{int} exceeds the parasitic frequency of the output filter, less attenuation might be guaranteed from it.

Fig. 7.5 provides additional information on the effective capacitance of C_b. In this setup, C_b is implemented by connecting one or more ceramic capacitors [166] with values between 4.7 nF and 12 nF in parallel (see **Fig. 7.6**). A reduction of the capacitance, due to the DC voltage offset, is expected and confirmed from the measurements. Knowing L_{ext} and measuring f_{ext}, the effective value of C_b can be calculated in the different cases; the resulting capacitance is always approximately half of the nominal value $C_{b,nom}$. For the sake of clarity, the reported value of capacitance refers to the effective one.

Overvoltage and oscillation can become more severe in case of higher switching speeds or in designs featuring bigger L_{ext}. **Fig. 7.7(a)** summarizes $v_{sw,pk}$ for different combinations of R_g and L_{ext} which, without C_b, have a strong

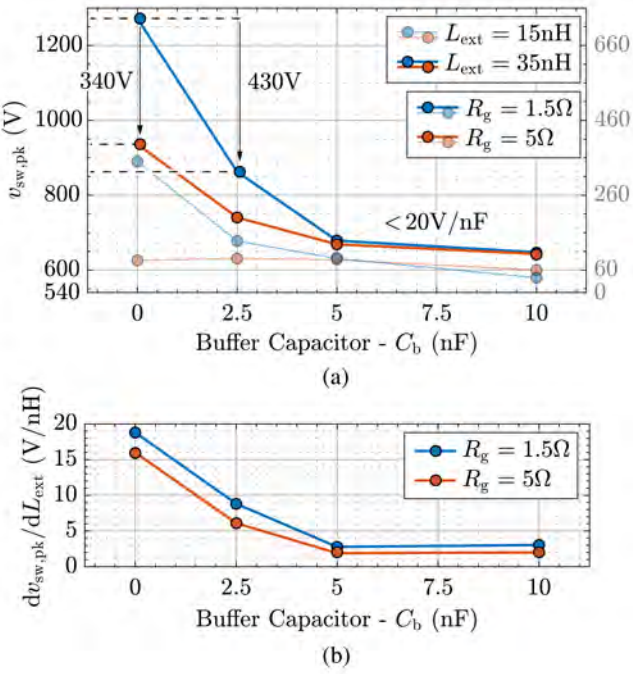


Fig. 7.7: (a) Measured peak of v_{sw} during hard turn-on switching transition of T_H with respect to C_b for four different combinations of L_{ext} and R_g. Without C_b, L_{ext} = 35 nH and R_g = 1.5 Ω cause v_{sw} to exceed the voltage rating of the considered MOSFETs. **(b)** Sensitivity of $v_{sw,pk}$ towards L_{ext}. Without C_b, $dv_{sw,pk}/dL_{ext}$ is above 15 V/nH, while with C_b bigger than 5 nF, it is limited below 3 V/nH in both cases.

influence on $v_{sw,pk}$. As can be noted, L_{ext} = 35 nH and R_g = 1.5 Ω cause v_{sw} to exit the SOA of the MOSFET. Increasing R_g to 5 Ω or integrating C_b = 2.5 nF is almost equally effective against $v_{sw,pk}$. However, the second option guarantees a better trade-off with respect to switching losses [167]. Clearly, the setup featuring smaller L_{ext} (light colors) shows reduced $v_{sw,pk}$ in the same conditions.

C_b = 2.5 nF is sufficient to maintain $v_{sw,pk}$ < 900 V for all the considered combinations. Increasing C_b to 5 nF is only effective on the worst-case, whereas C_b > 5 nF brings no further improvement from this point of view. This is clarified in **Fig. 7.7(b)**, where the sensitivity of $v_{sw,pk}$ towards L_{ext} is plotted. Almost independent of R_g, the sensitivity $dv_{sw,pk}/dL_{ext}$ drops from 15 V/nH

(without C_b) to 3 V/nH ($C_b > 5$ nF). For the rest of the analysis the value of C_b is fixed to 2.5 nF ($C_{b,nom} = 4.7$ nF).
To conclude, it is worth mentioning once again that the performance of this solution, i.e. the integration of C_b, is supported by the ultra-low inductance PM design. For example, assuming $L_{CL} = 15$ nH, it is clear that no value of C_b could reduce $v_{sw,pk}$ below the limit obtained with $L_{ext} = 15$ nH and without C_b integrated into the PM, i.e. 896 V.

7.4 Damping Network Optimization

As discussed in **Section 7.3**, C_b effectively limits $v_{sw,pk}$ and relaxes the design constraints on L_{PL}, but indirectly modifies the impedance of the input filter (Z_o in **Fig. 7.4(b)**) as shown in **Fig. 7.8**. As a consequence, the main resonant frequency, clearly visible from the time behavior of the switch node voltage v_{sw}, is shifted from f_{tot} to $f_{ext} < f_{tot}$. As described in **Section 7.3**, due to the reduction of R_{ac}, less damping is provided and the oscillation is prolonged. Then, with the considered values, f_{ext} enters the regulated EM spectrum negatively affecting the EM noise compatibility of the PEBB. Finally, the ringing of v_{sw} reflects on the current flowing through C_{dc} and degrades its lifetime.
This premise motivates the analysis and the optimization of a damping net-

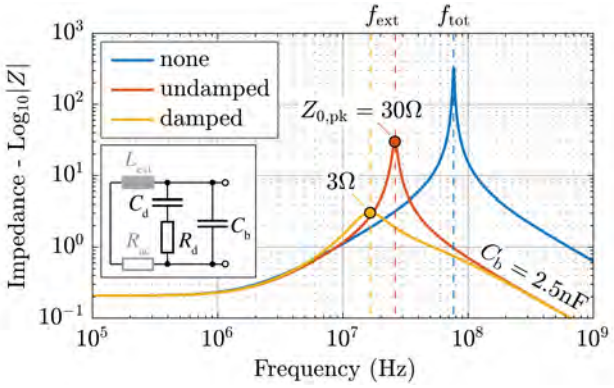


Fig. 7.8: Output impedance of the C_b-R_dC_d network Z_o for $C_b = 2.5$ nF with (yellow) and without (red) the damping network. The optimized damping network ($R_d = 1.5\,\Omega$ and $C_d = 5$ nF) reduces $Z_{o,pk}$ from 30 Ω to 3 Ω according to the specifications. The impedance without C_b seen from the AC terminal is also plotted (blue) to highlight the shifting of the main resonance from f_{tot} to f_{ext}.

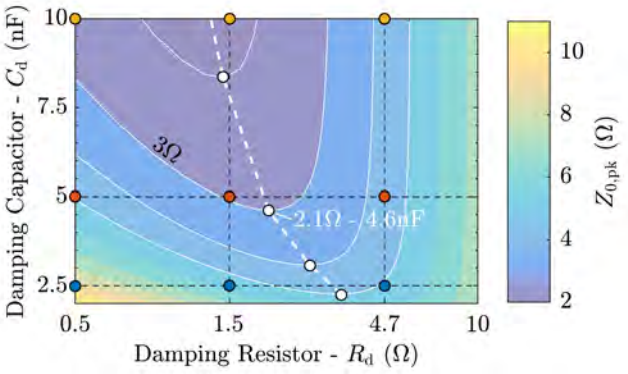


Fig. 7.9: Peak of the output impedance of the buffer-damping network $Z_{o,pk}$ for $0.5\,\Omega < R_d < 10\,\Omega$ and $2\,\text{nF} < C_d < 10\,\text{nF}$. The colored dots highlight the combinations of R_d and C_d whose associated v_{sw} measured waveforms are shown in **Fig. 7.10**. The white dashed line represents the locus of the optimum designs according to [168]. C_b is fixed to 2.5 nF, L_{ext} to 15 nH, and R_{ac} to 200 mΩ.

work presented in this section. Different damping solutions are discussed in literature [168]; the simplest damping approach avoiding steady-state losses is a series R_dC_d network in parallel with C_b [169, 170] (see **7.4(c)** and **Fig. 7.6**). This approach is selected to facilitate the integration into the PM.

In first place, a design procedure should be defined to dimension R_d and C_d, once L_{ext} and C_b are defined. [168] proposes an optimization routine that, given the maximum allowed peak of the buffer-damping (C_b-R_dC_d) network output impedance $Z_{o,pk}$, provides the value for R_d and C_d ensuring optimal damping, i.e. minimizing C_d. This closed form procedure is preferred over an analytical approach [171]. In order to explore the effectiveness of this solution, a wide set of measurements with damping networks featuring different combinations of R_d and C_d is performed, and the results are commented in the following.

Fig. 7.9 shows $Z_{o,pk}$ for different R_dC_d pairs in the range $0.5\,\Omega < R_d < 10\,\Omega$ and $2\,\text{nF} < C_d < 10\,\text{nF}$ with $L_{ext} = 15\,\text{nH}$, $C_b = 2.5\,\text{nF}$, and $R_{ac} = 200\,\text{m}\Omega$. Only three values of R_d (0.5 Ω, 1.5 Ω, and 4.7 Ω) and C_d (2.5 nF, 5 nF, and 10 nF) are considered in the experiments. Thus, the highlighted nine different combinations of R_d and C_d, having values of $Z_{o,pk}$ in the range between 1.8 Ω and 9.4 Ω, are analyzed. The performance of the damping network outside this range rapidly decays. In **Fig. 7.10**, the corresponding measured waveforms of v_{sw} are illustrated.

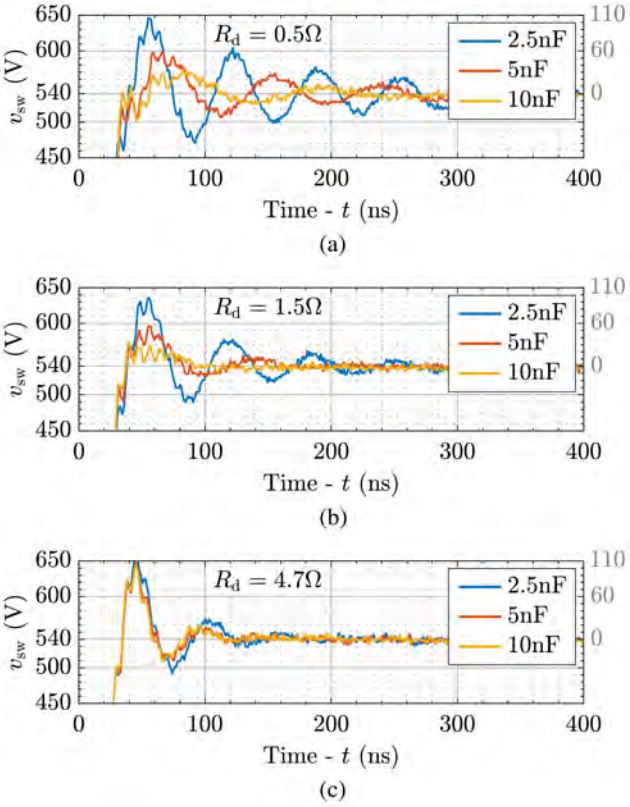


Fig. 7.10: Measured waveforms of v_{sw} for the nine combinations of R_d and C_d indicated with dots in **Fig. 7.9**. In particular: **(a)** $R_d = 0.5\,\Omega$, **(b)** $R_d = 1.5\,\Omega$, and **(c)** $R_d = 4.7\,\Omega$ with $C_d = 2.5$ nF (blue), $C_d = 2.5$ nF (red), and $C_d = 10$ nF (yellow).

Because of the additional capacitance C_d and resistance R_d, $v_{sw,pk}$ is now limited to values below 650 V, even if $C_b = 2.5$ nF is considered. As shown in red in **Fig. 7.10(b)**, $Z_{o,pk} = 3\,\Omega$ (e.g. $R_d = 1.5\,\Omega$ and $C_d = 5$ nF) results to be sufficient to limit $v_{sw,pk}$ below $V_{dc} + 50$ V and to extinguish the oscillation after its first peak in the considered conditions. Correspondingly, **Fig. 7.8** (yellow) shows how the integration of this R_dC_d network reduces $Z_{o,pk}$ from 30 Ω to 3 Ω, effectively damping the resonance. A C_b-R_dC_d network featuring a smaller $Z_{o,pk}$ (yellow in **Fig. 7.10(b)**) does not show significant improvement

Tab. 7.5: Components value for the optimized snubbers with $Z_{o,pk} = 3\,\Omega$.

L_{ext}	C_b	$C_{b,nom}$	C_d	$C_{d,nom}$	R_d
15 nH	2.5 nF	4.7 nF	5 nF	12 nF	1.5 Ω
35 nH	2.5 nF	4.7 nF	10 nF	24 nF	2 Ω

of the damping performance, however, the associated value of C_d increases, complicating the integration.

Fig. 7.10 additionally confirms how $Z_{o,pk}$ is a good indicator of the performance of the damping network. Given the shape of the isolines, **Fig. 7.10(c)** shows three measurements where, even changing the value of C_d, $Z_{o,pk}$ remains between 4 Ω and 5 Ω. As a consequence, the resulting v_{sw} waveforms are similar in the three cases. Differently, the three measurements reported in **Fig. 7.10(a)** cover almost the full range of $Z_{o,pk}$ (i.e. 2.5 Ω... 9.4 Ω) and the performance of the damping network significantly improves from almost ineffective to comparable with the optimized design. Ultimately, the values reported in the first row of **Tab. 7.5** (for $L_{ext} = 15$ nH) are selected.

In **Fig. 7.9**, the locus of [168]-optimum solutions, revisited to consider the influence of R_{ac}, is additionally marked with a white dashed line. As expected, fixed $Z_{o,pk}$, i.e. an isoline, the locus indicates the design featuring minimum C_d. Therefore, an alternative usage of the plot of **Fig. 7.9** consists in finding the value of R_d minimizing $Z_{o,pk}$, once the maximum value of C_d is given, e.g. from volume constraints. The entire optimization procedure is repeated for $L_{ext} = 35$ nH and the values of the resulting components are also reported in **Tab. 7.5** for comparison. Intuitively, a bigger C_d is now required to limit $Z_{o,pk}$ to 3 Ω, given the bigger L_{ext}.

In order to understand the correlation between the optimized designs and the value of L_{ext}, the sensitivity of $Z_{o,pk}$ towards L_{ext} is calculated and the results are reported in **Fig. 7.11**, where the curves are relative to the networks of **Tab. 7.5**. Given the same $C_b = 2.5$ nF, the damping network designed for $L_{ext} = 15$ nH requires only half of the overall capacitance but features four times higher sensitivity compared to the design optimized for $L_{ext} = 35$ nH. Being $Z_{o,pk}$ the FoM of the damping network, depending on the application, the second solution could be preferred. In fact, for the first design, considering 152 mΩ/nH, only 10 nH more than expected result in $Z_{o,pk} = 4.5\,\Omega$ and sub-optimal performance comparable to **Fig. 7.10(b)**. This information is important because L_{ext} is typically unknown to the PM designer who is sizing the C_b-R_dC_d network. Consequently, $Z_{o,pk}$ should be set with a certain margin

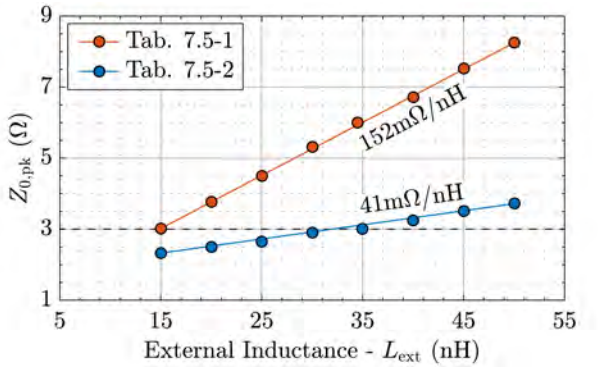


Fig. 7.11: Sensitivity of $Z_{o,pk}$ towards L_{ext} for different [168]-optimized R_dC_d combinations. If the network is designed ($Z_{o,pk} = 3\,\Omega$) for 15 nH (red), the required overall capacitance is less than in the case of 35 nH (blue), however the sensitivity is almost four times higher.

to the desired limit (e.g. $Z_{o,pk} = 1.5\,\Omega$ to obtain $3\,\Omega$ when L_{ext} is 10 nH more than expected), or a worst-case L_{ext} should be considered.
The behavior of the two optimized snubbers (**Tab. 7.5**) is finally examined. The measured peak voltage across R_d amounts to around 50 V in both cases and is therefore not of concern. Differently, the occurring losses could be problematic: in the considered setup, with a switching frequency of 30 kHz, the losses amount to 0.75 W and 1.25 W in the case of $L_{ext} = 15$ nH and 35 nH respectively. Intuitively, a more critical situation (i.e. $L_{ext} = 35$ nH) generates more losses to achieve the same performance. Nevertheless, in both cases a power resistor rated for 2 W [172] can be used, as shown in **Fig. 7.6**.

7.5 Design Procedure Guideline

A guideline of the described procedure for the design of the C_b-R_dC_d network is provided in this section. First, the followed measurements-based approach is considered:

- *Worst Case Conditions*: setup the DPT in the worst-case scenario, i.e. for the highest I_{out}, L_{ext} and L_g, etc.
- *Optimization Constraints*: define the safety margins $v_{gs,max}$ and $v_{sw,max}$. Limit the maximum value of C_b and C_d, i.e. C_{max}, that can be integrated into the PM, e.g. due to limited volume.

- *Buffer Capacitor*: measure $v_{sw,pk}$ after a hard turn-off switching transition of T_L in the DPT setup. Iteratively decrease the value of R_g and increase the value of C_b until the highest switching speed ($R_g = 0\,\Omega$ or $v_{gs} > v_{gs,max}$) limiting $v_{sw,pk} < v_{sw,max}$ with $C_b < C_{max}$ is reached. Further increasing L_{ext} only slightly increases $v_{sw,pk}$.

- *Parasitic Elements*: extract the values of L_{ext} and R_{ac} from the ringing and the damping at v_{sw}.

- *Damping Network*: for given C_b, L_{ext} and R_{ac} calculate Z_o for a defined range of R_d and $C_d < C_{max}$. Plot $Z_{o,pk}$ as a function of R_d and C_d and select the pair R_dC_d minimizing $Z_{o,pk}$.

- *Verification*: $v_{sw,pk}$ is reduced below $v_{sw,max}$ and the oscillation is optimally damped. Measure the losses occurring in R_d to guarantee continuous operation. Further increasing L_{ext} only slightly worsen the damping performance.

If at the end of the procedure the result is too conservative, stricter constraints on $v_{sw,max}$ and C_{max} can be considered and the procedure repeated. A more compact or more efficient, but as well effective, design is obtained. Differently, if the specifications cannot be met, the mentioned constraints must be eased or L_{ext} must be reduced.
A simplified simulation-based approach should be validated in parallel to the entire analysis. The equivalent circuit shown in **Fig. 7.4** can reproduce the damped and undamped measured waveforms of v_{sw} once all parameters are correctly set. While the values of the parasitic elements $R_{ac}(f)$, L_{ext}, and L_{CL} can be entrusted to finite-element simulators, the amplitude of the current step exciting the circuit, i.e. the peak of the switched current $i_{out,pk}$, is unknown. Unfortunately, the free-wheeling diode reverse recovery current peak and capacitive current peak (charging the parasitic capacitances), nonlinear and correlated to the MOSFETs' characteristics and dynamics, add to the load current i_{out}. Therefore, either full confidence is placed on the circuit model of the MOSFETs (when available), or conservative assumptions, based on the MOSFETs datasheet, are necessary. Nevertheless, the analytical approach summarized in **Fig. 7.4(c)** and **Tab. 7.4** is valuable, especially for a preliminary analysis of the problem.
Finally, it is worth noticing that the applicability of the guideline can be generally extended to PMs without integrated buffer capacitors, and to PCB-based converters where C_{dc} does not find place in the closest proximity of the bridge-leg.

7.6 I2MPECT 1200 V SiC Power Module

The PM presented in **Fig. 7.1** serves as basis to test the robustness of the planar interconnection technology, and the switching performance of the SiC MOSFETs and of the integrated buffer-damping network, necessary in the design of the full-scale PM described in this section. The most significant considerations are initially discussed, before analyzing estimated efficiency curves associated with the optimized hardware, and presenting measured waveforms.

7.6.1 Preliminary Considerations

The minimal cooling capability available in the aircraft power bay limits the semiconductor loss budget of each single-phase PM to $150\,\mathrm{W} = 0.01\,P_{\mathrm{out}}/3$, corresponding to a PM efficiency of $\eta = 99\,\%$. Additionally, the minimum switching frequency of the 3-Φ inverter is fixed at $f_{\mathrm{sw,min}} = 30\,\mathrm{kHz}$ to guarantee sufficient control dynamics [113], given the relatively high AC output frequency $f_{\mathrm{out}} = 400\,\mathrm{Hz}$.
The first degree-of-freedom in the realization of the PM is identified in the number N of dies to be connected in parallel to form each switch. For this reason, the estimated conduction losses P_{cond} and switching losses P_{sw} are calculated at the nominal operating point (see **Tab. 7.1**) for different values of N, with $f_{\mathrm{sw}} = f_{\mathrm{sw,min}}$, and considering a sinusoidal output current, i.e. neglecting the high frequency current ripple; in particular,

$$P_{\mathrm{cond}} = \frac{R_{\mathrm{ds,on}}(100\,^{\circ}\mathrm{C})}{N}\, I^2_{\mathrm{out,RMS}}, \tag{7.5}$$

is assumed for the conduction losses, while

$$P_{\mathrm{sw}} = f_{\mathrm{out}}\, N \sum_{\forall\, T_{\mathrm{sw}} \in T_{\mathrm{out}}} \left[k_{\mathrm{o}} + \left(k_1 \frac{I_{\mathrm{sw}}}{N} \right) + k_2 \left(\frac{I_{\mathrm{sw}}}{N} \right)^2 \right] \tag{7.6}$$

is derived for the switching losses. In (7.6), an appropriate value of switched current I_{sw} is selected for each switching period T_{sw} from the sampling of the output current i_{out}; thus, the dissipated switching energy E_{sw} is calculated in each T_{sw}, and all contributions in one AC output period T_{out} are summed. Finally, the total switching energy is multiplied with f_{out}, determining P_{sw}. The coefficients $k_{\mathrm{o}} = 154\,\mu\mathrm{J}$, $k_1 = 5.81\,\mathrm{V\,\mu s}$, and $k_2 = 181\,\Omega\,\mathrm{ns}$ are determined experimentally from switching loss measurements performed on the scaled PM. The results of these calculations are reported in **Fig. 7.12**, where also

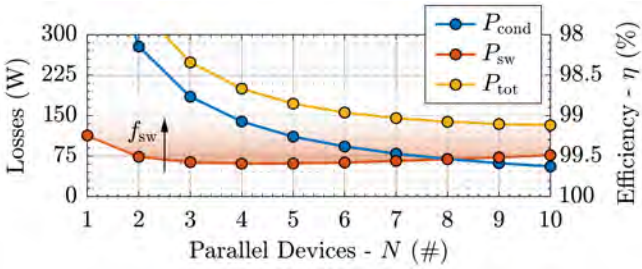


Fig. 7.12: Semiconductor loss breakdown, i.e. conduction losses P_{cond} (blue), switching losses P_{sw} (red) and total losses P_{tot} (yellow), in dependence of the number N of dies connected in parallel to form each switch in the PM.

the total losses $P_{tot} = P_{sw} + P_{cond}$ are indicated (yellow). It is interesting to notice how P_{cond} (blue) drops inversely proportional to N as expected, while P_{sw} (red) features different trends with respect to N (and does not increase proportionally with N), depending on the dominant term in the sum in (7.6). Nevertheless, P_{tot} appears practically flat for $N \geq 6$, hence $N = 6$ is selected to minimize cost and size of the PM. Moreover, with $N = 6$, the loss budget of 150 W is already reached with $f_{sw} = f_{sw,min}$, hence f_{sw} is fixed to 30 kHz. Separate SiC Schottky diodes connected in anti-parallel to the SiC MOSFETs are not considered, since their benefit is not yet proven [173].
The described loss models are considered as well to calculate the expected η of the PM with $N = 6$ for different values of f_{sw} and $I_{out,RMS}$. The results of this procedure are summarized in **Fig. 7.13**. In particular, **Fig. 7.13(a)-(b)** offer a cross-sectional view of the plot shown in **Fig. 7.13(c)** in case of $f_{sw} =$ 30 kHz and nominal output power, respectively. Thus, **Fig. 7.13(a)** provides an indication of the partial load efficiency of the PM, while **Fig. 7.13(b)** highlights how $\eta > 99\,\%$ can be achieved only with $f_{sw} \leq 30$ kHz as expected, which ultimately limits the possible downsizing of the filter elements. A further increase of f_{sw}, e.g. up to 100 kHz, would come at the expense of an efficiency reduction ($\eta = 98\,\%$), i.e. of a higher cooling requirement.
In addition to the described power stage formed by six SiC MOSFETs per half-bridge side, an optimized (according to the procedure described in **Section 7.5**) C_b-R_dC_d network is designed; in particular, three snubber formed by $C_b =$ 33 nF, $R_d = 3\,\Omega$ and $C_d = 9.4$ nF are integrated into the PM. Moreover, the temperature of the PM is measured with two PTC temperature sensors [174], while a shunt resistor [175] is used for measuring the output current. These components, the bus bars, and the contact sleeves are soldered with a lead-

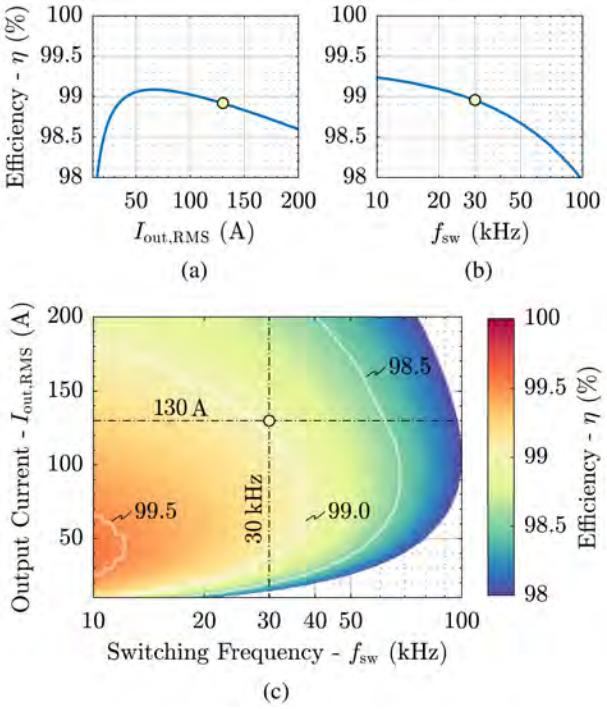


Fig. 7.13: Efficiency η of the optimized PM ($N = 6$) for different values of switching frequency f_{sw} and RMS value of the output current $I_{out,RMS}$. **(a)-(b)** Cross-sectional view of the η-map shown in **(c)** for $f_{sw} = 30\,kHz$ and ($P_{out} = 45\,kW$), respectively.

free soldering process. This process is also applied for attaching the AMB substrate to the Cu baseplate. The final PM design, including all mentioned components is shown in **Fig. 7.14**. The highly symmetric layout aims to evenly distribute the load current between the parallel dies, for conduction and during switching operation. The size of the PM and the requirement to provide input and output terminals at its short sides are constraints originating from the system design.

7.6.2 Gate Driver

Commercial gate drivers for PMs typically offer a single connector to the PM, and are mounted on top of it, hence they suffer from large and asymmetric

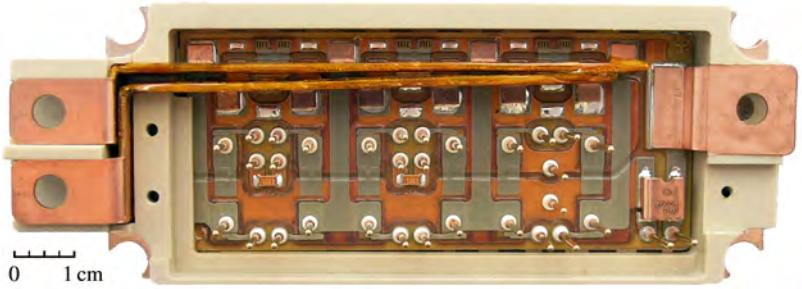


Fig. 7.14: Picture of the I2MPECT 1200 V SiC PM. The DC input and AC output terminals are placed at the opposite short sides. Contact sleeves are used for inserting press-fit pins to contact the gate driver board. The baseplate measures 122 mm×44 mm.

parasitic gate loop inductances, and lead to a significant volume increase. Differently, the designed gate driver circuit is integrated into the housing of the PM, and its functionalities are distributed in two compact PCBs to fully utilize the available space, as shown in **Fig. 7.15**.
The inner board (**Fig. 7.15(a)**) contains two (one per side) isolated gate driver ICs [176], each of them connected to six (one per die) dedicated push-pull current amplifiers [177]. This distributed driving approach ensures symmetric and minimized gate loop inductances. Thus, symmetric current sharing is facilitated also during the switching transitions. Furthermore, high driving currents are obtained, which ultimately enable high switching speeds. The outer board (**Fig. 7.15(b)**) hosts the sensing circuitry, e.g. substrate temperature, output current, and on-state voltage measurements, and other secondary functionalities. Finally, a connector communicates with the external control board, which provides the main supply voltage and the PWM signals.

7.6.3 Double Pulse Test Measurement

To prove the proper functioning of the designed PM, and to reveal the improvement enabled by the integration of the buffer-damping network, DPT measurements are performed on the realized hardware. In the DPTs, $V_{\mathrm{DC}} = 500\,\mathrm{V}$ is selected and I_{out} is increased up to 200 A. The switch node voltage v_{sw} is measured across the high-side MOSFETs. The drain current i_{sw} of the high-side MOSFETs is measured with a Rogowski-coil-based sensor at the DC_+ terminal. An inductor of 140 µH is connected to the AC terminal.
The results of the successful DPTs, performed with and without buffer-

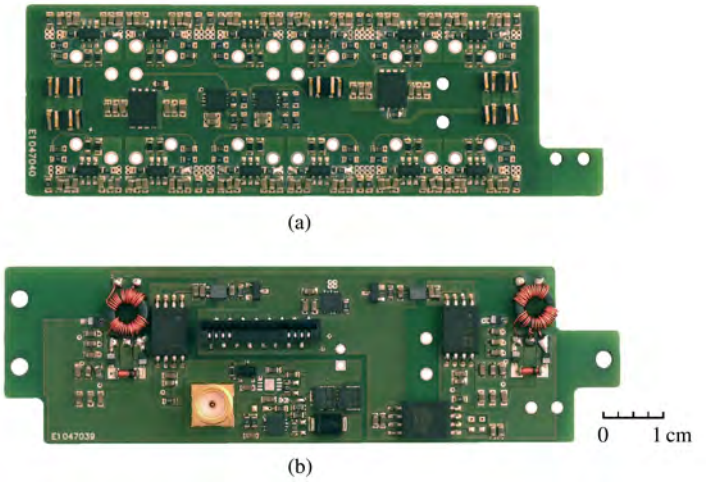


Fig. 7.15: Picture of the gate driver PCBs integrated into the I2MPECT 1200 V SiC PM. **(a)** Inner board containing two isolated gate driver ICs [176], each of them connected to six dedicated push-pull current amplifiers [177]. **(b)** Outer board hosting the sensing circuitry, other secondary functionalities, e.g. gate driver and auxiliary power isolation and generation of the required supply voltage levels, and a connector.

damping network on the same setup, are depicted in **Fig. 7.16**, highlighting how the use of the snubber greatly improves the switching behavior of the PM. The turn-off overvoltage spike is strongly reduced from approximately 300 V to 90 V, i.e. is 70 % lower. Additionally, the switch node voltage oscillation is greatly decreased and fades out in less than 400 ns. This allows to operate the PM with higher voltage safety margins or at higher V_{DC} values, i.e. to reduce the conduction losses, or to switch it at higher switching speeds, thus reducing the switching losses.

7.7 Conclusion

High power conversion efficiency and power density are the key cornerstones supporting the further electrification of air transport. Meanwhile, SiC MOSFETs are emerging as the semiconductors of choice in demanding power electronic applications. Hence, 1200 V SiC PMs for MEA applications, featuring a planar interconnection technology enabling ultra-low inductance designs, are analyzed in this chapter. Despite the low parasitic inductance

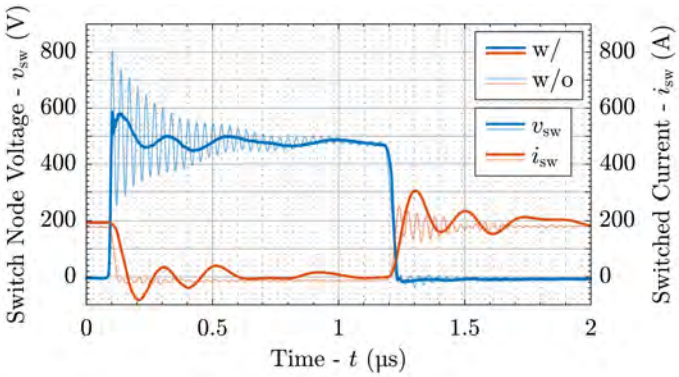


Fig. 7.16: Switched voltage v_{sw} (blue) and current i_{sw} (red) waveforms measured on the PM with integrated gate driver. The figure shows a comparison of switching 200 A (output inductor of 140 µH) at $V_{DC} = 500$ V without and with the three integrated snubbers ($C_b = 33$ nF, $R_d = 3\,\Omega$, and $C_d = 9.4$ nF).

of the designed PMs, the full exploitation of the high switching speeds characteristic of SiC semiconductors requires precautions concerning switching overvoltages and ringing at the switch node. Measurements proved that the integration of a buffer capacitor is generally an effective measure to minimize the drawbacks associated with the parasitic inductance of the connection from the PM to the external DC-link capacitor. Unfortunately, while this solution mitigates the overvoltage, it even aggravates the oscillation. Consequently, the integration of a R_dC_d damping network is recommended. Following this approach, in a limited footprint and with negligible losses, the switching overvoltage peak is significantly reduced and the oscillation is optimally damped. Hence, the designed PMs are operated in the specified conditions without experiencing any undesired effect. This outcome validates the effectiveness of the integrated buffer-damping network, and allows the designers to explore the performance enabled by SiC PMs, facilitating their adoption in MEA, and ultimately providing a best-in-class solution contributing to next-generation environmental friendly aerospace industry products.

Part 3

Next-Generation Converters with Wide-Bandgap Semiconductors

8

Three-Phase Buck-Boost Current Source Inverter System Employing Dual-Gate GaN e-FETs

This chapter summarizes the most relevant findings in the context of research on a three-phase current source inverter system, which are also published in:

- **M. Guacci**, M. Tatic, D. Bortis, Y. Kinoshita, H. Ishida, and J. W. Kolar, "Novel Three-Phase Two-Third-Modulated Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs," in *Proc. of the 7th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Xi'an, China, 2019.
- **M. Guacci**, D. Zhang, M. Tatic, D. Bortis, J. W. Kolar, Y. Kinoshita, and H. Ishida, "Three-Phase Two-Third-PWM Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 4, pp. 339–354, 2019.

Motivation

Power converters employing latest WBG semiconductors achieve unprecedented efficiency and power density targets. The recent development of monolithic bidirectional GaN switches suggests to investigate 3-Φ current DC-link converters, where only a single DC-link inductor is required to generate continuous sinusoidal output voltage waveforms and the bidirectional voltage blocking capability of these devices translates into reduced system complexity.

Executive Summary

Latest dual-gate (2G) monolithic bidirectional (MB) GaN e-mode FETs (e-FETs) enable a performance breakthrough of 3-Φ current DC-link inverters, e.g. in terms of power conversion efficiency, power density, cost, and complexity. In fact, a single 2G MB GaN e-FET can replace the two anti-series connected conventional power semiconductors required in this inverter topology to realize each four-quadrant (AC) switch with bidirectional voltage blocking capability, and allowing controlled bidirectional current flow. Furthermore, in case of 3-Φ buck-boost (bB) current source inverter (CSI) systems comprising a DC-link current impressing buck-type DC/DC input stage and a subsequent boost-type 3-Φ current DC-link inverter output stage, a variable DC-link current control strategy, based on a synergetic control concept, can be applied to significantly reduce the switching losses occurring in the 3-Φ inverter. This strategy is denominated *Two-Third PWM* (2/3-PWM), since by properly shaping the DC-link current with the input stage, the desired 3-Φ sinusoidal load phase currents can be generated by switching, in each switching period, only two out of the three phases of the output stage. Based on comprehensive circuit simulations and analytical calculations, a detailed explanation of the developed modulation and control schemes for different operating conditions is provided, and the reduction of losses enabled by 2/3-PWM is confirmed. Next, the seamless transition of the 3-Φ bB CSI system from 2/3-PWM to conventional 3/3-PWM is demonstrated. Finally, a 3.3 kW 3-Φ bB CSI system, applying 2/3-PWM and employing research samples of 2G MB GaN e-FETs in the 3-Φ inverter, is estimated to achieve an efficiency of 98.4 % and a power density of 18 kW/dm^3 at a switching frequency of 140 kHz.

8.1 Introduction

The 3-Φ voltage DC-link inverter is the industry preferred solution to perform compact and efficient DC/AC energy conversion in VSD and/or grid connected power electronic applications. To comply with the electromagnetic regulations and, in case of VSD, to avoid high frequency losses in the electric machine, insulation stress, and bearing wear-out [178], filter circuits are connected at the output of voltage DC-link inverters to generate continuous output voltage waveforms [179–181]. To limit the size and/or cost of the output filter, but also to increase the control bandwidth of the system, high switching frequencies, e.g. 100 kHz, are employed in VSD. In this context, WBG semiconductors, i.e. GaN and SiC, become key technologies to preserve a high power conversion efficiency, even outperforming conventional (without output filter) low frequency Si based solutions [182]. Additionally, when the

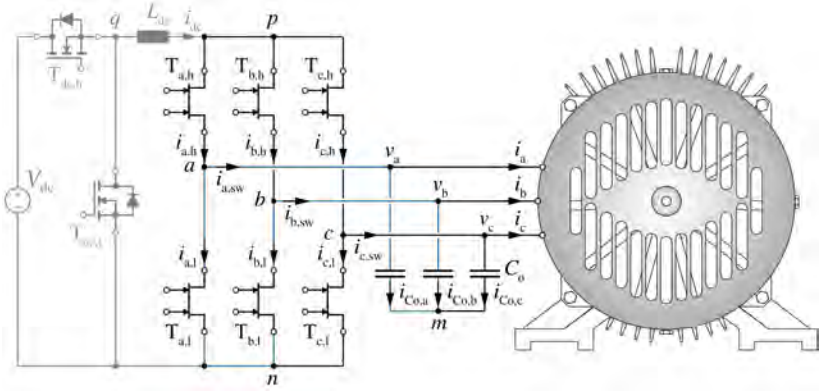


Fig. 8.1: Schematic of the 3-Φ buck-boost (bB) current source inverter (CSI) system analyzed in this chapter. The boost-type 3-Φ current DC-link inverter output stage (black) is formed by six 2G MB GaN e-FETs and connected to an electric machine, as in a VSD application. The buck-type DC/DC converter input stage (gray), connected to a supplying DC input voltage source, introduces the bB functionality, and allows to control and shape the DC-link current i_{dc}.

supplying DC input voltage varies in a wide range, e.g. when it is provided by the traction battery of an EV [183] or by a string of PV panels [184], voltage DC-link inverters are preceded by a boost-type DC/DC converter input stage [109], which regulates the DC input voltage of the 3-Φ inverter. Hence, the so obtained two-stage converter (including the output filter), i.e. a 3-Φ boost-buck (Bb) voltage source inverter (VSI) system, can operate in a wide DC input voltage range, and generate continuous output voltage waveforms, thus fulfilling the requirements of modern DC/AC power converters [109,178]. The functionality of a 3-Φ Bb VSI system can alternatively be achieved with the quasi-dual approach, i.e. the 3-Φ buck-boost (bB) current source inverter (CSI) system [185–187] shown in **Fig. 8.1**. It comprises a DC-link current impressing buck-type DC/DC input stage (gray) and a subsequent boost-type 3-Φ current DC-link inverter output stage (black) [188]. Advantageously, the DC-link inductor L_{dc} forms, in combination with the output capacitors C_o, an integrated output filter; i.e. the 3-Φ bB CSI system naturally generates continuous output voltage waveforms. Nevertheless, this quasi-dual solution is rarely adopted, mainly because of the higher count of power devices. In fact, a 3-Φ voltage DC-link inverter only requires six power semiconductors with unidirectional voltage blocking capability allowing controlled bidirectional

current flow, such as MOSFETs or IGBTs (with external anti-parallel diodes), which are the most widely used power devices. Consequently, VSI systems are often preferred and, especially when WBG power semiconductors are considered, high power conversion efficiencies and extreme power densities can be achieved at any power level [109, 113]. In contrast, a 3-Φ current DC-link inverter requires six power semiconductors with bidirectional voltage blocking capability, such as, e.g. symmetric Gate Turn Off thyristors. However, when design constraints demand switching frequencies above 10 kHz and bidirectional power flow is required without reversing the inverter DC input voltage, these switches are preferably realized by anti-series connecting two discrete components, e.g. two power transistors [189]. This ultimately causes an increase of chip area, cost, driving complexity, and conduction losses, which disfavor CSI systems in comparison with VSI systems.
Nevertheless, the unprecedented performance of WBG devices, enabling a significant reduction of switching and conduction losses compared to Si MOSFETs at a given operating point, stimulates further research on current DC-link converters featuring GaN [190] or SiC [191] power semiconductors. Additionally, recent development in the power semiconductor industry culminated in the realization of monolithic bidirectional [192] (MB) GaN e-mode FET (e-FET) research prototypes [193–196], which feature bidirectional voltage blocking capability and allow a controlled current flow in both directions, i.e. excellently fit the requirements of current DC-link inverters. In particular, ±600 V 26 mΩ research samples of a dual-gate (2G) MB GaN e-FET [197] are available from a major manufacturer of power semiconductors. Preliminary tests on these devices are performed in [198], however, their potential in a 3-Φ bB CSI system still remains unclear.
Beside these new components, other intrinsic characteristics [190] of 3-Φ bB CSI systems motivate the research on this circuit topology. In fact, while voltage DC-link inverters switch a constant voltage and a variable current, the opposite is true for current DC-link inverters. Since the switching losses are typically stronger influenced by the switched voltage than by the switched current [199], lower switching losses might occur in the current DC-link approach for the same processed power [200], eventually resulting in overall higher efficiencies [201]. Moreover, although capacitors (voltage DC-links) have a higher energy storage density than inductors (current DC-links), see **Appendix C**, a lower boundary for the volume of DC-link capacitors is often given by their current rating [202]. Differently, higher switching frequencies, i.e. WBG semiconductors, always enable the downsizing of magnetic components, as lower and lower inductance values can be selected. Additionally, different costs, operating temperature ranges, critical environmental

conditions, failure modes and failure rates are associated with capacitors and inductors. Hence, current DC-link inverters potentially show advantages over voltage DC-link inverters in certain applications.
In this chapter, the operating principle of the 3-Φ bB CSI system is introduced in **Section 8.2**. Ideal waveforms of the 3-Φ inverter support the explanation of a variable DC-link current control strategy denominated *Two-Third PWM* (2/3-PWM) [203–205]. Although the basic principle of 2/3-PWM is originally presented in [204, 205], it is as well briefly summarized in **Section 8.3** to provide a common basis for the subsequent analysis, which focuses on its range of applicability, resulting stress on the circuit components, e.g. switching losses, and operation supported by comprehensive simulation results (also in case of non-unity load power factor and load steps). In particular, analytic calculations, performed in **Section 8.4**, highlight the performance improvement of the 3-Φ inverter enabled by this concept. The developed synergetic control scheme, employed for the 3-Φ bB CSI system, is described in **Section 8.5**, and circuit simulations prove its functioning for different operating conditions. The considered 2G MB GaN e-FET research prototypes are presented in **Section 8.6** and compared to state-of-the-art power semiconductors. A prediction of the efficiency and power density achievable with the 3-Φ bB CSI system precedes **Section 8.7**, which concludes the chapter. Finally, an experimental hardware, designed to evaluate the switching performance of the 2G MB GaN e-FETs, is described, and measured switching waveforms are discussed in **Appendix D**.

8.2 Power Converter Operation

As first step of a comprehensive analysis of the 3-Φ bB CSI system shown in **Fig. 8.1**, its operating range and operating principle are described in this section.

8.2.1 Operating Range

The direction of power flow in the 3-Φ bB CSI system shown in **Fig. 8.1** is defined by the sign of the DC-link current i_{dc}. In fact, since the output voltage of the buck converter v_{qn} is unipolar, i.e. it is limited between 0 V and the supplying DC input voltage $V_{\mathrm{dc}} > 0\,\mathrm{V}$, the local average (over a switching period) of the input voltage of the 3-Φ inverter $\bar{v}_{\mathrm{pn}}$ must be positive to guarantee the controllability of i_{dc}, i.e. the stability of the system. However, still both directions of power flow are possible in the 3-Φ inverter, as it is

sufficient to invert the sign of i_{dc} (and not the one of $\bar{v}_{pn}$, as for a conventional system [206]) to feed power back to the supplying DC input voltage source. Nevertheless, when $\bar{v}_{pn}$ approaches 0 V, i.e. when the peak value $\hat{v}_{out}$ of the sinusoidal output voltages or the load power factor $\cos(\phi)$ of the supplied load are reduced [206], the controllability of i_{dc}, as well as the possibility to invert it, are limited. For this reason, the selected 3-Φ bB CSI system is particularly suited for VSD supplying synchronous machines operated with high power factors or driving passive mechanical loads, e.g. pumps and fans [207], and, in the case of grid connected power electronic applications, for PFC rectifiers and inverters, e.g. future bidirectional EV battery chargers and PV inverters, i.e. for systems typically operating with $\cos(\phi) \approx \pm 1$.
Irrespectively of this limitation, the DC/DC buck-type input stage based 3-Φ bB CSI system (see **Fig. 8.1**) is preferred to back-to-back AC/AC system comprising two DC-side connected 3-Φ inverters [206], to better suite the requirements of voltage DC-link systems and distributed voltage DC-link architectures, becoming more and more prominent in VSD [208].

8.2.2 Input-Output Voltage Gain

The two main control variables of the 3-Φ bB CSI system are the duty-cycle of the buck converter

$$\bar{s}_{Tdc,h} = \frac{\bar{v}_{qn}}{V_{dc}} = \frac{\bar{v}_{pn}}{V_{dc}}, \tag{8.1}$$

where $\bar{v}_{qn}$ indicates the local average over a switching period of v_{qn}, and the modulation index of the 3-Φ inverter

$$m_{dc/ac} = \frac{\hat{i}_{out}}{I_{dc}} = \frac{\bar{v}_{pn}}{\hat{v}_{out,ll}} \frac{2}{\sqrt{3}}, \tag{8.2}$$

if constant $i_{dc} = I_{dc}$ and $\cos(\phi) = +1$ are assumed. In (8.2), $\hat{i}_{out}$ and $\hat{v}_{out,ll}$ correspond to the peak values of the sinusoidal load phase currents i_{out} and sinusoidal line-to-line output voltages $v_{out,ll}$ generated by the 3-Φ inverter, respectively. Combining (8.1) and (8.2), the voltage gain g_v of the 3-Φ bB CSI system can be calculated as

$$g_v = \frac{\hat{v}_{out,ll}}{V_{dc}} = \frac{\bar{s}_{Tdc,h}}{m_{dc/ac}} \frac{2}{\sqrt{3}}. \tag{8.3}$$

Since $0 \leq \bar{s}_{Tdc,h} \leq 1$ and $0 \leq m_{dc/ac} \leq 1$, g_v can assume any positive value, i.e. the bB capability of the system is confirmed.

Although different combinations of $\bar{s}_{\mathrm{Tdc,h}}$ and $m_{\mathrm{dc/ac}}$ result in the same g_{v}, $\bar{s}_{\mathrm{Tdc,h}} = 1$ eliminates the switching losses in the buck converter (since $\mathrm{T}_{\mathrm{dc,h}}$ is permanently on), while $m_{\mathrm{dc/ac}} = 1$ minimizes I_{dc}, and thus the losses of the overall system for a given operating point [209]. Accordingly, these are the preferred values of $\bar{s}_{\mathrm{Tdc,h}}$ and $m_{\mathrm{dc/ac}}$ for a given g_{v}; hence, two operating modes, namely the *Buck-Mode* ($0 \leq \bar{s}_{\mathrm{Tdc,h}} < 1$, $m_{\mathrm{dc/ac}} = 1$) and the *Boost-Mode* ($\bar{s}_{\mathrm{Tdc,h}} = 1$, $0 \leq m_{\mathrm{dc/ac}} < 1$), can be defined [203]. From (8.3), the boundary between the *Buck-Mode* and the *Boost-Mode* can be calculated as

$$V_{\mathrm{dc}} = \frac{\sqrt{3}}{2}\,\hat{v}_{\mathrm{out,ll}}. \tag{8.4}$$

In particular, for $V_{\mathrm{dc}} > \sqrt{3}/2\,\hat{v}_{\mathrm{out,ll}}$, the system is operated in the *Buck-Mode*, whereas, when $V_{\mathrm{dc}} < \sqrt{3}/2\,\hat{v}_{\mathrm{out,ll}}$, the *Boost-Mode* is entered.

8.2.3 Simplified Operating Principle

The 3-Φ bB CSI system shown in **Fig. 8.1** is simplified to the circuit shown in **Fig. 8.2** (cf. **Fig. 13** in [206]) to explain its operation in the *Buck-Mode* and with power flowing from the supplying DC input voltage source to the supplied AC output load. For this purpose, the buck converter and L_{dc} are replaced by a current source $i_{\mathrm{dc}} > 0$, whereas the 3-Φ inverter is represented by two three-position switches $\mathrm{T_h}$ and $\mathrm{T_l}$. The two output terminals tapped by $\mathrm{T_h}$ and $\mathrm{T_l}$ define one state of the 3-Φ inverter out of overall $3^2 = 9$ possibilities;

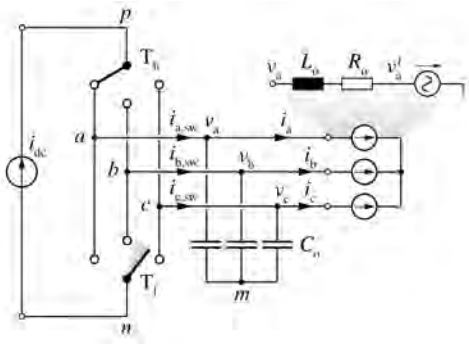


Fig. 8.2: Simplified representation of the 3-Φ bB CSI system shown **Fig. 8.1**. The two three-position switches $\mathrm{T_h}$ and $\mathrm{T_l}$, modulating the DC-link current $i_{\mathrm{dc}} > 0$ by alternately connecting the output terminals *a*, *b* and *c* to the DC-link terminals *p* and *n*, model the operation of the 3-Φ inverter.

e.g. in **Fig. 8.2**, a transition from state [ab] to [ac] is illustrated. The three shoot-through states [aa], [bb] and [cc] are denominated *zero states* in contrast to the remaining six states denominated *active states*. In the *zero states*, the 3-Φ inverter short-circuits the DC-link terminals p and n whereas, in the *active states*, it connects C_o and the load between them. Consequently, depending on the selected state, v_{pn} varies between 0 V (*zero states*) and the six possible $v_{out,ll}$ values, i.e. $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ca}$ (*active states*), while the switching stage output currents $i_{a,sw}$, $i_{b,sw}$ and $i_{c,sw}$ can either assume the value of 0 A (*zero states*) or of $\pm i_{dc}$ (*active states*). Hence, by appropriately switching T_h and T_l, and output filtering (through C_o), i_{dc} can be modulated and transformed into the sinusoidal load phase currents i_a, i_b and i_c.

8.3 Modulation Schemes

Two different modulation schemes, namely conventional PWM (3/3-PWM) and *Two-Third PWM* (2/3-PWM) [203–205] can be applied to the 3-Φ bB CSI system when operated in the *Buck-Mode*. Both approaches are described in this section with the support of idealized waveforms of the 3-Φ inverter, relative to its nominal operating point (see **Tab. 8.1**).

8.3.1 Conventional Pulse-Width Modulation

In the *Buck-Mode* (see **Section 8.2.3**), the buck converter controls i_{dc}, while the 3-Φ inverter is responsible for generating i_a, i_b and i_c. In case 3/3-PWM is applied, i_{dc} is controlled to a constant value I_{dc}. The most significant waveforms of the 3-Φ inverter in these conditions are summarized in **Fig. 8.3(a)**, **Fig. 8.4(a)** and **Fig. 8.5(a)**, where the encircled numbers define the six symmetric $\pi/3$-wide sectors of an AC output period.
In each interval of **Fig. 8.3(a)**, three of the six 2G MB GaN e-FETs forming

Tab. 8.1: Nominal specifications of the 3-Φ bB CSI system shown in **Fig. 8.1**.

	Description	Value
V_{dc}	supplying DC input voltage	400 V
$\hat{i}_{out}$	peak sinusoidal load phase current	11 A
$\hat{v}_{out}$	peak sinusoidal output voltage	196 V
f_{out}	output frequency	50 Hz
P_{out}	output power	3.3 kW

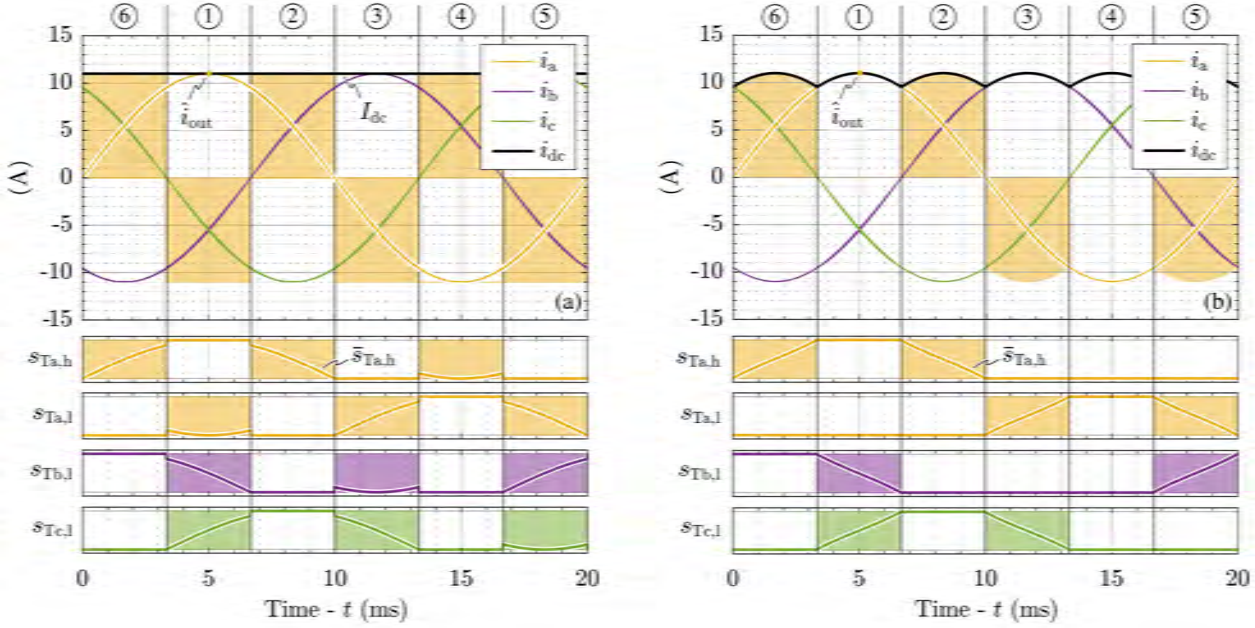


Fig. 8.3: DC-link current i_{dc}, sinusoidal load phase currents i_a, i_b and i_c with peak value $\hat{i}_{out}$, and gate control signals $s_{Ti,j}$ within one AC output period, in case **(a)** 3/3-PWM is applied ($i_{dc} = I_{dc}$) and **(b)** 2/3-PWM is applied ($i_{dc} = \max\{|i_a|, |i_b|, |i_c|\}$). The waveforms are given for the operating point specified in **Tab. 8.1**. The encircled numbers define the six symmetric $\pi/3$-wide intervals of an AC output period. The yellow area in the graphs of i_{out} indicates the switching stage output current of phase a, i.e. $i_{sw,a}$. The colored lines in the graphs of $s_{Ti,j}$ correspond to their local average $\bar{s}_{Ti,j}$ over a switching period. Further details are shown in **Fig. 8.4** and **Fig. 8.5**.

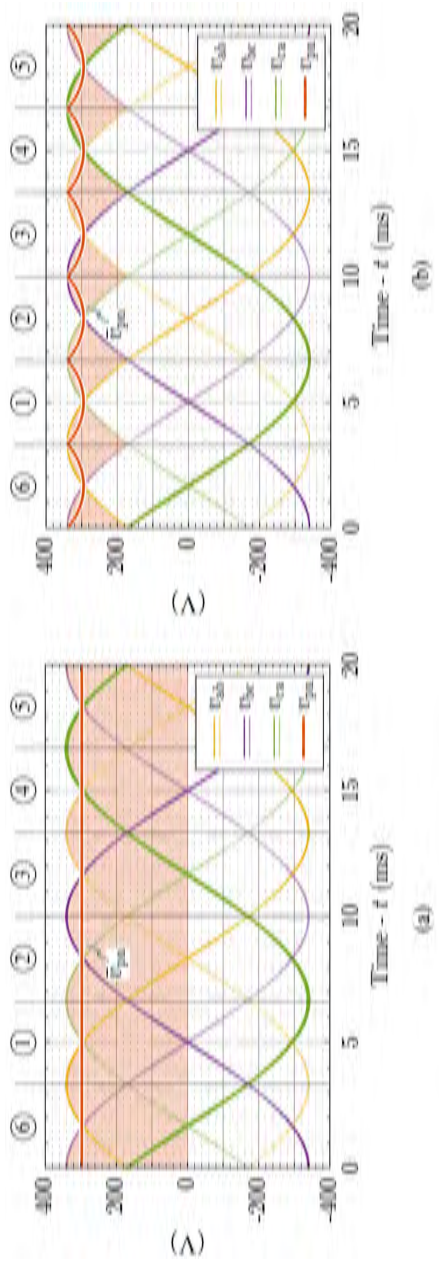


Fig. 8.4: Sinusoidal line-to-line output voltages $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ca}$, and input voltage of the 3-Φ inverter v_{pn} within one AC output period, in case **(a)** 3/3-PWM is applied and **(b)** 2/3-PWM is applied. The waveforms are given for the operating point specified in **Tab. 8.1**. The red lines correspond to the local average input voltage of the 3-Φ inverter $\bar{v}_{pn}$ over a switching period. Further details are shown in **Fig. 8.3** and **Fig. 8.5**.

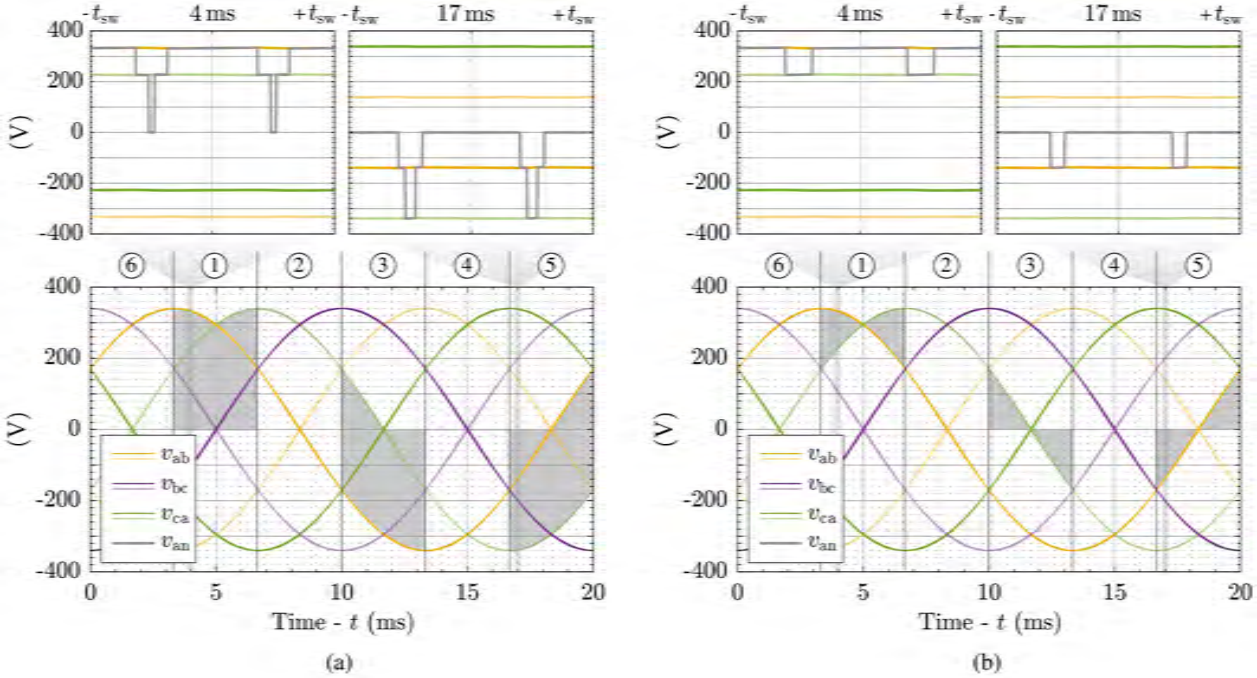


Fig. 8.5: Sinusoidal line-to-line output voltages $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ca}$, and voltage v_{an}, within one AC output period, in case **(a)** 3/3-PWM is applied and **(b)** 2/3-PWM is applied. The waveforms are given for the operating point specified in **Tab. 8.1**. The graphs in the upper part offer a zoomed view of v_{an} (gray) during a switching period. Further details are shown in **Fig. 8.3** and **Fig. 8.4**.

the 3-Φ inverter are operated with PWM, i.e. are switched with switching frequency f_{sw}. For example in sector ①, characterized by $i_a > |i_b|$ and $i_a > |i_c|$, $T_{a,h}$ is permanently on, while $T_{b,h}$ and $T_{c,h}$ are permanently off, and all three low-side switches $T_{i,l}$ are alternately switched within a switching period. In other words, the states [aa], [ab] and [ac] are alternately applied since, as visible in the space vector diagram of **Fig. 8.6(a)**, these are (in this sector) the closest neighbors of the vector of the reference sinusoidal load phase current $\vec{i}^*$, having $|\vec{i}^*| = m_{dc/ac}\, I_{dc} = \hat{i}_{out}$. Hence, $\vec{i}^*$ can be expressed as

$$\frac{\vec{i}^*}{I_{dc}} = \delta_{[aa]} \cdot [aa] + \delta_{[ab]} \cdot [ab] + \delta_{[ac]} \cdot [ac], \tag{8.5}$$

where $\delta_{[xy]}$ indicates the duty-cycle of the state [xy]. Intuitively, all other $\delta_{[xy]} = 0$.
In **Fig. 8.3**, the gate control signal $s_{Ti,j}$ of each 2G MB GaN e-FET $T_{i,j}$, and its corresponding local average over one switching period $\bar{s}_{Ti,j}$ are additionally shown. The conversion from $\delta_{[xy]}$ to $\bar{s}_{Ti,j}$ is immediately deduced from **Fig. 8.2**, and can be expressed as

$$\bar{s}_{Ti,h} = \sum_{y\,=\,a,\,b,\,c} \delta_{[iy]}, \quad \bar{s}_{Ti,l} = \sum_{x\,=\,a,\,b,\,c} \delta_{[xi]} \qquad (i = a, b, c). \tag{8.6}$$

Furthermore, from **Fig. 8.6(a)**, the duty-cycles of the *active states* $\delta_{[ab]}$ and $\delta_{[ac]}$ can be derived from the projections of $\vec{i}^*$ according to

$$\frac{|\vec{i}^*|}{I_{dc}} \begin{bmatrix} \cos\vartheta \\ \sin\vartheta \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} \delta_{[ac]} \\ \delta_{[ab]} \end{bmatrix} \quad (-\pi/6 < \vartheta < \pi/6), \tag{8.7}$$

where ϑ indicates the instantaneous phase angle of $\vec{i}^*$. The remaining fraction of the switching period is accounted for the *zero state*, whose duty-cycle $\delta_{[aa]}$ is calculated as

$$\delta_{[aa]} = 1 - (\delta_{[ac]} + \delta_{[ab]}) = 1 - m_{dc/ac} \cos\vartheta \geq 1 - \cos\vartheta \geq 0. \tag{8.8}$$

It should be noticed in (8.8), that even if $|\vec{i}^*| = I_{dc}$ as given for the *Buck-Mode*, when applying 3/3-PWM, $\delta_{[aa]} > 0$ results (except for the point in time in the middle of ①, i.e. for $\vartheta = 0$, where $\delta_{[aa]} = 0$). Hence, a free-wheeling interval, i.e. an interval during which I_{dc} bypasses the load flowing through $T_{a,h}$ and $T_{a,l}$, is present during every switching period in ①. Since (8.7) and (8.8) can be extended to the other five sectors (from ② to ⑥) based on symmetry considerations, it can be concluded that *zero states* are always necessary when 3/3-PWM is applied, i.e. the *zero state* and the two *active states* are occurring in each switching period.

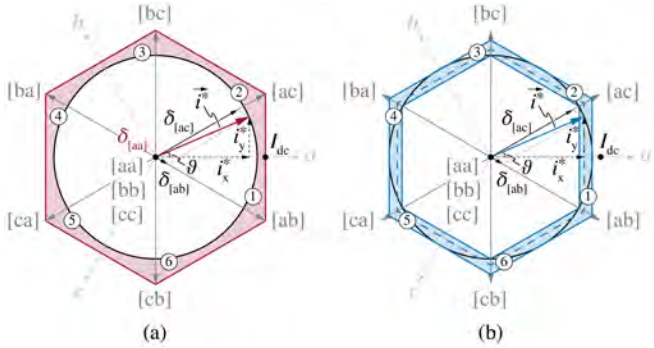


Fig. 8.6: Space vector diagram highlighting the nine states of the 3-Φ inverter and the vector of the reference sinusoidal load phase current $\vec{i}^*$, in case **(a)** 3/3-PWM is applied, i.e. the apothem of the hexagon is fixed to I_{dc}, and **(b)** 2/3-PWM is applied, i.e. the size of the hexagon is scaled according to the local value of i_{dc} varying over time. The encircled numbers define the six symmetric $\pi/3$-wide intervals of an AC output period, as described in **Fig. 8.3**.

8.3.2 Two-Third Pulse-Width Modulation

According to **Section 8.3.1**, a *zero state* free modulation should be preferred to maximize the efficiency of the 3-Φ bB CSI system. In fact, the transitions into (and out of) the *zero states* cause additional switching losses and, during the *zero states*, conduction losses occur even though no power is transferred to the load. Additionally, *zero states* are responsible for generating the highest common mode voltage [210]. Hence, rewriting (8.8) for $\delta_{[aa]} = 0$,

$$i_{dc} = \hat{i}_{out} \cos \vartheta = i_a \qquad (-\pi/6 < \vartheta < \pi/6) \tag{8.9}$$

is obtained. For symmetry, (8.9) can be generalized to

$$i_{dc} = \max\{|i_a|, |i_b|, |i_c|\}, \tag{8.10}$$

which is valid for the entire AC output period, neglecting the currents flowing in C_o. In other words, if the buck converter controls and shapes i_{dc} to be equal to the instantaneous largest load phase current absolute value, e.g. to i_a during ①, the free-wheeling interval is avoided (since, e.g. again during ①, $i_{dc} - i_a = 0$). Adjusting i_{dc} as described translates, in the space vector plane shown in **Fig. 8.6(b)**, into a continuous scaling of the dimensions of the hexagon over time, such that its perimeter matches the trajectory defined

by $\vec{i}^*$, resulting in $\delta_{[ac]} + \delta_{[ab]} = 1$, i.e. $\delta_{[aa]} = 0$. Following this approach, only the two *active states* [ab] and [ac] (instead of all three states) must be applied within one switching period; consequently, $T_{a,l}$ is permanently off and only two ($T_{b,l}$ and $T_{c,l}$) instead of three 2G MB GaN e-FETs are alternately switched, as illustrated in **Fig. 8.3(b)**. Accordingly, this concept is named 2/3-PWM and, as already speculated and further discussed in **Section 8.4.2**, it enables a significant reduction of switching losses.
As a consequence of (8.10), $\bar{v}_{pn}$ in **Fig. 8.4(b)** is not constant as in **Fig. 8.4(a)**, but still guarantees a constant power $\bar{v}_{pn}\, i_{dc}$ at the input of the 3-Φ inverter. Moreover, since the *zero states* are avoided, v_{pn} never assumes the value of 0 V. In **Fig. 8.5** the voltage v_{an} across $T_{a,l}$ is indicated for completeness. During ① in **Fig. 8.5(b)**, generated applying 2/3-PWM, v_{an} varies between v_{ab} and $-v_{ca}$, while in **Fig. 8.5(a)**, where 3/3-PWM is considered, it also reaches 0 V. The same reasoning can be extended to ⑤, where the three states of interest are [ca], [cb] and [cc] (see **Fig. 8.6**), yielding to v_{an} not assuming the value of $-v_{ca}$ in **Fig. 8.5(b)**.
Repeating the calculations described in **Section 8.2.2** with $i_{dc} = \hat{i}_{out} \cos\vartheta$, the range of applicability of 2/3-PWM can be determined as

$$V_{dc} > \frac{\sqrt{3}}{2} \frac{1}{\cos(\vartheta)} \hat{v}_{out,ll} \qquad (-\pi/6 < \vartheta < \pi/6). \tag{8.11}$$

Since $\sqrt{3}/2 < \cos(\vartheta) \leq 1$, (8.11) indicates that 2/3-PWM can be considered only if $V_{dc} > \hat{v}_{out,ll}$, i.e. in a subset of the *Buck-Mode* operating region. However, when $\sqrt{3}/2\, \hat{v}_{out,ll} < V_{dc} < \hat{v}_{out,ll}$, i.e. in the rest of the *Buck-Mode* region, 2/3-PWM and 3/3-PWM can be alternated depending on ϑ, as discussed more in detail in **Section 8.5.2**. In practice, the range of applicability of 2/3-PWM should be defined in the design phase of the 3-Φ bB CSI system, opportunely selecting V_{dc} as function of $\hat{v}_{out}$.

8.4 Analysis of the Two-Third Pulse-Width Modulation

Following the basic analysis of 2/3-PWM provided in **Section 8.3.2**, the enabled reduction of conduction and switching losses in the 3-Φ inverter are calculated in the following.

8.4.1 Reduction of Conduction Losses

Since i_{dc} continuously flows through L_{dc} and two MB GaN e-FETs, the conduction losses occurring in the 3-Φ inverter are proportional to the square of the RMS value of i_{dc}. Considering i_{dc} given by (8.10),

$$i_{dc,RMS} = \sqrt{\frac{1}{\pi/3} \int_{-\pi/6}^{+\pi/6} \hat{i}_{out}^2 \cos^2(\vartheta)\, \mathrm{d}\vartheta} = 0.96\, \hat{i}_{out} \tag{8.12}$$

results. Consequently, for a given operating point, the conduction losses are reduced by 8 % in case 2/3-PWM is applied. Similarly, the local average value of i_{dc} given by (8.10) can be calculated for each sector of an AC output period, obtaining $\langle i_{dc} \rangle = {}^{3}/_{\pi}\, \hat{i}_{out} = 0.95\, \hat{i}_{out}$.

8.4.2 Reduction of Switching Losses

To analyze the occurring switching losses, the 3-Φ bB CSI system illustrated in **Fig. 8.1** is simplified to the circuit schematic shown in **Fig. 8.7**. This representation is valid during ① but, according to the symmetry of the phases, similar diagrams can be derived for the rest of the AC output period.
Only the three low-side switches $T_{i,l}$ are considered in **Fig. 8.7**, since (during ①) the switching state of the three high-side switches $T_{i,h}$ is fixed, i.e. $T_{a,h}$

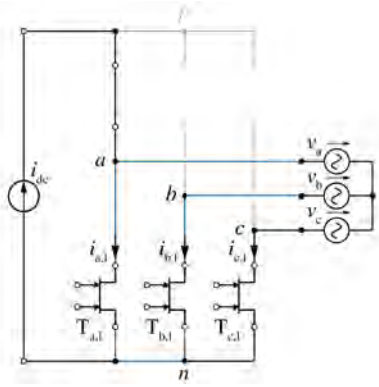


Fig. 8.7: Simplified representation of the 3-Φ bB CSI system shown in **Fig. 8.1** for the analysis of the switching losses in the 3-Φ inverter. Each pair of low-side switches forms a bridge-leg supplied from one of the sinusoidal line-to-line output voltages and having the DC-link current as load current.

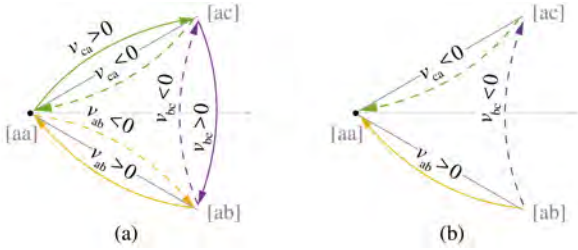


Fig. 8.8: Zoom of **Fig. 8.6** with arrows whose directions highlight under which condition (positive or negative) of the output line-to-line voltage v_{xy} (solid line for $v_{xy} > 0$ and dashed line for $v_{xy} < 0$), the indicated transition causes a hard commutation of the corresponding bridge-leg. **(a)** All transitions and **(b)** an exemplification considering $v_{ab} > 0$, i.e. hard commutation from [ab] to [aa] (solid), $v_{bc} < 0$, i.e. hard commutation from [ab] to [ac] (dashed), and $v_{ca} < 0$, i.e. hard commutation from [ac] to [aa] (dashed). All opposite transitions (non indicated in **(b)**) are soft commutations.

is permanently on, while $T_{b,h}$ and $T_{c,h}$ are permanently off. It can be recognized that the three line-to-line output voltages v_{xy} are applied across the corresponding pairs of low-side switches $T_{x,l}$ and $T_{y,l}$, and that one switch in turn conducts i_{dc}. Therefore, the series connection of $T_{x,l}$ and $T_{y,l}$ can be considered as a bridge-leg configuration supplied from v_{xy}, having the negative DC-link terminal n as switch node, and i_{dc} as load current. Consequently, the switching transition between two states, e.g. from [ab] to [ac], is nothing else than the commutation of a bridge-leg, e.g. of the one formed by $T_{b,l}$ and $T_{c,l}$, and supplied by v_{bc}.

Assuming $i_{dc} > 0$, uniquely the sign of v_{xy} determines whether a state transition corresponds to a ZVS transition or a hard-switching transition of the associated bridge-leg, as indicated in **Fig. 8.8**. In particular, in **Fig. 8.8**, the three states considered in ①, i.e. the three closest neighbors of the vector of the reference sinusoidal load phase current $\vec{i}^*$ (see **Section 8.3**), are shown and connected by arrows whose directions highlight under which condition (positive or negative) of v_{xy} (solid line for $v_{xy} > 0$ and dashed line for $v_{xy} < 0$), the respective state transition causes a hard commutation. For simplicity, only hard-switching losses, i.e. hard commutations, are considered in this analysis, i.e. ZVS losses are neglected.

Since i_{dc} is practically constant, the actual value of v_{xy} determines the switching losses of each state transition. Accordingly, the switching losses occurring in the 3-Φ inverter can be approximated by calculating the average value of the switched v_{xy} over the considered $\pi/3$-wide interval of an AC output period,

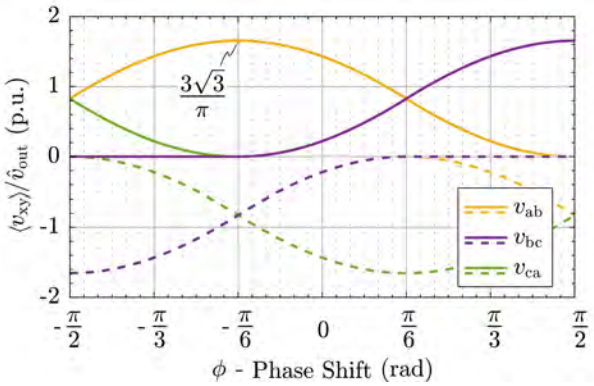


Fig. 8.9: Normalized average line-to-line voltages $\langle v_{xy}\rangle$ as function of the load phase shift ϕ. Positive and negative line-to-line voltages v_{xy} are averaged separately, obtaining $\langle v_{xy}^{+}\rangle$ (continuous lines) and $\langle v_{xy}^{-}\rangle$ (dashed lines). When v_{xy} is always positive (negative) for the considered ϕ, the dashed (continuous) line of corresponding color is 0. This is only shown for $\pm v_{bc}$, e.g. for v_{bc} with $-\pi/2<\phi<-\pi/6$; different $\langle v_{xy}\rangle$ overlap only when 0.

i.e. $\langle v_{sw}\rangle$, which is dependent on ϕ and on $\hat{v}_{out}$ [211, 212]. **Fig. 8.9** shows the average line-to-line voltages $\langle v_{xy}\rangle$ as a function of ϕ and normalized with respect to $\hat{v}_{out}$. Angular brackets $\langle\cdot\rangle$ are used to indicate the averaging over ①. For convenience, positive and negative v_{xy} are averaged separately, obtaining $\langle v_{xy}^{+}\rangle$ (continuous lines) and $\langle v_{xy}^{-}\rangle$ (dashed lines), such that each line in **Fig. 8.9** directly relates to one arrow in **Fig. 8.8(a)**. E.g. at $\phi = -\pi/6$, $\langle v_{ab}^{+}\rangle = 3\sqrt{3}/\pi\ \hat{v}_{out}$ features a maximum while $\langle v_{ab}^{-}\rangle = 0$, since $v_{ab} > 0$; hence, the state transition from [ab] to [aa] (continuous yellow line) corresponds to a hard commutation with maximum switching losses, while the transition in the opposite direction (from [aa] to [ab], dashed yellow line) is loss-less. For the same ϕ, the two state transitions from [ab] to [ac] and from [ac] to [aa] (dashed purple and green lines respectively) result as well in hard commutations, however, since $\langle v_{bc}^{-}\rangle = \langle v_{ca}^{-}\rangle = -3\sqrt{3}/2\pi\ \hat{v}_{out}$, much lower switching losses occur. The state transitions in the opposite directions (continuous purple and green lines) are again loss-less, since $\langle v_{bc}^{+}\rangle = \langle v_{ca}^{+}\rangle = 0$.
Finally, the sequence in which the states of the 3-Φ inverter are applied within one switching period ultimately defines which v_{xy} are switched; e.g. v_{ab} and v_{bc} are involved in the state sequence [aa]-[ab]-[ac], whereas v_{ab} is replaced by v_{ca} in the state sequence [aa]-[ac]-[ab]. For completeness, the simplest

Tab. 8.2: State sequences connecting all the three states indicated in the graph of **Fig. 8.8** as required for 3/3-PWM, and state sequence enabled by 2/3-PWM avoiding the *zero state* and requiring only two transitions.

Modulation	State Sequence	Note
3/3-PWM	... [ab], [aa] [ac] [ab], [aa] ...	cw-asym
	... [ac], [aa] [ab] [ac], [aa] ...	ccw-asym
	... [ac], [ac] [aa] [$\overset{\triangledown}{\text{ab}}$] [aa] [ac], [ac] ... ... [ab], [ab] [aa] [$\overset{\triangledown}{\text{ac}}$] [aa] [ab], [ab] ...	[aa]-sym
	... [aa], [aa] [ab] [$\overset{\triangledown}{\text{ac}}$] [ab] [aa], [aa] ... ... [ac], [ac] [ab] [$\overset{\triangledown}{\text{aa}}$] [ab] [ac], [ac] ...	[ab]-sym
	... [aa], [aa] [ac] [$\overset{\triangledown}{\text{ab}}$] [ac] [aa], [aa] ... ... [ab], [ab] [ac] [$\overset{\triangledown}{\text{aa}}$] [ac] [ab], [ab] ...	[ac]-sym
2/3-PWM	... [ac], [ab] [ac], [ab] ...	

state sequences relative to ① are listed in **Tab. 8.2**. When 3/3-PWM is applied, all neighboring states must be included in the switching sequence, which can be achieved with three or four transitions (in the simplest case). The two (clockwise and counter-clockwise) sequences formed by three transitions are asymmetric concerning the generated v_{pn} in a switching period, and can result in one or two hard-switching transitions, depending on the sign of each v_{xy}. The three sequences formed by four transitions, instead, showing a symmetry with respect to one state, result in symmetric v_{pn} and always in two hard-switching transitions. When 2/3-PWM is applied, instead, only the two *active states* have to be passed through; hence, this switching sequence requires only two transitions, only one of which is hard.
In case of 3/3-PWM, extending the procedure proposed in [212], it can be shown that the state sequence offering minimum switching losses [213] requires two hard-switching transitions with an average voltage

$$\langle v_{\text{sw},3/3} \rangle = \frac{3\sqrt{3}}{2\pi} \hat{v}_{\text{out}} \tag{8.13}$$

per switching period, independent of ϕ. In case of 2/3-PWM, instead, only the two *active states* [ab] and [ac] are applied within one switching period, i.e. the switched voltage, during ①, is always v_{bc}; hence, $\langle v_{\text{sw},2/3} \rangle$ (the counterpart

to $\langle v_{\mathrm{sw},3/3} \rangle$ for 2/3-PWM) can be calculated as the average of $|v_{\mathrm{bc}}|$ over the considered $\pi/3$-wide interval of an AC output period [204, 205], obtaining

$$\frac{\langle v_{\mathrm{sw},2/3} \rangle}{\hat{v}_{\mathrm{out}}} = \begin{cases} \dfrac{3\sqrt{3}}{\pi} \left(2 - \sqrt{3}\, \cos(\phi)\right) & (-\pi/6 < \phi < +\pi/6) \\ \dfrac{3\sqrt{3}}{\pi} \sin(\phi) & (+\pi/6 < |\phi| < +\pi/2). \end{cases} \tag{8.14}$$

The mathematical expressions (8.13) and (8.14) are visualized in **Fig. 8.10(a)**. The ratio between $\langle v_{\mathrm{sw},2/3} \rangle$ and $2 \langle v_{\mathrm{sw},3/3} \rangle$ (where the factor 2 accounts for the fact that two hard-switching transitions occur within one switching period in case of 3/3-PWM) is already an indicator of the reduction of switching losses enabled by 2/3-PWM; in particular

$$\frac{\langle v_{\mathrm{sw},2/3} \rangle}{2 \langle v_{\mathrm{sw},3/3} \rangle} = 2 - \sqrt{3}\, \cos(\phi) = 0.27 \tag{8.15}$$

is obtained for $\cos(\phi) = +1$.
More precisely, the hard-switching losses $P_{\mathrm{sw}} = E_{\mathrm{sw}} f_{\mathrm{sw}}$ occurring in the 3-Φ inverter can be calculated according to the conventional VI-overlap switching loss model. Considering only the dependency on the switched voltage given by (8.13) and (8.14), since the switched current is practically constant, E_{sw} can be approximated with

$$E_{\mathrm{sw},3/3} = 2 \left(k_1 \langle v_{\mathrm{sw},3/3} \rangle + k_2 \langle v_{\mathrm{sw},3/3} \rangle^2\right) \tag{8.16}$$

and

$$E_{\mathrm{sw},2/3} = k_1 \langle v_{\mathrm{sw},2/3} \rangle + k_2 \langle v_{\mathrm{sw},2/3} \rangle^2 \tag{8.17}$$

for the case of 3/3-PWM and 2/3-PWM, respectively. The values of k_1 and k_2 in (8.16) and (8.17) are determined by the considered operating point (see **Tab. 8.1**), and by the switching performance of the power semiconductors employed for the realization of the 3-Φ inverter. $k_1 = 60\,\mathrm{A\,ns}$ and $k_2 = 720\,\mathrm{pF}$ [214] are selected as an example in **Fig. 8.10(b)**, where (8.16) and (8.17) are depicted for comparison. It can be observed that 2/3-PWM clearly outperforms 3/3-PWM, as already speculated, especially for low values of ϕ, i.e. in approximately ohmic load conditions. This originates from the fact that 2/3-PWM requires only one hard-switching transition per switching period and, in addition, that the switched voltage $|v_{\mathrm{bc}}|$ is the smallest among all $|v_{\mathrm{xy}}|$ for low values of ϕ (see **Fig. 8.9**). In particular

$$\frac{E_{\mathrm{sw},2/3}}{E_{\mathrm{sw},3/3}} = 0.19 \tag{8.18}$$

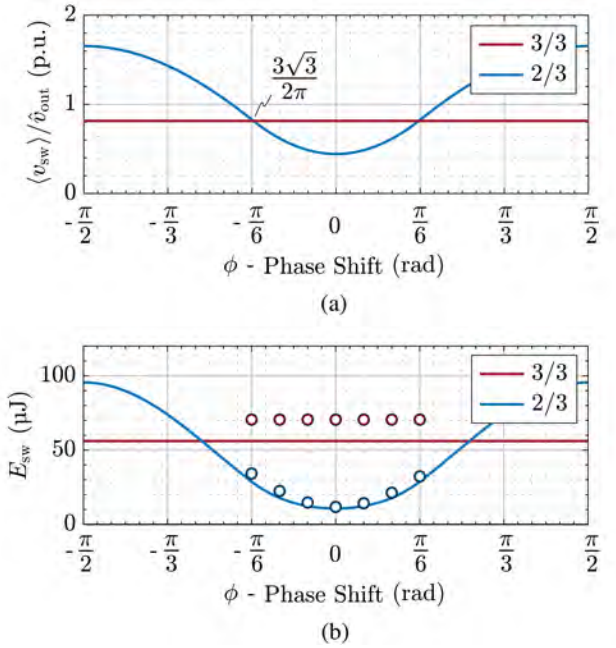


Fig. 8.10: (a) Normalized average (over the considered $\pi/3$-wide interval of an AC output period) line-to-line output voltages $\langle v_{sw} \rangle$ switched in the 3-Φ inverter, as function of the phase shift ϕ. **(b)** Switching energy E_{sw} dissipated in the 3-Φ inverter, i.e. considering all power semiconductors, in one switching period, for the operating point specified in **Tab. 8.1**, and as function of ϕ and of the selected modulation scheme. The lines indicate the results of the simplified analytical calculations, while the dots are obtained from circuit simulations.

is calculated for $\cos(\phi) = +1$, i.e. in the typical operating conditions of VSD supplying synchronous machines driving passive mechanical loads, or in case of PFC rectifiers, and of inverters feeding renewable energy into the grid. The result of (8.18) is lower (and more accurate) than the one of (8.15) as it takes the influence of the quadratic term present in (8.16) and (8.17) into account. Only for $\pi/3 < |\phi| < \pi/2$, $|v_{bc}|$ features a maximum; hence, all state sequences avoiding the transitions from [ab] to [ac] and vice versa result in lower switching losses. However, 2/3-PWM can nevertheless be applied and [aa] used only as a transitory state between [ac] and [ab], just to avoid the most lossy switching transition associated with the direct commutation from [ac] to [ab].

In this way, it is still possible to benefit from the reduction of conduction losses enabled by 2/3-PWM.
To prove the correctness of the developed analytic procedure, the switching energy E_{sw} is additionally calculated in a simulation environment. The same operating conditions (see **Tab. 8.1**) and switching loss models (cf. (8.16) and (8.17)) are selected, but the exact switched voltage and current values are now considered. The so obtained numerical results are indicated with dots in **Fig. 8.10(b)**, confirming the accuracy of the analytical results. The discrepancy between calculations and simulations is attributed to the averaging of v_{xy} over the considered $\pi/3$-wide interval of an AC output period, and to the neglection of the soft-switching losses, and of the losses occurring in the switch not involved in the commutation of i_{dc} [215]. A more detailed (but more complex) analytic derivation of E_{sw}, offering a better matching with the numerical results, can be found in [216].
In summary, it should be pointed out that, in particular for $\phi \approx 0$, the reduction of switching losses enabled by 2/3-PWM amounts up to 83 %.

8.5 Circuit Simulation

The detailed operation of the 3-Φ bB CSI system is discussed in this section through the analysis of circuit simulations, focusing on 2/3-PWM and on the developed synergetic control scheme.

8.5.1 Synergetic Control

A key requirement for the correct operation of the 3-Φ bB CSI system, in particular when 2/3-PWM is applied, is the precise control and shaping of i_{dc}; for this purpose, the control structure shown in **Fig. 8.11** is proposed and described in the following.
The input of the controller, indicated on the left-hand side of **Fig. 8.11(a)**, is the reference speed of the driven electric machine ω^*, assuming a VSD application. Comparing ω^* with the measured speed ω, a reference for the torque and hence for the sinusoidal load (motor) phase currents i_a^*, i_b^* and i_c^* is generated. Since this analysis focuses only on the operation of the 3-Φ bB CSI system, the speed and torque controller (typically implemented in a rotating dq-coordinate frame) is not discussed further.
The central part of the control structure, on the right-hand side of **Fig. 8.11(a)**, determines the reference switching stage output currents $i_{a,sw}^*$, $i_{b,sw}^*$ and $i_{c,sw}^*$ from i_a^*, i_b^* and i_c^* and compensates for the currents $i_{Co,a}$, $i_{Co,b}$ and $i_{Co,c}$ flowing

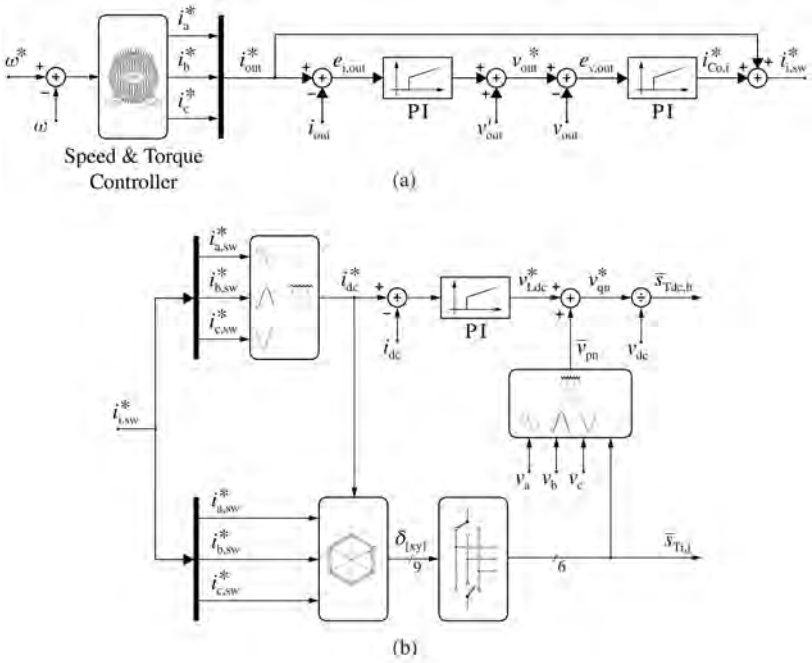


Fig. 8.11: Structure of the synergetic control of the 3-Φ bB CSI system (see **Fig. 8.1**) combining the regulation and shaping of i_{dc} with the generation of sinusoidal load phase currents. The input of the controller (left-hand side of **(a)**) is the reference speed of the driven electric machine ω^*, while the outputs (right-hand side of **(b)**) are the duty-cycle of the buck converter $\bar{s}_{Tdc,h}$, and the nine gate control signals (local average over a switching period) of the 3-Φ inverter $\bar{s}_{Ti,j}$. The illustrated control structure is applicable in the *Buck-Mode* (both for 2/3-PWM and for 3/3-PWM), and can be extended to the *Boost-Mode* as described in [203].

through C_o. As this part is identical for all the phases, the phase quantities i_a^*, i_b^* and i_c^* are unified in the generic reference sinusoidal load phase current i_{out}^*. Comparing i_{out}^* with the measured i_{out}, i.e. with the measured i_a, i_b and i_c, the error on the sinusoidal load phase current $e_{i,out}$ is calculated. Through a proportional-integral (PI) controller, $e_{i,out}$ is transformed into the reference sinusoidal output voltage v_{out}^* to be applied across C_o. Eventually, an estimation of v_{out}, i.e. v_{out}', can be feed-forwarded to improve the performance of the current controller. In case of VSD, v_{out}' (see **Fig. 8.2**), i.e. the back-electromotive force of the electric machine, can be obtained multiplying ω

with the speed constant of the considered machine. Similarly as for the case of i_{out}, comparing v^*_{out} with the measured v_{out}, the error on the sinusoidal output voltage $e_{v,out}$ is calculated. Again, through a PI controller, $e_{v,out}$ is transformed into the reference filter capacitor current $i^*_{Co,i}$ (i = a, b, c). Summing i^*_{out} with $i^*_{Co,i}$, the reference switching stage output current $i^*_{i,sw}$ (i = a, b, c) is finally obtained.

Phase quantities are necessary in the final part of the block diagram, which is shown in **Fig. 8.11(b)**; hence $i^*_{i,sw}$ is transformed back into $i^*_{a,sw}$, $i^*_{b,sw}$ and $i^*_{c,sw}$. This part is divided in two branches: one provides the duty-cycle of the buck converter $\bar{s}_{Tdc,h}$, while the other one determines the local average (over one switching period) gate control signals of the 3-Φ inverter $\bar{s}_{Ti,j}$.

In the upper branch of **Fig. 8.11(b)**, $i^*_{a,sw}$, $i^*_{b,sw}$ and $i^*_{c,sw}$ are first combined to generate the reference DC-link current i^*_{dc}, as defined in (8.10). Comparing i^*_{dc} with the measured i_{dc}, the reference voltage to be applied across L_{dc}, i.e. v^*_{Ldc}, is determined through the third PI controller. Summing v^*_{Ldc} with $\bar{v}_{pn}$, obtained from the lower branch, the reference output voltage of the buck converter v^*_{qn} is obtained. Finally, dividing v^*_{qn} with v_{dc}, also $\bar{s}_{Tdc,h}$ is determined.

In the lower branch, $i^*_{a,sw}$, $i^*_{b,sw}$, $i^*_{c,sw}$ and i^*_{dc} are first inserted in (8.7) to determine the nine duty-cycles $\delta_{[xy]}$. For example, for $\vartheta = 0$ (during ①, see **Fig. 8.6**), $\delta_{[ac]} = \delta_{[ab]} = 0.5$ (and all other $\delta_{[xy]} = 0$) results. Thus, the nine $\delta_{[xy]}$ are converted to the six $\bar{s}_{Ti,j}$, as indicated in (8.6). In the example, $\delta_{[ac]} = \delta_{[ab]} = 0.5$ translates into $\bar{s}_{Ta,h} = 1$, $\bar{s}_{Tb,l} = \bar{s}_{Tc,l} = 0.5$ and all other $\bar{s}_{Ti,j} = 0$. Finally, the six $\bar{s}_{Ti,j}$ are combined with the measured v_a, v_b and v_c to obtain

$$\bar{v}_{pn} = \sum_{i\,=\,a,\,b,\,c} \left(\bar{s}_{Ti,h} - \bar{s}_{Ti,l}\right) v_i, \tag{8.19}$$

required in the upper branch of **Fig. 8.11(b)**. In the example, (8.19) expands to $\bar{v}_{pn} = v_a - 0.5\,(v_b + v_c)$.

As clarified with this explanation, the control scheme shown in **Fig. 8.11** is considered as synergetic, since the upper and lower branches mutually contribute to the correct operation of the 3-Φ bB CSI system, i.e. the buck converter shapes i_{dc} in support of the generation of sinusoidal load phase currents, finally performed by the 3-Φ inverter. This control concept is applicable in the *Buck-Mode*, but can be easily extended to the *Boost-Mode* [203].

To conclude, it should be additionally noticed that, the exact same control structure can be considered for 3/3-PWM, except for (8.10). In case of 3/3-PWM, in fact, i^*_{dc} is constant and $i^*_{dc} = I^*_{dc} \geq i^*_{i,sw}$ (i = a, b, c) is necessary. As shown in the next section, this allows a seamless transition between 3/3-PWM and 2/3-PWM and vice versa.

8.5.2 Simulation Results

The functioning of the synergetic control scheme described in **Section 8.5.1** is verified in the following with the results of closed-loop circuit simulations of the 3-Φ bB CSI system for different operating conditions. The specifications reported in **Tab. 8.1** are generally considered. A switching frequency f_{sw} = 140 kHz, in combination with L_{dc} = 550 µH and C_o = 6.6 µF, ensures a peak-to-peak current ripple on i_{dc} of 10 % of the nominal $\hat{i}_{out}$ and negligible ripple on the sinusoidal output voltage. The load consists of an ideal voltage source with a comparably small series impedance (sufficient to limit the ripple on the sinusoidal load phase currents to similar values as the ripple on i_{dc}).
In particular, in the upper part of **Fig. 8.12**, the simulated waveforms of i_{dc} and i_{out} are shown together with the ones of v_{out}, for $\phi \approx \pi/6$ and $\pi/2$. Differently from the ideal case considered in **Fig. 8.3(b)**, a small discrepancy between i_{out} and i_{dc}, due to $i_{Co,i}$, can be observed here. Although the same values of $\hat{i}_{out}$ (hence i_{dc}) and $\hat{v}_{out}$ are considered in these plots, the different values of $\cos(\phi)$ result in different values of the output power P_{out}. Accordingly, the reduction of $\bar{v}_{pn}$, directly proportional to the one of P_{out}, is highlighted in the lower part of **Fig. 8.12**. For completeness, the simulated waveforms of i_{dc}, i_{out} and v_{out} are shown in **Fig. 8.13** for $-1 \leq \cos(\phi) \leq +1$. The smooth decrease of $\cos(\phi)$ can be noticed observing how, e.g. the waveforms of i_a and v_a, are in phase at time t = 0 s and in phase opposition at t = 80 ms. To guarantee the controllability of i_{dc}, i.e. to guarantee that $\bar{v}_{pn}$ is sufficiently positive when the direction of power flow is inverted (see **Section 8.5.1**), ϕ instantaneously varies from $\pi/2 - \pi/8$ to $\pi/2 + \pi/8$ at t = 40 ms. The same waveforms are summarized in **Fig. 8.14**, for $\cos(\phi) = \pm 1$, and for different values of $\hat{i}_{out}$, to analyze the dynamic response of the synergetic control scheme. Finally, the two operating modes described in **Section 8.2.2**, i.e. the *Buck-Mode* and the *Boost-Mode*, and the two modulation schemes presented in **Section 8.3**, i.e. 3/3-PWM and 2/3-PWM, are jointly shown in **Fig. 8.15**, for $\cos(\phi) = +1$. At t = 0 s, the supplying DC input voltage $v_{dc} > \hat{v}_{out,ll}$ allows both 3/3-PWM and 2/3-PWM in the *Buck-Mode*; hence, both modulations are independently applied in the first and second AC output periods, respectively. Starting at $t \approx 40$ ms, $v_{dc} < \hat{v}_{out,ll}$; thus, although still in the *Buck-Mode*, 2/3-PWM can be used only in combination with 3/3-PWM, depending on the instantaneous value of v_{out}. Once $v_{dc} < \sqrt{3}/2\, \hat{v}_{out,ll}$ is reached (after $t \approx 60$ ms), the *Boost-Mode* is entered.
To summarize, for all operating conditions of interest, i.e. for different values of $\cos(\phi)$ and $\hat{i}_{out}$, the 3-Φ bB CSI system outputs the desired current and voltage waveforms, and can be successfully operated with 2/3-PWM.

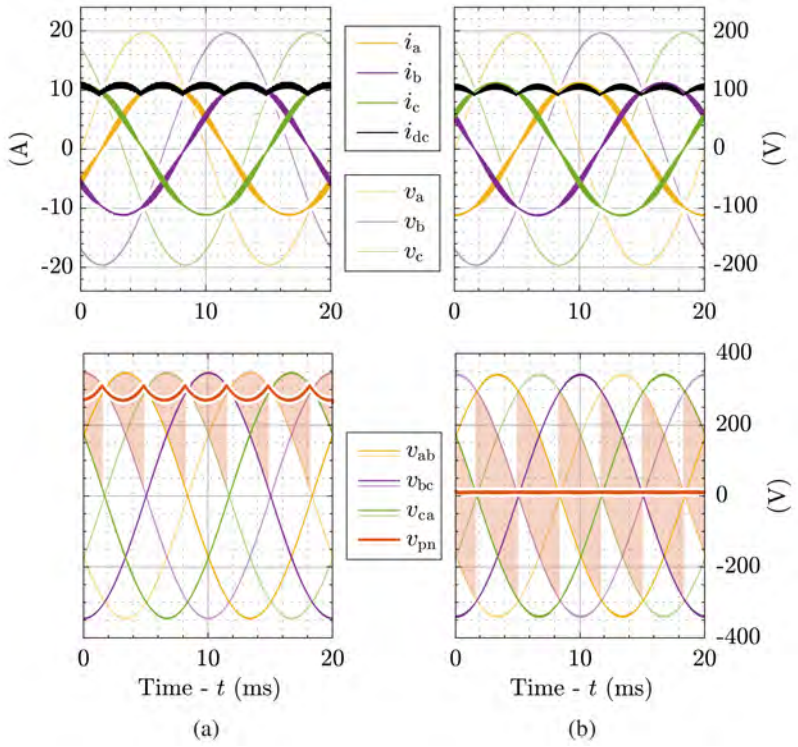


Fig. 8.12: DC-link current i_{dc}, sinusoidal load phase currents i_a, i_b and i_c, sinusoidal output voltages v_a, v_b and v_c, sinusoidal line-to-line output voltages $\pm v_{ab}$, $\pm v_{bc}$ and $\pm v_{ca}$, and input voltage of the 3-Φ inverter v_{pn} within one AC output period, in case 2/3-PWM is applied, for **(a)** phase shift of the sinusoidal load phase currents and sinusoidal output voltages $\phi \approx \pi/6$ and **(b)** $\phi \approx \pi/2$ (see **Tab. 8.1**). A switching frequency $f_{sw} = 140\,\text{kHz}$ is selected in combination with $L_{dc} = 550\,\mu\text{H}$ and $C_o = 6.6\,\mu\text{F}$ in all the following simulations. The load consists of an ideal voltage source with a comparably small series impedance (sufficient to limit the ripple on the sinusoidal load phase currents). Independent of the value of the load power factor $\cos(\phi)$, a constant peak value $\hat{i}_{out}$ of the sinusoidal load phase currents is maintained. The red lines in the graphs of $v_{out,ll}$ correspond to the local average input voltage of the 3-Φ inverter $\bar{v}_{pn}$ over a switching period.

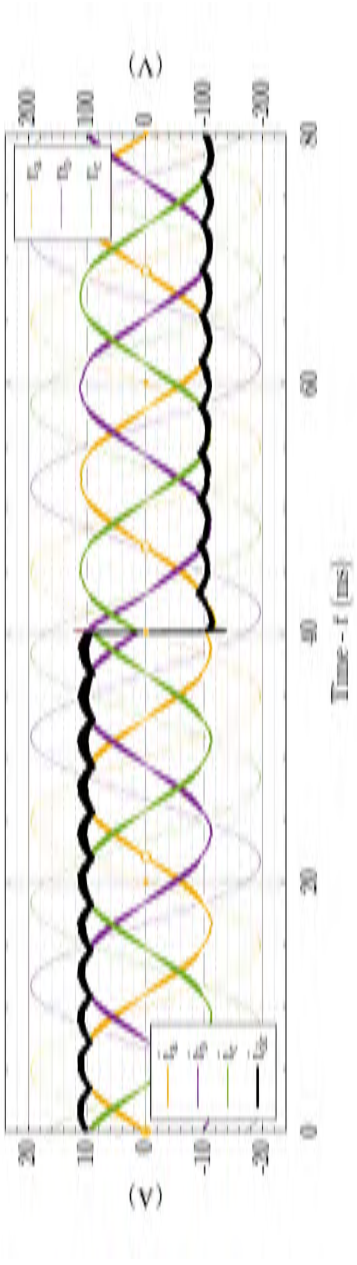


Fig. 8.13: DC-link current i_{dc}, sinusoidal load phase currents i_a, i_b and i_c, and sinusoidal output voltages v_a, v_b and v_c within four AC output periods, in case 2/3-PWM is applied, and for load power factor $\cos(\phi)$ decreasing linearly from +1 to −1 (see **Tab. 8.1**). Independent of the value of $\cos(\phi)$, a constant peak value $\hat{i}_{out}$ of the sinusoidal load phase currents is maintained. At time t = 40 ms, $\cos(\phi)$ reaches 0 and subsequently changes sign, i.e. the direction of power flow is reversed, and i_{dc} must be inverted accordingly.

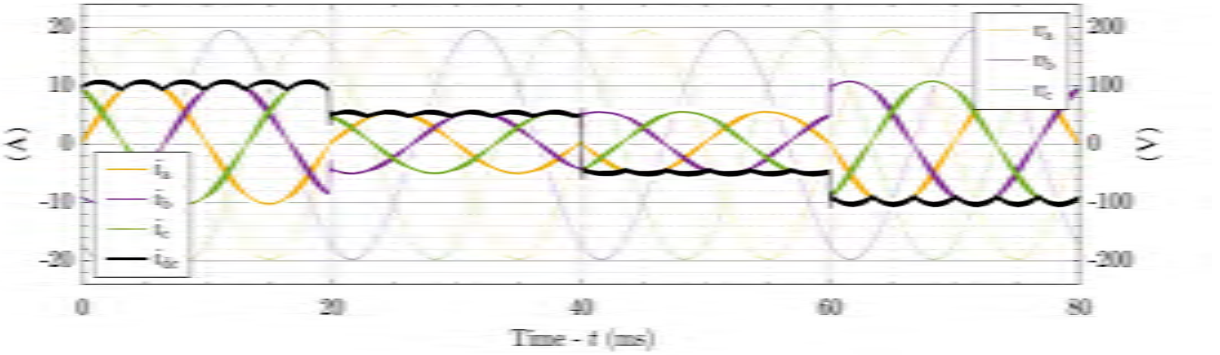


Fig. 8.14: DC-link current i_{dc}, sinusoidal load phase currents i_a, i_b and i_c, and sinusoidal output voltages v_a, v_b and v_c within four AC output periods, in case 2/3-PWM is applied, for load power factor $\cos(\phi) = +1$ for time $t < 40$ ms and $\cos(\phi) = -1$ for $t > 40$ ms, and for different peak values $\hat{i}_{out}$ of the sinusoidal load phase currents, i.e. for full and half rated output power P_{out} (see **Tab. 8.1**).

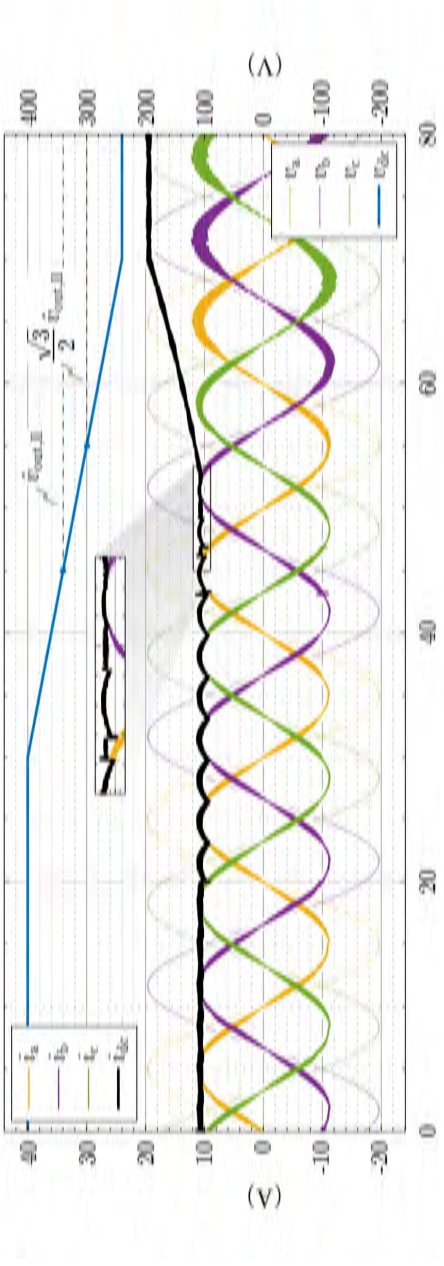


Fig. 8.15: DC-link current i_{dc}, sinusoidal load phase currents i_a, i_b and i_c, sinusoidal output voltages v_a, v_b and v_c, and supplying DC input voltage v_{dc} within four AC output periods, for load power factor $\cos(\phi) = +1$ (see **Tab. 8.1**). By reducing v_{dc}, a transition from the *Buck-Mode* to the *Boost-Mode* occurs; additionally, both 3/3-PWM and 2/3-PWM are shown in the *Buck-Mode*.

8.6 Aspects of Practical Realization

In this section, after introducing research samples of 2G MB GaN e-FETs, a prediction of the efficiency and power density achievable with the 3-Φ bB CSI system is provided.

8.6.1 Dual-Gate Monolithic Bidirectional GaN e-FET

The power devices selected for the realization of the 3-Φ inverter are ±600 V 26 mΩ 2G MB GaN e-FETs [198]. The main characteristics of this switch (currently only available as research sample) are compared in **Tab. 8.3** with the ones of the best-in-the-market conventional GaN power transistor in the same voltage class, i.e. a 650 V 25 mΩ GaN e-FET [217].
To extend the operation of the conventional devices to four-quadrants, while maintaining the same overall on-state resistance $R_{ss,on}$, two anti-series and two parallel devices must be connected as shown in **Fig. 8.16(a)**; this massively increases costs and, as highlighted by **Fig. 8.16(b)**, the required PCB area

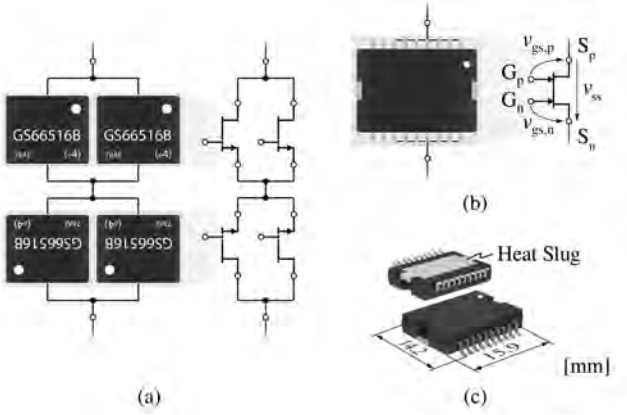
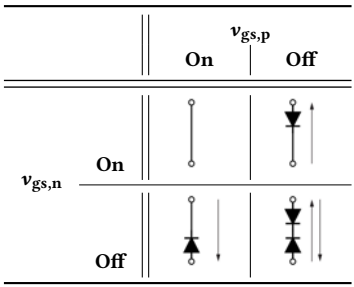


Fig. 8.16: Conventional realization of a switch with bidirectional voltage blocking capability and allowing controlled bidirectional current flow, i.e. of a four-quadrant (AC) switch, with **(a)** two anti-series/two parallel 650 V 25 mΩ GaN e-FETs [217] compared with **(b)** a single ±600 V 26 mΩ 2G MB GaN e-FET [198] (geometric proportions of the packages are preserved). Both solutions **(a)** and **(b)** achieve approximately the same voltage blocking capability and overall on-state resistance, however **(b)** enables a massive saving in terms of package size. **(c)** Perspective view of the 20-pin package of the 2G MB GaN e-FET.

Tab. 8.3: Main characteristics of the selected 2G MB GaN e-FET compared to the best-in-the-market conventional GaN power transistor in the same voltage class as a single device (1x) and in the two anti-series/two parallel configuration (4x).

Power Semiconductor			$V_{ss,MAX}$	$I_{ss,MAX}$	$R_{ss,on}$	$C_{oss,Q}$	$C_{rss,Q}$	**FoM** = $(R_{ss,on} C_{oss,Q})^{-1}$	**Size**
Manufacturer	**Part Number**			@ 25 °C	@ 25 - 150 °C	@ 400 V		@ 25 °C - 400 V	
Panasonic	EDLS06SMD		±600 V	92 A	26 - 43 mΩ	190 pF	40 pF	202 GHz	2.3 cm^2
GaN Systems	GS66516	(1x)	650 V	60 A	25 - 65 mΩ	281 pF	8 pF	142 GHz	1.0 cm^2
		(4x)	±650 V	120 A		562 pF	16 pF	71 GHz	4.0 cm^2

Tab. 8.4: Equivalent circuit of the 2G MB GaN e-FET depending on the applied gate voltages $v_{gs,n}$ and $v_{gs,p}$.



with respect to the solution based on the MB switch. Additionally, due to the increased parasitic output capacitance C_{oss}, the FoM [113] of the so obtained AC-switch becomes almost three times worse than the one of the MB device. To summarize, the considered 2G MB GaN e-FET is expected to allow a performance breakthrough of 3-Φ bB CSI systems, and potentially of all circuit topologies requiring AC-switches as, e.g. AC/AC matrix converters.
In order to simultaneously control the bidirectional voltage blocking and current flow capabilities of the 2G MB GaN e-FET (see **Table 8.4**), two gate voltages $v_{gs,n}$ and $v_{gs,p}$ must be separately applied to the 2G structure, as indicated in **Fig. 8.16(b)**. Alternatively, if only one gate is controlled, only unidirectional current flow is possible. The gate voltages $v_{gs,n}$ and $v_{gs,p}$ must be isolated from each other because of the common-drain structure which, based on a single drift layer, yields to lower values of $R_{ss,on}$ compared with the alternative common-source structure [195]. Additionally, the potential of the substrate must be left floating, while, in conventional GaN power transistors, the substrate is typically connected to the only source potential available; different switching behaviors of the 2G MB GaN e-FET are observed when the substrate is connected to the one or the other source potential.
Since the device is of Gate Injection Transistor (GIT) type [218], constant currents (in the mA-range) must flow through the gates to modulate the conductivity of the 2D electron gas channel during on-state. As visible in **Fig. 8.17(a)**, conventional gate driver circuits can be modified to include this feature [41]; alternatively, a GIT-specific IC [219], i.e. featuring a dedicated pin for supplying the constant gate current, can be used. Adopting the latter approach, the compact gate driver design illustrated in **Fig. 8.17(b)** is realized.

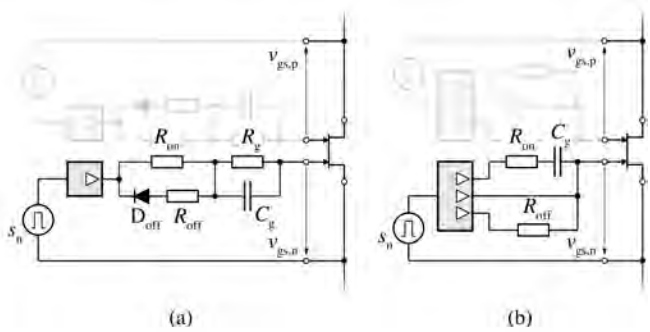


Fig. 8.17: (a) Conventional gate driver circuit based on a commercial IC and adapted to GITs [41], and **(b)** gate driver circuit for GITs based on a specific IC featuring a dedicated pin for the supplying of the constant gate current [219].

8.6.2 Performance Estimation of the Three-Phase Buck-Boost Current Source Inverter System

The presented 2G MB GaN e-FETs, whose operation is verified in **Appendix D**, together with the simulation results discussed in **Section 8.5.2**, demonstrate the feasibility of the 3-Φ bB CSI system operated with 2/3-PWM and allow to estimate its key performance indexes, i.e. the achievable efficiency and power density, e.g. for the specifications given in **Tab. 8.1**.
In particular, the design of the 3-Φ bB CSI system analyzed in the simulation environment (see **Fig. 8.12**) is estimated to achieve an efficiency $\eta = 98.4\,\%$, a volumetric power density $\rho = 16\,\mathrm{kW/dm^3}$, and a gravimetric power density $\beta = 6.1\,\mathrm{kW/kg}$, if a cooling system performance index CSPI $= 15\,\mathrm{W/K\,dm^3}$ is considered [220]. The power density figures are mainly limited by the volume ($81\,\mathrm{cm^3}$) and weight (240 g) of $L_{dc} = 550\,\mu\mathrm{H}$ [221]. Accordingly, if the allowed peak-to-peak current ripple on i_{dc} is increased from 10 % to 30 % of the nominal $\hat{i}_{out}$, L_{dc} can be reduced to 185 µH, resulting in a more compact and lighter inductor design, i.e. in a volume of $50\,\mathrm{cm^3}$ and in a weight of 115 g; thus, for the same $\eta = 98.4\,\%$, the power density increases to $\rho = 18\,\mathrm{kW/dm^3}$ and $\beta = 7.7\,\mathrm{kW/kg}$. If 3/3-PWM is applied to the same design, η drops below 98 %; an even more significant reduction is observed for higher values of f_{sw}, when the switching losses dominate the loss breakdown. In all designs, the buck converter is realized with the conventional GaN power transistor listed in **Tab. 8.3** [214]; moreover the same switching frequency is considered for the buck converter and for the 3-Φ inverter [203].

8.7 Conclusion

A 3-Φ buck-boost (bB) current source inverter (CSI) system employing a variable DC-link current control strategy denominated *Two-Third PWM* (2/3-PWM) and dual-gate (2G) monolithic bidirectional (MB) GaN e-mode FETs (e-FETs) in its boost-type 3-Φ current DC-link inverter output stage is analyzed in this chapter. Circuit simulations are performed to verify the operation of the 3-Φ bB CSI system, considering 2/3-PWM and the developed synergetic control concept. Moreover, analytic calculations quantify a reduction of the conduction losses of 8 %, and a massive reduction of the switching losses of 83 % (in case of unity load power factor), for 2/3-PWM in comparison with conventional 3/3-PWM. The operation of the 2G MB GaN e-FETs, which are suitable for any topology requiring AC-switches, is verified in a hardware prototype, where voltages up to 400 V and currents up to 10 A are continuously switched. These novel devices, in combination with 2/3-PWM, have the potential to significantly enhance the performance of 3-Φ bB CSI systems, ultimately favoring their usage in place of 3-Φ Bb VSI systems; in particular, a 3-Φ bB CSI system, rated for an output power $P_{\mathrm{out}} = 3.3\,\mathrm{kW}$, is estimated to simultaneously achieve an efficiency $\eta = 98.4\,\%$ and a volumetric power density $\rho = 18\,\mathrm{kW/dm^3}$ at a switching frequency $f_{\mathrm{sw}} = 140\,\mathrm{kHz}$ when 2/3-PWM is applied.

9

High Efficiency Weight-Optimized Fault-Tolerant Modular Multi-Cell Three-Phase Inverter for Next-Generation Aerospace Applications

This chapter summarizes the most relevant findings in the context of research on a novel modular multi-cell GaN inverter, which are also published in:

- **M. Guacci**, D. Bortis, and J. W. Kolar, "High-Efficiency Weight-Optimized Fault-Tolerant Modular Multi-Cell Three-Phase GaN Inverter for Next Generation Aerospace Applications," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Portland, OR, USA, 2018.

Motivation

The derived semiconductor loss models indicate that modular/multi-level power converters, having voltage waveforms of decreased harmonic content, can surpass the current limitations of conventional solutions, since they benefit from the superior performance of low voltage power semiconductors, while the modularity ensure compactness, scalability, reduced design effort, and fault-tolerant operation achieved through redundancy.

Executive Summary

The aircraft industry demands a significant increase of the efficiency and gravimetric power density of power converters for next generation aerospace applications. Between the two targets, i.e. an efficiency > 98 % and a gravimetric power density > 10 kW/kg, the specification concerning the converter weight is more challenging to fulfill. Since cooling systems and magnetic components dominate the weight breakdown of conventional converter concepts, multi-cell topologies, enabling improved semiconductor performance and reduced filtering requirements, are foreseen as promising solutions for the power electronics on-board of MEA. On the other hand, the necessary simultaneous operation of a high number of cells inevitably limits the reliability of multi-cell converters if redundancy is not provided. In this chapter, a favorable scaling trend of power density with respect to reliability, aiming to guarantee fault-tolerant operation without affecting the key performance figures of a power converter, is identified in modular multi-cell converters. Thus, a 45 kW weight-optimized modular multi-cell 3-Φ inverter featuring a redundant power stage is optimized, achieving an efficiency of 99 % and a gravimetric power density of 22.8 kW/kg.

9.1 Introduction

Driven by the advantages enabled by MEA concepts, i.e. decreased fuel consumption and CO_2 and NO_x emissions reduction, in 2010 the electric power demand of commercial airplanes surpassed the 1 MVA milestone on-board of the *Boeing* 787 [137]. As a consequence of the established next steps towards all-electric propulsion, this figure is expected to double in 2020, i.e. when the maiden flight of a 2 MW hybrid-electric propulsion system, developed in a collaboration among *Airbus*, *Siemens*, and *Rolls-Royce* [20], is scheduled. Furthermore, according to *Airbus* forecasts, the power requirements of next generation single aisle aircraft should reach 20 MW in the next decades [21]. Motivated by these trends, the power electronics roadmap for next generation aerospace applications is targeting to significantly improve efficiency η and gravimetric power density γ of power converters [222]. As an example, **Fig. 9.1** compares the goals in the $\eta\gamma$-performance space of two on-going projects focusing on MEA, with the figures of comparable (in terms of power rating) state-of-the-art prototypes (yellow dots). The *Horizon2020* European Project 636170 - *Integrated, Intelligent Modular Power Electronic Converter* (I2MPECT) [138] (red dots) and the NASA Government Contract NNX14AL79A - *High Speed, High Frequency Air-Core Machine and Drive* [223] (blue dots) set the minimum targets at $\eta = 98\,\%$ and $\gamma = 10\,\mathrm{kW/kg}$. From the comparison

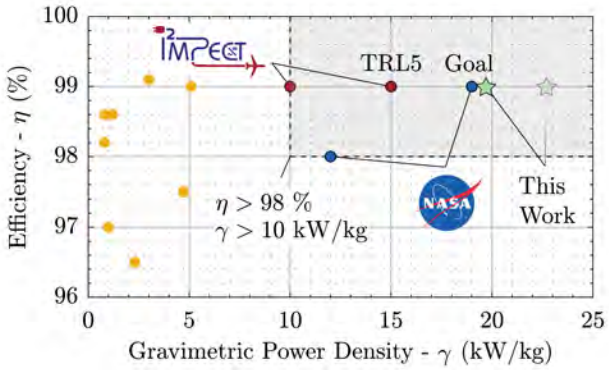


Fig. 9.1: $\eta\gamma$-performance space presenting the performance goals ($\eta > 98\,\%$ and $\gamma > 10\,\mathrm{kW/kg}$) of on-going projects focusing on power electronics for next generation aerospace applications, and the results of this work. The γ-target is significantly higher compared to the figures of state-of-the-art prototypes.

in **Fig. 9.1**, it becomes evident that the most demanding improvement with respect to the state-of-the-art concerns γ. The reason is identified in the fact that, for each kg on-board of an aircraft, roughly 1.7 t of fuel are burned, and 5.4 t of CO_2 are emitted per year from all the air traffic [137]. Thus, a reduction of weight can significantly help to meet the lowered emissions target [137]. The weight breakdown analysis of modern power converters reveals that cooling systems, and magnetic and capacitive filter components are the main contributors to the overall converters weight [224]. Increasing the switching frequency in conventional converter topologies (to reduce volume and weight of the magnetic components) faces a trade-off with maintaining a high efficiency, therefore different approaches must be evaluated. Moreover, the growing power demand on-board of MEA is inevitably accompanied by an increasing DC voltage level of the installed energy distribution network, e.g. from the actual 540 V [138] to 3 kV of the above mentioned prototype [21] (and reasonably further). Thus, as in general medium-voltage (MV) applications, conventional converter solutions will face limitations, e.g. in terms of blocking capability of power semiconductor devices and availability of capacitors [225]. Finally, high reliability, scalability, and reduced design and maintenance efforts are key features in the aircraft industry [136], hence also these aspects must be considered in the selection of alternative topologies. Multi-cell converters enable improved semiconductor performance and the

Tab. 9.1: Specifications of the considered 3-Φ inverter.

	Description	Value
V_{dc}	DC-link voltage	1000 V
P_{out}	output power	45 kW
f_{out}	output frequency	2 kHz
M_{index}	modulation index	0.9

downsizing of the magnetic components because of the diminished harmonic content of their voltage waveforms [226]. Consequently, they are identified as a candidate approach to meet the defined performance targets. Unfortunately, their increased complexity inevitably worsen the system reliability, thus providing redundancy becomes mandatory. The effectiveness of this strategy is proven with a decade of successful operation in MV applications [227]. However, only modular multi-cell topologies can combine high reliability with superior $\eta\gamma$-performance, since few redundant cells, which have a negligible impact on the converter power density (in case of a high total number of cells), are sufficient to achieve even higher reliability figures than conventional solutions [228]. Their modular structure additionally ensures straight-forward scalability, facilitating a flexible design [225].
Ultimately, in order to extend the advantages of modularity also to the electric machines connected to these converters, e.g. compressor units for the environmental control system, machines with several (more than three) sets of windings are preferred [229]. In this case, fault-tolerant operation after a partial failure (involving one or few sets of windings and/or corresponding inverter phases) is ensured, increasing the overall system reliability. Moreover, when the power electronics is integrated into the machine housing, additional advantages, e.g. in terms of system power density, and installation costs and complexity, are enabled [207].
The goal of this chapter is to investigate the achievable $\eta\gamma$-performance of a fault-tolerant modular multi-cell 3-Φ inverter designed according to the requirements of next generation aerospace applications, and to the specifications given in **Tab. 9.1**. **Section 9.2** discusses an analytical study, based on loss models and FoM, comparing the semiconductor performance in conventional and multi-cell inverter topologies. **Section 9.3** introduces the reliability figures of multi-cell converters, and evaluates the impact of different redundancy approaches on their power density. **Section 9.4** presents the trend towards Integrated Modular Motor Drives (IMMD) applied to modular multi-

cell inverters. Since the Stacked Polyphase Bridge (SPB) converter combines all the highlighted features, it is finally identified as the best candidate solution to fulfill the targeted performance. Hence, it is optimized in **Section 9.5** for the specifications of interest, achieving $\eta = 99\,\%$ and $\gamma = 22.8\,\mathrm{kW/kg}$ ($19.2\,\mathrm{kW/kg}$ adding one redundant cell, see **Fig. 9.1**). Finally, **Section 9.6** summarizes the results.

9.2 Performance Analysis of Power Semiconductors

The switching and conduction losses in the power semiconductors dominate the loss breakdown of modern power converters featuring a high power density [41]. Hence, accurate loss models based on the characteristics of state-of-the-art semiconductors can provide sensible estimations of their overall performance, and enable the comparison in terms of efficiency among different converter concepts. Therefore, with the final aim of designing a 99 % efficient 45 kW weight-optimized 3-Φ inverter, a semiconductor performance study is presented in this section.

9.2.1 Loss Models of Power Semiconductors

The semiconductors loss analysis is based on a conventional (single-phase) bridge-leg, for which switching and conduction loss models are developed and discussed herein.

In case of a hard-switching transition, the switching losses P_{sw} are separated in current-independent and current-dependent fractions [230]. The switching losses of soft-switching transitions are neglected, since proven to be typically one order of magnitude smaller [53]. The current-independent fraction of P_{sw}, i.e. $P_{\mathrm{sw,oss}} = f_{\mathrm{sw}} V_{\mathrm{dc}} Q_{\mathrm{oss}}\big|_{V_{\mathrm{dc}}}$ models the losses due to the charging and discharging processes of the parasitic output capacitance C_{oss} of the power semiconductors, with $Q_{\mathrm{oss}}\big|_{V_{\mathrm{dc}}}$ indicating the charge stored in C_{oss} when charged from 0 V to the DC voltage V_{dc}. If present, the additional charge Q_{rr} associated with the reverse recovery phenomenon should be added to Q_{oss}, but is neglected herein. The current-dependent fraction of P_{sw}, i.e. $P_{\mathrm{sw,vi}} = f_{\mathrm{sw}} 1/2 V_{\mathrm{dc}} I_{\mathrm{sw}} \left(t_{\mathrm{r,i}} + t_{\mathrm{f,v}}\right)$ is caused by the simultaneous existence of V_{dc} and of the switched current I_{sw} at the terminals of the turning on device. An experimental validation of this model can be observed analyzing a hard-switching transition of a phase-leg, e.g. in a Double Pulse Test setup with

inductive load: first the device current i_{ds} rises with a certain $^{di_{ds}}/_{dt}$ until I_{sw} is reached, while the voltage across the device v_{ds} is clamped to V_{dc}. As soon as $i_{ds} = I_{sw}$ (if the reverse recovery phenomenon is neglected), v_{ds} starts to decrease from V_{dc} to 0 V with a certain $^{dv_{ds}}/_{dt}$. Expressing the current rise time $t_{r,i}$ and the voltage fall time $t_{f,v}$ as $^{I_{sw}}/_{di_{ds}/dt}$ and $^{V_{dc}}/_{dv_{ds}/dt}$ respectively, highlights the possible reduction of switching losses, or the complementary increase of switching frequency f_{sw}, enabled by fast switching power semiconductors, e.g. SiC and GaN devices. Additionally, it clarifies how this benefit vanishes if the maximum switching speed is limited from external factors: for example, partial discharge induced motor windings isolation aging, and overvoltages due to reflections of voltage pulses in case of long motor cables are typical reasons to limit the $^{dv_{ds}}/_{dt}$ below 10 V/ns [231], whereas voltage oscillation and overshoot at the gate terminal of the device or at the bridge-leg switch node define the maximum $^{di_{ds}}/_{dt}$ [39].
The conduction losses P_{cond} are calculated as $R_{ds,on}I^2_{out,RMS}$, where $R_{ds,on}$ is the on-state resistance of the power semiconductors alternatively conducting the phase current. Sinusoidal phase currents and voltages with peak values $V_{out} = {}^{V_{dc}}/_{2}$ (no third harmonic injection) and $I_{out} = {}^{2\,P_{out}}/_{V_{out}}$, i.e. $I_{out,RMS} = {}^{2\sqrt{2}\,P_{out}}/_{V_{dc}}$, are assumed. Finally, $P_{semi} = P_{sw} + P_{cond}$ constitutes the overall semiconductors losses.

9.2.2 Figure of Merit of Power Semiconductors

The accuracy of the proposed loss models heavily depends on the underpinning parameters, e.g. $R_{ds,on}$ and Q_{oss}. A practical approach to consider and compare different power semiconductors is based on the corresponding FoM, and is introduced in this section [122]. A FoM consists of a numeric value obtained combining several characteristics of a device (e.g. of a power semiconductor), appropriately selected to be representative of its performance. The FoM calculated as $^{1}/_{(R_{ds,on}Q_{oss})}$ [123] is considered as a promising indicator for the analysis of interest, and therefore preferred [199]. **Fig. 9.2** summarizes the selected FoM of more than hundred commercially available Si, SiC, and GaN power semiconductors as function of their blocking voltage $V_{ds,MAX}$ (75 V… 1.7 kV). As can be noticed, a linear trend characterizes each semiconductor material in logarithmic-scale, hence

$$\mathrm{FoM}(V) = \frac{1}{R_{ds,on}Q_{oss}\big|_V} = aV^k \tag{9.1}$$

best interpolates the data. The coefficients of the model, different for each semiconductor material, are reported in **Tab. 9.2**. It is worth noticing how,

Tab. 9.2: Fitting coefficients of the FoM model aV^k.

	Si	GaN	SiC
a	$1.23 \cdot 10^{13}$	$1.63 \cdot 10^{12}$	$2.55 \cdot 10^{12}$
k	−2.05	−1.40	−1.48
$V_{ds,MAX}$ (V)	75... 900	100... 650	650... 1700

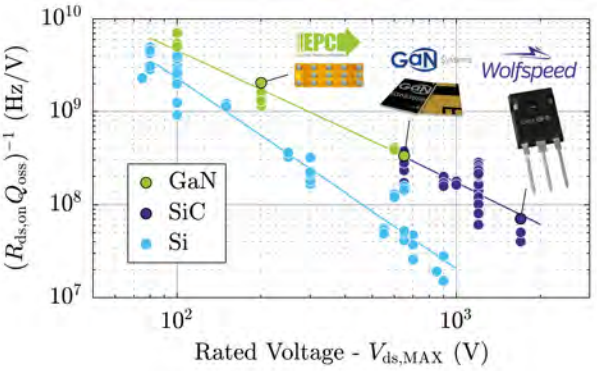


Fig. 9.2: FoM calculated as $1/(R_{ds,on}Q_{oss})$ of most of the currently commercially available Si, SiC, and GaN power semiconductors, as function of their blocking voltage. The model FoM = aV^k with the fitting coefficients reported in **Tab. 9.2** best interpolates the data.

GaN and SiC (comparable with each other) outperform Si as a result of their higher breakdown electric field and bandgap energy, and that all FoM trends scale over proportionally with respect to voltage, since $|k| > 1$ in all cases.

9.2.3 Conventional Inverter Concept

The proposed semiconductors loss models and FoM are combined in this section to evaluate the η-limit of a conventional inverter phase-leg. The specifications of **Tab. 9.1** are considered as reference for one phase-leg, i.e. $V_{dc} = 1000\,\text{V}$ and $P_{out,phase} = 15\,\text{kW}$. The values of $R_{ds,on}$ and Q_{oss} are calculated (eventually extrapolated) with the fitting coefficients of the FoM model (**Tab. 9.2**). In this ideal approximation $V = V_{dc} = V_{ds,MAX}$ is assumed, whereas in a real design a certain margin between V_{dc} and $V_{ds,MAX}$ is necessary, e.g. $V_{dc} \leq 2/3\, V_{ds,MAX}$.

To eliminate in a first step the dependency on the mentioned switching speed constraints, $\mathrm{d}i_{\mathrm{ds}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t \to \infty$ are assumed, i.e. $P_{\mathrm{sw,vi}} = 0$ and

$$P_{\mathrm{sw}} = P_{\mathrm{sw,oss}} = f_{\mathrm{sw}} V_{\mathrm{dc}} Q_{\mathrm{oss}}\big|_{V_{\mathrm{dc}}} = f_{\mathrm{sw}} \frac{V_{\mathrm{dc}}^{1+|k|}}{a} \frac{1}{R_{\mathrm{ds,on}}} \tag{9.2}$$

results. It can be noticed that $P_{\mathrm{cond}} \propto R_{\mathrm{ds,on}}$, while $P_{\mathrm{sw}} \propto 1/R_{\mathrm{ds,on}}$, thus $P_{\mathrm{cond}} \propto P_{\mathrm{sw}}^{-1}$. In fact, for a fixed voltage, increasing the chip area to reduce $R_{\mathrm{ds,on}}$ leads to a counter proportional increase of C_{oss}, consequently of Q_{oss}, and hence of P_{sw} in the considered model.
The described trend is visible in **Fig. 9.3(a)**, where η of a Si phase-leg is illustrated as function of f_{sw} and $R_{\mathrm{ds,on}}$. Fixing f_{sw}, P_{cond} and P_{sw} vary as described, leading to a minimum P_{semi}, when $P_{\mathrm{cond}} = P_{\mathrm{sw}}$. The weight breakdown analysis of modern power converters reveals that magnetic and capacitive filter components are the principal contributors to the overall weight. Since a higher f_{sw} reduces the filtering effort (i.e. the size of the filter components), the maximum f_{sw} ensuring the η-target is highlighted. $\eta = 99\,\%$ can only be reached if $f_{\mathrm{sw}} < 28\,\mathrm{kHz}$, even considering only P_{semi}.
The same calculations are repeated for a SiC phase-leg and the results are shown in **Fig. 9.3(b)**. Since $\mathrm{FoM_{SiC}}(1000\,\mathrm{V}) = 92\,\mathrm{MHz/V} \approx 10\,\mathrm{FoM_{Si}}(1000\,\mathrm{V})$, superior performance is expected. The η-target is shifted to 99.5 %, assuming a more reasonable loss breakdown where P_{semi} constitutes half of the overall allowed losses. Nevertheless, the f_{sw}-limit is increased by approximately a factor of three to 78 kHz. This preliminary result justifies the narrowing of the focus to WBG semiconductors.

9.2.4 Multi-Cell Inverter Concepts

The FoM-based analysis of achievable η and f_{sw} confirms the superior performance of WBG power semiconductors compared to Si, but does not take advantage yet of the over proportional voltage scaling of the FoM (notice $|k| > 1$ in **Tab. 9.2**). To evaluate this aspect, the performance of a generic multi-cell (e.g. Flying Capacitor or Modular Multi-Level) power converter concept is analyzed in this section adapting the previously developed procedure.
A phase-leg formed by the series connection of N cells, each rated for reduced power $P_{\mathrm{out,i}} = P_{\mathrm{out}}/N$ and DC voltage $V_{\mathrm{dc,i}} = V_{\mathrm{dc}}/N$, is considered to model the different multi-cell converter concepts. To deliver the same overall output power $P_{\mathrm{out,N}} = P_{\mathrm{out}} = N\,P_{\mathrm{out,i}}$, $I_{\mathrm{out,i}} = I_{\mathrm{out}}$ is necessary. In the rest of the section, subscript i defines a quantity relative to a single cell, whereas N

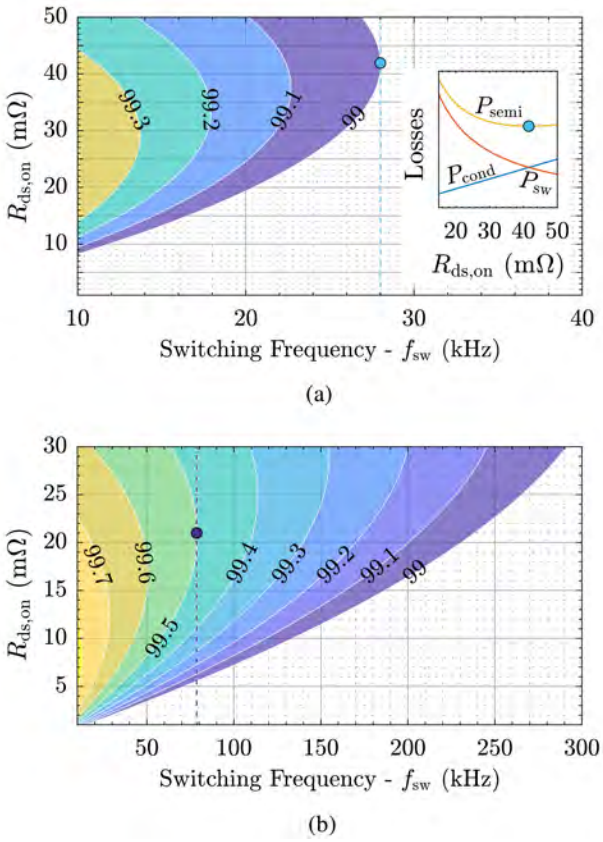


Fig. 9.3: The η-limit of **(a)** a Si and **(b)** a SiC (V_{dc} = 1000 V and $P_{out,phase}$ = 15 kW) bridge-leg as function of f_{sw} and $R_{ds,on}$. η = 99.5 % can only be achieved with WBG semiconductors in the considered f_{sw} range.

indicates the respective total for the complete phase-leg. Thus,

$$P_{semi,N} = N(P_{sw,i} + P_{cond,i}) \tag{9.3}$$

$$= N\left(f_{sw}\frac{(V_{dc}/N)^{1+|k|}}{a}\frac{1}{R_{ds,on}} + R_{ds,on}\left(\frac{2\sqrt{2}\,P_{out}/N}{V_{dc}/N}\right)^2\right) \tag{9.4}$$

$$= \frac{P_{sw}}{N^{|k|}} + NP_{cond} \tag{9.5}$$

is obtained and the optimum number of cells N_{opt} can be derived as

$$\frac{\mathrm{d}P_{\text{semi,N}}}{\mathrm{d}N} = 0 \quad \longrightarrow \quad N_{\text{opt}} = \sqrt[1+|k|]{\frac{|k|\,P_{\text{sw}}}{P_{\text{cond}}}}. \tag{9.6}$$

If $|k| = 1$ is assumed, $N_{\text{opt}} = \sqrt{P_{\text{sw}}/P_{\text{cond}}}$. The corresponding $P_{\text{semi,N}} = 2\sqrt{P_{\text{sw}}\,P_{\text{cond}}}$ features a minimum coinciding with the minimum P_{semi}. Consequently, if $|k| \leq 1$, multi-cell approaches would not be beneficial in terms of semiconductor performance.
In reality $|k| > 1$, hence, considering e.g. $N = 6$, $\text{FoM}_{\text{GaN}}(1000\,\text{V}/6 = 167\,\text{V}) = 1.26\,\text{GHz/V}$ is 2.3 times larger than $6\,\text{FoM}_{\text{SiC}}(1000\,\text{V}) = 0.55\,\text{GHz/V}$, i.e. the FoM scales over proportionally with respect to voltage. Accordingly, superior semiconductor performance is expected when multi-cell concepts are adopted.
Differently from **Section 9.2.3**, in this case, for each (f_{sw}, $R_{\text{ds,on}}$)-pair, the corresponding N_{opt} is derived according to (9.6) and considered in (9.3) to calculate η. N_{opt} and η are overlaid in **Fig. 9.4** to summarize the obtained results for a GaN phase-leg. GaN scales similarly to SiC according to the selected FoM, but GaN devices are available with lower $V_{\text{ds,MAX}}$, thus preferred in the multi-cell approach. It can be noticed that for high f_{sw} and low $R_{\text{ds,on}}$ (i.e. high Q_{oss}) values, high N_{opt} values are preferred to compensate for otherwise dominating P_{sw}, whereas the opposite is true in the complementary half-plane (low f_{sw} and high $R_{\text{ds,on}}$ values). $\eta = 99.5\,\%$ can be achieved with $f_{\text{sw}} = 173\,\text{kHz}$ and $N = 6$. N is in fact limited to six, since the modeled FoM unrealistically diverges to ∞ for higher values of N, leading to $\eta \longrightarrow 100\,\%$. The selected ideal GaN semiconductor features $R_{\text{ds,on}} = 4\,\text{m}\Omega$ and $Q_{\text{oss}} \approx 210\,\text{nC}$. Overall, significantly better semiconductor performance, e.g. $\eta > 99.5\,\%$ with $f_{\text{sw}} > 100\,\text{kHz}$, is achieved considering the multi-cell inverter concept. Volume and weight of the overall converter are assumed to reduce accordingly, since lower losses require lower cooling effort, i.e. smaller heat sinks, and a higher f_{sw} enables the downsizing of the filter and magnetic components.

9.3 Reliability Analysis of Multi-Cell Inverters

Since decades, failure-safe and fault-tolerant mechanical systems relying on redundancy are the core of the aircraft design industry [232]. In parallel with the paradigm shift towards MEA, higher reliability, eventually exceeding the capability of current solutions, is nowadays also required in power converters for aerospace applications [233]. In fact, a reliable system in a

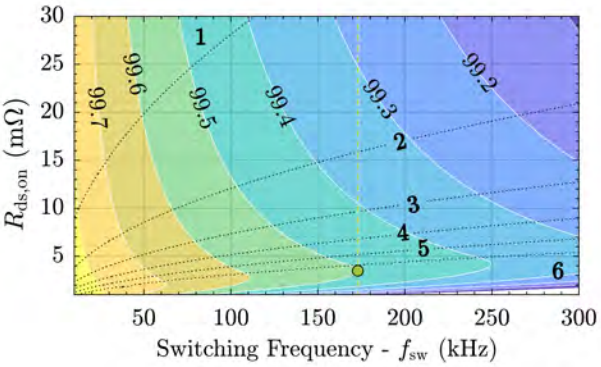


Fig. 9.4: The η-limit of a multi-cell GaN phase-leg (V_{dc} = 1000 V and $P_{out,phase}$ = 15 kW) as function of f_{sw} and $R_{ds,on}$. The multi-cell approach enables a significant performance improvement compared to the conventional ones, maintaining the η-target up to f_{sw} = 173 kHz when N = 6.

critical environment does not only guarantee the safety of its users, but as well reduces maintenance costs, extends operating times, and avoids costly unexpected interruptions of service [234]. Nevertheless, efficiency and low weight still maintain high priority among the specifications of power converters for aerospace applications [138], resulting in the challenge of identifying topologies able to simultaneously combine all the mentioned features.
In this section, the reliability problem is formalized, defining the framework for the comparison of different multi-cell inverter topologies. Finally, it is proven how the optimization of multi-cell inverters cannot be separated from an accurate analysis of their reliability. The higher number of cells, in fact, significantly affects the reliability of the overall converter, and this drawback can only be compensated by installing redundant elements, which negatively impact the power density.

9.3.1 Reliability Model

A common approach to formalize reliability problems [235] is based on the definition of the reliability function of a component. $R_{comp}(t)$ states the probability that a component does not fail until time t, i.e. that it is able to perform its associated function as intended and when required. The expectation of the continuous operating time of that component, i.e. the mean time between

(to) failures (MTBF), is obtained from the area underlying $R_{\text{comp}}(t)$ as

$$\text{MTBF}_{\text{comp}} = \int_0^\infty R_{\text{comp}}(t)\text{d}t. \tag{9.7}$$

Assuming a constant failure rate λ over time (only random failures occurring), a typical expression for $R_{\text{comp}}(t)$ is the unitary decaying exponential function

$$R_{\text{comp}}(t) = e^{-\lambda t}, \tag{9.8}$$

where $\lambda = 1/\text{MTBF}_{\text{comp}}$ since $\int_0^\infty e^{-\lambda t} = 1/\lambda$.
Engineering systems in critical environments are typically formed by the interconnection of several components, and ensure high reliability by means of redundancy. In the interest of this analysis, systems formed by $K + Q$ components, where K indicates the number of components necessary for the system to operate as intended, and Q is the number of installed redundant components, are considered. Moreover, all components are assumed to have the same $R_{\text{comp}}(t)$ (time dependency is not any more indicated). In this case, the reliability function of the system R_{sys} can be calculated [234] as

$$R_{\text{sys}} = \sum_{r=K}^{K+Q} \binom{K+Q}{r} R_{\text{comp}}^r (1 - R_{\text{comp}})^{K+Q-r}. \tag{9.9}$$

Finally, the mean time between failure of the system MTBF_{sys} can be estimated applying the definition of MTBF (expressed in (9.7) for R_{comp}) to R_{sys} obtained with (9.9). In case $K > 1$ and $Q = 0$ (system without redundancy), $R_{\text{sys}} = R_{\text{comp}}^K$ and $\text{MTBF}_{\text{sys}} = \text{MTBF}_{\text{comp}}/K$ can be significantly smaller than $\text{MTBF}_{\text{comp}}$. Differently, in case $K > 1$ and $Q \geq 1$ (system with redundancy), MTBF_{sys} can exceed $\text{MTBF}_{\text{comp}}$, depending on the ratio between K and Q, i.e. the reliability of the system can exceed the one of the single component, as aimed for when installing redundant elements.

9.3.2 Redundancy in Multi-Cell Inverters

The developed reliability model is applied in this section to calculate the reliability functions characterizing two identified categories of multi-cell inverters. Conventional inverter solutions are not included in the comparison, since their performance is judged insufficient to meet the target defined by the aircraft industry.
From the system point-of-view, multi-cell 3-Φ inverters without redundant

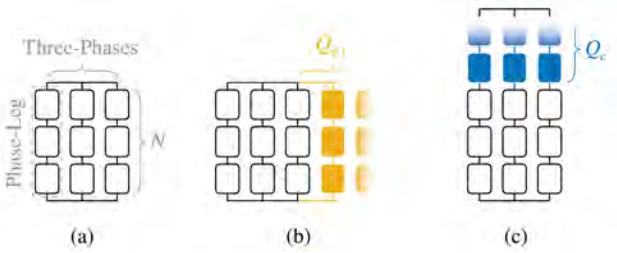


Fig. 9.5: System level structure of the considered multi-cell 3-Φ inverters in case $N = 3$, comparing **(a)** no redundancy, **(b)** phase-leg level redundancy, and **(c)** cell-level redundancy approaches.

elements are modeled first as series connection of N identical components, i.e. phase-leg cells (R_{cell}, $\text{MTBF}_{\text{cell}}$), forming the phase-leg system ($R_{\text{p-l}}$). Hence, three identical phase-leg systems, composed of N cells each, form the overall 3-Φ inverter system (R_{inv}, MTBF_{inv}). Thus, the total number of cells is $N_{\text{tot}} = 3\,N$, as shown in **Fig. 9.5(a)** for $N = 3$. The abstract concepts of component and system are therefore now transferred to the one phase-leg cell, the three phase-legs, and the 3-Φ inverter.

No Redundancy

Since the functioning of a phase-leg in multi-cell inverters generally requires the correct operation of all N cells forming it, $K = N$. Therefore, $R_{\text{p-l}} = R_{\text{cell}}^{N}$, $R_{\text{inv}} = R_{\text{p-l}}^{3} = R_{\text{cell}}^{3\,N}$, and consequently $\text{MTBF}_{\text{inv}} = {}^{\text{MTBF}_{\text{cell}}}/_{3\,N}$. **Fig. 9.6** shows R_{cell} (red) and R_{inv} (black dashed) in case of $N = 9$. MTBF_{inv} can be compared to $\text{MTBF}_{\text{cell}}$ visualizing the reduction of area underlying the respective reliability functions.

Phase-Leg Level Redundancy

Inverter topologies such as Flying Capacitor (FCC) and Neutral Point Clamped (NPC) converters, which have a multi-cell but not a modular phase-leg structure, are grouped in this category. In this case, as shown in **Fig. 9.5(b)**, redundancy can be introduced in a first approximation only by installing additional parallel phase-legs. Accordingly, N_{tot} can be calculated as $N_{\text{tot,p-l}} = N(3+Q_{\text{p-l}})$. In case of failure, the faulty phase-leg can be disconnected and replaced by any (to simplify the derivation) redundant one. Even if more convenient strategies to handle certain types of failures are proposed in literature [236],

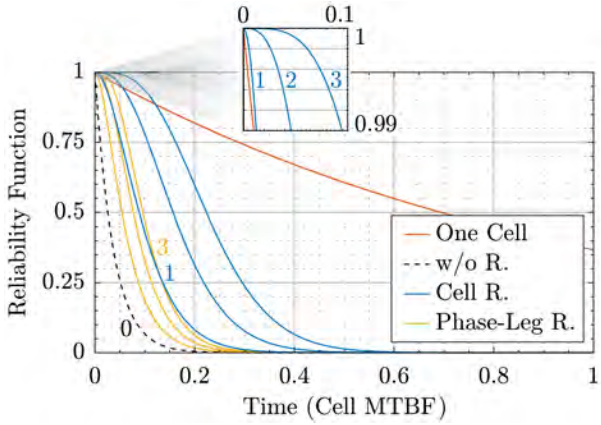


Fig. 9.6: R_{cell} (red) and R_{inv} when no redundancy (black dashed), phase-leg level redundancy (yellow), or cell-level redundancy (blue) are considered. The area underlying the curves defines MTBF_{inv} of the corresponding solution. The value of Q associated with a certain R_{inv} curve is indicated with matching colors.

only this generally valid approach is considered in this analysis.
To update R_{inv} in presence of redundancy, (9.9) must be computed with $R_{\text{comp}} = R_{\text{p-l}} = R_{\text{cell}}^{N}$, $K = 3$ for the number of phases, and any $Q = Q_{\text{p-l}} \geq 1$. The results for $Q_{\text{p-l}} = 1\ldots 3$ and $N = 9$ are shown in yellow in **Fig. 9.6**. $Q_{\text{p-l}} = 3$ is indicated to highlight the corresponding R_{inv}. A weak increase of MTBF_{inv} for each redundant phase-leg can be noticed.

Cell-Level Redundancy

Inverter topologies such as Modular Multi-Level (MMLC) and Cascaded H-Bridge (CHB) converters are grouped in this category, since they feature a modular multi-cell phase-leg structure, which allows to directly add redundant cells to each phase-leg, as shown in **Fig. 9.5(c)**. Thus, $N_{\text{tot,c}} = 3(N + Q_{\text{c}})$. In case of failure, the faulty cell can be bypassed, and a redundant one (in the same phase-leg) operated. Hence, $R_{\text{p-l}}$ can be calculated according to (9.9) with $R_{\text{comp}} = R_{\text{cell}}$, $K = N$ for the number of cells, and $Q = Q_{\text{c}} \geq 1$. R_{inv} obtained as $R_{\text{p-l}}^{3}$ for $Q_{\text{c}} = 1\ldots 3$ and $N = 9$ are shown in blue in **Fig. 9.6**, where $Q_{\text{c}} = 1$ is also indicated to highlight the corresponding R_{inv}. A more significant increase of MTBF_{inv} for each redundant cell can be noticed in this case.

9.3.3 Effect of Redundancy on Power Density

The discussed modeling of the two considered redundancy approaches provides the basis to define the scaling trends in terms of power density of multi-cell inverters with respect to reliability.
To enable this evaluation, $\mathrm{MTBF}_{\mathrm{inv}}$ is calculated as described in the previous section for the cases featuring $Q_{\text{p-l}} = 0 \ldots 3$, $Q_{\mathrm{c}} = 0 \ldots 3$, and $N = 3$, 6 and 9. After computing the percentage ratio $\mathrm{MTBF}_{\div} = 100\ {}^{\mathrm{MTBF}_{\mathrm{inv}}}/_{\mathrm{MTBF}_{\mathrm{cell}}}$, i.e. the ratio between the areas underlying each R_{inv} and R_{cell}, the obtained results are shown in **Fig. 9.7** as function of N_{tot}. $\mathrm{MTBF}_{\mathrm{cell}}$ is technology and design dependent, therefore a relative expression for $\mathrm{MTBF}_{\mathrm{inv}}$, i.e. $\mathrm{MTBF}_{\div}$, is preferred for the sake of generality. Since $\mathrm{MTBF}_{\mathrm{inv}} < \mathrm{MTBF}_{\mathrm{cell}}$ in all the cases, $\mathrm{MTBF}_{\div} < 100\,\%$. The system diagrams help visualizing again the evolution of the circuit structures in presence of the two considered levels of redundancy: $N = 3$ and $Q_{\text{p-l}} = Q_{\mathrm{c}} = 1$ ($N_{\mathrm{tot}} = 12$) are shown as an example.
In the graph, white dots indicate $\mathrm{MTBF}_{\div}$ with $Q = 0$, which follow the trend $N_{\mathrm{tot}} = 3\,N$ and $\mathrm{MTBF}_{\div} = {}^{100}/_{3\,N}\,\%$ highlighted by the arrow. Without redundancy, $\mathrm{MTBF}_{\div}$ drops $\propto {}^{1}/_{N}$, e.g. resulting in $\mathrm{MTBF}_{\mathrm{inv}} \approx 4\,\%\ \mathrm{MTBF}_{\mathrm{cell}}$ already with $N = 9$ ($N_{\mathrm{tot}} = 27$). Additionally, for a fixed value of N, two different splines (yellow and blue) describe the increasing trends of $\mathrm{MTBF}_{\div}$, depending on $Q_{\text{p-l}}$ and Q_{c}, according to the proposed model. It can be noticed that the values of $\mathrm{MTBF}_{\div}$ obtained with $Q_{\text{p-l}} = 3\,Q_{\mathrm{c}}$ are comparable between each other, e.g. $\mathrm{MTBF}_{\div} \approx 30\,\%$ for $N = 3$, $Q_{\text{p-l}} = 3$, and $Q_{\mathrm{c}} = 1$. In fact, e.g. installing one redundant cell per phase-leg ($Q_{\mathrm{c}} = 1$) or three redundant phase-legs ($Q_{\text{p-l}} = 3$) provides almost the same level of redundancy (cf. **Fig. 9.6**). Generally, increasing Q, the overall reliability is improved at the expense of increased N_{tot}.
For higher values of N, a second trend is identified in **Fig. 9.7**. Given the expressions of $N_{\mathrm{tot,c}}$ and $N_{\mathrm{tot,p\text{-}l}}$, it is clear that increasing Q_{c} by one increases $N_{\mathrm{tot,c}}$ by three (independent of N), whereas increasing $Q_{\text{p-l}}$ by the same amount increases $N_{\mathrm{tot,p\text{-}l}}$ by N. This translates into significantly flatter slopes of the yellow splines for increasing N or, in other words, to a much more severe impact of the phase-leg redundancy approach on the overall power density. A possible countermeasure to this drawback is identified in realizing each phase-leg as parallel connection of several phase-legs designed for reduced power. Although N_{tot} would be significantly increased, the resulting cells with reduced power would have a smaller weight and/or volume, and a better trade-off between power density and reliability might be found at the expense of increased complexity. Differently, for high values of N, the effect of increasing Q_{c} (i.e. of cell-level redundancy) on the power density becomes

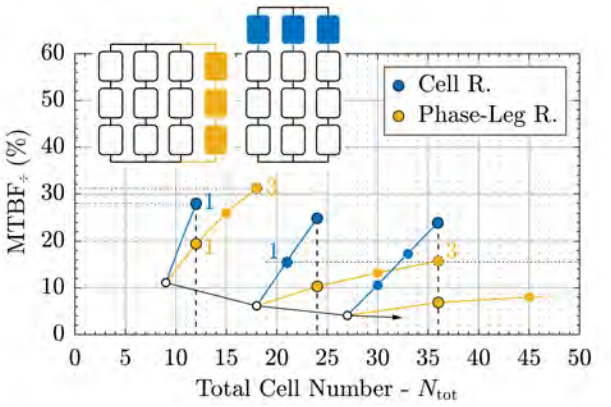


Fig. 9.7: MTBF÷ for $Q_{p\text{-}l} = 1...3$ (yellow), $Q_c = 1...3$ (blue), and $N = 3$, 6 and 9 as function of N_{tot}. The white dots indicate MTBF÷ with $Q = 0$. The system diagrams help visualizing the circuits structure in presence of the two levels of redundancy ($N = 3$, $Q_{p\text{-}l} = Q_c = 1$, and $N_{tot} = 12$).

even negligible.
Considering $Q_{p\text{-}l} = 3\,Q_c$ (e.g. $Q_c = 1$ and $Q_{p\text{-}l} = 3$), the two expressions describing the reduction of power density in converters adopting the two considered redundancy approaches are found as

$$\delta_{p\text{-}l} = \frac{3}{3 + Q_{p\text{-}l}}\delta_o \quad \overset{Q_{p\text{-}l}=3}{\longrightarrow} \quad \frac{\delta_o}{2} \tag{9.10}$$

and

$$\delta_c = \frac{N}{N + Q_c}\delta_o \quad \overset{Q_c=1}{\longrightarrow} \quad \frac{N}{N+1}\delta_o \quad \overset{N>>1}{\longrightarrow} \quad \delta_o, \tag{9.11}$$

for phase-leg and cell-level redundancies respectively. δ_o indicates the power density (with $Q = 0$) of a converter to which both redundancy approaches are ideally applicable. Consequently, $\delta_c \approx \delta_o = 2\,\delta_{p\text{-}l}$ holds when $N >> 1$. Therefore, when targeting a high reliability figure in a power density-optimized design, a converter topology where cell-level redundancy is possible must be generally preferred, since to guarantee the same level of redundancy, even twice the power density can be achieved (e.g. in case $Q_c = 1$ and $Q_{p\text{-}l} = 3$).
It is important to mention that a comparison in terms of power density and reliability of different converters should also take into account the inevitably

different designs of the cells forming them, since different designs might lead to incomparable power density and reliability figures. However, this aspect is strictly related to the specifications and to the selected topologies, and therefore cannot be discussed in general terms herein.
Moreover, although this analysis is limited to the power stage of the considered converters, it is worth mentioning that modularity is necessary, and must be extended to the overall converter, e.g. to control and measurement circuits, in order not to introduce a different bottleneck in the increase of reliability [237].

9.3.4 Safe Operating Time

The definition of MTBF introduced in **Section 9.3.1** leads to $R_{\text{comp}}(\text{MTBF}_{\text{comp}}) = e^{-1} = 0.37$, i.e. when $t = \text{MTBF}_{\text{comp}}$ the component failure probability results as $1 - R_{\text{comp}} = 63\,\%$, unacceptable in the critical application of interest and independent of λ. A different reliability indicator, i.e. the Safe Operating Time (SOT), defined as the time at which R_{inv} drops below a certain, still high (e.g. 99 %), reliability threshold, can be introduced to better compare the different redundant multi-cell solutions with the single cell baseline. The zoom of **Fig. 9.6**, highlighting $R_{\text{inv}} > 99\,\%$, shows how the cell-level redundancy approach (blue) with $N = 9$ and $Q_{\text{c}} \geq 1$ can even compete with the single cell (red) in terms of SOT, even if $\text{MTBF}_{\div} \approx 10\,\%$.

9.4 Integrated Modular Motor Drives

The two most common modular multi-cell inverter topologies, to which cell-level redundancy can be applied, are the CHB converter and the MMLC [234]. Unfortunately, severe limitations prevent their usage in power density oriented designs at the specified voltage and power ratings. The CHB converter requires an isolated, and therefore inevitably bulky, DC voltage supply per cell, while in the MMLC, a significant amount of capacitance needs to be installed at the DC-side of each cell to compensate for the output frequency power pulsation. Control schemes regulating the flow of fluctuating circulating currents to limit this drawback enable a reduction of the capacitance requirements [238], however, they are still insufficient to meet the power density targets. Additionally, it is worth mentioning that in applications involving electric machines, the system reliability can also be compromised by a failure of the load, e.g. due to the damaging of the motor windings isolation, which is at least as likely to occur as the considered failures in the

power stage [231]. For this reason, novel electric machine concepts often feature modular multi-phase stators with dedicated decoupled windings, able to tolerate a confined failure [229]. Accordingly, a trend towards compact modular multi-cell inverters, providing a power electronics interface suitable to drive multi-phase electric machines, can be identified in literature labeled as Integrated Modular Motor Drives (IMMD) [207].
Advantageously, IMMD in combination with multi-phase machines not only improve the system reliability. IMMD, in fact, are typically embedded in the machine housing, e.g. mounted on the end plate or on the surface of the stator iron, thus allowing to reduce the cables length, the electromagnetic emissions, design and installation costs and complexity, while increasing the system power density [239]. Since the mentioned benefits are the main design drivers in power electronics for the aerospace and automotive industries, special attention is nowadays placed on IMMD [240]. Minimizing the length of the cables connecting the inverter to the machine also prevents overvoltages due to the reflection of voltage pulses (which could occur in case of long cables), i.e. the limit on the maximum $^{dv_{ds}}/_{dt}$ can be increased [231] reducing the occurring switching losses (see **Section 9.2.1**). Adopting concentrated windings, a capacitive voltage divider rather than a transmission line best models the voltage distribution along the coil during a switching transient, i.e. the *first-turn* effect is not present [241]. Moreover, differently from the case of distributed windings, the maximum voltage difference between two adjacent turns is clearly defined, and therefore the isolation requirements can be reduced [231]. Finally, if the amplitude of the switched voltage waveform of each cell is below the partial discharge inception voltage of conventional windings isolation (typically above 1 kV [241]), $^{dv}/_{dt}$-filters and/or output filters can be omitted (depending on bearing current limits), pushing further the achievable power density.
A suitable IMMD converter topology combining all the mentioned advantages is the Stacked Polyphase Bridge (SPB) converter, originally developed for MV train applications twenty years ago [242], but recently re-proposed as an evolution of the Modular High Frequency (MHF) converter [243]. As illustrated in **Fig. 9.8**, each cell is formed by a 3-Φ inverter, therefore no power pulsation occurs at the DC-side, and the requirement of capacitance of each cell can be significantly reduced. Since the cell element is commercially available both as power module or as IC (depending on the voltage and power ratings), the design effort is minimized, and high availability is guaranteed. Moreover, with the integration of gate drivers into the power semiconductors packages [244], the power density of SPB converters can be pushed even further.

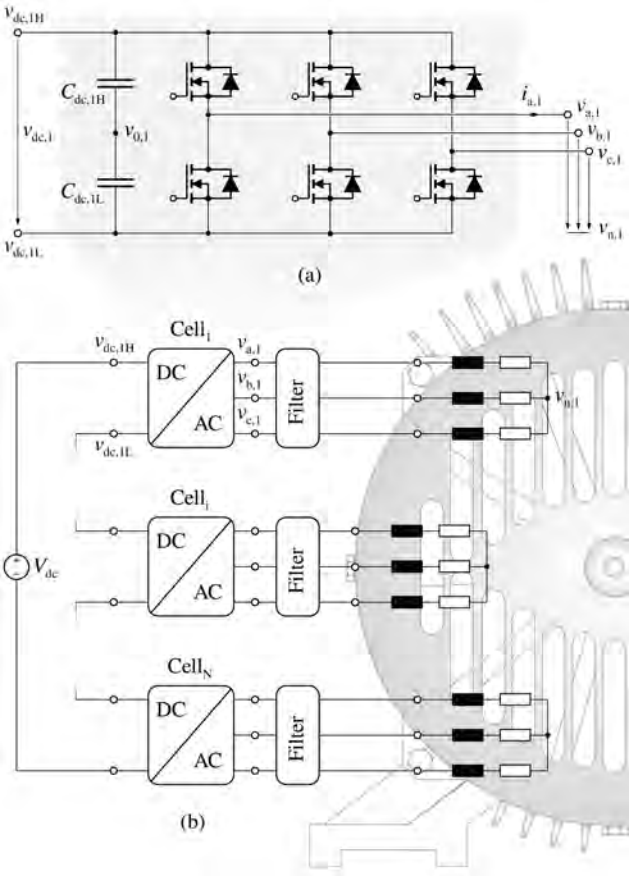


Fig. 9.8: Schematic of the SPB converter. The input series connection of **(a)** several identical 3-Φ inverter cells forms the **(b)** modular multi-cell structure of the overall converter, e.g. suitable to drive multi-phase electric machines.

Several recent studies on the SPB converter proved the stability of its DC-link [245], developed modulation schemes improving the harmonic content of the input waveforms [246], and distributed control strategies [247] even able to bypass failures affecting one cell [248]. Given its modular and scalable phase-leg structure and power dense cell design, this topology is identified as the most favorable converter solutions to fulfill the targeted performance.

9.5 Optimization of the Stacked Polyphase Bridge Inverter

In this section, the design of the 3-Φ SPB inverter is optimized with respect to gravimetric power density γ and efficiency η, according to the specifications reported in **Tab. 9.1**.

9.5.1 Optimization Algorithm - Design Space

The design variables subject to optimization, the constraints defining their range of variation, and the developed models computing the main contributions to the overall converter losses, weight, and volume are summarized herein.
First, the number of series connected cells N forming the SPB converter is varied from one to seven. A SPB converter with $N = 1$ is equivalent to a conventional 3-Φ inverter; this solution is considered only as benchmark for the multi-cell approaches. The nominal input voltage of each cell $V_{\mathrm{dc,i}} = {}^{V_{\mathrm{dc}}}/_{N}$, after considering a safety margin, defines the required power semiconductor voltage rating $V_{\mathrm{ds,MAX}}$. The best-in-class power device according to the considered FoM is selected for each value of N, as summarized in **Fig. 9.2** and **Tab. 9.3**. Once the power stage is fixed, f_{sw} is varied from 50 kHz to 250 kHz. In case an LC output filter is desired, its corner frequency f_{c} is defined as the maximum frequency that guarantees enough attenuation to the f_{sw} harmonic component, but still avoids that f_{out}-related components can excite the resonance of the LC filter elements (see **Tab. 9.4**). Several values of $L_{\mathrm{out,i}}$, logarithmically spaced in a range that avoids excessive inductor current ripple, inductive voltage drop, and capacitive current are considered. These constraints form the output filter design space highlighted in **Fig. 9.9** and defined in **Tab. 9.4**. The value of $C_{\mathrm{out,i}}$ is calculated according to $L_{\mathrm{out,i}}$ and f_{c}. $C_{\mathrm{dc,i}}$ is defined solely to limit the switching frequency voltage ripple on $V_{\mathrm{dc,i}}$. Additional constraints on $C_{\mathrm{dc,i}}$ defined by the application, e.g. energy storage requirements, do not affect the comparison in relative terms and are therefore neglected.
For each design derived from the combination of all the values assumed by the sweeping variables, all voltage and current waveforms in the converter are generated with accurate and computationally efficient analytical models. The related losses in the power semiconductors are calculated according to the loss models described in **Section 9.2.1**. Volume and weight of the power and gate driver PCBs are extrapolated from available hardware prototypes. Losses,

Tab. 9.3: Best-in-class power semiconductors.

N	Power Semiconductor			$V_{ds,MAX}$	$R_{ds,on}$ @ 100 °C	Q_{oss} @ $V_{dc,i,MAX}$
= 1	*Wolfspeed*	C2M0045170D	[250]	1.7 kV	68 mΩ	284 nC
≥ 2	*GaN Systems*	GS66516B-T	[217]	650 V	46 mΩ	126 nC
≥ 6	*EPC*	EPC2047	[124]	200 V	10 mΩ	82 nC

Tab. 9.4: Parameters defining the *LC* output filter design space.

	Constraint	Value
$a_{f,out}$	$f_c > a_{f,out} f_{out}$	4
$a_{f,sw}$	$f_c < f_{sw}/a_{f,sw}$	5
$f_{sw,min}$	$a_{f,sw} a_{f,out} f_{out}$	40 kHz
$a_{i,C}$	$I_{C,out} < a_{i,C} I_{out}$	40 %
$a_{i,L}$	$I_{L,out,ripple} < a_{i,L} I_{out}$	100 %
a_v	$V_{L,out} < a_v V_{out}$	17 %

weight, and volume of auxiliary circuits, e.g. control and measurement, are estimated in the same way. The more significant losses and the weight and volume of L_{out} are calculated and optimized by the software presented in [221]. Volume and weight of $C_{out,i}$ and $C_{dc,i}$ are derived from an exhaustive analysis of most commercially available electrolytic, film, and multi-layer ceramic capacitors in the voltage range of interest. For the necessary capacitance value, the most compact available solution is selected. Volume and weight of the heat sink are calculated with the CSPI method [249], considering CSPI = 15 W/K dm³, ΔT = 40 °C, and a weight density of 1.35 kg/dm³ (all obtained from available hardware prototypes).

9.5.2 Optimization Results - Performance Space

The results of the described optimization procedure are summarized in the $\eta\gamma$-Pareto plot illustrated in **Fig. 9.10(a)**. Only the approaches with N = 1, 2, and 6 are shown, since these designs correspond to the ones where the selected power devices are operated each at the maximum allowed voltage, and therefore result in the best performing solutions. In this case, in fact,

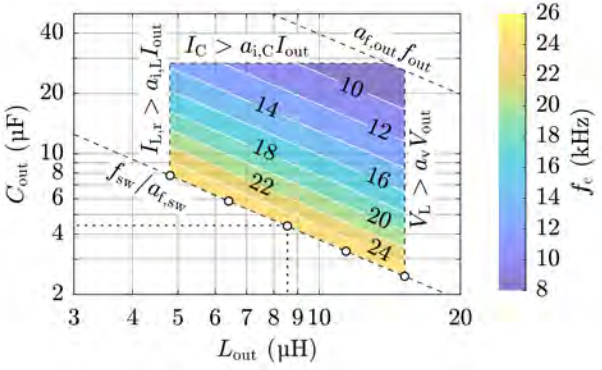


Fig. 9.9: *LC* output filter design space defined by the constraints reported in **Tab. 9.4** relative to f_{sw} and f_{out}, to the inductor current ripple ($I_{L,r}$), to the capacitive current (I_C), and to the inductive voltage drop (V_L). In case of variable frequencies, the minimum f_{sw} defines the maximum f_c and should be used to determine $a_{i,L}$, while the maximum f_{out} defines the minimum f_c and should be used for $a_{i,C}$ and a_v. Nominal V_{out} and I_{out} are generally considered. White dots highlight the selected combinations of L_{out} and C_{out} for a given f_{sw}.

the advantage of the over proportional improvement of the semiconductor performance with reduced blocking voltage requirement can best compensate for the drawbacks associated with the increased value of N, e.g. in terms of weight. Both multi-cell designs ($N = 2$ and 6) outperform the conventional 3-Φ inverter ($N = 1$) as expected from the analysis derived in **Section 9.2.4**. Although this more comprehensive study reasonably estimates more losses (since e.g. the total switching losses and the losses of L_{out} are considered), the expected trends are validated. The selected design (highlighted in **Fig. 9.10(a)** and described in **Tab. 9.5**) features $\eta = 99\,\%$ and $\gamma = 22.8\,\mathrm{kW/kg}$ (including the *LC* output filter of each cell), therefore meeting the aircraft industry targets (see **Fig. 9.1**). Details of its loss and weight breakdowns, relative to a single cell, are provided in **Fig. 9.10(b)** and **Fig. 9.10(c)**, respectively.
While the losses are almost evenly shared between the modeled source of losses, the weights are unequally distributed, with L_{out} responsible for $\approx 50\,\%$ of the cell weight. This prevents a further increase of γ, and is unexpected for a multi-cell converter. Typically, e.g. in FCC and MMLC, because of $V_{dc,i} = V_{dc}/N$ and due to the equivalent f_{sw}, i.e. $f_{sw,eq} \approx N f_{sw}$, the voltage-time area applied to L_{out} is reduced $\propto 1/N^2$. Thus, the value of L_{out} can be reduced by N^2 still ensuring the same current ripple of an equivalent single-

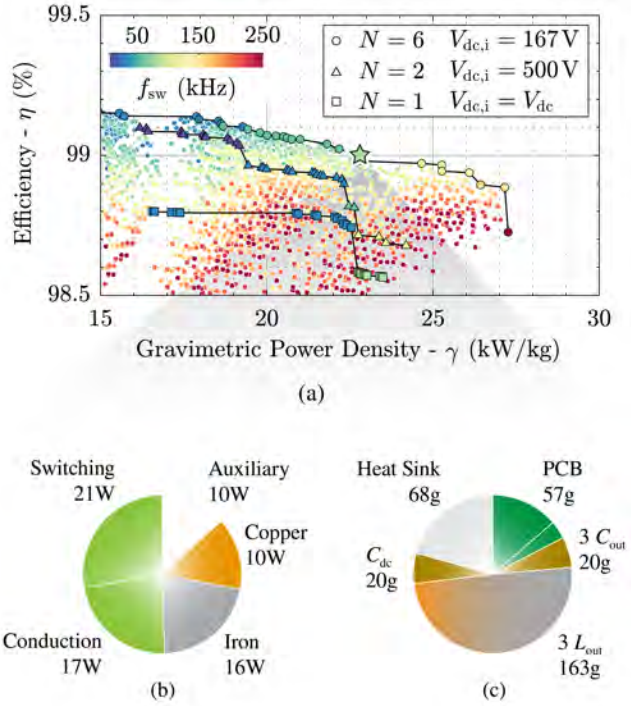


Fig. 9.10: (a) $\eta\gamma$-Pareto plot summarizing the results of the optimization of the 3-Φ SPB inverter. Both multi-cell solutions ($N = 2$ and 6) outperform the conventional inverter ($N = 1$). The selected design, featuring $\eta = 99\,\%$ and $\gamma = 22.8\,\mathrm{kW/kg}$ (including the LC output filter of each cell) is highlighted. Details of the **(b)** loss and **(c)** weight breakdowns of a single cell are provided.

cell solution. Hence, if the volume of a magnetic component is assumed to be proportional to the energy stored in it, also the volume (and approximately the weight) of L_{out} results reduced by N^2. In the case of the SPB converter, instead, the configuration of the cells does not enable the generation of $f_{sw,eq}$, and the reduction by factor N in the size of L_{out} enabled by $V_{dc,i} = V_{dc}/N$, is compensated by the necessity of N L_{out} elements per phase. Only the increase of f_{sw}, consequence of the over proportional voltage scaling of the FoM, allows to partially reduce the overall weight of the magnetic components. However, several motivations listed in **Section 9.4** suggest that the presence of LC output filters is unnecessary in IMMD based on SPB converters. Thus,

Tab. 9.5: Parameters of the selected Pareto design.

	Description	Value	Note
N	number of cells	6	
$V_{dc,i}$	cell input voltage	167 V	
f_{sw}	switching frequency	110 kHz	
L_{out}	output inductor	5 µH	E25/10 Kool Mμ
C_{out}	output capacitor	10 µF	200 V MMLC
C_{dc}	input capacitor	30 µF	200 V MMLC

Tab. 9.6: $SOT_{\div}$ and $\gamma\big|_{\eta=99\,\%}$ as function of N and Q_c.

		$SOT_{\div}$ (%) with N-Q_c cells					
R_{inv}(SOT)		1-0	2-0	2-1	6-0	6-1	6-2
0.9545	$\pm2\sigma$	33.3	16.7	164	5.56	62.8	159
0.9973	$\pm3\sigma$	„	„	650	„	246	978
0.9999	$\pm4\sigma$	„	„	3340	„	1260	8540
$\gamma\big\|_{\eta=99\,\%}$		–	19.3	12.9	22.8	19.5	17.1

output filters can potentially be neglected and, as can be extrapolated from **Fig. 9.10(c)**, twice as high figures of γ can be achieved.
Finally, it is worth commenting on the reliability performance of the designed modular multi-cell SPB converter. As discussed in **Section 9.3.4**, given the reliability critical application of interest, the concept of SOT is preferred to the one of MTBF. As expected, the percentage ratio between the SOT of the multi-cell approach and the one of a single half-bridge cell, i.e. $SOT_{\div}$, is very low when $Q_c = 0$ ($\approx {}^{100}/_{3\,N}\%$, similarly to $MTBF_{\div}$), and it worsens with increasing N (i.e. 5.56 % with $N = 6$). However, with $Q_c = 1$ and considering $SOT_{\div}$ at the time at which $R_{inv} = 99.73\,\%$ ($\pm3\sigma$ confidence range), the selected SPB design results even 2.5 times more reliable than a single half-bridge cell. In this case, γ is only partially affected, i.e. reduced to 19.5 kW/kg. The calculated $SOT_{\div}$ for all the values of N considered in **Fig. 9.10(a)**, different values of Q_c and confidence intervals are reported in **Tab. 9.6** together with the associated values of the γ-limit ensuring $\eta = 99\,\%$. As a consequence of the selected modular multi-cell topology, high $SOT_{\div}$ values can be reached, even with high values of N at reduced cost in terms of γ and η.

9.6 Conclusion

Meeting next generation aerospace requirements in terms of efficiency, gravimetric power density, and reliability of power converters demands a breakthrough in power electronics designs, since a significant improvement is necessary compared to the state-of-the-art. The identified over proportional voltage scaling of the power semiconductor performance suggests to investigate multi-cell approaches, which in addition enable the downsizing of the magnetic components. Unfortunately, the increased circuit complexity dramatically lowers the reliability figures of conventional approaches, and the introduction of redundant elements to compensate for this issue negatively affects the power density.
In this chapter, different multi-cell topologies are evaluated, with reference to the specifications of a 45 kW 3-Φ inverter for aerospace applications. Among them, modular solutions, able to achieve reliability figures comparable with the ones of conventional inverters, but still maintaining significantly higher performance, are preferred. The Stacked-Polyphase-Bridge (SPB) converter is selected, since it provides multiple 3-Φ outputs, and therefore can be combined with multi-phase machines e.g. in Integrated Modular Motor Drives, also reducing system design complexity and installation costs. A 3-Φ SPB inverter is finally optimized: a design featuring six cells employing GaN power semiconductors, associated *LC* filters and heat sinks, can achieve an efficiency of 99 % at a gravimetric power density of 22.8 kW/kg (19.2 kW/kg in case of one redundant cell) when switching at 110 kHz. Accordingly, the defined performance target is reached and high reliability is ensured, justifying the interest and highlighting the potential of the presented topology.

10 Conclusion and Outlook

Different technologies, measurement techniques, and power electronics concepts, facilitating the widespread adoption of WBG semiconductors in modern power converters, and enabling the full exploitation of their superior performance, are proposed and analyzed in this thesis. These advancements potentially support efficiency and power density breakthroughs demanded in next-generation MEA and EV power electronic applications, in order to reduce the power conversion losses and the weight of on-board converters. Accordingly, the described achievements pave the way for a rapid electrification of the transportation sector, targeting the reduction of its share of GHG emissions, by improving the energy efficiency of future aircraft and road vehicles.
The main findings of this thesis are summarized in detail in **Section 10.1**, while possible future research areas are discussed in **Section 10.2**.

10.1 Results of the Thesis

The main achievements of this thesis, divided according to the eight chapters constituting its core part, are summarized in the following. In particular:

PART 1 - **Novel Measurement Techniques for WBG Semiconductors**

- **Chapter 2**
  The analysis of an accurate and high bandwidth on-state voltage measurement circuit is the focus of this chapter. This measurement device allows to determine the on-state resistance $R_{\mathrm{ds,on}}$ of a power semiconductor during operation, hence to accurately estimate the instantaneous conduction losses occurring in a power converter. The actual value of $R_{\mathrm{ds,on}}$ is influenced by the operating conditions of the DUT, e.g. by the

junction temperature, conducted current, applied gate voltage, manufacturing variability, aging, and, in case of GaN power semiconductors, also the dynamic $R_{ds,on}$ phenomenon. Accordingly, the exact determination of $R_{ds,on}$ cannot rely only on datasheet information, but requires in situ measurements. On the other hand, once the $R_{ds,on}$ is comprehensively characterized, junction temperature and time-to-failure can be estimated from the on-state voltage measured for a given current value. Detailed design guidelines and calibration procedures, relative to the considered measurement device, allow to achieve both satisfactory accuracy ($< 2\,\%$) during on-state and fast dynamic response (settling time $< 50\,\text{ns}$) after a switching transition, enabled by the small parasitic input capacitance and by the $50\,\Omega$ output stage. Several challenges are addressed to ensure accurate on-state voltage measurements during operation, ultimately enabling the characterization of the on-state behavior of different WBG semiconductors.

- **Chapter 3**
  Two calorimetric switching loss measurement methods are presented and analyzed in this chapter. The first method is based on the observation of the temperature of the heat sink attached to the power stage formed by the DUT, while the second method relies on the direct measurement of the case temperature of the DUT. The measurement accuracy of the proposed methods is largely independent of the magnitude of the measured losses, from the electric parameters of the setup, and from the specifications of the necessary measurement probes. Hence, both methods are particularly suitable to evaluate the performance of fast switching power semiconductors, where the intrusiveness (in terms of parasitic capacitance and inductance) and limited bandwidth of voltage and current probes discourage the usage of conventional electric switching loss measurement methods. Additionally, both procedures consider thermal transients, i.e. the increase of temperature in the converter after turn-on in continuous operation, rather than thermal steady-state conditions, and thus offer conveniently reduced measurement times ranging from few tens of seconds to few minutes per operating point. The derived analytical expressions, describing the evolution of the temperatures in the measurement setup, provide a simple model-based method to estimate the occurring losses. Moreover, since few modifications to the measurement setup allow to vary the operating conditions of the DUT, e.g. from hard-switching to ZVS, comprehensive switching loss maps of different power semiconductors,

which are crucial for the design and optimization of power converters, can be easily obtained.

PART 2 - **Performance Bottlenecks of WBG Semiconductors**

- **Chapter 4**
  The losses occurring during the charging process of the output capacitance C_{oss} of GaN power semiconductors, responsible for compromising the efficiency of soft-switching power converters, are analyzed in this chapter. Benchmark soft-switching loss measurements performed in a dedicated calorimetric measurement setup allow to highlight their dependency on voltage and switching speed $\mathrm{d}v/\mathrm{d}t$. Confirming the hypothesis, approximately same loss magnitudes and dependencies are observed in a second measurement setup, where the C_{oss}-loss mechanism is isolated from all other losses occurring in continuous soft-switching operation, e.g. conduction losses, by generating high $\mathrm{d}v/\mathrm{d}t$ voltage waveforms across the C_{oss} of several permanently turned off transistors. A thorough analysis of the internal device structure allows to speculate the potential root cause of this loss mechanism, associated with the resistive behavior of the C-related defect band. A third measurement setup facilitates the identification of the region where the losses originate, i.e. the area forming the dielectric of the drain-substrate capacitance. The acquired knowledge culminates in the design of an enhanced power semiconductor offering a significant reduction (−70 %) of C_{oss}-losses. This achievement enables the realization of GaN-based power converters reaching unprecedented efficiency and power density figures.

- **Chapter 5**
  The impact of different circuit parameters on the dynamic on-state resistance $\mathrm{d}R_{on}$ phenomenon characterizing GaN power semiconductors is analyzed in this chapter through experimental measurements. Nowadays, designers cannot rely on datasheet information to accurately estimate the conduction losses of power converters featuring GaN devices, since no information on $\mathrm{d}R_{on}$ is reported, although its influence on the overall converter efficiency can be significant. First, the accuracy of the realized measurement setup is experimentally proven comparing $\mathrm{d}R_{on}$ of Si, SiC, and GaN power semiconductors. Only in the latter case, $\mathrm{d}R_{on}$ causes up to 30 % error on the results of calorimetric switching loss measurements. Moreover, the influence on $\mathrm{d}R_{on}$ of switching fre-

quency, blocking voltage and blocking time, and amplitude and sign of the conducted current is investigated. Thus, justifications for all the observed trends are provided, confirming the proposed hypotheses on the root cause of the phenomenon. In this context, a significant, i.e. up to +80 % in typical operating conditions, impact on the on-state voltage of the characterized GaN power semiconductor is observed. Finally, a guideline is proposed for translating the measured $\mathrm{d}R_{\mathrm{on}}$ into conduction losses of different converter topologies. The presented approach can facilitate the understanding and accelerate the mitigation of this phenomenon, and therefore potentially leads to a broader adoption of GaN power semiconductors in the power electronic industry.

- **Chapter 6**
  The conduction, thermal, and switching performance of the two 200 V GaN and Si power semiconductors offering the lowest value of on-state resistance $R_{\mathrm{ds,on}} = 10\,\mathrm{m\Omega}$ in the market are evaluated in this chapter. This voltage class is selected to develop comprehensive loss models supporting the optimization and design of modular and/or multi-level (M/ML) DC/AC power converters, which are identified as the key enablers to meet the stringent efficiency and power density targets defined by the modern aerospace and EV industries. The semiconductor performance of the selected devices is experimentally characterized in the designed measurement setups, according to the described procedures. The considered GaN e-FET offers comparable conduction performance and from three to six times lower switching losses than the Si power MOSFET, mostly originating from its smaller parasitic output capacitance; however, the latter is able to dissipate five times more power, given the lower thermal resistance of its package. Additionally, an unexpected switching loss mechanism is observed in the Si devices at hand, but this is explained and proven to be solved with modified research samples. Next, the influence of the semiconductor performance on the overall efficiency and power density of a basic converter, i.e. a hard-switching half-bridge operated as single-phase inverter, recognized as the fundamental building block of most M/ML topologies, is quantified considering the obtained measurement results. At a switching frequency $f_{\mathrm{sw}} = 140\,\mathrm{kHz}$, the Si-based half-bridge offers higher power ratings, while the GaN-based design is thermally limited to substantially lower ratings, but ensures 2 % higher efficiency. The ultimate goal of this analysis is to highlight the current performance

bottlenecks of GaN power semiconductors, thus to provide a guideline for the targeted development of this industry.

- **Chapter 7**
  A 1200 V SiC power module (PM) featuring an ultra-low inductance planar interconnection technology which replaces conventional bondwires and an integrated buffer-damping network is analyzed in this chapter. The higher switching speed, lower on-state voltage, and improved temperature withstanding capability of SiC PMs support the realization of compact, light-weight, and efficient Power Electronic Building Blocks, i.e. power converter modules with defined functionality and simplified interfaces, which are identified as key cornerstones for the electrification of air transport. The benefit of a low inductance design is highlighted, and impedance measurements on a scaled PM prototype confirm the benefits enabled by the planar interconnection technology. A parasitic power loop inductance of only 1.6 nH is achieved. The effectiveness (against switching overvoltages and oscillations) of the integrated buffer-damping network is clarified with the support of equivalent circuits. Furthermore, the enabled improvement is experimentally verified by means of measurements, first on a scaled PM prototype, then on the full-scale PM. An overvoltage reduction of approximately 70 % is achieved in both cases and the measured oscillations are negligible. The preliminary considerations relative to the design of the full-scale PM, e.g. the selection of the switching frequency and of the number of dies connected in parallel to form each switch, and of its gate driver are as well summarized; following this procedure, a power stage efficiency of 99 % is reached. Finally, the design guideline for the sizing of the buffer-damping network and the associated sensitivity analysis generalize the applicability of the proposed approach. The outcome of this study allows PM designers to fully utilize the high performance of SiC power semiconductors.

Part 3 - **Next-Generation Converters with WBG Semiconductors**

- **Chapter 8**
  The operating principle of a two-stage 3-Φ buck-boost GaN current source inverter system is analyzed in this chapter. Dual-gate monolithic bidirectional GaN e-FETs, instead of anti-series connected conventional power semiconductors, are employed in the boost-type 3-Φ current DC-link inverter output stage, and thus superior performance is achieved.

Moreover, using only a single magnetic component, i.e. the DC-link inductor, continuous 3-Φ sinusoidal load phase currents are generated at the output terminals of this converter, as in a conventional voltage source inverter featuring an additional output filter. The developed synergetic control scheme and/or variable DC-link current control strategy, denominated 2/3-PWM, significantly improves the converter performance for different operating conditions, and ensures sufficient dynamic response. In particular, by properly shaping the DC-link current with the buck-type DC/DC converter input stage, the desired 3-Φ sinusoidal load phase currents are generated by switching only two phases of the output stage. Accordingly, a significant reduction of conduction and switching losses (up to 8 % and 83 %, respectively) is enabled, especially for unity power factor operation, making this topology particularly suited for VSD supplying synchronous machines driving passive mechanical loads, e.g. pumps and fans.

- **Chapter 9**
  A modular multi-cell GaN inverter for next-generation aerospace applications is analyzed in this chapter. The multi-cell approach allows to take advantage of the enhanced switching performance of low voltage GaN e-FETs, while the modular structure ensures straight-forward scalability and fault-tolerant operation with a negligible impact on the overall converter power density, as demonstrated through analytic calculations based on the FoM of different power semiconductors. The analysis of the mean time between failures of the proposed topology confirms its superior availability compared to conventional solutions. Moreover, the possible integration of the converter into the machine housing reduces installation costs, avoids cables and electromagnetic (EM) emissions, and prevents voltage reflection phenomena. A multi-objective optimization procedure, considering an output power of 45 kW and a DC-link voltage of 1 kV (typical for MEA applications), results with an efficiency greater than 99 % up to a gravimetric power density of 22.8 kW/kg, making the proposed solution a favorable candidate to support the further electrification of air transport.

10.2 Future Trends and Research Areas

Although this thesis already covered numerous aspects concerning the characterization and use of WBG power semiconductors in modern power electronic

applications, e.g. EVs and MEA, several potential research areas, strictly connected to the obtained results, emerged in the course of the analysis, and should be investigated in the future to accelerate the electrification of the transportation sector. In particular:

PART 1 - **Novel Measurement Techniques for WBG Semiconductors**

- **Chapter 2**

  (i) Integration of a compact realization of the designed on-state voltage measurement circuit into a real power converter. The obtained information on the instantaneous value of the on-state voltage, in combination with the current information, would enable the condition monitoring of the DUT, e.g. its junction temperature estimation.

  (ii) Design of a desaturation circuit for over current protection based on the developed measurement circuit.

  (iii) Re-desing of the measurement circuit to allow measurements at multi-MHz switching frequencies and/or of power semiconductors rated for more than 600 V. To achieve this, different blocking diodes are necessary, or a new circuit topology must be investigated.

- **Chapter 3**

  (i) Automation of the developed calorimetric switching loss measurement setup/method, aiming to characterize a large number of power semiconductors with different specifications. This would allow to significantly extend the database necessary for the optimization of power converters with reduced effort.

  (ii) The proven accuracy and wide applicability of the setup/method could support the analysis of the impact of external circuit parameters, e.g. gate driver, gate resistance, gate voltage, commutation capacitance, anti-parallel diode, dead-time, etc. and of parasitic elements, e.g. commutation loop inductance, gate loop inductance, etc. on the switching losses.

  (iii) Deeper understanding of the origin and finally accurate modeling of the soft-switching losses in Si and SiC power semiconductors.

  (iv) Measurement of the switching losses in a power stage featuring parallel devices, i.e. more than one transistor per switch, to evaluate the impact of asymmetric switched current sharing.

PART 2 - **Performance Bottlenecks of WBG Semiconductors**

- **Chapter 4**

  (i) Experimental validation of the performance improvement at the converter level enabled by GaN power semiconductors featuring the modified epitaxial stack.

  (ii) Analysis of the switching performance of different GaN (but also Si and SiC) devices suffering from this loss mechanism, in order to generalize the hypotheses on its root cause and finally propose an analytical model allowing the designer to estimate these losses for different operating conditions and/or support the semiconductor manufacturers to identify a solution to mitigate them.

- **Chapter 5**

  (i) Investigation of the dynamic on-state resistance phenomenon at multi-MHz switching frequencies.

  (ii) Analysis of the dependencies of this loss mechanism considering a wider variation of circuit parameters, different circuit parameters, and for multiple GaN power semiconductors, in order to generalize and further validate the outcome of the conducted study.

- **Chapter 6**

  (i) Performance comparison of Si and WBG power semiconductors of different voltage levels, e.g. 600 V and 1.2 kV, in order to generalize the obtained results. A larger performance gap and a wider range of WBG devices are available at these voltage levels; moreover, the devices are offered in packages ensuring satisfactory thermal performance, which represented the main bottleneck for the considered 200 V GaN devices.

  (ii) Complete optimization of the selected power converter to quantify the advantages of the GaN-based solution in terms of efficiency and power density.

- **Chapter 7**

  (i) Experimental analysis of the effect of the integrated buffer-damping network on the voltage stress and on the performance, i.e. switching losses, EM emissions, etc. of the realized PMs, and

consideration of the enabled increase of the DC-link voltage to reduce the occurring conduction losses for the same output power.

(ii) Evaluation of the thermal performance of the full-scale PM.

(iii) Improvement of the simulation-based routine for the design of the buffer-damping network, concerning both the estimation of the parasitic elements present in the PMs and the switching performance of the power semiconductors.

(iv) Testing of the full-scale PM in a real power converter setup to evaluate the improvement enabled by the customized design, e.g. in terms of efficiency and power density of the whole system.

PART 3 - **Next-Generation Converters with WBG Semiconductors**

- **Chapter 8**

  (i) Performance evaluation, e.g. in terms of switching losses and dynamic on-state resistance, of the dual-gate monolithic bidirectional GaN e-FETs.

  (ii) Realization of a current source inverter system prototype to confirm the applicability of the developed control scheme and the effectiveness of the proposed modulation scheme.

  (iii) Performance comparison, e.g. considering efficiency, power density, cost, EM emissions, etc. of the proposed topology against the conventional voltage source approach.

- **Chapter 9**

  (i) Realization of the modular multi-cell inverter prototype to validate the results of the multi-objective optimization, hence confirming the superiority of this approach against the conventional solution.

  (ii) Experimental validation of the analyzed fault-tolerance capability based on the developed prototype.

  (iii) Verification of the discussed advantages of integrated modular motor drives, e.g. concerning lower filtering requirements.

  (iv) Evaluation of concepts for the realization of a power stage featuring six parallel connected GaN power semiconductors.

Appendices

A

Tuning of the On-State Voltage Measurement Circuit

The influence of a mismatch $v_{\Delta D}$ of the voltage drops of the diodes D_1 and D_2 can be accurately characterized. In particular, if

$$v_{D1} \neq v_{D2} = v_{D1} \pm v_{\Delta D} \tag{A.1}$$

then

$$v_m = \frac{1}{1+\beta}\,(v_{ds} \mp v_{\Delta D}). \tag{A.2}$$

As in the diode-based approach of **Fig. 2.2(b)**, a mismatch in the compensation of v_{D1} translates into an offset $v_{\Delta D}$ of v_m. However, **Section 2.3.2** proved how, with the necessary precautions, a good accuracy can be reached. An offset of v_m can results also from resistance mismatches. First, if

$$R_3 \neq R_4 \quad \longrightarrow \quad \frac{R_3}{R_4} = 1 \pm \delta_R \tag{A.3}$$

then

$$v_m = \frac{1}{1+\beta}\,\left((2 \pm \delta_R)\,v_1 - (1 \pm \delta_R)\,v_2\right) = \frac{1}{1+\beta}(v_{ds} \mp \delta_R\, v_{D2}). \tag{A.4}$$

Second, if

$$\frac{R_{1b}}{R_{1a}+R_{1b}} \neq \frac{R_{2b}}{R_{2a}+R_{2b}} = (1 \pm \rho_R)\frac{R_{1b}}{R_{1a}+R_{1b}} \tag{A.5}$$

then

$$v_m = \frac{1}{1+\beta}\,\left(2\,v_1 - (1 \pm \rho_R)\,v_2\right) = \frac{1}{1+\beta}(v_{ds} \mp\ \rho_R v_2). \tag{A.6}$$

These consideration are relevant for the calibration of the proposed OVMC, and e.g. facilitate the understanding of the causes of inaccuracy from the error trends. In particular, while $v_{\Delta \mathrm{D}}$ in (A.2) and $\delta_{\mathrm{R}} v_{\mathrm{D}_2}$ in (A.4) are practically constant error terms, $\rho_{\mathrm{R}} v_2$ in (A.6) is proportional to the variable measured voltage. Moreover, it becomes clear that precision resistors should be used for R_1-R_4.

B

Propagation of Uncertainty of the External Losses

In order to calculate the impact of $\sigma_{P_{\text{ext}}}$ on $\sigma_{P_{\text{sw}}}$, the parameter k_{sw} is defined as

$$P_{\text{sw}} = k_{\text{sw}}\, P_{\text{tot}} = \frac{k_{\text{sw}}}{1 - k_{\text{sw}}} P_{\text{ext}} \tag{B.1}$$

with $0 \leq k_{\text{sw}} \leq 1$. When k_{sw} approaches 1, mainly P_{sw} contributes to P_{tot}. Intuitively, $\sigma_{P_{\text{ext}}}$ has a minor influence on $\sigma_{P_{\text{sw}}}$. Analytically, applying the propagation of uncertainty on P_{sw},

$$\sigma_{P_{\text{sw}}} = \sqrt{\left(\frac{\partial P_{\text{sw}}}{\partial P_{\text{tot}}}\sigma_{P_{\text{tot}}}\right)^2 + \left(\frac{\partial P_{\text{sw}}}{\partial P_{\text{ext}}}\sigma_{P_{\text{ext}}}\right)^2} = \sqrt{\sigma_{P_{\text{tot}}}^2 + \sigma_{P_{\text{ext}}}^2} \tag{B.2}$$

and

$$\sigma_{\%P_{\text{sw}}} = \frac{\sigma_{P_{\text{sw}}}}{P_{\text{sw}}} = \sqrt{\left(\frac{\sigma_{P_{\text{tot}}}}{P_{\text{sw}}}\right)^2 + \left(\frac{\sigma_{P_{\text{ext}}}}{P_{\text{sw}}}\right)^2} \tag{B.3}$$

$$= \sqrt{\left(\frac{\sigma_{P_{\text{tot}}}}{k_{\text{sw}}\, P_{\text{tot}}}\right)^2 + \left(\frac{1 - k_{\text{sw}}}{k_{\text{sw}}}\frac{\sigma_{P_{\text{ext}}}}{P_{\text{ext}}}\right)^2} \tag{B.4}$$

$$= \frac{1}{k_{\text{sw}}}\sqrt{\sigma_{\%P_{\text{tot}}}^2 + (1 - k_{\text{sw}})^2\, \sigma_{\%P_{\text{ext}}}^2} \tag{B.5}$$

are obtained. For the purpose of this analysis $\sigma_{P_{\text{tot}}} = 0$ is assumed and (B.3) simplifies to

$$\sigma_{\%P_{\text{sw}}} = \pm\frac{P_{\text{ext}}}{P_{\text{sw}}}\sigma_{\%P_{\text{ext}}} \quad \longrightarrow \quad -\frac{P_{\text{ext}}}{P_{\text{sw}}}\sigma_{\%P_{\text{ext}}} = -\frac{1 - k_{\text{sw}}}{k_{\text{sw}}}\sigma_{\%P_{\text{ext}}}. \tag{B.6}$$

As anticipated, when $k_{\mathrm{sw}} = 1$ there is no influence of $\sigma_{P_{\mathrm{ext}}}$ on $\sigma_{P_{\mathrm{sw}}}$. However, this is only ideal: operating the measurement setup as described, P_{ext} is unavoidable and P_{sw} is limited from f_{sw}.

C

Volumetric Energy Density of Inductors and Capacitors

The volume and DC (current or voltage) rating R_{dc} of several thousand commercial inductors, with nominal inductance values ranging from 1 µH to 1 mH, and capacitors (electrolytic, ceramic, and film), with nominal capacitance values ranging from 1 µF to 1 mF, are analyzed in this section. Computing their typical volumetric energy densities E_{vol}, a practical rule of thumb for the estimation of their volume, given their value and R_{dc}, is finally provided. The results of this analysis are summarized in **Fig. C.1**, where the volumetric densities X_{vol} (expressed in µH/cm^3 or µF/cm^3) of the considered compo-

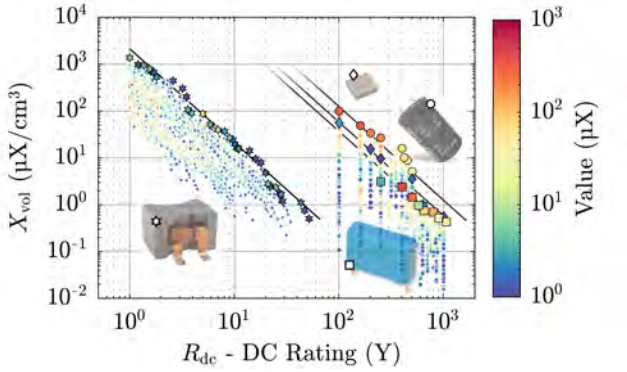


Fig. C.1: Volumetric density X_{vol} of several thousand commercial inductors with nominal values ranging from 1 µH to 1 mH and capacitors (electrolytic, ceramic, and film) ranging from 1 µF to 1 mF, as function of their respective DC rating R_{dc} in double-logarithmic scale.

Tab. C.1: Volumetric energy density E_{vol} of commercial inductors and capacitors.

Component		E_{vol} (J/dm^3)
Capacitor	Electrolytic	626.0
	Ceramic	274.5
	Film	180.5
Inductor		0.9

nents are plotted as function of their respective R_{dc} (expressed in A or V, i.e. Y in **Fig. C.1**) in double-logarithmic scale. It is evident how inductors and capacitors group in two separate regions. Moreover, for each component category, i.e. inductors, electrolytic capacitors, etc., the highest values of X_{vol} per each R_{dc} can be nicely interpolated (black lines) by the function

$$X_{\text{vol}} = k\, R_{\text{dc}}^{-2}, \tag{C.1}$$

where k can be written as

$$k = 2\,\frac{1}{2} X_{\text{vol}}\, R_{\text{dc}}^2 \quad \rightarrow \quad k = 2\, E_{\text{vol}}. \tag{C.2}$$

The resulting values of $E_{\text{vol}} = {}^{k}/_{2}$ are listed in **Tab. C.1**, and provide approximate quantitative information, which can be sufficient in a preliminary design phase to estimate the volume of these reactive components.

D

Experimental Verification of the Dual-Gate Monolithic Bidirectional GaN e-FETs

A test bench PCB for the 2G MB GaN e-FETs introduced in **Section 8.6.1** is realized as illustrated in **Fig. D.1** and **Fig. D.2**. It implements the three switches forming one side (e.g. the low-side) of the 3-Φ inverter, since, as clarified in **Section 8.4.2**, this is sufficient, due to symmetry properties, to characterize the performance of the entire 3-Φ inverter. In addition to the three $T_{i,l}$, the realized PCB includes the associated gate drivers [219] (see

Fig. D.1: Perspective view of the test bench PCB. The PCB has a square shape, with each edge measuring 7.1 cm. Details of the components are provided in **Fig. D.2(a)** and **(b)**.

Fig. D.2: (a) Top view and **(b)** mirrored bottom view of the test bench PCB comprising the three 2G MB GaN e-FETs $T_{i,l}$ forming the low-side of the 3-Φ inverter, their respective gate drivers [219] with isolated signal transmission and isolated power supply, and a fraction of the overall output filter capacitors C_o [93], in addition to robust power and signal connectors. **(c)** Bridge-leg formed by $T_{a,l}$ and $T_{b,l}$ on which the waveforms shown in **Fig. D.3** are measured. The blue line should help to recognize this bridge-leg structure in **Fig. 8.1** and **Fig. 8.7**.

Fig. 8.17(b)) with isolated signal transmission and isolated power supply, and a fraction of the overall output filter capacitors C_o [93].
In particular, the bridge-leg formed by $T_{a,l}$ and $T_{b,l}$, depicted in **Fig. D.2(c)**, is considered in the following. This bridge-leg is operated connecting a supplying DC input voltage source V_{ba} between the terminals *b* and *a*, and a *RL* load at the switch node *n* to sink the load current i_{dc}. Measured waveforms of the switch node voltage v_{na} and of i_{dc} are recorded and plotted in **Fig. D.3(a)** for $V_{ba} = 400\,\text{V}$, and $\langle i_{dc} \rangle = 5\,\text{A}$ (blue) and 0 A (red) in soft-switching (ZVS and ZCS) and hard-switching conditions. No significant overvoltage or oscillations are observed on v_{na}, while turn-off ZCS and hard-switching transitions are performed at switching speeds $\mathrm{d}v/\mathrm{d}t \approx 15\,\text{V/ns}$ (red and blue in **Fig. D.3(c)**, respectively). Moreover, the voltage slope occurring for the turn-on ZVS transition (blue in **Fig. D.3(b)**) confirms the expected $C_{oss,Q}$ value calculated according to $2\,C_{oss,Q} = {}^{i_{dc}}/_{\mathrm{d}v/\mathrm{d}t}$ (cf. **Tab. 8.3**).
For 2G MB GaN e-FETs (and AC-switches in general), particular care must be taken during the switching transition, such that always a path for the switched current is provided, while one of the two switches involved in the commutation blocks the (bipolar) switched voltage (see **Fig. 8.17(a)**). Hence, the four gate signals $s_{Ti,lp}$ and $s_{Ti,ln}$ are generated according to a current sign-dependent multi-step commutation strategy [198], as illustrated in the lower part of **Fig. D.3(b)** and **(c)** for the case of $i_{dc} > 0$. Additionally, the zoomed view of the measured v_{na} is overlaid with the equivalent circuits of the bridge-leg (I, II and III) determined by $s_{Ti,lp}$ and $s_{Ti,ln}$ (see **Fig. 8.17(a)**). These plots highlight how, depending on the type of switching transition, i.e. ZVS, ZCS, or hard-switching, the commutation takes place at different instants of the multi-step sequence.

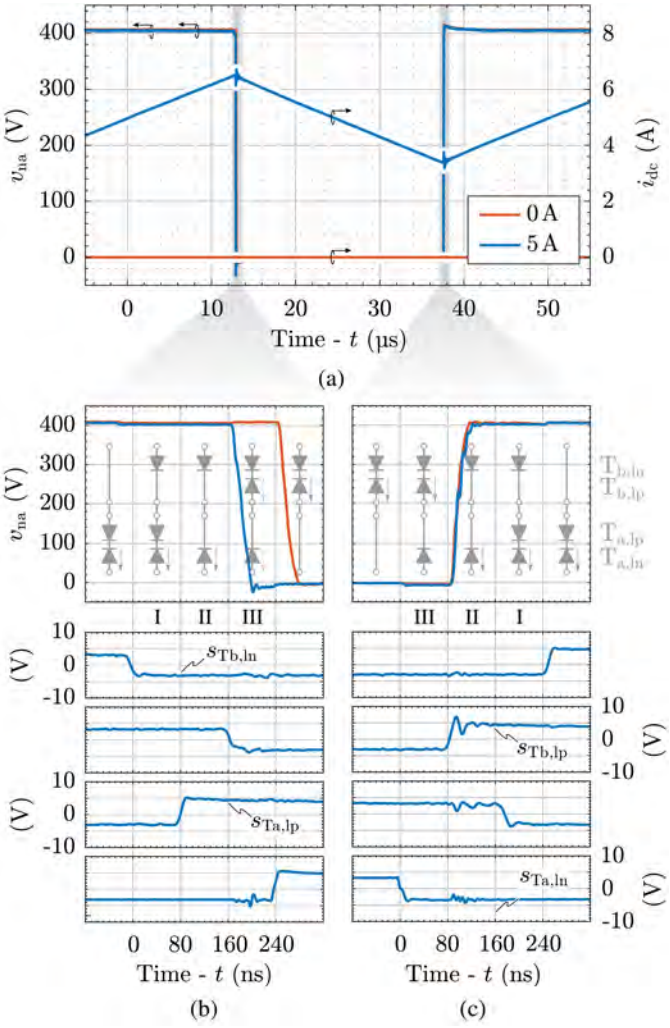


Fig. D.3: (a) Measured waveforms of the switch node voltage v_{na} and of the load current i_{dc} during continuous operation of the bridge-leg shown in **Fig. D.2(c)**, for a supplying DC input voltage $V_{ba} = 400\,V$, and an average output current $\langle i_{dc} \rangle = 5\,A$ (blue) and 0 A (red). **(b)-(c)** Zoomed view of v_{na} during a turn-on ZVS transition (blue in **(b)**), a turn-on ZCS transition (red in **(b)**), a turn-off ZCS transition (red in **(c)**), and a turn-off hard-switching transition (blue in **(c)**). The associated gate signals $s_{Ti,lp}$ and $s_{Ti,ln}$ and respective equivalent circuit of the bridge-leg are additionally shown.

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