Basic Considerations and Topologies of Switched-Mode Assisted Linear Power Amplifiers

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***Abstract*— This paper presents a combined power amplifier system consisting of a linear amplifier unit with a switched-mode (class D) current dumping stage arranged in parallel. With this topology, the fundamental drawback of conventional linear power amplifiers—the high loss—is avoided. Compared to a pure class D (switching) amplifier, the presented system needs no output filter to reduce the switching frequency harmonics. This filter (usually of multistage type) generally deteriorates the transient response of the system and impairs the feedback loop design. Furthermore, the low-frequency distortions of switching amplifiers caused by the interlock delay of their power transistors are avoided with the presented switched-mode assisted linear amplifier system. This can be considered as a master–slave system with a guiding linear amplifier and a supporting class D slave unit. The paper describes the operating principle of the system, analyzes the fundamental relationships for the circuit design, and presents simulation results. Finally, various further topologies of switched-mode assisted linear amplifiers are given.**

***Index Terms*— Class D converters, dc–ac power conversion, power amplifiers, switching amplifiers.**

I. Introduction

Conventional linear power amplifiers (Fig. 1(a)) are replaced by switching (class D) amplifiers (Fig. 1(b)) in an increased quantity to overcome the essential drawback of linear amplifier systems, i.e., the high losses (especially in the case of nonresistive or nonlinear loads or if signals with high peak-to-rms ratio are amplified [1]). Nevertheless, if the output voltages have to be of very high quality (e.g., for high-end audio applications or for test and measuring equipment), switching amplifiers show significant limitations. The output voltage of a class D amplifier implies substantial switching-frequency components (high frequency distortions) which have to be reduced by a proper low-pass filter. However, this filter—which has to be in general of higher order type—reduces the dynamic response and increases the output impedance of the whole amplifier system. Also, the interlock delay time of the usually applied bridge topologies, and/or a ripple of the dc supply voltage $\pm U$ and/or the on-state voltages of the power semiconductor devices (transistors and freewheeling diodes), may result in low-frequency distortion [2] which hardly can be reduced by the described switching frequency output filter, but has to be lowered by using a special control loop design [3], [4]. A further problem of switching amplifiers is the possible occurrence of subharmonic frequency components which may

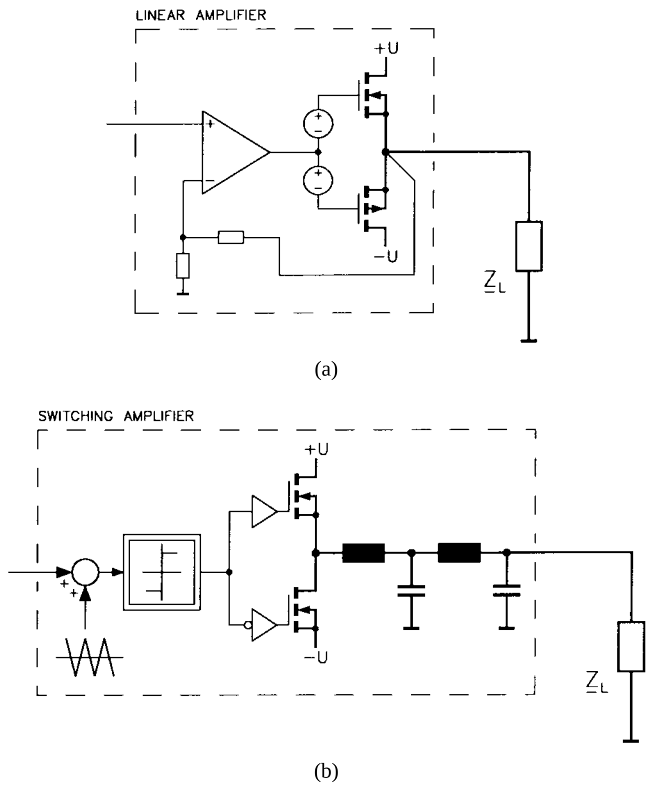

Fig. 1. Simplified circuit diagram of (a) a linear power amplifier and (b) a class D switching amplifier (the internal body diodes of the switching power MOSFET's are not shown).

result for a small signal-to-switching-frequency ratio, or if a pulse width modulation strategy with not constant switching frequency (e.g., hysteresis control or sigma–delta modulation) is applied. This subharmonic noise basically cannot be lowered by the output low-pass filter because the relevant frequency components lie within the power bandwidth of the amplifier.

To avoid the disadvantages described above, a concept originally proposed in [5] consisting of a parallel arrangement of a class D switching system and a conventional linear amplifier stage (Fig. 2) is analyzed. There, the output filter of the switching amplifier is reduced to a single coupling inductor determining the switching frequency ripple. Although the linear amplifier, therefore, can be considered as active filter which compensates the switching frequency ripple and the modulation noise, the basic idea of the proposed switched-mode assisted linear amplifier is that the linear amplifier acts as the guiding master system, whereas the task of the class D (slave) stage is to take over the current of the linear stage

Manuscript received February 13, 1996; revised July 13, 1996.

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Publisher Item Identifier S 0278-0046(97)00079-8.

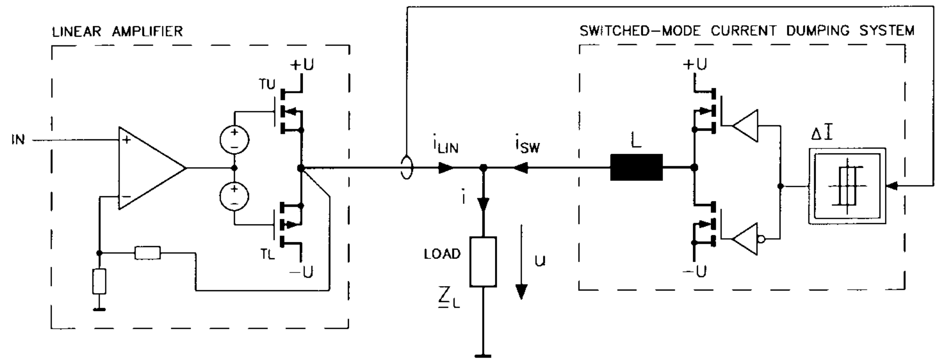


Fig. 2. Circuit diagram of a switched-mode assisted linear power amplifier.

(current dumping). In the ideal (stationary) case, the linear power amplifier only has to deliver the ripple of the class D stage which significantly reduces its power losses. Contrary to a (passive) output filter of a conventional switching amplifier, the linear amplifier of the proposed concept also reduces low-frequency distortions and subharmonic components. It has to be pointed out, however, that a very low output impedance of the linear system part is of paramount importance in order to get a high noise rejection. This circumstance has to be considered by an appropriate design of the linear amplifier circuitry and feedback system. Furthermore, the switched-mode assisted linear amplifier only allows a significant reduction but not a complete loss elimination as an idealized class D amplifier. Therefore, considering the losses, the proposed system can be seen as an intermediate solution between pure linear and pure class D power amplifiers. As an advantage of the proposed system, it has to be mentioned that the dynamic response of the whole system is determined by the linear stage and, therefore, not influenced by an output filter.

II. System Control—Calculation of Power Losses

The guidance of the class D part is realized by a current controller whose reference value is identical to the current through the load. Thus, only the control error and the ripple have to be delivered by the linear stage. Instead of an explicit subtraction of reference value (load current i) and actual value (class D stage output current $i_{\rm SW}$), the calculation of the controlling quantity can be done in an implicit manner by direct measurement of the linear stage output current $i_{\rm LIN}$. In the simplest case, the current controller can be a hysteresis controller (Fig. 2), which results in a nonconstant switching frequency within the fundamental period of the amplified signal. As an alternative, a pulse width modulator (PWM) with a superimposed linear current controller, or other types of current controllers being well-known from switched-mode power supplies (e.g., conductance control), can be applied. The usage of a PWM allows a switching frequency being constant which is, however, of not essential significance for this application, as stated before. An advantage of the hysteresis controller is its inherent overmodulation ability which yields a more efficient utilization of the dc supply voltage $\pm U$. On the other hand, PWM current controllers with their well-defined switching instants allow an easier extension of the class D stage to a parallel arrangement being operated in an optimum phase-shifted manner, in order to reduce the total ripple current or increase the effective switching frequency, respectively. However, it should be mentioned that there exist solutions for two hysteresis-controlled converter branches (arranged in parallel) where a suboptimal phase shift can be achieved in a very simple way (Section V).

In the following, the losses of the linear amplifier stage shall be calculated for the case that a hysteresis current controller with a constant tolerance band ΔI is applied. It is assumed that the load current i and the output voltage u can be treated as constant within the switching interval T, or that there exists a sufficient signal-to-switching frequency ratio, respectively (Fig. 3). Furthermore, the power transistors are assumed to be ideal (neglection of delay times, on-state voltages, etc.). Also, dc supply voltage variations are neglected.

Switching Frequency: With the assumptions given above, the output voltage u (averaged within a pulse interval T) is determined by the duty cycle δ. If we apply the definition $m = u/U$ for normalizing the output voltage $(m = -1 \cdots +1)$, we get

$$\delta = \frac{1 + u/U}{2} = \frac{1+m}{2}. \tag{1}$$

According to $u_L = L\ di_{\rm SW}/dt$, the switching frequency $f_s = 1/T$ can be calculated

$$f_S = f_{S,\max} \cdot (1 - m^2) \quad \text{with} \quad f_{S,\max} = \frac{U}{2L \cdot \Delta I}. \tag{2}$$

Power Losses: The power losses of the linear stage depend on its operating mode, where one has to distinguish between class A (linear amplifier with quiescent current eliminating crossover distortions) and class B (without quiescent current) mode. The following table gives the local losses (i.e., the losses averaged within a switching period T) of the upper transistor TU and the lower transistor TL of the linear stage, where it is assumed that for class A mode the quiescent current is as small as possible $(I_{\rm Q} = I_{\rm Q,min} = \Delta I/4)$ (see Fig. 3(e)).

For $I_{\rm Q} = \Delta I/4$, the class A mode losses are twice the losses of the class B mode. The total transistor losses p_T are not dependent on the modulation index m and, therefore, the local transistor losses p_T also represent the global losses (i.e., the losses averaged within the fundamental period of the amplified signal) $p_T = P_T$.

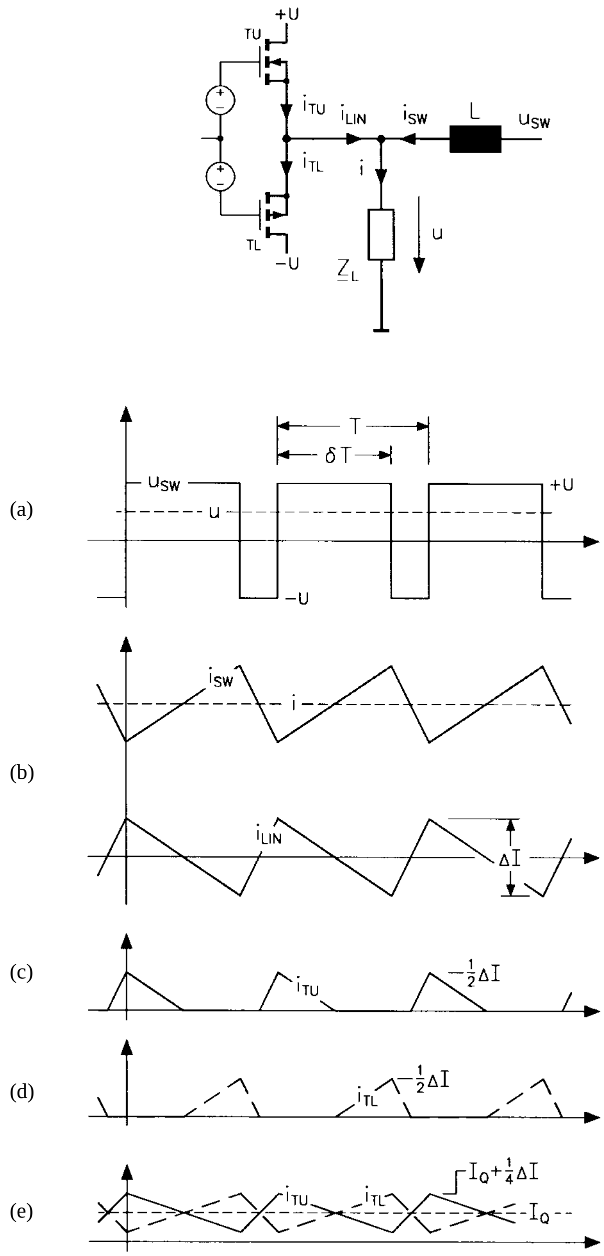


Fig. 3. Voltage and current waveforms of a switched-mode assisted linear power amplifier. (a) Switching stage output voltage. (b) Output currents of the class D system and of the linear stage. (c) and (d) Transistor currents for class B mode of the linear amplifier part. (e) Currents for class A mode.

Influence of the Switching Frequency on the Amplifier Bandwidth: According to (3), shown at the bottom of the page, the demand for low power losses implies a small ripple amplitude ΔI. However, for a defined maximum switching frequency $f_{S,\max}$, this would result in the usage of a high value of the inductance L. On the other hand, a higher value of L reduces the power bandwidth f_B of the switched-mode current dumping stage. If we normalize ΔI with respect to the value U/R (maximum load current, resistive load $\underline{Z}_L = R$ assumed), i.e., $k_\Delta = \Delta I/(U/R)$, we receive from (3):

$$P_T = \frac{U \cdot \Delta I}{4} = \frac{U^2}{R} \cdot \frac{1}{4} k_\Delta \tag{4}$$

for a class B linear stage ($k_\Delta \cdots$ normalized ripple amplitude). The power bandwidth of the current dumping stage can be defined as $f_B = R/(2\pi L)$ (if full output voltage utilization has to be achieved without overmodulation). Using (2), this leads to

$$\frac{f_{S,\max}}{f_B} = \frac{\pi}{k_\Delta}. \tag{5}$$

This shows clearly that the switching frequency-to-bandwidth ratio is linked to the losses of the linear system. For a given maximum switching frequency and a required power bandwidth of the whole amplifier the current ripple (and, therefore, the power losses) are fixed. However, there are some possibilities to overcome this fundamental limitation: (1) usage of a higher supply voltage for the switching stage (reduced modulation index); (2) splitting up the current dumping stage into several parallel branches operated in a phase shifted manner or application of a three-level topology (simultaneous reduction of L and of ΔI); and (3) higher order-type coupling impedance of the switching stage (e.g., $L \rightarrow LCL$). However, it has to be noted that the described effect only limits the power bandwidth of the current dumping stage and not of the whole amplifier system whose dynamic response (especially the slew rate) is determined by the linear stage. (Full power operation of the amplifier above f_B, however, can cause a thermal overload of the linear stage.)

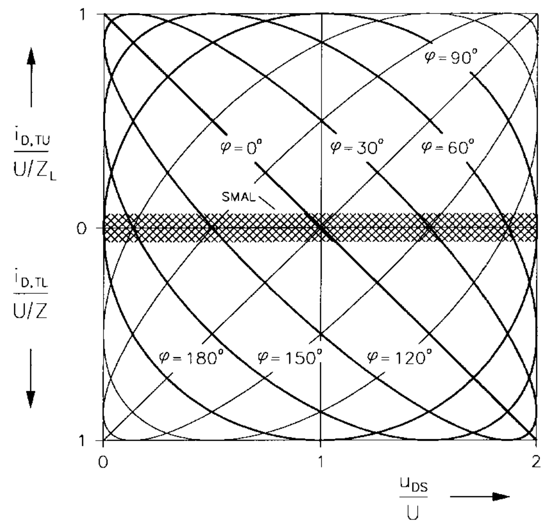
III. Dimensioning Example—Simulation Results

In the following, a prototype system of a 1-kVA switched-mode assisted amplifier system with the nominal values $U = \pm$ 80 V, $R = 2.5\ \Omega$ (resistive load $\underline{Z}_L = R$; RMS value of the sinusoidal output voltage: 50 V), $f_B = 10$ kHz, $f_{S,\max} =$ 200 kHz shall be calculated briefly.

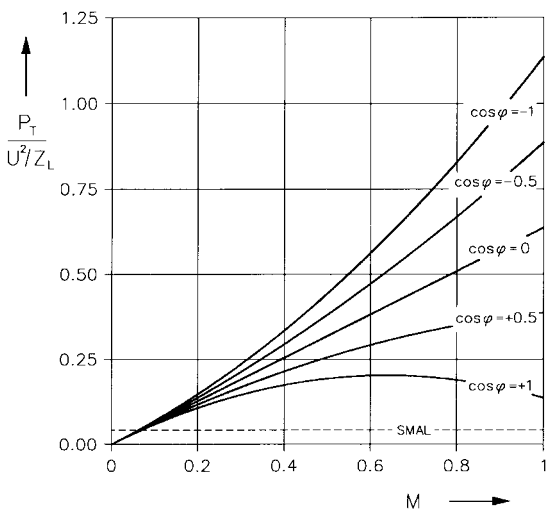
According to (5), we receive k_Δ =0.157, i.e., a current ripple of $\Delta I = 5$ A and a total power loss $P_T \approx$ 100/200 W (class B/class A mode). As can be seen from Fig. 4(b), the power losses of the proposed system are far beneath the losses

	class B	class A
$i_{TU,\text{avg}} = i_{TL,\text{avg}} =$	$\frac{1}{8}\Delta I$	$\frac{1}{4}\Delta I$
$p_{TU} = (U - u) \cdot i_{TU,\text{avg}} =$	$U\Delta I \cdot \frac{1}{8}(1-m)$	$U\Delta I \cdot \frac{1}{4}(1-m)$
$p_{TL} = (U + u) \cdot i_{TL,\text{avg}} =$	$U\Delta I \cdot \frac{1}{8}(1+m)$	$U\Delta I \cdot \frac{1}{4}(1+m)$
$P_T = p_{TU} + p_{TL} =$	$U\Delta I \cdot \frac{1}{4}$	$U\Delta I \cdot \frac{1}{2}$

(3)

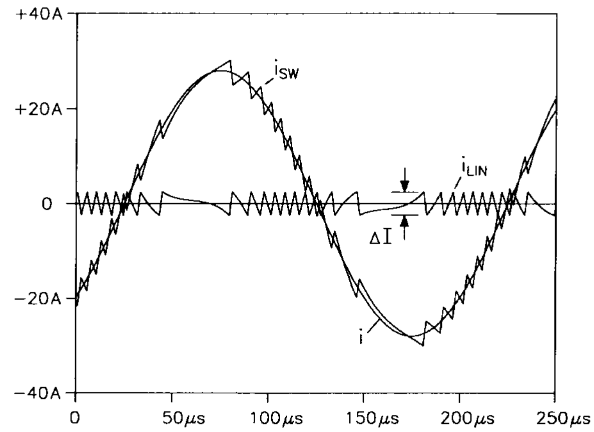


(a)

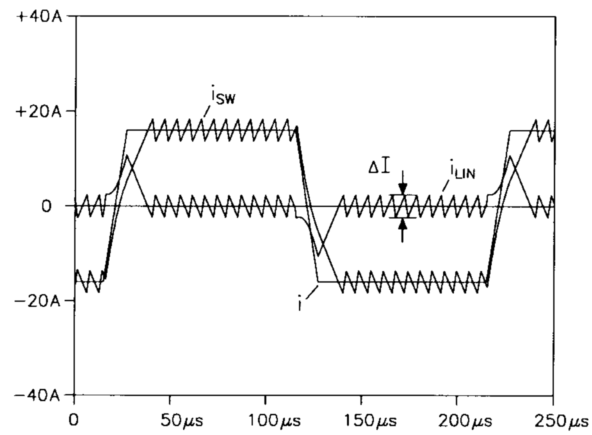


(b)

Fig. 4. (a) MOSFET $U_{\rm DS}/I_{\rm D}$-trajectories (load lines) and (b) power losses of a conventional linear power amplifier and of a switched-mode assisted linear (SMAL) amplifier (both class B mode) for sinusoidal output voltage (normalized amplitude M = Û/U) and different load current displacement factors cos φ. (The losses are normalized to U^2/Z_L, U ... supply voltage, Z_L ··· magnitude of the complex load impedance).



(a)



(b)

Fig. 5. Simulated current wave shapes of a 1 kW switched-mode assisted linear power amplifier (a) Sine wave response. (b) Pulse response (parameters: U = ±80 V, R = 2.5**Ω**, f_B = 10 kHz, $f_{S,\max}$ = 200 kHz, ΔI = 5 A).

of conventional linear power amplifiers, especially for the case of nonresistive loads (e.g., the losses of a conventional linear amplifier would be $P_T \approx 1$ kW for $M = 1$ and $\cos\varphi = 0.5$). However, it has to be admitted that the losses shown in Fig. 4 for the switched-mode assisted amplifier do not include the losses of the switching stage. On the other hand, the efficiency of switched-mode bridge topologies usually lies above 95%, so that the total losses of switched-mode assisted amplifiers would not be increased significantly.

The current wave shapes of the simulated 1-kW amplifier system are shown in Fig. 5. There, the pulse response demonstrates the limited slew rate of the switched-mode current dumping system. In this case, the output current of the linear amplifier $i_{\rm LIN}$ not only has to compensate the ripple of the switching state, but also has to take over the dynamic current peaks ($i_{\rm LIN}$, therefore, cannot be guided completely within the tolerance band ΔI). This effect results in increased power losses of the linear stage.

IV. Linear Stage Design—Output Impedance

A very low magnitude Z of the high-frequency output impedance $\underline{Z}$ of the linear stage is of fundamental importance for a high output voltage signal-to-noise ratio (SNR) of the system because the ripple current ΔI of the switching stage generates a noise voltage $Z \cdot \Delta I$. If we strive for an SNR of, e.g., $\geq$80 dB, for the system simulated in the previous section an output impedance of $Z \leq 2\hat{U}/(\Delta I \cdot 10^{\rm SNR/20}) \approx 3$ mΩ has to be guaranteed, which complicates the design of the linear stage.

Today, the output stages of linear amplifiers usually are realized by using power MOSFET source followers [6]. The output impedance of source followers is defined by the transconductance g_m of, e.g., the upper transistor and is also influenced by the output impedance R_i of the driver stage (Fig. 6) in the upper frequency region.

In general, the transconductance of power MOSFET's is far too low to get an output impedance in the desired milliohms-range (Fig. 7—*open loop*: $Z \approx 0.8\ \Omega$ for the assumed maximum switching frequency $f_{S,\max} = 200$ kHz). Actually,

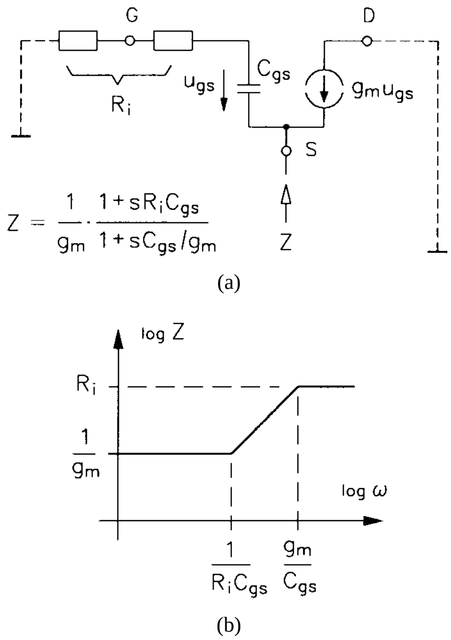


Fig. 6. Output impedances of source followers. (a) Equivalent circuit. (b) Frequency response.

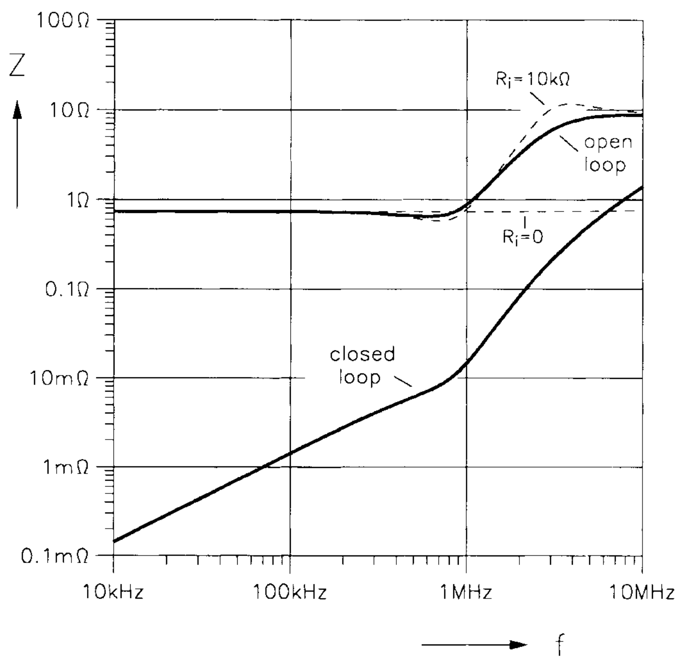


Fig. 7. Output impedance of the linear amplifier stage.

this fact is not of primary significance because the effective output impedance is reduced by the loop gain of the feedback system (introduced originally to improve the linearity of the amplifier). For the described system, we have to adjust the loop gain to $\approx$ 50 dB at 200 kHz. A higher loop gain would allow to further increase the SNR, but would reduce the stability margin of the linear amplifier system. The frequency response of the amplifier mainly is determined by that of the voltage booster stage (Fig. 8) because the output current buffer usually shows a much higher bandwidth due to the application of MOSFET's and a high-frequency driver stage using bipolar video transistors. Contrary to conventional linear power amplifiers, the frequency design of the voltage booster has to be performed not only regarding the power bandwidth, but also has to consider the switching frequency of the current dumping stage in order to get the described reduction of the output impedance. Therefore, we use a symmetric wide-band push–pull differential amplifier arrangement with a relatively low gain of 10 (defined by the internal current feedback resistors) which, on the other side, is high enough to use a conventional op-amp as feedback amplifier (output voltage swing $\pm$7 V). This op-amp is used as a PI-controller to increase the loop gain (and, therefore, reduce the switching frequency noise components) in the region of lower frequencies and to enhance the linearity of the system.

A further improvement of the loop gain could be achieved by the well-known principle of splitting up the voltage booster into a low-frequency part with full output voltage swing (for amplification of the actual input signal) and a high-frequency small-signal path being arranged in parallel to increase the loop gain in the switching frequency region [7]. However, in any case, the design of the feedback loop has to be adopted if the load impedance shows a capacitive portion due to the then given additional phase shift. In this case, it would be more efficient to directly improve the output impedance of the current buffer stage using a feedforward compensation [8] or an inner feedback/feedforward corrector scheme as proposed in [9]. It has to be noted that, concerning the output impedance, the realization of the output stage using bipolar power transistors would probably be a better solution because of their higher transconductance as compared to MOSFET's. On the other hand, power MOSFET's have the advantage of a rectangular safe operating area which is of importance for the pulse response of the amplifier (Fig. 5(b)).

V. Topology Survey

Concluding the paper, we want to give a brief survey of further topologies of switched-mode assisted linear power amplifiers. Fig. 9(a) shows a topology for reduction of the linear stage power losses by ripple cancellation using, e.g., four switching stages arranged in parallel and operated in a phase-shifted manner. The easiest way to obtain the optimum phase shift is the application of an explicit PWM with a superimposed linear current controller instead of the hysteresis current controller described so far. In this case, however, special controller extensions have to be added to guarantee a uniform current sharing between the several converter branches [10]. But, also, if hysteresis current controllers are applied (quasi-) optimal phase-shifted output currents of the single converter branches can be realized using coupled (or partially common) output inductors [11]. If the total ripple amplitude of each converter branch exceeds twice the average output current, soft-switching can be obtained by adding capacitors across the switching transistors [12]. The primary advantage of this structure is that the worse

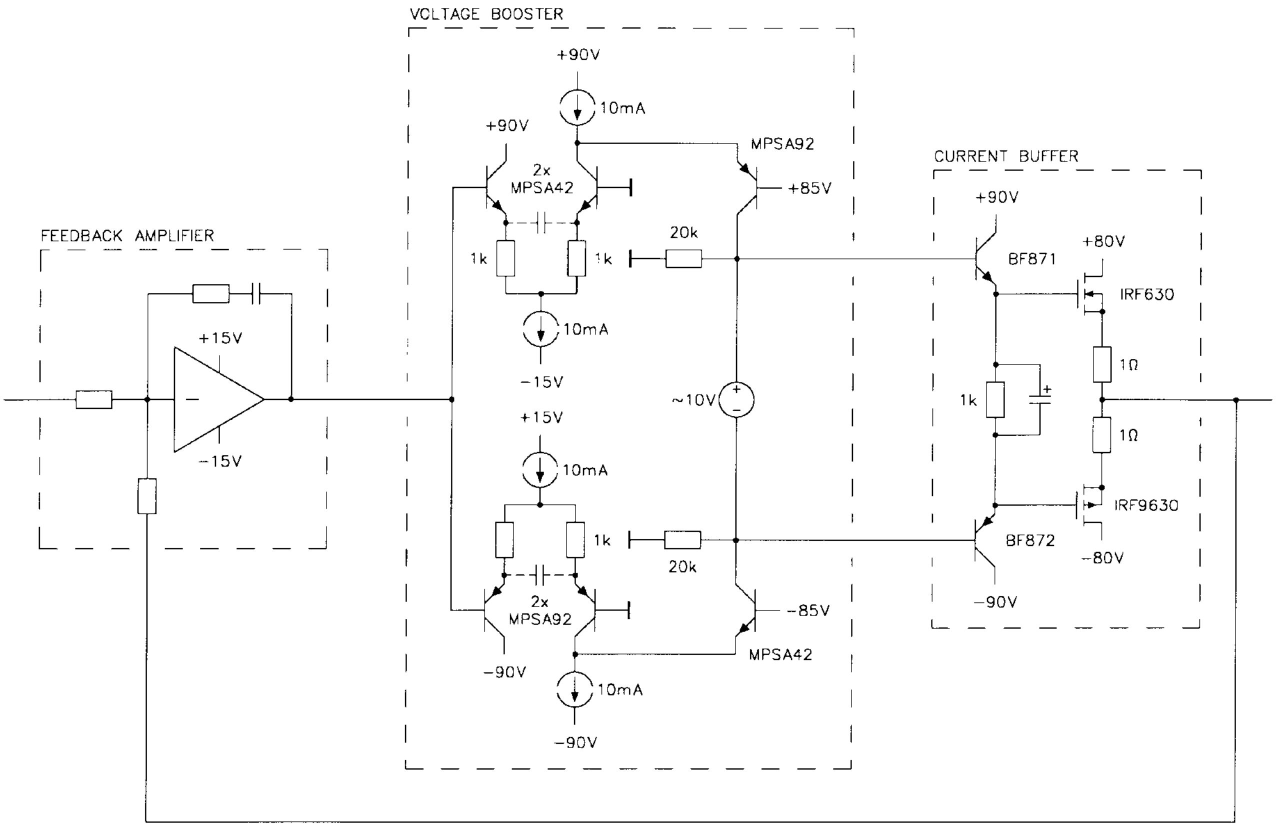


Fig. 8. Schematic diagram of the linear amplifier stage.

switching behavior of the MOSFET body diodes does not further contribute to the switching losses. However, the on-state losses are increased by ≈33% due to the triangular current waveform and the resistive on-state characteristic of power MOSFET's.

Contrary to the parallel converter branches discussed before, a ripple reduction also can be achieved using a switching stage of multilevel structure (e.g., shown in Fig. 9(b), the well-known three-level converter) which is of interest especially for high output voltages because switching power transistors with lower rated voltage can be used (e.g., 500 V power MOSFET's instead of 1000 V types which would lower the on-sate losses noticeably).

Fig. 9(c) shows a modification which is also of interest in the higher voltage region. P-channel power MOSFET's used in the linear amplifier stage usually are available only with rated voltages lower than 200–500 V. If the tolerance band of the hysteresis current controller is modified in that way, i.e., the linear stage only has to support positive output currents, the p-channel part can be omitted. However, in this case, the pulse response of the whole system is not uniform due to the different slew rates of the rising (defined by the linear stage) and the falling (defined by the switching stage) slope.

A freewheeling action of the relatively slow internal body diodes of the power MOSFET's can be avoided in the hard-switching mode by using the circuit topology shown in Fig. 9(d). There, explicit fast-recovery diodes can be used. The two branches of the system operate in parallel only concerning the ripple currents. Contrary to the circuit of Fig. 9(a), a very simple phase-shifted PMW control scheme can be applied because no load sharing has to be provided.

The presented fundamental operating principle of switched-mode assisted linear power amplifiers can also be extended to isolated converter structures which are of special interest because this solution avoids the explicit power supply unit (usually a switched-mode power supply for generating the dc supply voltage $\pm U$ being isolated from the mains). An isolated switched-mode assisted linear amplifier can be realized by the application of a full-bridge switching converter and a high-frequency isolating transformer (Fig. 9(e)). However, for nonresistive amplifier loads, a bidirectional power flow capability has to be considered and an active "rectifier" stage (four bidirectional switches at the secondary side of the high-frequency transformer) would be necessary [13], [14]. The switched-mode stage is supplied, for example, by the rectified ac mains voltage, whereas an additional dc–dc converter (not shown in Fig. 9(e)) is required to generate the (isolated) supply voltage of the linear amplifier stage (realized here also using a full-bridge topology). The output power of the dc–dc converter is about in the range of the losses of the linear part and, therefore, relatively small as compared to the total output power of the amplifier. A further possibility for achieving an isolated current dumping stage would be the application of a class D amplifier based on a four-quadrant Cuk-converter as described in [15] (Fig. 9(f)), which would reduce the number of switching transistors significantly as compared to the topology of Fig. 9(e).

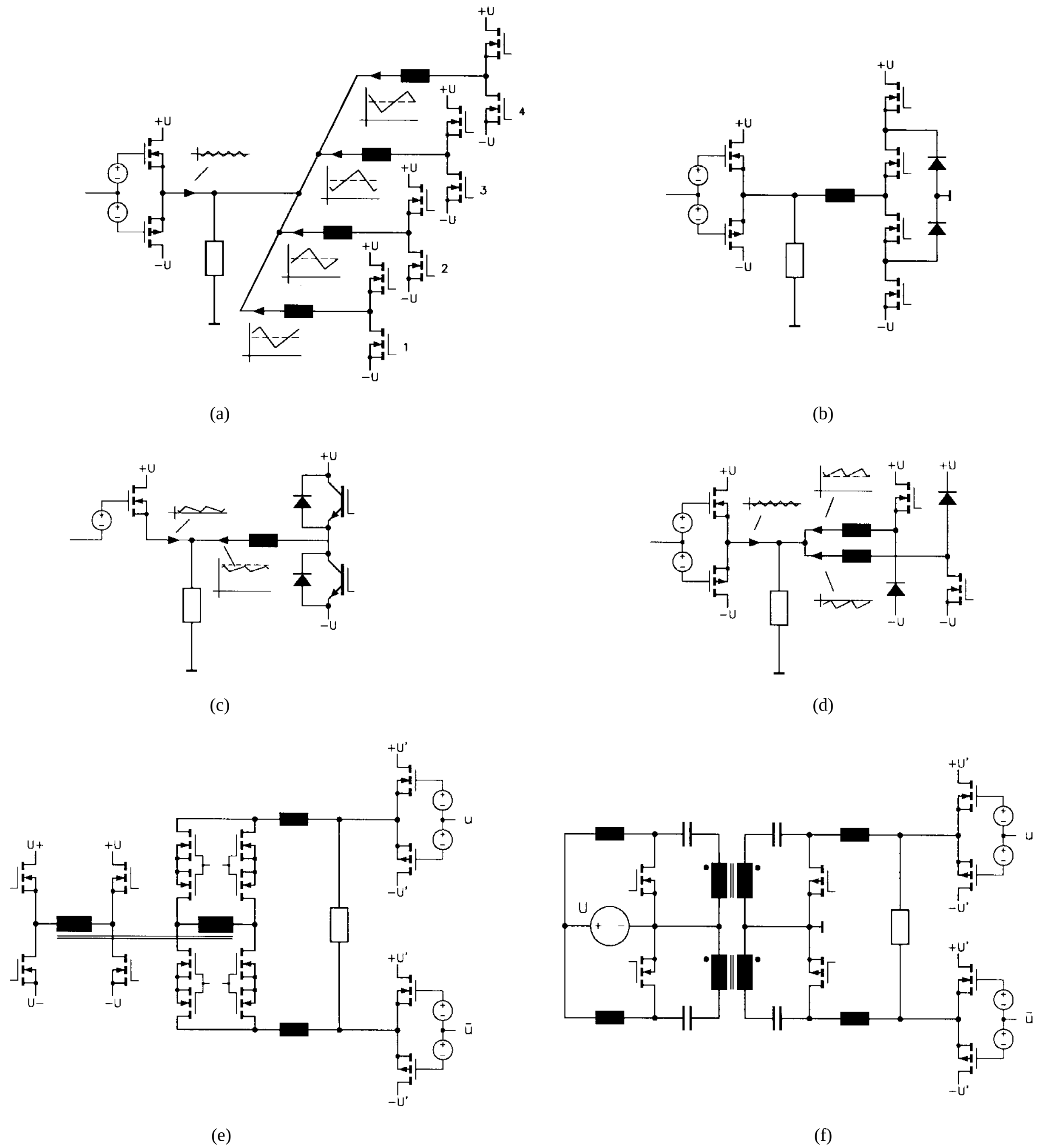


Fig. 9. Further topologies of switched-mode assisted linear power amplifiers. (a) Ripple reduction by multiple bridge legs operated with a phase shift. (b) Ripple reduction using a three-level topology. (c) Avoiding the p-channel MOSFET of the linear stage (high-voltage applications). (d) Ripple reduction using two parallel branches with explicit freewheeling diodes (e.g., Schottky-diodes). (e) Isolated topology using bidirectional rectification and a linear amplifier in full-bridge configuration. (f) Isolated topology using a four-quadrant Cuk-converter.

In this paper, the basic relationships of combining linear power amplifiers with current-dumping switching amplifiers has been presented. Presently, a laboratory model of the system which is described and simulated in Section IV is realized. Measuring results, and experiences taken from the practical realization, will be presented in a future paper. Furthermore, the analysis of an extension of the proposed system applying a capacitive coupling of the linear stage to the switching stage for a further improvement of the system efficiency is under preparation.

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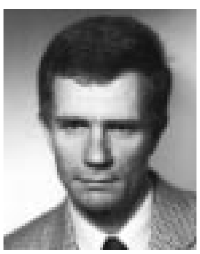

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He is the author of approximately 100 technical and scientific papers and patents and two books concerning automatic control and power electronics, the latter of which is being prepared for its fourth edition. His current activities lie in the area of power electronics and associated controls, especially as used for power supplies and electrical drives.