Power Electronic Systems
Laboratory

Proceedings of the IEEE Energy Conversion Congress & Expo (ECCE USA 2016), Milwaukee, WI, USA, September 18-22, 2016

Comparative Evaluation of a Triangular Current Mode (TCM) and Clamp-Switch TCM DC-DC Boost Converter

O. Knecht,
D. Bortis,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Comparative Evaluation of a Triangular Current Mode (TCM) and Clamp-Switch TCM DC-DC Boost Converter

O. Knecht, D. Bortis and J. W. Kolar
Power Electronic Systems Laboratory, ETH Zürich, Switzerland, Email: knecht@lem.ee.ethz.ch

***Abstract*— For the power management of a wireless power transfer system for implantable mechanical heart pumps, an additional boost DC-DC converter stage is needed in order to control the power delivered to the implant. Particularly, battery powered and implantable medical devices pose special demands on the efficiency and/or power density of the employed converters. Accordingly, soft-switching and/or high switching frequencies must be targeted. Modulation schemes that allow for Zero-Voltage-Switching (ZVS) such as Triangular Current Mode (TCM) offer a highly efficient operation, but suffer from a large operating frequency variation, which is mainly limited by the digital control. Therefore the Clamp-Switch TCM (CL-TCM) converter can be employed which allows also for the control of the switching frequency variation. In this paper, the CL-TCM and the TCM converter are compared regarding the power conversion efficiency and the power density of the converter. Since the CL-TCM converter is not well known in the literature, the converter is analysed in detail and a modulation scheme is explained that allows for ZVS for all switches in the entire range of operation. In addition, the requirements for ZVS and a control scheme (i.e. timing calculations) are provided for the converter in order to limit the maximum switching frequency. The modulation and control scheme are verified with a hardware prototype. Finally, the performance of the CL-TCM converter is measured and compared to the performance of the converter operated in TCM mode. The measurements show that the CL-TCM converter offers similar performance compared to the TCM operation at lower inductor power density, but has the advantage of a significantly reduced switching frequency variation. In applications, where a very high power density is needed, the TCM converter outperforms the CL-TCM converter in terms of efficiency.**

***Index Terms*—boost converter, clamp switch, triangular current mode (TCM) , zero voltage switching (ZVS)**

I. Introduction

Inductive Power Transfer (IPT) technology has proven to be a promising solution for powering medical implants without the need for a galvanic contact. As part of the Zurich Heart Project, a prototype of a highly efficient IPT system has been built [1] in order to supply electrical power to an implantable blood pump, such as a Left Ventricular Assist Device (LVAD), replacing the percutaneous driveline which is used in today's state-of-the-art implantable Mechanical Circulatory Support Systems (MCSS) and which imposes a severe risk of infection to the patient.

The basic structure of the power management of this Transcutaneous Energy Transfer (TET) system is shown in **Fig. 1**. The TET system's main power supply is a rechargeable battery pack which is carried by the patient. The power is fed to the IPT system which consists of an inverter stage, the energy transfer coils and a synchronous rectifier stage on the secondary side. In addition, an implanted backup battery allows for a temporary completely untethered operation of the LVAD. The typical continuous average power consumption of current state-of-the-art LVADs is in a range of 4-7 W with peak power consumption of up to 12 W [2], [3]. However, the maximum power transfer capability of the TET system has to be in a range of up to 25-30 W during the charging process of the implanted backup battery. The optimization of the IPT system in [1] has shown that it is beneficial to operate the IPT system at a higher input and output voltage $U_{\mathrm{DC},1}$ and $U_{\mathrm{DC},2}$ than the typical nominal battery pack output voltage of 14.8 V. Therefore, an additional boost converter is placed in between the primary battery and the inverter circuit. Similarly, a bidirectional DC-DC converter is needed on the secondary side as charging controller for the implanted backup battery, which is able to operate either in buck or boost mode, depending on the direction of the power flow (i.e. buck-mode for charging the battery). The design of the implanted DC-DC converter is particularly challenging because of the limited available volume and the need for a very high power conversion efficiency in order to limit the heating of the surrounding tissue to a safe level. In this work, the focus is on the realization of the primary side boost converter, where the main objective is the achievement of a high power conversion efficiency in order to allow for an extension of the runtime of the main battery.

Common realizations of quasi-resonant boost converters, that allow for Zero-Voltage-Switching (ZVS) are known in the literature as Synchronous Conduction Mode (SCM) [4], [5] or Triangular Current Mode (TCM) [6]–[8] operation. However as will be discussed in **Section II**, these modulation schemes show limitations regarding the power conversion efficiency or operability. Therefore, a second ZVS converter topology comprising an inductor clamp switch [9], [10] and featuring a limited switching frequency variation is analysed in detail and compared to the TCM operation. In addition, a modulation scheme [11] of the Clamp-Switch TCM (CL-TCM) converter is presented in **Section III** that allows for ZVS of all switches in the entire range of operation, i.e. in the input or output voltage and power range. The fundamental design considerations and the timing calculations [10] needed for the operation of the CL-TCM converter are provided in **Section IV**. In **Section V** the realized hardware prototype of the CL-TCM converter is presented and its performance is compared to the TCM operation using experimental results. Concluding remarks are given in **Section VI**.

II. Converter Evaluation

The very basic structure of the boost converter that can be operated either in hard-switched or soft-switched SCM or TCM operation is shown in **Fig. 1(b)**. In hard-switched operation, the inductor current is always positive and the switch T_2 experiences a hard turn-on when the positive inductor current is commutated from the body diode of switch T_1 to the low-side switch T_2. As a result, the losses in the switch are increased significantly. Soft-switching of the converter can be achieved if the inductor current has a negative value at the end of the time interval T_{off}. If the negative inductor current is able to deliver enough charge during the dead-time interval to fully discharge the parasitic output capacitance of the switch T_2 and charge the output capacitance of T_1, the switch T_2 can turn on with negligible

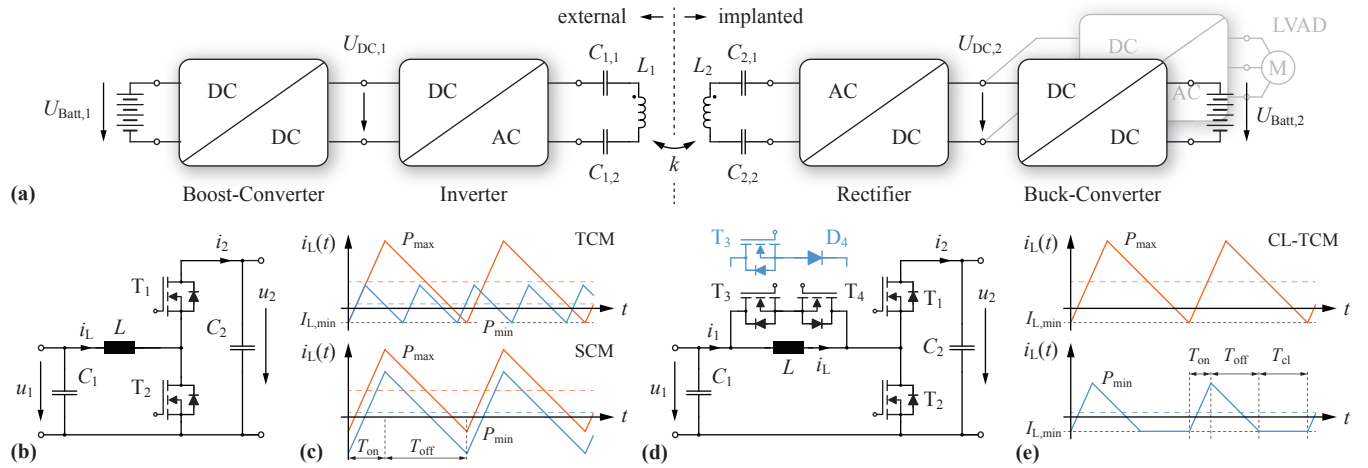


Figure 1: (a) Basic power management concept of the Transcutaneous Energy Transfer (TET) system. (b) Standard boost converter topology and (c) the inductor waveforms for Synchronous Conduction Mode (SCM) and Triangular Current Mode (TCM) operation. (d) Clamp-Switch TCM (CL-TCM) boost converter topology and (e) the associated inductor current waveforms.

power loss. The inductor current waveform of the TCM and SCM operation of the converter are shown schematically in **Fig. 1(c)** for minimum and maximum output power. In the SCM operation, the inductor peak-to-peak current ripple is constant and independent of the output power. As a result, the switching frequency can be kept at a constant value, but the converter suffers from a low power conversion efficiency at light load conditions due to the high RMS inductor current. A better performance is offered by the TCM operation where the minimum inductor current $I_{\mathrm{L,min}}$ is kept at a constant value, large enough to ensure ZVS. The output power is then controlled by varying the on-time interval T_{on} of the switch T_2. As a result, the RMS inductor current is reduced at part load operation, but the switching frequency increases significantly. Assuming a constant input voltage and a lossless operation, the variation of the switching frequency can be expressed with

$$n_{f,\mathrm{TCM}} = \frac{f_{\max}}{f_{\min}} = \frac{(P_{\max} - I_{\mathrm{L,min}} u_1)}{(P_{\min} - I_{\mathrm{L,min}} u_1)} \frac{(u_{2,\max} - u_1)}{(u_{2,\min} - u_1)} \frac{u_{2,\min}}{u_{2,\max}} . \quad (1)$$

The frequency variation depends on the output power and output voltage variation $u_2 \in [u_{2,\min}, u_{2,\max}]$ and can be very large, depending on the range of operation. The maximum switching frequency $f_{\max}$ occurs at minimum output power and maximum voltage conversion ratio and is mainly limited by the time delays in the measurement and control circuit, as the switching time intervals need to be calculated and synchronized to the zero-crossings of the inductor current.

In order to address this drawback, an additional clamp-switch is introduced in parallel to the inductor, comprising an anti-series connection of the two switches T_3 and T_4 enabling bidirectional voltage blocking, as it is shown in **Fig. 1(d)**. Note that the on-state resistance of the clamp-switches can be higher compared to the switches T_1 and T_2, since they do not have to directly conduct the load current. Hence, a switch with lower parasitic output capacitance can be used for the clamp-switches. For unidirectional power flow, the clamp-switch can be implemented with only one switch T_3 and diode D_4.

At maximum output power, the CL-TCM operation corresponds to the TCM operation. Hence, the inductor current has a triangular shape with a negative inductor current $I_{\mathrm{L,min}}$ that allows for ZVS of the two main switches T_1 and T_2. However, at light load operation, the clamp-switch allows to introduce a free-wheeling state for the inductor current after the turn-off of the switch T_1 and hence, stretches the switching period as it is shown in **Fig. 1(e)**. As a result, the switching frequency variation is reduced significantly, which relaxes the requirements for the control circuit and allows to operate the converter at a higher switching frequency in the entire range of operation when compared to the TCM converter, implemented for the same maximum switching frequency.

The clamp-switch converter topology is implemented e.g. in the Picor Cool-Power ZVS Buck Regulator Series provided by Vicor and is explained briefly in [9]. However, the realization of the clamp-switch itself is not shown and the soft-switching is shown only for the switches T_1 and T_2 and no ZVS modulation scheme for the full converter is described. Therefore, in the following section, the operation of the CL-TCM is explained in detail and a new modulation scheme [11] is shown which guarantees soft-switching for all switches.

III. CL-TCM Modulation Scheme

The detailed operating principle of the proposed modulation of the CL-TCM converter in boost operation is shown in **Fig. 2**. The inductor current and switch-node voltage waveforms belonging thereto are shown in **Fig. 3(a)**. Starting with the first time interval $[t_0, t_1]$, switch T_2 is conducting and the inductor current rises linearly. The clamp switch T_4 is in on-state and the body diode of switch T_3 is in blocking state and prevents a short circuit of the input capacitor C_1. As soon as the inductor current reaches the value $I_{\mathrm{L},1}$, switch T_2 turns off and the inductor current charges the parasitic output capacitance of switch T_2, while discharging the output capacitances of T_1 and T_3. During $[t_1, t_2]$, the voltage u_{sw} rises until the body diode of switch T_3 starts to conduct. In $[t_2, t_3]$ the inductor voltage is clamped to the diode forward voltage drop u_{DF} and switch T_3 can be turned on at nearly zero voltage at t_3. The time interval $[t_3, t_4]$ is an intermediate step, where the inductor current is free-wheeling through the clamp switches. This step is important in order to reverse the voltage blocking capability of the clamp switches, before the inductor current starts decreasing and reverses its direction at time t_6'. In practice, the time interval $[t_3, t_4]$ must be as short as possible in order to minimize the power loss in the clamp switches. At t_4, switch T_4 is turned off and during $[t_4, t_5]$

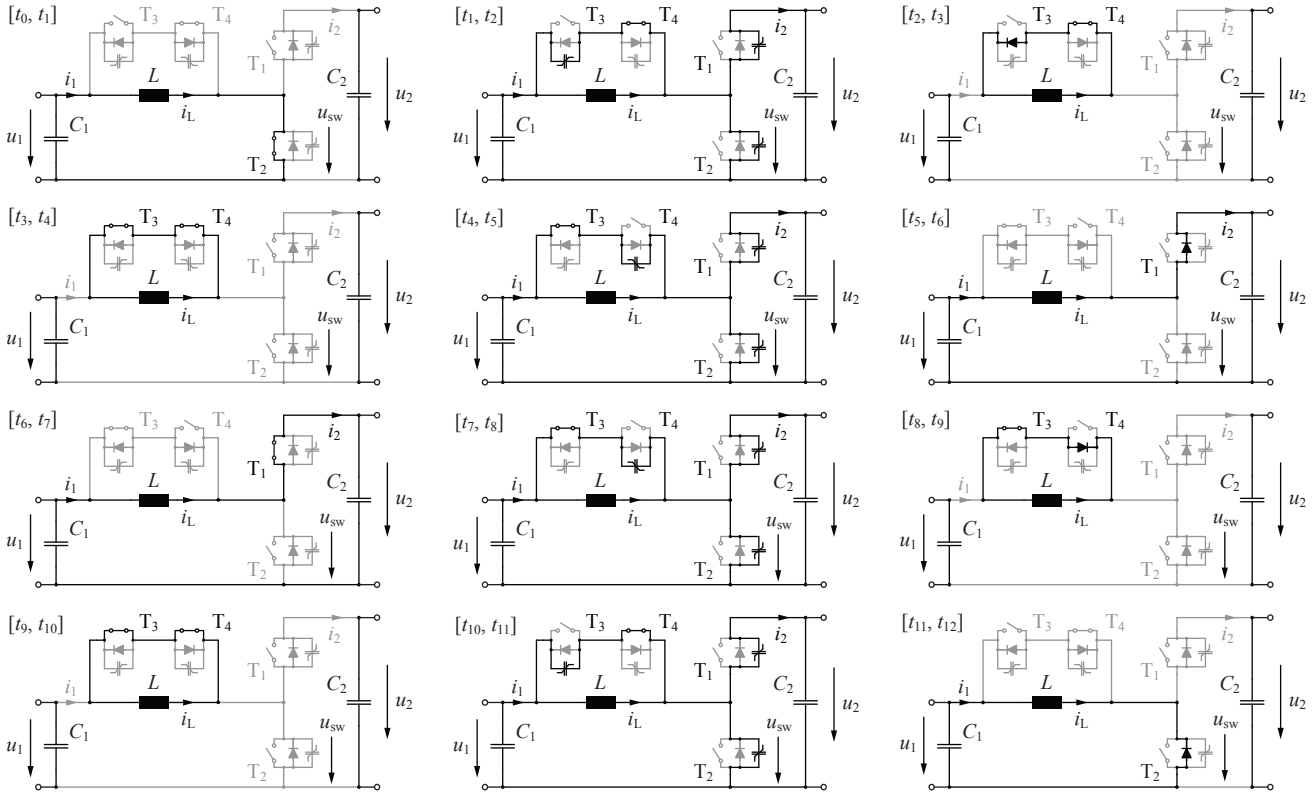


Figure 2: Operating states of the proposed ZVS modulation scheme for a full switching cycle $[t_0, t_{12}]$.

the inductor current charges the parasitic output capacitance of the switches T_2 and T_4 and further discharges the output capacitance of T_1. As soon as the parasitic output capacitance of switch T_1 is fully discharged, the anti-parallel diode starts to conduct in t_5 and clamps the voltage across the switch to u_{DF} as shown in the time interval $[t_5, t_6]$. As a result, at time t_6, switch T_1 can be turned on at zero voltage. Note that the diode of switch T_4 is in blocking state and prevents a short circuit of the converter's input and output terminal. In the time interval $[t_6, t_7]$ the inductor current is supplied to the output and is decreasing. The zero-crossing of the inductor current at time $t_6^{'}$ is detected and is used to determine the turn-off time delay of switch T_1 that is needed in order to generate the required negative inductor current $I_{\mathrm{L},0}$ to achieve ZVS of the switches in the remaining time intervals.

At t_7, switch T_1 is turned off and the negative inductor current discharges the parasitic output capacitance of the switches T_2 and T_4, while charging the output capacitance of switch T_1 during $[t_7, t_8]$. When the voltage u_{sw} reaches a value of $(u_1 + u_{\mathrm{DF}})$ at t_8, the anti-parallel diode of switch T_4 starts to conduct. As a result, switch T_4 can be turned on at zero voltage at the time t_9. During the time interval $[t_9, t_{10}]$, the inductor current is free-wheeling in negative direction through the clamp-switch. In this time interval there is no energy delivered from the input to the output and can therefore be used as a degree of freedom to control the switching period and the amount of power delivered to the load. In the clamping time interval, the inductor current amplitude is continuously decreasing due to the power losses in the clamp switches and in the inductor. This has to be taken into account if the clamping time interval is very large, because the current amplitude could fall below a minimum value, where ZVS of switch T_2 cannot be achieved anymore in the following time intervals. At t_{10}, switch T_3 is turned off and the negative inductor current continues discharging the parasitic output capacitance of switch T_2 until the switch-node voltage u_{sw} reaches zero and the diode of switch T_2 starts to conduct as shown in time interval $[t_{11}, t_{12}]$. The inductor current is rising and switch T_2 must be turned on before the current zero crossing to allow for ZVS of T_2.

Similar to the analysis provided in [8] for TCM operation, an u-Zi-diagram (phase diagram) shown in **Fig. 3(b)** is used to reveal the basic criteria that must be met in order to achieve soft-switching of the switches after the resonant transitions. In this representation, constant parasitic output capacitances are assumed for the switches $\mathrm{T}_1 - \mathrm{T}_4$. Therefore, as explained in [8], the resonant transition time and the required currents to enable ZVS can be calculated with good approximation using the charge equivalent capacitance of the switches. For the hardware prototype described in **Section V**, each switch is composed of a Gallium Nitride (GaN) Field Effect Transistor (FET) placed in parallel with an additional Schottky diode to lower the voltage drop across the switch in diode conduction mode. The total capacitance C_{tot} of the switch is therefore given by the sum of the switch output capacitance C_{oss} and the Schottky diode junction capacitance C_{j}. **Fig. 4(a)** shows the total capacitance given by the employed GaN FET EPC2016C and the Schottky diode MBR1H100SF, as well as the total stored charge Q_{tot} and the charge equivalent capacitance which can be calculated using [12],

$$C_{\mathrm{Q,eq}}(V) = \frac{1}{V} \int_0^V C_{\mathrm{tot}}(v) \mathrm{d}v \,. \tag{2}$$

The resonant transition in the time intervals $[t_7, t_8]$ and $[t_{10}, t_{11}]$ can be described in the u-Zi-diagram as a circle with the center at

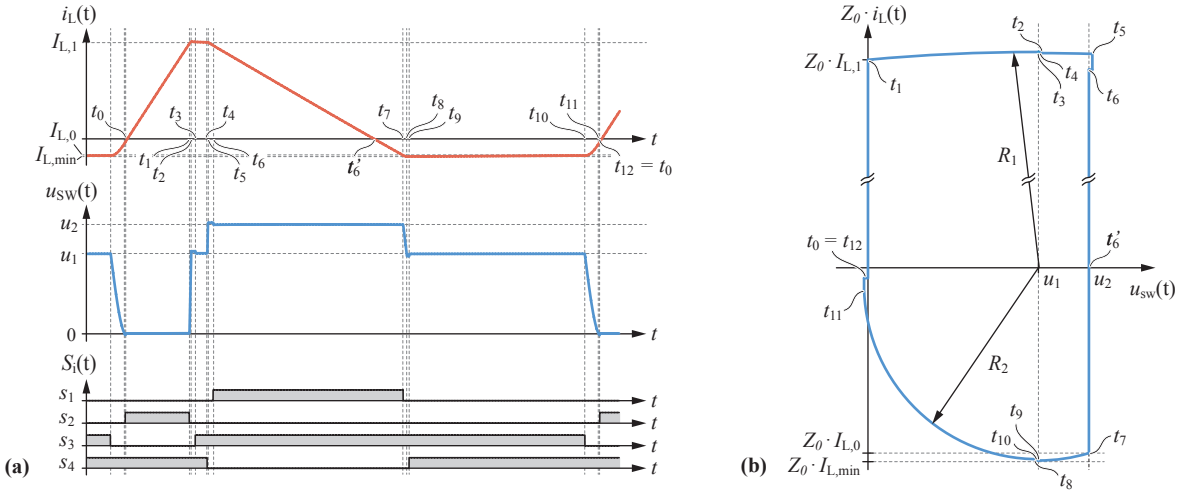


Figure 3: (a) Typical waveforms of the inductor current i_L and switch-node voltage u_sw and the switching states t_1 to t_{12}. (b) u-Zi-diagram, showing the scaled inductor current $Z_0 i_\mathrm{L}(t)$ with respect to the switch-node voltage $u_\mathrm{sw}(t)$.

$u_\mathrm{sw} = u_1$ and $i_\mathrm{L} = 0$ and a radius given by

$$R_2 = \sqrt{(Z_0 I_{\mathrm{L},0})^2 + (u_2 - u_1)^2}, \quad \text{with} \quad Z_0 = \sqrt{\frac{L}{C_{\mathrm{Q,eq,tot}}}} \,. \tag{3}$$

As shown in **Fig. 4(b)**, during the time interval $[t_7, t_8]$ the capacitance C_{T1} is charged from 0 V to $(u_2 - u_1)$, neglecting the forward voltage drop u_DF of the Schottky diode. The capacitances C_{T2} and C_{T4} are discharged from u_2 to u_1 and from $(u_2 - u_1)$ to 0 V, respectively. Assuming the same non-linear capacitance C_tot for each switch, the total delivered charge and the associated charge equivalent capacitance can be calculated with

$$\begin{aligned} \Delta Q_{\mathrm{C,T1}} &= \int_0^{u_2-u_1} C_{\mathrm{tot,T1}}(v)\mathrm{d}v \\ \Delta Q_{\mathrm{C,T2}} &= \int_0^{u_2} C_{\mathrm{tot,T2}}(v)\mathrm{d}v - \int_0^{u_1} C_{\mathrm{tot,T2}}(v)\mathrm{d}v \\ \Delta Q_{\mathrm{C,T4}} &= \int_0^{u_2-u_1} C_{\mathrm{tot,T4}}(v)\mathrm{d}v \\ \Delta Q_{\mathrm{tot,c}} &= \Delta Q_{\mathrm{C,T1}} + \Delta Q_{\mathrm{C,T2}} + \Delta Q_{\mathrm{C,T4}} \end{aligned} \,. \tag{4}$$

and

$$C_{\mathrm{Q,eq,tot,c}} = \frac{\Delta Q_{\mathrm{tot,c}}}{\Delta U_{\mathrm{tot,c}}} = \frac{\Delta Q_{\mathrm{tot,c}}}{(u_2 - u_1)} \,. \tag{5}$$

Similar considerations can be made for the time interval $[t_{10}, t_{11}]$. In this case, at the end of the clamping interval, the resonant transition is initiated with the turn-off of switch $\mathrm{T_3}$. The switching state of the converter and the flow of the current in the parasitic capacitances is shown in **Fig. 4(c)**. The capacitance C_{T2} is further discharged from u_1 to 0 V and the capacitances C_{T1} and C_{T3} are charged from $(u_2 - u_1)$ to u_2 and from 0 V to u_1, respectively. The total delivered charge is then given by

$$\begin{aligned} \Delta Q_{\mathrm{C,T1}} &= \int_0^{u_2} C_{\mathrm{tot,T1}}(v)\mathrm{d}v - \int_0^{u_2-u_1} C_{\mathrm{tot,T1}}(v)\mathrm{d}v \\ \Delta Q_{\mathrm{C,T2}} &= \int_0^{u_1} C_{\mathrm{tot,T2}}(v)\mathrm{d}v \\ \Delta Q_{\mathrm{C,T3}} &= \int_0^{u_1} C_{\mathrm{tot,T3}}(v)\mathrm{d}v \\ \Delta Q_{\mathrm{tot,d}} &= \Delta Q_{\mathrm{C,T1}} + \Delta Q_{\mathrm{C,T2}} + \Delta Q_{\mathrm{C,T3}} \end{aligned} \,, \tag{6}$$

and the charge equivalent capacitance can be calculated with

$$C_{\mathrm{Q,eq,tot,d}} = \frac{\Delta Q_{\mathrm{tot,d}}}{\Delta U_{\mathrm{tot,d}}} = \frac{\Delta Q_{\mathrm{tot,d}}}{u_1} \,. \tag{7}$$

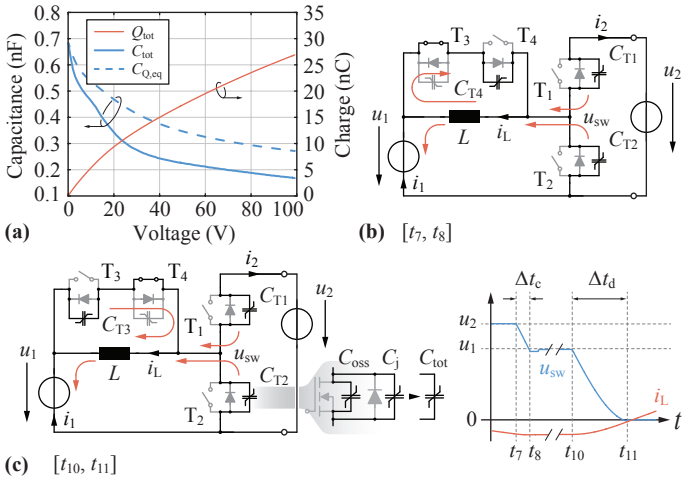


Figure 4: (a) Total switch output capacitance, charge-equivalent capacitance and stored charge. (b) Illustration of the current flow during the resonant voltage transition in time interval $[t_7, t_8]$ and (c) in time interval $[t_{10}, t_{11}]$.

Hence, the total charge equivalent capacitance associated with the total resonant transition from t_7 to t_{11} can be calculated with

$$C_{\mathrm{Q,eq,tot}} = \frac{\Delta Q_{\mathrm{tot,c}} + \Delta Q_{\mathrm{tot,d}}}{u_2} \,. \tag{8}$$

The absolute minimum inductor current $I_{\mathrm{L},0}$ at the time instant t_7, required for soft-switching of the switch $\mathrm{T_2}$ at the time t_{11} can then be calculated using (3) and (8)

$$I_{\mathrm{L},0} \leq -\frac{1}{Z_0}\sqrt{u_2\,(2u_1 - u_2)} \,, \quad \text{for} \quad \left(u_1 \geq \frac{u_2}{2}\right) \,. \tag{9}$$

In this case, the critical operating point, where soft-switching of $\mathrm{T_2}$ could be lost, is at the minimum output voltage, regardless of the power delivered to the load.

The time interval $\Delta t_c = t_8 - t_7$ of the resonant transition can then be calculated using the geometric relations depicted in the u-Zi-diagram and the equation for the radius R_2 given in (3),

$$\Delta t_\mathrm{c} = \frac{1}{\omega_{0,\mathrm{c}}}\left[\arctan\left(\frac{I_{\mathrm{L},0} Z_{0,\mathrm{c}}}{u_2 - u_1}\right) + \frac{\pi}{2}\right] \,, \tag{10}$$

with the characteristic impedance and the resonant frequency calculated with the charge equivalent capacitance given in (5),

$$Z_{0,c} = \sqrt{\frac{L}{C_{\mathrm{Q,eq,tot,c}}}} \quad \text{and} \quad \omega_{0,c} = \frac{1}{\sqrt{L \cdot C_{\mathrm{Q,eq,tot,c}}}} \,. \tag{11}$$

The peak negative inductor current can then be calculated with

$$I_{\mathrm{L,min}} = -\frac{R_2}{Z_{0,\mathrm{c}}} = -\frac{1}{Z_{0,\mathrm{c}}} \sqrt{(Z_{0,c} I_{\mathrm{L},0})^2 + (u_2 - u_1)^2} \,. \tag{12}$$

Similar to the previous case, the time interval $\Delta t_d = t_{10} - t_{11}$ of the resonant transition can be calculated using equation (11), substituted with the charge equivalent capacitance from (7) and is given by

$$\Delta t_d = \frac{1}{\omega_{0,\mathrm{d}}} \arcsin\left(\frac{u_1}{|I_{\mathrm{L,min}}| \cdot Z_{0,\mathrm{d}}}\right) \,. \tag{13}$$

Due to the large inductor current $I_{\mathrm{L},1}$ at time t_1, the time intervals $[t_1, t_2]$ and $[t_4, t_5]$ are very short and can be neglected in the general case. The critical operating point where soft-switching of T_1 could be lost is at the maximum output voltage and very low output power.

Note that the modelling of the resonant transition using the charge equivalent capacitance is an approximation only. But as shown in **Fig. 4(a)**, the total charge of the GaN FETs and the parallel Schottky diode does not show a high non-linearity. Hence, the equations (10)-(13) allow for an accurate modelling of the operation of the CL-TCM converter during the resonant voltage transitions and a relative error of less than 5 % was obtained for time intervals Δt_c and Δt_d when compared to a circuit simulation. The minimum negative inductor current $I_{\mathrm{L},0}$ required to achieve ZVS can be predicted using equation (9). However, a relative error of up to 10 % was obtained for the specifications and range of operation used for the prototype converter.

Based on the operating principle shown in this section, the control scheme of the converter was derived similar to [10] as presented in the following section.

IV. CL-TCM Boost Operation

For TCM operation, the on-time of the switch T_2 is the only degree of freedom available in order to control the power delivered to the load. But for the CL-TCM modulation, the clamping time interval $[t_9, t_{10}]$ is an additional degree of freedom which is used to control the switching frequency variation of the converter. In order to minimize the RMS inductor current, it is beneficial to emulate TCM operation at the nominal output power, where the clamping time interval is set to zero. This implies that the operating frequency is still allowed to vary in a certain range due to variations of the input or output voltage. However, for constant terminal voltages but varying output power, the clamping time interval is used to control the average input current, while maintaining a constant switching frequency. A constant switching frequency could also be maintained despite a variation of the terminal voltages, but in this case, the adjustment of the clamping time-interval would lead to an increase of the inductor RMS current and is therefore not desirable.

The digital control circuit can be implemented as illustrated in **Fig. 5**. The operation of the converter is determined by the time intervals T_{on}, T_{off} and T_{cl}. In order to set the negative inductor current $I_{\mathrm{L,min}}$, the zero crossing of the current needs to be sensed. For the converter prototype, the inductor current was measured directly at the inductor using a 10 mΩ resistor in the inductor current path. However, it is recommended to measure the current i_{T2} at the resistor R_{cm} depicted in **Fig. 5** in order to determine the zero crossing of the

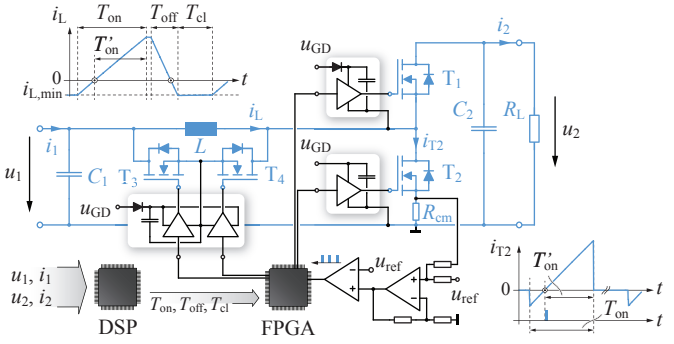


Figure 5: Realization of the control structure and recommended implementation of the inductor current zero crossing detection using a current measurement resistor at the low-side switch T_2.

inductor current during time interval T_{on}, which has the advantage of a reduced power loss and a significant simplification of the measurement circuit.

At a rising inductor current, as soon as the current zero crossing is detected, the switch T_2 is held in on-state until to the end of the time interval T'_{on}. This ensures a synchronization of the inductor current to the desired minimum and maximum value such that the required average input current is achieved. The total on-time of switch T_2 can be calculated for a desired average input current I_{in} and input voltage u_1 using

$$T_{\mathrm{on}} = \frac{L}{u_1} \left(\sqrt{4 I_{\mathrm{in}} \left(\frac{P_{\mathrm{max}}}{u_1} - I_{\mathrm{L,min}} \right) + I_{\mathrm{L,min}}^2} + |I_{\mathrm{L,min}}| \right) \,, \tag{14}$$

and therefore, assuming that the inductor current starts rising always from the desired negative value $I_{\mathrm{L,min}}$, the remaining on-time T'_{on} is estimated with

$$T'_{\mathrm{on}} = T_{\mathrm{on}} - \frac{L}{u_1} |I_{\mathrm{L,min}}| \,. \tag{15}$$

The remaining time intervals T_{off} and T_{cl} can then be calculated with

$$T_{\mathrm{off}} = T_{\mathrm{on}} \left(\frac{u_1}{u_2 - u_1} \right) \quad \text{and} \quad T_{\mathrm{cl}} = T_{\mathrm{p,Pmax}} - T_{\mathrm{on}} - T_{\mathrm{off}} \,, \tag{16}$$

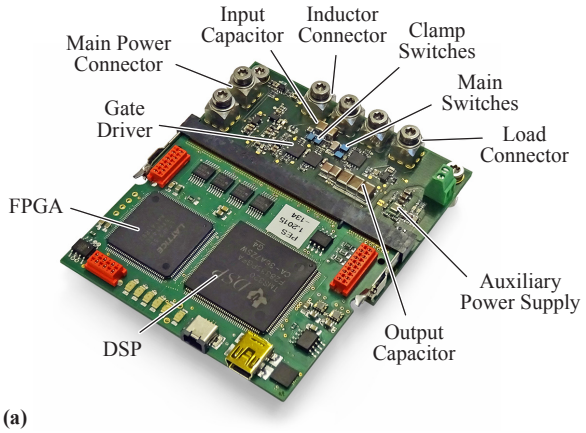
using the switching period T_{p} evaluated for the nominal output power P_{max}, calculated with

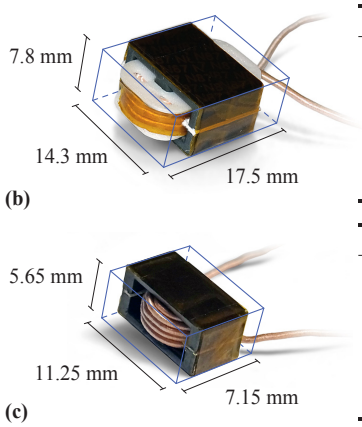
$$T_{\mathrm{p,Pmax}} = \frac{2 u_2 L \left(P_{\mathrm{max}}/u_1 - I_{\mathrm{L,min}} \right)}{u_1 \left(u_2 - u_1 \right)} \,. \tag{17}$$

Note that the equations (14)-(17) assume a lossless operation of the converter and the resonant transition times are neglected. In a practical design, these equations can be evaluated using a Digital Signal Processor (DSP) or the timing intervals can be calculated in advance for a defined range of operation and during operation, the timing values are interpolated using a look-up table. An FPGA is used in addition to keep track of the timing and to control the gate signals. Note that an update of the timing values is needed only when a change of the load conditions is detected or due to a change of the output voltage reference. Therefore, the update frequency is limited to the controller bandwidth, which is usually much slower than the switching frequency.

As a result of this control scheme, the switching frequency variation is independent of the variation of the output power and can be expressed with

$$n_{f,\mathrm{CL}} = \frac{f_{\mathrm{max,CL}}}{f_{\mathrm{min,CL}}} = \frac{u_{2,\mathrm{min}}}{u_{2,\mathrm{max}}} \cdot \frac{(u_{2,\mathrm{max}} - u_1)}{(u_{2,\mathrm{min}} - u_1)} \,. \tag{18}$$





Parameter	Value
Inductance	7.51 µH
Litz Wire	300 x 40 µm
Turns	9
Core Material	N87
Core	2x EELP 14
Total Air Gap	0.56 mm
Power Density	15.4 W/cm^3

Parameter	Value
Inductance	4.39 µH
Litz Wire	135 x 40 µm
Turns	9
Core Material	N87
Core	ER 11/5
Total Air Gap	0.46 mm
Power Density	66.0 W/cm^3

Figure 6: (a) Hardware prototype of the CL-TCM converter including the control board. (b)-(c) Realization and technical specifications of the inductors used for the performance evaluation of the CL-TCM converter.

Accordingly, the inductance value can be determined using (17) such that a specified maximum switching frequency $f_{\max}$ is not exceeded for the specified range of operation,

$$L = \frac{u_1^2 \left(u_{2,\max} - u_1\right)}{2u_{2,\max} f_{\max} \left(P_{\max} - u_1 I_{\mathrm{L,min}}\right)} \,. \tag{19}$$

If the CL-TCM converter is designed for the same maximum switching frequency as for TCM operation, the inductance value needed for the CL-TCM converter is much smaller compared to the inductance value needed for TCM operation. The ratio of the inductance needed for the CL-TCM and TCM converter for this particular case is given mainly by the output power range and can be calculated with

$$n_{\mathrm{L}} = \frac{L_{\mathrm{CL}}}{L_{\mathrm{TCM}}} = \frac{P_{\min} - I_{\mathrm{L,min,TCM}} \cdot u_1}{P_{\max} - I_{\mathrm{L,min,CL}} \cdot u_1} \,. \tag{20}$$

On the other hand, if the CL-TCM converter is designed for the same minimum switching frequency as for TCM operation with the same range of output voltage and output power, the required inductance value is the same for both modes of operation.

In order to verify the proposed operation of the CL-TCM converter, a hardware prototype was built and is presented in the following section together with experimental results.

V. Hardware Prototype & Measurements

Fig. 6(a) shows the hardware prototype of the CL-TCM converter. As mentioned in the previous sections, the EPC2016C GaN FETs are used for the prototype, operated with the half-bridge gate-driver LM5113. As shown in **Fig. 5**, a boot-strap power supply was used also for the clamp switch gate drivers which allows for a very simple and compact design of the additional four-quadrant switch. The converter is controlled with a DSP/FPGA control board comprising a Texas Instruments TMS320F28335 DSP and a Lattice LFXP2-5E FPGA. The control board is not optimized for this converter and could be designed with significantly reduced footprint and power loss. The prototype is designed according to the specifications given by the application for an input voltage of 14.8 V and an output voltage range of 20-50 V.

In order to directly compare the CL-TCM and TCM operation of the converter, the same inductor is used for both modes of operation, such that both converter have the same minimum switching frequency. The hardware realization and the technical specifications of the inductors are shown in **Fig. 6(b)** and **(c)**. The inductor shown in **Fig. 6(b)** is

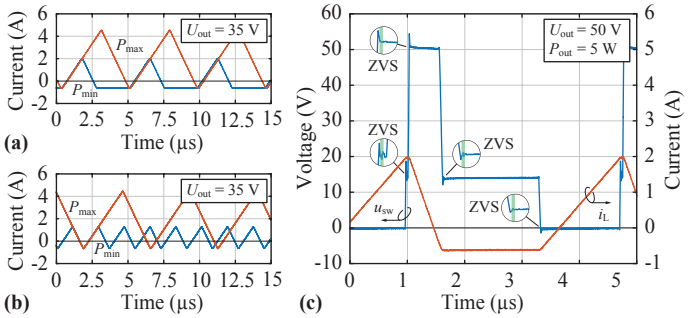


Figure 7: (a)-(b) Measured inductor current waveforms of the prototype converter in CL-TCM operation and TCM mode respectively. (c) Measured CL-TCM converter switch-node voltage u_{sw} and inductor current i_{L} indicating ZVS operation.

built using two EELP 14 core sets with the EPCOS N87 material. The inductor is designed for high-efficiency operation with a minimum converter switching frequency of 100 kHz and has therefore a rather low peak power density of 15.4 W/cm^3. The second inductor shown in **Fig. 6(c)** is built using an ER 11/5 core set in order to achieve a high peak inductor power-density of 66 W/cm^3, and is designed such that the switching frequency reaches a maximum value of $f_{\max} = 1\,\mathrm{MHz}$ in TCM mode.

For the measurements, the output power range is set to 5-30 W and the output voltage is set to 20 V, 35 V and 50 V. The converter was operated in open-loop and the input voltage was kept in a range of 14.4-14.8 V. The inductor current waveform for minimum and maximum output power for an output voltage of 35 V is shown in **Fig. 7(a)** and **(b)** for CL-TCM and TCM operation respectively. Soft-switching of the switches $\mathrm{T_1}$-$\mathrm{T_4}$ was achieved at any point of operation and is shown in **Fig. 7(c)** as an example for minimum output power and an output voltage of 50 V.

Fig. 8(a)-(c) show the measured and calculated inductor current characteristics, the switching frequency and the timing values T_{on}, T_{off} and T_{cl} set by the DSP to operate the converter in CL-TCM mode. **Fig. 8(d)-(f)** show the same measured and calculated parameter for the converter operated in TCM mode. The inductor shown in **Fig. 6(b)** was used for the measurements and the peak negative inductor current $i_{\mathrm{L,min}}$ was set to -0.67 A for both modes of operation such that the total dead-time needed for the time intervals $[t_7, t_9]$ and $[t_{10}, t_{12}]$ was

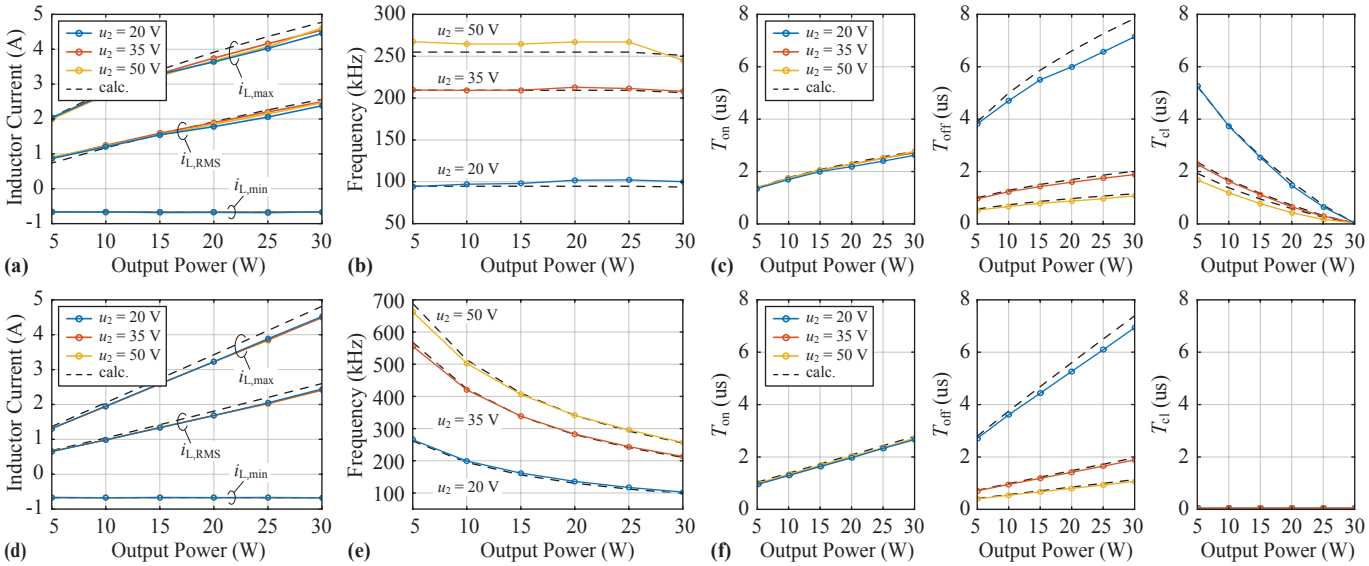


Figure 8: (a) Measured and calculated minimum, maximum and RMS inductor current values of the prototype CL-TCM converter. (b) Measured and calculated switching frequency and (c) on-, off- and clamping-time intervals of the CL-TCM converter. (d)-(f) show the same parameter measured for the converter operated in TCM mode.

not larger than 100 ns, which allows to neglect the dead-times for the timing calculations in the open-loop operation of the converter. For the TCM converter, the minimum inductor current could generally be chosen lower compared to the CL-TCM converter, because of the reduced switch capacitance that needs to be charged to allow for ZVS.

As expected, at maximum output power, the peak inductor current in CL-TCM mode is similar to the TCM operation and the operating frequency measurement in **Fig. 8(b)** confirms the constant switching frequency of the CL-TCM converter at a fixed input and output voltage. As discussed in **Section IV**, this comes at the expense of a higher peak and RMS inductor current at low output power when compared to the TCM operation. The switching frequency of the TCM converter varies by a factor of 6.4, whereas the operating frequency of the CL-TCM converter varies only by factor of 2.7 and is in good agreement with the result obtained with equation (18). As predicted by the equations (14)-(17), the clamping-time interval T_{cl} shown in **Fig. 8(c)** approaches zero at the nominal output power of 30 W which corresponds to the TCM operation.

The input and output power of the converter was calculated based on the measurement of the terminal voltage and current using Agilent 34410A multimeter. The power loss and the achieved DC-DC efficiency of the CL-TCM and TCM converter is shown in **Fig. 9**. The constant power loss caused by the current and voltage measurement circuit of the converter is measured separately and amounts to 37.2 mW. The constant power loss caused by the DSP/FPGA board is 994 mW, where the DSP accounts approximately for 87 % of the losses. These constant power losses can be reduced significantly (down to 200-300 mW), using a more suitable controller and are therefore not included in the power loss and efficiency measurement. As indicated in **Fig. 9(b)** and **(d)**, a constant power loss of up to 300 mW could be accepted for the control circuit in order to achieve a minimum efficiency of 90 % in the entire range of operation.

The CL-TCM and TCM converter show almost the same efficiency at minimum and maximum output power. From the increased switching frequency of the TCM converter at low output power, it could be expected that the power losses are higher compared to the CL-TCM operation. The measurements show that this is not the case because as the switching frequency of the TCM converter increases, the RMS inductor current decreases linearly with decreasing output power, which compensates for the increased AC losses in the inductor core and winding.

In order compare the degradation of the performance with increasing power density of the converter, the switching frequency variation and the DC-DC efficiency was measured for both converter operating modes with the inductor shown in **Fig. 6(c)**. **Fig. 10(a)** depicts the measured switching frequency variation. The operating frequency of the TCM converter varies from 171 kHz to 1.02 MHz by a factor of 5.96. The CL-TCM converter instead has a maximum switching frequency of 400 kHz and the frequency varies only by a factor of 2.6.

The result of the efficiency measurement is shown in **Fig. 10(b)** for both prototype inductors. Again, the constant power loss of the DSP/FPGA board is not included in this measurement. Additionally, the negative peak inductor current was increased to -0.75 A in order to achieve ZVS within the 100 ns total dead-time with the reduced inductance value. Again, the two converter show very similar efficiencies. However, for the worst case operating point which is at an output voltage of 50 V and an output power of 30 W, the efficiency of the CL-TCM converter is decreasing with a steeper slope compared to the TCM operation as the power density of the inductor is increased. As explained in **Section IV**, the CL-TCM emulates TCM operation at maximum output power. Hence, the clamping time intervals are reduced to 35 ns but are not completely omitted for the measurement in order to maintain the same modulation scheme for the entire range of operation, which is the main reason why the measured efficiency of the CL-TCM converter is lower than the efficiency of the TCM converter at maximum output power as it is shown in **Fig. 10(b)**.

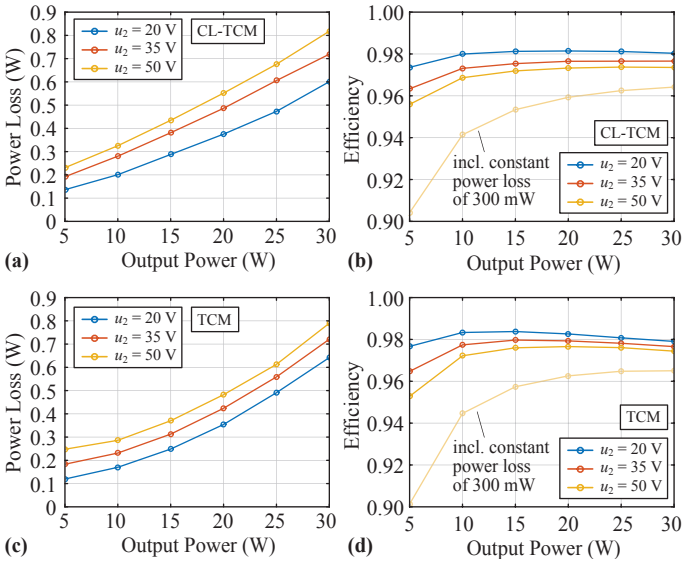


Figure 9: (a)-(b) Measured power loss and DC-DC efficiency of the CL-TCM converter at variable output power and different output voltages. (c)-(d) Measured converter performance with TCM operation. Note that these measurements do not include the constant power loss of the DSP/FPGA board.

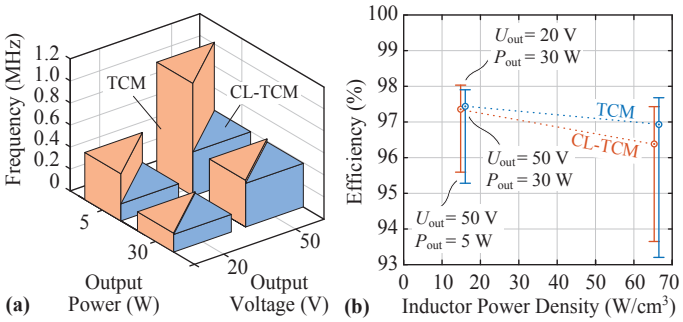


Figure 10: (a) Measured switching frequency variation of the CL-TCM and TCM converter with the inductor shown in **Fig. 6(c)**. (b) Measured DC-DC efficiency of the CL-TCM and TCM converter with respect to the power density of the two inductors shown in **Fig. 6(b)** and **(c)**. Note that the efficiency does not include the power losses of the DSP/FPGA board.

VI. Conclusions

In this paper the CL-TCM converter is explained in detail and a ZVS modulation scheme is provided that allows for soft-switching of all switches. In addition, the conditions for ZVS operation are identified and a control scheme is proposed that allows for a significant reduction of the switching frequency variation, while maintaining a low RMS inductor current. The effort for the control of the TCM and CL-TCM converter is similar and the additional clamp-switch and boot-strap gate drive do not constitute a significant increase of circuit complexity in the case of a low voltage application. The reduced switching frequency variation of the CL-TCM converter helps to relax the requirements for the control circuit and for the application at hand where a high power conversion efficiency is desired, the CL-TCM and TCM converter achieve both similar performance at a lower power density of the inductor. However, for applications where a very high power density is needed, the TCM converter shows a superior performance in terms of efficiency and power density compared to the CL-TCM converter, mainly because of the reduced amount of switches needed for TCM operation. On the other hand, for example in applications where Electromagnetic Interference (EMI) must be reduced, the CL-TCM converter simplifies the filter design due to the decreased switching frequency variation.

Future work will also include a comparison of the CL-TCM and TCM converter to the conventional hard-switched boost converter. Due to the significant improvements in modern wide-band-gap semiconductor devices, the switching losses in a hard-switched converter are not the main decisive factor which determines the most suitable converter topology or modulation scheme and in low power applications, the constant power loss generated by the control circuit has a significant impact on the outcome of the comparison between soft-switched and hard-switched converters. Therefore a careful, application specific analysis of the converter topologies and modulation schemes is mandatory in order to reveal the advantages and limitations of each topology.

Acknowledgment

The authors gratefully acknowledge the financial support by the Baugarten foundation. This work is part of the Zurich Heart project under the umbrella of "University Medicine Zurich/Hochschulmedizin Zürich". Further thanks goes to Andrés Cao for the design of the hardware prototype in the course of his semester project.

References

[1] O. Knecht, R. Bosshard, and J. W. Kolar, "High-efficiency transcutaneous energy transfer for implantable mechanical heart support systems," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6221–6236, 2015.

[2] T. Pirbodaghi, C. Cotter, and K. Bourque, "Power consumption of rotary blood pumps: pulsatile versus constant-speed mode," *Artif. Organs*, vol. 38, no. 12, pp. 1024–1028, 2014.

[3] M. S. Slaughter and T. J. Myers, "Transcutaneous energy transmission for mechanical circulatory support systems: history, current status, and future prospects," *J. Card. Surg.*, vol. 25, no. 4, pp. 484–489, 2010.

[4] D. M. Sable, F. C. Lee, and B. H. Cho, "A zero-voltage-switching bidirectional battery charger/discharger for the NASA EOS satellite," in *Proc. 17th IEEE App. Power Electron. Conf. and Expo. (APEC)*, 1992, pp. 614–621.

[5] J. S. Lai, B. York, A. Koran, Y. Cho, B. Whitaker, and H. Miwa, "High-efficiency design of multiphase synchronous mode soft-switching converter for wide input and load range," in *Proc. Int. Power Electron. Conf. (IPEC)*, 2010, pp. 1849–1855.

[6] C. P. Henze, H. C. Martin, and D. W. Parsley, "Zero-voltage switching in high frequency power converters using pulse width modulation," in *Proc. 3rd IEEE App. Power Electron. Conf. and Expo. (APEC)*, 1992, pp. 33–40.

[7] S. G. Yoon, J. M. Lee, J. H. Park, I. K. Lee, and B. H. Cho, "A frequency controlled bidirectional synchronous rectifier converter for HEV using super-capacitor," in *Proc. 35th IEEE Annual Power Electron. Specialists Conf. (PESC)*, 2004, pp. 135–140.

[8] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, 2014.

[9] C. R. Swartz, "High performance ZVS buck regulator removes barriers to increased power throughput in wide input range point-of-load applications," 2016, Jan. 4. [Online]. Available: http://www.vicorpower.com/documents/whitepapers/Picor/wp_HighPerfomanceZVS.pdf

[10] L. Meier, "Design, Optimization and Implementation of a Bidirectional 1-3kW DC/DC Converter," Master's thesis, Dept. Elect. Eng., Swiss Federal Inst. Technol. Zurich (ETHZ), 2014.

[11] D. Bortis and J. W. Kolar, "DC/DC Konverter und Verfahren zur Steuerung eines weich schaltenden bidirektionalen DC/DC Konverters (in German)," Swiss Patent Application CH 00120/15, Jan. 3, 2015.

[12] F. Krismer, "Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies," Ph.D. dissertation, Dept. Elect. Eng., Swiss Federal Inst. Technol. Zurich (ETHZ), Zurich, Switzerland, 2010.