New Lossless Turn-On and Turn-Off (Snubber) Networks for Inverters, Including Circuits for Blocking Voltage Limitation

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Abstract—**Transistorized pulsewidth modulated (PWM) inverters require careful dimensioning of turn-on and turn-off circuits in order to minimize switching loss in the power transistors. New lossless circuits are described. In particular the turn-off circuits show a highly reduced part count compared to circuits known from the literature. The turn-on circuits apply energy recovery. Furthermore, due to a special circuit the voltage across the power transistor is strictly limited. This is important especially due to the usually low voltage blocking capability of high-current power transistors.**

I. Introduction

IN GENERAL, turn-on and turn-off networks (snubbers) are circuits used for the reduction of switching losses of power devices in power electronic circuits. These networks are situated in series or in parallel to the power devices, respectively. The power devices taken into account in this paper are mainly power transistors and gate turn-offs (GTO's). One major purpose of using such snubbers is to keep the power device operating within its safe operating area (SOAR).

Two different types of snubbers can be defined: dissipative and nondissipative (lossless) types. While the term nondissipative is based on an idealization, the underlying basic difference can be shown as follows.

1) In dissipative snubbers the whole energy stored in this network is converted into heat [1], [2], [10]. This type obviously is not qualified for high switching frequencies and/or high switched power levels.

2) Nondissipative snubber networks should be called snubbers with low losses or, better, snubbers without fundamental losses. Losses are only caused by nonideal device properties, such as conduction and switching losses of the switching devices contained in the snubber networks [2]. It is certainly possible, as frequently realized, to combine dissipative turn-on networks with nondissipative turn-off networks and vice versa [1], [3].

Since the losses of dissipative snubbers reduce the efficiency of power electronic circuits to a great extent, especially for higher switching frequencies, nondissipative turn-on and turn-off snubbers are used here. One other important point is the part count of the additional power devices required by the snubbers. The circuits for inverters applied so far use snubbers developed for one switching device (as applied in a chopper). This means multiple application of the same snubber circuits—four times for one-phase bridge inverters and six times for three-phase inverters. This relatively high part count in many cases is detrimental to practical application due to the additional cost involved. Therefore, a circuit with a reduced part count for inverter application has been developed here.

A final point to be observed is the maximum voltage across the switching device. Due to the rather limited voltage blocking capability, especially of high-current power transistors, this parameter is of paramount practical and economic importance. A circuit has been developed here which allows us to limit this voltage to a given amount.

II. Requirements for Ideal Turn-On and Turn-Off Snubbers

The basic requirements stated in the introduction lead to the following points, which should be fulfilled by ideal snubber circuits:

1) no fundamental losses;
2) part count as low as possible;
3) no additional discharging (and charging) currents caused by the snubbers should flow through the power devices; (This is especially important for high operating frequencies, where high current peaks have to be admitted for fast charging and discharging of the snubber capacitors. This would mean that the power devices would have to be oversized.)
4) no additional switching devices;
5) no additional voltage and/or current sources for the snubbers should be required; (This is important for high switching power levels.)
6) limit the switching strain (voltage and current levels) on snubber circuit devices to the order of magnitude of the (main) switching devices;
7) high reliability and safety of operation;
8) the functioning shall be independent of the various operating conditions (such as load current, switching frequency, etc.).

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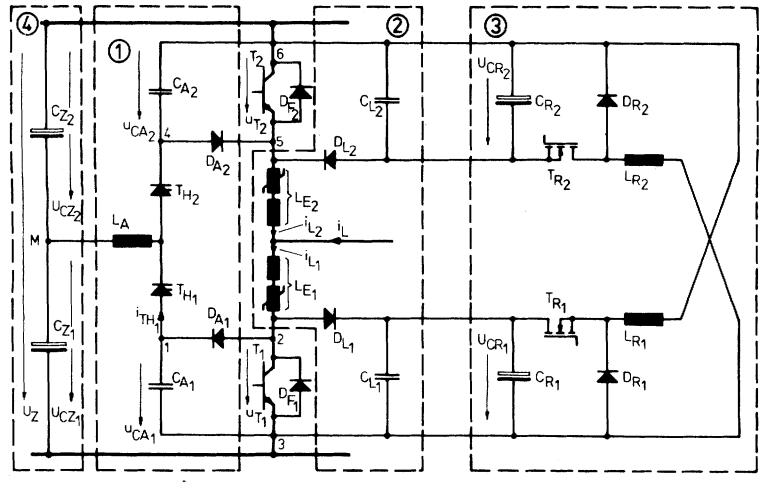

Fig. 1. Pole changer (one phase leg of inverter). Block 1) turn-off snubber (network). 2) turn-on snubber. 3) blocking voltage limitation circuit for power switching devices (here, transistors T_1 and T_2) necessary only once for three phase inverters. 4) capacitors for providing dc voltage link, which form capacitive center of inverter supply voltage. This center comes automatically for voltage applications above 450 V as here because this is beyond the usual limits of industrial electrolytic capacitors today. Then capacitors must be used in series.

Obviously, not all of the points mentioned can be realized in a practical and economical way. In particular, simultaneous fulfilment of 3) and 4) seems to be impossible as will be explained later. If 4) cannot be fulfilled, 7) has to be observed very carefully, e.g., due to the additional control circuits necessary in this case.

III. Realization

A. Inverter Structure

In the following the approach used to come very close to the requirements stated in Section II shall be described. The power circuit is shown in Fig. 1. The circuit used for measurements is a three-phase transistor inverter with dc voltage link (440 V $\pm$ 10 percent). The maximum switching frequency is $f_{p\max} = 50$ kHz, the maximum load current is $i_{L\max} = 180$ A. For the power switching devices, two Darlington configurations are used in parallel where each Darlington consists of three stages: first stage—power MOSFET BUZ 88 A, Siemens; second and third stages—high power Darlington device with a separate fast recovery flyback diode D67FP7, General Electric.

B. Turn-Off Snubber

Turn-off snubbers are circuits lying in parallel to the power switching device (T, e.g., T_1, T_2 in Fig. 1) whose major element is a capacitor. The load current commutates into the turn-off snubber at the turn-off time of T. The dimensioning of the snubber has to be such that the load line always remains within the SOAR (especially within the reverse bias (RB), SOAR for negative voltage at the base). Furthermore, the turn-off snubbers are used to reduce the switching loss per switching cycle by shifting the load line toward smaller switching losses in the active region. This makes such snubbers mandatory above a certain operating frequency.

The main problem of the turn-off snubbers lies in proper discharging of the turn-off capacitor. The following possibilities exist:

a) discharging via a resistance R and the power device T in the conventional RCD network; (The energy stored in the capacitor C_A is dissipated into heat in R and in T, the discharging current is added to the load current.)
b) discharging, e.g., via resonant (ringing) circuits with energy feedback into the dc voltage link. So far this method has employed discharging current also through the power device T [5]. In some operating conditions of inverters this method can lead to an unwanted discharge of the capacitor C_A via the load (when the diode D_F, lying antiparallel to T, is conducting).

(To understand this let us assume that $i_L > 0$. Then T_1 and D_{F_2} conduct i_L alternatively. If conventional RCD snubber networks are used—or any snubber network where at least part of discharging the C_{A_i} is performed via the transistor T_i—C_{A_2} would be discharged when D_{F_2} conducts i_L. C_{A_2} would then be recharged when T_1 conducts again. This means that C_{A_2} is charged and discharged unnecessarily each time the other transistor T_1 is turned on and off. During recharging the transistor current would be the sum of the load current and the recharging current. Inductances in series to the transistors would be necessary to define the peak currents during the recharging interval. The highest transistor current would be the (maximum) load current plus the recharging peak current. In the new circuit described here the recharging peak current is only added to the load current i_L as long a $|i_L| \leq i_{L_\epsilon}$. For $|i_L| > i_{L_\epsilon}$ no recharging via the opposite transistor is necessary, as explained later.) This effect has been avoided in applications by inserting a diode D_s in series to T. However, on the one hand, D_s has to carry the load current, which leads to considerable additional losses, and on the other hand this method is only applicable where T and D_F

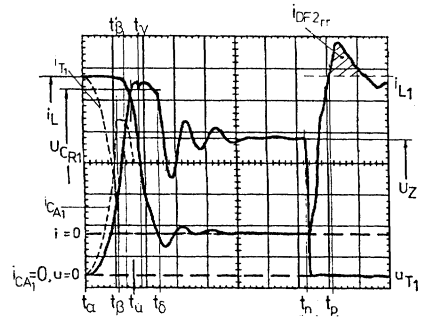

Fig. 2. Turn-on and turn-off behavior of T_1 using snubbers; i_L = 100 A. Scale: i_L, i_{L_1} = 20 A/div (i.e., between full lines); u_{T_1} = 100 V/div; time (horizontal axis) = 2 μs/div. For meaning of electrical variables see Fig. 1 and the Appendix.

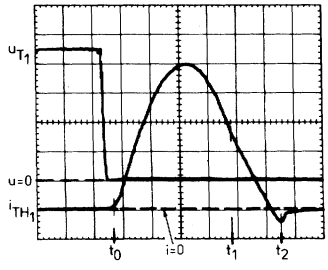

Fig. 3. Voltage across power transistor T_1 and current through T_{H_1} to illustrate discharge of turn-off snubber capacitor C_{A_1}. Scale as in Fig. 2, with time = 1 μs/div. Here, $u_{C_{A_1}}(t = t_0) = U_{C_{R_1}} > 2U_{C_{Z_1}}$.

are separate devices. The latter condition is against today's trend to higher integration. Another method to overcome unwanted discharging is to insert a switching device into the discharging circuit.

Since in all the methods proposed so far the discharging current is added to the load current in T, the new method introduced here applies a discharging method for C_A via an additional switching device. The discharging current does not flow through T.

The function of circuit block 1 in Fig. 1 is as follows. When t_1 is turned off (assuming $i_L > 0$), C_{A_1} is charged via D_{A_1}; i_L commutates to D_{F_2} starting when $u_{C_{A_1}} > U_Z$. The voltage across T_1 is always limited to U_{CR1} (see Fig. 2) by a circuit to be described later. From Fig. 3 it can be seen that, at turn-on of T_1, C_{A_1} is discharged via L_A into M by turning on thyristor T_{H_1}. Thereby the snubber is brought back into its initial status. For M the center of the capacitive voltage divider, built up by the electrolytic capacitors used for providing the inverter dc voltage link, can be applied. Fig. 3 shows that for $u_{CA1} = U_{CR1} > 2U_{CZ1}$ the current i_{TH_1} consists of two different parts. One part (between t_0 and t_1) is determined by the circuit $C_{A_1} - T_{H_1} - L_A - C_{Z_1}$, therefore resulting in a sinusoidal current, $U_{CZ1} \approx$ constant. The second part (for t_1, t_2) is linear because there i_{TH_1} is determined by the circuit $L_A - C_{Z_1} - T_1/D_{F_1} - D_{A_1} - T_{H_1}$ where $u_{CA1} = OV$ for this period (t_1, t_2), $U_{CZ1} \approx$ constant. (Whether and where T_1 or D_{F_1} conducts depends on the size of i_L.)

C_{A_2} is also discharged into M. For asymmetries caused by device tolerances, unequal voltages $U_{CR_{1,2}}$, and unequal discharging rates of C_{A_1} and C_{A_2} unequal, the voltage level

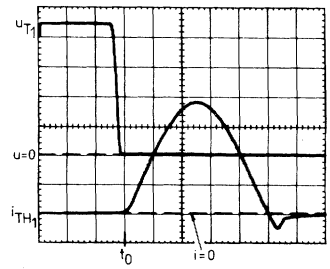

Fig. 4. As for Fig. 3, but $u_{C_{A_1}}(t = t_0) = 2U_{Z_{C_1}}$.

of M is being shifted. However, its final level is stable because the current amplitudes of $i_{TH1,2}$ behave contrary to U_{CZ1}. For example, for n times discharging of C_{A_1} for one discharging C_{A_2} the stable voltage level is $U_{CZ1} = n/(n + 1) \cdot U_Z$, whose relationship can easily be derived by viewing the equilibrium of charges. For given switching frequency, the dynamics of the voltage level change of M is dependent on the ratio of the capacitance values of $C_{Z_{1,2}}$ and $C_{A_{1,2}}$. For discharges of C_{A_1} that are always complete, $u_{C_{A_1}} = U_{C_{R_1}} > 2U_{CZ1}$, has to be guaranteed. In the limit, i.e., for $U_{C_{R_1}} = 2U_{CZ1}$, $i_{T_{H_1}}$ is quite sinusoidal (Fig. 4).

A further problem with all low-loss turn-off snubbers lies in the fact that, during transistor (in general, the power switching device) turn-off, the capacitor has to be charged to a minimum voltage level. This is necessary in order to make possible its complete discharging in one cycle. For given maximum pulse frequency and given snubber capacitor value, the load current value i_{L_ϵ} can be obtained, for which after turn-off of the switch the load current commutates completely into the corresponding freewheeling branch within the minimum turn-off time. This automatically is connected with charging of the snubber capacitor C_{A_i}, belonging to the T_i being turned off up to $U_{C_{R_1}}$.

For $i_L < i_{L_\epsilon}$, e.g., after turn-off of T_1 the opposite device T_2 must be turned on after a time delay to avoid shorting the dc voltage link. It is necessary to turn on T_2 for continuation of the charging of C_{A_1} via T_2, L_{E_1}, and L_{E_2}. Turning on T_2 requires previous discharging of C_{A_2}, here via T_{H_2} in order to provide the turn-off snubber action, as required in most cases, i.e., where $i_{L_2} > 0$, for the following turn-off of T_2. When after the turn-off of T_2 subsequently T_1 is turned on again, T_1 conducts the sum of load current and charging current for C_{A_2} (Fig. 5). As mentioned, this is only the case for very small load currents, $i_L < i_{L_\epsilon}$.

The deviation of the current wave from a sine wave is caused by saturating reactors in the inverter leg whose purpose is described later. The voltage form of u_{t_2} from t_d on essentially corresponds to the voltage form occurring at the turn-off of $T_{1,2}$ (see Fig. 2). Fig. 6 shows the conditions for load current $\approx$ zero. As shown in Fig. 5 the recharging current of C_{A_2} is added to the load current that is commutated from D_{F_2} to T_1. Then T_1 has to carry both the load and the recharging current. As indicated for $i_L > i_{L_\epsilon}$ no additional charging is necessary. Therefore, for such i_L the opposite transistor is not turned on, and its associate turn-off snubber is not being discharged. By

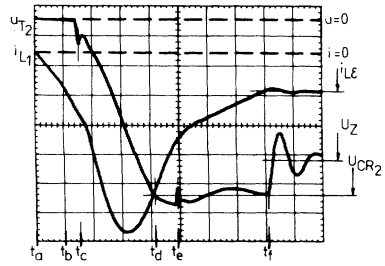

Fig. 5. Recharging of C_{A_2} via $L_{E_{1,2}}$ after turning on T_1 and previous conduction of D_{F_2} for $0 < i_L < i_{L_\epsilon}$. $i_L = 25$ A, $U_{C_{R_2}} = 580$ V, $U_Z = 440$ V. Scale as in Fig. 3. t_a: turn-on of T_1 (L_{E_1} not in saturation, L_{E_2} in saturation). t_b: L_{E_1} going into saturation. t_c: D_{F_2} ceases to conduct, current commutates into C_{A_2}, D_{A_2}. Voltage spike is caused by lead inductances in circuits 4, 5, 6. t_d: $u_{C_{A_2}}$ reaches $U_{C_{R_2}}$, which means that condition for subsequent complete discharging of C_{A_2} (in next cycle) is fulfilled. Refer to the text. t_e: D_{A_2} ceases to conduct; voltage spike is caused by sudden end of reverse current in D_{A_2}. t_e–t_f: demagnetization of L_{E_1} and L_{E_2} by $U_{C_{R_2}} - U_Z$ (lying directly across L_{E_1} and L_{E_2} in series). t_f: L_{E_1} and L_{E_2} are demagnetized; u_{T_2} approaches U_Z via damped oscillation which is caused by RC snubber attached to D_{F_2}; additional snubbers (not shown in Fig. 1) are necessary to reduce sufficiently rate of voltage rises across T_2 at turn-off of D_{F_2}. Further details are given in the Appendix.

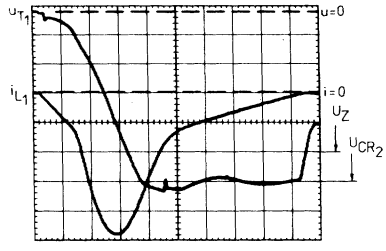

Fig. 6. As for Fig. 5, but $i_L \approx 0$ (no-load condition).

proper dimensioning of $L_{E_{1,2}}$ it becomes possible to keep the sum of i_{L_ϵ} and the peak of the charging current below $i_{L\max} + i_{DFL\max}$. There, $i_{L\max}$ · · · maximum load current, $i_{DFL\max}$ · · · peak reverse current through D_F for $i_{L\max}$ (see Fig. 2). A further aspect for dimensioning of $L_{E_{1,2}}$ is the recharging time period t_{ch} given by $C_{A_{1,2}}$, i_{L_ϵ}, and $L_{E_{1,2}}$. This time period must be coordinated with the maximum pulse frequency. t_{ch} extends at least from t_a to t_f. With these facts the dimensioning of the transistors with respect to the current is practically given by the load current.

Guidelines for dimensioning of $L_{A_{1,2}}$ and of the thyristors $T_{H_{1,2}}$ are given in the following. For given turn-off capacitances $C_{A_{1,2}}$ and the minimum pulse duration, the value of L_A is fixed; the linear part of the discharging current $i_{T_{H_{1,2}}}$ and the quenching time of the thyristors $T_{H_{1,2}}$ have to be taken into account. The discharge current peaks (Figs. 4, 5) may reach high levels where high maximum pulse frequencies are to be handled.

C. Turn-On Snubber

1) General Concepts: In general, turn-on snubbers are based on an inductance connected in series with the transistor T (power switching device). Thereby at turn-on of T a load line shall be maintained within the forward bias SOAR (FBSOAR). In particular, the snubbers reduce the turn-on switching loss in T. If one considers circuits with no snubbers at all but certainly load lines within the SOAR, in general the turn-off switching losses will dominate.

The second task of the turn-on snubber is to reduce the reverse current peak through D_F. The D_F to be considered here is the one lying antiparallel to the opposite T. This D_F has been carrying the load current before turning on the T now to be considered for turn-on. The reverse current peak through D_F is being added to the load current in T being turned on. It is evident that such diodes with large reverse recovered charge and resulting high reverse recovery current peak make oversizing of the transistor T necessary.

Here the problem of handling the energy originating from the snubber action is to be treated in the same way as that for the turn-off snubber. This energy is stored in the snubber. Basically, there are two methods for handling this energy, but both methods are associated with a blocking voltage increase across the transistors:

a) dissipation of the magnetic energy into heat in resistors, Zener diodes, etc.;
b) basically lossless energy feedback into the dc voltage link (or into another additional dc voltage source [2]).

Only method b) is of interest here. Again, two approaches can be given.

b1) Energy feedback via power converters working in turn as flyback and forward converters into the dc voltage link [4]: The problems encountered here are high blocking voltages across the transistors, across the diodes (lying on the secondary [4]), or across both transistors and diodes. In practical applications this problem is increased by the transformer stray inductances, which cause further increase of the transistor blocking voltages.

b2) Limitation of the blocking voltage across the transistor (in general, the power switching device) to a defined value larger than the dc link voltage value: The magnetization energy is transferred into the limitation circuit, consisting of energy storage with a possibility of energy feedback into the dc voltage link.

Method b2) is realized here. The energy storage mentioned for any n-phase bridge application is required only twice—once for the upper half bridge, once for the lower half. This means a substantial reduction of the part count as compared to already known systems, e.g., for three-phase applications. The energy storage is realized as a capacitor whose voltage is kept constant by a step-down converter feeding into the dc voltage link (block 3 in Fig. 1). Other methods for energy feedback are conceivable.

2) Energy Relationships of Block 2 (Fig. 1): Block 2 is only operational with block 3. The initial conditions shall be given by $i_L > 0$, T_1 turned off; i_L is flowing through D_{F_2}. At turn-on of T_1 the sum of the load current i_L and the reverse recovery current of D_{F_2} will be taken over by T_1 (Fig. 7). From t_x on D_{F_2} ceases to conduct. If the reverse recovery current is equal to its maximum $i_{RRD2\max}$, then during the subsequent complete demagneti-

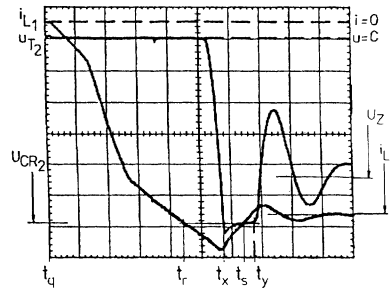

Fig. 7. Current commutation from D_{F_2} to T_1. Nonlinear current behavior is caused by saturating inductances $L_{E_1} \approx L_{E_2}$; small differences between L_{E_1} and L_{E_2} are caused by the production process. $U_{CR} = 580$ V, $U_Z = 440$ V, $i_L = 125$ A. Scale as in Fig. 2, with time = 500 ns/div. Further details are given in the Appendix.

zation of L_{E_2} and partial demagnetization of L_{E_1} approximately the following amount of energy is delivered into C_{R_1} and C_{L_1} via the counter voltage $U_{CR_2} - U_Z$

$$2\frac{1}{2}L_E \cdot i^2_{RRD2\max} \cdot \frac{U_{CR2}}{U_{CR_2} - U_Z}.$$

For this, one has to keep in mind that the load current continues to flow approximately unchanged; $L_{E_1} = L_{E_2} = L_E$ are assumed to be of the nonsaturating type. This energy amount is dependent on the ratio U_{CR2}/U_Z and is much higher than the energy stored in L_{E_1} and L_{E_2} due to $i_{RRD2\max}$. This is because of the fact that due to the direction of the current during the whole time of current flow in L_{E_2} energy is transferred from the dc supply into the voltage limiting circuits (see Fig. 7, interval $[t_x, t_y]$).

C_{L_2} is a small capacitor with low inductance lying parallel to C_{R_2}. C_{L_2} keeps transistor blocking voltage spikes small (see t_x in Fig. 7), which are caused by lead inductances between points 5 in Fig. 1 and C_{R_2}. Remember that C_{R_2} is common to all power switches of the upper half bridge. Other devices, such as C_{L_2} (or C_{L_i}) and D_{L_2} (or D_{L_i}), are needed for each power switching device separately.

At turn-off of T_1, i_{L_1} (starting at t_u in Fig. 2) flows through D_{L_1}, C_{L_1}, and C_{R_1} until the current in L_{E_1} goes to zero and L_{E_2} has taken over the entire load current. Thereby the energy content of C_{L_1} and C_{R_1} is increased by

$$2 \cdot \left|\frac{1}{2}L_E \cdot i^2_{L_1}\right| \cdot \frac{U_{CR1}}{U_{CR1} - U_Z}$$

$$= \frac{U_{CR1}}{U_{CR1} - U_Z} \cdot \left[L_E \cdot i^2_{L_1} - \frac{C_A(U_{CR1} - U_Z)^2}{2}\right].$$

L_E again is assumed to be of the nonsaturating type.

During the recharging oscillations (discussed in Section III-B), energy is transferred from, or via, respectively, L_{E_1} and L_{E_2} into the voltage limitation circuit in time interval $[t_d, t_f]$. As can be deducted from the graphs in Figs. 5 and 6 this energy amount is approximately independent of the load current. The circuit was designed for relatively high pulse frequency; this leads to the fact that the mentioned energy amount is in the same order of magnitude as the previously given energy amount, which basically is directly dependent on the load current, for $i_L = i_{L\max}$. The contribution due to the reverse recovery current peaks of D_{F_1} and D_{F_2} is negligible in the region of high load currents. It can be calculated that for load currents $i_L < i_{L_\epsilon}$ and $i_L \approx i_{L\max}$ the highest amounts of energy are fed into the limiting circuits. The energy also has to be fed back into the dc source (U_Z) to keep $U_{CR1,2}$ constant. The essential part of the energies mentioned is due to the load current.

3) Criteria for the dimensioning of $L_{E1,2}$: The requirements are

a) reduction of the reverse recovery current in the D_{F_i};

b) limitation of the amplitude of the recharging oscillation (described in Section III-B) and thereby determination of the recharging time based upon given $C_{A1,2}$;

c) reduction of the turn-on losses of the power switching devices;

d) considering a) and b), for any given current the energy amount fed into the limiting circuits due to the inductances should be as small as possible, because this energy determines the size of the step-down converter (block 3 in Fig. 1).

Some basic facts for the requirements listed above include the following.

a) Due to the nonlinearity of saturable inductances, the diodes (especially $D_{F_{1,2}}$) have enough time (starting when the current commutating away from the branch containing the diode becomes zero) to "forget the history." In physical terms this means that there is enough time for reduction of the minority carriers in the junction by recombination. Therefore, the reverse recovery current peak is greatly reduced when compared to cases where only air coils are applied.

An additional advantage resulting from the application of saturating reactors is that the *RC* snubbers for $D_{E_{1,2}}$ can be kept smaller [6]. These relatively small additional snubbers (not shown in Fig. 1) turned out to be necessry in practice for limitation of the blocking voltage rate of rise across T_i. Keeping the snubbers small results in reduced snubber losses.

b) The amplitude of the recharging oscillation for saturable inductances is determined by the remaining inductance of $L_{E_{1,2}}$ in the saturated state. Therefore, this value must not be below a specified minimum value. The recharging time (see Fig. 5, time interval $[t_a, t_f]$) for C_{A_2} is substantially increased due to the nonlinearity of saturable inductances if compared with air coils. For both cases approximately the same amplitude of the recharging oscillation is assumed.

c) The turn-on losses are lower for saturable inductances than for air coils. However, they are of minor importance within the overall switching losses if turn-on snubbers are assumed.

d) For a comparison of the energy amounts fed from the saturable and nonsaturable inductances into $C_{R_{1,2}}$ we will assume the same currents (e.g., $i_{L_{1,01}}$ or $i_{L_{1,02}}$ as shown

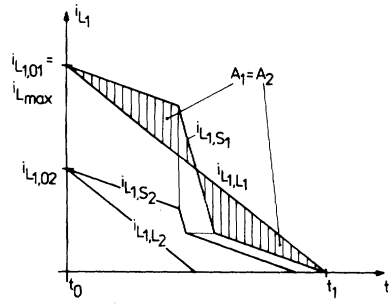

Fig. 8. Simplified behavior of i_{L_1} for load current commutation from T_1 into D_{E_2} (compare with Fig. 2). t_0 in Fig. 8 approximately corresponds with t_u in Fig. 2. $i_{L1S1,2} \cdots L_{E1,2}$, saturable; $i_{L1L1,2} \cdots L_{E1,2}$, nonsaturable.

for two cases in Fig. 8) flowing in the inductances at the beginning of conduction of $D_{L_{1,2}}$.

As starting values, $i_{L_{1,01}}$ and $i_{L_{1,02}}$ shall be given (see Fig. 8). The value of a comparable nonsaturable inductance shall be determined such that the mean rate of current change $i_{L\max}/t_1$ is the same as for the saturable case. The nonsaturable inductance also shall be applicable with respect to points a)–c). A somewhat higher reverse recovery current peak $i_{rrDFi,\max}$ will result due to the less steep slope at t_1. The amount of energy always fed into the limiting circuit is

$$U_{C_{R1}} \cdot \int_{t_0}^{t_1} i_{L_1}\, dt.$$

For $i_{L_{1,01}} = i_{L\max}$, according to the choice of a comparable nonsaturable inductance, we have

$$U_{C_{R1}} \cdot \int_{t_0}^{t_1} i_{L_{1,S1}}\, dt = U_{C_{R1}} \cdot \int_{t_0}^{t_1} i_{L_{1,L1}}\, dt$$

where S means saturable and L is the air coil. For $i_{L_{1,02}} = i_{L\max}/2$, a substantial difference exists in the energy amounts fed into C_{R1} (see Fig. 8)—the voltage is constant, the current time area is much different for both cases. Although this amount does not directly influence the peak power of the step-down converters, their mean power and their losses are affected.

Consideration of d) introduces an optimization problem where the following aspects are essential: the diode turn-off behavior, the maximum inverter pulse frequency, and the recharging current amplitude (discussed in Section III-B).

If, as here, high pulse frequencies are desired, the nonlinear characteristic of $L_{E_{1,2}}$ has to be designed such that little difference exists as compared to the linear characteristic of air coils. Therefore, one can use air coils for $L_{E_{1,2}}$ if one does not want to optimize absolutely the behavior; there will not be substantial differences between the optima gained with a combination of saturable and nonsaturable inductances and the results gained with application of air coils only. For the purpose of reduced material consumption the linear inductances can be most advantageously realized for the upper and lower leg as one coil with center tap.

Lead inductances between dc voltage link capacitors and the inverter can be considered as contributions to the linear part of $L_{E_{1,2}}$ but are only fully equivalent in their function for certain wiring configurations.

This means that separate lead wires have to lead from the dc voltage link capacitor to each pole changer. A common lead to all three pole changers would lead to interferences. If, e.g., two C_{A_i} have to be recharged simultaneously via their respective opposite transistor (Figs. 5, 6, and 13), another ringing frequency would be observed due to paralleling two C_{A_i}. This would change the times shown in Figs. 5 and 6, i.e., the recharging time of the C_{A_i} would be increased by $\sqrt{2}$. This factor becomes $\sqrt{3}$ if all three C_{A_i} are recharged simultaneously. The latter case might happen for no-load conditions.

However, in any case this simplifies the mechanical construction significantly because no buffer capacitors have to be applied immediately at the bridge. Therefore also the problem of oscillations induced by inverter switching is reduced; such oscillations would take place in the ringing circuit built up by the dc voltage link capacitors, the buffer capacitors, and the lead inductances between them [1]. These oscillations in general would be damped very little; due to generally high current amplitudes they would cause a substantial additional current stress on the capacitors. In general the optimization will result in small values for $L_{E_{1,2}}$. Therefore, the rate of current rise will be on the order of magnitude of 100 A/μs in the inverter leg in the case of a bridge short circuit. Turning off even upon "immediate" recognition of a failure would certainly not make possible an operation within the RBSOAR. Keeping the load line in the RBSOAR would usually require waiting for discharging the turn-off capacitor. Also, for energy reasons this capacitor will not usually be dimensioned for handling transistor currents of the order of magnitude given by discharging time multiplied by the rate of current rise. It is likely that the short-circuit current will exceed the transistor surge current before the earliest possible turn-off point of time.

IV. Discussion of the Results

The results obtained will be discussed here by considering the requirements stated in Section II.

1) The requirement of being basically lossless is fulfilled. Only a few published turn-on and turn-off snubbers have met this point so far (e.g., [7], [11]).

2) The part count of the power devices is largely reduced when compared to existing circuits, as in [2] and [7].

3), 4) To guarantee that for high switching frequency the maximum current to be switched by the transistor is not substantially larger than the maximum load current, realization of 4) had to be omitted in favor of 3). In snubber circuits with active switching devices described in the literature so far, despite the introduction of such active devices the discharge of the snubber is via the transistor T. This leads to considerable additional current stress in T for a given turn-off snubber capacitor $C_{A_{1,2}}$ and for a given maximum pulse frequency.

5) This requirement has been met only for the turn-off snubber. The additional voltage level introduced in the turn-on snubber, however, makes possible an exact definition (dimensioning) of the blocking voltage stress on the transistors. This allows a better utilization of the transistor voltage limits. Furthermore, energy feedback into the dc voltage links poses no problems. A similar approach has been followed in [2], but restricted to step-down converters. One must be careful, however; some circuits proposed in the literature for energy feedback provide no net energy feedback into the dc source. Their additional circuits proposed for energy feedback withdraw additional energy from the power source, and only this additional energy is fed back. The net energy withdrawn by the snubbers from the dc source before and after adding the circuits has not changed. The main feature for energy feedback is a switching device such as T_{R1} in Fig. 1 for actively controlling power flow and especially a voltage (as U_{CR1} in Fig. 1) higher than the voltage of that dc source where the energy is fed back in.

6) The fulfillment of this requirement can be readily seen from the circuit functional description. This requirement would not be met by using the turn-on snubber of, e.g., [4]; there relatively high voltages result across the diode on the secondary of the transformer used for energy feedback of the turn-on inductance.

7) This problem is common to all snubber circuits whose function is based on switching devices, including their control circuits. However, an inclusion of a function control for the networks into the safety concept of the system is easily possible.

8) This requirement is certainly fulfilled. The operation of the snubbers is not connected to a certain switching frequency as would be the case if the methods of, e.g., [8] or [9] were applied.

V. Conclusion

This paper shows that under consideration of the special inverter structure low-loss snubbers (stress-relieving networks) can be designed showing low complexity. The complexity is substantially lower as compared to arrangements where snubbers developed for step-down converters are used for bridge type inverters. The approach followed here also leads to a largely reduced part count, especially when the polyphase inverter structure is taken into account. The feedback of the energy stored in the snubbers into the dc voltage link poses no problems.

The discharge of the turn-off snubbers is controlled here by special circuits dependent on the direction and amount of the load current. This discharge is basically lossless; it does not operate via the power switching devices (transistors $T_i = T_{1,2}$ in Fig. 1) and therefore imposes no additional current stress on the T_i. Inverters built up with such stress-relieved power switching devices make it possible to control the oscillating currents caused by the snubbers in the inverter legs such that the maximum transistor current is only determined by the load. The exact transistor blocking voltage limitation in the system is very important in view of the limited voltage blocking capability of high-power transistors. Furthermore, the mechanical construction is simplified.

For GTO's the problem of stress relief at turn-off is practically the same. One significant limitation for the application range of GTO's, especially for higher switching frequencies, is given by the losses in the conventional RCD snubbers used today. It seems to be advisable, therefore, to investigate the applicability to GTO's of the snubber circuits proposed here since there are no basic differences with respect to replacing RCD snubbers by low-loss snubbers.

Appendix
Further Circuit Details and Detailed Explanation of Current and Voltage Behavior

Here a detailed description of the function of the circuit shown in Fig. 1 is given. For this purpose, in Figs. 2, 5, and 7, several distinct time intervals are considered. See also Figs. 9–14. Furthermore, a detailed analysis requires consideration of local snubbers and of stray inductances. The local snubbers are used for limiting the voltage peaks caused by stray inductances and by switching (turn-off) of the diodes. Although there is no absolute theoretical necessity for their application, their use allows application of lower voltage devices. Furthermore, electromagnetic influences (EMI) are reduced. The snubbers usually consist of relatively small capacitors and resistors, small in both size and value. They are mounted as close as possible to the switching devices. They do not have to be considered for the general functional description of the circuit; they are only necessary for explanation of the various oscillations taking place. Although some of these oscillations are not really characteristic for circuit operation in general, the explanations would not be complete without proper consideration.

We now turn to the behavior in each time interval shown in Figs. 2, 5 and 7; see Fig. 9.

$[t_\alpha, t_\beta]$: In t_α (where T_1 starts to turn off), current $i_{C_{A1}}$ starts to charge up C_{A1} according to

$$i_{C_{A1}} = C_{A1} \cdot \frac{du_{C_{A1}}}{dt} \approx C_{A1} \frac{du_{T1}}{dt}.$$

Also, $i_{T1} = i_{L1} - i_{C_{A1}}$ can be written with $i_{L1} \approx$ constant $= I_L$ in this time interval.

One can say that in a short time interval before reaching U_Z, u_{T1} rises proportional to time ($i_{L1} = i_L \approx$ constant with T_1 almost turned off completely, giving time linear charging of C_{A1}) and then enters an oscillation about U_Z, because then D_{F2} starts to conduct. Then a ringing circuit is formed containing U_Z, D_{F2} (conducting), L_{E2}, L_{E1}, D_{A1} (conducting), and C_{A1}.

$[t_\beta, t_u]$: This time interval starts when i_{T1} becomes zero. Then T_1 is turned off completely, $i_{C_{A1}}$ has reached I_L (note the different zero levels in Fig. 2). We also have $i_{L1} = i_{C_{A1}}$. When, in t'_B, u_{T1} has reached U_Z, current starts to flow

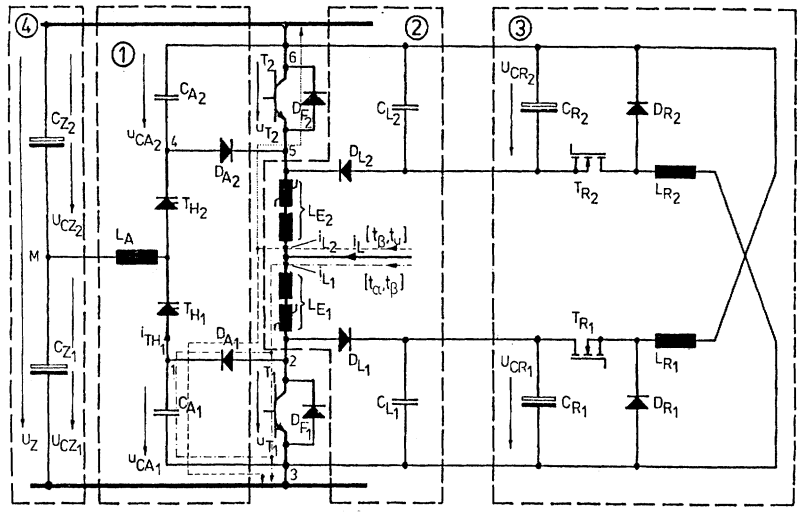

Fig. 9. Current paths for $[t_\alpha, t_u]$.

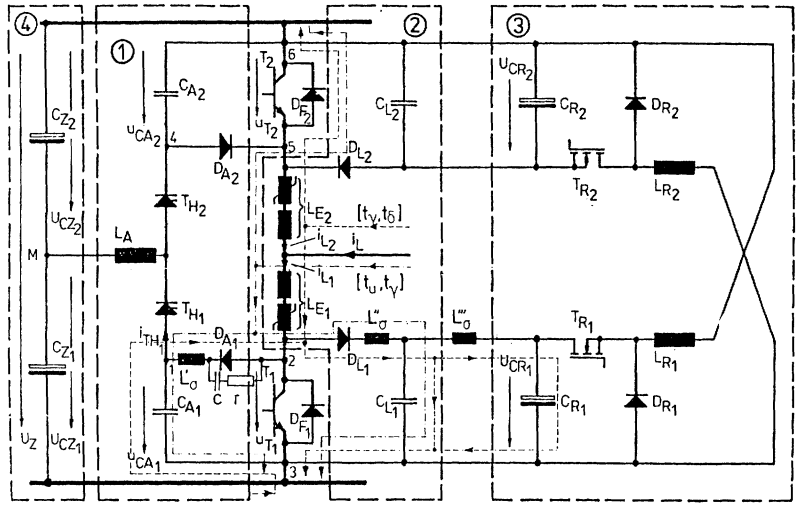

Fig. 10. Current paths for $[t_u, t_\delta]$. In order to explain oscillations taking place in this interval, stray inductances L_σ and local snubbers such as r, c across D_{A_1} have to be taken into account.

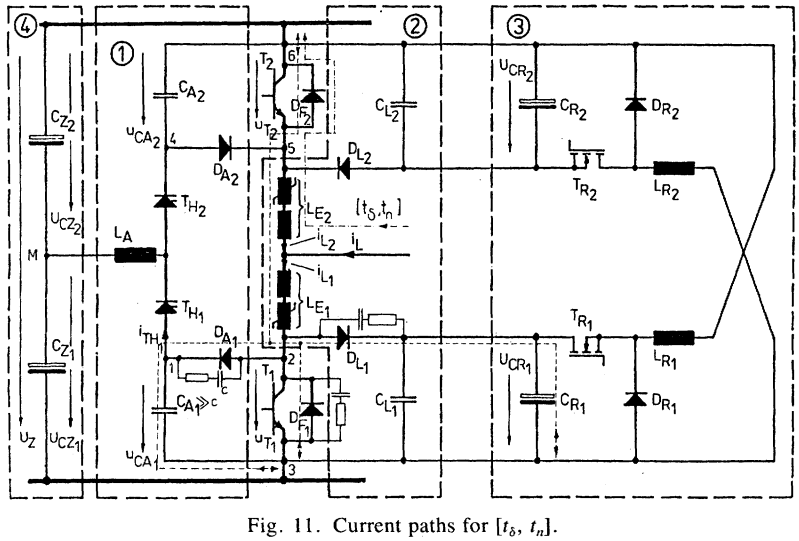

Fig. 11. Current paths for $[t_\delta, t_n]$.

through L_{E_2}. When u_{T_1} reaches $u_{C_{R_1}}$, D_{L_1} will start to conduct. See Fig. 10.

$[t_u, t_\gamma]$: This interval starts when D_{L_1} starts to conduct. i_{L_1} is split up into two components: $i_{C_{A_1}}$ and $i_{D_{L_1}}$. Actually, paralleling C_{A_1} and C_{L_1} lets u_{T_1} rise less steeply after t_u. In this interval $u_{C_{A_1}} > u_{T_1} > u_{C_{L_1}}$. In this interval $i_{C_{A_1}}$ and $i_{D_{A_1}}$ change direction until in about t_γ the reverse recovery current of D_{A_1} ceases suddenly. Then this current commutates to r, resulting in a sudden voltage drop $i_{C_{A_1}} \cdot r = i_R \cdot r$ directed in the opposite direction as compared to

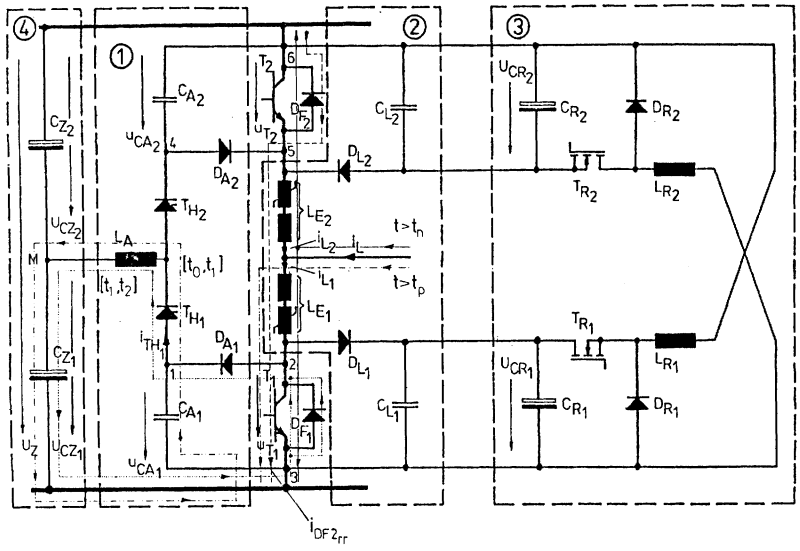

Fig. 12. Current paths for $[t_n, t_p]$ and $t > t_p$.

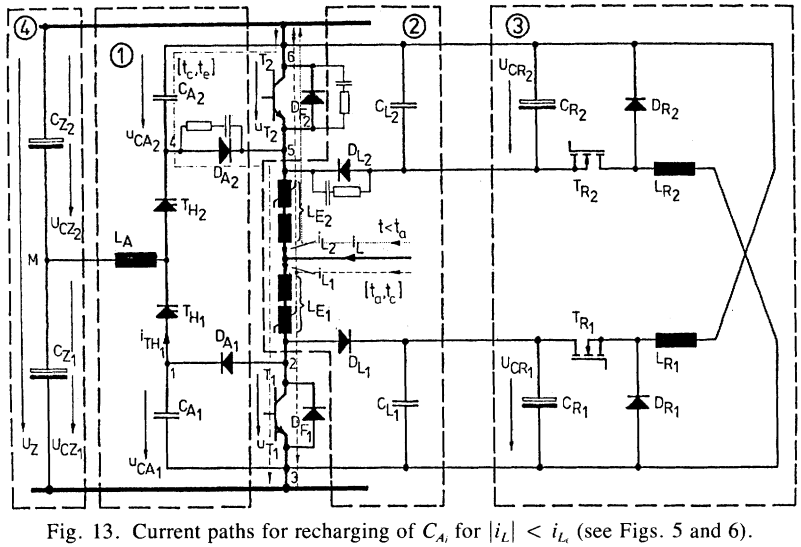

Fig. 13. Current paths for recharging of C_{A_i} for $|i_L| < i_{L_c}$ (see Figs. 5 and 6).

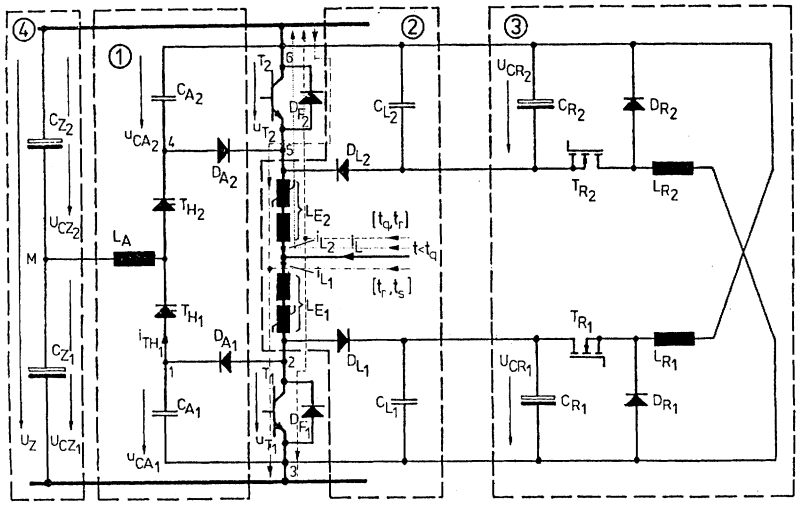

Fig. 14. Current paths corresponding to Fig. 7.

u_{CA_1}. This sudden voltage drop shows up as a spike in u_{T_1} in t_γ.

$[t_\gamma, t_\delta]$: Starting with $u_{T_1} = u_{CR_1}$, the combination of ringing circuits consisting of C_{A_1}, c, L'_σ, L''_σ, L'''_σ, C_{L_1}, and C_{R_1} starts to oscillate. i_R becomes zero in $t_\gamma + \epsilon$, soon after t_γ. The snubber is dimensioned to result in an aperiodic current and voltage, giving a sharp rise of u_{T_1} after t_γ. Also, the voltage division between L'_σ and L''_σ must be observed. Then (after $t_\gamma + \epsilon$) $i_{L_1} \approx i_{D_{L_1}}$; $di_{D_{L_1}}/dt \approx$ constant (see Fig. 2) because u_{CR_1} is controlled to give constant

voltage. The lead length between C_{L_1} and C_{R_1} forms another ringing circuit together with these two capacitances. C_{L_1} is a relatively small impulse-type capacitor; C_{R_1} is relatively large and is the same for the whole inverter. Then

$$u_{T_1} = L''_\sigma \frac{di_{D_{L_1}}}{dt} + u_{C_{L_1}} \quad \text{for} \quad [t_\gamma + \epsilon, t_\delta],$$

with $u_{C_{L_1}}$ oscillating in the ringing circuit C_{L_1}, L'''_σ, C_{R_1} D_{L_1} will block in t_δ (when $i_{L_1} = i_{D_{L_1}} = 0$, the reverse current is neglected, see Fig. 10). Then too, $-i_{L_2} = i_L$. Furthermore, one can notice three different parts in the drop of i_{L_1} in $[t_\beta, t_\delta]$, which at first only correspond to L_{E_1} in saturation, then to L_{E_1} and L_{E_2} in saturation, and finally only to L_{E_2} in saturation. See Fig. 11.

$[t_\delta, t_n]$: At the beginning of this time interval the whole load current is already commutated to D_{F_2}. Now a damped oscillation (see Fig. 2: i_{L_1}, u_{T_1}) between the local snubbers of D_{A_1}, D_{F_1}, and D_{L_1}, the inductances L_{E_1} and L_{E_2}, and the dc-voltage link starts.

The reason for the oscillation is given by the different voltage levels that exist across T_1 at the beginning and the end of interval $[t_\delta, t_n]$. In t_δ, $u_{D_{L_1}} = 0$ because immediately before t_δ the diode D_{L_1} was still conducting charging current for the capacitor C_{L_1}, forming the demagnetization current of L_{E_1}. Demagnetization starts in t'_β, the time when u_{T_1} becomes $> U_Z$, i.e., when a voltage across L_{E_1} against i_{L_1} is being built up. In t_δ this demagnetization is finished ($i_{L_1} = 0$, see Fig. 2). Furthermore, in t_δ we have $u_{T_1} \approx$ 600 V $= U_{C_{R_2}}$ because D_{L_1} was conducting.

In t_n, $u_{T_1} = 440$ V $= U_Z$ because then $i_{L_1} = 0$, $i_{L_2} = -i_L$ = constant and $L_{E_1}\, di_{L_1}/dt = 0$, $L_{E_2}\, di_{L_2}/dt = 0$, $u_{T_2} \approx 0$ (because D_{F_2} conducts the load current). Therefore, D_{A_1} and D_{L_1} are turned off because $u_{C_{A_1}}$ and $u_{C_{L_1}}$ remained at 600 V. See Fig. 12.

$t > t_n$: In t_n, T_1 is turned on (Fig. 2); in t_p, i_{L_1} reaches i_L. The opposite is true for i_{L_2}: $i_{L_2} = -i_L$ in t_n, $i_{L_2} = 0$ in t_p. In $t_0 = t_n$, T_{H_1} is turned on, leading to the discharge of C_{A_1} (Figs. 3, 4). The details of this discharge-oscillation have been described earlier. Fig. 12 shows clearly that D_{F_1} will not conduct $i_{T_{H_1}}$ if i_{L_1} has risen to a value in t_1 larger than $i_{T_{H_1}}$ at this point in time. For $t > t_p$, the load current i_L is flowing only in L_{E_1} until T_1 is turned off again.

Immediately following t_p, L_{E_1} also has to carry the reverse recovery current $i_{D_{F_{2rr}}}$ of the freewheeling diode D_{F_2}. The three different rates of rise of i_{L_1} can be observed in $[t_n, t_p]$ as before. At first L_{E_1} is not in saturation, then L_{E_1} and L_{E_2} are in saturation, and finally, L_{E_2} goes out of saturation.

Recharging of C_{A_i} for $|i_L| \leq i_{L_\epsilon}$: As described earlier, for small i_L ($|i_L| < i_{L_\epsilon}$), special precautions have to be taken because some uncertainty exists as to which transistor (T_1 or T_2) will conduct the load current next; for small i_L a change of the sign of i_L is possible. Therefore, both transistors are turned on alternately. Furthermore, turning on any transistor T_i requires discharging of the corresponding capacitor C_{A_i} in order to make the subsequent snubber action possible at the turn-off of this transistor. During alternating turn-on the snubber capacitors are charged up to the starting value, which is necessary for the subsequent complete discharge. Discharging is performed via T_{H_i} (Figs. 3, 4). Then in t_a (Figs. 5, 13), $u_{C_{A_2}} = 0$. The load current is assumed to flow through D_{F_2} for $t = t_a$ and a certain interval before t_a. In t_a, T_1 is turned on. Now the load current will commutate from D_{F_2} into T_1, forced by U_Z; its rise is limited by L_{E_1}, L_{E_2} as previously discussed in similar cases. When in t_c (Fig. 5) the reverse recovery current in D_{F_2} ceases, C_{A_2} and D_{A_2} start to conduct. C_{A_2} is now charged via D_{A_2}, L_{E_2}, L_{E_1}, and T_1. Without $i_{C_{A_2}}$, one would have noticed a maximum of i_{L_1} in t_c, showing the reverse recovery current peak of D_{F_2} added to i_{L_ϵ}. The further rise of i_{L_1} (Fig. 5) after t_c can now be attributed to $i_{C_{A_2}}$. The basic form of i_{L_1} without $i_{C_{A_2}}$ can be seen in Fig. 2 for $t > t_p$.

As indicated in the caption of Fig. 5, the voltage spike of u_{T_2} in t_c is caused by the lead inductances in the circuit 4, 5, 6 (Fig. 13). For a more exact analysis, the local snubbers (Fig. 13) in this circuit have to be taken into account: when the reverse recovery current in D_{F_2} ceases, it commutates at first into the local snubber across D_{F_2}. This effect is similar to the effect described earlier for the voltage spike across T_1 at time t_γ, which was caused by commutation of the reverse recovery current in D_{A_1} into r (Fig. 11). The only difference is the reversed polarity of the voltage spikes: the D_{A_1} are in the opposite direction as compared to the D_{F_i}.

The further shape of u_{T_2} can be explained as for u_{T_1} for Figs. 1, 2, 9, and 10. The reduced steepness of u_{T_2} in $[t_d, t_e]$ compared to the time interval before t_d compares with the effects explained for interval $[t_u, t_\gamma]$ in Fig. 2. In t_e, $i_{D_{A_2}}$ becomes zero, the sudden reverse current termination, resulting in a sudden voltage drop across the snubber resistor previously described for D_{A_1} (time t_γ in Figs. 2, 10). The voltage in point 5 has become $U_{C_{R_2}} \approx -600$ V with respect to point 6. This is because C_{A_2} is part of a ringing circuit (U_Z, C_{A_2}, D_{A_2}, L_{E_2}, L_{E_1}, and T_1) and is charged above $U_Z = 440$ V. When u_{T_2} reaches 600 V, D_{L_2} starts to conduct and a ringing circuit $U_Z - C_{L_2} - D_{L_2} - L_{E_2} - L_{E_1} - T_1$ is formed. There, $U_{C_{L_2}}$ is held approximately constant ($\approx U_{C_{R_2}} \approx 600$ V). This means that u across L_{E_1}, L_{E_2} is held to about $U_{C_{R_2}} - U_Z \approx 160$ V; superimposed are oscillations due to stray inductances and local snubbers. In $[t_e, t_f]$, i_{L_2} in D_{L_2} oscillates via C_{L_2}, C_{R_2} and the stray inductance of the lead wire between these two capacitances.

i_{L_ϵ} has to be determined in practice; if $|i_L| < i_{L_\epsilon}$ is measured, the alternative operation of the two transistors is performed; if $|i_L| \geq i_{L_\epsilon}$, only that one of the two transistors is operated which will carry the load current. For $|i_L| < i_{L_\epsilon}$, this recharging of the snubber capacitors C_{A_i} is performed via the opposite transistor. For $|i_L| \geq i_{L_\epsilon}$, recharging of C_{A_i} is performed after turning off T_i. For small $|i_L|$, this time interval for the latter approach would either be too long, or charging up to $u_{C_{A_i}} \geq U_Z$, might not be possible at all, then the alternative operation with recharging via the opposite transistor takes place. One sees that dimensioning of the circuit requires determining that i_{L_ϵ}

where recharging of the C_{A_i} to a voltage $\geq U_Z$ can be guaranteed (see Section III-B).

For Fig. 6 only the recharging path shown in Fig. 13 is valid because $i_L = 0$ for Fig. 6. However, oscillations via C_{L_2}, L_{E_1}, and L_{E_2} still take place. Fig. 14 is used to explain Fig. 7 in more detail: for $t < t_q$, the load current is assumed to flow only through D_{F_2}, caused by a previous turn-off of T_1. In t_q, T_1 is turned on again, resulting in a current commutation from D_{F_2}, L_{E_2} into T_1, L_{E_1}. Again, the three different rates of rise in i_{L_1} can be observed. In t_r, i_{L_1} is assumed to have reached i_L; $-i_{D_{F_2}} = i_{L_2}$ becomes zero. Then, in $[t_r, t_s]$, the reverse recovery current of D_{F_2} can be observed. In t_x, when the reverse current flow in D_{F_2} starts to decline sharply, D_{A_2} and D_{L_2} start to conduct.

In $[t_x, t_y]$ oscillations in u_{T_2} can be observed as already explained for Fig. 2 for the interval $[t_\gamma, t_\delta]$ for u_{T_1}. The same is true for the oscillations for $t > t_y$ in Fig. 7, which have been explained for Fig. 2 for the interval $[t_\delta, t_n]$ for u_{T_1}. Because C_{A_2} has been previously charged to $u_{C_{A_2}} = U_{C_{R_2}}$ and D_{A_2} blocks this voltage, u_{T_2} is determined only by the turn-off behavior of D_{F_2} and by the local snubbers D_{F_2}, D_{L_2}, and D_{A_2}. This explains the fast rise of u_{T_2} before t_x. This is the same as following t_n in Fig. 2, but in Figs. 5 and 6 a much lower rate of rise of u_{T_2} is observed because there the shape of u_{T_2} is determined by C_{A_2}, L_{E_1}, and L_{E_2}.

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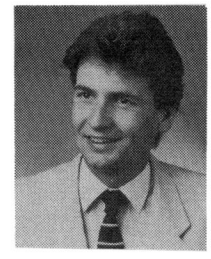

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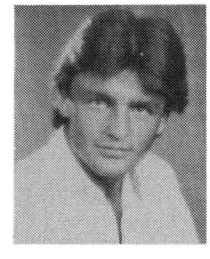
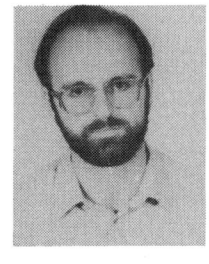


Johann W. Kolar was born in Upper Austria on July 15, 1959. He graduated from technical high school in Salzburg in 1978 and is currently finishing the M.Sc. degree in the Power Electronics Section of the Vienna University of Technology, Vienna, Austria.

He now works in the Power Electronics Section in the area of inverter development.



Franz J. Haselsteiner was born in Lower Austria on April 28, 1957. He graduated from technical high school in Waidhofen/Ybbs, Lower Austria, in 1977. He received the M.Sc. degree from the Vienna University of Technology, Vienna, Austria, in 1985.

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